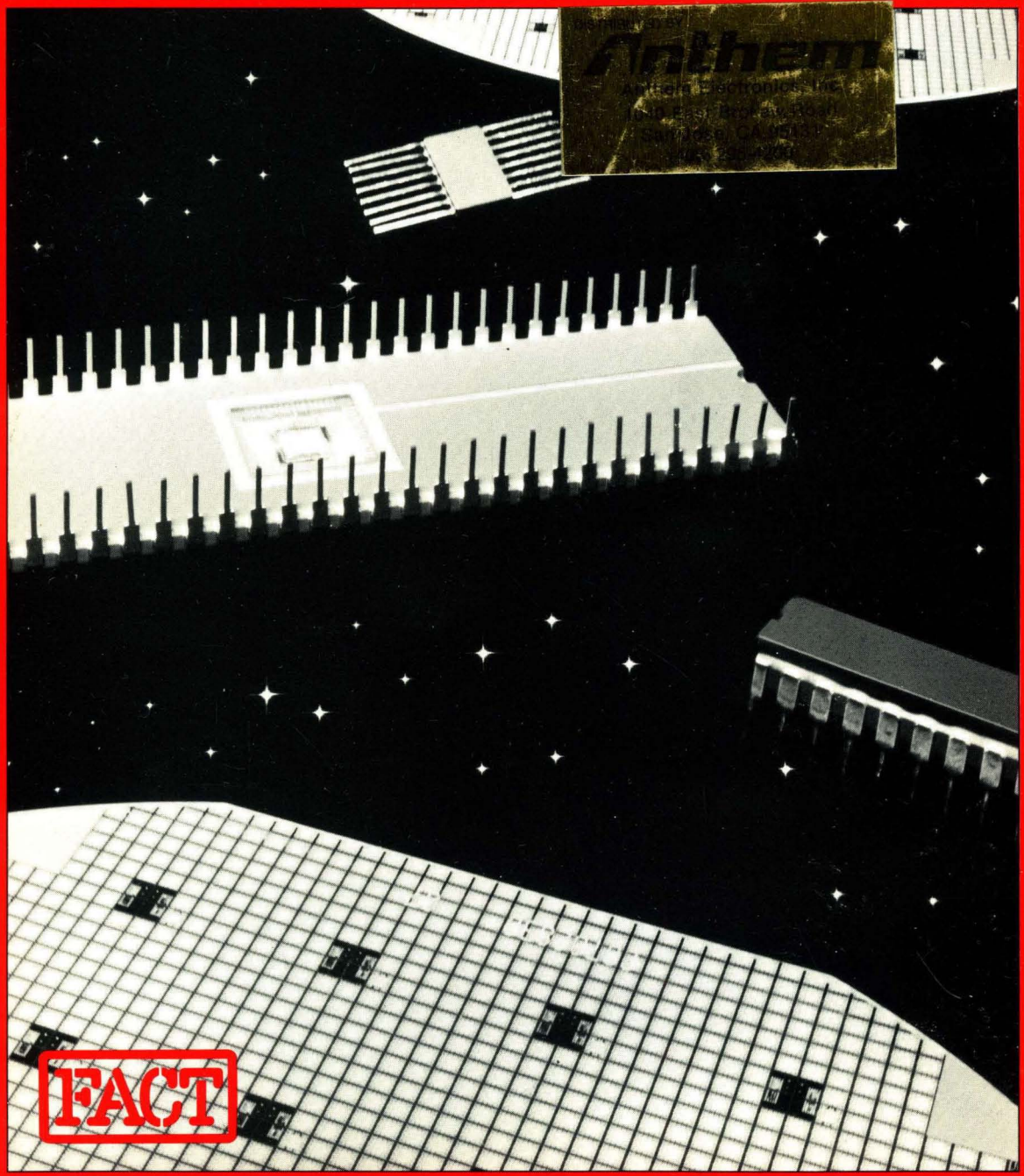
FAIRCHILD

Fairchild Advanced CMOS Technology

Logic Data Book



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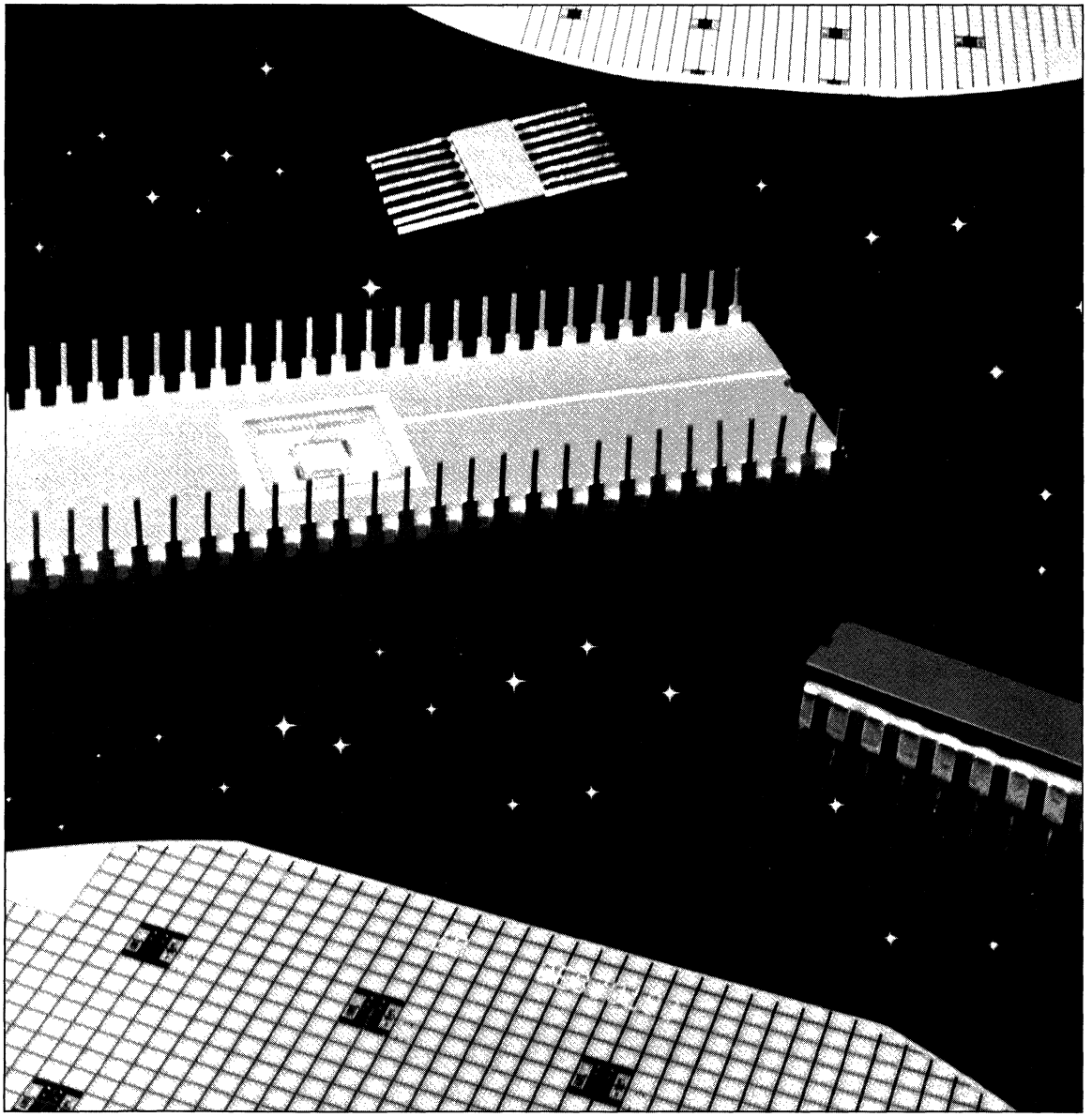

FACT

Digital and Analog Unit
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Introduction

This data book presents advanced information on Fairchild's very high-speed, low-power CMOS logic family, fabricated with Fairchild's state-of-the-art CMOS process.

FACT (Fairchild Advanced CMOS Technology) utilizes Fairchild's 1.3 μm Isoplanar silicon gate CMOS process to attain speeds similar to that of Advanced Low Power Schottky while retaining the advantages of CMOS logic, namely, ultra low power and high noise immunity. As an added benefit, FACT offers the system designer superior line driving characteristics and excellent ESD and latch-up immunity.

The FACT family consists of devices in two categories:

1. **AC,** standard logic functions with CMOS compatible inputs and TTL and MOS compatible outputs;
2. **ACT,** standard logic functions with TTL compatible inputs and TTL and MOS compatible outputs.

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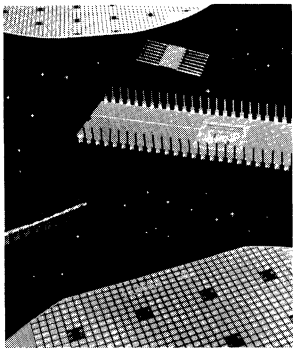

Literature Classification

PRELIMINARY

Preliminary: This product is in sampling or preproduction stage. This document contains advanced information and specifications that are subject to change without notice. Fairchild reserves the right to make changes at any time in order to improve design and provide the best product possible.

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Product Index and Selection Guide

Product Index

'ACXX Devices — CMOS Input Levels

Selection Guide

Gates

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NAND		
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Function	Device	Clock Inputs	Page No.
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Function	Device	3-State Outputs	Master Reset	Page No.
Dual D	54AC/74AC74	No	Yes	5-22
Dual D	54ACT/74ACT74	No	Yes	5-22
Dual J$\overline{K}$	54AC/74AC109	No	Yes	5-29
Dual J$\overline{K}$	54ACT/74ACT109	No	Yes	5-29
Quad D	54AC/74AC175	No	Yes	5-89
Quad D	54ACT/74ACT175	No	Yes	5-89
Quad D	54AC/74AC379	No	No	5-185
Quad D	54ACT/74ACT379	No	No	5-185
Hex D	54AC/74AC174	No	Yes	5-85
Hex D	54ACT/74ACT174	No	Yes	5-85
Hex D	54AC/74AC378	No	No	5-180
Hex D	54ACT/74ACT378	No	No	5-180
Octal D	54AC/74AC273	No	Yes	5-137
Octal D	54ACT/74ACT273	No	Yes	5-137
Octal D	54AC/74AC374	Yes	No	5-170
Octal D	54ACT/74ACT374	Yes	No	5-170
Octal D	54AC/74AC377	No	No	5-175
Octal D	54ACT/74ACT377	No	No	5-175
Octal D	54AC/74AC534	Yes	No	5-233
Octal D	54ACT/74ACT534	Yes	No	5-233
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Function	Device	3-State Outputs	Broadside Pinout	Page No.
Octal	54AC/74AC373	Yes	No	5-165
Octal	54ACT/74ACT373	Yes	No	5-165
Octal D	54AC/74AC563	Yes	Yes	5-241
Octal D	54ACT/74ACT563	Yes	Yes	5-241
Octal D	54AC/74AC573	Yes	Yes	5-260
Octal D	54ACT/74ACT573	Yes	Yes	5-260
Octal Transparent	54AC/74AC533	Yes	No	5-228
Octal Transparent	54ACT/74ACT533	Yes	No	5-228
Octal Transparent	54AC/74AC845	Yes	Yes	5-385
Octal Transparent	54ACT/74ACT845	Yes	Yes	5-385
Octal Transparent	54AC/74AC846	Yes	Yes	5-385
Octal Transparent	54ACT/74ACT846	Yes	Yes	5-385
9-Bit Transparent	54AC/74AC843	Yes	Yes	5-378
9-Bit Transparent	54ACT/74ACT843	Yes	Yes	5-378
9-Bit Transparent	54AC/74AC844	Yes	Yes	5-378
9-Bit Transparent	54ACT/74ACT844	Yes	Yes	5-378
10-Bit Transparent	54AC/74AC841	Yes	Yes	5-373
10-Bit Transparent	54ACT/74ACT841	Yes	Yes	5-373
10-Bit Transparent	54AC/74AC842	Yes	Yes	5-373
10-Bit Transparent	54ACT/74ACT842	Yes	Yes	5-373

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Function	Device	Parallel Entry	Reset	U/D	3-State Outputs	Page No.
BCD Decade	54AC/74AC160	S	A	No	No	5-59
BCD Decade	54ACT/74ACT160	S	A	No	No	5-59
BCD Decade	54AC/74AC162	S	S	No	No	5-59
BCD Decade	54ACT/74ACT162	S	S	No	No	5-59
4-Bit Decade	54AC/74AC190	A	—	Yes	No	5-94
4-Bit Decade	54AC/74AC192	A	A	Yes	No	5-102
4-Bit Decade	54AC/74AC568	S	S/A	Yes	Yes	5-251
4-Bit Binary	54AC/74AC161	S	A	No	No	5-66
4-Bit Binary	54ACT/74ACT161	S	A	No	No	5-66
4-Bit Binary	54AC/74AC163	S	S	No	No	5-66
4-Bit Binary	54ACT/74ACT163	S	S	No	No	5-66
4-Bit Binary	54AC/74AC168	S	—	Yes	No	5-77
4-Bit Binary	54AC/74AC169	S	—	Yes	No	5-77
4-Bit Binary	54AC/74AC191	A	—	Yes	No	5-94
4-Bit Binary	54AC/74AC193	A	A	Yes	No	5-102
4-Bit Binary	54AC/74AC569	S	S/A	No	Yes	5-251

S = Synchronous
A = Asynchronous

Buffers/Line Drivers

Function	Device	Enable Inputs (Level)	Inverting/ Non-Inverting	Broadside Pinout	Page No.
Octal	54AC/74AC240	2(L)	I	No	5-109
Octal	54ACT/74ACT240	2(L)	I	No	5-109
Octal	54AC/74AC241	1(H) & 1(L)	N	No	5-112
Octal	54ACT/74ACT241	1(H) & 1(L)	N	No	5-112
Octal	54AC/74AC244	2(L)	N	No	5-115
Octal	54ACT/74ACT244	2(L)	N	No	5-115
Octal	54AC/74AC540	2(L)	I	Yes	5-238
Octal	54ACT/74ACT540	2(L)	I	Yes	5-238
Octal	54AC/74AC541	1(H) & 1(L)	N	Yes	5-238
Octal	54ACT/74ACT541	1(H) & 1(L)	N	Yes	5-238

L = LOW H = HIGH

FIFOs

Function	Device	Input	Output	3-State Outputs	Page No.
64 x 9 FIFO Memory	54AC/74AC708	Parallel	Parallel	Yes	5-296
64 x 9 FIFO Memory	54ACT/74ACT708	Parallel	Parallel	Yes	5-296
64 x 9 FIFO	54AC/74AC723	Parallel	Parallel	Yes	5-314
64 x 9 FIFO	54ACT/74ACT723	Parallel	Parallel	Yes	5-314
512 x 9 FIFO	54AC/74AC725	Parallel	Parallel	Yes	5-330
512 x 9 FIFO	54ACT/74ACT725	Parallel	Parallel	Yes	5-330

Decoders/Demultiplexers

Function	Device	LOW Enable	Active-HIGH Enable	Active-LOW Outputs	Active-Address Inputs	Page No.
1-of-8	54AC/74AC138	2	1	8	3	5-34
1-of-8	54ACT/74ACT138	2	1	8	3	5-34
Dual 1-of-4	54AC/74AC139	1 & 1	No	4 & 4	2 & 2	5-39
Dual 1-of-4	54ACT/74ACT139	1 & 1	No	4 & 4	2 & 2	5-39

Arithmetic Functions

Function	Device	Features	Page No.
16 x 16 Multiplier/Accumulator	54AC/74AC1010	2s Complement & Unsigned Arithmetic	5-392
16 x 16 Multiplier/Accumulator	54ACT/74ACT1010	2s Complement & Unsigned Arithmetic	5-392
16 x 16 Multiplier	54AC/74AC1016	2s Complement & Unsigned Arithmetic	5-402
16 x 16 Multiplier	54ACT/74ACT1016	2s Complement & Unsigned Arithmetic	5-402
16 x 16 Multiplier	54AC/74AC1017	Common Clock	5-413
16 x 16 Multiplier	54ACT/74ACT1017	Common Clock	5-413
Arithmetic Logic Unit for DSP	54AC/74AC705	16-Bit ALU and 8 x 8 Parallel Multiplier/ Accumulator	5-284
Arithmetic Logic Unit for DSP	54ACT/74ACT705	16-Bit ALU and 8 x 8 Parallel Multiplier/ Accumulator	5-284

Shift Registers

Function	Device	No. of Bits	Reset	Serial Inputs	3-State Outputs	Page No.
Octal Shift/Storage	54AC/74AC299	8	A	2	Yes	5-142
Octal Shift/Storage	54ACT/74ACT299	8	A	2	Yes	5-142
Octal Shift/Storage	54AC/74AC323	8	S	2	Yes	5-149
Octal Shift/Storage	54ACT/74ACT323	8	S	2	Yes	5-149

A = Asynchronous S = Synchronous

Multiplexers

Function	Device	Enable Inputs (Level)	True Output	Complement Output	Page No.
8-Input	54AC/74AC151	1(L)	Yes	Yes	5-43
8-Input	54ACT/74ACT151	1(L)	Yes	Yes	5-43
8-Input	54AC/74AC251	1(L)	Yes	Yes	5-121
8-Input	54ACT/74ACT251	1(L)	Yes	Yes	5-121
Dual 4-Input	54AC/74AC153	2(L)	Yes	No	5-47
Dual 4-Input	54ACT/74ACT153	2(L)	Yes	No	5-47
Dual 4-Input	54AC/74AC253	2(L)	Yes	No	5-125
Dual 4-Input	54ACT/74ACT253	2(L)	Yes	No	5-125
Dual 4-Input	54AC/74AC352	2(L)	No	Yes	5-156
Dual 4-Input	54ACT/74ACT352	2(L)	No	Yes	5-156
Dual 4-Input	54AC/74AC353	2(L)	No	Yes	5-161
Dual 4-Input	54ACT/74ACT353	2(L)	No	Yes	5-161
Quad 2-Input	54AC/74AC157	1(L)	Yes	No	5-51
Quad 2-Input	54ACT/74ACT157	1(L)	Yes	No	5-51
Quad 2-Input	54AC/74AC158	1(L)	No	Yes	5-55
Quad 2-Input	54ACT/74ACT158	1(L)	No	Yes	5-55
Quad 2-Input	54AC/74AC257	1(L)	Yes	No	5-129
Quad 2-Input	54ACT/74ACT257	1(L)	Yes	No	5-129
Quad 2-Input	54AC/74AC258	1(L)	No	Yes	5-133
Quad 2-Input	54ACT/74ACT258	1(L)	No	Yes	5-133

Comparators

Function	Device	Features	Page No.
Octal Identity Comparator	54AC/74AC520	Expandable	5-223
Octal Identity Comparator	54ACT/74ACT520	Expandable	5-223
Octal Identity Comparator	54AC/74AC521	Expandable	5-223
Octal Identity Comparator	54ACT/74ACT521	Expandable	5-223

Transceivers/Registered Transceivers

Function	Device	Registered	Enable Inputs (Level)	3-State Output	Page No.
Octal Bidirectional Transceiver	54AC/74AC245	No	1(L)	Yes	5-118
Octal Bidirectional Transceiver	54ACT/74ACT245	No	1(L)	Yes	5-118
Octal Bus Transceiver & Register	54AC/74AC646	Yes	1(L) & 1(H)	Yes	5-276
Octal Bus Transceiver & Register	54AC/74AC648	Yes	1(L) & 1(H)	Yes	5-280
Octal Bidirectional Transceiver	54AC/74AC640	No	1(L)	Yes	5-270
Octal Bidirectional Transceiver	54ACT/74ACT640	No	1(L)	Yes	5-270
Octal Bidirectional Transceiver	54AC/74AC643	No	1(L)	Yes	5-273
Octal Bidirectional Transceiver	54ACT/74ACT643	No	1(L)	Yes	5-273

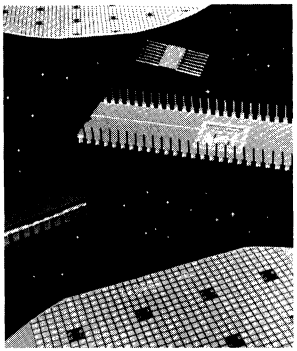
FGC Series—Sub 2μ Silicon Gate CMOS

Product	Gate Equiv.	I/O Levels	Typical Internal Gate Delay (ns)	Typical Buffer Delay[1]		Power (W)	Max I/O	Packaging[2]
				Input (ns)	Output (ns)			
FGC0500	540	TTL/CMOS	1.1	2.1	2.3	*	40	20, 24, 28, 40 PDIP 20, 24, 28, 40 CDIP 44 PLCC 44 CLCC
FGC1200	1188	TTL/CMOS	1.1	2.0	3.8	*	73	24, 28, 40, 48 PDIP 24, 28, 40, 48 CDIP 44, 68 PLCC 44, 68, 84 CLCC 68, 84 PPGA 68, 84 CPGA
FGC2400	2625	TTL/CMOS	1.1	2.0	3.8	*	105	24, 28, 40, 48, 64 PDIP 24, 28, 40, 48, 64 CDIP 44, 68, 84 PLCC 44, 68, 84 CLCC 68, 84, 120 PPGA 68, 84, 120 CPGA
FGC4000	3960	TTL/CMOS	1.1	2.0	3.8	*	133	40, 48 PDIP 40, 48 CDIP 44, 68, 84 PLCC 44, 68, 84 CLCC 68, 84, 120, 144 PPGA 68, 84, 120, 144 CPGA 132 CFPAK
FGC6000	6000	TTL/CMOS	1.1	2.0	3.8	*	158	68, 84 PLCC 68, 84 CLCC 84, 120, 144 PPGA 84, 120, 144, 180 CPGA 132 CFPAK
FGC8000	7896	TTL/CMOS	1.1	2.0	3.8	*	181	84 PLCC 84 CLCC 144 PPGA 144, 180, 209 CPGA

[1]FGC series input buffer delays for CMOS input with fanout = 2 and statistical wirelength. FGC series output buffer delay for CL = 15 pF.

[2]PDIP = Plastic Dual In-Line, CDIP = Ceramic Dual In-Line Side Brazed, PLCC = Plastic Leaded Chip Carrier (J-Bend Leads), CLCC = Ceramic Leaded Chip Carrier (J-Bend Leads), CPGA = Ceramic Pin Grid Array, PPGA = Plastic Pin Grid Array, CFPAK = Ceramic Flatpak. Consult local sales office for package availability.

*Power dissipation for CMOS arrays is design/array dependent with worst case ranging from 0.25-1.0 W.



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FACT Descriptions and Family Characteristics

Fairchild Advanced CMOS Technology — FACT — Logic

Fairchild Digital introduced FACT (Fairchild Advanced CMOS Technology) logic, a family of high-speed advanced CMOS circuits, in 1985.

FACT logic offers a unique combination of high speed, low power dissipation, high noise immunity, wide fanout capability, extended power supply range and high reliability.

This data book describes the product line with device specifications as well as material discussing design considerations and comparing the FACT family to predecessor technologies.

The 1.3-micron silicon gate CMOS process utilized in this family has been proven in the field of high performance gate arrays, Fairchild's 32-Bit Microprocessor, CLIPPER, and FACT. It has been further enhanced to meet and exceed the JEDEC standards for 74ACXX logic.

For direct replacement of LS, ALS and other TTL devices, the 'ACT circuits with TTL-type input thresholds are included in the FACT family. These include the more popular bus drivers/transceivers as well as many other 54ACT/74ACTXXX devices.

Characteristics

- Full Logic Product Line
- Industry Standard Functions and Pinouts for SSI, MSI and LSI
- Meets or Exceeds JEDEC Standards for 74ACXX Family
- TTL Inputs on Selected Circuits
- High Performance Outputs
  - Common Output Structure for Standard and Buffer Drivers
  - Output Sink/Source Current of 24 mA
  - Transmission Line Driving 50 ohm (Commercial)/75 ohm (Military) Guaranteed
- Operation from 2 - 6 Volts Guaranteed
- Temperature Range -40°C to +85°C (Commercial), -55°C to +125°C (Military)
- Improved ESD Protection Network
- High Current Latch-Up Immunity

Interfacing

FACT devices have a wide operating voltage range (V_{CC} = 2 to 6 VDC) and sufficient current drive to interface with most other logic families available today.

Device designators are as follows:

'AC — This is a high-speed CMOS device with CMOS input switching levels and buffered CMOS outputs that can drive ± 24 mA of I_{OH} and I_{OL} current. Industry standard 'AC nomenclature and pinouts are used.

'ACT — This is a high-speed CMOS device with a TTL-to-CMOS input buffer stage. These device inputs are designed to interface with TTL outputs operating with a V_{CC} = 5 V ± 0.5 V with V_{OH} = 2.4 V and V_{OL} = 0.4 V, but are functional over the entire FACT operating voltage range of 2.0 to 5.5 VDC. These devices have buffered outputs that will drive CMOS or TTL devices with no additional interface circuitry. 'ACT devices have the same output structures as 'AC devices.

Low Power CMOS Operation

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, FACT draws three orders of magnitude less power than the equivalent LS or ALS TTL device. This enhances system reliability; because costly regulated high current power supplies, heat sinks and fans are eliminated, FACT logic devices are ideal for portable systems such as laptop computers and backpack communications systems. Operating power is also very low for FACT logic. Power consumption of various technologies with a clock frequency of 1 MHz is shown below.

FACT	= 0.1 mW/Gate
ALS	= 1.2 mW/Gate
LS	= 2.0 mW/Gate
HC	= 0.1 mW/Gate

Figure 2-1: Icc vs Vcc

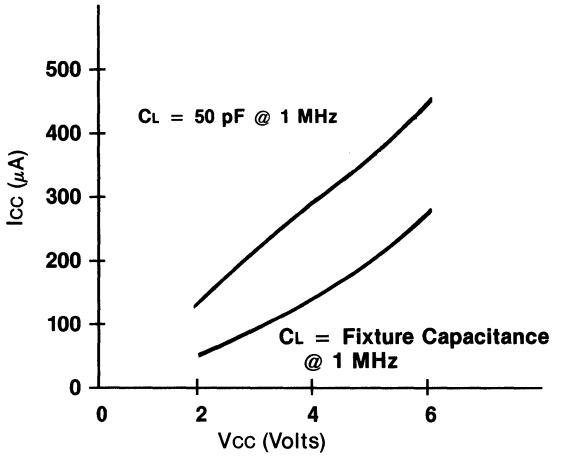


Figure 2-1 illustrates the effects of Icc versus power supply voltage (Vcc) for two load capacitance values: 50 pF and stray capacitance. The clock frequency was 1 MHz for the measurements.

AC Performance

In comparison to LS, ALS and HC families, FACT devices have faster internal gate delays as well as the basic gate delays. Additionally, as the level of integration increases, FACT logic leads the way to very high-speed systems.

The example below describes typical values for a 74XX138, 3-to-8 line decoder.

FACT	= 6.0 ns @ C_L = 50 pF
ALS	= 12.0 ns @ C_L = 50 pF
LS	= 22.0 ns @ C_L = 15 pF
HC	= 17.5 ns @ C_L = 50 pF

AC performance specifications are guaranteed at 5.0 V ± 0.5 V and 3.3 V ± 0.3 V. For worst case design at 2.0 V Vcc on all device types, the formula below can be used to determine AC performance.

AC performance at 2.0 V Vcc = 1.9 × AC specification at 3.3 V.

Multiple Output Switching

Propagation delay is affected by the number of outputs switching simultaneously. Typically, devices with more than one output will follow the rule: for each output switching, derate the databook specification by 250 ps. This effect typically is not significant on an octal device unless more than four outputs are switching simultaneously. This derating is valid for the entire temperature range and 5.0 V ± 10% Vcc.

Noise Immunity

The noise immunity of a logic family is also an important equipment cost factor in terms of decoupling components, power supply dynamic resistance and regulation as well as layout rules for PC boards and signal cables.

The comparisons shown describe the difference between the input threshold of a device and the output voltage, $|V_{IL} - V_{OL}| / |V_{IH} - V_{OH}|$ at 4.5 V Vcc.

FACT	= 1.25/1.25 V
ALS	= 0.4/0.7 V
LS	= 0.3/0.7 V @ 4.75 V Vcc
HC	= 0.8/1.25 V

Output Characteristics

All FACT outputs are buffered to ensure consistent output voltage and current specifications across the family. Both 'AC and 'ACT device types have the same output structures. Two clamp diodes are internally connected to the output pin to suppress voltage overshoot and undershoot in noisy system applications which can result from impedance mismatching. The balanced output design allows for controlled edge rates and equal rise and fall times.

All devices ('AC or 'ACT) are guaranteed to source and sink 24 mA. Commercial devices, 74AC/ACTXXX, are capable of driving 50 ohm transmission lines, while military grade devices, 54AC/ACTXXX, can drive 75 ohm transmission lines.

IOL/IOH Characteristics

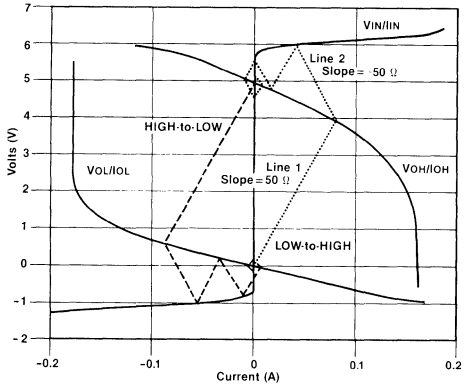
FACT	= 24/-24 mA
ALS	= 24/-15 mA
LS	= 8/-0.4 mA @ 4.75 V Vcc
HC	= 4/-4 mA

Dynamic Output Drive

Traditionally, in order to predict what incident wave voltages would occur in a system, the designer was required to do an output analysis using a Bergeron diagram. Not only is this a long and time consuming operation, but the designer needed to depend upon the accuracy and reliability of the manufacturer-supplied 'typical' output I/V curve. Additionally, there was no way to guarantee that any supplied device would meet these 'typical' performance values across the operating voltage and temperature limits. Fortunately for the system designers, Fairchild has taken the necessary steps to guarantee incident wave switching on transmission lines with impedances as low as 50 ohms for the commercial temperature range and 75 ohms for the military temperature range.

Figure 2-2 shows a Bergeron diagram for switching both HIGH-to-LOW and LOW-to-HIGH. On the right side of the graph ($I_{out} > 0$), are the V_{OH} and I_{IH} curves for FACT logic while on the left side ($I_{out} < 0$), are the curves for V_{OL} and I_{IL}. Although we will only discuss here the LOW-to-HIGH transition, the information presented may be applied to a HIGH-to-LOW transition.

Figure 2-2: Gate Driving 50 Ohm Line Reflection Diagram



Begin analysis at the V_{OL} (quiescent) point. This is the intersection of the V_{OL}/I_{OL} curve for the output and the V_{IN}/I_{IN} curve for the input. For CMOS inputs and outputs, this point will be approximately 100 mV. Then draw a 50 ohm load line from this intersection to the V_{OH}/I_{OH} curve as shown by Line 1. This intersection is the voltage that the incident wave will have. Here it occurs at approximately 3.95 V. Then draw a line with a slope of -50 ohms from this first intersection point to the V_{IN}/I_{IN} curve as shown by Line 2. This second intersection will be the first reflection back from the input gate. Continue this process of drawing the load lines from each intersection to the next. Lines terminating on the V_{OH}/I_{OH} curve should have positive slopes while lines terminating on the V_{IN}/I_{IN} curve should have negative slopes.

Each intersection point predicts the voltage of each reflected wave on the transmission line. Intersection points on the V_{OH}/I_{OH} curve will be waves travelling from the driver to the receiver while intersection points on the V_{IN}/I_{IN} curve will be waves travelling from the receiver to the driver.

Figures 2-3a and 2-3b show the resultant waveforms. Each division on the time scale represents the propagation delay of the transmission line.

Figure 2-3a: Resultant Waveforms Driving 50 Ohm Line — Theoretical

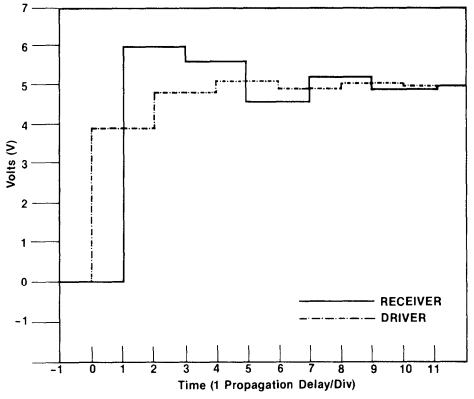


Figure 2-3a: Resultant Waveforms Driving 50 Ohm Line — Actual

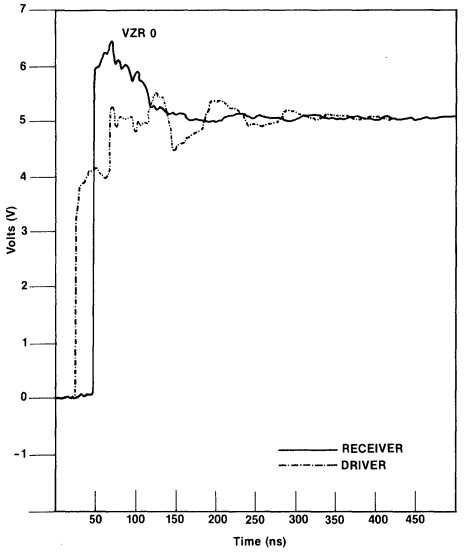


Figure 2-3b: Resultant Waveforms Driving 50 Ohm Line — Actual

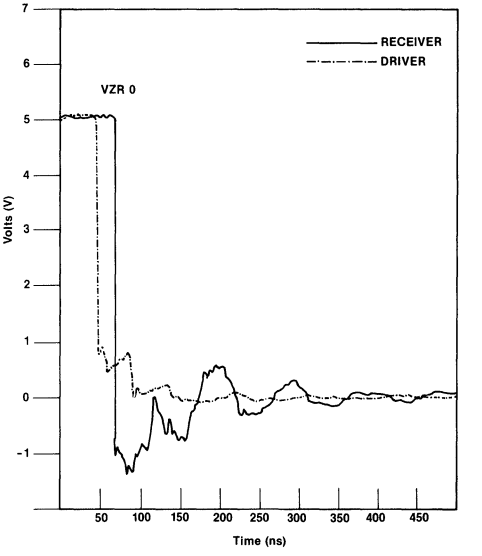
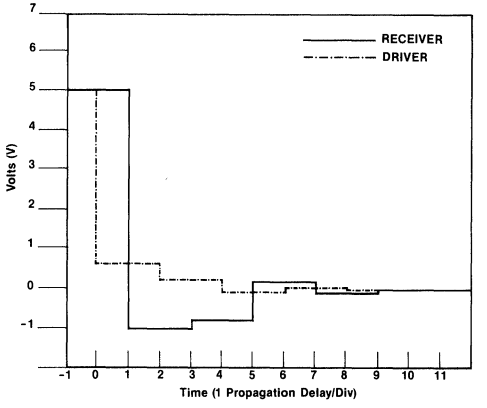


Figure 2-3b: Resultant Waveforms Driving 50 Ohm Line — Theoretical



While this exercise can be done for FACT, it is no longer necessary. FACT is guaranteed to drive an incident wave of enough voltage to switch another FACT input.

We can calculate what current is required by looking at the Bergeron diagram. The quiescent voltage on the line will be within 100 mV of either rail. We know what voltage is required to guarantee a valid voltage at the receiver. This is either 70% or 30% of V_{CC}. The formula for calculating the current and voltage required is $|(V_{OQ} - V_I)/Z_O|$ at V_I. For V_{OQ} = 100 mV, V_{IH} = 3.85 V, V_{CC} = 5.5 V and Z_O = 50 ohms, the required I_{OH} at 3.85 V is 75 mA. For the HIGH-to-LOW transition, V_{OQ} = 5.4 V, V_{IL} = 1.35 V and Z_O = 50 ohms, I_{OL} is 75 mA at 1.65 V. FACT's I/O specifications include these limits. For transmission lines with impedances greater than 50 ohms, the current requirements are less and switching is still guaranteed.

It is important to note that the typical 24 mA drive specification is not adequate to guarantee incident wave switching. The only way to guarantee this is to guarantee the current required to switch a transmission line from the output quiescent point to the valid V_{IN} level.

The following performance charts are provided in order to aid the designer in determining dynamic output current drive of FACT devices with various power supply voltages.

Figure 2-4: Output Characteristics V_{OH}/I_{OH}, 'AC00

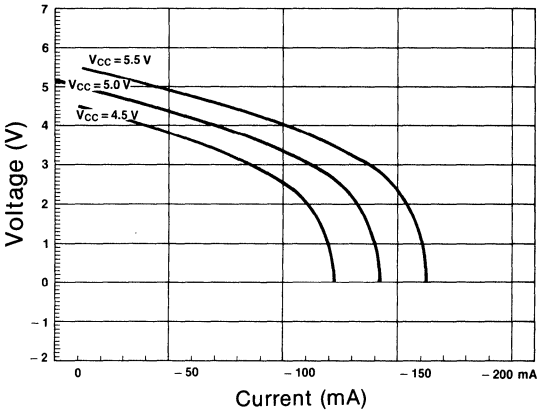


Figure 2-5: Output Characteristics V_{OL}/I_{OL}, 'AC00

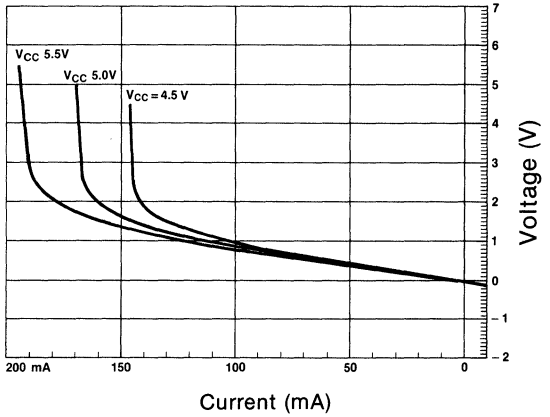
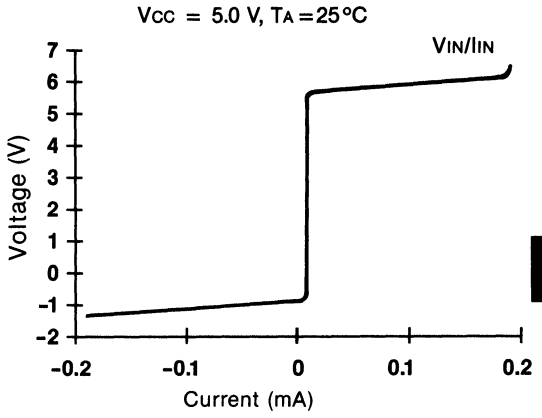


Figure 2-6: Input Characteristics V_{IN}/I_{IN}



2

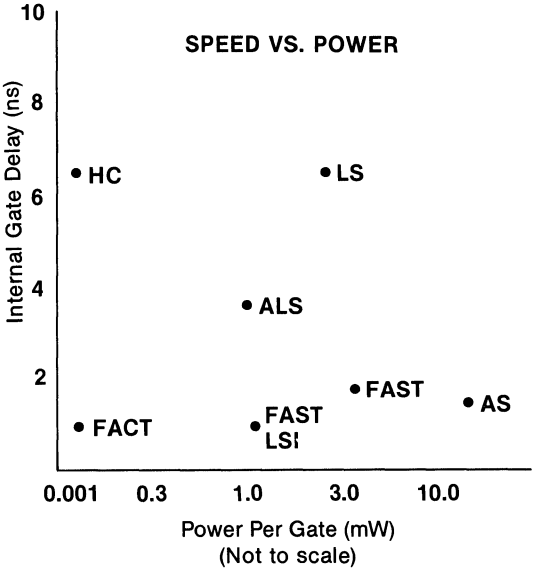
Choice of Voltage Specifications

To obtain better performance and higher density, semiconductor technologies are reducing the vertical and horizontal dimensions of integrated device structures. Due to a number of electrical limitations in the manufacture of VLSI devices and the need for low voltage operation in memory cards, it was decided by the JEDEC committee to establish interface standards for devices operating at 3.3 V ± 0.3 V. To this end, Fairchild Digital guarantees all of its devices operational at 3.3 V ± 0.3 V. Note also that AC and DC specifications are guaranteed between 3.0 and 5.5 V. Operation of FACT logic is also guaranteed from 2.0 to 6.0 V on V_{CC}.

Operating Voltage Ranges

FACT	=	2.0 to 6.0 V
ALS	=	5.0 V ± 10%
LS	=	5.0 V ± 5%
HC	=	2.0 to 6.0 V

Figure 2-7: Internal Gate Delays



FACT Replaces LS, ALS, HCMOS

Fairchild's Advanced CMOS family is specifically designed to outperform the LS, ALS and HCMOS families. Figure 2-7 shows the relative position of various logic families in speed/power performance. FACT exhibits 1 ns internal propagation delays while consuming 1 μW of power.

The Logic Family Comparisons table below summarizes the key performance specifications for various competitive technology logic families.

Figure 2-8: Logic Family Comparisons
General Characteristics (All Max Ratings)

Characteristics	Symbol	LS	ALS	HCMOS	FACT		Unit
					'AC	'ACT	
Operating Voltage Range	$V_{CC/EE/DD}$	5±5%	5±10%	2.0 to 6.0	2.0 to 6.0	2.0 to 6.0	V
Operating Temperature Range	T_A 74 Series T_A 54 Series	0 to +70 -55 to +125	0 to +70 -55 to +125	-40 to +85 -55 to +125	-40 to +85 -55 to +125	-40 to +85 -55 to +125	°C
Input Voltage (limits)	V_{IH} (min)	2.0	2.0	3.15	3.15	2.0	V
	V_{IL} (max)	0.8	0.8	0.9	1.35	0.8	V
Output Voltage (limits)	V_{OH} (min)	2.7	2.7	V_{CC}-0.1	V_{CC}-0.1	V_{CC}-0.1	V
	V_{OL} (max)	0.5	0.5	0.1	0.1	0.1	V
Input Current	I_{IH}	20	20	+1.0	+1.0	+1.0	μA
	I_{IL}	-400	-200	-1.0	-1.0	-1.0	μA
Output Current at V_O (limit)	I_{OH}	-0.4	-0.4	-4.0@V_{CC}-0.8	-24@V_{CC}-0.8	-24@V_{CC}-0.8	mA
	I_{OL}	8.0	8.0	4.0 @0.4 V	24 @0.4 V	24 @ 0.4 V	mA
DC Noise Margin LOW/HIGH	DCM	0.3/0.7	0.4/0.7	0.8/1.25	1.25/1.25	0.7/2.4	V

Note: All DC parameters are specified over the commercial temperature range.

Figure 2-8: Logic Family Comparisons, cont'd.

Speed/Power Characteristics (All Typical Ratings)

Characteristics	Symbol	LS	ALS	HCMOS	FACT	Unit
Quiescent Supply Current/Gate	I_G	0.4	0.2	0.0005	0.0005	mA
Power/Gate (Quiescent)	P_G	2.0	1.2	0.0025	0.0025	mW
Propagation Delay	t_P	7.0	5.0	8.0	5.0	ns
Speed Power Product	—	14	6.0	0.02	0.01	pJ
Clock Frequency D/FF	f_{max}	33	50	50	160	MHz

Propagation Delay (Commercial Temperature Range)

	Product		LS	ALS	HCMOS	FACT	Unit
t_{PLH}/t_{PHL}	74XX00	Typ	10.0	5.0	8.0	5.0	ns
		Max	15.0	11.0	23.0	8.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX74	Typ	25.0	12.0	23.0	8.0	ns
		Max	40.0	18.0	44.0	10.5	ns
t_{PLH}/t_{PHL} (Clock to Q)	74XX163	Typ	18.0	10.0	20.0	5.0	ns
		Max	27.0	17.0	52.0	10.0	ns

Conditions: (LS) $V_{CC} = 5.0$ V, $C_L = 15$ pF, 25°C;
(ALS/HC/FACT) $V_{CC} = 5.0$ V ± 10%, $C_L = 50$ pF, Typ values at 25°C, Max values at 0 to 70°C for ALS, -40 to +85°C for HC/FACT.

Circuit Characteristics

Power Dissipation

One advantage to using CMOS logic is its extremely low power consumption. During quiescent conditions, FACT will consume several orders of magnitude less current than its bipolar counterparts. But DC power consumption is not the whole picture. Any circuit will have AC power consumption, whether it is built with CMOS or bipolar technologies.

Power consumption of a circuit can be calculated using the formula:

$$PD = [(C_L + C_{PD}) \bullet V_{CC} \bullet V_S \bullet f] + [I_Q \bullet V_{CC}]$$

where

- PD = power dissipation
- C_L = load capacitance
- C_{PD} = device power capacitance
- V_{CC} = power supply
- V_S = output voltage swing
- f = frequency of operation
- I_Q = quiescent current

Power consumption for FACT is dependent on the supply voltage, frequency of operation, internal capacitance and load. V_S will be V_{CC} and I_Q can be considered negligible for CMOS. Therefore, the simplified formula for CMOS is:

$$PD = (C_L + C_{PD})\, V_{CC}^2\, f$$

C_{PD} values for CMOS devices are calculated by measuring the power consumption of a device at two different frequencies. C_{PD} is calculated in the following manner:

1. The power supply voltage is set to V_{CC} = 5.5 VDC.
2. Signal inputs are set up so that as many outputs as possible are switching, giving a worst-case situation per JEDEC C_{PD} conditions (see Section 3).
3. The power supply current is measured and recorded at input frequencies of 200 kHz and 1 MHz.
4. The power dissipation capacitance is calculated by solving the two simultaneous equations

   $$P_1 = (C_{PD} \bullet V_{CC}^2 \bullet f_1) + (I_{CC} \bullet V_{CC})$$
   $$P_2 = (C_{PD} \bullet V_{CC}^2 \bullet f_2) + (I_{CC} \bullet V_{CC})$$

   giving

   $$C_{PD} = (P_1 - P_2)/V_{CC}^2(f_1 - f_2)$$

   or

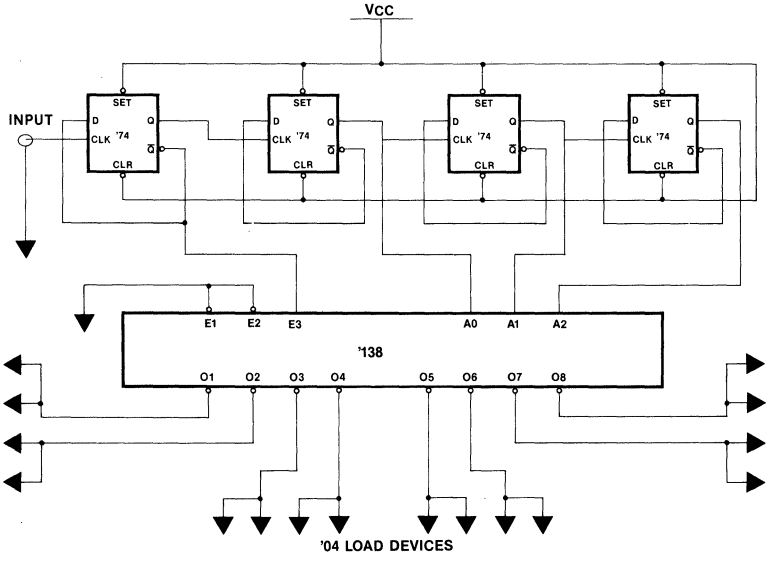
   $$C_{PD} = (I_1 - I_2)/V_{CC}(f_1 - f_2)$$

   where

   I_1 = supply current at f_1 = 200 kHz.
   I_2 = supply current at f_2 = 1 MHz.

On FACT device data sheets, C_{PD} is a typical value and is given either for the package or for the individual device (i.e., gates, flip-flops, etc.) within the package.

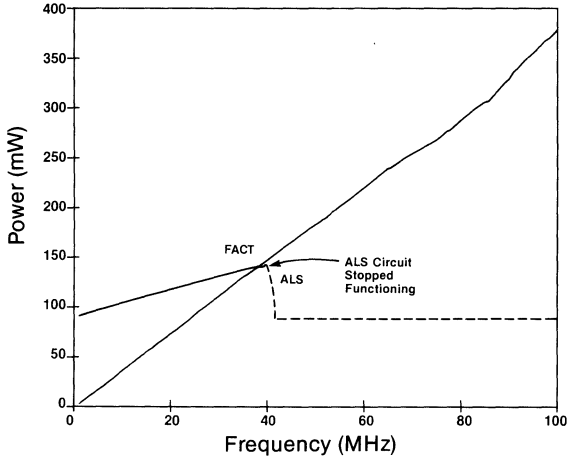
Figure 2-9: Power Demonstration Circuit Schematic



The circuit shown in Figure 2-9 was used to compare the power consumption of FACT versus ALS devices.

Two identical circuits were built on the same board and driven from the same input. In the circuit, the input signal was driven into four D-type flip-flops which act as divide-by-2 frequency dividers. The outputs from the flip-flops were connected to the inputs of a '138 decoder. This generated eight non-overlapping clock pulses on the outputs of the '138, which were then connected to an '04 inverter. The input frequency was then varied and the power consumption was measured. Figure 2-10 illustrates the results of these measurements.

Figure 2-10: FACT vs. ALS Circuit Power



Below 40 MHz, the FACT circuit dissipates much less power than the ALS version. It is interesting to note that when the frequency went to zero, the FACT circuit's power consumption also went to zero; the ALS circuit continued to dissipate almost 100 mW. Another advantage of FACT is its capabilities above 40 MHz. At this frequency, the first 74ALS74 D-type flip-flop ceased to operate. Once this occurred, the entire circuit stopped working and the power consumption fell to its quiescent value. The FACT device, however, continued functioning beyond the limit of the frequency generator, which was 100 MHz.

This graph shows two advantages of FACT circuits (power and speed). FACT logic delivers increased performance in addition to offering the power savings of CMOS.

Refer to Section 3 for test philosophies regarding power dissipation.

Specification Derivation

At first glance, the specifications for FACT logic might appear to be widely spread, possibly indicating wide design margins are required. However, several effects are reflected in each specification.

Figures 2-11a through 2-11e illustrate how the data from the characterization of actual devices is transformed into the specifications that appear on the data sheet. This data is taken from the 'AC245.

Figure 2-11a shows the data taken (from one part) on a typical, single path, t_{PHL} from A_n to B_n, over temperature at 5.0 V; there is negligible variation in the value of t_{PHL}. The next graph, Figure 2-11b, depicts data taken on the same device; this set of curves represents the data on all paths A to B and B to A. The data on this plot indicates only a small variation for t_{PHL}.

The graphs in Figures 2-11a and 2-11b include data at 5.0 V; Figure 2-11c shows the variation of delay times over the standard 5.0 ± 0.5 V voltage range. Note there is only a ± 6% variation in delay time due to voltage effects.

Now refer to Figure 2-11d which illustrates the process effects on delay time. This graph indicates that the process effects contribute to the spread in specifications more than any other factor in that the effects of the theoretical process spread can increase or decrease specification times by 30%. Because this 30% spread represents considerably more than ± 3 standard deviations, this guarantees an increase in the manufacturability and the quality level of FACT product. To further ensure parts within specification will pass on testers at the limits of calibration, tester guardbands are incorporated.

With voltage and process effects added (Figure 2-11e), the full range of the specification can be seen. For reference, the data sheet values are shown on the graph.

This linear behavior with temperature and voltage is typical of CMOS. Although the graphs are drawn for a specific device, other part types have very similar graphical representations. Therefore, for performance-critical applications, where not all variables need to be taken into account at once, the user can narrow the specifications. For example, all parts in a critically timed subcircuit are together on a board, so it may be assumed the devices are at the same supply and temperature.

Figure 2-11a: t_{PHL}, An to Bn, Single Path

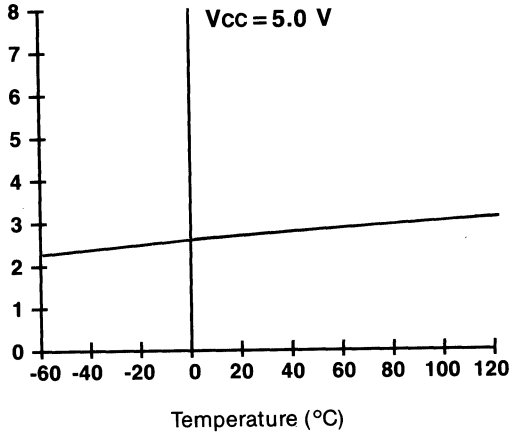


Figure 2-11b: t_{PHL}, A to B, All Paths

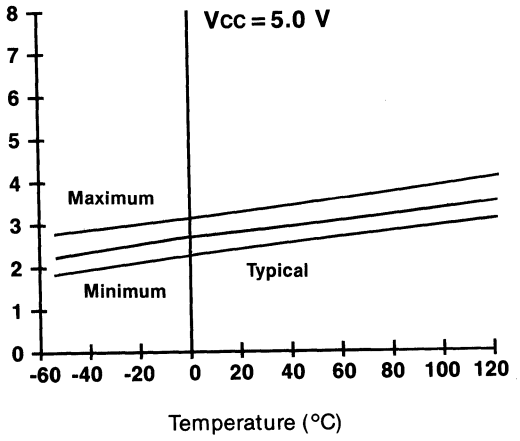


Figure 2-11c: Voltage Effects on Delay Times

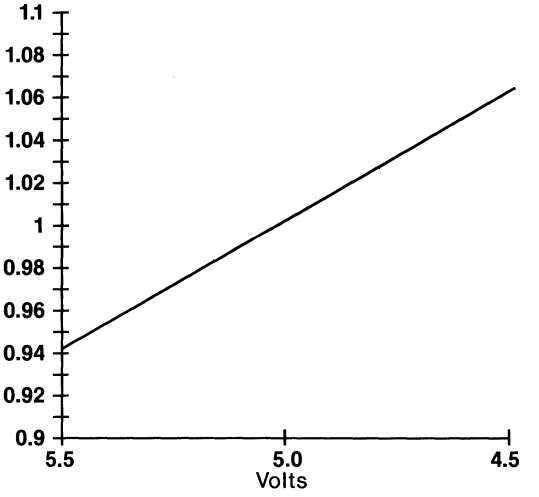


Figure 2-11d: FACT Process Effects on Delay Times

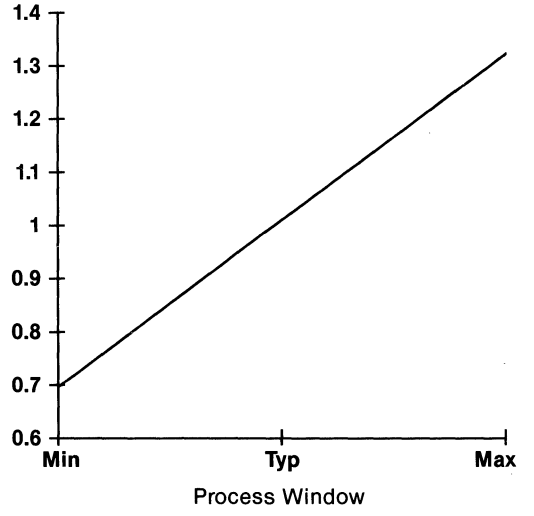
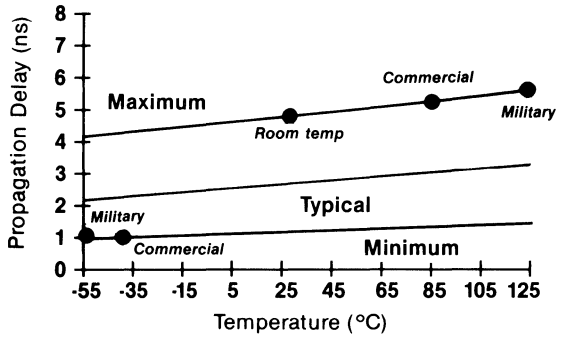


Figure 2-11e: t_{PHL}, A to B, with Voltage and Process Variation



The same reasoning can be applied to setup and hold times. Consider the 'AC74. The setup time is 3.0 ns while the hold time is 0 ns. Theoretically, if these numbers were violated, the device would malfunction; however, in actuality, the device probably will not malfunction. Looking at the typical setup and hold times gives a better understanding of the device operation.

At 25°C and 5.0 V, the setup time is 1.5 ns while the hold time is -1.5 ns. They are the same; a positive setup time means the control signal to be valid before the clock edge, a positive hold time indicates the control signal will be held valid after the clock edge for the specified time, and a negative hold time means the control signal can transition before the clock edge. FACT devices were designed to be as immune to metastability as possible. This is reflected in the typical specifications. The true 'critical' time where the input is actually sampled is extremely short: less than 50 ps.

By applying the same reasoning as we did to the propagation delays to the setup and hold times, it becomes obvious that the spread from setup to hold time (3 ns worst-case) really covers devices across the entire process/temperature/voltage spread. The real difference between the setup and hold times for any single device, at a specified temperature and voltage, is negligible.

Capacitive Loading Effects

In addition to temperature and power supply effects, capacitive loading effects for loads greater than 50 pF should be taken into account for propagation delays of FACT devices. Minimum delay numbers may be determined from the table below. Propagation delays are measured to the 50% point of the output waveform.

Parameter	Voltage (V)			Units
	3.0	4.5	5.5	
trise	31	22	19	ps/pF
tfall	18	13	12.5	ps/pF

$T_A = 25°C$

The two graphs following, Figures 2-12 and 2-13, describe propagation delays on FACT devices as affected by variations in power supply voltage (V_{CC}) and lumped load capacitance (C_L). Figures 2-14 and 2-15 show the effects of lumped load capacitance on rise and fall times for FACT devices.

Figure 2-12: Propagation Delay vs. V_{CC} ('AC00)

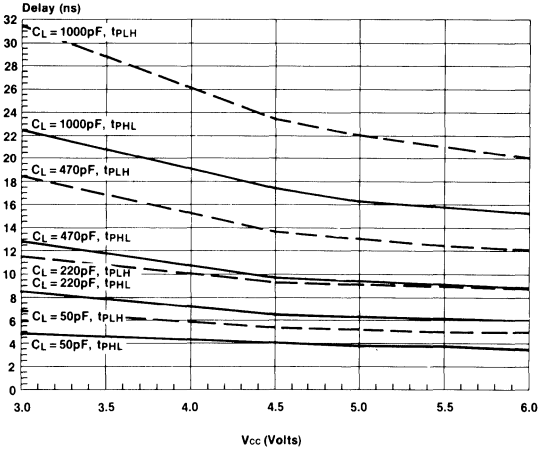


Figure 2-13: Propagation Delay vs. C_L (74AC00)

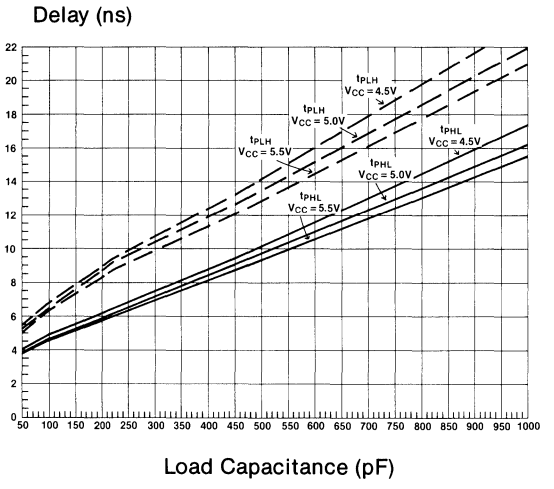


Figure 2-14: t_{rise} vs. Capacitance

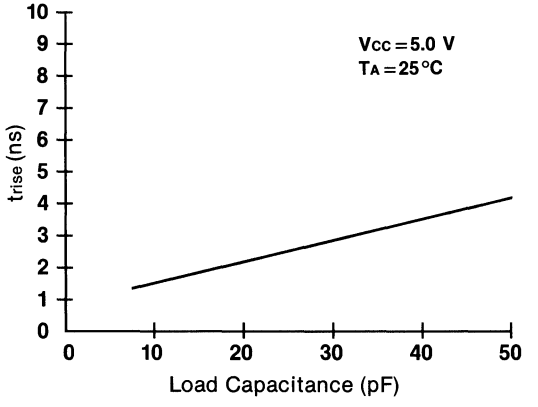
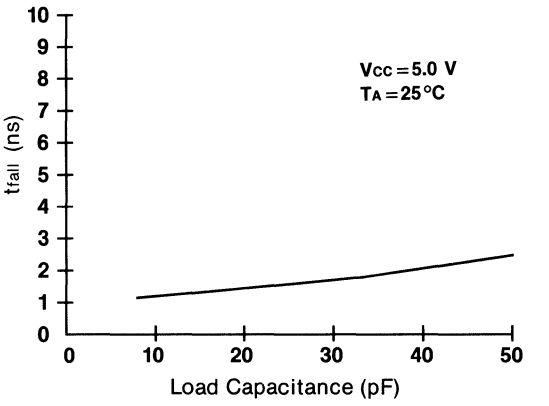


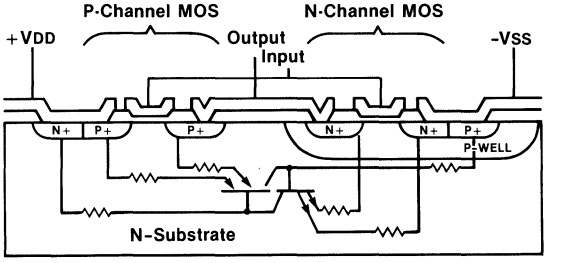
Figure 2-15: t_{fall} vs. Capacitance



Latch-up

A major problem with CMOS has been its sensitivity to latch-up, usually attributed to high parasitic gains and high input impedance. FACT logic is guaranteed not to latch-up with dynamic currents of 100 mA forced into or out of the inputs or the outputs under worst case conditions (T_A = 125°C and V_{CC} = 5.5 VDC). At room temperature the parts can typically withstand dynamic currents of over 450 mA. For most designs, latch-up will not be a problem, but the designer should be aware of its causes and how to prevent it.

Figure 2-16: CMOS Inverter Cross Section with Latch-up Circuit Schematic



FACT devices have been specifically designed to reduce the possibility of latch-up occurring; Fairchild accomplished this by lowering the gain of the parasitic transistors, reducing substrate and p-well resistivity to increase external drive current required to cause a parasitic to turn ON, and careful design and layout to minimize the substrate-injected current coupling to other circuit areas.

Electrostatic Discharge (ESD) Sensitivity

FACT circuits show excellent resistance to ESD-type damage. These logic devices are classified as category 'B' of MIL-STD-883C, test method 3015, and withstand 4000 V typically. FACT logic is guaranteed to have 2000 V ESD immunity on all inputs and outputs. FACT parts do not require any special handling procedures. However, normal handling precautions should be observed as in the case of any semiconductor device.

Figure 2-17 shows the ESD test circuit used in the sensitivity analysis for this specification. Figure 2-18 is the pulse waveform required to perform the sensitivity test.

The test procedure is as follows: five pulses, each of 2000 V, are applied to every combination of pins with a five second cool-down period between each pulse. The polarity is then reversed and the same procedure, pulse and pin combination used for an additional five discharges. Continue until all pins have been tested. If none of the devices from the sample population fails the DC and AC test characteristics, the device shall be classified as category B of MIL-STD-883C, TM-3015. For further specifications of TM-3015, refer to the relevant standard. The voltage is increased and the testing procedure is again performed; this entire process is repeated until all pins fail. This is done to thoroughly evaluate all pins.

Figure 2-17: ESD Test Circuit

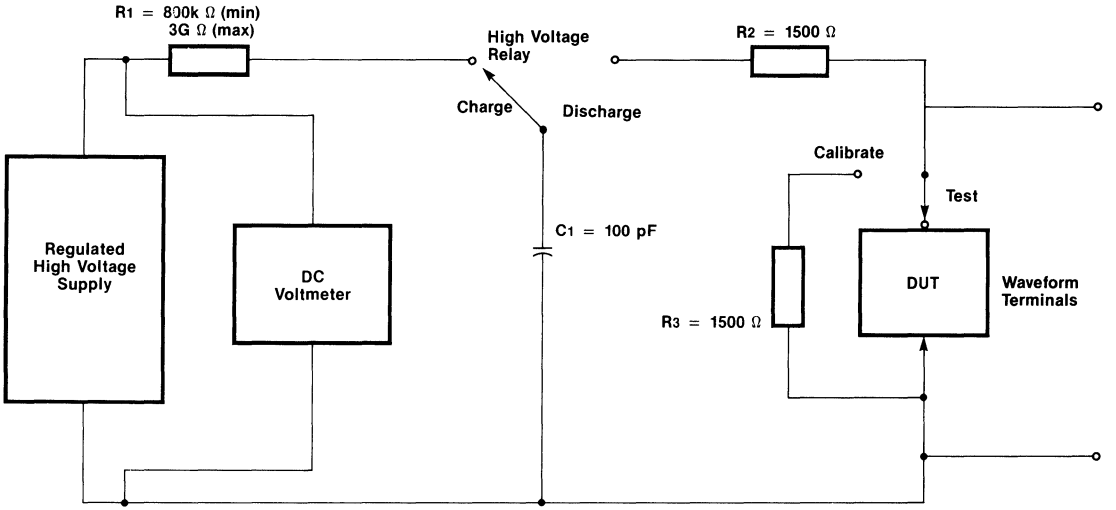
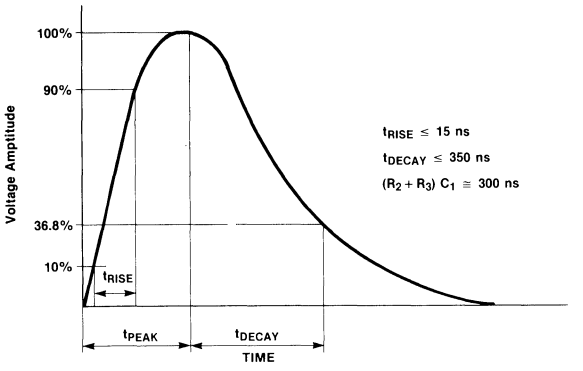


Figure 2-18: ESD Pulse Waveform



Radiation Tolerance

Semiconductors subjected to radiation environments undergo degradation in operating life as their exposure to radiation increases. As technology advances, so does the demand for radiation-tolerant devices. Fairchild is meeting this challenge by developing the FACT family into a comprehensive radiation tolerant product for present and future rad-hard needs. Such applications include:

- Space
  - Satellites
  - Space Stations
- Airborne and Military
  - Fighters/Bombers
  - Missile Systems
  - Ground Based Systems
  - Navigation & Communications
- Commercial
  - Power Stations
  - Medical
  - Food and Bacterial Control

Radiation tolerant semiconductors increase the useful life of the product in which it is incorporated. Additionally, radiation tolerant devices reduce shielding requirements and improve stabilization of parametric performance, resulting in cost reductions for shielding and weight, reduce power consumption and size.

Radiation Test Limits

Listed below are Fairchild's proposed procedures to test and guarantee FACT devices for radiation exposure limits:

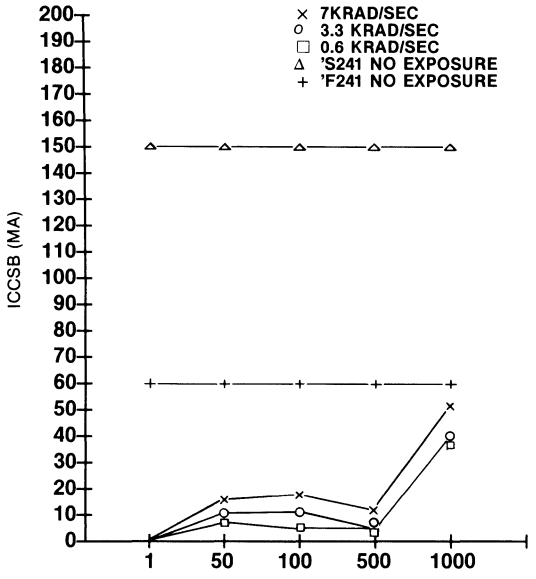
- Total Dose
  - Method 1019 per MIL-STD-883
  - Individual limits per FACT radiation tolerant data sheet specification
  - No functional failures
  - Gamma rays
- Transient Dose/Latchup
  - Methods 1020, 1021 per MIL-STD-883
  - Minimum transient upset threshold specification
  - Minimum latchup threshold specification
  - Device burnout specification
  - Gamma rays
- Neutron
  - Test not required for CMOS product
- Single Event Upset
  - To be announced in the future
  - Alpha Particle Radiation

Summary of Testing

To demonstrate and verify FACT's performance in radiation environments, we have tested several of our standard device types to total dose, transient dose and latch-up parameters. Standard manufacturing techniques were used in the production of all circuits. Devices of the same type were manufactured from the same wafer.

Test results, although limited to a small one-time sampling of the FACT product line, offer an indication of how various radiation environments affect specific standard FACT product. In most instances the standard FACT devices that were exposed to varying levels of total dose radiation showed reduced power consumption over functionally similar FAST and Schottky device types in non-radiation environments. Figure 2-19 shows a typical comparison of a FACT device's (54AC241) power consumption at various dose rates compared with functionally similar FAST (54F241) and Schottky (54S241) as tested in a non-radiation environment.

Figure 2-19: Total Dose Response (54AC241)



For total dose testing, all devices were subjected up to a 1 Mrad(Si) limit. There were no functional failures. Yet, based on the testing, parametric changes did occur.

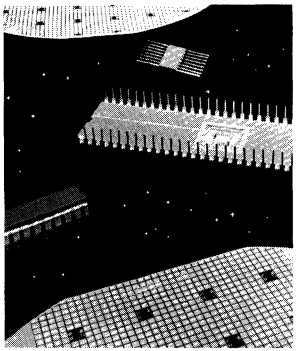
Transient dose testing evaluated how these devices would respond to quick bursts of radiation energies. Results were varied due to biasing and input conditions. Devices were generally free of transient upset and/or latch-up up to the range of 3×10^9 to 4.4×10^9 rads(Si)/second.

All devices were also taken to 5×10^{10} rads(Si)/second to determine if burnout would occur. There was no burnout at this level.

FACT is Radiation Tolerant

FACT logic employs the use of thin gate oxides, oxidation cycles, and annealing steps that enhance the tolerance of the standard FACT product line.

We are conducting additional testing and are evaluating further design enhancements for increased radiation tolerance levels of our FACT devices. Our current goal is a radiation tolerant FACT product line which exceeds the U.S. Government's VHSIC Phase II radiation requirements. At that time, Fairchild radiation tested products will be guaranteed at various total dose tolerance levels ranging between 50 Krads(Si) and 1 Mrad(Si).



Specifying FACT Devices

Traditionally, when a semiconductor manufacturer completed a new device for introduction, specifications were based on the characterization of just a few parts. While these specifications were appealing to the designer, they were often too tight and, over time, the IC manufacturers had difficulty producing devices to the original specs. This forced the manufacturer to relax circuit specifications to reflect the actual performance of the device.

As a result, designers were required to review system designs to ensure the system would remain reliable with the new specifications. Fairchild realized and understood the problems associated with characterizing devices too aggressively.

To provide more realistic and manufacturable specs, Fairchild devised a systematic and thorough process to generate specifications. Devices are selected from multiple wafer lots to ensure process variations are taken into account. In addition, the process parameters are measured and compared to the known process limits. With more than two years of experience manufacturing FACT logic, Fairchild can accurately predict how these wafer lots compare with the best and worse case lots that can possibly be expected.

This method of characterizing parts more accurately represents the product across time, voltage, temperature and process rather than portraying the fastest possible device. FACT circuits are therefore guaranteed to be manufacturable over time without the need to respecify timing.

These specification guidelines allow designers to design systems more efficiently since the devices used will behave as documented. Unspecified guardbands no longer need to be added by the designer to ensure system reliability.

Power Dissipation — Test Philosophy

In an effort to reduce confusion about measuring C_{PD}, a JEDEC standard test procedure (7A Appendix E) has been adopted which specifies the test setup for each type of device. This allows a device to be exercised in a consistent manner for the purpose of specification comparison. All device measurements are made with V_{CC} = 5.0 V at 25°C, with 3-state outputs both enabled and disabled.

Gates:	Switch one input. Bias the remaining inputs such that the output switches.
Latches:	Switch the Enable and D inputs such that the latch toggles.
Flip-Flops:	Switch the clock pin while changing D (or bias J and K) such that the output(s) change each clock cycle. For parts with a common clock, exercise only one flip-flop.
Decoders:	Switch one address pin which changes two outputs.
Multiplexers:	Switch one address pin with the corresponding data inputs at opposite logic levels so that the output switches.
Counters:	Switch the clock pin with other inputs biased such that the device counts.
Shift Registers:	Switch the clock pin with other inputs biased such that the device counts.
Transceivers:	Switch one data input. For bidirectional devices enable only one direction.
Parity Generator:	Switch one input.
Priority Encoders:	Switch the lowest priority input.
Load Capacitance:	Each output which is switching should be loaded with the standard 50 pF. The equivalent

If the device is tested at a high enough frequency, the static supply current can be ignored. Thus at 1 MHz, the following formula can be used to calculate C_{PD}:

$C_{PD} = I_{CC}/(V_{CC})\ (1 \times 10^6)$ - Equivalent Load Capacitance

Ratings and Specifications

Figure 3-1: Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Limits	Units
Supply Voltage	V_{CC}		-0.5 to 7.0	V
DC Input Diode Current or DC Input Voltage	I_{IK} V_I	$V_I = -0.5$ $V_I = V_{CC} + 0.5$	-20 20 -0.5 to $V_{CC} + 0.5$	mA mA V
DC Output Diode Current or DC Output Voltage	I_{OK} V_O	$V_O = -0.5$ $V_O = V_{CC} + 0.5$	-20 20 -0.5 to $V_{CC} + 0.5$	mA mA V
DC Output Source or Sink Current	I_O		± 50	mA
DC V_{CC} or Ground Current Per Output Pin	I_{CC} or I_{GND}		± 50	mA
Storage Temperature	T_{STG}		-65 to 150	°C

[1]Absolute maximum ratings are those values beyond which damage to the device may occur. Obviously the databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, output/input loading variables. Fairchild does not recommend operation of FACT circuits outside databook specifications.

Figure 3-2: Recommended Operating Conditions

Parameter		Symbol	Conditions	Limits	Units
Supply Voltage (unless otherwise specified)		V_{CC}		2.0 to 6.0	V
Input Voltage		V_I		0 to V_{CC}	V
Output Voltage		V_O		0 to V_{CC}	V
Operating Temperature	74AC/ACT 54AC/ACT	T_A		-40 to +85 -55 to +125	°C °C
Junction Temperature	CDIP PDIP	T_J		175 140	°C
Input Rise and Fall Time[2] (typical) (except Schmitt inputs) 'AC devices V_{IN} from 30% to 70% of V_{CC}		t_r, t_f	V_{CC} @ 3.0 V V_{CC} @ 4.5 V V_{CC} @ 5.5 V	150 40 25	ns/V ns/V ns/V
Input Rise and Fall Time[2] (typical) (except Schmitt inputs) 'ACT devices V_{IN} from 0.8 to 2.0 V, V_{meas} from 0.8 to 2.0 V		t_r, t_f	V_{CC} @ 4.5 V V_{CC} @ 5.5 V	10 8	ns/V ns/V

[2]See individual data sheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	Conditions	Vcc (V)	74AC		54AC	74AC	Units
				TA = 25°C		TA = -55° to +125°C	TA = -40° to +85°C	
				Typ	Guaranteed Limits			
VIH	Minimum High Level Input Voltage	VOUT = 0.1 V or VCC-0.1 V	3.0	1.5	2.1	2.1	2.1	V
			4.5	2.25	3.15	3.15	3.15	
			5.5	2.75	3.85	3.85	3.85	
VIL	Maximum Low Level Input Voltage	VOUT = 0.1 V or VCC-0.1 V	3.0	1.5	0.9	0.9	0.9	V
			4.5	2.25	1.35	1.35	1.35	
			5.5	2.75	1.65	1.65	1.65	
VOH	Minimum High Level Output Voltage	IOUT = -50 μA	3.0	2.99	2.9	2.9	2.9	V
			4.5	4.49	4.4	4.4	4.4	
			5.5	5.49	5.4	5.4	5.4	
		*VIN = VIL or VIH						
		IOH -12 mA	3.0		2.56	2.4	2.46	V
		IOH -24 mA	4.5		3.86	3.7	3.76	
		IOH -24 mA	5.5		4.86	4.7	4.76	
VOL	Maximum Low Level Output Voltage	IOUT = 50 μA	3.0	0.002	0.1	0.1	0.1	V
			4.5	0.001	0.1	0.1	0.1	
			5.5	0.001	0.1	0.1	0.1	
		*VIN = VIL or VIH						
		IOL 12 mA	3.0		0.32	0.4	0.37	V
		IOL 24 mA	4.5		0.32	0.4	0.37	
		IOL 24 mA	5.5		0.32	0.4	0.37	
IIN	Maximum Input Leakage Current	VI = VCC, GND	5.5		±0.1	±1.0	±1.0	μA
IOZ	Maximum 3-State Current	VI (OE) = VIL, VIH VI = VCC, VGND VO = VCC, GND	5.5		±0.5	±10.0	±5.0	μA
IOLD	†Minimum Dynamic Output Current	VOLD = 1.1 V	5.5			57	86	mA
IOHD		VOHD = 3.85 V	5.5			-50	-75	mA

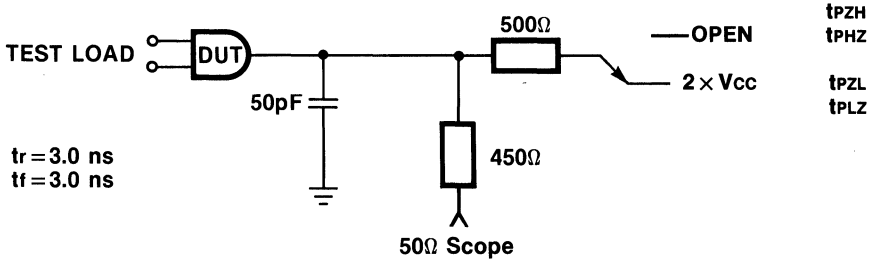
*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 20 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	Conditions	Vcc (V)	74ACT		54ACT	74ACT	Units
				TA = 25°C		TA = -55° to +125°C	TA = -40° to +85°C	
				Typ	Guaranteed Limits			
VIH	Minimum High Level Input Voltage	VOUT = 0.1 V or VCC-0.1 V	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V
VIL	Maximum Low Level Input Voltage	VOUT = 0.1 V or VCC-0.1 V	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V
VOH	Minimum High Level	IOUT = -50 μA	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V
		*VIN = VIL or VIH IOH -24 mA -24 mA	4.5 5.5	0.0001	3.86 4.86	3.70 4.70	3.76 4.76	V
VOL	Maximum Low Level Output Voltage	IOUT = 50 μA	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V
		*VIN = VIL or VIH IOL 24 mA 24 mA	4.5 5.5		0.32 0.32	0.40 0.40	0.37 0.37	V
IIN	Maximum Input	VI = VCC, GND	5.5		±0.1	±1.0	±1.0	μA
IOZ	Maximum 3-State Current	VI = VIL, VIH VO = VCC, GND	5.5		±0.5	±10.0	±5.0	μA
ICCT	Maximum Icc/Input	VI = VCC-2.1 V	5.5	0.6		1.6	1.5	mA
IOLD	†Minimum Dynamic Output Current	VOLD = 1.1 V	5.5			57	86	mA
IOHD		VOHD = 3.85 V	5.5			-50	-75	mA

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

Figure 3-3: AC Loading Circuit



AC Loading and Waveforms

Loading Circuit

Figure 3-3 shows the AC loading circuit used in characterizing and specifying propagation delays of all FACT devices ('AC and 'ACT) unless otherwise specified in the data sheet of a specific device.

The use of this load, which is equivalent to the FAST (Fairchild Advanced Schottky TTL) test jig, differs somewhat from previous (HCMOS) practice, provides more meaningful information and minimizes problems of instrumentation and customer correlation. In the past, +25°C propagation delays for TTL devices were specified with a load of 15 pF to ground; this required great care in building test jigs to minimize stray capacitance and implied the use of high impedance, high frequency scope probes. FAST circuits changed to 50 pF of capacitance allowing more leeway in stray capacitance and also loading the device during rising or falling output transitions. This more closely resembles the in-loading to be expected in average applications and thus gives the designer more useful delay figures. We have incorporated this scheme into the FACT product line. The net effect of the change in AC load is to increase the average observed propagation delay by about 1 ns.

The 500 ohm resistor to ground can be a high frequency passive probe for a sampling oscilloscope, which costs much less than the equivalent high impedance probe. Alternately, the 500 ohm resistor to ground can simply be a 450 ohm resistor feeding into a 50 ohm coaxial cable leading to a sampling scope input connector, with the internal 50 ohm termination of the scope completing the path to ground. This is the preferred scheme for correlation. (See Figure 3-3.) With this scheme there should be a matching cable from the device input pin to the other input of the sampling scope; this also serves as a 50 ohm termination for the pulse generator that supplies the input signal.

Shown in Figure 3-3 is a second 500 ohm resistor from the device output to a switch. For most measurements this switch is open; it is closed for measuring one set of the Enable/Disable parameters (LOW-to-OFF and OFF-to-LOW) of a 3-state output. With the switch closed, the pair of 500 ohm resistors and the 2 × Vcc supply voltage establish a quiescent HIGH level.

Figure 3-4a: Test Input Signal Levels

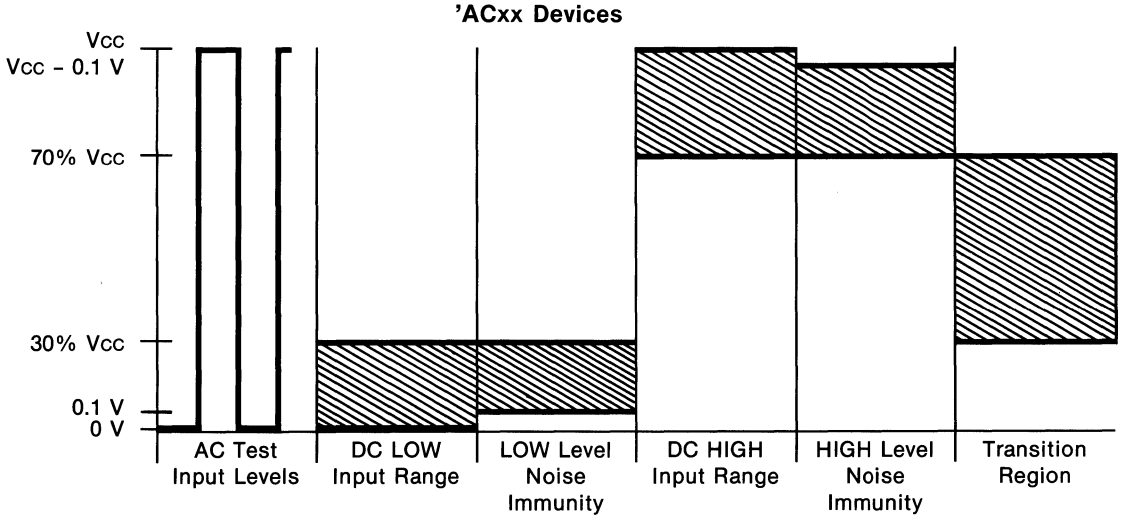
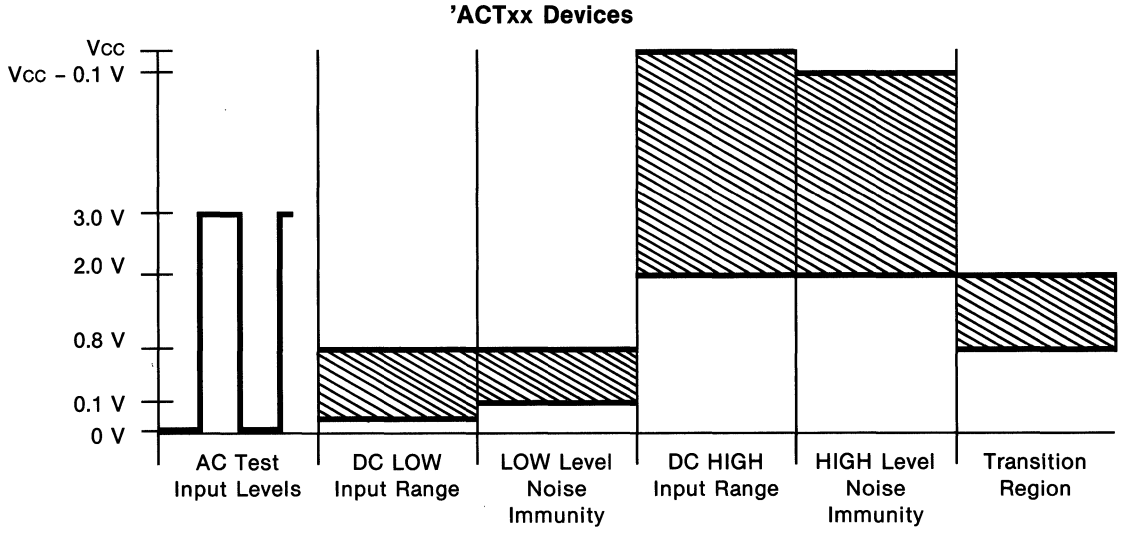


Figure 3-4b: Test Input Signal Levels



Test Conditions

Figures 3-4a and 3-4b describe the input signal voltage levels to be used when testing FACT circuits. The AC test conditions follow industry convention requiring V_{IN} to range from 0 V for a logic LOW to 3.0 V for a logic HIGH for 'ACT devices and 0 V to V_{CC} for 'AC devices. The DC parameters are normally tested with V_{IN} at guaranteed input levels, that is V_{IH} to V_{IL} (see data tables for details). Care must be taken to adequately decouple these high performance parts and to protect the test signals from electrical noise. In an electrically noisy environment, (e.g., a tester and handler not specifically designed for high speed work), DC input levels may need to be adjusted to increase the noise margin to allow for the extra noise in the tester which would not be seen in a system.

Noise immunity testing is performed by raising V_{IN} to the nominal supply voltage of 5.0 V then dropping to a level corresponding to V_{IH} characteristics, and then raising again to the 5.0 V level. Noise tests can also be performed on the V_{IL} characteristics by raising V_{IN} from 0 V to V_{IL}, then returning to 0 V. Both V_{IH} and V_{IL} noise immunity tests should not induce a switch condition on the appropriate outputs of the FACT device.

Good high frequency wiring practices should be used in constructing test jigs. Leads on the load capacitor should be as short as possible to minimize ripples on the output waveform transitions and to minimize undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} bypass capacitor should be provided at the test socket, also with minimum lead lengths.

Rise and Fall Times

Input signals should have rise and fall times of 3.0 ns and signal swing of 0 V to 3.0 V V_{CC} for 'ACT devices or 0 V to V_{CC} for 'AC devices. Rise and fall times less than or equal to 1 ns should be used for testing f_{max} or pulse widths.

CMOS devices, including 4000 Series CMOS, HC, HCT and FACT families, tend to oscillate when the input rise and fall times become lengthy. As a direct result of its increased performance, FACT devices can be more sensitive to slow input rise and fall times than other lower performance technologies.

It is important to understand why this oscillation occurs. Consider the outputs, where the problem is initiated. Usually, CMOS outputs drive capacitive loads with low DC leakage. When the output changes from a HIGH level to a LOW level, or from a LOW level to a HIGH level, this capacitance has to be charged or discharged. With the present high performance technologies, this charging or discharging takes place in a very short time, typically 2-3 ns. The requirement to charge or discharge the capacitive loads quickly creates a condition where the instantaneous current change through the output structure is quite high. A voltage is generated across the Vcc or ground leads inside the package due to the inductance of these leads. The internal ground of the chip will change in reference to the outside world because of this induced voltage.

Consider the input. If the internal ground changes, the input voltage level appears to change to the DUT. If the input rise time is slow enough, its level might still be in the device threshold region, or very close to it, when the output switches. If the internally-induced voltage is large enough, it is possible to shift the threshold region enough so that it re-crosses the input level. If the gain of the device is sufficient and the input rise or fall time is slow enough, then the device may go into oscillation. As device propagation delays become shorter, the inputs will have less time to rise or fall through the threshold region. As device gains increase, the outputs will swing more, creating more induced voltage. Instantaneous current change will be greater as outputs become quicker, generating more induced voltage.

Package-related causes of output oscillation are not entirely to blame for problems with input rise and fall time measurements. All testers have Vcc and ground leads with a finite inductance. This inductance needs to be added to the inductance in the package to determine the overall voltage which will be induced when the outputs change. As the reference for the input signals moves further away from the pin under test, the test will be more susceptible to problems caused by the inductance of the leads and stray noise. Any noise on the input signal will also cause problems. With FACT logic having gains as high as 100, it merely takes a 50 mV change in the input to generate a full 5 V swing on the output.

Figure 3-5: Waveform for Inverting and Non-Inverting Functions

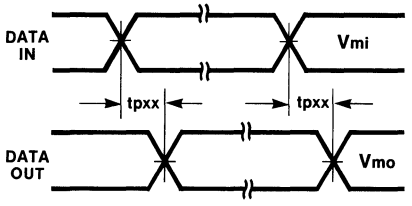
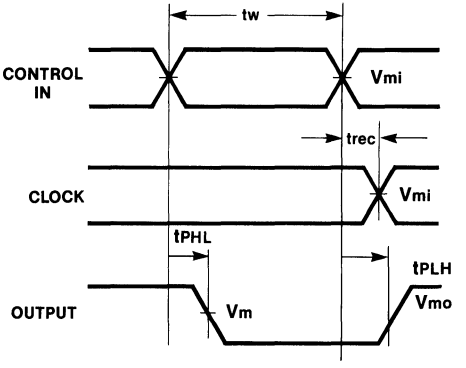


Figure 3-6: Propagation Delay, Pulse Width and trec Waveforms



*Vmi = 50% Vcc for 'AC devices; 1.5 V for 'ACT devices
Vmo = 50% for 'AC/'ACT devices

Figure 3-7: 3-State Output High Enable and Disable Times

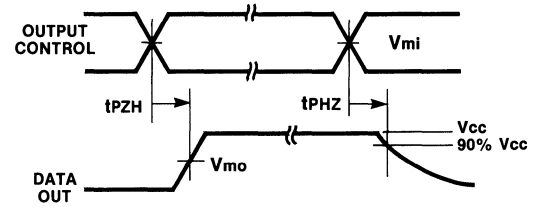


Figure 3-8: 3-State Output Low Enable and Disable Times

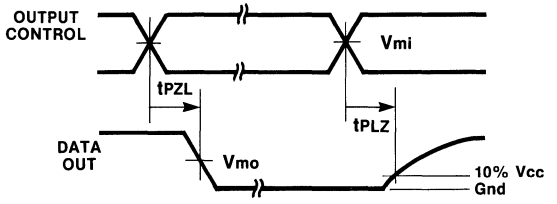
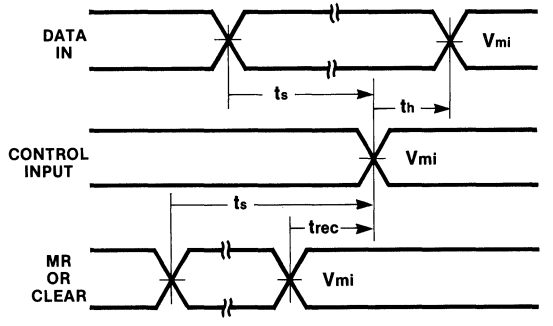


Figure 3-9: Setup Time, Hold Time and Recovery Time



*V_{mi} = 50% Vcc for 'AC devices; 1.5 V for 'ACT devices
V_{mo} = 50% Vcc for 'AC/'ACT devices

Propagation Delays, f_{max}, Set and Hold Times

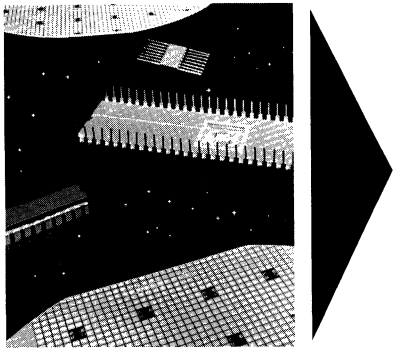
A 1.0 MHz square wave is recommended for most propagation delay tests. The repetition rate must necessarily be increased for testing f_{max}. A 50% duty cycle should always be used when testing f_{max}. Two pulse generators are usually required for testing such parameters as setup time, hold time, recovery time, etc.

Enable and Disable Times

Figures 3-7 and 3-8 show that the disable times are measured at the point where the output voltage has risen or fallen by 10% from the voltage rail level (i.e., ground for t_{PLZ} or Vcc for t_{PHZ}). This change enhances the repeatability of measurements, reduces test times, and gives the system designer more realistic delay times to use in calculating minimum cycle times. Since the high impedance state rising or falling waveform is RC-controlled, the first 10% of change is more linear and is less susceptible to external influences. More importantly, perhaps from the system designer's point of view, a change in voltage of 10% is adequate to ensure that a device output has turned OFF. Measuring to a larger change in voltage merely exaggerates the apparent Disable time and thus penalizes system performance since the designer must use the Enable and Disable times to devise worst case timing signals to ensure that the output of one device is disabled before that of another device is enabled.

Electrostatic Discharge

Precautions should be taken to prevent damage to devices by electrostatic discharge. Static charge tends to accumulate on insulated surfaces such as synthetic fabrics or carpeting, plastic sheets, trays, foam, tubes or bags, and on ungrounded electrical tools or appliances. The problem is much worse in a dry atmosphere. In general, it is recommended that individuals take the precaution of touching a known ground before handling devices. To effectively avoid electrostatic damage to FACT devices, it is recommended that individuals wear a grounded wrist strap when handling devices. More often, handling equipment, which is not properly grounded, causes damage to parts. Ensure that all plastic parts of the tester, which are near the device, are conductive and connected to ground.



Design Considerations

Today's system designer is faced with the problem of keeping ahead when addressing system performance and reliability. Fairchild's Advanced CMOS helps designers achieve these goals.

FACT (Fairchild Advanced CMOS Technology) logic was designed to alleviate many of the drawbacks that are common to current technology logic circuits. FACT logic combines the low static power consumption and the high noise margins of CMOS with a high fan-out, low input loading and a 50 ohm transmission line drive capability (comparable to Fairchild's FAST bipolar technology family) to offer a complete family of 1.3-micron SSI, MSI and LSI devices.

Performance features such as advanced Schottky speeds at CMOS power levels, advanced Schottky drive, excellent noise, ESD and latch-up immunity are characteristics that designers of state-of-the-art systems require. FACT logic answers all of these concerns in one family of products. To fully utilize the advantages provided by FACT, the system designer should have an understanding of the flexibility as well as the trade-offs of CMOS design. The following section discusses common design concerns relative to the performance and requirements of FACT.

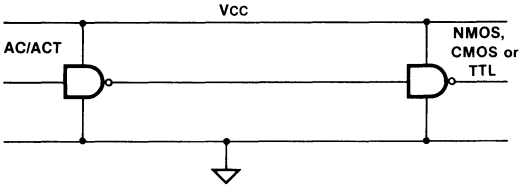
There are five items of interest which need to be evaluated when implementing FACT devices in new designs:

- Interfacing — interboard and technology interfaces, battery backup and power down or live insert/extract systems require some special thought.
- Transmission Line Driving — FACT has line driving capabilities superior to all CMOS families and most TTL families.
- Noise effects — As edge rates increase, the probability of crosstalk and ground bounce problems increases. The enhanced noise immunity and high threshold levels improve FACT's resistance to crosstalk problems.
- Board Layout — Prudent board layout will ensure that most noise effects are minimized.
- Power Supplies and Decoupling — Maximize ground and Vcc traces to keep Vcc/ground impedance as low as possible; full ground/Vcc planes are best. Decouple any device driving a transmission line; otherwise add one capacitor for every package.

Interfacing

FACT devices have outputs which combine balanced CMOS outputs with high current line driving capability. Each standard output is guaranteed to source or sink 24 mA of current at worst case conditions. This allows FACT circuits to drive more loads than standard advanced Schottky parts; FACT can directly drive ALS, AS, LS, HC and HCT devices.

Figure 4-1: Interfacing FACT to NMOS, CMOS and TTL

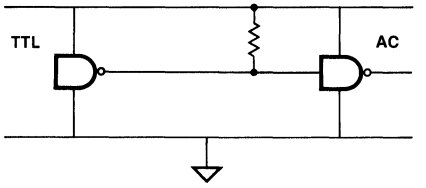


FACT devices can be directly driven by both NMOS and CMOS families, as shown in Figure 4-1, operating at the same rail potential without special considerations. This is possible due to the low input loading of FACT product, guaranteed to be less than 1 μA per input.

Some older technologies, including all existing TTL families, will not be able to drive FACT circuits directly; this is due to inadequate high level capability, which is guaranteed to 2.4 V. There are two simple approaches to the TTL-to-FACT interface problem. A TTL-to-CMOS converter can be

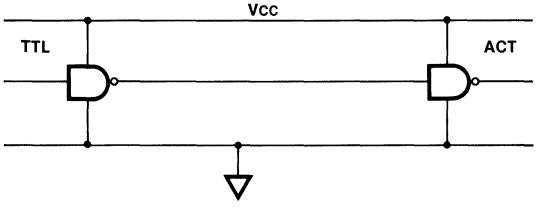
constructed employing a resistor pull-up to Vcc of approximately 4.7k ohms, which is depicted in Figure 4-2. The correct HIGH level is seen by the CMOS device while not loading down the TTL driver.

Figure 4-2: V_{IH} Pull-Up on TTL Outputs



Unfortunately, there will be designs where including a pull-up resistor will not be acceptable. In these cases, such as a terminated TTL bus, Fairchild has designed devices which offer thresholds that are TTL-compatible (Figure 4-3). These interfaces tend to be slightly slower than their CMOS-level counterparts due to an extra buffer stage required for level conversion.

Figure 4-3: TTL Interfacing to 'ACT



ECL devices cannot directly drive FACT devices. Interfacing FACT-to-ECL can be accomplished by using TTL-to-ECL translators and 10125 ECL-to-TTL translators in addition to following the same rules on the TTL outputs to CMOS inputs (i.e., a resistor pull-up to Vcc of approximately 4.7k ohms). The translation can also be accomplished by a resistive network. A three-resistor interface between FACT and ECL logic is illustrated in Figure 4-4a. Figures 4-4b and 4-4c show the translation from ECL-to-FACT, which is somewhat more complicated. These two examples offer some possible interfaces between ECL and FACT logic.

Figure 4-4a: Resistive FACT-to-ECL Translation

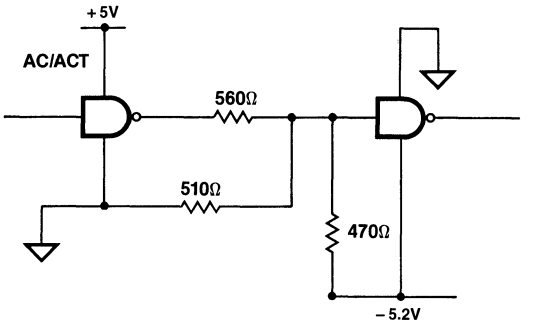


Figure 4-4b: Single-Ended ECL-to-'AC Circuit

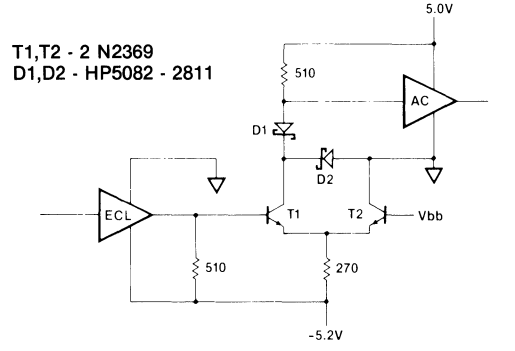
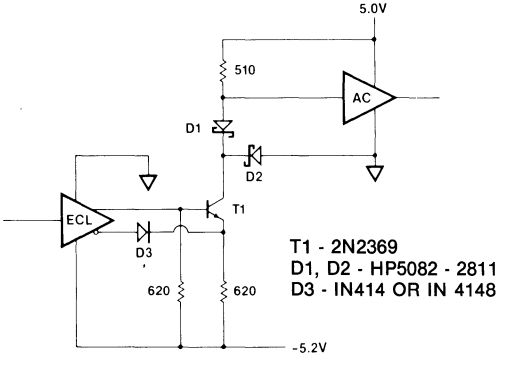
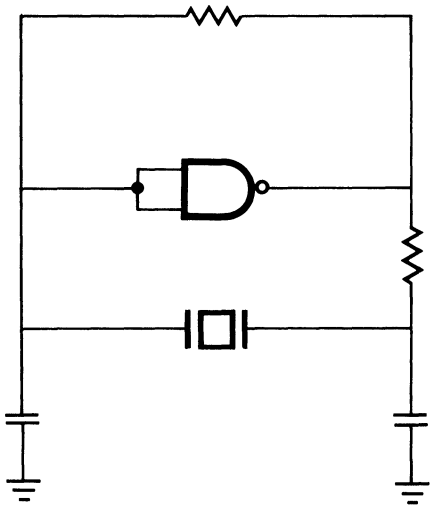


Figure 4-4c: Differential Output ECL-to-'AC Circuit



It should be understood that for FACT, as with other CMOS technologies, input levels that are between specified input values will cause both transistors in the CMOS structure to be conducting. This will cause a low resistive path from the supply rail to ground, increasing the power consumption by several orders of magnitude. It is important that CMOS inputs are always driven as close as possible to the rail.

Figure 4-5: Crystal Oscillator Circuit Implemented with FACT 'AC00



Line Driving

With the available high-speed logic families, designers can reach new heights in system performance. Yet, these faster devices require a closer look at transmission line effects.

Although all circuit conductors have transmission line properties, these characteristics become significant when the edge rates of the drivers are equal to or less than three times the propagation delay of the line. Significant transmission line properties may be exhibited in an example where devices have edge rates of 3 ns and lines of 8 inches or greater, assuming propagation delays of 1.7 ns/ft for an unloaded printed circuit trace.

Of the many properties of transmission lines, two are of major interest to the system designer: Z_{oe}, the effective equivalent impedance of the line, and t_{pde}, the effective propagation delay down the line. It should be noted that the intrinsic values of line impedance and propagation delay, Z_o and t_{pd}, are geometry-dependent. Once the intrinsic values are known, the effects of gate loading can be calculated. The loaded values for Z_{oe} and t_{pde} can be calculated with:

$$Z_{oe} = \frac{Z_o}{\sqrt{1+C_t/C_l}}$$

$$t_{pde} = t_{pd}\sqrt{1+C_t/C_l}$$

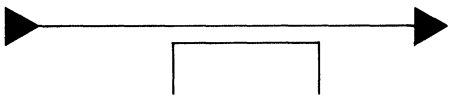
where C_l = intrinsic line capacitance and C_t = additional capacitance due to gate loading.

The formulas indicate that the loading of lines decreases the effective impedance of the line and increases the propagation delay. Lines that have a propagation delay greater than one third the rise time of the signal driver should be evaluated for transmission line effects. When performing transmission line analysis on a bus, only the longest, most heavily loaded and the shortest, least loaded lines need to be analyzed. All lines in a bus should be terminated equally; if one line requires termination, all lines in the bus should be terminated. This will ensure similar signals on all of the lines.

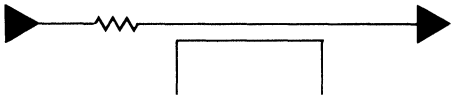
There are several termination schemes which may be used. Included are series, parallel, AC parallel and Thevenin terminations. AC parallel and series terminations are the most useful for low power applications since they do not consume any DC power. Parallel and Thevenin terminations experience high DC power consumption.

Termination Schemes

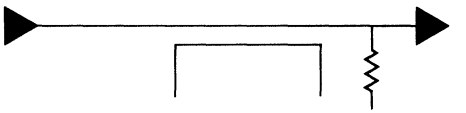
Figure 4-6: Termination Schemes



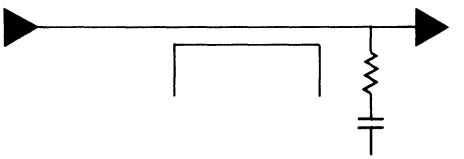
a: No Termination



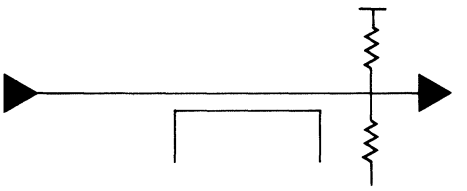
b: Series Termination



c: Parallel Termination



d: AC Parallel Termination



e: Thevenin Termination

Series Terminations
Series terminations are most useful in high-speed applications where most of the loads are at the far end of the line. Loads that are between the driver and the end of the line will receive a two-step waveform. The first wave will be the incident wave. The amplitude is dependent upon the output impedance of the driver, the value of the series resistor and the impedance of the line according to the formula

$$V_W = V_{CC} \bullet Z_{oe}/(Z_{oe} + R_S + Z_S)$$

The amplitude will be one-half the voltage swing if Rs (the series resistor) plus the output impedance (Z_S) of the driver is equal to the line impedance. The second step of the waveform is the reflection from the end of the line and will have an amplitude equal to that of the first step. All devices on the line will receive a valid level only after the wave has propagated down the line and returned to the driver. Therefore, all inputs will see the full voltage swing within two times the delay of the line.

Parallel Termination
Parallel terminations are not generally recommended for CMOS circuits due to their power consumption, which can exceed the power consumption of the logic itself. The power consumption of parallel terminations is a function of the resistor value and the duty cycle of the signal. In addition, parallel termination tends to bias the output levels of the driver towards either V_{CC} or ground. While this feature is not desirable for driving CMOS inputs, it can be useful for driving TTL inputs.

AC Parallel Termination
AC parallel terminations work well for applications where the delays caused by series terminations are unacceptable. The effects of AC parallel terminations are similar to the effects of standard parallel terminations. The major difference is that the capacitor blocks any DC current path and helps to reduce power consumption.

Thevenin Termination
Thevenin terminations are also not generally recommended due to their power consumption. Like parallel termination, a DC path to ground is created by the terminating resistors. The power consumption of a Thevenin termination, though, will generally not be a function of the signal duty cycle. Thevenin terminations are more applicable for driving CMOS inputs because they do not bias the output levels as paralleled terminations do. It should be noted that lines with Thevenin terminations should not be left floating since this will cause the input levels to float between V_{CC} or ground, increasing power consumption.

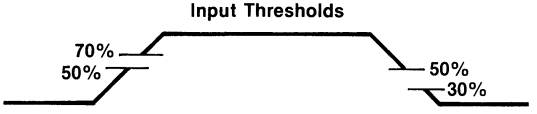
FACT circuits have been designed to drive 50 ohm transmission lines over the full commercial temperature range and 75 ohm transmission lines over the military temperature range. This is guaranteed by the FACT family's specified dynamic

drive capability of 86 mA sink and 75 mA source current. This ensures incident wave switching on 50 ohm transmission lines and is consistent with the 3 ns rated edge transition time.

FACT devices also feature balanced output totem pole structures to allow equal source and sink current capability. This gives rise to balanced edge rates and equal rise and fall times. Balanced drive capability and transition times eliminate both the need to calculate two different delay times for each signal path and the requirement to correct signal polarity for the shortest delay time.

FACT product inputs have been created to take full advantage of high output levels to deliver the maximum noise immunity to the system designer. V_{IH} and V_{IL} are specified at 70% and 30% of V_{CC} respectively. The corresponding output levels, V_{OH} and V_{OL}, are specified to be within 0.1 V of the rails, of which the output is sourcing or sinking 20 μA or less. These noise margins are outlined in Figure 4-7.

Figure 4-7: Input Threshold

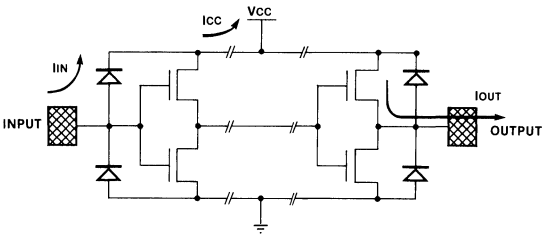


CMOS Bus Loading

CMOS logic devices have clamp diodes from all inputs and outputs to V_{CC} and ground. While these diodes increase system reliability by damping out undershoot and overshoot noise, they can cause problems if power is lost.

Figure 4-8 exemplifies the situation when power is removed. Any input driven above the V_{CC} pin will forward-bias the clamp diode. Current can then flow into the device, and out V_{CC} or any output that is HIGH. Depending upon the system, this current, I_{IN}, can be quite high, and may not allow the bus voltage to reach a valid HIGH state. One possible solution to eliminate this problem is to place a series resistor in the line.

Figure 4-8: Noise Effects



Noise Effects

FACT offers the best noise immunity of any competing technology available today. With input thresholds specified at 30% and 70% of V_{CC} and outputs that drive to within 100 mV of the rails, FACT devices offer noise margins approaching 30% of V_{CC}. At 5 V V_{CC}, FACT's specified input and output levels give almost 1.5 V of noise margin for both ground- and V_{CC}-born noise. With realistic input thresholds closer to 50% of V_{CC}, the actual margins approach 2.5 V.

However, even the most advanced technology cannot alone eliminate noise problems. Good circuit board layout techniques are essential to take full advantage of the superior performance of FACT circuits.

Well-designed circuit boards also help eliminate manufacturing and testing problems.

Another recommended practice is to segment the board into a high-speed area, a medium-speed area and a low-speed area. The circuit areas with high current requirements (i.e., buffer circuits and high-speed logic) should be as close to the power supplies as possible; low-speed circuit areas can be furthest away.

Decoupling capacitors should be adjacent to all buffer chips; they should be distributed throughout the logic: one capacitor per chip. Transmission lines need to be terminated to keep reflections minimal. To minimize crosstalk, long signal lines should not be close together.

Crosstalk

The problem of crosstalk and how to deal with it is becoming more important as system performance and board densities increase. Crosstalk is the capacitive coupling of signals from one line to

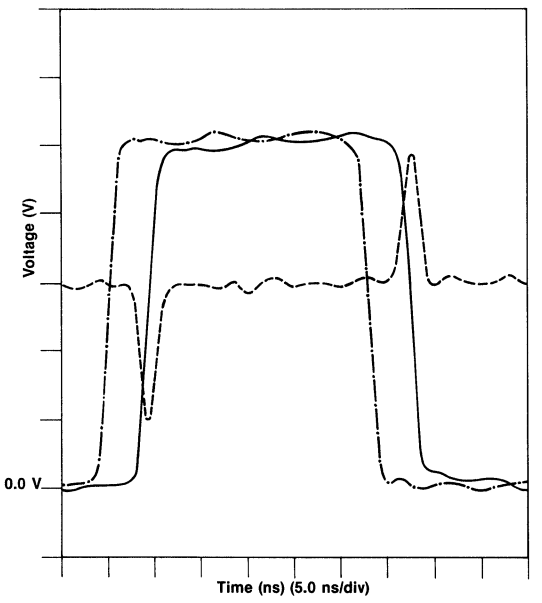
another. The amplitude of the noise generated on the inactive line is directly related to the edge rates of the signal on the active line, the proximity of the two lines and the distance that the two lines are adjacent.

Crosstalk has two basic causes. Forward crosstalk, Figure 4-9a, is caused by the wavefront propagating down the printed circuit trace at two different velocities. This difference in velocities is due to the difference in the dielectric constants of air ($\epsilon_r = 1.0$) and epoxy glass ($\epsilon_r = 4.7$). As the wave propagates down the trace, this difference in velocities will cause one edge to reach the end before the other. This delay is the cause of forward crosstalk; it increases with longer trace length, so consequently the magnitude of forward crosstalk will increase with distance.

Reverse crosstalk, Figure 4-9b, is caused by the mutual inductance and capacitance between the lines which is a transformer action. Reverse crosstalk increases linearly with distance up to a critical length. This critical length is the distance that the signal can travel during its rise or fall time.

Although crosstalk cannot be totally eliminated, there are some design techniques that can reduce system problems resulting from crosstalk. FACT's industry-leading noise margins make systems immune to crosstalk-related problems easier to design. FACT's AC noise margins, shown in Figures 4-10a and 4-10b, exemplify the outstanding immunity to everyday noise which can effect system reliability.

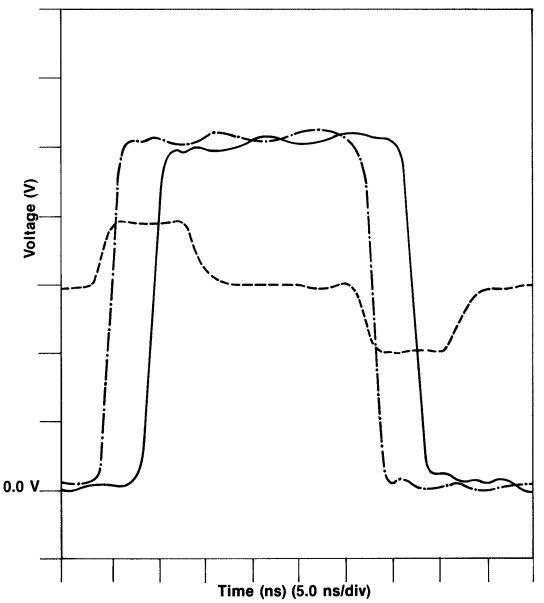
Figure 4-9a: Forward Crosstalk on PCB Traces



Key	Vertical Scale	Horizontal Scale
-·-·-· Active Driver	1.0 V/Div	50 ns/Div
-------- Forward Crosstalk	0.2 V/Div	5.0 ns/Div
—— Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

Figure 4-9b: Reverse Crosstalk on PCB Traces



Key	Vertical Scale	Horizontal Scale
-·-·-· Active Driver	1.0 V/Div	50 ns/Div
-------- Reverse Crosstalk	0.2 V/Div	5.0 ns/Div
—— Active Receiver	1.0 V/Div	5.0 ns/Div

This figure shows traces taken on a test fixture designed to exaggerate the amplitude of crosstalk pulses.

Figure 4-10a: High Noise Margin

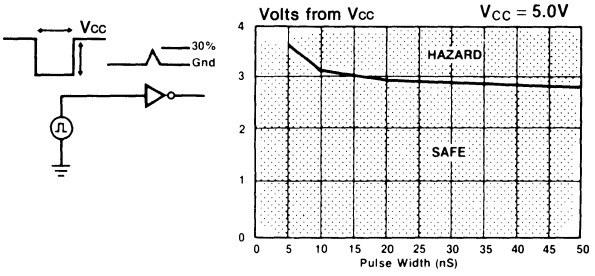
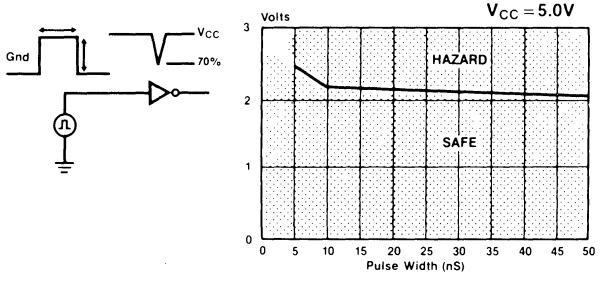


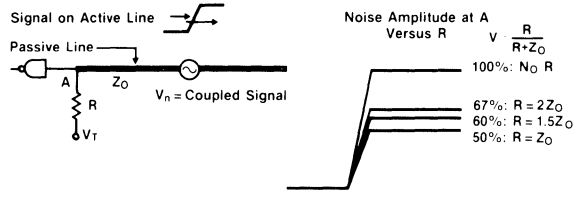
Figure 4-10b: Low Noise Margin



With over 2.0 V of noise margins, the FACT family offers better noise rejection than any other comparable technology.

In any design, the distance that lines run adjacent to each other should be kept as short as possible. The best situation is when the lines are perpendicular to each other. For those situations where lines must run parallel, the effects of crosstalk can be minimized by line termination. Terminating a line in its characteristic impedance reduces the amplitude of an initial crosstalk pulse by 50%. Terminating the line will also reduce the amount of ringing. Crosstalk problems can also be reduced by moving lines further apart or by inserting ground lines or planes between them.

Figure 4-11: Effects of Termination on Crosstalk



Ground Bounce

Ground bounce occurs as a result of the intrinsic characteristics of the leadframes and bondwires of the packages used to house CMOS devices. As edge rates and drive capability increase in advanced logic families, the effects of these intrinsic electrical characteristics become more pronounced.

Figure 4-12a shows a simple circuit model for a device in a leadframe driving a standard test load. The inductor L1 represents the parasitic inductance in the ground lead of the package; inductor L2 represents the parasitic inductance in the power lead of the package; inductor L3 represents the parasitic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor CL and RL represent the standard test load on the output of the device.

Figure 4-12a: Output Model

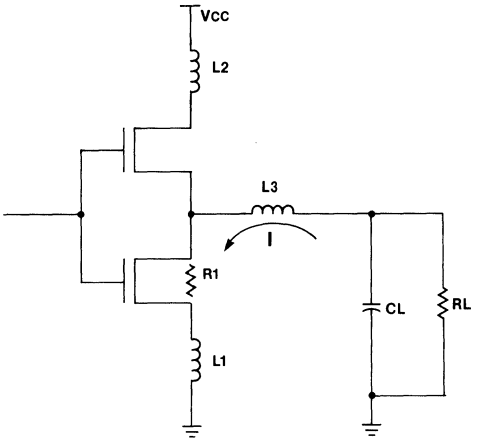


Figure 4-12b: Output Voltage

Figure 4-12c: Output Current

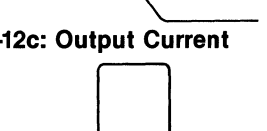
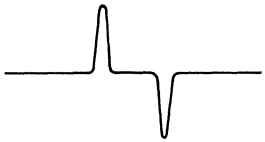


Figure 4-12d: Inductor Voltage



The three waveforms shown in Figures 4-12b, c and d, depict how ground bounce is generated. The first waveform shows the voltage (V) across the load as it is switched from a logic HIGH to a logic LOW. The output slew rate is dependent upon the characteristics of the output transistor, the inductors L1 and L3, and C_L, the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [$I = C_L \cdot dV/dt$]. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [$V_{gb} = -L \cdot (dI/dt)$].

There are many factors which affect the amplitude of the ground bounce. Included are:

- Number of outputs switching simultaneously: more outputs results in more ground bounce.
- Type of output load: capacitive loads generate two to three times more ground bounce than typical system traces. Increasing the capacitive load to approximately 60-70 pF increases ground bounce. Beyond 70 pF, ground bounce drops off due to the filtering effect of the load. Moving the load away from the output reduces the ground bounce.
- Location of the output pin: outputs closer to the ground pin exhibit less ground bounce than those further away.
- Voltage: lowering V_{CC} reduces ground bounce.
- Test fixtures: standard test fixtures generate 30 to 50% more ground bounce than a typical system since they use capacitive loads which both increase the AC load and form LCR tank circuits that oscillate.

Ground bounce produces several symptoms:

- Altered device states. FACT logic does not exhibit this symptom.
- Propagation delay degradation. FACT devices are characterized not to degrade more than 250 ps per additional output switching.
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.
- Quiet output noise. FACT logic's worst-case quiet output noise has been measured to be approximately 500-1100 mV in actual system applications.

Observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce:

First, use caution when driving asynchronous TTL-level inputs from CMOS octal outputs, or

Second, use caution when running control lines (set, reset, load, clock, chip select) which are glitch-sensitive through the same devices that drive data or address lines.

When it is not possible to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:

- Locate these outputs as close to the ground pin as possible.
- Use the lowest V_{CC} possible or separate the power supplies.
- Use board design practices which reduce any additive noise sources, such as crosstalk, reflections, etc.

Design Rules

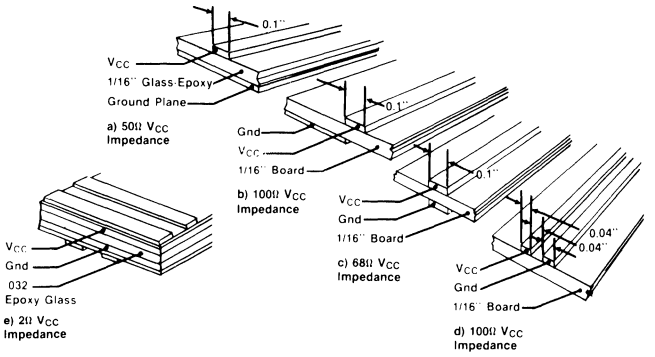
The set of design rules listed below are recommended to ensure reliable system operation by providing the optimum power supply connection to the devices. Most designers will recognize these guidelines as those they have employed with advanced bipolar logic families.

- Use multi-layer boards with V_{CC} and ground planes, with the device power pins soldered directly to the planes to insure the lowest power line impedances possible.
- Use decoupling capacitors for every device, usually 0.10 μF should be adequate. These capacitors should be located as close to the ground pin as possible.
- Do not use sockets or wirewrap boards whenever possible.
- Do not connect capacitors from the outputs directly to ground.

Decoupling Requirements

Fairchild Advanced CMOS, as with other high-performance, high-drive logic families, has special decoupling and printed circuit board layout requirements. Adhering to these requirements will ensure the maximum advantages are gained with FACT products.

Figure 4-13: Power Distribution Impedances

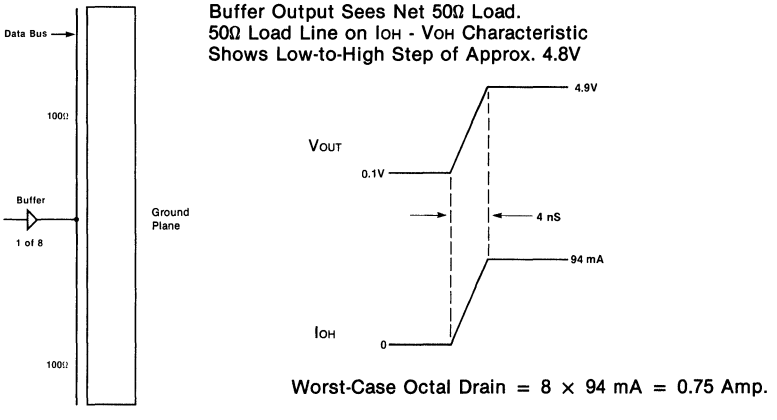


Local high frequency decoupling is required to supply power to the chip when it is transitioning from a LOW to a HIGH value. This power is necessary to charge the load capacitance or drive a line impedance. Figure 4-13 displays various Vcc and ground layout schemes along with associated impedances.

For most power distribution networks, the typical impedance is between 50 and 100 ohms. This impedance appears in series with the load impedance and will cause a droop in the Vcc at the part. This limits the available voltage swing at the local node, unless some form of decoupling is used. This drooping of rails will cause the rise and fall times to become elongated. Consider the example described in Figure 4-14 to calculate the amount of decoupling necessary. This circuit utilizes an 'AC240 driving a 100 ohm bus from a point somewhere in the middle.

4

Figure 4-14: Octal Buffer Driving a 100 Ohm Bus



Being in the middle of the bus, the driver will see two 100 ohm loads in parallel, or an effective impedance of 50 ohms. To switch the line from rail to rail, a drive of 94 mA is needed; more than 750 mA will be required if all eight lines switch at once. This instantaneous current requirement will generate a voltage across the impedance of the power lines, causing the actual Vcc at the chip to droop. This droop limits the voltage swing available to the driver. The net effect of the voltage droop will lengthen device rise and fall times and slow system operation. A local decoupling capacitor is required to act as a low impedance supply for the driver chip during high current conditions. It will maintain the voltage within acceptable limits and keep rise and fall times to a minimum. The necessary values for decoupling capacitors can be calculated with the formula given in Figure 4-15.

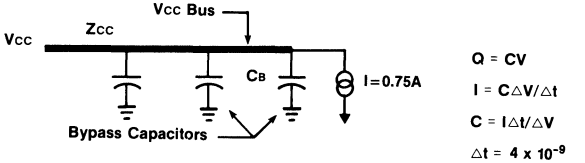
In this example, if the Vcc droop is to be kept below 0.1 V and the edge rate equals 4 ns, a 0.030 μf capacitor is needed.

It is good practice to distribute decoupling capacitors evenly through the logic, placing one capacitor for every package.

Capacitor Types

Decoupling capacitors need to be of the high K ceramic type with low equivalent series resistance (ESR), consisting primarily of series inductance and series resistance. Capacitors using 5ZU dielectric have suitable properties and make a good choice for decoupling capacitors; they offer minimum cost and effective performance.

Figure 4-15: Formula for Calculating Decoupling Capacitors



$Q = CV$

$I = C\Delta V/\Delta t$

$C = I\Delta t/\Delta V$

$\Delta t = 4 \times 10^{-9}$

Specify Vcc Droop = 0.1 V max.

$$C = \frac{0.750 \times 4 \times 10^{-9}}{0.1} = 30 \times 10^{-9} = 0.030\mu F$$

Select $C_B \geq 0.047\mu F$

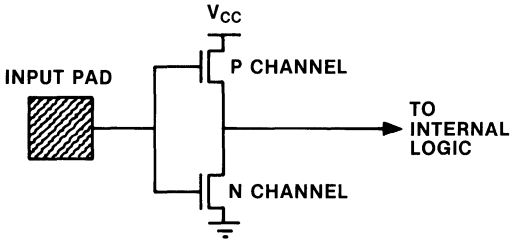
Place one decoupling capacitor adjacent to each package driving any transmission line and distribute others evenly thoughout the logic. One capacitor per three packages.

TTL-Compatible CMOS Designs Require Delta Icc Consideration

The FACT product line is comprised of two types of advanced CMOS circuits: 'AC and 'ACT devices. 'ACT indicates an advanced CMOS device with TTL-type input thresholds for direct replacement of LS and ALS circuits. As this 'ACT series is used to replace TTL, the Delta I_{CCT} specification must be considered; this spec may be confusing and misleading to the engineer unfamiliar with CMOS.

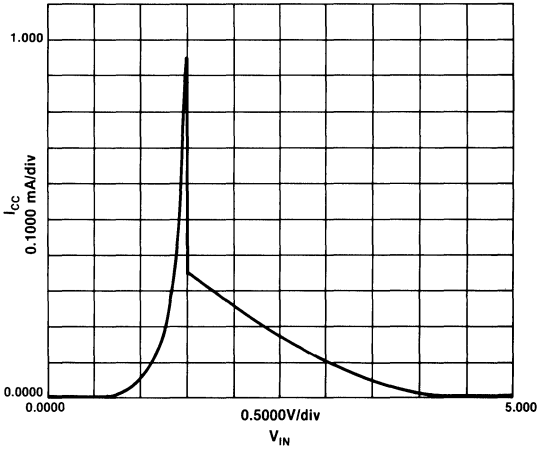
It is important to understand the concept of Delta I_{CCT} and how to use it within a design. First, consider where Delta I_{CCT} initiates. Most CMOS input structures are of the totem pole type with an n-channel transistor in a series with a p-channel transistor as illustrated below.

Figure 4-16: CMOS Input Structure



These two transistors can be modeled as variable resistors with resistances varying according to the input voltage. The resistance of an ON transistor is approximately 50 ohms while the resistance of an OFF transistor is generally greater than 5 Mohm. When the input to this structure is at either ground or Vcc, one transistor will be ON and one will be OFF. The total series resistance of this pair will be the combination of the two individual resistances, greater than 5 Mohm. The leakage current will then be less than 1 μA. When the input is between ground and Vcc, the resistance of the ON transistor will increase while the resistance of the OFF transistor will decrease. The net resistance will drop due to the much larger value of the OFF resistance. The total series resistance can be as low as 600 ohms. This reduction in series resistance of the input structure will cause a corresponding increase in Icc as current flows through the input structure. The following graph depicts typical Icc variance with input voltage for an 'ACT device.

Figure 4-17: Icc versus Input Voltage for 'ACT Devices



The Delta Icc specification is the increase in Icc. For each input at Vcc-2.1 V, the Delta Icc value should be added to the quiescent supply current to arrive at the circuit's worst-case static Icc value.

Fortunately, there are several factors which tend to reduce the increase in Icc per input. Most TTL devices will be able to drive FACT inputs well beyond the TTL output specification due to FACT's low input loading in a typical system. FAST logic outputs can drive 'ACT-type inputs down to 200 mV and up to 3.5 V. Additionally, the typical Icc increase per input will be less than the specified limit. As shown in the graph above, the Icc increase at Vcc-2.1 V is less than 200 μA in the typical system. Experiments have shown that the Icc of an 'ACT240 series device typically increases only 200 μA when all of the inputs are connected to a FAST device instead of ground or Vcc.

It is important when designing with FACT, as with any TTL-compatible CMOS technology, that the Delta Icc specification be considered. Designers should be aware of the spec's significance and that the data book specification is a worst-case value; most systems will see values that are much less.

Testing Advanced CMOS Devices with I/O Pins

There are more and more CMOS families becoming available which can replace TTL circuits. Although testing these new CMOS units with programs and fixtures which were developed for bipolar devices will yield acceptable results most of the time, there are some cases where this approach will cause the test engineer problems.

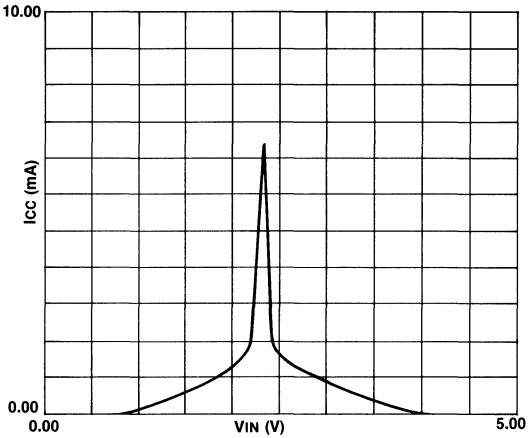
Such is the case with parts that have a bidirectional pin, exemplified by the '245 Octal Transceiver. If the proper testing methods are not followed, these types of parts may not pass those tests for Icc and input leakage currents, even when there is no fault with the devices.

CMOS circuits, unlike their bipolar counterparts, have static Icc specification orders of magnitude less than standard load currents. Most CMOS Icc specifications are usually less than 100 μA. When conducting an Icc test, greater care must be taken so that other currents will not mask the actual Icc of the device. These currents are usually sourced from the inputs and outputs.

Since the static Icc requirements of CMOS devices are so low, output load currents must be prevented from masking the current load of the device during an Icc test. Even a standard 500 ohm load resistor will sink 10 mA at 5 V, which is more than twice the Icc level being tested. Thus, most manufacturers will specify that all outputs must be unloaded during Icc tests.

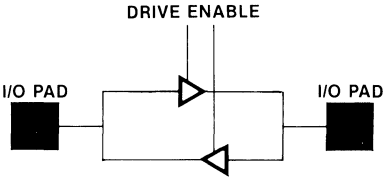
Another area of concern is identified when considering the inputs of the device. When the input is in the transition region, Icc can be several orders of magnitude greater than the specification. When the input voltage is in the transition region, both the n-channel and the p-channel transistors in the input totem-pole structure will be slightly ON, and a conduction is created from Vcc to ground. This conduction path leads to the increased Icc current seen in the Icc vs. VIN curve. When the input is at either rail, the input structure no longer conducts. Most Icc testing is done with all of the inputs tied to either Vcc or ground. If the inputs are allowed to float, they will typically float to the middle of the transition region, and the input structure will conduct an order of magnitude more current than the actual Icc of the device under test which is being measured by the tester.

Figure 4-18: Icc versus IIN



When testing the Icc of a CMOS '245, problems can arise depending upon how the test is conducted. Note the structure of the '245's I/O pins illustrated below.

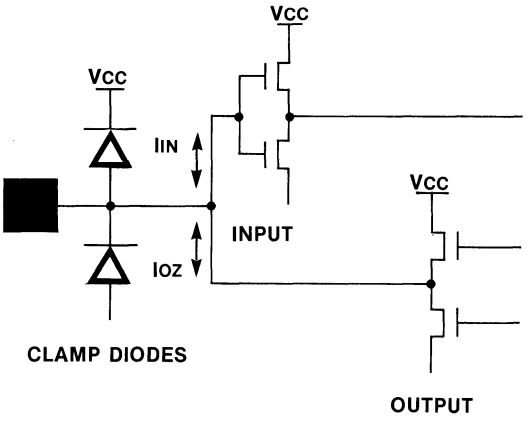
Figure 4-19: '245 I/O Structure



Each I/O pin is connected to both an input device and an output device. The pin can be viewed as having three states: input, output and output disabled. However, only two states actually exist.

The pin is either an input or an output. When testing the Icc of the device, the pins selected as outputs by the T/R signal must either be enabled and left open or be disabled and tied to either rail. If the output device is disabled and allowed to float, the input device will also float, and an excessive amount of current will flow from Vcc to ground. A simple rule to follow is to treat any output which is disabled as an input. This will help insure the integrity of an Icc test.

Figure 4-20: I/O Pin Internal Structure



Another area which might precipitate problems is the measurement of the leakages on I/O pins. The I/O pin internal structure is depicted below.

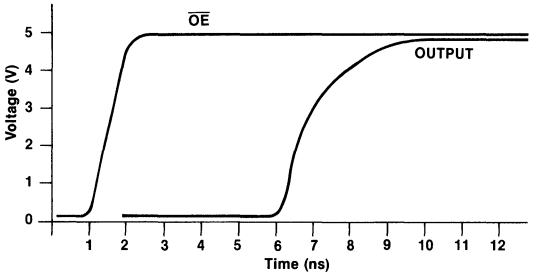
The pin is internally connected to both an input device and an output device; the limit for a leakage test must be the combined IIN specification of the input and the IOZ specification of the output. For FACT devices, IIN is specified at ± 1 μA while IOZ is specified at ± 5 μA. Combining these gives a limit of ±6 μA for I/O pins. Usually, I/O pins will show leakages that are less than the IOZ specification of the output alone.

Testing CMOS circuits is no more difficult than testing their bipolar counterparts. However, there are some areas of concern that will be new to many test engineers beginning to work with CMOS. Becoming familiar with and understanding these areas of concern prior to creating a test philosophy will avert many problems that might otherwise arise later.

Testing Disable Times of 3-State Outputs in a Transmission Line Environment

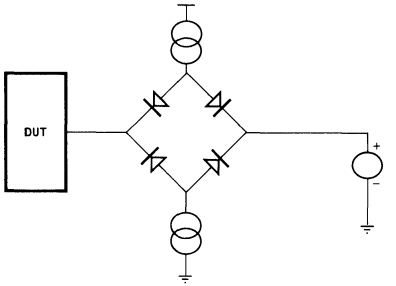
Traditionally, the disable time of a 3-state buffer has been measured from the 50% point on the disable input, to the 10% or 90% point on the output. On a bench test site, the output waveform is generated by a load capacitor and a pull-up/pull-down resistor. This circuit gives an RC charge/discharge curve as shown below.

Figure 4-21: Typical Bench 3-State Waveform



ATE test sites generally are unable to duplicate the bench test structure. ATE test loads differ because they are usually programmable and are situated away from the actual device. A commonly used test load is a Wheatstone bridge. The following figure illustrates the Wheatstone bridge test structure when used on the MCT 2000 test-system to duplicate the bench load.

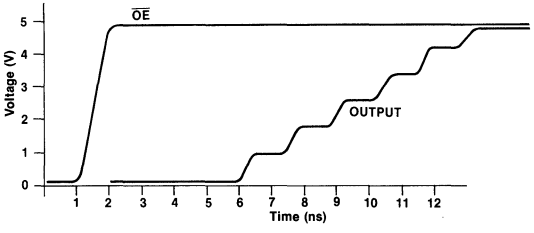
Figure 4-22: MCT Wheatstone Bridge Test Load



The voltage source provides a pull-up/pull-down voltage while the current sources provide I_{OH} and I_{OL}. When devices with slow output slew rates are tested with the ATE load, the resultant waveforms closely approximate the bench waveform, and a high degree of correlation can be achieved. However, when devices with high output slew rates are tested, different results are observed that make correlating tester results with bench results more difficult. This difference is due to the transmission line properties of the test equipment. Most disable tests are preceded by establishing a current flow through the output structure. Typically, these currents will be between 5 mA and 20 mA. The device is then disabled, and a comparator detects when the output has risen to the 10% or 90% level.

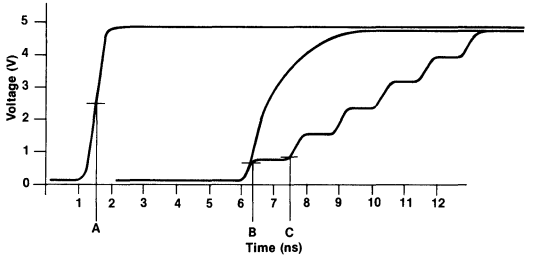
Consider the situation where the connection between the device under test (DUT) and the comparator is a transmission line. Visualize the device output as a switch; the effect is easier to see. There is current flowing through the line, and then the switch is opened. At the device end, the reflection coefficient changes from 0 to 1. This generates a current edge flowing back down the line equal to the current flowing in the line prior to the opening of the switch. This current wave will propagate down the line where it will encounter the high impedance tester load. This will cause the wave to be reflected back down the line toward the DUT. The current wave will continue to reflect in the transmission line until it reaches the voltage applied to the tester load. At this point, the current source impedance decreases and it will dissipate the current. A typical waveshape on a modern ATE is depicted in Figure 4-23.

Figure 4-23: Typical ATE 3-State Waveform

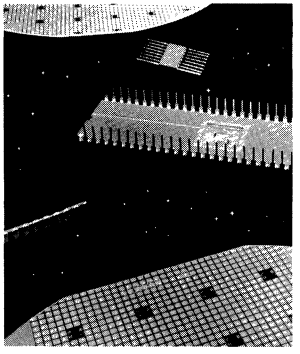


Transmission line theory states the voltage level of this current wave is equal to the current in the line times the impedance of the line. With typical currents as low as 5 mA and impedances of 50 to 60 ohms, this voltage step can be as minimal as 250 mV. If the comparator was programmed to the 10% point, it would be looking for a step of 550 mV at 5.5 V Vcc. Three reflections of the current pulse would be required before the comparator would detect the level. It is this added delay time caused by the transmission line environment of the ATE that may cause parts to fail customers' incoming tests, even though the device meets specifications. The figure below graphically shows this stepout.

Figure 4-24: Measurement Stepout



Point A represents the typical 50% measurement point on tester driven waveforms. Point B represents the point at which the delay time would be measured on a bench test fixture. Point C represents where the delay time could be measured on ATE fixtures. The delay time measured on the ATE fixture can vary from the bench measured delay time to some greater value, depending upon the voltage level that the tester is set. If the voltage level of the tester is close to voltage levels of the plateaus, the results may become non-repeatable.



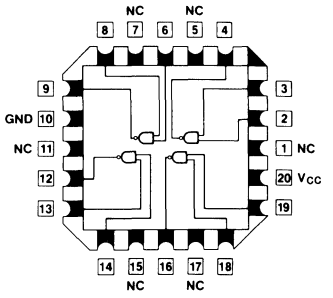
54AC/74AC00 • 54ACT/74ACT00

Quad 2-Input NAND Gate

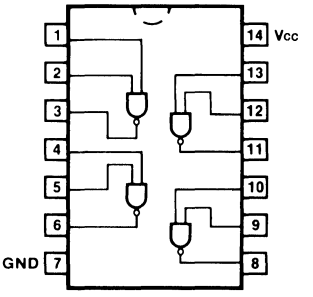
- **Outputs Source/Sink 24 mA**
- **'ACT00 has TTL-Compatible Inputs**

Ordering Code: See Section 6

Connection Diagrams



Pin Assignment for LCC



Pin Assignment for DIP, Flatpak and SOIC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	80	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT00)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.0	7.0	9.5	1.0	11.0	1.0	10.0	ns	3-5
		5.0	1.0	6.0	8.0	1.0	8.5	1.0	8.5		
t_{PHL}	Propagation Delay	3.3	1.0	5.5	8.0	1.0	9.0	1.0	8.5	ns	3-5
		5.0	1.0	4.5	6.5	1.0	7.0	1.0	7.0		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0	1.0	5.5	9.0	1.0	9.5	1.0	9.5	ns	3-5
t_{PHL}	Propagation Delay	5.0	1.0	4.0	7.0	1.0	8.0	1.0	8.0	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	30.0	pF	$V_{CC} = 5.5$ V

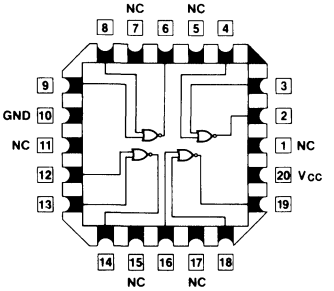
54AC/74AC02

Quad 2-Input NOR Gate

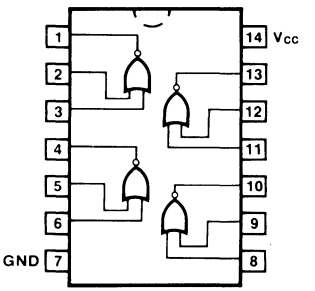
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 6

Connection Diagrams



Pin Assignment for LCC



Pin Assignment for DIP, Flatpak and SOIC

5

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	80	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3 5.0	1.0 1.0	5.0 4.0	7.5 6.0	1.0 1.0	9.0 7.0	1.0 1.0	8.0 6.5	ns	3-5
t_{PHL}	Propagation Delay	3.3 5.0	1.0 1.0	5.0 4.5	7.5 6.5	1.0 1.0	9.0 7.5	1.0 1.0	8.0 7.0	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	30.0	pF	$V_{CC} = 5.5$ V

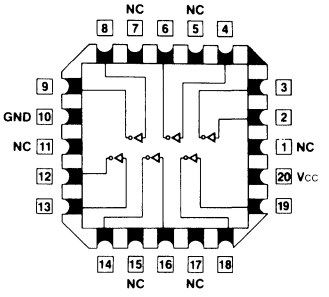
54AC/74AC04 • 54ACT/74ACT04

Hex Inverter

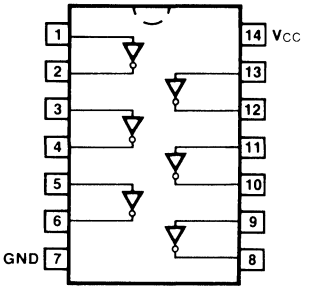
- **Outputs Source/Sink 24 mA**
- **'ACT04 has TTL-Compatible Inputs**

Ordering Code: See Section 6

Connection Diagrams



Pin Assignment for LCC



Pin Assignment for DIP, Flatpak and SOIC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	80	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT04)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.0	4.5	9.0	1.0	11.0	1.0	10.0	ns	3-5
		5.0	1.0	4.0	7.0	1.0	8.5	1.0	7.5		
t_{PHL}	Propagation Delay	3.3	1.0	4.5	8.5	1.0	10.0	1.0	9.5	ns	3-5
		5.0	1.0	3.5	6.5	1.0	7.5	1.0	7.0		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0		4.5						ns	3-6
t_{PHL}	Propagation Delay	5.0		3.9						ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	30.0	pF	$V_{CC} = 5.5$ V

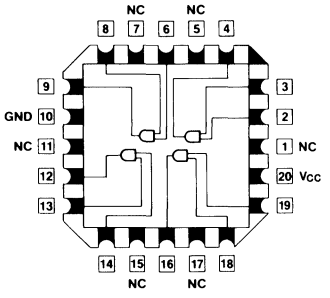
54AC/74AC08 • 54ACT/74ACT08

Quad 2-Input AND Gate

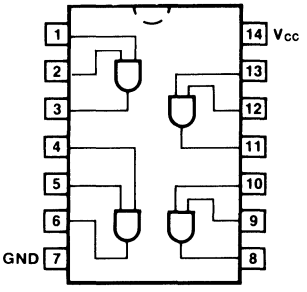
- **Outputs Source/Sink 24 mA**
- **'ACT08 has TTL-Compatible Inputs**

Ordering Code: See Section 6

Connection Diagrams



Pin Assignment for LCC



Pin Assignment for DIP, Flatpak and SOIC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	80	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT08)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.0	7.5	9.5	1.0	12.0	1.0	10.0	ns	3-5
		5.0	1.0	5.5	7.5	1.0	9.0	1.0	8.5		
t_{PHL}	Propagation Delay	3.3	1.0	7.0	8.5	1.0	11.5	1.0	9.0	ns	3-5
		5.0	1.0	5.5	7.0	1.0	8.5	1.0	7.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0		6.5					ns	3-5
t_{PHL}	Propagation Delay	5.0		6.7					ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	20.0	pF	$V_{CC} = 5.5$ V

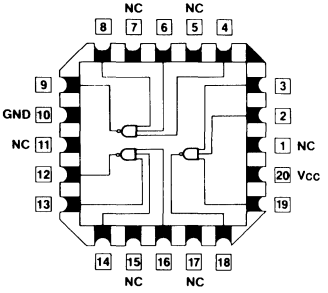
54AC/74AC10

Triple 3-Input NAND Gate

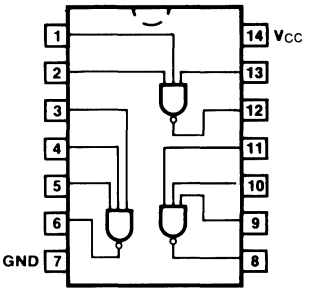
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 6

Connection Diagrams



Pin Assignment for LCC



Pin Assignment for DIP, Flatpak and SOIC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	80	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.0	6.0	9.5	1.0	11.0	1.0	10.5	ns	3-5
		5.0	1.0	4.5	7.0	1.0	8.5	1.0	8.0		
t_{PHL}	Propagation Delay	3.3	1.0	5.5	8.5	1.0	10.0	1.0	10.0	ns	3-5
		5.0	1.0	4.0	6.0	1.0	7.0	1.0	6.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	25.0	pF	$V_{CC} = 5.5$ V

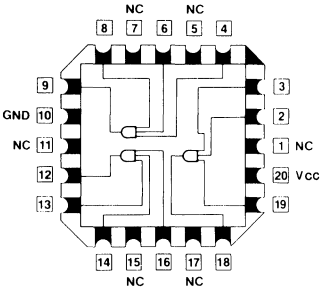
54AC/74AC11

Triple 3-Input AND Gate

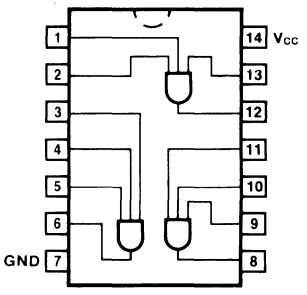
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 6

Connection Diagrams



Pin Assignment for LCC



Pin Assignment for DIP, Flatpak and SOIC

5

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	80	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3 5.0	1.0 1.0	5.5 4.0	9.5 8.0	1.0 1.0	11.0 8.5	1.0 1.0	10.0 8.5	ns	3-5
t_{PHL}	Propagation Delay	3.3 5.0	1.0 1.0	5.5 4.0	8.5 7.0	1.0 1.0	10.5 8.0	1.0 1.0	9.5 7.5	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	20.0	pF	$V_{CC} = 5.5$ V

54AC/74AC14 • 54ACT/74ACT14

Hex Inverter Schmitt Trigger

Description

The 'AC/'ACT14 contains six logic inverters which accept standard CMOS input signals (TTL levels for 'ACT14) and provide standard CMOS output levels. They are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals. In addition, they have a greater noise margin than conventional inverters.

The 'AC/'ACT14 has hysteresis between the positive-going and negative-going input thresholds (typically 1.0 V) which is determined internally by transistor ratios and is essentially insensitive to temperature and supply voltage variations.

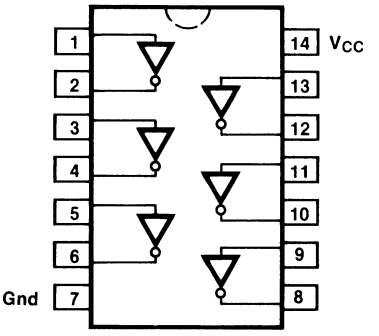
- **Outputs Source/Sink 24 mA**
- **'ACT14 has TTL-Compatible Inputs**

Ordering Code: See Section 6

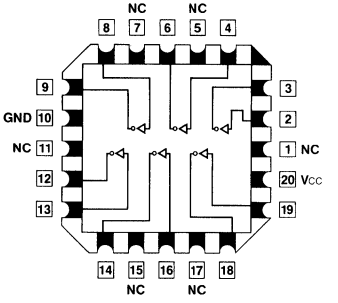
Function Table

Input	Output
A	O
L	H
H	L

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

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DC Characteristics (unless otherwise specified)

Symbol	Parameter	Vcc (V)	54AC	54ACT	74AC	74ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current		80	80	40	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current		4.0	4.0	4.0	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT14)			1.6		1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case
V_{t+}	Maximum Positive Threshold	3.0 4.5 5.5	2.2 3.2 3.9	2.0	2.2 3.2 3.9	2.0	V	T_A = Worst Case
V_{t-}	Minimum Negative Threshold	3.0 4.5 5.5	0.5 0.9 1.1	0.8	0.5 0.9 1.1	0.8	V	T_A = Worst Case
$V_{h(max)}$	Maximum Hysteresis	3.0 4.5 5.5	1.2 1.4 1.6	1.2	1.2 1.4 1.6	1.2	V	T_A = Worst Case
$V_{h(min)}$	Minimum Hysteresis	3.0 4.5 5.5	0.3 0.4 0.5	0.4	0.3 0.4 0.5	0.4	V	T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3 5.0	1.0 1.0	9.5 7.0	13.5 10.0	1.0 1.0	16.0 12.0	1.0 1.0	15.0 11.0	ns	3-5
t_{PHL}	Propagation Delay	3.3 5.0	1.0 1.0	7.5 6.0	11.5 8.5	1.0 1.0	14.0 10.0	1.0 1.0	13.0 9.5	ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0		7.4						ns	3-5
t_{PHL}	Propagation Delay	5.0		8.6						ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

5

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	25.0	pF	$V_{CC} = 5.5$ V

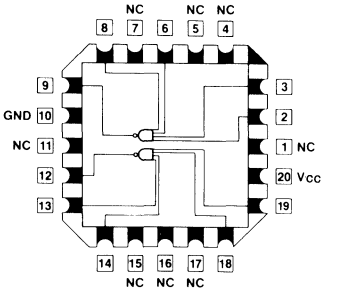
54AC/74AC20

Dual 4-Input NAND Gate

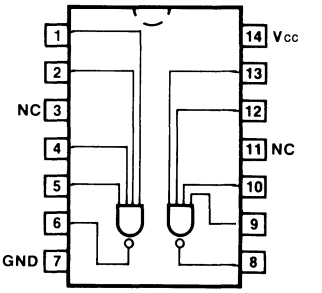
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 6

Connection Diagrams



Pin Assignment for LCC



Pin Assignment for DIP, Flatpak and SOIC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	80	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.0	6.0	8.5	1.0	11.0	1.0	10.0	ns	3-5
		5.0	1.0	5.0	7.0	1.0	8.5	1.0	8.0		
t_{PHL}	Propagation Delay	3.3	1.0	5.0	7.0	1.0	10.0	1.0	9.0	ns	3-5
		5.0	1.0	4.0	6.0	1.0	7.0	1.0	7.0		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	40.0	pF	$V_{CC} = 5.5$ V

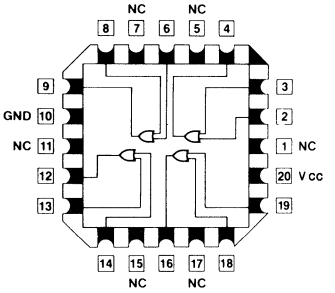
54AC/74AC32 • 54ACT/74ACT32

Quad 2-Input OR Gate

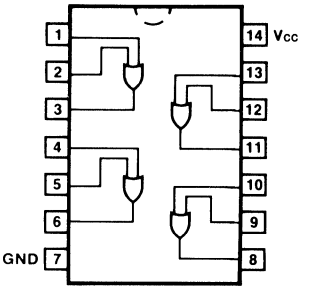
- **Outputs Source/Sink 24 mA**
- **'ACT32 has TTL-Compatible Inputs**

Ordering Code: See Section 6

Connection Diagrams



Pin Assignment for LCC



Pin Assignment for DIP, Flatpak and SOIC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	80	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT32)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	3.3	1.0	7.0	9.0	1.0	12.0	1.0	10.0	ns	3-5
		5.0	1.0	5.5	7.5	1.0	9.0	1.0	8.5		
t_{PHL}	Propagation Delay	3.3	1.0	7.0	8.5	1.0	11.5	1.0	9.0	ns	3-5
		5.0	1.0	5.0	7.0	1.0	8.5	1.0	7.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay	5.0		7.2						ns	3-5
t_{PHL}	Propagation Delay	5.0		6.6						ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	20.0	pF	$V_{CC} = 5.5$ V

5

54AC/74AC74 • 54ACT/74ACT74

Dual D-Type Positive Edge-Triggered Flip-Flop

Description

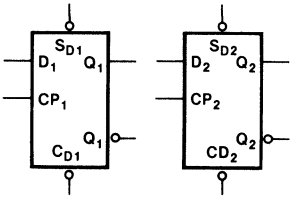
The 'AC/'ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:
- LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

- **Outputs Source/Sink 24 mA**
- **'ACT74 has TTL-Compatible Inputs**

Ordering Code: See Section 6

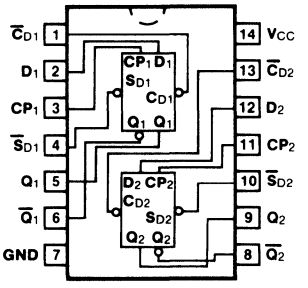
Logic Symbol



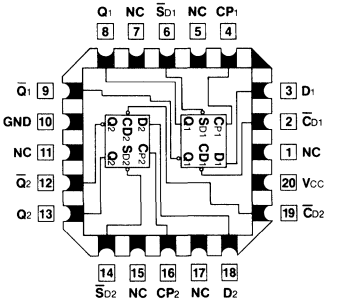
Pin Names

D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



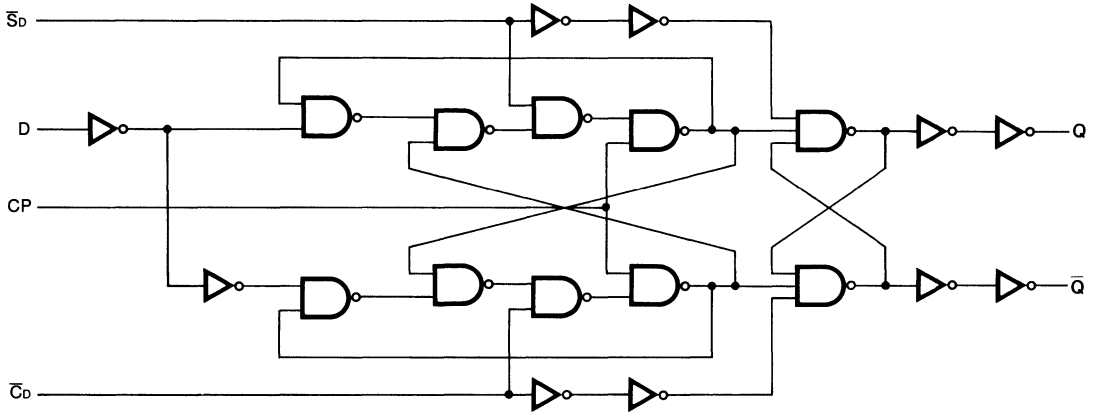
Pin Assignment for LCC

Truth Table (Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	⌐	H	H	L
H	H	⌐	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
Q_0($\overline{Q}_0$) = Previous Q($\overline{Q}$) before LOW-to-HIGH Transition of Clock

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	80	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT74)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	100 140	125 160		95 95		95 125		MHz	3-3
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	12.0 9.0	1.0 1.0	14.5 10.5	1.0 1.0	13.0 10.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	10.5 8.0	12.0 9.5	1.0 1.0	20.0 14.5	1.0 1.0	13.5 10.5	ns	3-6
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	13.5 10.0	1.0 1.0	17.5 11.0	1.0 1.0	16.0 10.5	ns	3-6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	14.0 10.0	1.0 1.0	16.0 11.5	1.0 1.0	14.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW D_n to CP_n	3.3 5.0	1.5 1.0	4.0 3.0	5.0 3.5	4.5 3.0	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP_n	3.3 5.0	−2.0 −1.5	0 0	0.5 0.5	0 0	ns	3-9
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	3.3 5.0	3.0 2.5	5.5 4.5	8.0 5.5	7.0 5.0	ns	3-6
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3 5.0	−2.5 −2.0	0 0	0.5 0.5	0 0	ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	210		95		125		MHz	3-3
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	5.5	9.5	1.0	11.5	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	6.0	10.0	1.0	12.5	1.0	11.5	ns	3-6
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	7.5	11.0	1.0	14.0	1.0	13.0	ns	3-6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	6.0	10.0	1.0	12.0	1.0	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW D_n to CP_n	5.0	1.0	3.0	4.0	3.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP_n	5.0	−0.5	1.0	1.0	1.0	ns	3-9
t_w	CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ Pulse Width	5.0	3.0	5.0	6.5	6.0	ns	3-6
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	−2.5	0	0	0	ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	35.0	pF	$V_{CC} = 5.5$ V

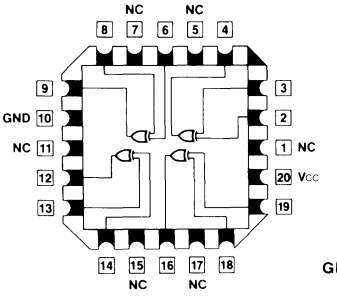
54AC/74AC86

Quad 2-Input Exclusive-OR Gate

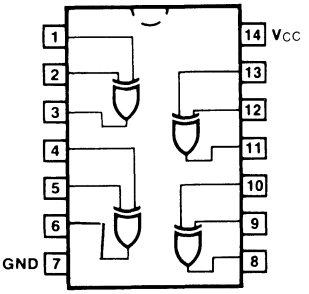
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 6

Connection Diagrams



Pin Assignment for LCC



Pin Assignment for DIP, Flatpak and SOIC

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	80	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay Inputs to Outputs	3.3 5.0		6.0 4.5						ns	3-5
t_{PLH}	Propagation Delay Inputs to Outputs	3.3 5.0		6.5 4.5						ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC109 • 54ACT/74ACT109

Dual J$\overline{K}$ Positive Edge-Triggered Flip-Flop

Description

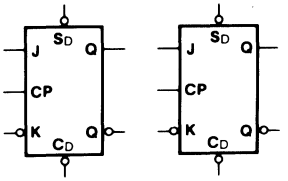
The 'AC/'ACT109 consists of two high-speed completely independent transition clocked J$\overline{K}$ flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The J$\overline{K}$ design allows operation as a D flip-flop (refer to 'AC/'ACT74 data sheet) by connecting the J and $\overline{K}$ inputs together.

Asynchronous Inputs:
- LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

- **Outputs Source/Sink 24 mA**
- **'ACT109 has TTL-Compatible Inputs**

Ordering Code: See Section 6

Logic Symbol

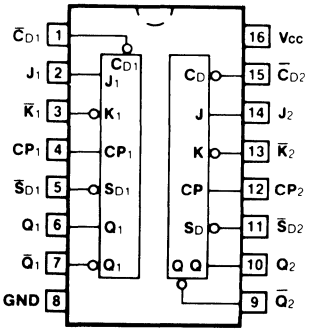


Truth Table

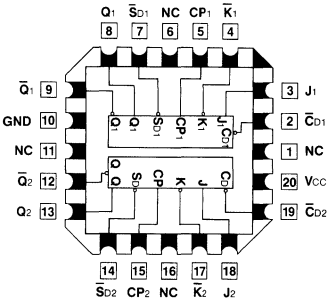
Inputs					Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$-
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	⌐	L	L	L	H
H	H	⌐	H	L	Toggle	
H	H	⌐	L	H	Q_0	$\overline{Q}_0$-
H	H	⌐	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$-

H = HIGH Voltage Level
L = LOW Voltage Level
⌐ = LOW-to-HIGH Transition
X = Immaterial
$Q_0(\overline{Q}_0)$ = Previous $Q_0(\overline{Q}_0)$ before LOW-to-HIGH Transition of Clock

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



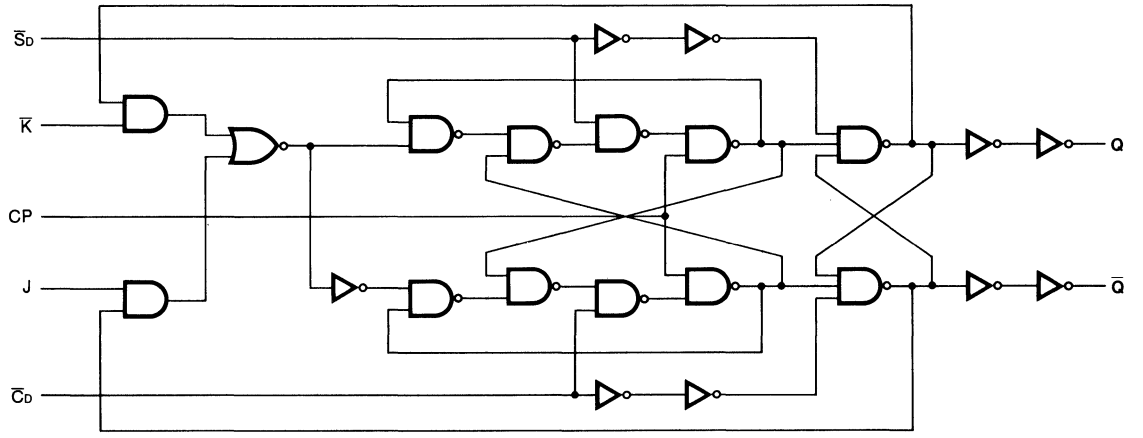
Pin Assignment for LCC

Pin Names

J_1, J_2, $\overline{K}_1$, $\overline{K}_2$	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, Q_2, $\overline{Q}_1$, $\overline{Q}_2$	Outputs

5

Logic Diagram (one half shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	80	40	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	4.0	4.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT109)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	125 150	150 175		90 95		100 125		MHz	3-3
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	13.5 10.0	1.0 1.0	17.5 11.0	1.0 1.0	16.0 10.5	ns	3-6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	14.0 10.0	1.0 1.0	16.0 11.5	1.0 1.0	14.5 10.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	8.0 6.0	12.0 9.0	1.0 1.0	14.5 10.5	1.0 1.0	13.0 10.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	3.3 5.0	1.0 1.0	10.0 7.5	12.0 9.5	1.0 1.0	20.0 14.5	1.0 1.0	13.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3 5.0	3.5 2.0	6.5 4.5	8.0 5.5	7.5 5.0	ns	3-9
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	3.3 5.0	−1.5 −0.5	0 0.5	1.0 1.0	0 0.5	ns	3-9
t_w	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	3.3 5.0	2.0 2.0	4.0 3.5	8.0 5.5	4.5 3.5	ns	3-6
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	3.3 5.0	−2.5 −1.5	0 0	0 0	0 0	ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	145	210		95		125		MHz	3-3
t_{PLH}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	7.0	11.0	1.0	14.0	1.0	13.0	ns	3-6
t_{PHL}	Propagation Delay CP_n to Q_n or $\overline{Q}_n$	5.0	1.0	6.0	10.0	1.0	12.0	1.0	11.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	5.5	9.5	1.0	11.5	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to Q_n or $\overline{Q}_n$	5.0	1.0	6.0	10.0	1.0	12.5	1.0	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	0.5	2.0	2.5	2.5	ns	3-9
t_h	Hold Time, HIGH or LOW J_n or $\overline{K}_n$ to CP_n	5.0	0	2.0	2.0	2.0	ns	3-9
t_w	Pulse Width CP_n or $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$	5.0	3.0	5.0	6.5	6.0	ns	3-6
t_{rec}	Recovery Time $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to CP	5.0	−2.5	0	0	0	ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	35.0	pF	$V_{CC} = 5.5$ V

54AC/74AC138 • 54ACT/74ACT138

1-of-8 Decoder/Demultiplexer

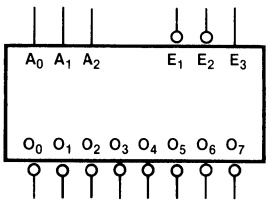
Description

The 'AC/'ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'AC/'ACT138 devices or a 1-of-32 decoder using four 'AC/'ACT138 devices and one inverter.

- **Demultiplexing Capability**
- **Multiple Input Enable for Easy Expansion**
- **Active LOW Mutually Exclusive Outputs**
- **Outputs Source/Sink 24 mA**
- **'ACT138 has TTL-Compatible Inputs**

Ordering Code: See Section 6

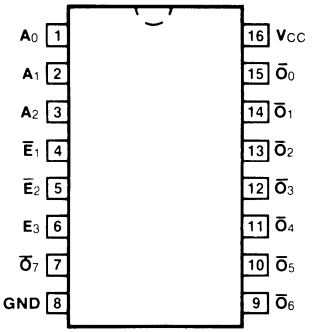
Logic Symbol



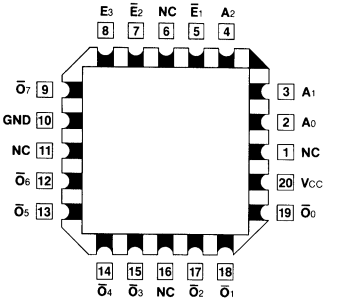
Pin Names

A_0 - A_2	Address Inputs
$\overline{E}_1$ - $\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$ - $\overline{O}_7$	Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

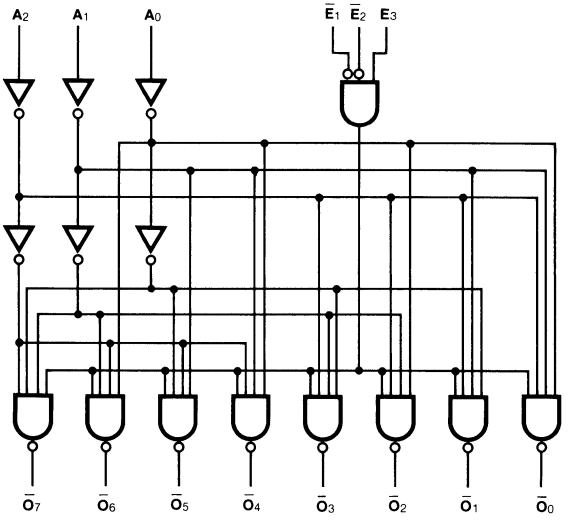
The 'AC/'ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$ - $\overline{O}_7$). The 'AC/'ACT138 features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enabled function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'AC/'ACT138 devices and one inverter (See Figure a). The 'AC/'ACT138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

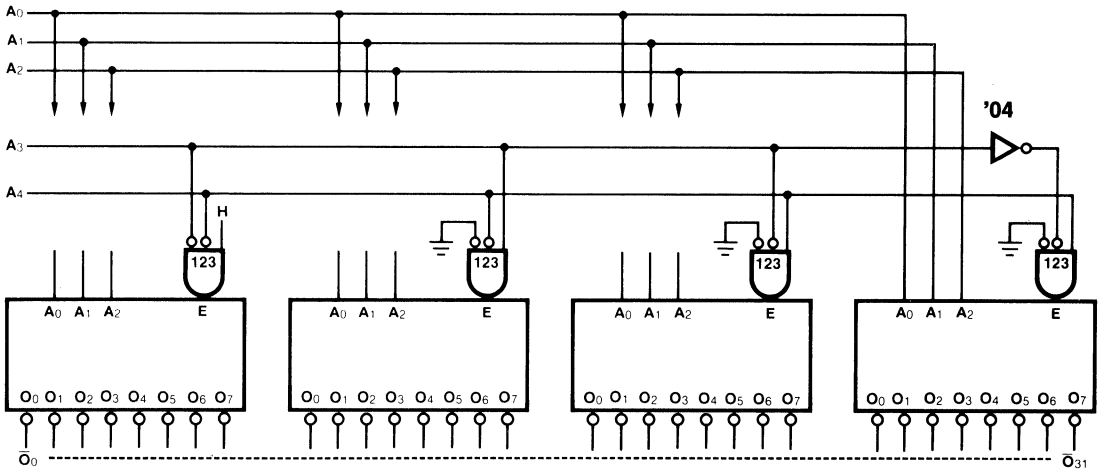
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure a: Expansion to 1-of-32 Decoding



DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT138)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.3	1.0	8.5	13.0	1.0	16.0	1.0	15.0	ns	3-6
		5.0	1.0	6.5	9.5	1.0	12.0	1.0	10.5		
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.3	1.0	8.0	12.5	1.0	15.0	1.0	14.0	ns	3-6
		5.0	1.0	6.0	9.0	1.0	11.5	1.0	10.5		
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.3	1.0	11.0	15.0	1.0	16.5	1.0	16.0	ns	3-6
		5.0	1.0	8.0	11.0	1.0	13.0	1.0	12.0		
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.3	1.0	9.5	13.5	1.0	15.5	1.0	15.0	ns	3-6
		5.0	1.0	7.0	9.5	1.0	12.0	1.0	10.5		
t_{PLH}	Propagation Delay E_3 to $\overline{O}_n$	3.3	1.0	11.0	15.5	1.0	17.0	1.0	16.5	ns	3-6
		5.0	1.0	8.0	11.0	1.0	13.5	1.0	12.5		
t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$	3.3	1.0	8.5	13.0	1.0	15.0	1.0	14.0	ns	3-6
		5.0	1.0	6.0	8.0	1.0	11.0	1.0	9.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.0	7.0	10.5	1.0	12.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.0	6.5	10.5	1.0	12.5	1.0	11.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.0	8.0	11.5	1.0	13.5	1.0	12.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.0	7.5	11.5	1.0	12.5	1.0	12.5	ns	3-6
t_{PLH}	Propagation Delay E_3 to $\overline{O}_n$	5.0	1.0	8.0	12.0	1.0	14.0	1.0	13.0	ns	3-6
t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$	5.0	1.0	6.5	10.5	1.0	12.0	1.0	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	60.0	pF	$V_{CC} = 5.5$ V

54AC/74AC139 • 54ACT/74ACT139

Dual 1-of-4 Decoder/Demultiplexer

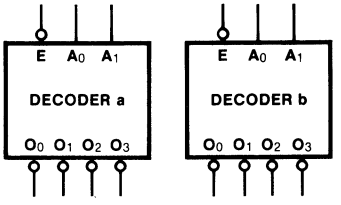
Description

The 'AC/'ACT139 is a high-speed, dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually-exclusive active-LOW outputs. Each decoder has an active-LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the 'AC/'ACT139 can be used as a function generator providing all four minterms of two variables.

- **Multifunction Capability**
- **Two Completely Independent 1-of-4 Decoders**
- **Active LOW Mutually Exclusive Outputs**
- **Outputs Source/Sink 24 mA**
- **'ACT139 has TTL-Compatible Inputs**

Ordering Code: See Section 6

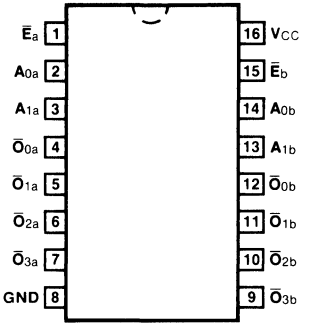
Logic Symbol



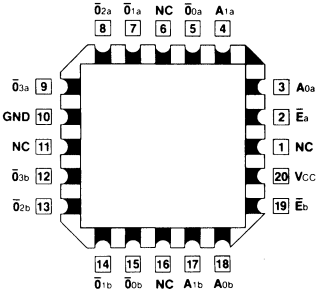
Pin Names

A_0, A_1	Address Inputs
$\overline{E}$	Enable Inputs
$\overline{O}_0$ - $\overline{O}_3$	Outputs

Connection Diagrams



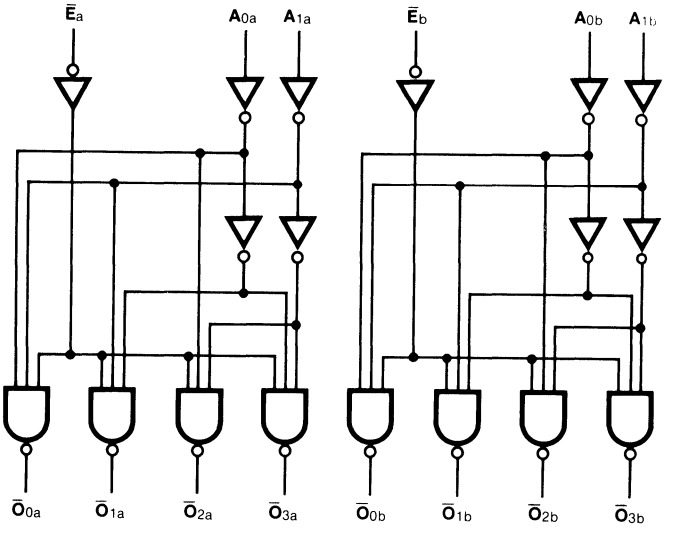
Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

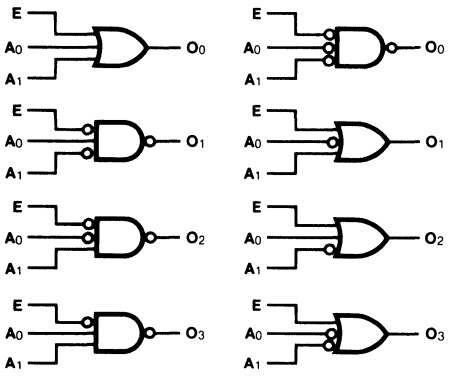
The 'AC/'ACT139 is a high-speed dual 1-of-4 decoder/demultiplexer. The device has two independent decoders, each of which accepts two binary weighted inputs (A_0 - A_1) and provides four mutually exclusive active-LOW outputs ($\overline{O}_0$ - $\overline{O}_3$). Each decoder has an active-LOW enable ($\overline{E}$). When $\overline{E}$ is HIGH all outputs are forced HIGH. The enable can be used as the data input for a 4-output demultiplexer application. Each half of the 'AC/'ACT139 generates all four minterms of two variables. These four minterms are useful in some applications, replacing multiple gate functions as shown in Figure a, and thereby reducing the number of packages required in a logic network.

Truth Table

Inputs			Outputs			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Figure a: Gate Functions (each half)



DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT139)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.3	1.0	8.0	11.5	1.0	14.5	1.0	13.0	ns	3-6
		5.0	1.0	6.5	8.5	1.0	11.0	1.0	9.5		
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.3	1.0	7.0	10.0	1.0	12.5	1.0	11.0	ns	3-6
		5.0	1.0	5.5	7.5	1.0	10.0	1.0	8.5		
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	3.3	1.0	9.5	12.0	1.0	14.5	1.0	13.0	ns	3-6
		5.0	1.0	7.0	8.5	1.0	11.0	1.0	10.0		
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	3.3	1.0	8.0	10.0	1.0	12.5	1.0	11.0	ns	3-6
		5.0	1.0	6.0	7.5	1.0	10.0	1.0	8.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.0	6.0	8.5	1.0	12.0	1.0	9.5	ns	3-6
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.0	6.0	9.5	1.0	11.0	1.0	10.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	5.0	1.0	7.0	10.0	1.0	12.5	1.0	11.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{O}_n$	5.0	1.0	7.0	9.5	1.0	12.0	1.0	10.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	40.0	pF	$V_{CC} = 5.5$ V

54AC/74AC151 • 54ACT/74ACT151

1-of-8 Decoder/Demultiplexer

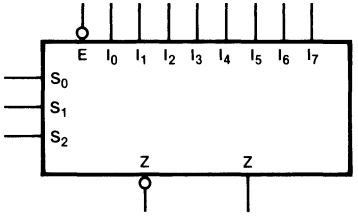
Description

The 'AC/'ACT151 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one line of data from up to eight sources. The 'AC/'ACT151 can be used as a universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

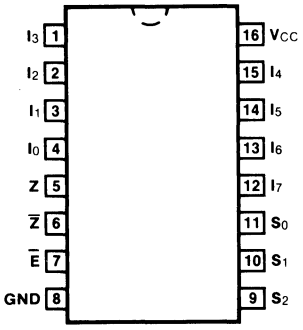
- **Outputs Source/Sink 24 mA**
- **'ACT151 has TTL-Compatible Inputs**

Ordering Code: See Section 6

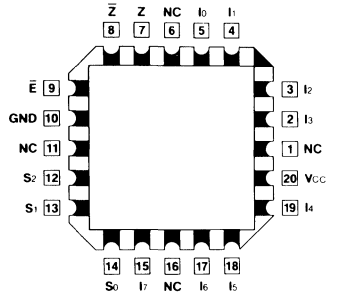
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Truth Table

Inputs				Outputs	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Pin Names

I_0 - I_7	Data Inputs
S_0 - S_2	Select Inputs
$\overline{E}$	Enable Input
Z	Data Output
$\overline{Z}$	Inverted Data Output

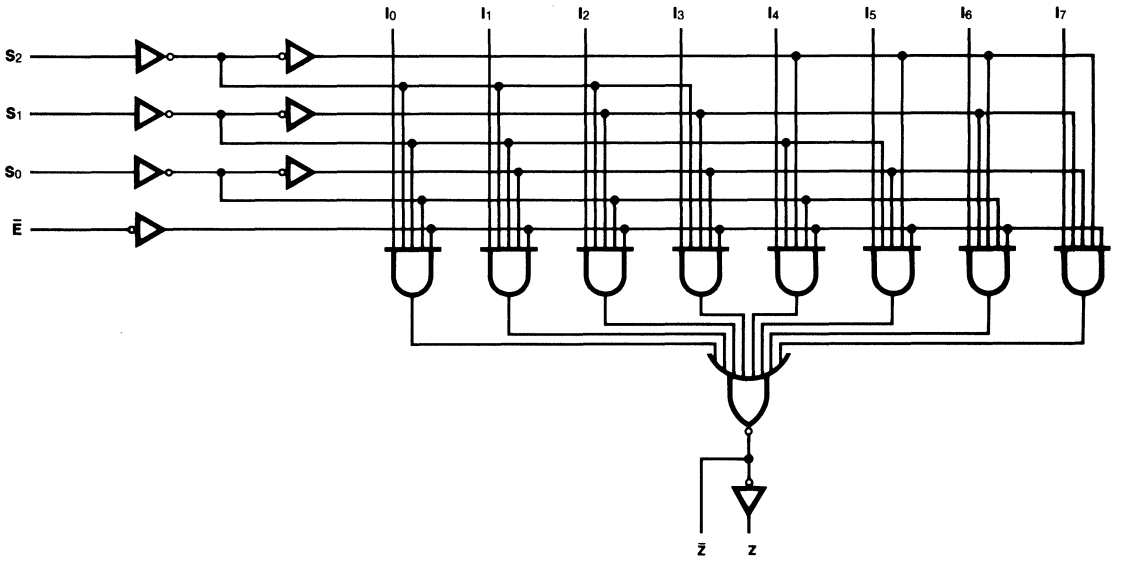
Functional Description

The 'AC/'ACT151 is a logic implementation of a single pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Enable input ($\overline{E}$) is active LOW. When it is not activated, the complementary output is HIGH and the true output is LOW regardless of all other inputs. The logic function provided at the output is:

$$Z = \overline{E} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

The 'AC/'ACT151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the 'AC/'ACT151 can provide any logic function of four variables and its complement.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT151)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

5

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	1.0	11.5	18.0	1.0	22.0	1.0	20.0	ns	3-6
		5.0	1.0	8.5	13.0	1.0	15.5	1.0	15.0		
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	1.0	12.0	18.0	1.0	22.0	1.0	20.0	ns	3-6
		5.0	1.0	8.5	13.0	1.0	15.5	1.0	15.0		
t_{PLH}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	3.3	1.0	8.0	13.0	1.0	15.5	1.0	14.0	ns	3-6
		5.0	1.0	6.0	10.0	1.0	12.0	1.0	11.0		
t_{PHL}	Propagation Delay $\overline{E}$ to Z or $\overline{Z}$	3.3	1.0	8.5	13.0	1.0	15.5	1.0	14.0	ns	3-6
		5.0	1.0	6.5	10.0	1.0	12.0	1.0	11.0		
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	1.0	9.5	14.0	1.0	16.0	1.0	15.5	ns	3-5
		5.0	1.0	7.0	10.5	1.0	12.0	1.0	11.0		
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	1.0	9.5	15.0	1.0	18.0	1.0	16.0	ns	3-5
		5.0	1.0	7.0	11.0	1.0	13.0	1.0	12.0		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z	5.0	1.0	12.5	15.5			1.0	17.0	ns	3-6
t_{PHL}	Propagation Delay S_n to Z	5.0	1.0	12.5	15.5			1.0	16.5	ns	3-6
t_{PLH}	Propagation Delay S_n to $\overline{Z}$	5.0	1.0	12.5	15.0			1.0	16.5	ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}$	5.0	1.0	12.5	16.5			1.0	18.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}$ to Z	5.0	1.0	10.0	9.5			1.0	10.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}$ to Z	5.0	1.0	10.5	9.0			1.0	10.0	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}$ to $\overline{Z}$	5.0	1.0	10.0	8.5			1.0	9.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}$	5.0	1.0	10.5	10.0			1.0	10.5	ns	3-6
t_{PLH}	Propagation Delay I_n to Z	5.0	1.0	11.0	11.5			1.0	12.5	ns	3-6
t_{PHL}	Propagation Delay I_n to Z	5.0	1.0	11.0	12.0			1.0	13.5	ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}$	5.0	1.0	11.0	12.0			1.0	13.0	ns	3-6
t_{PHL}	Propagation Delay I_n to $\overline{Z}$	5.0	1.0	11.0	12.5			1.0	14.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	70.0	pF	$V_{CC} = 5.5$ V

54AC/74AC153 • 54ACT/74ACT153

Dual 4-Input Multiplexer

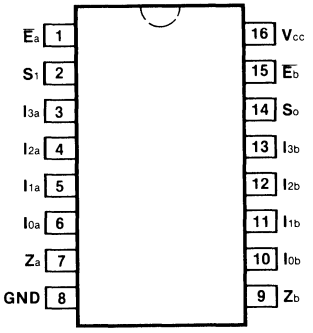
Description

The 'AC/'ACT153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the 'AC/'ACT153 can act as a function generator and generate any two functions of three variables.

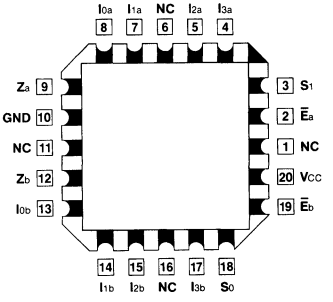
- **Outputs Source/Sink 24 mA**
- **'ACT153 has TTL-Compatible Inputs**

Ordering Code: See Section 6

Connection Diagrams

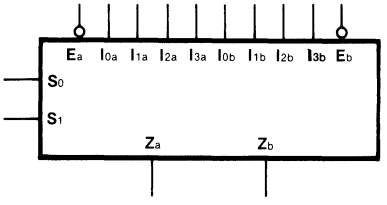


Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Logic Symbol



Pin Names

I_{0a} - I_{3a}	Side A Data Inputs
I_{0b} - I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{E}_a$	Side A Enable Input
$\overline{E}_b$	Side B Enable Input
Z_a	Side A Output
Z_b	Side B Output

5

Functional Description

The 'AC/'ACT153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The 'AC/'ACT153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

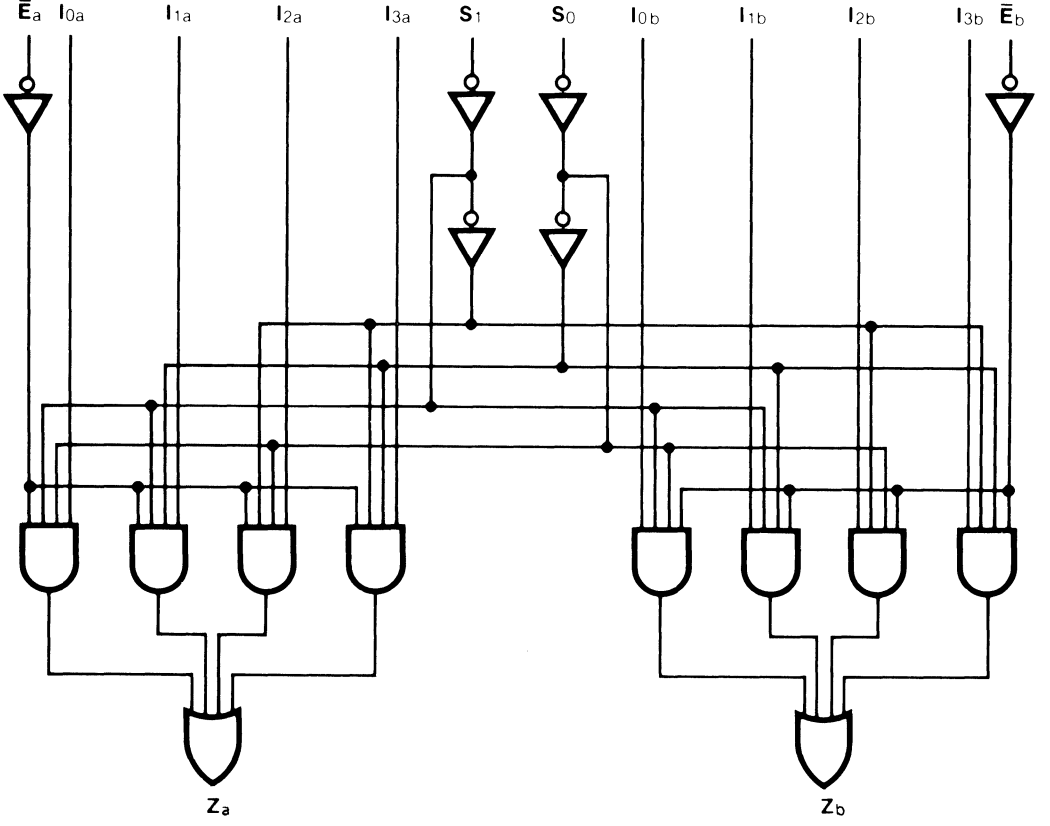
$$Z_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$
$$Z_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

Truth Table

Select Inputs		Inputs (a or b)					Output
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Z
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A =$ Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT153)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, $T_A =$ Worst Case

5

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	3.3	1.0	9.5	15.0	1.0	19.5	1.0	17.5	ns	3-6
		5.0	1.0	6.5	11.0	1.0	14.0	1.0	12.5		
t_{PHL}	Propagation Delay S_n to Z_n	3.3	1.0	8.5	14.5	1.0	18.0	1.0	16.5	ns	3-6
		5.0	1.0	6.5	11.0	1.0	13.5	1.0	12.0		
t_{PLH}	Propagation Delay $\overline{E}_n$ to Z_n	3.3	1.0	8.0	13.5	1.0	16.5	1.0	16.0	ns	3-6
		5.0	1.0	5.5	9.5	1.0	12.5	1.0	11.0		
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	3.3	1.0	7.0	11.0	1.0	14.0	1.0	12.5	ns	3-6
		5.0	1.0	5.0	8.0	1.0	10.0	1.0	9.0		
t_{PLH}	Propagation Delay I_n to Z_n	3.3	1.0	7.5	12.5	1.0	16.0	1.0	14.5	ns	3-5
		5.0	1.0	5.5	9.0	1.0	11.5	1.0	10.5		
t_{PHL}	Propagation Delay I_n to Z_n	3.3	1.0	7.0	11.5	1.0	14.5	1.0	13.0	ns	3-5
		5.0	1.0	5.0	8.5	1.0	10.5	1.0	10.0		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	5.0	1.0	7.0	11.5	1.0	15.0	1.0	13.5	ns	3-6
t_{PHL}	Propagation Delay S_n to Z_n	5.0	1.0	7.0	11.5	1.0	14.5	1.0	13.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	1.0	6.5	10.5	1.0	13.5	1.0	12.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to Z_n	5.0	1.0	6.0	9.5	1.0	11.5	1.0	11.0	ns	3-6
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.0	5.5	9.5	1.0	12.5	1.0	11.0	ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.0	5.5	9.5	1.0	12.0	1.0	11.0	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	65.0	pF	$V_{CC} = 5.5$ V

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Quad 2-Input Multiplexer

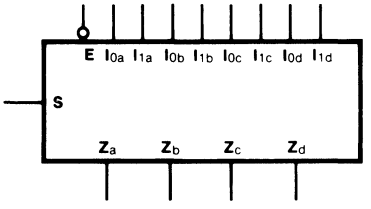
Description

The 'AC/'ACT157 is a high-speed quad 2-input multiplexer. Four bits of data from two sources can be selected using the common Select and Enable inputs. The four outputs present the selected data in the true (noninverted) form. The 'AC/'ACT157 can also be used as a function generator.

- **Outputs Source/Sink 24 mA**
- **'ACT157 has TTL-Compatible Inputs**

Ordering Code: See Section 6

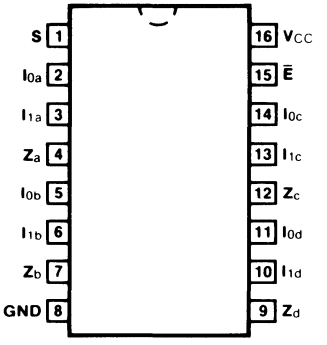
Logic Symbol



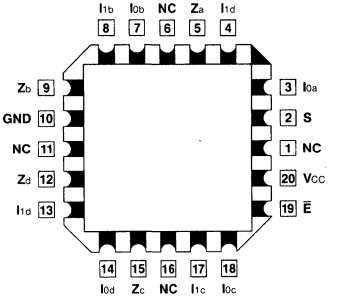
Pin Names

I_{0a} - I_{0d}	Source 0 Data Inputs
I_{1a} - I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
Z_a-Z_d	Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

5

Functional Description

The 'AC/'ACT157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The 'AC/'ACT157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$Z_a = \overline{E} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$
$Z_b = \overline{E} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$
$Z_c = \overline{E} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$
$Z_d = \overline{E} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$

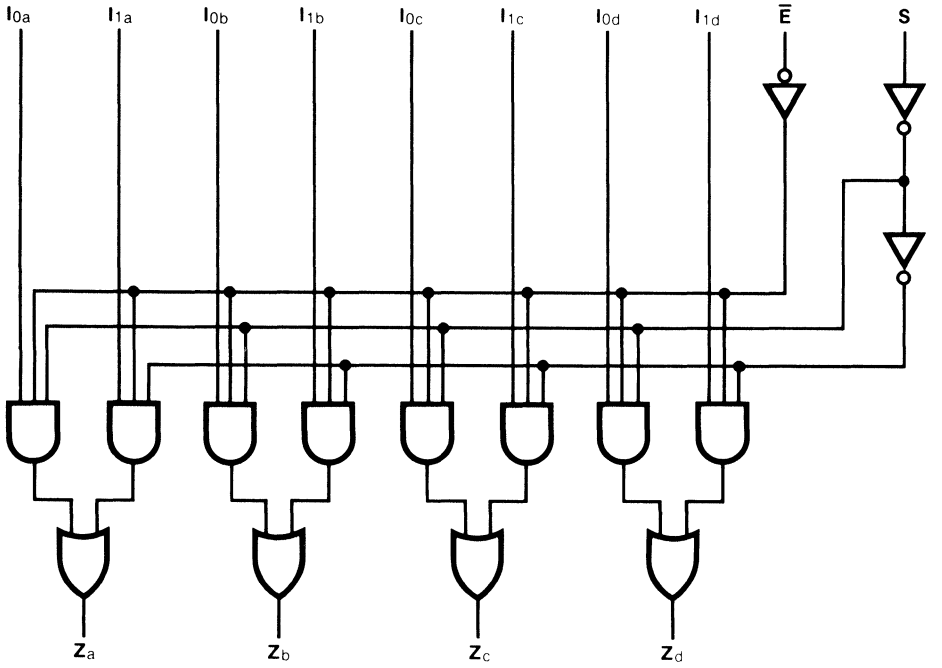
A common use of the 'AC/'ACT157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'AC/'ACT157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

Inputs				Outputs
$\overline{E}$	S	I_0	I_1	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT157)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

5

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to Z_n	3.3	1.0	7.0	11.5	1.0	14.5	1.0	13.0	ns	3-6
		5.0	1.0	5.5	9.0	1.0	11.0	1.0	10.0		
t_{PHL}	Propagation Delay S to Z_n	3.3	1.0	6.5	11.0	1.0	13.5	1.0	12.0	ns	3-6
		5.0	1.0	5.0	8.5	1.0	10.5	1.0	9.5		
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	3.3	1.0	7.0	11.5	1.0	14.0	1.0	13.0	ns	3-6
		5.0	1.0	5.5	9.0	1.0	10.5	1.0	10.0		
t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	3.3	1.0	6.5	11.0	1.0	13.0	1.0	12.0	ns	3-6
		5.0	1.0	5.5	9.0	1.0	10.5	1.0	9.5		
t_{PLH}	Propagation Delay I_n to Z_n	3.3	1.0	5.0	8.5	1.0	10.0	1.0	9.0	ns	3-5
		5.0	1.0	4.0	6.5	1.0	7.5	1.0	7.0		
t_{PHL}	Propagation Delay I_n to Z_n	3.3	1.0	5.0	8.0	1.0	10.0	1.0	9.0	ns	3-5
		5.0	1.0	4.0	6.5	1.0	7.5	1.0	7.0		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to Z_n	5.0	1.0	5.5	9.0	1.0	13.0	1.0	10.0	ns	3-6
t_{PHL}	Propagation Delay S to Z_n	5.0	1.0	5.5	9.5	1.0	12.5	1.0	10.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}$ to Z_n	5.0	1.0	6.0	10.0	1.0	13.0	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}$ to Z_n	5.0	1.0	5.0	8.5	1.0	12.5	1.0	9.0	ns	3-6
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.0	4.0	7.0	1.0	10.0	1.0	8.5	ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.0	4.5	7.5	1.0	10.0	1.0	8.5	ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.5$ V

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Quad 2-Input Multiplexer

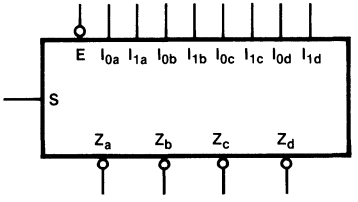
Description

The 'AC/'ACT158 is a high-speed quad 2-input multiplexer. It selects four bits of data from two sources using the common Select and Enable inputs. The four buffered outputs present the selected data in the inverted form. The 'AC/'ACT158 can also be used as a function generator.

- **Outputs Source/Sink 24 mA**
- **'ACT158 has TTL-Compatible Inputs**

Ordering Code: See Section 6

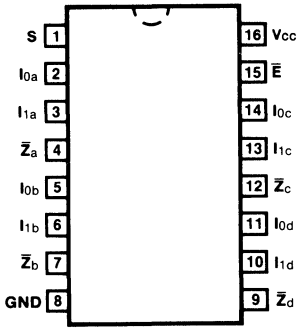
Logic Symbol



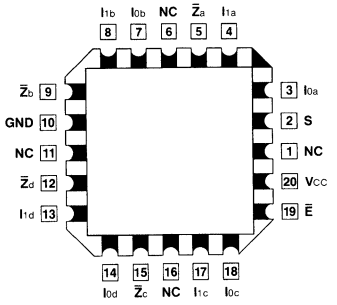
Pin Names

I_{0a} - I_{0d}	Source 0 Data Inputs
I_{1a} - I_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
$\overline{Z}_a$ - $\overline{Z}_d$	Inverted Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

5

Functional Description

The 'AC/'ACT158 quad 2-input multiplexer selects four bits of data from two sources under the control of a common Select input (S) and presents the data in inverted form at the four outputs. The Enable input ($\overline{E}$) is active-LOW. When $\overline{E}$ is HIGH, all of the outputs ($\overline{Z}$) are forced HIGH regardless of all other inputs. The 'AC/'ACT158 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input.

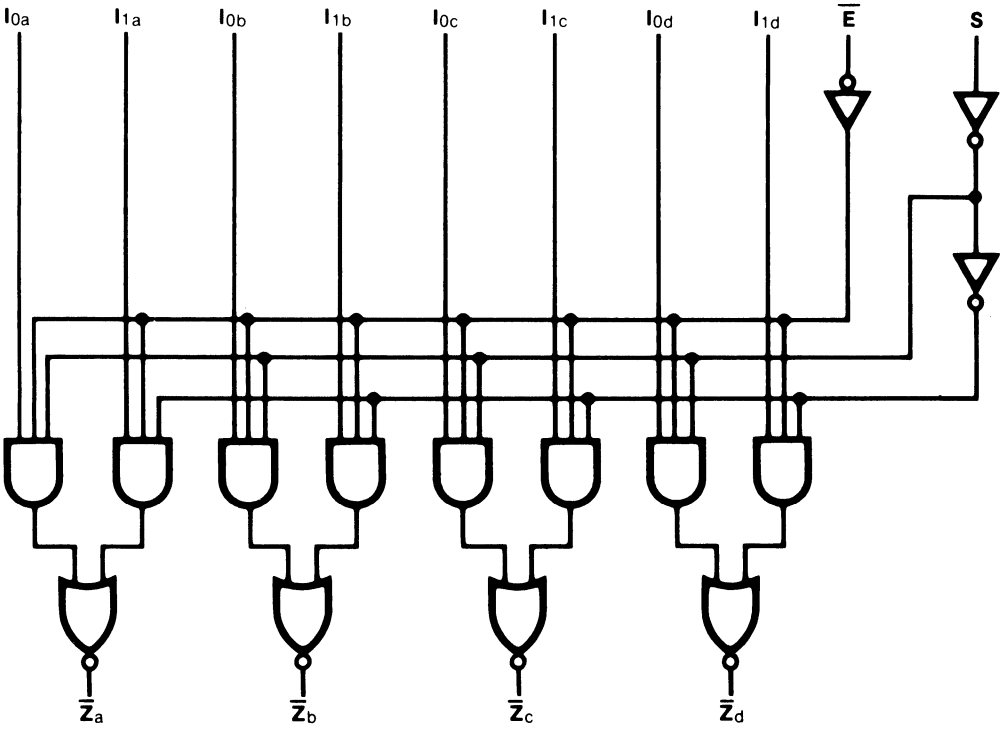
A common use of the 'AC/'ACT158 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The 'AC/'ACT158 can generate four functions of two variables with one variable common. This is useful for implementing gating functions.

Truth Table

Inputs				Output
$\overline{E}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT158)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	3.3	1.0	7.0	11.5	1.0	13.5	1.0	12.5	ns	3-6
		5.0	1.0	5.5	9.0	1.0	10.5	1.0	9.5		
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	3.3	1.0	7.0	11.5	1.0	14.0	1.0	12.5	ns	3-6
		5.0	1.0	5.5	9.0	1.0	10.5	1.0	10.0		
t_{PLH}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	3.3	1.0	7.5	12.0	1.0	14.5	1.0	13.0	ns	3-6
		5.0	1.0	6.0	9.5	1.0	11.0	1.0	10.5		
t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	3.3	1.0	7.0	11.0	1.0	13.0	1.0	12.0	ns	3-6
		5.0	1.0	5.5	8.5	1.0	10.0	1.0	9.5		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3	1.0	5.5	9.0	1.0	10.5	1.0	10.0	ns	3-5
		5.0	1.0	4.0	7.0	1.0	8.5	1.0	7.5		
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3	1.0	5.0	8.0	1.0	9.5	1.0	8.5	ns	3-5
		5.0	1.0	4.0	6.5	1.0	7.5	1.0	6.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	5.0	1.0	6.0	9.5	1.0	12.0	1.0	11.0	ns	3-6
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	5.0	1.0	5.5	9.0	1.0	11.0	1.0	10.0	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	5.0	1.0	5.5	9.5	1.0	11.0	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}$ to $\overline{Z}_n$	5.0	1.0	5.5	9.5	1.0	11.5	1.0	10.5	ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.0	4.5	8.0	1.0	9.5	1.0	8.5	ns	3-6
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.0	4.0	6.5	1.0	8.0	1.0	7.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.5$ V

54AC/74AC160 • 54ACT/74ACT160
54AC/74AC162 • 54ACT/74ACT162

Synchronous Presettable BCD Decade Counter

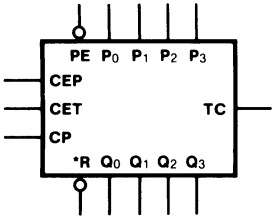
Description

The 'AC/'ACT160 and 'AC/'ACT162 are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/'ACT160 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'AC/'ACT162 has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock.

- **Synchronous Counting and Loading**
- **High-Speed Synchronous Expansion**
- **Typical Count Rate of 120 MHz**
- **Outputs Source/Sink 24 mA**
- **'ACT160 and 'ACT162 have TTL-Compatible Inputs**

Ordering Code: See Section 6

Logic Symbol

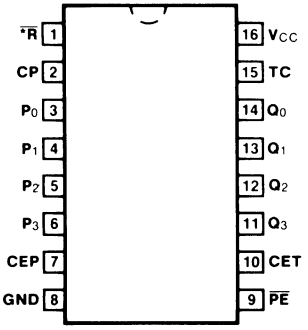


* $\overline{MR}$ for '160
* $\overline{SR}$ for '162

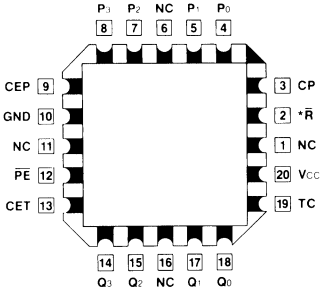
Pin Names

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$ ('160)	Asynchronous Master Reset Input
$\overline{SR}$ ('162)	Synchronous Reset Input
P_0 - P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0 - Q_3	Flip-Flop Outputs
TC	Terminal Count Output

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

* $\overline{MR}$ for '160
* $\overline{SR}$ for '162

Functional Description

The 'AC/'ACT160 and 'AC/'ACT162 count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '160) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('160), synchronous reset ('162), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, '160), Synchronous Reset ($\overline{SR}$, '162), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('160) or $\overline{SR}$ ('162) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'AC/'ACT160 and 'AC/'ACT162 use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 9. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the 'AC/'ACT160 and 'AC/'ACT162 decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

Logic Equations: Count Enable = $CEP \bullet CET \bullet \overline{PE}$

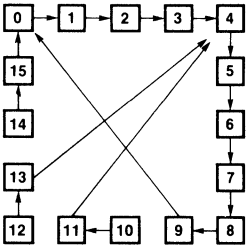
$TC = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3 \bullet CET$

Mode Select Table

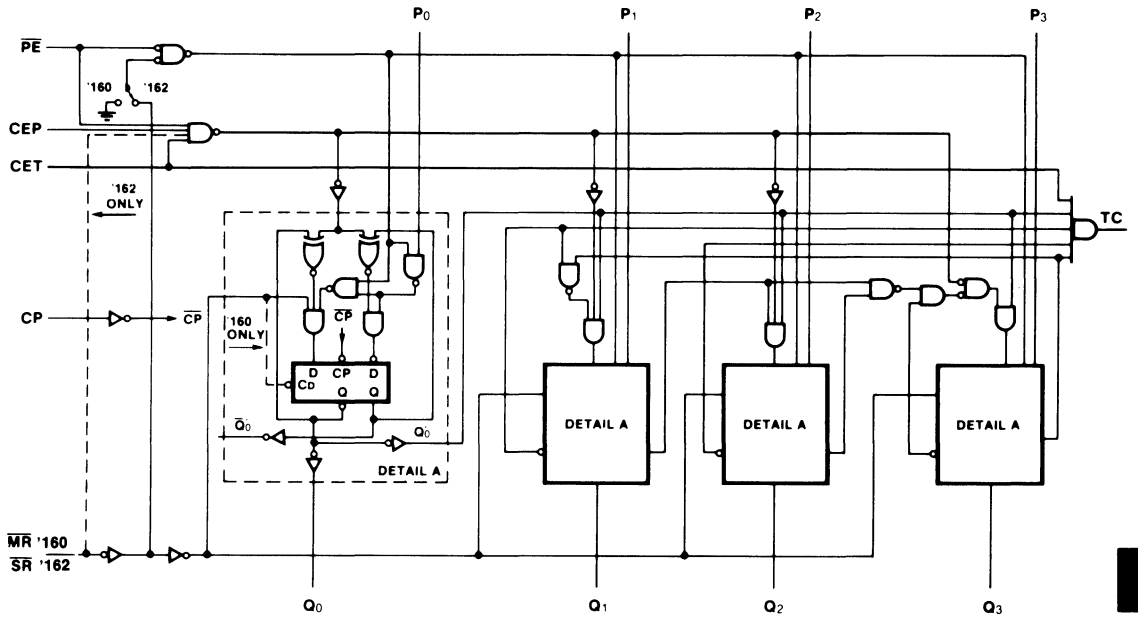
*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For '162 only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT160/162)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0		87 118						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	3.3 5.0		7.5 5.5						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	3.3 5.0		8.5 6.0						ns	3-6
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	3.3 5.0		9.5 7.0						ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0		11.0 8.0						ns	3-6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0		7.5 5.5						ns	3-6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0		8.5 6.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n ('AC160)	3.3 5.0		8.5 6.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('AC160)	3.3 5.0		8.5 6.0						ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	5.5 4.0				ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −5.0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	3.3 3.3	5.5 4.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5				ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5				ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0				ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0				ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0				ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW ('AC160)	3.3 5.0	4.5 3.0				ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP ('AC160)	3.3 5.0	0 0				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

5

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0		118						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	5.0		5.5						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	5.0		6.0						ns	3-6
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	5.0		7.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)	5.0		7.0						ns	3-6
t_{PLH}	Propagation Delay CP to TC	5.0		7.0						ns	3-6
t_{PHL}	Propagation Delay CP to TC	5.0		8.0						ns	3-6
t_{PLH}	Propagation Delay CET to TC	5.0		5.5						ns	3-6
t_{PHL}	Propagation Delay CET to TC	5.0		6.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n ('ACT160)	5.0		6.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('ACT160)	5.0		6.0						ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0				ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP ('ACT162)	5.0	4.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP ('ACT162)	5.0	−5.5				ns	3-9
t_s	Setup Time, HIGH OR LOW $\overline{PE}$ or $\overline{MR}$ to CP ('ACT160)	5.0	4.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{MR}$ to CP ('ACT160)	5.0	−5.5				ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5				ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0				ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0				ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0				ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW ('ACT160)	5.0	3.0				ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP ('ACT160)	5.0	0				ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC161 • 54ACT/74ACT161
54AC/74AC163 • 54ACT/74ACT163

Synchronous Presettable Binary Counter

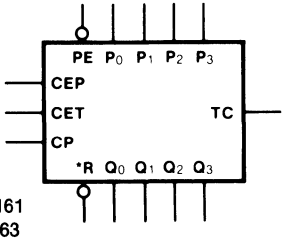
Description

The 'AC/'ACT161 and 'AC/'ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'AC/'ACT161 has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'AC/'ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

- **Synchronous Counting and Loading**
- **High-Speed Synchronous Expansion**
- **Typical Count Rate of 125 MHz**
- **Outputs Source/Sink 24 mA**
- **'ACT161 and 'ACT163 have TTL-Compatible Inputs**

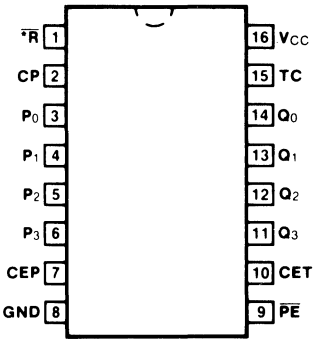
Ordering Code: See Section 6

Logic Symbol

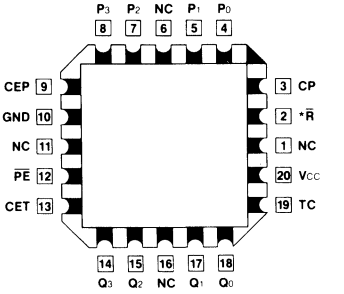


* $\overline{MR}$ for '161
* $\overline{SR}$ for '163

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

* $\overline{MR}$ for '161
* $\overline{SR}$ for '163

Pin Names

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$ ('161)	Asynchronous Master Reset Input
$\overline{SR}$ ('163)	Synchronous Reset Input
P_0 - P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0 - Q_3	Flip-Flop Outputs
TC	Terminal Count Output

Functional Description

The 'AC/'ACT161 and 'AC/'ACT163 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the '161) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('161), synchronous reset ('163), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, '161), Synchronous Reset ($\overline{SR}$, '163), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('161) or $\overline{SR}$ ('163) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'AC/'ACT161 and 'AC/'ACT163 use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'AC568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = CEP•CET•$\overline{PE}$

$TC = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet CET$

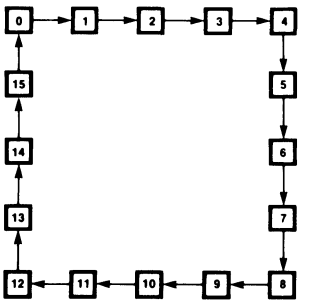
5

Mode Select Table

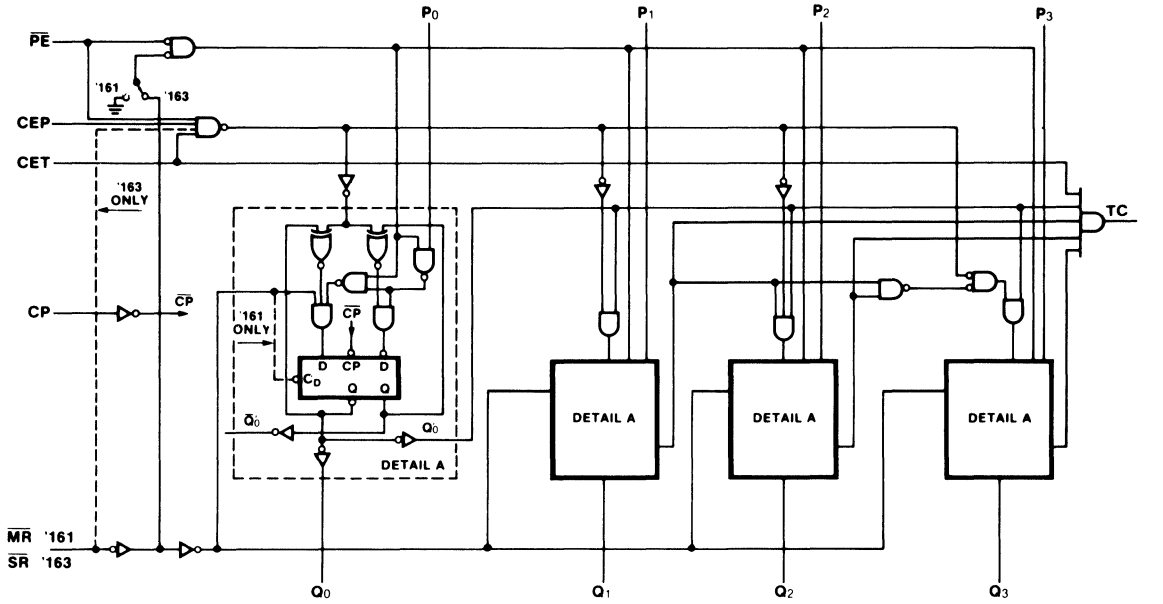
*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For '163 only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



Block Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT161/163)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC161 $T_A = +25°C$, $C_L = 50$ pF			54AC161 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC161 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0		87 118						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0		7.5 5.5						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0		8.5 6.0						ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0		11.0 8.0						ns	3-6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0		7.5 5.5						ns	3-6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0		8.5 6.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0		8.5 6.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	3.3 5.0		11.0 8.0						ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC161 $T_A = +25°C$ $C_L = 50$ pF		54AC161 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC161 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	5.5 4.0				ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −5.0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	5.5 4.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	5.5 4.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−7.5 −5.5				ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5				ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0				ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0				ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0				ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	4.5 3.0				ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT161 $T_A = +25°C$, $C_L = 50$ pF			54ACT161 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT161 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	115	125				100		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	5.5	9.5			1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	6.0	10.5			1.0	11.5	ns	3-6
t_{PLH}	Propagation Delay CP to TC	5.0	1.0	7.0	11.0			1.0	12.5	ns	3-6
t_{PHL}	Propagation Delay CP to TC	5.0	1.0	8.0	12.5			1.0	13.5	ns	3-6
t_{PLH}	Propagation Delay CET to TC	5.0	1.0	5.5	8.5			1.0	10.0	ns	3-6
t_{PHL}	Propagation Delay CET to TC	5.0	1.0	6.0	9.5			1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.0	6.0	10.0			1.0	11.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to TC	5.0	1.0	8.0	13.5			1.0	14.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT161		54ACT161	74ACT161	Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	9.5		11.5	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0	0		0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{MR}$ to CP	5.0	4.0	8.5		9.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{MR}$ to CP	5.0	−5.5	−0.5		−0.5	ns	3-9
t_s	Setup Time HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5		9.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5		−0.5	ns	3-9
t_s	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5		6.5	ns	3-9
t_h	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0		0	ns	3-9
t_w	Clock Pulse Width (Load) HIGH or LOW	5.0	2.0	3.0		3.5	ns	3-6
t_w	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.0		3.5	ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	3.0	3.0		7.5	ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	0	0		0.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.5$ V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC163 $T_A = +25°C$ $C_L = 50$ pF			54AC163 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC163 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 110	87 118				60 95		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.0			1.0 1.0	13.5 9.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	3.3 5.0	1.0 1.0	8.5 6.0	12.0 9.5			1.0 1.0	13.0 10.0	ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	1.0 1.0	9.5 7.0	15.0 10.5			1.0 1.0	16.5 11.5	ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	1.0 1.0	11.0 8.0	14.0 11.0			1.0 1.0	15.5 11.5	ns	3-6
t_{PLH}	Propagation Delay CET to TC	3.3 5.0	1.0 1.0	7.5 5.5	9.5 6.5			1.0 1.0	11.0 7.5	ns	3-6
t_{PHL}	Propagation Delay CET to TC	3.3 5.0	1.0 1.0	8.5 6.0	11.0 8.5			1.0 1.0	12.5 9.5	ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC163 $T_A = +25°C$ $C_L = 50$ pF		54AC163 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC163 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	5.5 4.0	13.5 8.5		16.0 10.5	ns	3-9
th	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	−7.0 −5.0	−1.0 0		−0.5 0	ns	3-9
ts	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	5.5 4.0	14.0 9.5		16.5 11.0	ns	3-9
th	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	−7.5 −5.5	−1.0 −0.5		−0.5 0	ns	3-9
ts	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	5.5 4.0	11.5 7.5		14.0 8.5	ns	3-9
th	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	−7.5 −5.0	−1.0 −0.5		−0.5 0	ns	3-9
ts	Setup Time, HIGH or LOW CEP or CET to CP	3.3 5.0	3.5 2.5	6.0 4.5		7.0 5.0	ns	3-9
th	Hold Time, HIGH or LOW CEP or CET to CP	3.3 5.0	−4.5 −3.0	0 0		0 0.5	ns	3-9
tw	Clock Pulse Width (Load) HIGH or LOW	3.3 5.0	3.0 2.0	3.5 2.5		4.0 3.0	ns	3-6
tw	Clock Pulse Width (Count) HIGH or LOW	3.3 5.0	3.0 2.0	4.0 3.0		4.5 3.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT163 $T_A = +25°C$, $C_L = 50$ pF			54ACT163 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT163 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	5.0	120	128				105		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	5.5	10.0			1.0	11.0	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	5.0	1.0	6.0	11.0			1.0	12.0	ns	3-6
t_{PLH}	Propagation Delay CP to TC	5.0	1.0	7.0	11.5			1.0	13.5	ns	3-6
t_{PHL}	Propagation Delay CP to TC	5.0	1.0	8.0	13.5			1.0	15.0	ns	3-6
t_{PLH}	Propagation Delay CET to TC	5.0	1.0	5.5	9.0			1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay CET to TC	5.0	1.0	6.0	10.0			1.0	11.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT163 $T_A = +25°C$ $C_L = 50$ pF		54ACT163 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT163 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW P_n to CP	5.0	4.0	10.0		12.0	ns	3-9
th	Hold Time, HIGH or LOW P_n to CP	5.0	−5.0	0.5		0.5	ns	3-9
ts	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	4.0	10.0		11.5	ns	3-9
th	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	−5.5	−0.5		−0.5	ns	3-9
ts	Setup Time HIGH or LOW $\overline{PE}$ to CP	5.0	4.0	8.5		10.5	ns	3-9
th	Hold Time, HIGH or LOW $\overline{PE}$ to CP	5.0	−5.5	−0.5		0	ns	3-9
ts	Setup Time, HIGH or LOW CEP or CET to CP	5.0	2.5	5.5		6.5	ns	3-9
th	Hold Time, HIGH or LOW CEP or CET to CP	5.0	−3.0	0		0.5	ns	3-9
tw	Clock Pulse Width HIGH or LOW	5.0	2.0	3.5		3.5	ns	3-6
tw	Clock Pulse Width (Count) HIGH or LOW	5.0	2.0	3.5		3.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.5$ V

54AC/74AC168 • 54AC/74AC169

4-Stage Synchronous Bidirectional Counters

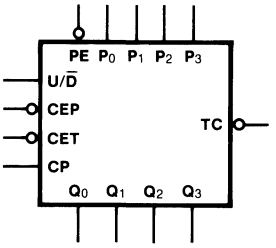
Description

The 'AC168 and 'AC169 are fully synchronous 4-stage up/down counters. The 'AC168 is a BCD decade counter; the 'AC169 is a modulo-16 binary counter. Both feature a preset capability for programmable operation, carry lookahead for easy cascading and a U/$\overline{D}$ input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the LOW-to-HIGH transition of the Clock.

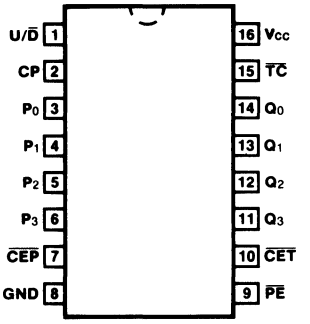
- **Synchronous Counting and Loading**
- **Built-in Lookahead Carry Capability**
- **Presettable for Programmable Operation**
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 6

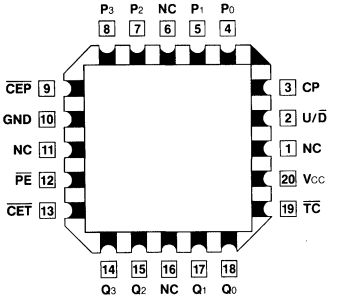
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



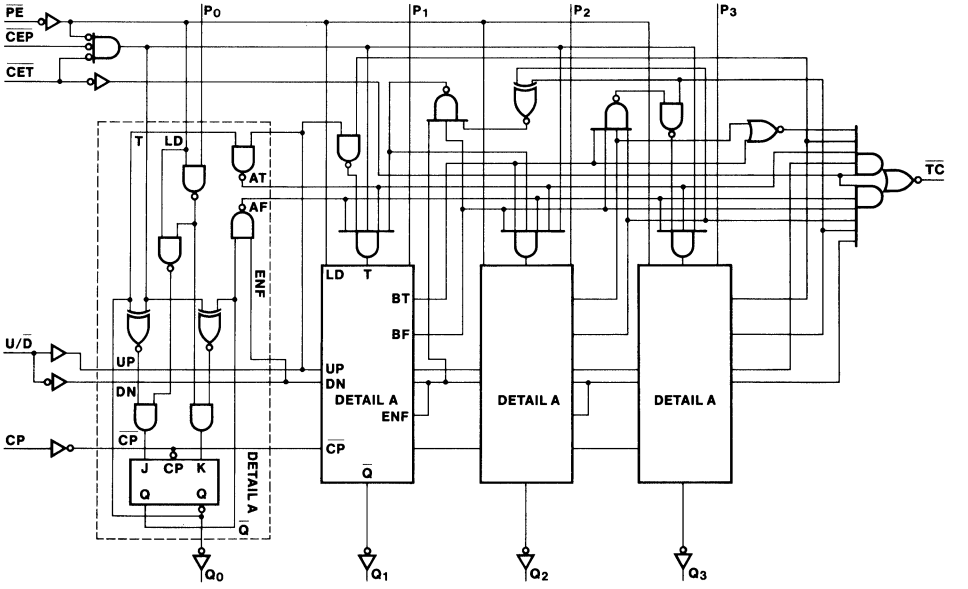
Pin Assignment for LCC

Pin Names

$\overline{CEP}$	Count Enable Parallel Input
$\overline{CET}$	Count Enable Trickle Input
CP	Clock Pulse Input
P_0 - P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
U/$\overline{D}$	Up-Down Count Control Input
Q_0 - Q_3	Flip-Flop Outputs
$\overline{TC}$	Terminal Count Output

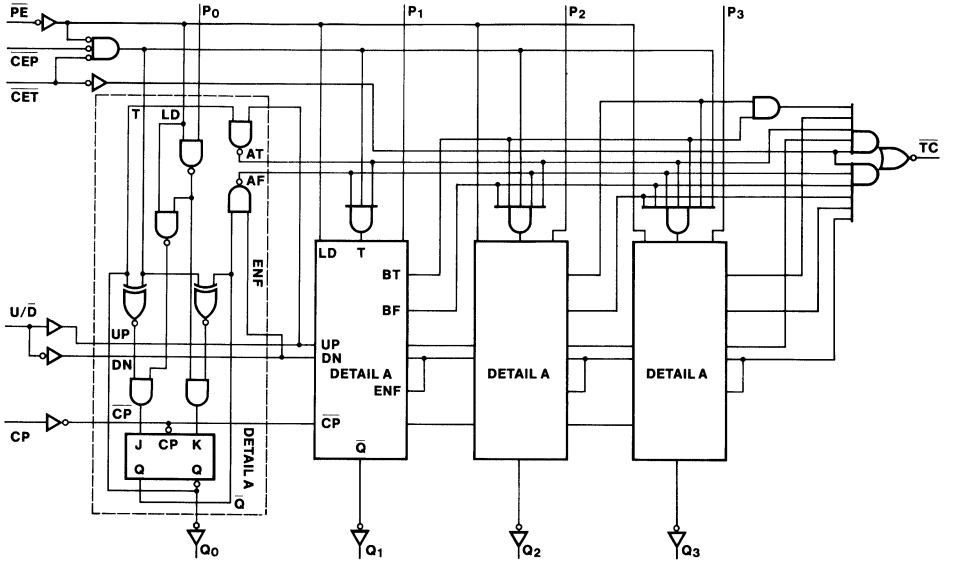
Logic Diagrams

'AC168



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

'AC169



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'AC168 and 'AC169 use edge-triggered J-K-type flip-flops and have no constraints on changing the control or data input signals in either state of the Clock. The only requirement is that the various inputs attain the desired state at least a setup time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedence over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is LOW, the data on the P_0-P_3 inputs enters the flip-flops on the next rising edge of the Clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be LOW and $\overline{PE}$ must be HIGH; the U/$\overline{D}$ input then determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW, provided that $\overline{CET}$ is LOW, when a counter reaches zero in the Count Down mode or reaches 9 (15 for the 'AC169) in the Count Up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel ($\overline{CEP}$) input level. The $\overline{TC}$ output of the 'AC168 decade counter can also be LOW in the illegal states 11, 13 and 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'AC169 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (see logic equations below).

1) Count Enable = $\overline{CEP} \bullet \overline{CET} \bullet \overline{PE}$
2) Up: ('AC168): $\overline{TC} = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (Up) \bullet \overline{CET}$
   ('AC169): $\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (Up) \bullet \overline{CET}$
3) Down (both): $\overline{TC} = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (Down) \bullet \overline{CET}$

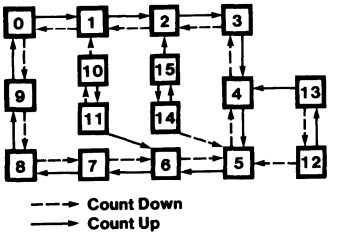
Mode Select Table

$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	Action on Rising Clock Edge
L	X	X	X	Load (P_n to Q_n)
H	L	L	H	Count Up (Increment)
H	L	L	L	Count Down (Decrement)
H	H	X	X	No Change (Hold)
H	X	H	X	No Change (Hold)

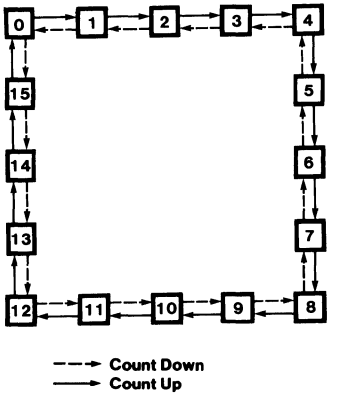
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagrams

'AC168



'AC169



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DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC168 $T_A = +25°C$, $C_L = 50$ pF			54AC168 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC168 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		118 154						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0		10.5 7.5						ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{TC}$	3.3 5.0		13.5 9.5						ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{TC}$	3.3 5.0		13.5 9.5						ns	3-6
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0		11.0 8.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0		9.5 7.0						ns	3-6
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0		10.5 7.5						ns	3-6
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$	3.3 5.0		9.0 6.5						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC168 $T_A = +25°C$ $C_L = 50$ pF		54AC168 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC168 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	3.0 1.5				ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	1.5 0.5				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	7.5 4.5				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	4.5 2.0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	7.0 4.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	6.0 4.0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 2.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 1.5				ns	3-9
t_s	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	3.3 5.0	12.5 9.0				ns	3-9
t_h	Hold Time, HIGH or LOW U/$\overline{D}$ to $\overline{CP}$	3.3 5.0	7.0 4.0				ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC169 $T_A = +25°C$ $C_L = 50$ pF			54AC169 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC169 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	75 100	118 154		55 75		65 90		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0	1.0 1.0	9.5 7.0	13.0 10.0	1.0 1.0	16.0 12.0	1.0 1.0	14.5 11.0	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0	1.0 1.0	10.5 7.5	14.5 11.0	1.0 1.0	17.5 13.0	1.0 1.0	16.0 12.0	ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{TC}$	3.3 5.0	1.0 1.0	13.5 9.5	18.0 13.0	1.0 1.0	22.5 16.0	1.0 1.0	22.0 14.0	ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{TC}$	3.3 5.0	1.0 1.0	13.5 9.5	18.0 13.0	1.0 1.0	23.0 16.0	1.0 1.0	20.5 14.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	11.0 8.0	15.0 10.5	1.0 1.0	18.5 13.0	1.0 1.0	16.5 12.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	9.5 7.0	12.5 9.0	1.0 1.0	16.0 11.5	1.0 1.0	14.5 10.0	ns	3-6
t_{PLH}	Propagation Delay $U/\overline{D}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	11.0 8.0	15.0 10.5	1.0 1.0	19.0 13.5	1.0 1.0	17.0 12.0	ns	3-6
t_{PHL}	Propagation Delay $U/\overline{D}$ to $\overline{TC}$	3.3 5.0	1.0 1.0	10.0 7.0	13.5 9.5	1.0 1.0	17.0 12.0	1.0 1.0	15.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC169 $T_A = +25°C$ $C_L = 50$ pF		54AC169 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC169 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	3.0 1.5	4.5 2.5	6.0 3.0	5.0 2.5	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	1.5 0.5	0.5 1.5	0.5 1.5	0.5 1.5	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	7.5 4.5	10.5 7.0	14.0 9.0	12.5 8.0	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ to CP	3.3 5.0	4.5 2.0	0 0.5	0.5 1.0	0 1.0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	7.0 4.0	10.0 6.5	13.5 9.0	12.0 8.0	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CET}$ to CP	3.3 5.0	6.0 4.0	0 0.5	0.5 1.0	0 1.0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 2.0	5.5 3.5	7.0 4.5	6.5 4.0	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	3.5 1.5	0 0.5	0 0.5	0 0.5	ns	3-9
t_s	Setup Time, HIGH or LOW U/$\overline{D}$ to CP	3.3 5.0	7.0 4.5	10.0 6.5	13.0 8.5	11.5 7.5	ns	3-9
t_h	Hold Time, HIGH or LOW U/$\overline{D}$ to $\overline{CP}$	3.3 5.0	7.0 4.0	0 0.5	0 0.5	0 0.5	ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	2.0 2.0	3.0 3.0	5.0 5.0	4.0 3.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	60.0	pF	$V_{CC} = 5.5$ V

54AC/74AC174 • 54ACT/74ACT174

Hex D Flip-Flop With Master Reset

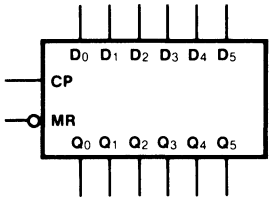
Description

The 'AC/'ACT174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the LOW-to-HIGH clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

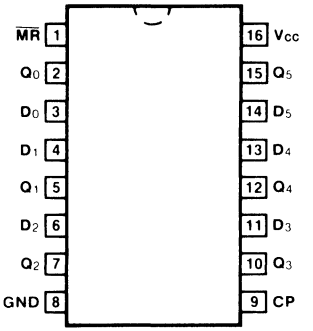
- **Outputs Source/Sink 24 mA**
- **'ACT174 has TTL-Compatible Inputs**

Ordering Code: See Section 6

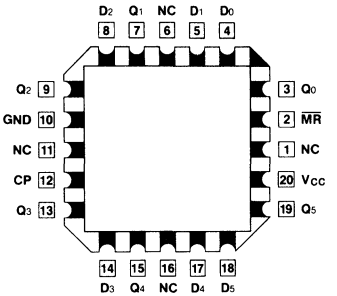
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Pin Names

D_0 - D_5	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0 - Q_5	Outputs

5

Functional Description

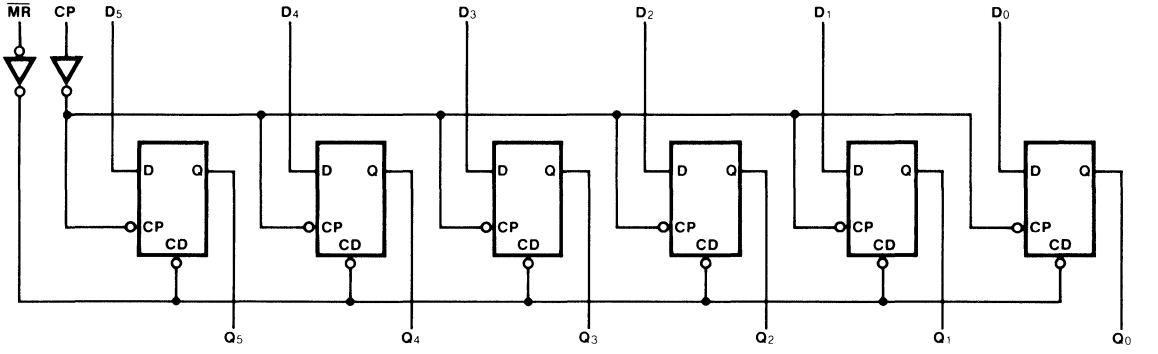
The 'AC/'ACT174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flop's output following the LOW-to-HIGH Clock (CP) transition. A LOW input to the Master Reset ($\overline{MR}$) will force all outputs LOW independent of Clock or Data inputs. The 'AC/'ACT174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

Inputs			Output
$\overline{MR}$	CP	D	Q
L	X	X	L
H	⌐	H	H
H	⌐	L	L
H	L	X	Q

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition of Clock

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT174)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	90 100	100 125		65 90		70 100		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	1.0 1.0	9.0 6.0	11.5 8.5	1.0 1.0	14.0 10.5	1.0 1.0	12.5 9.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	1.0 1.0	8.5 6.0	11.0 8.0	1.0 1.0	13.0 10.0	1.0 1.0	12.0 9.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0	1.0 1.0	9.0 7.0	11.5 9.0	1.0 1.0	13.5 11.0	1.0 1.0	12.5 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW D_n to CP	3.3 5.0	2.5 2.0	6.5 5.0	7.5 5.5	7.0 5.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	1.0 0.5	3.0 3.0	3.0 3.0	3.0 3.0	ns	3-9
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0	7.0 5.0	ns	3-6
t_w	CP Pulse Width	3.3 5.0	1.0 1.0	5.5 5.0	7.0 5.0	7.0 5.0	ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0	2.5 2.0	3.0 2.0	2.5 2.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	165	200		95		140		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	5.0	1.0	7.0	10.5	1.0	11.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	5.0	1.0	7.0	10.5	1.0	11.0	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.0	6.5	9.5	1.0	12.0	1.0	11.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW D_n to CP	5.0	0.5	1.5	1.5	1.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.0	2.0	2.0	2.0	ns	3-9
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	1.5	3.0	5.0	3.5	ns	3-6
t_w	CP Pulse Width HIGH or LOW	5.0	1.5	3.0	5.0	3.5	ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	−1.0	0.5	0.5	0.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	85.0	pF	$V_{CC} = 5.5$ V

54AC/74AC175 • 54ACT/74ACT175

Quad D Flip-Flop

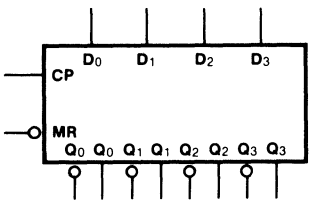
Description

The 'AC/'ACT175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the LOW-to-HIGH clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when LOW.

- **Edge-Triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **Asynchronous Common Reset**
- **True and Complement Output**
- **Outputs Source/Sink 24 mA**
- **'ACT175 has TTL-Compatible Inputs**

Ordering Code: See Section 6

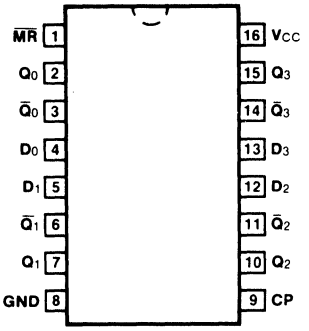
Logic Symbol



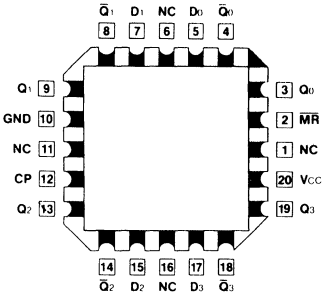
Pin Names

D_0 - D_3	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0 - Q_3	True Outputs
$\overline{Q}_3$ - $\overline{Q}_3$	Complement Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

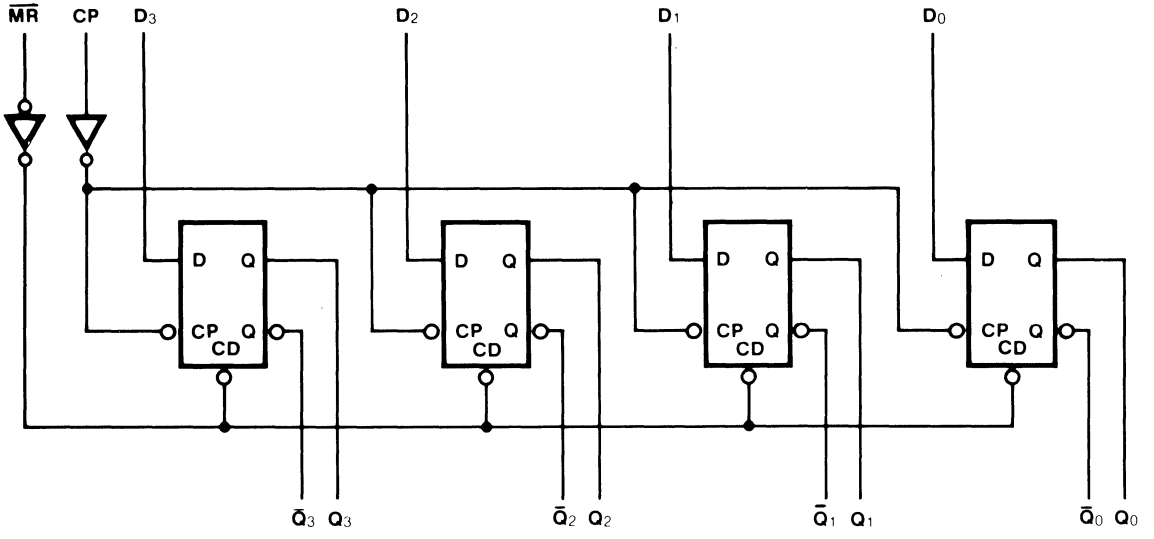
The 'AC/'ACT175 consists of four edge-triggered D flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the LOW-to-HIGH clock (CP) transition, causing individual Q and $\overline{Q}$ outputs to follow. A LOW input on the Master Reset ($\overline{MR}$) will force all Q outputs LOW and $\overline{Q}$ outputs HIGH independent of Clock or Data inputs. The 'AC/'ACT175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

Truth Table

Inputs	Outputs	
@t_n, $\overline{MR}$ = H	@t_{n+1}	
D_n	Q_n	$\overline{Q}_n$
L	L	H
H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
t_n = Bit Time before Clock Pulse
t_{n+1} = Bit Time after Clock Pulse

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT175)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		118 160						MHz	3-3
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3 5.0		9.5 7.0						ns	3-6
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	3.3 5.0		8.5 6.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	3.3 5.0		7.5 5.5						ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{Q}_n$	3.3 5.0		8.5 6.0						ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	4.5 3.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0				ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	5.5 4.0				ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	5.5 4.0				ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	0 0				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	175	160		95		145		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n or $\overline{Q}_n$	5.0	1.0	6.0	10.0	1.0	11.5	1.0	11.0	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n or $\overline{Q}_n$	5.0	1.0	7.0	11.0	1.0	13.0	1.0	12.0	ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.0	6.0	9.5	1.0	11.5	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	1.0	5.5	9.5	1.0	11.0	1.0	10.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT	Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		
			Typ	Guaranteed Minimum				
t_s (H)	Setup Time D_n to CP	5.0	3.0	2.0	2.5	2.0	ns	3-9
t_s (L)	Setup Time D_n to CP	5.0	3.0	2.5	3.0	2.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.0	1.0	1.0	ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	4.0	3.0	5.0	3.5	ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	4.0	3.5	5.0	4.0	ns	3-6
t_{rec}	Recovery Time, $\overline{MR}$ to CP	5.0	0	0	0.5	0	ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.5$ V

54AC/74AC190 • 54AC/74AC191

Up/Down Counters with Preset and Ripple Clock

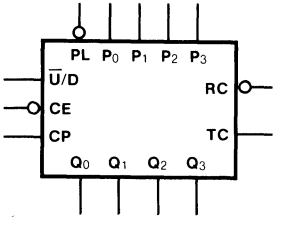
Description

The 'AC190 is a reversible BCD (8421) decade counter. The 'AC191 is a reversible modulo 16 binary counter. Both feature synchronous counting and asynchronous presetting. The preset feature allows the 'AC190 and 'AC191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and the Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

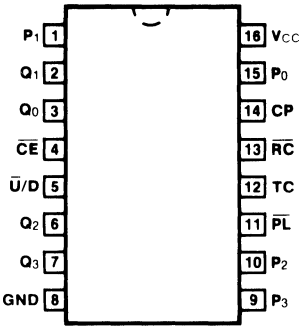
- **High-speed—120 MHz Typical Count Frequency**
- **Synchronous Counting**
- **Asynchronous Parallel Load**
- **Cascadable**
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 6

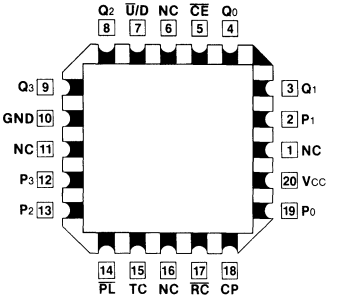
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Pin Names

$\overline{CE}$	Count Enable Input
CP	Clock Pulse Input
P_0 - P_3	Parallel Data Inputs
$\overline{PL}$	Asynchronous Parallel Load Input
$\overline{U}$/D	Up/Down Count Control Input
Q_0 - Q_3	Flip-Flop Outputs
$\overline{RC}$	Ripple Clock Output
TC	Terminal Count Output

Functional Description

The 'AC190/'AC191 are synchronous up/down counters. The 'AC190 is a BCD decade counter while the 'AC191 is organized as a 4-bit binary counter. Both contain four edge-triggered flip-flops with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load ($\overline{PL}$) input is LOW, information present on the Parallel Load inputs (P_0 - P_3) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the $\overline{CE}$ input inhibits counting. When $\overline{CE}$ is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U}$/D input signal, as indicated in the Mode Select Table. $\overline{CE}$ and $\overline{U}$/D can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.

Two types of outputs are provided as overflow/underflow indicators. The terminal count (TC) output is normally LOW. It goes HIGH when the circuits reach zero in the count down mode or 9 ('AC190) or 15 ('AC191) in the count up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U}$/D is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock ($\overline{RC}$) output. The $\overline{RC}$ output is normally HIGH. When $\overline{CE}$ is LOW and TC is HIGH, $\overline{RC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures a and b. In Figure a, each $\overline{RC}$ output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on $\overline{CE}$ inhibits the $\overline{RC}$ output pulse, as indicated in the $\overline{RC}$ Truth Table. A disadvantage of

Mode Select Table

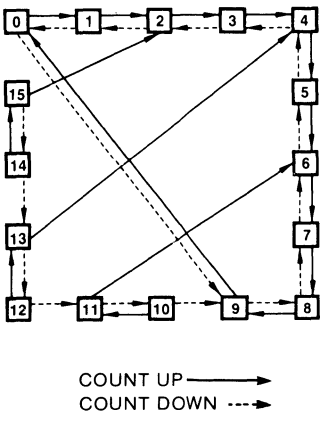
Inputs				Mode
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	⌐	Count Up
H	L	H	⌐	Count Down
L	X	X	X	Preset (Asyn.)
H	H	X	X	No Change (Hold)

$\overline{RC}$ Truth Table

Inputs			Outputs
$\overline{CE}$	TC*	CP	$\overline{RC}$
L	H	⌐⌐	⌐⌐
H	X	X	H
X	L	X	H

*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

State Diagram



this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.

A method of causing state changes to occur simultaneously in all stages is shown in Figure b. All clock inputs are driven in parallel and the $\overline{RC}$ outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the $\overline{RC}$ output of any device goes HIGH shortly after its CP input goes HIGH.

The configuration shown in Figure c avoids ripple delays and their associated restrictions. The $\overline{CE}$ input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures a and b doesn't apply, because the TC output of a given stage is not affected by its own $\overline{CE}$.

Figure a: N-Stage Counter Using Ripple Clock

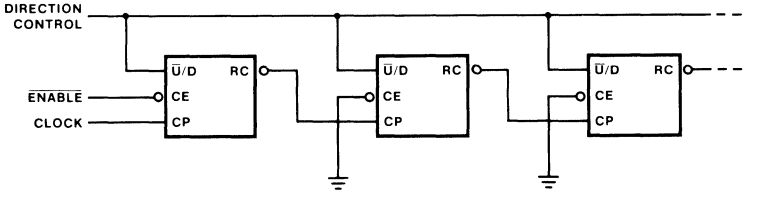


Figure b: Synchronous N-Stage Counter Using Ripple Carry/Borrow

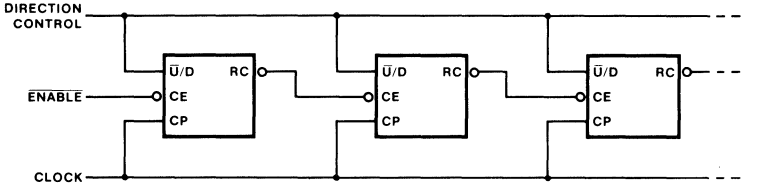
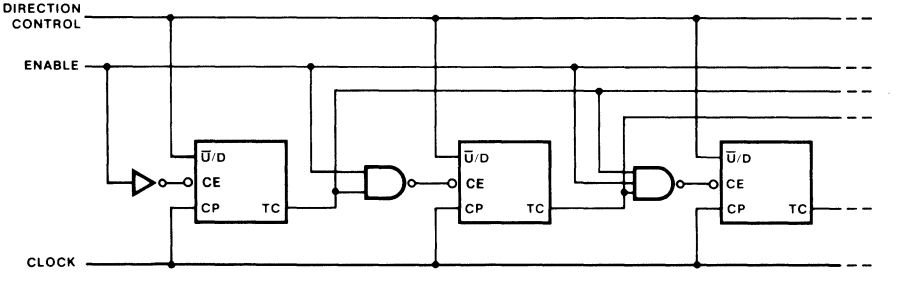
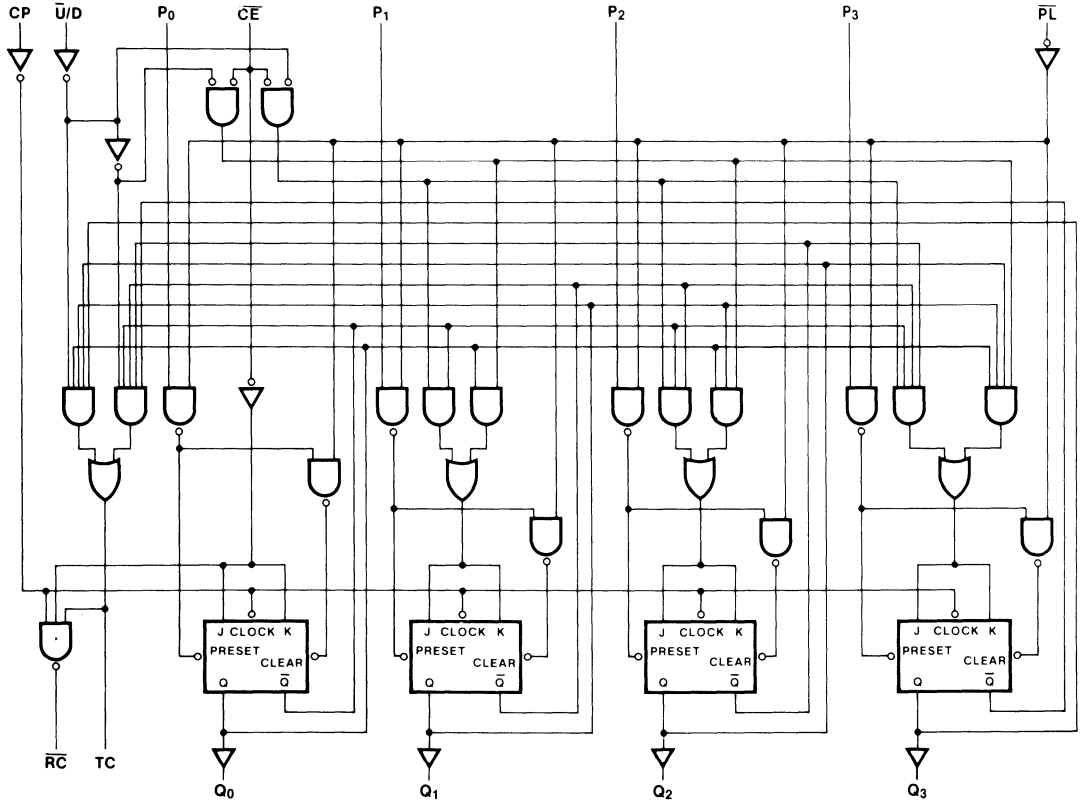


Figure c: Synchronous N-Stage Counter With Parallel Gated Carry/Borrow



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC190 $T_A = +25°C$, $C_L = 50$ pF			54AC190 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC190 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0		88 120						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0		10.5 7.5						ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0		15.0 11.0						ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0		13.0 9.5						ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{RC}$	3.3 5.0		9.0 6.5						ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{RC}$	3.3 5.0		9.5 7.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0		8.5 6.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	3.3 5.0		11.0 8.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	3.3 5.0		10.5 7.5						ns	3-6
t_{PLH}	Propagation Delay $\overline{U}$/D to TC	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{U}$/D to TC	3.3 5.0		9.5 7.0						ns	3-6
t_{PLH}	Propagation Delay P_n to Q_n	3.3 5.0		10.5 7.5						ns	3-6
t_{PHL}	Propagation Delay P_n to Q_n	3.3 5.0		9.5 7.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0		11.5 8.5						ns	3-6
t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0		11.5 8.5						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC190 $T_A = +25°C$ $C_L = 50$ pF		54AC190 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC190 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	4.5 3.0				ns	3-9
t_h	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	−0.5 −0.5				ns	3-9
t_s	Setup Time, LOW $\overline{CE}$ to CP	3.3 5.0	7.0 5.0				ns	3-9
t_h	Hold Time, LOW $\overline{CE}$ to CP	3.3 5.0	−1.5 −1.0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{U}/D$ to CP	3.3 5.0	7.0 5.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{U}/D$ to CP	3.3 5.0	−1.5 −1.0				ns	3-9
t_w	$\overline{PL}$ Pulse Width, LOW	3.3 5.0	5.5 6.0				ns	3-6
t_w	CP Pulse Width, LOW	3.3 5.0	5.5 6.0				ns	3-6
t_{rec}	Recovery Time $\overline{PL}$ to CP	3.3 5.0	4.5 3.0				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC191 $T_A = +25°C$, $C_L = 50$ pF			54AC191 $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC191 $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0	70 90	105 133		60 80		65 85		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	3.0 2.0	8.5 6.0	15.0 11.0	1.0 1.0	17.5 13.0	1.0 1.0	16.0 12.0	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	3.0 2.0	8.5 6.0	14.5 10.5	1.0 1.0	17.5 12.5	1.0 1.0	16.0 11.5	ns	3-6
t_{PLH}	Propagation Delay CP to TC	3.3 5.0	4.0 3.0	10.5 7.5	18.0 12.0	1.0 1.0	22.0 15.5	1.0 1.0	20.0 14.0	ns	3-6
t_{PHL}	Propagation Delay CP to TC	3.3 5.0	4.5 3.0	10.5 7.5	17.5 12.5	1.0 1.0	20.5 15.0	1.0 1.0	19.0 13.5	ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{RC}$	3.3 5.0	3.0 2.5	7.5 5.5	12.0 9.5	1.0 1.0	14.5 11.0	1.0 1.0	13.5 10.5	ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{RC}$	3.3 5.0	2.5 2.0	7.0 5.0	11.5 8.5	1.0 1.0	14.0 10.0	1.0 1.0	12.5 9.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0	2.5 1.5	7.0 5.0	12.0 8.5	1.0 1.0	15.0 10.5	1.0 1.0	13.5 9.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{CE}$ to $\overline{RC}$	3.3 5.0	2.5 1.5	6.5 5.0	11.0 8.0	1.0 1.0	14.0 10.0	1.0 1.0	12.5 9.0	ns	3-6
t_{PLH}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	3.3 5.0	2.5 1.5	6.5 5.0	12.5 9.0	1.0 1.0	16.0 11.5	1.0 1.0	14.5 10.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{U}$/D to $\overline{RC}$	3.3 5.0	2.5 1.5	7.0 5.0	12.0 8.5	1.0 1.0	15.5 11.0	1.0 1.0	13.5 10.0	ns	3-6
t_{PLH}	Propagation Delay $\overline{U}$/D to TC	3.3 5.0	2.5 2.0	7.0 5.0	11.5 8.5	1.0 1.0	14.5 10.5	1.0 1.0	13.5 9.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{U}$/D to TC	3.3 5.0	2.5 1.5	6.5 5.0	11.0 8.5	1.0 1.0	13.5 10.5	1.0 1.0	12.5 9.5	ns	3-6
t_{PLH}	Propagation Delay P_n to Q_n	3.3 5.0	3.0 2.0	8.0 5.5	13.5 9.5	1.0 1.0	17.0 11.5	1.0 1.0	15.5 10.5	ns	3-6
t_{PHL}	Propagation Delay P_n to Q_n	3.3 5.0	3.0 2.0	7.5 5.5	13.0 9.5	1.0 1.0	16.5 11.5	1.0 1.0	14.5 10.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0	3.5 2.0	9.5 5.5	14.5 9.5	1.0 1.0	19.0 11.5	1.0 1.0	17.5 10.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0	3.0 2.0	8.0 6.0	13.5 10.0	1.0 1.0	16.5 12.0	1.0 1.0	15.5 11.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC191 $T_A = +25°C$ $C_L = 50$ pF		54AC191 $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC191 $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	1.0 0.5	3.0 2.0	3.5 3.0	3.0 2.5	ns	3-9
t_h	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	-1.5 -0.5	0.5 1.0	1.0 1.0	1.0 1.0	ns	3-9
t_s	Setup Time, LOW $\overline{CE}$ to CP	3.3 5.0	3.0 1.5	6.0 4.0	7.5 5.0	7.0 4.5	ns	3-9
t_h	Hold Time, LOW $\overline{CE}$ to CP	3.3 5.0	-4.0 -2.5	-0.5 0	-0.5 0	-0.5 0	ns	3-9
t_s	Setup Time, HIGH or LOW, $\overline{U}$/D to CP	3.3 5.0	4.0 2.5	8.0 5.5	10.5 7.0	9.0 6.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{U}$/D to CP	3.3 5.0	-5.0 -3.0	0 0.5	0 0.5	0 0.5	ns	3-9
t_w	$\overline{PL}$ Pulse Width, LOW	3.3 5.0	2.0 1.0	3.5 1.0	4.5 1.0	4.0 1.0	ns	3-6
t_w	CP Pulse Width, LOW	3.3 5.0	2.0 2.0	3.5 3.0	4.5 4.0	4.0 4.0	ns	3-6
t_{rec}	Recovery Time $\overline{PL}$ to CP	3.3 5.0	-0.5 -1.0	0 0	0 0	0 0	ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	75.0	pF	$V_{CC} = 5.5$ V

54AC/74AC192 • 54AC/74AC193

Up/Down Counters with Separate Up/Down Clocks

Description

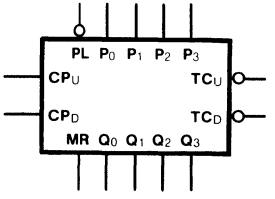
The 'AC192 is an up/down BCD decade (8421) counter. The 'AC193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs.

Separate Terminal Count Up and Terminal Count Down outputs are provided that are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

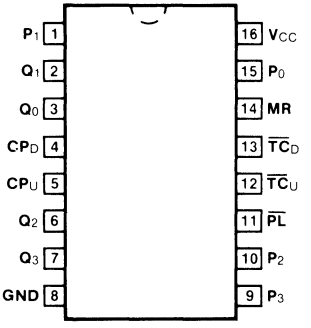
- **High-Speed—120 MHz Typical Count Frequency**
- **Synchronous Counting**
- **Asynchronous Parallel Load and Master Reset**
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 6

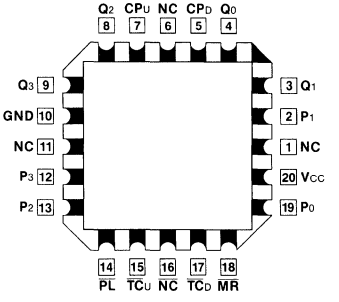
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC

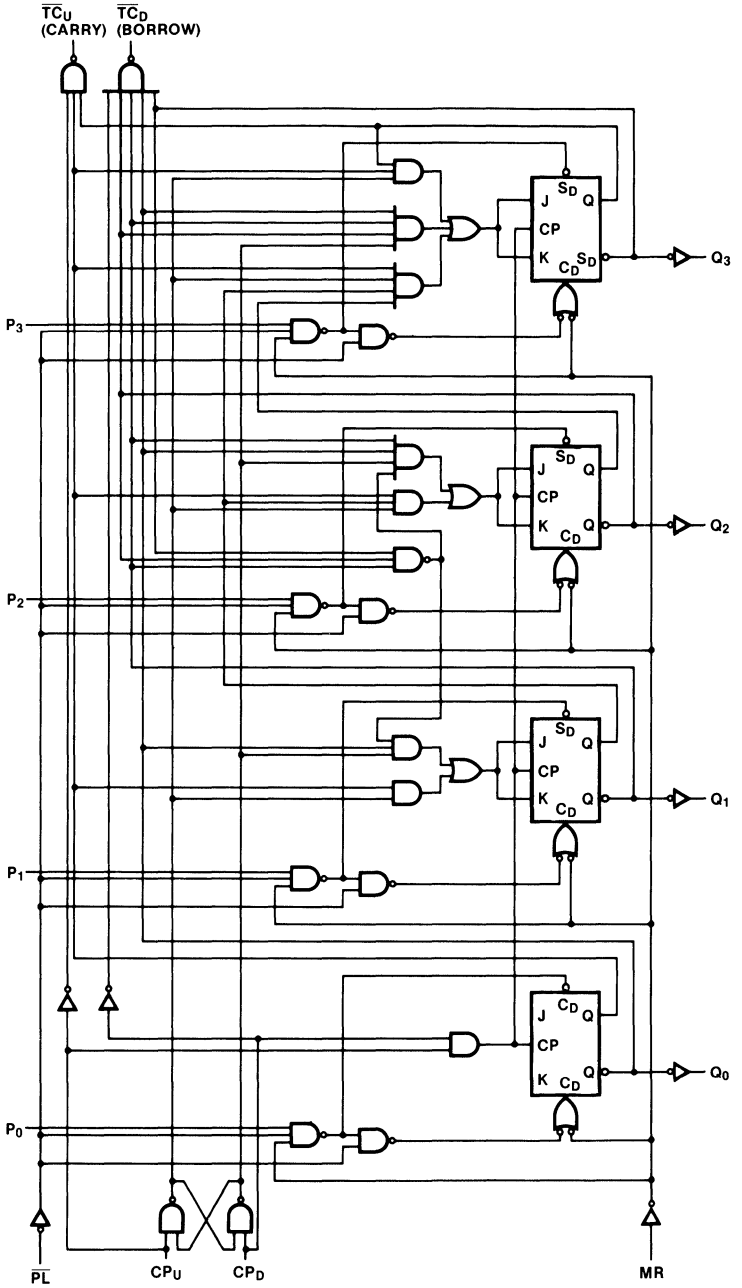


Pin Assignment for LCC

Pin Names

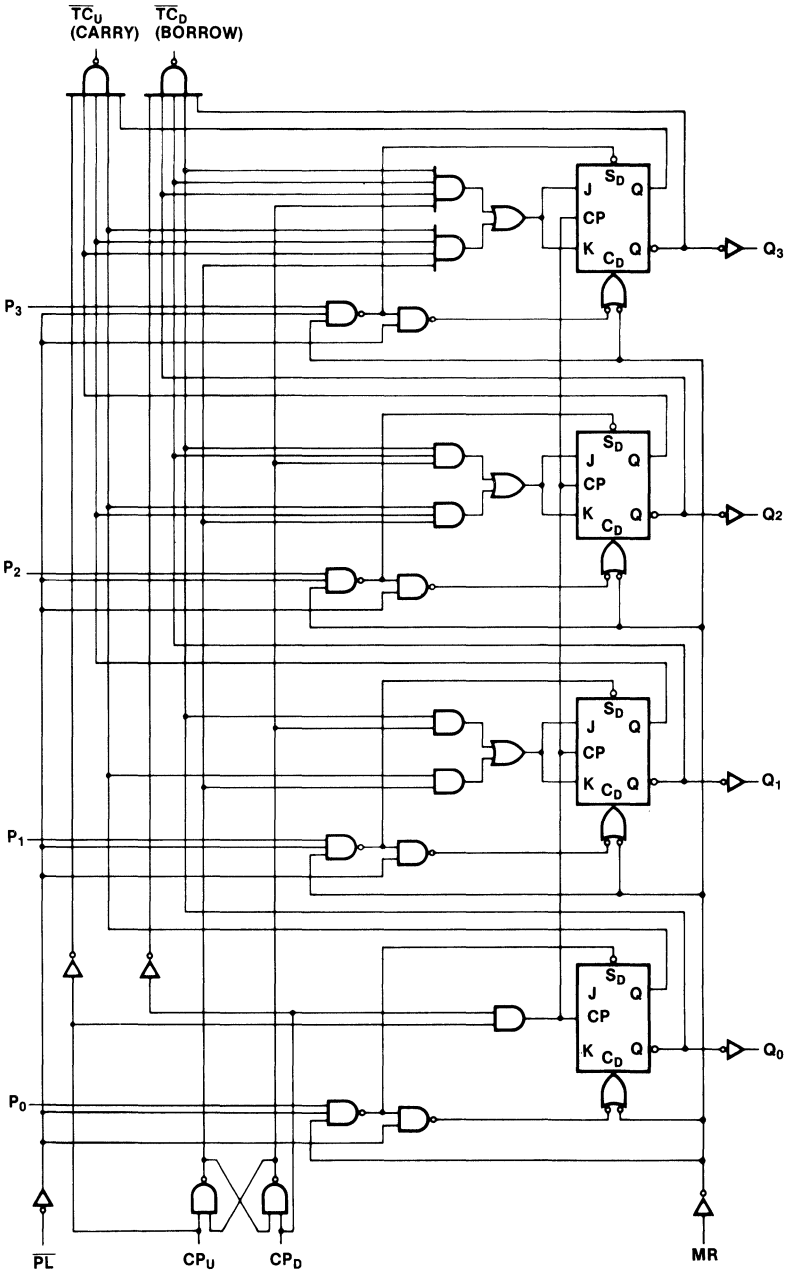
CP_U	Count Up Clock Input
CP_D	Count Down Clock Input
MR	Asynchronous Master Reset Input
$\overline{PL}$	Asynchronous Parallel Load Input
P_0 - P_3	Parallel Data Inputs
Q_0 - Q_3	Flip-flop Outputs
$\overline{TC}_D$	Terminal Count Down (Borrow) Output
$\overline{TC}_U$	Terminal Count Up (Carry) Output

Logic Diagram
'AC192



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagram
'AC193



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'AC192/'AC193 are asynchronously presettable counters. The 'AC192 is a decade counter while the 'AC193 is organized for 4-bit binary operation. They both contain four edge-triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state; 9 ('AC192) or 15 ('AC193), the reset HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

$$\overline{TC}_U = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3 \bullet \overline{CP}_U \text{ ('AC192)}$$
$$\overline{TC}_U = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet \overline{CP}_U \text{ ('AC193)}$$
$$\overline{TC}_U = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet \overline{CP}_D$$

Both the 'AC192 and the 'AC193 have an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input (P_0 - P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

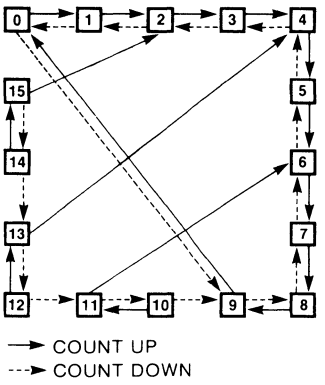
Function Table

MR	$\overline{PL}$	CP_U	CP_D	Mode
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⌐	H	Count Up
L	H	H	⌐	Count Down

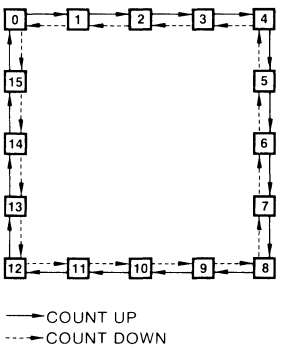
H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level ⌐ = LOW-to-HIGH Transition

State Diagrams

'AC192



'AC193



DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	3.3 5.0		88 120						MHz	3-3
t_{PLH}	Propagation Delay C_{PU} or C_{PD} to $\overline{TC_U}$ or $\overline{TC_D}$	3.3 5.0		15.0 11.0						ns	3-6
t_{PHL}	Propagation Delay C_{PU} or C_{PD} to $\overline{TC_U}$ or $\overline{TC_D}$	3.3 5.0		13.0 9.5						ns	3-6
t_{PLH}	Propagation Delay C_{PU} or C_{PD} to Q_n	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay C_{PU} or C_{PD} to Q_n	3.3 5.0		10.5 7.5						ns	3-6
t_{PLH}	Propagation Delay P_n to Q_n	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay P_n to Q_n	3.3 5.0		9.5 7.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0		12.5 9.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{PL}$ to Q_n	3.3 5.0		11.0 8.0						ns	3-6
t_{PHL}	Propagation Delay MR to Q_n	3.3 5.0		12.5 9.0						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics, continued

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay MR to $\overline{TC}_U$	3.3 5.0		12.5 9.0						ns	3-6
t_{PHL}	Propagation Delay MR to $\overline{TC}_D$	3.3 5.0		11.0 8.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		11.5 8.5						ns	3-6
t_{PHL}	Propagation Delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		9.5 7.0						ns	3-6
t_{PLH}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		11.5 8.5						ns	3-6
t_{PHL}	Propagation Delay P_n to $\overline{TC}_U$ or $\overline{TC}_D$	3.3 5.0		11.5 8.5						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW, P_n to $\overline{PL}$	3.3 5.0	4.5 3.0				ns	3-9
t_h	Hold Time, HIGH or LOW P_n to $\overline{PL}$	3.3 5.0	−0.5 −0.5				ns	3-9
t_w	$\overline{PL}$ Pulse Width, LOW	3.3 5.0	8.5 6.0				ns	3-6
t_w	CP_U or CP_D Pulse Width, LOW	3.3 5.0	5.5 4.0				ns	3-6
t_w	CP_U or CP_D Pulse Width, LOW (Change of Direction)	3.3 5.0	9.0 6.5				ns	3-6
t_w	MR Pulse Width, HIGH	3.3 5.0	7.0 5.0				ns	3-6
t_{rec}	Recovery Time $\overline{PL}$ to CP_U or CP_D	3.3 5.0	4.5 3.0				ns	3-9
t_{rec}	Recovery Time MR to CP_U or CP_D	3.3 5.0	8.5 6.0				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC240 • 54ACT/74ACT240

Octal Buffer/Line Driver With 3-State Outputs

Description

The 'AC/'ACT240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Outputs Source/Sink 24 mA**
- **'ACT240 has TTL-Compatible Inputs**

Ordering Code: See Section 6

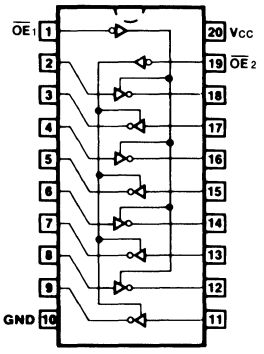
Truth Tables

Inputs		Outputs
$\overline{OE}_1$	D	(Pins 12, 14, 16, 18)
L	L	H
L	H	L
H	X	Z

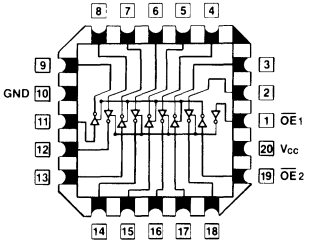
Inputs		Outputs
$\overline{OE}_2$	D	(Pins 3, 5, 7, 9)
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

5

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT240)	1.6	1.5	mA	$V_{IN} = V_{CC}-2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	6.0 4.5	8.0 6.5	1.0 1.0	11.0 8.5	1.0 1.0	9.0 7.0	ns	3-5
t_{PHL}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	5.5 4.5	8.0 6.0	1.0 1.0	10.5 8.0	1.0 1.0	8.5 6.5	ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	6.0 5.0	10.5 7.0	1.0 1.0	11.5 9.0	1.0 1.0	11.0 8.0	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	7.0 5.5	10.0 8.0	1.0 1.0	13.0 10.5	1.0 1.0	11.0 8.5	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	7.0 6.5	10.0 9.0	1.0 1.0	12.5 10.5	1.0 1.0	10.5 9.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	7.5 6.5	10.5 9.0	1.0 1.0	13.5 11.0	1.0 1.0	11.5 9.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	1.0	6.0	8.5	1.0	9.5	1.0	9.5	ns	3-5
t_{PHL}	Propagation Delay Data to Output	5.0	1.0	5.5	7.5	1.0	9.0	1.0	8.5	ns	3-5
t_{PZH}	Output Enable Time	5.0	1.0	7.0	8.5	1.0	10.0	1.0	9.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	7.0	9.5	1.0	11.5	1.0	10.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	8.0	9.5	1.0	11.0	1.0	10.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	6.5	10.0	1.0	11.5	1.0	10.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.5$ V

54AC/74AC241 • 54ACT/74ACT241

Octal Buffer/Line Driver With 3-State Outputs

Description

The 'AC/'ACT241 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter or receiver which provides improved PC board density.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Outputs Source/Sink 24 mA**
- **'ACT241 has TTL-Compatible Inputs**

Ordering Code: See Section 6

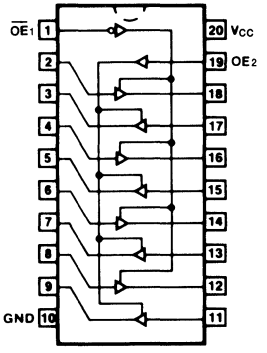
Truth Tables

Inputs		Outputs
$\overline{OE}_1$	D	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

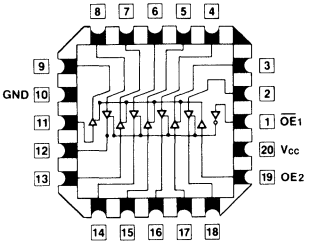
Inputs		Outputs
OE_2	D	(Pins 3, 5, 7, 9)
H	L	L
H	H	H
L	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT241)	1.6	1.5	mA	$V_{IN} = V_{CC}-2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	6.0 5.0	9.0 7.0	1.0 1.0	12.0 9.5	1.0 1.0	10.0 7.5	ns	3-5
t_{PHL}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	6.0 4.5	9.0 7.0	1.0 1.0	11.0 9.0	1.0 1.0	10.5 7.5	ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	6.5 5.5	12.5 9.0	1.0 1.0	13.0 10.0	1.0 1.0	13.0 9.5	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	7.0 5.5	12.0 9.0	1.0 1.0	13.0 10.0	1.0 1.0	13.0 9.5	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	8.0 6.5	12.0 10.0	1.0 1.0	13.0 11.5	1.0 1.0	12.5 10.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	7.0 6.0	12.5 10.0	1.0 1.0	13.0 11.5	1.0 1.0	13.5 10.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	1.0	6.5	9.0	1.0	10.0	1.0	10.0	ns	3-5
t_{PHL}	Propagation Delay Data to Output	5.0	1.0	7.0	9.0	1.0	10.0	1.0	10.0	ns	3-5
t_{PZH}	Output Enable Time	5.0	1.0	6.0	9.0	1.0	11.5	1.0	10.0	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	7.0	10.0	1.0	12.5	1.0	11.0	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	8.0	10.5	1.0	12.5	1.0	11.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	7.0	10.5	1.0	12.5	1.0	11.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.5$ V

54AC/74AC244 • 54ACT/74ACT244

Octal Buffer/Line Driver With 3-State Outputs

Description

The 'AC/'ACT244 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus-oriented transmitter/receiver which provides improved PC board density.

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**
- **Outputs Source/Sink 24 mA**
- **'ACT244 has TTL-Compatible Inputs**

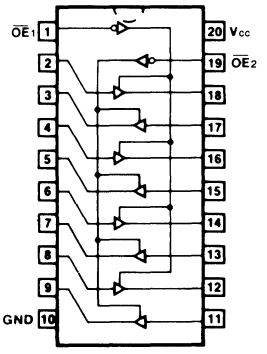
Truth Tables

Inputs		Outputs
$\overline{OE}_1$	D	(Pins 12, 14, 16, 18)
L	L	L
L	H	H
H	X	Z

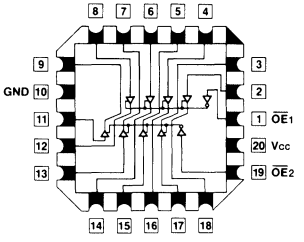
Inputs		Outputs
$\overline{OE}_2$	D	(Pins 3, 5, 7, 9)
L	L	L
L	H	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

5

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT244)	1.6	1.5	mA	$V_{IN} = V_{CC}-2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	6.5 5.0	9.0 7.0	1.0 1.0	12.5 9.5	1.0 1.0	10.0 7.5	ns	3-5
t_{PHL}	Propagation Delay Data to Output	3.3 5.0	1.0 1.0	6.5 5.0	9.0 7.0	1.0 1.0	12.0 9.0	1.0 1.0	10.0 7.5	ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	6.0 5.0	10.5 7.0	1.0 1.0	11.5 9.0	1.0 1.0	11.0 8.0	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	7.5 5.5	10.0 8.0	1.0 1.0	13.0 10.5	1.0 1.0	11.0 8.5	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	7.0 6.5	10.0 9.0	1.0 1.0	12.5 10.5	1.0 1.0	10.5 9.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	7.5 6.5	10.5 9.0	1.0 1.0	13.0 11.0	1.0 1.0	11.5 9.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output	5.0	1.0	6.5	9.0	1.0	10.0	1.0	10.0	ns	3-5
t_{PHL}	Propagation Delay Data to Output	5.0	1.0	7.0	9.0	1.0	10.0	1.0	10.0	ns	3-5
t_{PZH}	Output Enable Time	5.0	1.0	6.0	8.5	1.0	9.5	1.0	9.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	7.0	9.5	1.0	11.0	1.0	10.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	9.5	1.0	11.0	1.0	10.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	7.5	10.0	1.0	11.5	1.0	10.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.5$ V

54AC/74AC245 • 54ACT/74ACT245

Octal Bidirectional Transceiver With 3-State Inputs/Outputs

Description

The 'AC/'ACT245 contains eight non-inverting bidirectional buffers with 3-state outputs and is intended for bus-oriented applications. Current sinking capability is 24 mA at both the A and B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B ports to A ports. The Output Enable input, when HIGH, disables both A and B ports by placing them in a High Z condition.

- **Noninverting Buffers**
- **Bidirectional Data Path**
- **A and B Outputs Source/Sink 24 mA**
- **'ACT245 has TTL-Compatible Inputs**

Ordering Code: See Section 6

Pin Names

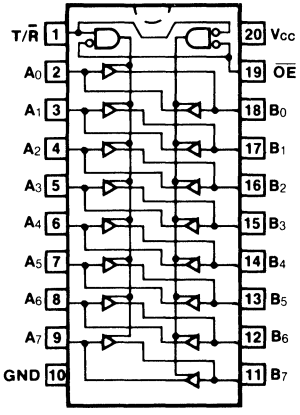
$\overline{OE}$	Output Enable Input
$T/\overline{R}$	Transmit/Receive Input
A_0 - A_7	Side A 3-State Inputs or 3-State Outputs
B_0 - B_7	Side B 3-State Inputs or 3-State Outputs

Truth Table

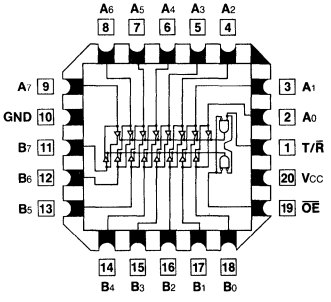
Inputs		Outputs
$\overline{OE}$	$T/\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT245)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	3.3	1.0	5.0	8.5	1.0	11.5	1.0	9.0	ns	3-5
		5.0	1.0	3.5	6.5	1.0	8.5	1.0	7.0		
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	3.3	1.0	5.0	8.5	1.0	10.0	1.0	9.0	ns	3-5
		5.0	1.0	3.5	6.0	1.0	7.5	1.0	7.0		
t_{PZH}	Output Enable Time	3.3	1.0	7.0	11.5	1.0	13.5	1.0	12.5	ns	3-7
		5.0	1.0	5.0	8.5	1.0	10.0	1.0	9.0		
t_{PZL}	Output Enable Time	3.3	1.0	7.5	12.0	1.0	14.5	1.0	13.5	ns	3-8
		5.0	1.0	5.5	9.0	1.0	10.5	1.0	9.5		
t_{PHZ}	Output Disable Time	3.3	1.0	6.5	12.0	1.0	13.5	1.0	12.5	ns	3-7
		5.0	1.0	5.5	9.0	1.0	10.5	1.0	10.0		
t_{PLZ}	Output Disable Time	3.3	1.0	7.0	11.5	1.0	14.0	1.0	13.0	ns	3-8
		5.0	1.0	5.5	9.0	1.0	10.5	1.0	10.0		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	5.0	1.0	4.0	7.5	1.0	9.0	1.0	8.0	ns	3-5
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	5.0	1.0	4.0	8.0	1.0	10.0	1.0	9.0	ns	3-5
t_{PZH}	Output Enable Time	5.0	1.0	5.0	10.0	1.0	12.0	1.0	11.0	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	5.5	10.0	1.0	13.0	1.0	12.0	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	5.5	10.0	1.0	12.0	1.0	11.0	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	5.0	10.0	1.0	12.0	1.0	11.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
$C_{I/O}$	Input/Output Capacitance	15.0	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	45.0	pF	$V_{CC} = 5.5$ V

54AC/74AC251 • 54ACT/74ACT251

8-Input Multiplexer With 3-State Outputs

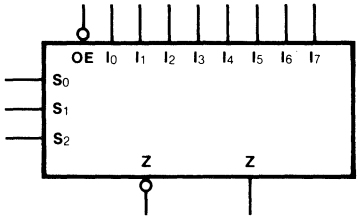
Description

The 'AC/'ACT251 is a high-speed 8-input digital multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. It can be used as universal function generator to generate any logic function of four variables. Both true and complementary outputs are provided.

- **Multifunctional Capability**
- **On-Chip Select Logic Decoding**
- **Inverting and Noninverting 3-State Outputs**
- **Outputs Source/Sink 24 mA**
- **'ACT251 has TTL-Compatible Inputs**

Ordering Code: See Section 6

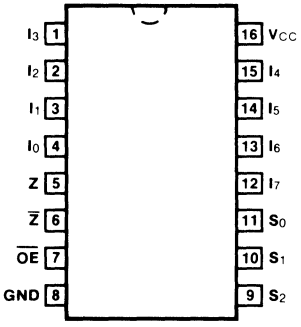
Logic Symbol



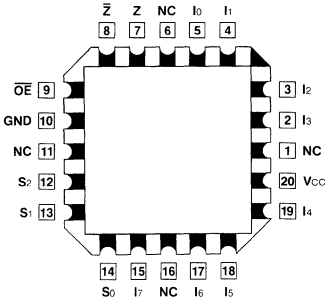
Pin Names

S_0 - S_2	Select Inputs
$\overline{OE}$	3-State Output Enable Input
I_0 - I_7	Multiplexer Inputs
Z	3-State Multiplexer Output
$\overline{Z}$	Complementary 3-State Multiplexer Output

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

5

Functional Description

This device is a logical implementation of a single-pole, 8-position switch with the switch position controlled by the state of three Select inputs, S_0, S_1, S_2. Both true and complementary outputs are provided. The Output Enable input ($\overline{OE}$) is active LOW. When it is activated, the logic function provided at the output is:

$$Z = \overline{OE} \bullet (I_0 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_1 \bullet S_0 \bullet \overline{S}_1 \bullet \overline{S}_2 + I_2 \bullet \overline{S}_0 \bullet S_1 \bullet \overline{S}_2 + I_3 \bullet S_0 \bullet S_1 \bullet \overline{S}_2 + I_4 \bullet \overline{S}_0 \bullet \overline{S}_1 \bullet S_2 + I_5 \bullet S_0 \bullet \overline{S}_1 \bullet S_2 + I_6 \bullet \overline{S}_0 \bullet S_1 \bullet S_2 + I_7 \bullet S_0 \bullet S_1 \bullet S_2)$$

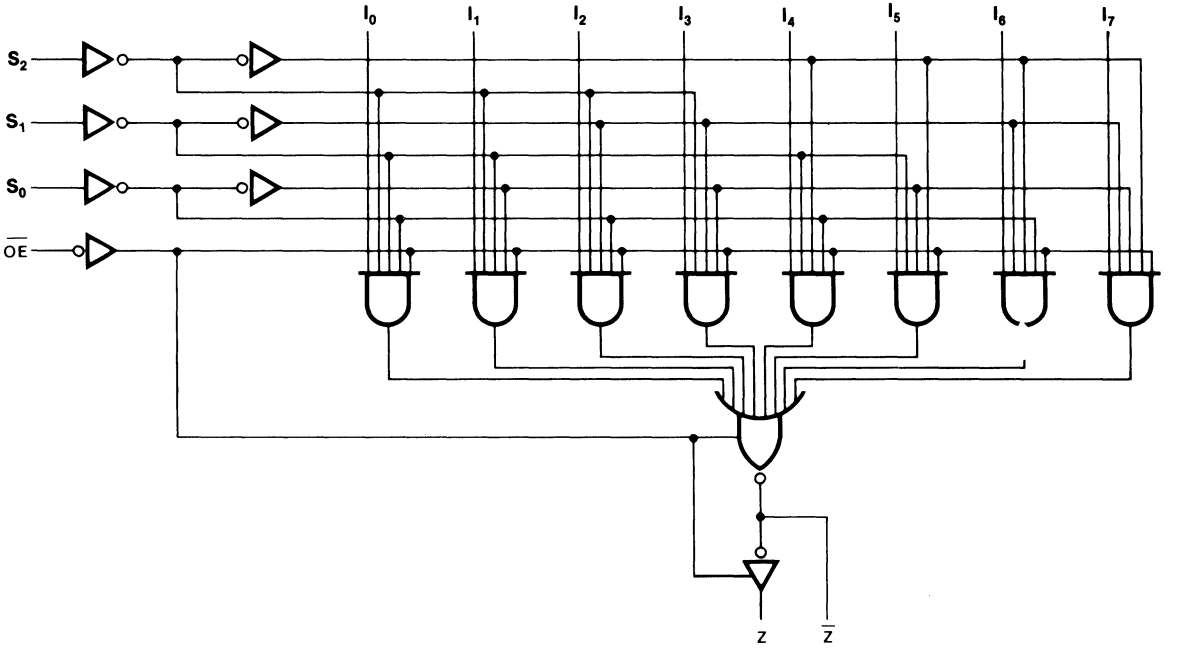
When the Output Enable is HIGH, both outputs are in the high impedance (High Z) state. This feature allows multiplexer expansion by tying the outputs of up to 128 devices together. When the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. The Output Enable signals should be designed to ensure there is no overlap in the active-LOW portion of the enable voltages.

Truth Table

Inputs				Outputs	
$\overline{OE}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	Z	Z
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT251)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	1.0	11.5	17.5	1.0	21.0	1.0	19.0	ns	3-6
		5.0	1.0	8.5	12.5	1.0	15.5	1.0	13.5		
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	3.3	1.0	11.0	17.5	1.0	21.0	1.0	19.0	ns	3-6
		5.0	1.0	8.0	12.5	1.0	15.5	1.0	13.5		
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	1.0	10.0	14.0	1.0	17.0	1.0	15.5	ns	3-5
		5.0	1.0	7.0	10.0	1.0	12.0	1.0	11.0		
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	3.3	1.0	9.0	14.0	1.0	16.5	1.0	15.5	ns	3-5
		5.0	1.0	6.5	10.0	1.0	12.0	1.0	11.0		
t_{PZH}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.0	7.5	11.0	1.0	13.0	1.0	12.0	ns	3-7
		5.0	1.0	5.5	8.0	1.0	10.0	1.0	9.0		
t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	1.0	7.5	11.0	1.0	13.0	1.0	12.0	ns	3-8
		5.0	1.0	5.5	8.0	1.0	10.0	1.0	9.0		
t_{PHZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	3.5	8.5	11.5	3.5	14.0	3.5	13.0	ns	3-7
		5.0	2.5	7.0	9.5	2.5	11.0	2.5	10.0		
t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	3.3	4.0	7.0	11.0	4.0	13.0	4.0	12.0	ns	3-8
		5.0	3.0	5.5	8.0	3.0	10.0	3.0	8.5		

*Voltage Range 3.3 is 3.3 V ±0.3 V
Voltage Range 5.0 is 5.0 V ±0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z or $\overline{Z}$	5.0	1.0	7.0	13.5	1.0	16.5	1.0	13.0	ns	3-6
t_{PHL}	Propagation Delay S_n to Z or $\overline{Z}$	5.0	1.0	7.5	13.0	1.0	16.0	1.0	14.5	ns	3-6
t_{PLH}	Propagation Delay I_n to Z or $\overline{Z}$	5.0	1.0	5.5	10.0	1.0	13.0	1.0	10.5	ns	3-5
t_{PHL}	Propagation Delay I_n to Z or $\overline{Z}$	5.0	1.0	6.5	10.5	1.0	13.0	1.0	12.0	ns	3-5
t_{PZH}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.0	5.0	9.0	1.0	11.0	1.0	9.0	ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.0	4.5	9.0	1.0	11.0	1.0	8.5	ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.0	6.0	10.5	1.0	12.0	1.0	10.0	ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to Z or $\overline{Z}$	5.0	1.0	4.5	9.0	1.0	11.0	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	70.0	pF	$V_{CC} = 5.5$ V

54AC/74AC253 • 54ACT/74ACT253

Dual 4-Input Multiplexer With 3-State Outputs

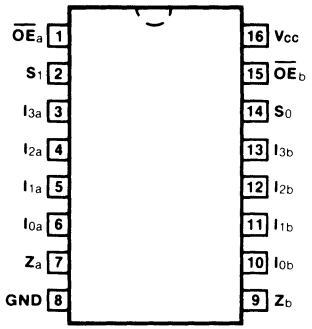
Description

The 'AC/'ACT253 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus oriented systems.

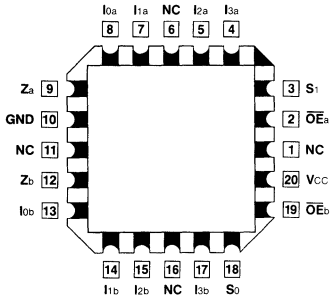
- **Multifunction Capability**
- **Noninverting 3-State Outputs**
- **Outputs Source/Sink 24 mA**
- **'ACT253 has TTL-Compatible Inputs**

Ordering Code: See Section 6

Connection Diagrams

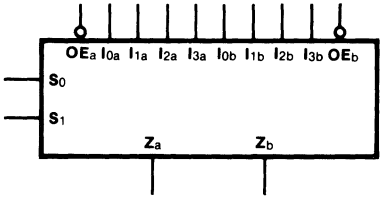


Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Logic Symbol



Pin Names

I_{0a} - I_{3a}	Side A Data Inputs
I_{0b} - I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
Z_a, Z_b	3-State Outputs

5

Functional Description

The 'AC/'ACT253 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. This device is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown:

$$Z_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$Z_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

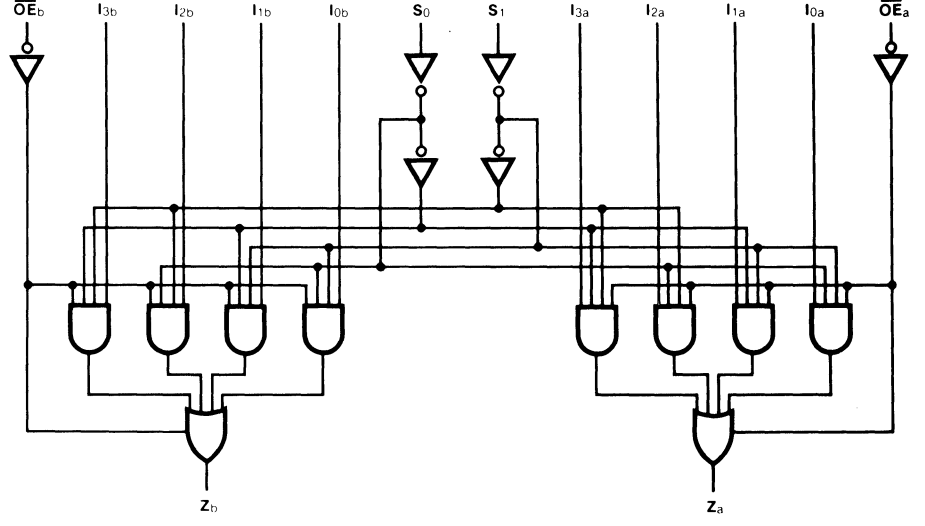
Truth Table

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Z
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs S_0 and S_1 are common to both sections.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT253)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

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Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	3.3	1.0	8.5	15.5	1.0	19.5	1.0	17.5	ns	3-6
		5.0	1.0	6.5	11.0	1.0	13.5	1.0	12.5		
t_{PHL}	Propagation Delay S_n to Z_n	3.3	1.0	9.5	16.0	1.0	20.0	1.0	18.0	ns	3-6
		5.0	1.0	7.0	11.5	1.0	15.0	1.0	13.0		
t_{PLH}	Propagation Delay I_n to Z_n	3.3	1.0	7.0	14.5	1.0	19.0	1.0	17.0	ns	3-5
		5.0	1.0	5.5	10.0	1.0	13.0	1.0	11.5		
t_{PHL}	Propagation Delay I_n to Z_n	3.3	1.0	7.5	13.0	1.0	16.0	1.0	15.0	ns	3-5
		5.0	1.0	5.5	9.5	1.0	12.0	1.0	11.0		
t_{PZH}	Output Enable Time	3.3	1.0	4.5	8.0	1.0	9.5	1.0	8.5	ns	3-7
		5.0	1.0	3.5	6.0	1.0	7.0	1.0	6.5		
t_{PZL}	Output Enable Time	3.3	1.0	5.0	8.0	1.0	10.0	1.0	9.0	ns	3-8
		5.0	1.0	3.5	6.0	1.0	7.5	1.0	7.0		
t_{PHZ}	Output Disable Time	3.3	1.0	5.5	9.5	1.0	11.0	1.0	10.0	ns	3-7
		5.0	1.0	5.0	8.0	1.0	9.5	1.0	8.5		
t_{PLZ}	Output Disable Time	3.3	1.0	5.0	8.0	1.0	9.5	1.0	9.0	ns	3-8
		5.0	1.0	4.0	7.0	1.0	8.0	1.0	7.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF			$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF			
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to Z_n	5.0	1.0	7.0	11.5	1.0	14.5	1.0	13.0	ns	3-6
t_{PHL}	Propagation Delay S_n to Z_n	5.0	1.0	7.5	13.0	1.0	16.0	1.0	14.5	ns	3-6
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.0	5.5	10.0	1.0	12.0	1.0	11.0	ns	3-5
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.0	6.5	11.0	1.0	13.5	1.0	12.5	ns	3-5
t_{PZH}	Output Enable Time	5.0	1.0	4.5	7.5	1.0	9.5	1.0	8.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	5.0	8.0	1.0	9.5	1.0	9.0	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	6.0	9.5	1.0	11.0	1.0	10.0	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	4.5	7.5	1.0	9.0	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.5$ V

54AC/74AC257 • 54ACT/74ACT257

Quad 2-Input Multiplexer With 3-State Outputs

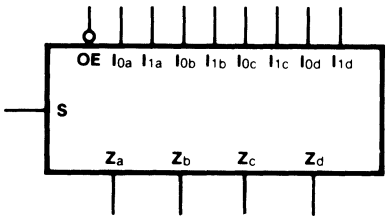
Description

The 'AC/'ACT257 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a Common Data Select input. The four outputs present the selected data in true (noninverted) form. The outputs may be switched to a high impedance state by placing a logic HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented systems.

- **Multiplexer Expansion by Tying Outputs Together**
- **Noninverting 3-State Outputs**
- **Outputs Source/Sink 24 mA**
- **'ACT257 has TTL-Compatible Inputs**

Ordering Code: See Section 6

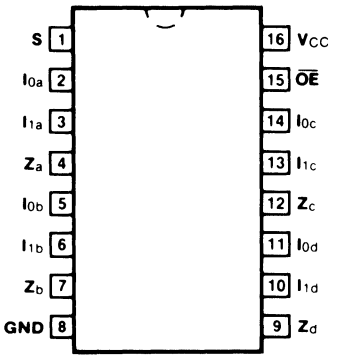
Logic Symbol



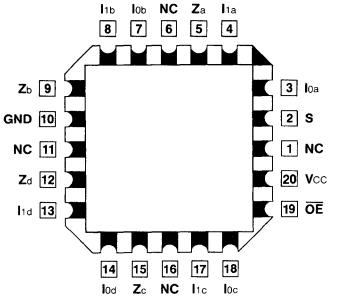
Pin Names

S	Common Data Select Input
$\overline{OE}$	3-State Output Enable Input
I_{0a} - I_{0d}	Data Inputs from Source 0
I_{1a} - I_{1d}	Data Inputs from Source 1
Z_a - Z_d	3-State Multiplexer Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

The 'AC/'ACT257 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a Common Data Select input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in true (noninverted) form. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$Z_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$Z_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$Z_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$Z_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

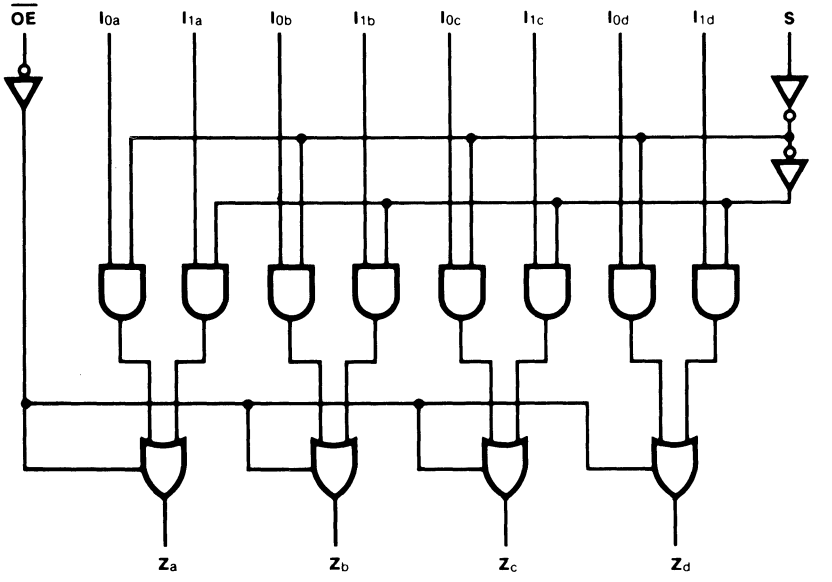
When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure the Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	Z
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT257)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay In to Zn	3.3 5.0		5.0 4.0						ns	3-5
t_{PHL}	Propagation Delay In to Zn	3.3 5.0		6.0 4.5						ns	3-5
t_{PLH}	Propagation Delay S to Zn	3.3 5.0		7.0 5.0						ns	3-6
t_{PHL}	Propagation Delay S to Zn	3.3 5.0		7.5 5.5						ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		6.5 5.0						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		5.5 5.0						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		5.5 5.0						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		5.5 5.0						ns	3-8

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to Z_n	5.0	1.0	5.0	7.0	1.0	8.0	1.0	7.5	ns	3-6
t_{PHL}	Propagation Delay I_n to Z_n	5.0	1.0	6.0	7.5	1.0	9.5	1.0	8.5	ns	3-6
t_{PLH}	Propagation Delay S to Z_n	5.0	1.0	7.0	9.5	1.0	11.5	1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay S to Z_n	5.0	1.0	7.0	10.5	1.0	12.5	1.0	11.5	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	6.0	8.0	1.0	9.5	1.0	9.0	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	6.0	8.0	1.0	9.5	1.0	9.0	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	6.5	9.0	1.0	10.5	1.0	10.0	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	6.0	7.5	1.0	9.0	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.5$ V

54AC/74AC258 • 54ACT/74ACT258

Quad 2-Input Multiplexer With 3-State Outputs

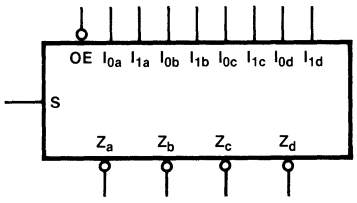
Description

The 'AC/'ACT258 is a quad 2-input multiplexer with 3-state outputs. Four bits of data from two sources can be selected using a common data select input. The four outputs present the selected data in the complement (inverted) form. The outputs may be switched to a high impedance state with a HIGH on the common Output Enable ($\overline{OE}$) input, allowing the outputs to interface directly with bus-oriented sytems.

- **Multiplexer Expansion by Tying Outputs Together**
- **Inverting 3-State Outputs**
- **Outputs Source/Sink 24 mA**
- **'ACT258 has TTL-Compatible Inputs**

Ordering Code: See Section 6

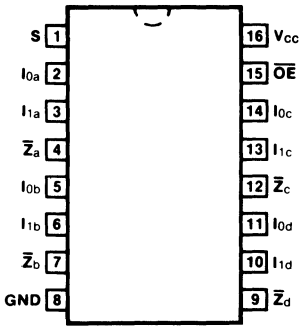
Logic Symbol



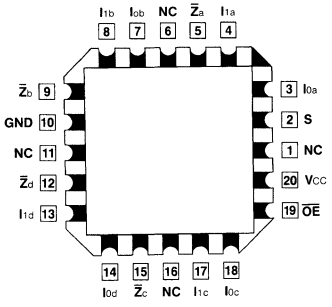
Pin Names

S	Common Data Select Input
$\overline{OE}$	3-State Output Enable Input
I_{0a} - I_{0d}	Data Inputs from Source 0
I_{1a} - I_{1d}	Data Inputs from Source 1
$\overline{Z}_a$ - $\overline{Z}_d$	3-State Inverting Data Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

The 'AC/'ACT258 is a quad 2-input multiplexer with 3-state outputs. It selects four bits of data from two sources under control of a common Select input (S). When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The data on the selected inputs appears at the outputs in inverted form. The 'AC/'ACT258 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE} \bullet (I_{1a} \bullet S + I_{0a} \bullet \overline{S})$$
$$\overline{Z}_b = \overline{OE} \bullet (I_{1b} \bullet S + I_{0b} \bullet \overline{S})$$
$$\overline{Z}_c = \overline{OE} \bullet (I_{1c} \bullet S + I_{0c} \bullet \overline{S})$$
$$\overline{Z}_d = \overline{OE} \bullet (I_{1d} \bullet S + I_{0d} \bullet \overline{S})$$

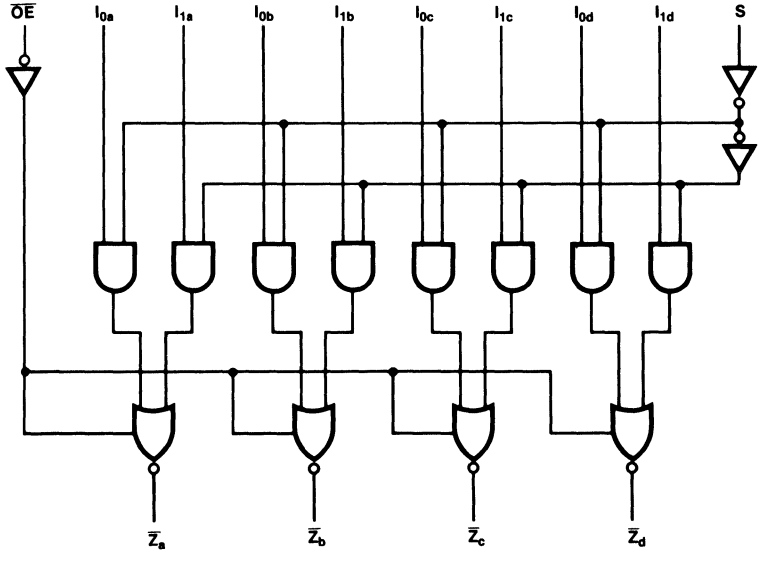
When the Output Enable input ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs of the 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	$\overline{Z}$
H	X	X	X	Z
L	H	X	L	H
L	H	X	H	L
L	L	L	X	H
L	L	H	X	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT258)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3	1.0	6.0	9.5	1.0	12.0	1.0	11.0	ns	3-5
		5.0	1.0	4.5	7.5	1.0	9.5	1.0	8.5		
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3	1.0	5.0	8.5	1.0	10.5	1.0	9.5	ns	3-5
		5.0	1.0	4.0	6.5	1.0	7.5	1.0	7.0		
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	3.3	1.0	7.5	12.0	1.0	15.0	1.0	14.0	ns	3-6
		5.0	1.0	6.0	9.5	1.0	12.0	1.0	10.5		
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	3.3	1.0	7.5	11.5	1.0	14.0	1.0	13.0	ns	3-6
		5.0	1.0	5.5	9.0	1.0	10.5	1.0	10.0		
t_{PZH}	Output Enable Time	3.3	1.0	6.0	9.5	1.0	11.5	1.0	10.5	ns	3-7
		5.0	1.0	4.5	7.5	1.0	9.0	1.0	8.5		
t_{PZL}	Output Enable Time	3.3	1.0	5.5	9.0	1.0	10.5	1.0	10.0	ns	3-8
		5.0	1.0	5.5	7.0	1.0	8.5	1.0	8.0		
t_{PHZ}	Output Disable Time	3.3	1.0	5.5	10.0	1.0	11.5	1.0	11.5	ns	3-7
		5.0	1.0	5.5	8.5	1.0	9.5	1.0	9.0		
t_{PLZ}	Output Disable Time	3.3	1.0	5.5	9.0	1.0	10.5	1.0	10.0	ns	3-8
		5.0	1.0	5.0	7.0	1.0	8.5	1.0	8.0		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.0	6.5	8.5			1.0	9.5	ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0	1.0	5.5	7.5			1.0	8.0	ns	3-5
t_{PLH}	Propagation Delay S to $\overline{Z}_n$	5.0	1.0	7.5	10.5			1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay S to $\overline{Z}_n$	5.0	1.0	7.0	9.5			1.0	11.0	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	6.5	8.5			1.0	9.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	6.5	8.5			1.0	9.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	9.0			1.0	10.0	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	6.0	8.0			1.0	9.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	55.0	pF	$V_{CC} = 5.5$ V

54AC/74AC273 • 54ACT/74ACT273

Octal D Flip-Flop

Description

The 'AC/'ACT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

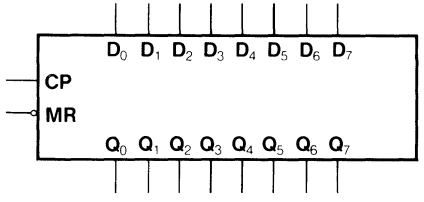
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

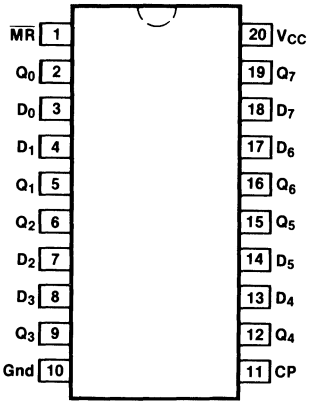
- **Ideal Buffer for MOS Microprocessor or Memory**
- **Eight Edge-Triggered D Flip-Flops**
- **Buffered Common Clock**
- **Buffered, Asynchronous Master Reset**
- **See '377 for Clock Enable Version**
- **See '373 for Transparent Latch Version**
- **See '374 for 3-State Version**
- **Outputs Source/Sink 24 mA**
- **'ACT273 has TTL-Compatible Inputs**

Ordering Code: See Section 6

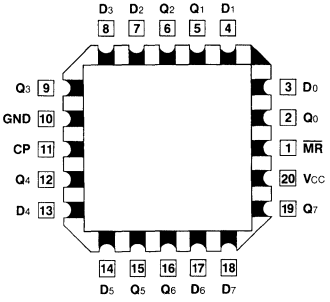
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC

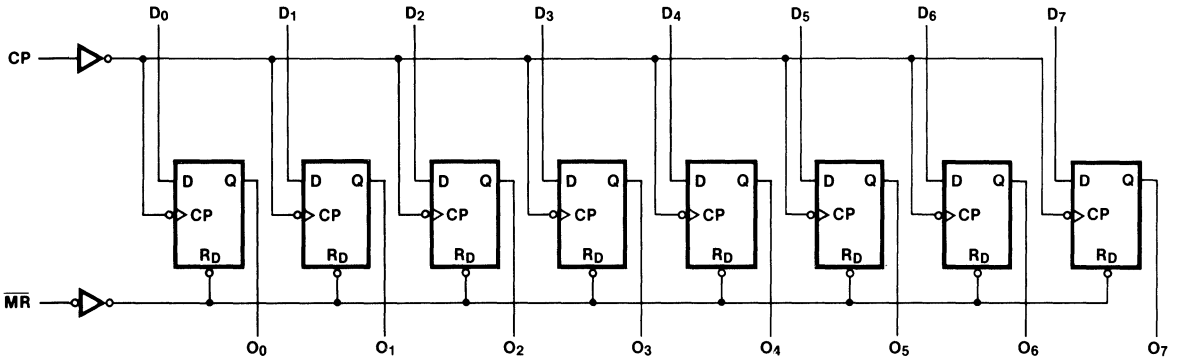


Pin Assignment for LCC

Pin Names

D_0 - D_7	Data Inputs
$\overline{MR}$	Master Reset
CP	Clock Pulse Input
Q_0 - Q_7	Data Outputs

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	$\overline{MR}$	CP	Dn	Qn
Reset (Clear)	L	X	X	L
Load '1'	H	⌐	H	H
Load '0'	H	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT273)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	90 140	125 175		75 95		75 125		MHz	3-3
t_{PLH}	Propagation Delay Clock to Output	3.3 5.0	1.0 1.0	7.0 5.5	12.5 9.0	1.0 1.0	19.0 11.0	1.0 1.0	14.0 10.0	ns	3-6
t_{PHL}	Propagation Delay Clock to Output	3.3 5.0	1.0 1.0	7.0 5.0	13.0 10.0	1.0 1.0	16.0 11.5	1.0 1.0	14.5 11.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Output	3.3 5.0	1.0 1.0	7.0 5.0	13.0 10.0	1.0 1.0	16.0 11.5	1.0 1.0	14.0 10.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW, Data to CP	3.3 5.0	3.5 2.5	5.5 4.0	6.5 5.0	6.0 4.5	ns	3-9
t_h	Hold Time, HIGH or LOW Data to CP	3.3 5.0	−2.0 −1.0	0 1.0	0 1.0	0 1.0	ns	3-9
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5	5.5 4.0	6.5 5.0	6.0 4.5	ns	3-6
t_w	$\overline{MR}$ Pulse Width HIGH or LOW	3.3 5.0	2.0 1.5	5.5 4.0	6.5 5.0	6.0 4.5	ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	3.3 5.0	1.5 1.0	3.5 2.0	4.5 3.0	4.5 3.0	ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		200						MHz	3-3
t_{PLH}	Propagation Delay Clock to Output	5.0		6.0						ns	3-6
t_{PHL}	Propagation Delay Clock to Output	5.0		6.5						ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Output	5.0		7.0						ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW, Data to CP	5.0	3.0				ns	3-9
t_h	Hold Time, HIGH or LOW Data to CP	5.0	−2.5				ns	3-9
t_w	Clock Pulse Width HIGH or LOW	5.0	2.5				ns	3-6
t_w	$\overline{MR}$ Pulse Width, HIGH or LOW	5.0	2.5				ns	3-6
t_{rec}	Recovery Time $\overline{MR}$ to CP	5.0	−1.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.5$ V

5

54AC/74AC299 • 54ACT/74ACT299

8-Input Universal Shift/Storage Register With Common Parallel I/O Pins

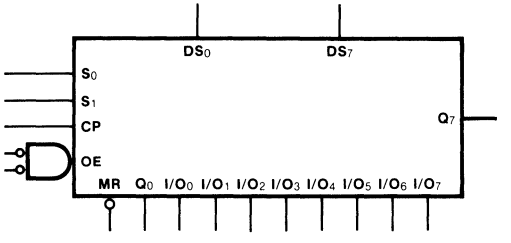
Description

The 'AC/'ACT299 is an 8-bit universal shift/storage register with 3-state outputs. Four modes of operation are possible: hold (store), shift left, shift right and load data. The parallel load inputs and flip-flop outputs are multiplexed to reduce the total number of package pins. Additional outputs are provided for flip-flops Q_0, Q_7 to allow easy serial cascading. A separate active LOW Master Reset is used to reset the register.

- **Common Parallel I/O for Reduced Pin Count**
- **Additional Serial Inputs and Outputs for Expansion**
- **Four Operating Modes: Shift Left, Shift Right, Load and Store**
- **3-State Outputs for Bus-Oriented Applications**
- **Outputs Source/Sink 24 mA**
- **'ACT299 has TTL-Compatible Inputs**

Ordering Code: See Section 6

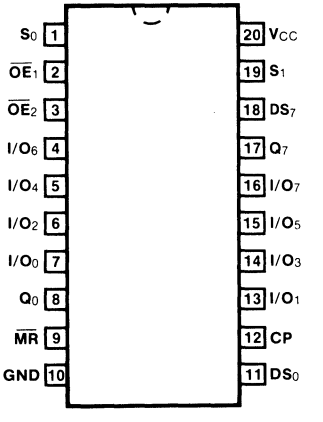
Logic Symbol



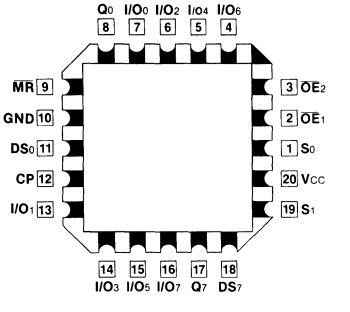
Pin Names

CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{MR}$	Asynchronous Master Reset
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs
I/O_0 - I/O_7	Parallel Data Inputs or 3-State Parallel Outputs
Q_0, Q_7	Serial Outputs

Connection Diagrams

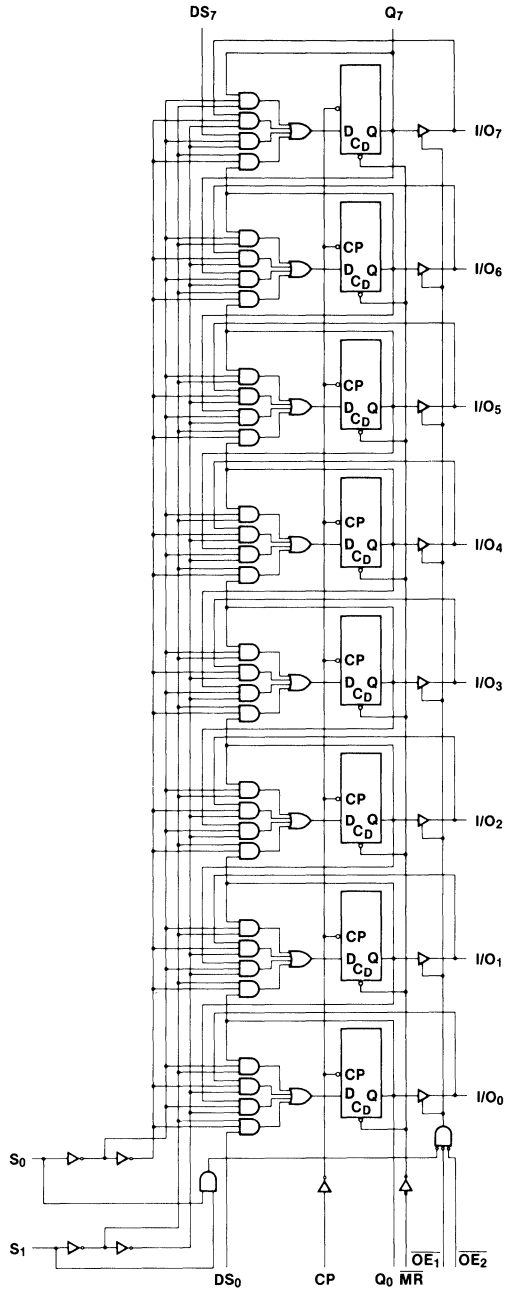


Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'AC/'ACT299 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1, as shown in the Truth Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{MR}$ overrides the Select and CP inputs and resets the flip-flops. All other state changes are initiated by the rising edge of the clock. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Truth Table

Inputs				Response
$\overline{MR}$	S_1	S_0	CP	
L	X	X	X	Asynchronous Reset; Q_0 - Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT299)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	3.3 5.0		55 130						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	3.3 5.0		31.0 12.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	3.3 5.0		30.0 13.0						ns	3-6
t_{PLH}	Propagation Delay CP to I/O_n	3.3 5.0		28.0 11.0						ns	3-6
t_{PHL}	Propagation Delay CP to I/O_n	3.3 5.0		28.0 12.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to I/O_n	3.3 5.0		33.0 14.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to I/O_n	3.3 5.0		31.0 13.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to I/O_n	3.3 5.0		24.0 10.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	3.3 5.0		24.0 10.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to I/O_n	3.3 5.0		25.0 13.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	3.3 5.0		24.0 12.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	12.0 5.0				ns	3-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	0 0				ns	3-9
t_s	Setup Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	3.3 5.0	6.0 3.0				ns	3-9
t_h	Hold Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	3.3 5.0	0 0				ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	9.0 4.0				ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	7.0 4.0				ns	3-6
t_{rec}	Recovery Time, $\overline{MR}$ to CP	3.3 5.0	0 0				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	5.0		125						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	5.0		11.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	5.0		12.0						ns	3-6
t_{PLH}	Propagation Delay CP to I/O_n	5.0		10.0						ns	3-6
t_{PHL}	Propagation Delay CP to I/O_n	5.0		12.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	5.0		14.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_0 or Q_7	5.0		13.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to I/O_n	5.0		10.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to I/O_n	5.0		10.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to I/O_n	5.0		12.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to I/O_n	5.0		11.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

5

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	5.0				ns	3-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	0				ns	3-9
t_s	Setup Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	5.0	3.0				ns	3-9
t_h	Hold Time, HIGH or LOW I/O_n, DS_0 or DS_7 to CP	5.0	0				ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	4.0				ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0	4.0				ns	3-6
t_{rec}	Recovery Time, $\overline{MR}$ to CP	5.0	0				ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC323 • 54ACT/74ACT323

8-Bit Universal Shift/Storage Register With Synchronous Reset and Common I/O Pins

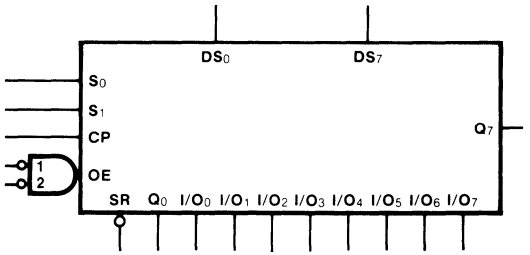
Description

The 'AC/'ACT323 is an 8-bit universal shift/storage register with 3-state outputs. Its function is similar to the 'AC/'ACT299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

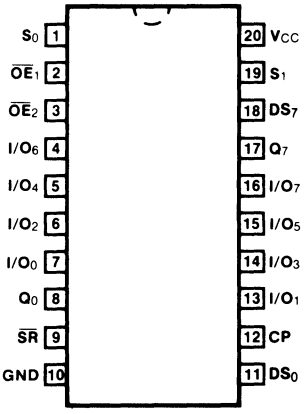
- **Common Parallel I/O for Reduced Pin Count**
- **Additional Serial Inputs and Outputs for Expansion**
- **Four Operating Modes: Shift Left, Shift Right, Load and Store**
- **3-State Outputs for Bus-Oriented Applications**
- **Outputs Source/Sink 24mA**
- **'ACT323 has TTL-Compatible Inputs**

Ordering Code: See Section 6

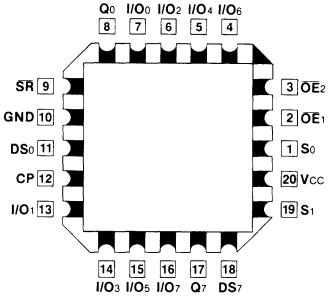
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC

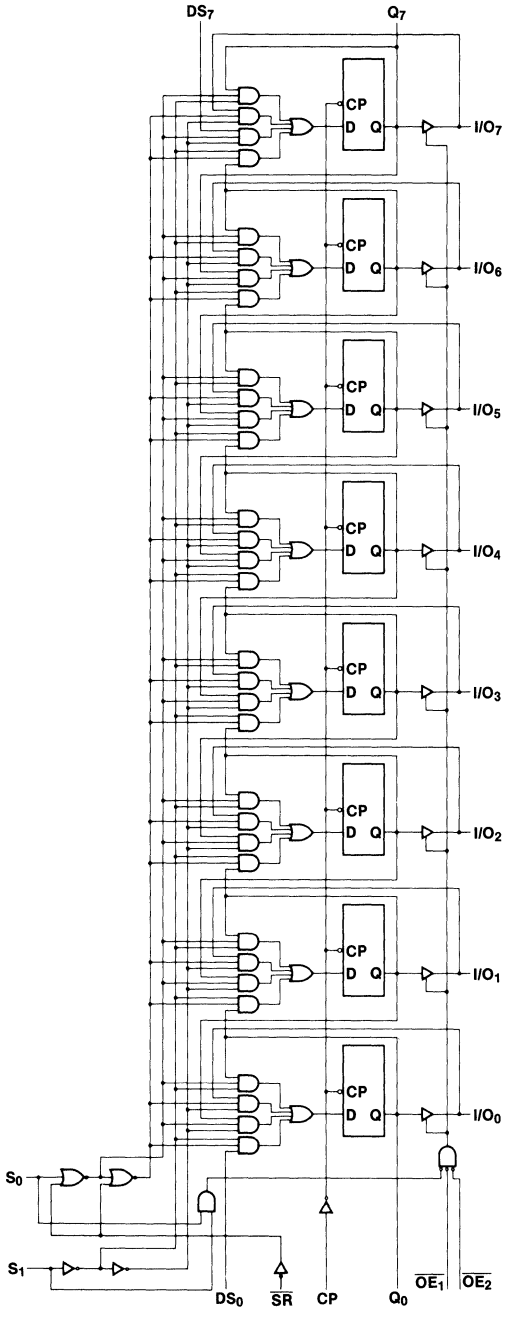


Pin Assignment for LCC

Pin Names

CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{SR}$	Synchronous Reset Input
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable Inputs
I/O_0 - I/O_7	Multiplexed Parallel Data Inputs or 3-State Parallel Data Outputs
Q_0, Q_7	Serial Outputs

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Functional Description

The 'AC/'ACT323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
$\overline{SR}$	S_1	S_0	CP	
L	X	X	⌐	Synchronous Reset; Q_0-Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT323)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	3.3 5.0		55 130						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	3.3 5.0		31.0 12.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	3.3 5.0		30.0 13.0						ns	3-6
t_{PLH}	Propagation Delay CP to I/O_n	3.3 5.0		28.0 11.0						ns	3-6
t_{PHL}	Propagation Delay CP to I/O_n	3.3 5.0		28.0 12.0						ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		24.0 10.0						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		24.0 10.0						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		25.0 13.0						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		24.0 12.0						ns	3-8

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	12.0 5.0				ns	3-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	3.3 5.0	0 0				ns	3-9
t_s	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	3.3 5.0	5.0 5.0				ns	3-9
t_h	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	3.3 5.0	0 0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	4.0 2.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	0 0				ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	9.0 4.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Input Frequency	5.0		125						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	5.0		12.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	5.0		13.0						ns	3-6
t_{PLH}	Propagation Delay CP to I/O_n	5.0		10.0						ns	3-6
t_{PHL}	Propagation Delay CP to I/O_n	5.0		12.0						ns	3-6
t_{PZH}	Output Enable Time	5.0		10.0						ns	3-7
t_{PZL}	Output Enable Time	5.0		10.0						ns	3-8
t_{PHZ}	Output Disable Time	5.0		12.0						ns	3-7
t_{PLZ}	Output Disable Time	5.0		11.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	5.0				ns	3-9
t_h	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	0				ns	3-9
t_s	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	3.0				ns	3-9
t_h	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	2.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	0				ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	4.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC352 • 54ACT/74ACT352

Dual 4-Input Multiplexer

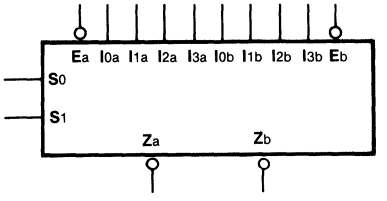
Description

The 'AC/'ACT352 is a very high-speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The 'AC/'ACT352 is the functional equivalent of the 'AC/'ACT153 except with inverted outputs.

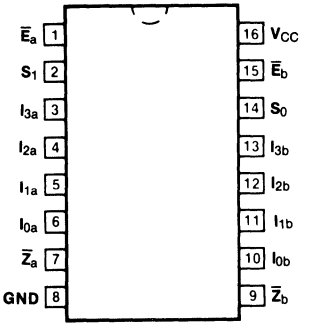
- **Inverted Version of the 'AC/'ACT153**
- **Separate Enables for Each Multiplexer**
- **Outputs Source/Sink 24 mA**
- **'ACT352 has TTL-Compatible Inputs**

Ordering Code: See Section 6

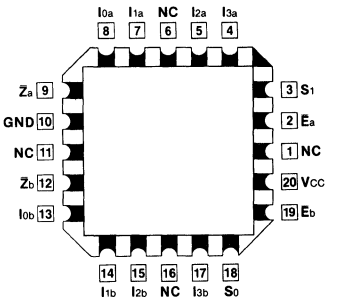
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Pin Names

I0a - I3a	Side A Data Inputs
I0b - I3b	Side B Data Inputs
S0, S1	Common Select Inputs
Ēa	Side A Enable Input
Ēb	Side B Enable Input
Z̄a, Z̄b	Multiplexer Outputs

Functional Description

The 'AC/'ACT352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs ($\overline{Z}_a$, $\overline{Z}_b$) are forced HIGH.

The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$\overline{Z}_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

The 'AC/'ACT352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'AC/ACT352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

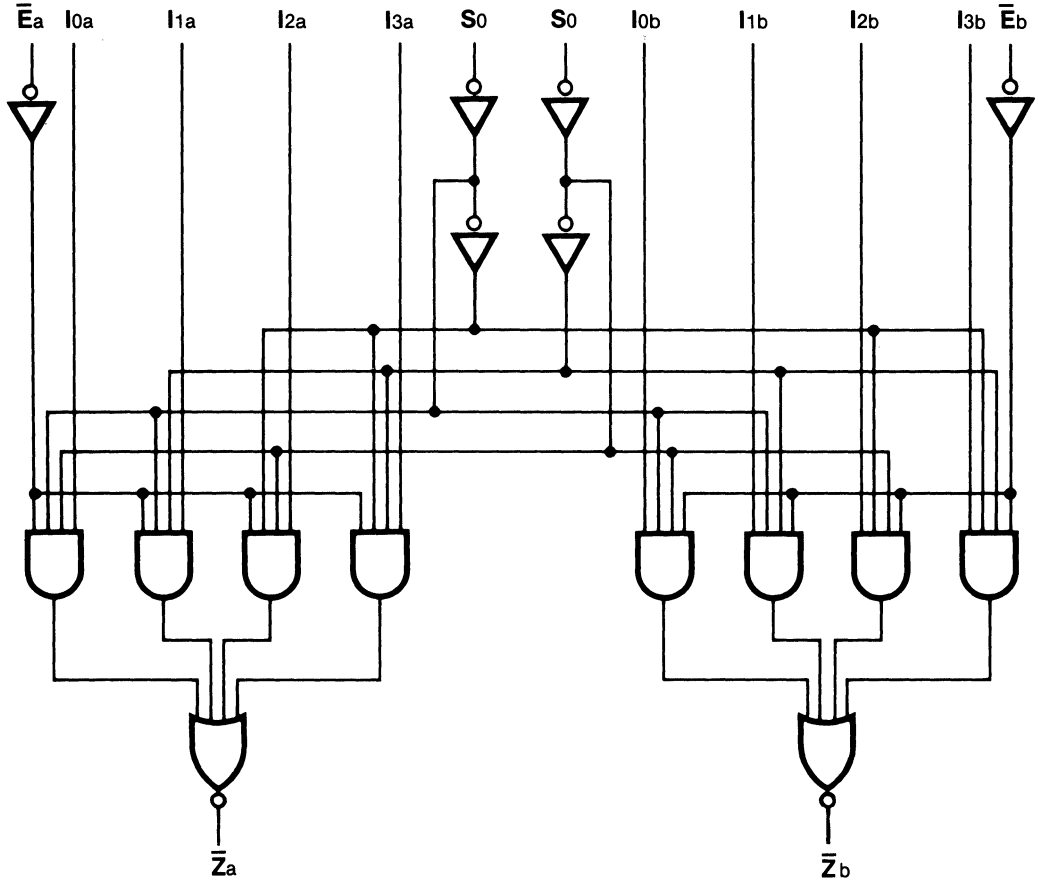
5

Truth Table

Select Inputs		Inputs (a or b)					Outputs
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	$\overline{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT352)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to $\overline{Z}_n$	3.3 5.0		9.0 6.5						ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	3.3 5.0		9.0 6.5						ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	3.3 5.0		6.5 5.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	3.3 5.0		6.5 5.0						ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0		8.5 6.0						ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0		8.5 6.0						ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

5

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to $\overline{Z}_n$	5.0		7.0						ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	5.0		7.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	5.0		5.5						ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	5.0		5.5						ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0		6.5						ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0		6.5						ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC353 • 54ACT/74ACT353

Dual 4-Input Multiplexer With 3-State Outputs

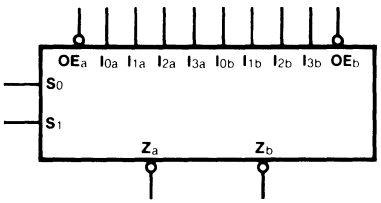
Description

The 'AC/'ACT353 is a dual 4-input multiplexer with 3-state outputs. It can select two bits of data from four sources using common Select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ($\overline{OE}$) inputs, allowing the outputs to interface directly with bus-oriented systems.

- **Inverted Version of the 'AC/'ACT253**
- **Multifunction Capability**
- **Separate Enables for Each Multiplexer**
- **Outputs Source/Sink 24 mA**
- **'ACT353 has TTL-Compatible Inputs**

Ordering Code: See Section 6

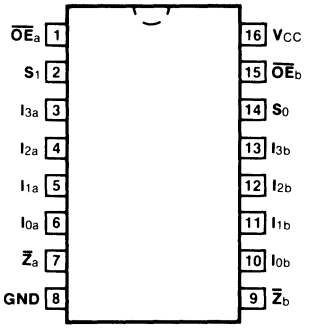
Logic Symbol



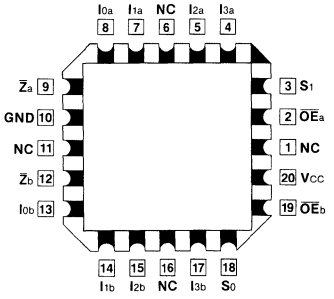
Pin Names

I_{0a} - I_{3a}	Side A Data Inputs
I_{0b} - I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{OE}_a$	Side A Output Enable Input
$\overline{OE}_b$	Side B Output Enable Input
$\overline{Z}_a$, $\overline{Z}_b$	3-State Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC and PCC

5

Functional Description

The 'AC/'ACT353 contains two identical 4-input multiplexers with 3-state outputs. They select two bits from four sources selected by common Select inputs (S_0, S_1). The 4-input multiplexers have individual Output Enable ($\overline{OE}_a$, $\overline{OE}_b$) inputs which, when HIGH, force the outputs to a high impedance (High Z) state. The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{OE}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$\overline{Z}_b = \overline{OE}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

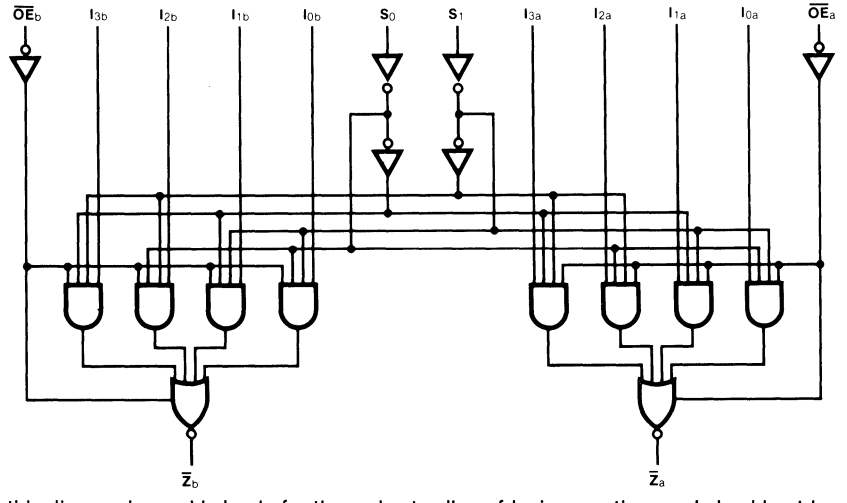
Truth Table

Select Inputs		Data Inputs				Output Enable	Outputs
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	$\overline{Z}$
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
H	L	X	L	X	X	L	H
H	L	X	H	X	X	L	L
L	H	X	X	L	X	L	H
L	H	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Address inputs S_0 and S_1 are common to both sections.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT353)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to $\overline{Z}_n$	3.3 5.0		9.0 6.5						ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	3.3 5.0		9.0 6.5						ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0		6.5 5.0						ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0		6.5 5.0						ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0		5.5 4.0						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		6.0 4.5						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 5.5						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		5.5 4.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to $\overline{Z}_n$	5.0		7.0						ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	5.0		7.0						ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0		5.5						ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0		5.5						ns	3-5
t_{PZH}	Output Enable Time	5.0		4.5						ns	3-7
t_{PZL}	Output Enable Time	5.0		5.0						ns	3-8
t_{PHZ}	Output Disable Time	5.0		6.0						ns	3-7
t_{PLZ}	Output Disable Time	5.0		4.5						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC373 • 54ACT/74ACT373

Octal Transparent Latch With 3-State Outputs

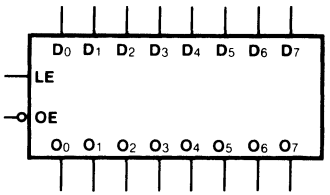
Description

The 'AC/'ACT373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

- **Eight Latches in a Single Package**
- **3-State Outputs for Bus Interfacing**
- **Outputs Source/Sink 24 mA**
- **'ACT373 has TTL-Compatible Inputs**

Ordering Code: See Section 6

Logic Symbol

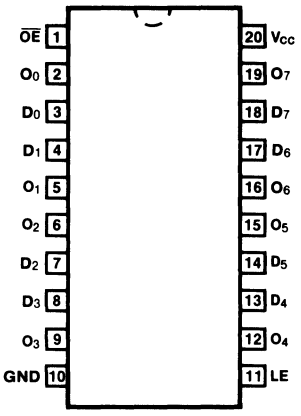


Truth Table

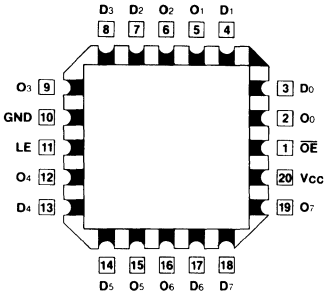
Inputs			Outputs
$\overline{OE}$	LE	Dn	On
H	X	X	Z
L	H	L	L
L	H	H	H
L	L	X	O0

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O0 = Previous O0 before
LOW-to-HIGH Transition of Clock

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

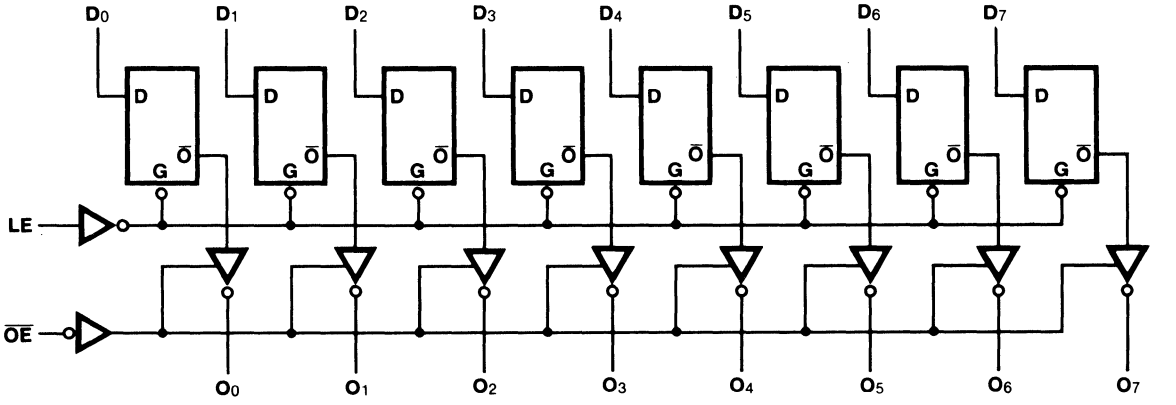
Pin Names

D0 - D7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
O0 - O7	3-State Latch Outputs

Functional Description

The 'AC/'ACT373 contains eight D-type latches with 3-state standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state standard outputs are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the standard outputs are in the 2-state mode. When $\overline{OE}$ is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT373)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3	1.0	10.0	13.5	1.0	16.5	1.0	15.0	ns	3-5
		5.0	1.0	7.0	9.5	1.0	11.5	1.0	10.5		
t_{PHL}	Propagation Delay D_n to O_n	3.3	1.0	9.5	13.0	1.0	16.0	1.0	14.5	ns	3-5
		5.0	1.0	7.0	9.5	1.0	11.5	1.0	10.5		
t_{PLH}	Propagation Delay LE to O_n	3.3	1.0	10.0	13.5	1.0	16.5	1.0	15.0	ns	3-6
		5.0	1.0	7.5	9.5	1.0	12.0	1.0	10.5		
t_{PHL}	Propagation Delay LE to O_n	3.3	1.0	9.5	12.5	1.0	15.0	1.0	14.0	ns	3-6
		5.0	1.0	7.0	9.5	1.0	11.0	1.0	10.5		
t_{PZH}	Output Enable Time	3.3	1.0	9.0	11.5	1.0	14.0	1.0	13.0	ns	3-7
		5.0	1.0	7.0	8.5	1.0	10.5	1.0	9.5		
t_{PZL}	Output Enable Time	3.3	1.0	8.5	11.5	1.0	13.5	1.0	13.0	ns	3-8
		5.0	1.0	6.5	8.5	1.0	10.0	1.0	9.5		
t_{PHZ}	Output Disable Time	3.3	1.0	10.0	12.5	1.0	16.0	1.0	14.5	ns	3-7
		5.0	1.0	8.0	11.0	1.0	13.5	1.0	12.5		
t_{PLZ}	Output Disable Time	3.3	1.0	8.0	11.5	1.0	13.0	1.0	12.5	ns	3-8
		5.0	1.0	6.5	8.5	1.0	10.5	1.0	10.0		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	3.3	3.5	5.5	6.5	6.0	ns	3-9
		5.0	2.0	4.0	5.0	4.5		
t_h	Hold Time, HIGH or LOW D_n to LE	3.3	−3.0	0	1.0	0	ns	3-9
		5.0	−1.5	0	1.0	0		
t_w	LE Pulse Width, HIGH	3.3	4.0	5.5	6.5	6.0	ns	3-6
		5.0	2.0	4.0	5.0	4.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0	1.0	8.5	10.0	1.0	12.5	1.0	11.5	ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	5.0	1.0	8.0	10.0	1.0	12.5	1.0	11.5	ns	3-5
t_{PLH}	Propagation Delay LE to O_n	5.0	1.0	8.5	11.0	1.0	12.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay LE to O_n	5.0	1.0	8.0	10.0	1.0	11.5	1.0	11.5	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	8.0	9.5	1.0	11.5	1.0	10.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	7.5	9.0	1.0	11.0	1.0	10.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	9.0	11.0	1.0	14.0	1.0	12.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	7.5	8.5	1.0	11.0	1.0	10.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	3.0	7.0	8.5	8.0	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0	0	1.0	1.0	ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.0	7.0	8.5	8.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	40.0	pF	$V_{CC} = 5.5$ V

54AC/74AC374 • 54ACT/74ACT374

Octal D-Type Flip-Flop With 3-State Outputs

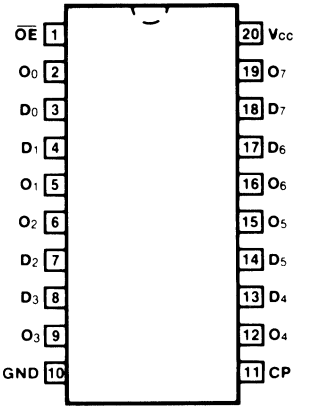
Description

The 'AC/'ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops.

- **Buffered Positive Edge-Triggered Clock**
- **3-State Outputs for Bus-Oriented Applications**
- **Outputs Source/Sink 24 mA**
- **See '273 for Reset Version**
- **See '377 for Clock Enable Version**
- **See '373 for Transparent Latch Version**
- **See '574 for Broadside Pinout Version**
- **See '564 for Broadside Pinout Version with Inverted Outputs**
- **'ACT374 has TTL-Compatible Inputs**

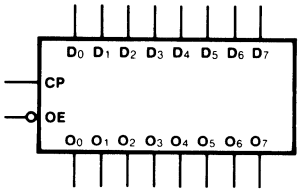
Ordering Code: See Section 6

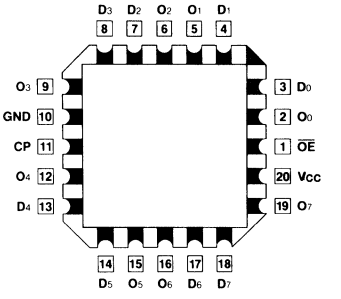
Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC

Logic Symbol





Pin Assignment for LCC

Pin Names

D_0 - D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-State Output Enable Input
O_0 - O_7	3-State Outputs

Functional Description

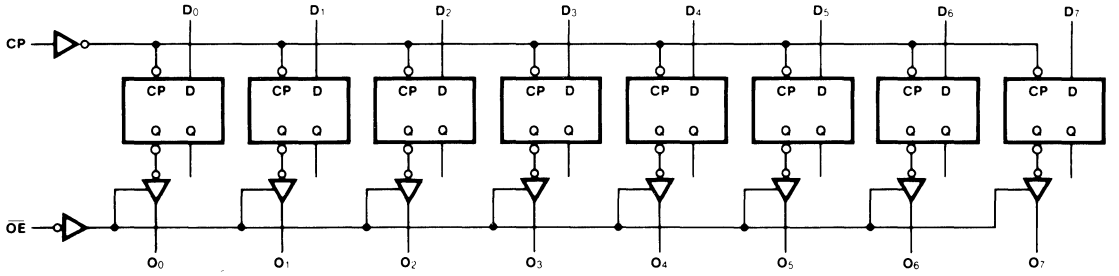
The 'AC/'ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Truth Table

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT374)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	60 100	110 155		60 95		60 100		MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0	1.0 1.0	11.0 8.0	13.5 9.5	1.0 1.0	16.5 12.0	1.0 1.0	15.5 10.5	ns	3-6
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0	1.0 1.0	10.0 7.0	12.5 9.0	1.0 1.0	15.0 11.0	1.0 1.0	14.0 10.0	ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0	1.0 1.0	9.5 7.0	11.5 8.5	1.0 1.0	14.0 10.5	1.0 1.0	13.0 9.5	ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0	1.0 1.0	9.0 6.5	11.5 8.5	1.0 1.0	14.0 10.5	1.0 1.0	13.0 9.5	ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0	1.0 1.0	10.5 8.0	12.5 11.0	1.0 1.0	16.0 12.5	1.0 1.0	14.5 12.5	ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0	1.0 1.0	8.0 6.5	11.5 8.5	1.0 1.0	13.0 10.5	1.0 1.0	12.5 10.0	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0	5.5 4.0	6.5 5.0	6.0 4.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 −4.0	1.0 1.5	1.0 1.5	1.0 1.5	ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	4.0 2.5	5.5 4.0	6.5 5.0	6.0 4.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	100	160		70		90		MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	5.0	1.0	8.5	10.0	1.0	12.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay CP to O_n	5.0	1.0	8.0	9.5	1.0	12.0	1.0	11.0	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	8.0	9.5	1.0	11.5	1.0	10.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	8.0	9.0	1.0	11.5	1.0	10.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	8.5	11.5	1.0	13.0	1.0	12.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	7.0	8.5	1.0	11.0	1.0	10.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0	7.0	5.5	5.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0	1.5	1.5	1.5	ns	3-9
t_w	CP Pulse Width, HIGH or LOW	5.0	2.0	7.0	5.0	5.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	80.0	pF	$V_{CC} = 5.5$ V

54AC/74AC377 • 54ACT/74ACT377

Octal D Flip-Flop With Clock Enable

Description

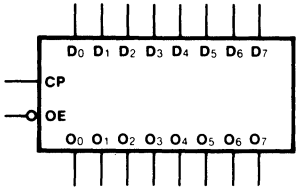
The 'AC/'ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable ($\overline{CE}$) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

- **Ideal for Addressable Register Applications**
- **Clock Enable for Address and Data Synchronization Applications**
- **Eight Edge-Triggered D Flip-Flops**
- **Buffered Common Clock**
- **Outputs Source/Sink 24 mA**
- **See '273 for Master Reset Version**
- **See '373 for Transparent Latch Version**
- **See '374 for 3-State Version**
- **'ACT377 has TTL-Compatible Inputs**

Ordering Code: See Section 6

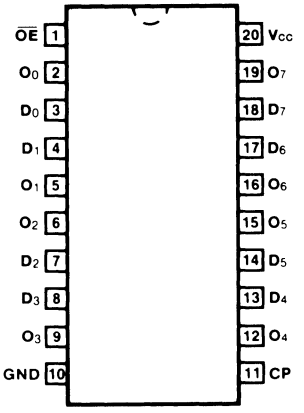
Logic Symbol



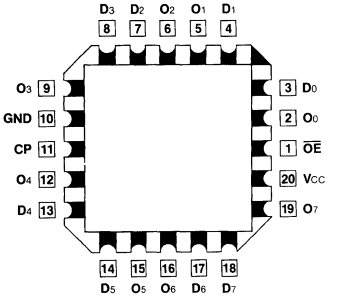
Pin Names

D_0 - D_7	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
Q_0 - Q_7	Data Outputs
CP	Clock Pulse Input

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

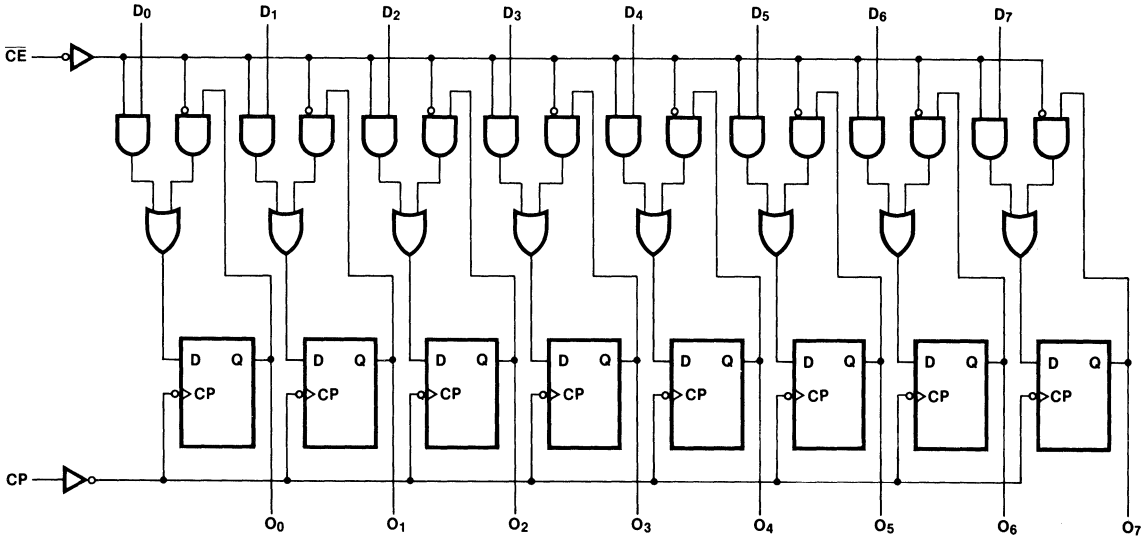
5

Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	$\overline{CE}$	Dn	Qn
Load '1'	⌐	L	H	H
Load '0'	⌐	L	L	L
Hold (Do Nothing)	⌐	H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT377)	1.6	1.5	mA	$V_{IN} = V_{CC}-2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0	90 140	125 175		75 95		75 125		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0	1.0 1.0	8.0 6.0	13.0 9.0	1.0 1.0	14.0 10.0	1.0 1.0	14.0 10.0	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0	1.0 1.0	8.5 6.5	13.0 10.0	1.0 1.0	15.0 11.0	1.0 1.0	14.5 11.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	3.5 2.5	5.5 4.0	7.5 6.0	6.0 4.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−2.0 −1.0	0 1.0	0 1.0	0 1.0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CE}$ to CP	3.3 5.0	4.0 2.5	6.0 4.0	9.5 6.0	7.5 4.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CE}$ to CP	3.3 5.0	−3.5 −2.0	0 1.0	0 1.0	0 1.0	ns	3-9
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5	5.5 4.0	6.5 5.0	6.0 4.5	ns	3-6

*Voltage Range 3.3 is 3.0 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	140	175		85		125		MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	5.0	1.0	6.5	9.0	1.0	11.0	1.0	10.0	ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	5.0	1.0	7.0	10.0	1.0	12.0	1.0	11.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT	Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	2.5	4.5	7.0	5.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−1.0	1.0	1.0	1.0	ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CE}$ to CP	5.0	2.5	4.5	7.0	5.5	ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CE}$ to CP	5.0	−1.0	1.0	1.0	1.0	ns	3-9
t_w	Clock Pulse Width HIGH or LOW	5.0	2.0	4.0	5.5	4.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	90.0	pF	$V_{CC} = 5.5$ V

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Parallel D Register With Enable

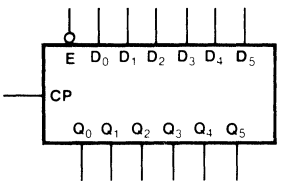
Description

The 'AC/'ACT378 is a 6-bit register with a buffered common Enable. This device is similar to the 'AC/'ACT174, but with common Enable rather than common Master Reset.

- **6-Bit High-Speed Parallel Register**
- **Positive Edge-Triggered D-Type Inputs**
- **Fully Buffered Common Clock and Enable Inputs**
- **Outputs Source/Sink 24 mA**
- **'ACT378 has TTL-Compatible Inputs**

Ordering Code: See Section 6

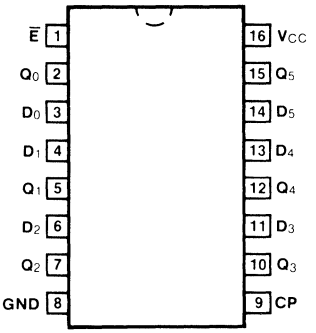
Logic Symbol



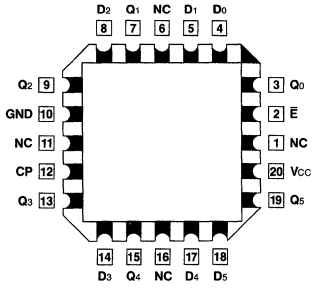
Pin Names

$\overline{E}$	Enable Input
D_0 - D_5	Data Inputs
CP	Clock Pulse Input
Q_0 - Q_5	Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

The 'AC/'ACT378 consists of six edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

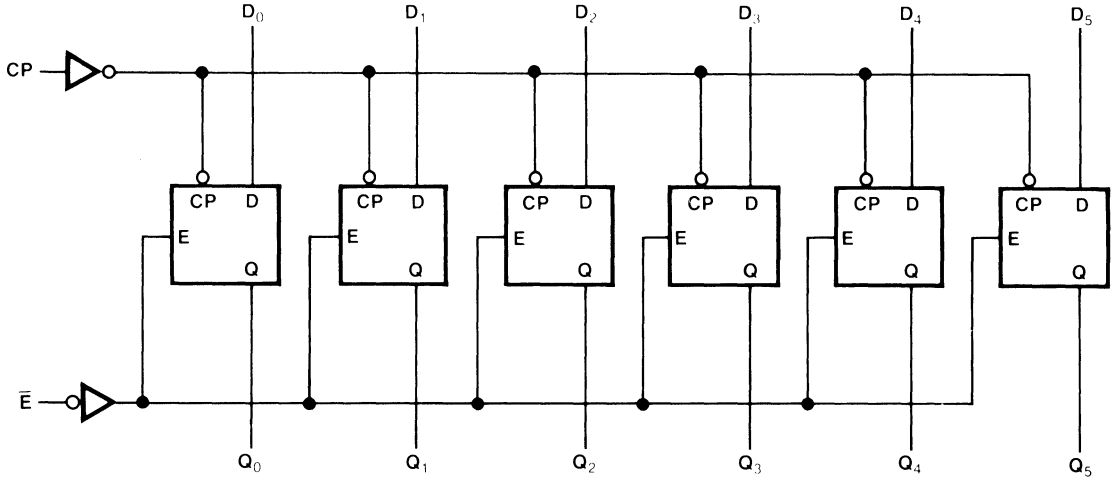
When the $\overline{E}$ input is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input.

Truth Table

Inputs			Outputs
$\overline{E}$	CP	Dn	Qn
H	⌐	X	No Change
L	⌐	H	H
L	⌐	L	L

H = HIGH Voltage Level
L = LOW Voltage level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°$
I_{CCT}	Maximum Additional Icc/Input ('ACT378)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		74 100						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	3.3 5.0		8.5 6.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	3.3 5.0		7.5 5.5						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	4.5 3.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	1.5 1.0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{E}$ to CP	3.3 5.0	−1.5 −1.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{E}$ to CP	3.3 5.0	0 0				ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	8.5 6.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		100						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n	5.0		6.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n	5.0		5.5						ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	3.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{E}$ to CP	5.0	− 1.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{E}$ to CP	5.0	0				ns	3-9
t_w	CP Pulse Width, HIGH or LOW	5.0	6.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC379 • 54ACT/74ACT379

Quad Parallel Register With Enable

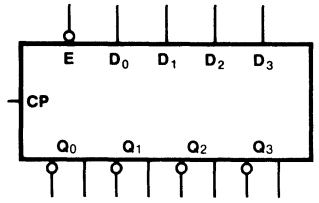
Description

The 'AC/'ACT379 is a 4-bit register with a buffered common Enable. This device is similar to the 'AC/'ACT175 but features the common Enable rather than common Master Reset.

- **Edge-Triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **Buffered Common Enable Input**
- **True and Complement Outputs**
- **Outputs Source/Sink 24 mA**
- **'ACT379 has TTL-Compatible Inputs**

Ordering Code: See Section 6

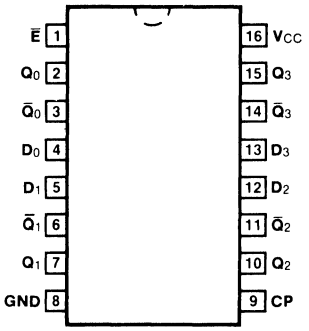
Logic Symbol



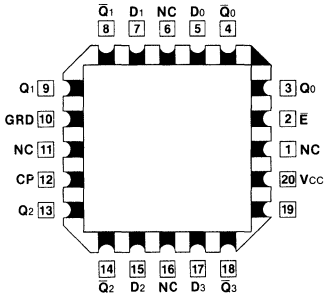
Pin Names

$\overline{E}$	Enable Input
D_0 - D_3	Data Inputs
CP	Clock Pulse Input
Q_0 - Q_3	Flip-Flop Outputs
$\overline{Q}_0$ - $\overline{Q}_3$	Complement Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC and PCC

5

Functional Description

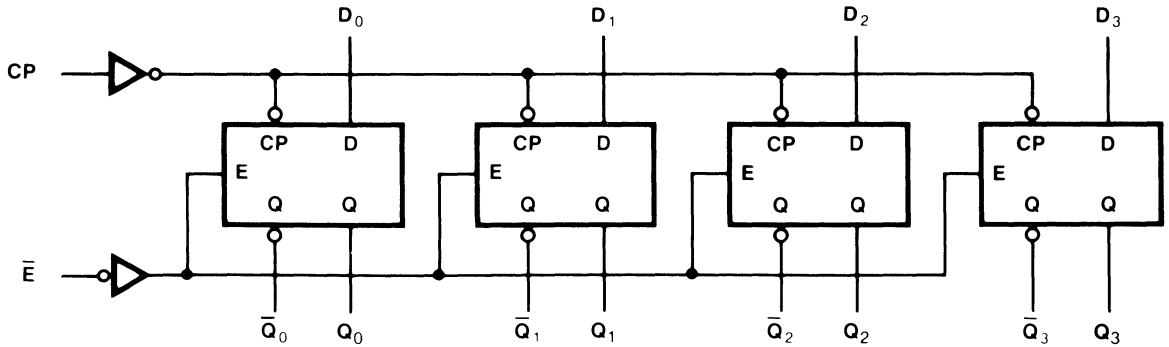
The 'AC/'ACT379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and $\overline{Q}$ outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops. When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input.

Truth Table

Inputs			Outputs	
$\overline{E}$	CP	Dn	Qn	$\overline{Q}_n$
H	⌐	X	NC	NC
L	⌐	H	H	L
L	⌐	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



PLease note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT379)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		118 160						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n, $\overline{Q}_n$	3.3 5.0		8.5 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	3.3 5.0		8.5 6.0						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	4.5 3.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{E}$ to CP	3.3 5.0	4.5 3.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{E}$ to CP	3.3 5.0	3.0 2.0				ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	5.5 4.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		160						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_n, $\overline{Q}_n$	5.0		7.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_n, $\overline{Q}_n$	5.0		6.0						ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	3.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{E}$ to CP	5.0	3.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{E}$ to CP	5.0	2.0				ns	3-9
t_w	CP Pulse Width, HIGH or LOW	5.0	4.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC398 • 54ACT/74ACT398
54AC/74AC399 • 54ACT/74ACT399

Quad 2-Port Register

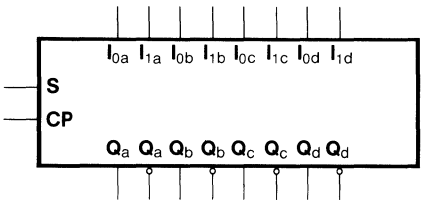
Description

The 'AC/'ACT398 and 'AC/'ACT399 are the logical equivalents of a quad 2-input multiplexer feeding into four edge-triggered flip-flops. A common Select input determines which of the two 4-bit words is accepted. The selected data enters the flip-flop on the rising edge of the clock. The 'AC/'ACT399 is the 16-pin version of the 'AC/'ACT398, with only the Q outputs of the flip-flops available.

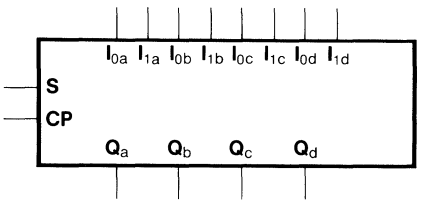
- **Select Inputs from Two Data Sources**
- **Fully Positive Edge-Triggered Operation**
- **Both True and Complement Outputs—'AC/'ACT398**
- **Outputs Source/Sink 24 mA**
- **'ACT398 and 'ACT399 have TTL-Compatible Inputs**

Ordering Code: See Section 6

Logic Symbols

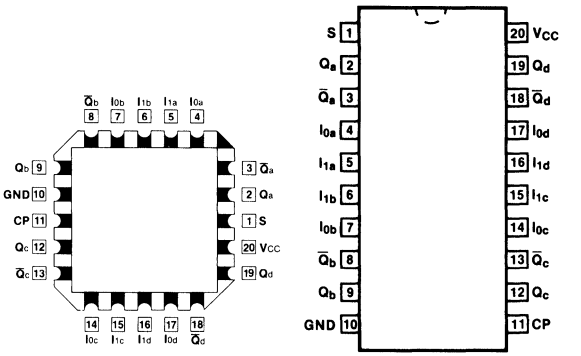


'AC/'ACT398

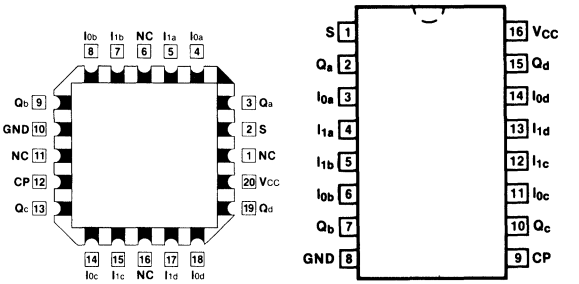


'AC/'ACT399

Connection Diagrams



'AC/'ACT398



'AC/'ACT399

Pin Assignment for LCC

Pin Assignment for DIP, Flatpak and SOIC

Pin Names

S	Common Select Input
CP	Clock Pulse
I0a - I0d	Data Inputs from Source 0
I1a - I1d	Data Inputs from Source 1
Qa - Qd	Register True Outputs
$\overline{Q}_a$ - $\overline{Q}_d$	Register Complementary Outputs ('AC/'ACT398)

Functional Description

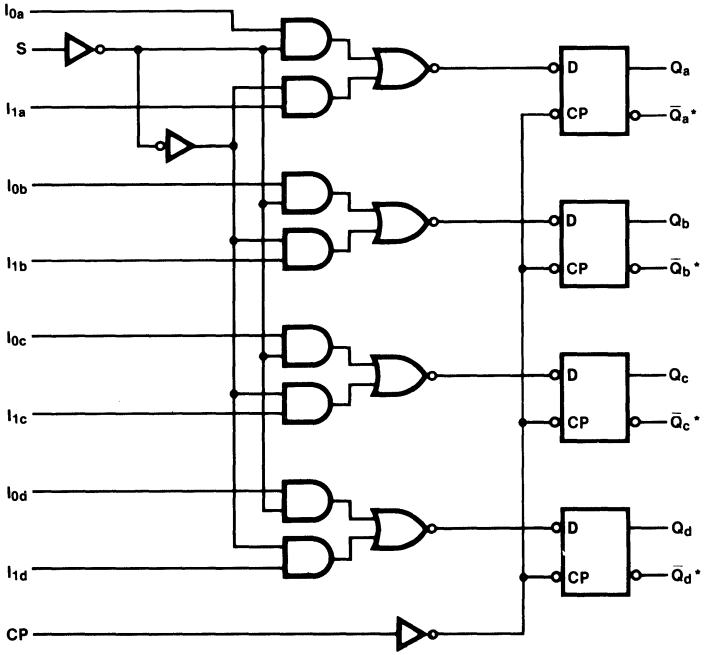
The 'AC/ACT398 and 'AC/'ACT399 are high-speed quad 2-port registers. They select four bits of data from either of two sources (Ports) under control of a common Select input (S). The selected data is transferred to a 4-bit output register synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit D-type output register is fully edge-triggered. The Data inputs (I_{0x}, I_{1x}) and Select input (S) must be stable only a setup time prior to and hold time after the LOW-to-HIGH transition of the Clock input for predictable operation. The 'AC/'ACT398 has both Q and $\overline{Q}$ outputs.

Function Table

Inputs				Outputs	
S	I_0	I_1	CP	Q	$\overline{Q}$*
L	L	X	⌐	L	H
L	H	X	⌐	H	L
H	X	L	⌐	L	H
H	X	H	⌐	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
* = 'AC/'ACT398 only

Logic Diagram



*'AC/'ACT398 only

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT398/399)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Input Clock Frequency	3.3 5.0		180 160						MHz	3-3
t_{PLH}	Propagation Delay CP to Q_0 or $\overline{Q}$	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q_0 or $\overline{Q}$	3.3 5.0		8.5 6.0						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW I_n to CP	3.3 5.0	4.5 3.0				ns	3-9
t_h	Hold Time, HIGH or LOW I_n to CP	3.3 5.0	0 0				ns	3-9
t_s	Setup Time, HIGH or LOW S to CP ('398)	3.3 5.0	4.5 3.0				ns	3-9
t_s	Setup Time, HIGH or LOW S to CP ('399)	3.3 5.0	4.5 3.0				ns	3-9
t_h	Hold Time, HIGH or LOW S to CP	3.3 5.0	−1.5 −1.0				ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	5.5 4.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Input Clock Frequency	5.0		160						MHz	3-3
t_{PLH}	Propagation Delay CP to Q or $\overline{Q}$	5.0		7.0						ns	3-6
t_{PHL}	Propagation Delay CP to Q or $\overline{Q}$	5.0		6.0						ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

5

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW I_n to CP	5.0	3.0				ns	3-9
t_h	Hold Time, HIGH or LOW I_n to CP	5.0	0				ns	3-9
t_s	Setup Time, HIGH or LOW S to CP ('398)	5.0	3.0				ns	3-9
t_s	Setup Time, HIGH or LOW S to CP ('399)	5.0	3.0				ns	3-9
t_h	Hold Time, HIGH or LOW S to CP	5.0	−1.0				ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	5.5				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54ACT/74ACT488

General Purpose Interface Bus (GPIB) Circuit

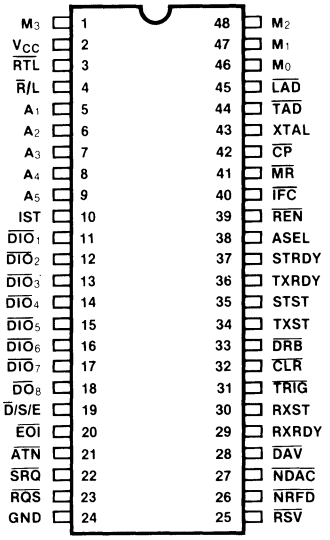
Description

The 'ACT488 is a FACT LSI circuit containing all of the logic necessary to interface Talk, Listen and Talk/Listen type instruments and system components in accordance with the IEEE-488 standard for programmable instrumentation. All outputs that drive the IEEE-488 bus are guaranteed to sink 48 mA and all bus inputs have Schmitt triggers and bus terminating networks. All pins that interface to the instrument logic are TTL-compatible.

The 'ACT488 has programming inputs that determine whether it is to be a talker, listener or both, single or dual address, high or low speed, etc., according to the instrument and system requirements. It operates with a minimum of external support logic and readily interfaces with most microprocessors. It operates from a single voltage supply and a 10 MHz single phase clock, and it is capable of operating the bus handshake at the full 1 MHz data rate. It offers a variety of handshaking and status connections to the instrument logic for versatility and ease of design.

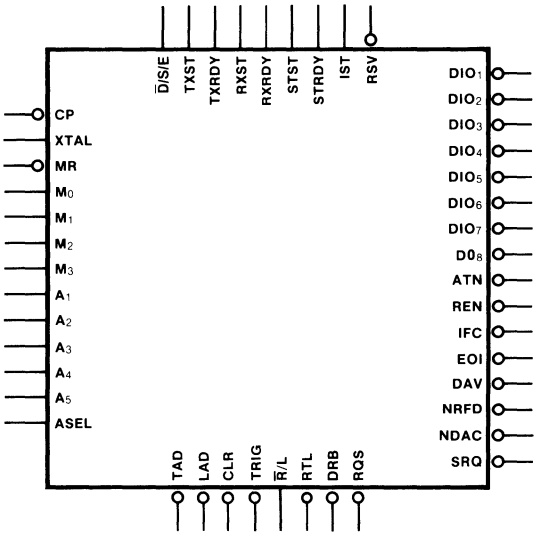
- **Single Supply Voltage**
- **Complete Source and Acceptor Handshake Logic**
- **Same or Separate Talk and Listen Address**
- **Secondary Address Capability**
- **Talk Only or Listen Only Capability**
- **Source Handshake Delay Programmable for Low or High Speed**
- **Serial Poll Capability**
- **Parallel Poll Capability**
- **Sync Trigger and Device Clear Outputs**
- **Implements Remote/Local Function**
- **On-Chip Clock Oscillator**
- **Service Request Interrupt Facility**
- **All Bus I/O Signals Comply with the IEEE-488 (1980) and IEC-625-1 Input Threshold, Termination and Output Specifications**
- **All Instrument Interface Signals are LS-TTL-Compatible**
- **GPIB Pins Present No Electrical Load when Device is Powered Off**

Connection Diagram



Pin Assignment for DIP

Logic Symbol



Pin Names

A_1 - A_5	Address Inputs
$\overline{ATN}$	Attention Input
$\overline{CP}$	Clock Input
$\overline{IFC}$	Interface Clear Input
IST	Instrument Status Input
M_0 - M_3	Mode Control Inputs
$\overline{MR}$	Master Reset Input
$\overline{REN}$	Remote Enable Input
$\overline{RSV}$	Request Service Input
$\overline{RTL}$	Return to Local Input
RXRDY	Receiver Ready Input
STRDY	Status Ready Input
TXRDY	Transmitter Ready Input
$\overline{DAV}$	Data Valid Input Output
$\overline{DIO_1}$ - $\overline{DIO_7}$	Data Inputs Outputs
$\overline{DO_8}$	Data Output
$\overline{EOI}$	End or Identify Input
$\overline{NDAC}$	Not Data Accepted Input Output
$\overline{NRFD}$	Not Ready for Data Input Output
ASEL	Address Select Output
$\overline{CLR}$	Device Clear Output
$\overline{D}$/S/E	Data/Status Output or End-of-String Output
$\overline{DRB}$	Bus Drive Enable Output
$\overline{LAD}$	Listen Address Status Output
$\overline{RQS}$	Requested Service Status Output
RXST	Receiver Strobe Output
$\overline{R}$/L	Remote/Local Output
$\overline{SRQ}$	Service Request Output
STST	Status Strobe Output
$\overline{TAD}$	Talk Address Status Output
TXST	Transmitter Strobe Output
$\overline{TRIG}$	Device Trigger Output
XTAL	Crystal Output

GPIB Protocol

A full description and specification of the GPIB system is published in the IEEE document "IEEE Standard Interface for Programmable Instrumentation" IEEE Std 488-1978 and is used as the reference in this description.

The standard is a 16-wire interface that can transmit byte serial data at rates of up to one megabyte/second. Using this standard up to 15 individual devices (instruments or system components) may be interconnected in a star or linear network, with a maximum cable length of 20 m and automatically controlled or programmed. Data may be exchanged between instruments or between a controller and instruments. The use of a bus extender or a controller which can handle a number of separate instrument buses allows more than 15 instruments to be used in a system:

Talkers — These instruments can only transmit data (when addressed), e.g., a timer or counter.

Listeners — These instruments can only receive information, e.g., a programmable power supply or a printer.

Talker/Listeners — These instruments can receive data or functional instructions and later transmit data, e.g., a programmable DVM or multi-channel A/D converter.

Controller — A device that is able to generate control instructions for instruments on the bus, e.g., a mini-computer or programmable calculator.

The 'ACT488 is designed for use in any of the first three types of devices.

The 16-wire bus is organized as three functional groups (Figure 1). The 8-line Data bus ($\overline{DIO_1}$-$\overline{DIO_7}$, $\overline{DO_8}$) is used to transfer commands in bit parallel/byte serial form from Talkers to Listeners. The 3-line Data Byte Transfer Control bus ($\overline{NRFD}$, $\overline{NDAC}$ and $\overline{DAV}$) implements a data handshake which ensures that information transfer proceeds as fast as the device will allow but no faster than the slowest device currently addressed as active (Figure 2). The 5-line General Interface Management bus ($\overline{ATN}$, $\overline{REN}$, $\overline{EOI}$, $\overline{IFC}$ and $\overline{SRQ}$) is principally used by the Controller.

In its simplest configuration the GPIB can consist of only two instruments, a Talker and a Listener; in its most complex configuration up to 961 instruments could be controlled by one or more mini-computers. A bus controller dictates the role of each device by making the $\overline{ATN}$ line LOW and sending Talk and/or Listen Addresses on the bus data lines. Those devices with matching addresses are activated accordingly. Device addresses are set by switches or PC board jumpers. In single address mode each device has a 5-bit address allowing up to 31 different addresses (one code is used as an unaddress command). In extended address mode each device has a 10-bit address, allowing up to 961 different addresses and the Controller must send two bytes in order to activate a device.

In the configuration shown in Figure 1 a sequence to initiate a data transfer from device A to device D would proceed as follows:

Controller sends $\overline{ATN}$ (attention) command;

whenever the $\overline{ATN}$ line goes LOW, devices using the Data bus immediately stop all operations. The Controller keeps the $\overline{ATN}$ line LOW during the remainder of this sequence.

Controller sends UNL (unlisten) command; this instruction disables any devices that are in Listen mode.

Controller sends Talk Address command to device A; this instruction puts device A into Talk mode and disables any other devices that had been in that mode.

Controller sends Listen Address command to device D, putting it in Listen mode.

When the Controller stops sending $\overline{ATN}$, the bus will be released for data transfer functions and device A will begin transmitting to device D.

The $\overline{SRQ}$ line allows any device to interrupt the Controller and request service. The Controller can identify the interrupting devices by conducting a Serial Poll. To do this it issues an Unlisten (UNL) command followed by a Serial Poll Enable (SPE) command and then the Talk Address of each device in turn. The interrupting device will optionally drive $\overline{DIO}_7$ LOW. Alternately the Controller can conduct a Parallel Poll by making both $\overline{EOI}$ and $\overline{DIO}$ line previously assigned via a Parallel Poll Enable (PPE) command.

The $\overline{REN}$ line allows the Controller to put all Listen addressed instruments into remote control mode, while the $\overline{IFC}$ line allows the Controller to initialize the system.

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Figure 1: Interface Capabilities and Bus Structure

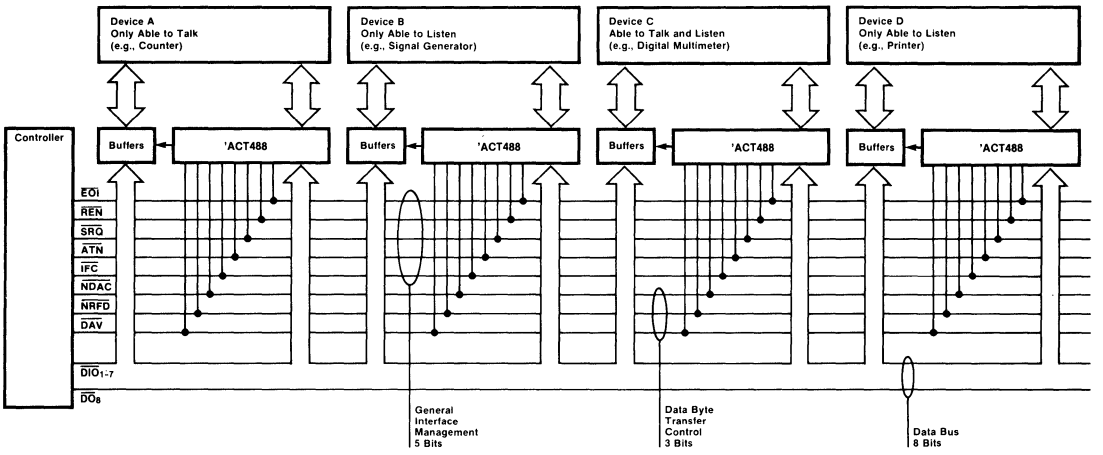
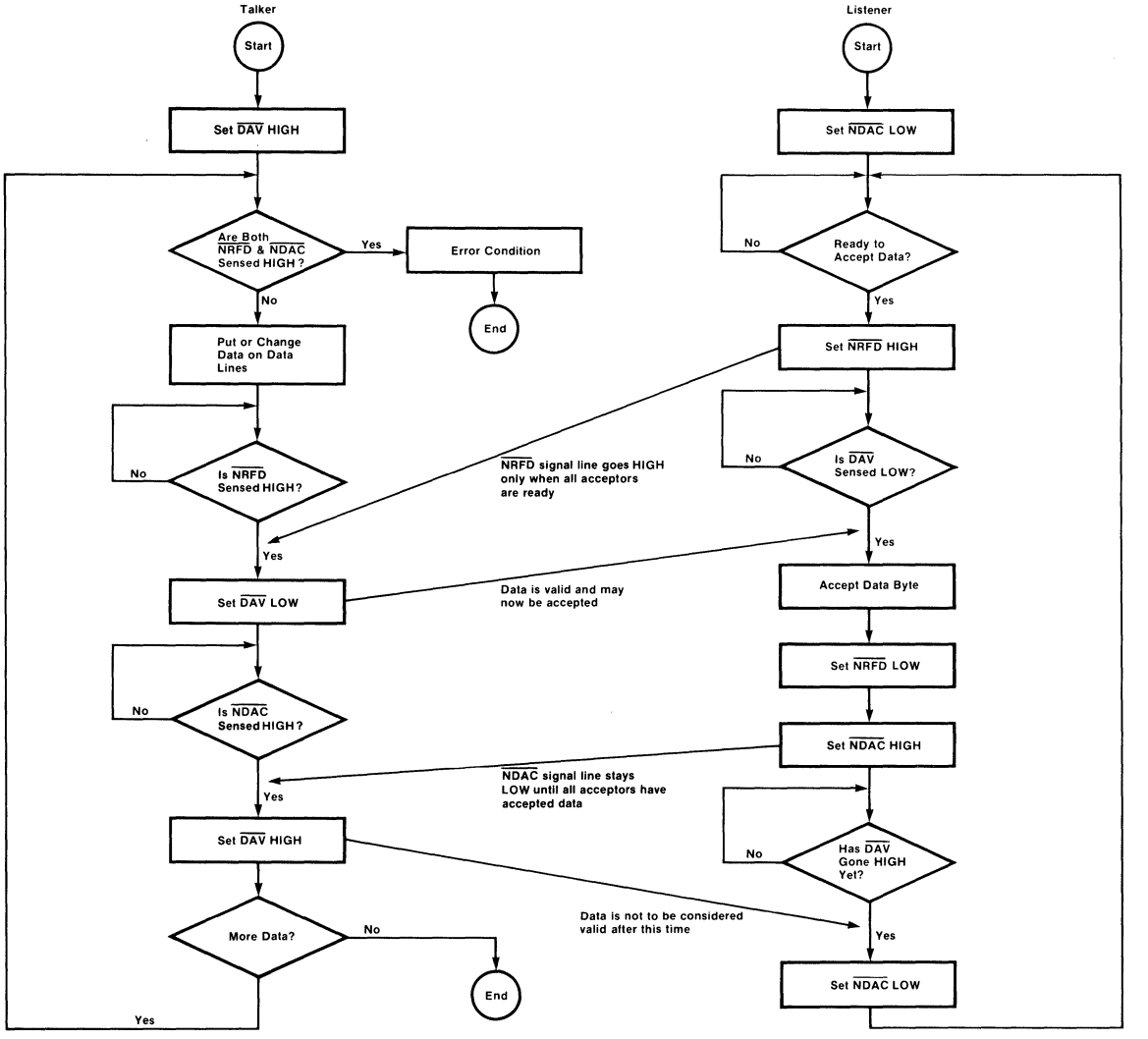
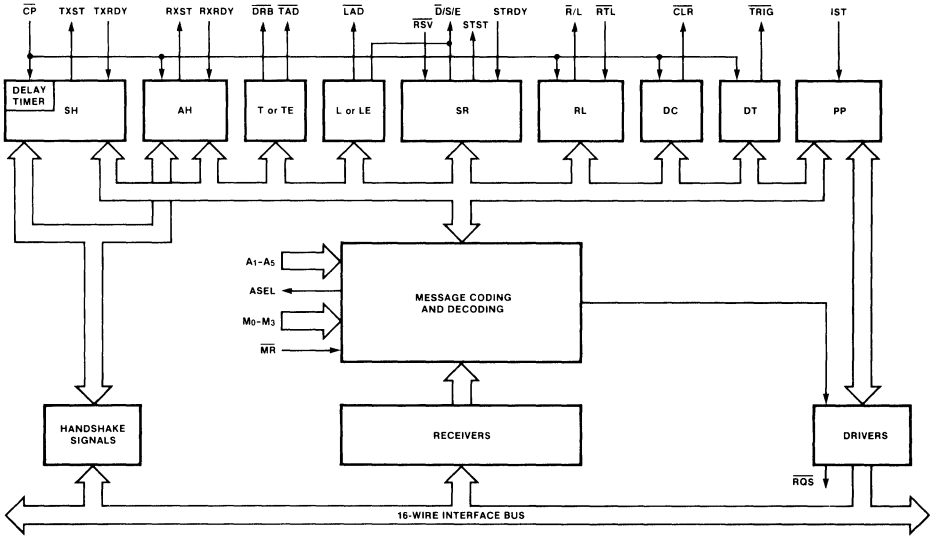


Figure 2: Source and Acceptor Handshake Logic



'ACT488 Functional Block Diagram



Functions Implemented by the 'ACT488

Acceptor Handshake (AH)
Controls the acquisition of addresses, interface commands and data bytes from the bus. The AH passes data bytes to the instrument logic via a 2-wire handshake (RXST, RXRDY) and a status output ($\overline{LAD}$).

Source Handshake (SH)
Controls the passing of data bytes and status information from the instrument to the bus. The SH communicates with the instrument via a 2-wire handshake (TXST, TXRDY) and a status output ($\overline{TAD}$). It has two operating speeds, selectable via the M_0 - M_3 inputs. Low speed is used with open collector data drivers and gives a setting delay of 2.0 μs. High speed is used with 3-state bus drivers and gives a setting delay of 1.1 μs for the first byte sent and 0.5 μs for the subsequent bytes (clock frequency 10 MHz).

Listener or Extended Listener (L or LE)
Either the single or extended address L functions can be selected by the M_0 - M_3 inputs. The 'ACT488 flags the listener addressed status via the $\overline{LAD}$ output. The listen address is defined by the A_1 - A_5 inputs and, where the extended address feature is used, the ASEL output controls an external multiplexer to select the primary or secondary address as required.

Talker or Extended Talker (T or TE)
Either the single or extended address T function can be selected. The T function employs the M_0 - M_3 and A_1 - A_5 inputs in the same manner as the L function. The 'ACT488 flags the talker addressed status via the $\overline{TAD}$ output. The T function also incorporates the Serial Poll Function.

Talker/Listener, Extended Talker/Listener
For instruments with both talk and listen capabilities, the 'ACT488 implements both the T and L functions. In this mode, the "Untalk if My Listen Address" and "Unlisten if My Talk Address" feature is standard. Where the single address mode is selected, different Talk and Listen addresses can be used. In the extended address mode, the Talk and Listen addresses must be identical.

Device Trigger, Device Clear (DT, DC)
These functions generate a pulse on the Trigger or Clear output upon receipt of the relevant bus command.

Remote Local (RL)
The complete RL function is implemented, including the Local Lock-Out feature.

Talk Only, Listen Only
The 'ACT488 can operate in either of these two modes via the M_0 - M_3 input code selection.

Service Request (SR)
The 'ACT488 initiates an SR on receipt of the $\overline{RSV}$ input and returns its status on the $\overline{RQS}$ line when serial polled. The $\overline{RQS}$ output can be used to drive the $\overline{DIO}_7$ bus line directly.

Parallel Poll (PP)
The Controller assigns, via the PPE command, one of the eight data lines for use as the Parallel Poll Response output. When the Controller issues the IDY command, the 'ACT488 compares the state of the IST input with the state defined by the last PPE command. If the comparison is True, the previously assigned $\overline{DIO}$ line is driven LOW by the 'ACT488.

Pin Functions

488 Bus Signals
All bus inputs have Schmitt trigger buffers, and all bus outputs can sink 48 mA. Each bus signal is terminated with a resistive load and meets the DC load characteristics specified in Section 3.5.3 of the IEEE Std 488-1978 specification.

$\overline{DIO}_1$ - $\overline{DIO}_7$ (Data Input/Output)—These are used as inputs to receive addresses and interface commands. They are used as outputs, along with $\overline{DO}_8$ to provide Parallel Poll response.

$\overline{ATN}$ (Attention)—This is an input from the GPIB Controller. When $\overline{ATN}$ is LOW the 'ACT488 interprets the data on $\overline{DIO}_1$ - $\overline{DIO}_7$ lines as commands or addresses. If the 'ACT488 is interrupted by $\overline{ATN}$ while sending data, it will relinquish control of the Data and Management lines within 200 ns.

$\overline{DAV}$ (Data Valid)— A bidirectional signal with a 3-state output driver, $\overline{DAV}$ is part of the handshake system and is driven LOW by current talker when a valid data byte, command or address is on the GPIB. $\overline{DAV}$ is treated as an input when the 'ACT488 is addressed to Listen or is receiving $\overline{ATN}$. It is an output when the 'ACT488 is addressed to Talk and $\overline{ATN}$ is HIGH.

$\overline{NRFD}$ (Not Ready for Data)—A bidirectional signal with an open-drain output driver, $\overline{NRFD}$ is part of the handshake system and is driven LOW to indicate that an instrument is not ready to receive data. The 'ACT488 drives $\overline{NRFD}$ HIGH when addressed as a Listener and the instrument is ready to accept a data byte or when $\overline{ATN}$ is LOW and the 'ACT488 is ready to accept an address or interface command. $\overline{NRFD}$ is treated as an input when the 'ACT488 is addressed to Talk.

$\overline{NDAC}$ (Not Data Accepted)—A bidirectional signal with an open-drain output driver, $\overline{NDAC}$ is part of the handshake system and is pulled LOW to indicate that a device has not yet accepted a data byte. $\overline{NDAC}$ is treated as an input when the 'ACT488 is addressed to Talk. It is an output and is driven LOW when the 'ACT488 is addressed to Listen and the instrument has not accepted a data byte or when receiving $\overline{ATN}$ and the 'ACT488 has not accepted an address or interface command.

$\overline{SRQ}$ (Service Request)—This is an open-drain output driven LOW when the instrument requests service (via $\overline{RSV}$) from the Controller.

$\overline{RQS}$ (Requested Service)—A 48 mA 3-state output, enabled during a Serial Poll response and driven LOW if the 'ACT488 initiated an $\overline{SRQ}$, $\overline{RQS}$ can be directly connected to $\overline{DIO}_7$ in applications where it is the only status information to be sent.

$\overline{EOI}$ (End or Identify)—This is an input from the GPIB Controller used to elicit a Parallel Poll response, or from the current active talker to indicate the End-of-String (END) message.

$\overline{REN}$ (Remote Enable)—This is an input driven by the Controller. The Controller drives it LOW when it needs to remotely program an instrument.

$\overline{IFC}$ (Interface Clear)—This is an input from the Controller, driven LOW to clear the interface logic (Figure 18).

Instrument Interface and Auxiliary Pins
Instrument Logic Signals—All instrument logic signals are standard low-power Schottky-compatible.

$\overline{CP}$ (10 MHz Clock)—Used to clock internal-state it flip-flops, and is divided down internally to generate the SH data setting delay. All output changes are synchronous with the negative clock edge. The $\overline{CP}$ input can be driven by an external oscillator or used in conjunction with XTAL output, as a crystal oscillator (Figure 6).

XTAL (Crystal)—Used to connect a crystal for the on-chip oscillator (Figure 6).

$\overline{MR}$ (Active-LOW Master Reset)—Initializes all internal latches and is completely asynchronous. After a reset, all outputs to the GPIB are passive HIGH and $\overline{RQS}$ is in the High-Z state; $\overline{R}$/L, $\overline{TRIG}$, $\overline{CLR}$, $\overline{DRB}$, ASEL, $\overline{TAD}$ and $\overline{LAD}$ are HIGH; $\overline{D}$/S/E, RXST, STST and TXST are LOW.

M_0 - M_3 (Mode Control Inputs)—Defines one of fourteen possible operating modes for the 'ACT488. M_0 - M_3 are HIGH-true inputs.

A_1 - A_5 (Device Address Inputs)—Defines the instrument address and originates from switches, PC jumpers or software-loaded register. Where different Talk and Listen addresses are required or when the secondary address feature is used, these inputs must be externally multiplexed, using the ASEL output to control the multiplexer. A_1 - A_5 are HIGH-true inputs (H = 1, L = 0) and thus have the opposite polarity of the $\overline{DIO_1}$ - $\overline{DIO_5}$ addresses.

ASEL (Address Select Output)—Selects, via an external multiplexer, the Talk/Listen or primary/secondary address input, depending on the operating mode selected; LOW for Talk or primary address; HIGH for Listen or secondary address (Figure 11).

$\overline{LAD}$, $\overline{TAD}$ (Address Status Outputs)—Indicate the Listen-Address or Talk-Address status respectively. They are also activated in the Talk-Only and Listen-Only modes. The outputs are active-LOW to facilitate driving LED indicator lamps (Figures 7, 10).

RXST (Receiver Strobe Output)—Forms part of the handshake logic to pass data bytes to the instrument. When addressed to Listen, the 'ACT488 takes RXST HIGH when a valid data byte is on the bus and holds it HIGH until the instrument signals (via the RXRDY input) that it has processed the byte. RXST may be inverted and connected to RXRDY, in which case the 'ACT488 will receive data bytes from the bus at a data rate determined solely by the bus handshake (Figure 8).

TXST (Transmit Strobe Output)—Forms part of the handshake logic to pass data bytes from the instrument to the bus. When addressed to Talk, the 'ACT488 takes TXST HIGH to signal the instrument that the bus has accepted the data. TXST does not go LOW again until the instrument has acknowledged that the byte has been accepted (via the TXRDY input). TXST may be inverted and connected to TXRDY, in which case the 'ACT488 will transmit data bytes to the bus at a data rate determined solely by the bus handshake (Figure 9).

STST (Status Strobe Output)—Forms part of the handshake logic to pass a status byte from the instrument to the bus during a Serial Poll sequence. It operates in conjunction with the STRDY input in the same way as the TXST and TXRDY signals. STST may be inverted and connected to STRDY, in which case the status byte will be repeated as long as the 'ACT488 is addressed to Talk (Figure 16).

RXRDY (Receiver Ready Input)—Forms part of the handshake logic controlling the passing of data from the bus to the instrument. RXRDY is driven HIGH when the instrument is ready to receive a data byte and LOW to acknowledge receipt of a data byte (Figure 8).

TXRDY (Transmitter Ready Input)—Forms part of the handshake logic controlling the passing of data from the instrument to the bus. When the 'ACT488 is addressed to Talk, TXRDY is driven HIGH when the instrument has a data byte to send and LOW to acknowledge that the byte has been accepted by the bus (Figure 9).

STRDY (Status Ready Input)—Forms part of the handshake logic controlling the passing of a status byte to the bus during a Serial Poll sequence. It operates in a similar fashion to TXRDY (Figure 16).

$\overline{RSV}$ (Request Service Input)—Is pulled LOW by the instrument to request service and initiate an $\overline{SRQ}$ interrupt to the controller. This interrupt will be cleared if $\overline{RSV}$ goes HIGH before it is serviced, but once the $\overline{SRQ}$ is serviced, $\overline{RSV}$ must, after exiting SPAS, go HIGH then LOW to initiate another service request (Figure 16).

$\overline{CLR}$ (Clear Output)—Issues a negative impulse when the 'ACT488 receives a Device Clear (DC) command, or when it is addressed to Listen and receives a Selected Device Clear. The $\overline{CLR}$ Output will stay LOW during Accept Data State (ACDS) or until $\overline{ATN}$ goes HIGH (Figure 13).

$\overline{TRIG}$ (Trigger Output)—Issues a negative pulse when the 'ACT488 is addressed to Listen and receives a DT command. The $\overline{TRIG}$ output will stay LOW during ACDS or until $\overline{ATN}$ goes HIGH (Figure 13).

$\overline{DRB}$ (Drive Bus Output)—Taken LOW to enable an external data bus driver when the 'ACT488 is addressed to Talk and is in the Talker Active State. $\overline{DRB}$ will go LOW one clock period after $\overline{ATN}$ goes HIGH, and will go HIGH asynchronously within 200 ns (typically 70 ns) after $\overline{ATN}$ goes LOW (Figures 9, 10, 11). $\overline{DRB}$ can also be used to tell the instrument logic to fetch the first byte.

$\overline{RQS}$ (Requested Service Output)—A 48 mA 3-state output, enabled during a Serial Poll response and driven LOW if the 'ACT488 initiated an $\overline{SRQ}$. $\overline{RQS}$ can be directly connected to $\overline{DIO_7}$ in applications where it is the only status information to be sent (Figures 4, 5, 16).

$\overline{D}$/S/E (Data/Status or END Output)—Valid during the Talk Addressed state and indicates to the instrument logic whether the information to be sent via the bus is to be data or status (LOW for data, HIGH for status). A status byte is sent only in response to a Serial Poll, and, in this case, $\overline{D}$/S/E may be used to control a multiplexer to select data or status as the source to the bus data drivers (Figures 4, 5, 16). Valid during the Listener Active State (LACS) to indicate that the current talker is sending the END message; a HIGH output indicates that the END message is true.

$\overline{R}$/L (Remote/Local Output)—Goes LOW when the Controller puts the instrument into Remote mode via the $\overline{REN}$ command (Figures 14, 15).

$\overline{RTL}$ (Return to Local Input)—Taken LOW to request return of the instrument to local control. $\overline{RTL}$ will set $\overline{R}$/L HIGH unless the Controller has put the 'ACT488 into Local Lock-out state (Figure 14).

IST (Instrument Status Input)—Used by the Parallel Poll logic, IST is compared with the logic state defined by $\overline{DIO_4}$ during the last PPE command. If IST is in the defined state, the 'ACT488 will make an affirmative response to the next IDY message by making the assigned $\overline{DIO}$ line LOW. Note that IST is a HIGH-true input while $\overline{DIO_4}$ is LOW-true (Figure 17).

Operating Modes

The 'ACT488 has fourteen operating modes, defined by a 4-bit input code (M_0 - M_3) which would normally be selected by switches or PC board jumpers.

Table 1 defines the input codes and operating modes.

Table 1

Mode Inputs				Operating Mode	Function
M_0	M_1	M_2	M_3		
L	L	L	L	Off Line	The device cannot take part in any GPIB operations
L	L	L	H	TON (LOW Speed)[1]	The device goes directly to the talk addressed state and can source data to the bus
L	L	H	L	LON	The device goes directly to the listen addressed state and can receive data from the bus
L	L	H	H	TON (HIGH Speed)[1]	As for TON (LOW Speed)
L	H	L	L	T (LOW Speed)[1]	Talker only, single address mode
L	H	L	H	TE (LOW Speed)[1]	Talker only, extended address mode
L	H	H	L	T (HIGH Speed)[1]	Talker only, single address mode
L	H	H	H	TE (HIGH Speed)[1]	Talker only, extended address mode
H	L	L	L	L	Listener only, single address mode
H	L	L	H	LE	Listener only, extended address mode
H	H	L	L	T/L (LOW Speed)[1,2]	Talker/Listener, dual address mode
H	H	L	H	TE/LE (LOW Speed)[1]	Talker/Listener, extended address mode
H	H	H	L	T/L (HIGH Speed)[1,2]	Talker/Listener, dual address mode
H	H	H	H	TE/LE (HIGH Speed)[1]	Talker/Listener, extended address mode

Notes

1. The LOW speed talker option is selected where open-collector data drivers are used. The delay from putting valid data on the GPIB to $\overline{DAV}$ going true is 2.0 μs. The HIGH speed option is selected where 3-state drivers are used. The setting delay (data to $\overline{DAV}$) is 1.1 μs for the first byte sent after a LOW to HIGH transition of $\overline{ATN}$ and 500 ns for subsequent bites.
2. For dual address Talker/Listener modes the Talk and Listen addresses can be different.

Table 2

$\overline{DO_8}$	$\overline{DIO_7}$	$\overline{DIO_6}$	$\overline{DIO_5}$	$\overline{DIO_4}$	$\overline{DIO_3}$	$\overline{DIO_2}$	$\overline{DIO_1}$	
X	H	L	$\overline{A_5}$	$\overline{A_4}$	$\overline{A_3}$	$\overline{A_2}$	$\overline{A_1}$	Primary Listen Address
X	H	L	L	L	L	L	L	Unlisten
X	L	H	$\overline{A_5}$	$\overline{A_4}$	$\overline{A_3}$	$\overline{A_2}$	$\overline{A_1}$	Primary Talk Address
X	L	H	L	L	L	L	L	Untalk
X	L	L	$\overline{S_5}$	$\overline{S_4}$	$\overline{S_3}$	$\overline{S_2}$	$\overline{S_1}$	Secondary Address

Addressing Modes

Where extended addressing or different Talk and Listen addresses are required, the address codes must be externally multiplexed, using ASEL (Figure 3). In the extended address modes, ASEL is LOW for the primary address and HIGH for the secondary address (Figure 11). In the dual address modes, ASEL is HIGH for the Listen address and LOW for the Talk address.

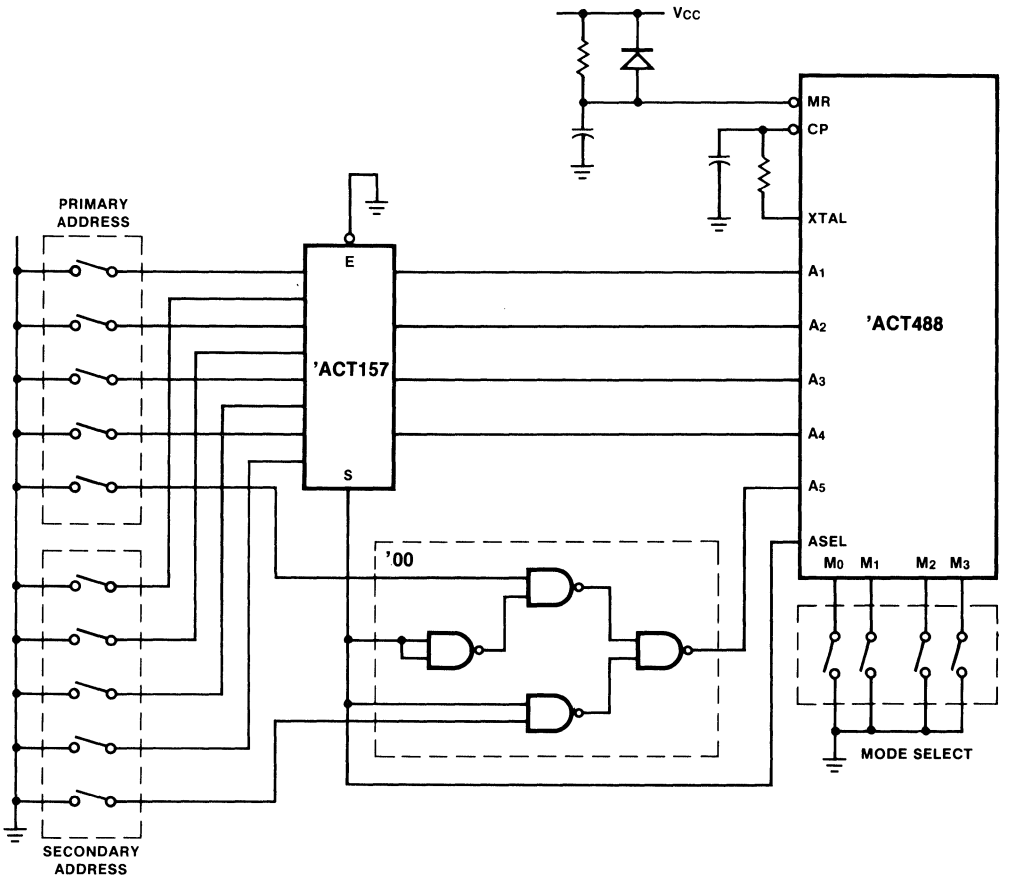
In single address mode the 'ACT488 will go into the addressed state on receipt of the primary address. In extended address mode it will go to the addressed state on receipt of its secondary address if, and only if, it has received its primary address. If a device is addressed to Talk and receives its Listen address it will un-address as a Talker and go to Listener addressed state, and vice versa. A Talker Addressed device will un-address if it receives a non-matching talk address. The 'ACT488 indicates its address status on the $\overline{TAD}$, $\overline{LAD}$ and $\overline{D}$/S/E outputs (Table 3).

5

Table 3: Status Codes

$\overline{TAD}$	$\overline{LAD}$	$\overline{D}$/S/E	State
H	H	L	Off Line
H	L	L	Addressed to Listen (LADS)
L	H	L	Addressed to Talk (TADS)
L	H	H	Serial Poll Mode (SPM)
H	L	H	Receiving END Message (LACS)

Figure 3: Address Multiplexer



Status Response

In Serial Poll Active State (SPAS) the instrument is requested to return a status byte, via the usual handshake, to the Controller. Seven bits are defined by the instrument. Bit 7 denotes the Request Service Status ($\overline{RQS}$) and is provided by the 'ACT488 on the $\overline{RQS}$ output. If the instrument provides no status, other than $\overline{RQS}$, then the $\overline{RQS}$ output can drive the bus directly (Figure 4). If the instrument provides status information this can be multiplexed to the bus using $\overline{D}$/S/E (Figure 5). After the bus handshake, the instrument can send a second status byte by making STRDY LOW then HIGH again, which starts the handshake. The sequence can be repeated to send additional bytes, as long as $\overline{ATN}$ remains HIGH (Figure 16).

Figure 4: Status Bit Driven Direct by RQS

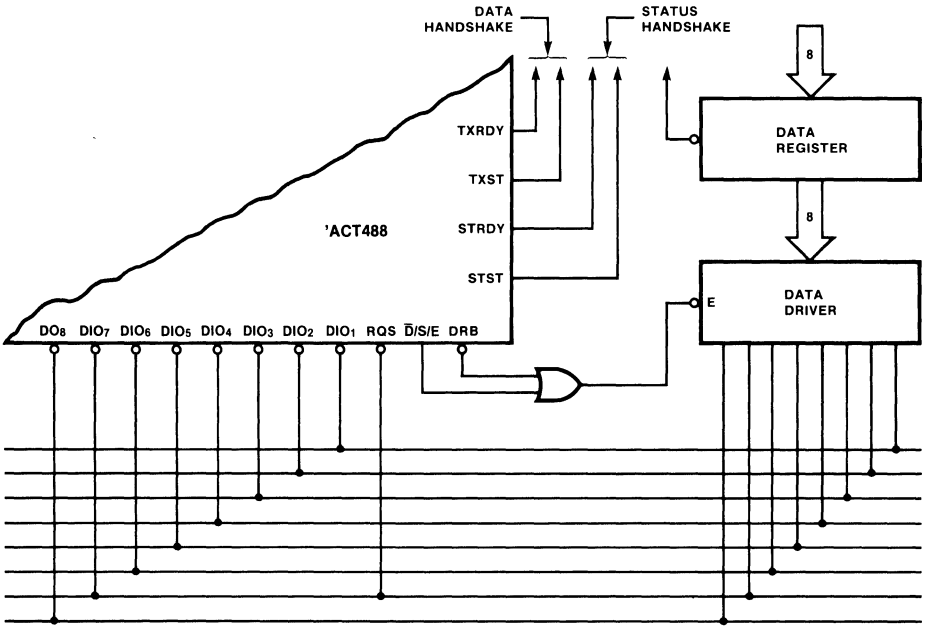
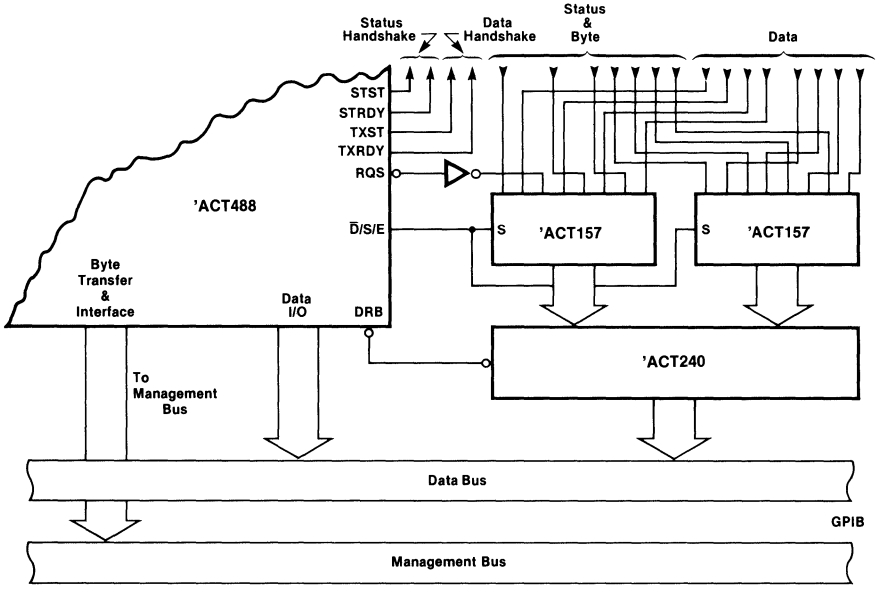


Figure 5: Status Byte Multiplexing



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Clock Input

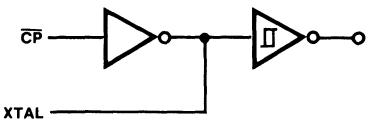
The $\overline{CP}$ and XTAL inputs allow the 'ACT488 either to accept external clock pulses or to generate its own clock (Figure 6).

a. An external clock can drive $\overline{CP}$. The XTAL pin may used as an inverted buffered version of the external clock, but has limited drive capability.

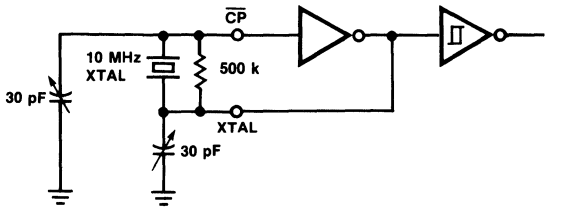
b. The $\overline{CP}$ and XTAL pins will form a stable crystal oscillator by connecting a 10 MHz crystal and an RC network to provide positive feedback. XTAL may be used to clock external circuits provided it is buffered.

Figure 6: Clock Timing Component Connections

a.



b.



Timing Sequences

A 10 MHz clock frequency is recommended to give the correct Source Handshake delays. The 'ACT488 can be clocked at a slower rate if the GPIB is not running at its maximum data rate of 1M byte. The lowest clock frequency allowable is dependent on the GPIB speed.

Regardless of clock frequency, the 'ACT488 will respond to $\overline{ATN}$ within 200 ns by disabling $\overline{NRFD}$, $\overline{NDAC}$ and $\overline{DAV}$ while forcing $\overline{DRB}$ HIGH to disable the data drivers. In Parallel Poll sequences the relevant $\overline{DIO}$ line will be enabled or disabled within 200 ns of an IDY transition.

Since the internal logic of the 'ACT488 is synchronous with the $\overline{CP}$ input, while in general all inputs are asychronous, the precise timing of all responses to external signals is subject to a maximum uncertainty equal to one clock period. This is illustrated in the following timing diagrams, where some delays are defined as t_{CP} + tx (i.e., clock period + propagation delay).

Listen Address Sequence (Figure 7)

a. Controller takes $\overline{ATN}$ line LOW followed by

b. putting the Listen address on the GPIB.

c. Within (t_{CP} + t_{PHL}) the 'ACT488 takes $\overline{NRFD}$ and $\overline{NDAC}$ LOW,

d. and a t_{CP} later takes $\overline{NRFD}$ HIGH, indicating that the 'ACT488 is ready for data.

e. After a delay TCDAV(L) (determined by the Controller logic), the Controller takes $\overline{DAV}$ LOW.

f. Within (t_{CP} + t_{PHL}) the 'ACT488 takes $\overline{NRFD}$ LOW and

g. three clock periods later $\overline{NDAC}$ goes HIGH, indicating that the 'ACT488 has accepted the data,

h. followed by $\overline{LAD}$ indicating listen addressed status.

i. After a Controller dependent delay, TCDAV(H), the $\overline{DAV}$ line goes HIGH and

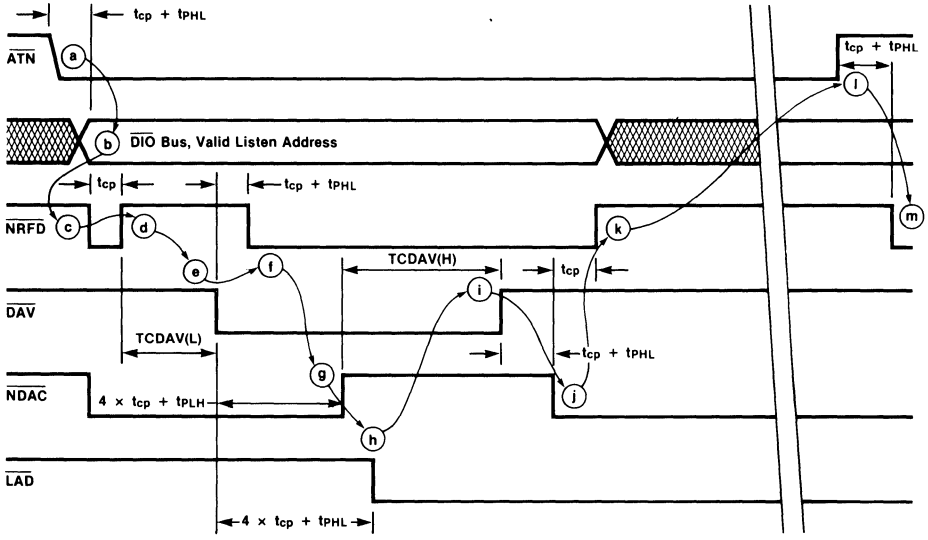
j. within (t_{CP} + t_{PHL}) the 'ACT488 takes $\overline{NDAC}$ LOW.

k. A t_{CP} later the 'ACT488 allows $\overline{NRFD}$ to go HIGH. $\overline{NRFD}$ stays HIGH until the Controller takes $\overline{ATN}$ HIGH, unless a further command is sent over the GPIB when a similar handshake sequence takes place.

l. $\overline{ATN}$ goes HIGH followed by

m. $\overline{NRFD}$ going LOW within (t_{CP} + t_{PHL}). This occurs if the instrument is not ready to receive data (RXRDY LOW). If RXRDY is HIGH, $\overline{NRFD}$ will stay HIGH allowing a data transfer to take place.

Figure 7: Timing Diagram for Listen Address Sequence



Note: $\overline{\text{ATN}}$, $\overline{\text{DIO}}$ bus and $\overline{\text{DAV}}$ driven by controller; $\overline{\text{NRFD}}$, $\overline{\text{NDAC}}$ driven by 'ACT488.

5

Data Transfer from Bus to Listener (Figure 8)[1]
Assuming the instrument logic responds to RXST within one clock period (Figure 8a).

a. The instrument signals it is ready to receive a byte by taking RXRDY HIGH (keeping RXRDY LOW constitutes an "$\overline{\text{NRFD}}$ hold").

b. Provided the 'ACT488 is in the Listen Addressed State (LADS), $\overline{\text{NRFD}}$ is taken HIGH within (t_{CP} + t_{PHL}).

c. When the current Talker sees the $\overline{\text{NRFD}}$ line HIGH it takes $\overline{\text{DAV}}$ LOW after a setting delay TTDAV(L).

d. The 'ACT488 takes RXST HIGH within (t_{CP} + t_{PLH}) to inform the instrument that the GPIB data is valid and takes $\overline{\text{NRFD}}$ LOW.

e. Assuming the instrument responds by pulsing RXRDY LOW within one clock period (t_{PRX} < t_{CP}) then RXST will remain HIGH only for one clock.

f. At the same time as RXST returns LOW, $\overline{\text{NDAC}}$ is taken HIGH to inform the Talker that data has been accepted.

g. After a delay TTDAV(H) determined by the Talker, the $\overline{\text{DAV}}$ line goes HIGH.

h. Within (t_{CP} + t_{PHL}) $\overline{\text{NDAC}}$ goes LOW

i. followed by $\overline{\text{NRFD}}$ going HIGH one clock later.

This assumes that the instrument logic is slow and requires more than one clock period to process a data byte (Figure 8b).

The timing sequence is identical to Figure 8a until RXST goes HIGH.

a. After RXST goes HIGH the instrument delays t_{PRX} (> 1 clock cycle) before taking RXRDY LOW.

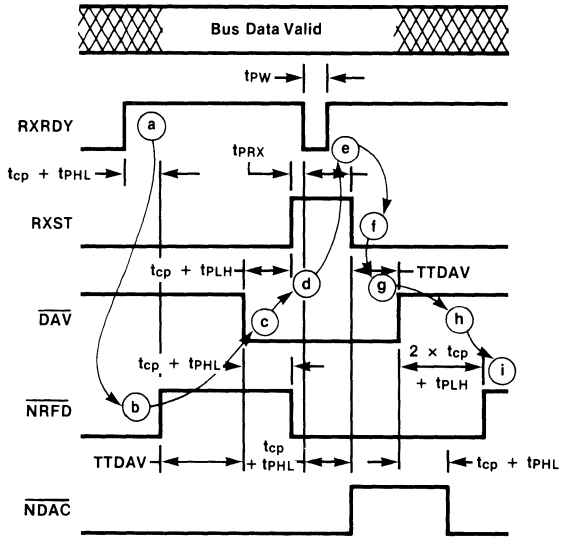
b. RXST will remain HIGH and $\overline{\text{NDAC}}$ will remain LOW during this period, causing the bus data to be maintained valid.

c. RXST goes LOW, and $\overline{\text{NDAC}}$ goes HIGH within (t_{CP} + t_{PHL}) of RXRDY.

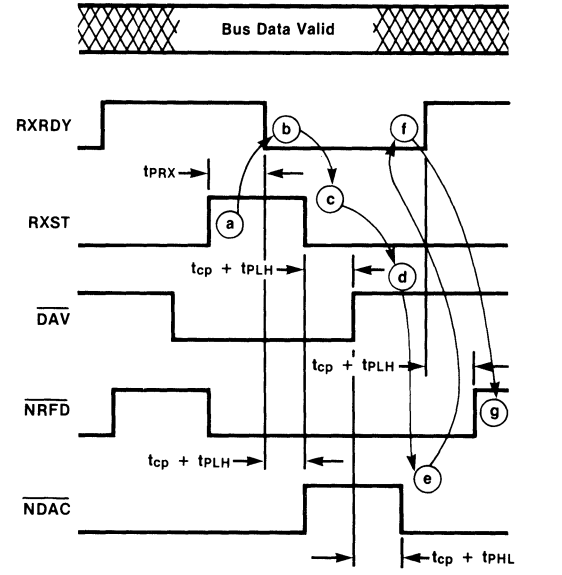
[1]In applications where the bus data can be latched by the RXST rising edge and handshaking is not necessary, RXRDY can be driven by RXST via an inverter.

Figure 8: Timing Diagram, Data Transfer from Bus to Listener

a.



b.



[2]In order to get the source handshake delays specified in IEEE Std 488-1978, tCP must be 100 ns (fCLOCK = 10 MHz).

d. After a delay TTDAV(H) the Talker takes $\overline{DAV}$ HIGH.

e. Within (tCP + tPHL) $\overline{NDAC}$ goes LOW.

f. Assuming the instrument is not ready (i.e., is holding RXRDY LOW) the 'ACT488 holds $\overline{NRFD}$ LOW preventing another data transfer from starting.

g. Within (tCP + tPLH) of RXRDY going HIGH, $\overline{NRFD}$ goes HIGH and the next data transfer cycle can start.

Data Transfer from Talker to GPIB (Figure 9)[2]

a. $\overline{ATN}$ goes HIGH after completion of a Talk address sequence; $\overline{TAD}$ (not shown) is already LOW.

b. Within (tCP + tPHL) $\overline{DRB}$ goes LOW to enable the bus drivers.

c. At a time determined by the instrument logic, TXRDY goes HIGH.

d. If $\overline{NRFD}$ is already HIGH, the 'ACT488 drives $\overline{DAV}$ LOW after delay T1 (11 x tCP + tPHL in high or 20 x tCP + tPHL in low speed). If $\overline{NRFD}$ is LOW, $\overline{DAV}$ will stay HIGH until $\overline{NRFD}$ goes HIGH (assuming T1 has expired). The $\overline{DAV}$ LOW period corresponds to the Source Transfer State (STRS).

e. The Listener(s) responds by eventually taking $\overline{NDAC}$ HIGH.

f. Within (tCP + tPLH) 'ACT488 takes $\overline{DAV}$ HIGH and TXST HIGH to inform the instrument that the data has been accepted and a new byte can be presented.

g. The instrument takes TXRDY LOW and holds it there until it has provided a new byte, h or h'. The minimum time TXRDY must be LOW is tPWL.

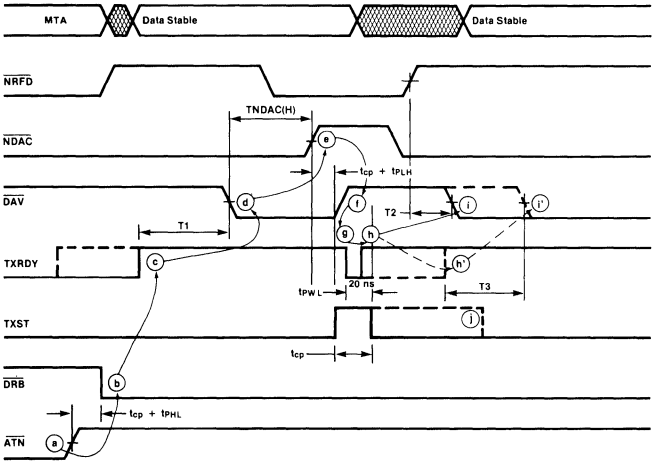
h. If TXRDY pulses LOW within tCP of TXST, TXST(H) will be a minimum of tCP wide. Otherwise TXST goes LOW within (tCP + tPHL) of TXRDY, f. After the first byte is sent, T1 drops from 11 x tCP to 5 x tCP in high-speed mode.

i. If TXRDY is HIGH before $\overline{NRFD}$, $\overline{DAV}$ goes low within T2 of $\overline{NRFD}$ going HIGH (5 x tCP in high speed or 20 x tCP in low speed).

If TXRDY does not go HIGH until h' (after $\overline{NRFD}$ goes HIGH) $\overline{DAV}$ goes LOW T3 later, i' (T3 = 6 x tCP in HIGH and 21 x tCP in low speed).

If the Talk sequence is interrupted by $\overline{ATN}$ while the instrument is generating a new byte (between f and h), $\overline{DRB}$ will go HIGH within 200 ns and the $\overline{DAV}$ line will be relinquished. $\overline{DRB}$ will return LOW and the sequence will continue within (tCP + tPHL) of $\overline{ATN}$ going HIGH. If the 'ACT488 is in high speed mode the first data byte sent will have a delay T1 = 11 x tCP.

Figure 9: Timing Diagram Data Transfer from Talker to Bus



Notes
$\overline{NRFD}$, $\overline{NDAC}$ are driven by the current listener(s); $\overline{DAV}$ is driven by 'ACT488.
T1 = 11 x tCP + tPHL in high speed, 20 x tCP + tPHL in low speed
T2 = 5 x tCP + tPHL in high speed, 20 x tCP + tPHL in low speed
T3 = 6 x tCP + tPHL in high speed, 21 x tCP + tPHL in low speed

Figure 10: Talk Address Sequence

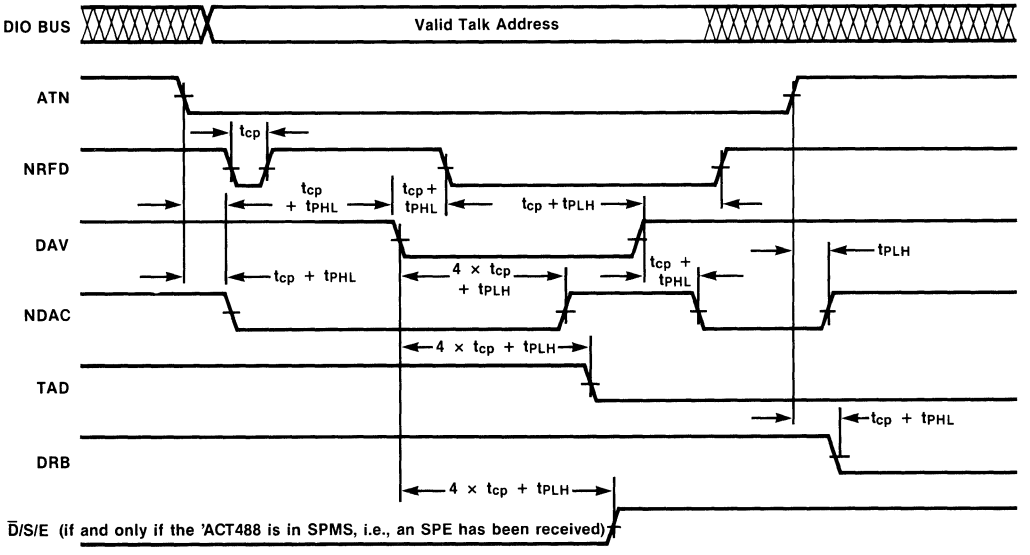


Figure 11: Timing Diagram for Secondary Address Sequence

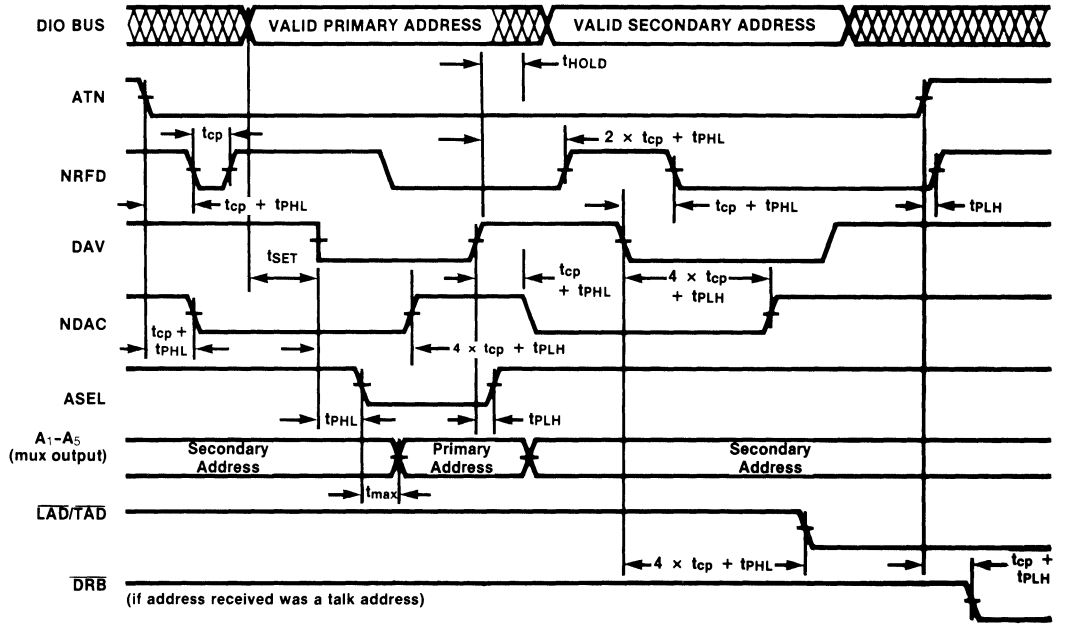
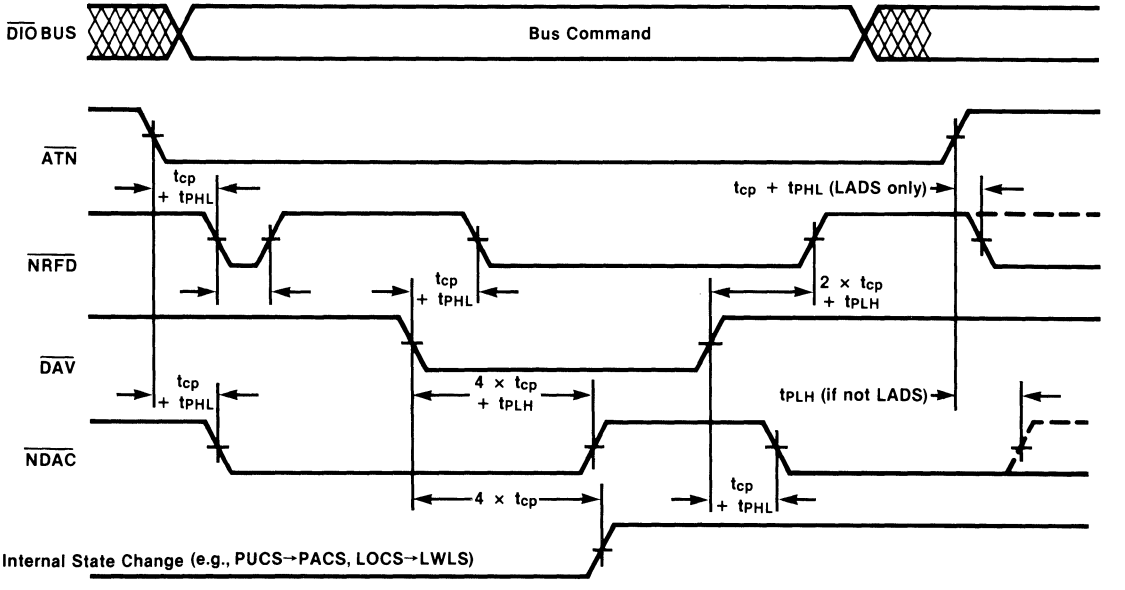


Figure 12: Timing Diagram for 'ACT488 Receiving Bus Commands



Note: Internal state changes do not necessarily change any 'ACT488 outputs.

Figure 13: Timing Diagram for Device Clear and Device Trigger Commands

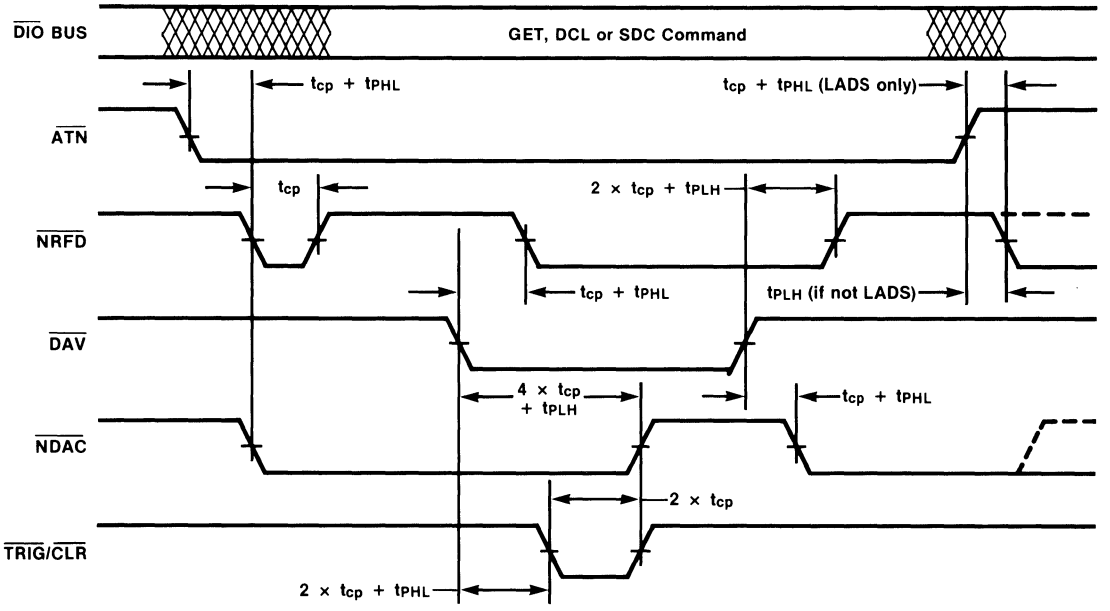
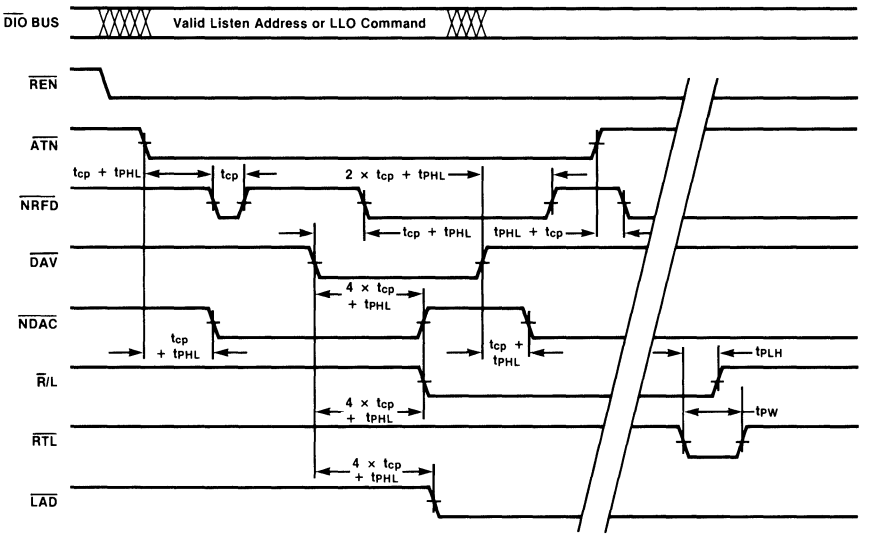
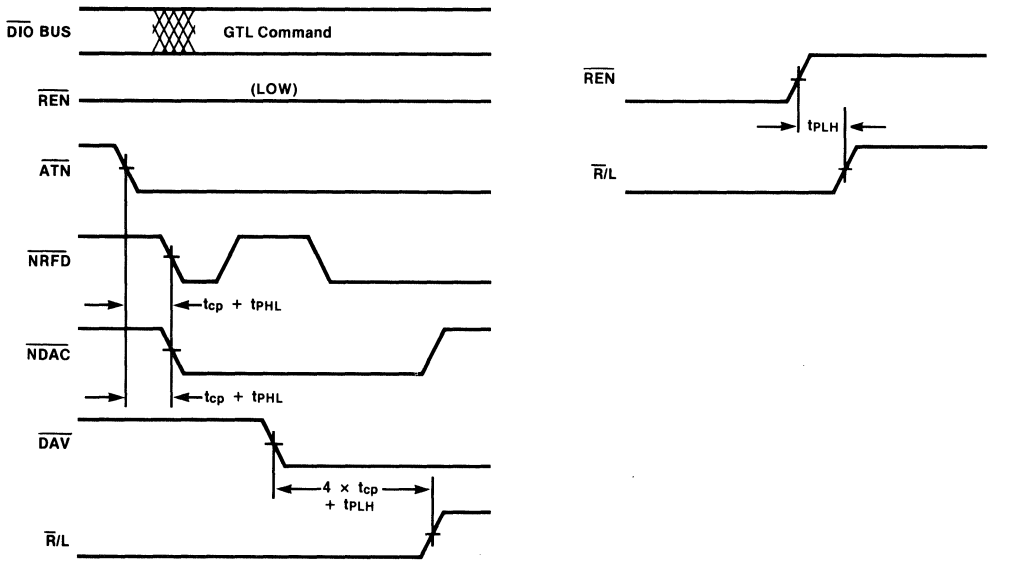


Figure 14: Timing Diagram for Remote/Local Logic (Starting in LOCAL State)



Note: If LLO has been sent, $\overline{RTL}$ will not cause $\overline{R}$/L to change.

Figure 15: Timing Diagram for Remote/Local Logic (Starting in REMOTE State)



Serial Poll Sequence (Figure 16)

a. The Controller has sent the Unlisten (UNL) and Serial Poll Enable (SPE) commands, generally in response to a LOW signal on $\overline{SRQ}$, and places a Talk address on the GPIB. The 'ACT488 is sending the Service Request ($\overline{SRQ}$) message, which was caused by the instrument logic making $\overline{RSV}$ LOW.

b. The 'ACT488 allows $\overline{NRFD}$ to float passive HIGH to initiate normal handshake routine.

c. The Controller forces $\overline{DAV}$ LOW. Since $\overline{ATN}$ is also LOW, the 'ACT488 receives the GPIB information as the message My Talk Address (MTA).

d. $\overline{NRFD}$ is active, acknowledging that the device is receiving a data byte.

e. The 'ACT488 enters the Talker Addressed State at time (4 x t_{CP} + t_{PLH}) after $\overline{DAV}$ was forced LOW.

f. $\overline{D}$/S/E goes HIGH at time (4 x t_{CP} + t_{PLH}) after $\overline{DAV}$ was forced LOW. This indicates that the 'ACT488 is in the Serial Poll Mode.

g. $\overline{NDAC}$ is allowed to float passive HIGH, indicating that the command data byte has been received.

h. The Controller takes $\overline{DAV}$ HIGH.

i. $\overline{NDAC}$ is pulled LOW, showing that the 'ACT488 is ready for a new handshake cycle.

j. The Controller allows the bus to float.

k. The Controller releases $\overline{ATN}$. Because the 'ACT488 is in the Serial Poll Mode, it now enters the Serial Poll Active State (SPAS), which prevails until the Controller makes $\overline{ATN}$ LOW again.

l. $\overline{DRB}$ goes active LOW, allowing the instrument to place its status byte on the bus. $\overline{DRB}$ goes LOW at time (t_{CP} + t_{PHL}) after $\overline{ATN}$ goes HIGH.

m. When the 'ACT488 enters SPAS, $\overline{SRQ}$ goes HIGH at time t_{PLH} after $\overline{ATN}$ goes HIGH.

n. The instrument indicates that a status byte is ready by taking STRDY HIGH. This may occur earlier than shown, without affecting any of the foregoing.

o. $\overline{DRB}$ enables the 3-state output $\overline{RQS}$ when in SPAS. $\overline{RQS}$ goes LOW at time (t_{CP} + t_{PZL}) after $\overline{ATN}$ is released.

p. The Controller has taken $\overline{NRFD}$ HIGH, acknowledging that it is ready for the status byte.

q. The 'ACT488 takes $\overline{DAV}$ LOW after the time interval T_1, which starts either at the rising edge of STRDY or the falling edge of $\overline{DRB}$, whichever occurs later. The $\overline{DAV}$ LOW period corresponds to the Source Transfer State (STRS).

r. The Controller takes $\overline{NRFD}$ LOW.

s. The instrument may release $\overline{RSV}$ at any time after the 'ACT488 enters SPAS.

t. The Controller takes $\overline{DNAC}$ HIGH, acknowledging that it has received the status byte.

u. The 'ACT488 releases $\overline{DAV}$ at time (t_{CP} + t_{PLH}) after $\overline{NDAC}$ goes HIGH.

v. STST goes HIGH at time (t_{CP} + t_{PLH}) after $\overline{NDAC}$ goes HIGH. This tells the instrument that the status byte has been accepted. The instrument takes STRDY LOW to indicate that the data is no longer valid and to allow STST to go LOW again one t_{CP} after STRDY goes LOW.

w. The controller takes $\overline{NDAC}$ LOW once more after $\overline{DAV}$ goes HIGH.

x. The data on the bus is no longer valid. If the $\overline{ATN}$ line remains HIGH, the instrument can provide another status byte by making STRDY HIGH to indicate valid data and to start the handshake.

y. At the completion of the Serial Poll of this instrument, the Controller assumes control of the bus by forcing $\overline{ATN}$ LOW.

z. $\overline{DRB}$ goes HIGH at time t_{PLH} after $\overline{ATN}$ goes LOW. This places the bus drivers of this instrument in the high-impedance (3-state output) or off (open-drain outputs) state.

aa. Since $\overline{DRB}$ is no longer valid, the $\overline{RQS}$ output reverts to its high-impedance state.

bb. $\overline{NRFD}$ goes HIGH, indicating that devices are ready to receive a command from the bus.

cc. The Controller forces $\overline{DAV}$ LOW to show that it has placed a control byte on the bus.

dd. $\overline{NRFD}$ goes LOW to acknowledge $\overline{DAV}$.

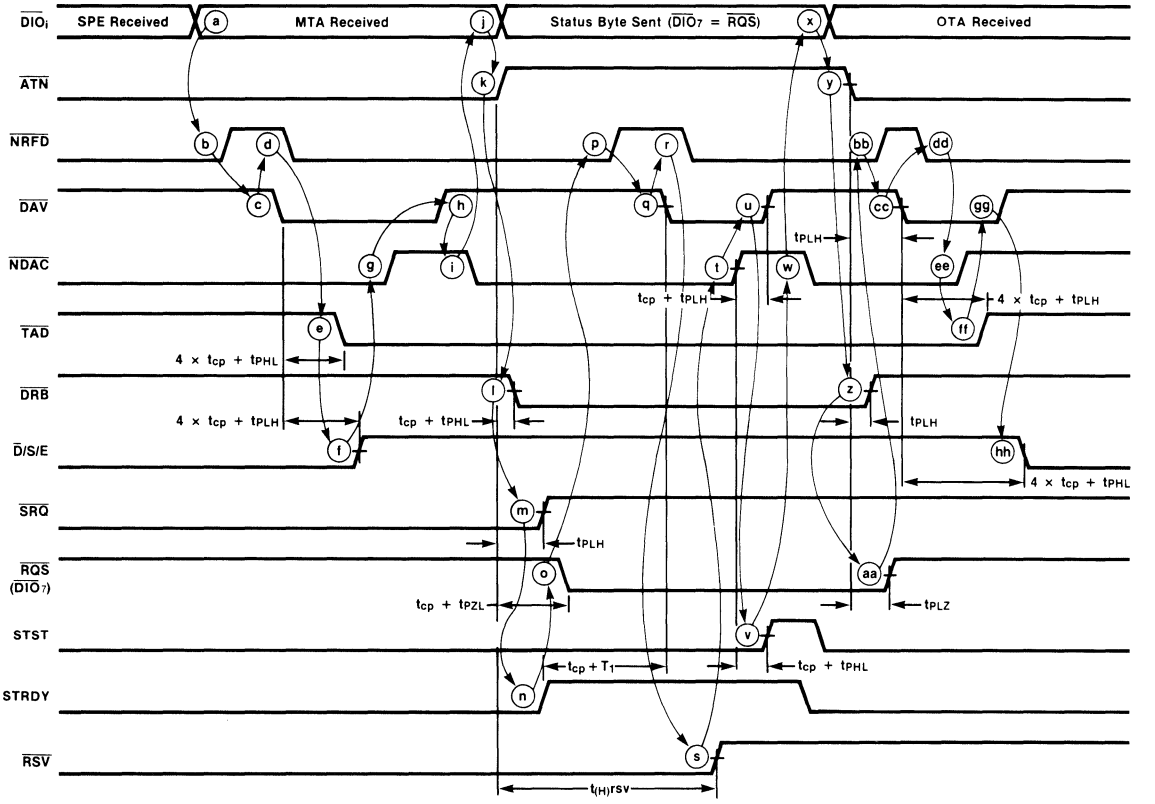
ee. $\overline{NDAC}$ goes HIGH when devices all acknowledge acceptance of the command byte.

ff. The 'ACT488 has received the Other Talk Address (OTA) command and reverts to its unaddressed state. $\overline{TAD}$ goes HIGH at time (4 x t_{CP} + t_{PLH}) after $\overline{DAV}$ went LOW.

gg. $\overline{DAV}$ is set HIGH by the Controller.

hh. Because the 'ACT488 has been unaddressed it is no longer in the Serial Poll Active State (SPAS). The $\overline{D}$/S/E output goes LOW at time (4 x t_{CP} + t_{PHL}) after $\overline{DAV}$ went HIGH. The 'ACT488 is still in the Serial Poll Mode State (SPMS), however, and will return to SPAS ($\overline{D}$/S/E HIGH, STST and STRDY valid) if subsequently addressed to talk. The 'ACT488 enters the Serial Poll Idle State (SPIS) when the Controller either issues the Serial Poll Disable (SPD) command or makes $\overline{IFC}$ LOW.

Figure 16: Timing Diagram for Serial Poll Sequence



Parallel Poll Sequence (Figure 17)

a. The Controller sends the instrument's listen address,

b. then the Controller issues the Parallel Poll Configure command: this enables the 'ACT488 to receive a subsequent PPE command.

c. The Contoller issues the Parallel Poll Enable command. Bits $\overline{D}_1$ - $\overline{D}_3$ of the command byte determine which data output ($\overline{DIO}_j$) will be valid when the IDY command is sent. Bit $\overline{D}_4$ of the command is compared with IST (Instrument Status) during the IDY command.

d. The Controller issues the Unlisten command. The 'ACT488 will now not respond to further PPE commands, allowing the Controller to configure other instruments.

e. The Instrument Status bit (IST) is set by the instrument before an IDENTIFY command is received. IST must be in a stable state when IDY is received so the setup and hold times must be observed (t_s IST and t_h IST).

f. During the IDY command the Controller releases the data lines $\overline{DIO}_1$ - $\overline{DIO}_7$, $\overline{DO}_8$. The assigned data line $\overline{DIO}_j$ will be taken active LOW by the 'ACT488 if IST compares with bit $\overline{D}_4$ of the PPE command.

g. The IDY Message is received (IDY = $\overline{EOI}$ • $\overline{ATN}$). At this time the Instrument Status bit IST is latched in the 'ACT488, and the output data $\overline{DIO}_j$ is true if IST compares with bit $\overline{D}_4$ of the PPE command. $\overline{DIO}_j$ is LOW if $\overline{D}_4$ was LOW and IST was HIGH, or if $\overline{D}_4$ was HIGH and IST was LOW.

h. The 'ACT488 enables data bit $\overline{DIO}_j$ after a delay t_{PHL} from the time $\overline{EOI}$ goes active LOW. $\overline{DIO}_j$ remains valid while IDY is active. Note that this is an asynchronous message sent and is not governed by the handshake protocol.

i. IST may be altered not less than time t_h IST after IDY is active. Because IST is latched by IDY it will not affect the status byte sent during the IDY routine.

j. IDY is false and the 'ACT488 stops sending a status byte. Outputs $\overline{DIO}_1$ - $\overline{DIO}_7$, $\overline{DO}_8$ again float passive HIGH.

k. The status bit $\overline{DIO}_j$ floats passive HIGH at a time not greater than t_{PLH} after IDY goes FALSE.

l. The Controller can now place information on the data bus.

m. Once the 'ACT488 has been configured via steps a-c, the Controller can examine IST at any time by issuing the IDY command. To change the $\overline{D}_1$ - $\overline{D}_4$ assignment of a particular 'ACT488, the Controller must address it to listen, issue the PPC command, then the Parallel Poll Disable (PPD) command (which clears the $\overline{D}_1$ - $\overline{D}_4$ latches), then the PPE command with the revised $\overline{D}_1$ - $\overline{D}_4$ assignment. The $\overline{D}_1$ - $\overline{D}_4$ assignment will also be cleared by the universal Parallel Poll Unconfigure (PPU) command or by $\overline{MR}$, but not by $\overline{IFC}$. PPU, $\overline{MR}$ or the MLA/PPC/PPD sequence puts the 'ACT488 in the Parallel Poll Idle State (PPIS) and it will not respond to IDY until it is subsequently reconfigured.

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Figure 17: Timing Diagram for Parallel Poll Sequence

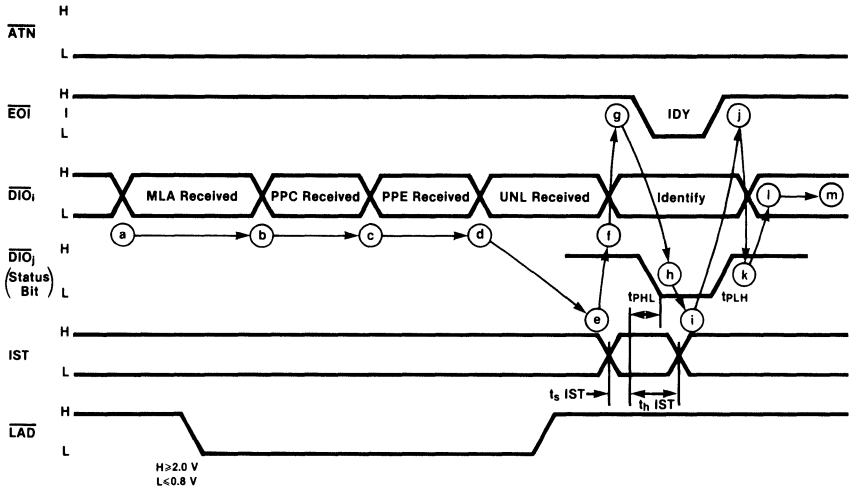
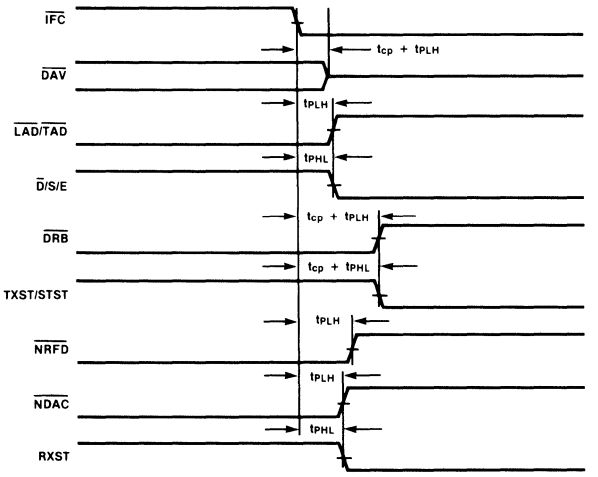


Figure 18: IFC Timing Diagram



Absolute Maximum Ratings

(above which the useful life may be impaired)

Storage Temperature	—65°C to +150°C
Temperature (Ambient) Under Bias	—55°C to +125°C
Vcc Pin Potential to Ground Pin	—0.5 V to +7.0 V
*Input Voltage (DC)	Bus Pins 0.5 to 12 V; Others 0 to Vcc +0.5 V
*Input Current (DC)	±20 mA
Voltage Applied to Outputs (Output HIGH)	—0.5 V to +5.5 V
Output Current (DC) (Output LOW)	Bus Pins +64 mA; Others +24 mA

*Either input voltage limit or input current limit is sufficient to protect the inputs.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54ACT	74ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current			μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current			μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT488)			mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case
V_{IH}	Input HIGH Voltage All Inputs (except $\overline{CP}$)	2.0		V	Recognized as a HIGH Signal Over Recommended V_{CC} Range
V_{IL}	Input LOW Voltage All Inputs (except $\overline{CP}$)		0.8	V	Recognized as a LOW Signal Over Recommended V_{CC} Range
$V_{T+}-V_{T-}$	Hysteresis Voltage	Typ = 0.4		V	All Bus Inputs
V_{CD}	Input Clamp Diode Voltage			V	I_{IN} = -18 mA
V_{OH}	Output HIGH Voltage $\overline{RQS}$, $\overline{DAV}$	2.4		V	I_{OH} = -5.2 mA
	$\overline{DIO_1}$ - $\overline{DIO_7}$, $\overline{DO_8}$, $\overline{SRQ}$, $\overline{NRFD}$, $\overline{NDAC}$	2.6		V	Open Collector Bus Pins I_{OH} = 0 mA
	$\overline{R}$/L, $\overline{D}$/S/E, RXST, TXST, STST, $\overline{CLR}$, $\overline{TRIG}$, $\overline{DRB}$, ASEL, XTAL, $\overline{LAD}$, $\overline{TAD}$	2.5		V	I_{OH} = -0.4 mA
V_{OL}	Output LOW Voltage $\overline{DIO_1}$ - $\overline{DIO_7}$, $\overline{DO_8}$, $\overline{SRQ}$, $\overline{RQS}$, $\overline{NRFD}$, $\overline{NDAC}$, $\overline{DAV}$		0.5	V	I_{OL} = 48 mA
	All Other Outputs		0.4	V	I_{OL} = 4.0 mA
			0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current			μA	$V_{IN} = 2.7$ V
I_{IL}	Input LOW Current			mA	$V_{IN} = 0.4$ V
I_{POFS}	Leakage into GPIB Pins in Powered-off State			μA	V_{IN} = 2.5 V

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DC Characteristics (cont'd)

Symbol	Parameter	54ACT	74ACT	Units	Conditions
I_{OZH}	3-State Output OFF Current HIGH			μA	V_{OUT} = 2.4 V
I_{OZL}	3-State Output OFF Current LOW			μA	V_{OUT} = 0.4 V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0								MHz	3-3
t_{PLH}	Propagation Delay $\overline{CP}$ to $\overline{NRFD}$	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{NRFD}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{ATN}$ to $\overline{NRFD}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{CP}$ to $\overline{NDAC}$	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{NDAC}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{ATN}$ to $\overline{NDAC}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{CP}$ to $\overline{DAV}$	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{DAV}$	5.0								ns	3-6
t_{PLZ}	Output Disable Time $\overline{ATN}$ to $\overline{DAV}$	5.0								ns	3-8
t_{PHZ}	Output Disable Time $\overline{ATN}$ to $\overline{DAV}$	5.0								ns	3-7
t_{PZH}	Output Enable Time $\overline{CP}$ to $\overline{DAV}$	5.0								ns	3-7
t_{PLZ}	Output Disable Time $\overline{CP}$ to $\overline{DAV}$	5.0								ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics (cont'd)

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHZ}	Output Disable Time $\overline{CP}$ to $\overline{DAV}$	5.0								ns	3-7
t_{PLH}	Propagation Delay $\overline{IFC}$ to $\overline{LAD}$ or $\overline{TAD}$	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{IFC}$ to $\overline{D}$/S/E	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{CP}$ to $\overline{LAD}$ or $\overline{TAD}$	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{LAD}$ or $\overline{TAD}$	5.0								ns	3-6
t_{PLH}	Propagation Delay M_0 - M_3 to $\overline{LAD}$ or $\overline{TAD}$	5.0								ns	3-6
t_{PHL}	Propagation Delay M_0 - M_3 to $\overline{LAD}$ or $\overline{TAD}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{CP}$ to RXST, TXST or STST	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{CP}$ to RXST, TXST or STST	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{CP}$ to $\overline{DRB}$	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{DRB}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{ATN}$ to $\overline{DRB}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{CP}$ to $\overline{TRIG}$ or $\overline{CLR}$	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{TRIG}$ or $\overline{CLR}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{DAV}$ to ASEL	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{DAV}$ to ASEL	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to RXST, TXST, STST or $\overline{D}$/S/E	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{LAD}$, $\overline{TAD}$ or $\overline{R}$/L	5.0								ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics (cont'd)

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{NRFD}$, $\overline{NDAC}$, $\overline{DAC}$, $\overline{DIO_1}$ - $\overline{DIO_7}$, $\overline{DO_8}$ or $\overline{SRQ}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{CP}$ to XTAL	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{CP}$ to XTAL	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{CP}$ to $\overline{R}$/L	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{R}$/L	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{RTL}$ to $\overline{R}$/L	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{REN}$ to $\overline{R}$/L	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{CP}$ to $\overline{D}$/S/E	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{CP}$ to $\overline{D}$/S/E	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{RSV}$ to $\overline{SRQ}$	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{RSV}$ to $\overline{SRQ}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{ATN}$ to $\overline{SRQ}$	5.0								ns	3-6
t_{PZL}	Output Enable Time $\overline{CP}$ to $\overline{RQS}$	5.0								ns	3-6
t_{PZH}	Output Enable Time $\overline{CP}$ to $\overline{RQS}$	5.0								ns	3-6
t_{PLZ}	Output Disable Time $\overline{ATN}$ to $\overline{RQS}$	5.0								ns	3-8
t_{PHZ}	Output Disable Time $\overline{ATN}$ to $\overline{RQS}$	5.0								ns	3-7
t_{PLH}	Propagation Delay $\overline{EOI}$ to $\overline{DIO_1}$ - $\overline{DIO_7}$, $\overline{DO_8}$	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{EOI}$ to $\overline{DIO_1}$ - $\overline{DIO_7}$, $\overline{DO_8}$	5.0								ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics (cont'd)

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay $\overline{EOI}$ to $\overline{D/S/E}$	5.0								ns	3-6
t_{PHL}	Propagation Delay $\overline{EOI}$ to $\overline{D/S/E}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{DR}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{ISC}$ to $\overline{TAD}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{ISC}$ to $\overline{LAD}$	5.0								ns	3-6
t_{PLH}	Propagation Delay $\overline{MR}$ to $\overline{RQS}$	5.0								ns	3-6
t_{PLZ}	Propagation Delay Mode to $\overline{NRFD}$	5.0								ns	3-8
t_{PLZ}	Propagation Delay Mode to $\overline{NDAC}$	5.0								ns	3-8
t_{PZH}	Propagation Delay Mode to $\overline{DAV}$	5.0								ns	3-7
t_{PHZ}	Propagation Delay Mode to $\overline{DAV}$	5.0								ns	3-7

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW IST to $\overline{EOI}$	5.0					ns	3-9
t_h	Hold Time, HIGH or LOW IST to $\overline{EOI}$	5.0					ns	3-9
t_s	Setup Time, LOW $\overline{RSV}$ to $\overline{ATN}$	5.0					ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Operating Requirements (cont'd)

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_h	Hold Time, LOW $\overline{RSV}$ to $\overline{ATN}$	5.0					ns	3-9
t_s	Setup Time, LOW $\overline{ATN}$ to $\overline{CP}$	5.0					ns	3-9
t_h	Hold Time, LOW $\overline{ATN}$ to $\overline{CP}$	5.0					ns	3-9
t_w (H) t_w (L)	$\overline{CP}$ Pulse Width	5.0					ns	3-6
t_w	Pulse Width, LOW RXRDY, TXRDY or STRDY	5.0					ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	5.0					ns	3-6
t_w	$\overline{RTL}$ Pulse Width, LOW	5.0					ns	3-6
t_s (H) t_s (L)	Setup Time $\overline{DIO_1}$ - $\overline{DIO_7}$ to $\overline{CP}$	5.0					ns	3-9
t_h (H) t_h (L)	Hold Time $\overline{DIO_0}$ - $\overline{DIO_7}$ to $\overline{CP}$	5.0					ns	3-9
t_s	Setup Time, HIGH or LOW, $\overline{DAV}$ to $\overline{CP}$	5.0					ns	3-9
t_h	Hold Time, HIGH or LOW, $\overline{DAV}$ to $\overline{CP}$	5.0					ns	3-9
t_s (H) t_s (L)	Setup Time RXRDY, TXRDY, STRDY	5.0					ns	3-9
t_s (H) t_s (L)	Setup Time $\overline{NRFD}$ to $\overline{CP}$	5.0					ns	3-9
t_s (H)	Setup Time $\overline{NDAC}$ to $\overline{CP}$	5.0					ns	3-9
t_s (H) t_s (L)	Setup Time Address to $\overline{CP}$	5.0					ns	3-9
t_w (L)	$\overline{IFC}$ Pulse Width, LOW	5.0					ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Symbol	Parameter	54/74ACIACT Typ	Units	Conditions
C_{IN}	Input Capacitance		pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

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8-Bit Identity Comparator

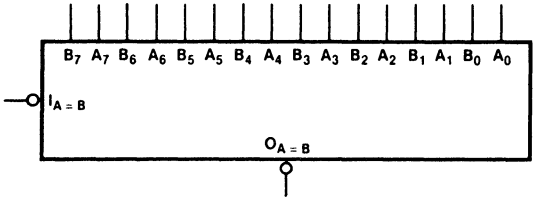
Description

The 'AC/'ACT520/521 are expandable 8-bit comparators. They compare two words of up to eight bits each and provide a LOW output when the two words match bit for bit. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input. The '521 features a pull-up resistor on each input.

- **Compares Two 8-Bit Words in 6.5 ns Typ**
- **Expandable to Any Word Length**
- **20-Pin Package**
- **Outputs Source/Sink 24 mA**
- **'521 has Input Pull-Up Resistors**
- **'ACT520 and 'ACT521 have TTL-Compatible Inputs**

Ordering Code: See Section 6

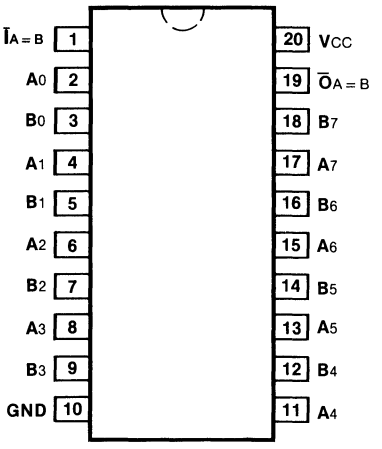
Logic Symbol



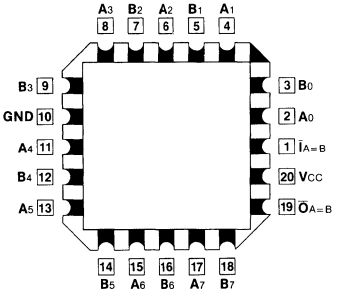
Pin Names

A_0 - A_7	Word A Inputs
B_0 - B_7	Word B Inputs
$\overline{I}_{A=B}$	Expansion or Enable Input
$\overline{O}_{A=B}$	Identity Output

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

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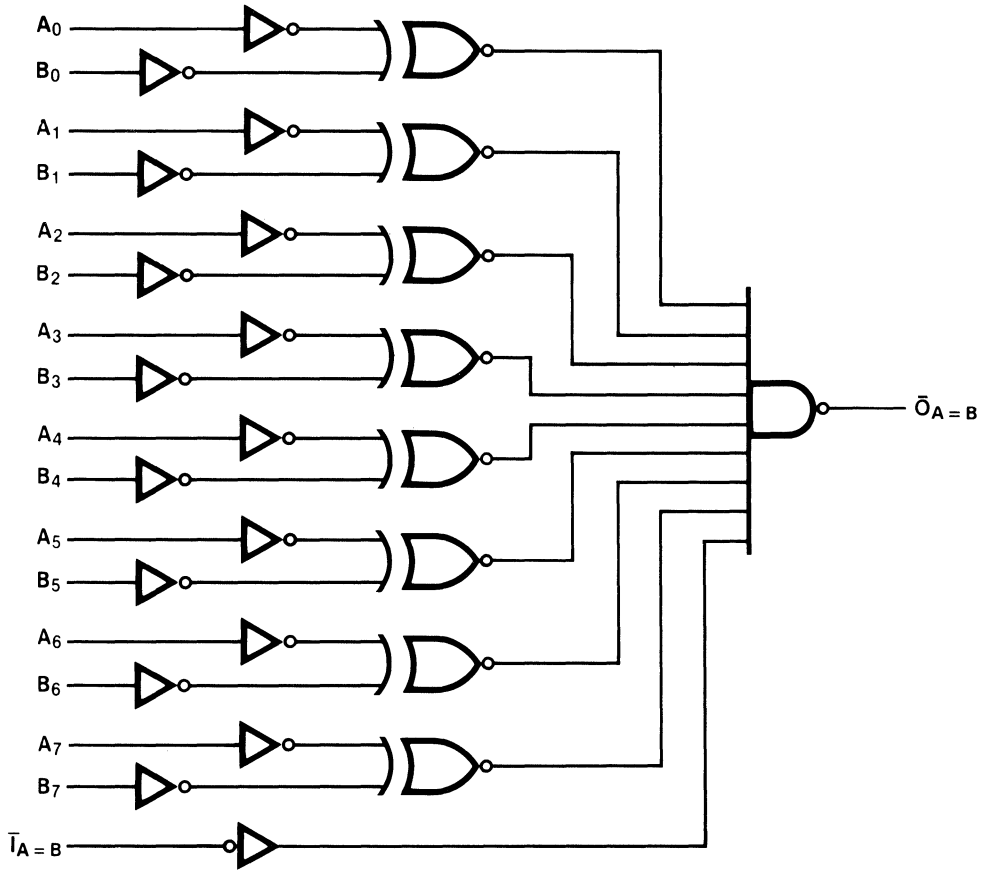
Truth Table

Inputs		Outputs
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B*	L
L	A ≠ B	H
H	A = B*	H
H	A ≠ B	H

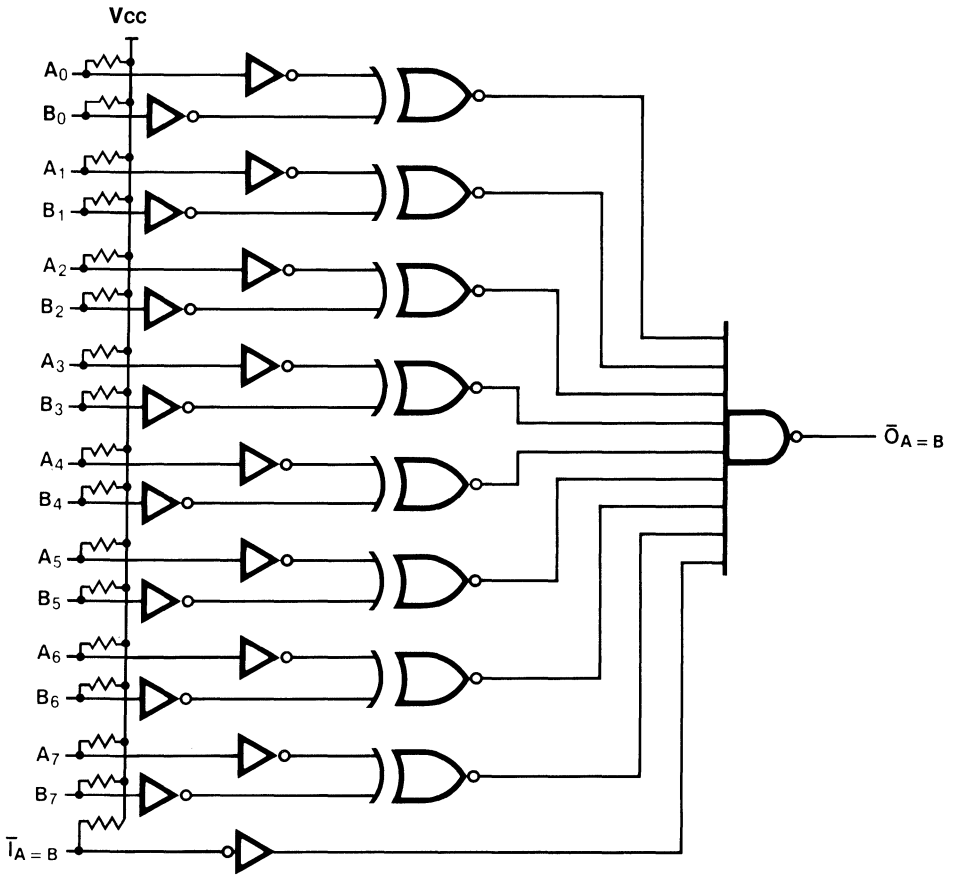
H = HIGH Voltage Level
L = LOW Voltage level
*$A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

Logic Diagram ('AC/'ACT520)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagram ('AC/'ACT521)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT520/521)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.3		13.0						ns	3-6
		5.0		9.5							
t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	3.3		13.0						ns	3-6
		5.0		9.5							
t_{PLH}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3		9.0						ns	3-6
		5.0		6.5							
t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	3.3		9.5						ns	3-6
		5.0		7.0							

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	5.0		9.5						ns	3-6
t_{PHL}	Propagation Delay A_n or B_n to $\overline{O}_{A=B}$	5.0		9.5						ns	3-6
t_{PLH}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0		6.5						ns	3-6
t_{PHL}	Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	5.0		7.0						ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

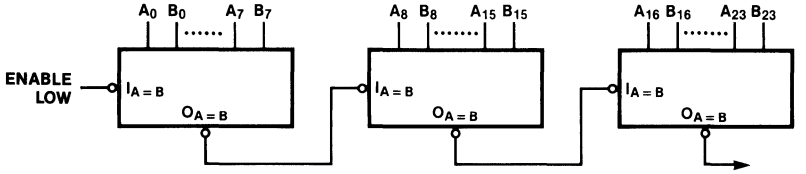
Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

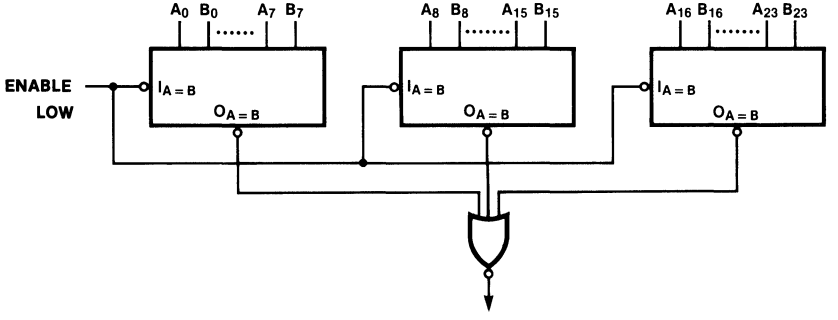
Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

Applications

Ripple Expansion



Parallel Expansion



54AC/74AC533 • 54ACT/74ACT533

Octal Transparent Latch With 3-State Outputs

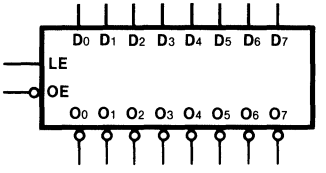
Description

The 'AC/'ACT533 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state. The 'AC/'ACT533 is the same as the 'AC/'ACT373, except that the outputs are inverted on the 'AC/'ACT533. For functional description please refer to the 'AC/'ACT373 data sheet.

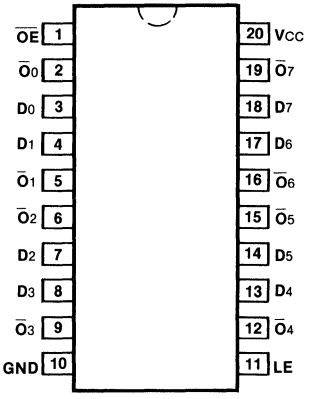
- **Eight Latches in a Single Package**
- **3-State Outputs for Bus Interfacing**
- **Outputs Source/Sink 24 mA**
- **'ACT533 has TTL-Compatible Inputs**
- **Inverted Output Version of 'ACT373**

Ordering Code: See Section 6

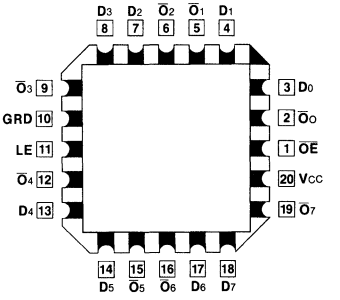
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC

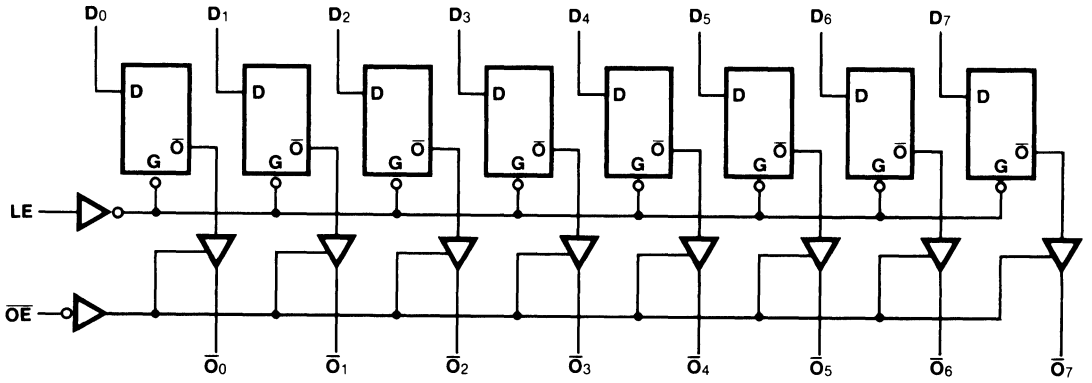


Pin Assignment for LCC

Pin Names

D_0 - D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Input
$\overline{O}_0$ - $\overline{O}_7$	Complementary 3-State Outputs

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT533)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to $\overline{O}_n$	3.3 5.0		8.0 5.0						ns	3-5
t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	3.3 5.0		7.0 5.0						ns	3-5
t_{PLH}	Propagation Delay LE to $\overline{O}_n$	3.3 5.0		8.0 5.0						ns	3-6
t_{PHL}	Propagation Delay LE to $\overline{O}_n$	3.3 5.0		7.0 5.0						ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		6.5 4.5						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		6.0 4.5						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 5.0						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		5.0 3.5						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	3.5 2.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	−2.5 −1.5				ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	3.0 2.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to $\overline{O}_n$	5.0		7.0						ns	3-5
t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	5.0		6.5						ns	3-5
t_{PLH}	Propagation Delay LE to $\overline{O}_n$	5.0		6.5						ns	3-6
t_{PHL}	Propagation Delay LE to $\overline{O}_n$	5.0		6.0						ns	3-6
t_{PZH}	Output Enable Time	5.0		6.0						ns	3-7
t_{PZL}	Output Enable Time	5.0		5.5						ns	3-8
t_{PHZ}	Output Disable Time	5.0		7.5						ns	3-7
t_{PLZ}	Output Disable Time	5.0		5.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	2.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−1.5				ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC534 • 54ACT/74ACT534

Octal D-Type Flip-Flop With 3-State Outputs

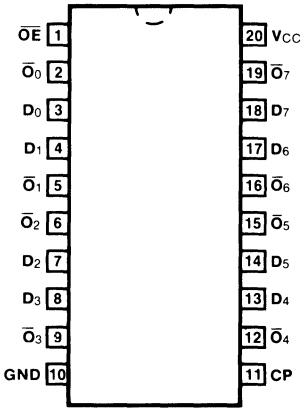
Description

The 'AC/'ACT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The 'AC/'ACT534 is the same as the 'AC/'ACT374 except that the outputs are inverted.

- **Edge-Triggered D-Type Inputs**
- **Buffered Positive Edge-Triggered Clock**
- **3-State Outputs for Bus-Oriented Applications**
- **Outputs Source/Sink 24 mA**
- **'ACT534 has TTL-Compatible Inputs**
- **Inverted Output Version of 'AC/'ACT374**

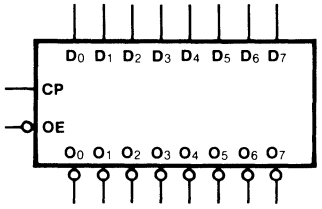
Ordering Code: See Section 6

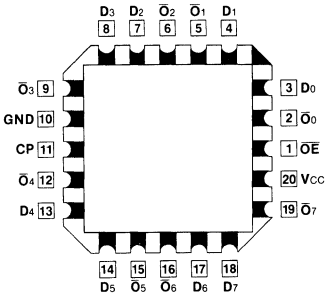
Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC

Logic Symbol





Pin Assignment for LCC

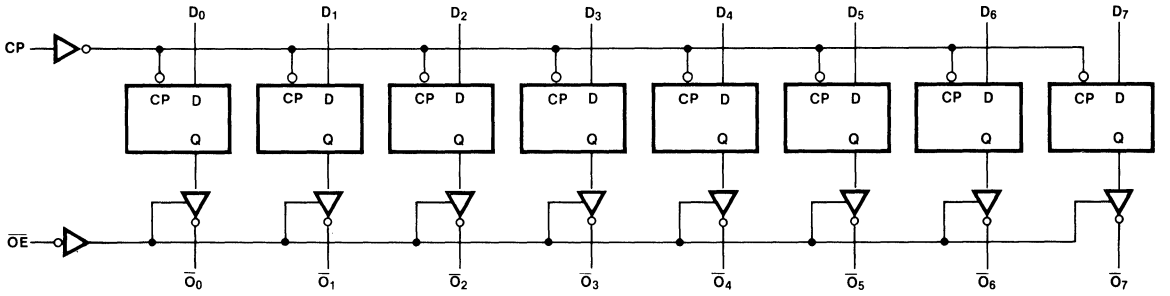
Pin Names

D_0 - D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-State Output Enable Input
$\overline{O}_0$ - $\overline{O}_7$	Complementary 3-State Outputs

Functional Description

The 'AC/'ACT534 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT534)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		125 150						MHz	3-3
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0		10.0 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0		9.5 6.5						ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		8.5 6.5						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		8.5 6.0						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		9.0 7.0						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		7.5 6.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 −0.5				ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	3.5 2.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		100						MHz	3-3
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	5.0		6.5						ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{O}_n$	5.0		6.0						ns	3-6
t_{PZH}	Output Enable Time	5.0		5.5						ns	3-7
t_{PZL}	Output Enable Time	5.0		5.5						ns	3-8
t_{PHZ}	Output Disable Time	5.0		7.0						ns	3-7
t_{PLZ}	Output Disable Time	5.0		5.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5				ns	3-9
t_w	CP Pulse Width, HIGH or LOW	5.0	2.5				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC540 • 54ACT/74ACT540
54AC/74AC541 • 54ACT/74ACT541

Octal Buffer/Line Driver With 3-State Outputs

Description

The 'AC/'ACT540 and 'AC/'ACT541 are octal buffer/line drivers designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers. The 'AC/'ACT541 is a noninverting option of the 'AC/'ACT540.

These devices are similar in function to the 'AC/'ACT240 and 'AC/'ACT244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

- **3-State Outputs**
- **Inputs and Outputs Opposite Side of Package, Allowing Easier Interface to Microprocessors**
- **Output Source/Sink 24 mA**
- **'AC/'ACT540 Provides Inverted Outputs**
- **'AC/'ACT541 Provides Noninverted Outputs**
- **'ACT540 and 'ACT541 have TTL-Compatible Inputs**

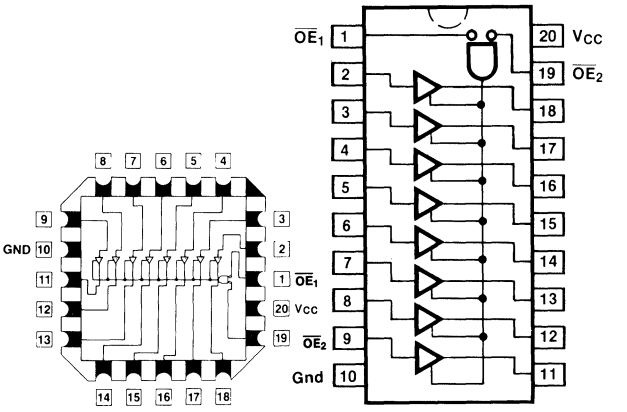
Ordering Code: See Section 6

Truth Table

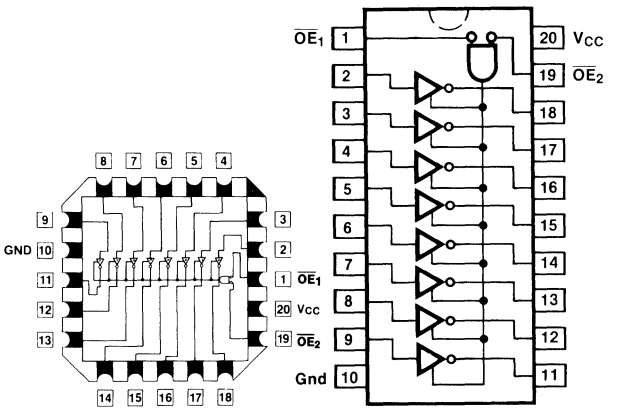
Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	D	'540	'541
L	L	H	L	L
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Connection Diagrams



'AC/'ACT540



'AC/'ACT541

Pin Assignment for LCC

Pin Assignment for DIP, Flatpak and SOIC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT540/541)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output ('AC540)	3.3 5.0	1.0 1.0	5.5 4.0	7.5 6.0	1.0 1.0	9.0 7.0	1.0 1.0	8.0 6.5	ns	3-5
t_{PHL}	Propagation Delay Data to Output ('AC540)	3.3 5.0	1.0 1.0	5.0 4.0	7.0 5.5	1.0 1.0	8.0 6.5	1.0 1.0	7.5 6.0	ns	3-5
t_{PZH}	Output Enable Time ('AC540)	3.3 5.0	1.0 1.0	8.5 6.5	11.0 8.5	1.0 1.0	13.0 10.0	1.0 1.0	12.0 9.5	ns	3-7
t_{PZL}	Output Enable Time ('AC540)	3.3 5.0	1.0 1.0	7.5 6.0	10.0 7.5	1.0 1.0	12.0 9.0	1.0 1.0	11.0 8.5	ns	3-8
t_{PHZ}	Output Disable Time ('AC540)	3.3 5.0	1.0 1.0	8.5 7.5	13.0 10.5	1.0 1.0	15.5 12.0	1.0 1.0	14.0 11.0	ns	3-7
t_{PLZ}	Output Disable Time ('AC540)	3.3 5.0	1.0 1.0	7.0 6.0	10.0 8.0	1.0 1.0	12.0 10.0	1.0 1.0	11.0 9.0	ns	3-8
t_{PLH}	Propagation Delay Data to Output ('AC541)	3.3 5.0	1.0 1.0	5.5 4.0	8.0 6.0	1.0 1.0	10.0 7.0	1.0 1.0	9.0 6.5	ns	3-5
t_{PHL}	Propagation Delay Data to Output ('AC541)	3.3 5.0	1.0 1.0	5.5 4.0	8.0 6.0	1.0 1.0	9.5 7.0	1.0 1.0	8.5 6.5	ns	3-5
t_{PZH}	Output Enable Time ('AC541)	3.3 5.0	1.0 1.0	8.0 6.0	11.5 8.5	1.0 1.0	13.5 10.0	1.0 1.0	12.5 9.5	ns	3-7
t_{PZL}	Output Enable Time ('AC541)	3.3 5.0	1.0 1.0	7.0 5.5	10.0 7.5	1.0 1.0	12.5 9.0	1.0 1.0	11.5 8.5	ns	3-8
t_{PHZ}	Output Disable Time ('AC541)	3.3 5.0	1.0 1.0	9.0 7.0	12.5 9.5	1.0 1.0	15.0 12.0	1.0 1.0	14.0 10.5	ns	3-7
t_{PLZ}	Output Disable Time ('AC541)	3.3 5.0	1.0 1.0	6.5 5.5	9.5 7.5	1.0 1.0	11.0 9.0	1.0 1.0	10.5 8.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Data to Output ('ACT540)	5.0		6.0						ns	3-5
t_{PHL}	Propagation Delay Data to Output ('ACT540)	5.0		5.5						ns	3-5
t_{PZH}	Output Enable Time ('ACT540)	5.0		8.0						ns	3-7
t_{PZL}	Output Enable Time ('ACT540)	5.0		6.5						ns	3-8
t_{PHZ}	Output Disable Time ('ACT540)	5.0		10.0						ns	3-7
t_{PLZ}	Output Disable Time ('ACT540)	5.0		7.0						ns	3-8
t_{PLH}	Propagation Delay Data to Output ('ACT541)	5.0		6.0						ns	3-5
t_{PHL}	Propagation Delay Data to Output ('ACT541)	5.0		6.0						ns	3-5
t_{PZH}	Output Enable Time ('ACT541)	5.0		8.0						ns	3-7
t_{PZL}	Output Enable Time ('ACT541)	5.0		6.5						ns	3-8
t_{PHZ}	Output Disable Time ('ACT541)	5.0		10.0						ns	3-7
t_{PLZ}	Output Disable Time ('ACT541)	5.0		7.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	30.0	pF	$V_{CC} = 5.5$ V

54AC/74AC563 • 54ACT/74ACT563

Octal D-Type Latch With 3-State Outputs

Description

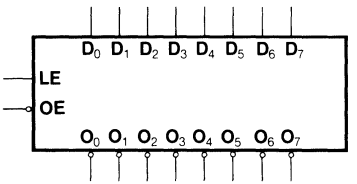
The 'AC/'ACT563 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

The 'AC/'ACT563 device is functionally identical to the 'AC/'ACT573, but with inverted outputs.

- **Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors**
- **Useful as Input or Output Port for Microprocessors**
- **Functionally Identical to 'AC/'ACT573 but with Inverted Outputs**
- **Outputs Source/Sink 24 mA**
- **'ACT563 has TTL-Compatible Inputs**

Ordering Code: See Section 6

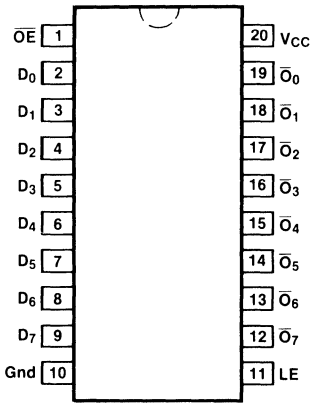
Logic Symbol



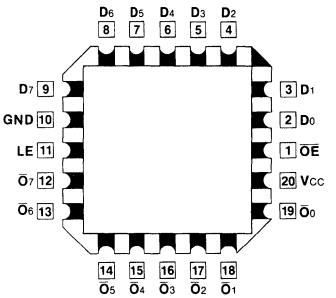
Pin Names

D_0 - D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	3-State Output Enable Input
$\overline{O}_0$ - $\overline{O}_7$	3-State Latch Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

5

Functional Description

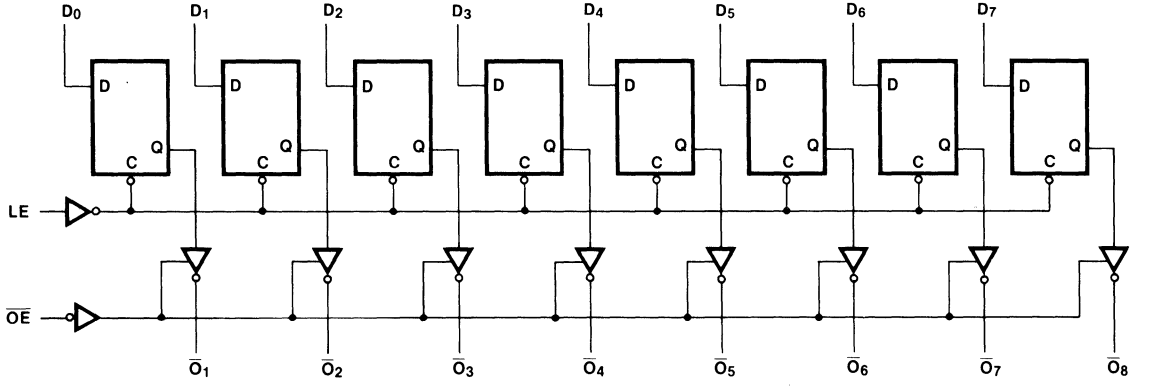
The 'AC/'ACT563 contains eight D-type latches with 3-state complementary outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but that does not interfere with entering new data into the latches.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	LE	D	Q	O	
H	X	X	X	Z	High Z
H	H	L	H	Z	High Z
H	H	H	L	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT563)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to $\overline{O}_n$	3.3 5.0		7.5 5.0						ns	3-5
t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	3.3 5.0		7.0 4.5						ns	3-5
t_{PLH}	Propagation Delay LE to $\overline{O}_n$	3.3 5.0		7.5 5.0						ns	3-6
t_{PHL}	Propagation Delay LE to $\overline{O}_n$	3.3 5.0		8.0 5.5						ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		6.0 4.0						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		6.0 4.0						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 5.0						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		5.0 3.5						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW, D_n to LE	3.3 5.0	2.0 1.5				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	−2.5 −1.5				ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	3.0 2.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to $\overline{O}_n$	5.0	1.0	7.0	11.5	1.0	14.0	1.0	12.5	ns	3-5
t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	5.0	1.0	6.0	10.0	1.0	12.0	1.0	11.0	ns	3-5
t_{PLH}	Propagation Delay LE to $\overline{O}_n$	5.0	1.0	6.5	10.5	1.0	12.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay LE to $\overline{O}_n$	5.0	1.0	5.5	9.5	1.0	11.5	1.0	10.5	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	5.5	9.0	1.0	11.0	1.0	10.0	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	5.5	8.5	1.0	10.5	1.0	9.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	6.5	10.5	1.0	12.5	1.0	11.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	4.5	8.0	1.0	9.5	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT	Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW, D_n to LE	5.0	1.5	4.0	5.0	4.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−2.0	0	0	0	ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.0	3.0	5.0	3.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.5$ V

54AC/74AC564 • 54ACT/74ACT564

Octal D-Type Latch With 3-State Outputs

Description

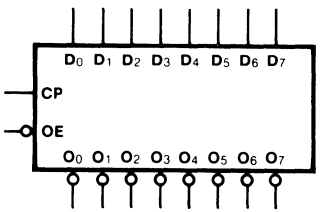
The 'AC/'ACT564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'AC/'ACT564 device is functionally identical to the 'AC/'ACT574, but with inverted outputs.

- **Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors**
- **Useful as Input or Output Port for Microprocessors**
- **Functionally Identical to 'AC/'ACT574 but with Inverted Outputs**
- **3-State Outputs for Bus-Oriented Applications**
- **Outputs Source/Sink 24 mA**
- **'ACT564 has TTL-Compatible Inputs**

Ordering Code: See Section 6

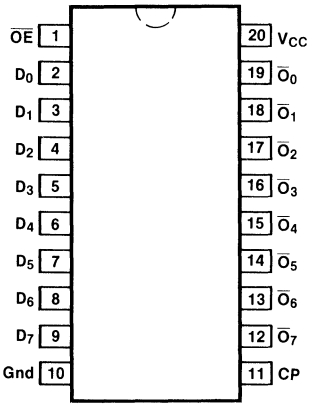
Logic Symbol



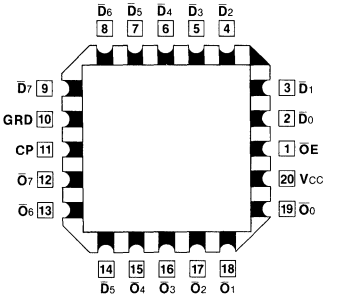
Pin Names

D_0 - D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-State Output Enable Input
$\overline{O}_0$ - $\overline{O}_7$	3-State Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

The 'AC/'ACT564 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

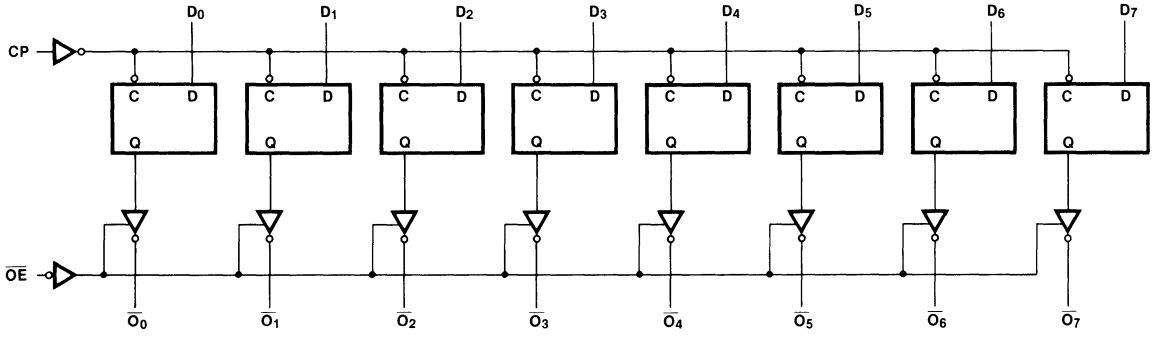
Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	⌐	L	H	Z	Load
H	⌐	H	L	Z	Load
L	⌐	L	H	H	Data Available
L	⌐	H	L	L	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT564)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		110 150						MHz	3-3
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0		10.5 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0		9.5 6.0						ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		8.5 6.5						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		8.0 5.5						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		9.5 7.0						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		7.5 5.5						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF Typ	54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF Guaranteed Minimum	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF Guaranteed Minimum	Units	Fig. No.
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 −0.5			ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	3.5 2.5			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	85	90		65		75		MHz	3-3
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	5.0	1.0	6.5	10.5	1.0	12.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{O}_n$	5.0	1.0	6.0	9.5	1.0	11.5	1.0	10.5	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	5.5	9.0	1.0	10.5	1.0	9.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	5.5	8.5	1.0	10.5	1.0	9.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	10.5	1.0	12.5	1.0	11.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	5.0	8.0	1.0	9.0	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT	Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = −55°C to +125°C CL = 50 pF	TA = −40°C to +85°C CL = 50 pF		
			Typ	Guaranteed Minimum				
ts	Setup Time, HIGH or LOW Dn to CP	5.0	1.0	2.5	3.0	3.0	ns	3-9
th	Hold Time, HIGH or LOW Dn to CP	5.0	−0.5	1.0	1.0	1.0	ns	3-9
tw	LE Pulse Width, HIGH or LOW	5.0	2.5	3.0	5.0	3.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
CIN	Input Capacitance	4.5	pF	VCC = 5.5 V
CPD	Power Dissipation Capacitance	50.0	pF	VCC = 5.5 V

54AC/74AC568 • 54AC/74AC569

4-Bit Bidirectional Counters With 3-State Outputs

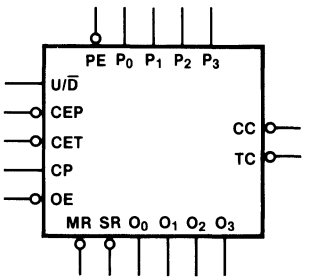
Description

The 'AC568 and 'AC569 are fully synchronous, bidirectional counters with 3-state outputs. The 'AC568 is a BCD decade counter; the 'AC569 is a modulo 16 binary counter. They feature preset capability for programmable operation, carry lookahead for easy cascading, and a U/$\overline{D}$ input to control the direction of counting. For maximum flexibility there are both synchronous and master asynchronous reset inputs as well as both Clocked Carry ($\overline{CC}$) and Terminal Count ($\overline{TC}$) outputs. All state changes except Master Reset are initiated by the rising edge of the clock. A HIGH signal on the Output Enable ($\overline{OE}$) input forces the output buffers into the high-impedance state but does not prevent counting, resetting or parallel loading.

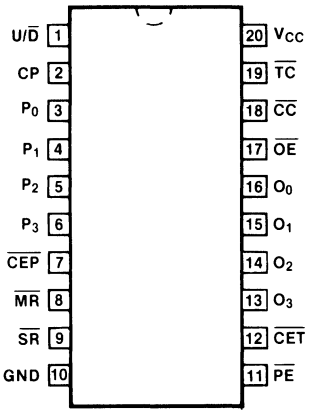
- **Synchronous Counting and Loading**
- **Lookahead Carry Capability for Easy Cascading**
- **Preset Capability for Programmable Operation**
- **3-State Outputs for Bus Organized Systems**
- **Outputs Source/Sink 24 mA**
- **Synchronous and Asynchronous Resets**

Ordering Code: See Section 6

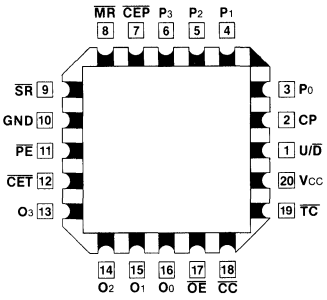
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



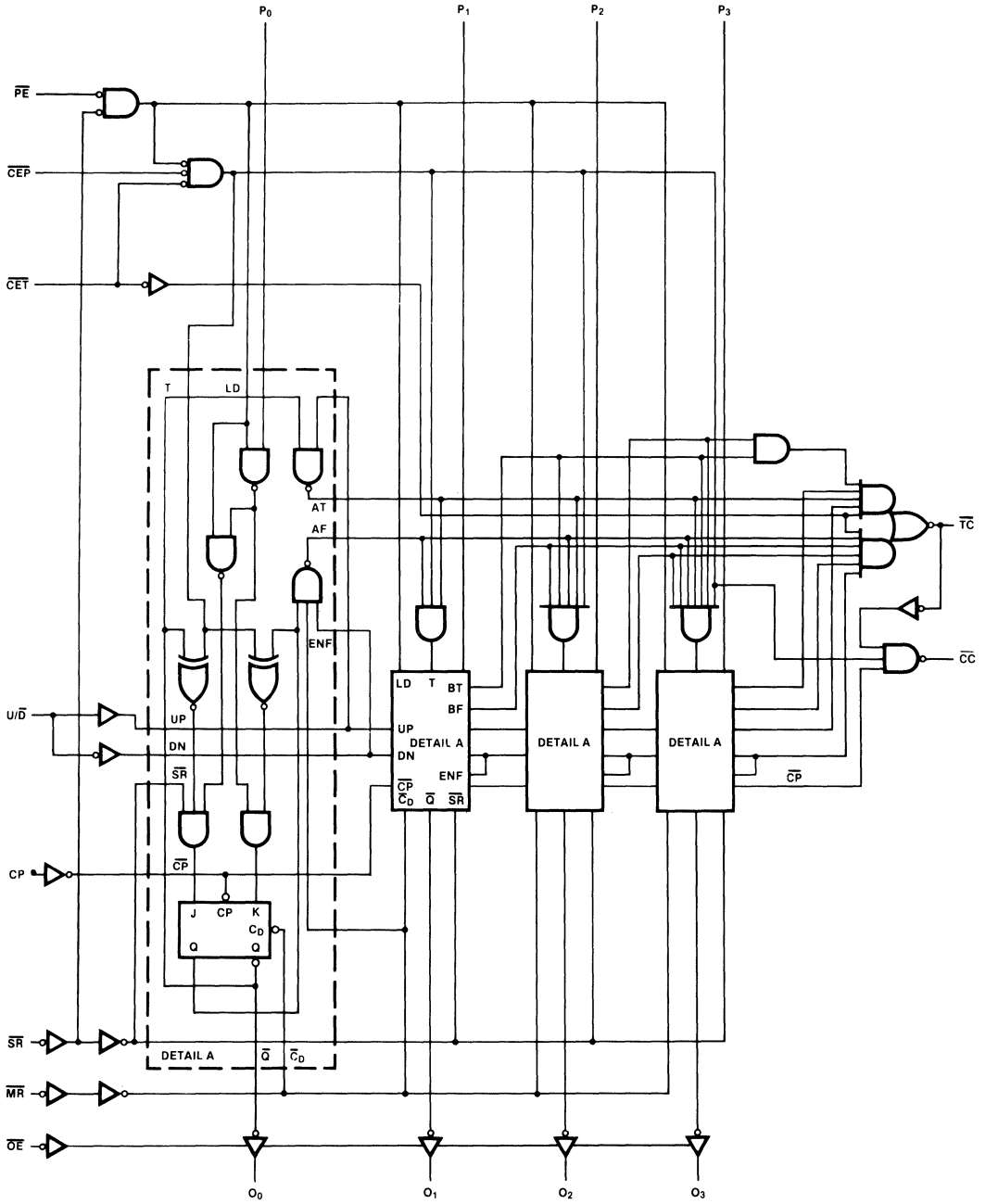
Pin Assignment for LCC and PCC

Pin Names

P0 - P3	Parallel Data Inputs
$\overline{CEP}$	Count Enable Parallel Input
$\overline{CET}$	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{PE}$	Parallel Enable Input
U/$\overline{D}$	Up/Down Count Control Input
$\overline{OE}$	Output Enable Input
$\overline{MR}$	Master Reset Input
$\overline{SR}$	Synchronous Reset Input
O0 - O3	3-State Parallel Data Outputs
$\overline{TC}$	Terminal Count Output
$\overline{CC}$	Clocked Carry Output

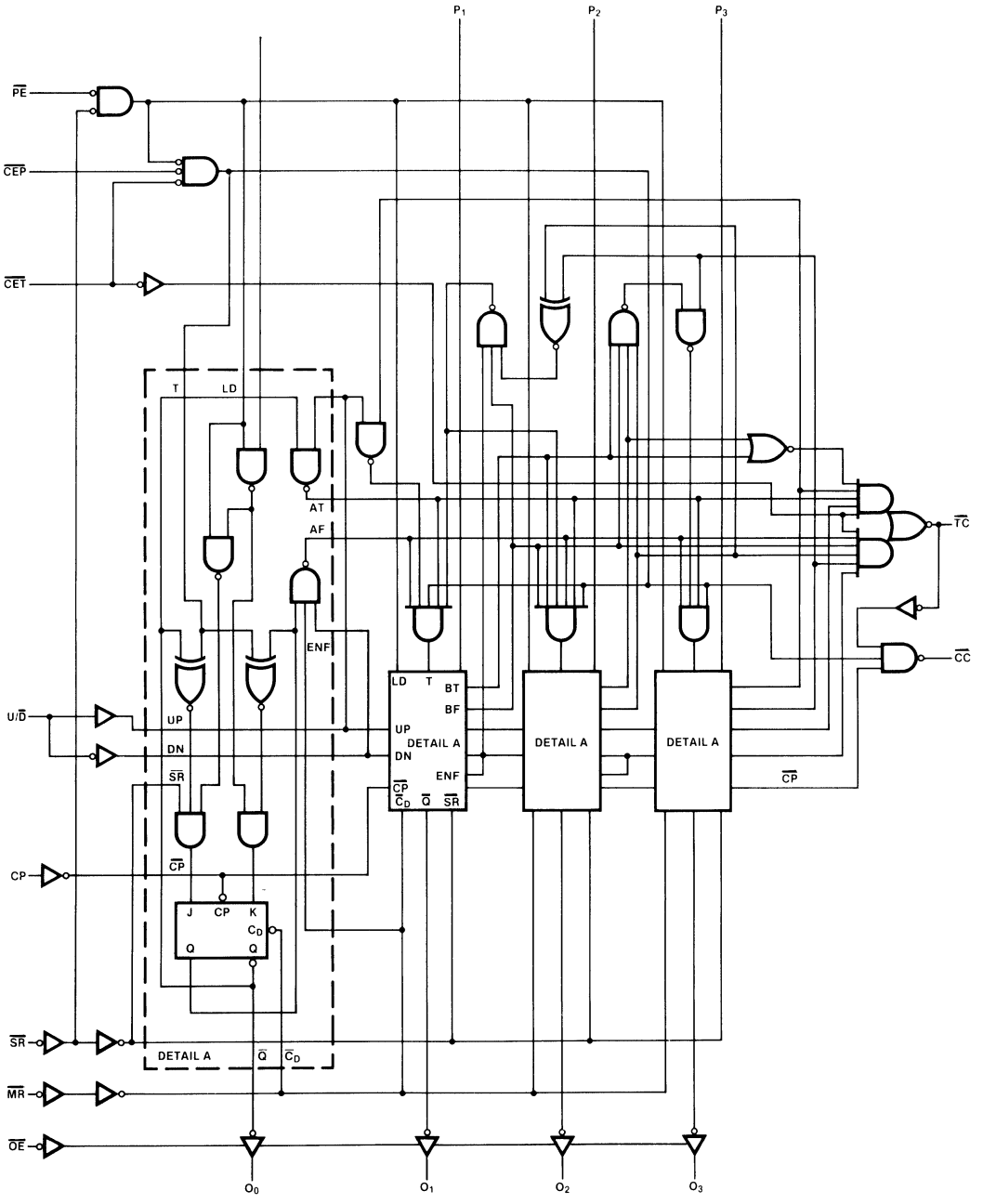
5

Logic Diagram (²AC568)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

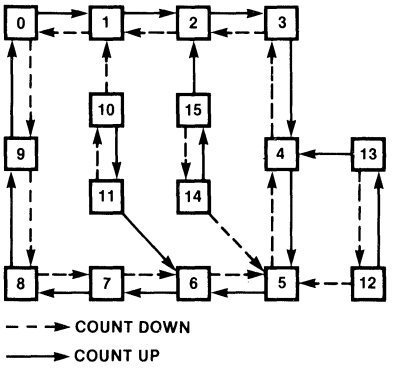
Logic Diagram ('AC569)



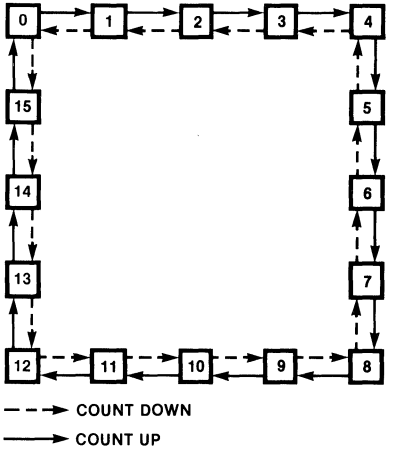
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

State Diagrams

'AC568



'AC569



Logic Equations:

Count Enable = $\overline{CEP} \bullet \overline{CET} \bullet PE$

Up ('AC568): $\overline{TC} = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3 \bullet (Up) \bullet \overline{CET}$

('AC569): $\overline{TC} = Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3 \bullet (Up) \bullet \overline{CET}$

Down (Both): $\overline{TC} = \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3 \bullet (Down) \bullet \overline{CET}$

Functional Description

The 'AC568 counts modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) it will increment to 0 (LLLL) in the Up mode; in Down mode it will decrement from 0 to 9. The 'AC569 counts in the modulo-16 binary sequence. From state 15 it will increment to state 0 in the Up mode; in the Down mode it will decrement from 0 to 15. The clock inputs of all flip-flops are driven in parallel through a clock buffer. All state changes (except due to Master Reset) occur synchronously with the LOW-to-HIGH transition of the Clock Pulse (CP) input signal.

The circuits have five fundamental modes of operation, in order of precedence: asynchronous reset, synchronous reset, parallel load, count and hold. Five control inputs—Master Reset ($\overline{MR}$), Synchronous Reset ($\overline{SR}$), Parallel Enable ($\overline{PE}$), Count Enable Parallel ($\overline{CEP}$) and Count Enable Trickle ($\overline{CET}$)—plus the Up/Down (U/$\overline{D}$) input determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces the flip-flop Q outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows the Q outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (Pn) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{MR}$, $\overline{SR}$ and $\overline{PE}$ HIGH, $\overline{CEP}$ and $\overline{CET}$ permit counting when both are LOW. Conversely, a HIGH signal on either $\overline{CEP}$ or $\overline{CET}$ inhibits counting.

The 'AC568 and 'AC569 use edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, $\overline{CEP}$, $\overline{CET}$ or U/$\overline{D}$ inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

Two types of outputs are provided as overflow/underflow indicators. The Terminal Count ($\overline{TC}$) output is normally HIGH and goes LOW providing $\overline{CET}$ is LOW, when the counter reaches zero in the Down mode, or reaches maximum (9 for the 'AC568, 15 for the 'AC569) in the Up mode. $\overline{TC}$ will then remain LOW until a state change occurs, whether by counting or presetting, or until U/$\overline{D}$ or $\overline{CET}$ is changed. To implement synchronous multistage counters, the connections between the $\overline{TC}$ output and the $\overline{CEP}$ and $\overline{CET}$ inputs can provide either slow or fast carry propagation. Figure a shows the connections for simple ripple carry, in which the clock period must be longer than the CP to $\overline{TC}$ delay of the first stage, plus the cumulative

$\overline{CET}$ to $\overline{TC}$ delays of the intermediate stages, plus the $\overline{CET}$ to CP setup time of the last stage. This total delay plus setup time sets the upper limit on clock frequency. For faster clock rates, the carry lookahead connections shown in Figure b are recommended. In this scheme the ripple delay through the intermediate stages commences with the same clock that causes the first stage to tick over from max to min in the Up mode, or min to max in the Down mode, to start its final cycle. Since this final cycle takes 10 ('AC568) or 16 ('AC569) clocks to complete, there is plenty of time for the ripple to progress through the intermediate stages. The critical timing that limits the clock period is the CP to $\overline{TC}$ delay of the first stage plus the $\overline{CEP}$ to CP setup time of the last stage. The $\overline{TC}$ output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, registers or counters. For such applications, the Clocked Carry ($\overline{CC}$) output is provided. The $\overline{CC}$ output is normally HIGH. When $\overline{SR}$ and $\overline{PE}$ are HIGH, and $\overline{CEP}$, $\overline{CET}$ and $\overline{TC}$ are LOW, the $\overline{CC}$ output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again, as shown in the $\overline{CC}$ Truth Table. When the Output Enable ($\overline{OE}$) is LOW, the parallel data outputs O_0 - O_3 are active and follow the flip-flop Q outputs. A HIGH signal on $\overline{OE}$ forces O_0 - O_3 to the high-Z state but does not prevent counting, loading or resetting.

Mode Select Table

Inputs						Operating Mode
$\overline{MR}$	$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	
L	X	X	X	X	X	Asynchronous Reset
H	L	X	X	X	X	Synchronous Reset
H	H	L	X	X	X	Parallel Load
H	H	H	H	X	X	Hold
H	H	H	X	H	X	Hold
H	H	H	L	L	H	Count Up
H	H	H	L	L	L	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

$\overline{CC}$ Truth Table

Inputs						Output
$\overline{SR}$	$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	$\overline{TC}$*	CP	$\overline{CC}$
L	X	X	X	X	X	H
X	L	X	X	X	X	H
X	X	H	X	X	X	H
X	X	X	H	X	X	H
X	X	X	X	H	X	H
H	H	L	L	L	⊓	⊓

* = $\overline{TC}$ is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

5

Figure a: Multistage Counter with Ripple Carry

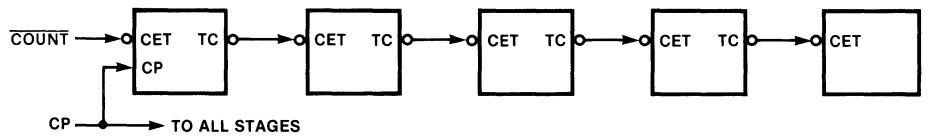
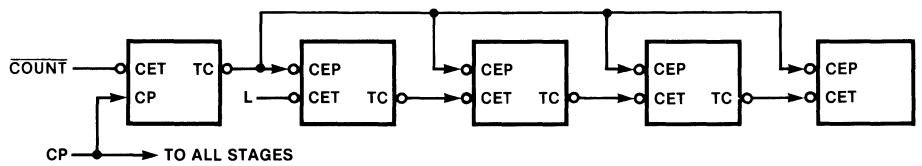


Figure b: Multistage Counter with Lookahead Carry



DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		87 117						MHz	3-3
t_{PLH}	Propagation Delay CP to O_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0		10.0 7.5						ns	3-6
t_{PHL}	Propagation Delay CP to O_n ($\overline{PE}$ HIGH or LOW)	3.3 5.0		11.0 8.0						ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{TC}$	3.3 5.0		16.5 12.0						ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{TC}$	3.3 5.0		16.5 12.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0		10.5 7.5						ns	3-6
t_{PHL}	Propagation Delay $\overline{CET}$ to $\overline{TC}$	3.3 5.0		10.0 7.0						ns	3-6
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('568)	3.3 5.0		10.5 7.5						ns	3-6
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('568)	3.3 5.0		9.0 6.5						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics (cont'd)

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('569)	3.3 5.0		10.5 7.5						ns	3-6
t_{PHL}	Propagation Delay U/$\overline{D}$ to $\overline{TC}$ ('569)	3.3 5.0		9.0 6.5						ns	3-6
t_{PLH}	Propagation Delay CP to $\overline{CC}$	3.3 5.0		11.0 8.0						ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{CC}$	3.3 5.0		9.5 7.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{CEP}$ or $\overline{CET}$ to $\overline{CC}$	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{CEP}$ or $\overline{CET}$ to $\overline{CC}$	3.3 5.0		9.5 7.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{MR}$ to O_n	3.3 5.0		12.5 9.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		7.5 5.5						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		7.5 5.5						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		9.5 7.0						ns	3-7
t_{PZL}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		11.0 8.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW P_n to CP	3.3 5.0	8.0 6.0				ns	3-9
t_h	Hold Time, HIGH or LOW P_n to CP	3.3 5.0	0 0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	3.3 5.0	8.0 12.5				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{CEP}$ or $\overline{CET}$ to CP	3.3 5.0	0 0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	12.5 9.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{PE}$ to CP	3.3 5.0	0 0				ns	3-9
t_s	Setup Time, HIGH or LOW U/$\overline{D}$ to CP ('568)	3.3 5.0	12.5 9.0				ns	3-9
t_s	Setup Time, HIGH or LOW U/$\overline{D}$ to CP ('569)	3.3 5.0	12.5 9.0				ns	3-9
t_h	Hold Time, HIGH or LOW U/$\overline{D}$ to CP	3.3 5.0	0 0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	4.0 3.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{SR}$ to CP	3.3 5.0	−1.5 −1.0				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements (cont'd)

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	4.0 3.0				ns	3-6
t_w	$\overline{MR}$ Pulse Width, LOW	3.3 5.0	4.0 3.0				ns	3-6
t_{rec}	$\overline{MR}$ Recovery Time	3.3 5.0	4.0 3.0				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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Capacitance

Symbol	Parameter	54/74AC Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC573 • 54ACT/74ACT573

Octal D-Type Latch With 3-State Outputs

Description

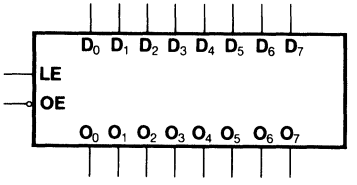
The 'AC/'ACT573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

The 'AC/'ACT573 is functionally identical to the 'AC/'ACT373 but has inputs and outputs on opposite sides.

- **Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors**
- **Useful as Input or Output Port for Microprocessors**
- **Functionally Identical to 'AC/'ACT373**
- **3-State Outputs for Bus Interfacing**
- **Outputs Source/Sink 24 mA**
- **'ACT573 has TTL-Compatible Inputs**

Ordering Code: See Section 6

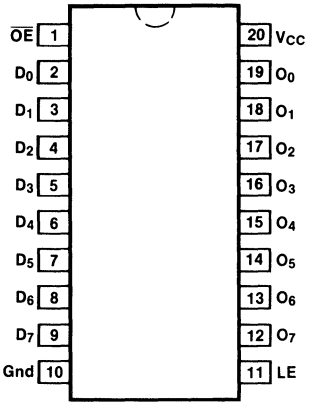
Logic Symbol



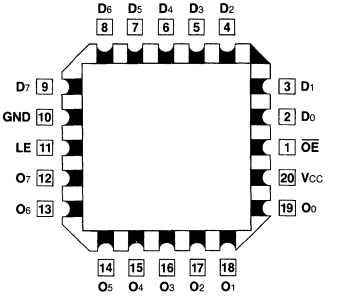
Pin Names

D_0 - D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	3-State Output Enable Input
O_0 - O_7	3-State Latch Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

The 'AC/'ACT573 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

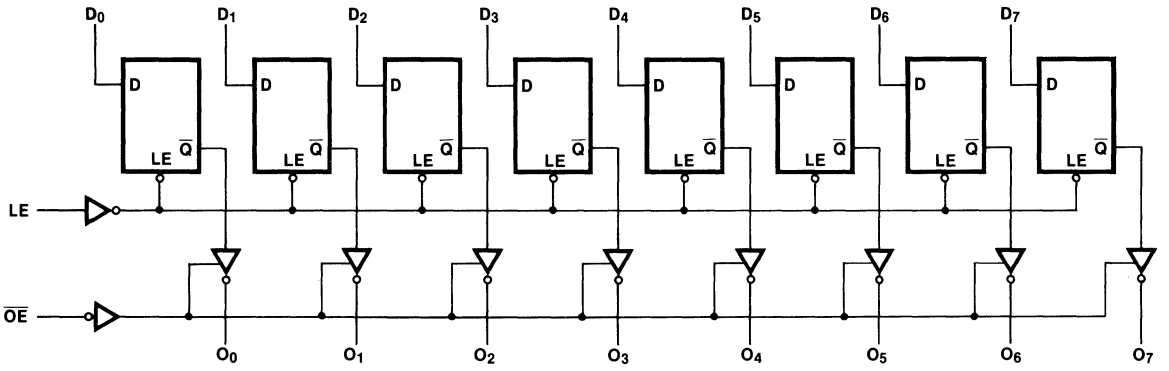
Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	H
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before LOW-to-HIGH Transition of Clock

5

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT573)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3 5.0		9.0 6.0						ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	3.3 5.0		9.0 6.0						ns	3-5
t_{PLH}	Propagation Delay LE to O_n	3.3 5.0		9.0 6.0						ns	3-6
t_{PHL}	Propagation Delay LE to O_n	3.3 5.0		8.0 5.5						ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		7.0 5.5						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		7.5 5.5						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		8.5 6.5						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		6.5 5.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	2.0 1.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	0 0				ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0	1.0	6.0	10.5	1.0	13.5	1.0	12.0	ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	5.0	1.0	6.0	10.5	1.0	13.5	1.0	12.0	ns	3-5
t_{PLH}	Propagation Delay LE to O_n	5.0	1.0	6.0	10.5	1.0	13.0	1.0	12.0	ns	3-6
t_{PHL}	Propagation Delay LE to O_n	5.0	1.0	5.5	9.5	1.0	12.0	1.0	10.5	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	5.5	10.0	1.0	11.5	1.0	11.0	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	5.5	9.5	1.0	11.0	1.0	10.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	6.5	11.0	1.0	13.5	1.0	12.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	5.0	8.5	1.0	10.5	1.0	9.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT	Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	1.5	3.0	3.5	3.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−1.5	0	0.5	0	ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.0	3.5	5.0	4.0	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	25.0	pF	$V_{CC} = 5.5$ V

54AC/74AC574 • 54ACT/74ACT574

Octal D-Type Flip-Flop With 3-State Outputs

Description

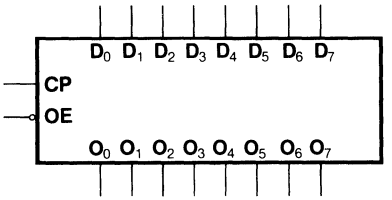
The 'AC/'ACT574 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'AC/'ACT574 is functionally identical to the 'AC/'ACT374 except for the pinouts.

- **Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors**
- **Useful as Input or Output Port for Microprocessors**
- **Functionally Identical to 'AC/'ACT374**
- **3-State Outputs for Bus-Oriented Applications**
- **Outputs Source/Sink 24 mA**
- **'ACT574 has TTL-Compatible Inputs**

Ordering Code: See Section 6

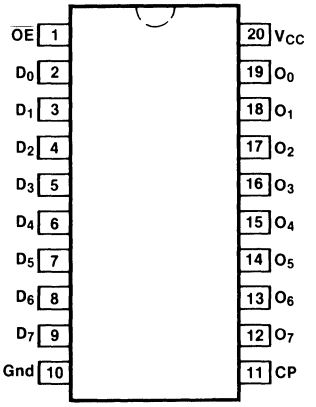
Logic Symbol



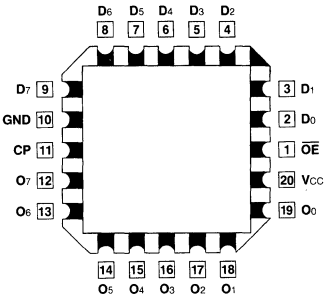
Pin Names

D_0 - D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-State Output Enable Input
O_0 - O_7	3-State Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

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Functional Description

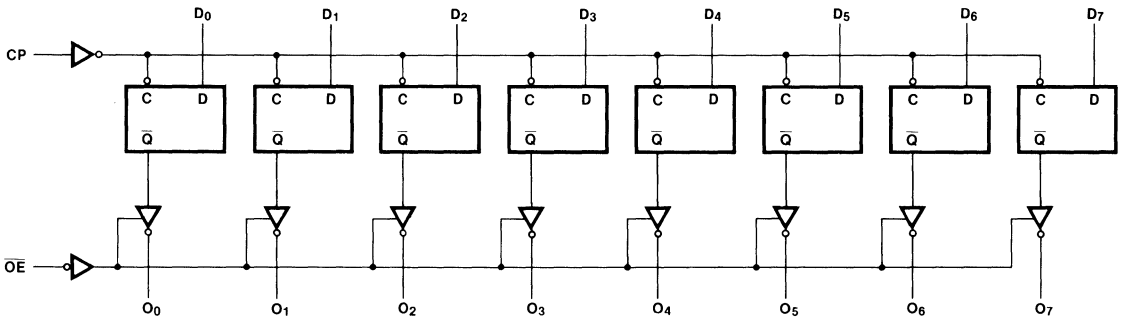
The 'AC/'ACT574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	On	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	⌐	L	L	Z	Load
H	⌐	H	H	Z	Load
L	⌐	L	L	L	Data Available
L	⌐	H	H	H	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Clock Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT574)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		110 160						MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0		10.0 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0		10.0 6.5						ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		6.5 5.0						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		6.0 4.0						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 5.0						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		5.0 3.5						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	0 0				ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	4.0 2.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	100	110		70		85		ns	3-3
t_{PLH}	Propagation Delay CP to O_n	5.0	1.0	7.0	11.0	1.0	13.0	1.0	12.0	ns	3-6
t_{PHL}	Propagation Delay CP to O_n	5.0	1.0	6.5	10.0	1.0	12.5	1.0	11.0	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	6.4	9.5	1.0	11.0	1.0	10.0	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	6.0	9.0	1.0	11.5	1.0	10.0	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	10.5	1.0	12.5	1.0	11.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	5.5	8.5	1.0	10.0	1.0	9.0	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT	Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW D_n to CP	5.0	1.5	2.5	3.0	2.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	1.0	1.0	1.0	ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	2.5	3.0	5.0	4.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

5

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	40.0	pF	$V_{CC} = 5.5$ V

54AC/74AC640 • 54ACT/74ACT640

Octal Bidirectional Transceiver With 3-State Outputs

Description

The 'AC/'ACT640 octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from bus A to bus B when T/$\overline{R}$ = HIGH, or from bus B to bus A when T/$\overline{R}$ = LOW. The enable input can be used to disable the device so the buses are effectively isolated.

- **Bidirectional Data Path**
- **A and B Outputs Sink 24 mA/Source -24 mA**
- **'ACT640 has TTL-Compatible Inputs**

Ordering Code: See Section 6

Pin Names

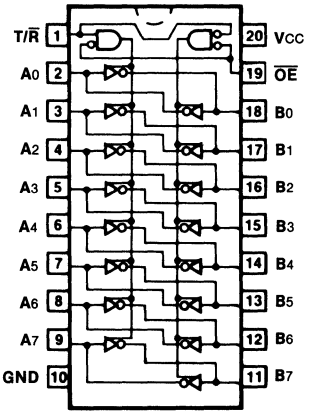
A_0 - A_7	Side A Inputs or 3-State Outputs
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
B_0 - B_7	Side B Inputs or 3-State Outputs

Truth Table

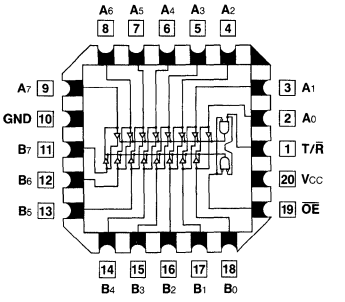
$\overline{OE}$	T/$\overline{R}$	Applied Inputs	Valid Direction I/P→O/P	Output
H	X	X	X	X
L	H	H	A to B	L
L	H	L	A to B	H
L	L	H	B to A	L
L	L	L	B to A	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT640)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	3.3 5.0		5.5 4.0						ns	3-5
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	3.3 5.0		5.5 4.0						ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0		8.0 6.0						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		7.5 5.5						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 6.0						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		7.5 6.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	5.0		5.0						ns	3-5
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	5.0		5.0						ns	3-5
t_{PZH}	Output Enable Time	5.0		7.0						ns	3-7
t_{PZL}	Output Enable Time	5.0		6.0						ns	3-8
t_{PHZ}	Output Disable Time	5.0		6.5						ns	3-7
t_{PLZ}	Output Disable Time	5.0		6.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
$C_{I/O}$	Input/Output Capacitance	15.0	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC643 • 54ACT/74ACT643

Octal Bidirectional Transceiver With 3-State Outputs

Description

The 'AC/'ACT643 octal bus transceiver is designed for asynchronous two-way communication between data buses. The device transmits data from bus A to bus B when T/$\overline{R}$ = HIGH, or from bus B to bus A when T/$\overline{R}$ = LOW. The enable input can be used to disable the device so the buses are effectively isolated.

- **Noninverting Buffers**
- **Bidirectional Data Path**
- **A and B Outputs Sink 24 mA/Source -24 mA**
- **'ACT643 has TTL-Compatible Inputs**

Ordering Code: See Section 6

Pin Names

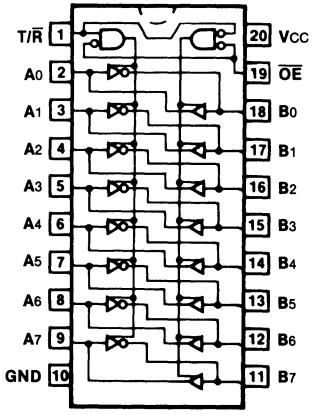
A_0 - A_7	Side A Inputs or 3-State Outputs
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
B_0 - B_7	Side B Inputs or 3-State Outputs

Truth Table

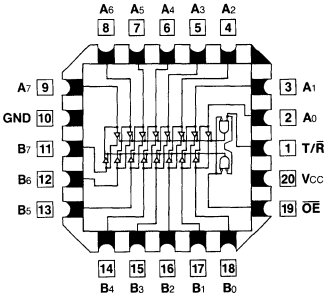
$\overline{OE}$	T/$\overline{R}$	Applied Inputs	Valid Direction I/P→O/P	Output
H	X	X	X	X
L	H	H	A to B	L
L	H	L	A to B	H
L	L	H	B to A	H
L	L	L	B to A	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

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DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional I_{CC}/Input ('ACT643)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	3.3 5.0		5.5 4.0						ns	3-5
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	3.3 5.0		5.5 4.0						ns	3-5
t_{PZH}	Output Enable Time	3.3 5.0		8.0 6.0						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		7.5 5.5						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		7.0 6.0						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		7.5 6.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to B_n or B_n to A_n	5.0		5.0						ns	3-5
t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	5.0		5.0						ns	3-5
t_{PZH}	Output Enable Time	5.0		7.0						ns	3-7
t_{PZL}	Output Enable Time	5.0		6.0						ns	3-8
t_{PHZ}	Output Disable Time	5.0		6.5						ns	3-7
t_{PLZ}	Output Disable Time	5.0		6.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
$C_{I/O}$	Input/Output Capacitance	15.0	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC646

Octal Transceiver/Register With 3-State Outputs

Description

The 'AC646 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CAB or CBA). The four fundamental data handling functions available are illustrated in the following figures.

Real Time Transfer A-Bus to B-Bus

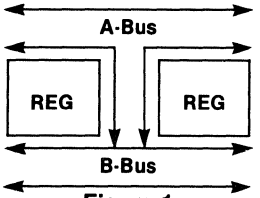


Figure 1

Real Time Transfer B-Bus to A-Bus

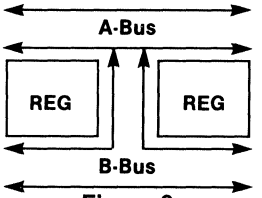


Figure 2

Storage from Bus to Register

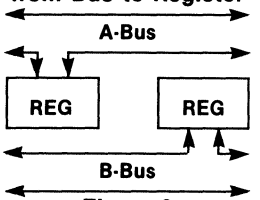


Figure 3

Transfer from Register to Bus

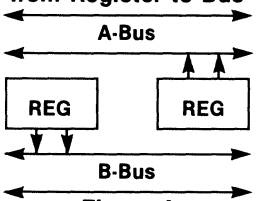
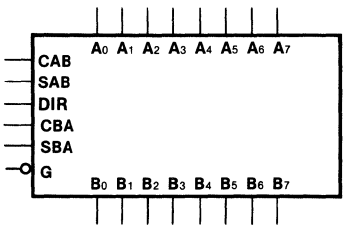


Figure 4

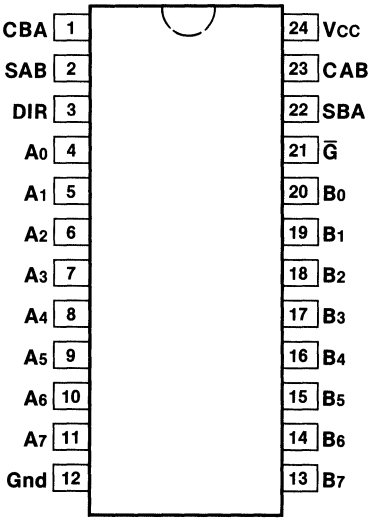
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data Transfers**
- **Choice of True and Inverting Data Paths**
- **3-State Outputs**
- **300 mil Slim Dual In-Line Package**
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 6

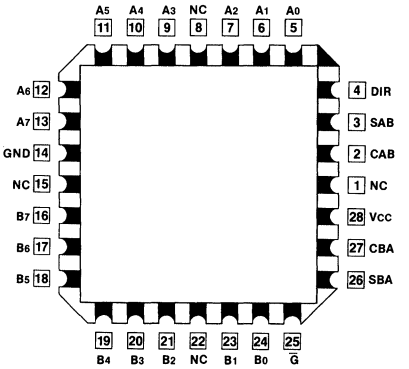
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Pin Names

A_0 - A_7	Data Register Inputs
	Data Register A Outputs
B_0 - B_7	Data Register B Inputs
	Data Register B Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\overline{G}$	Output Enable Inputs

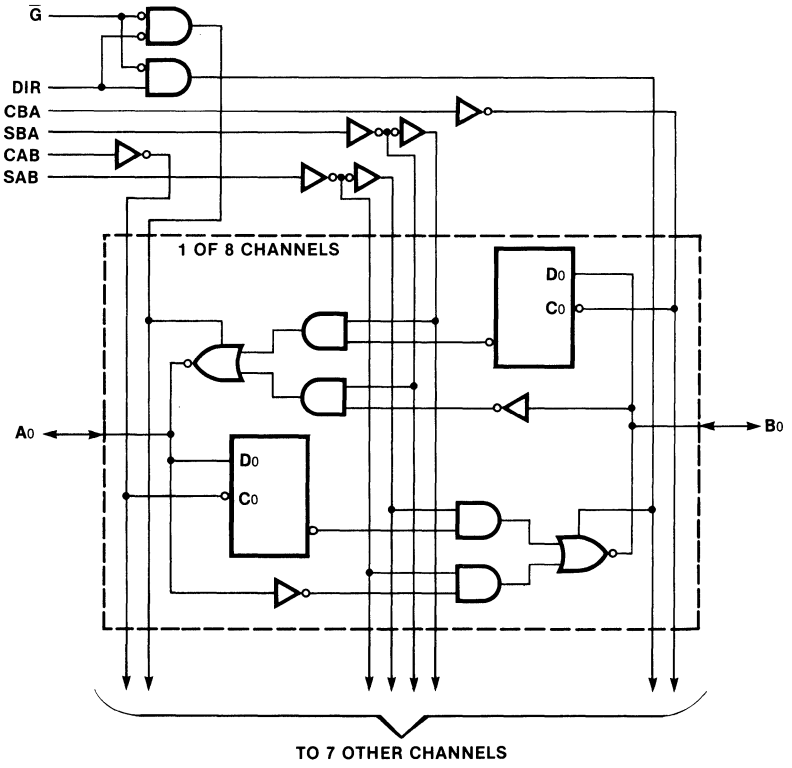
Function Table

Inputs						Data I/O*		Operation or Function
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A_0 - A_7	B_0 - B_7	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	⌐	⌐	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the appropriate clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0	10.5 7.5	16.5 12.0	1.0 1.0	21.0 14.5	1.0 1.0	18.5 13.0	ns	3-6
t_{PHL}	Propagation Delay Clock to Bus	3.3 5.0	1.0 1.0	9.5 6.5	14.5 10.5	1.0 1.0	18.0 12.5	1.0 1.0	16.0 11.5	ns	3-6
t_{PLH}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0	7.5 5.0	12.0 8.0	1.0 1.0	15.0 10.0	1.0 1.0	13.5 9.0	ns	3-5
t_{PHL}	Propagation Delay Bus to Bus	3.3 5.0	1.0 1.0	7.5 5.0	12.5 9.0	1.0 1.0	15.5 11.0	1.0 1.0	13.5 9.5	ns	3-5
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (w/ A_n or B_n HIGH or LOW)	3.3 5.0	1.0 1.0	8.5 6.0	13.5 10.0	1.0 1.0	17.0 12.0	1.0 1.0	15.5 11.0	ns	3-6
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (w/ A_n or B_n HIGH or LOW)	3.3 5.0	1.0 1.0	8.5 6.0	13.5 10.0	1.0 1.0	17.0 12.0	1.0 1.0	15.0 11.0	ns	3-6
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	7.0 5.0	11.5 8.5	1.0 1.0	14.0 10.0	1.0 1.0	12.5 9.0	ns	3-7
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	7.5 5.5	12.5 9.0	1.0 1.0	15.5 11.0	1.0 1.0	14.0 10.0	ns	3-8
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	8.0 6.5	12.5 10.0	1.0 1.0	14.5 12.0	1.0 1.0	13.5 11.0	ns	3-7
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3 5.0	1.0 1.0	7.5 6.0	12.0 9.5	1.0 1.0	15.0 11.5	1.0 1.0	13.5 10.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table 1 data sheet from your Fairchild sales engineer or account representative.

AC Characteristics, cont'd

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PZH}	Enable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	6.5 5.0	11.0 7.5	1.0 1.0	13.5 9.5	1.0 1.0	12.0 8.5	ns	3-7
t_{PZL}	Enable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	7.0 5.0	11.5 8.0	1.0 1.0	14.5 10.0	1.0 1.0	13.0 9.0	ns	3-8
t_{PHZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	7.5 5.5	11.5 9.5	1.0 1.0	13.5 10.5	1.0 1.0	12.5 10.0	ns	3-7
t_{PLZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	7.5 5.5	12.0 9.5	1.0 1.0	15.0 10.5	1.0 1.0	13.5 10.5	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Set-up Time, HIGH or LOW Bus to Clock	3.3 5.0	2.0 1.5	5.0 4.0	6.0 4.5	5.5 4.5	ns	3-9
t_h	Hold time, HIGH or LOW Bus to Clock	3.3 5.0	−1.5 −0.5	0 0.5	0.5 1.0	0 1.0	ns	3-9
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0	2.0 2.0	3.5 3.5	5.0 5.0	4.5 3.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table 1 data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
$C_{I/O}$	Input/Output Capacitance	15.0	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	60.0	pF	$V_{CC} = 5.5$ V

54AC/74AC648

Octal Transceiver/Register With 3-State Outputs

Description

The 'AC648 consists of registered bus transceiver circuits, with outputs, D-type flip-flops and control circuitry providing multiplexed transmission of data directly from the input bus or from the internal storage registers. Data on the A or B bus will be loaded into the respective registers on the LOW-to-HIGH transition of the appropriate clock pin (CAB or CBA). The four fundamental data handling functions available are illustrated in the following figures.

Real Time Transfer A-Bus to B-Bus

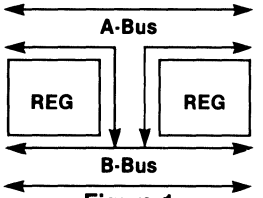


Figure 1

Real Time Transfer B-Bus to A-Bus

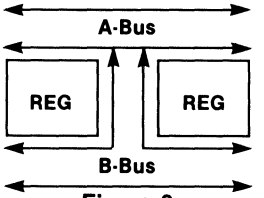


Figure 2

Storage from Bus to Register

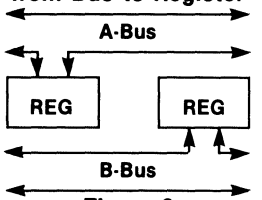


Figure 3

Transfer from Register to Bus

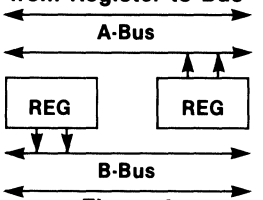
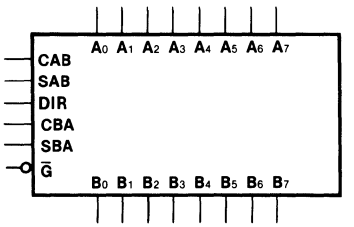


Figure 4

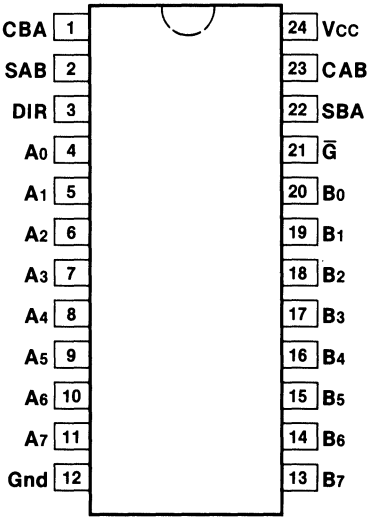
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data Transfers**
- **Choice of True and Inverting Data Paths**
- **3-State Outputs**
- **300 mil Slim Dual In-Line Package**
- **Outputs Source/Sink 24 mA**

Ordering Code: See Section 6

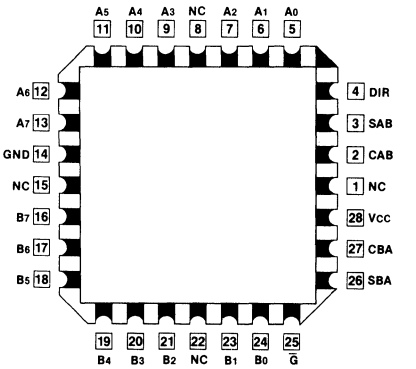
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Pin Names

A_0 - A_7	Data Register Inputs
	Data Register A Outputs
B_0 - B_7	Data Register B Inputs
	Data Register B Outputs
CAB, CBA	Clock Pulse Inputs
SAB, SBA	Transmit/Receive Inputs
DIR, $\overline{G}$	Output Enable Inputs

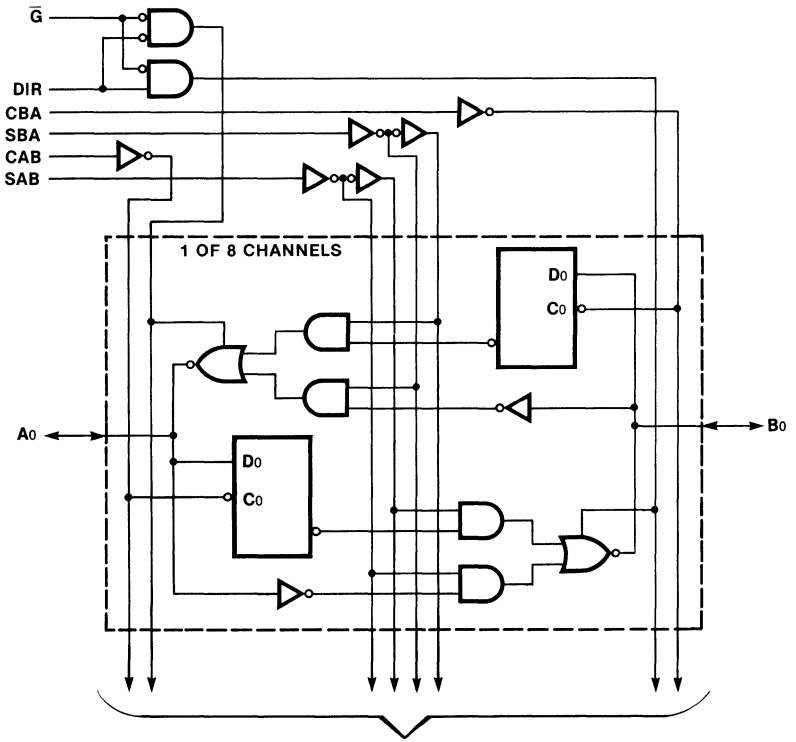
Function Table

Inputs						Data I/O*		Operation or Function
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	$A_0 - A_7$	$B_0 - B_7$	
H	X	H or L	H or L	X	X	Input	Input	Isolation
H	X	⌐	⌐	X	X			Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus

*The data output functions may be enabled or disabled by various signals at the G and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock inputs.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC	74AC	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$

AC Characteristics

Symbol	Parameter	V_{CC}* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay Clock to Bus	3.3	1.0	10.0	15.5	1.0	18.5	1.0	17.0	ns	3-6
		5.0	1.0	7.0	11.0	1.0	13.0	1.0	12.0		
t_{PHL}	Propagation Delay Clock to Bus	3.3	1.0	8.5	13.5	1.0	16.5	1.0	14.5	ns	3-6
		5.0	1.0	6.0	10.5	1.0	13.0	1.0	11.5		
t_{PLH}	Propagation Delay Bus to Bus	3.3	1.0	6.0	10.0	1.0	12.0	1.0	11.0	ns	3-5
		5.0	1.0	4.0	7.0	1.0	8.5	1.0	7.5		
t_{PHL}	Propagation Delay Bus to Bus	3.3	1.0	5.5	9.0	1.0	11.0	1.0	10.0	ns	3-5
		5.0	1.0	3.5	7.5	1.0	9.0	1.0	8.0		
t_{PLH}	Propagation Delay SBA or SAB to A_n or B_n (with A_n or B_n HIGH or LOW)	3.3	1.0	7.5	12.5	1.0	15.0	1.0	14.0	ns	3-6
		5.0	1.0	5.5	9.0	1.0	11.0	1.0	10.0		
t_{PHL}	Propagation Delay SBA or SAB to A_n or B_n (with A_n or B_n HIGH or LOW)	3.3	1.0	7.5	12.5	1.0	15.5	1.0	14.0	ns	3-6
		5.0	1.0	5.5	9.5	1.0	11.5	1.0	10.5		
t_{PZH}	Enable Time $\overline{G}$ to A_n or B_n	3.3	1.0	6.5	11.0	1.0	12.5	1.0	11.5	ns	3-7
		5.0	1.0	5.0	8.0	1.0	9.5	1.0	9.0		
t_{PZL}	Enable Time $\overline{G}$ to A_n or B_n	3.3	1.0	7.0	11.0	1.0	13.5	1.0	12.5	ns	3-8
		5.0	1.0	5.0	8.0	1.0	9.5	1.0	9.0		
t_{PHZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3	1.0	7.5	12.0	1.0	13.5	1.0	13.0	ns	3-7
		5.0	1.0	6.0	10.0	1.0	12.0	1.0	11.0		
t_{PLZ}	Disable Time $\overline{G}$ to A_n or B_n	3.3	1.0	7.0	11.5	1.0	13.5	1.0	12.5	ns	3-8
		5.0	1.0	5.5	9.0	1.0	10.5	1.0	10.0		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics, cont'd

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PZH}	Enable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	6.0 4.5	12.5 9.5	1.0 1.0	15.5 11.5	1.0 1.0	14.0 10.5	ns	3-7
t_{PZL}	Enable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	6.5 4.5	13.0 9.0	1.0 1.0	15.0 10.0	1.0 1.0	14.5 10.5	ns	3-8
t_{PHZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	7.0 5.5	11.5 9.0	1.0 1.0	15.0 10.5	1.0 1.0	13.5 10.0	ns	3-7
t_{PLZ}	Disable Time DIR to A_n or B_n	3.3 5.0	1.0 1.0	7.0 5.0	13.5 9.5	1.0 1.0	15.5 11.5	1.0 1.0	15.0 10.0	ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW, Bus to Clock	3.3 5.0	2.0 1.5	3.0 2.0	4.0 2.5	3.5 2.0	ns	3-9
t_n	Hold Time, HIGH or LOW, Bus to Clock	3.3 5.0	-1.5 -0.5	0 1.0	0 1.0	0 1.0	ns	3-9
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0	2.0 2.0	3.5 3.0	4.5 3.5	4.0 3.0	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	65.0	pF	$V_{CC} = 5.5$ V
$C_{I/O}$	Input/Output Capacitance	15.0	pF	$V_{CC} = 5.5$ V

54AC/74AC705 • 54ACT/74ACT705

Arithmetic Logic Unit for Digital Signal Processing Applications

Description

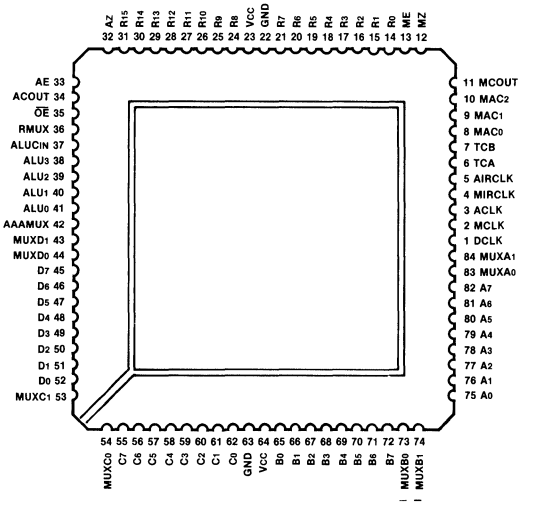
The 'AC/'ACT705 is a high-speed arithmetic processing integrated circuit which is packaged in an 84-pin leadless chip carrier. It features separate input busses that provide data and instruction codes to a high-speed single-cycle 16-bit ALU and an 8-bit by 8-bit parallel multiplier/accumulator.

The ALU is a 16-bit parallel design which supports sixteen arithmetic and logic functions, as well as carry-in/out and borrow-in/out. The multiplier/accumulator, which offers a full 16-bit product, provides for unsigned, signed, mixed mode and imaginary number multiplication. Product accumulation with sum and difference arithmetic is available in each multiplier operating mode.

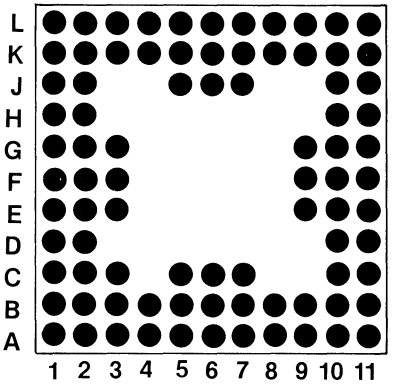
The 16-bit results of the ALU and multiplier/accumulator are multiplexed to a single set of 3-state output buffers. The two ALU and multiplier/accumulator carry-out bits, as well as the 4-bit status field indicating ALU and multiplier/accumulator error conditions make up the remaining six bits of the entire 22-bit output.

- **84-Pin PCC, CPGA**
- **Outputs Source/Sink 8 mA**
- **'ACT705 has TTL-Compatible Inputs**
- **High Throughput Achieved with High Degree of Parallelism in the Architecture**
- **Pipelined Stages**
- **High-Speed 16-Bit ALU and an 8 x 8 Complex Multiplier**
- **31.0 ns (Typical at 25°C, 5.0 V) Cycle 16-Bit Full ALU Performs Sixteen Boolean and Arithmetic Functions with Carry-In and Carry-Out**
- **50.0 ns (Typical at 25°C, 5.0 V) Cycle 8 x 8 Parallel Multiplier Supports Unsigned, Signed, Complex or Mixed Mode Multiplications, Produces 16-Bit Result with Carry-Out**
- **Separate Data and Instruction Busses Allow Instruction Fetches in Parallel with Execution — Single Cycle Operation**
- **Accepts 8- or 16-Bit Data and Delivers a 16-Bit Output**
- **Data Register Bank Configured to Accept a Combination of 8- or 16-Bit Data**

Connection Diagrams



Pin Assignment for PCC



Pin Assignment for CPGA

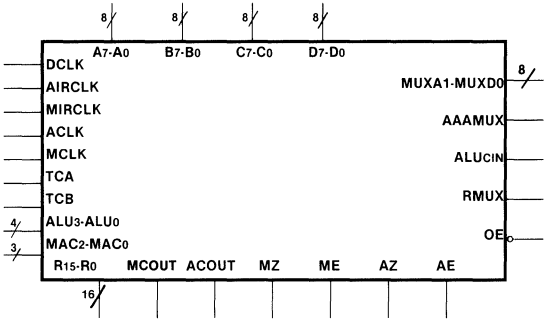
- **Separate Clocks for ALU Instruction, Multiplier Instruction, Data, ALU Accumulator and Multiplier Accumulator Registers**
- **Clustered Clock Pins for Ease of Board Design**
- **16-Bit ALU/Accumulator with Feedback to ALU Input**
- **Status of Accumulator Inputs is Monitored: Conditions Monitored Include Twos Complement Overflow, Underflow or Equal-to-Zero**

Applications

- **Voice-Band Signal Processing**
- **Discrete Fourier Transform Applications:**
  - **FIR Filters**
  - **IIR Filters**
- **Fast Fourier Transform Applications:**
  - **Spectrum Analysis**
  - **Speech Recognition**

Ordering Code: See Section 6

Logic Symbol

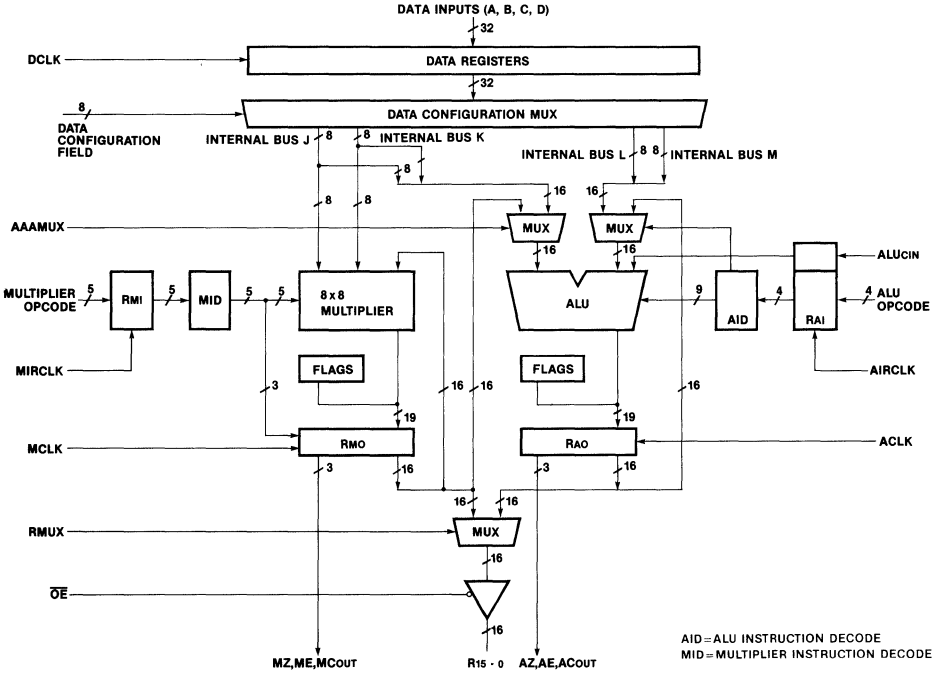


Pin Names

A_7 - A_0	Data Inputs
B_7 - B_0	Data Inputs
C_7 - C_0	Data Inputs
D_7 - D_0	Data Inputs
DCLK	Data Register Clock
AIRCLK	ALU Instruction Register Clock
MIRCLK	Multiplier Instruction Register Clock
ACLK	ALU Accumulator Register Clock
MCLK	Multiplier Accumulator Clock
TCA, TCB	Multiplier Opcode Input
ALU_3 - ALU_0	ALU Opcode Input
MAC_2 - MAC_0	Multiplier Opcode Input
$MUXA_1$ - $MUXD_0$	Data Configuration Field Inputs
AAAMUX	Multiplier Accumulator Path Enable Input
$ALUC_{IN}$	ALU Carry-In/Borrow-Out Input
RMUX	Multiplexing Input
$\overline{OE}$	Output Enable Input
R_{15} - R_0	Result Output
MCOUT, ACOUT	Carry-Out Outputs
MZ, ME, AZ, AE	Error Status Flag Outputs

5

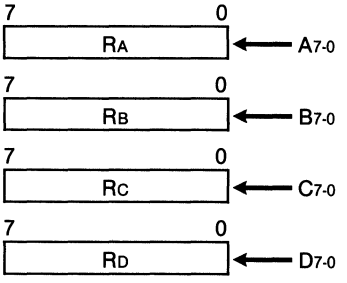
Block Diagram



Functional Description

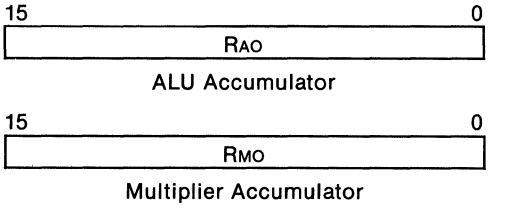
On-Chip Registers

1. Data



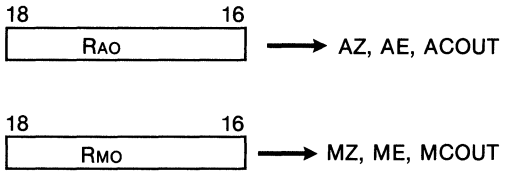
2. Instruction

3. Accumulator



Status

4. Flags and Carry-Out



Signal Descriptions

Data Inputs

ALUCIN, A_7 - A_0, B_7 - B_0, C_7 - C_0, D_7 - D_0: Data inputs.

Input Clocks

DCLK, AIRCLK, MIRCLK: Input data is loaded on the rising edge of these clocks.

Outputs

R_{15} - R_0: Result
MCOUT: Multiplier/Accumulator Carry-Out
ACOUT: ALU Carry-Out
MZ, ME, AZ, AE: Error Status Flags

Output Clocks

ACLK, MCLK: Output data is loaded into the output register on the rising edge of this clock.

Other Signals

ALU_3 - ALU_0: ALU Instruction Input
MAC_2 - MAC_0, TCA, TCB: Multiplier Instruction Input
$MUXA_0$, A_1, B_0, B_1, C_0, C_1, D_0, D_1: Multiplexer Select Signals for Input Data

Control Signals

Clock Signals

Dedicated signals for controlling the five sets of positive edge-triggered on-chip registers.

- DCLK: Data Registers (R_A, R_B, R_C, R_D)
- AIRCLK: ALU Instruction Register (R_{AI})
- MIRCLK: Multiplier Instruction Register (R_{MI})
- ACLK: ALU Accumulator Register (R_{AO})
- MCLK: Multiplier/Accumulator Register (R_{MO})

Control Signals, cont'd

ALUCIN
Clocked ALU Carry-In/Borrow-Out Signal.
1 → Carry-In to ALU
0 → Borrow from ALU

MUXA1, MUXA0 . . . MUXD0 (Data Configuration Field, see Table A)
Level signals for configuring the ALU and multiplier operands in 256 possible ways with the contents of RA, RB, RC, RD.
MUXA1, MUXA0: Control the state of internal bus J7 - J0
MUXB1, MUXB0: Control the state of internal bus K7 - K0
MUXC1, MUXC0: Control the state of internal bus L7 - L0
MUXD1, MUXD0: Control the state of internal bus M7 - M0

AAAMUX
Level signal for enabling/disabling the 16-bit multiplier/accumulator path to the ALU.
0 → Path enabled. ALU takes operand from RM0.
1 → Path disabled. ALU takes operand from internal buses J7 - J0 and K7 - K0.

ALU3 - ALU0
Clocked ALU opcode. See Table B.

MAC2 - MAC0, TCB, TCA
Clocked multiplier opcode. See Table C.

RMUX
Level signal for multiplexing the contents of RM0 and RA0.
0 → Output RM015 - RM00
1 → Output RA015 - RA00

$\overline{OE}$
Active LOW Enable signal for making available the 16-bit result, R15 - R0.

Instruction Format

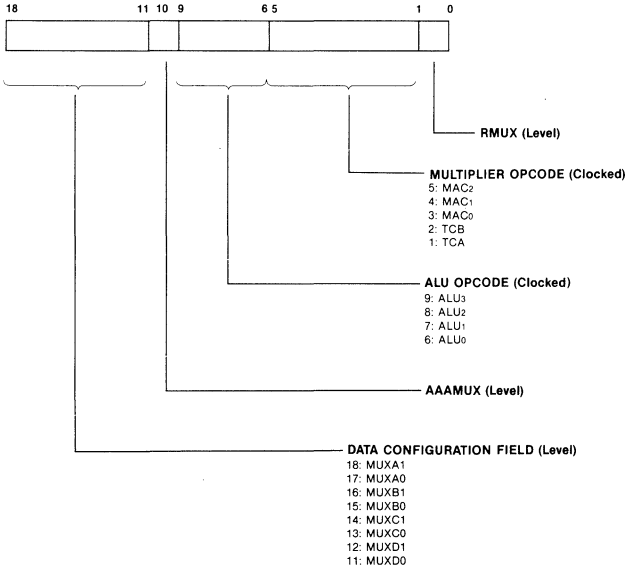


Table A: Data Input Configuration

Data Configuration Field										Internal Buses			
$MUXA_1$	$MUXA_0$	$MUXB_1$	$MUXB_0$	$MUXC_1$	$MUXC_0$	$MUXD_1$	$MUXD_0$	$J_7 - J_0$	$K_7 - K_0$	$L_7 - L_0$	$M_7 - M_0$
0	0							$R_{A7} - R_{A0}$			
0	1							$R_{B7} - R_{B0}$			
1	0							$R_{C7} - R_{C0}$			
1	1							$R_{D7} - R_{D0}$			
		0	0						$R_{A7} - R_{A0}$		
		0	1						$R_{B7} - R_{B0}$		
		1	0						$R_{C7} - R_{C0}$		
		1	1						$R_{D7} - R_{D0}$		
				0	0					$R_{A7} - R_{A0}$	
				0	1					$R_{B7} - R_{B0}$	
				1	0					$R_{C7} - R_{C0}$	
				1	1					$R_{D7} - R_{D0}$	
						0	0				$R_{A7} - R_{A0}$
						0	1				$R_{B7} - R_{B0}$
						1	0				$R_{C7} - R_{C0}$
						1	1				$R_{D7} - R_{D0}$

Table B: Arithmetic and Logic Operations

Signal										Function
AAAMUX	ALU_3	ALU_2	ALU_1	ALU_0	MAC_2	MAC_1	MAC_0	TCB	TCA	
X	0	0	0	0	X	X	X	X	X	Clear ALU Output
0	0	0	0	1	X	X	X	X	X	($L_8 - L_0$ ‖ $M_8 - M_0$) minus $R_{MO16} - R_{MO0}$
0	0	0	1	0	X	X	X	X	X	$R_{MO16} - R_{M00}$ minus ($L_8 - L_0$ ‖ $M_8 - M_0$)
0	0	0	1	1	X	X	X	X	X	$R_{MO16} - R_{MO0}$ plus ($L_8 - L_0$ ‖ $M_8 - M_0$)
0	0	1	0	0	X	X	X	X	X	$R_{MO16} - R_{MO0}$ XOR ($L_8 - L_0$ ‖ $M_8 - M_0$)
0	0	1	0	1	X	X	X	X	X	$R_{MO16} - R_{MO0}$ OR ($L_8 - L_0$ ‖ $M_8 - M_0$)
0	0	1	1	0	X	X	X	X	X	$R_{MO16} - R_{MO0}$ AND ($L_8 - L_0$ ‖ $M_8 - M_0$)
0	0	1	1	1	X	X	X	X	X	$R_{MO16} - R_{MO0}$ plus $\{0\}_{16-0}$
X	1	0	0	0	X	X	X	X	X	Preset ALU Output
0	1	0	0	1	X	X	X	X	X	$R_{AO16} - R_{AO0}$ minus $R_{MO16} - R_{MO0}$
0	1	0	1	0	X	X	X	X	X	$R_{MO16} - R_{MO0}$ minus $R_{AO16} - R_{AO0}$
0	1	0	1	1	X	X	X	X	X	$R_{MO16} - R_{MO0}$ plus $R_{AO16} - R_{AO0}$

Table B: Arithmetic and Logic Operations, cont'd

Signal										Function
AAAMUX	ALU_3	ALU_2	ALU_1	ALU_0	MAC_2	MAC_1	MAC_0	TCB	BCA	
0	1	1	0	0	X	X	X	X	X	RMO_{16} - RMO_0 XOR RAO_{16} - RAO_0
0	1	1	0	1	X	X	X	X	X	RMO_{16} - RMO_0 OR RAO_{16} - RAO_0
0	1	1	1	0	X	X	X	X	X	RMO_{16} - RMO_0 AND RAO_{16} - RAO_0
0	1	1	1	1	X	X	X	X	X	RMO_{16} - RMO_0 XOR $\{0\}_{16\text{-}0}$
1	0	0	0	1	X	X	X	X	X	(L_8 - L_0 ‖ M_8 - M_0) minus (J_8 - J_0 ‖ K_8 - K_0)
1	0	0	1	0	X	X	X	X	X	(J_8 - J_0 ‖ K_8 - K_0) minus (L_8 - L_0 ‖ M_8 - M_0)
1	0	0	1	1	X	X	X	X	X	(J_8 - J_0 ‖ K_8 - K_0) plus (L_8 - L_0 ‖ M_8 - M_0)
1	0	1	0	0	X	X	X	X	X	(J_8 - J_0 ‖ K_8 - K_0) XOR (L_8 - L_0 ‖ M_8 - M_0)
1	0	1	0	1	X	X	X	X	X	(J_8 - J_0 ‖ K_8 - K_0) OR (L_8 - L_0 ‖ M_8 - M_0)
1	0	1	1	0	X	X	X	X	X	(J_8 - J_0 ‖ K_8 -K_0) AND (L_8 - L_0 ‖ M_8 - M_0)
1	0	1	1	1	X	X	X	X	X	(J_8 - J_0 ‖ K_8 - K_0) plus $\{0\}_{16\text{-}0}$
1	1	0	0	1	X	X	X	X	X	RAO_{16} - RAO_0 minus (J_8 - J_0 ‖ K_8 - K_0)
1	1	0	1	0	X	X	X	X	X	(J_8 - J_0 ‖ K_8 - K_0) minus RAO_{16} - RAO_0
1	1	0	1	1	X	X	X	X	X	(J_8 - J_0 ‖ K_8 - K_0) plus RAO_{16} - RAO_0
1	1	1	0	0	X	X	X	X	X	(J_8 - J_0 ‖ K_8 - K_0) XOR RAO_{16} - RAO_0
1	1	1	0	1	X	X	X	X	X	(J_8 - J_0 ‖ K_8 - K_0) OR RAO_{16} - RAO_0
1	1	1	1	0	X	X	X	X	X	(J_8 - J_0 ‖ K_8 - K_0) AND RAO_{16} - RAO_0
1	1	1	1	1	X	X	X	X	X	(J_8 - J_0 ‖ K_8 - K_0) XOR $\{0\}_{16\text{-}0}$

Note: Combination of ALU and multiplier opcodes allowed.

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Table C: Multiplication Operations

Signal										Function
AAAMUX	ALU_3	ALU_2	ALU_1	ALU_0	MAC_2	MAC_1	MAC_0	TCB	TCA	
X	X	X	X	X	0	0	0	0	0	$(J_8 - J_0 \times K_8 - K_0)$
X	X	X	X	X	0	0	0	0	1	$(J'_8 - J'_0 \times K_8 - K_0)$
X	X	X	X	X	0	0	0	1	0	$(J_8 - J_0 \times K'_8 - K'_0)$
X	X	X	X	X	0	0	0	1	1	$(J'_8 - J'_0 \times K'_8 - K'_0)$
X	X	X	X	X	0	0	1	0	0	$(J_8 - J_0 \times K_8 - K_0)$ plus $RMO'_{16} - RMO'_0$
X	X	X	X	X	0	0	1	0	1	$(J'_8 - J'_0 \times K_8 - K_0)$ plus $RMO'_{16} - RMO'_0$
X	X	X	X	X	0	0	1	1	0	$(J_8 - J_0 \times K'_8 - K'_0)$ plus $RMO'_{16} - RMO'_0$
X	X	X	X	X	0	0	1	1	1	$(J'_8 - J'_0 \times K'_8 - K'_0)$ plus $RMO'_{16} - RMO'_0$
X	X	X	X	X	0	1	0	X	X	Clear $RMO_{16} - RMO_0$
X	X	X	X	X	0	1	1	0	0	Undefined
X	X	X	X	X	0	1	1	0	1	$(J'_8 - J'_0 \times K_8 - K_0)$ minus $RMO'_{16} - RMO'_0$
X	X	X	X	X	0	1	1	1	0	$(J_8 - J_0 \times K'_8 - K'_0)$ minus $RMO'_{16} - RMO'_0$
X	X	X	X	X	0	1	1	1	1	$(J'_8 - J'_0 \times K'_8 - K'_0)$ minus $RMO'_{16} - RMO'_0$
X	X	X	X	X	1	0	0	0	0	Undefined
X	X	X	X	X	1	0	0	0	1	$(-J'_8 - J'_0 \times K_8 - K_0)$
X	X	X	X	X	1	0	0	1	0	$(-J_8 - J_0 \times K'_8 - K'_0)$
X	X	X	X	X	1	0	0	1	1	$(-J'_8 - J'_0 \times K'_8 - K'_0)$
X	X	X	X	X	1	0	1	0	0	Undefined
X	X	X	X	X	1	0	1	0	1	$(-J'_8 - J'_0 \times K_8 - K_0)$ plus $RMO'_{16} - RMO'_0$
X	X	X	X	X	1	0	1	1	0	$(-J_8 - J_0 \times K'_8 - K'_0)$ plus $RMO'_{16} - RMO'_0$
X	X	X	X	X	1	0	1	1	1	$(-J'_8 - J'_0 \times K'_8 - K'_0)$ plus $RMO'_{16} - RMO'_0$
X	X	X	X	X	1	1	0	X	X	Preset $RMO_{16} - RMO_0$
X	X	X	X	X	1	1	1	0	0	Undefined
X	X	X	X	X	1	1	1	0	1	$(-J'_8 - J'_0 \times K_8 - K_0)$ minus $RMO'_{16} - RMO'_0$
X	X	X	X	X	1	1	1	1	0	$(-J_8 - J_0 \times K'_8 - K'_0)$ minus $RMO'_{16} - RMO'_0$
X	X	X	X	X	1	1	1	1	1	$(-J'_8 - J'_0 \times K'_8 - K'_0)$ minus $RMO'_{16} - RMO'_0$

Notes: Combination of ALU and multiplier opcodes allowed.
' stands for twos complement representation of a number.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74AC/ACT 25°C	54AC/ACT	74AC/ACT	Units	Conditions
		Typ	Guaranteed Limit			
I_{IN}	Maximum Input Current		0.1	10.0	1.0	μA	V_{CC} = Max V_{IN} = V_{CC}
I_{OZ}	Maximum 3-State Current		0.5	10.0	5.0	μA	High Z, V_{CC} = Max V_{OUT} = 0 to V_{CC}
I_{CCQ}	Supply Current, Quiescent	50.0	2.0	10.0	10.0	mA	V_{CC} = Max, V_{IN} = 0 V
V_{OH}	Minimum HIGH Level Output	4.49	4.4	4.4	4.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		5.49	5.4	5.4	5.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			3.86	3.70	3.76	V	I_{OH} = − 8 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = − 8 mA, V_{CC} = 5.5 V
V_{OL}	Maximum HIGH Level Output	0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 4.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 5.5 V
I_{OLD}	Minimum Dynamic Output Current			32	32	mA	V_{CC} = 5.5 V V_{OLD} = 2.2 V
I_{OHD}	Minimum Dynamic Output Current			− 32	− 32	mA	V_{CC} = 5.5 V V_{OHD} = 3.3 V

Note 1: Test Load 50 pF, 500 ohm to Ground

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_A	Arithmetic Operation Time	3.3 5.0		31.0						ns	1
t_L	Logic Operation Time	3.3 5.0		24.0						ns	1
t_M	Multiply Time	3.3 5.0		60.0						ns	2
t_D	Output Delay	3.3 5.0		7.0						ns	1,2
t_{ENA}	3-State Output Enable Delay	3.3 5.0		7.0						ns	1,2
t_{DIS}	3-State Output Disable Delay	3.3 5.0		8.5						ns	1,2
t_s	Input Register Setup Time	3.3 5.0		3.0						ns	1,2
t_h	Input Register Hold Time	3.3 5.0		0						ns	1,2
t_w	Clock Pulse Width	3.3 5.0		5.0						ns	1,2

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_A	Arithmetic Operation Time	5.0		31.0						ns	1
t_L	Logic Operation Time	5.0		24.0						ns	1
t_M	Multiply Time	5.0		50.0						ns	2
t_D	Output Delay	5.0		7.0						ns	1,2
t_{ENA}	3-State Output Enable Delay	5.0		7.0						ns	1,2
t_{DIS}	3-State Output Disable Delay	5.0		8.5						ns	1,2
t_s	Input Register Setup Time	5.0		3.0						ns	1,2
t_h	Input Register Hold Time	5.0		0						ns	1,2
t_w	Clock Pulse Width	5.0		5.0						ns	1,2

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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Waveforms

Figure 1: Arithmetic Logic Operation

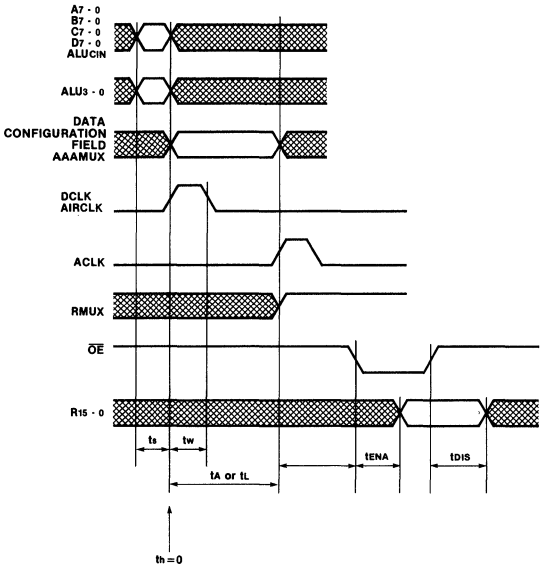
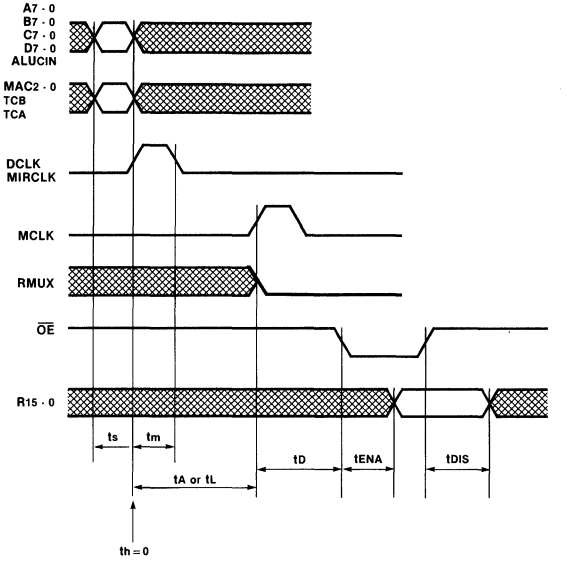


Figure 2: Multiplication



CPGA Pinout

Pinout to Signal

Pinout	Signal	Pinout	Signal
A1	MCOUT	F3	GND_2
A2	MAC_1	F9	VCC_1
A3	MAC_0	F10	C_2
A4	TCA	F11	B_0
A5	ACLK	G1	R_8
A6	MCLK	G2	R_9
A7	$MUXA_0$	G3	VCC_2
A8	A_5	G9	GND_1
A9	A_3	G10	C_1
A10	A_2	G11	C_0
A11	$MUXB_1$	H1	R_{11}
B1	R_0	H2	R_{12}
B2	MZ	H10	C_4
B3	MAC_2	H11	C_3
B4	TCB	J1	R_{13}
B5	MIRCLK	J2	R_{15}
B6	A_6	J5	ALU_2
B7	A_7	J6	$MUXD_1$
B8	A_4	J7	$MUXD_0$
B9	A_1	J10	C_7
B10	A_0	J11	C_5
B11	B_7	K1	R_{14}
C1	R_1	K2	AE
C2	ME	K3	ACOUT
C3	NO	K4	$ALUC_{IN}$
	CONNECTION	K5	ALU_1
C5	AIRCLK	K6	AAAMUX
C6	DCLK	K7	D_6
C7	$MUXA_1$	K8	D_3
C10	$MUXB_0$	K9	D_0
C11	B_6	K10	$MUXC_0$
D1	R_3	K11	C_6
D2	R_2	L1	AZ
D10	B_5	L2	$\overline{OE}$
D11	B_4	L3	RMUX
E1	R_6	L4	ALU_3
E2	R_5	L5	ALU_0
E3	R_4	L6	D_5
E9	B_3	L7	D_7
E10	B_2	L8	D_4
E11	B_1	L9	D_2
F1	R_{10}	L10	D_1
F2	R_7	L11	MUXC1

Signal to Pinout

Signal	Pinout	Signal	Pinout
MZ	B2	$MUXC_0$	K10
ME	C2	C_7	J10
R_0	B1	C_6	K11
R_1	C1	C_5	J11
R_2	D2	C_4	H10
R_3	D1	C_3	H11
R_4	E3	C_2	F10
R_5	E2	C_1	G10
R_6	E1	C_0	G11
R_7	F2	GND_1	G9
GND_2	F3	VCC_1	F9
VCC_2	G3	B_0	F11
R_8	G1	B_1	E11
R_9	G2	B_2	E10
R_{10}	F1	B_3	E9
R_{11}	H1	B_4	D11
R_{12}	H2	B_5	D10
R_{13}	J1	B_6	C11
R_{14}	K1	B_7	B11
R_{15}	J2	$MUXB_0$	C10
AZ	L1	$MUXB_1$	A11
AE	K2	A_0	B10
ACOUT	K3	A_1	B9
$\overline{OE}$	L2	A_2	A10
RMUX	L3	A_3	A9
$ALUC_{IN}$	K4	A_4	B8
ALU_3	L4	A_5	A8
ALU_2	J5	A_6	B6
ALU_1	K5	A_7	B7
ALU_0	L5	$MUXA_0$	A7
AAAMUX	K6	$MUXA_1$	C7
MUXD1	J6	DCLK	C6
$MUXD_0$	J7	MCLK	A6
D_7	L7	ACLK	A5
D_6	K7	MIRCLK	B5
D_5	L6	AIRCLK	C5
D_4	L8	TCA	A4
D_3	K8	TCB	B4
D_2	L9	MAC_0	A3
D_1	L10	MAC_1	A2
D_0	K9	MAC_2	B3
$MUXC_1$	L11	MCOUT	A1

5

54AC/74AC708 • 54ACT/74ACT708

64 x 9 First-In, First-Out Memory

Description

The 'AC/'ACT708 is an expandable first-in, first-out memory organized as 64 words by 9 bits. An 85 MHz shift-in and 60 MHz shift-out data rate make it ideal for high-speed applications. It uses a dual port RAM architecture with pointer logic to achieve the high speed with almost negligible fall-through time.

Separate Shift-In (SI) and Shift-Out (SO) clocks control the use of synchronous or asynchronous write or read. Other controls include a Master Reset ($\overline{MR}$) and Output Enable ($\overline{OE}$) for initializing the internal registers and allowing the data outputs to be 3-stated. Input Ready (IR) and Output Ready (OR) signal when the FIFO is ready for I/O operations. The status flags HF and FULL indicate when the FIFO is full, empty or half full.

The FIFO can be expanded to increase the depth by cascading or to provide different word lengths by tying off unused data inputs.

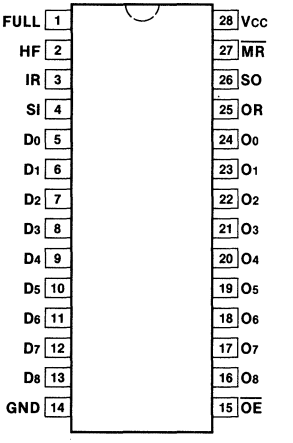
- **64-Words by 9-Bit Dual Port RAM Organization.**
- **85 MHz Shift-In, 60 MHz Shift-Out Data Rate with Flags, Typical 'ACT708**
- **Expandable in Word Depth and Width Dimensions**
- **'ACT708 has TTL-Compatible Inputs**
- **Asychronous or Synchronous Operation**
- **Asynchronous Master Reset**
- **Outputs Source/Sink 8 mA**
- **3-State Outputs**
- **Full ESD Protection**
- **Output and Input Pins Directly in Line for Easy Board Layout**
- **TRW 1030 Work-Alike Operation Available**

Applications

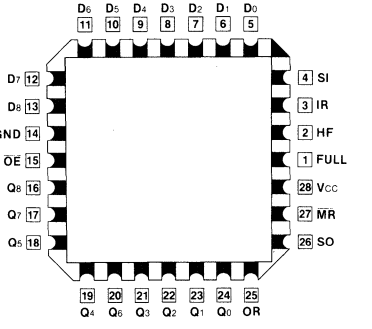
- **High-Speed Disk or Tape Controllers**
- **A/D Output Buffers**
- **High-Speed Graphics Pixel Buffer**
- **Video Time Base Correction**
- **Digital Filtering**

Ordering Code: See Section 6

Connection Diagrams

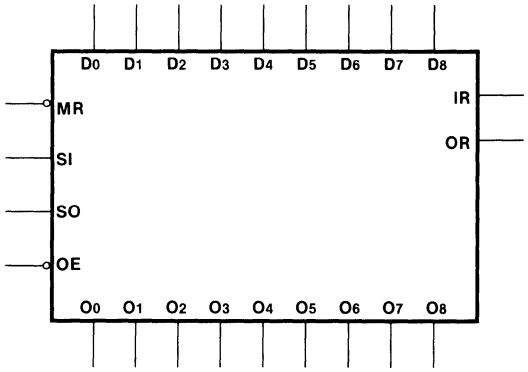


Pin Assignment for DIP and Flatpak



Pin Assignment for LCC and PCC

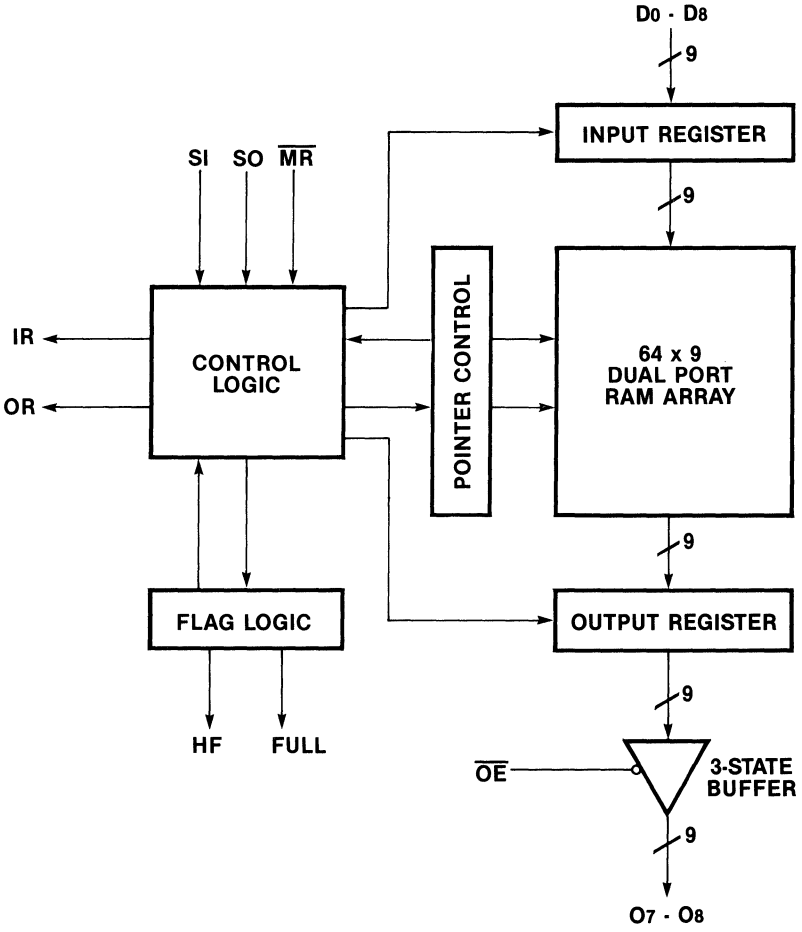
Logic Symbol



Pin Names

D_0 - D_8	Data Inputs
$\overline{MR}$	Master Reset
$\overline{OE}$	Output Enable Input
SI	Shift-In
SO	Shift-Out
IR	Input Ready
OR	Output Ready
HF	Half Full Flag
FULL	Full Flag
O_0 - O_8	Data Outputs

Block Diagram



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Functional Description

Inputs

Data Inputs (D_0 - D_8)
Data inputs for 9-bit wide data are TTL-compatible ('ACT708). Word width can be reduced by tying unused inputs to ground and leaving the corresponding outputs open.

Reset ($\overline{MR}$)
Reset is accomplished by pulsing the $\overline{MR}$ input LOW. During normal operation $\overline{MR}$ is HIGH. A reset is required after power up to guarantee correct operation. On reset, the data outputs go LOW, IR goes HIGH, OR goes LOW, HF and FULL go LOW. During reset, both internal read and write pointers are set to the first location in the array.

Shift-In (SI)
Data is written into the FIFO by pulsing SI HIGH. When Shift-In goes HIGH, the data is loaded into an internal data latch. Data setup and hold times need to be adhered to with respect to the falling edge of SI. The write cycle is complete after the falling edge of SI. The shift-in is independent of any ongoing shift-out operation. After the first word has been written into the FIFO, the falling edge of SI makes HF go HIGH, indicating a non-empty FIFO. The first data word appears at the output after the falling edge of SI. After half the memory is filled, the next rising edge of SI makes FULL go HIGH indicating a half-full FIFO. When the FIFO is full, any further shift-ins are disabled.

When the FIFO is empty and $\overline{OE}$ is LOW, the falling edge of the first SI will cause the first data word just shifted-in to appear at the output, even though SO may be LOW.

Shift-Out (SO)
Data is read from the FIFO by the Shift-Out signal provided the FIFO is not empty. SO going HIGH causes OR to go LOW indicating that output stage is busy. On the falling edge of SO, new data reaches the output after propagation delay t_D. If the last data has been shifted-out of the memory, OR continues to remain LOW, and the last word shifted-out remains on the output pins.

Output Enable ($\overline{OE}$)
$\overline{OE}$ LOW enables the 3-state output buffers. When $\overline{OE}$ is HIGH, the outputs are in a 3-state mode.

Outputs

Data Outputs (O_0 - O_8)
Data outputs are enabled when $\overline{OE}$ is LOW and in the 3-state condition when $\overline{OE}$ is HIGH.

Input Ready (IR)
IR HIGH indicates data can be shifted-in. When SI goes HIGH, IR goes LOW, indicating input stage is busy. IR stays LOW when the FIFO is full and goes HIGH after the falling edge of the first shift-out.

Output Ready (OR)
OR HIGH indicates data can be shifted-out from the FIFO. When SO goes HIGH, OR goes LOW, indicating output stage is busy. OR is LOW when the FIFO is reset or empty and goes HIGH after the falling edge of the first shift-in.

Half-Full (HF)
This status flag along with the FULL status flag indicates the degree of fullness of the FIFO. On reset, HF is LOW; it rises on the falling edge of the first SI. The rising edge of the SI pulse that fills up the FIFO makes HF go LOW. Going from the empty to the full state with SO LOW, the falling edge of the first SI causes HF to go HIGH, the rising edge of the 33rd SI causes FULL to go HIGH, and the rising edge of the 64th SI causes HF to go LOW.

When the FIFO is full, HF is LOW and the falling edge of the first shift-out causes HF to go HIGH indicating a "non-full" FIFO.

Full Flag (FULL)
This status flag along with the HF status flag indicates the degree of fullness of the FIFO. On reset, FULL is LOW. When half the memory is filled, on the rising edge of the next SI, the FULL flag goes HIGH. It remains set until the difference between the write pointer and the read pointer is less than or equal to one-half of the total memory of the device. The FULL flag then goes LOW on the rising edge of the next SO.

Status Flags Truth Table

HF	FULL	Status Flag Conditions
0	0	Empty
0	1	Full
1	0	<32 Locations Filled
1	1	≥32 Locations Filled

Reset Truth Table

Inputs			Outputs				
$\overline{MR}$	SI	SO	IR	OR	HF	FULL	O_0 - O_8
1	X	X	X	X	X	X	X
0	X	X	1	0	0	0	0

Modes of Operation

Mode 1: Shift In Sequence for FIFO Empty to Full

Sequence of Operation

1. Input Ready is initially HIGH; HF and FULL flags are LOW. The FIFO is empty and prepared for valid data. OR is LOW indicating that the FIFO is not yet ready to output data.

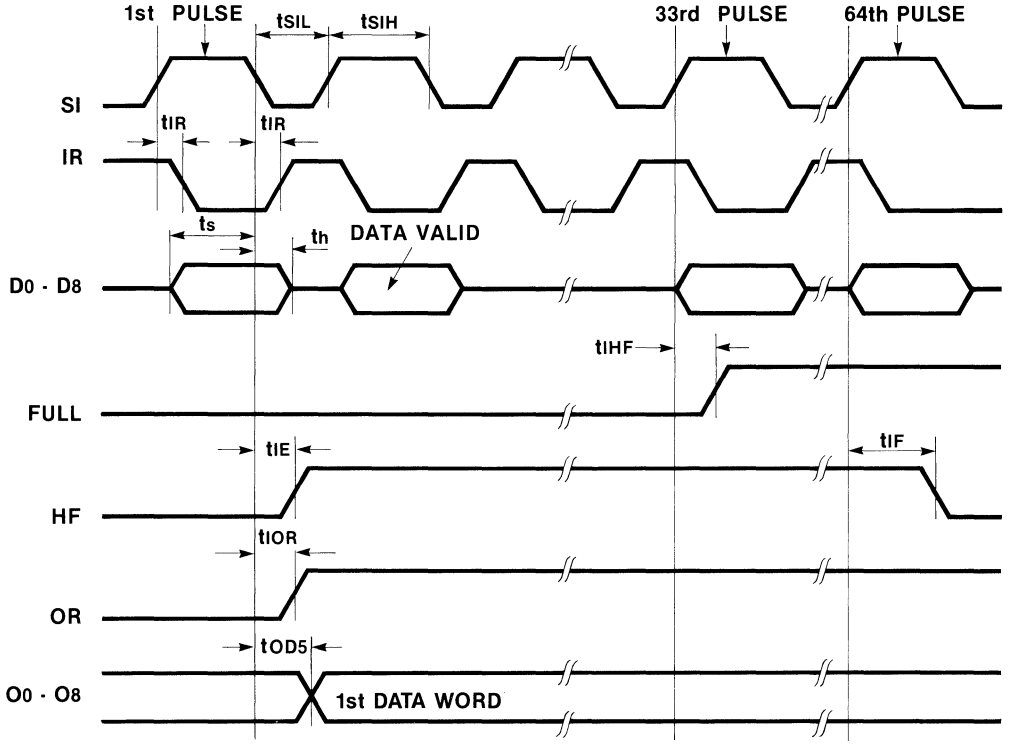
2. Shift-In is set HIGH, and data is loaded into the FIFO. Data has to be settled t_s before the falling edge of SI and held t_h after.

3. Input Ready (IR) goes LOW propagation delay t_{IR} after SI goes HIGH: input stage is busy.

4. Shift-In is set LOW; IR goes HIGH indicating the FIFO is ready for additional data. Data just shifted-in arrives at output propagation delay t_{OD5} after SI falls. OR goes HIGH propagation delay t_{IOR} after SI goes LOW, indicating the FIFO has valid data on its outputs. HF goes HIGH propagation delay t_{IE} after SI falls, indicating the FIFO is no longer empty.

5. The process is repeated through the 64th data word. On the rising edge of the 33rd SI, FULL flag goes HIGH propagation delay t_{IHF} after SI, indicating a half-full FIFO. HF goes LOW propagation delay t_{IF} after the rising edge of the 64th pulse indicating that the FIFO is full. Any further shift-ins are disabled.

Figure 1: Modes of Operation
Mode 1



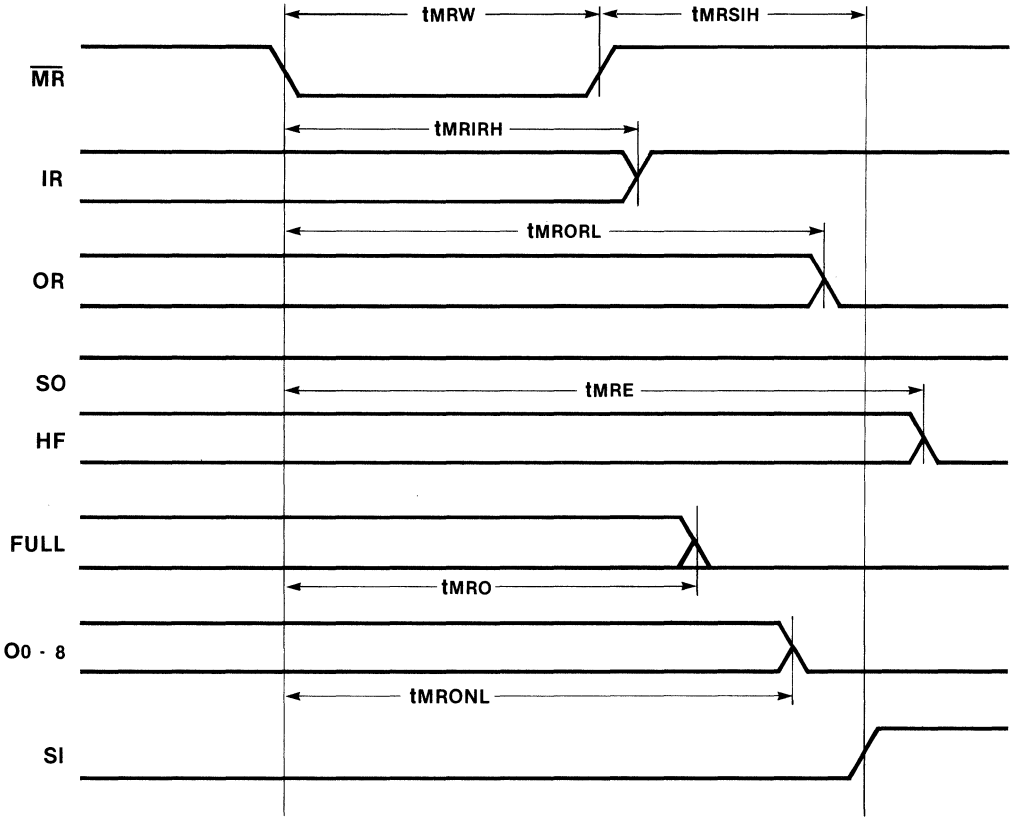
Note: SO and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH.

Mode 2: Master Reset

Sequence of Operation

1. Input and Output Ready, HF and FULL can be in any state before the reset sequence with Master Reset ($\overline{MR}$) HIGH.
2. Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width t_{MRW} before rising again.
3. Master Reset rises.
4. IR rises (if not HIGH already) to indicate ready to write state recovery time t_{MRIRH} after the falling edge of $\overline{MR}$. Both HF and FULL will go LOW indicating an empty FIFO, occurring recovery times t_{MRE} and t_{MRO} respectively after the falling edge of $\overline{MR}$. OR falls recovery time t_{MRORL} after $\overline{MR}$ falls. Data at outputs goes LOW recover time t_{MRONL} after $\overline{MR}$ goes LOW.
5. Shift-In goes HIGH a minimum of recovery time t_{MRSIH} after $\overline{MR}$ goes HIGH.

Figure 2: Modes of Operation
Mode 2

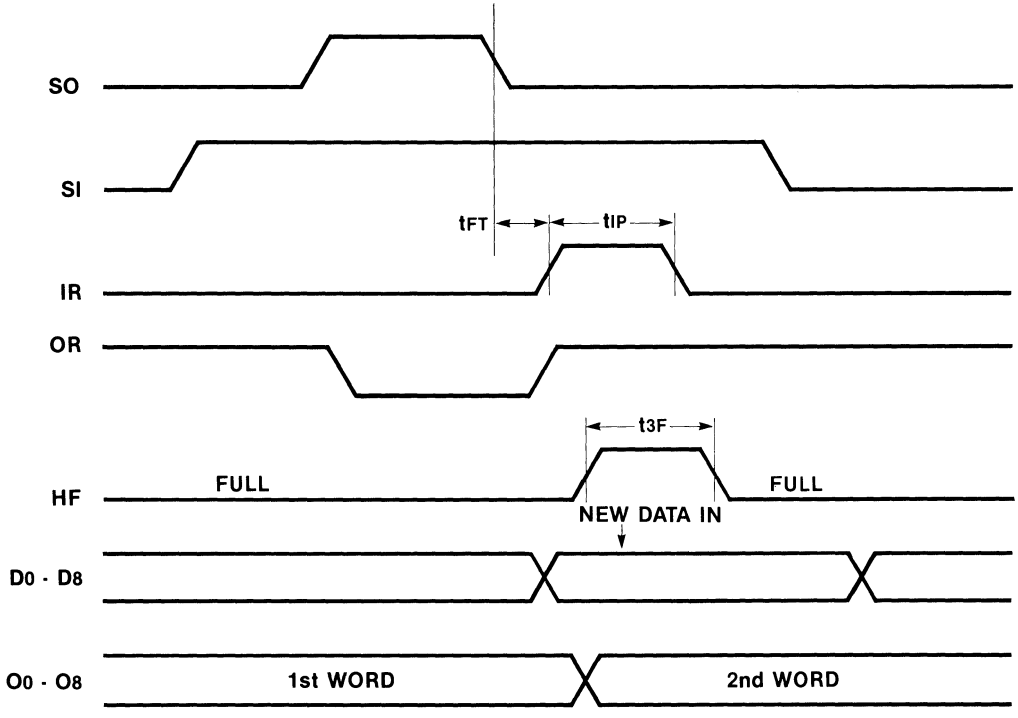


Mode 3: With FIFO Full, Shift-In is Held HIGH in Anticipation of an Empty Location

Sequence of Operation

1. The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. Shift-Out is LOW. IR is LOW.
2. Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after propagation delay t_D. New data is written into the FIFO after SO goes LOW.
3. Input Ready goes HIGH fall-through time t_{FT} after the falling edge of SO. Also, HF goes HIGH t_{OF} after SO falls, indicating that the FIFO is no longer full.
4. IR returns LOW pulse width t_{IP} after rising and shifting fresh data in. Also, HF returns LOW pulse width t_{3F} after rising, indicating the FIFO is once more full.
5. Shift-In is brought LOW to complete the shift-in process and maintain normal operation.

Figure 3: Modes of Operation
Mode 3



Note: $\overline{MR}$ and FULL are HIGH; $\overline{OE}$ is LOW.

Mode 4: Shift-Out Sequence, FIFO Full to Empty

Sequence of Operation

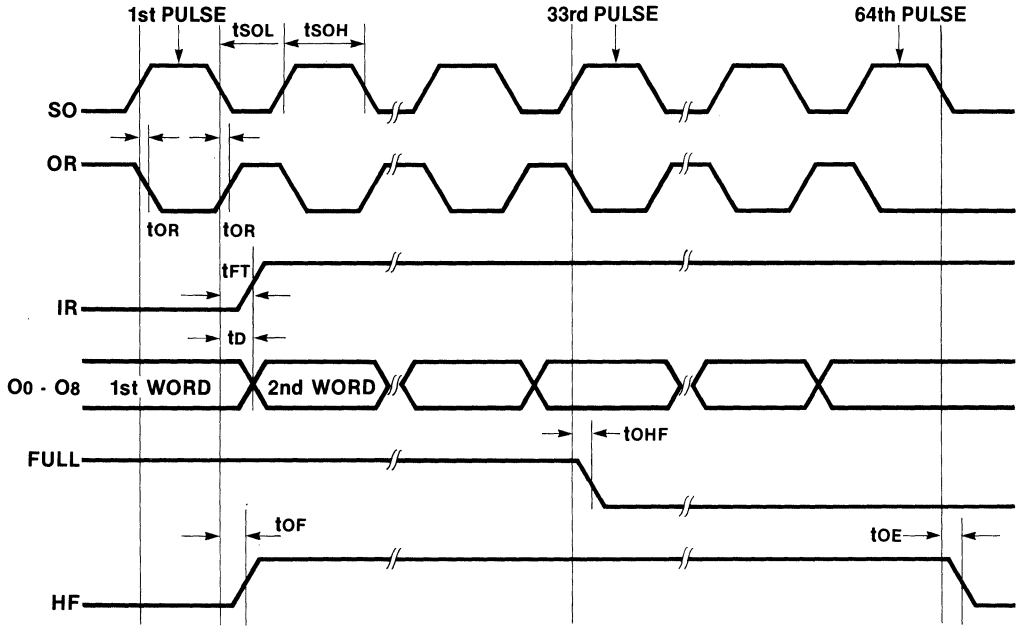
1. FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.

2. SO goes HIGH, resulting in OR going LOW propagation delay t_{OR} after SO rises. OR LOW indicates output stage is busy.

3. SO goes LOW, new data reaches output propagation delay t_D after SO falls; OR goes HIGH propagation delay t_{OR} after SO falls and HF rises propagation delay t_{OF} after SO falls. IR rises fall-through time t_{FT} after SO falls.

4. Repeat process through the 64th SO pulse. FULL flag goes LOW propagation delay t_{OHF} after the rising edge of 33rd SO, indicating that the FIFO is less than half full. On the falling edge of the 64th SO, HF goes LOW propagation delay t_{OE} after SO, indicating the FIFO is empty. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.

Figure 4: Modes of Operation
Mode 4



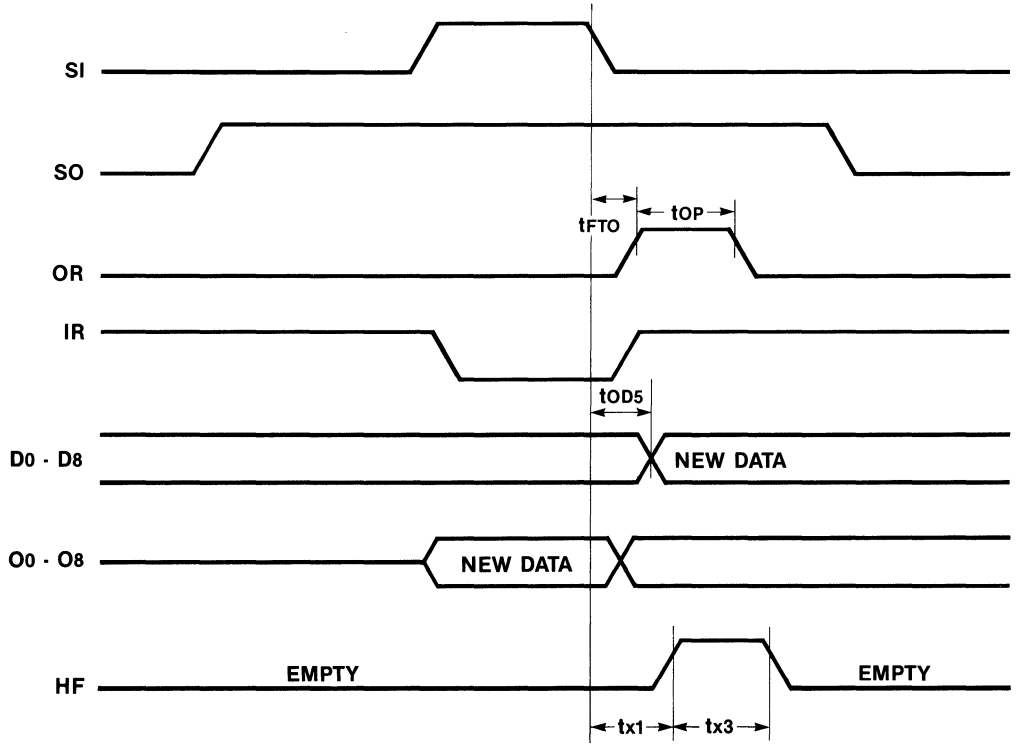
Note: SI and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH; D_0 - D_8 are immaterial.

Mode 5: With FIFO Empty, Shift-Out is Held HIGH in Anticipation of Data

Sequence of Operation

1. FIFO is initially empty; Shift-Out goes HIGH.
2. Shift-In pulse loads data into the FIFO and IR falls. HF rises propagation delay t_{X1} after the falling edge of SI.
3. OR rises fall-through time t_{FTO} after the falling edge of Shift-In, indicating that new data is ready to be output.
4. Data arrives at output propagation delay t_{OD5} after the falling edge of Shift-In.
5. OR goes LOW pulse width t_{OP} after rising and HF goes LOW pulse width t_{X3} after rising, indicating that the FIFO is empty once more.
6. Shift-Out goes LOW, necessary to complete the Shift-Out process.

Figure 5: Modes of Operation
Mode 5



Note: FULL is LOW; $\overline{MR}$ is HIGH; $\overline{OE}$ is LOW; $t_{DOF} = t_{FTO} - t_{OD5}$. Data output transition—valid data arrives at output stage t_{DOF} after OR is HIGH.

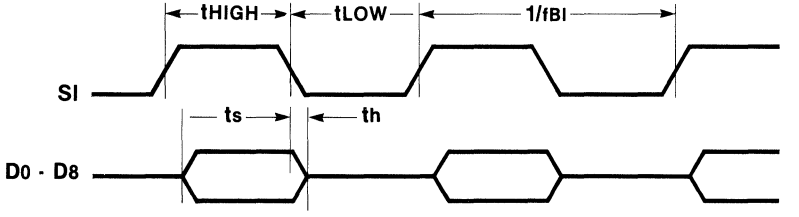
Mode 6: Shift-In Operation in High-Speed Burst Mode

Sequence of Operation

1. Shift-In goes HIGH, loading data into the FIFO. IR is ignored.
2. Shift-in goes LOW pulse width t_{HIGH} time later, loading is complete.
3. Shift-In rises again for the second load pulse width t_{LOW} after the falling edge.

The burst-in rate is determined by SI HIGH and LOW. Data is shifted-in, ignoring the IR flag. Any SI after the FIFO is filled up will be ignored.

Figure 6: Modes of Operation
Mode 6



Note: $\overline{MR}$ is HIGH; $t_{HIGH} > t_{SIH}$; $t_{LOW} > t_{SIL}$; $t_{HIGH} + t_{LOW} \geq 1/f_{BI}$.

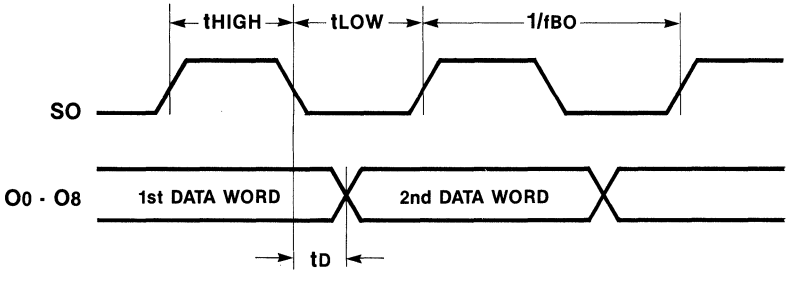
Mode 7: Shift-Out Operation in High Speed Burst Mode

Sequence of Operation

1. Shift-Out is LOW; valid data is available on output with OR ignored.
2. Shift-Out rises; data out is latched.
3. Shift-Out falls; new data is loaded onto output.

The Burst-out rate is determined by minimum SO HIGH and LOW. The OR flag is ignored.

Figure 7: Modes of Operation
Mode 7



Note: $\overline{OE}$ is LOW; $\overline{MR}$ is HIGH; $t_{HIGH} > t_{SOH}$; $t_{LOW} > t_{SOL}$; $t_{HIGH} + t_{LOW} \geq 1/f_{BO}$.

FIFO Expansion

Word Width Expansion

Word width can be increased by connecting the corresponding input control signals of multiple devices. Flags can be monitored on any one device (Figure 8), or composite flag signals can be achieved by ANDing the corresponding flags.

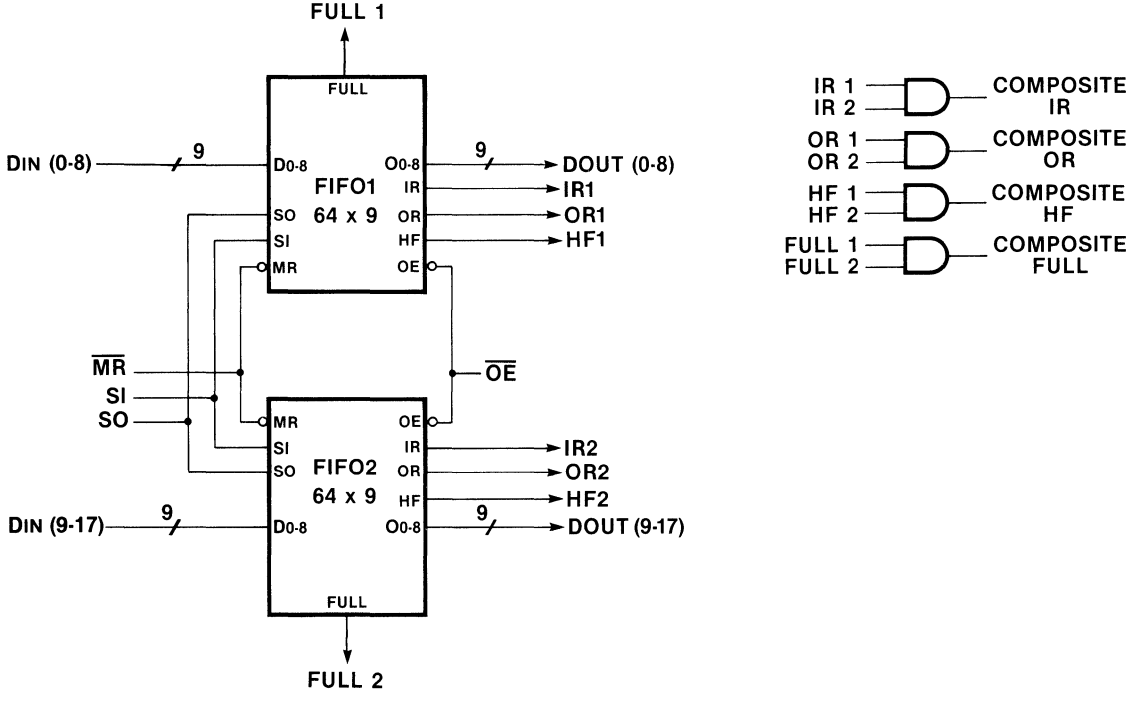
Depth Expansion

Depth Expansion can be achieved by connecting as shown in Figure 9. No external circuitry is required for handshaking, which is achieved by the internal FIFO signals IR and OR.

When n FIFOs are cascaded to attain a 64n-word FIFO, the SI signal is connected to the first FIFO and the SO signal to the nth FIFO. The IR and OR signals are monitored from the first and last FIFOs respectively. The IR signal from each FIFO is connected to its preceding SO signal: IR(n)→SO(n-1); IR(n-1)→SO(n-2) . . . IR(2)→SO(1). The OR signal from each FIFO is connected to its succeeding SI signal: i.e., OR(1)→SI(2); OR(2)→SI(3) . . . OR(n-1)→SI(n). Handshaking signals are shown in Figure 10.

FIFO1 operates in Mode 5 during Shift-In until FIFO2 is filled. FIFO2 operates in Mode 3 during Shift-Out until FIFO1 is empty. Data from FIFO1 is written into FIFO2 after a word is read from FIFO2. To achieve this, the $\overline{OE}$ pin is grounded for FIFO1. In general, for n FIFOs, all $\overline{OE}$ pins except the nth FIFO's $\overline{OE}$ pin are enabled. 3-state control of the outputs can be achieved by controlling the nth FIFO's $\overline{OE}$ pin.

Figure 8: Word Width Expansion — 64 x 18 FIFO



Note: Monitor flags from any one FIFO, or AND the corresponding flags to obtain a composite signal.

Figure 9: Depth Expansion Mode — 128 x 9 FIFO

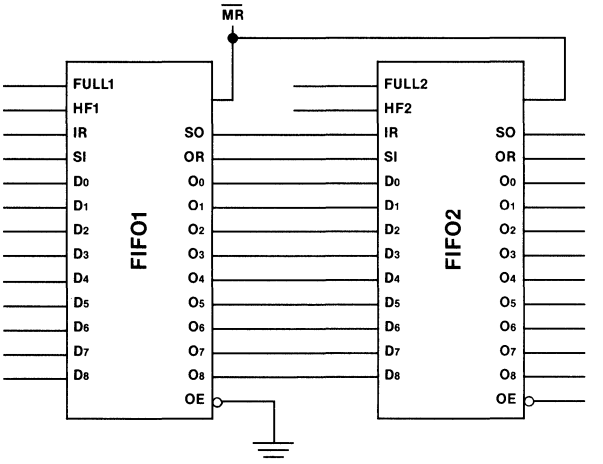
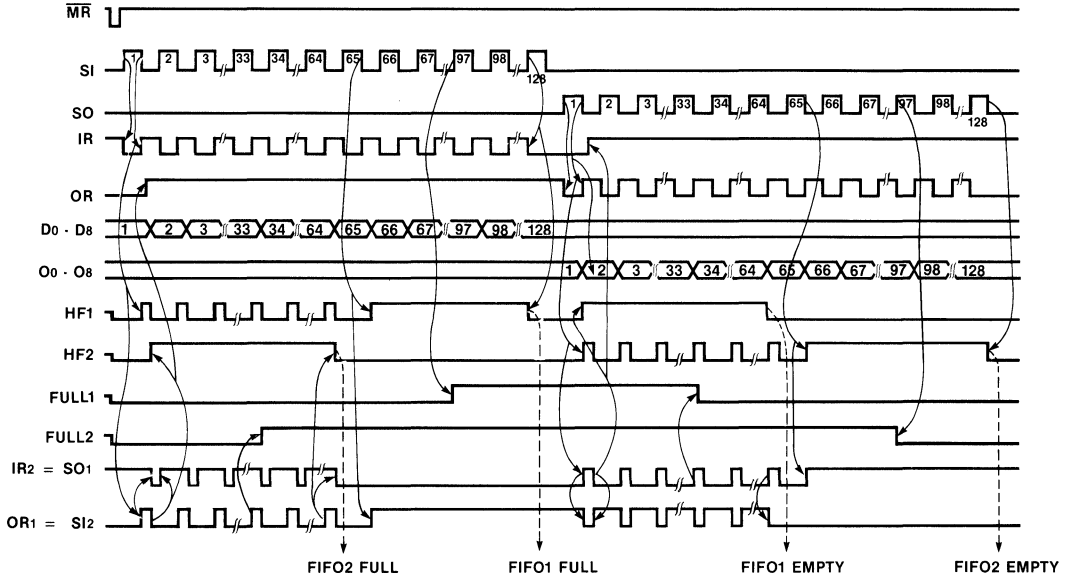


Figure 10: Handshaking for Depth Expansion Mode—128 x 9 FIFO



Note: The numbers for SI and SO indicate the pulse numbers. The numbers for data in and data out indicate data words: 1 is first data word, 2 is second data word, etc.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74AC/ACT 25°C	54AC/ACT	74AC/ACT	Units	Conditions
		Typ	Guaranteed Limit			
I_{IN}	Maximum Input Current		0.1	10.0	1.0	μA	V_{CC} = Max V_{IN} = V_{CC}
I_{OZ}	Maximum 3-State Current		0.5	10.0	5.0	μA	High Z, V_{CC} = Max V_{OUT} = 0 to V_{CC}
I_{CCQ}	Supply Current, Quiescent	50.0	2.0	10.0	10.0	mA	V_{CC} = Max, V_{IN} = 0 V
I_{CCD}	Supply Current, 20 MHz Loaded	325		150	150	mA	V_{CC} = Max, f = 20 MHz Test Load: See Note 1
V_{OH}	Minimum HIGH Level Output	4.49	4.4	4.4	4.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		5.49	5.4	5.4	5.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			3.86	3.70	3.76	V	I_{OH} = – 8 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = – 8 mA, V_{CC} = 5.5 V
V_{OL}	Maximum HIGH Level Output	0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 4.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 5.5 V
I_{OLD}	Minimum Dynamic Output Current			32	32	mA	V_{CC} = 5.5 V V_{OLD} = 2.2 V
I_{OHD}	Minimum Dynamic Output Current			– 32	– 32	mA	V_{CC} = 5.5 V V_{OHD} = 3.3 V

Note 1: Test Load 50 pF, 500 ohm to Ground

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay, t_{IR} SI to IR	3.3 5.0		8.5 5.5						ns	1
t_{PLH}	Propagation Delay, t_{IHF} SI to >HF	3.3 5.0		13.0 9.5						ns	1
t_{PHL}	Propagation Delay, t_{IF} SI to Full Condition	3.3 5.0		13.0 9.5						ns	1
t_{PLH}	Propagation Delay, t_{IE} SI to Not Empty	3.3 5.0		12.5 9.0						ns	1
t_{PLH}	Propagation Delay, t_{IOR} SI to OR	3.3 5.0		13.0 9.5						ns	1
t_{PLH}	Recovery Time, t_{MRIRH} $\overline{MR}$ to IR	3.3 5.0		9.5 7.0						ns	2
t_{PHL}	Recovery Time, t_{MRORL} $\overline{MR}$ to OR	3.3 5.0		20.0 15.0						ns	2
t_{PHL}	Recovery Time, t_{MRO} $\overline{MR}$ to Full Flag	3.3 5.0		9.5 7.0						ns	2
t_{PHL}	Recovery Time, t_{MRE} $\overline{MR}$ to HF Flag	3.3 5.0		20.0 15.0						ns	2
t_{PHL}	Recovery Time, t_{MRONL} $\overline{MR}$ to O_n, LOW	3.3 5.0		11.0 8.0						ns	2
t_w	IR Pulse Width, t_{IP}	3.3 5.0		38.0 28.0						ns	3
t_w	HF Pulse Width, t_{3F}	3.3 5.0		40.0 30.0						ns	3
t_{PHL}, t_{PLH}	Propagation Delay, t_D SO to Data Out	3.3 5.0		23.0 17.0						ns	4
t_{PHL}	Propagation Delay, t_{OHF} SO to <HF	3.3 5.0		11.0 8.0						ns	4
t_{PLH}	Propagation Delay, t_{OF} SO to Not Full	3.3 5.0		15.0 11.0						ns	4
t_{PLH}, t_{PHL}	Propagation Delay, t_{OR} SO to OR	3.3 5.0		9.5 7.0						ns	4

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics, cont'd

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay, t_{OE} SO to Empty	3.3 5.0		12.5 9.0						ns	4
t_{PHL}, t_{PLH}	Propagation Delay, t_{OD5} SI to New Data Out	3.3 5.0		22.0 16.0						ns	1, 5
t_{PLH}	Propagation Delay, t_{X1} SI to HF	3.3 5.0		13.0 9.5						ns	5
t_{PLH}	Propagation Delay, t_{DOF} OR HIGH to Data Out	3.3 5.0		 -11.5						ns	5
t_{PLH}	Fall-Through Time, t_{FTO} SI to OR	3.3 5.0		16.0 11.5						ns	5
t_W	OR Pulse Width, t_{OP}	3.3 5.0		23.0 17.0						ns	5
t_W	HF Pulse Width, t_{X3}	3.3 5.0		26.0 19.0						ns	5
t_{PLH}	Fall-Through Time, t_{FT} SO to IR	3.3 5.0		18.5 13.5						ns	3
t_{PZL}	Output Enable $\overline{OE}$ to O_n	3.3 5.0		7.5 5.5						ns	3-8
t_{PLZ}	Output Disable $\overline{OE}$ to O_n	3.3 5.0		6.0 4.5						ns	3-8
t_{PZH}	Output Enable $\overline{OE}$ to O_n	3.3 5.0		9.0 6.5						ns	3-7
t_{PHZ}	Output Disable $\overline{OE}$ to O_n	3.3 5.0		9.0 6.5						ns	3-7
f_{SI}	Maximum SI Clock Frequency	3.3 5.0		60 85						MHz	1
f_{SO}	Maximum SO Clock Frequency	3.3 5.0		50 60						MHz	4
f_{BO}	Maximum Clock Frequency SO Burst Mode	3.3 5.0		55 65						MHz	7
f_{BI}	Maximum Burst-In Clock	3.3 5.0		60 85						MHz	6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_w	SI Pulse Width, t_{SIH} HIGH	3.3 5.0	4.0 1.5				ns	1, 6
t_w	SI Pulse Width, t_{SIL} LOW	3.3 5.0	4.0 1.5				ns	1, 6
t_s	Setup Time, HIGH or LOW, D_n to SI	3.3 5.0	2.0 1.0				ns	1
t_h	Hold Time, HIGH or LOW, D_n to SI	3.3 5.0	3.0 1.5				ns	1
t_w	$\overline{MR}$ Pulse Width, t_{MRW}	3.3 5.0	17.0 13.0				ns	2
t_{rec}	Recovery Time, t_{MRSIH} $\overline{MR}$ to SI	3.3 5.0	7.0 4.0				ns	2
t_w	SO Pulse Width, t_{SOH} HIGH	3.3 5.0	4.5 2.0				ns	4, 7
t_w	SO Pulse Width, t_{SOL} LOW	3.3 5.0	12.5 9.0				ns	4, 7

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay, t_{IR} SI to IR	5.0	1.0	6.5	11.0	1.0	14.0	1.0	12.0	ns	1
t_{PLH}	Propagation Delay, t_{IHF} SI to >HF	5.0	1.0	10.5	17.0	1.0	21.5	1.0	19.5	ns	1
t_{PHL}	Propagation Delay, t_{IF} SI to Full Condition	5.0	1.0	10.5	16.5	1.0	21.5	1.0	19.5	ns	1
t_{PLH}	Propagation Delay, t_{IE} SI to Not Empty	5.0	1.0	10.0	15.5	1.0	19.5	1.0	17.5	ns	1
t_{PLH}	Propagation Delay, t_{IOR} SI to OR	5.0	1.0	10.5	16.5	1.0	21.5	1.0	19.0	ns	1
t_{PLH}	Recovery Time, t_{MRIRH} $\overline{MR}$ to IR	5.0	13.5	8.5		17.5		15.5		ns	2
t_{PHL}	Recovery Time, t_{MRORL} $\overline{MR}$ to OR	5.0	25.5	16.5		32.5		29.0		ns	2
t_{PHL}	Recovery Time, t_{MRO} $\overline{MR}$ to Full Flag	5.0	14.0	9.0		17.5		16.0		ns	2
t_{PHL}	Recovery Time, t_{MRE} $\overline{MR}$ to HF Flag	5.0	27.5	17.5		34.0		30.5		ns	2
t_{PHL}	Recovery Time, t_{MRONL} $\overline{MR}$ to O_n, LOW	5.0	15.0	9.0		18.5		17.0		ns	2
t_W	IR Pulse Width, t_{IP}	5.0	43.0	28.0		58.5		51.5		ns	3
t_W	HF Pulse Width, t_{3F}	5.0	46.5	30.0		64.5		56.0		ns	3
t_{PHL}, t_{PLH}	Propagation Delay, t_D SO to Data Out	5.0	1.0	18.5	29.5	1.0	38.0	1.0	34.5	ns	4
t_{PHL}	Propagation Delay, t_{OHF} SO to <HF	5.0	1.0	8.5	13.5	1.0	17.5	1.0	15.5	ns	4
t_{PLH}	Propagation Delay, t_{OF} SO to Not Full	5.0	1.0	12.5	19.5	1.0	24.0	1.0	22.0	ns	4
t_{PLH}, t_{PHL}	Propagation Delay, t_{OR} SO to OR	5.0	1.0	7.0	11.5	1.0	14.5	1.0	13.5	ns	4
t_{PLH}	Propagation Delay, t_{OE} SO to Empty	5.0	1.0	9.5	15.5	1.0	19.5	1.0	17.5	ns	4

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics, cont'd

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}, t_{PLH}	Propagation Delay, t_{OD5} SI to New Data Out	5.0	1.0	19.0	30.5	1.0	38.5	1.0	35.5	ns	1, 5
t_{PLH}	Propagation Delay, t_{X1} SI to HF	5.0	1.0	10.0	16.0	1.0	19.5	1.0	18.0	ns	5
t_{PLH}	Propagation Delay, t_{DOF} OR HIGH to Data Out	5.0	1.0	-11.5	-8.5	1.0	-12.5	1.0	-11.5	ns	5
t_{PLH}	Fall-Through Time, t_{FTO} SI to OR	5.0	1.0	13.5	21.0	1.0	26.0	1.0	24.0	ns	5
t_w	OR Pulse Width, t_{OP}	5.0	26.0	17.0		35.0		30.5		ns	5
t_w	HF Pulse Width, t_{X3}	5.0	30.5	20.5		41.5		36.5		ns	5
t_{PLH}	Fall-Through Time, t_{FT} SO to IR	5.0	1.0	15.0	23.5	1.0	34.0	1.0	30.5	ns	3
t_{PZL}	Output Enable $\overline{OE}$ to O_n	5.0	1.0	6.5	11.0	1.0	13.5	1.0	12.0	ns	3-8
t_{PLZ}	Output Disable $\overline{OE}$ to O_n	5.0	1.0	5.0	8.5	1.0	10.0	1.0	9.5	ns	3-8
t_{PZH}	Output Enable $\overline{OE}$ to O_n	5.0	1.0	7.0	12.0	1.0	14.5	1.0	13.0	ns	3-7
t_{PHZ}	Output Disable $\overline{OE}$ to O_n	5.0	1.0	7.0	12.0	1.0	13.5	1.0	13.0	ns	3-7
f_{SI}	Maximum SI Clock Frequency	5.0	55	85		40		45		MHz	1
f_{SO}	Maximum SO Clock Frequency	5.0	42	60		30		35		MHz	4
f_{BO}	Maximum Clock Frequency SO Burst Mode	5.0	42	65		30		35		MHz	7
f_{BI}	Maximum Burst-In Clock	5.0	55	85		40		45		MHz	6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT	Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		
			Typ	Guaranteed Minimum				
t_w	SI Pulse Width, t_{SIH} HIGH	5.0	1.5	3.0	3.5	3.5	ns	1, 6
t_w	SI Pulse Width, t_{SIL} LOW	5.0	1.5	3.0	3.0	3.0	ns	1, 6
t_s	Setup Time, HIGH or LOW, D_n to SI	5.0	1.0	3.5	4.0	4.0	ns	1
t_h	Hold Time, HIGH or LOW, D_n to SI	5.0	1.5	3.5	4.5	4.0	ns	1
t_w	$\overline{MR}$ Pulse Width, t_{MRW}	5.0	13.0	20.0	26.0	24.5	ns	2
t_{rec}	Recovery Time, t_{MRSIH} $\overline{MR}$ to SI	5.0	4.5	7.5	9.0	8.5	ns	2
t_w	SO Pulse Width, t_{SOH} HIGH	5.0	2.0	3.5	5.0	4.5	ns	4, 7
t_w	SO Pulse Width, t_{SOL} LOW	5.0	9.0	14.0	19.0	17.0	ns	4, 7

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V

54AC/74AC723 • 54ACT/74ACT723

64 x 9 First-In, First-Out Memory

Description

The 'AC/'ACT723 is an expandable first-in, first-out memory organized as 64 words by 9 bits. An 85 MHz shift-in and 60 MHz shift-out (typical) data rate make it ideal for high-speed applications. It uses a dual port RAM architecture with pointer logic to achieve the high speed with almost negligible fall-through time.

Separate Shift-In (SI) and Shift-Out (SO) clocks control the use of synchronous or asynchronous write or read. Other controls include a Master Reset ($\overline{MR}$) and Output Enable ($\overline{OE}$) for initializing the internal registers and allowing the data outputs to be 3-stated. Input Ready (IR) and Output Ready (OR) signal when the FIFO is ready for I/O operations.

The FIFO can be expanded to increase the depth by cascading or provide different word lengths by tying off unused data inputs.

- **64-Words by 9-Bit Dual Port RAM Organization**
- **85 MHz Shift-In, 60 MHz Shift-Out Data Rate with Flags, Typical**
- **Expandable in Word Depth and Width Dimensions**
- **'ACT723 has TTL-Compatible Inputs**
- **Asychronous or Synchronous Operation**
- **Asynchronous Master Reset**
- **Outputs Sink/Source 8 mA**
- **3-State Outputs**
- **Full ESD Protection**
- **Output and Input Pins Directly in Line for Easy Board Layout**
- **TRW 1030 Work-Alike* Operation**

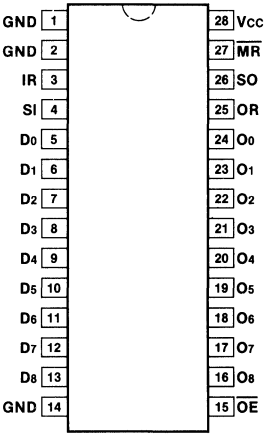
Applications

- **High-Speed Disk or Tape Controllers**
- **A/D Output Buffers**
- **High-Speed Graphics Pixel Buffer**
- **Video Time Base Correction**
- **Digital Filtering**

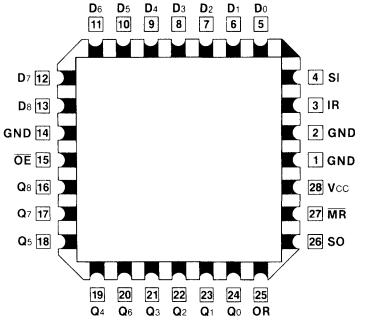
Ordering Code: See Section 6

*The TRW1030 has data setup and hold times with respect to the rising edge of SI. The 'AC/'ACT723 has data setup and hold times with respect to the falling edge of SI.

Connection Diagrams

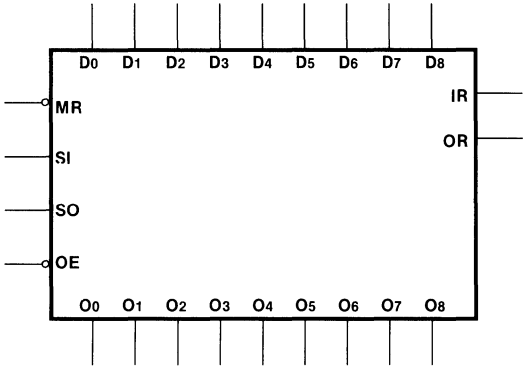


Pin Assignment for DIP and Flatpak



Pin Assignment for LCC and PCC

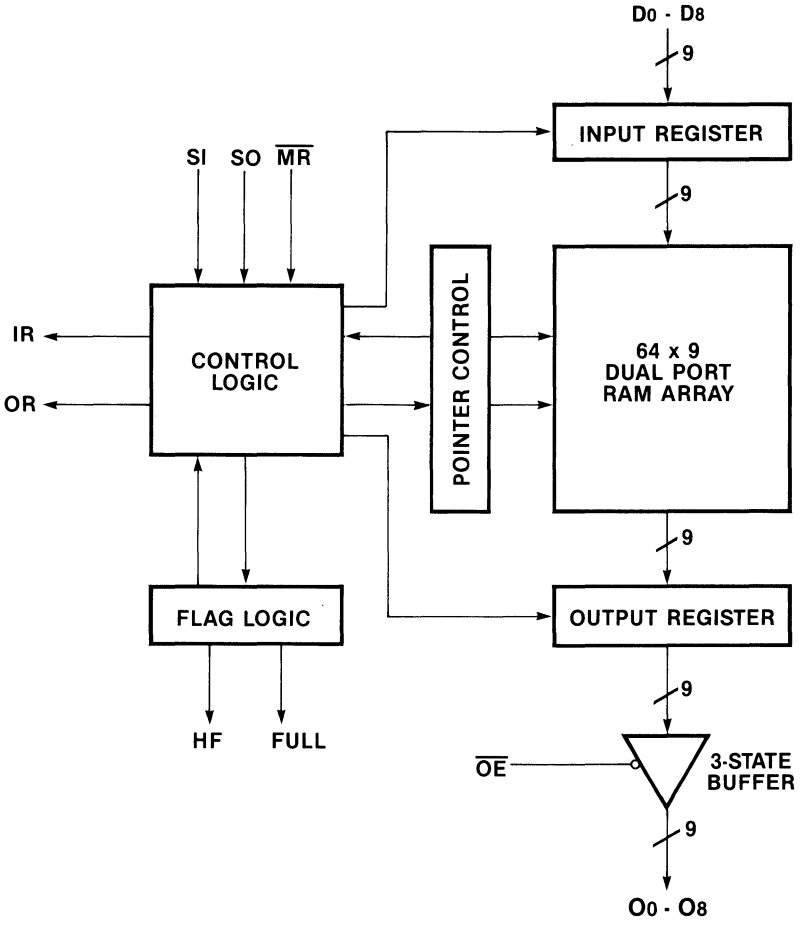
Logic Symbol



Pin Names

D_0 - D_8	Data Inputs
$\overline{MR}$	Master Reset
$\overline{OE}$	Output Enable Input
SI	Shift-In
SO	Shift-Out
IR	Input Ready
OR	Output Ready
O_0 - O_8	Data Outputs

Block Diagram



5

Functional Description

Inputs

Data Inputs (D_0 - D_8)
Data inputs for 9-bit wide data are TTL-compatible ('ACT723). Word width can be reduced by tying unused inputs to ground and leaving the corresponding outputs open.

Reset ($\overline{MR}$)
Reset is accomplished by pulsing the $\overline{MR}$ input LOW. During normal operation $\overline{MR}$ is HIGH. A reset is required after power up to guarantee correct operation. On reset, the data outputs go LOW, IR goes HIGH, and OR goes LOW. During reset, both internal read and write pointers are set to the first location in the array.

Shift-In (SI)
Data is written into the FIFO by pulsing SI HIGH. When Shift-In goes HIGH, the data is loaded into and internal data latch. Data setup and hold times need to be adhered to with respect to the falling edge of SI. The write cycle is complete after the falling edge of SI. The shift-in is independent of any ongoing shift-out operation.

When the FIFO is empty and $\overline{OE}$ is LOW, the falling edge of the first SI will cause the first data word just shifted-in to appear at the output, even though SO may be LOW.

Shift-Out (SO)
Data is read from the FIFO by the Shift-Out signal provided the FIFO is not empty. SO going HIGH causes OR to go LOW indicating that output stage is busy. On the falling edge of SO, new data reaches the output after propagation delay t_D. If the last data has been shifted-out of the memory, OR continues to remain LOW, and the last word shifted-out remains on the output pins.

Output Enable ($\overline{OE}$)
$\overline{OE}$ LOW enables the 3-state output buffers. When $\overline{OE}$ is HIGH, the outputs are in a 3-state mode.

Outputs

Data Outputs (O_0 - O_8)
Data outputs are enabled when $\overline{OE}$ is LOW and in the 3-state condition when $\overline{OE}$ is HIGH.

Input Ready (IR)
IR HIGH indicates data can be shifted-in. When SI goes HIGH, IR goes LOW, indicating input stage is busy. IR stays LOW when the FIFO is full and goes HIGH after the falling edge of the first shift-out.

Output Ready (OR)
OR HIGH indicates data can be shifted-out from the FIFO. When SO goes HIGH, OR goes LOW, indicating output stage is busy. OR is LOW when the FIFO is reset or when there is no valid data and goes HIGH after the falling edge of the first shift-in.

Reset Truth Table

Inputs			Outputs		
$\overline{MR}$	SI	SO	IR	OR	O_0 - O_8
1	X	X	X	X	X
0	X	X	1	0	0

Modes of Operation

Mode 1: Shift-In Sequence for FIFO Empty to Full

Sequence of Operation

1. Input ready is initially HIGH; the FIFO is empty and prepared for valid data. OR is LOW indicating that the FIFO is not yet ready to output data. Assume Shift-Out is LOW for this mode.

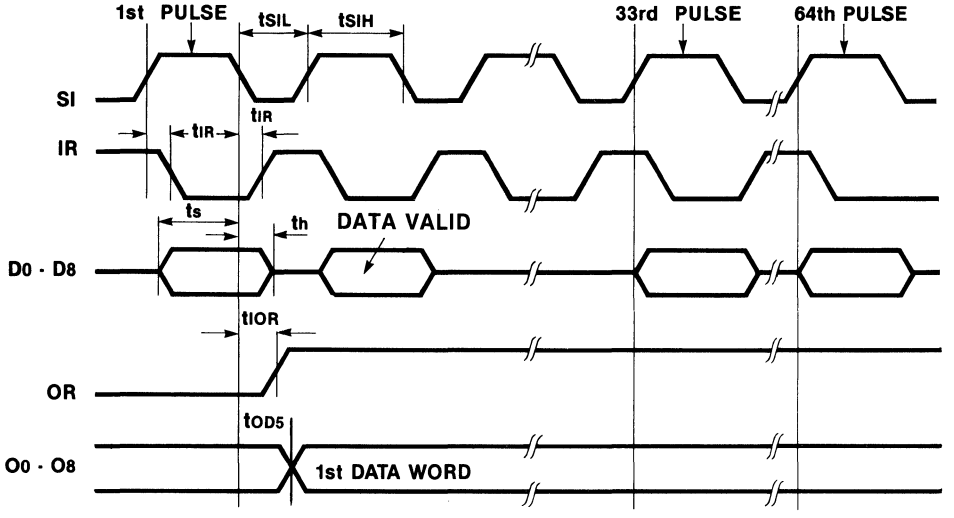
2. Shift-In is set HIGH, and data is loaded into the FIFO. Data has to be settled setup time t_S before the falling edge of SI and held hold time t_H after.

3. Input Ready (IR) goes LOW propagation delay t_{IR} after SI goes HIGH; input stage is busy.

4. Shift-In is set LOW; IR goes HIGH indicating the FIFO is ready for additional data. Data just shifted in arrives at output propagation delay t_{OD5} after SI falls. OR goes HIGH propagation delay t_{IOR} after SI goes LOW, indicating the FIFO has valid data on its outputs.

5. The process is repeated through the 64th data word. IR goes LOW on the falling edge of the 64th SI and remains LOW indicating a full FIFO. Any further shift-ins are disabled.

Figure 1: Modes of Operation
Mode 1



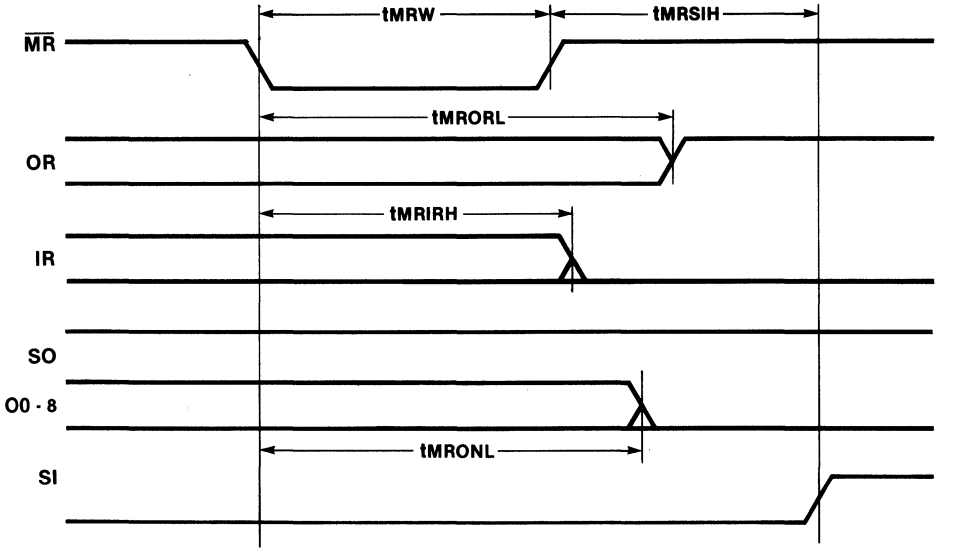
Note: SO and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH.

Mode 2: Master Reset

Sequence of Operation

1. Input and Output Ready can be in any state before the reset sequence with Master Reset HIGH ($\overline{MR}$).
2. Master Reset goes LOW and clears the FIFO, setting up all essential internal states. Master Reset must be LOW pulse width t_{MRW} before rising again.
3. Master Reset rises.
4. IR rises (if not HIGH already) to indicate ready to write state recovery time t_{MRIRH} after the falling edge of $\overline{MR}$. OR falls recovery time t_{MRORL} after $\overline{MR}$ falls. Data at outputs goes LOW recovery time t_{MRONL} after $\overline{MR}$ goes LOW.
5. Shift-In must be delayed a minimum of recovery time t_{MRSIH}.

Figure 2: Modes of Operation Mode 2

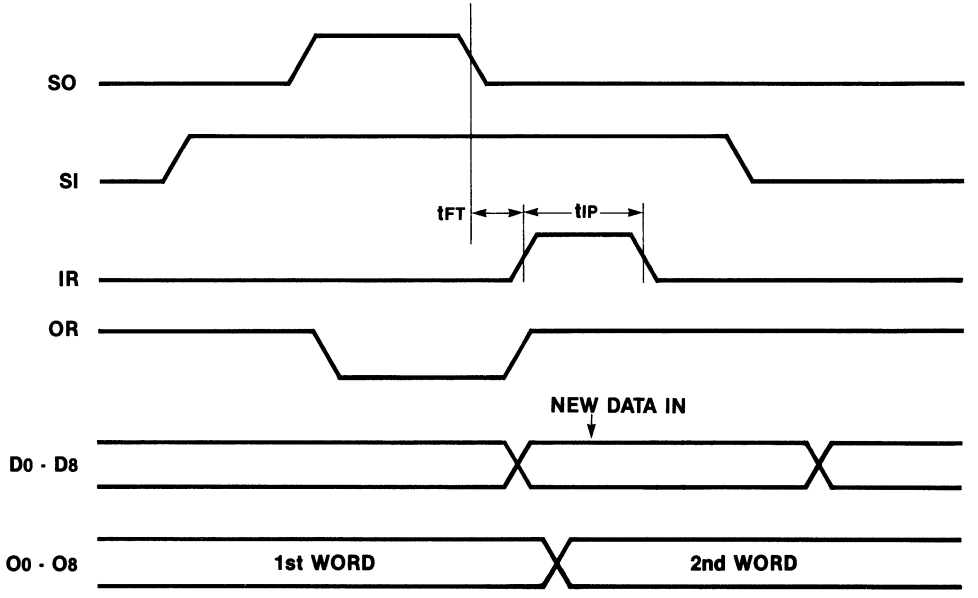


Mode 3: With FIFO Full, Shift-In is Held HIGH in Anticipation of an Empty Location

Sequence of Operation

1. The FIFO is initially full and Shift-In goes HIGH. OR is initially HIGH. IR and SO are LOW.
2. Shift-Out is pulsed HIGH, Shift-Out pulse propagates and the first data word is latched on the rising edge of SO. OR falls on this edge. On the falling edge of SO, the second data word appears after OR propagation delay t_D.
3. Input Ready goes HIGH fall-through time t_{FT} after the falling edge of SO.
4. IR returns LOW pulse width t_{IP} after rising and shifting fresh data in.
5. Shift-In is brought LOW to complete the shift process and maintain normal operation.

Figure 3: Modes of Operation
Mode 3



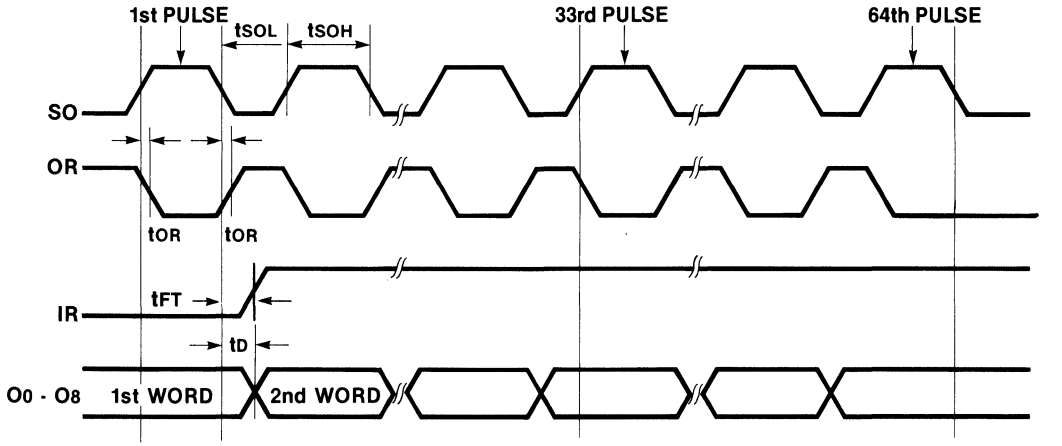
Note: $\overline{MR}$ is HIGH; $\overline{OE}$ is LOW.

Mode 4: Shift-Out Sequence, FIFO Full to Empty

Sequence of Operation

1. FIFO is initially full and OR is HIGH, indicating valid data is at the output. IR is LOW.
2. SO goes HIGH, resulting in OR going LOW propagation delay t_{OR} after SO rises. OR LOW indicates output stage is busy.
3. SO goes LOW, new data reaches output propagation delay t_D after SO falls; OR goes HIGH propagation delay t_{OR} after SO falls, IR rises fall-through time t_{FT} after SO falls.
4. Repeat process through the 64th SO pulse. OR stays LOW after 64th SO indicating an empty FIFO. The SO pulse may rise and fall again with an attempt to unload an empty FIFO. This results in no change in the data on the outputs as the 64th word stays latched.

Figure 4: Modes of Operation
Mode 4



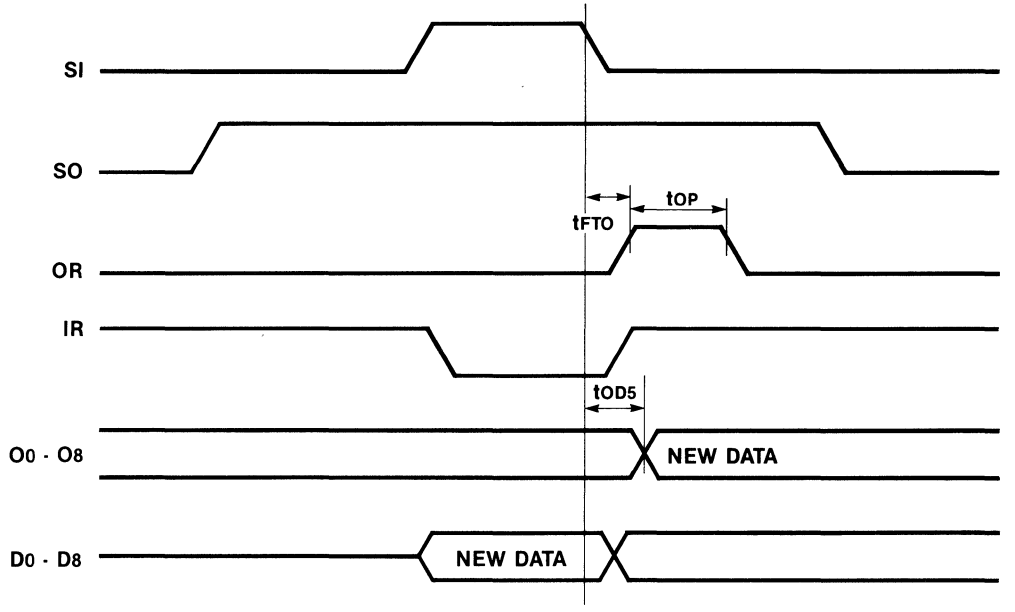
Note: SI and $\overline{OE}$ are LOW; $\overline{MR}$ is HIGH; D_0 - D_8 are immaterial.

Mode 5: With FIFO Empty, Shift-Out is Held HIGH in Anticipation of Data

Sequence of Operation

1. FIFO is initially empty; Shift-Out goes HIGH. IR is HIGH; OR is LOW.
2. Shift-In pulse HIGH loads data into the FIFO and IR falls.
3. OR rises fall through time t_{FTO} after the falling edge of Shift-In, indicating that new data is ready to be output.
4. Data arrives at output propagation delay t_{OD5} after the falling edge of Shift-In.
5. OR goes LOW pulse width t_{OP} after rising, indicating that the FIFO is empty once more.
6. Shift-Out goes LOW, necessary to complete the Shift-Out process.

Figure 5: Modes of Operation
Mode 5



Note: $\overline{MR}$ is HIGH; $\overline{OE}$ is LOW; $t_{DOF} = t_{FTO} - t_{OD5}$ — data output transition, valid data arrives at output stage t_{DOF} after OR is HIGH.

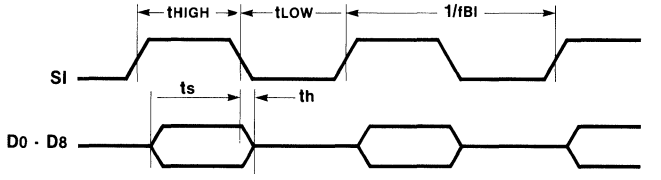
Mode 6: Shift-In Operation in High-Speed Burst Mode

Sequence of Operation

1. Shift-In goes HIGH, loading data into the FIFO. IR is ignored.
2. Shift-in goes LOW pulse width t_{HIGH} time later; loading is complete.
3. Shift-In rises again for the second load pulse width t_{LOW} after the falling edge.

The burst-in rate is determined by SI HIGH and LOW. Data is shifted-in ignoring the IR flag. Any SI after the FIFO is filled up will be ignored.

Figure 6: Modes of Operation Mode 6



Note: $\overline{MR}$ is HIGH; $t_{HIGH} > t_{SIH}$; $t_{LOW} > t_{SIL}$; $t_{HIGH} + t_{LOW} > 1/f_{BI}$.

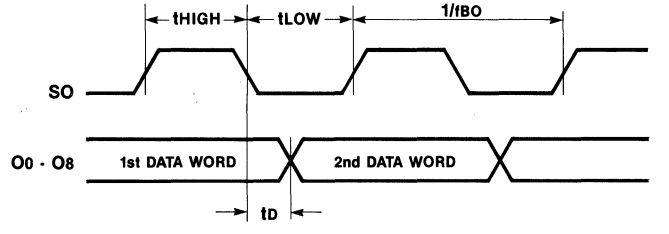
Mode 7: Shift-Out Operation in High-Speed Burst Mode

Sequence of Operations

1. Shift-Out is LOW; valid data is available on output with OR ignored.
2. Shift-Out rises; data out is latched.
3. Shift-Out falls pulse width time t_{HIGH} after rise Shift-Out is complete; new data is loaded onto output.

The burst-out rate is determined by SO HIGH and LOW. The OR flag is ignored.

Figure 7: Modes of Operation Mode 7



Note: $\overline{OE}$ is LOW; $\overline{MR}$ is HIGH; $t_{HIGH} > t_{SOH}$; $t_{LOW} > t_{SOL}$; $t_{HIGH} + t_{LOW} > 1/f_{BO}$.

FIFO Expansion

Word Width Expansion

Word width can be increased by connecting the corresponding input control signals of multiple devices. Flags can be monitored on any one device (Figure 8), or composite flag signals can be achieved by ANDing the corresponding flags.

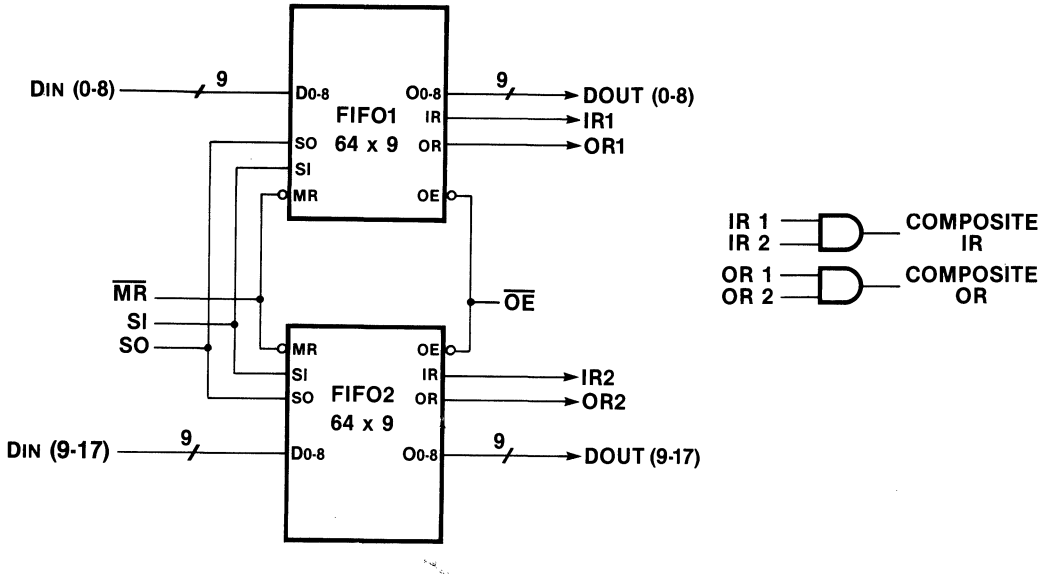
Depth Expansion

Depth expansion can be achieved by connecting as shown in Figure 9. No external circuitry is required for handshaking, which is achieved by the internal FIFO signals IR and OR.

When n FIFOs are cascaded to attain a 64n word FIFO, the SI signal is connected to the first FIFO and the SO signal to the nth FIFO. The IR and OR signals are monitored from the first and last FIFOs respectively. The IR signal from each FIFO is connected to its preceding SO signal: IR(n)→SO(n-1); IR(n-1)→SO(n-2) . . . IR(2)→SO(1). The OR signal from each FIFO is connected to its succeeding SI signal: i.e., OR(1)→SI(2); OR(2)→SI(3) . . . OR(n-1)→SI(n). Handshaking signals are shown in Figure 10.

FIFO 1 operates in Mode 5 during SI until FIFO2 is filled. FIFO2 operates in Mode 3 during SO until FIFO1 is empty. Data from FIFO1 is written into FIFO2 after a word is read from FIFO2. To achieve this, the $\overline{OE}$ pin is grounded for FIFO1. In general, for n FIFOs, all $\overline{OE}$ pins but the nth FIFO's $\overline{OE}$ pin are enabled. 3-state control of the outputs can then be achieved by controlling the nth FIFO's $\overline{OE}$ pin.

Figure 8: Word Width Expansion — 64 x 18 FIFO



Note: Monitor flags from any one FIFO or AND the corresponding flags to obtain a composite signal.

Figure 9: Depth Expansion Mode — 128 x 9 FIFO

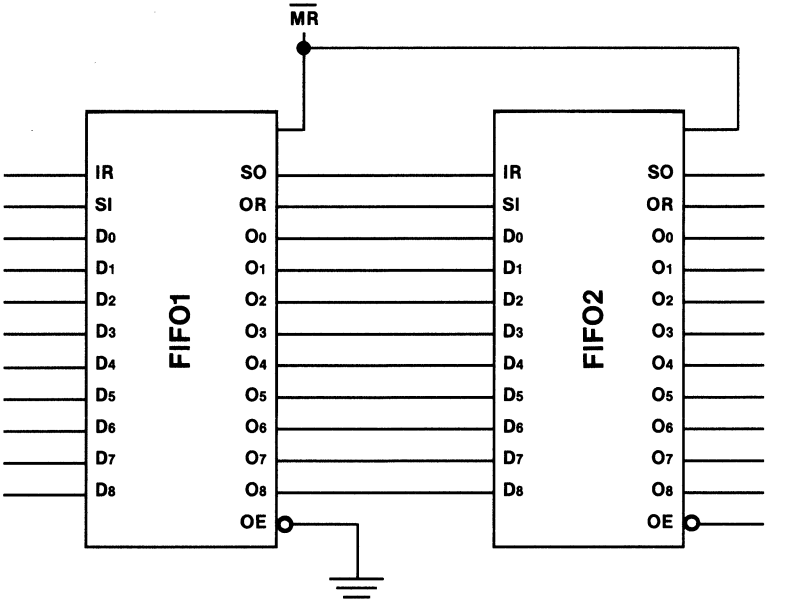
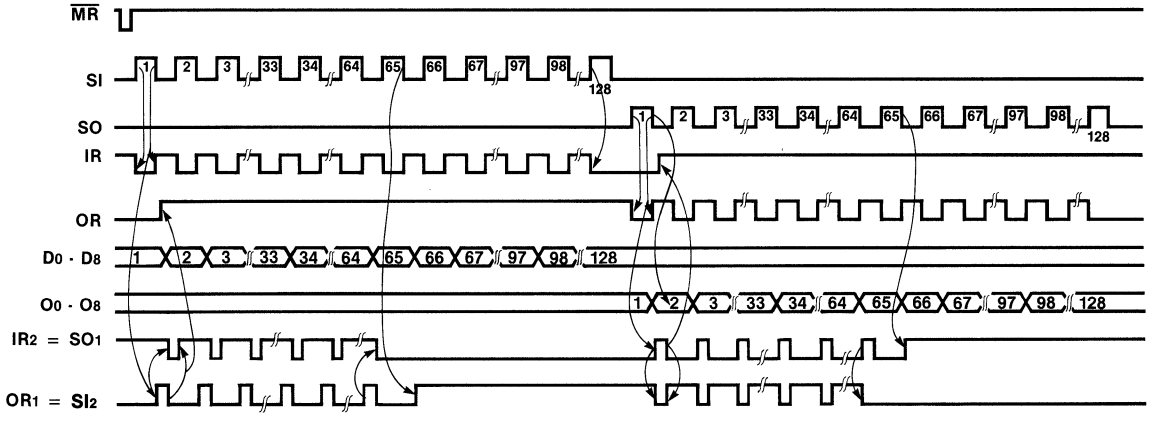


Figure 10: Handshaking for Depth Expansion Mode — 128 x 9 FIFO



Note: The numbers for SI and SO indicate the pulse numbers. The numbers for data in and data out indicate data words: 1 is the first data word, 2 is the second data word, etc.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74AC/ACT 25°C	54AC/ACT	74AC/ACT	Units	Conditions
		Typ	Guaranteed Limit			
I_{IN}	Maximum Input Current		0.1	10.0	1.0	μA	V_{CC} = Max V_{IN} = V_{CC}
I_{OZ}	Maximum 3-State Current		0.5	10.0	5.0	μA	High Z, V_{CC} = Max V_{OUT} = 0 to V_{CC}
I_{CCQ}	Supply Current, Quiescent	50.0	2.0	10.0	10.0	mA	V_{CC} = Max, V_{IN} = 0 V
I_{CCD}	Supply Current, 20 MHz Loaded	325		150	150	mA	V_{CC} = Max, f = 20 MHz Test Load: See Note 1
V_{OH}	Minimum HIGH Level Output	4.49	4.4	4.4	4.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		5.49	5.4	5.4	5.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			3.86	3.70	3.76	V	I_{OH} = −8 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = −8 mA, V_{CC} = 5.5 V
V_{OL}	Maximum HIGH Level Output	0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 4.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 5.5 V
I_{OLD}	Minimum Dynamic Output Current			32	32	mA	V_{CC} = 5.5 V V_{OLD} = 2.2 V
I_{OHD}	Minimum Dynamic Output Current			−32	−32	mA	V_{CC} = 5.5 V V_{OHD} = 3.3 V

Note 1: Test Load 50 pF, 500 ohm to Ground

5

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PHL}	Propagation Delay, t_{IR} SI to IR	3.3 5.0		8.5 5.5						ns	1
t_{PLH}	Propagation Delay, t_{IOR} SI to OR	3.3 5.0		13.0 9.5						ns	1
t_{PHL}, t_{PLH}	Propagation Delay, t_D SO to Data Out	3.3 5.0		23.0 17.0						ns	4
t_{PLH}, t_{PHL}	Propagation Delay, t_{OR} SO to OR	3.3 5.0		9.5 7.0						ns	4
t_{PHL}, t_{PLH}	Propagation Delay, t_{OD5} SI to New Data Out	3.3 5.0		22.0 16.0						ns	1, 5
t_{PLH}	Fall-Through Time, t_{FTO} SI to OR	3.3 5.0		16.0 11.5						ns	5
t_{PLH}	Fall-Through Time, t_{FT} SO to IR, HIGH	3.3 5.0		18.5 13.5						ns	3
t_{PZL}	Output Enable $\overline{OE}$ to On	3.3 5.0		7.5 5.5						ns	3-8
t_{PLZ}	Output Disable $\overline{OE}$ to On	3.3 5.0		6.0 4.5						ns	3-8
t_{PZH}	Output Enable $\overline{OE}$ to On	3.3 5.0		9.0 6.5						ns	3-7
t_{PHZ}	Output Disable $\overline{OE}$ to On	3.3 5.0		9.0 6.5						ns	3-7
t_{rec}	Recovery Time, t_{MRIRH} $\overline{MR}$ to IR	3.3 5.0		9.5 7.0						ns	2
t_{rec}	Recovery Time, t_{MRORL} $\overline{MR}$ to OR	3.3 5.0		20.0 15.0						ns	2
t_{rec}	Recovery Time, t_{MRONL} $\overline{MR}$ to On, LOW	3.3 5.0		11.0 8.0						ns	2
t_w	IR Pulse Width, t_{IP}	3.3 5.0		38.0 28.0						ns	3
t_w	OR Pulse Width, t_{OP}	3.3 5.0		23.0 17.0						ns	5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics, cont'd

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{SI}	Maximum SI Clock Frequency	3.3 5.0		60 85						MHz	1
f_{SO}	Maximum SO Clock Frequency	3.3 5.0		50 60						MHz	4
f_{BO}	Maximum Clock Frequency, SO Burst Mode	3.3 5.0		55 65						MHz	7
f_{BI}	Maximum Burst In Clock	3.3 5.0		60 85						MHz	6

*Voltage Range 3.3 is 3.3 V. ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_w	SI Pulse Width, t_{SIH} HIGH	3.3 5.0	4.0 1.5				ns	1, 6
t_w	SI Pulse Width, t_{SIL} LOW	3.3 5.0	4.0 1.5				ns	1, 6
t_s	Setup Time, HIGH or LOW, D_n to SI	3.3 5.0	2.0 1.0				ns	1
t_h	Hold Time, HIGH or LOW, D_n to SI	3.3 5.0	3.0 1.5				ns	1
t_w	$\overline{MR}$ Pulse Width, t_{MRW}	3.3 5.0	17.0 13.0				ns	2
t_{rec}	Recovery Time, t_{MRSIH} $\overline{MR}$ to SI	3.3 5.0	7.0 4.0				ns	2
t_w	SO Pulse Width, t_{SOH} HIGH	3.3 5.0	4.5 2.0				ns	4, 7
t_w	SO Pulse Width, t_{SOL} LOW	3.3 5.0	12.5 9.0				ns	4, 7

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}, t_{PLH}	Propagation Delay, t_{IR} SI to IR	5.0		6.5						ns	1
t_{PLH}	Propagation Delay, t_{IOR} SI to OR	5.0		10.5						ns	1
t_{PHL}, t_{PLH}	Propagation Delay, t_D SO to Data Out	5.0		18.5						ns	4
t_{PHL}, t_{PHL}	Propagation Delay, t_{OR} SO to OR	5.0		7.0						ns	4
t_{PHL}, t_{PLH}	Propagation Delay, t_{OD5} SI to New Data Out	5.0		19.0						ns	1, 5
t_{PLH}	Fall-Through Time, t_{FTO} SI to OR	5.0		13.5						ns	5
t_{PLH}	Fall-Through Time, t_{FT} SO to IR, HIGH	5.0		15.0						ns	3
t_{PZL}	Output Enable $\overline{OE}$ to O_n	5.0		6.5						ns	3-8
t_{PLZ}	Output Disable $\overline{OE}$ to O_n	5.0		5.0						ns	3-8
t_{PZH}	Output Enable $\overline{OE}$ to O_n	5.0		6.5						ns	3-7
t_{PHZ}	Output Disable $\overline{OE}$ to O_n	5.0		6.5						ns	3-7
t_{rec}	Recovery Time, t_{MRIRH} $\overline{MR}$ to IR	5.0		8.5						ns	2
t_{rec}	Recovery Time, t_{MRORL} $\overline{MR}$ to OR	5.0		16.5						ns	2
t_{rec}	Recovery Time, t_{MRONL} $\overline{MR}$ to O_n, LOW	5.0		9.0						ns	2
t_w	IR Pulse Width, t_{IP}	5.0		28.0						ns	3
t_w	OR Pulse Width, t_{OP}	5.0		17.0						ns	5
f_{SI}	Maximum SI Clock Frequency	5.0		85						MHz	1
f_{SO}	Maximum SO Clock Frequency	5.0		60						MHz	4

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics, cont'd

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{BO}	Maximum Clock Frequency, SO Burst Mode	5.0		65						MHz	7
f_{BI}	Maximum Burst In Clock	5.0		85						MHz	6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_w	SI Pulse Width, t_{SIH} HIGH	5.0	1.5				ns	1, 6
t_w	SI Pulse Width, t_{SIL} LOW	5.0	1.5				ns	1, 6
t_s	Setup Time, HIGH or LOW, D_n to SI	5.0	1.0				ns	1
t_h	Hold Time, HIGH or LOW, D_n to SI	5.0	1.5				ns	1
t_w	$\overline{MR}$ Pulse Width, t_{MRW}	5.0	13.0				ns	2
t_{rec}	Recovery Time, t_{MRSIH} $\overline{MR}$ to SI	5.0	4.5				ns	2
t_w	SO Pulse Width, t_{SOH} HIGH	5.0	2.0				ns	4, 7
t_w	SO Pulse Width, t_{SOL} LOW	5.0	9.0				ns	4, 7

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representatve.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V

54AC/74AC725 • 54ACT/74ACT725

512 x 9 First-In, First-Out Memory (FIFO)

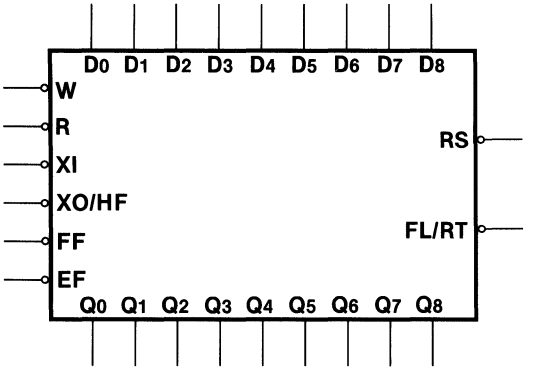
Description

The 512 x 9 FIFO is a first-in, first-out dual port memory capable of asynchronous, simultaneous read and write. Other important features are: expansion capability in both the word depth and bit width, half-full flag capability in the single device mode, empty and full warning flags, ring pointers for zero fall-through time; it is suited for high-speed applications.

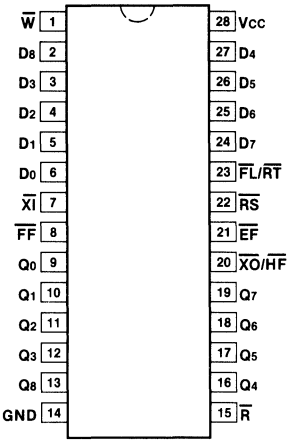
- **First-In, First-Out Dual Port Memory**
- **512 x 9 Organization**
- **Low Power Consumption**
- **Asynchronous and Simultaneous Read and Write**
- **Fully Expandable by Word Depth and/or Bit Width**
- **Half-Full Flag Capability in Single Device Mode**
- **Master/Slave Multiprocessing Applications**
- **Bidirectional and Rate Buffer Applications**
- **Empty and Full Warning Flags**
- **Auto Retransmit Capability**
- **Outputs Source/Sink 8 mA**
- **'ACT725 has TTL-Compatible Inputs**
- **Pin and Functionally Compatible with IDT7201**
- **35 MHz Read; Write-Read Capability**

Ordering Code: See Section 6

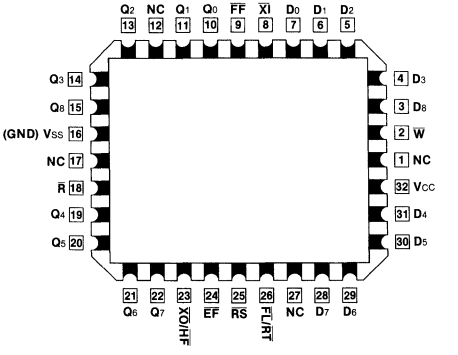
Logic Symbol



Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC

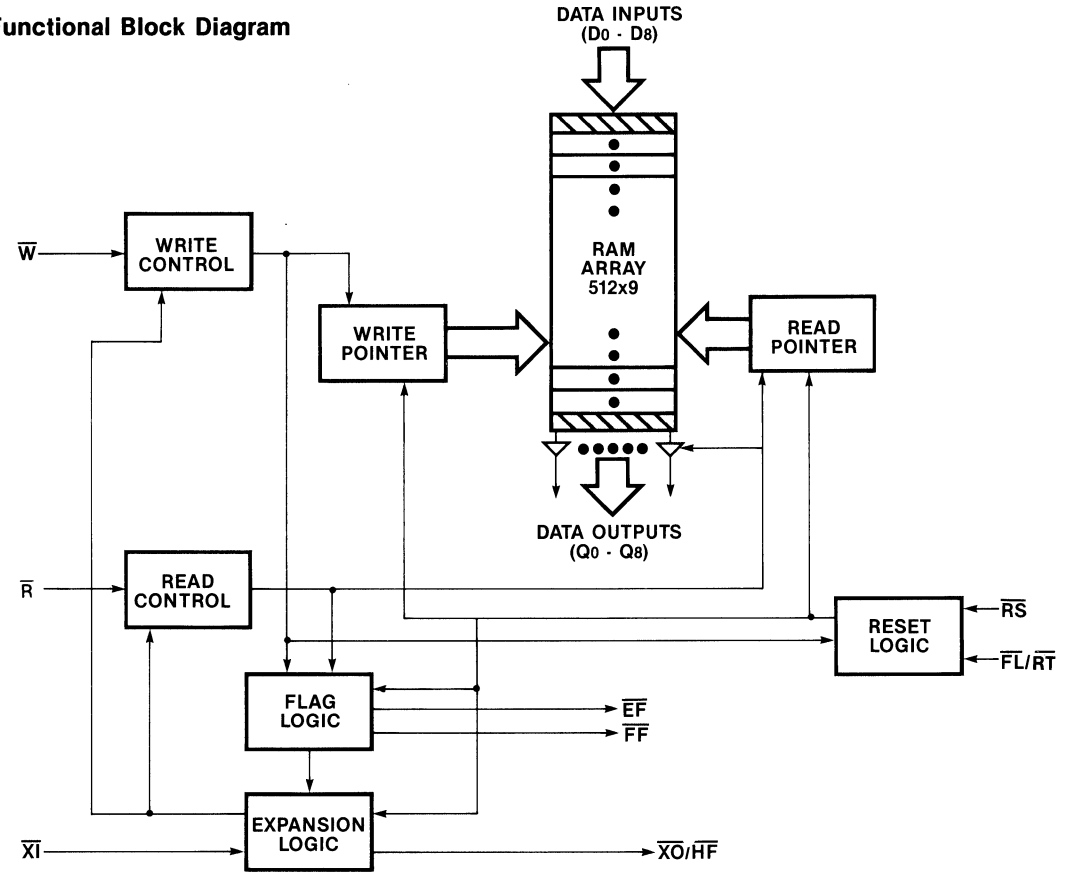


Pin Assignment for LCC and PCC

Pin Names

D0 - D8	Data Inputs
Q0 - Q8	Data Outputs
$\overline{W}$	Write Enable
$\overline{R}$	Read Enable
$\overline{XI}$	Expansion In
$\overline{XO/HF}$	Expansion Out, Half-Full Flag
$\overline{EF}$	Empty Flag
$\overline{FF}$	Full Flag
$\overline{RS}$	Reset
$\overline{FL/RT}$	First Load/Retransmit

Functional Block Diagram



Functional Description

The 'AC/'ACT725 is a dual port memory which loads and empties data on a first-in, first-out basis. The device uses full and empty flags to prevent data overflow and underflow. Expansion logic allows for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins.

The device employs a 9-bit wide data array for control and parity bits which are under the control of the user. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. It also features a RETRANSMIT ($\overline{RT}$) capability; the read pointer is reset to its initial position when $\overline{RT}$ is pulsed LOW to allow for retransmission from the beginning of data. A half-full flag is available in the single device mode and width expansion modes.

The 'AC/'ACT725 is ideal for those applications which require asynchronous and simultaneous read/writes in multiprocessing and rate buffer applications.

Signal Descriptions

Inputs

Data In (D_0 - D_8)
Data inputs for 9-bit wide data.

Controls

Reset ($\overline{RS}$)
When the Reset ($\overline{RS}$) input is taken LOW, a reset is accomplished. During reset, both internal read and write pointers are set to the first location. A reset is required upon power up before a write operation can take place. Both the Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) inputs must be HIGH during reset. Half-Full Flag ($\overline{HF}$) will be reset to HIGH after Master Reset ($\overline{RS}$).

Write Enable ($\overline{W}$)
A write cycle is initiated on the falling edge of $\overline{W}$ when a Full Flag ($\overline{FF}$) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the Write Enable ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When half of the memory is filled and the falling edge of the next write operation occurs, the Half-Full Flag ($\overline{HF}$) will be set to LOW and will remain LOW until the difference between the write pointer and the read pointer is less than or equal to one-half of the total memory of the device. $\overline{HF}$ is then reset by the rising edge of the read operation.

To prevent data overflow, $\overline{FF}$ will go LOW, inhibiting further write operations. Upon the completion of a valid read operation, $\overline{FF}$ will go HIGH after t_{RFF}, allowing a valid write to begin.

Read Enable ($\overline{R}$)
A read cycle is initiated on the falling edge of Read Enable ($\overline{R}$) if the Empty Flag ($\overline{EF}$) is not set. The data is accessed on a first-in, first-out basis; it is independent of any ongoing write operations. After $\overline{R}$ goes HIGH, the data outputs (Q_0 - Q_8) return to a high impedance condition until the next read operation. When all data has been read from the FIFO, $\overline{EF}$ will go LOW and inhibit further read operations; the data outputs remain in a high impedance state. Upon completing a valid write operation, $\overline{EF}$ will go HIGH after t_{WEF}, and a valid read can then begin.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)
This is a dual purpose output. In the multiple device mode, $\overline{FL}/\overline{RT}$ is grounded, indicating it is the first device loaded.

In the single device mode, this pin acts as the retransmit input. The single device mode is initiated by grounding the Expansion In ($\overline{XI}$).

The 'AC/'ACT725 can retransmit data when the Retransmit Enable control ($\overline{RT}$) input is pulsed LOW. A retransmit operation sets the internal read pointer to the first location and will not affect the write pointer. $\overline{R}$ and $\overline{W}$ must be HIGH during retransmit. Retransmit is useful when less than 512 writes are performed between resets. The retransmit feature is not compatible with Depth Expansion mode; it will affect $\overline{HF}$ depending on the relative locations of the read and write pointers.

Expansion In ($\overline{XI}$)
$\overline{XI}$ is a dual purpose input. Expansion In ($\overline{XI}$) is grounded to indicate an operation in the single device mode. $\overline{XI}$ is connected to Expansion Out ($\overline{XO}$) of the previous device in the Depth Expansion or Daisy Chain mode.

Outputs

Full Flag ($\overline{FF}$)
If brought LOW, the Full Flag ($\overline{FF}$) will inhibit further write operation when the write pointer is one location from the read pointer; the device is full. If the read pointer is not moved after $\overline{RS}$, $\overline{FF}$ will go LOW after 512 writes.

Expansion Out/Half Full Flag ($\overline{XO}/\overline{HF}$)
This is a dual purpose output. In the single device mode, when $\overline{XI}$ is grounded, $\overline{XO}/\overline{HF}$ acts as an indicator of a half-full memory.

When half of the memory is filled, on the falling edge of the next write operation, $\overline{HF}$ will be set LOW and will remain set until the difference between the write pointer and the read pointer is less than or equal to one-half of the total memory of the device. $\overline{HF}$ is then reset by the rising edge of the read operation.

In the Multiple Device mode, $\overline{XI}$ is connected to Expansion Out ($\overline{XO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain; $\overline{XO}/\overline{HF}$ provides a pulse to the next device when the previous device reaches the last location of memory.

Data Outputs (Q_0 - Q_8)
Data outputs for 9-bit wide data. These outputs are in a high impedance condition whenever $\overline{R}$ is HIGH.

Truth Tables

Table 1: Reset and Transmit Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location 0	Location 0	0	1	1
Retransmit	1	0	0	Location 0	Unchanged	X	X	X
Read/Write	1	1	0	Increment*	Increment*	X	X	X

*Pointer will increment if flag is HIGH

Table 2: Reset and First Load Truth Table Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset First Device	0	0	*	Location 0	Location 0	0	1
Reset All Other Devices	0	0	*	Location 0	Location 0	0	1
Read/Write	1	X	*	X	X	X	X

*$\overline{XI}$ is connected to $\overline{XO}$ of previous device (see Figure 12)
$\overline{RS}$ = Reset input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag output, $\overline{FF}$ = Full Flag output, $\overline{XI}$ = Expansion input, $\overline{HF}$ = Half-Full Flag input

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DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74AC/ACT 25°C	54AC/ACT	74AC/ACT	Units	Conditions
		Typ	Guaranteed Limit			
I_{IN}	Maximum Input Current		0.1	10.0	1.0	μA	V_{CC} = Max V_{IN} = V_{CC}
I_{OZ}	Maximum 3-State Current		0.5	10.0	5.0	μA	High Z, V_{CC} = Max V_{OUT} = 0 to V_{CC}
I_{CCQ}	Supply Current, Quiescent	50.0	2.0	10.0	10.0	mA	V_{CC} = Max, V_{IN} = 0 V
V_{OH}	Minimum HIGH Level Output	4.49	4.4	4.4	4.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		5.49	5.4	5.4	5.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			3.86	3.70	3.76	V	I_{OH} = −8 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = −8 mA, V_{CC} = 5.5 V
V_{OL}	Maximum HIGH Level Output	0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 4.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 5.5 V
I_{OLD}	Minimum Dynamic Output Current			32	32	mA	V_{CC} = 5.5 V V_{OLD} = 2.2 V
I_{OHD}	Minimum Dynamic Output Current			−32	−32	mA	V_{CC} = 5.5 V V_{OHD} = 3.3 V

Note 1: Test Load 50 pF, 500 ohm to Ground

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_A	Access Time	3.3 5.0								ns	
t_{RLZ}	Read Pulse LOW to Data Bus at Low Z	3.3 5.0								ns	
t_{WLZ}	Write Pulse HIGH to Data Bus at Low Z	3.3 5.0								ns	
t_{DV}	Data Valid from Read Pulse HIGH	3.3 5.0								ns	
t_{RHZ}	Read Pulse HIGH to Data Bus at High Z	3.3 5.0								ns	
t_{EFL}	Reset to Empty Flag LOW	3.3 5.0								ns	
t_{REF}	Read LOW to Empty Flag LOW	3.3 5.0								ns	
t_{RFF}	Read HIGH to Full Flag HIGH	3.3 5.0								ns	
t_{WEF}	Write HIGH to Empty Flag HIGH	3.3 5.0								ns	
t_{WFF}	Write LOW to Full Flag LOW	3.3 5.0								ns	
t_{WHF}	Write LOW to Half Full Flag LOW	3.3 5.0								ns	
t_{RHF}	Read HIGH to Half Full Flag HIGH	3.3 5.0								ns	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_{RC}	Read Cycle Time	3.3 5.0					ns	
t_{RR}	Read Recovery Time	3.3 5.0					ns	
t_{RPW}	Read Pulse Width	3.3 5.0					ns	
t_{WC}	Write Cycle Time	3.3 5.0					ns	
t_W	Write Pulse Width	3.3 5.0					ns	
t_{REC}	Write Recovery Time	3.3 5.0					ns	
t_S	Data Setup Time	3.3 5.0					ns	
t_H	Data Hold Time	3.3 5.0					ns	
t_{RSC}	Reset Cycle Time	3.3 5.0					ns	
t_W	Reset Pulse Width	3.3 5.0					ns	
t_{REC}	Reset Recovery Time	3.3 5.0					ns	
t_{RTC}	Retransmit Cycle Time	3.3 5.0					ns	
t_W	Retransmit Pulse Width	3.3 5.0					ns	
t_{REC}	Retransmit Recovery Time	3.3 5.0					ns	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_A	Access Time	5.0								ns	
t_{RLZ}	Read Pulse LOW to Data Bus at Low Z	5.0								ns	
t_{WLZ}	Write Pulse HIGH to Data Bus at Low Z	5.0								ns	
t_{DV}	Data Valid from Read Pulse HIGH	5.0								ns	
t_{RHZ}	Read Pulse HIGH to Data Bus at High Z	5.0								ns	
t_{EFL}	Reset to Empty Flag LOW	5.0								ns	
t_{REF}	Read LOW to Empty Flag LOW	5.0								ns	
t_{RFF}	Read HIGH to Full Flag HIGH	5.0								ns	
t_{WEF}	Write HIGH to Empty Flag HIGH	5.0								ns	
t_{WFF}	Write LOW to Full Flag LOW	5.0								ns	
t_{WHF}	Write LOW to Half Full Flag LOW	5.0								ns	
t_{RHF}	Read HIGH to Half Full Flag HIGH	5.0								ns	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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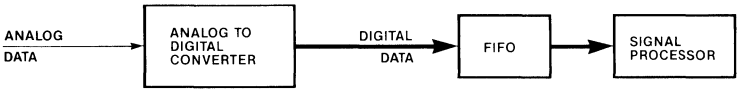
AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_{RC}	Read Cycle Time	5.0					ns	
t_{RR}	Read Recovery Time	5.0					ns	
t_{RPW}	Read Pulse Width	5.0					ns	
t_{WC}	Write Cycle Time	5.0					ns	
t_W	Write Pulse Width	5.0					ns	
t_{REC}	Write Recovery Time	5.0					ns	
t_S	Data Setup Time	5.0					ns	
t_H	Data Hold Time	5.0					ns	
t_{RSC}	Reset Cycle Time	5.0					ns	
t_W	Reset Pulse Width	5.0					ns	
t_{REC}	Reset Recovery Time	5.0					ns	
t_{RTC}	Retransmit Cycle Time	5.0					ns	
t_W	Retransmit Pulse Width	5.0					ns	
t_{REC}	Retransmit Recovery Time	5.0					ns	

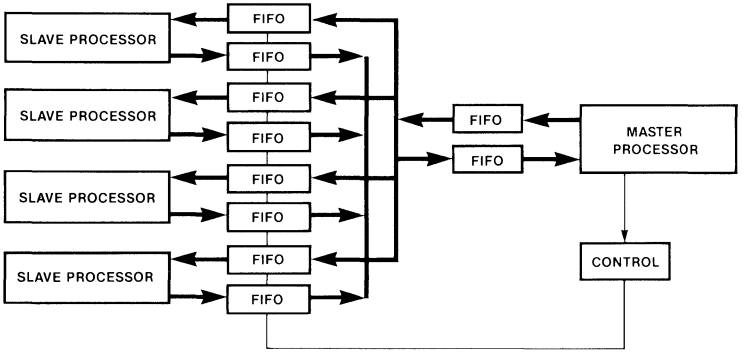
*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Figure 1

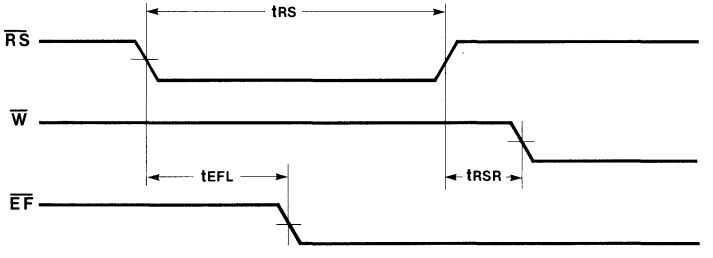


a: Typical Application — Signal Processing System



b: Typical Application — High-Speed Multiprocessing System

Figure 2: Reset



Notes: $t_{RSC} = t_{RS} + t_{RSR}$
$\overline{W}$ and $\overline{R}$ = V_{IH} during RESET

Figure 3: Asynchronous Write and Read Operation

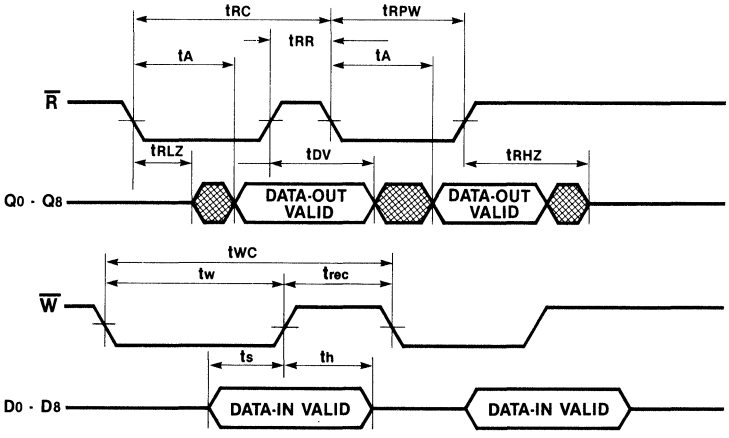


Figure 4: Full Flag from Last Write to First Read

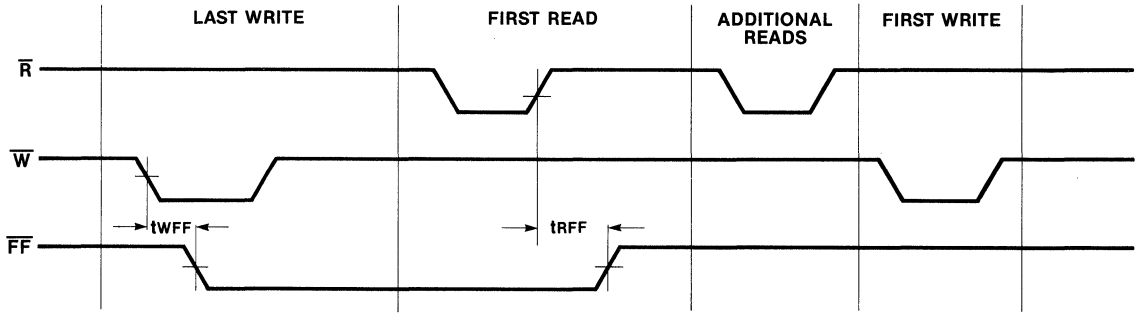


Figure 5: Empty Flag from Last Read to First Write

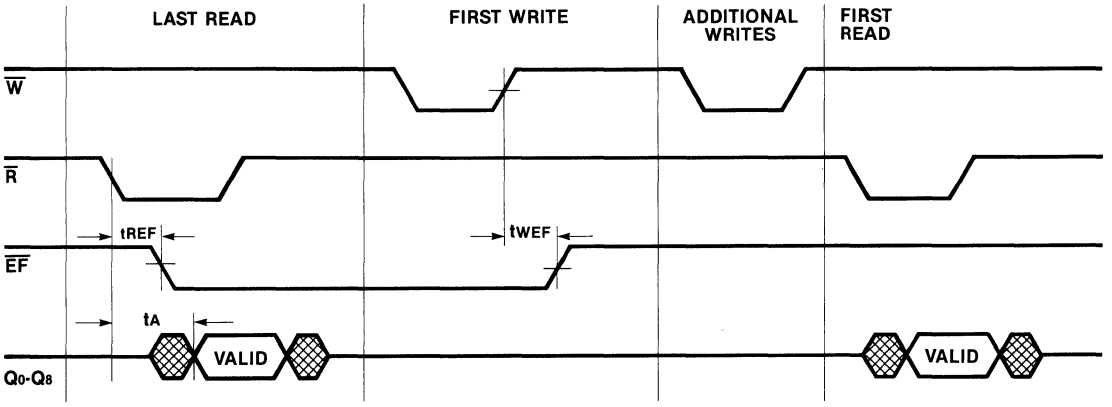
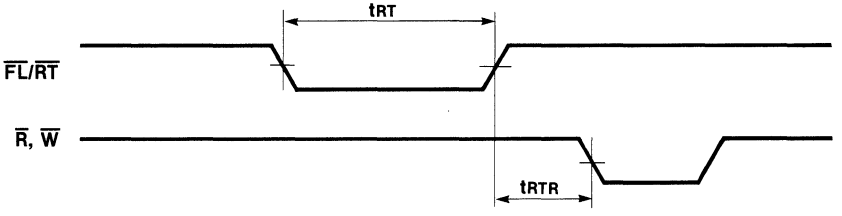


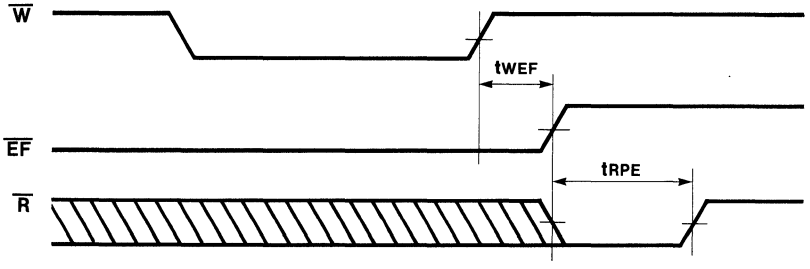
Figure 6: Retransmit



Notes: $t_{RTC} = t_{RT} + t_{RTR}$

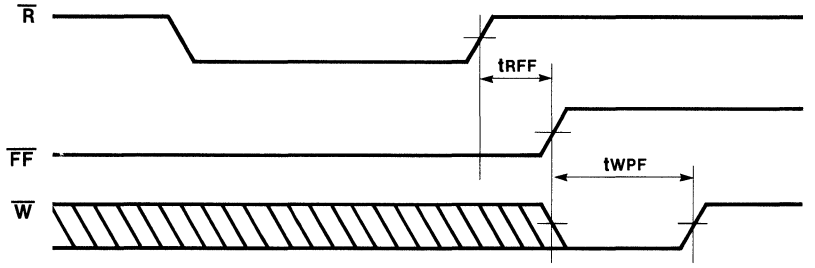
EF/HF may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}.

Figure 7: Empty Flag Timing



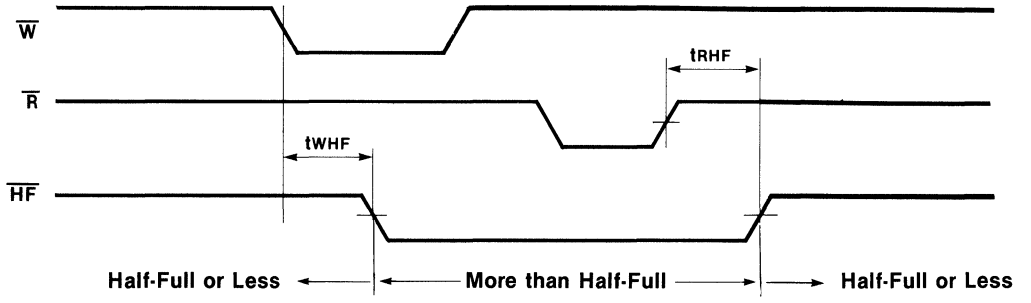
Note: $t_{RPE} = t_{RPW}$

Figure 8: Full Flag Timing



Note: $t_{WPF} = t_{WPW}$

Figure 9: Half-Full Flag Timing

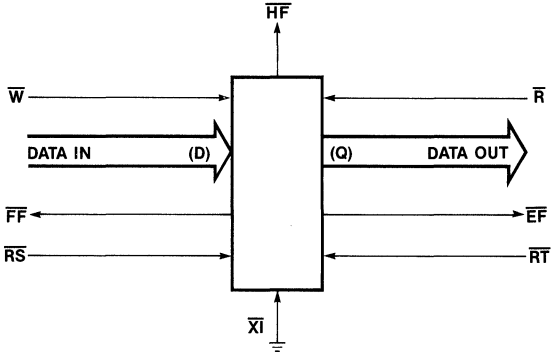


Operating Modes

Single Device Mode
A single 'AC/'ACT725 device may be utilized for applications requiring 512 words or less. The 'AC/'ACT725 is in a single device configuration when Expansion In ($\overline{XI}$) is grounded. In this mode, $\overline{HF}$ flag is valid.

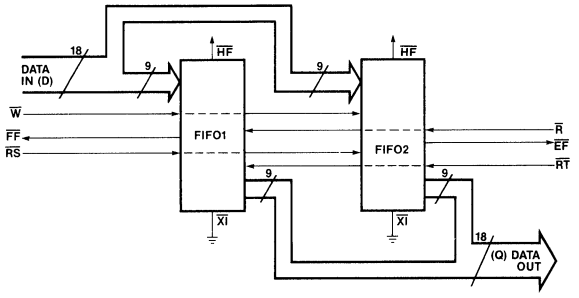
Width Expansion Mode
Word width may be easily increased by connecting the corresponding input control signals of multiple devices. Status flags, $\overline{EF}$, $\overline{FF}$ and $\overline{HF}$, can be detected from any one device. Any word width can be obtained with additional 'AC/'ACT725s.

Figure 10: Block Diagram of Single 512 x 9 FIFO



Operating Modes, cont'd

Figure 11: Block Diagram of 512 x 18 x 18 FIFO Memory Used in Width Expansion Mode



Notes: Flag detection is accomplished by monitoring $\overline{FF}$, $\overline{EF}$ and $\overline{HF}$ on any device used in the width expansion configuration. Output signals should not be connected together.

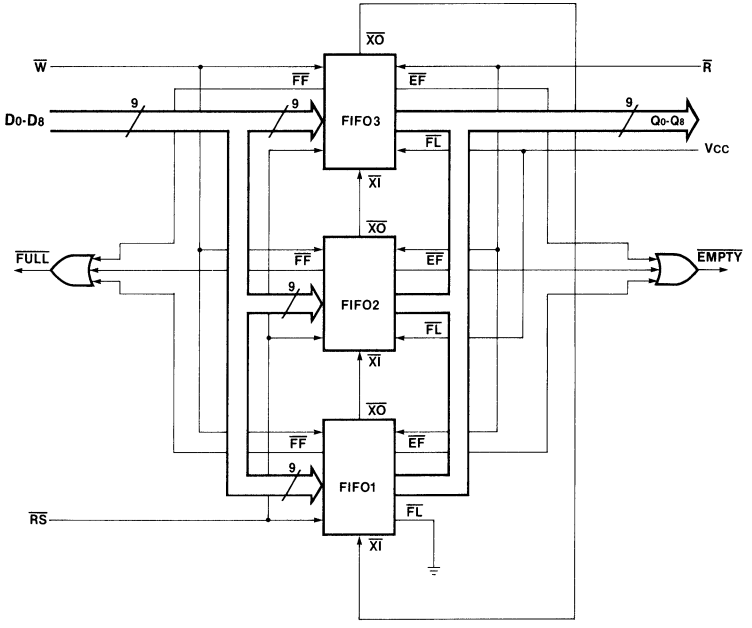
Depth Expansion (Daisy Chain) Mode

The 'AC/'ACT725 can easily be adapted to applications when the requirements are for greater than 512 words. Any depth can be obtained with additional 'AC/'ACT725 devices. The 'AC/'ACT725 operates in the Depth Expansion mode when:

1. $\overline{FL}$ of the first device is grounded.
2. $\overline{FL}$ pins of all other devices are HIGH.
3. $\overline{XO}$ of each device is tied to $\overline{XI}$ of the next device.
4. External logic is needed to generate a composite $\overline{FF}$ and $\overline{EF}$. This requires ORing all $\overline{EF}$s and all $\overline{FF}$s, i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$.
5. The $\overline{RT}$ function and $\overline{HF}$ are not available in the Depth Expansion mode.

5

Figure 12: Block Diagram of a 1536 x 9 FIFO Memory (Depth Expansion)

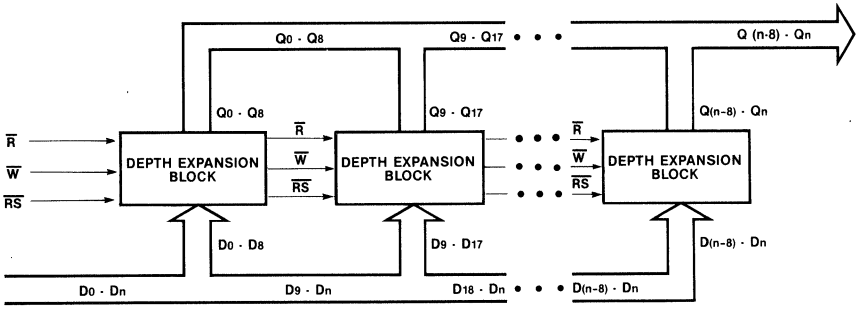


Operating Modes, cont'd

Compound Expansion Mode
The two expansion techniques described previously can be combined in a straightforward manner to achieve large FIFO arrays.

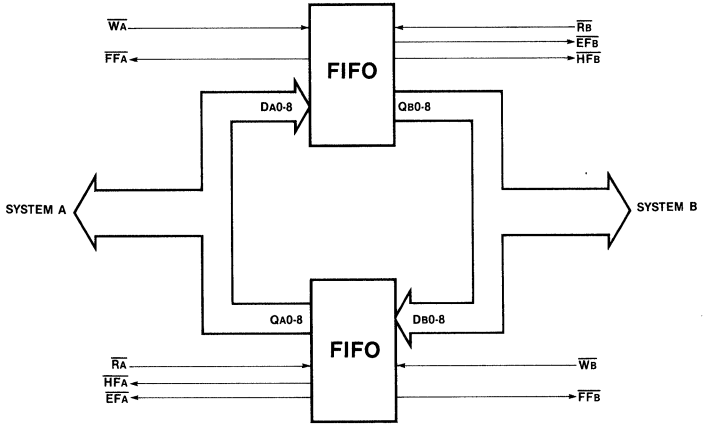
Bidirectional Mode
Applications which require data buffering between two systems (where each system is capable of read and write operations) can be achieved by pairing '725s as shown in Figure 14. Care must be taken to assure that the appropriate flag is monitored by each system ($\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in the Bidirectional Mode.

Figure 13: Compound FIFO Expansion



Notes: For depth expansion block, see Depth Expansion and Figure 12.
For flag detection, see Width Expansion and Figure 11.

Figure 14: Bidirectional FIFO Mode



Data Flow-Through Modes
Two types of flow-through modes are permitted with the '725: read flow-through and write flow-through.

For the read flow-through mode (Figure 15), the FIFO permits reading a single word of data immediately upon writing one word of data into the completely empty FIFO.

In the write flow-through mode (Figure 16), the FIFO permits writing a single word of data immediately after reading one word of data from a completely full FIFO.

Figure 15: Read Data Flow-Through Mode

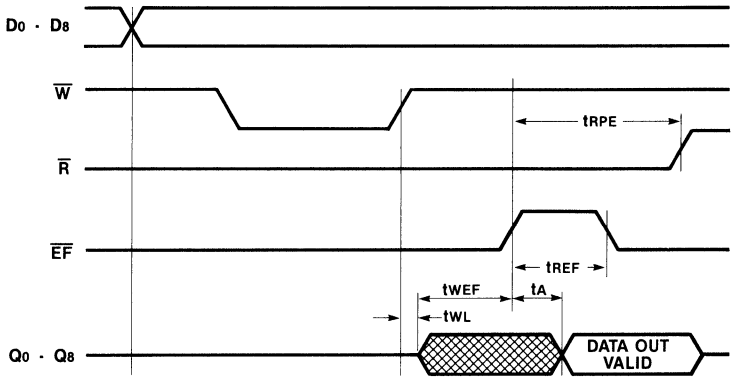
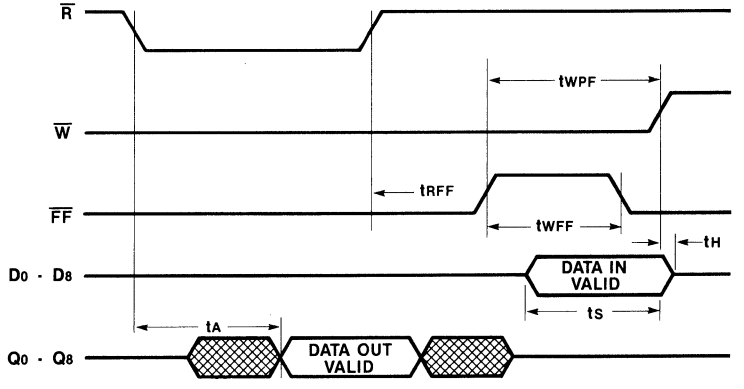


Figure 16: Write Data Flow-Through Mode



54AC/74AC818 • 54ACT/74ACT818

8-Bit Diagnostic Register

Description

The 'AC/'ACT818 is a high-speed, general-purpose pipeline register with an on-board diagnostic register for performing serial diagnostics and/or writable control store loading.

The D-to-Y path provides an 8-bit parallel data path pipeline register for normal system operation. The diagnostic register can load parallel data to or from the pipeline register and can output data through the D input port (as in WCS loading).

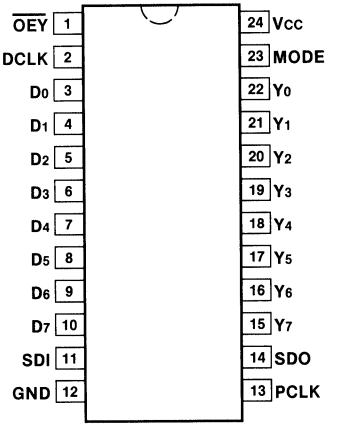
The 8-bit diagnostic register has multiplexer inputs that select parallel inputs from the Y-port or adjacent bits in the diagnostic register to operate as a right-shift-only register. This register can then participate in a serial loop throughout the system where normal data, address, status and control registers are replaced with 'AC/'ACT818 diagnostic pipeline registers. The loop can be used to scan in a complete test routine starting point (Data, Address, etc.). Then after a specified number of machine cycles it scans out the results to be inspected for the expected results. WCS loading can be accomplished using the same technique. An instruction word can be serially shifted into the shadow register and written into the WCS RAM by enabling the D output.

- **On-Line and Off-Line System Diagnostics**
- **Swaps the Contents of Diagnostic Register and Output Register**
- **Diagnostic Register and Diagnostic Testing**
- **Cascadable for Wide Control Words as Used in Microprogramming**
- **Edge-Triggered D Registers**
- **Outputs Source/Sink 24 mA**
- **'ACT818 has TTL-Compatible Inputs**
- **'ACT818 is Functionally- and Pin-Compatible to AMD 29818 and MMI 74S818**

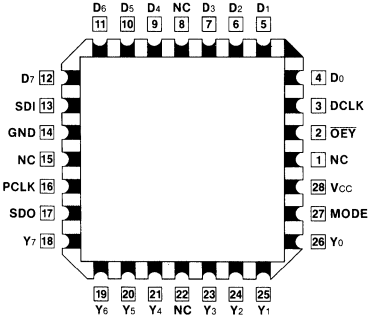
Applications

- **Register for Microprogram Control Store**
- **Status Register**
- **Data Register**
- **Instruction Register**
- **Interrupt Mask Register**
- **Pipeline Register**
- **General Purpose Register**
- **Parallel-Serial/Serial-Parallel Converter**

Connection Diagrams

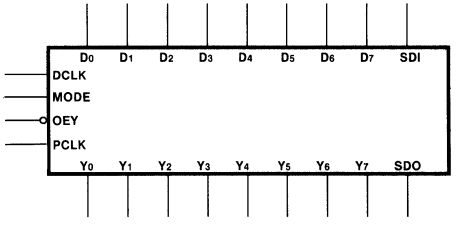


Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC and PCC

Logic Symbol

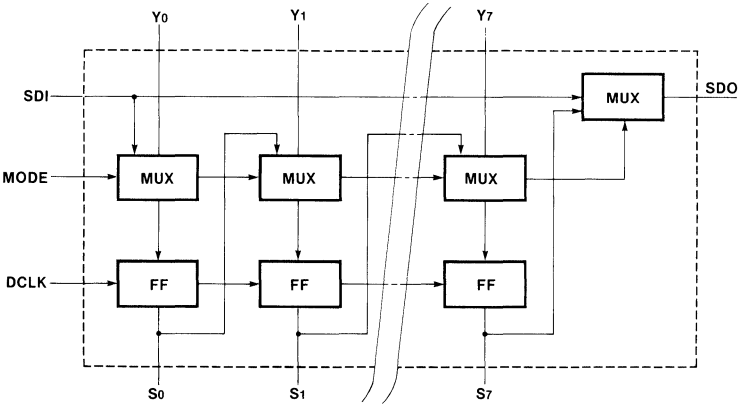


Pin Names

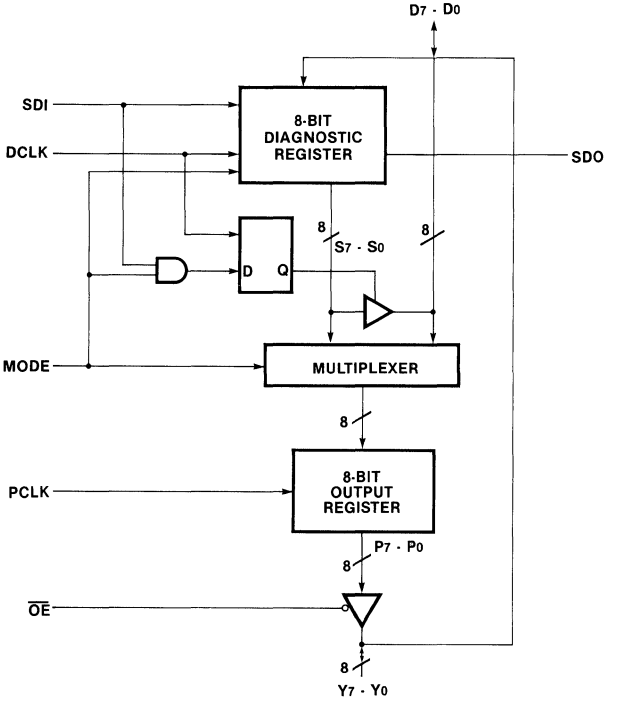
D_0 - D_7	Data Inputs
SDI	Serial Data Input
DCLK	Diagnostics Clock
MODE	Control Input
PCLK	Pipeline Register Clock
$\overline{OEY}$	Output Enable Input
SDO	Serial Data Output
Y_0 - Y_7	Data Outputs

Ordering Code: See Section 6

Diagnostic Register



Block Diagram



5

Functional Description

Data transfers into the diagnostic register occur on the LOW-to-HIGH transition of DCLK. Mode and SDI determine what data source will be loaded. The pipeline register is loaded on the LOW-to-HIGH transition of PCLK. Mode selects whether the data source is the data input or the diagnostic register output. Because of the independence of the clock inputs, data can be shifted in the diagnostic register via DCLK and loaded into the pipeline register from the data input via PCLK simultaneously, as long as no setup or hold times are violated. This simultaneous operation is legal.

Function Table

Inputs				Outputs			Operation
SDI	MODE	DCLK	PCLK	SDO	Diagnostic Reg.	Pipeline Reg.	
X	L	⌐	X	S7	SI<SI-1, SO<SDI	NA	Serial Shift; D_7 - D_0 disabled
X	L	X	⌐	S7	NA	PI<DI	Normal Load Pipeline Register
L	H	⌐	X	L	SI<YI	NA	Load Diagnostic Register from Y; DI disabled
X	H	X	⌐	SDI	NA	PI<SI	Load Pipeline Register from Diagnostic Register
H	H	⌐	X	H	Hold	NA	Hold Diagnostic Register; DI enabled

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74AC/ACT		54AC/ACT	74AC/ACT	Units	Conditions
		Typ	Guaranteed Limit				
I_{IN}	Maximum Input Current		±0.1	±10.0	±1.0	μA	V_{CC} = Max V_{IN} = V_{CC}
I_{OZ}	Maximum 3-State Current		±0.5	±10.0	±5.0	μA	$\overline{OE}$ = V_{IH}, V_{CC} = Max V_{OUT} = 0, V_{CC}
I_{CC}	Maximum Quiescent Supply Current		1.0			mA	V_{CC} = Max
I_{CCT}	Maximum Additional Icc/Input ('ACT818)			1.6	1.5	mA	V_{IN} = V_{CC}-2.1 V V_{CC} = 5.5 V
V_{OH}	Minimum LOW Level Output Y0 - Y7 Outputs		3.86	3.70	3.76	V	I_{OH} = -24 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = -24 mA, V_{CC} = 5.5 V
	Minimum HIGH Level Output D0 - D7, SDO Outputs		3.86	3.70	3.76	V	I_{OH} = -8 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = -8 mA, V_{CC} = 5.5 V
V_{OL}	Maximum LOW Level Output Y0 - Y7 Outputs		0.32	0.40	0.37	V	I_{OL} = 24 mA, V_{CC} = 4.5 V
			0.32	0.40	0.37	V	I_{OL} = 24 mA, V_{CC} = 5.5 V
	Maximum HIGH Level Output D0 - D7, SDO Outputs		0.32	0.40	0.37	V	I_{OL} = 8 mA, V_{CC} = 4.5 V
			0.32	0.40	0.37	V	I_{OL} = 8 mA, V_{CC} = 5.5 V
I_{OLD}	Minimum Dynamic Output Current, Y0 - Y7 Outputs			57	86	mA	V_{CC} = 5.5 V V_{OLD} = 1.1 V
I_{OHD}	Minimum Dynamic Output Current, Y0 - Y7 Outputs			-50	-75	mA	V_{CC} = 5.5 V V_{OHD} = 3.85 V
I_{OLD}	Minimum Dynamic Output Current, D0 - D7, SDO Outputs. See Note.			32	32	mA	V_{CC} = 5.5 V V_{OLD} = 2.2 V
I_{OHD}	Minimum Dynamic Output Current, D0 - D7, SDO Outputs. See Note.			-32	-32	mA	V_{CC} = 5.5 V V_{OHD} = 3.3 V

Note: Test Load 50 pF, 500 ohm to Ground

5

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay PCLK to Y	3.3 5.0		6.5 4.5						ns	3-6
t_{PLH}	Propagation Delay PCLK to Y	3.3 5.0		6.5 5.0						ns	3-6
t_{PHL}	Propagation Delay MODE to SDO	3.3 5.0		9.0 6.5						ns	3-6
t_{PLH}	Propagation Delay MODE to SDO	3.3 5.0		10.0 7.5						ns	3-6
t_{PHL}	Propagation Delay SDI to SDO	3.3 5.0		9.0 6.5						ns	3-6
t_{PLH}	Propagation Delay SDI to SDO	3.3 5.0		9.0 6.5						ns	3-6
t_{PHL}	Propagation Delay DCLK to SDO	3.3 5.0		12.0 8.5						ns	3-6
t_{PLH}	Propagation Delay DCLK to SDO	3.3 5.0		12.5 9.0						ns	3-6
t_{PZL}	Output Enable Time $\overline{OEY}$ to Y(x)	3.3 5.0		6.0 4.0						ns	3-8
t_{PLZ}	Output Disable Time $\overline{OEY}$ to Y(x)	3.3 5.0		6.0 4.5						ns	3-8
t_{PZL}	Output Enable Time DCLK to D(x)	3.3 5.0		11.0 8.0						ns	3-8
t_{PLZ}	Output Disable Time DCLK to D(x)	3.3 5.0		8.5 6.5						ns	3-8
t_{PZH}	Output Enable Time $\overline{OEY}$ to Y(x)	3.3 5.0		7.0 5.0						ns	3-7
t_{PHZ}	Output Disable Time $\overline{OEY}$ to Y(x)	3.3 5.0		9.0 6.5						ns	3-7
t_{PZH}	Output Enable Time DCLK to D(x)	3.3 5.0		9.0 6.5						ns	3-7
t_{PHZ}	Output Disable Time DCLK to D(x)	3.3 5.0		9.0 6.5						ns	3-7

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
ts	Setup Time D to PCLK	3.3 5.0	5.0 3.5				ns	3-9
th	Hold Time D to PCLK	3.3 5.0	-1.5 -1.0				ns	3-9
ts	Setup Time MODE to PCLK	3.3 5.0	5.5 4.0				ns	3-9
th	Hold Time MODE to PCLK	3.3 5.0	-1.5 -1.0				ns	3-9
ts	Setup Time Y TO DCLK	3.3 5.0	1.5 1.0				ns	3-9
th	Holt time Y TO DCLK	3.3 5.0	0 0				ns	3-9
ts	Setup Time MODE to DCLK	3.3 5.0	4.0 3.0				ns	3-9
th	Hold Time MODE to DCLK	3.3 5.0	-0.5 -0.5				ns	3-9
ts	Setup Time SDI to DCLK	3.3 5.0	4.0 3.0				ns	3-9
th	Hold Time SDI to DCLK	3.3 5.0	-0.5 -0.5				ns	3-9
ts	Setup Time DCLK to PCLK	3.3 5.0	9.5 7.0				ns	3-9
ts	Setup Time PCLK to DCLK	3.3 5.0	11.0 8.0				ns	3-9
tw	Pulse Width PCLK HIGH or LOW	3.3 5.0	5.5 4.0				ns	3-6
tw	Pulse Width DCLK HIGH or LOW	3.3 5.0	11.0 8.0				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PHL}	Propagation Delay PCLK to Y	5.0		6.5						ns	3-6
t_{PLH}	Propagation Delay PCLK to Y	5.0		6.5						ns	3-6
t_{PHL}	Propagation Delay MODE to SDO	5.0		8.5						ns	3-6
t_{PLH}	Propagation Delay MODE to SDO	5.0		9.5						ns	3-6
t_{PHL}	Propagation Delay SDI to SDO	5.0		8.0						ns	3-6
t_{PLH}	Propagation Delay SDI to SDO	5.0		8.0						ns	3-6
t_{PHL}	Propagation Delay DCLK to SDO	5.0		11.0						ns	3-6
t_{PLH}	Propagation Delay DCLK to SDO	5.0		11.0						ns	3-6
t_{PZL}	Output Enable Time $\overline{OEY}$ to Y(x)	5.0		6.5						ns	3-8
t_{PLZ}	Output Disable Time $\overline{OEY}$ to Y(x)	5.0		6.5						ns	3-8
t_{PZL}	Output Enable Time DCLK to D(x)	5.0		9.5						ns	3-8
t_{PLZ}	Output Disable Time DCLK to D(x)	5.0		9.0						ns	3-8
t_{PZH}	Output Enable Time $\overline{OEY}$ to Y(x)	5.0		7.5						ns	3-7
t_{PHZ}	Output Disable Time $\overline{OEY}$ to Y(x)	5.0		9.0						ns	3-7
t_{PZH}	Output Enable Time DCLK to D(x)	5.0		8.5						ns	3-7
t_{PHZ}	Output Disable Time DCLK to D(x)	5.0		9.5						ns	3-7

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time D to PCLK	5.0	3.0				ns	3-9
t_h	Hold Time D to PCLK	5.0	-1.0				ns	3-9
t_s	Setup Time MODE to PCLK	5.0	4.0				ns	3-9
t_h	Hold Time MODE to PCLK	5.0	-1.0				ns	3-9
t_s	Setup Time Y TO DCLK	5.0	1.0				ns	3-9
t_h	Hold time Y TO DCLK	5.0	0				ns	3-9
t_s	Setup Time MODE to DCLK	5.0	5.0				ns	3-9
t_h	Hold Time MODE to DCLK	5.0	-0.5				ns	3-9
t_s	Setup Time SDI to DCLK	5.0	4.0				ns	3-9
t_h	Hold Time SDI to DCLK	5.0	0				ns	3-9
t_s	Setup Time DCLK to PCLK	5.0	8.0				ns	3-9
t_s	Setup Time PCLK to DCLK	5.0	8.0				ns	3-9
t_w	Pulse Width PCLK HIGH or LOW	5.0	4.0				ns	3-6
t_w	Pulse Width DCLK HIGH or LOW	5.0	10.0				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC821 • 54ACT/74ACT821
54AC/74AC822 • 54ACT/74ACT822

10-Bit D-Type Flip-Flop

Description

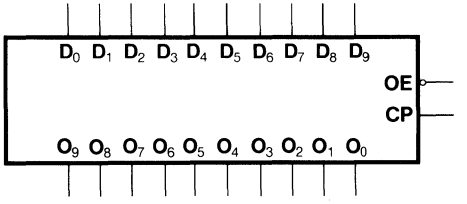
The 'AC/'ACT821 and 'AC/'ACT822 are 10-bit D-type flip-flops with 3-state outputs arranged in a broadside pinout.

The 'AC/'ACT821 and 'AC/'ACT822 are functionally identical to the AM29821 and AM29822.

- **3-State Outputs for Bus Interfacing**
- **Inverting ('822) or Noninverting ('821) Outputs**
- **Outputs Source/Sink 24 mA**
- **'ACT821 and 'ACT822 have TTL-Compatible Inputs**

Ordering Code: See Section 6

Logic Symbol ('AC/'ACT821)*

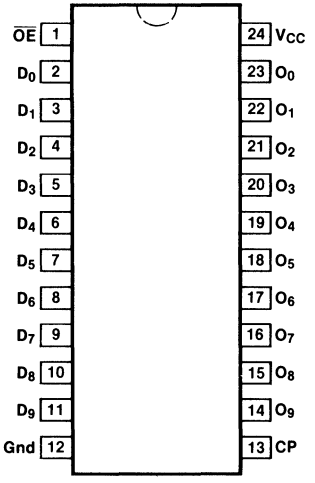


*The 'AC/'ACT822 has inverting outputs.

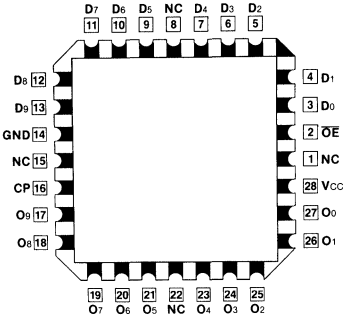
Pin Names

D_0 - D_9	Data Inputs
O_0 - O_9	Data Outputs ('AC/'ACT821)
$\overline{O_0}$ - $\overline{O_9}$	Data Outputs ('AC/'ACT822)
$\overline{OE}$	Output Enable
CP	Clock Input

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

The 'AC/'ACT821 and 'AC/'ACT822 consist of ten D-type edge-triggered flip-flops. The buffered Clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}$ LOW the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The 'AC/'ACT821 and 'AC/'ACT822 are functionally and pin compatible with the AM29821 and AM29822.

Function Table

Inputs			Internal	Outputs		Function
$\overline{OE}$	CP	D	Q	O ('821)	$\overline{O}$ ('822)	
H	⌐	L	L	Z	Z	High Z
H	⌐	H	H	Z	Z	High Z
L	⌐	L	L	L	H	Load
L	⌐	H	H	H	L	Load

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
⌐ = LOW-to-HIGH Clock Transition

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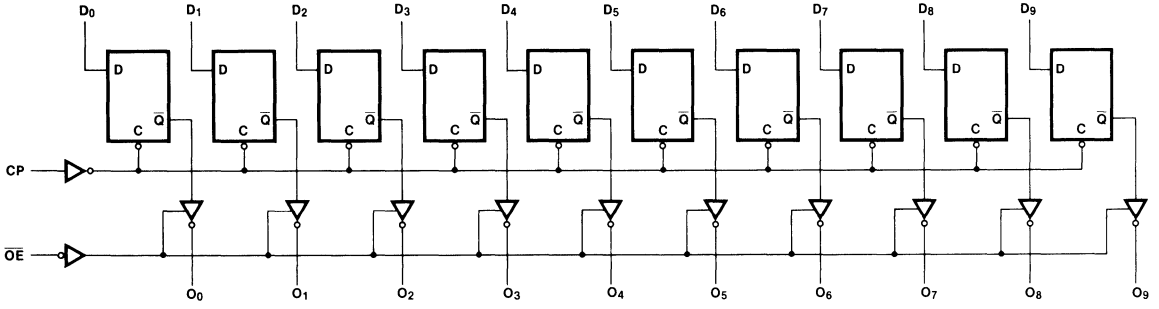
Logic Diagram ('AC/'ACT821)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate progagation delays. The 'AC/'ACT822 also has the same logic diagram with inverting outputs.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT821/822)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		100 125						MHz	3-3
t_{PLH}	Propagation Delay CP to On	3.3 5.0		9.5 6.5						ns	3-6
t_{PHL}	Propagation Delay CP to On	3.3 5.0		9.5 6.5						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to On	3.3 5.0		7.5 5.5						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to On	3.3 5.0		8.0 6.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to On	3.3 5.0		10.5 7.5						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to On	3.3 5.0		9.0 6.5						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	3.0 2.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.5				ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	120	110				110		MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	5.0	1.0	8.0	9.5			1.0	10.5	ns	3-6
t_{PHL}	Propagation Delay CP to O_n	5.0	1.0	8.0	9.5			1.0	10.5	ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0	1.0	7.0	10.5			1.0	11.5	ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0	1.0	7.5	10.5			1.0	12.0	ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.0	10.0	12.0			1.0	13.0	ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0	1.0	9.5	10.5			1.0	11.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT		54ACT	74ACT	Units	Fig. No.
			$T_A = +25°C$ $C_L = 50$ pF		$T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	$T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	2.0	2.0		2.5	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	2.0		2.5	ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	3.0	4.5		5.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	35.0	pF	$V_{CC} = 5.5$ V

54AC/74AC823 • 54ACT/74ACT823
54AC/74AC824 • 54ACT/74ACT824

9-Bit D-Type Flip-Flop

Description

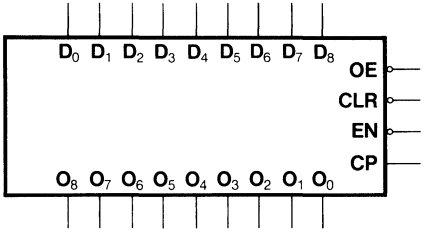
The 'AC/'ACT823 and 'AC/'ACT824 are 9-bit buffered registers. They feature Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The 'AC/'ACT 823 offers noninverting outputs and the 'AC/'ACT824 offers inverting outputs.

The 'AC/'ACT823 is fully compatible with AMD's AM29823.

- **Outputs Source/Sink 24 mA**
- **3-State Outputs for Bus Interfacing**
- **Inputs and Outputs are on Opposite Sides**
- **'ACT823 and 'ACT824 have TTL-Compatible Inputs**

Ordering Code: See Section 6

Logic Symbol ('AC/'ACT823)*

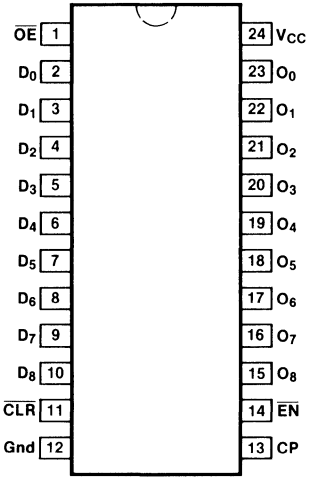


*The 'AC/'ACT824 has inverting outputs.

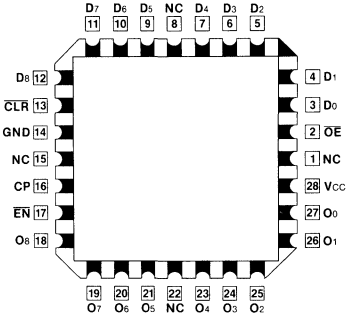
Pin Names

D_0 - D_8	Data Inputs
O_0 - O_8	Data Outputs ('AC/'ACT823)
$\overline{O}_0$ - $\overline{O}_8$	Data Outputs ('AC/'ACT824)
$\overline{OE}$	Output Enable
$\overline{CLR}$	Clear
CP	Clock Input
$\overline{EN}$	Clock Enable

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

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Functional Description

The 'AC/'ACT823 and 'AC/'ACT824 consist of nine D-type edge-triggered flip-flops. These have 3-state outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}$ LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These devices are ideal for parity bus interfacing in high performance systems.

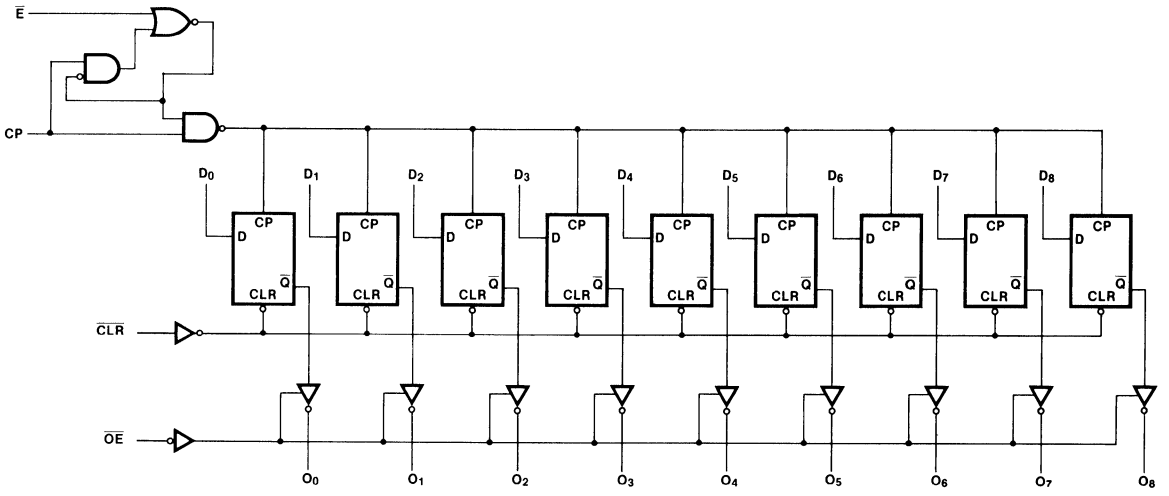
When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Outputs		Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	Q	O ('823)	$\overline{O}$ ('824)	
H	X	L	⌐	L	L	Z	Z	High Z
H	X	L	⌐	H	H	Z	Z	High Z
H	L	X	X	X	L	Z	Z	Clear
L	L	X	X	X	L	L	L	Clear
H	H	H	X	X	NC	Z	Z	Hold
L	H	H	X	X	NC	NC	NC	Hold
H	H	L	⌐	L	L	Z	Z	Load
H	H	L	⌐	H	H	Z	Z	Load
L	H	L	⌐	L	L	L	H	Load
L	H	L	⌐	H	H	H	L	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

Logic Diagram ('AC/'ACT823)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The 'AC/'ACT824 also has the same logic diagram with inverting outputs.

5

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT823/824)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		100 125						MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0		9.5 6.5						ns	3-6
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0		9.5 6.5						ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	3.3 5.0		14.5 10.5						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		7.5 5.5						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		8.0 6.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		10.5 7.5						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		8.5 6.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF	54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	3.0 2.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.5			ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	3.3 5.0	3.0 2.0			ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	3.3 5.0	2.0 1.5			ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5			ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	3.3 5.0	5.0 3.5			ns	3-6
t_{rec}	$\overline{CLR}$ to CP Recovery Time	3.3 5.0	2.0 1.5			ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		110						MHz	3-3
t_{PLH}	Propagation Delay CP to On	5.0		8.0						ns	3-6
t_{PHL}	Propagation Delay CP to On	5.0		8.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to On	5.0		12.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to On	5.0		7.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to On	5.0		7.5						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to On	5.0		10.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to On	5.0		8.5						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D to CP	5.0	2.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	5.0	2.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	5.0	1.5				ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	3.0				ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	4.0				ns	3-6
t_{rec}	$\overline{CLR}$ to CP Recovery Time	5.0	1.5				ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

5

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC825 • 54ACT/74ACT825
54AC/74AC826 • 54ACT/74ACT826

8-Bit D-Type Flip-Flop

Description

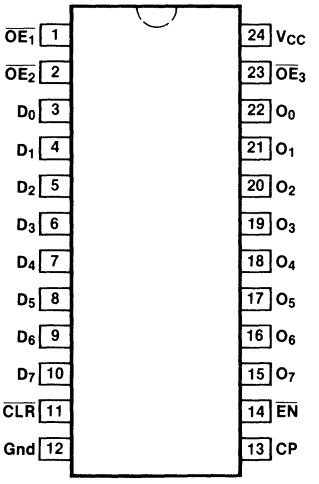
The 'AC/'ACT825 and 'AC/'ACT826 are 8-bit buffered registers. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multi-use control of the interface. The'AC/'ACT825 has noninverting outputs; the 'AC/'ACT826 has inverting outputs.

The 'AC/'ACT825 is fully compatible with AMD's AM29825.

- **Outputs Source/Sink 24 mA**
- **Inputs and Outputs are on Opposite Sides**
- **'ACT825 and 'ACT826 have TTL-Compatible Inputs**

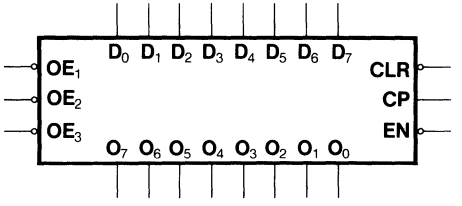
Ordering Code: See Section 6

Connection Diagrams

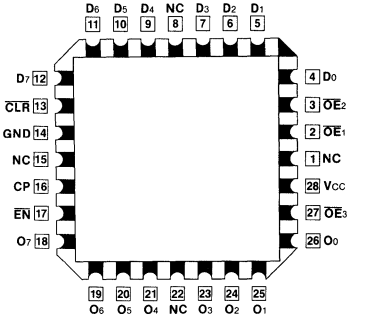


Pin Assignment for DIP, Flatpak and SOIC

Logic Symbol ('AC/'ACT825)*



*The 'AC/'ACT826 has inverting outputs.



Pin Assignment for LCC

Pin Names

D_0 - D_7	Data Inputs
O_0 - O_7	Data Outputs ('AC/'ACT825)
$\overline{O_0}$ - $\overline{O_7}$	Data Outputs ('AC/'ACT826)
$\overline{OE_1}$, $\overline{OE_2}$, $\overline{OE_3}$	Output Enables
$\overline{EN}$	Clock Enable
$\overline{CLR}$	Clear
CP	Clock Input

Functional Description

The 'AC/'ACT825 and 'AC/'ACT826 consist of eight D-type edge-triggered flip-flops. These devices have 3-state outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}_1$, $\overline{OE}_2$ and $\overline{OE}_3$ LOW, the contents of the flip-flops are available at the outputs. When one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the outputs go to the high impedance state.

Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The 'AC/'ACT825 and 'AC/'ACT826 have Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These pins are ideal for parity bus interfacing in high performance systems.

When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

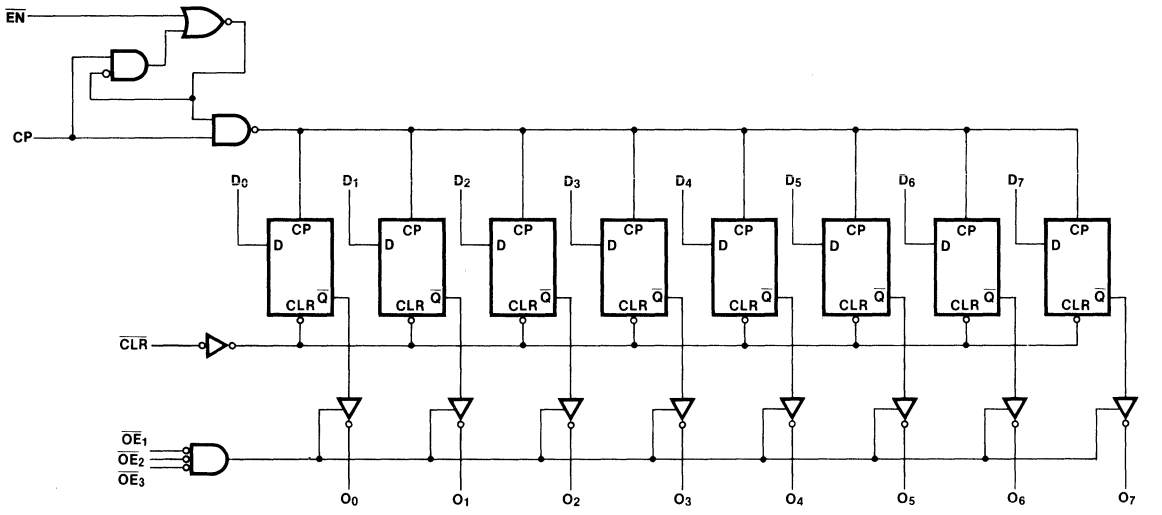
Function Table

Inputs					Internal	Outputs		Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	Dn	Q	O ('825)	$\overline{O}$ ('826)	
H	X	L	⌐	L	L	Z	Z	High Z
H	X	L	⌐	H	H	Z	Z	High Z
H	L	X	X	X	L	Z	Z	Clear
L	L	X	X	X	L	L	L	Clear
H	H	H	X	X	NC	Z	Z	Hold
L	H	H	X	X	NC	NC	NC	Hold
H	H	L	⌐	L	L	Z	Z	Load
H	H	L	⌐	H	H	Z	Z	Load
L	H	L	⌐	L	L	L	H	Load
L	H	L	⌐	H	H	H	L	Load

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

5

Logic Diagram ('AC/'ACT825)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The 'AC/'ACT826 also has the same logic diagram with inverting outputs.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT825/826)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		100 125						MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	3.3 5.0		9.0 6.5						ns	3-6
t_{PHL}	Propagation Delay CP to O_n	3.3 5.0		9.0 6.5						ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	3.3 5.0		14.5 10.5						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		9.0 6.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		9.5 6.5						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		12.5 8.5						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		12.0 7.5						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

5

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	3.0 2.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.5				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	3.3 5.0	3.0 2.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	3.3 5.0	2.0 1.5				ns	3-9
t_w	CP Pulse Width HIGH or LOW	3.3 5.0	3.5 2.5				ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	3.3 5.0	5.0 3.5				ns	3-6
t_{rec}	$\overline{CLR}$ to CP Recovery Time	3.3 5.0	2.0 1.5				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0		110						MHz	3-3
t_{PLH}	Propagation Delay CP to O_n	5.0		8.0						ns	3-6
t_{PHL}	Propagation Delay CP to O_n	5.0		8.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0		12.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0		7.5						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0		8.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		11.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.5						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

5

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	2.0				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	1.0				ns	3-9
t_s	Setup Time, HIGH or LOW $\overline{EN}$ to CP	5.0	2.0				ns	3-9
t_h	Hold Time, HIGH or LOW $\overline{EN}$ to CP	5.0	1.5				ns	3-9
t_w	CP Pulse Width HIGH or LOW	5.0	3.0				ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	3.5				ns	3-6
t_{rec}	$\overline{CLR}$ to CP Recovery Time	5.0	1.5				ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC841 • 54ACT/74ACT841
54AC/74AC842 • 54ACT/74ACT842

10-Bit Transparent Latch

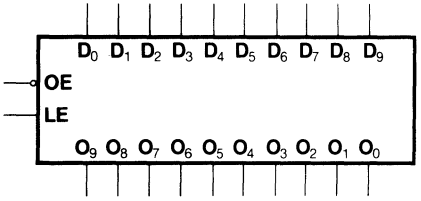
Description

The 'AC/'ACT841 and 'AC/'ACT842 bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'AC/'ACT841 is a 10-bit transparent latch, a 10-bit version of the 'AC/'ACT373.

- **'ACT841 and 'ACT842 have TTL-Compatible Inputs**

Ordering Code: See Section 6

Logic Symbol ('AC/'ACT841)*

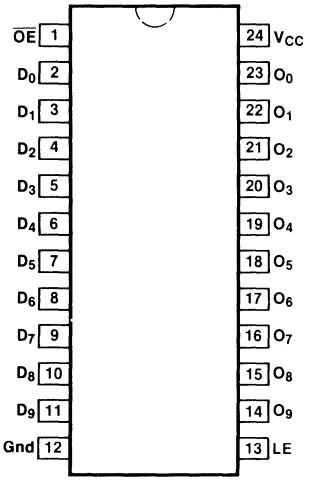


*The 'AC/'ACT842 has inverting outputs.

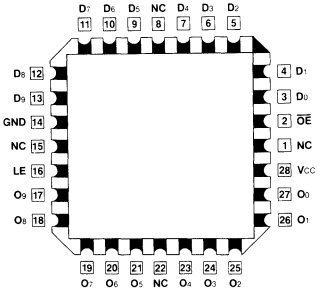
Pin Names

D_0 - D_9	Data Inputs
O_0 - O_9	Data Outputs ('AC/'ACT841)
$\overline{O}_0$ - $\overline{O}_9$	Data Outputs ('AC/'ACT842)
$\overline{OE}$	Output Enable
LE	Latch Enable

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

5

Functional Description

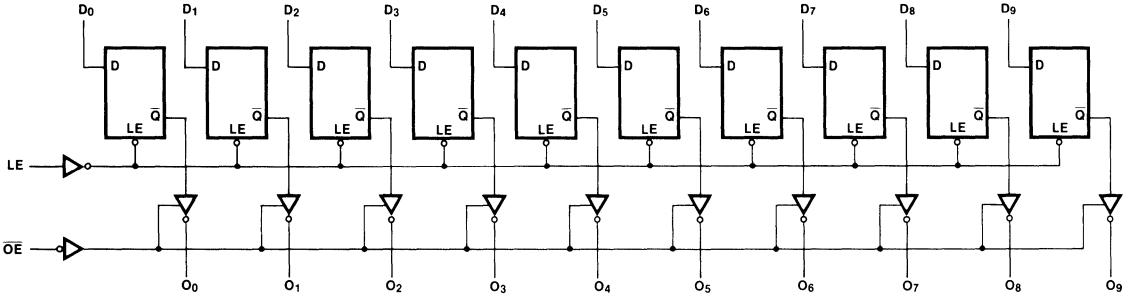
The 'AC/'ACT841 and 'AC/'ACT842 consist of ten D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup and hold time is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedance state.

Function Table

Inputs			Internal	Output		Function
$\overline{OE}$	LE	D	Q	O ('841)	$\overline{O}$ ('842)	
X	X	X	X	Z	Z	High Z
H	H	L	L	Z	Z	High Z
H	H	H	H	Z	Z	High Z
H	L	X	NC	Z	Z	Latched
L	H	L	L	L	H	Transparent
L	H	H	H	H	L	Transparent
L	L	X	NC	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram ('AC/'ACT841)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate progagation delays. The 'AC/'ACT842 has the same logic diagram with inverting outputs.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT841/842)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3		17.0						ns	3-5
		5.0		12.0							
t_{PHL}	Propagation Delay D_n to O_n	3.3		16.5						ns	3-5
		5.0		11.0							
t_{PLH}	Propagation Delay LE to O_n	3.3		18.5						ns	3-6
		5.0		13.0							
t_{PHL}	Propagation Delay LE to O_n	3.3		17.0						ns	3-6
		5.0		12.0							
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3		14.5						ns	3-7
		5.0		10.0							
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3		11.5						ns	3-8
		5.0		8.0							
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3		13.0						ns	3-7
		5.0		9.0							
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3		13.0						ns	3-8
		5.0		9.0							

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

5

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	4.0 2.5				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	0 0				ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.5				ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0		12.0						ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	5.0		11.0						ns	3-5
t_{PLH}	Propagation Delay LE to O_n	5.0		13.0						ns	3-6
t_{PHL}	Propagation Delay LE to O_n	5.0		12.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0		10.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0		8.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	2.5				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0				ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.5				ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

5

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC843 • 54ACT/74ACT843
54AC/74AC844 • 54ACT/74ACT844

9-Bit Transparent Latch

Description

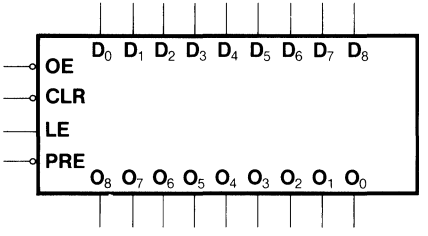
The 'AC/'ACT843 and 'AC/'ACT844 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity.

The 'AC/'ACT843 is functionally and pin compatible with AMD's AM29843.

- **'ACT843 and 'ACT844 have TTL-Compatible Inputs**

Ordering Code: See Section 6

Logic Symbol ('AC/'ACT843)*

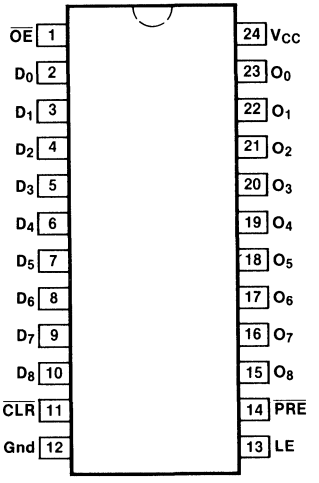


*The 'AC/'ACT844 has inverting outputs.

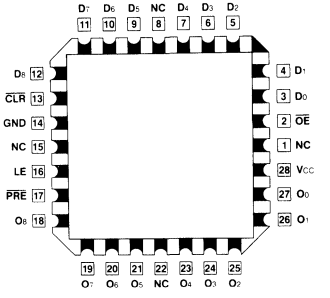
Pin Names

D_0 - D_8	Data Inputs
O_0 - O_8	Data Outputs ('AC/'ACT843)
$\overline{O}_0$ - $\overline{O}_8$	Data Outputs ('AC/'ACT844)
$\overline{OE}$	Output Enable
LE	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

The 'AC/'ACT843 and 'AC/'ACT844 consist of nine D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state. In addition to the LE and $\overline{OE}$ pins, the 'AC/'ACT843 and 'AC/'ACT844 have a Clear ($\overline{CLR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overides $\overline{CLR}$.

Function Tables

Inputs					Internal	Outputs		Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D	Q	O ('843)	$\overline{O}$ ('844)	
H	H	H	H	L	L	Z	Z	High Z
H	H	H	H	H	H	Z	Z	High Z
H	H	H	L	X	NC	Z	Z	Latched
H	H	L	H	L	L	L	H	Transparent
H	H	L	H	H	H	H	L	Transparent
H	H	L	L	X	NC	NC	NC	Latched
H	L	L	X	X	H	H	L	Preset
L	H	L	X	X	L	L	H	Clear
L	L	L	X	X	H	H	L	Preset
L	H	H	L	X	L	Z	Z	Clear/High Z
H	L	H	L	X	H	Z	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

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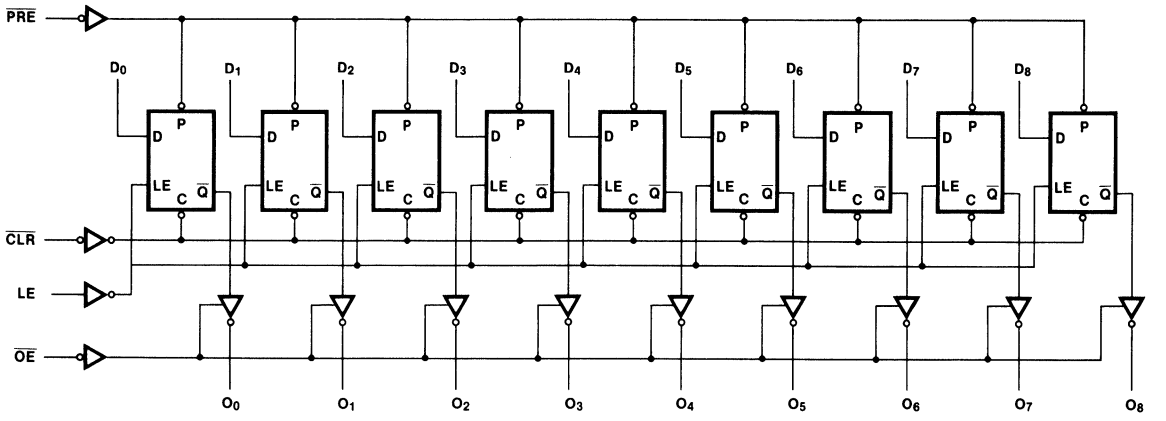
Logic Diagram ('AC/'ACT843)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The 'AC/'ACT844 has the same logic diagram with inverting outputs.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT843/844)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3 5.0		17.0 12.0						ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	3.3 5.0		16.5 11.0						ns	3-5
t_{PLH}	Propagation Delay LE to O_n	3.3 5.0		18.5 13.0						ns	3-6
t_{PHL}	Propagation Delay LE to O_n	3.3 5.0		17.0 12.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	3.3 5.0		17.0 12.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	3.3 5.0		17.0 12.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		14.5 10.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		11.5 8.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		13.0 9.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		13.0 9.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$ $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	4.0 2.5				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	0 0				ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.5				ns	3-6
t_w	$\overline{PRE}$ Pulse Width, LOW	3.3 5.0	4.0 2.5				ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	3.3 5.0	4.0 2.5				ns	3-6
t_{rec}	$\overline{PRE}$ Recovery Time	3.3 5.0	5.0 4.0				ns	3-9
t_{rec}	$\overline{CLR}$ Recovery Time	3.3 5.0	5.0 4.0				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0		12.0						ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	5.0		11.0						ns	3-5
t_{PLH}	Propagation Delay LE to O_n	5.0		13.0						ns	3-6
t_{PHL}	Propagation Delay LE to O_n	5.0		12.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	5.0		12.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0		12.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0		10.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0		8.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	2.5				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0				ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.5				ns	3-6
t_w	$\overline{PRE}$ Pulse Width, LOW	5.0	2.5				ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	2.5				ns	3-6
t_{rec}	$\overline{PRE}$ Recovery Time	5.0	5.0				ns	3-9
t_{rec}	$\overline{CLR}$ Recovery Time	5.0	5.0				ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC845 • 54ACT/74ACT845
54AC/74AC846 • 54ACT/74ACT846

8-Bit Transparent Latch

Description

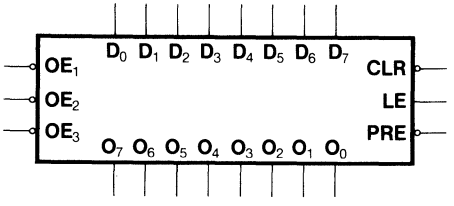
The 'AC/'ACT845 and 'AC/'ACT846 bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide easy expansion through multiple $\overline{OE}$ controls.

The 'AC/'ACT845 is functionally and pin compatible with AMD's AM29845.

- **'ACT845 and 'ACT846 have TTL-Compatible Inputs**

Ordering Code: See Section 6

Logic Symbol ('AC/'ACT845)*

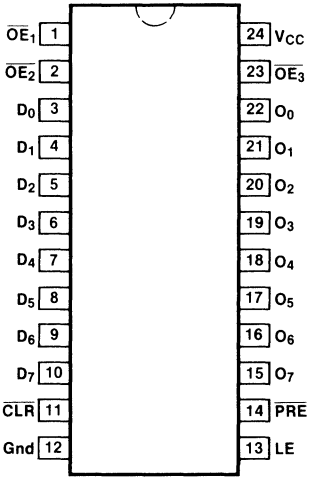


*The 'AC/'ACT846 has inverting outputs.

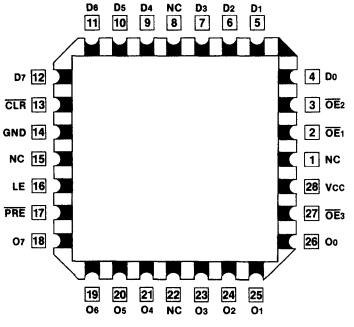
Pin Names

D_0 - D_7	Data Inputs
O_0 - O_7	Data Outputs ('AC/'ACT845)
$\overline{O}_0$ - $\overline{O}_7$	Data Outputs ('AC/'ACT846)
$\overline{OE}_1$ - $\overline{OE}_3$	Output Enables
LE	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

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Functional Description

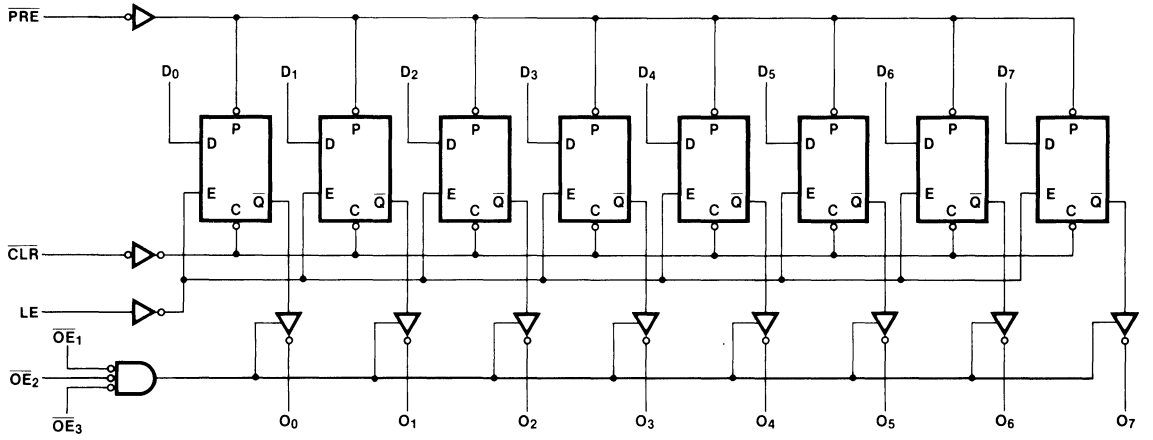
The 'AC/'ACT845 and 'AC/'ACT846 consist of eight D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) are LOW. When any one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the bus output is in the high impedance state.

Function Table

Inputs					Internal	Outputs		Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}_1$-$\overline{OE}_3$	LE	D	Q	O ('845)	$\overline{O}$ ('846)	
H	H	H	H	L	L	Z	Z	High Z
H	H	H	H	H	H	Z	Z	High Z
H	H	H	L	X	NC	Z	Z	Latched
H	H	L	H	L	L	L	H	Transparent
H	H	L	H	H	H	H	L	Transparent
H	H	L	L	X	NC	NC	NC	Latched
H	L	L	X	X	H	H	L	Preset
L	H	L	X	X	L	L	H	Clear
L	L	L	X	X	H	H	L	Preset
L	H	H	L	X	L	Z	Z	Clear/High Z
H	L	H	L	X	H	Z	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram ('AC/'ACT845)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The 'AC/'ACT846 has the same logic diagram with inverting outputs.

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DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT845/846)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3		17.0						ns	3-5
		5.0		12.0							
t_{PHL}	Propagation Delay D_n to O_n	3.3		16.5						ns	3-5
		5.0		11.0							
t_{PLH}	Propagation Delay LE to O_n	3.3		18.5						ns	3-6
		5.0		13.0							
t_{PHL}	Propagation Delay LE to O_n	3.3		17.0						ns	3-6
		5.0		12.0							
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	3.3		17.0						ns	3-6
		5.0		12.0							
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	3.3		17.0						ns	3-6
		5.0		12.0							
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3		14.5						ns	3-7
		5.0		10.0							
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3		11.5						ns	3-8
		5.0		8.0							
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3		13.0						ns	3-7
		5.0		9.0							
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3		13.0						ns	3-8
		5.0		9.0							

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW, D_n to LE	3.3 5.0	4.0 2.5				ns	3-9
t_h	Hold Time, HIGH or LOW, D_n to LE	3.3 5.0	0 0				ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.5				ns	3-6
t_w	$\overline{PRE}$ Pulse Width, LOW	3.3 5.0	4.0 2.5				ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	3.3 5.0	4.0 2.5				ns	3-6
t_{rec}	$\overline{PRE}$ Recovery Time	3.3 5.0	5.0 4.0				ns	3-9
t_{rec}	$\overline{CLR}$ Recovery Time	3.3 5.0	5.0 4.0				ns	3-9

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0		12.0						ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	5.0		11.0						ns	3-5
t_{PLH}	Propagation Delay LE to O_n	5.0		13.5						ns	3-6
t_{PHL}	Propagation Delay LE to O_n	5.0		12.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	5.0		12.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0		12.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0		10.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0		18.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$ $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	2.5				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0				ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.5				ns	3-6
t_w	$\overline{PRE}$ Pulse Width, LOW	5.0	2.5				ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	2.5				ns	3-6
t_{rec}	$\overline{PRE}$ Recovery Time	5.0	5.0				ns	3-9
t_{rec}	$\overline{CLR}$ Recovery Time	5.0	5.0				ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

54AC/74AC1010 • 54ACT/74ACT1010

16 x 16 Parallel Multiplier/Accumulator

Description

The 'AC/'ACT1010 is a high-speed, low-power 16 x 16 bit parallel multiplier with a 35-bit accumulator that is ideally suited for real-time digital signal processing applications. Fabricated using 1.3-micron FACT technology, the 'AC/'ACT1010 offers a very low power alternative (10% of the power of bipolar and NMOS counterparts) and exceptional speed (55 ns maximum multiply accumulate) performance.

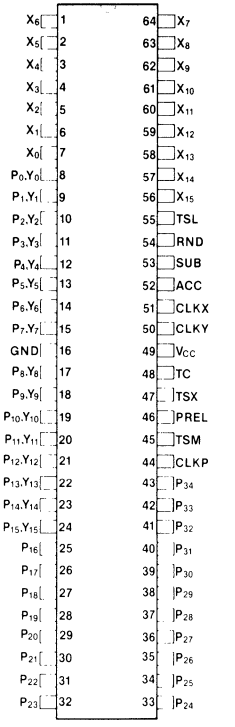
The 'AC/'ACT1010 is a pin and functional replacement for TRW's TDC1010; the 'ACT1010 operates from a single Vcc supply and is compatible with standard TTL logic levels.

The architecture of the 'AC/'ACT1010 features one 16-bit input port dedicated to the X input registers (controlled by CLKX), one 16-bit I/O port used for loading the Y input registers (controlled by CLKY) and for preloading and displaying the LSP of the P output registers (controlled by CLKP), one 16-bit I/O port for preloading and displaying the MSP of the P output registers (controlled by CLKP), and one 3-bit I/O port for loading and displaying the contents of the XTP (most significant bits) of the P output registers (also controlled by CLKP).

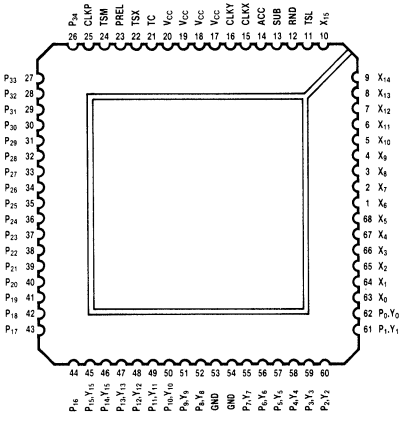
When the unregistered preload input (PREL) is active, all the output buffers are forced into a high impedance state. By using the 3-state controls (TSX, TSM and TSL) as register enables, external data is loaded on the rising edge of each CLKP pulse.

Both twos complement and unsigned magnitude arithmetic are supported through the registered TC line. The accumulator functions are enabled through the registered ACC line. When the registered SUB signal is active/inactive, the accumulator data is subtracted from/added to the multiplier product. The result is loaded into the accumulator registers for use in subsequent operations. The multiplier product is automatically sign extended for twos complement arithmetic with the accumulator. The registered RND signal controls rounding of the arithmetic result if active,

Connection Diagrams



Pin Assignment for DIP



Pin Assignment for PCC

a '1' is added to the MSB of the LSP of multiplication result and then fed into the accumulator circuitry.

The function of the data busses, X, Y and P and the effect of the format pins, TC, RND, ACC, and SUB can be described mathematically by:

$$P[nT] = \sum_{i=0}^{15}\{X_i \bullet 2^i\} \bullet \sum_{i=0}^{15}\{Y_i \bullet 2^i\} + (-1)^{SUB} \bullet ACC \bullet \sum_{i=0}^{34}\{Pi[(n-1)T] \bullet 2^i\} + RND \bullet 2^{15}$$

where T is the clock period of CLKP, n represents the number of the clock cycle, X, Y, RND, ACC and SUB values are the values found in the registers t_{MA} ns before clock period n.

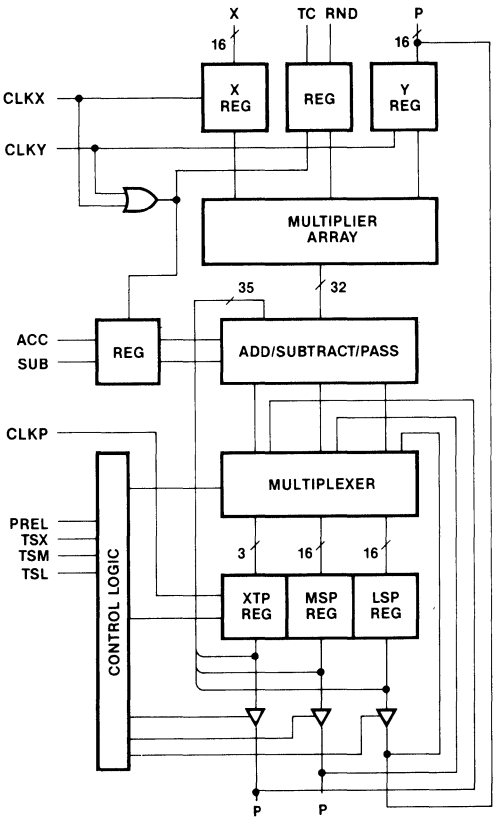
- **16 x 16 Parallel Multiplier/Accumulator**
- **High Speed—55 ns Multiply/Accumulate Time**
- **Selectable Accumulation, Subtraction, Rounding and Preloading with a 35-Bit Result**
- **Pin and Functionally Compatible with the TRW TDC1010J**
- **High Drive (8 mA) Output Capability**
- **Low Power Consumption (less than 250 mW typical)—Less Than 7% of the Power of Compatible Bipolar and 14% of the Power of NMOS Designs**
- **Inputs and Outputs Directly TTL-Compatible**
- **Single Vcc Supply**
- **±2000 V ESD Protection**

Ordering Code: See Section 6

Pin Names

X_0 - X_{15}	Multiplicand Data Inputs
Y_0 - Y_{15}	Multiplier Data Inputs
CLKX, CLKY	Input Clocks
ACC	Accumulate Input
SUB	Subtract Input
RND	Round Input
PREL	Preload Input
TC	Twos Complement Control Input
TSM, TSX, TSL	3-State Output Controls
CLKP	Output Clock
P_{15} - P_0	Least Significant Product (LSP)
P_{31} - P_{16}	Most Significant Product (MSP)
P_{34} - P_{32}	Extended Product Output (XTP)

Block Diagram



Functional Description

Signal Descriptions

Inputs:	
XIN (X_{15} - X_0)	Multiplicand Data Inputs
YIN (Y_{15} - Y_0)	Multiplier Data Inputs
Input Clocks:	
CLKX, CLKY	Input data is loaded on the rising edge of these clocks.
Outputs:	
XTP (P_{34} - P_{32})	Extended Product Output (3-bits)
MSP (P_{31} - P_{16})	Most Significant Product
LSP (P_{15} - P_0)	Least Significant Product
Output Clock:	
CLKP	Output data is loaded into the output register on the rising edge of this clock.

Controls

ACC (Accumulate)

When ACC is HIGH, the contents of the output registers (XTP, MSP and LSP) are added to or subtracted from the multiplier output. When ACC is LOW, the device acts as a simple multiplier with no accumulation being performed and the next product generated will be stored directly into the output registers. The ACC signal is loaded on the rising edge of the CLKX or CLKY and must be valid for the duration of the data input.

SUB (Subtract)

When the ACC and SUB signals are both HIGH, the contents of the output registers are subtracted from the next product generated and the difference is stored back into the output registers at the rising edge of the next CLKP. When ACC is HIGH and SUB is LOW, an addition instead of a subtraction is performed. Like the ACC signal, the SUB signal is loaded into the SUB register at the rising edge of either CLKX or CLKY and must be valid over the same period as the input data is valid. When the ACC is LOW, SUB acts as a "don't care" input.

RND (Round)

A HIGH level at this input adds a '1' to the most significant bit of the LSP to round up the XTP and MSP data. RND, like ACC and SUB, is loaded on the rising edge of either CLKX or CLKY and must be valid for the duration of the input data.

PREL (Preload)

When the PREL input is HIGH, the output is driven to a HIGH impedance state. When the TSX, TSL and TSM inputs are also high, the contents of the output register can be preset to the preload data applied to the output pins at the rising of CLKP. The PREL, TSM, TSL and TSX inputs must all be valid over the same period that the preload input is valid.

YIN/LSP Output

Shares functions between 16-bit data input (YIN) and the least significant product output (LSP).

TSX, TSL, TSM (3-State Output Controls)

The XTP, MSP and LSP registers are controlled by direct non-registered control signals. These output drivers are at high impedance (disabled) when control signals TSX, TSM and TSL are HIGH and are enabled when TSX, TSM and TSL are LOW.

Notes on Twos Complement Formats

1. In twos complement notation, the location of the binary point that signifies the separation of the fractional and integer fields is just after the sign, between the sign bit (-2^0) and the next significant bit for the multiplier inputs. This same format is carried over to the output format, except that the extended significance of the integer field is provided to extend the utility of the accumulator. In the case of the output notation, the output binary point is located between the -2^0 and 2^{-1} bit positions. The location of the binary point is arbitrary, as long as there is consistency with both the input and output formats. The number field can be considered entirely integer with the binary point just to the right of the least significant bit for the input, product and the accumulated sum.

2. When in the non-accumulating mode, the first four bits (P_{34} to P_{31}) will all indicate the sign of the product. Additionally, the P_{30} term will also indicate the sign except for one exceptional case when multiplying $(-1) \times (-1)$. With the additional bits that are available in this multiplier, the $(-1) \times (-1)$ is a valid operation that yields a $(+1)$ product.

3. In operations that require the accumulation of single products or sum of products, there is no change in format. To allow for a valid summation beyond the available for a single multiplication product, three additional significant bits (guard bits) are provided. This is the same as if the product was accumulated off-chip in a separate 35-bit wide adder. Taking the sign at the most significant bit position will guarantee that the largest number field will be used. When the accumulated sum only occupies the right hand portion of the accumulator, the sign will be extended into the lesser significant bit positions.

Preload Truth Table

PREL	TSX	TSM	TSL	XTP	MSP	LSP
0	0	0	0	Q	Q	Q
0	0	0	1	Q	Q	High Z
0	0	1	0	Q	High Z	Q
0	0	1	1	Q	High Z	High Z
0	1	0	0	High Z	Q	Q
0	1	0	1	High Z	Q	High Z
0	1	1	0	High Z	High Z	Q
0	1	1	1	High Z	High Z	High Z
1	0	0	0	High Z	High Z	High Z
1	0	0	1	High Z	High Z	PL
1	0	1	0	High Z	PL	High Z
1	0	1	1	High Z	PL	PL
1	1	0	0	PL	High Z	High Z
1	1	0	1	PL	High Z	PL
1	1	1	0	PL	PL	High Z
1	1	1	1	PL	PL	PL

Notes:

High Z = Output buffers at high impedance (output disabled).

Q = Output buffers at low impedance. Contents of output register will be transferred to output pins.

PL = Output buffers at high impedance, or output disabled. Preload data supplied externally at output pins will be loaded into the output register at the rising edge of CLKP.

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Figure 1: Fractional Twos Complement Notation

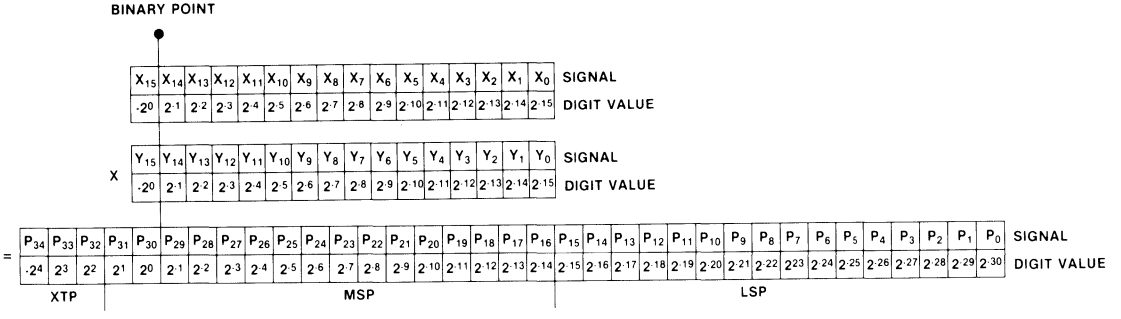


Figure 2: Fractional Unsigned Magnitude Notation

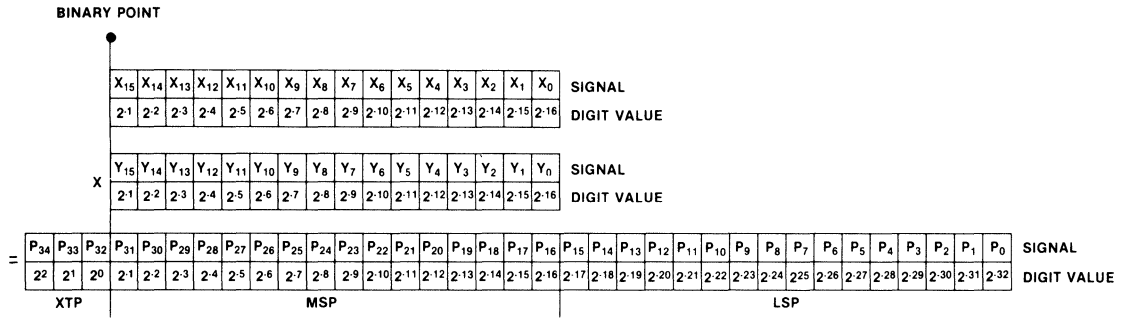


Figure 3: Integer Twos Complement Notation

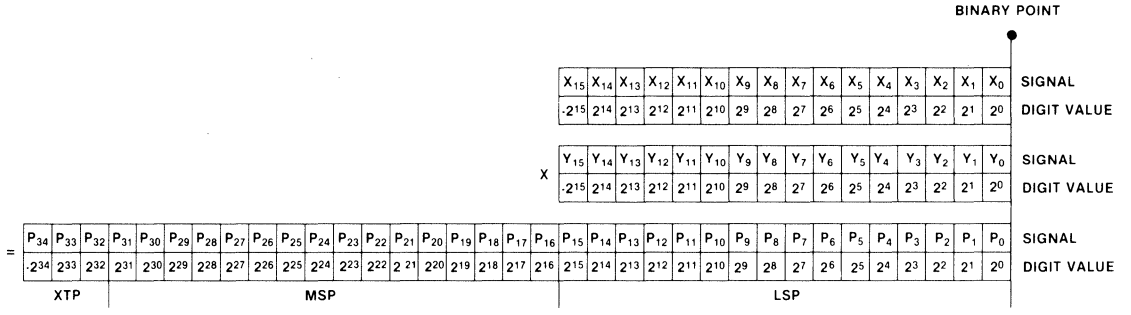
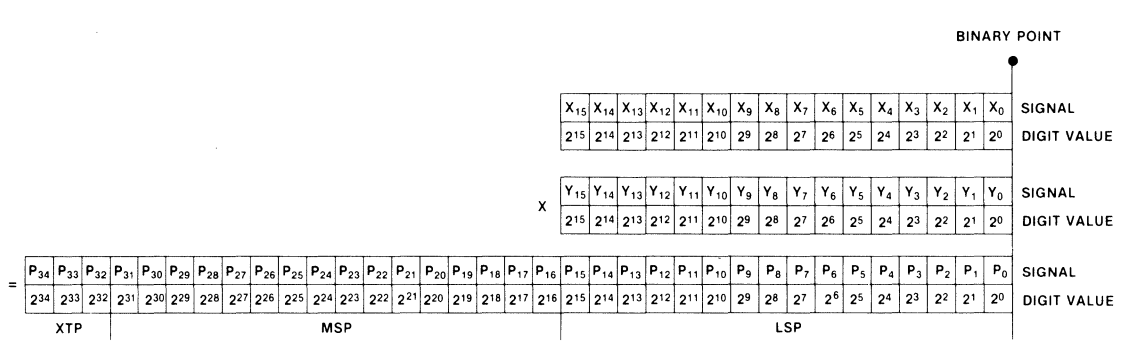


Figure 4: Integer Unsigned Magnitude Notation



Recommended Operating Conditions

Symbol	Parameter		Conditions	Limits	Units
V_{CC}	Supply Voltage (unless otherwise specified)			2.0 to 6.0	V
V_I	Input Voltage			0 to V_{CC}	V
V_O	Output Voltage			0 to V_{CC}	V
T_A	Operating Temperature	74AC/ACT 54AC/ACT		−40 to +85 −55 to +125	°C °C
Sr	Maximum Slew Rate (except for Schmitt inputs)		V_{IN} V_{meas} V_{CC}@4.5V V_{CC}@5.5V	0.8 to 2.0 0.8 to 2.0 10.0 8.0	V V ns ns

Absolute Maximum Ratings*

Symbol	Parameter	Conditions	Limits	Units
V_{CC}	Supply Voltage		−0.5 to 7.0	V
I_{IK} V_I	DC Input Diode Current or DC Input Voltage	$V_I = 0.5$ $V_I = V_{CC} + 0.5$	−20 20 −0.5 to V_{CC} + 0.5	mA mA V
I_{OK} V_O	DC Output Diode Current or DC Output Voltage	$V_O = -0.5$ $V_O = V_{CC} + 0.5$	−20 20 −0.5 to V_{CC} + 0.5	mA mA V
I_O	DC Output Source or Sink Current, Per Output Pin		±15	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		±20	mA
T_{STG}	Storage Temperature		−65 to 150	°C

*Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

AC Test Conditions

Input Pulse Levels	GND to 3.0 V
Input Rise and Fall Times	3 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load	See Figures 5 and 6

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol		Max	Unit	Conditions
C_{IN}	Input Capacitance	7.0	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	5.0	pF	V_{OUT} = 0V

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74AC/ACT 25°C	54AC/ACT	74AC/ACT	Units	Conditions
		Typ	Guaranteed Limit			
I_{IN}	Maximum Input Current		0.1	10.0	1.0	μA	V_{CC} = Max V_{IN} = V_{CC}
I_{OZ}	Maximum 3-State Current		0.5	10.0	5.0	μA	High Z, V_{CC} = Max V_{OUT} = 0 to V_{CC}
I_{CCQ}	Supply Current, Quiescent	1.0	2.0	10.0	10.0	mA	V_{CC} = Max, V_{IN} = 0 V TSL, TSM, TSX = 5.0 V
I_{CCD}	Supply Current, 12.4 MHz Loaded	300		325	325	mA	V_{CC} = Max, f = 12.4 MHz TSL, TSM, TSX = 5.0 V Test Load: See Note 1
I_{CCD}	Supply Current, 20 MHz Loaded	325		350	350	mA	V_{CC} = Max, f = 20 MHz TSL, TSM, TSX = 5.0 V Test Load: See Note 1
V_{OH}	Minimum High Level Output	4.49	4.4	4.4	4.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 4.5 V
		5.49	5.4	5.4	5.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = 20 μA, V_{CC} = 5.5 V
			3.86	3.70	3.76	V	I_{OH} = −8 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = −8 mA, V_{CC} = 5.5 V
V_{OL}	Maximum High Level Output	0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 20 μA, V_{CC} = 4.5 V
		0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 20 μA, V_{CC} = 5.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 4.5 V
			0.32	0.4	0.37	V	I_{OL} = 8 mA, V_{CC} = 5.5 V
I_{OLD}	Minimum Dynamic Output Current			32	32	mA	V_{CC} = 5.5 V V_{OLD} = 2.2 V
I_{OHD}	Minimum Dynamic Output Current			−32	−32	mA	V_{CC} = 5.5 V V_{OHD} = 3.3 V

Note 1: Test Load 50 pf, 500 ohm to Ground

AC Characteristics

Symbol	Parameter	Vcc* (V)	54AC				74AC				Units	Fig. No.
			$T_A = -55°C$ to $+125°C$				$T_A = -40°C$ to $+85°C$					
			1010-60		1010-70		1010-55		1010-65			
			Min	Max	Min	Max	Min	Max	Min	Max		
t_{MA}	Multiply-Accumulate Time	3.3 5.0									ns	5
t_D	Output Delay	3.3 5.0									ns	5
t_{ENA}	3-State Output[1] Enable Delay	3.3 5.0									ns	6
t_{DIS}	3-Stage Output[1] Disable Delay	3.3 5.0									ns	6
t_s	Input Register Setup Time	3.0 5.0									ns	7, 9
t_h	Input Register Hold Time	3.3 5.0									ns	7, 9
t_w	Clock Pulse Width	3.3 5.0									ns	9

Note 1: Transition is measured to ±500 mV from steady state voltage with loading specified in Figure 6.

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	54ACT				74ACT				Units	Fig. No.
			$T_A = -55°C$ to $+125°C$				$T_A = -40°C$ to $+85°C$					
			1010-60		1010-70		1010-55		1010-65			
			Min	Max	Min	Max	Min	Max	Min	Max		
t_{MA}	Multiply-Accumulate Time	5.0						55.0		65.0	ns	5
t_D	Output Delay	5.0						19.5		19.5	ns	5
t_{ENA}	3-State Output[1] Enable Delay	5.0						14.0		14.0	ns	6
t_{DIS}	3-Stage Output[1] Disable Delay	5.0						14.0		14.0	ns	6
t_s	Input Register Setup Time	5.0					5.0		5.0		ns	7, 9
t_h	Input Register Hold Time	5.0					1.0		1.0		ns	7, 9
t_w	Clock Pulse Width	5.0					3.5		3.5		ns	9

Note 1: Transition is measured to ±500 mV from steady state voltage with loading specified in Figure 6.

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Figure 5: AC Output Test Load

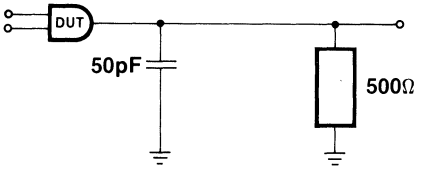


Figure 6: Output 3-State Delay Load

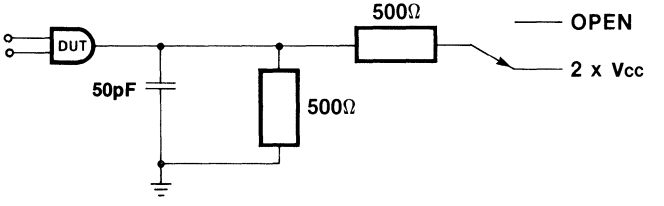


Figure 7: Setup and Hold Time

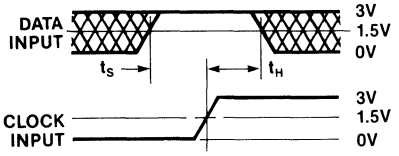


Figure 8: State Control Timing

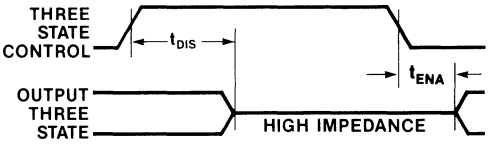
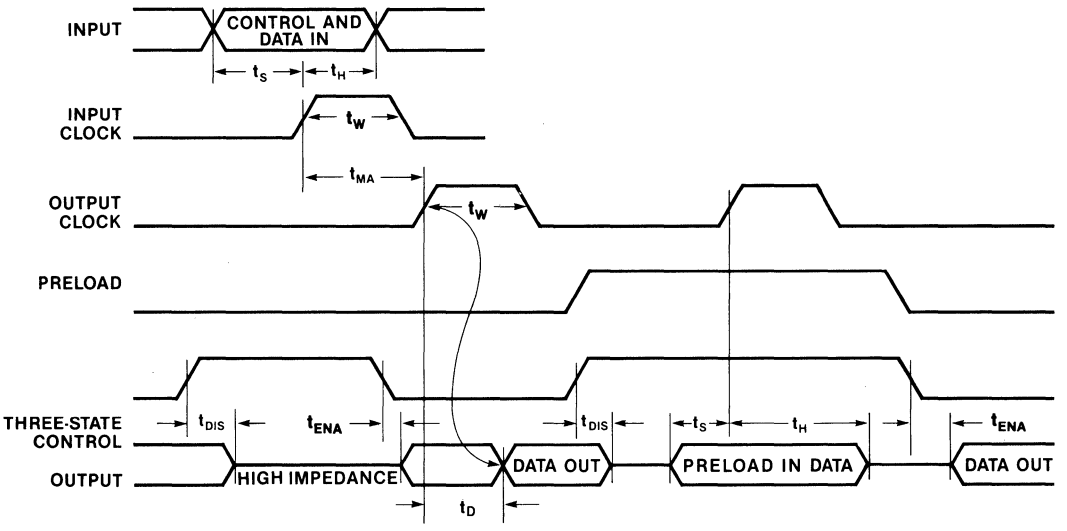


Figure 9: Timing Diagram



5

54AC/74AC1016 • 54ACT/74ACT1016

16 × 16 Parallel Multiplier

Description

The 'AC/ACT1016 is a high-speed, low power 16 × 16-bit parallel multiplier that is ideally suited for real-time digital signal processing applications. Fabricated using advanced FACT technology, the '1016 offers a very low power alternative and exceptional performance.

The 'AC/ACT1016 is a pin and functional replacement for TRW's MPY016H; the 'AC/ACT1016 operates from a single Vcc supply and is compatible with standard TTL logic levels.

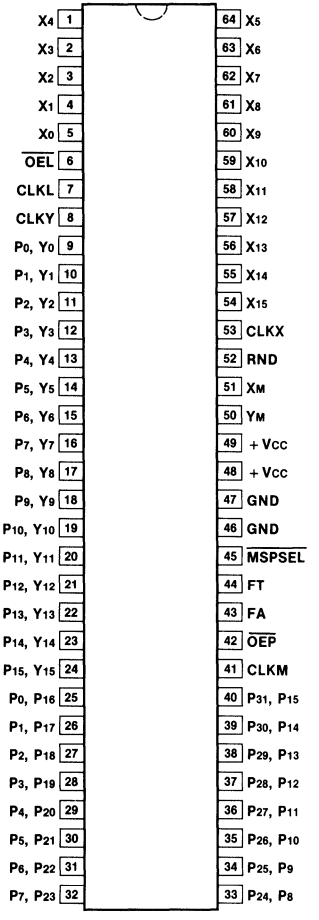
The architecture of the 'ACT1016 features one 16-bit port dedicated to the X input registers (controlled by CLKX), one 16-bit I/O port used for loading the Y input registers (controlled by CLKY) and for displaying the Least Significant Product (LSP), and one 16-bit output port multiplexed between displaying the Least Significant Product (LSP) and the Most Significant Product (MSP). The I/O port direction is controlled by $\overline{OEL}$ and the output port 3-state control is controlled by $\overline{OEP}$. The result is registered if FT is LOW (controlled by CLKL for the LSP and CLKM for the MSP) and unregistered if FT is held HIGH.

Twos complement, unsigned magnitude and mixed mode multiplications are possible through the twos complement X and Y mode controls, XM and YM, respectively. These mode controls are registered, controlled by the input clocks CLKX and CLKY.

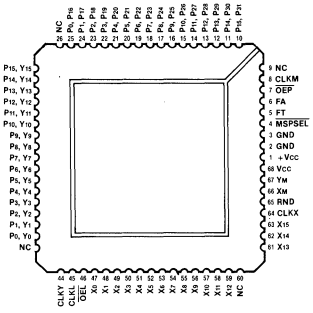
Result rounding is controlled by the registered RND signal (controlled by both CLKX and CLKY). Selection of one of the two rounding modes is determined by the FA signal.

- **16 × 16 Parallel Multiplier**
- **Selectable Rounding Modes**
- **Twos Complement, Unsigned Magnitude and Mixed Mode Multiplication**
- **Pin and Functionally Compatible with TRW MPY016H**
- **Provides Low Voltage, High-Speed Operation**
- **Single Vcc Supply**
- **± 2000 V ESD Protection**
- **Source/Sink 8 mA**
- **3-State Outputs**
- **'ACT1016 has TTL-Compatible Inputs**

Connection Diagrams



Pin Assignment for DIP



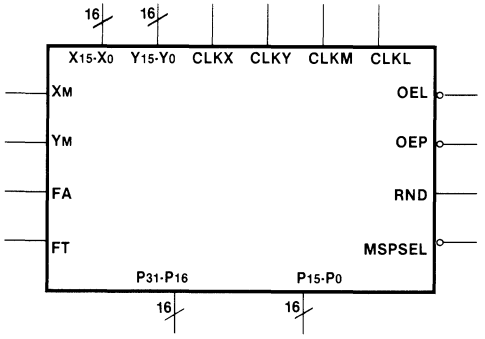
Pin Assignment for PCC

Ordering Code: See Section 6

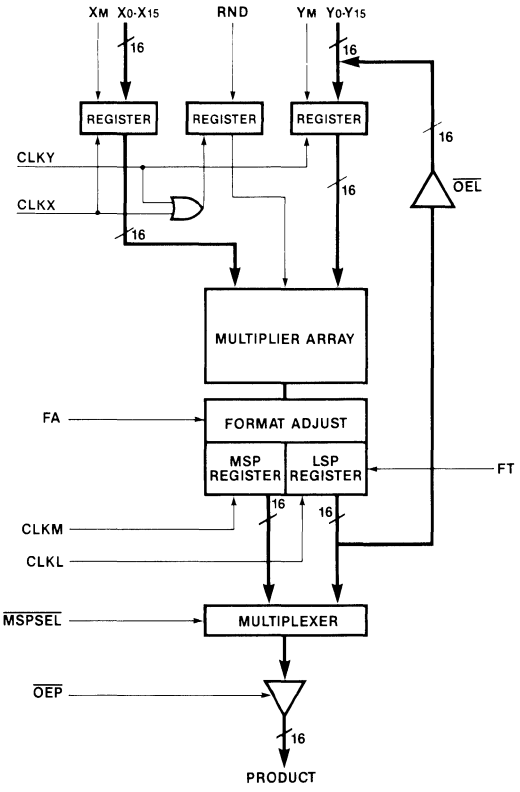
Pin Names

X_{15} - X_0	Multiplicand Data Inputs
Y_{15} - Y_0	Multiplier Data Inputs
CLKX, CLKY	Input Clocks
CLKM	Input Clock, MSP
CLKL	Input Clock, LSP
X_M, Y_M	Mode Control Inputs
FA	Format Adjust Control
FT	Format Transparent Control
$\overline{OEL}$	3-State Enable, LSP Routing
$\overline{OEP}$	3-State Enable, Product Output Port
RND	Round Control, MSP
$\overline{MSPSEL}$	MSP Select
P_{31} - P_{16}	MSP Outputs
P_{15} - P_0	LSP Outputs

Logic Symbol



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

5

Signal Descriptions

Inputs

X_{IN} (X_{15} - X_0)
Sixteen multiplicand data inputs.

Y_{IN} (Y_{15} - Y_0)
Sixteen multiplier data inputs. This is also an output port for P_{15} - P_0.

Input Clocks

CLKX
The rising edge of this clock loads the X_{15} - X_0 data input register along with the X mode and round registers.

CLKY
The rising edge of this clock loads the Y_{15} - Y_0 data input register along with the Y mode and round registers.

CLKM
The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL
The rising edge of this clock loads the Least Significant Product (LSP) register.

Controls

X_M, Y_M
Mode control inputs for each data word. A LOW input designates an unsigned data input, and a HIGH input designates twos complement.

FA
When the Format Adjust (FA) Control is HIGH, a full 32-bit product is selected. When this control is LOW, a left-shifted 31-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional twos complement applications (see multiplier input/output formats).

FT
When the Format Transparent (FT) Control is HIGH, both the MSP and LSP registers are transparent.

$\overline{OEL}$
The $\overline{OEL}$ input is the 3-state enable for routing LSP through Y_{IN}/LSP_{OUT} port.

$\overline{OEP}$
The $\overline{OEP}$ is the 3-state enable for the product output port.

RND
The Round control is used for the rounding of the MSP. When this control is HIGH, A '1' is added to the Most Significant Bit (MSB) of the LSP. Note that this bit depends on the state of the format adjust (FA) control.

If FA is LOW when RND is HIGH, a '1' will be added to the 2^{-16} bit (P_{14}). If FA is HIGH when RND is HIGH, a '1' will be added to the 2^{-15} bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH.

Note also that rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

$\overline{MSPSEL}$
When $\overline{MSPSEL}$ is LOW, the Most Significant Product (MSP) is selected. When HIGH, the Least Significant Product (LSP) is available at the product output port.

Outputs

MSP (P_{31} - P_0)
The MSP is the Most Significant Product output.

LSP (P_{15} - P_0)
The LSP is the Least Significant Product output.

$Y_{15\text{-}0}$/LSP_{OUT} (Y_{15} - Y_0 or P_{15} - P_0)
This is the Least Significant Product (LSP) output available when $\overline{OEL}$ is LOW. It is also an output port for Y_{15} - Y_0.

Figure 1: Fractional Twos Complement Notation

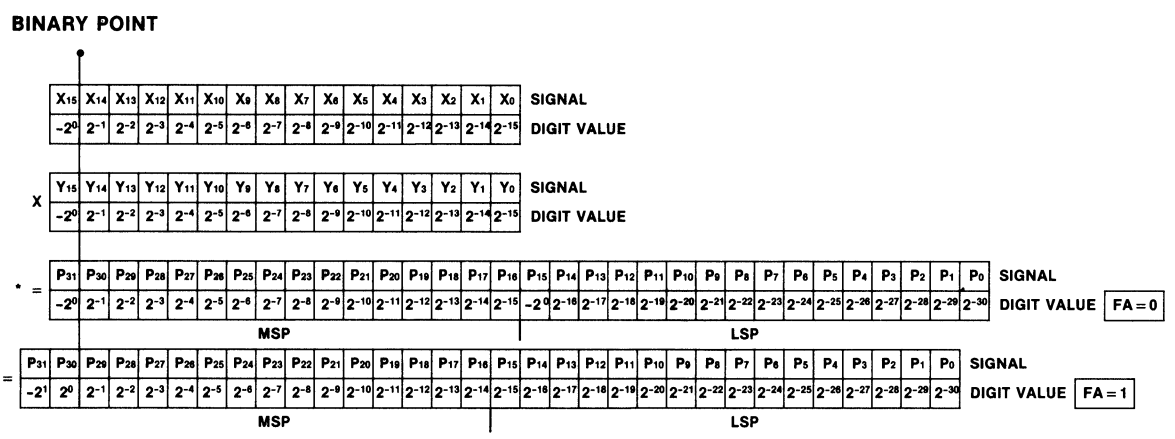


Figure 2: Fractional Unsigned Magnitude Notation

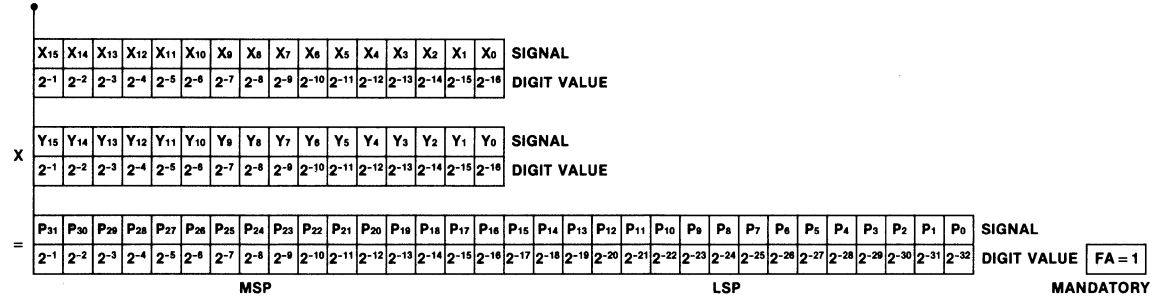
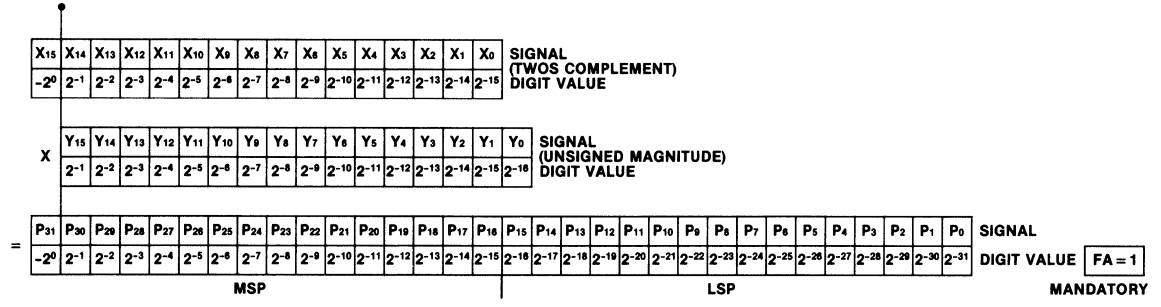


Figure 3: Fractional Mixed-Mode Notation



*In this format an overflow occurs in the attempted multiplication of the twos complement number 1000...0 with 1000.00 yielding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

Figure 4: Integer Twos Complement Notation

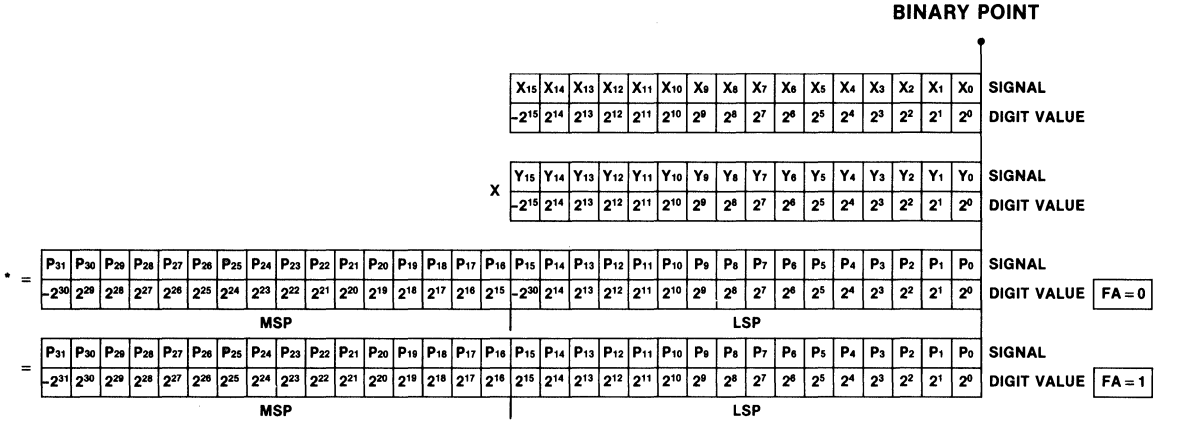


Figure 5: Integer Unsigned Magnitude Notation

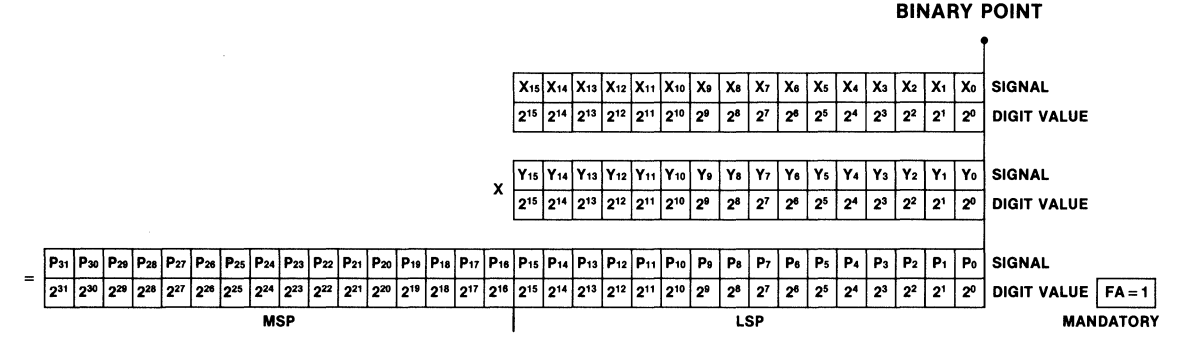
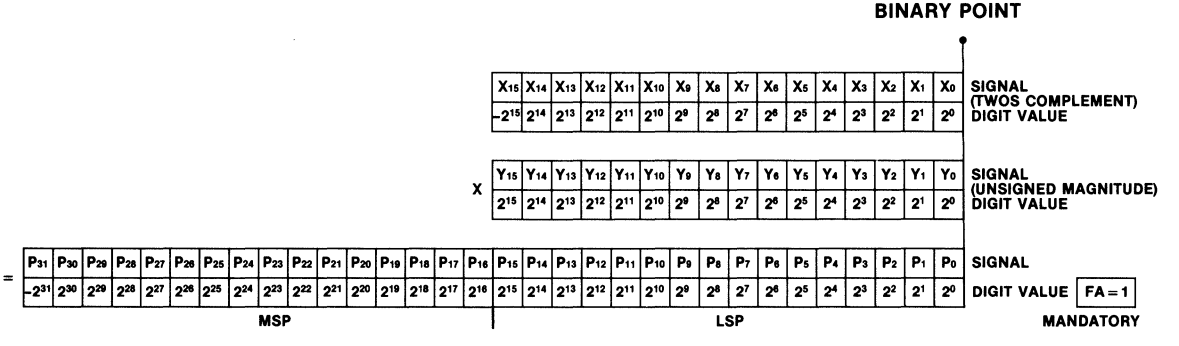


Figure 6: Integer Mixed Mode Notation



*In this format an overflow occurs in the attempted multiplication of the twos complement number 1000...0 with 1000.00 yielding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

Recommended Operating Conditions

Symbol	Parameter		Conditions	Limits	Units
V_{CC}	Supply Voltage (unless otherwise specified)			2.0 to 6.0	V
V_I	Input Voltage			0 to V_{CC}	V
V_O	Output Voltage			0 to V_{CC}	V
T_A	Operating Temperature	74AC/ACT 54AC/ACT		−40 to +85 −55 to +125	°C °C
S_r	Maximum Slew Rate (except for Schmitt inputs)		V_{IN} V_{meas} V_{CC}@4.5V V_{CC}@5.5V	0.8 to 2.0 0.8 to 2.0 10.0 8.0	V V ns ns

Absolute Maximum Ratings*

Symbol	Parameter	Conditions	Limits	Units
V_{CC}	Supply Voltage		−0.5 to 7.0	V
I_{IK} V_I	DC Input Diode Current or DC Input Voltage	$V_I = 0.5$ $V_I = V_{CC} + 0.5$	−20 20 −0.5 to V_{CC} + 0.5	mA mA V
I_{OK} V_O	DC Output Diode Current or DC Output Voltage	$V_O = -0.5$ $V_O = V_{CC} + 0.5$	−20 20 −0.5 to V_{CC} + 0.5	mA mA V
I_O	DC Output Source or Sink Current, Per Output Pin		±15	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		±20	mA
T_{STG}	Storage Temperature		−65 to +150	°C

*Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

AC Test Conditions

Input Pulse Levels	GND to 3.0 V
Input Rise and Fall Times	3 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load	See Figures 7 and 8

Capacitance

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Input Capacitance	7.0	pF	$V_{IN} = 0$ V
C_{OUT}	Output Capacitance	5.0	pF	$V_{OUT} = 0$ V

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74AC/ACT		54AC/ACT	74AC/ACT	Units	Conditions
		Typ	Guaranteed Limit				
I_{IN}	Maximum Input Current		± 0.1	± 10.0	± 1.0	μA	V_{CC} = Max V_{IN} = V_{CC}, 0
I_{OZ}	Maximum 3-State Current		0.5	10.0	5.0	μA	High Z, V_{CC} = Max V_{OUT} = 0, V_{CC}
I_{CCQ}	Supply Current, Quiescent	0.50	2.0	10.0	10.0	mA	V_{CC} = Max, V_{IN} = 0 V
I_{CCD}	Supply Current, 12.4 MHz Loaded	300		325	325	mA	V_{CC} = Max, f = 12.4 MHz Test Load: See Note 1
I_{CCD}	Supply Current, 20 MHz Loaded	325		350	350	mA	V_{CC} = Max, f = 20 MHz Test Load: See Note 1
V_{OH}*	Minimum HIGH Level Output	4.49	4.4	4.4	4.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = -50 μA, V_{CC} = 4.5 V
		5.49	5.4	5.4	5.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = -50 μA, V_{CC} = 5.5 V
			3.86	3.70	3.76	V	I_{OH} = – 8 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = – 8 mA, V_{CC} = 5.5 V
V_{OL}*	Maximum HIGH Level Output	0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 50 μA, V_{CC} = 4.5 V
		0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 50 μA, V_{CC} = 5.5 V
			0.45	0.50	0.50	V	I_{OL} = 8 mA, V_{CC} = 4.5 V
			0.45	0.50	0.50	V	I_{OL} = 8 mA, V_{CC} = 5.5 V
I_{OLD}	Minimum Dynamic Output Current			32	32	mA	V_{CC} = 5.5 V, V_{OLD} = 2.2 V. See Note 2.
I_{OHD}	Minimum Dynamic Output Current			– 32	– 32	mA	V_{CC} = 5.5 V, V_{OHD} = 3.3 V. See Note 2.

Note 1: Test Load 50 pF, 500 ohm to Ground

Note 2: Only one output loaded at a time, maximum duration of test 2 ms.

*All outputs loaded.

AC Characteristics

Symbol	Parameter	Vcc* (V)	54AC				74AC				Units	Fig. No.
			$T_A = -55°C$ to $+125°C$				$T_A = -40°C$ to $+85°C$					
			1016-80		1016-65		1016-65		1016-55			
			Min	Max	Min	Max	Min	Max	Min	Max		
t_{MUC}	Unclocked Multiply Time	3.3 5.0									ns	11
t_{MC}	Clocked Multiply Time	3.3 5.0									ns	11, 12
t_{PDSEL}	$\overline{\text{MSPSEL}}$ to Product Out	3.3 5.0									ns	11
t_{PDP}	Output Clock to P	3.3 5.0									ns	11
t_{PDY}	Output Clock to Y	3.3 5.0									ns	11
t_{ENA}	3-State Enable Time[2]	3.3 5.0									ns	10
t_{DIS}	3-State Disable Time[2]	3.3 5.0									ns	10
t_{HCL}	Clock LOW Hold Time CLKXY Relative to CLKML[1]	3.3 5.0									ns	11, 12
t_s	Setup Time X,Y, RND	3.3 5.0									ns	9, 11
t_h	Hold Time X, Y, RND	3.3 5.0									ns	9, 11
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0									ns	11

Note 1: To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.

Note 2: Transition is measured to ±500 mV from steady state voltage with loading specified in Figure 8.

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	Vcc* (V)	54ACT				74ACT				Units	Fig. No.
			$T_A = -55°C$ to $+125°C$				$T_A = -40°C$ to $+85°C$					
			1016-80		1016-65		1016-65		1016-55			
			Min	Max	Min	Max	Min	Max	Min	Max		
t_{MUC}	Unclocked Multiply Time	5.0						80.0		65.0	ns	11
t_{MC}	Clocked Multiply Time	5.0						65.0		55.0	ns	11, 12
t_{PDSEL}	$\overline{\text{MSPSEL}}$ to Product Out	5.0						13.0		13.0	ns	11
t_{PDP}	Output Clock to P	5.0						20.0		20.0	ns	11
t_{PDY}	Output Clock to Y	5.0						20.0		20.0	ns	11
t_{ENA}	3-State Enable Time[2]	5.0						10.0		10.0	ns	10
t_{DIS}	3-State Disable Time[2]	5.0						12.5		12.5	ns	10
t_{HCL}	Clock LOW Hold Time CLKXY Relative to CLKML[1]	5.0					0		0		ns	11, 12
t_s	Setup Time X,Y, RND	5.0					5.5		5.5		ns	9, 11
t_h	Hold Time X, Y, RND	5.0					1.0		1.0		ns	9, 11
t_w	Clock Pulse Width HIGH or LOW	5.0					3.5		3.5		ns	11

Note 1: To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.

Note 2: Transition is measured to ±500 mV from steady state voltage with loading specified in Figure 8.

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Figure 7: AC Output Test Load

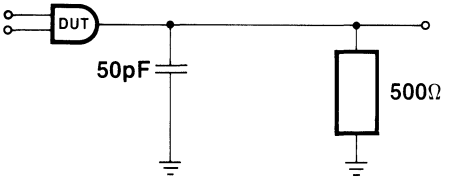


Figure 8: Output 3-State Delay Load

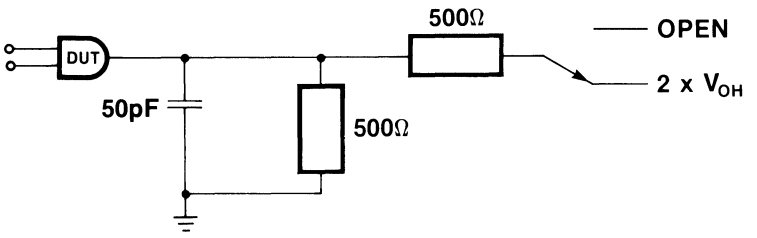


Figure 9: Setup and Hold Time

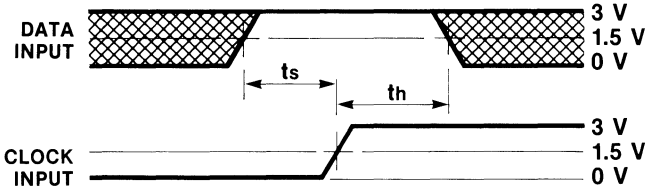


Figure 10: 3-State Control Timing Diagram

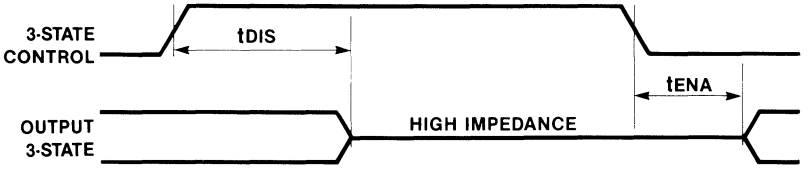


Figure 11: '1016 Timing Diagram

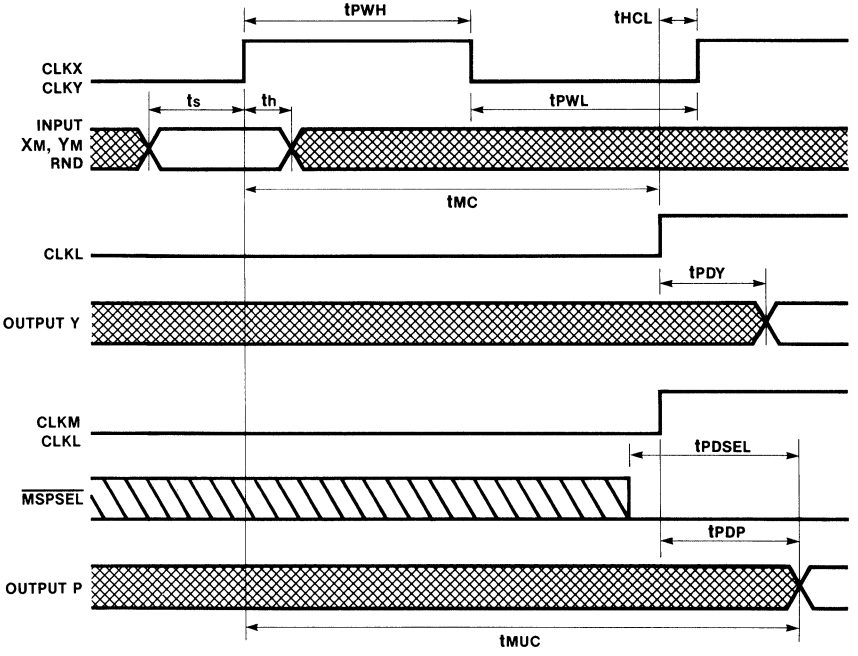
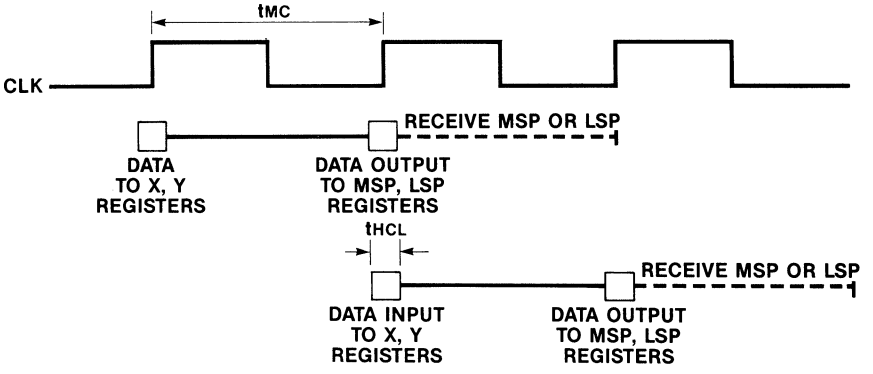


Figure 12: Simplified Timing Diagram — Typical Application



54AC/74AC1017 • 54ACT/74ACT1017

16 × 16 Parallel Multiplier

Description

The 'AC/'ACT1017 is a high-speed, low power 16 × 16-bit parallel multiplier that is ideally suited for real-time digital signal processing applications. Fabricated using advanced FACT technology, the 'AC/'ACT1017 offers a very low power alternative and exceptional performance.

The 'AC/'ACT1017 is a pin and functional replacement for AMD's Am29517; the 'AC/'ACT1017 operates from a single V_{CC} supply and is compatible with standard TTL logic levels.

The 'AC/'ACT1017 performs the same mathematical functions as the 'AC/'ACT1016 but has a single clock, CLK, and three register enables making it ideal for microcoded applications.

The architecture of the 'AC/'ACT1017 features one 16-bit port dedicated to the X input registers (enabled by $\overline{ENX}$), one 16-bit I/O port used to load the Y input registers (controlled by $\overline{ENY}$) and for displaying the Least Significant Product (LSP), and one 16-bit output port multiplexed between displaying the Least Significant Product (LSP) and the Most Significant Product (MSP).

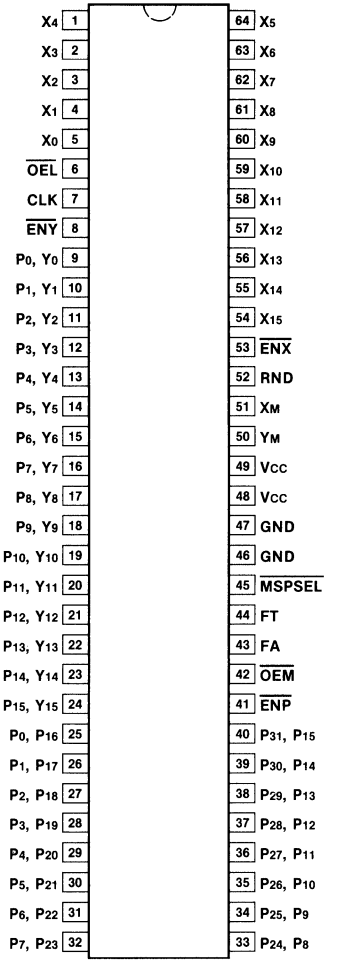
The I/O port direction is controlled by $\overline{OEL}$ and the output port 3-state control is controlled by $\overline{OEM}$.

The result is registered if FT is LOW (all 32 register bits enabled by $\overline{ENP}$) and unregistered if FT is held HIGH.

Twos complement, unsigned magnitude and mixed mode multiplications are possible through the twos complement X and Y mode controls, X_M and Y_M, respectively. These mode controls are registered, controlled by the input clock (CLK).

Result rounding is controlled by the registered RND signal (controlled by CLK). Selection of one of the two rounding modes is determined by the FA signal.

Connection Diagram



Pin Assignment for DIP

5

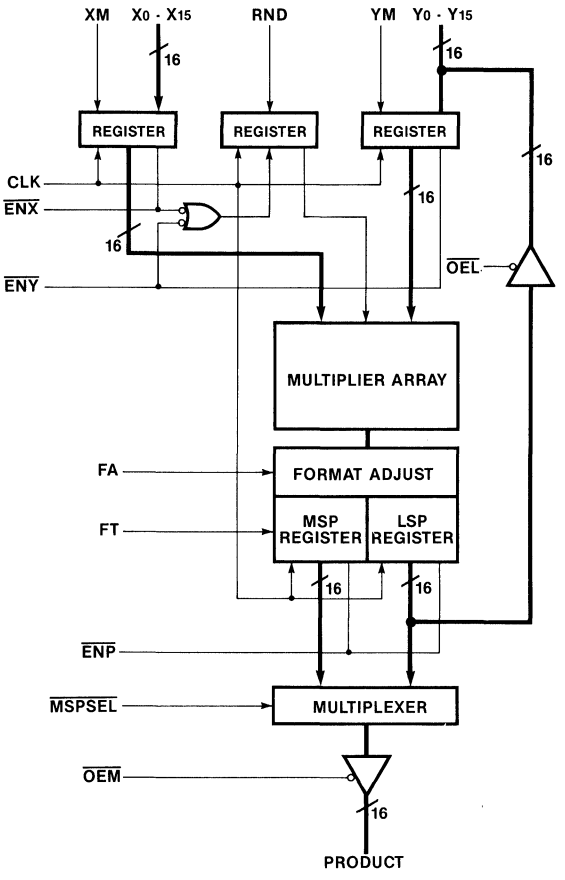
- **16 × 16 Parallel Multiplier**
- **Selectable Rounding Modes**
- **Twos Complement, Unsigned Magnitude and Mixed Mode Multiplication**
- **Pin and Functionally Compatible with Am29517**
- **'ACT1017 Interfaces Directly to TTL**
- **'AC1017 Provides Low Voltage, High-Speed Operation**
- **Single V_{CC} Supply**
- **± 2000 V ESD Protection**
- **High Drive 8 mA Outputs**
- **Single Input Clock**

Pin Names

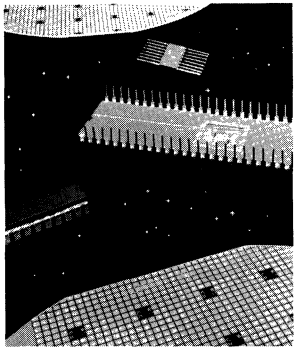
X_{15} - X_0	Multiplicand Data Inputs
Y_{15} - Y_0	Multiplier Data Inputs
CLK	Input Clock
$\overline{ENX}$	Register Enable, X_{15} - X_0
$\overline{ENY}$	Register Enable, Y_{15} - Y_0
$\overline{ENP}$	Register Enable, MSP and LSP
X_M, Y_M	Mode Control Inputs
FA	Format Adjust Control
FT	Format Transparent Control
$\overline{OEL}$	3-State Enable, LSP Routing
$\overline{OEM}$	3-State Enable, MSP Routing
RND	Round Control, MSP
$\overline{MSPSEL}$	MSP Select
P_{31} - P_{16}	MSP Outputs
P_{15} - P_0	LSP Outputs

Ordering Code: See Section 6

Logic Diagram



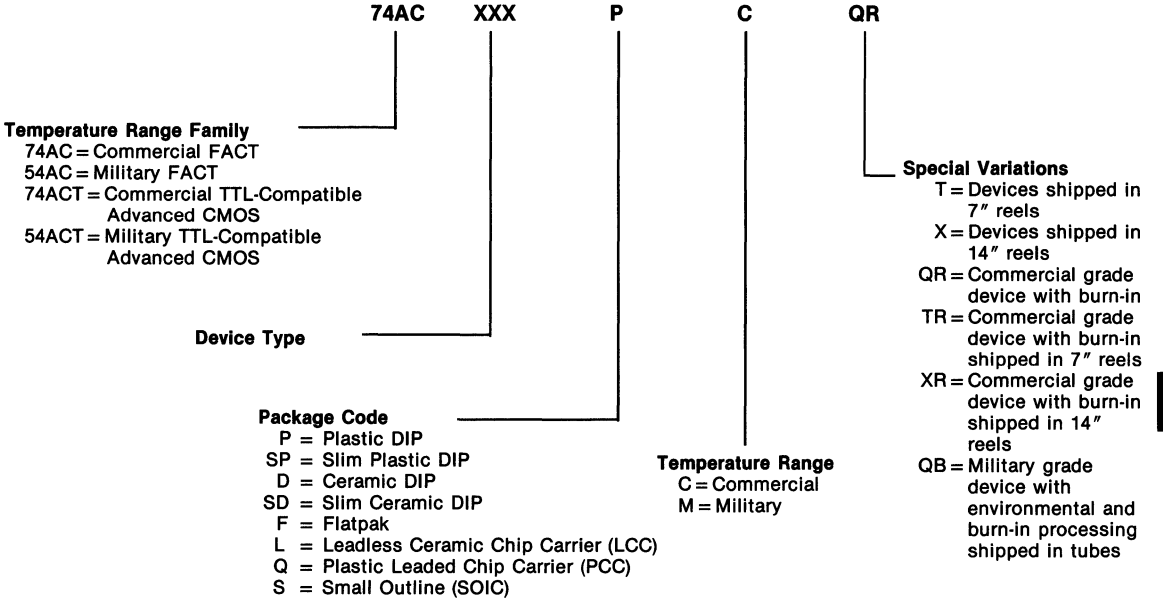
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



FAIRCHILD

Ordering Information/ Package Outlines

The Product Index and Selection Guide in Section 1 lists only the basic device numbers. This basic number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



Package	Package Code
Plastic DIP	P
Slim Plastic DIP	SP
Ceramic DIP	D
Slim Ceramic DIP	SD
Flatpak	F
Leadless Ceramic Chip Carrier (LCC)	L
Plastic Chip Carrier (PCC)	Q
Small Outline (SOIC)	S

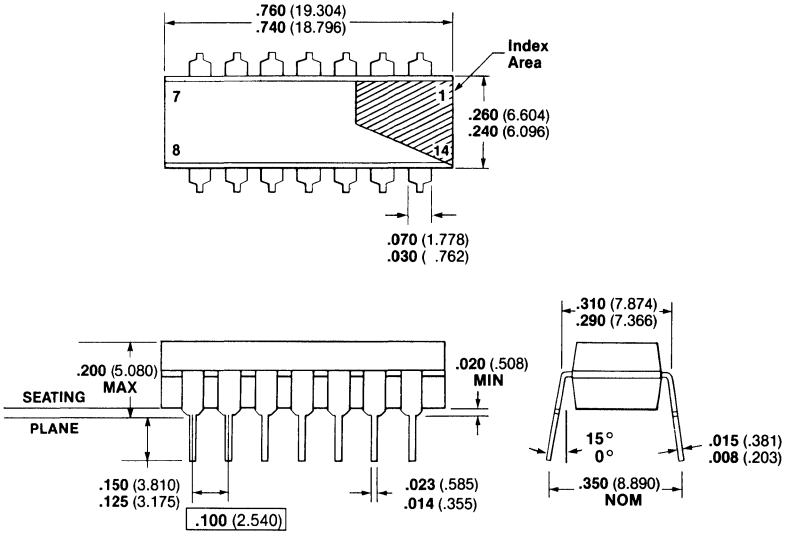
Temperature Range	Temperature Code
Commercial	
-40°C to +85°C	C
Military	
-55°C to +125°C	M

Package Outlines

The package outlines indicated above are shown in the detailed outline drawings in this section.

14 Lead Plastic Dual In-Line Package

Ordering Codes: 74ACXXXPC
74ACTXXXPC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

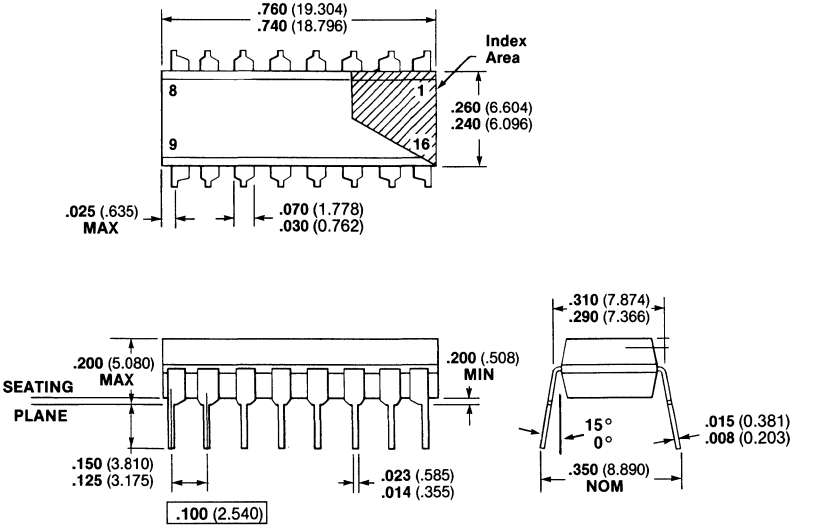
Notch or Lead One ID shall be within index area.

Leads are copper alloy, solder coated. Plastic is novolac epoxy.

Package weight is 0.9 gram.

16 Lead Plastic Dual In-Line Package

Ordering Codes: 74ACXXXPC
74ACTXXXPC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

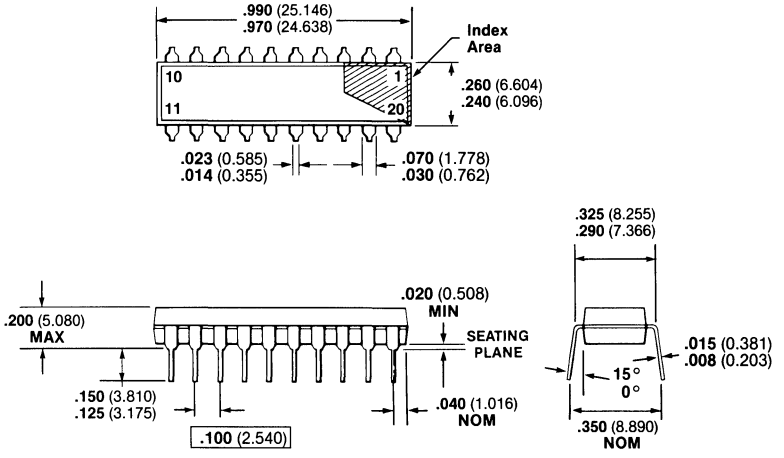
Notch or Lead One ID shall be within index area.

Leads are copper alloy, solder coated. Plastic is novolac epoxy.

Package weight is 0.9 gram.

20 Lead Plastic Dual In-Line Package

Ordering Codes: 74ACXXXPC
74ACTXXXPC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

Notch or Lead One ID shall be within index area.

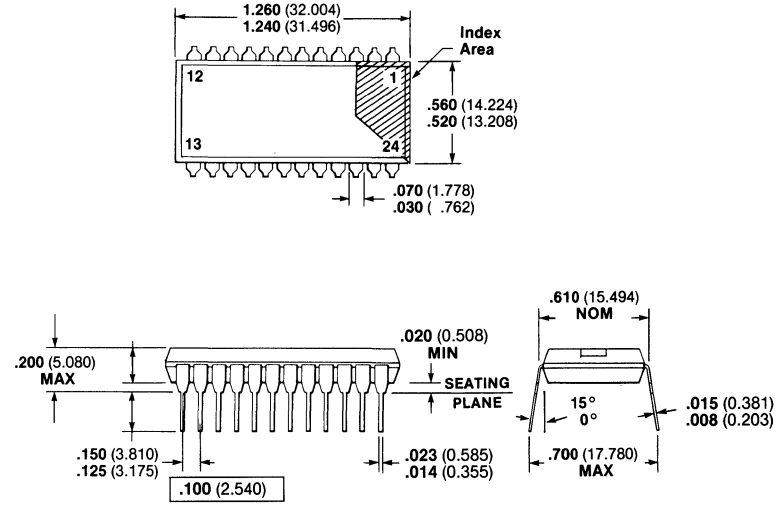
Leads are copper alloy, solder coated. Plastic is novolac epoxy.

Package weight is 1.2 grams.

6

24 Lead Plastic Dual In-Line Package

Ordering Codes: 74ACXXXPC
74ACTXXXPC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

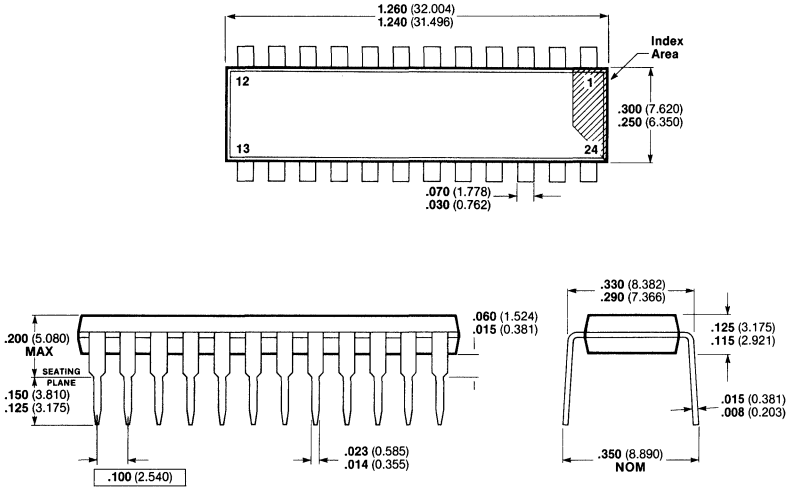
Notch or Lead One ID shall be within index area.

Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 4.0 grams.

24 Lead Slim (0.300″ Wide) Plastic Dual In-Line

Ordering Codes: 74ACXXXSPC
74ACTXXXSPC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

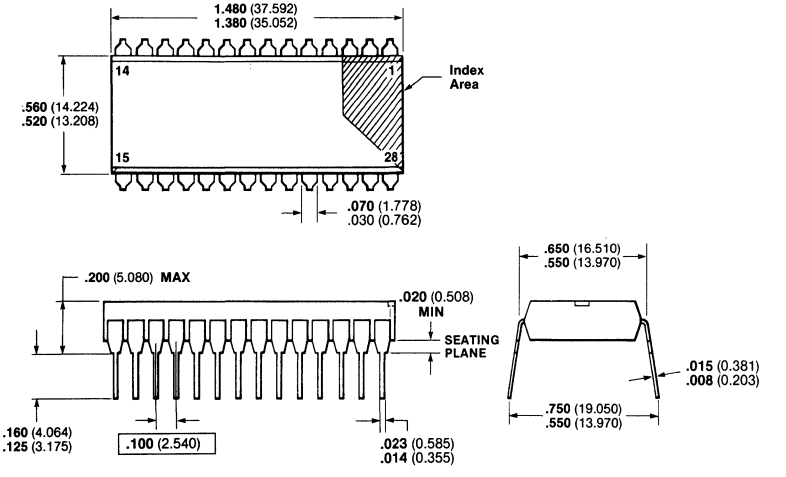
Notch or Lead One ID shall be within index area.

Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 1.8 grams.

28 Lead Plastic Dual In-Line Package

Ordering Codes: 74ACXXXPC
74ACTXXXPC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

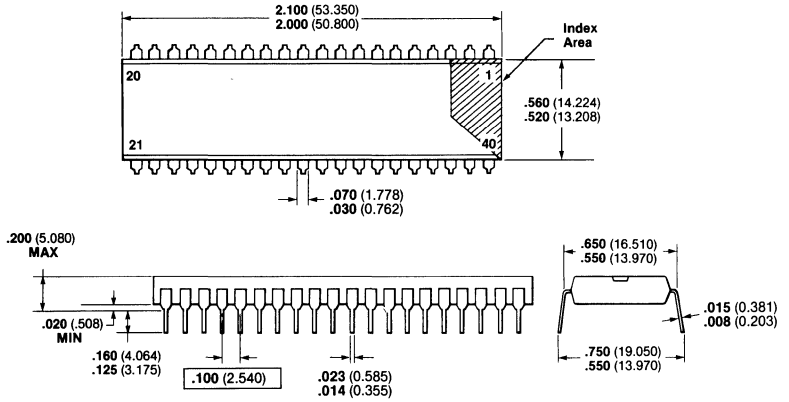
Notch or Lead One ID shall be within index area.

Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 4.2 grams.

40 Lead Plastic Dual In-Line Package

Ordering Codes: 74ACXXXPC
74ACTXXXPC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

Notch or Lead One ID shall be within index area.

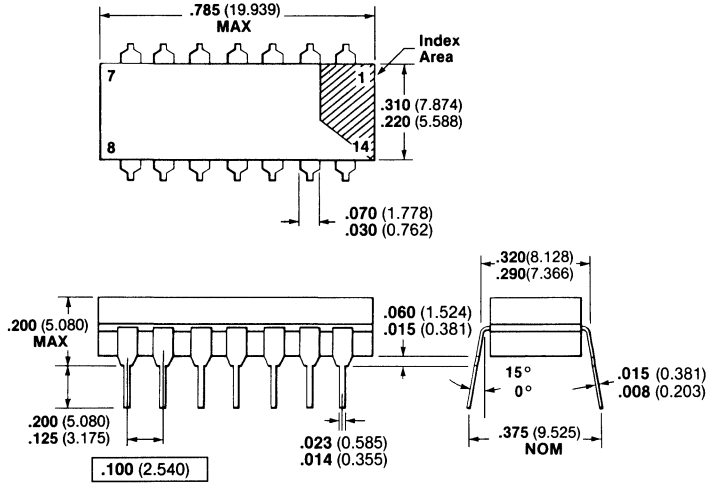
Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 6.5 grams.

6

14 Lead Ceramic Dual In-Line Package

Ordering Codes: 74ACXXXDC
74ACTXXXDC
54ACXXXDM
54ACTXXXDM



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

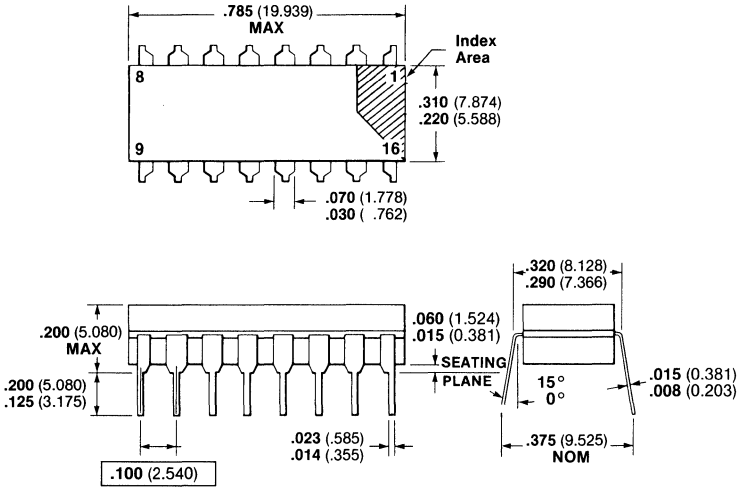
Notch or Lead One ID shall be within index area.

Leads are alloy 42, either tin plated or solder coated. Base and lid are 90% minimum alumina (black) sealed with glass.

Package weight is 2.0 grams.

16 Lead Ceramic Dual In-Line Package

Ordering Codes: 74ACXXXDC
74ACTXXXDC
54ACXXXDM
54ACTXXXDM



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

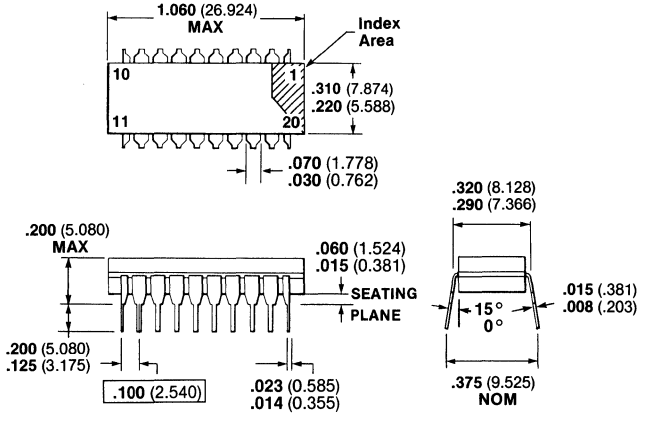
Notch or Lead One ID shall be within index area.

Leads are alloy 42, either tin plated or solder coated. Base and lid are 90% minimum alumina (black) sealed with glass.

Package weight is 2.2 grams.

20 Lead Ceramic Dual In-Line Package

Ordering Codes: 74ACXXXDC
74ACTXXXDC
54ACXXXDM
54ACTXXXDM



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

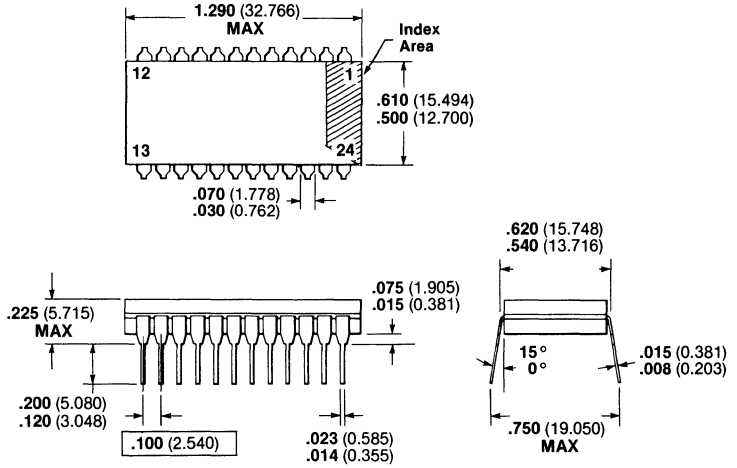
Notch or Lead One ID shall be within index area.

Leads are alloy 42, either tin plated or solder coated. Base and lid are 90% minimum alumina (black) sealed with glass.

Package weight is 2.4 grams.

24 Lead Ceramic Dual In-Line

Ordering Codes: 74ACXXXDC
74ACTXXXDC
54ACXXXDM
54ACTXXXDM



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

Notch or Lead One ID shall be within index area.

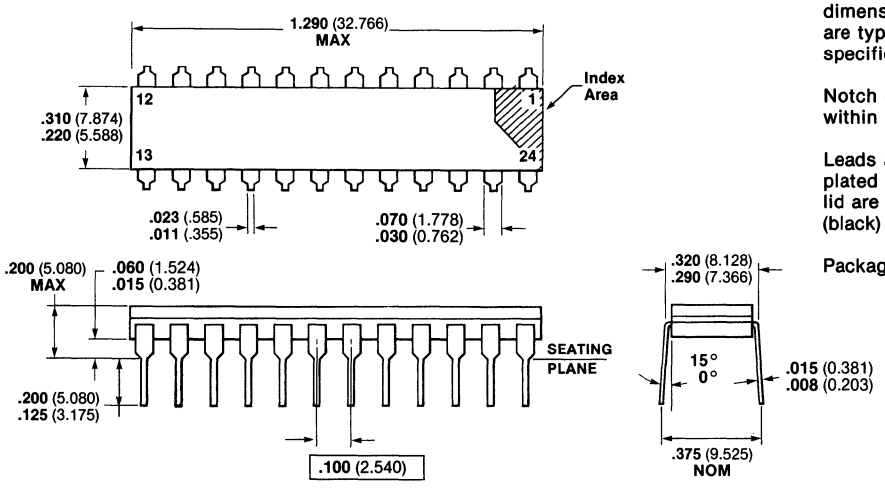
Leads are alloy 42, either tin plated or solder coated. Base and lid are 90% minimum alumina (black) sealed with glass.

Package weight is 6.8 grams.

6

24 Lead Slim (0.300″ Wide) Ceramic Dual In-Line

Ordering Codes: 74ACXXXSDC
74ACTXXXSDC
54ACXXXSDM
54ACTXXXSDM



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

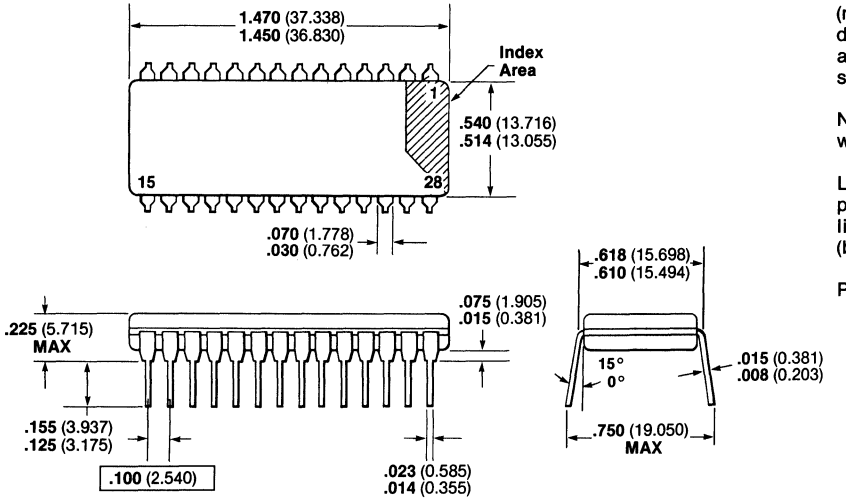
Notch or Lead One ID shall be within index area.

Leads are alloy 42, either tin plated or solder coated. Base and lid are 90% minimum alumina (black) sealed with glass.

Package weight is 3.9 grams.

28 Lead Ceramic Dual In-Line Package

Ordering Codes: 74ACXXXDC
74ACTXXXDC
54ACXXXDM
54ACTXXXDM



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

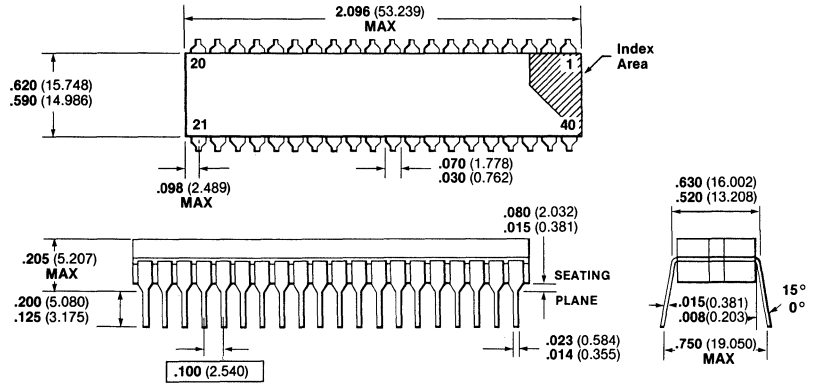
Notch or Lead One ID shall be within index area.

Leads are alloy 42, either tin plated or solder coated. Base and lid are 90% minimum alumina (black) sealed with glass.

Package weight is 7.5 grams.

40 Lead Ceramic Dual In-Line Package

Ordering Codes: 74ACXXXDC
74ACTXXXDC
54ACXXXDM
54ACTXXXDM



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

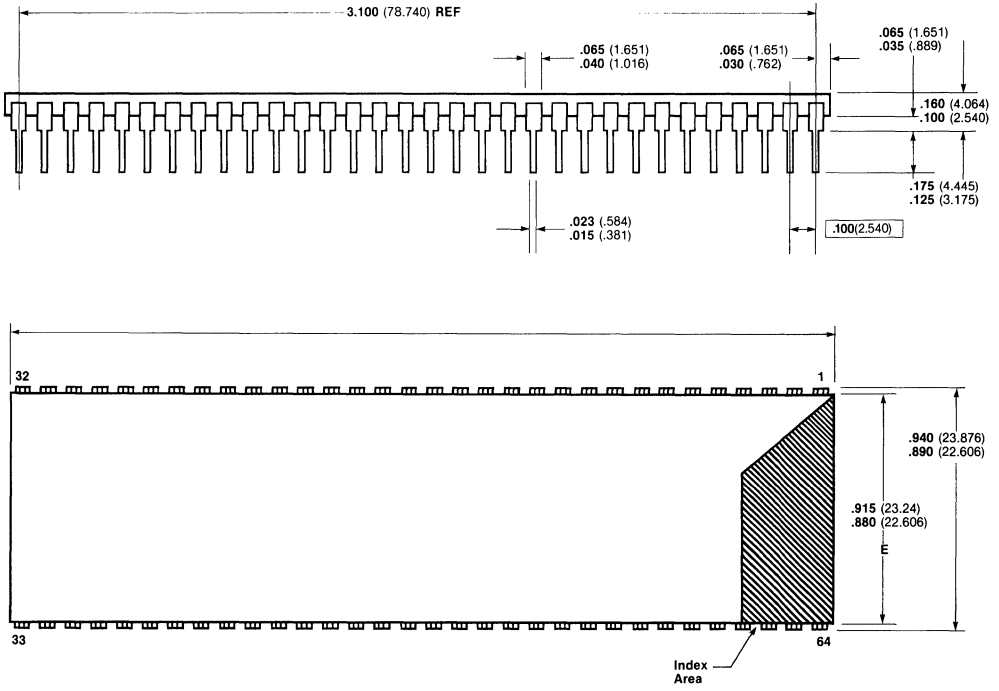
Notch or Lead One ID shall be within index area.

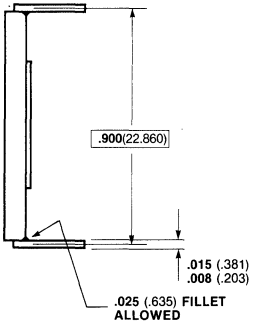
Leads are alloy 42, either tin plated or solder coated. Base and lid are 90% minimum alumina (black) sealed with glass.

Package weight is 12.0 grams.

64 Lead Side Brazed Dual In-Line Package

Ordering Codes: 74ACXXXDC
74ACTXXXDC
54ACXXXDM
54ACTXXXDM





Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

Notch or Lead One ID shall be within index area. Metallization in notch may be electrically active.

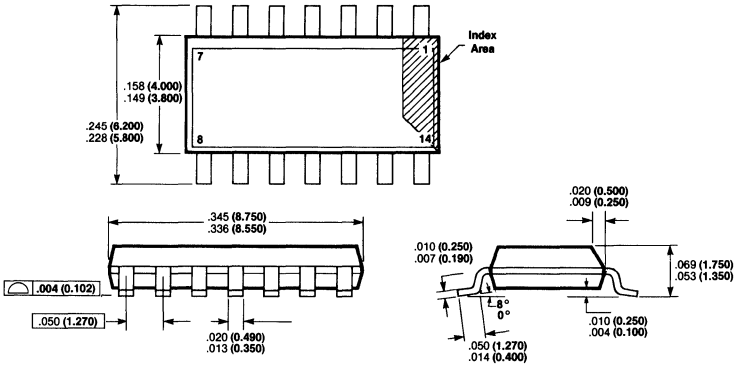
Leads are Kovar or alloy 42 with gold tin or solder coating. Substrate is 90% alumina (black). Lid is Kovar sealed with gold tin solder.

Package weight is 16.0 grams.

6

14 Lead Small Outline Integrated Circuit (SOIC)

Ordering Codes: 74ACXXXSC
74ACTXXXSC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in inches **(millimeters).** Controlling dimensions: Metric. Dimensions are typical unless otherwise specified.

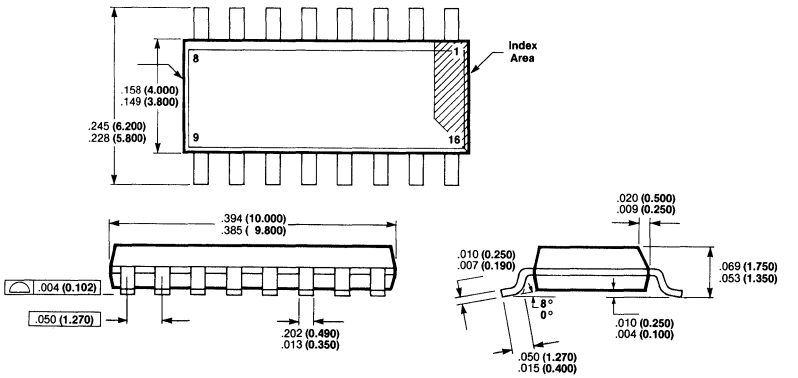
Notch or Lead One ID shall be within index area.

Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 0.14 gram.

16 Lead Small Outline Integrated Circuit (SOIC)

Ordering Codes: 74ACXXXSC
74ACTXXXSC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in inches **(millimeters).** Controlling dimensions: Metric. Dimensions are typical unless otherwise specified.

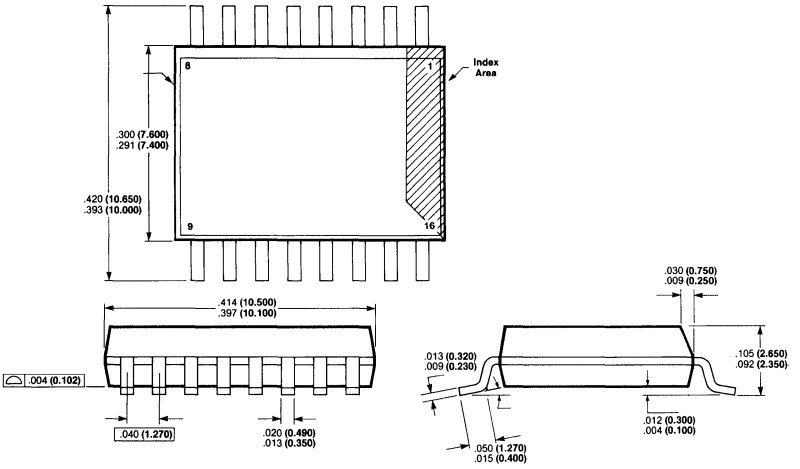
Notch or Lead One ID shall be within index area.

Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 0.16 gram.

16 Lead (0.300" Wide) Small Outline Integrated Circuit (SOIC)

Ordering Codes: 74ACXXXSC
74ACTXXXSC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in inches **(millimeters).** Controlling dimensions: Metric. Dimensions are typical unless otherwise specified.

Notch or Lead One ID shall be within index area.

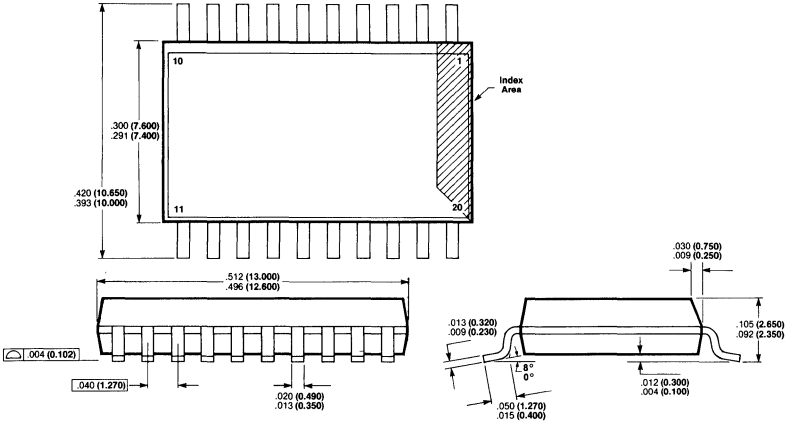
Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 0.46 gram.

6

20 Lead Small Outline Integrated Circuit (SOIC)

Ordering Codes: 74ACXXXSC
74ACTXXXSC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in inches **(millimeters).** Controlling dimensions: Metric. Dimensions are typical unless otherwise specified.

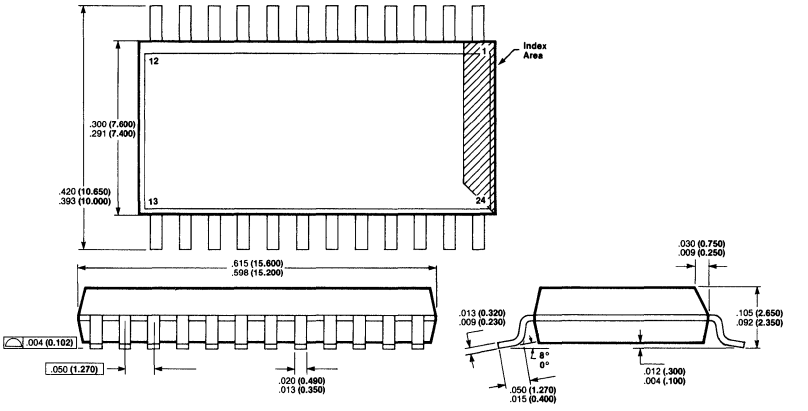
Notch or Lead One ID shall be within index area.

Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 0.55 gram.

24 Lead Small Outline Integrated Circuit (SOIC)

Ordering Codes: 74ACXXXSC
74ACTXXXSC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in inches **(millimeters).** Controlling dimensions: Metric. Dimensions are typical unless otherwise specified.

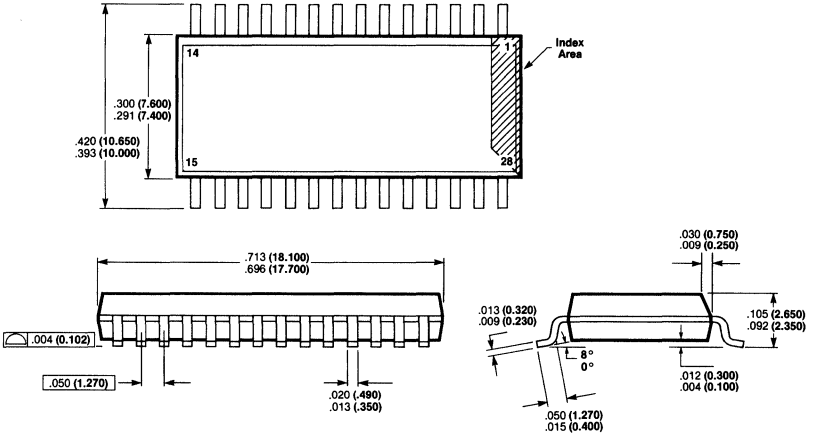
Notch or Lead One ID shall be within index area.

Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 0.66 gram.

28 Lead Small Outline Integrated Circuit (SOIC)

Ordering Codes: 74ACXXXSC
74ACTXXXSC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in inches **(millimeters).** Controlling dimensions: Metric. Dimensions are typical unless otherwise specified.

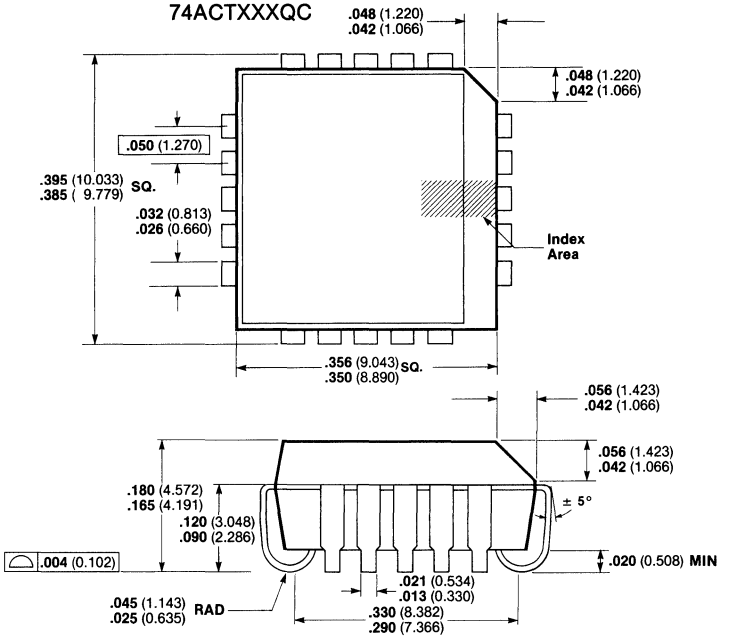
Notch or Lead One ID shall be within index area.

Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 0.77 gram.

20 Lead Plastic Chip Carrier (PCC)

Ordering Codes: 74ACXXXQC
74ACTXXXQC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

Notch or Lead One ID shall be within index area.

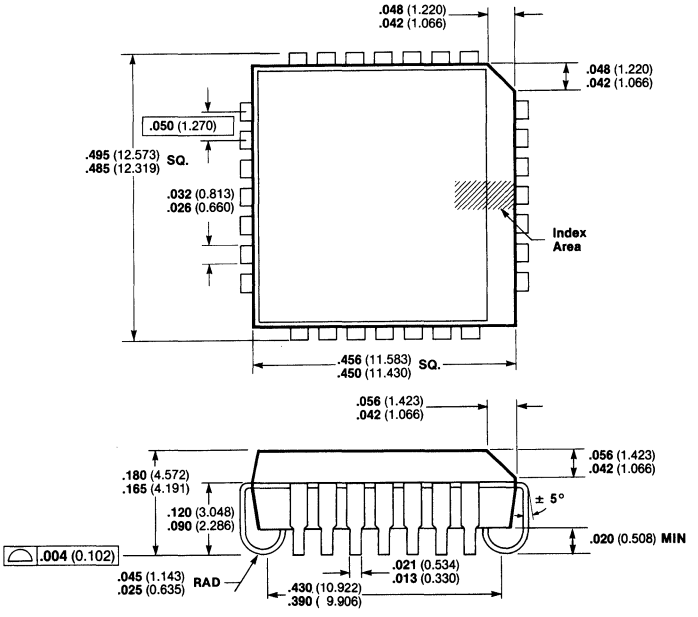
Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 0.7 gram.

6

28 Lead Plastic Chip Carrier (PCC)

Ordering Codes: 74ACXXXQC
74ACTXXXQC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

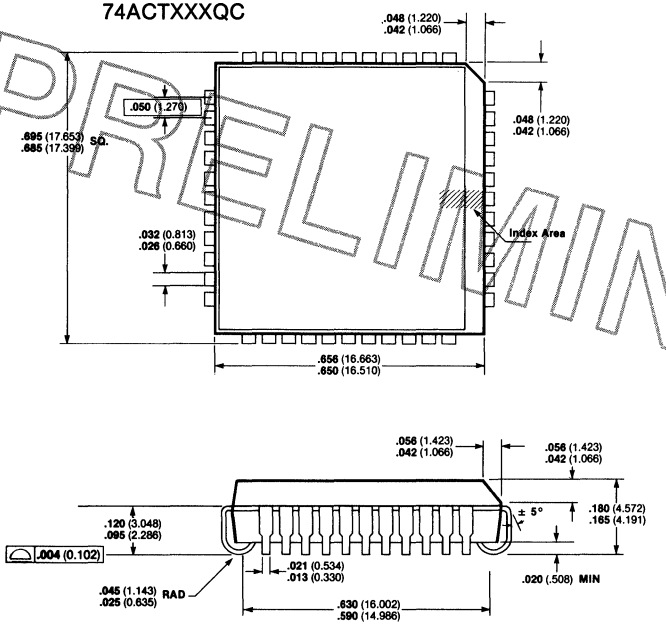
Notch or Lead One ID shall be within index area.

Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 1.1 grams.

44 Lead Plastic Chip Carrier (PCC)

Ordering Codes: 74ACXXXQC
74ACTXXXQC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

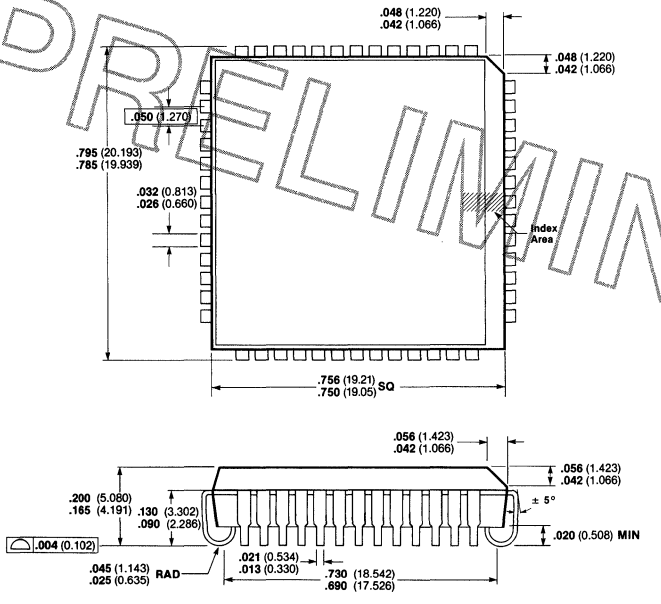
Notch or Lead One ID shall be within index area.

Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 2.3 grams.

52 Lead Plastic Chip Carrier (PCC)

Ordering Codes: 74ACXXXQC
74ACTXXXQC



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

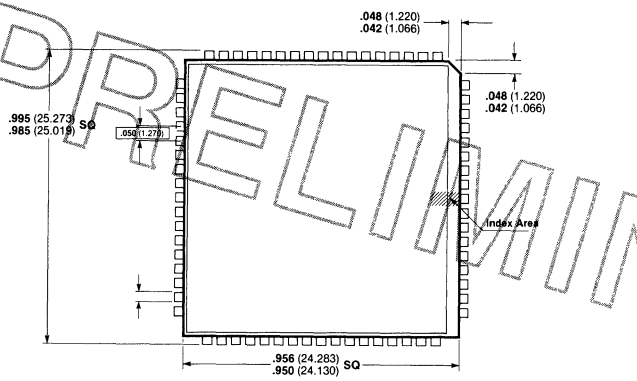
Notch or Lead One ID shall be within index area.

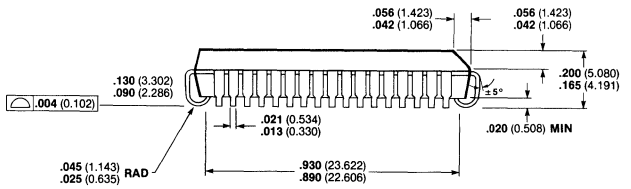
Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 3.2 grams.

68 Lead Plastic Chip Carrier (PCC)

Ordering Codes: 74ACXXXQC
74ACTXXXQC





Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

Notch or Lead One ID shall be within index area.

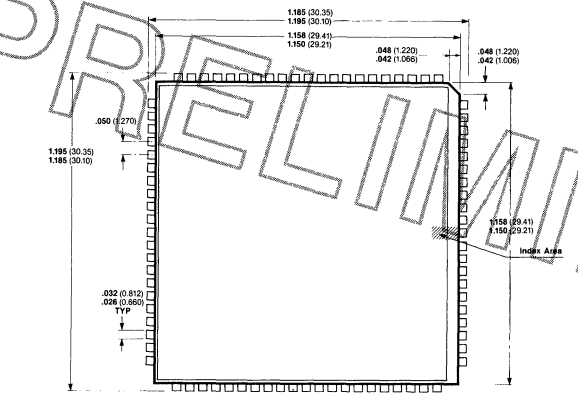
Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

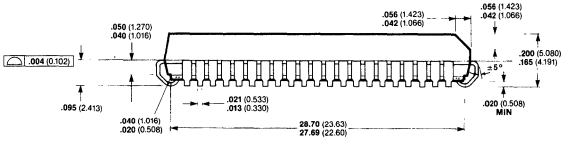
Package weight is 4.7 grams.

6

84 Lead Plastic Chip Carrier (PCC)

Ordering Codes: 74ACXXXQC
74ACTXXXQC





Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

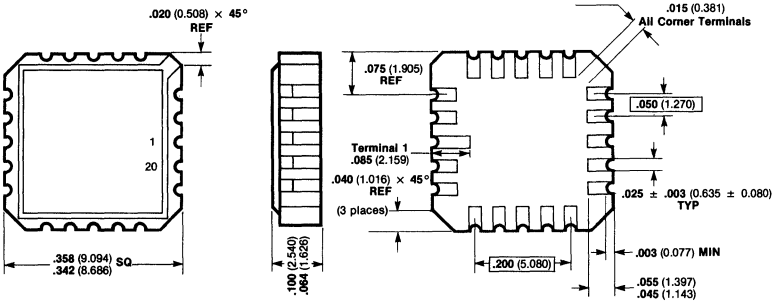
Notch or Lead One ID shall be within index area.

Leads are copper alloy, either tin plated or solder coated. Plastic is novolac epoxy.

Package weight is 6.3 grams.

20 Terminal Ceramic Leadless Chip Carrier (LCC)

Ordering Codes: 74ACXXXLC
74ACTXXXLC
54ACXXXLM
54ACTXXXLM



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

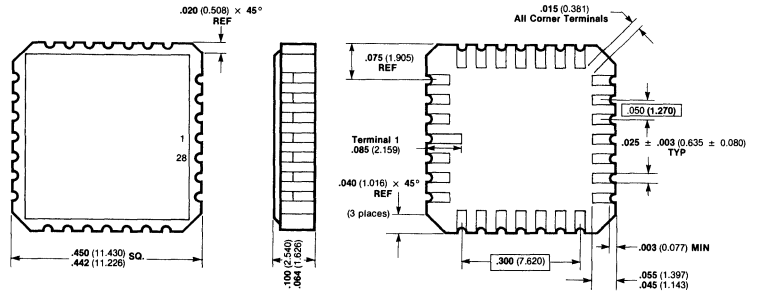
Terminal One is indicated by elongated metallization on package bottom.

Terminals are coated with gold, tin or solder. Package is 90% minimum alumina (black); lid is solder seal metal.

Package weight is 0.5 gram.

28 Terminal Ceramic Leadless Chip Carrier (LCC)

Ordering Codes: 74ACXXXLC
74ACTXXXLC
54ACXXXLM
54ACTXXXLM



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

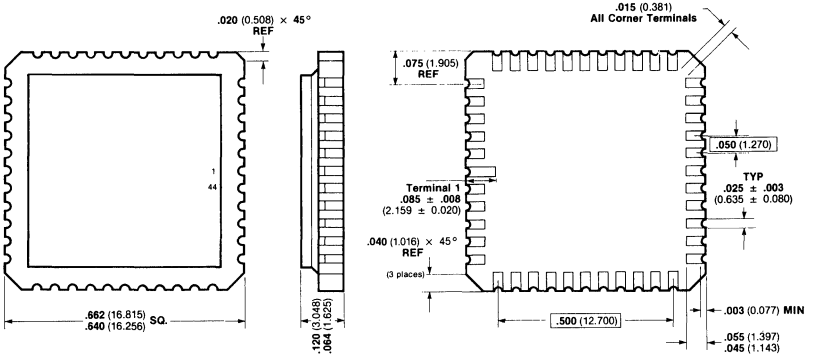
Terminal One is indicated by elongated metallization on package bottom.

Terminals are coated with gold, tin or solder. Package is 90% minimum alumina (black); lid is solder seal metal.

Package weight is 0.8 gram.

44 Terminal Ceramic Leadless Chip Carrier (LCC)

Ordering Codes: 74ACXXXLC
74ACTXXXLC
54ACXXXLM
54ACTXXXLM



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

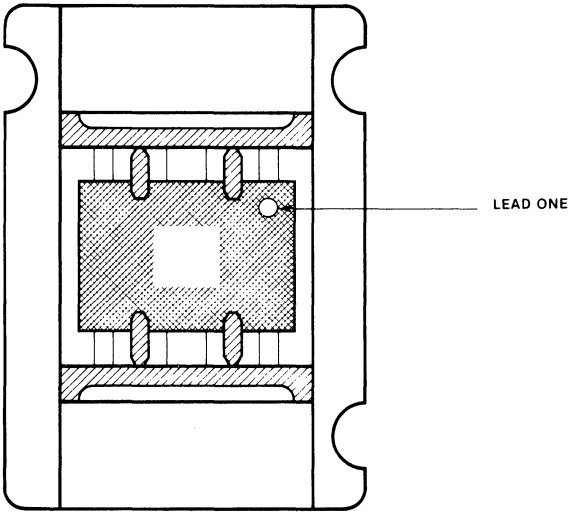
Terminal One is indicated by elongated metallization on package bottom.

Terminals are coated with gold, tin or solder. Package is 90% minimum alumina (black); lid is solder seal metal.

Package weight is 1.7 grams.

6

Cerpak



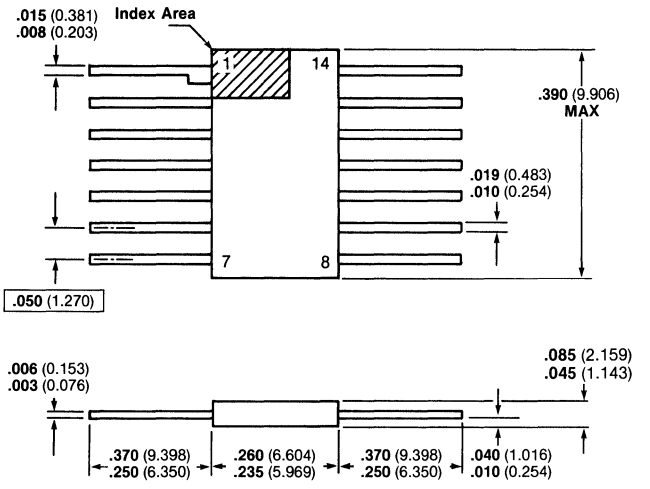
Standard carrier loading locates Lead One of the device adjacent to the side with the double notch, mark side up.

Standard carriers are one-piece designs for 14, 16, 20 and 24 lead Cerpaks.

Carriers are molded of polysulfone, capable of withstanding normal IC handling over the temperature range of -55°C to +150°C.

14 Lead Ceramic Flatpak

Ordering Codes: 54ACXXXFM
54ACTXXXFM



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

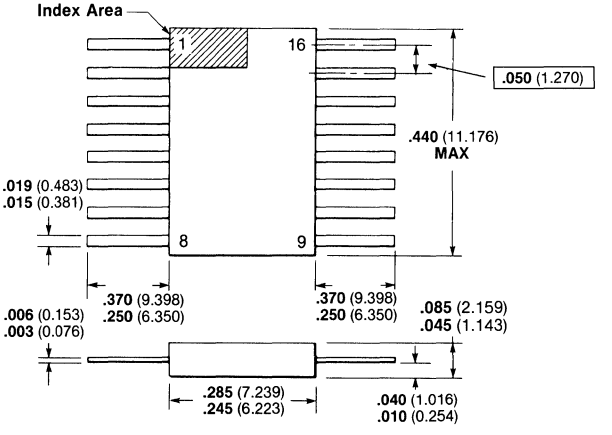
Notch or Lead One ID shall be within Index Area, or a tab shall be on Lead One.

Leads are alloy 42, either tin plated or solder coated. Base and lid are 90% minimum alumina (black) sealed with glass.

Package weight is 0.4 gram.

16 Lead Ceramic Flatpak

Ordering Codes: 54ACXXXFM
54ACTXXXFM



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

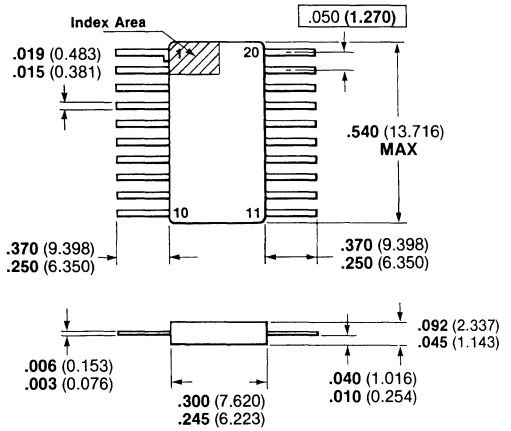
Notch or Lead One ID shall be within Index Area, or a tab shall be on Lead One.

Leads are alloy 42, either tin plated or solder coated. Base and lid are 90% minimum alumina (black) sealed with glass.

Package weight is 0.4 gram.

20 Lead Ceramic Flatpak

Ordering Codes: 54ACXXXFM
54ACTXXXFM



Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

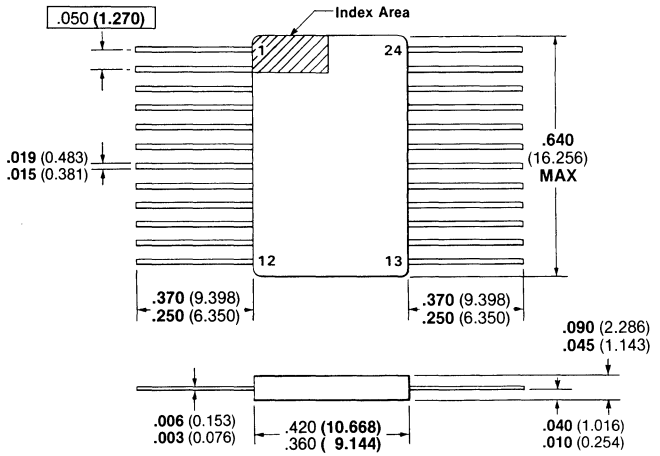
Notch or Lead One ID shall be within Index Area, or a tab shall be on Lead One.

Leads are alloy 42, either tin plated or solder coated. Base and lid are 90% minimum alumina (black) sealed with glass.

Package weight is 0.6 gram.

24 Lead Ceramic Flatpak

Ordering Codes: 54ACXXXFM
54ACTXXXFM



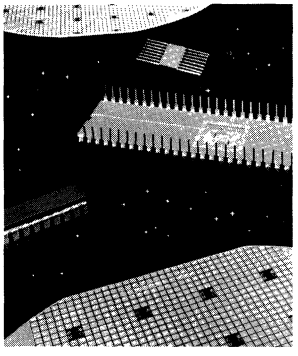
Notes
Dimensions and tolerances per ANSI Y14.5M-1982.

Dimensions are in **inches** (millimeters). Controlling dimensions: Inches. Dimensions are typical unless otherwise specified.

Notch or Lead One ID shall be within Index Area, or a tab shall be on Lead One.

Leads are alloy 42, either tin plated or solder coated. Base and lid are 90% minimum alumina (black) sealed with glass.

Package weight is 0.8 gram.



FAIRCHILD

FGC Series
Advanced 2-Micron CMOS Gate Array Family

Description

The FGC Series is an advanced, high performance CMOS gate array family designed for LSI implementation of existing discrete logic systems and new designs requiring high density and low power. With up to 8000 gates and high I/O to gate ratios, the FGC family offers single gate array solutions to a wide variety of digital logic applications. Table 1 summarizes the important characteristics of this gate array family.

Designed with true 2-micron design rules, the FGC Series is fabricated on an advanced, dual metal, oxide isolated, fully implanted CMOS process. Effective channel lengths of 1.3 microns coupled with reduced junction area capacitance allows system clock speeds up to 50 MHz. Internal gate propagation delays range from 1.1 ns typically to 1.9 ns worst case industrial and 2.0 ns for military operation.[1] Operating from a single 5 V power supply, these arrays exhibit extremely low power dissipation, typically 20 μW/gate/MHz.

FGC Series Features

- **500, 1200, 2400, 4000, 6000 and 8000 Gates**
- **True 2-micron Silicon Gate CMOS Technology**
- **High Performance—Typical Internal Delays 1.1 ns**
- **8 mA Output Drive Current Standard**
- **Low Power Dissipation—Typically 20 μW/gate/MHz**
- **Selectable CMOS or TTL I/O**
- **No Internal Cells Required for I/O Buffer**
- **Single 5 V Power Supply**
- **On-Chip Testability Features (Except FGC0500)**
- **Wide Choice of Package Pin Counts and Styles**
- **Complete Integrated CAD Support**
- **Second Source—VLSI Technology, Inc.**

[1] 2-input NAND. Fanout = 2, typical interconnect metal
Additional conditions include:
Industrial: V_{DD} = 4.5 V, T_j = 85°C, worst case process parameters
Military: V_{DD} = 4.5 V, T_j = 125°C, worst case process parameters

Array Organization

The general layout of the FGC6000 can be seen in Figure 7-1. Electrical components are organized into structural features called cells. Macro circuits, which are the basic building block of logic design, are comprised of one or more cells.

All FGC Series arrays use the same basic internal cell and I/O cell structure. Thus the same macros can be used throughout the FGC family.

The bussing structure for the FGC Series isolates the I/O cells from the internal array. Both the V_{DD} and V_{SS} bus surround the array in second metal (dual-layer metal process) and are brought into the internal array area via a power rail structure. Each cell is connected to the power rail through the substrate which reduces the resistance and internal latch-up susceptibility.

Figure 7-1: FGC6000 Die

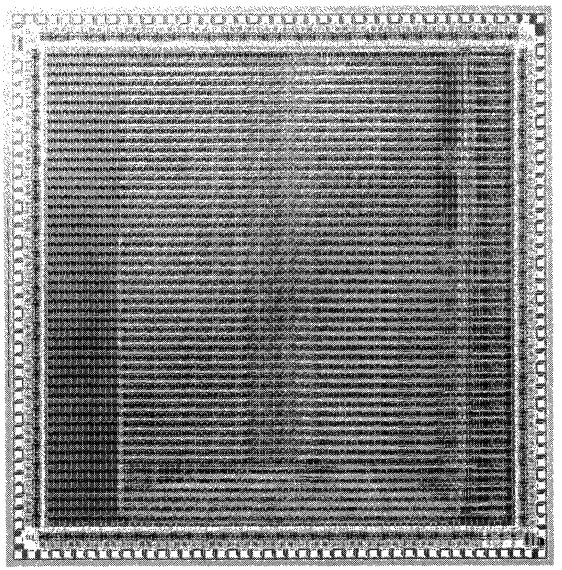


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Table 7-1: FGC Gate Array Family

	FGC0500	FGC1200	FGC2400	FGC4000	FGC6000	FGC8000
Total Cells	360	792	1728	2640	4000	5358
Equivalent Gates[2]	540	1188	2592	3960	6000	8037
Input Only	0	27	39	47	55	63
Inputs/Outputs	40	46	70	86	106	118
Total I/O	40	73	109	133	161	181
Power Pins	4	8	8	8	8	16
Testability Pins	0	3	3	3	3	3
Total Pins	44	84	120	144	172	200

[2] An equivalent gate is defined as one 2-input NAND.

Internal Cell Description

The basic internal cell of the FGC Series is shown in Figure 7-2. The cell consists of six transistors; three p-channel and three n-channel. The cell employs a bent gate pattern to optimize performance and minimize die size. Logic functions implemented with a single cell include two inverters, an inverter and a transmission gate, a two-input NAND or NOR and an inverter, and a three-input NAND or NOR.

Internal cells are preconnected to form macros, the basic logic element from which a design is implemented. The FGC Series shares a common macro library, which consists of most 7400 series logic functions. Additionally, macros to support enhanced testability design methodologies, such as scan test, are also available. Table 4 summarizes AC performance of commonly used macros.

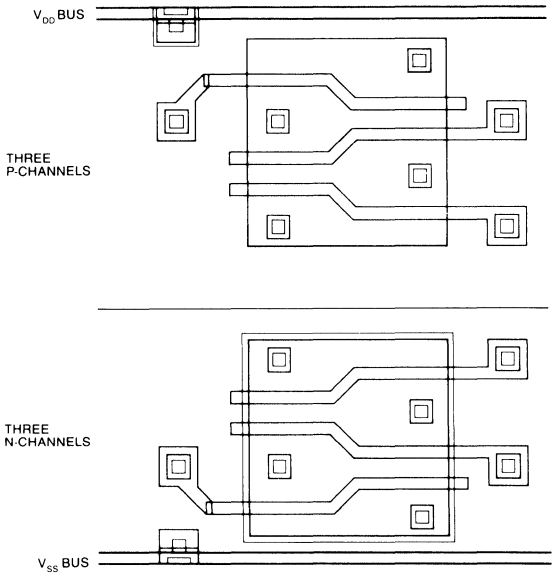
Internal Cell Features

- 6-transistor cell (3 p-channel, 3 n-channel)
  Greater routing efficiency over 4-transistor cell designs

- Single cell logic functions
  Two single inverters
  Inverter and transmission gate
  2-input NAND or NOR and inverter
  3-input NAND or NOR

- Bent gate pattern
  Reduces junction capacitance
  15% area reduction over standard design

Figure 7-2: FGC Series Internal Cell



I/O Buffers

All I/O buffers contain built-in flexibility to allow both standard totem pole or 3-state output options without utilizing any internal cells. Additionally, each input can be individually programmed for either CMOS or TTL interface. This feature is available as a macro option, and is easily specified in the initial stages of logic design. Typical performance of input and output buffers is shown in Tables 5 and 6. The buffers have been designed to source or sink 8 mA (10 mA for FGC0500) across the industrial temperature range and 6 mA (8 mA for FGC0500) across the military range.

There are two cell types, input only and input/output, which are interspersed around the array (see Figure 7-3). Advantages of this configuration includes increased I/Os for a given gate count, reduced signal lengths and improved routability.

Input Protection

Input protection is incorporated into all I/O macros. As illustrated in Figure 7-4, dual V_{DD} and V_{SS} guard rings effectively reduce parasitic betas by providing recombination paths for minority carriers. This guard ring approach protects against up to 1200 V of static discharge.

Figure 7-4: Input Protection

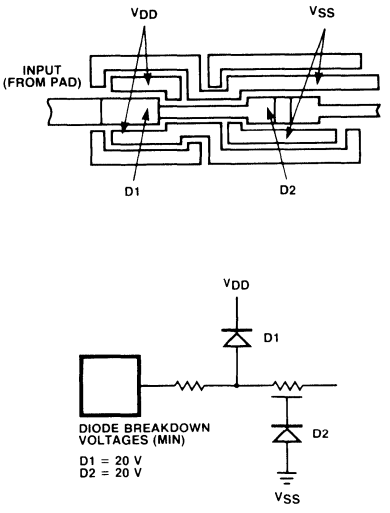


Figure 7-3: I/O Buffer Layout

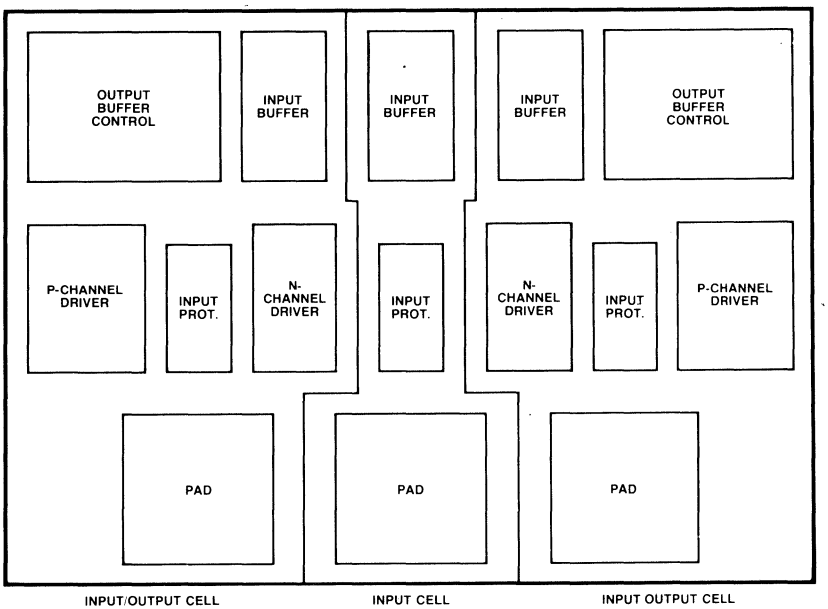


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Table 7-2: Absolute Maximum Ratings Chart

Symbol	Parameter	Range	Unit
V_{DD}	Supply Voltage	−0.5 to +6	V
V_I	Input Voltage	−0.5 to V_{DD} +0.5	V
I_I	DC Input Current	±20	mA
T_{STG}	Storage Temperature Ceramic Package Plastic Package	 −65 to +150 −40 to +125	°C
T_A	Ambient Temperature Under Bias[3] Military Commercial/Industrial	 −55 to +125 −40 to +85	°C
T_L	Lead Temperature (Soldering, 10 seconds)	300	°C

[3] Junction temperature not to exceed ambient temperature by more than 20°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7-3: DC Characteristics (V_{DD} = 5.0 V ± 10%, T_A = −55°C to +125°C, unless otherwise specified)

Symbol	Parameter	Min	Max	Unit	Conditions
V_{IH}	Input HIGH Voltage[4] CMOS Input TTL Input (Industrial) TTL Input (Military)	 3.15 2.0 2.25	 V_{DD} V_{DD} V_{DD}	V	Guaranteed Input HIGH Voltage T_A = 125°C, V_{DD} = 4.5 V T_A = 0°C, V_{DD} = 5.25 V T_A = −55°C, V_{DD} = 5.5 V
V_{IL}	Input LOW Voltage[4] CMOS Input TTL Input	 -0.5 -0.5	 1.35 0.8	V	Guaranteed Input LOW Voltage
V_{OH}	Output HIGH Voltage	V_{DD} − 0.05		V	I_{OH} = −1 μA, T_A = 125°C, V_{DD} = 4.5 V
	OB01F(FGC0500)	3.7		V	I_{OH} = −10 mA, T_A = 85°C, V_{DD} = 4.5 V I_{OH} = −8 mA, T_A = 125°C, V_{DD} = 4.5 V
	Other Output Buffers	3.7		V	I_{OH} = −8 mA, T_A = 85°C, V_{DD} = 4.5 V I_{OH} = −6 mA, T_A = 125°C, V_{DD} = 4.5 V
V_{OL}	Output LOW Voltage		0.1	V	I_{OL} = 1 μA, T_A = 125°C, V_{DD} = 4.5 V
	OB01F(FGC0500)		0.4	V	I_{OL} = 10 mA, T_A = 85°C, V_{DD} = 4.5 V I_{OL} = 8 mA, T_A = 125°C, V_{DD} = 4.5 V
	Other Output Buffers		0.4	V	I_{OL} = 8 mA, T_A = 85°C, V_{DD} = 4.5 V I_{OL} = 6 mA, T_A = 125°C, V_{DD} = 4.5 V

Table 7-3: DC Characteristics, continued
(V_{DD} = 5.0 V ± 10%, T_A = −55°C to +125°C, unless otherwise specified)

Symbol	Parameter	Min	Max	Unit	Conditions
I_{IN}	Input Leakage Current	−10	10	μA	V_{IN} = V_{DD} or GND (Without Pullup Resistor)
I_{OZ}	3-State Output Leakage Current	−10	10	μA	V_{OUT} = V_{DD} or GND
C_{IN}	Input Capacitance		5	pF	Excluding Package
C_{OUT}	Output Capacitance		5	pF	Excluding Package
$C_{I/O}$	Transceiver Capacitance		5	pF	Excluding Package

[4] V_{IH} and V_{IL} are steady state specifications and are specified with respect to the device ground pin. All functional tests are performed using additional margins to account for AC noise.

AC Characteristics for Selected Macros

Table 7-4: Internal Cell

Macro	Cells	Description	Symbol	Typical Propagation Delay (ns) Fanout = 2	Worst Case Propagation Delay (ns) Commercial/Industrial[5] Fanout 2	Commercial/Industrial[5] Fanout 4	Military[6] Fanout 2	Military[6] Fanout 4
INV11	1	2 1x Inverters	t_{PLH} t_{PHL}	1.1 0.4	2.1 0.9	3.3 1.3	2.2 0.9	3.5 1.5
NA02	1	2-Input NAND	t_{PLH} t_{PHL}	1.4 0.8	2.5 1.8	3.8 2.7	2.8 1.9	4.1 2.9
NA04	2	4-Input NAND	t_{PLH} t_{PHL}	1.7 1.9	3.3 4.0	4.6 5.7	3.7 4.4	5.1 6.3
NOR02	1	2-Input NOR	t_{PLH} t_{PHL}	1.9 0.6	4.1 1.2	6.4 1.7	4.5 1.4	7.0 1.9
NOR04	2	4-Input NOR	t_{PLH} t_{PHL}	4.3 0.7	9.7 1.4	14.2 2.0	10.8 1.5	15.7 2.1
DFP01	4	D Flip-Flop (Clock→Q)	t_{PLH} t_{PHL}	2.6 2.1	5.4 4.2	6.5 4.8	5.9 4.7	7.2 5.3
DFP04	6	D Flip-Flop with Set, Reset (Clock →Q)	t_{PLH} t_{PHL}	3.1 3.2	6.4 6.4	7.6 6.9	7.0 7.1	8.2 7.8

[5] V_{DD} = 4.5 V, T_j = 85°C, Worst Case Process, Worst Case Wirelength.
[6] V_{DD} = 4.5 V, T_j = 125°C, Worst Case Process, Worst Case Wirelength.

Table 7-5: Input Buffer

Macro	Description	Symbol	Typical Propagation Delay (ns) Fanout=2	Worst Case Propagation Delay (ns) Commercial/Industrial[5,7] Fanout 2	Commercial/Industrial[5,7] Fanout 4	Military[6,7] Fanout 2	Military[6,7] Fanout 4
IOC011F	CMOS with Pullup, FGC0500	t_{PLH} t_{PHL}	1.9 2.2	3.5 3.9	4.0 4.5	3.6 4.2	4.3 4.9
IOT011F	TTL with Pullup, FGC0500	t_{PLH} t_{PHL}	1.5 2.1	4.1 6.3	4.9 7.1	4.4 7.1	5.2 8.0
IOC011	CMOS with Pullup	t_{PLH} t_{PHL}	1.9 2.0	2.4 3.6	3.0 4.0	2.7 3.8	3.3 4.3
IOT011	TTL with Pullup	t_{PLH} t_{PHL}	2.6 2.9	3.6 4.3	4.1 5.1	3.9 5.0	4.5 5.8

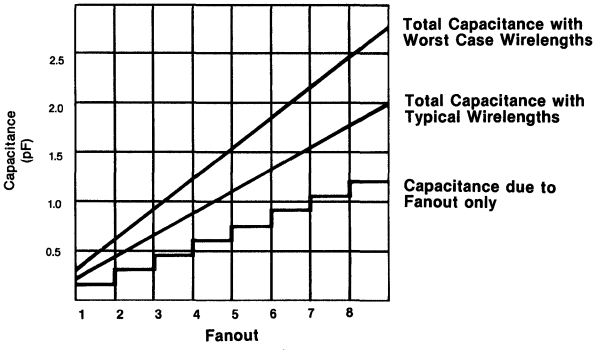
[7] CMOS Input t_r, t_f=5 ns, FAST™ Input t_r, t_f=2.5 ns.

Table 7-6: Output Buffer

Macro	Description	Symbol	Typical Propagation Delay (ns) Capacitive Load=15 pF	Worst Case Propagation Delay (ns) Commercial/Industrial[5] Capacitive Load (pF) 15	50	100	Military[6] Capacitive Load (pF) 15	50	100
OB01F	High Drive, FGC0500	t_{PLH} t_{PHL}	2.0 2.6	3.6 4.6	6.0 6.7	9.5 9.7	3.7 5.0	6.1 7.1	9.6 10.1
OB03F OB04F	3-State, FGC0500 Standard, FGC0500	t_{PLH} t_{PHL}	2.5 2.8	5.0 5.2	8.1 8.0	12.6 12.0	5.4 5.6	8.9 8.4	13.9 12.4
OB03 OB04	3-State Standard	t_{PLH} t_{PHL}	3.3 4.2	6.0 6.5	9.1 9.3	13.6 13.3	6.6 7.1	10.1 9.9	15.1 13.9

[5] V_{DD}=4.5 V, T_J=85°C, Worst Case Process, Worst Case Wirelength.
[6] V_{DD}=4.5 V, T_J=125°C, Worst Case Process, Worst Case Wirelength.

Figure 7-5: Capacitance Estimate for FGC Series Internal Macros



The figure illustrates variations of capacitance due to fanout and wirelength of an estimated average of internal cell macros. Typical wirelengths are based on an assumption of 15 mils length per connection, 30% first-layer and 70% second-layer metal routing. Worst case wirelengths assume 30 mils length per connection with 50% first-layer and 50% second-layer metallization.

Testability Features

Incorporated into the FGC Series (excluding the FGC0500) is a range of features to enhance design testability and simplify device testing. Three dedicated pads are located on each gate array, which may be bonded out to access three types of tests: output buffer parametric tests, DC functional tests, and an AC monitor test. A summary of each test is included in Table 7 and described more fully below.

The output parametric tests allow DC data to be measured on all outputs by controlling the three input pins, TEST, TOE (Test Output Enable), and TDAT (Test Data). This feature avoids the need for a lengthy test program to force outputs into the correct state for parametric testing.

System initialization can be greatly simplified by the JAM RESET feature. All flip-flops in a design can be simultaneously reset to zero, thereby avoiding long vector sequences to initialize a device into a known state. Alternately, scan testing is also supported, which among other features, allows the array to be initialized by serially writing data into each flip-flop.

An on-chip ring oscillator is provided as an indicator of AC performance of each device. The frequency is monitored by Fairchild at the wafer level as part of the outgoing test procedure. This signal may also be bonded out at the expense of an I/O pad and used as an incoming customer acceptance criterion.

Packaging

Fairchild offers the following packages and pin counts for the FGC Series: Plastic and Ceramic DIPs: 24, 40; Plastic and Ceramic Pin Grid Arrays: 68, 84, 100, 120, 132, 144, 180; Plastic and Ceramic J-Bend Chip Carriers: 44, 68, 84.

Table 7-7: FGC Series Testability Features

Type	Inputs			Output	Tests Performed	Description
	$\overline{\text{TEST}}$	$\overline{\text{TOE}}$	TDAT	ACOUT		
Output Buffer Parametric Tests	1	1	1	Disabled		Normal operation
	0	0	TDAT	Disabled	V_{OH}, V_{OL}, I_{OH}, I_{OL}	Test Data signal, TDAT, appears on all outputs
	0	1	0	Enabled	3-State Leakage	All outputs in 3-state mode
	0	1	1	Disabled	Standby Current	Measurement of static power dissipation
DC Functional Tests	1	1	0	Disabled	Jam Reset[8]	Resets all flip-flops to a LOW state
	1	0	Scan Data	Disabled	Scan Test[8]	Allows data to be serially scanned into all flip-flops
AC Monitor	0	1	0	Enabled	Ring Oscillator Frequency	Enables on-chip ring oscillator to monitor AC performance

[8] These tests are examples of Design for Testability techniques that the test pins can perform when additional internal cell logic is used.

CAD Support

Fairchild supports various options for design implementation, working either through FAIRCAD,™ Fairchild's in-house, computer-aided design system, or through one of several commercially available computer-aided engineering workstations. Using any of the hardware options, the designer may elect to perform any or all of the design steps or delegate responsibility to a Fairchild applications engineer.

Faircad Design Implementation

FAIRCAD, Fairchild's computer-aided design system, provides a user-friendly, technology-independent environment for building FGC Series gate arrays. FAIRCAD's fully integrated CAD tools allow the designer to perform all design functions from schematic entry, circuit analysis and fault grading to layout and automatic test vector generation. FAIRCAD can easily be learned and used by those with no prior CAD experience. Complete training is provided in a one-week class that takes the user through an entire design example.

FAIRCAD's high-level command menu and on-line help provides additional support by guiding the user step-by-step through the design cycle. Controlled program execution assures proper file management and adherence to design rules. In addition, summaries generated automatically after executing each program may be printed at any time for review. FAIRCAD supports off-hour batch submission—an effective method of increasing productivity while reducing CPU charges by running computer-intensive programs during non-prime-time hours.

In addition to design tools for implementing each of the steps illustrated below in Figure 7-6, FAIRCAD offers a number of system utilities including electronic mail, system/job status querying, color or B/W plot generation, as well as total CPU cost accounting.

FAIRCAD can be accessed at FAIRTECH Design Centers in Northern and Southern California; Dallas, Texas; Boston, Massachusetts; Minneapolis, Minnesota; Maitland, Florida and in international design centers in Reading, England and Tokyo, Japan. Additionally, a variety of compatible alphanumeric and graphic CRTs at customer sites can be linked to FAIRCAD through dial-up or leased lines. Further information on FAIRCAD's capabilities can be found in the Fairchild Gate Array CAD Support brochure, with comprehensive documentation available in the FAIRCAD User's Manual.

Workstation Implementation

Fairchild supports gate array design on Daisy Systems, Mentor Graphics and, in the future, Valid Logic and CAE computer-aided engineering workstations. Designers using workstations are provided with diskettes containing the macro library with all symbols and simulation models, and software for design verification, logic simulation, timing calculations and netlist generation.

Placement and routing is performed at a FAIRTECH Design Center after the netlist is transferred to FAIRCAD. Final netlengths are transferred back to the workstation for timing verification.

Figure 7-6: FAIRCAD Design Flow

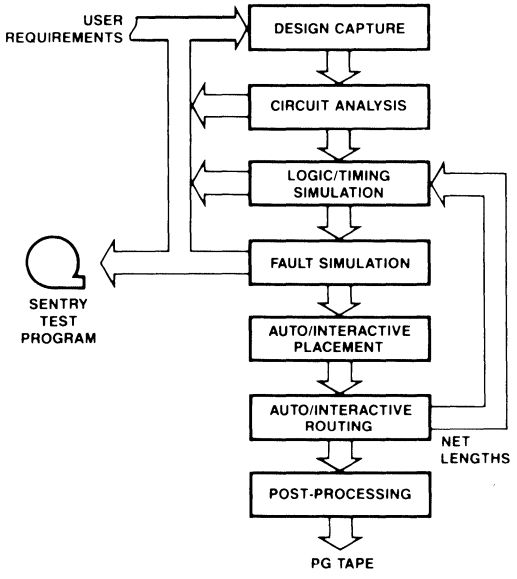
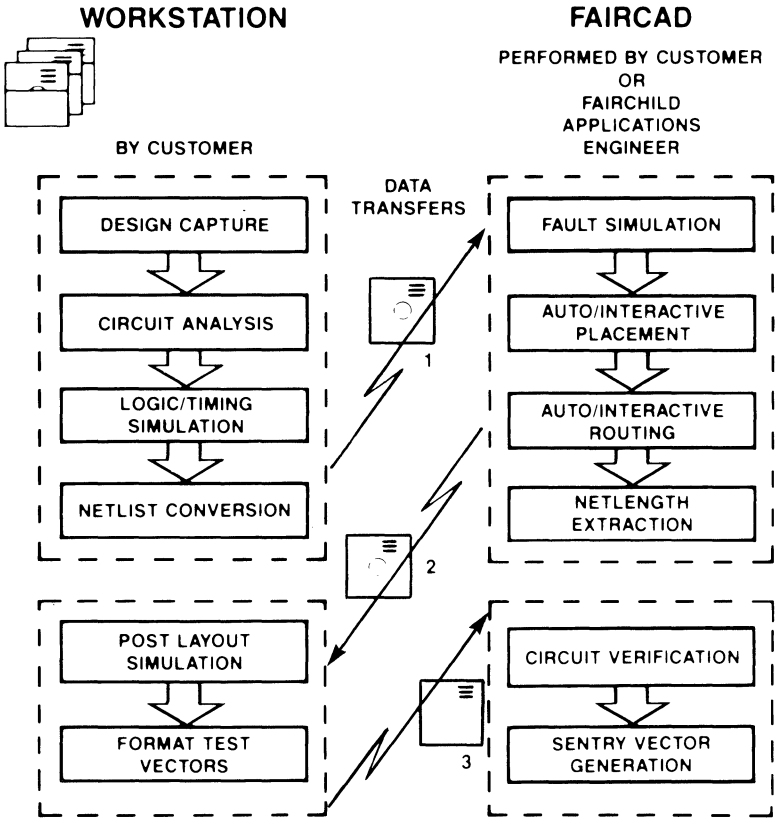
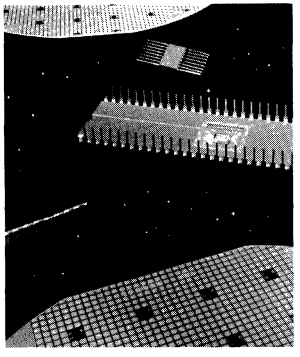


Figure 7-7: Typical Engineering Workstation Design Flow





FAIRCHILD

FAIRCAD™ Semicustom Design System

FAIRCAD Features

- **Interactive Design Capture**
- **Design Rule Checking**
- **Interactive Logic and Timing Simulation**
- **Controllability Fault Analysis**
- **Auto/Interactive Placement and Routing**
- **Test Vector Formatting for ATE**

Introduction

FAIRCAD™—Fairchild's fully integrated, technology independent gate array design software—supports all design tasks from design capture through final design database creation for prototype manufacturing. And FAIRCAD is available on tape for installation on the VAX VMS system, including the MicroVAX II. A proven tool for designing circuitry using our CMOS and ECL gate arrays, FAIRCAD combines engineering graphics with powerful programs to compile, analyze, simulate, place and route system designs. FAIRCAD is menu-driven with extensive on-line help listings and a built-in system monitor to ensure the proper program sequence is adhered to. Figure 8-1 illustrates the typical FAIRCAD design flow.

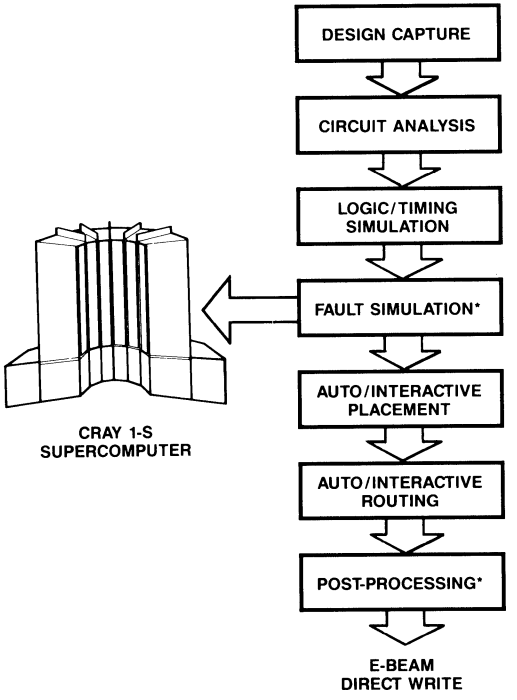
Fault simulation on FAIRCAD is eased through the use of our Cray 1-S Supercomputer in Milpitas, California; fault simulation on the Cray can be as much as 50 times faster than on other simulation devices. Remote communication links to the Cray make designing at your location even more convenient. And turnaround times at Fairchild have been further reduced by our in-house Cambridge E-Beam Direct-Write-On-Silicon System.

Schematic Capture

- **Multiple Windows**
- **Hierarchical Schematics**
- **Menu-Driven**
- **Mouse Command Entry**
- **Complete ECL and CMOS Libraries**

With FAIRCAD's schematic capture program designs may be entered in either the schematic input mode or netlist input mode. The schematic input mode accesses FAIRCAD's fully interactive, menu-driven graphics design entry program. The Structure Description Language (SDL) generates a netlist—a listing of all component interconnections in your design—to be entered into FAIRCAD on magnetic tape or through a keyboard.

Figure 8-1: Typical FAIRCAD Design Flow



*Completed at Fairchild in Milpitas, CA

8

Schematic Input

FAIRCAD schematic capture simplifies the entering and editing of a semicustom design. FAIRCAD programs are completely menu-driven and extensive on-line help listings are accessed by simply typing "H" followed by a carriage return. The schematic capture menu is shown in Figure 8-2. Logic components are accessed from the macro library of the chosen technology and, with a single keystroke, positioned within the design. Facilities such as COMPONENT MOVE and ALIGN quickly organize and structure a design. Interconnection of components is also quick using connection rubberbanding, which makes line segments visible during the actual connection procedure; visible connections are "stretched" between entry points with the system crosshairs.

WINDOW commands allow editing up to four different symbols, schematics, or windows of the same schematic or symbol simultaneously. Names, text, components, and pins can be aligned horizontally or vertically using FAIRCAD's alignment feature.

Netlist Input Mode

With this method a standard keyboard terminal is used to alphanumerically enter a netlist. Two Fairchild programs permit "describing" a circuit to FAIRCAD. One program, using the SDL, accepts design information in the form of component descriptions and interconnections (netlist). The other program loads the manually generated netlist into the FAIRCAD database and checks for errors in connections, names, nets, etc. FAIRCAD will promptly inform the user of any errors located. The SDL can also be used for editing the manually entered netlist.

Figure 8-2: FAIRCAD Schematic Capture Menu Features

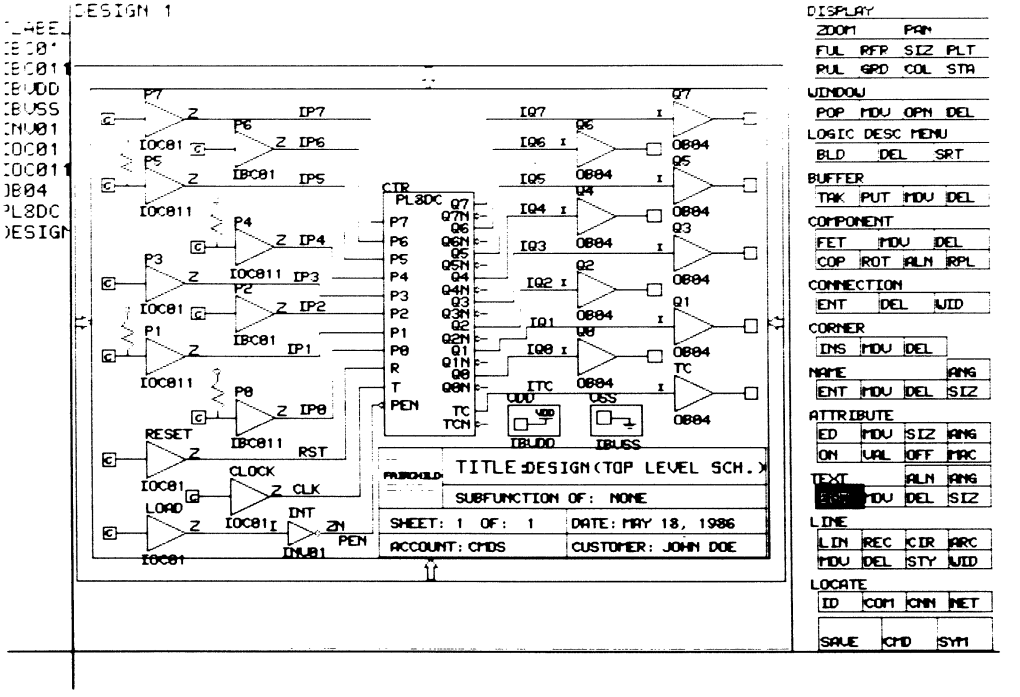


Figure 8-3: Sample Circuit Network Analysis Summary

```
                                NETWORK ANALYSIS SUMMARY
                                ------------------------

POWER SUMMARY TABLE
-------------------

                          Minimum                                Nominal                                Maximum
                Itt(A)    Itt(A)    Icc(A)   PD(W)    Itt(A)    Itt(A)    Icc(A)   PD(W)    Itt(A)    Itt(A)    Icc(A)   PD(W)
                On-Chip   Off-Chip                     On-Chip   Off-Chip                     On-Chip   Off-Chip
                -------------------------------------  -------------------------------------  -------------------------------------
Macros:         0.001     0.040     0.010    0.08     0.001     0.040     0.013    0.11     0.002     0.040     0.017    0.15

Bias Drivers
(Max.):                             0.329    1.55                         0.419    2.18                         0.548    3.13
                -------------------------------------  -------------------------------------  -------------------------------------

Totals:         0.001     0.040     0.339    1.63     0.001     0.040     0.432    2.29     0.002     0.040     0.565    3.28
                -------------------------------------  -------------------------------------  -------------------------------------

                          VCC =       0.00                         VCC =       0.00                         VCC =       0.00
                          VEE =      -4.70                         VEE =      -5.20                         VEE =      -5.70
                          VTT =      -1.90                         VTT =      -2.00                         VTT =      -2.10

CELL UTILIZATION SUMMARY
------------------------

CELL TYPE        NUMBER USED   NUMBER AVAILABLE   PERCENT USED
---------        -----------   ----------------   ------------

INTERNAL             165             1728            9.55%
INPUT                  5               35           14.29%
I/O                   17               70           24.29%

NET/COMPONENT/PIN NAME   ERROR   TYPE      ERROR DESCRIPTION
----------------------------------------------------------------------------------------------------
CTR/BUF0                   9      *E       REGULAR LCS INPUTS AND TRANSLATED INPUTS CANNOT BE CONNECTED SIMULTANEOUSLY.

CTR/BUF1                   7      *E       WIRED-OR MACROS MUST HAVE IDENTICAL MACRO POWER.

CTR/BUF22                  8      *E       ILLEGAL OPEN INPUT PIN.

CTR/BUF23                  6       W       MACRO OUTPUT NOT CONNECTED.

CTR/BUF30                  6       W       MACRO OUTPUT NOT CONNECTED.

CTR/BUF31                 10       W       OUTPUT PIN(S) NOT CONNECTED.

CTR/BUF32                  6       W       MACRO OUTPUT NOT CONNECTED.

CTR/BUF33                  6      *E       ONLY INTERNAL CELL MACROS CAN HAVE OUTPUT DOTTING.

MACRO USAGE SUMMARY
-------------------

MACRO NAME     CELL TYPE     NUMBER USED

2NA04          INTERNAL            1
AND02          INTERNAL            9
BUF02          INTERNAL           39
DFP02          INTERNAL            9
INV01          INTERNAL           16
INV11          INTERNAL            4
MX021          INTERNAL            9
NOR02          INTERNAL            2
NOR03          INTERNAL            4
OR02           INTERNAL            7
OR104          INTERNAL            2
XNOR021        INTERNAL            4
XOR02          INTERNAL            3
IOC01          I/O                 5
IOC011         I/O                 3
OBU4           I/O                 4
IBVCC          INPUT               2
IBGND          INPUT               1
IBVDD          INPUT               1
IBVSS          INPUT               1
```

8

Circuit Design Rule Checking

FAIRCAD's circuit analyzer checks the design to find problems early in the design cycle. This program extracts a netlist from a capture design and checks it for design rule violations, calculates power dissipation and summarizes the usage of logic macros. The design rule checker also analyzes netlists produced using FAIRCAD's Netlist Input Mode. See Figure 8-3 for a sample netlist summary. Errors found in your design must be corrected before design continuation. Circuit analysis checks fan-out, determines bias types required for each macro (ECL only), and automatically places additional power pads where required. Illegal macro interconnections such as the following are also checked:

- **Illegal open pins**
- **Wired OR/on-chip bussing violations**
- **Unbiasable connections**
- **Incompatible circuits**
- **Excessive fanout**
- **Net naming conflicts**

Simulation

- **Hierarchical**
- **Accurate Default Delays Automatically Calculated**
- **Access to Internal Nodes**
- **Hex/Octal Input to Circuits**
- **Flexible Simulation Programming**

Simulation is used after the design has been entered into FAIRCAD and a netlist generated without any logic design violations. Logic, timing, and hierarchical simulation, as well as test program generation, are available on FAIRCAD. With hierarchical simulation you can simulate any block of a design as if it were an independent design: this hierarchical approach facilitates efficient design partitioning while maintaining consistency and improving the integration of the overall circuit. See Figure 8-4 for a sample FAIRCAD timing simulation output.

First, using typical, automatically calculated propagation delays for all components, logic simulation is performed on FAIRCAD to check the accuracy of the logic. Initially, fault simulation is run to determine whether the input test patterns—provided by the designer—successfully diagnose the existence of injected faults. Then, after placement and routing are complete, corrected delay times can be computed using actual wiring distances. To speed the computer-intensive task of fault simulation, access to Fairchild's Cray 1-S Supercomputer (located in Milpitas, California) is provided. Now, controllability analysis is run by FAIRCAD at your facility to generate a potentially detectable and undetectable faults listing. Test vectors are produced for automatic test equipment (ATE) with programs that create and edit package-pin files and supply input/output pin information.

Logic/Timing Simulation

FAIRCAD's logic and timing simulators are used for accurately gauging the functionally and performance of the design early in the design cycle. Using FAIRCAD, nodes can be set to specific values; simulated and compared results may be with the expected results. FAIRCAD's easy-to-learn Fortran-like control language provides the ability to inspect and set internal nodes, do conditional branching, looping, and simulate such conditions as circuit stability. Simulation on FAIRCAD can be hierarchical; any block (or an entire circuit) in the hierarchy can be simulated, saving time and facilitating circuit debugging.

Both logic and timing simulation check for violations such as minimum pulse width, setup time, hold and release time. The FAIRCAD timing program allows simulation of one timestep, one clock cycle, or multiple timesteps at a time, and inspection of internal nodes and I/Os simultaneously. Prior to placement and routing, default metal lengths and default wire delays are used; after placement and routing, actual metal delays are used.

Fault Simulation

Fault simulation informs the user if, by inspecting the design's output pins, manufacturing defects modeled as "stuck-at" faults can be detected. To ensure test vectors screen potential manufacturing defects (short, open, pin hole, etc.), Fairchild provides access to a Cray 1-S Supercomputer and a powerful fault simulation program. In FAIRCAD, fault simulation is divided into two steps—controllability and observability. Controllability, invoked by a single command in the test sequence,

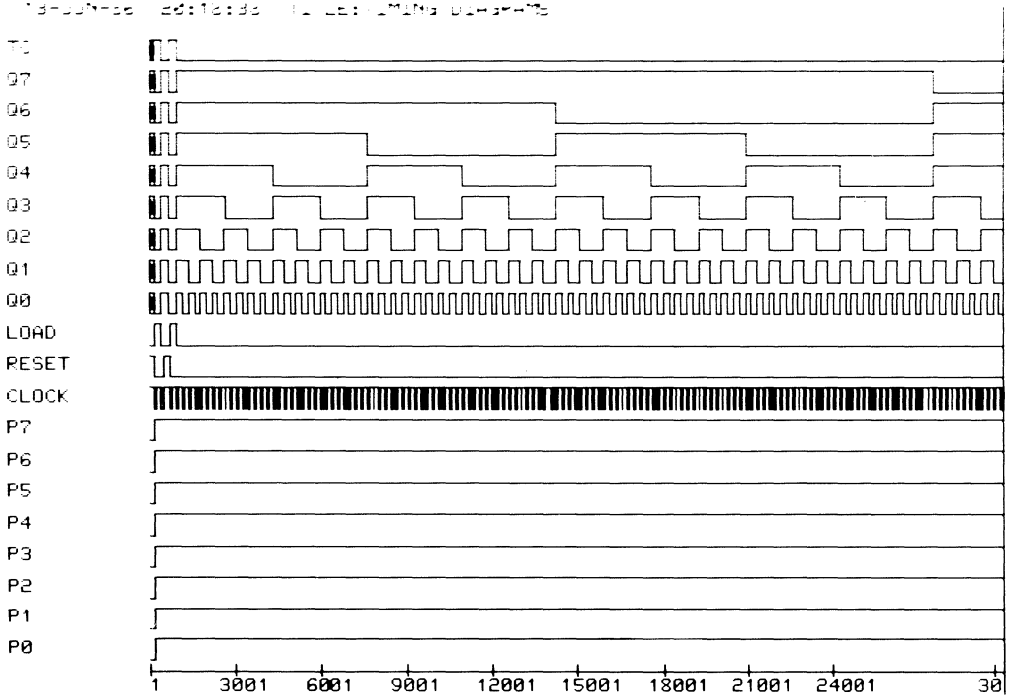
determines the percent of internal nodes being toggled by the vectors provided. In short, this analysis shows how effective the test vectors are in controlling the faults. Observability, which is accomplished using the parallel fault simulator on the Cray 1-S Supercomputer, propagates the faults to primary outputs; this determines if the faults are detectable.

Placement

- **Automatic/Interactive**
- **Automatic Improvement**
- **Prohibits Design Rule Violations**
- **Congestion Parameter Settings**

FAIRCAD's powerful placement program allows random, manual, or automatic placement of components. FAIRCAD provides the ability to interactively place I/Os and/or critical path components in minutes. Automatic placement programs (automatic parameters, placement and improvement) are available to help achieve the optimum placement of your design. Placement, like all other interactive FAIRCAD programs, is menu-driven with extensive "help" features that list all possible user options. Many important display features such as cell and component outlines are also provided.

Figure 8-4: FAIRCAD Timing Waveforms



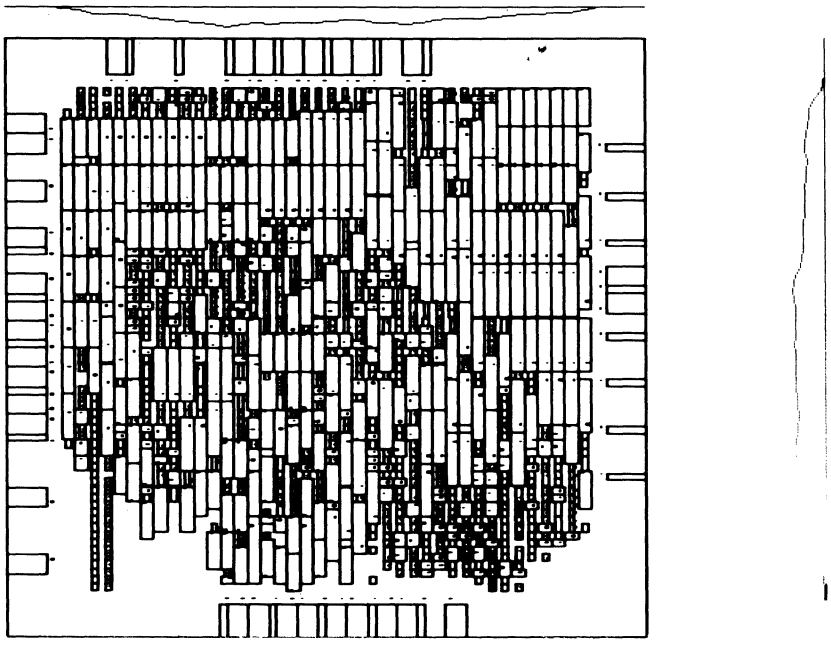
Before placement, a FAIRCAD program compiles and merges the netlist (generated by the circuit design rule checker) and chip databases into a format suitable for both placement and routing. An output listing is then produced that contains the following:

- **Circuit Netlist Description**
- **Overall Circuit Summary**
- **Detailed Summary of Component Macro Types**
- **Detailed Summary of Components**
- **Detailed Summary of Nets**
- **Component-Net Cross Reference List**

To aid in the organizing of the placement, an extensive display menu is available for viewing selected component outlines, labels, cells, etc.

Single-keystroke commands allow you to change the color of various levels, make a hard copy of what is currently visible on the terminal screen, graph congestion values, or show placement obstructions. The congestion graph feature, illustrated in Figure 8-5, helps you minimize interconnect length and congestion by automatically graphing vertical and horizontal placements. Cell "overlaps" are averted with a program that automatically informs you if a selected component placement overlaps others previously placed.

Figure 8-5: FAIRCAD Placement with Congestion Graph Feature



Routing

- **Automatic/Interactive**
- **Automatic Improvement**
- **Prohibits Design Rule Violations**
- **Congestion Parameter Settings**

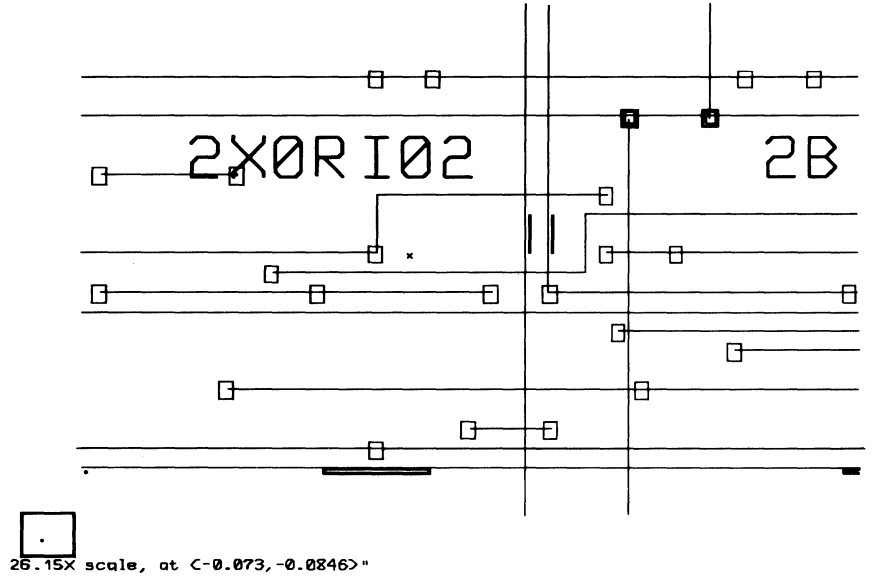
Like placement, FAIRCAD's routing program has both manual and automatic features and is completely interactive. Critical nets may be pre-routed and the automatic router invoked to finish routing the design. Manual routing, completely menu-driven, is available for specifying critical paths and editing disconnects. FAIRCAD's program for viewing the design reads information from the design file and allows viewing of unconnected nets; "airlines"—diagonal lines—are drawn between unconnected pins. As an additional safeguard against errors, FAIRCAD employs the automatic Design Rule Checker (DRC).

Automatically invoked each time you exit the routing editor, the DRC warns of any design rule violation. Table 8-1 lists FAIRCAD routing features. Figure 8-6 shows a typical routing display.

Table 8-1: Routing Programs and Functions

Program	Functions
Route Chip Automatically	automatically routes component interconnections
View the Chip	allows you to view various aspects of your design at any time after design file generation
Manual Routing	allows you to pre-route critical nets and edit routing

Figure 8-6: FAIRCAD Routing Display



8

Engineering Support

Fairchild applications engineers, the experts of gate array design, are available for assistance during the work week and, by arrangement, can complete some or all of FAIRCAD's design tasks for you.

Instruction

Because you may only have a workable concept of what you want your circuit to do, Fairchild places a premium on instruction. Courses are taught by knowledgeable applications engineers at FAIRTECH design centers, and by special arrangement can be taught at your facility. Classrooms equipped with color graphics terminals—one per student—and video projection systems provide the perfect place to explore gate array design.

A first-time customer will take both the hardware design course (1-2 days) for his chosen gate array family and the FAIRCAD training course (5 days). Since FAIRCAD is technology independent, the FAIRCAD seminar need not be repeated to accomplish a design using a different Fairchild gate array family. Instruction on FAIRCAD system installation and administration is also available. A complete listing of class dates and times is available at Fairchild Design Centers and sales offices. Training credits are provided with NRE charges for each design option.

FAIRCAD Hardware Requirements

To run FAIRCAD at your facility you must have the DEC VMS operating system and FAIRCAD-compatible hardware. The following lists operating system and hardware requirements:

- **VMS Operating System V4.2**
- **MicroVAX II, VAX 11/750, 11/780, 11/785, 8600, 8650**
- **Tektronix Graphics Terminals 4113, 4115, 4107, 4109, 4125**
- **VT100-Compatible Terminals (one for each graphics terminal)**
- **9-Track Tape Drive**

FAIRCAD, databases and accompanying files require approximately 50 Megabytes of storage space. In addition to space required for FAIRCAD and its files, approximately 50 Megabytes of storage space is also required for the chosen array.

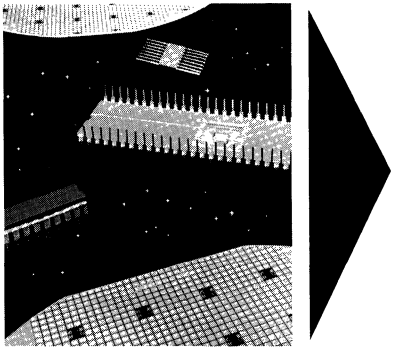
MicroVAX II

FAIRCAD is available for use on the DEC MicroVAX II. All FAIRCAD design tasks, including simulation, placement and routing, can be accomplished using the MicroVAX at your facility. Access to the Cray 1-S Supercomputer for fault simulation is available when designing with the MicroVAX II. Two MicroVAX II configurations are supported for FAIRCAD—the workstation and minicomputer configurations. The workstation configuration, which supports 1-2 users, requires the following:

- **BA123 MicroVAX II cabinet (World Box)**
- **Three 71 Megabyte disk drives (two for single user)**
- **RQDX3 disk controller**
- **1-2 Tektronix graphics terminals (4107, 4109, 4113, 4115, 4125)**
- **1-2 VT220 (VT100-compatible) terminals (one for each graphics terminal)**
- **TK50 tape drive**
- **MicroVMS operating system**

The minicomputer configuration, supporting 1-8 users, includes the following:

- **H9642 MicroVAX II cabinet**
- **5 Megabytes (min) memory**
- **RA81 456 Megabyte fixed disk**
- **1-4 Tektronix graphics terminals (4107, 4109, 4113, 4115, 4125)**
- **1-4 VT220 (VT100-compatible) terminals (one for each graphics terminal)**
- **TK50 tape drive**
- **MicroVMS operating system**



FAIRCHILD

CMOS Arrays Packaging Guide

Introduction

This guide describes the packaging options available for FGC Series CMOS gate arrays. A wide selection of lead counts and package styles, including dual in-line, leaded chip carriers, pin grid arrays and ceramic flatpaks, is offered. Table 9-1 lists the package styles and lead counts available and planned for each array in the FGC Series.

The following paragraphs summarize the data presented in the table.

Dual In-Line Packages

Plastic and ceramic dual in-line packages with lead counts from 20 to 64 are available for FGC Series arrays with fewer than 4000 equivalent gates. Refer to Table 9-1 for product applicability.

Quad Packages

Plastic and ceramic leaded chip carriers (J-bend) with lead counts from 44 to 84 are available for the entire FGC Series of arrays. Refer to Table 9-1 for specific product applicability.

Pin Grid Arrays

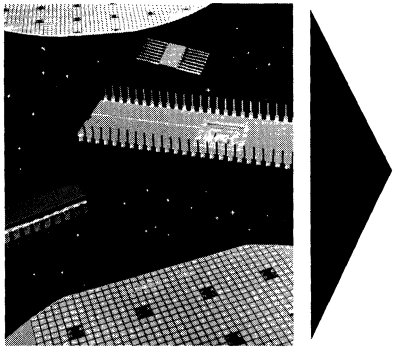
Plastic and ceramic pin grid arrays with lead counts from 68 to 209 are available for all FGC Series arrays except the FGC0500. Refer to Table 9-1 for specific product applicability.

Table 9-1: FGC Series Package Selection Guide

Lead Count	Style	FGC 0500	FGC 1200	FGC 2400	FGC 4000	FGC 6000	FGC 8000
20	PDIP	A					
20	CDIP	P					
24	PDIP	A	A	A			
24	CDIP	A	A	A			
28	PDIP	P	P	A			
28	CDIP	A	A	A			
40	PDIP	A	A	A	P		
40	DCIP	A	A	A	P		
44	PLCC	A	A	A	A		
44	CLCC	P	A	A	P		
48	PDIP		A	A	A		
48	CDIP		A	A	A		
64	PDIP			A			
64	CDIP			A			
68	PLCC		P	A	A	A	
68	CLCC		A	P	P	A	
68	PPGA		A	A	P		
68	CPGA		A	A	A		
84	PLCC			P	A	A	P
84	CLCC		P	A	A	A	P
84	PPGA		A	A	P	P	
84	CPGA		A	A	A	P	
120	PPGA			A	A	P	
120	CPGA			A	A	A	
132	CFPAK				P	P	
144	PPGA				P	A	A
144	CPGA				A	A	A
180	CPGA					A	A
209	CPGA						A

PDIP = Plastic Dual In-Line Package
CDIP = Ceramic Dual In-Line Side Brazed Package
PLCC = Plastic Leaded Chip Carrier (J-Bend Leads)
CLCC = Ceramic Leaded Chip Carrier (J-Bend Leads)
PPGA = Plastic Pin Grid Array
CPGA = Ceramic Pin Grid Array
CFPAK = Ceramic Flatpak

A = Available
P = Planned



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Notes

Notes

DC Characteristics for 'AC Family Devices

Symbol	Parameter	Conditions	Vcc (V)	74AC		54AC	74AC	Units
				$T_A = 25°C$		$T_A =$ −55° to +125°C	$T_A =$ −40° to +85°C	
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	$V_{OUT} = 0.1$ V or $V_{CC}-0.1$ V	3.0	1.5	2.1	2.1	2.1	V
			4.5	2.25	3.15	3.15	3.15	
			5.5	2.75	3.85	3.85	3.85	
V_{IL}	Maximum Low Level Input Voltage	$V_{OUT} = 0.1$ V or $V_{CC}-0.1$ V	3.0	1.5	0.9	0.9	0.9	V
			4.5	2.25	1.35	1.35	1.35	
			5.5	2.75	1.65	1.65	1.65	
V_{OH}	Minimum High Level Output Voltage	$I_{OUT} = -50\ \mu A$	3.0	2.99	2.9	2.9	2.9	V
			4.5	4.49	4.4	4.4	4.4	
			5.5	5.49	5.4	5.4	5.4	
		*$V_{IN} = V_{IL}$ or V_{IH}						
		I_{OH} −12 mA	3.0		2.56	2.4	2.46	V
		I_{OH} −24 mA	4.5		3.86	3.7	3.76	
		I_{OH} −24 mA	5.5		4.86	4.7	4.76	
V_{OL}	Maximum Low Level Output Voltage	$I_{OUT} = 50\ \mu A$	3.0	0.002	0.1	0.1	0.1	V
			4.5	0.001	0.1	0.1	0.1	
			5.5	0.001	0.1	0.1	0.1	
		*$V_{IN} = V_{IL}$ or V_{IH}						
		I_{OL} 12 mA	3.0		0.32	0.4	0.37	V
		I_{OL} 24 mA	4.5		0.32	0.4	0.37	
		I_{OL} 24 mA	5.5		0.32	0.4	0.37	
I_{IN}	Maximum Input Leakage Current	$V_I = V_{CC}$, GND	5.5		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3-State Current	V_I (OE) = V_{IL}, V_{IH} $V_I = V_{CC}$, V_{GND} $V_O = V_{CC}$, GND	5.5		±0.5	±10.0	±5.0	μA
I_{OLD}	†Minimum Dynamic Output Current	$V_{OLD} = 1.1$ V	5.5			57	86	mA
I_{OHD}		$V_{OHD} = 3.85$ V	5.5			−50	−75	mA

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 20 ms, one output loaded at a time.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	Conditions	Vcc (V)	74ACT		54ACT	74ACT	Units
				$T_A = 25°C$		$T_A = -55°$ to $+125°C$	$T_A = -40°$ to $+85°C$	
				Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	$V_{OUT} = 0.1$ V or $V_{CC}-0.1$ V	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low Level Input Voltage	$V_{OUT} = 0.1$ V or $V_{CC}-0.1$ V	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High Level	$I_{OUT} = -50\ \mu A$	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V
		*$V_{IN} = V_{IL}$ or V_{IH} I_{OH} −24 mA −24 mA	4.5 5.5	0.0001	3.86 4.86	3.70 4.70	3.76 4.76	V
V_{OL}	Maximum Low Level Output Voltage	$I_{OUT} = 50\ \mu A$	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V
		*$V_{IN} = V_{IL}$ or V_{IH} I_{OL} 24 mA 24 mA	4.5 5.5		0.32 0.32	0.40 0.40	0.37 0.37	V
I_{IN}	Maximum Input	$V_I = V_{CC}$, GND	5.5		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3-State Current	$V_I = V_{IL}$, V_{IH} $V_O = V_{CC}$, GND	5.5		±0.5	±10.0	±5.0	μA
I_{CCT}	Maximum Icc/Input	$V_I = V_{CC}-2.1$ V	5.5	0.6		1.6	1.5	mA
I_{OLD}	†Minimum Dynamic Output Current	$V_{OLD} = 1.1$ V	5.5			57	86	mA
I_{OHD}		$V_{OHD} = 3.85$ V	5.5			−50	−75	mA

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

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