Operation Codes, Numerical Listing

OP	MNEM	BY	CY	OP	MNEM	BY	CY	OP	MNEM	BY	CY	OP	MNEM	BY	CY
00	LR A,KU	1	1	17	ST	1	2.5	4r	LR A,r	1	1	90	BR	2	3.5
01	LR A,KL	1	1	18	COM	1	1	5r	LR r,A	1	1	91	BM	2	3.5/3**
02	LR A,QU	1	1	19	LNK	1	1	6.0a	LISU a	1	1	92	BNC	2	3.5/3**
03	LR A,QL	1	1	1A	DI	1	2	6.1a	LISL a	1	1	93	BF 3	2	3.5/3**
04	LR KU,A	1	1	1B	EI*	1	2	70	CLR	1	1	94	BNZ	2	3.5/3**
05	LR KL,A	1	1	1C	POP*	1	2	7i	LIS i	1	1	95	BF 5	2	3.5/3**
06	LR QU,A	1	1	1D	LR W,J*	1	2	80	BT 0	2	3	96	BF 6	2	3.5/3**
07	LR QL,A	1	1	1E	LR J,W	1	1	81	BP	2	3.5/3**	97	BF 7	2	3.5/3**
08	LR K,P	1	4	1F	INC	1	1	82	BC	2	3.5/3**	98	BNO	2	3.5/3**
09	LR P,K	1	4	20	LI	2	2.5	83	BT 3	2	3.5/3**	99	BF 9	2	3.5/3**
0A	LR A,IS	1	1	21	NI	2	2.5	84	BZ	2	3.5/3**	9A	BF A	2	3.5/3**
0B	LR IS,A	1	1	22	OI	2	2.5	85	BT 5	2	3.5/3**	9B	BF B	2	3.5/3**
0C	PK*	1	4	23	XI	2	2.5	86	BT 6	2	3.5/3**	9C	BF C	2	3.5/3**
0D	LR P0,Q	1	4	24	AI	2	2.5	87	BT 7	2	3.5/3**	9D	BF D	2	3.5/3**
0E	LR Q,DC	1	4	25	CI	2	2.5	88	AM	1	2.5	9E	BF E	2	3.5/3**
0F	LR DC,Q	1	4	26	IN	2	4	89	AMD	1	2.5	9F	BF F	2	3.5/3**
10	LR DC,H	1	4	27	OUT*	2	4	8A	NM	1	2.5	Aa	INS a	1	4***
11	LR H,DC	1	4	28	PI*	3	6.5	8B	OM	1	2.5	Ba	OUTSa*	1	4***
12	SR 1	1	1	29	JMP*	3	5.5	8C	XM	1	2.5	Cr	AS r	1	1
13	SL 1	1	1	2A	DCI	3	6	8D	CM	1	2.5	Dr	ASD r	1	2
14	SR 4	1	1	2B	NOP	1	1	8E	ADC	1	2.5	Er	XS r	1	1
15	SL 4	1	1	2C	XDC	1	2	8F	BR7	2	2.5 2**	Fr	NS r	1	1
16	LM	1	2.5	3r	DS r	1	1.5								

Mnemonics, Alphabetical Listing

MNEM	CODE	BY	CY	MNEM	CODE	BY	CY	MNEM	CODE	BY	CY	MNEM	CODE	BY	CY
ADC	8E	1	2.5	CM	8D	1	2.5	LR A,QL	03	1	1	NM	8A	1	2.5
AI ii	24 ii	2	2.5	COM	18	1	1	LR A,QU	02	1	1	NOP	2B	1	1
AM	88	1	2.5	DCI aaaa	2A aa aa	3	6	LR A,r	4r	1	1	NS r	Fr	1	1
AMD	89	1	2.5	DI	1A	1	2	LR DC,H	10	1	4	OI ii	22 ii	2	2.5
AS r	Cr	1	1	DS r	3r	1	1.5	LR DC,Q	0F	1	4	OM	8B	1	2.5
ASD r	Dr	1	2	EI*	5B	1	2	LR H,DC	11	1	4	OUT* aa	27 aa	2	4
BC aa**	82 aa	2	3.5/3	INC	1F	1	1	LR IS,A	0B	1	1	OUTS* a	Ba	1	4***
BF taa**	9t aa	2	3.5/3	IN aa	26 aa	2	4***	LR J,W	1E	1	1	PI* aaaa	28 aa aa	3	6.5
BM aa**	91 aa	2	3.5/3	INS a	Aa	1	4	LR KL,A	05	1	1	PK*	0C	1	4
BNC aa**	92 aa	2	3.5/3	JMP* aaaa	29 aa aa	3	5.5	LR K,P	08	1	4	POP*	1C	1	2
BNO aa**	98 aa	2	3.5/3	LI ii	20 ii	2	2.5	LR KU,A	04	1	1	SL 1	13	1	1
BNZ aa**	94 aa	2	3.5/3	LIS i	7i	1	1	LR P,K	09	1	4	SL 4	15	1	1
BP aa**	81 aa	2	3.5/3	LISL a	6.1 a****	1	1	LR P0,Q	0D	1	4	SR 1	12	1	1
BR aa**	90 aa	2	3.5	LISU a	6.0 a****	1	1	LR Q,DC	0E	1	4	SR 4	14	1	1
BR7 aa**	8F aa	2	2.5/3	LM	16	1	2.5	LR QL,A	07	1	1	ST	17	1	2.5
BT taa**	8t aa	2	3.5/3	LNK	19	1	1	LR QU,A	06	1	1	XDC	2C	1	2
BZ aa**	84 aa	2	3.5/3	LR A,IS	0A	1	1	LR r,A	5r	1	1	XI ii	23 ii	2	2.5
CI ii	25 ii	2	2.5	LR A,KL	01	1	1	LR W,J*	1D	1	2	XM	8C	1	2.5
CLR	70	1	1	LR A,KU	00	1	1	NI ii	21 ii	2	2.5	XS r	Er	1	1

* Privileged instruction
** Use second number if branch is not taken
*** 2 cycles for CPU Ports, non-privileged instruction
**** 3-bit octal digit

OP = Operation code
BY = Bytes
CY = Cycles

— = Status Unaffected
0 = Status Cleared
1 = Status Set

Register Organization in F8

Input/Output Ports Assignment

3850 CPU				
I/O Port A	00			
I/O Port B	01			
3851 PSU				
I/O Port A	x0*	x4	x8	xC
I/O Port B	x1*	x5	x9	xD
Local Interrupt Control	x2*	x6	xA	xE
Timer Port	x3*	x7	xB	xF
3852 Dynamic Memory Interface	**Version**	**A**		**B**
General Purpose Latch		0C		EC
RAM Refresh & DMA Control		0D		ED

*Cannot use 00, 01, 02, 03

3853 Static Memory Interface						
Interrupt Vector (MSB)						0C
Interrupt Vector (LSB)						0D
Local Interrupt Control						0E
Timer Port						0F
3854 DMA			Register			
	P2	P1	00	01	02	03
	0	0	F0	F1	F2	F3
	0	1	F4	F5	F6	F7
	1	0	F8	F9	FA	FB
	1	1	FC	FD	FE	FF

Local Interrupt Control Codes

00	Disable local interrupt
01	Enable local interrupt, select external interrupt
11	Enable local interrupt, select internal interrupt
10	Disable local interrupt

Scratchpad Addressing Modes

r = 0 through B:		Direct addressing; address contained in the 4 lower bits of the instruction.
r = C,D,E:	Assembly Mnemonic	Indirect addressing; address contained in ISAR.
	r = S	r = H'C' ISAR is unmodified . . .
	r = 1	r = H'D' ISAR is incremented . . .
	r = D	r = H'E' ISAR is decremented . . . after execution.
r = F		Illegal operation

Only ISARL is affected by Increment and Decrement scratchpad addressing modes. ISARU remains unchanged.

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F8 and F3870 Microprocessor User Reference Card

Accumulator Group Instructions

Operation	MNEM	Code	Function	Bytes	Cycles	Ovf	Zero	Cry	Sign
Add Carry	LNK	19	ACC ← (ACC) + CB	1	1	1/0	1/0	1/0	1/0
Add Immediate	AI ii	24 ii	ACC ← (ACC) + H'ii'	2	2.5	1/0	1/0	1/0	1/0
AND Immediate	NI ii	21 ii	ACC ← (ACC) ∧ H'ii'	2	2.5	0	1/0	0	1/0
Clear	CLR	70	ACC ← H'00'	1	1	—	—	—	—
Compare Immediate	CI ii	25 ii	H'ii' + $\overline{(ACC)}$ + 1	2	2.5	1/0	1/0	1/0	1/0
Complement	COM	18	ACC ← (ACC) ⊕ H'FF'	1	1	0	1/0	0	1/0
Exclusive-OR Immediate	XI ii	23 ii	ACC ← (ACC) ⊕ H'ii'	2	2.5	0	1/0	0	1/0
Increment	INC	1F	ACC ← (ACC) + 1	1	1	1/0	1/0	1/0	1/0
Load Immediate	LI ii	20 ii	ACC ← H'ii'	2	2.5	—	—	—	—
Load Immediate Short	LIS i	7i	ACC ← H'0i'	1	1	—	—	—	—
OR Immediate	OI ii	22 ii	ACC ← (ACC) ∨ H'ii'	2	2.5	0	1/0	0	1/0
Shift Left One	SL 1	13	ACC Shift Left 1	1	1	0	1/0	0	1/0
Shift Left Four	SL 4	15	ACC Shift Left 4	1	1	0	1/0	0	1/0
Shift Right One	SR 1	12	ACC Shift Right 1	1	1	0	1/0	0	1
Shift Right Four	SR 4	14	ACC Shift Right 4	1	1	0	1/0	0	1

Scratchpad Register Instructions

Add Binary	AS r	Cr	ACC ← (ACC) + (r)	1	1	1/0	1/0	1/0	1/0
Add Decimal	ASD r	Dr	ACC ← (ACC) + (r)	1	2	1/0	1/0	1/0	1/0
AND	NS r	Fr	ACC ← (ACC) ∧ (r)	1	1	0	1/0	0	1/0
Decrement	DS r	3r	r ← (r) + H'FF'	1	1.5	1/0	1/0	1/0	1/0
Exclusive OR	XS r	Er	ACC ← (ACC) ⊕ (r)	1	1	0	1/0	0	1/0
Load	LR A,KU	00	ACC ← (r12)	1	1	—	—	—	—
Load	LR A,KL	01	ACC ← (r13)	1	1	—	—	—	—
Load	LR A,QU	02	ACC ← (r14)	1	1	—	—	—	—
Load	LR A,QL	03	ACC ← (r15)	1	1	—	—	—	—
Load	LR A,r	4r	ACC ← (r)	1	1	—	—	—	—
Load	LR KU,A	04	r12 ← (ACC)	1	1	—	—	—	—
Load	LR KL,A	05	r13 ← (ACC)	1	1	—	—	—	—
Load	LR QU,A	06	r14 ← (ACC)	1	1	—	—	—	—
Load	LR QL,A	07	r15 ← (ACC)	1	1	—	—	—	—
Load	LR r,A	5r	r ← (ACC)	1	1	—	—	—	—

Scratchpad Address Register Instructions

Load ISAR	LR IS,A	0B	ISAR ← (ACC)	1	1	—	—	—	—
Load ISAR Lower	LISL a	6,1a****	ISARL ← a	1	1	—	—	—	—
Load ISAR Upper	LISU a	6,0a****	ISARU ← a	1	1	—	—	—	—
Store ISAR	LR A,IS	0A	ACC ← (ISAR)	1	1	—	—	—	—

Memory Reference Instructions

Data Counter is always incremented: DC ← DC + 1

Add Binary	AM	88	ACC ← (ACC) + ((DC))	1	2.5	1/0	1/0	1/0	1/0
Add Decimal	AMD	89	ACC ← (ACC) + ((DC))	1	2.5	1/0	1/0	1/0	1/0
AND	NM	8A	ACC ← (ACC) ∧ ((DC))	1	2.5	0	1/0	0	1/0
Compare	CM	8D	((DC)) + $\overline{(ACC)}$ + 1	1	2.5	1/0	1/0	1/0	1/0
Exclusive OR	XM	8C	ACC ← (ACC) ⊕ ((DC))	1	2.5	0	1/0	0	1/0
Load	LM	16	ACC ← ((DC))	1	2.5	—	—	—	—
Logical OR	OM	8B	ACC ← (ACC) ∨ ((DC))	1	2.5	0	1/0	0	1/0
Store	ST	17	((DC)) ← (ACC)	1	2.5	—	—	—	—

Program Counter Instructions

Jump* †	JMP aaaa	29 aa aa	PC0 ← H'aaaa'	3	5.5	—	—	—	—
Call to Subroutine* †	PI aaaa	28 aa aa	PC1 ← (PC0); PC0 ← H'aa'	3	6.5	—	—	—	—
Call to Subroutine*	PK	0C	PC1 ← (PC0); PC0U ← (r12); PC0L ← (r13)	1	4	—	—	—	—
Load Stack Register	LR P,K	09	PC1U ← (r12); PC1L ← (r13)	1	4	—	—	—	—
Load Program Counter	LR P0,Q	0D	PC0U ← (r14); PC0L ← (r15)	1	4	—	—	—	—
Return from Subroutine*	POP	1C	PC0 ← (PC1)	1	2	—	—	—	—
Store Stack Register	LR K,P	08	r12 ← (PC1U); r13 ← (PC1L)	1	4	—	—	—	—

† alters contents of accumulator

Data Counter Instructions

Add to Data Counter	ADC	8E	DC ← (DC) + (ACC)	1	2.5	—	—	—	—
Load DC Immediate	DCI aaaa	2A aa aa	DC ← H'aaaa'	3	6	—	—	—	—
Load Data Counter	LR DC,H	10	DCU ← (r10); DCL ← (r11)	1	4	—	—	—	—
Load Data Counter	LR DC,Q	0F	DCU ← (r14); DCL ← (r15)	1	4	—	—	—	—
Store Data Counter	LR H,DC	11	r10 ← (DCU); r11 ← (DCL)	1	4	—	—	—	—
Store Data Counter	LR Q,DC	0E	r14 ← (DCU); r15 ← (DCL)	1	4	—	—	—	—
Exchange DC ††	XDC	2C	DC0 ⇄ DC1	1	2	—	—	—	—

Status Register Instructions

Load Status Register*	LR W,J	1D	W ← (r9)	1	2	1/0	1/0	1/0	1/0
Store Status Register	LR J,W	1E	r9 ← (W)	1	1	—	—	—	—

Input/Output Instructions

Input	IN aa	26 aa	ACC ← (Input Port aa)	2	4	0	1/0	0	1/0
Input Short	INS a	Aa	ACC ← (Input Port a)	1	4***	0	1/0	0	1/0
Output*	OUT aa	27 aa	Output Port aa ← (ACC)	2	4	—	—	—	—
Output Short*	OUTS a	Ba	Output Port a ← (ACC)	1	4***	—	—	—	—

Interrupt Instructions

Disable Interrupt	DI	1A	Reset ICB	1	2	—	—	—	—
Enable Interrupt*	EI	1B	Set ICB	1	2	—	—	—	—

No Operation Instruction

No Operation	NOP	2B	PC0 ← (PC0) + 1	1	1	—	—	—	—

††F8 instruction only — not for F387X

Branch Instructions

If the test condition is not met, PC0 ← (PC0) + 2; execution complete in 3 cycles.

Branch on Carry	BC aa	82 aa	PC0 ← (PC0) + 1 + H'aa' if C = 1	2	3.5/3**	—	—	—	—
Branch on Positive	BP aa	81 aa	PC0 ← (PC0) + 1 + H'aa' if S = 1	2	3.5/3**	—	—	—	—
Branch on Zero	BZ aa	84 aa	PC0 ← (PC0) + 1 + H'aa' if Z = 1	2	3.5/3**	—	—	—	—
Branch on True	BT t,aa	8t aa	PC0 ← (PC0) + 1 + H'aa' if any test is true, t = test condition	2	3.5/3**	—	—	—	—

2^2	2^1	2^0
Zero	CB	Sign

Branch if Negative	BM aa	91 aa	PC0 ← (PC0) + 1 + H'aa' if S = 0	2	3.5/3**	—	—	—	—
Branch if No Carry	BNC aa	92 aa	PC0 ← (PC0) + 1 + H'aa' if C = 0	2	3.5/3**	—	—	—	—
Branch if No Overflow	BNO aa	98 aa	PC0 ← (PC0) + 1 + H'aa' if O = 0	2	3.5/3**	—	—	—	—
Branch if Not Zero	BNZ aa	94 aa	PC0 ← (PC0) + 1 + H'aa' if Z = 0	2	3.5/3**	—	—	—	—
Branch if False	BF t,aa	9t aa	PC0 ← (PC0) + 1 + H'aa' if all tests are false, t = test condition	2	3.5/3**	—	—	—	—

2^3	2^2	2^1	2^0
OVF	Zero	CB	Sign

Branch if ISAR (L) ≠ 7	BR7 aa	8F aa	PC0 ← (PC0) + 1 + H'aa' if ISARL ≠ 7,	2	2.5	—	—	—	—
			PC0 ← (PC0) + 2 if ISARL = 7		2.0	—	—	—	—
Branch Relative	BR aa	90 aa	PC0 ← (PC0) + 1 + H'aa'	2	3.5	—	—	—	—

* Privileged instruction
** Use second number if branch is not taken
*** 2 cycles for CPU Ports, non-privileged instruction
**** 3-bit octal digit

Branch Conditions for BF Instruction

Operand	Status Flags Tested					
t	OVF	Zero	Carry	Sign	Definition	Comments
0	0	0	0	0	Unconditional Branch relative	
1	0	0	0	1	Branch on negative	BM
2	0	0	1	0	Branch if no carry	BNC
3	0	0	1	1	Branch if no carry and negative	
4	0	1	0	0	Branch if not zero	BNZ
5	0	1	0	1	Branch on negative	Same as t = 1
6	0	1	1	0	Branch if no carry and result is not zero	
7	0	1	1	1	Branch if no carry and negative	Same as t = 3
8	1	0	0	0	Branch if there is no overflow	BNO
9	1	0	0	1	Branch if negative and no overflow	
A	1	0	1	0	Branch if no overflow and no carry	
B	1	0	1	1	Branch if no overflow, no carry and negative	
C	1	1	0	0	Branch if no overflow and not zero	
D	1	1	0	1	Branch if negative and no overflow	Same as t = 9
E	1	1	1	0	Branch if no overflow, no carry and not zero	
F	1	1	1	1	Branch if no overflow, no carry and negative	Same as t = B

Branch Conditions for BT Instruction

Operand	Status Flags Tested				
t	Zero	Carry	Sign	Definition	Comments
0	0	0	0	Do not branch	An effective 3 cycle NO-OP, 2 Bytes
1	0	0	1	Branch if positive	Same as BP
2	0	1	0	Branch on carry	Same as BC
3	0	1	1	Branch if positive or on carry	
4	1	0	0	Branch if zero	Same as BZ
5	1	0	1	Branch if positive	Same as t = 1
6	1	1	0	Branch if zero or on carry	
7	1	1	1	Branch if positive or on carry	Same as t = 3