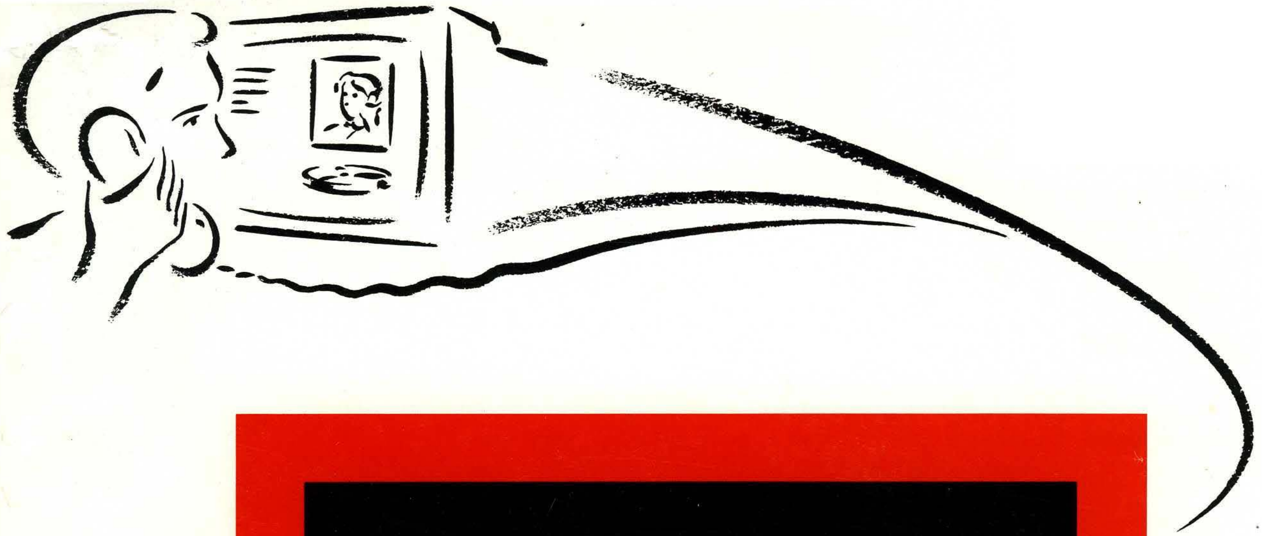
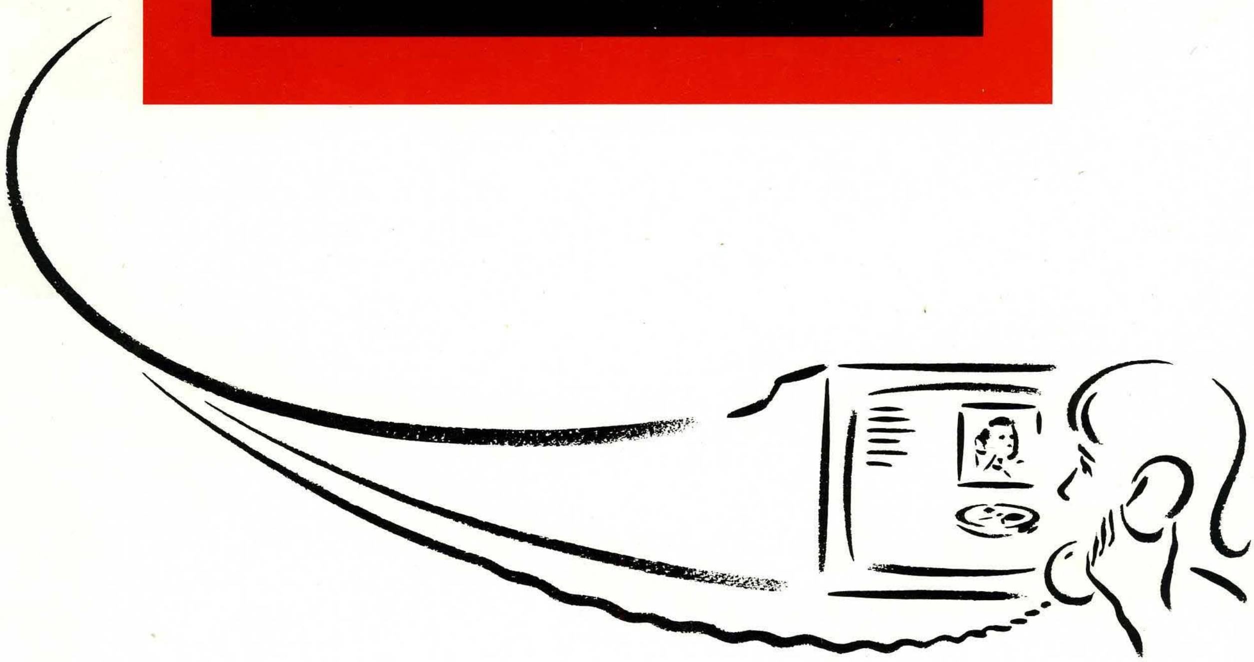


FUJITSU

Asynchronous Transfer Mode

ICs for ATM
1993



This brochure contains information on Fujitsu's ATM technology. In chapter one you will discover Fujitsu's vast worldwide network of sales offices and design centers and find important information regarding Fujitsu's philosophy and quality and reliability program.

The following chapters give a comprehensive explanation of ATM including the actual definition, target market, product features, support, applications, overview and operation, and a summary.

If you would like more information on ATM, or other Fujitsu products, simply fill out the enclosed reply card and drop it in the mail. Or, just call us. The attached list on the back page provides you with an address and telephone list of Fujitsu sales offices worldwide.

Printed in Germany.

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Fujitsu worldwide

Fujitsu. Local partnership, global leadership
Fujitsu Electronic Devices Group is a major force on the global electronics scene. Along with the Computer and Telecommunications divisions it forms a $29 billion company having more than 162,000 employees worldwide. Continuing success stems from three major factors.

Customer satisfaction
With a twenty years of leadership in computers, telecommunications and electronics devices, Fujitsu is uniquely placed to provide total solutions, often across traditional technology boundaries.

Partnership & synergy
Helping Fujitsu respond quickly and precisely to customer needs; to build on areas of strength while developing products highly tuned to customer needs.

Creating new technologies
Maintaining technical leadership means investing in technologies that will drive systems far into the future. Which is why Fujitsu spends 10% of sales annually on research, design and development, carried out in its centers of excellence throughout the world.

Around the world, day after day, Fujitsu's time to market cycles provide customers with the products they want, when they need them.

Figure 1: Fujitsu Electronic Devices worldwide presence


Sales Offices
Manufacturing Plants
R & D Centers
Headquarters

Quality you can rely on

Fujitsu's worldwide reputation for quality starts with excellence in technology and in people. Monitored by experienced quality control teams, every aspect of the company and its products follows rigorous management procedures - many of them recognized internationally. Worldwide, Fujitsu's major facilities anticipate ISO9000 approval by 1995.

Quality throughout
Quality is checked to relevant standards at every stage of the manufacturing process, with statistical process control ensuring rigorous, objective conformity to strict controls and norms.

But Fujitsu quality goes way beyond formal targets, by applying a unique system of individual initiative in quality control - the jishu check.

Jishu. Spontaneous and self-initiated excellence
In Japanese jishu means 'spontaneous and self-initiated.' Thus each Fujitsu employee applies advanced skills and training to find as many defective products as possible, and reject them. Jishu checks mean best-attainable quality.

Reliability. Built in from the start

The Fujitsu Reliability Progam is your guarantee of absolute product dependability. Right at the start, market research identifies key reliability criteria from analysis of applications and customer needs. This is the benchmark throughout the product's life.

Qualification and approvals
Engineering tests on pre-production samples provide the vital qualification data.

- Comprehensive environmental and mechanical characterization: lead integrity, thermal shock, vibration, mechanical shock, sealing and solderability.
- Stress testing: thermal cycling and pressure, temperature, humidity (PTH) bias.
- Endurance testing: life tests at high/low temperatures and high humidity.

Screening to your specifications
As well as the standard reliability grade, IC products for the most demanding applications are screened to high-reliability specifications. Burn-in eliminates early-life failures, while high/low temperature tests ensure reliability, e.g., for automotive components.

Monitoring. Confirming product reliability
During volume production, performance standards are maintained through continuing environmental and endurance tests, including 100-cycle thermal checks and 3,000-hour life tests.

Open partnership
Customer response closes the quality loop. For example, failure analysis helps to improve Fujitsu products and manufacturing procedures continuously. This feedback is vital. After all, Fujitsu's reputation for quality depends on its customers.

In quality, reliability and in every transaction, at Fujitsu, the customer comes first. Always.

Asynchronous Transfer Mode - ATM

What is ATM ?

ATM is a protocol which defines the transport of information in fixed-length packets or 'cells'. This technique was defined by the Consultative Committee for International Telephone & Telegraph (CCITT) during the mid-80s as a basis for the broadband public networks of the next century. The first standards appeared in the CCITT's "Blue Books" issued in 1988. In 1991, four companies (Sprint, Northern Telecom, Cisco Systems and Adaptive) established the "ATM Forum" to investigate the use of ATM within private networks. This forum has now grown to over 250 members, with representatives from all major sectors of the industry including workstation vendors, LAN and WAN equipment suppliers, service providers and PTTs, and other potential users. Fujitsu is a principal member. The ATM Forum's main goal is to accelerate the use of ATM by enabling interoperability between equipment from different vendors. It has also become a major influence on the development of ATM standards.

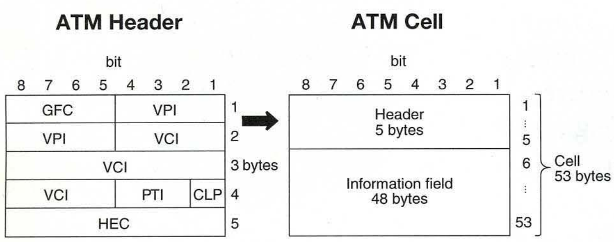
Technical Features

ATM is a technology that combines the best features of switched and packet-based techniques. It is based on a 53-byte cell, with a 48-byte information field and a 5-byte header (see Fig. 2). The header contains a 'cell-identifier' which associates the cell with a particular connection. This structure is the key to ATM's technical benefits such as high-speed operation, scalability and support for multiple data types.

The fixed cell length, and the identifier information in the header, allow switching to be performed in hardware significantly increasing the potential speed. The cell-identifier has two parts; virtual path and virtual circuit. A virtual path may be regarded as equivalent to a trunk line in a telephone network, transporting many simultaneous calls (virtual circuits). Switching can be performed using one or both fields (see Fig. 3). This ability to support multiple, independent connections means different data types may be mixed on the same physical link. The short, fixed cell length minimizes the latency in gaining access to the communications channel. Compared to existing packet networks, with their long, variable-length frames, this improves ATM's ability to transport delay-sensitive traffic such as voice and video.

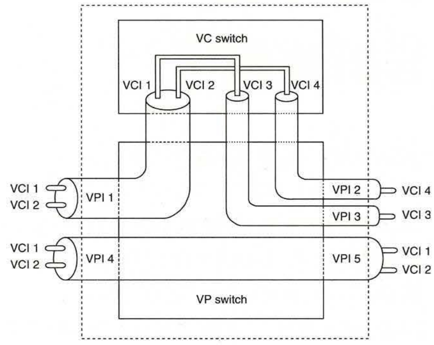
The ATM protocol is independent of the physical transmission medium selected. This enables the most appropriate interface to be chosen for each connection. Future upgrades can be achieved by changing only the physical layer functions.

ATM Cell Format Figure 2



CLP Cell loss priority
GFC Generic flow control
HEC Header error control
PTI Payload type indicator
VCI Virtual channel identifier
VPI Virtual path identifier

Virtual Circuit/ Virtual Path Switching Figure 3



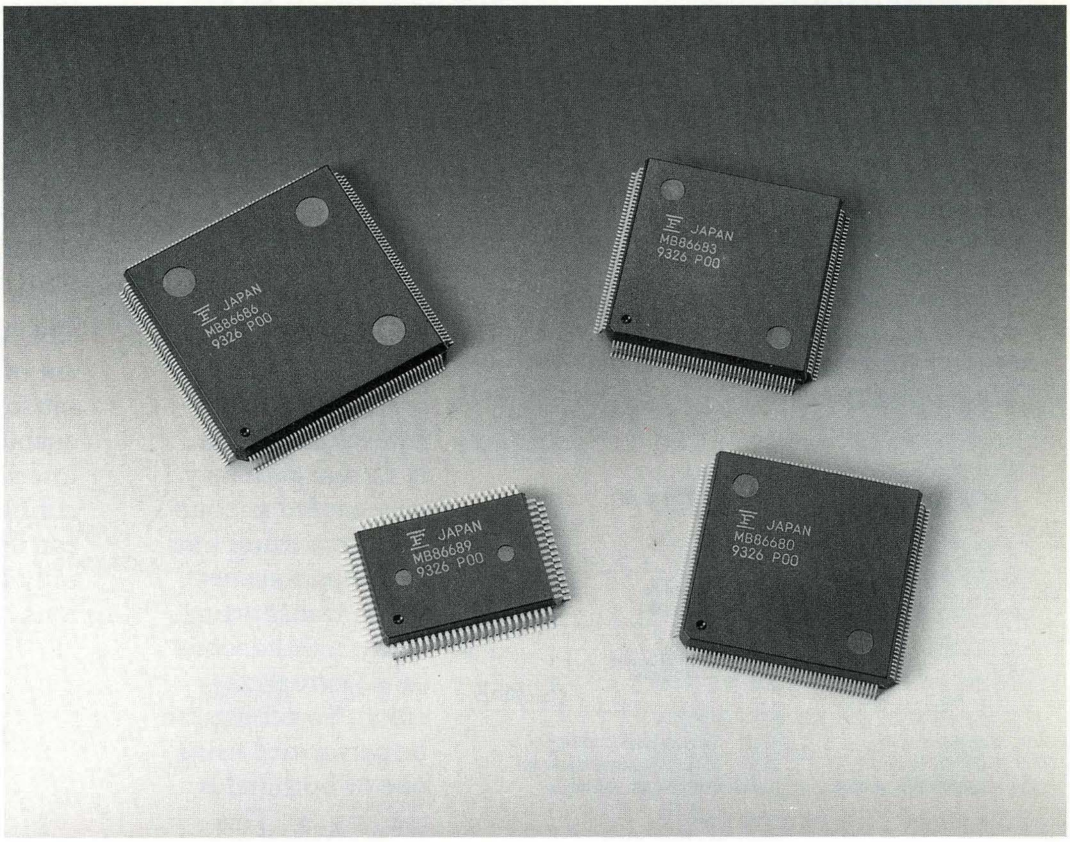
VCI Virtual channel identifier
VP Virtual path
VPI Virtual path identifier

ATM in the Private Network

The first commercial applications of ATM are expected to be in private networks as a solution to the performance limitations of current networking methods. These limitations stem from the use of 'shared-media' technologies such as Ethernet, where the average bandwidth available at any workstation is only some fraction of the theoretical maximum. Due to the rapid increase in workstation processor power, the move to client-server networks, and the growth in demand for data communications, this restriction is expected to cause increasing problems. New applications, especially those involving video/imaging data, will only worsen the situation. One approach to network 'bottlenecks' has been to segment the network into ever smaller sections by use of bridges and/or routers. However, this makes network management, already a problem with shared media due to the difficulties in locating faults or congestion, more difficult. In addition to addressing these issues, any alternative technology must offer the user a high degree of 'future-proofing'.

ATM offers technical advantages in terms of operation speed, scalability and support for various types of data. Hardware switching enables ATM to offer immediate increases in network speeds. Future upgrades can be achieved by the addition of switching capacity or through developments in silicon technology, and will be simpler to implement due to ATM's 'media-independence.' The support it offers for delay-sensitive traffic makes ATM the best solution for new, 'multimedia' applications. As ATM is a connection-oriented protocol, the task of statistics gathering and network management is simplified.

Finally, ATM is the first protocol intended for use in both local and wide-area applications, and is the basis for the public networks of the future. It therefore offers the potential to combine today's separate data and telecommunications networks into one, hence reducing complexity and costs.



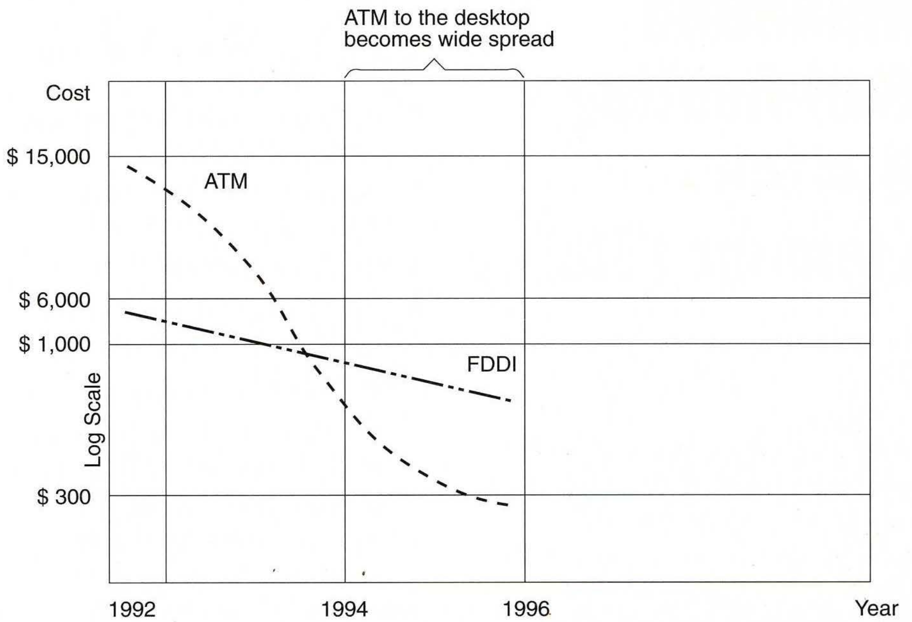
Fujitsu and ATM

In recognition of the importance of local technical expertise, Fujitsu has established R&D centers in both Europe and the U.S. The design activities at these centers focus on application areas of specific local importance. The main focus in the U.S is therefore on RISC processors and Ethernet products, to reflect the strength of U.S workstation and LAN vendors. In Europe, the telecommunications market is the focal point, with the development of several products for narrowband ISDN.

Fujitsu's European design team, based in Manchester, UK, is a balanced combination of IC design experts, and communications systems specialists. This balance is vital to the successful implementation of complex communications functions in silicon. The ATM program arose from this design center's narrowband ISDN activities. However, the importance of ATM in the LAN/WAN market was recognized at an early stage, and this has had a major influence on the design goals.

The main objective of the program was to map the major ATM functions, defined by existing standards, into silicon. The ICs must also enable equipment vendors to offer end user pricing per ATM port that would be competitive

ATM versus FDDI Cost Projection Figure 4



with other technologies. Despite its many technical advantages, cost will play a major part in the speed of ATM acceptance. One possible model for the trend in ATM pricing is shown in Fig. 4.

Fujitsu's first four products correspond to key elements of the ATM protocol; a self-routing switch element (SRE), an adaptation layer controller (ALC), a cell header processor (ATC) and a network terminator (NTC). Their development has involved significant liaison with several leading systems suppliers. They provide a comprehensive set of functions to enable the design of a wide range of ATM equipment for both local and wide area networking applications.

These devices represent only the first step of Fujitsu's long-term ATM commitment. Fujitsu will continue to use its worldwide resources to develop further leading-edge ATM ICs which will address new functions and applications as standards and the ATM market develop.

Device Descriptions

MB86680 Self-Routing Switch Element (SRE)

Overview
The SRE is a 4x4 cell-switch building-block, which can be used as the basis for a variety of 155Mbps ATM switch fabrics. Although various interconnection topologies can be used, the SRE is ideally suited to the construction of compact matrices due to its row and column expansion ports. These provide re-timed, buffered outputs to simplify device interconnection.

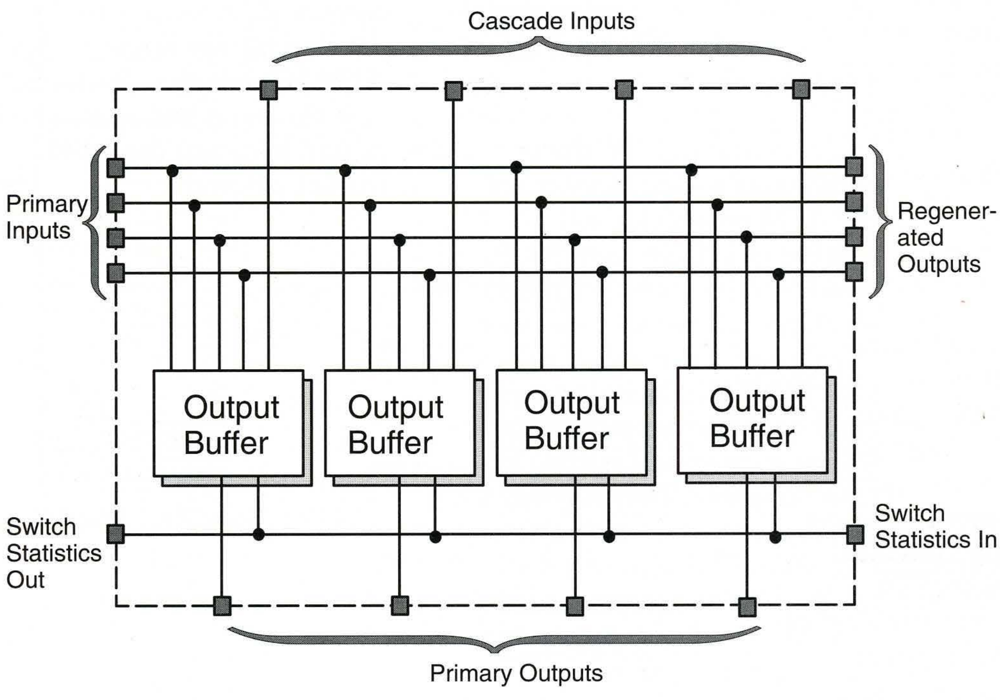
Other key features of the device are:

- Selectable high and low priority queues
- Output queued for non-blocking operation
- Multicast support
- Selective cell discard based on CLP bit and selectable queue fill level
- Statistics gathering for cell discards and buffer overflows
- Routing tag processing is programmable to enable flexibility of switch architecture
- Supplied in 176-pin plastic quad flat package

Operation
A block diagram of the device is shown in Fig. 5. All inputs and outputs are 8-bit parallel, with independent strobe signals. The SRE selects the relevant output for an incoming cell based on a routing tag previously appended to the cell header. This function can be performed either by the Address Translation Controller or the Adaptation Layer Controller, depending on the direction of data flow and the switch configuration.
Extensive simulation has been performed to analyze the behavior of switch fabrics based on the SRE for a wide variety of traffic types and loading factors. A simulation software package is available from Fujitsu to allow users to analyze the performance of the switch in their specific application.
Any switch topology can be defined, and the input traffic can be modelled in terms of parameters such as burst length, peak and average rates. The most important factors are burst length and peak rate. Data having a combination of high peak rate and long burst length should be 'shaped' prior to entering the switch. This is a function that can be performed by the ALC.

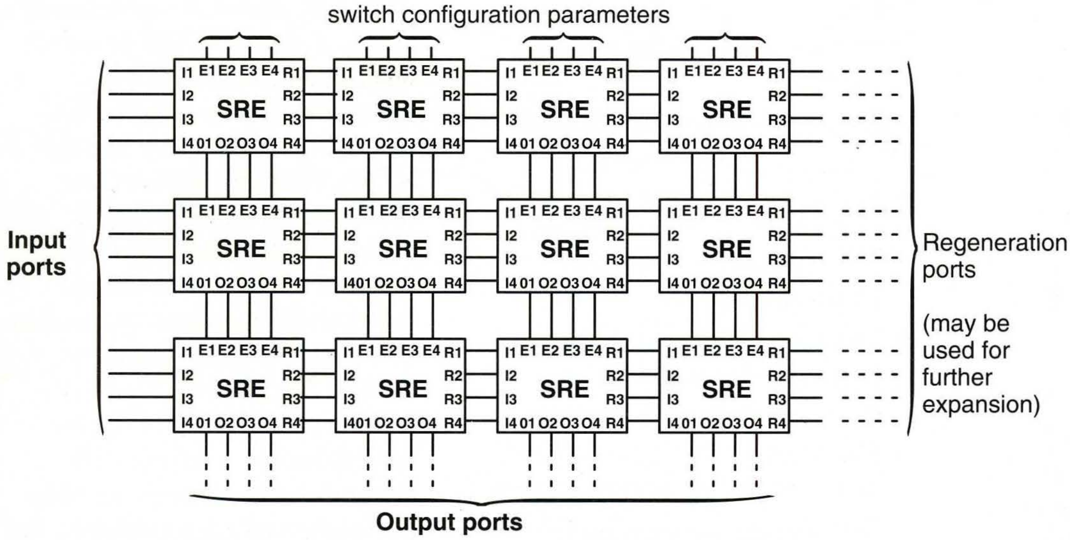
SRE Block Diagram

Figure 5



SRE Switch Matrix

Figure 6

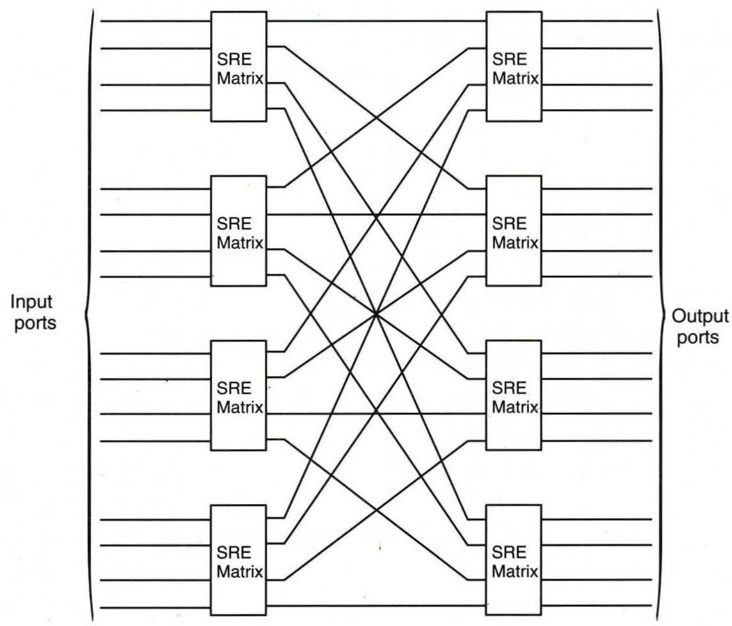


The use of the SRE in a typical matrix application is shown in Fig. 6. As well as re-generating the expansion output port signals to remove the need for any buffering between switch elements, the pin-out of the SRE has been defined to enable devices to be laid out on the board as shown. This enables extremely compact switches to be constructed. One other interesting feature of the SRE is the configuration method. Switch configuration parameters are defined using the input expansion port pins of switches in the top row of the matrix. This information is passed serially to all other SREs during system initialization.

Since the number of elements in a matrix increases proportionally to the square of the number of inputs, the SRE is best suited for relatively small switches (up to 32x32). This should be adequate for most customer premises applications, but larger structures can be achieved by connecting individual matrices in a multi-path delta configuration (Fig. 7). Each switch element can use a selectable part of the tag field, therefore intermediate address translation/tag generation is unnecessary.

Delta Switch Configuration

Figure 7



MB86683 Network Termination Controller (NTC)

Overview

ATM cells may be transported across many different types of physical interfaces. Some examples which have been defined for use with ATM are SDH/SONET type interfaces at 155Mbps, 100Mbps over multimode fiber, a U.S DS3 (45Mbps) service, and its European equivalent, an E3, 34Mbps service. The CCITT has also defined a standard for the transfer of unframed ATM cells. Each physical interface will have specific requirements in terms of framing and synchronization. These functions are defined by the Transmission Convergence (TC) sub-layer of the ATM protocol model.

The NTC is a full-duplex network terminator, which supports multiple interface types. The key features of this device are:

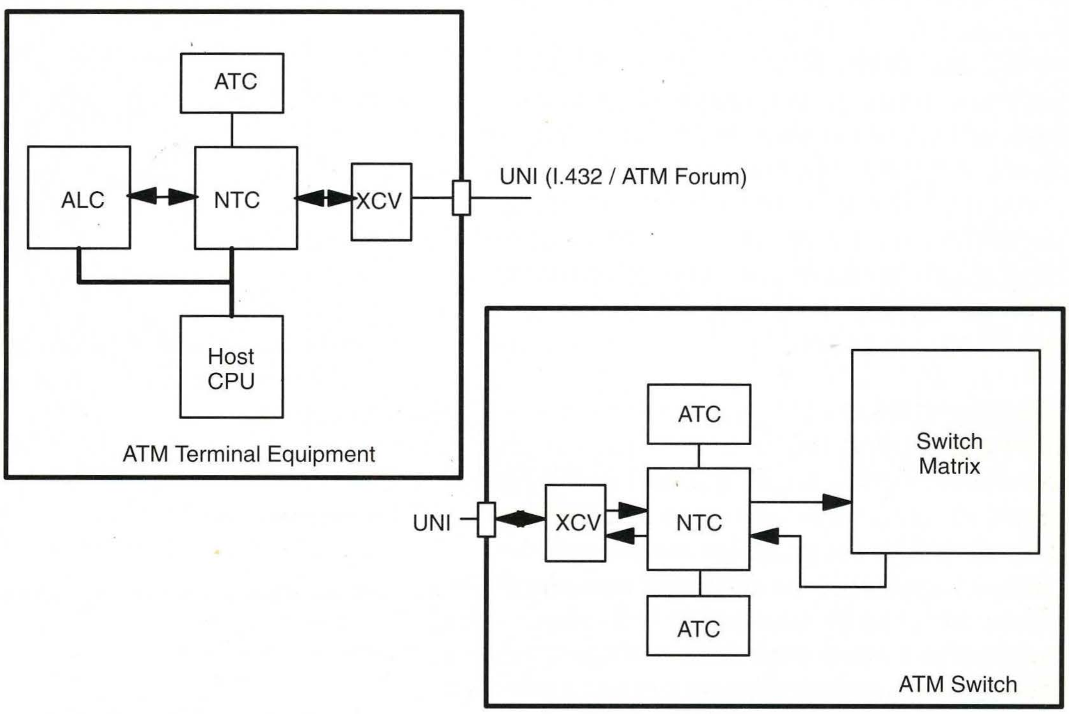
- Implements all TC sub-layer functions for physical media based on SDH/SONET, DS3, E3 and unframed cells
- Direct connection to external transceiver via 8-bit parallel interface
- Support for framed physical layer OAM functions
- Statistics gathering on a per virtual circuit basis including cell and error counts and alarm conditions
- On-chip DMA controller for high-speed transfer of statistics to system memory
- Interfaces directly to Address Translation Controller to perform real-time cell header translation
- Supplied in 176-pin plastic quad flat package

Operation

Two possible configurations involving the NTC are shown in Fig. 8. In the ATM terminal equipment, the NTC is connected to the Adaptation Layer Controller. It takes the ATM cells generated by the ALC and performs all the framing functions required by the selected physical media. An external transceiver handles media-dependent functions such as line coding, clock recovery, etc. The NTC also scrambles the payload data, using one of two polynomials. If no user cells are available, the NTC will generate idle cells to maintain a constant cell-stream on the network. Other cell

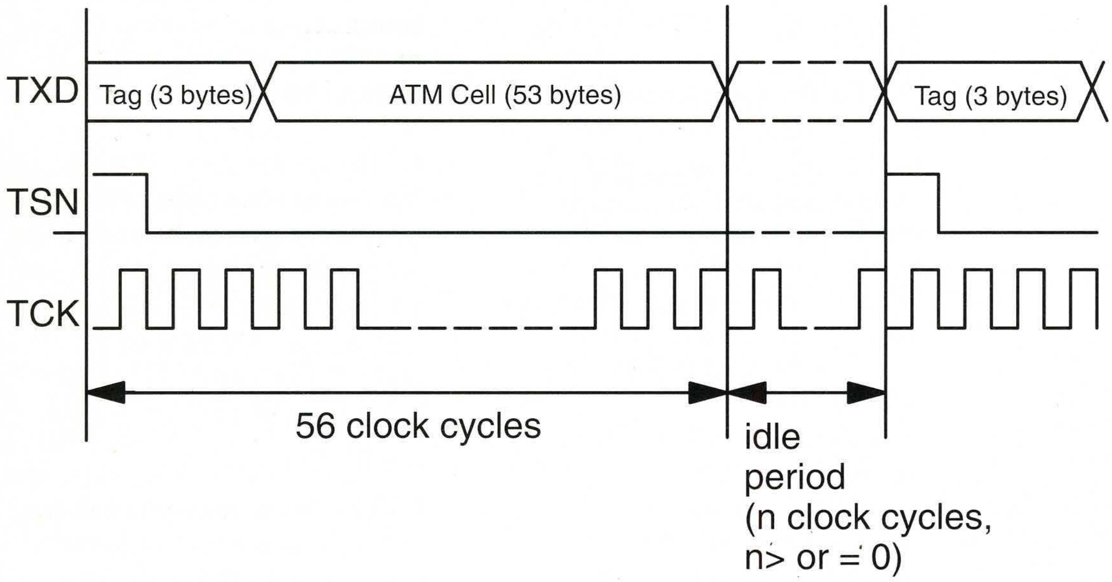
NTC Applications

Figure 8



Asynchronous Cell Stream Format

Figure 9



Note : Tag may be 0, 1, 2 or 3 bytes

types, such as signalling cells, can be inserted into the cell flow using the on-chip DMA controller.

In the receive direction, the NTC synchronizes to the framed data, and to the ATM cells. Statistics information is extracted from the framing bytes, and the payload data unscrambled. The statistics collected are stored on a per virtual circuit basis, either on-chip, or if insufficient space exists, in local memory. The NTC contains a cell buffer which effectively decouples network and system clocks. Cells are temporarily stored here while optional address translation on the VPI/VCI fields of received cell headers is performed by the ATC. The relevant header fields are passed across a local interface an a byte basis. Once the ATC has completed any translation, the new header value is returned to the NTC, appended to the cell information field, and the cell output to the ALC across the asynchronous cell stream interface. This is shown in Fig. 9, and is common to all of Fujitsu's ATM products.

The ATM switch example shows the NTC connected to a switch matrix, which could be based on the SRE. Two ATCs are connected, allowing address translation to be performed in both directions. This might be useful, for example, when a multicast cell is received at the switch output and the address must be translated before transmission. In the receive direction, the NTC and ATC must also add the routing tag information needed by the switch matrix. This is selectable in length, up to 3 bytes, to allow flexibility in the switch configuration, and will be output before the cell header.

MB86686 Adaption Layer Controller (ALC)

Overview
The adaptation layer of the ATM protocol model defines the methods by which user data is packaged into the information fields of a sequence of cells. This includes dividing the data up into 48-byte segments, and adding sufficient overhead to ensure the data can be successfully reassembled at the receiver. These functions broadly correspond to the convergence and segmentation/reassembly sub-layers of the adaptation layer. A number of different adaptation layer procedures exist to support different types, or classes, of traffic, as shown in Fig. 10. These have been defined based on parameters such as the bit rate (constant/variable), the need for synchronization between data source and sink and the connection mode (connection-oriented/connectionless). As an example, voice and video services, which are synchronous, constant bit rate processes, are supported by AAL 1, while data such as X.25, Frame Relay and TCP/IP, which have variable bit rates and no timing relationship required between transmitter and receiver, is handled by AAL 3/4. During the original definition phase, AAL3 and AAL4 were merged into a single protocol, and a further, simplified version, AAL5, has also been added. In the first applications of ATM within the local area, it is this second type of traffic which is likely to be most important.

Operation
The Adaptation Layer Controller (ALC) provides a complete implementation of both AAL3/4 and AAL5 procedures. User data is transferred to and from system memory via an on-chip high-speed DMA controller which can interface to a variety of 32- and 64-bit bus structures. The ALC is a full bi-directional device and can support up to 1K simultaneous connections in both receive and transmit directions at network speeds up to 155Mbps. Other key features include:

- Support for up to 12 peak segmentation rates, with two sub-rate options selectable on a per VC basis
- Leaky-bucket averaging algorithm for each VC
- Programmable peak and average rates for total ALC cell stream output
- Routing tag generation for direct connection to switch
- Supplied in 208-pin plastic quad flat pack

There are many possible system configurations that can be used. Fig. 11 gives just two of the

Classes of Traffic and Associated AAL Layers

Figure 10

	Class A	Class B	Class C	Class D
Timing relation between source and destination	Required		Not required	
Bit rate	Constant		Variable	
Connection mode	Connection oriented			Connectionless
AAL Types	1	2	3/4, 5	3/4

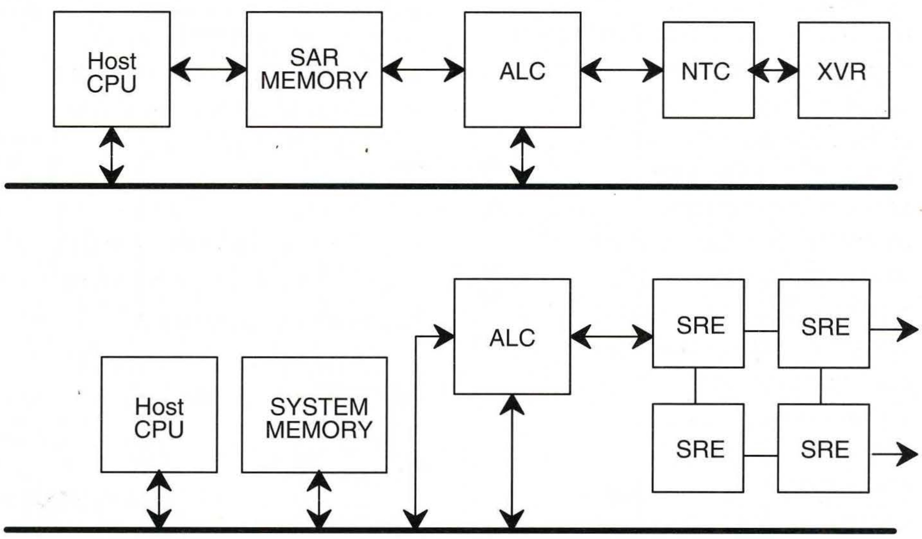
possibilities. In the first, the ALC is used in a high-performance terminal application. On the network side, it connects via the NTC to a physical layer transceiver. On the system side, a dedicated dual-port Segmentation And Reassembly (SAR) RAM is connected to the ALC via a dedicated bus. Packets for segmentation and packets being reassembled are stored in the SAR memory, together with the data structures used to communicate between ALC and the host CPU. Control of the ALC is exercised via a separate 16-/32-bit port.

The second application shows the ALC in a switch application. Here the ALC interfaces directly to one port of an SRE. In this case, the application is a lower performance one, and hence the SAR memory can be part of host system memory. The ALC acts as a second bus master, negotiating access to the bus when required. The control port is connected to the same bus. When packets are segmented, the ALC also adds the routing tag information prior to passing the cells into the switch matrix. It can also check the HEC field of cells received from the switch to verify correct reception. Such a situation might be required where existing 'legacy' networks, such as Ethernet, must be connected into an ATM environment.

Communication between host and ALC is handled via a set of shared queues in the SAR memory. This is shown in Fig. 12. Packets are queued for segmentation at one of 12 peak rates by the host writing a pointer to the relevant Transmit Buffer Descriptor onto the Transmit Pending queue. The transmit descriptor defines the location and size of the user data, as well as a pointer to an associated entry in the Circuit Reference Table (CRT). The

ALC System Configurations

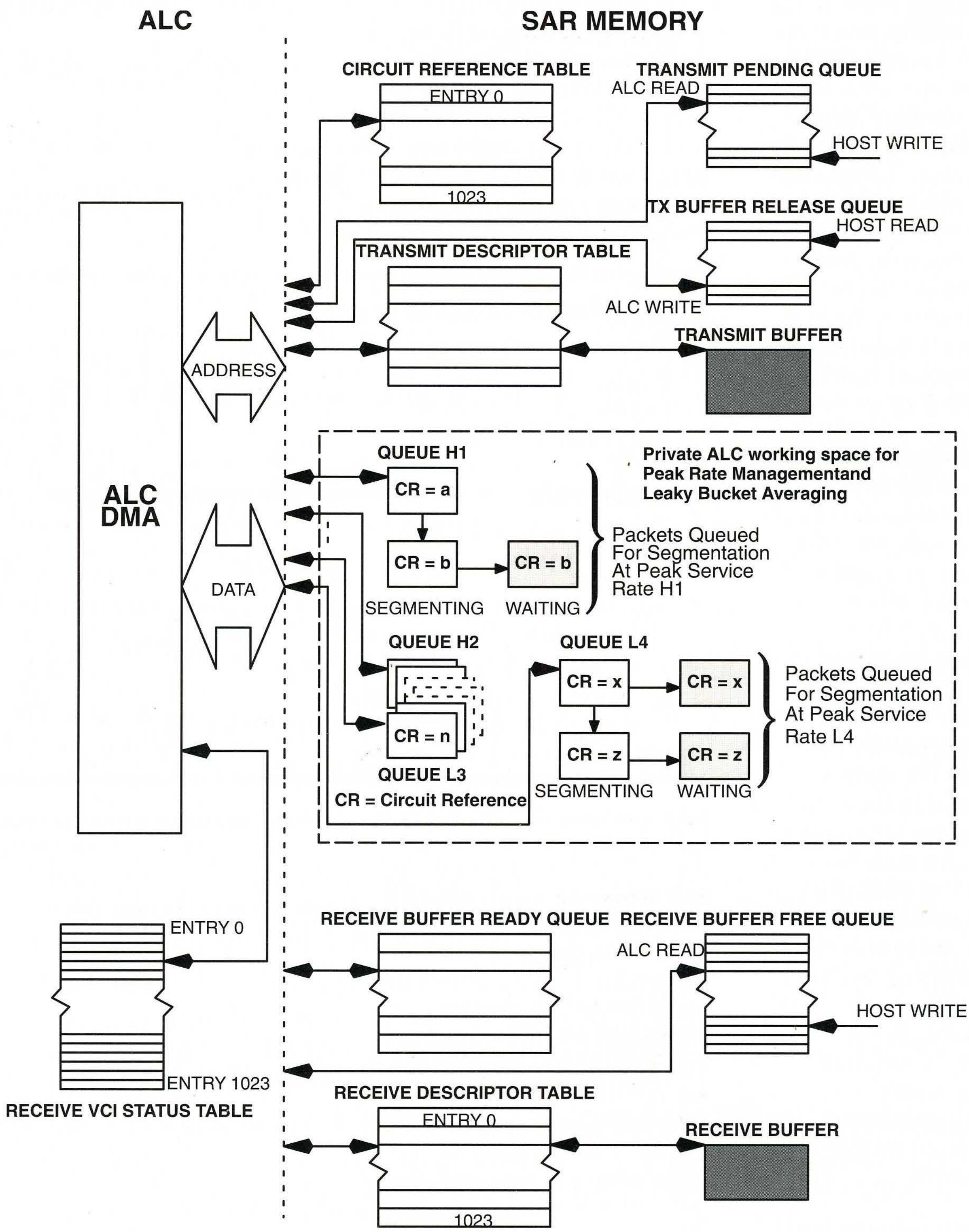
Figure 11



CRT defines the values of the cell header fields, the optional routing tag and the queue and service interval to be used for the packet. It also contains the leaky-bucket parameters associated with the virtual circuit to be used. The queues are serviced at user-defined intervals. Depending on the VC the status of the leaky-bucket algorithm determines whether a cell will be created. This gives the user total control over the traffic patterns generated by the ALC. In addition to the per-VC shaping, the peak and average rates of the total ALC cell steam output can also be defined.

Shared Data Structures

Figure 12



MB86689 Address Translation Controller

Overview

The final part of the ATM protocol is the ATM layer itself, where the functions of the cell header fields are defined. Part of the task of the header is the assignment of cells to a particular connection by means of the virtual path and virtual circuit identifiers. These fields are used by an ATM switch to determine the correct output port for a given cell. Since the VPI/VCI values on this outgoing link may differ from those used on the input to the cell, translation of these values may be necessary. These functions can be implemented using the Address Translation Controller (ATC).

Operation

This ATC performs real-time translation of ATM header information for serial rates up to 155Mbps. It also can supply a routing tag up to 3 bytes long that is used by the ATM switch fabric to determine the correct destination for each cell. Other features include:

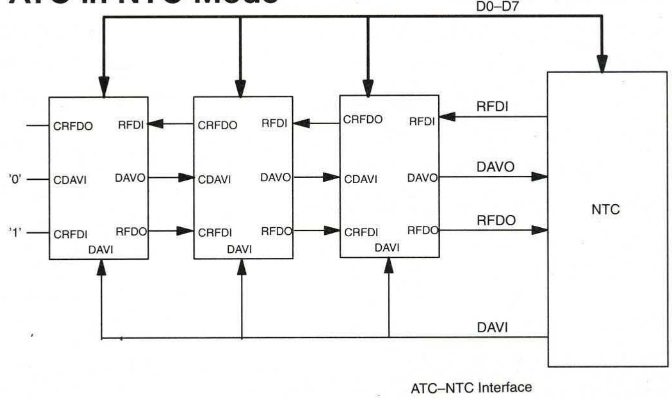
- 1024-entry CAM
- Full 28-bit comparison for each entry, with optional bit-masking
- Supports multiple matches for multicast operation
- Supports CLP and congestion indication/removal for each entry
- Multiple ATCs can be cascaded to support larger addressing range
- Supplied in 80-pin plastic quad flat pack

Normally the ATC interfaces to the NTC as shown in Fig. 13. This also shows how more than one ATC can be cascaded, if necessary. Transfer of cell header bytes between the two devices is co-ordinated by a simple hand-shaking procedures. Once the search process is complete, the ATC transfers the new header values, plus the optional routing tag bytes, back to the NTC. This will always be achieved within one cell interval.

In certain cases, for example when interfacing to an ATM backplane, the NTC functions may be unnecessary. In this case, the ATC can simply be connected as shown in Fig. 14. In this case, the ATC interfaces directly to the cell stream using the same type of parallel interface as the other Fujitsu devices. The cell header will be translated as the bytes are received, the user information being passed unmodified. In an application such as this, the ATC can be used to map any range of VPI/VCI values onto an appropriate range for the ALC which requires con-tiguous values.

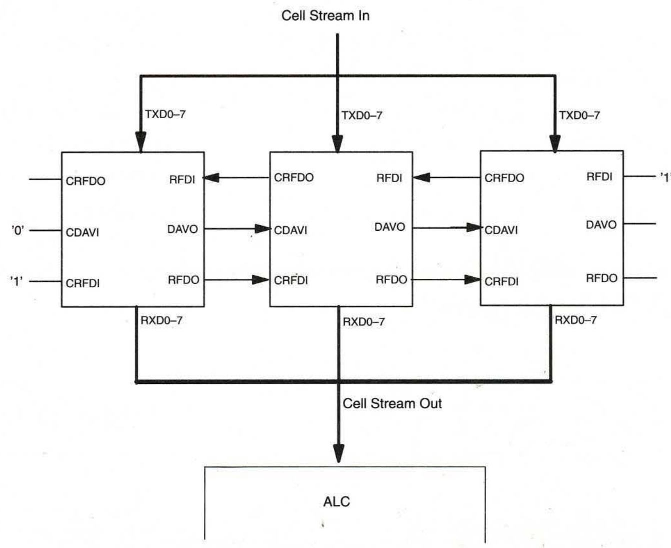
ATC in NTC Mode

Figure 13



ATC Cell Stream Mode

Figure 14

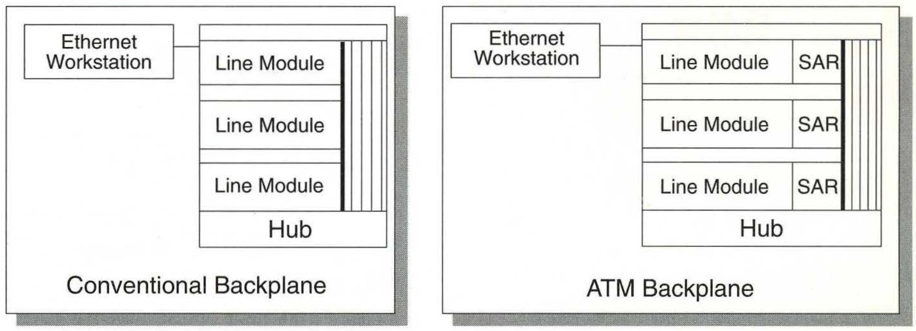


ATM Applications

Where will ATM first appear, and how do Fujitsu's products map onto these applications? Although the exact development path for ATM is the subject for debate, products from several vendors have already been announced and, in some cases, are already in use. The first applications will be in the local area for ATM backplanes, backbone networks and ATM LANs.

The backplane
The concept of the ATM backplane is shown in Fig. 15. Most present LAN hubs use the LAN technology itself to connect segments internally and hence are encountering the same performance problems. By upgrading the backplane structure to use ATM as a technology, these bandwidth limitations can be overcome.

Conventional and ATM Backplanes Figure 15

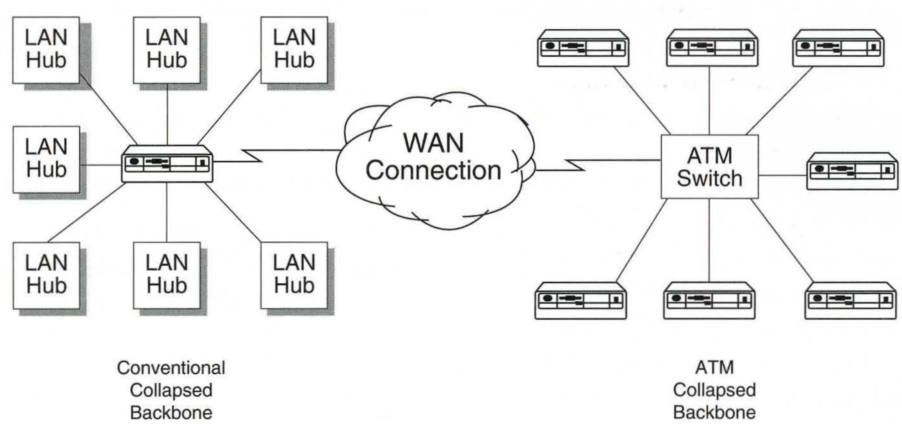


The existing LAN interface cards must be modified to generate and terminate ATM cells at the backplane interface. This function can be performed by the Fujitsu Adaptation Layer Controller (ALC). Since all ATM traffic remains internal, many manufacturers have adopted this approach short-term until addressing and signalling standards are finalized.

The backbone
In backbone networks, ATM offers an attractive alternative to FDDI, the technology originally developed for this application. FDDI is a shared-media technique, with the associated disadvantages. It also has no specific support for constant bit rate data such as voice and video, and is limited to a maximum speed of 100Mbps. Besides its capacity to handle all data types, an ATM-based replacement could immediately offer speeds of 155Mbps, with the prospect of much higher bit rates if required in the future.

In more local environments, the concept of a 'collapsed' backbone may be advantageous. This approach, where the backbone connection is contained within a single piece of equipment, is currently offered in certain router products. The main limitation here is the number of sub-nets that can be supported, due to physical constraints within the router itself. To overcome this in the future, this backbone could be implemented by an ATM switch. Local connectivity would be provided via hubs, fitted with ATM interfaces. This scenario is shown in Fig. 16.

ATM Backbone Figure 16



The desktop

A further LAN application will be the delivery of ATM to the desktop. This would enable the creation of workgroups of ATM users to run specific high-performance or multimedia type applications. This would be provided by an ATM local switch, or hub, plus an ATM adapter card in the workstation, to deliver a dedicated 155Mbps per user.

ATM-LAN

Figure 17

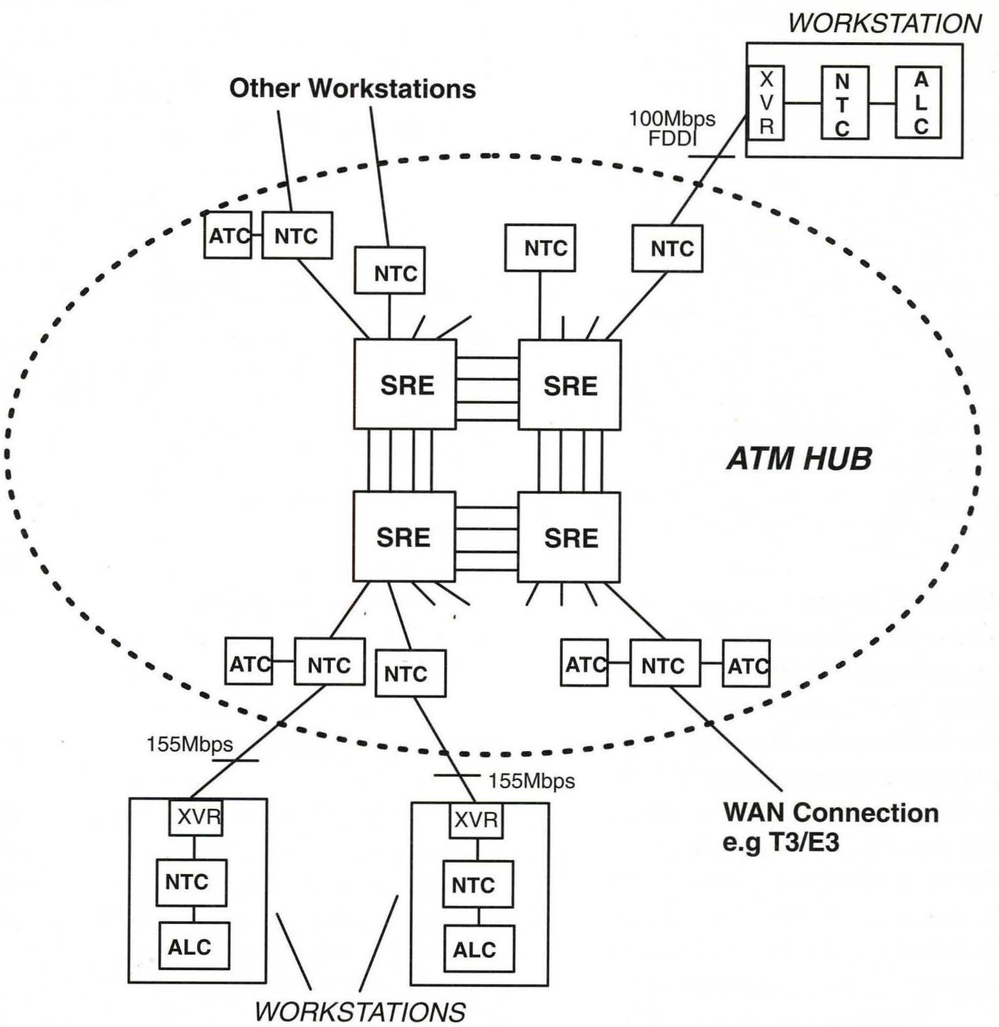


Fig. 17 shows how the Fujitsu products map onto this application. At the workstation, ATM connectivity is achieved by combining the ALC, which creates the ATM cells from user data and the NTC, which maps these cells onto the chosen physical link, for example a SONET based 155Mbps connection over fiber. The only additional component would be the 'media dependent' transceiver.

At the hub, ATM cells are extracted from incoming frames by the NTC. This device, together with the ATC, performs any required VPI/VCI translation before the cell is passed to the ATM switch. The ATC also appends a user-configurable routing tag which can be used by the switching array to select the correct destination output. The SRE could form the basis of such an array, being ideally suited to application in compact switching matrices. The switching elements process the routing tag to identify the correct output port. A further ATC at the output port can re-generate the VPI/VCI field before the cell is transmitted.

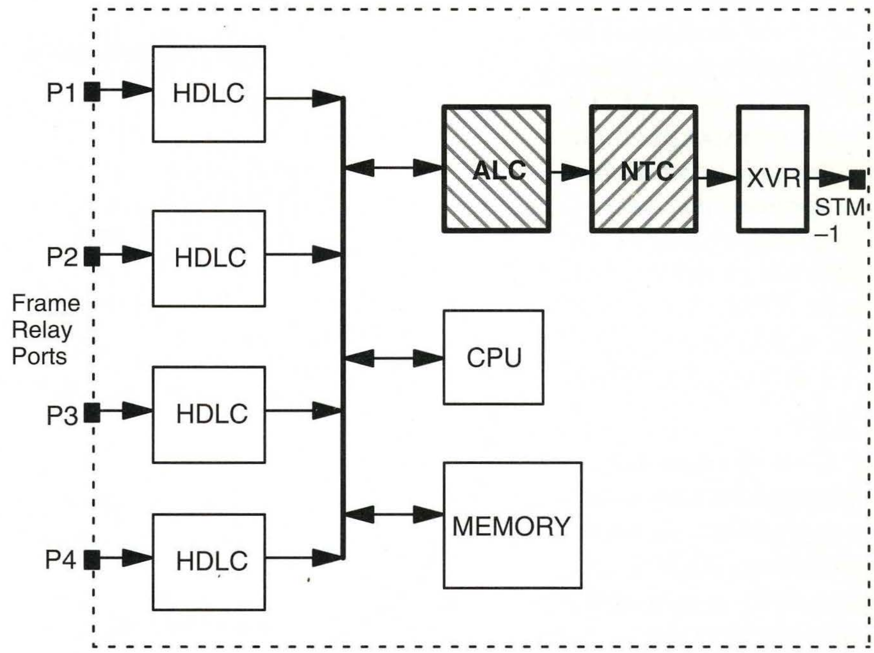
WAN applications

What about ATM in the wide area? The increase in LANs has led to a corresponding need for interconnection. This has largely been addressed by Frame Relay services, but these are relatively low speed. The use of ATM as a high-speed transport mechanism for Frame Relay data seems the most likely initial application for ATM in the wide-area, given that any public service offering is at least two years away.
A representation of a Frame Relay-ATM Interworking Unit is shown in Fig. 18. Several high-speed leased lines at T1 or T3 rates, are terminated at the HDLC framing level. User data packets are stored in local memory. These packets are then processed into ATM cells by the ALC, and transmitted onto a higher-speed 155Mbps ATM link after framing functions have been handled by the NTC. The same devices handle reception of cells from the ATM network and transfer of user data to memory.

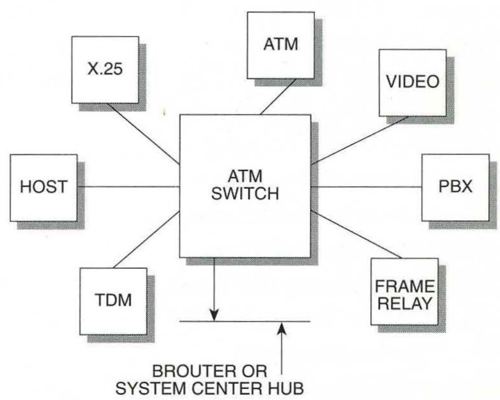
A further attractive feature of ATM is its ability to enable efficient use of bandwidth shared between multiple users, and hence utilize costly leased-line connections more effectively. Access to the WAN is likely to be via some kind of ATM Multiplexer as shown in Fig. 19. This acts as a concentrator for all the users' existing networks, e.g, X.25, Frame Relay, PABX, LAN, Video, etc. The multiplexer could be based on an ATM switch matrix, with a selection of service cards (interfaces to user networks), and line cards to provide WAN connection via various interfaces such as SONET or DS3.

Regardless of the eventual ATM migration path, Fujitsu has products appropriate for any potential application.

ATM-Frame Relay Interworking Figure 18



ATM-Multiplexer Figure 19



Summary

ATM's ability to offer immediate performance improvements, while ensuring a growth path for the future, is combined with unique capabilities for the support of new applications and services. This makes it the logical choice for the communications networks of the future. For the first time, a common protocol exists for both public and private networks, enabling simplified operation and management. The activities of the ATM Forum will be vital to encourage the widespread availability of compatible equipment and attractive services. However, ATM will only be successful if it is price competitive. The availability of the right silicon is vital to ensure this.

Fujitsu's initial product range covers all the major functional areas defined by the ATM protocol, and delivers the most complete solution yet seen for customer premises applications. Designed to conform to all current ATM standards, the devices lead the way both in performance and price, and are supported by the resources of one of the world's leading semiconductor companies.

The four devices do, however, only represent the first step in a long-term commitment to ATM. New applications areas will emerge with their own specific requirements. One example is the workstation connectivity market, vital to the rate of growth of the overall ATM market. This application will call for specialized silicon, to enable the necessary cost goals to be achieved. Fujitsu therefore plans to introduce a new, single-chip ATM access controller within the first half of 1994, targeted at workstation adapter cards and motherboards. This will include segmentation, reassembly and framing functions, and will maintain Fujitsu's price/performance leadership.

Fujitsu will continue to use its worldwide resources to introduce new, leading-edge products as ATM standards, and the market itself, develop.

Headquarters

Asia

Fujitsu Microelectronics Asia PTE Ltd.
No. 51 Bras Basah Road
Plaza by the Park
06-04/07 Singapore 0718
Tel: 65-336-1600
Telex: 55573
Fax: 65-3361609

Europe

Fujitsu Mikroelektronik GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchschlag
Germany
Tel.: 06103-690-0
Telex: 411963
Fax: 06103-690-122

Japan

Fujitsu Limited
Semiconductor Marketing
Furukawa Sogo Bldg.
6-1 Marunouchi, 2-chome
Chiyoda-ku, Tokyo 100, Japan
Tel: 03-3216-3211
Telex: 781-2224361
Fax: 03-3216-9771

U.S.A.

Fujitsu Microelectronics Inc.
3545 North First Street
San Jose CA 95134-1804
Tel: 408-922-9000
Telex: 910-671-4915
Fax: 408-432-9044

Sales Offices - Worldwide

Asia

HONG KONG
Fujitsu Microelectronics Pacific Asia, Ltd.
Rooms 616-617, Tower B,
New Mandarin Plaza
14 Science Museum Rd.
Tsimshatsui East, Kowloon
Tel: 852-723-0393
Fax: 852-721-6555

SINGAPORE
Fujitsu Microelectronics Asia PTE Ltd.
No. 51 Bras Basah Road
Plaza by the Park
06-04/07 Singapore 0718
Tel: 65-336-1600
Telex: 55573
Fax: 65-3361609

TAIWAN
Fujitsu Microelectronics Pacific Asia, Ltd.
Rm. 1906, Taipei World Center, 333,
Keelung Road, Section 1
Taipei 10548
Tel: 886-2-757-6548
Fax: 886-2-757-6571

Europe

FRANCE
Fujitsu Mikroelektronik GmbH
Immeuble le Trident 3-5
Voie Felix Eboue F-94024
Creteil, Cedex
Tel: 01-451312-12
Fax: 01-451312-13

GERMANY
Fujitsu Mikroelektronik GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchschlag
Tel: 06103-690-0
Fax: 06103-690-122

Fujitsu Mikroelektronik GmbH
Carl-Zeiss-Ring 11
85737 Ismaning/Munich
Tel: 0 89-960944-0
Fax: 0 89-960944-22

Fujitsu Mikroelektronik GmbH
Am Joachimsberg 10-12
71083 Herrenberg
Tel: 07032-4085
Fax: 07032-4088

ITALY
Fujitsu Microelectronics Italia SRL
Centro Direzionale, Milanofiori
Strada No. 4-Palazzo A 2
I-20094 Assago (Milano)
Tel: 02-8246-170
Fax: 02-8246-189

SWEDEN
Fujitsu Microelectronics, Ltd.
Kung Hans Väg 12
S-191 76 Sollentuna, Sweden
Tel: 08-6266720
Fax: 08-6266711

UNITED KINGDOM
Fujitsu Microelectronics, Ltd.
Hargrave House, Belmont Road,
Maidenhead Berkshire, SL6 6NE
Tel: 0628-76100
Fax: 0628-781484

USA

CALIFORNIA
Fujitsu Microelectronics, Inc.
2880 Lakeside Drive, Suite 250
Santa Clara, CA 95054
Tel: 408-982-1800

Fujitsu Microelectronics, Inc.
Century Center, 2603 Main Street, #510
Irvine, CA 92714
Tel: 714-724-8777
Fax: 714-724-8778

COLORADO
Fujitsu Microelectronics, Inc.
5445 DTC Parkway, P4
Englewood, CO 80111
Tel: 303-740-8880
Fax: 303-740-8988

GEORGIA
Fujitsu Microelectronics, Inc.
3500 Parkway Lane, #210,
Norcross, GA 30092
Tel: 404-449-8539
Fax: 404-441-2016

ILLINOIS
Fujitsu Microelectronics, Inc.
One Pierce Place, #1130
Itasca, IL 60143-2681
Tel: 708-250-8580
Fax: 708-250-8591

MASSACHUSETTS
Fujitsu Microelectronics, Inc.
1000 Winter Street, #2500,
Waltham, MA 02154
Tel: 617-487-0029
Fax: 617-890-9002

MINNESOTA
Fujitsu Microelectronics, Inc.
3460 Washington Drive, #209
Eagan, MN 55122-1303
Tel: 612-454-0323
Fax: 612-454-0601

NEW YORK
Fujitsu Microelectronics, Inc.
898 Veterans Memorial Highway
Building 2, Suite 310
Hauppauge, NY 11788
Tel: 516-582-8700
Fax: 516-582-3855

OREGON
Fujitsu Microelectronics, Inc.
15220 NW Greenbrier Parkway, # 360
Beaverton, OR 97006
Tel: 503-690-1909
Fax: 503-690-8074

TEXAS
Fujitsu Microelectronics, Inc.
14785 Preston Rd., #274
Dallas, TX 75240
Tel: 214-233-9394
Fax: 214-386-7917

Fujitsu Microelectronics, Inc.
20515 SH 249, Suite 485
Houston, TX 77070
Tel: 713-379-1061

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