1993

GoldStar

MOS MEMORY

DATA BOOK

- DRAM
- DRAM MODULE
- VIDEO RAM
- SRAM
- MASK ROM

GoldStar
GOLDSTAR ELECTRON CO., LTD.

GoldStar

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DATA BOOK

- DRAM
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GoldStar Electron

DATA BOOK & MANUAL LIST

1) PRODUCT GUIDE
2) MEMORY DATA BOOK
3) TTL DATA BOOK
4) HIGH SPEED CMOS LOGIC DATA BOOK
5) MOS LOGIC GD4000 SERIES DATA BOOK
6) Z80 FAMILY DATA BOOK
7) GENERAL PURPOSE IC DATA BOOK
8) CONSUMER IC DATA BOOK
9) MICRO-PERIPHERAL IC DATA BOOK
10) TELECOM IC DATA BOOK
11) 1.2μm CMOS STANDARD CELL DATA BOOK
    — MACROCELL MANUAL
12) 1.2μm CMOS GATE ARRAY DATA BOOK
    — MACROCELL MANUAL
13) GMCS400 SERIES USER'S MANUAL
14) Q.A.MANUAL

■ Product Status

DEFINITIONS

Data Sheet Indentification	Product Status	Definition
Objective Specification	**Formative or In Design**	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data and supplementary data will be published at a later date. GoldStar Electron Co., Ltd. reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. GoldStar Electron Co., Ltd. reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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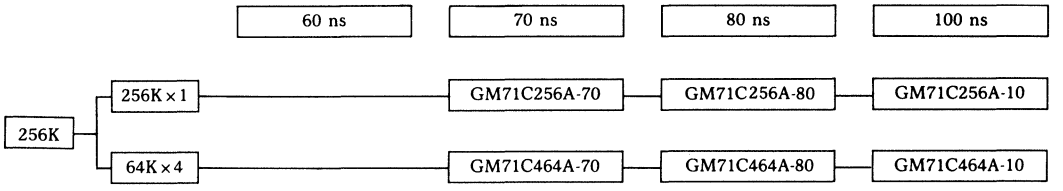
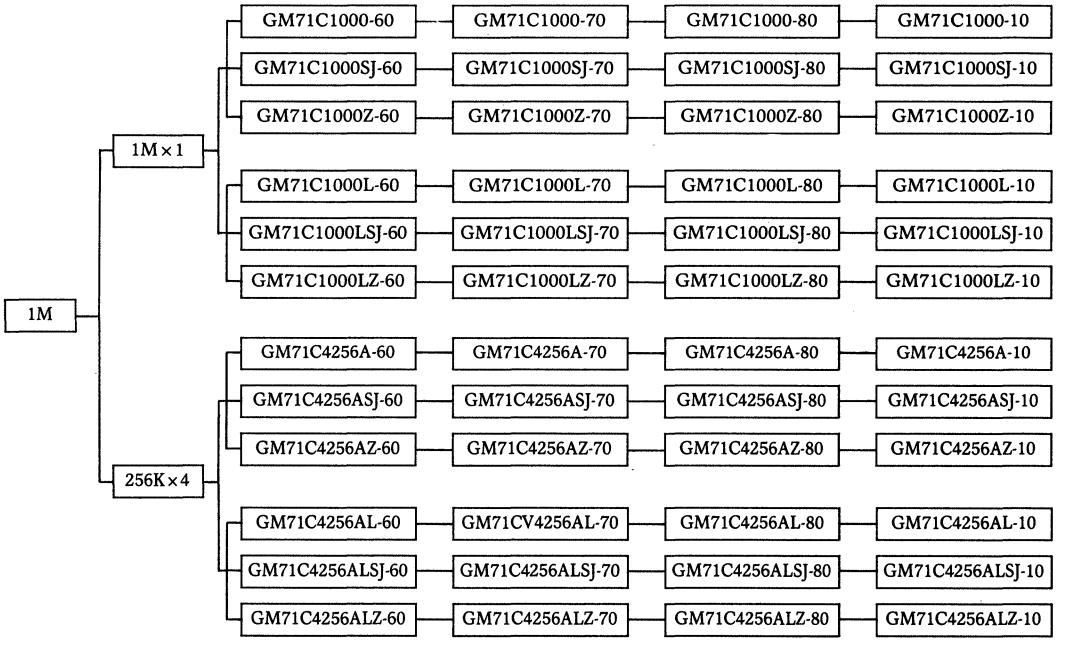
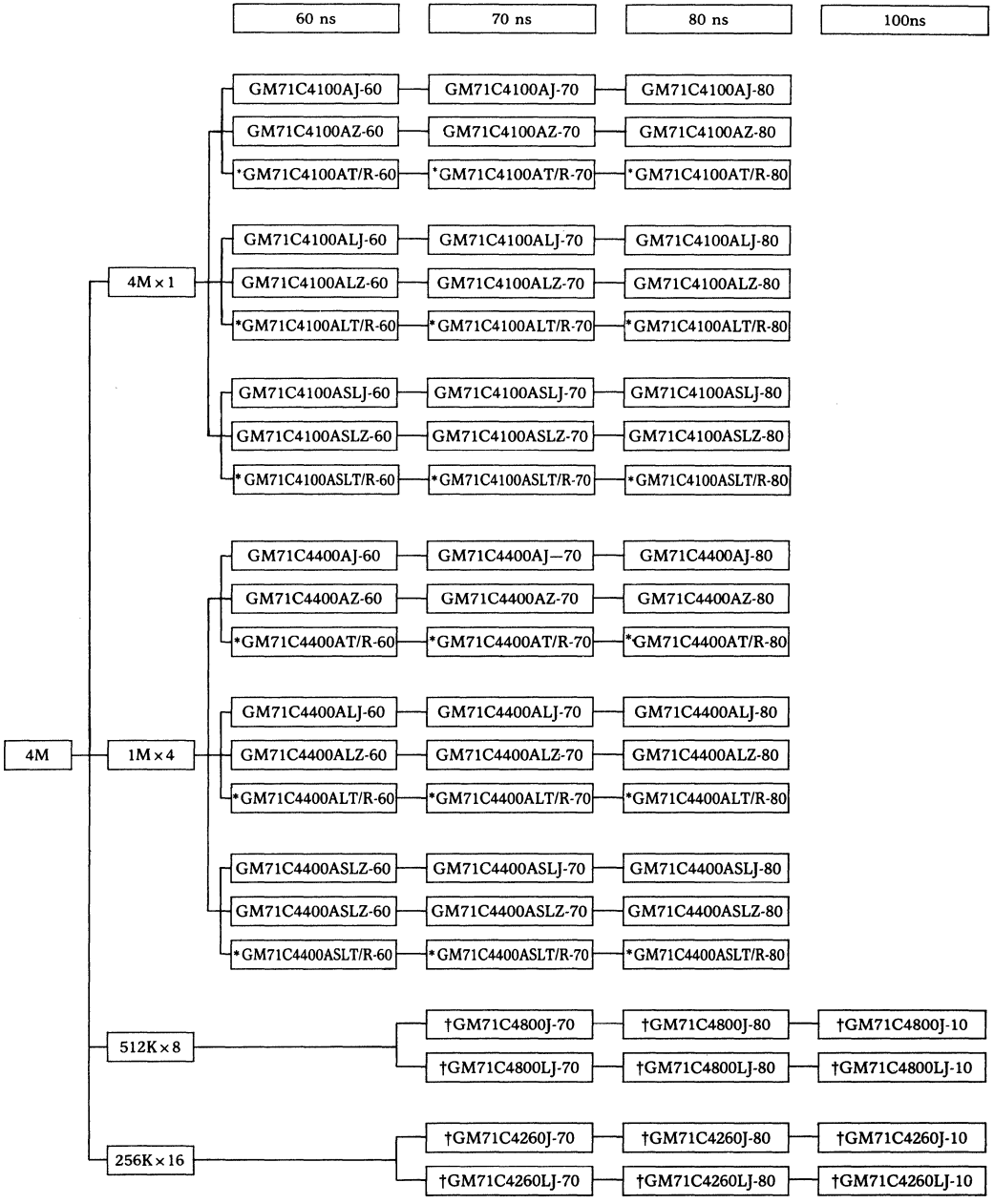
1. DRAM


60 ns
70 ns
80 ns
100 ns
256K
256K x 1
GM71C256A-70
GM71C256A-80
GM71C256A-10
64K x 4
GM71C464A-70
GM71C464A-80
GM71C464A-10


1M
1M x 1
GM71C1000-60
GM71C1000-70
GM71C1000-80
GM71C1000-10
GM71C1000SJ-60
GM71C1000SJ-70
GM71C1000SJ-80
GM71C1000SJ-10
GM71C1000Z-60
GM71C1000Z-70
GM71C1000Z-80
GM71C1000Z-10
GM71C1000L-60
GM71C1000L-70
GM71C1000L-80
GM71C1000L-10
GM71C1000LSJ-60
GM71C1000LSJ-70
GM71C1000LSJ-80
GM71C1000LSJ-10
GM71C1000LZ-60
GM71C1000LZ-70
GM71C1000LZ-80
GM71C1000LZ-10
256K x 4
GM71C4256A-60
GM71C4256A-70
GM71C4256A-80
GM71C4256A-10
GM71C4256ASJ-60
GM71C4256ASJ-70
GM71C4256ASJ-80
GM71C4256ASJ-10
GM71C4256AZ-60
GM71C4256AZ-70
GM71C4256AZ-80
GM71C4256AZ-10
GM71C4256AL-60
GM71CV4256AL-70
GM71C4256AL-80
GM71C4256AL-10
GM71C4256ALSJ-60
GM71C4256ALSJ-70
GM71C4256ALSJ-80
GM71C4256ALSJ-10
GM71C4256ALZ-60
GM71C4256ALZ-70
GM71C4256ALZ-80
GM71C4256ALZ-10

DRAM (Continued)



Note *: Coming Soon †: Under Development

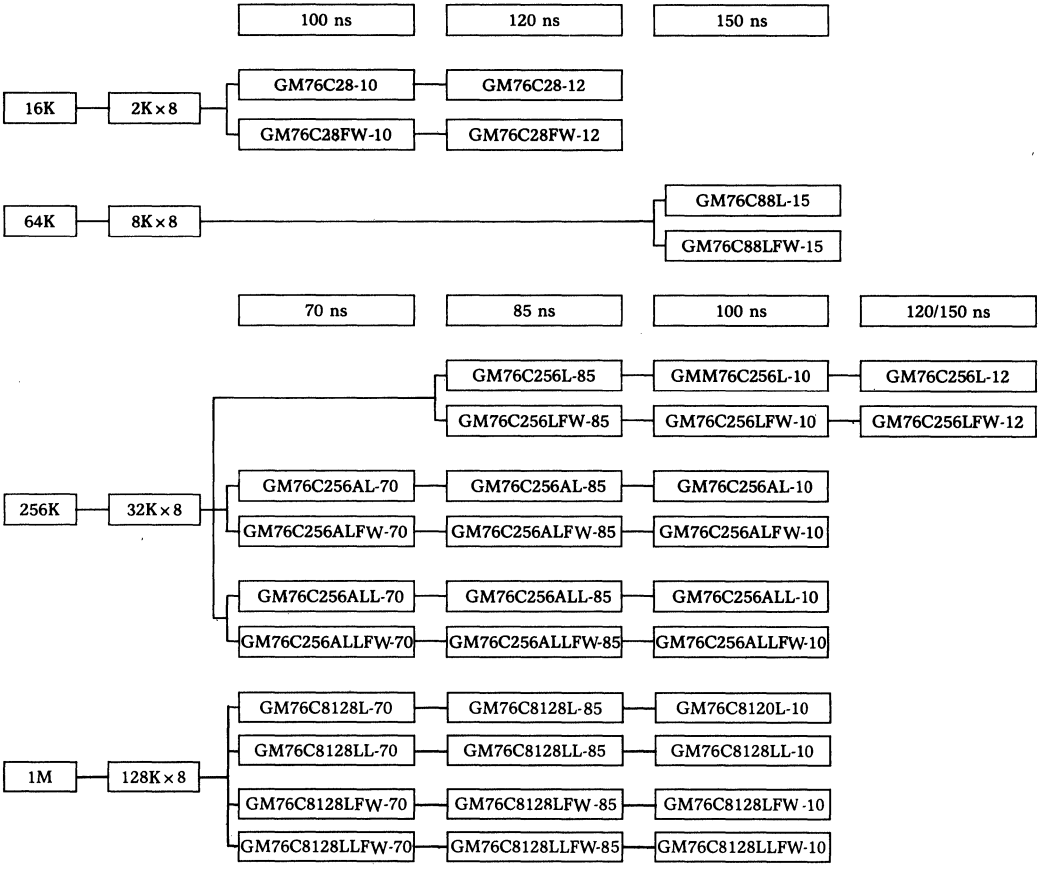
2. DRAM MODULE

	60 ns	70 ns	80 ns	100 ns	
256K×8		GMM78256S-70	GMM78256S-80	GMM78256S-10	
256K×9		GMM79256NS-70	GMM79256NS-80	GMM79256NS-10	
1M×8	GMM781000S-60	GMM781000S-70	GMM781000S-80		
	GMM781000NS-60	GMM781000NS-70	GMM781000NS-80		
1M×9	GMM791000S-60	GMM791000S-70	GMM791000S-80		
	GMM791000NS-60	GMM791000NS-70	GMM791000NS-80		
4M×8	GMM784000S-60	GMM784000S-70	GMM784000S-80		
4M×9	GMM794000S-60	GMM794000S-70	GMM794000S-80		
1M×32	GMM7321000SG-60	GMM7321000SG-70	GMM7321000SG-80		
1M×36	GMM7361000SG-60	GMM7361000SG-70	GMM7361000SG-80		(Both Side)
	GMM7361000SGS-60	GMM7361000SGS-70	GMM7361000SGS-80		(Single Side)
2M×32	GMM7322000SG-60	GMM7322000SG-70	GMM7322000SG-80		
2M×36	GMM7362000SG-60	GMM7362000SG-70	GMM7362000SG-80		
1M×40	GMM7401000SG-60	GMM7401000SG-70	GMM7401000SG-80		(Single Side)
2M×40	GMM7402000SG-60	GMM7402000SG-70	GMM7402000SG-80		(Both Side)

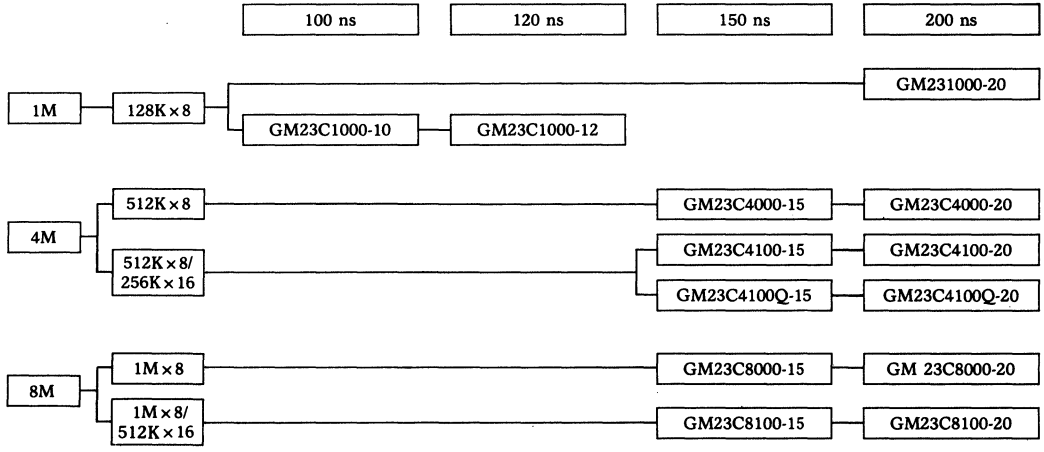
3. MULTIPORT VIDEO RAM

		80 ns	100 ns	120 ns
256K	64K×4	GM53C261Z-80	GM53C261Z-10	GM53C261Z-12

4. SRAM



5. MASK ROM



Note †: Under development

RAMS

Process	Org.	Type No.	Max Access Time(ns)	Current(mA)		Feature	Package (Mil)	Available
				Active	S/B			

DYNAMIC RAM

CMOS	256K×1	GM71C256A - 70	70	70	3	FAST	16 DIP	NOW
		- 80	80	60		PAGE		
		- 10	100	50		MODE		
	64K×4	GM71C464A - 70	70	80	3	FAST	18 DIP	NOW
		- 80	80	70		PAGE		
		- 10	100	65		MODE		
	1M×1	GM71C1000 - 60	60	90	1	FAST	18 DIP	NOW
		- 70	70	80		PAGE	20 SOJ	"
		- 80	80	70		MODE	20 ZIP	"
		- 10	100	60				
		GM71C1000L - 60	60	90	0.2	FAST	18 DIP	NOW
		- 70	70	80		PAGE	20 SOJ	"
		- 80	80	70		MODE/	20 ZIP	"
		- 10	100	60		L-POWER		
	256K×4	GM71C4256A - 60	60	90	1	FAST	20 DIP	NOW
		- 70	70	80		PAGE	20 SOJ	"
		- 80	80	70		MODE	20 ZIP	"
		- 10	100	60				
		GM71C4256AL - 60	60	90	0.2	FAST	20 DIP	NOW
		- 70	70	80		PAGE	20 SOJ	"
		- 80	80	70		MODE/	20 ZIP	"
		- 10	100	60		L-POWER		
	4M×1	GM71C4100A - 60	60	110	1	FAST	20 SOJ	NOW
		- 70	70	100		PAGE	(300)	
		- 80	80	90		MODE	20 ZIP	"
							20 TSOP	1Q/'93
		GM71C4100AL - 60	60	110	0.2	FAST	20 SOJ	NOW
		- 70	70	100		PAGE	(300)	
		- 80	80	90		MODE/	20 ZIP	"
						L-POWER	20 TSOP	1Q/'93
		GM71C4100ASL - 60	60	110	0.1	FAST	20 SOJ	NOW
		- 70	70	100		PAGE	(300)	
		- 80	80	90		MODE/	20 ZIP	"
						SL-POWER	20 TSOP	1Q/'93
	1M×4	GM71C4400A - 60	60	110	1	FAST	20 SOJ	NOW
		- 70	70	100		PAGE	(300)	
		- 80	80	90		MODE	20 ZIP	"
							20 TSOP	1Q/'93
		GM71C4400AL - 60	60	110	0.2	FAST	20 SOJ	NOW
		- 70	70	100		PAGE	(300)	
		- 80	80	90		MODE/	20 ZIP	"
						L-POWER	20 TSOP	1Q/'93
		GM71C4400ASL - 60	60	110	0.1	FAST	20 SOJ	NOW
		- 70	70	100		PAGE	(300)	
		- 80	80	90		MODE/	20 ZIP	"
						SL-POWER	20 TSOP	1Q/'93

RAMS

Process	Org.	Type No.	Max Access Time(ns)	Current(mA)		Feature	Package (Mil)	Available
				Active	S/B			

DYNAMIC RAM (Continued)

CMOS	512K×8	GM71C4800 - 70	70	110	1	FAST PAGE MODE	28 SOJ (400) 28 TSOP	3Q/'93
		- 80	80	100				
		- 10	100	90				
		GM71C4800L - 70	70	110	0.2	FAST PAGE/ L-POWER	28 SOJ (400) 28 TSOP	3Q/'93
		- 80	80	100				
		- 10	100	90				
	256K×16	GM71C4260 - 70	70	170	1	FAST PAGE MODE	40 SOJ (400) 40 TSOP	3Q/'93
		- 80	80	150				
		- 10	100	130				
		GM71C4260L - 70	70	170	0.2	FAST PAGE/ L-POWER	40 SOJ (400) 40 TSOP	3Q/'93
		- 80	80	150				
		- 10	100	130				

RAMS

DRAM MODULE

Process	Org.	Type No.	Max Access Time(ns)	Current(mA) Active	Current(mA) S/B	Feature	Package (Mil)	Available
CMOS	256K×8	GMM78256S - 60	60	180		FAST PAGE MODE	30 PIN SOCKET	NOW
		- 70	70	160				
		- 80	80	140				
	256K×9	GMM79256NS - 70	70	245		FAST PAGE MODE	30 PIN SOCKET	NOW
		- 80	80	200	5			
		- 10	100	170				
	1M×8	GMM781000S - 60	60	720		FAST PAGE MODE	30 PIN SOCKET	NOW
		- 70	70	640	8			
		- 80	80	560				
		GMM781000NS - 60	60	220		FAST PAGE MODE	30 PIN SOCKET (2 CHIP)	NOW
		- 70	70	200	2			
		- 80	80	180				
	1M×9	GMM791000S - 60	60	810		FAST PAGE MODE	30 PIN SOCKET	NOW
		- 70	70	720	9			
		- 80	80	630				
		GMM791000NS - 60	60	310		FAST PAGE MODE	30 PIN SOCKET (3 CHIP)	NOW
		- 70	70	280	3			
		- 80	80	250				
	4M×8	GMM784000S - 60	60	880		FAST PAGE MODE	30 PIN SOCKET	NOW
		- 70	70	800	8			
		- 80	80	720				
	4M×9	GMM794000S - 60	60	990		FAST PAGE MODE	30 PIN SOCKET	NOW
		- 70	70	900	9			
		- 80	80	810				
	1M×32	GMM7321000SG - 60	60	880		FAST PAGE MODE	72 PIN SOCKET	NOW
		- 70	70	800	8			
		- 80	80	720				
	1M×36	GMM7361000SG - 60	60	1240		FAST PAGE MODE	72 PIN SOCKET	NOW H=25.4mm
		- 70	70	1120	12			
		- 80	80	1000				
		GMM7361000SGS- 60	60	1240		FAST PAGE MODE	72 PIN SOCKET	NOW H=31.75mm
		- 70	70	1120	12			
		- 80	80	1000				
	2M×32	GMM7322000SG - 60	60	896		FAST PAGE MODE	72 PIN SOCKET	NOW
		- 70	70	816	16			
		- 80	80	736				
	2M×36	GMM7362000SG - 60	60	1264		FAST PAGE MODE	72 PIN SOCKET	NOW
		- 70	70	1144	24			
		- 80	80	1024				
	1M×40	GMM7401000SG - 60	60	1100		FAST PAGE MODE	72 PIN SOCKET	NOW
		- 70	70	1000	10			
		- 80	80	900				
	2M×40	GMM7402000SG - 60	60	1120		FAST PAGE MODE	72 PIN SOCKET	NOW
		- 70	70	1020	20			
		- 80	80	920				

RAMS

MULTIPORT VIDEO RAM

Process	Org.	Type No.	Max Access Time(ns)	Current(mA) Active	Current(mA) S/B	Feature	Package (Mil)	Available
CMOS	64K×4	GM53C261 - 80	80	70	6	FAST PAGE MODE	24 ZIP (400)	NOW
		- 10	100	60				
		- 12	120	50				

STATIC RAM

CMOS	2K×8	GM76C28AL - 10	100	60	0.05		24DIP/SOP (600/330)	NOW
		- 12	120	50				
	8K×8	GM76C88AL - 15	150	40	0.1	L-Power	28DIP/SOP (600/330)	NOW
	32K×8	GM76C256 - 85	85	70	1		28DIP/SOP (600/330)	NOW
		- 10	100					
		- 12	120					
		GM76C256L - 85	85	70	0.1	L-Power	28DIP/SOP (600/330)	NOW
		- 10	100					
		- 12	120					
		GM76C256AL - 70	70	70	0.1	L-Power ADVANCED VERSION	28DIP/SOP (600/330)	NOW
		- 85	85					
		- 10	100					
		GM76C256ALL - 70	70	70	0.02	LL-Power ADVANCED VERSION	28DIP/SOP (600/330)	NOW
		- 85	85					
		- 10	100					
	128K×8	GM76C8128L - 70	70	70	0.1	L-Power	32DIP/SOP (600/525)	NOW
		- 85	85					
		- 10	100					
		GM76C8128LL - 70	70	70	0.05	LL-Power	32DIP/SOP (600/525)	NOW
		- 85	85					
		- 10	100					

ROM

MASK ROM

Process	Org.	Type No.	Max Access Time(ns)	Current(mA) Active	Current(mA) S/B	Feature	Package (Mil)	Available
NMOS	128K×8	GM231000 - 20	200	100	20		28 DIP	NOW
CMOS		GM23C1000 - 10	100	40	0.03		28 DIP	NOW
		- 12	120					
	512K×8	GM23C4000 - 15	150	60	1.15		32 DIP 32 SOP	NOW
		- 20	200					
		- 25	250					
	512K×8/ 256K×16	GM23C4100 - 15	150	60	1.5	byte-word switchable	40 DIP 44 QFP	NOW
		- 20	200					
		- 25	250					
	1M×8	GM23C8000 - 15	150	50	0.03		32 DIP	4Q/'92
		- 20	200					
	1M×8/ 512K×16	GM23C8100 - 15	150	50	0.03	byte-word switchable	42 DIP	3Q/'92
		- 20	200					

DYNAMIC RAM

GoldStar	Hitachi	Toshiba	NEC	Fujitsu	Mitsubishi	TI
GM71C256A	HM51256	TC51256	uPD41256	MB81256	M5M4256A	TMS4256
GM71C464A	HM51464	–	μPD41464	MB81464	M5M4464A	TMS4464
GM71C1000	HM511000A	TC511000	μPD421000	MB81C1000A	M5M41000B	TMX4C1024
GM71C1000L	HM511000AL	TC511000L	–	MB81C1000AL	–	–
GM71C4256A	HM514256A	TC514256	μPD424256	MB81C4256A	M5M44C256B	TMS44C256
GM71C4256AL	HM514256AL	–	–	MB81C4256AL	–	–
GM71C4100A	HM514100A	TC514100A	μPD424100	MB814100	M5M44100A	–
GM71C4100AL	HM514100AL	TC514100AL	–	–	M5M44100A-L	–
GM71C4100ASL	HM514100ASL	–	–	–	–	–
GM71C4400A	HM514400A	TC514400A	μPD424400	MB814400	M5M44400A	–
GM71C4400AL	HM514400AL	TC514400AL	–	–	M5M44400A-L	–
GM71C4400ASL	HM514400ASL	–	–	–	–	–
GM71C4800	HM514800	TC514800A	μPD424800	MB814800	M5M44800A	–
GM71C4800L	HM514800L	TC514800AL	–	–	–	–
GM71C4260	HM514260	TC514260A	μPD424260	MB814260	M5M44260A	–
GM71C4260L	HM514260L	TC514260AL	–	–	–	–

DRAM MODULE

GoldStar	Hitachi	Toshiba	NEC	Fujitsu	Mitsubishi	TI
GMM78256S	HB56D25608	THM82500AS	MC-41256A8	MB85214	MH25608J/JA	TM4256FL8
GMM79256NS	HB56D25609	THM925000AS	MC-41256A9	MB85227	MH25609J/JA	TM4256GU9
GMM781000S	HB56A18	THM81000AS	MC-421000A8	MB85230	MH1M08A0J/JA	–
GMM791000S	HB56A19	THM91000AS	MC-421000A9A	MB85235	MH1M09B0J	TM024GAD9
GMM791000NS	–	THM91070S	–	–	–	–
GMM784000S	HB56A48	THM84000ASG	MC-42400A8A	MB85285	MH4M08A0DJ	–
GMM794000S	HB56A49	THM94000ASG	MC-42400A9A	MB85295	MH4M09A0DJ	–
GMM7321000SG	HB56D132R	THM321000ASG	MC-421000A32	–	HM1M32DJ	–
GMM7361000SG	HB56D136	THM361040ASG	MC-421000A36	–	MH1M36DJ	–
GMM7322000SG	HB56D232	THM322020ASG	MC-422000A32	–	HM2M32EJ	–
GMM7362000SG	HB56D236	THM362040ASG	MC-422000A36	–	HM2M36CJ	–
GMM7401000SG	HB56A140	THM401000ASG	–	–	–	–
GMM7402000SG	HB56A240	THM402020ASG	–	–	–	–

MULTIPORT VIDEO RAM

GoldStar	Hitachi	NEC	Fujitsu	Mitsubishi	TI	Vitelic
GM53C261	HM53461*	μPD41264*	MB81461*	M5M4C264	TMS4461*	V53C261

(NOTE) *: Not fully compatible

STATIC RAM

GoldStar	Hitachi	Toshiba	NEC	Fujitsu	Mitsubishi	Sony
GM76C28A	HM6116/L	TC5517	μPD446	MB8416	M5M5117	CXK5816
GM76C88AL	HM6264AL	TC5565A/L	μPD4364L	MB8464L	M5M5165	CXK5864B
GM76C256AL/ALL	HM62256/L/AL	TC55257A/AL	μPD43256A	MB84256A/AL	M5M5255B	CXK58257
GM76C8128/L/LL	HM628128L	TC55100/L	μPD431000	MB841000AL	M5M51998	TM562828

MASK ROM

GoldStar	Hitachi	Toshiba	NEC	Fujitsu	Mitsubishi	Sharp
GM231000	HN62321	TC531000	μPD23C1000	MB831000	M5M23C100	LH531000A
GM23C4000	HN623×4	TC534000	μPD23C4001E	MB834100	M5M23C401	LH534300
GM23C4100	HN624×4	—	μPD23C4000	MB834200	M5M23C400	LH534000
GM23C1000	HN62321P	TC531000CP	μPD23C1000AC	MB831000	M5M23C1000	LH231000BD
GM23C8100	HN62418P	TC538200P	μPD23C8000	MB838200	M5M23800P	LH538000D

A. TERMS AND DEFINITIONS

VOLTAGES

V_{IH} High-level input voltage
An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-level input voltage
An input voltage level with the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{OH} High-level output voltage
The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-level output voltage
The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output.

V_{DD} V_{CC}, V_{PP} Supply Voltage
The voltages supplied to the corresponding voltage pins that are required for the device to the function.

CURRENT

I_{IH} High-level input current
The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL} Low-level input current
The current flowing into* an input when a specified low-level voltage is applied to that input.

I_{OH} High-level output current
The current flowing* the output with a specified high-level output voltage V_{OH} applied.

I_{OL} Low-level output current
The current flowing *the output with a specified low-level output voltage V_{OL} applied.

*Note: The current flowing out of a terminal is a negative value.

$I_{O(off)}$ Off-state output current
The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.
*Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

I_{OS} Short-circuit output current
The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CC}, I_{DD} Supply Current
The current into, respectively, the V_{DD},V_{CC} supply terminal.

DYNAMIC CHARACTERISTICS

t_A Access Time

The time interval between the application of a specific input pulse and the availability of valid signals at an output.

(Example)

t_{ACC} : Address access time
t_{ACS} : Chip select access time
t_{OE} : Output enable access time

t_{RC} Cycle Time

The time interval between the start and end of a cycle.

(Example)

t_{RC} : Read cycle time
t_{WC} : Write cycle time

t_{SU} Setup Time

The time interval for which a signal is applied and maintained at a specified intput terminal before an active transition occurs at another specified input terminal.

(Example)

t_{AS} : Address set-up time
t_{DW} : Input data set-up time
t_{ASW} : Write address set-up time

t_{HOLD} Hold Time

The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.

(Example)

t_{RAH} : Row address hold time
t_{DH} : Input data hold time
t_{ROH} : Output data hold time from $\overline{RAS}$

t_W Pulse Duration (width)

The time interval between specified reference points on the leading and trailing edges of the pules waveform.

(Example)

t_{WP} : Write pulse duration
t_{SP} : Chip select pulse width

t_{REF} Refresh time interval

The time interval between the beginings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

The refresh time interval is the actual time interval between two refresh operations and is determined by the system in which the digital circuit operates. A maximum value is specified that is the longest interval for which correct operation of the digital is guaranteed.

(Example)

t_{REF} : Refresh time interval

Transition times (also called rise and fall times)

The time interval between two reference points (10% and 90% unless otherwise specified) on the same waveform that is changing from the defined low level to the defined high level (rise time) or from the defined high level to the defined low level (fall time).

Valid time

(a) General
The time interval during which a signal is (or should be) valid.

(b) Output data-valid time
The time interval in which output data contines to be valid following a change of input conditions that could cause the output data to change at the end of the interval.

Enable time (of a three-state output)

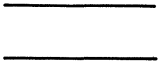
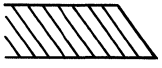
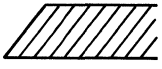
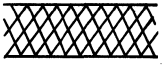
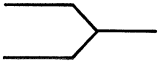
The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Note: For memories these intervals are often classified as access times.

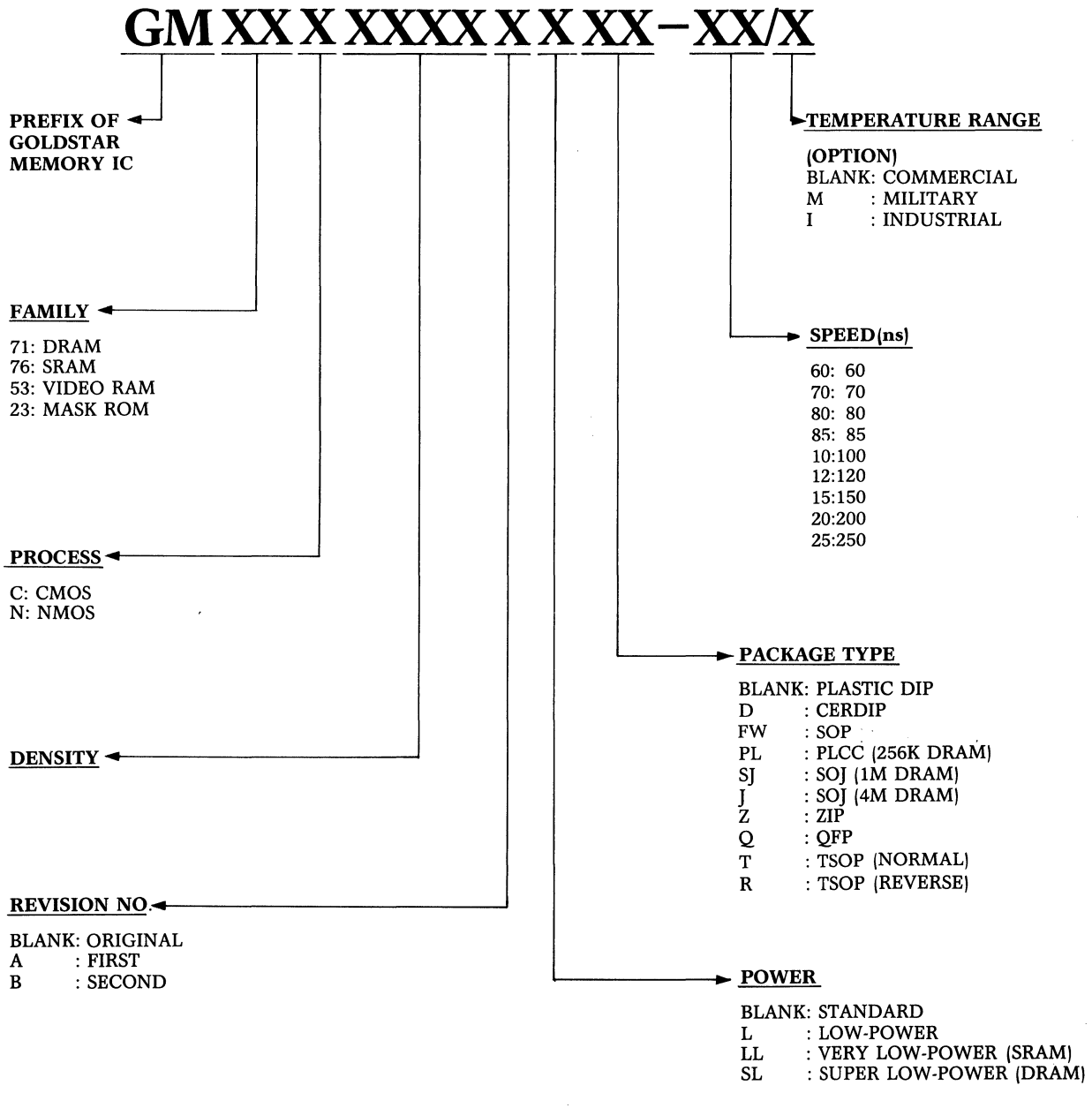
Disable time (of a three-state output)

The time interval between the specified reference points on the input and output voltage waveforms, which the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

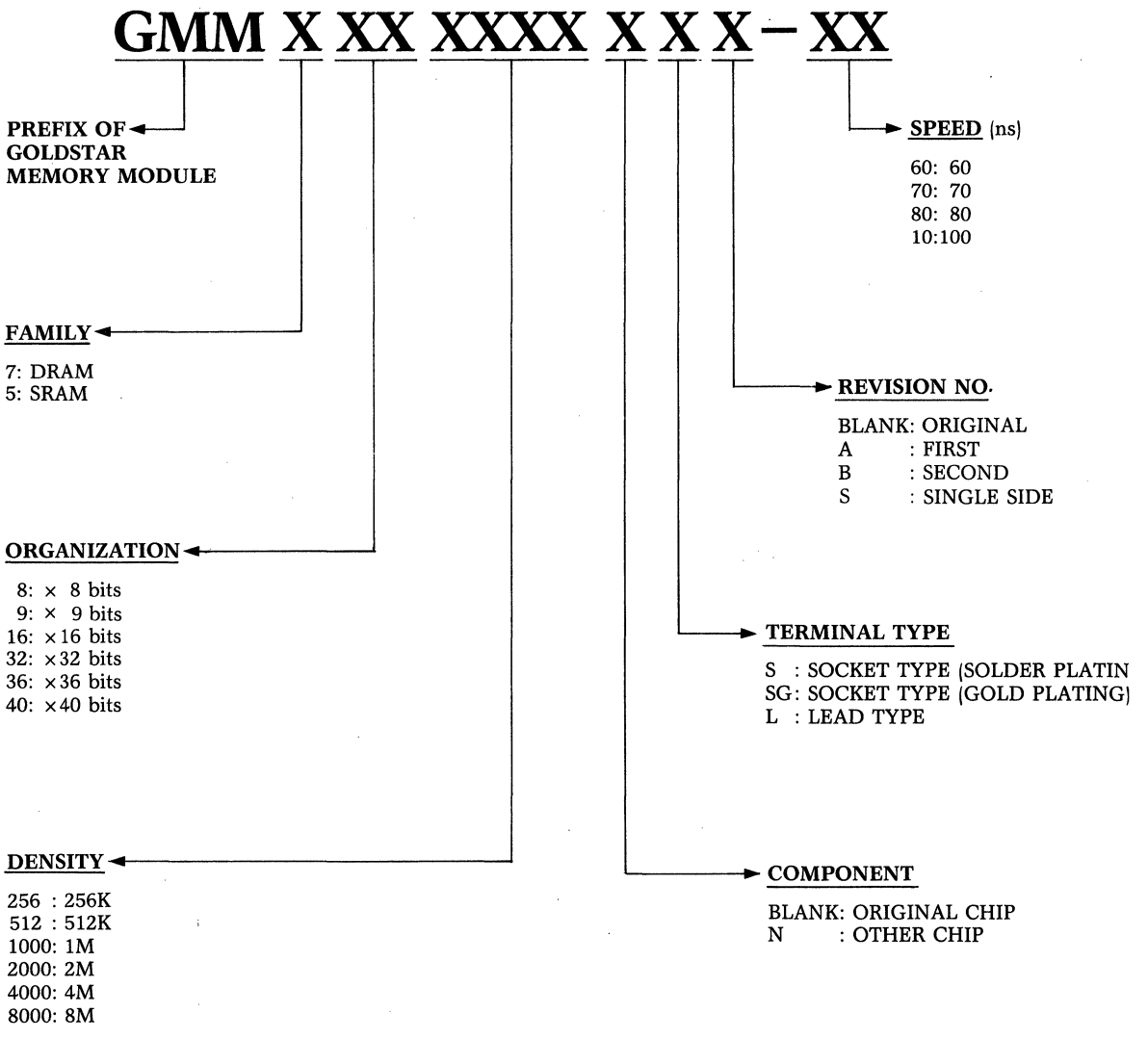
B. WAVEFORMS

Symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	N/A	HIGH IMPEDANCE

GOLDSTAR MEMORY
ORDERING INFORMATION — I (COMPONENT)



GOLDSTAR MEMORY
ORDERING INFORMATION — II (MODULE)

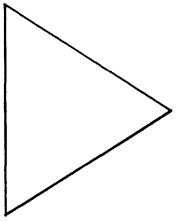


PACKAGE SERIES FOR MOS MEMORY

Type	ORG	DIP	SOJ	ZIP	SOP	QFP	TSOP
DRAM	256K×1	300MIL/16PIN					
	64K×4	300MIL/18PIN					
	1M×1	300MIL/18PIN	300MIL/20PIN	400MIL/20PIN			
	256K×4	300MIL/20PIN	300MIL/20PIN	400MIL/20PIN			
	4M×1		300MIL/20PIN	400MIL/20PIN			TYPE II
	1M×4		300MIL/20PIN	400MIL/20PIN			TYPE II
	512K×8		400MIL/28PIN				TYPE II
	256K×16		400MIL/40PIN				TYPE II
V-RAM	64K×4			400MIL/24PIN			
SRAM	2K×8	600MIL/24PIN			330MIL/24PIN		
	8K×8	600MIL/28PIN			330MIL/28PIN		
	32K×8	600MIL/28PIN			330MIL/28PIN		
	128K×8	600MIL/32PIN			525MIL/32PIN		
MASK ROM	128K×8	600MIL/28PIN					
	512K×8	600MIL/32PIN					
	512K×8/ 256K×16	600MIL/40PIN				44PIN	

*Note: PACKAGE NAME

DIP : DUAL IN-LINE PACKAGE
SOJ : SMALL OUTLINE J-LEADED PACKAGE
ZIP : ZIG ZAG IN-LINE PACKAGE
SOP : SMALL OUTLINE PACKAGE
QFP : QUADRATIC FLAT PACKAGE
TSOP: THIN SMALL OUTLINE PACKAGE



GM71C256A

262,144 WORDS × 1 BIT
CMOS DYNAMIC RAM

Description

The GM71C256A is the new generation dynamic RAM organized 262,144 × 1 Bit. GM71C256A has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C256A offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71C256A to be packaged in a standard 16 pin DIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

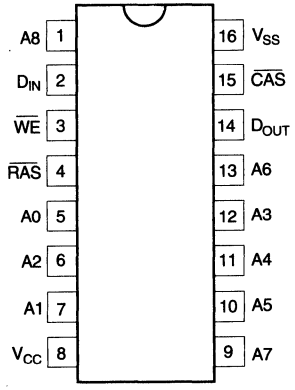
Features

- 262,144 × 1 Bit Organization
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GM71C256A-70	70	15	130	50
GM71C256A-80	80	20	145	55
GM71C256A-10	100	25	175	60

- Low Power
  Active: 385/330/275 mW (MAX)
  Standby: 16.5 mW (CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and output TTL Compatible
- 256 Refresh Cycles/4 ms

Pin Configuration
16 DIP



Pin Description

Pin	Function	Pin	Function
A0 ~ A8	Address Inputs	D_{IN}	Data Input
$\overline{RAS}$	Row Address Strobe	D_{OUT}	Data Output
$\overline{CAS}$	Column Address Strobe	V_{CC}	Power (+5V)
$\overline{WE}$	Write Enable	V_{SS}	Ground

Ordering Information

Type No.	Access Time	Package
GM71C256A-70	70ns	300 Mil
GM71C256A-80	80ns	16 Pin
GM71C256A-10	100ns	Plastic DIP

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature (Plastic)	−55 ~ 125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−1.0 ~ 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	−1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	6.5	V
V_{IL}	Input Low Voltage	−1.0	—	0.8	V

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	70ns	—	70	mA	1,2
		80ns	—	60		
		100ns	—	50		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z)		—	3.5	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	70ns	—	70	mA	2
		80ns	—	60		
		100ns	—	50		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	70ns	—	45	mA	1,3
		80ns	—	40		
		100ns	—	35		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V, D_{OUT} = High-Z)		—	3	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	70ns	—	70	mA	
		80ns	—	60		
		100ns	—	50		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	4	mA	1
$I_{I(L)}$	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 6.5V$)		−10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 6.5V$)		−10	10	μA	

Note 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

Capacitance (V_{CC} = 5V ± 10%, T_A = 25°C)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address, D_{IN})	—	4	pF	1
C_{I2}	Input Capacitance (Clocks)	—	5	pF	1
C_O	Data Capacitance (D_{OUT})	—	6	pF	1,2

Note 1. Capacitance is sampled and not 100% tested.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C, Note 1,14)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	145	—	175	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	55	—	65	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	75,000	80	75,000	100	75,000	ns	
$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width in Read Cycle	15	75,000	20	75,000	25	75,000	ns	
$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width in Write Cycle	20	—	25	—	30	—	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	15	—	15	—	15	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	20	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	55	25	60	25	75	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	35	20	40	20	55	ns	9
$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	15	—	20	—	25	—	ns	
$t_{RSH(W)}$	$\overline{RAS}$ Hold Time (Write Cycle)	25	—	25	—	30	—	ns	
t_{AR}	Column Address Hold Time from $\overline{RAS}$	55	—	60	—	70	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	80	—	100	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	15	—	ns	
t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	7
t_{REF}	Refresh Period	—	4	—	4	—	4	ms	

Read Cycle

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	—	80	—	100	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	—	25	ns	3,4
t_{AA}	Access Time from Column Address	—	35	—	40	—	45	ns	3,5
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	5	—	5	—	5	—	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	5	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	40	—	45	—	ns	
t_{OFF}	Output Buffer Turn-off Delay Time	0	15	0	20	0	25	ns	6

Write Cycle

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55	—	60	—	70	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	20	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	30	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	25	—	30	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	15	—	20	—	ns	11
t_{DHR}	Data-in Hold Time Referenced to $\overline{RAS}$	55	—	60	—	70	—	ns	

Read-Modify-Write Cycle

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Write Cycle Time	155	—	175	—	210	—	ns	
t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	95	—	110	—	135	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	70	—	80	—	100	—	ns	10
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	—	20	—	25	—	ns	10
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	35	—	40	—	45	—	ns	10

Refresh Cycle

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	20	—	25	—	30	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	0	—	ns	

Fast Page Mode Cycle

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	50	—	55	—	60	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	15	—	15	—	20	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	75,000	—	75,000	—	75,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	45	—	50	—	55	ns	13

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71C256A-70		GM71C256A-80		GM71C256A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	75	—	85	—	95	—	ns	

Notes :

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. $t_{OFF}(max)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RCD}(max)$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{CWD} and t_{RWD}, t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : if $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle : if $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, the cycle is a read-write and the data output will contain data read from the selected cell : if neither of the above sets of conditions is satisfied, the condition of the data out(at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or Read-modify-Write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

TIMING WAVEFORMS

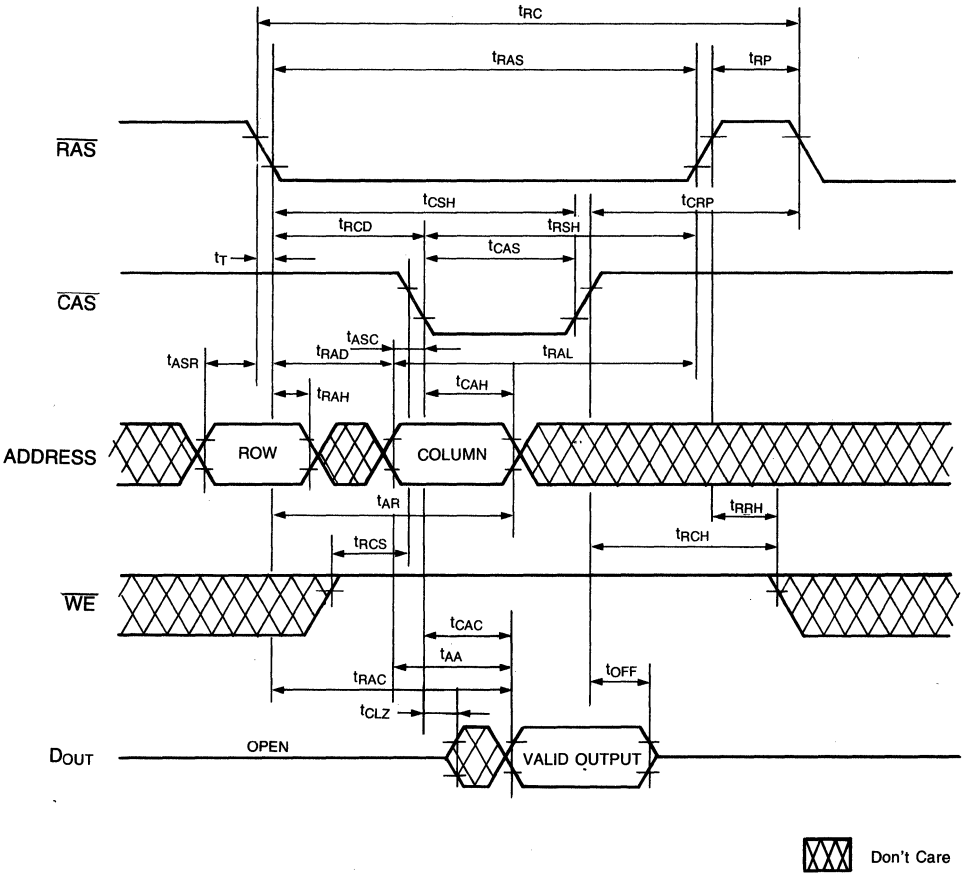


FIGURE 1. READ CYCLE

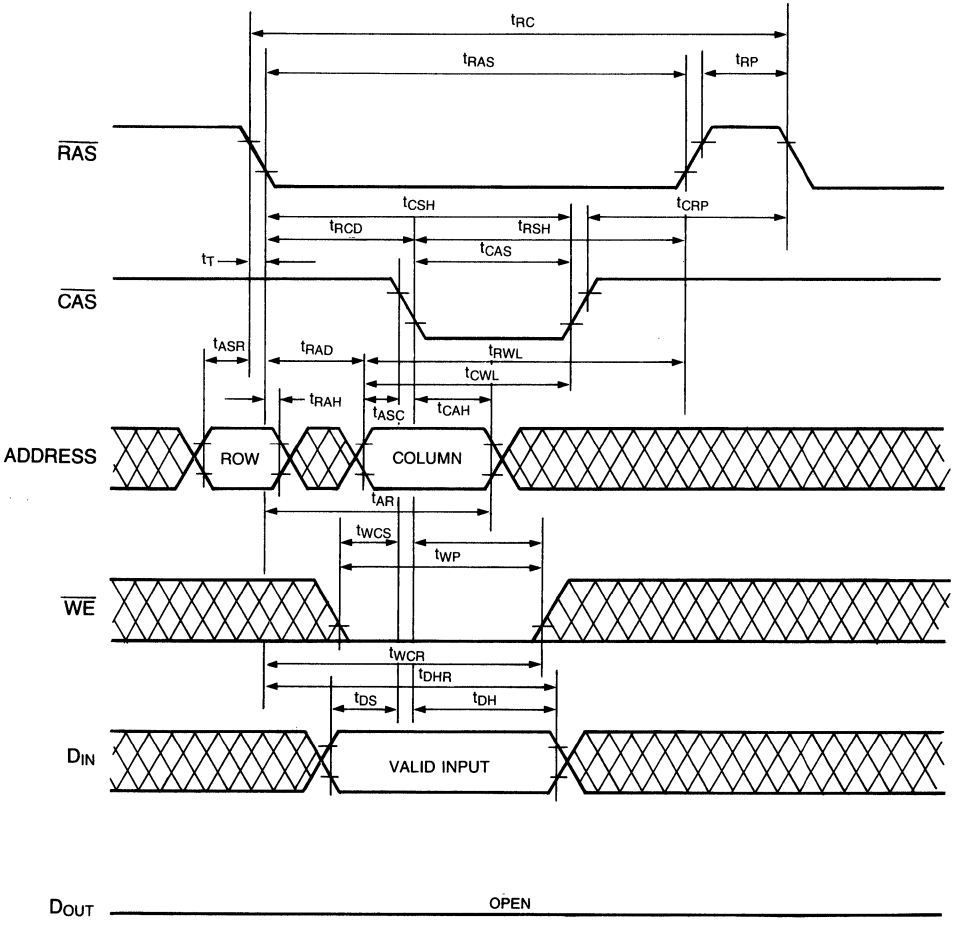


FIGURE 2. EARLY WRITE CYCLE

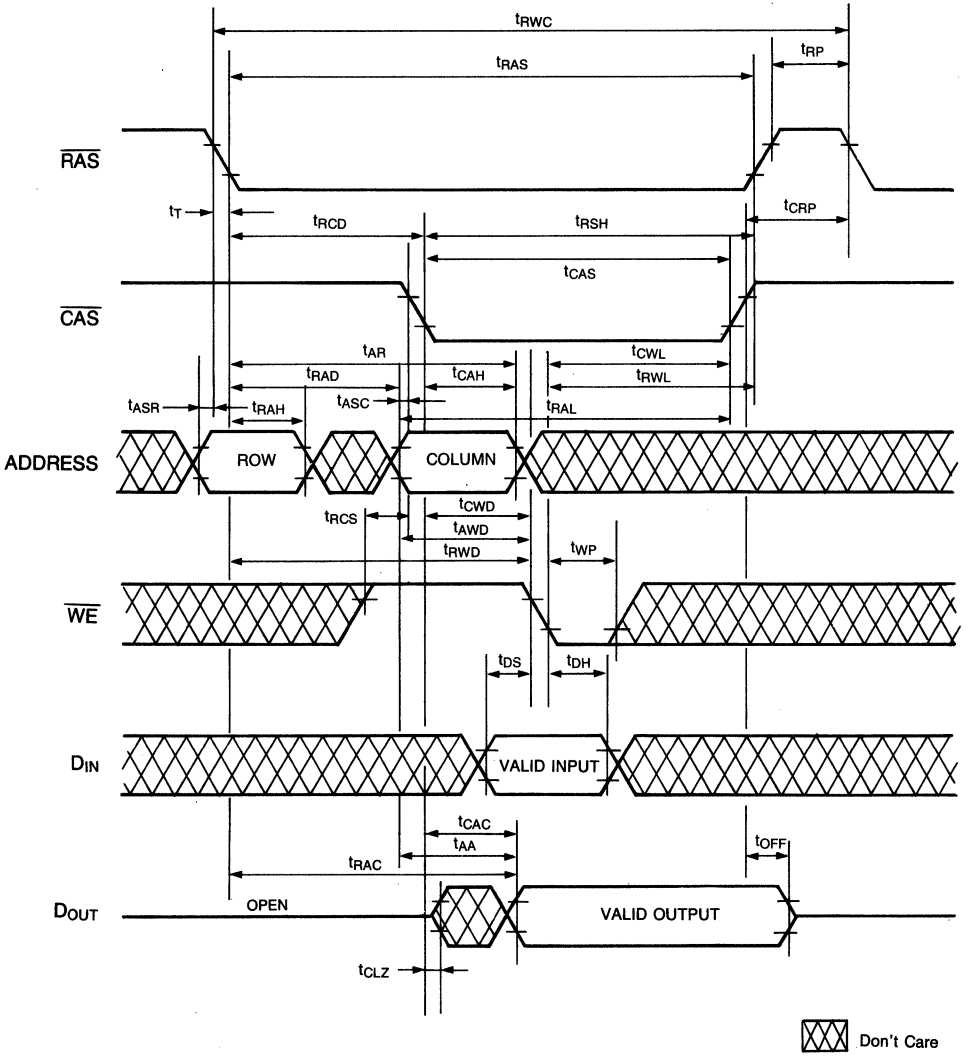


FIGURE 3. READ-MODIFY-WRITE CYCLE

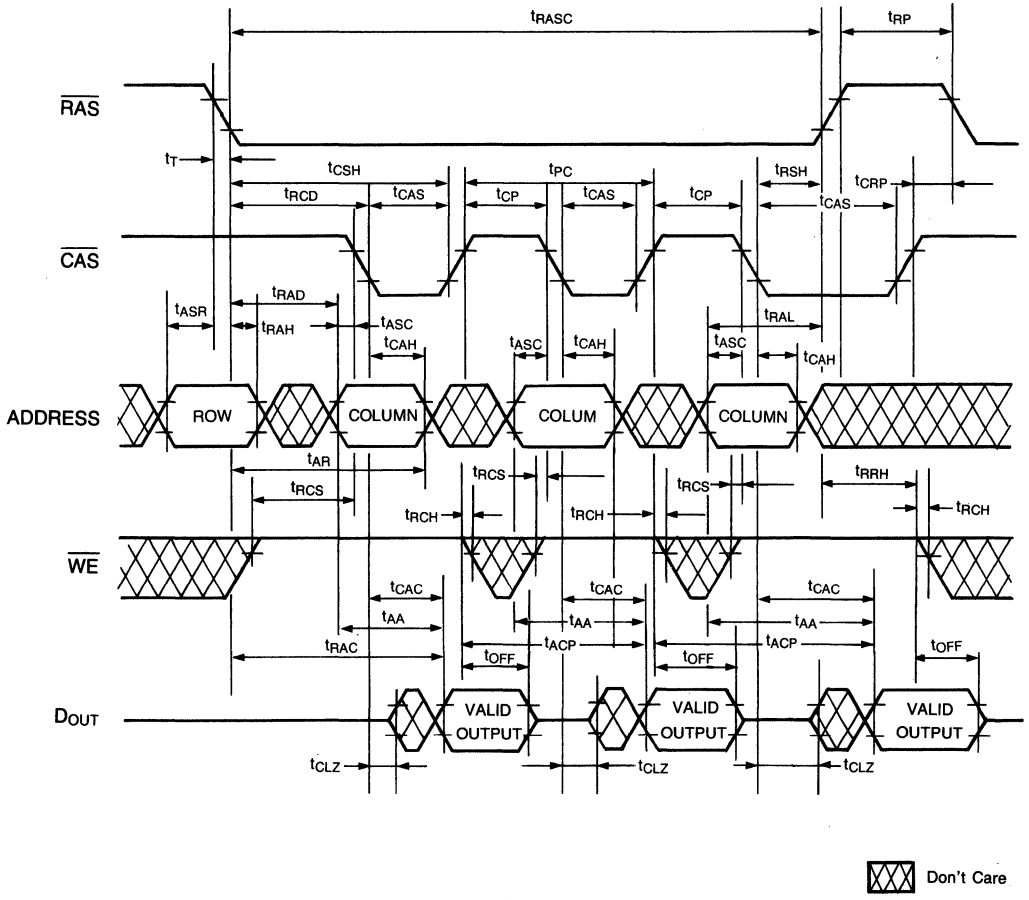


FIGURE 4. FAST PAGE MODE READ CYCLE

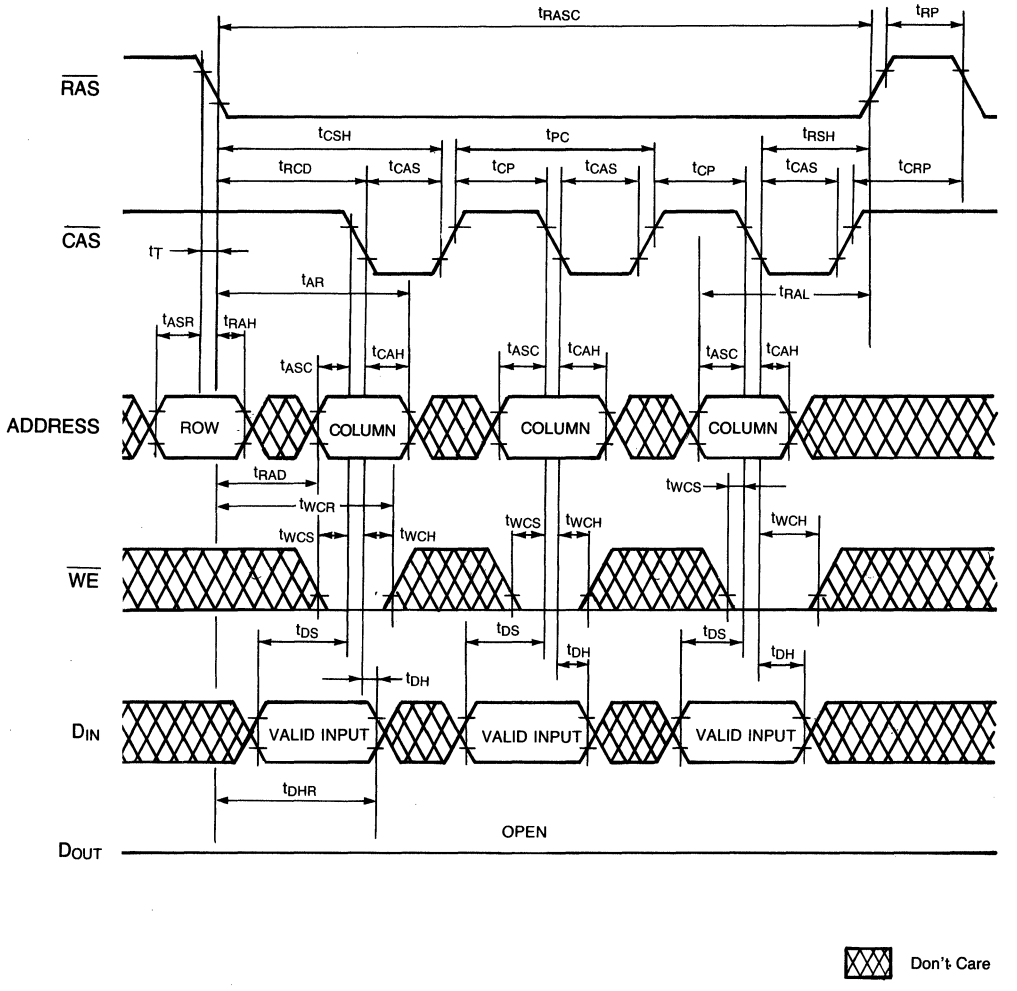


FIGURE FAST PAGE MODE WRITE CYCLE

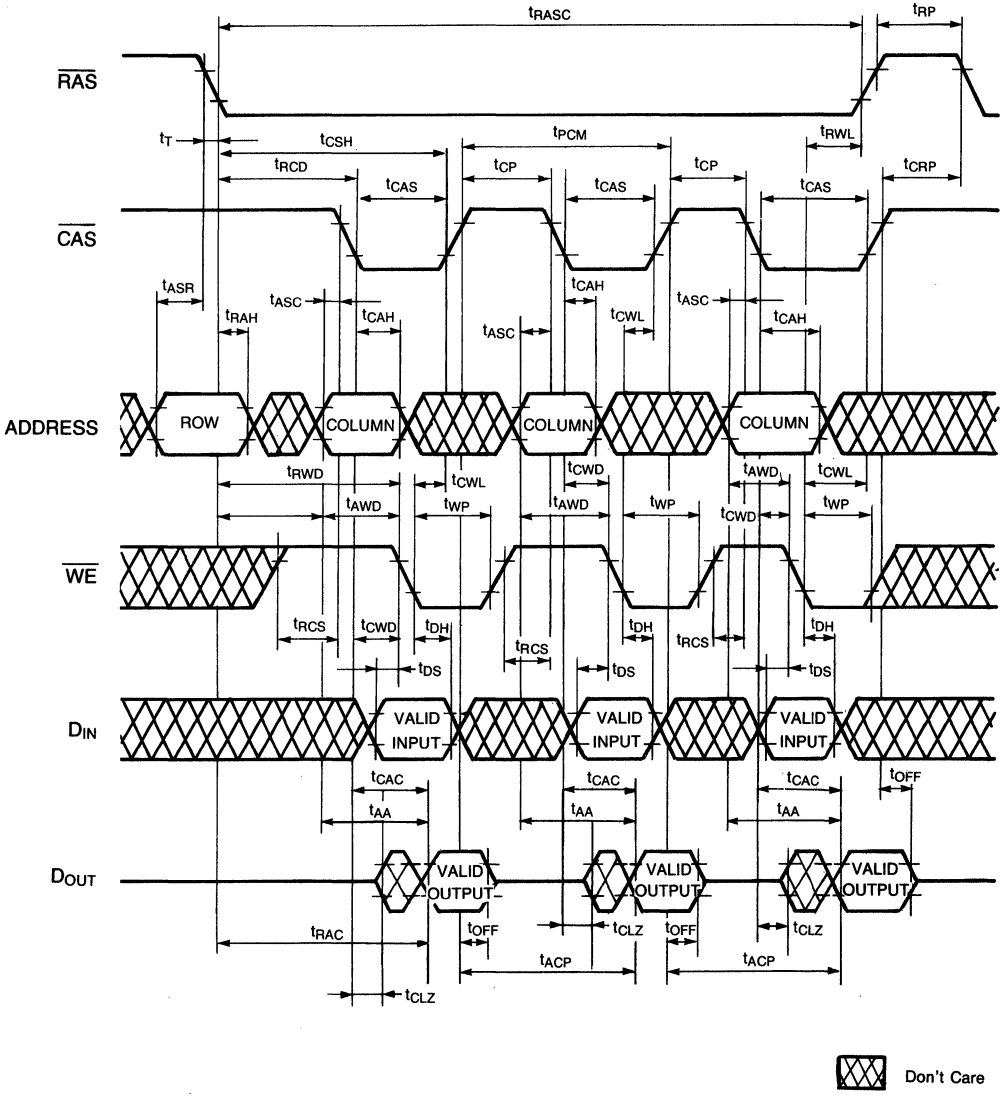


FIGURE FAST PAGE MODE READ-MODIFY-WRITE CYCLE

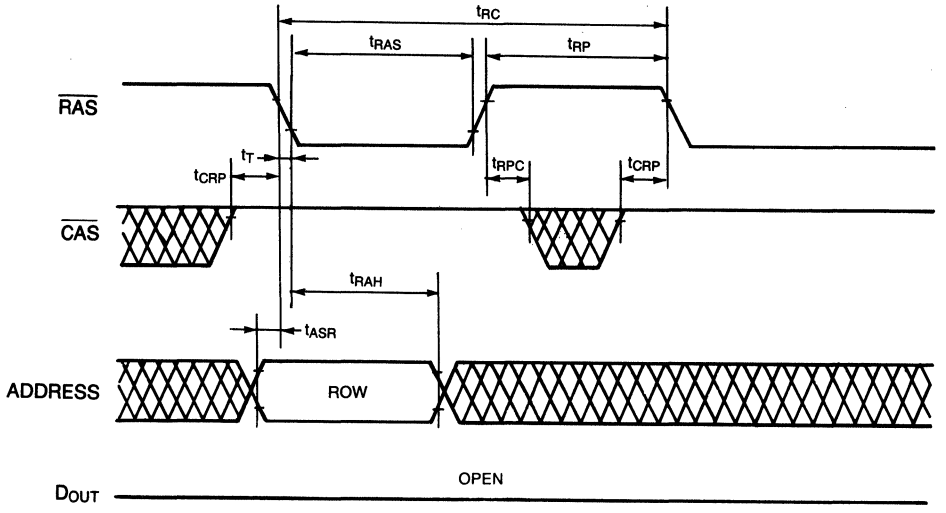


FIGURE 7. RAS-ONLY-REFRESH CYCLE

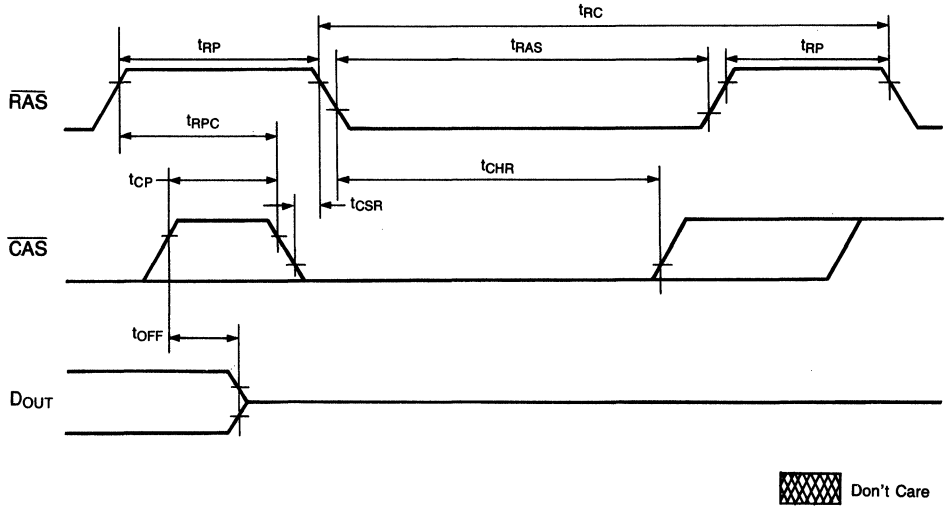


FIGURE 8. CAS BEFORE RAS REFRESH CYCLE

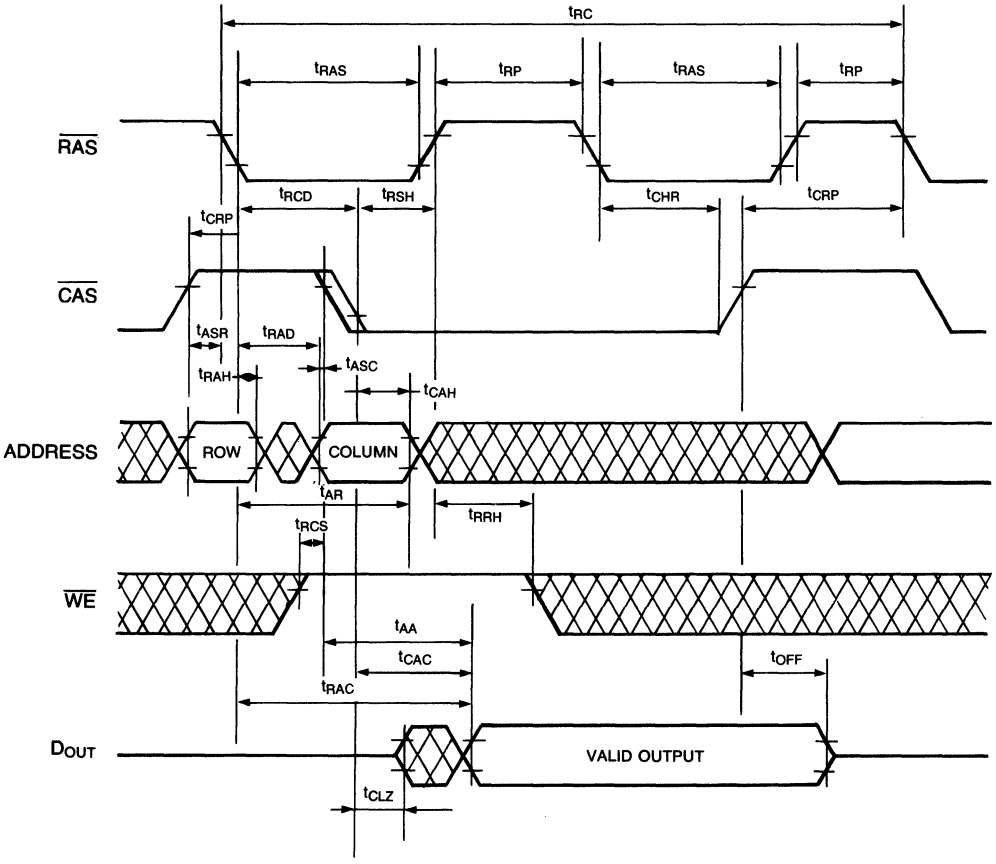


FIGURE 9. HIDDEN REFRESH CYCLE (READ)

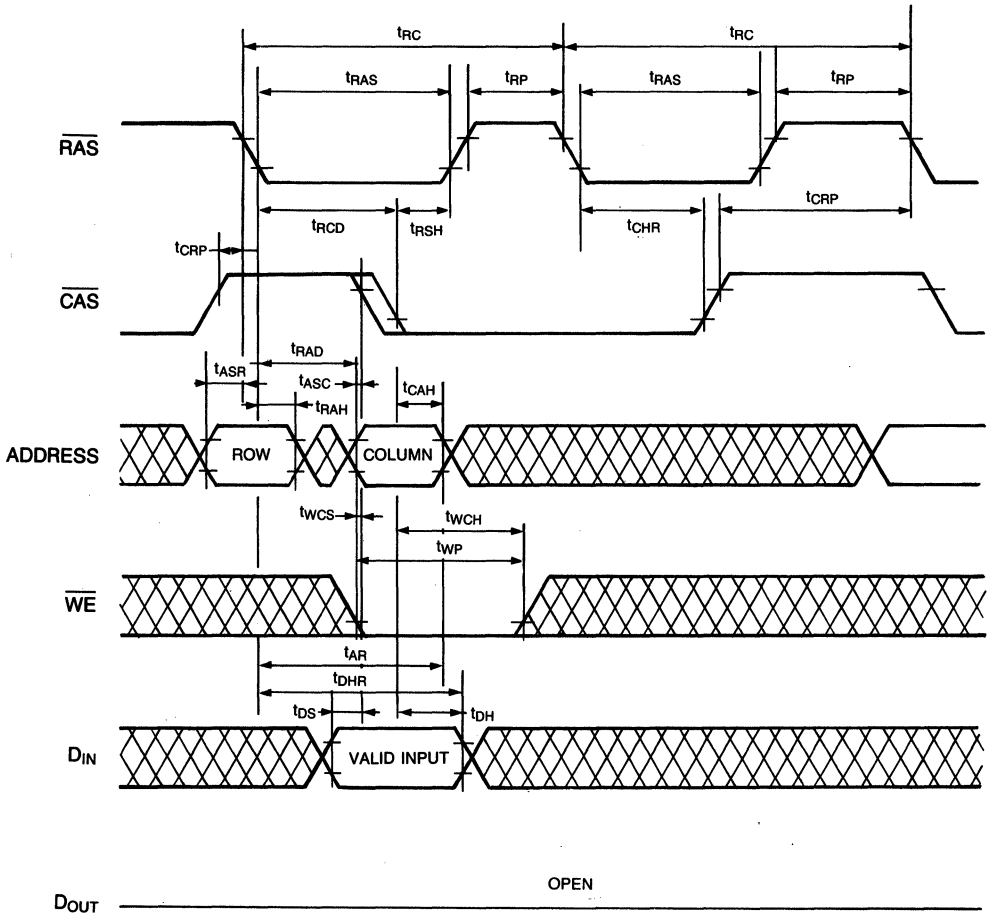


FIGURE 10. HIDDEN REFRESH CYCLE (WRITE)

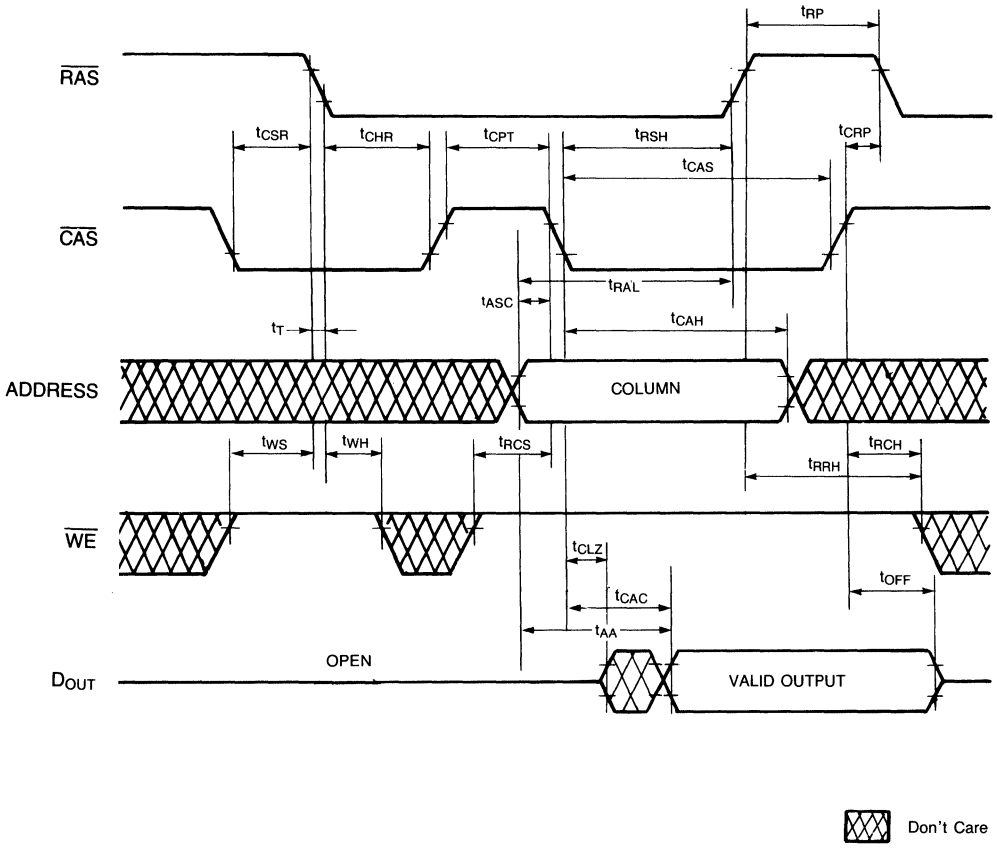


FIGURE 11. $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER CHECK CYCLE (READ)

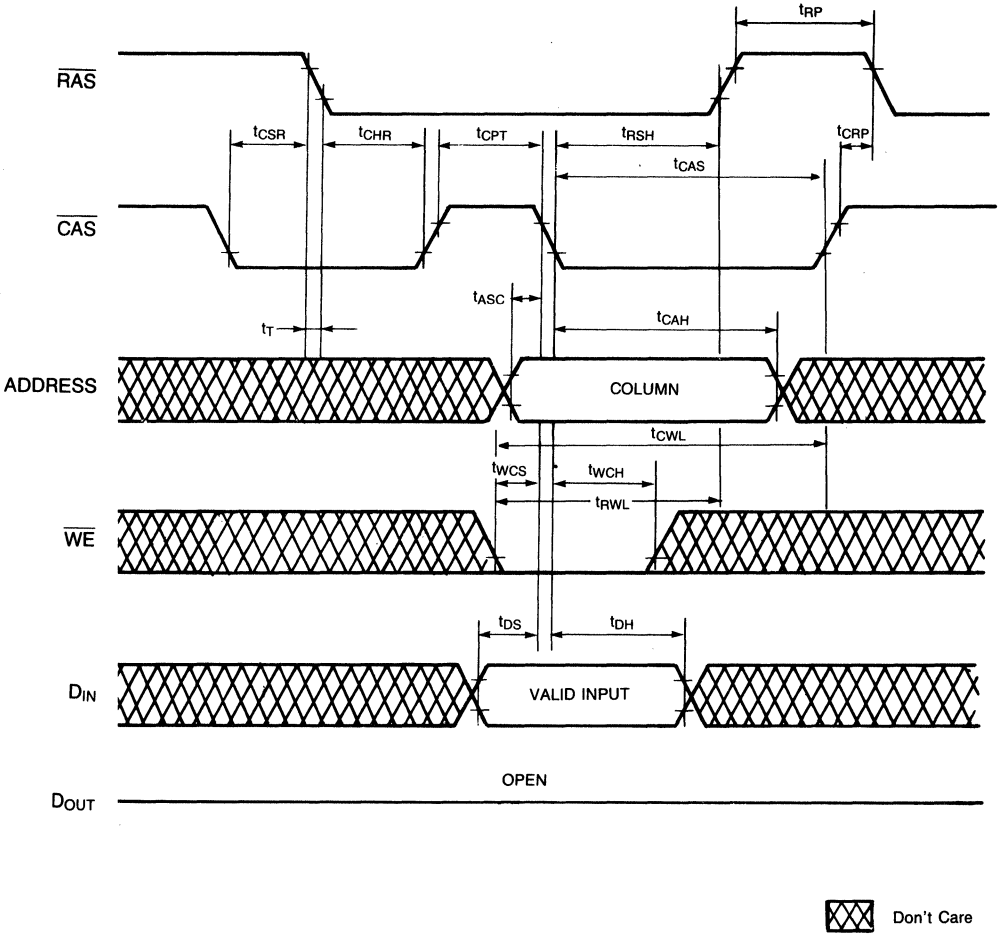
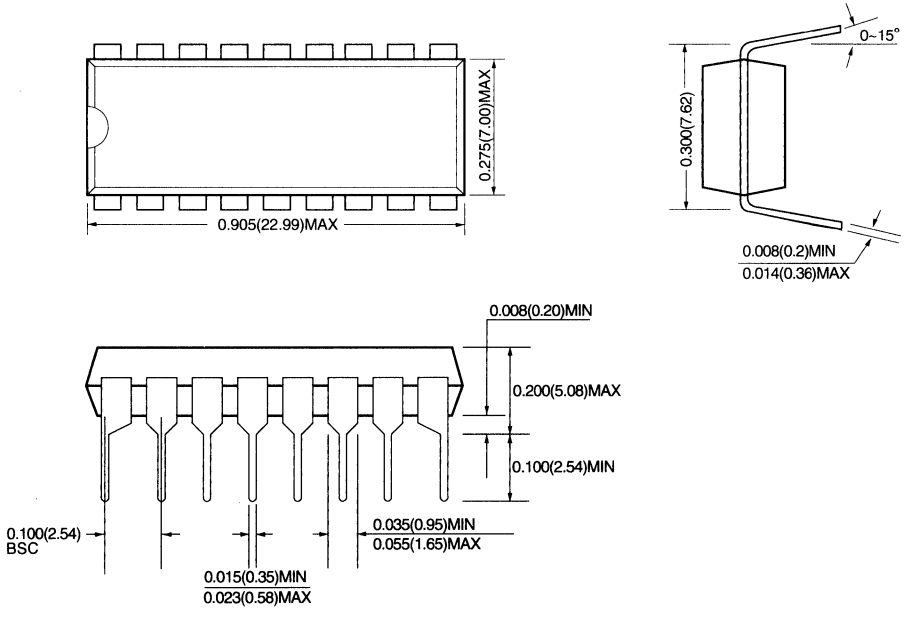


FIGURE 12. $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER CHECK CYCLE (WRITE)

Package Dimensions

16 DIP

Unit: inches (mm)



GM71C464A

65,536 WORDS × 4 BIT
CMOS DYNAMIC RAM

Description

The GM71C464A is the new generation dynamic RAM organized 65,536×4 Bit. GM71C464A has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C464A offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71C464A to be packaged in a standard 18 pin DIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

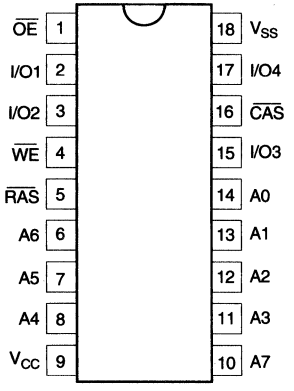
Features

- 65,536×4 Bit Organization
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GM71C464A-70	70	25	130	50
GM71C464A-80	80	30	145	55
GM71C464A-10	100	35	175	65

- Low Power
  Active: 385/330/247 mW (MAX)
  Standby: 16.5 mW (CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 256 Refresh Cycles/4 ms

Pin Configuration
18 DIP



Pin Description

Pin	Function	Pin	Function
A0 ~ A7	Address Inputs	$\overline{OE}$	Output Enable e
$\overline{RAS}$	Row Address Strobe	I/O1 ~ I/O4	Data Input, Output
$\overline{CAS}$	Column Address Strobe	V_{CC}	Power (+5V)
$\overline{WE}$	Write Enable	V_{SS}	Ground

Ordering Information

Type No.	Access Time	Package
GM71C464A-70	70ns	300 Mil
GM71C464A-80	80ns	18 Pin
GM71C464A-10	100ns	Plastic DIP

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature (Plastic)	−55 ~ 125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−1.0 ~ 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	−1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	6.5	V
V_{IL}	Input Low Voltage	−1.0	—	0.8	V

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	70ns	—	80	mA	1,2
		80ns	—	70		
		100ns	—	65		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	3.5	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	70ns	—	75	mA	2
		80ns	—	65		
		100ns	—	55		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{PC} = t_{PC} min)	70ns	—	45	mA	1,3
		80ns	—	45		
		100ns	—	35		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V)		—	3	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	70ns	—	70	mA	
		80ns	—	65		
		100ns	—	55		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	4	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 6.5V) All Other Pins Not Under Test = 0V		−10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 6.5V)		−10	10	μA	

Note 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

Capacitance (V_{CC} = 5V ± 10%, T_A = 25°C)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	—	4	pF	1
C_{I2}	Input Capacitance (Clocks)	—	5	pF	1
$C_{I/O}$	Data Input/Data Output (Data-In/Out)	—	6	pF	1,2

Note 1. Capacitance is sampled and not 100% tested.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C, Note 1,14)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C464A-70		GM71C464A-80		GM71C464A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	145	—	175	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	55	—	65	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	75,000	80	75,000	100	75,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25	75,000	30	75,000	35	75,000	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	15	—	15	—	15	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	20	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	25	45	25	50	25	65	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	35	20	40	20	55	ns	9
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	0	—	0	—	0	—	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25	—	30	—	35	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	80	—	100	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	15	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	25	—	30	—	ns	
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	—	0	—	0	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	7
t_{AR}	Column Address Hold Time from $\overline{RAS}$	55	—	60	—	70	—	ns	
t_{REF}	Refresh Period	4	—	4	—	4	—	ms	

Read Cycle

Symbol	Parameter	GM71C464A-70		GM71C464A-80		GM71C464A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	—	80	—	100	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	—	25	—	30	—	35	ns	3,4
t_{AA}	Access Time from Column Address	—	35	—	40	—	45	ns	3,5
t_{OAC}	Access Time from $\overline{OE}$	—	15	—	20	—	25	ns	
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time $\overline{CAS}$	5	—	5	—	5	—	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	5	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	40	—	45	—	ns	
t_{OFF1}	Output Buffer Turn-off Delay Time	0	15	0	15	0	15	ns	6
t_{OFF2}	Output Buffer Turn-off to Delay Time from $\overline{OE}$	0	15	0	20	0	25	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	20	—	25	—	ns	
t_{CLZ}	$\overline{CAS}$ to Low-Z Output	0	—	0	—	0	—	ns	

Write Cycle

Symbol	Parameter	GM71C464A-70		GM71C464A-80		GM71C464A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55	—	60	—	70	—	Ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	20	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25	—	30	—	35	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25	—	30	—	35	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	15	—	20	—	ns	11
t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	55	—	60	—	70	—	ns	

Read-Modify-Write Cycle

Symbol	Parameter	GM71C464A-70		GM71C464A-80		GM71C464A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Write Cycle Time	195	—	225	—	265	—	ns	
t_{RRW}	$\overline{RAS}$ Pulse Width	125	—	145	—	175	—	na	
t_{CRW}	$\overline{CAS}$ Pulse Width	80	—	95	—	110	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	95	—	110	—	135	—	ns	10
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	50	—	55	—	60	—	ns	10
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60	—	70	—	80	—	ns	10
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	15	—	20	—	25	—	ns	

Refresh Cycle

Symbol	Parameter	GM71C464A-70		GM71C464A-80		GM71C464A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	20	—	25	—	30	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	0	—	ns	

Fast Page Mode Cycle

Symbol	Parameter	GM71C464A-70		GM71C464A-80		GM71C464A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	50	—	55	—	65	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Recharge Time	15	—	15	—	20	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	75,000	—	75,000	—	75,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	45	—	50	—	55	ns	13
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45	—	50	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71C464A-70		GM71C464A-80		GM71C464A-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	80	—	90	—	100	—	ns	

Notes :

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. $t_{OFF1}(max)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RCD}(max)$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : if $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle : if $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, the cycle is a read-write and the data output will contain data read from the selected cell : if neither of the above sets of conditions is satisfied, the condition of the data out(at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or Read-Modify-Write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

TIMING WAVEFORMS

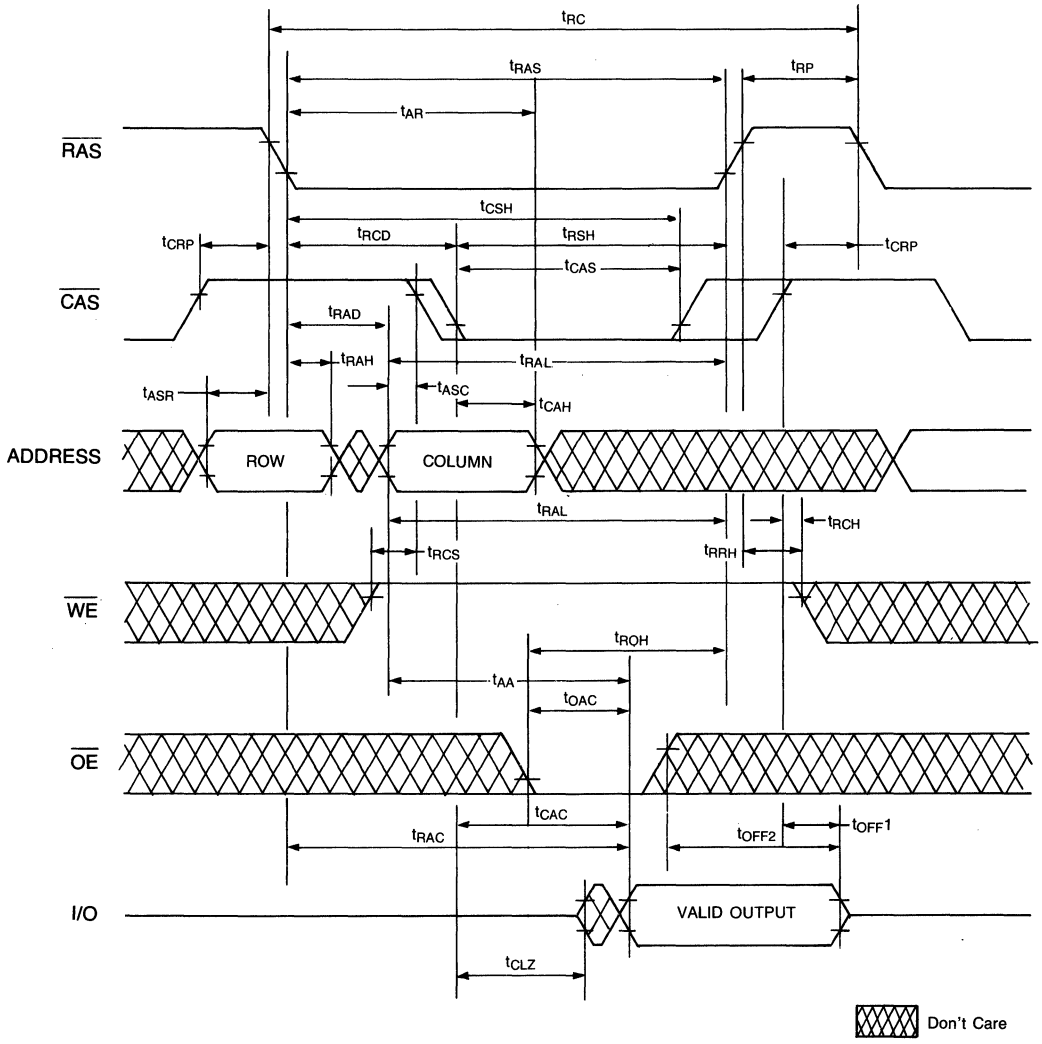


FIGURE 1. READ CYCLE

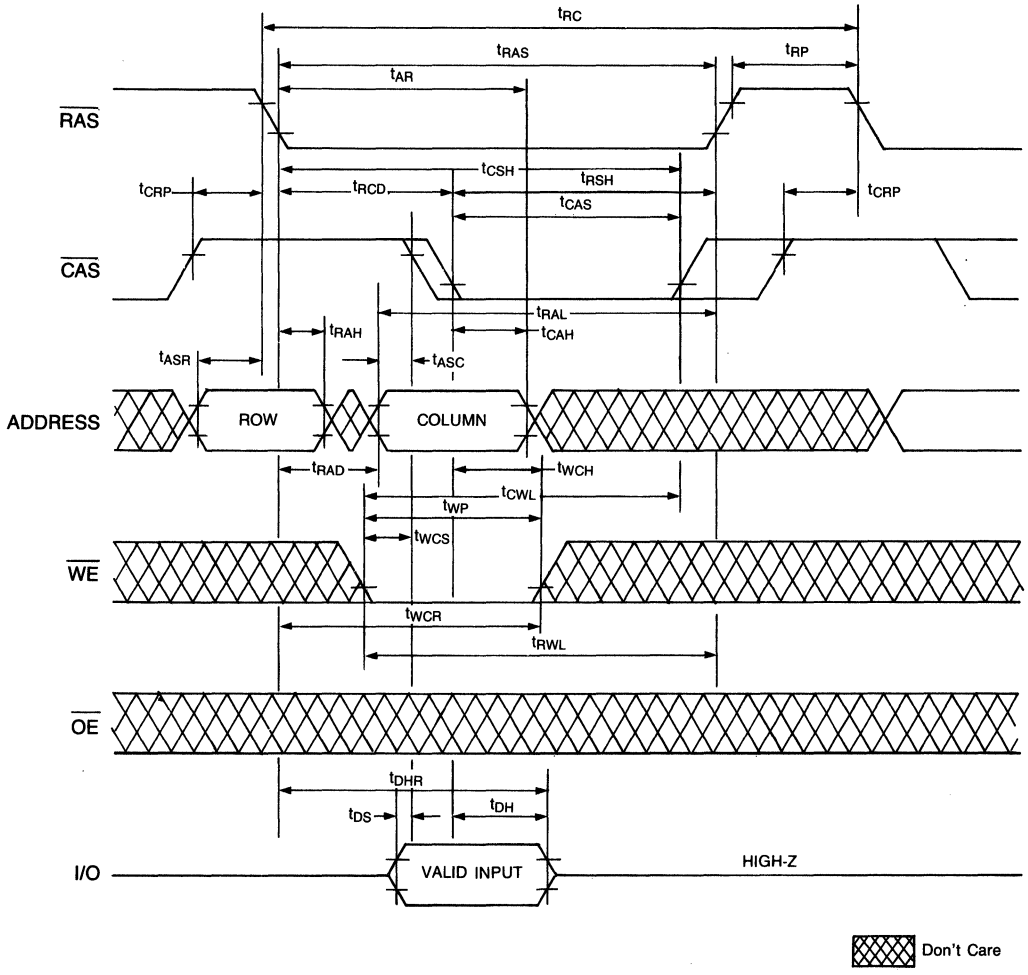


FIGURE 2. EARLY WRITE CYCLE

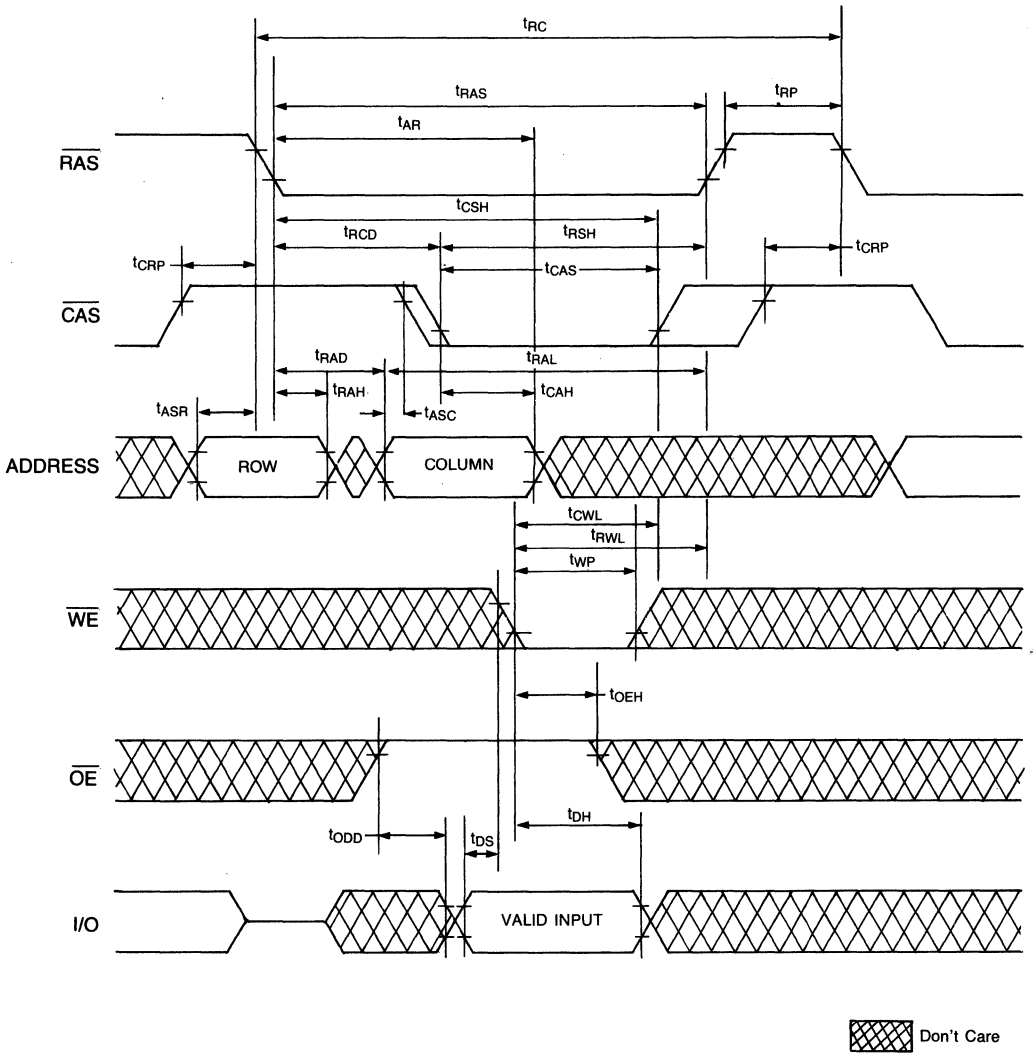


FIGURE 3. WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)

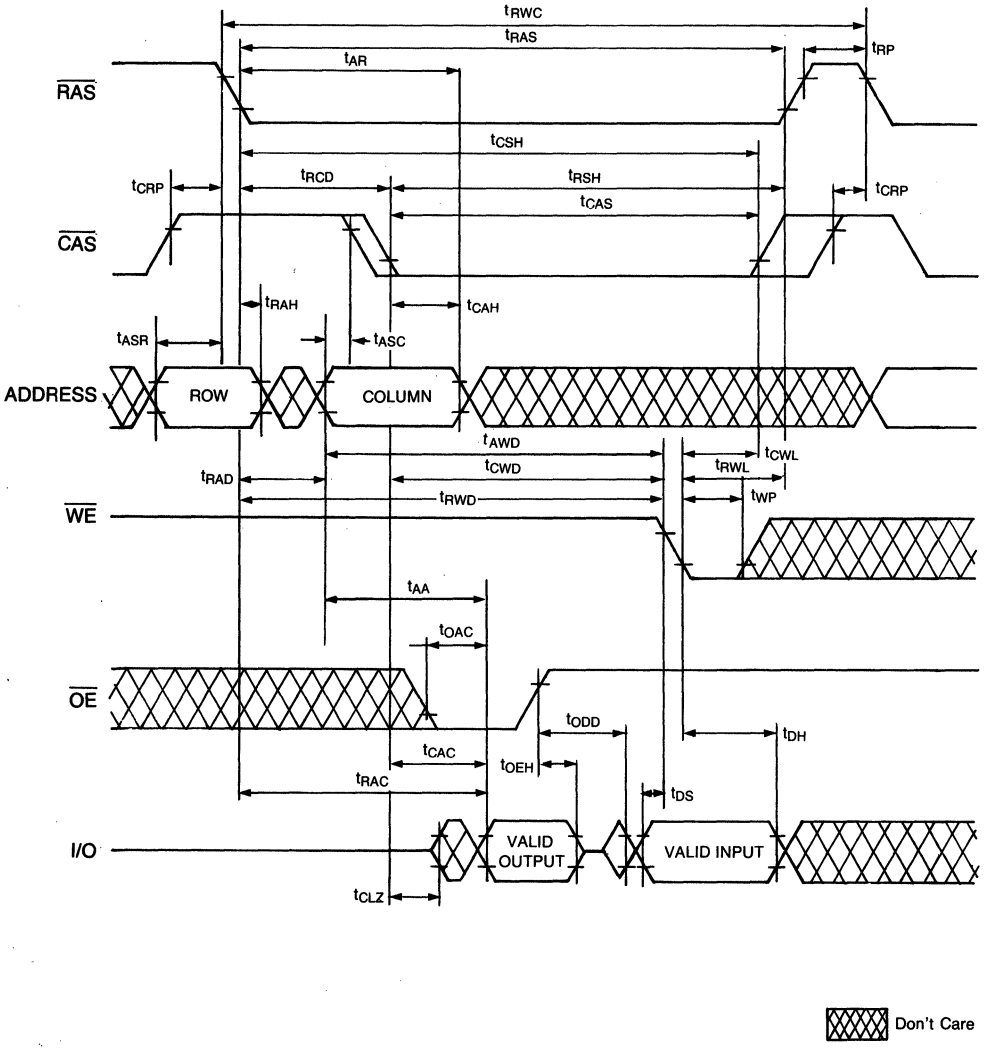


FIGURE 4. READ-MODIFY-WRITE CYCLE

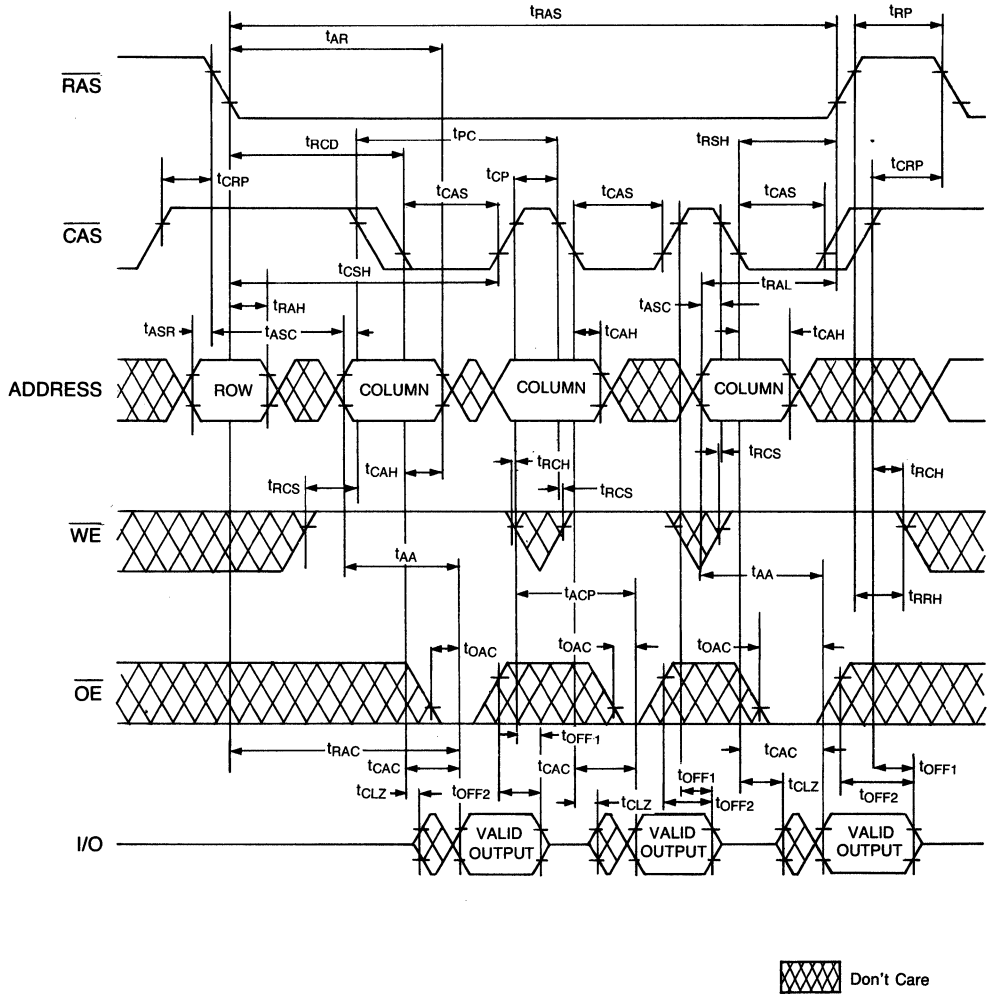


FIGURE 5. FAST PAGE MODE READ CYCLE

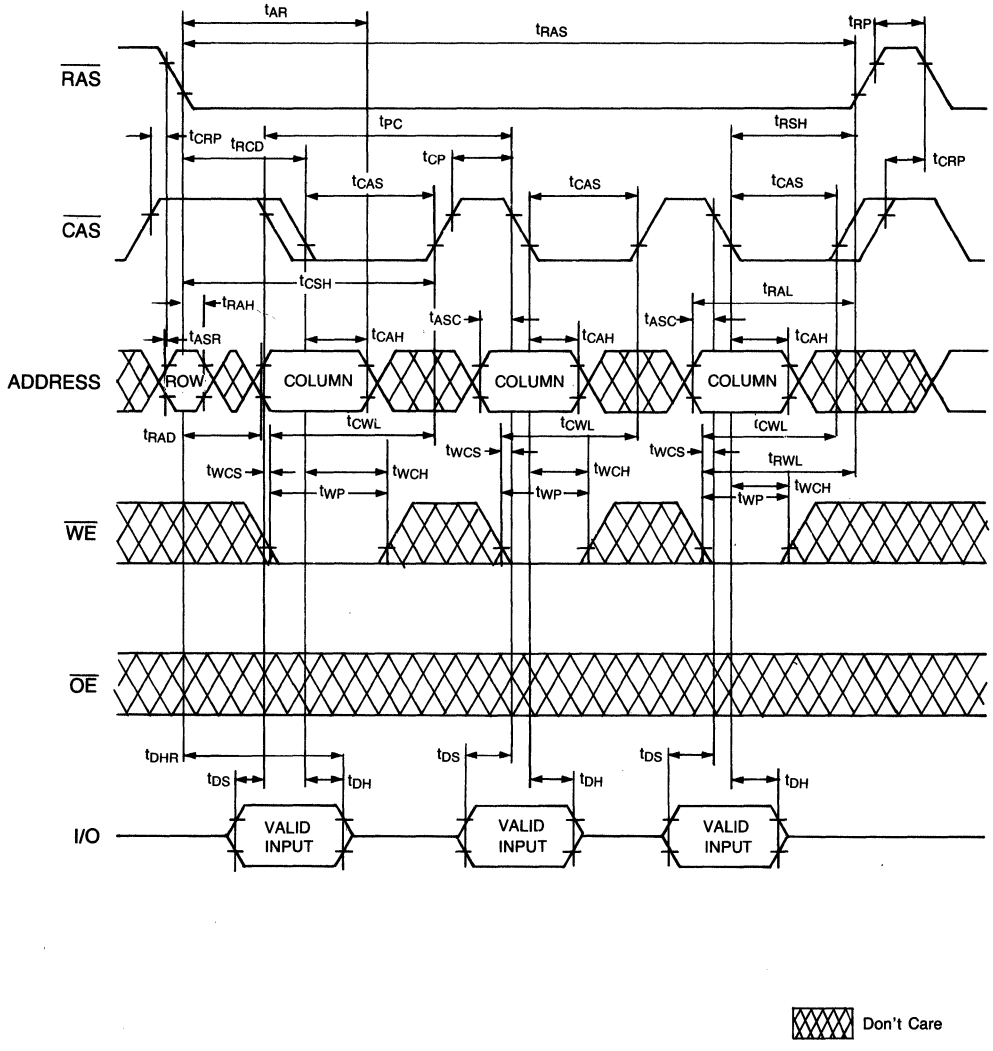


FIGURE 6. FAST PAGE MODE WRITE CYCLE

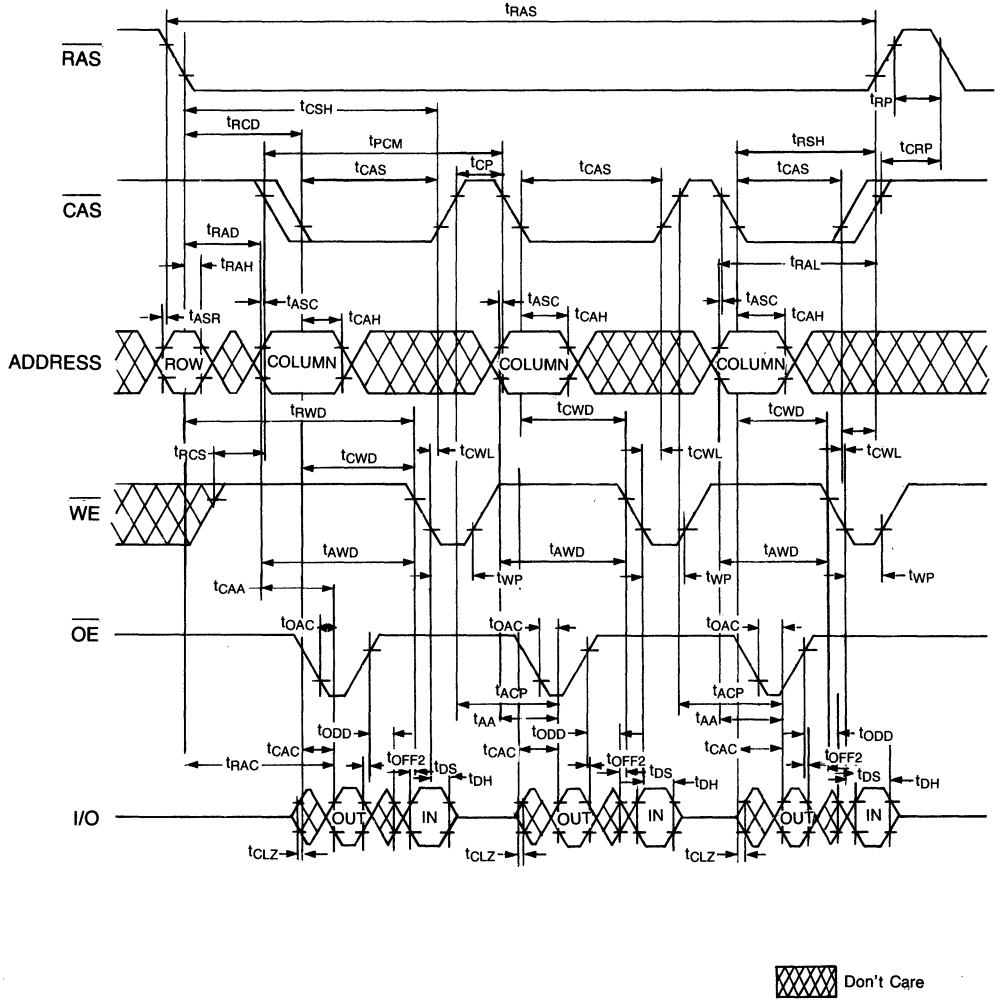


FIGURE FAST PAGE MODE READ-MODIFY-WRITE CYCLE

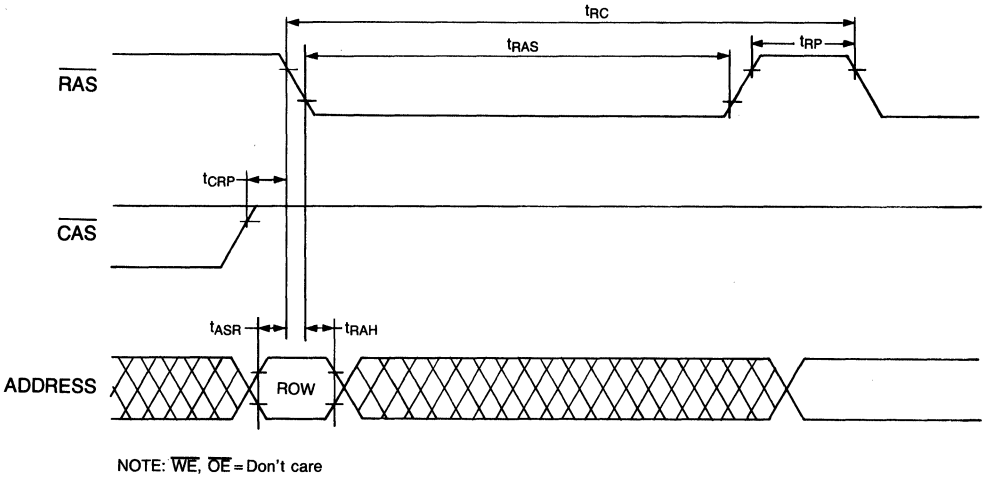


FIGURE 8. RAS ONLY REFRESH CYCLE

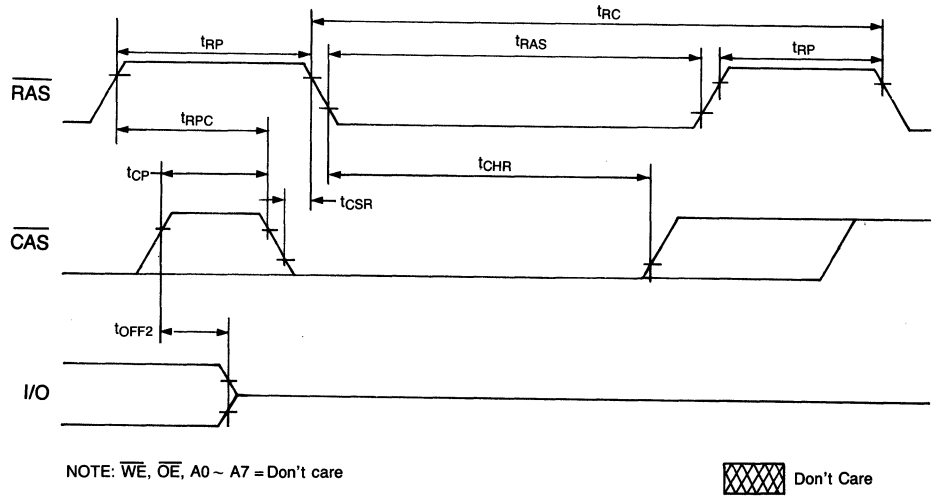


FIGURE 9. CAS BEFORE RAS REFRESH CYCLE

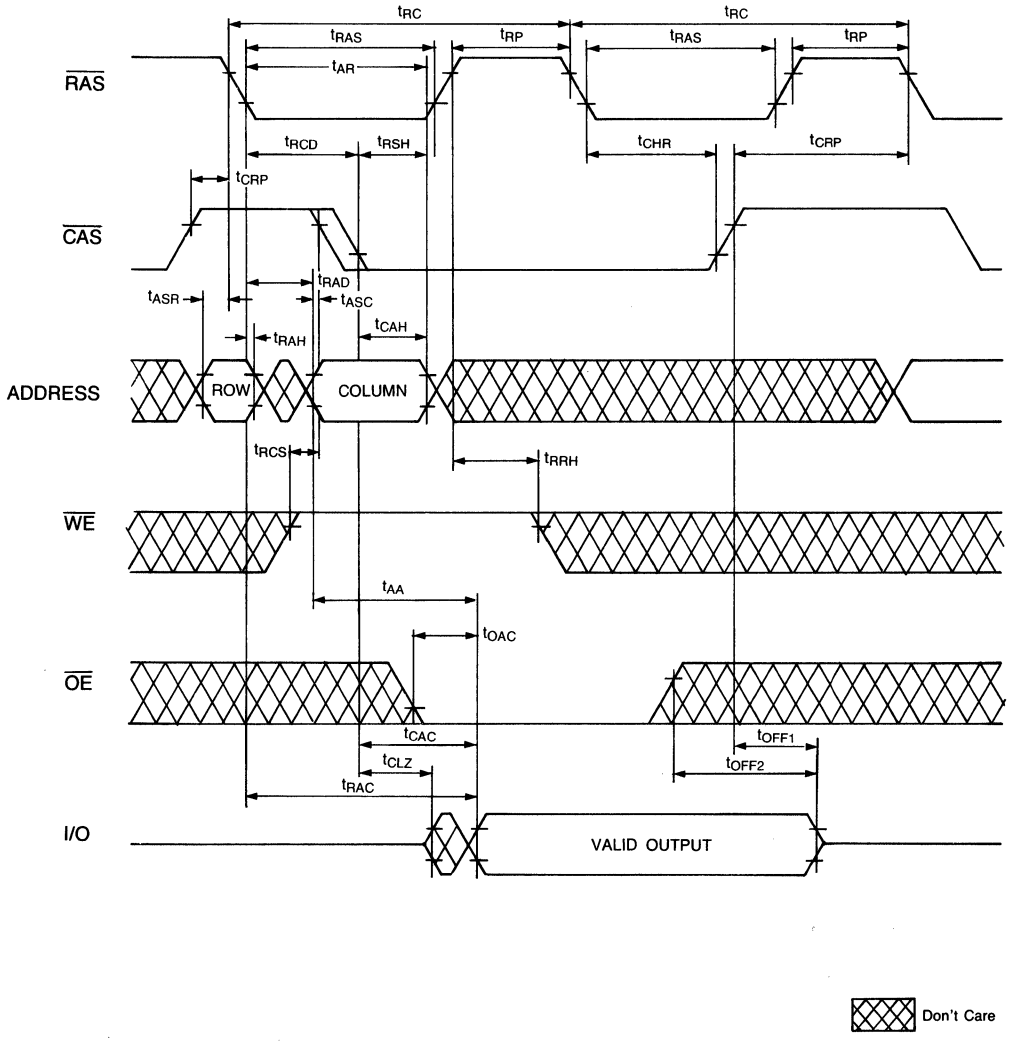


FIGURE 10. HIDDEN REFRESH CYCLE (READ)

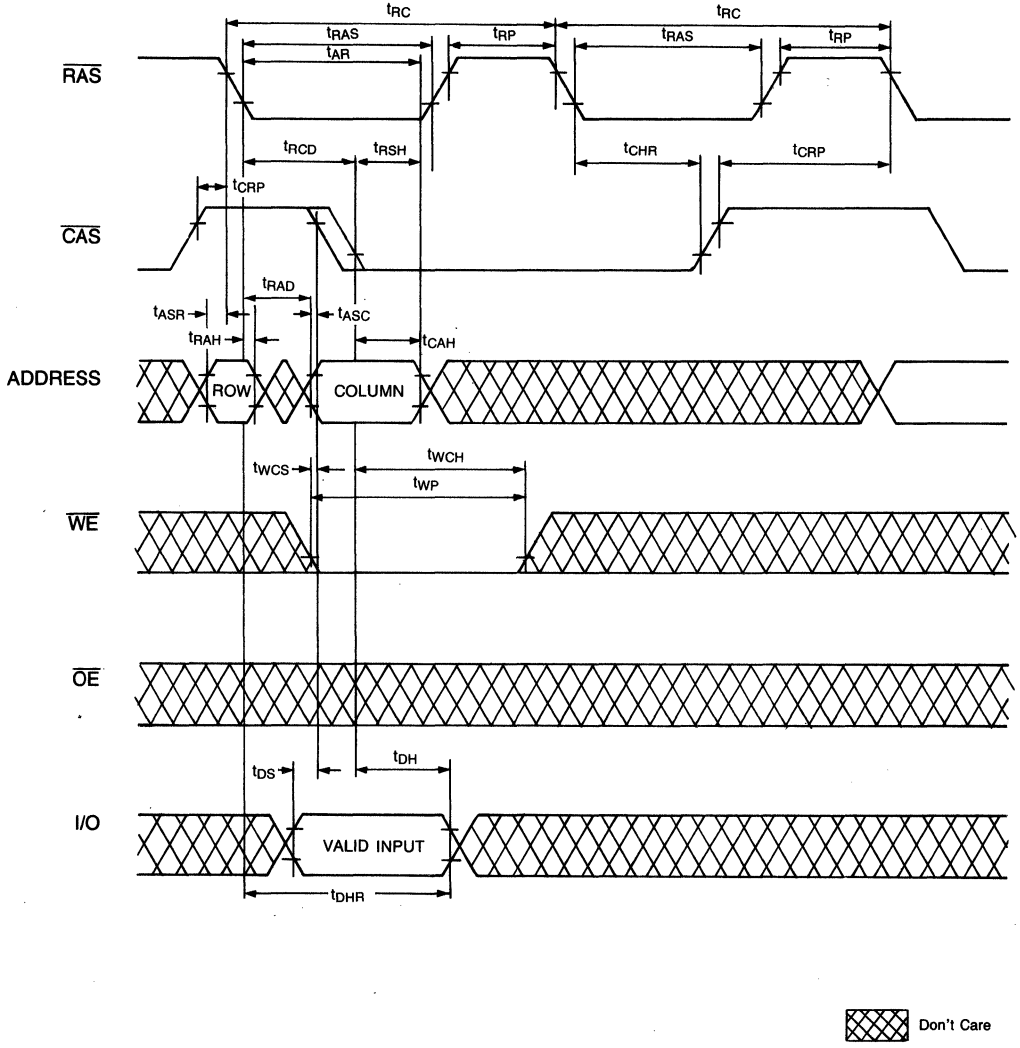


FIGURE 11. HIDDEN REFRESH CYCLE (WRITE)

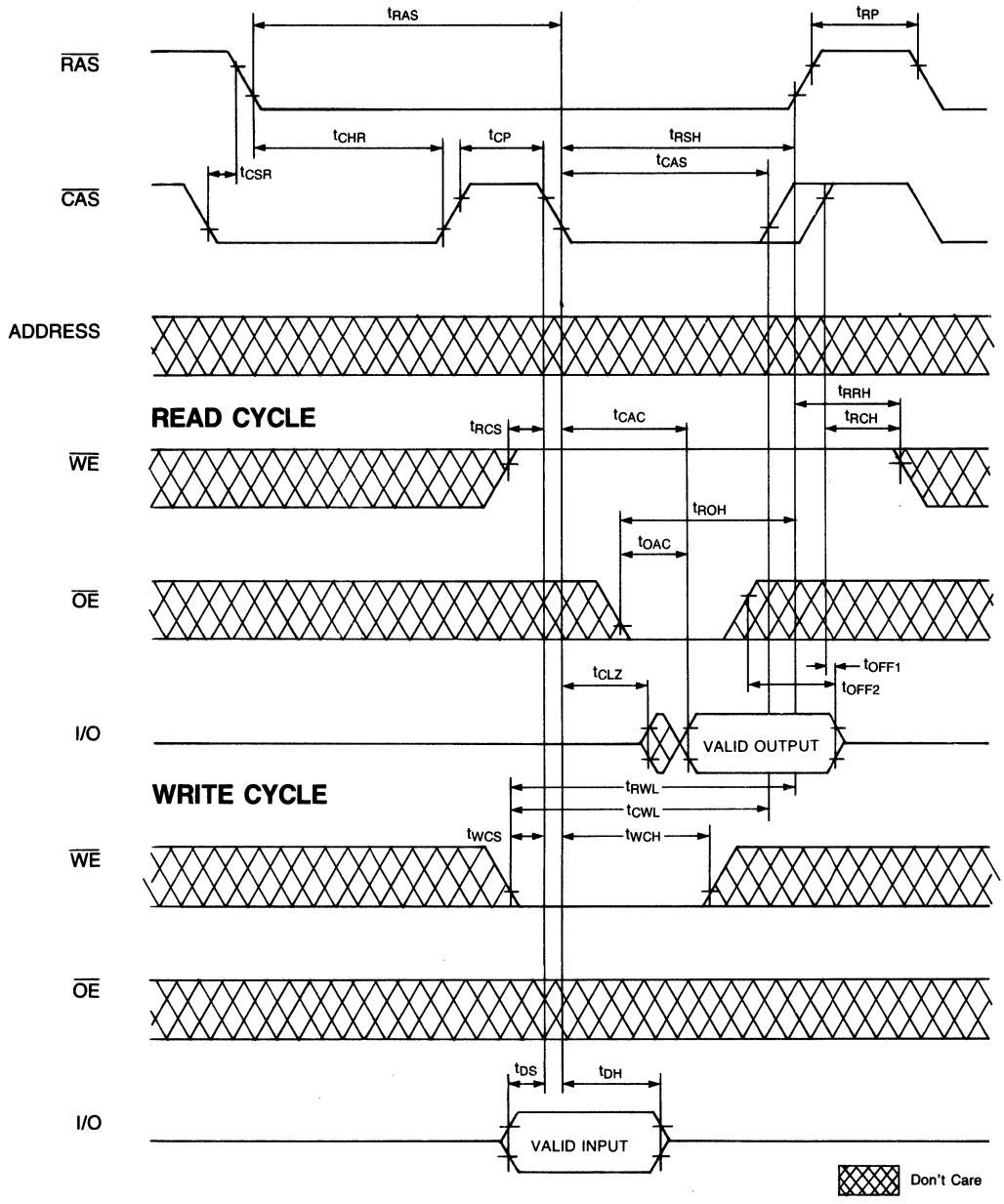
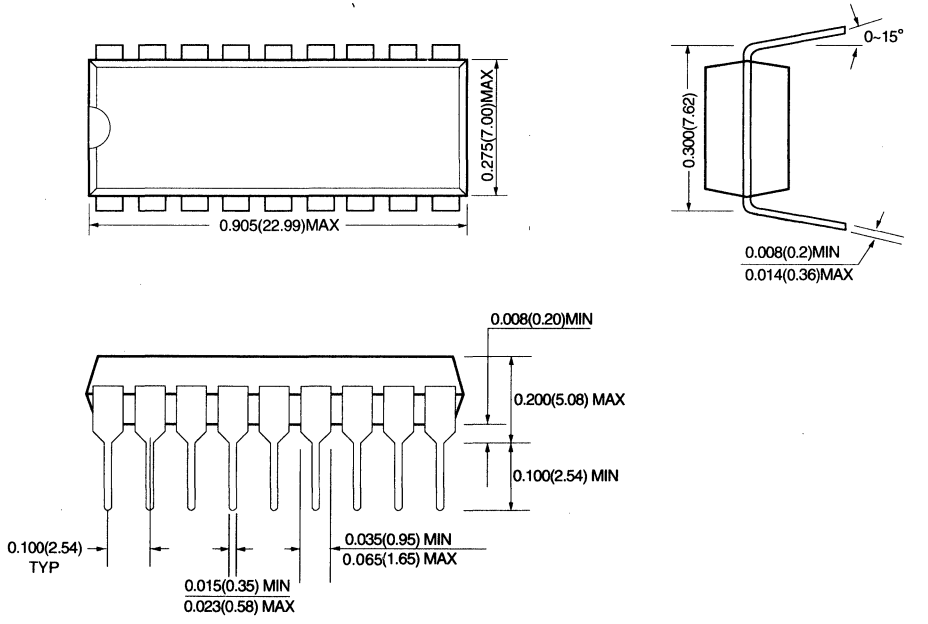


FIGURE 12. $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE

Package Dimensions

18 DIP

Unit: inches (mm)



GM71C1000/L

1,048,576 WORDS×1 BIT
CMOS DYNAMIC RAM

Description

The GM71C1000/L is the new generation dynamic RAM organized 1,048,576×1 Bit. GM71C1000/L has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C1000/L offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71C1000/L to be packaged in a standard 18 pin DIP, 20 pin SOJ and ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

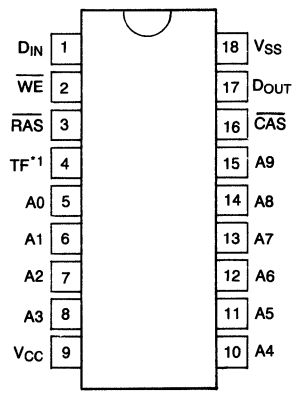
- 1,048,576×1 Bit Organization
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit:ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GM71C1000/L-60	60	20	120	45
GM71C1000/L-70	70	20	130	50
GM71C1000/L-80	80	25	160	55
GM71C1000/L-10	100	25	190	55

- Low Power
  Active: 495/440/385/330mW (MAX)
  Standby: 5.5mW (CMOS level: MAX)
  1.1mW (L-series)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and output TTL Compatible
- 512 Refresh Cycles/8ms
- 512 Refresh Cycles/64ms (L-series)
- Battery Back Up Operation (L-series)

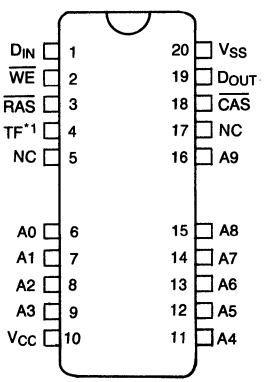
Pin Configuration

18 DIP



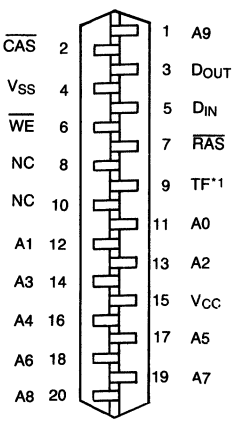
(TOP VIEW)

20 (26) SOJ



(TOP VIEW)

20 ZIP



(BOTTOM VIEW)

Pin Description

Pin	Function	Pin	Function
A0 ~ A9	Address Inputs	D_{IN}	Data Input
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{WE}$	Write Enable	TF*1	Test Function
D_{OUT}	Data Output	NC	No Connection

Note *1. TF pin can be connected with any line or unconnected provided the voltage level of TF pin must be kept lower than V_{CC} + 0.5V.

Ordering Information

Type No.	Access Time	Package
GM71C1000/L-60 GM71C1000/L-70 GM71C1000/L-80 GM71C1000/L-10	60ns 70ns 80ns 100ns	300 Mil 18 Pin Plastic DIP
GM71C1000SJ/LSJ-60 GM71C1000SJ/LSJ-70 GM71C1000SJ/LSJ-80 GM71C1000SJ/LSJ-10	60ns 70ns 80ns 100ns	300 Mil 20 (26) Pin Plastic SOJ
GM71C1000Z/LZ-60 GM71C1000Z/LZ-70 GM71C1000Z/LZ-80 GM71C1000Z/LZ-10	60ns 70ns 80ns 100ns	400 Mil 20 Pin Plastic ZIP

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature (Plastic)	−55 ~ 125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−1.0 ~ 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	−1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	6.5	V
V_{IL}	Input Low Voltage	−2.0	—	0.8	V

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	90	mA	1,2
		70ns	—	80		
		80ns	—	70		
		100ns	—	60		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z)		—	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	—	90	mA	2
		70ns	—	80		
		80ns	—	60		
		100ns	—	50		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	60ns	—	80	mA	1,3
		70ns	—	70		
		80ns	—	50		
		100ns	—	50		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V, D_{OUT} = High-Z)		—	1	mA	
			—	200	μA	4
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	80	mA	
		70ns	—	70		
		80ns	—	60		
		100ns	—	50		
I_{CC7}	Battery Back Up Current Average Power Supply Current, Battery Back Up Mode ($\overline{CAS}$ = $\overline{CAS}$ before $\overline{RAS}$ Cycling or 0.2V, $\overline{WE}$ = V_{CC} − 0.2V or 0.2V, A0 ~ A9 = V_{CC} − 0.2V or 0.2V, D_{IN} = V_{CC} − 0.2V, 0.2V or Open: t_{RC} = 125μs)		—	300	μA	4,5
I_{CC8}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	5	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V)		−10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		−10	10	μA	

Note 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}
4. L Series
5. t_{RAS}(max) = 1μs is applied to refresh of battery back up.

Capacitance (V_{CC}=5V ± 10%, T_A=25°C)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address, D_{IN})	—	5	pF	1
C_{I2}	Input Capacitance (Clocks)	—	7	pF	1
C_O	Data Capacitance (D_{OUT})	—	7	pF	1,2

Note 1. Capacitance is sampled and not 100% tested.
2. $\overline{CAS}$=V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC}=5V±10%, T_A=0 ~70°C, Note 1,14)
Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C1000/L-60		GM71C1000/L-70		GM71C1000/L-80		GM71C1000/L-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	120	—	130	—	160	—	190	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	50	—	70	—	80	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	25	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	12	—	15	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	20	—	20	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	22	55	25	75	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	17	40	20	55	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	20	—	25	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	100	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	10	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	—	8	—	8	—	8	—	8	ms	
	Refresh Period (L-Series)	—	64	—	64	—	64	—	64	ms	

Read Cycle

Symbol	Parameter	GM71C1000/L-60		GM71C1000/L-70		GM71C1000/L-80		GM71C1000/L-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	—	80	—	100	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	20	—	25	—	25	ns	3,4
t_{AA}	Access Time from Column Address	—	30	—	35	—	40	—	45	ns	3,5
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	0	—	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	10	—	10	—	10	—	10	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	45	—	ns	
t_{OFF}	Output Buffer Turn-off Delay Time	—	20	—	20	—	20	—	25	ns	6

Write Cycle

Symbol	Parameter	GM71C1000/L-60		GM71C1000/L-70		GM71C1000/L-80		GM71C1000/L-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	15	—	20	—	20	—	ns	
t_{WP}	Write Command Pulse Width	10	—	10	—	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	20	—	25	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	20	—	25	—	25	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	15	—	20	—	20	—	ns	11

Read-Modify-Write Cycle

Symbol	Parameter	GM71C1000/L-60		GM71C1000/L-70		GM71C1000/L-80		GM71C1000/L-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Write Cycle Time	145	—	155	—	190	—	220	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	60	—	70	—	80	—	100	—	ns	10
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	20	—	20	—	25	—	25	—	ns	10
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	30	—	35	—	40	—	45	—	ns	10

Refresh Cycle

Symbol	Parameter	GM71C1000/L-60		GM71C1000/L-70		GM71C1000/L-80		GM71C1000/L-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	15	—	15	—	20	—	20	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Symbol	Parameter	GM71C1000/L-60		GM71C1000/L-70		GM71C1000/L-80		GM71C1000/L-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	50	—	55	—	55	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	—	10	—	10	—	10	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	100,000	—	100,000	—	100,000	—	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	—	50	—	50	ns	13
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	50	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71C1000/L-60		GM71C1000/L-70		GM71C1000/L-80		GM71C1000/L-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	70	—	75	—	85	—	85	—	ns	

Notes :

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. $t_{OFF}(max)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RCD}(max)$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{CWD}, t_{RWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : if $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle : if $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$ and $t_{AWD} \geq t_{AWD}(min)$, the cycle is a read-write and the data output will contain data read from the selected cell : if neither of the above sets of conditions is satisfied, the condition of the data out(at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or Read-Modify-Write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

TIMING WAVEFORMS

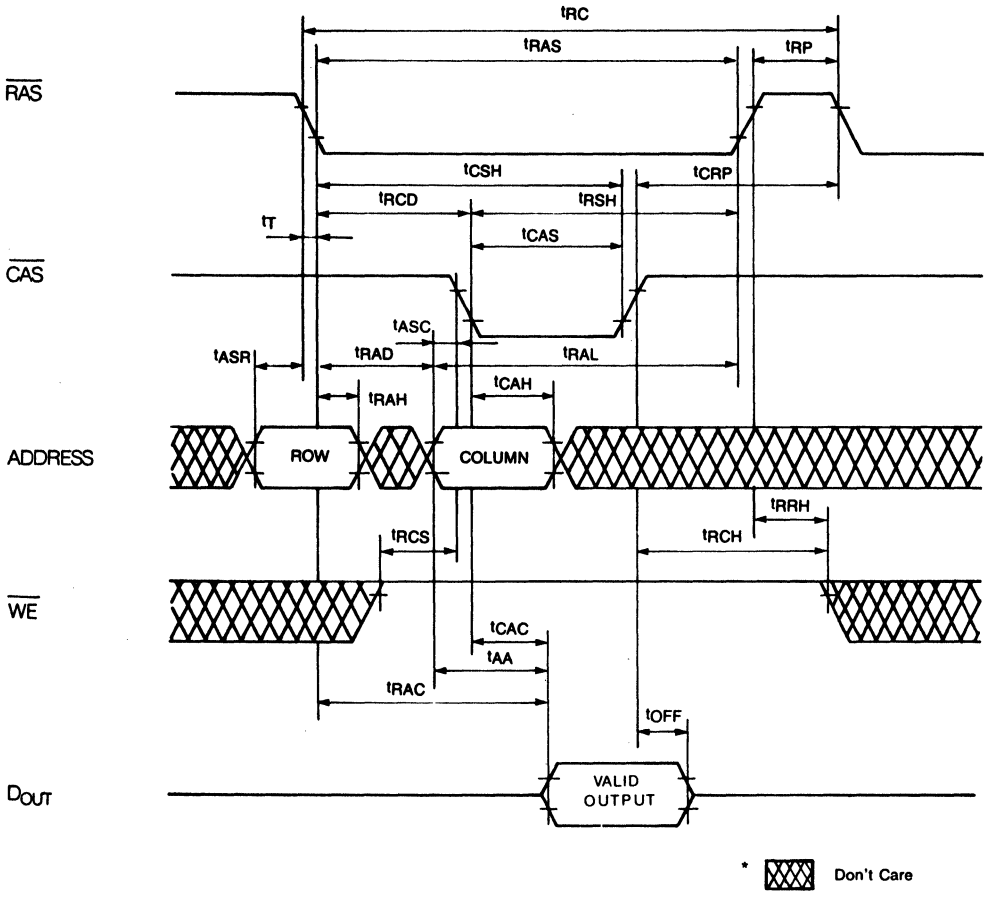


FIGURE 1. READ CYCLE

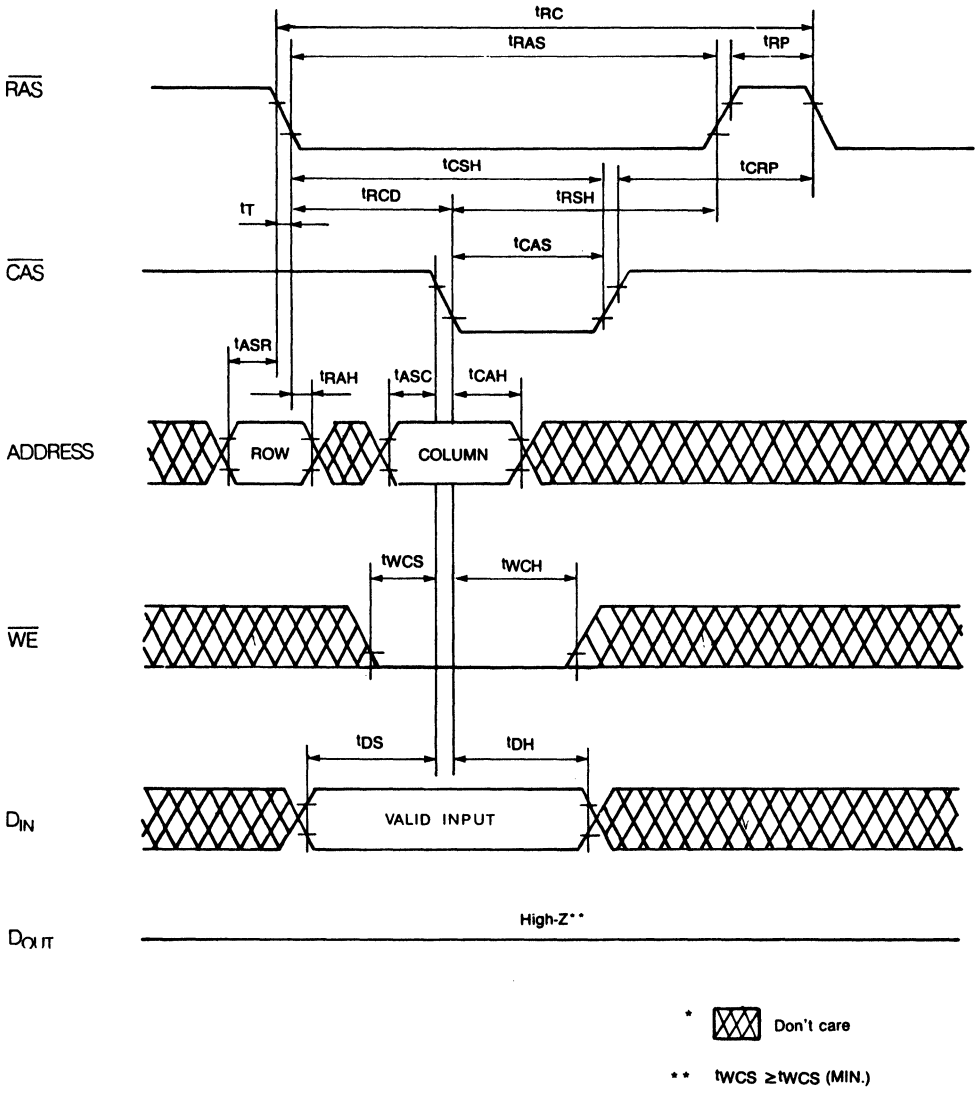


FIGURE 2. EARLY WRITE CYCLE

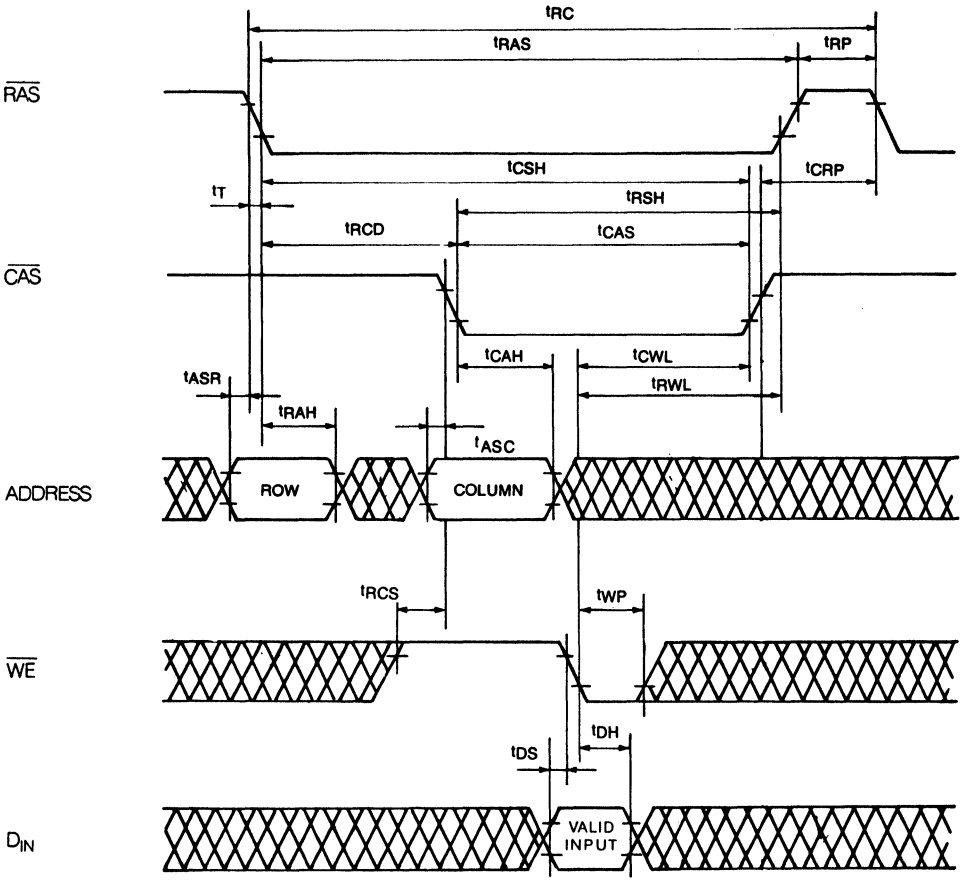


FIGURE 3. DELAYED WRITE CYCLE

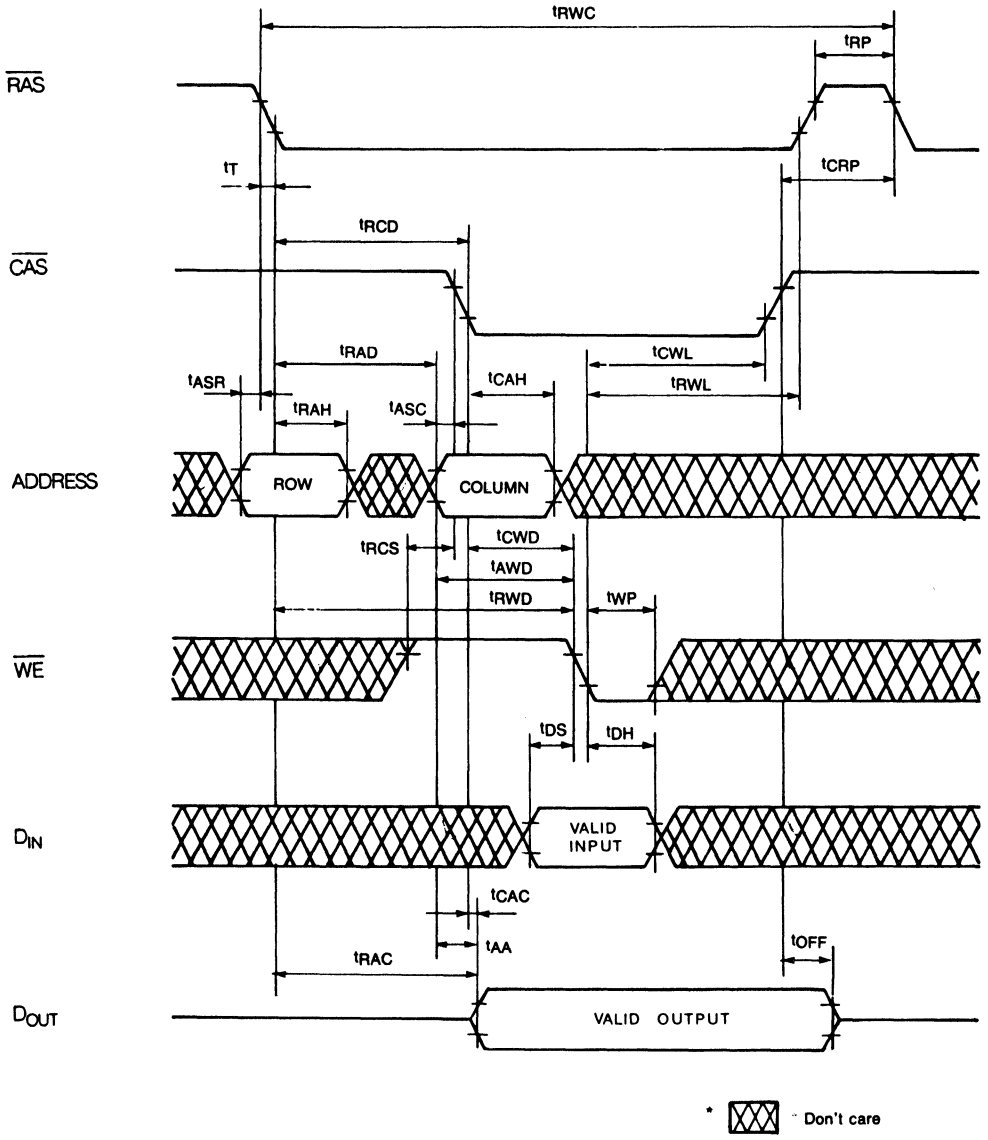


FIGURE 4. READ-MODIFY-WRITE CYCLE

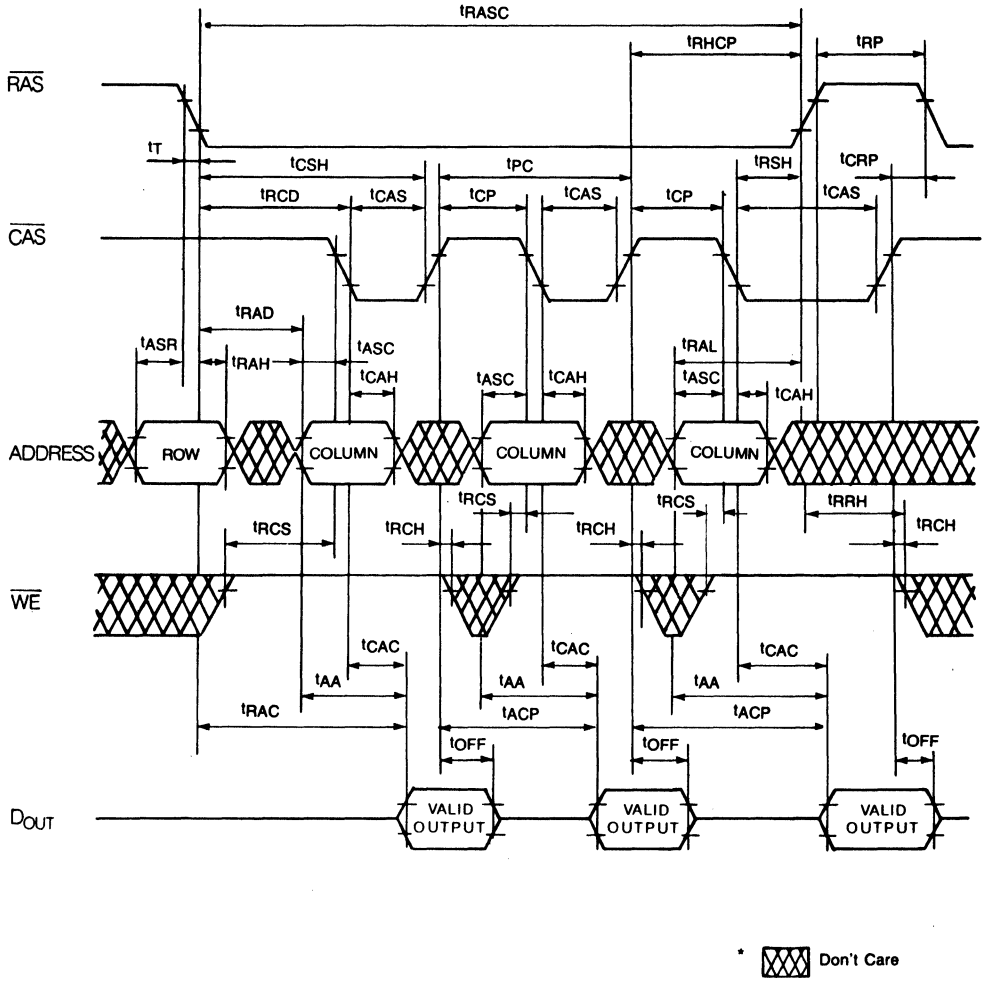


FIGURE 5. FAST PAGE MODE READ CYCLE

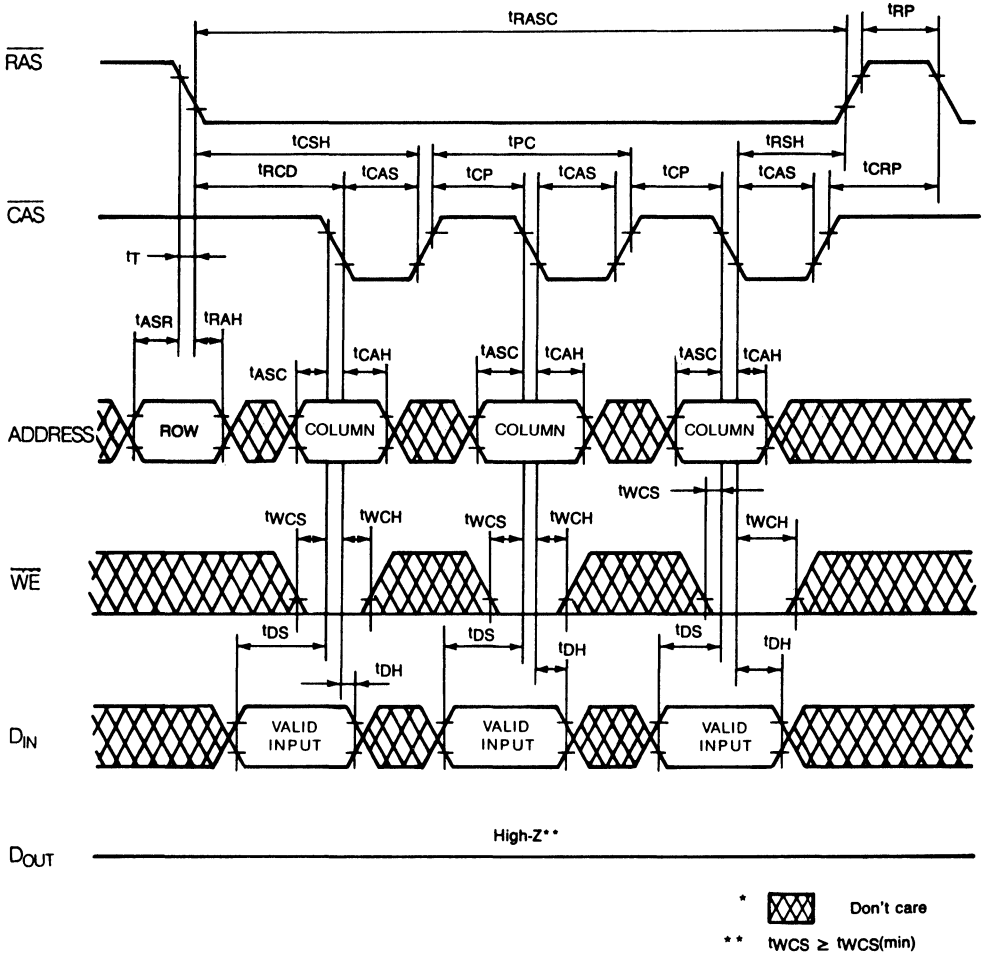


FIGURE 6. FAST PAGE MODE WRITE CYCLE

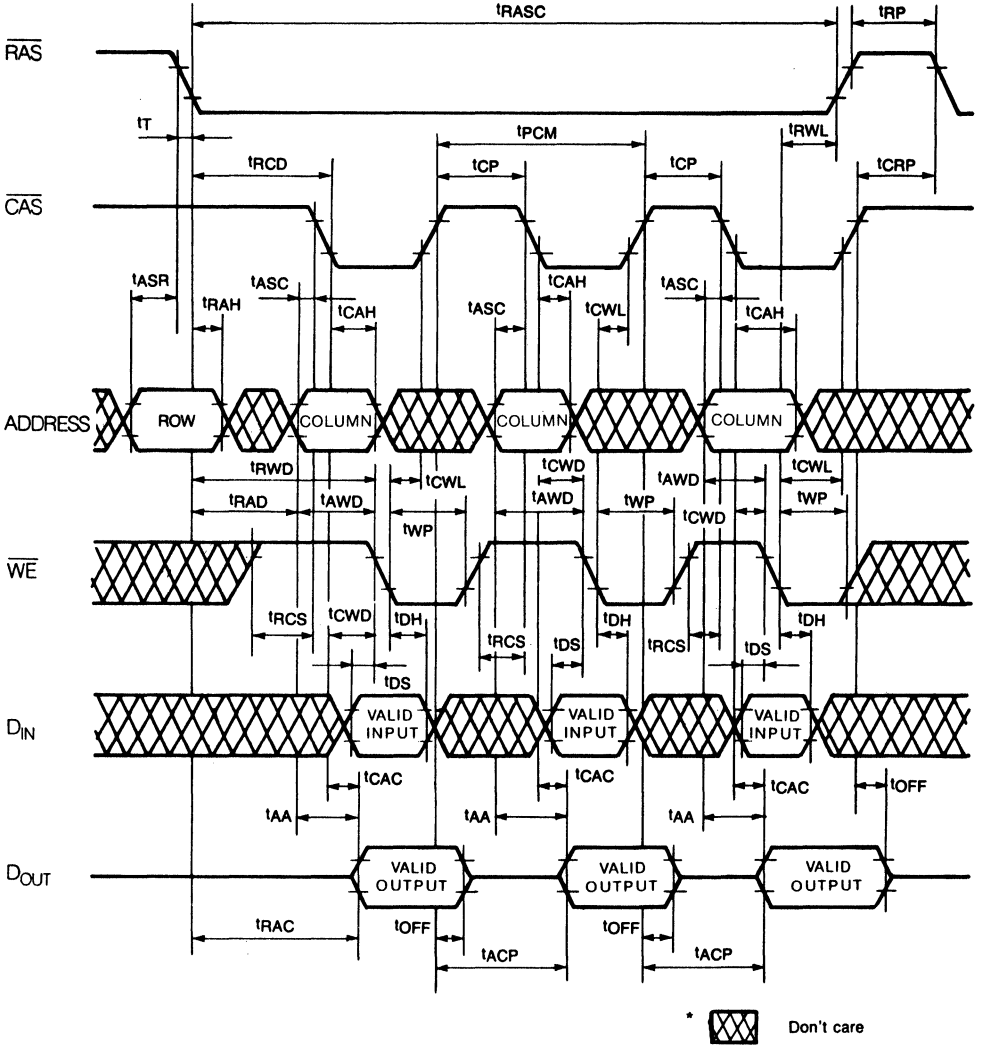


FIGURE 7. FAST PAGE MODE READ-MODIFY-WRITE CYCLE

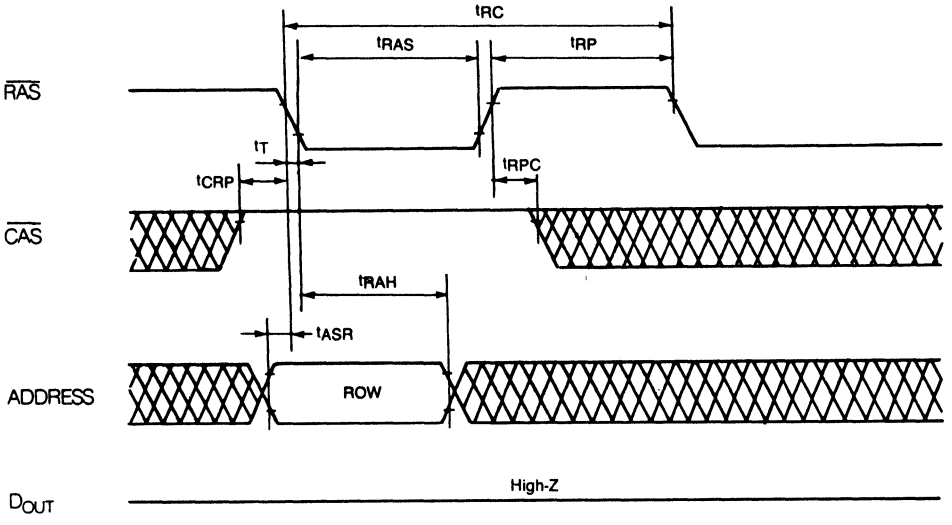


FIGURE 8. RAS-ONLY-REFRESH CYCLE

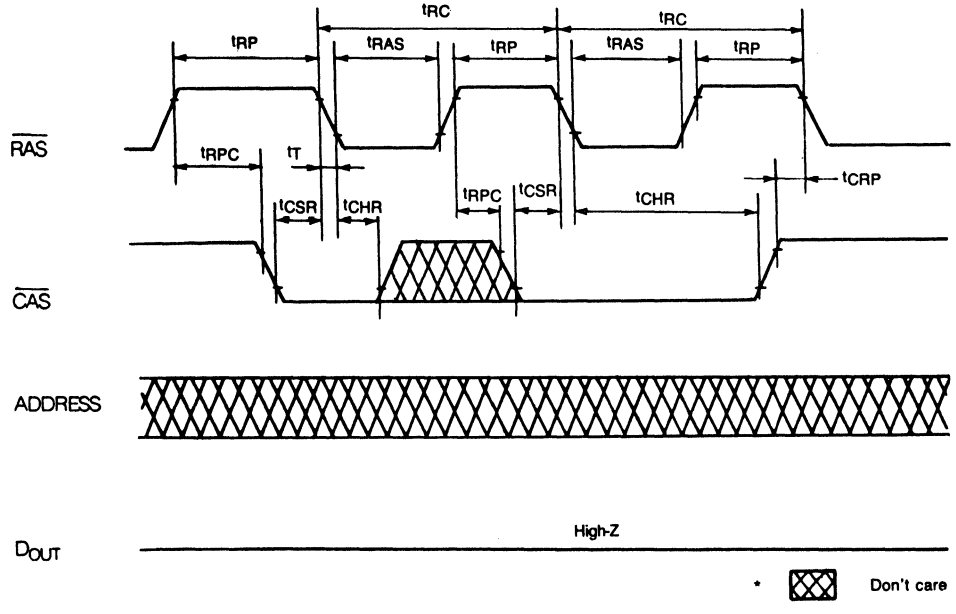


FIGURE 9. CAS BEFORE RAS REFRESH CYCLE

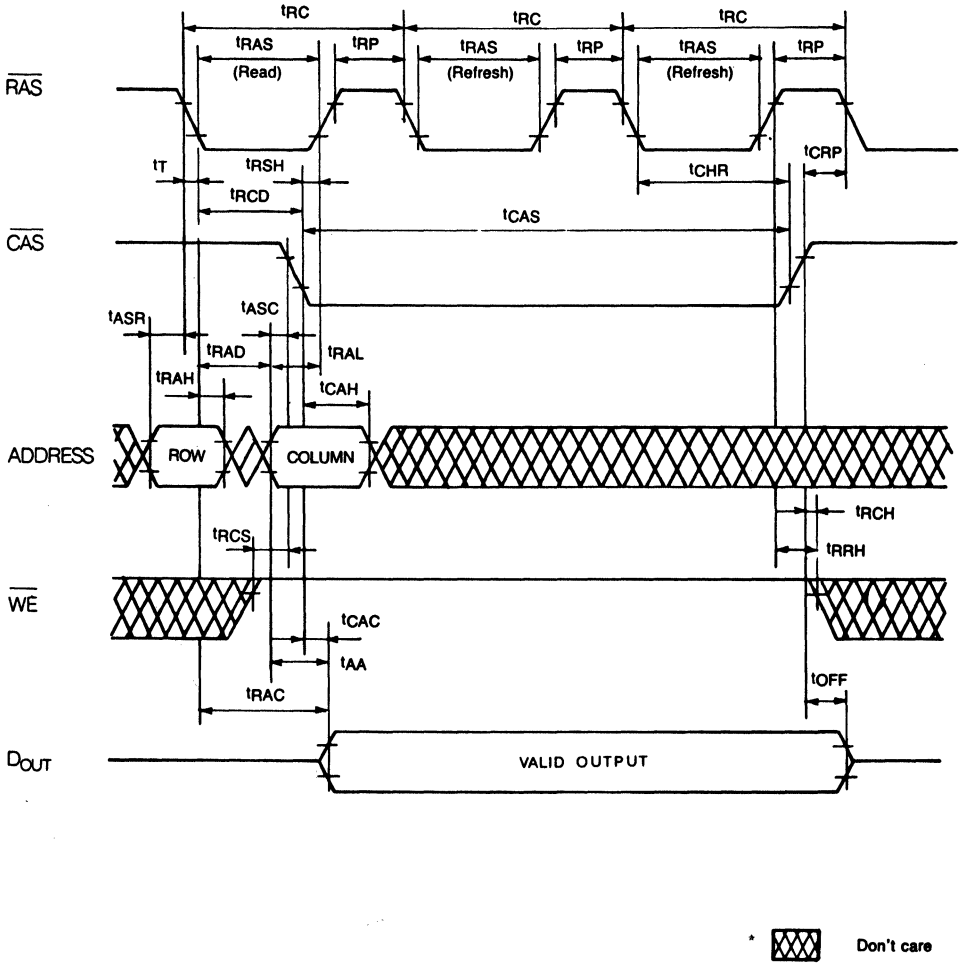
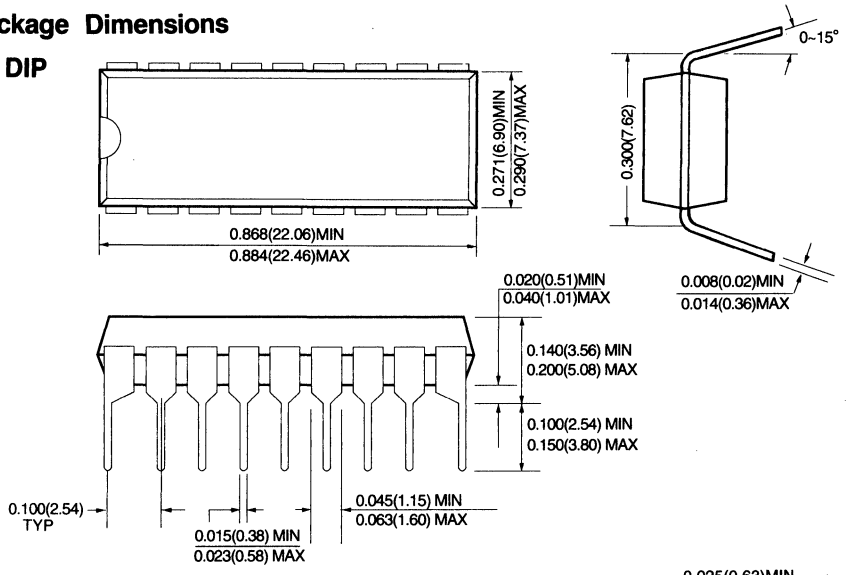


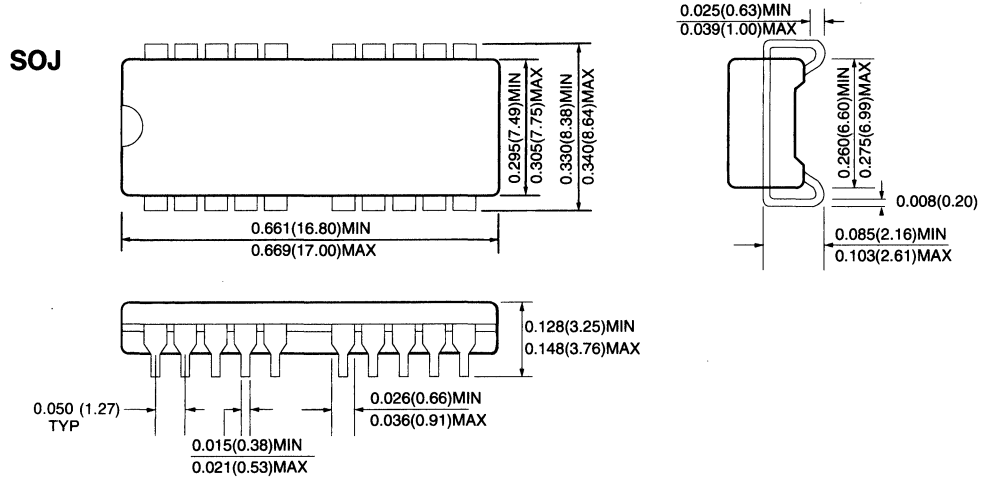
FIGURE 10. HIDDEN REFRESH CYCLE

Package Dimensions

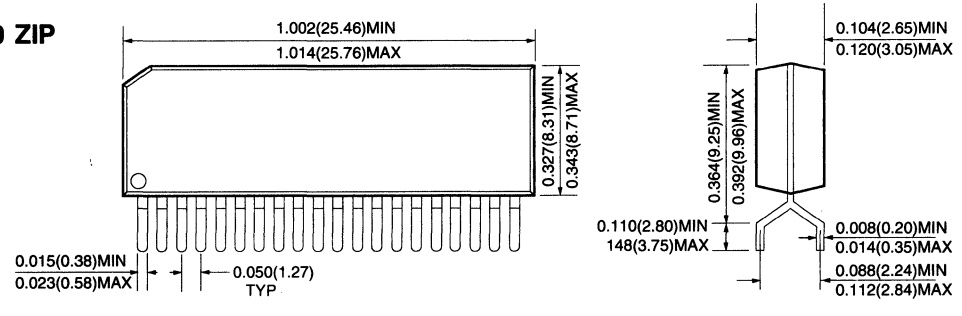
18 DIP



20 SOJ



20 ZIP



GM71C4256A/AL

262,144 WORDS×4 BIT
CMOS DYNAMIC RAM

Description

The GM71C4256A/AL is the new generation dynamic RAM organized 262,144×4 Bit. GM71C-4256A/AL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C-4256A/AL offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71C4256A/AL to be packaged in a standard 20 pin DIP, SOJ and ZIP. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

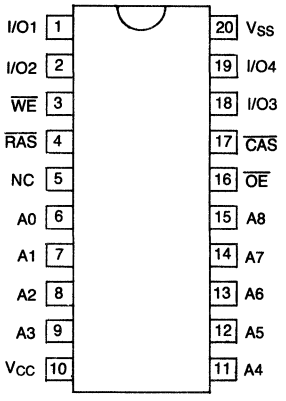
- 262,144×4 Bit Organization
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit:ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GM71C4256A/AL-60	60	20	120	45
GM71C4256A/AL-70	70	20	130	50
GM71C4256A/AL-80	80	25	160	55
GM71C4256A/AL-10	100	25	190	55

- Low Power
  Active: 495/440/385/330mW (MAX)
  Standby: 5.5mW (CMOS level: MAX)
  1.1mW (L-series)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 512 Refresh Cycles/8ms
- 512 Refresh Cycles/64ms (L-series)
- Battery Back Up Operation (L-series)

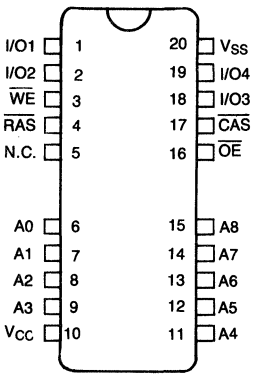
Pin Configuration

20 DIP



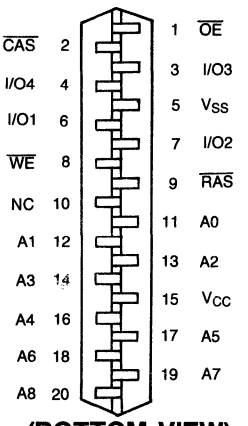
(TOP VIEW)

20(26) SOJ



(TOP VIEW)

20 ZIP



(BOTTOM VIEW)

Pin Description

Pin	Function	Pin	Function
A0 ~ A8	Address Inputs	I/O ~ I/O4	Data Input, Output
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{WE}$	Write Enable	NC	No Connection
$\overline{OE}$	Output Enable		

Ordering Information

Type No.	Access Time	Package
GM71C4256A/AL-60 GM71C4256A/AL-70 GM71C4256A/AL-80 GM71C4256A/AL-10	60ns 70ns 80ns 100ns	300 Mil 20 Pin Plastic DIP
GM71C4256ASJ/ALSJ-60 GM71C4256ASJ/ALSJ-70 GM71C4256ASJ/ALSJ-80 GM71C4256ASJ/ALSJ-10	60ns 70ns 80ns 100ns	300 Mil 20 (26) Pin Plastic SOJ
GM71C4256AZ/ALZ-60 GM71C4256AZ/ALZ-70 GM71C4256AZ/ALZ-80 GM71C4256AZ/ALZ-10	60ns 70ns 80ns 100ns	400 Mil 20 Pin Plastic ZIP

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature (Plastic)	−55 ~ 125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−1.0 ~ 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	−1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	6.5	V
V_{IL}	Input Low Voltage (I/O Pin)	−1.0	—	0.8	V
V_{IL}	Input Low Voltage (Others)	−2.0	—	0.8	V

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	90	mA	1,2
		70ns	—	80		
		80ns	—	70		
		100ns	—	60		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	—	90	mA	2
		70ns	—	80		
		80ns	—	70		
		100ns	—	60		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling: t_{PC} = t_{PC} min)	60ns	—	80	mA	1,3
		70ns	—	70		
		80ns	—	60		
		100ns	—	50		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V)		—	1	mA	
			—	200	μA	4
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	80	mA	
		70ns	—	70		
		80ns	—	70		
		100ns	—	60		
I_{CC7}	Battery Back Up Current Average Power Supply Current, Battery Back Up Mode ($\overline{CAS}$ = CAS before $\overline{RAS}$ Cycling or 0.2V, $\overline{OE}$ = V_{CC} − 0.2V, $\overline{WE}$ = V_{CC} − 0.2V or 0.2V, A0 ~ A8 = V_{CC} − 0.2V or 0.2V, I/O1 ~ 4 = V_{CC} − 0.2V, 0.2V or Open: t_{RC} = 125μs)		—	300	μA	4,5
I_{CC8}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	5	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V) All Other Pins Not Under Test = 0V		−10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		−10	10	μA	

Note 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}
4. L Series
5. t_{RAS}(max) = 1μs is applied to refresh of battery back up.

Capacitance (V_{CC}=5V ± 10%, T_A=25°C)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (A0~A8)	—	5	pF	1
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	—	7	pF	1
$C_{I/O}$	Data Input/Data Output	—	10	pF	1,2

*Note 1. Capacitance is sampled and not 100% tested.
2. $\overline{CAS}$=V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC}=5V±10%, T_A=0~70°C, Note 1,14)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C4256A/AL-60		GM71C4256A/AL-70		GM71C4256A/AL-80		GM71C4256A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	120	—	130	—	160	—	190	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	50	—	70	—	80	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	25	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	12	—	15	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	20	—	20	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	22	55	25	75	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	17	40	20	55	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	20	—	25	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	100	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	10	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	20	—	20	—	20	—	25	—	ns	
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	—	0	—	0	—	0	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	—	8	—	8	—	8	—	8	ms	
	Refresh Period (L-Series)	—	64	—	64	—	64	—	64	ms	

Read Cycle

Symbol	Parameter	GM71C4256A/AL-60		GM71C4256A/AL-70		GM71C4256A/AL-80		GM71C4256A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	—	80	—	100	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	20	—	25	—	25	ns	3,4
t_{AA}	Access Time from Column Address	—	30	—	35	—	40	—	45	ns	3,5
t_{OAC}	Access Time from $\overline{OE}$	—	20	—	20	—	25	—	25	ns	
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	0	—	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	10	—	10	—	10	—	10	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	45	—	ns	
t_{OFF1}	Output Buffer Turn-off Delay Time	—	20	—	20	—	20	—	25	ns	6
t_{OFF2}	Output Buffer Turn-off Delay Time from $\overline{OE}$	—	20	—	20	—	20	—	25	ns	6
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	20	—	20	—	25	—	ns	

Write Cycle

Symbol	Parameter	GM71C4256A/AL-60		GM71C4256A/AL-70		GM71C4256A/AL-80		GM71C4256A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	15	—	20	—	20	—	ns	
t_{WP}	Write Command Pulse Width	10	—	10	—	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	20	—	25	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	20	—	25	—	25	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	15	—	20	—	20	—	ns	11

Read-Modify-Write Cycle

Symbol	Parameter	GM71C4256A/AL-60		GM71C4256A/AL-70		GM71C4256A/AL-80		GM71C4256A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Write Cycle Time	170	—	180	—	220	—	255	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	85	—	95	—	110	—	135	—	ns	10
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	45	—	55	—	60	—	ns	10
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	55	—	60	—	70	—	80	—	ns	10
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	20	—	20	—	25	—	25	—	ns	

Refresh Cycle

Symbol	Parameter	GM71C4256A/AL-60		GM71C4256A/AL-70		GM71C4256A/AL-80		GM71C4256A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	15	—	15	—	20	—	20	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Symbol	Parameter	GM71C4256A/AL-60		GM71C4256A/AL-70		GM71C4256A/AL-80		GM71C4256A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	50	—	55	—	55	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	—	10	—	10	—	10	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	100,000	—	100,000	—	100,000	—	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	—	50	—	50	ns	13
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	50	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71C4256A/AL-60		GM71C4256A/AL-70		GM71C4256A/AL-80		GM71C4256A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	95	—	100	—	110	—	115	—	ns	

Notes :

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}$(max) and $t_{RAD} \leq t_{RAD}$(max).
5. Assumes that $t_{RCD} \leq t_{RCD}$(max) and $t_{RAD} \geq t_{RAD}$(max).
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only: if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : if $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle : if $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min) and $t_{AWD} \geq t_{AWD}$(min), the cycle is a read-write and the data output will contain data read from the selected cell : if neither of the above sets of conditions is satisfied, the condition of the data out(at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or Read-Modify-Write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

TIMING WAVEFORMS

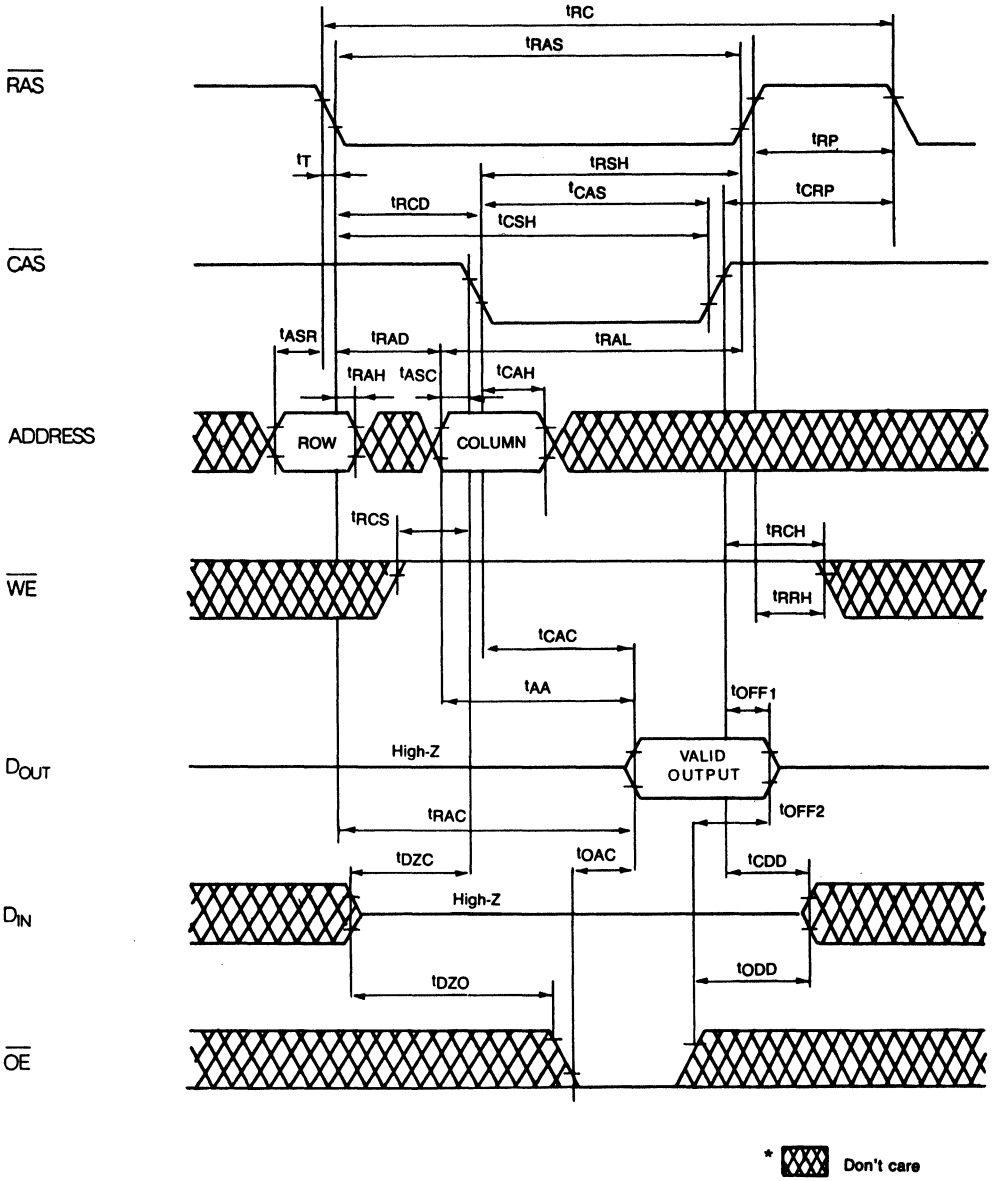


FIGURE 1. READ CYCLE

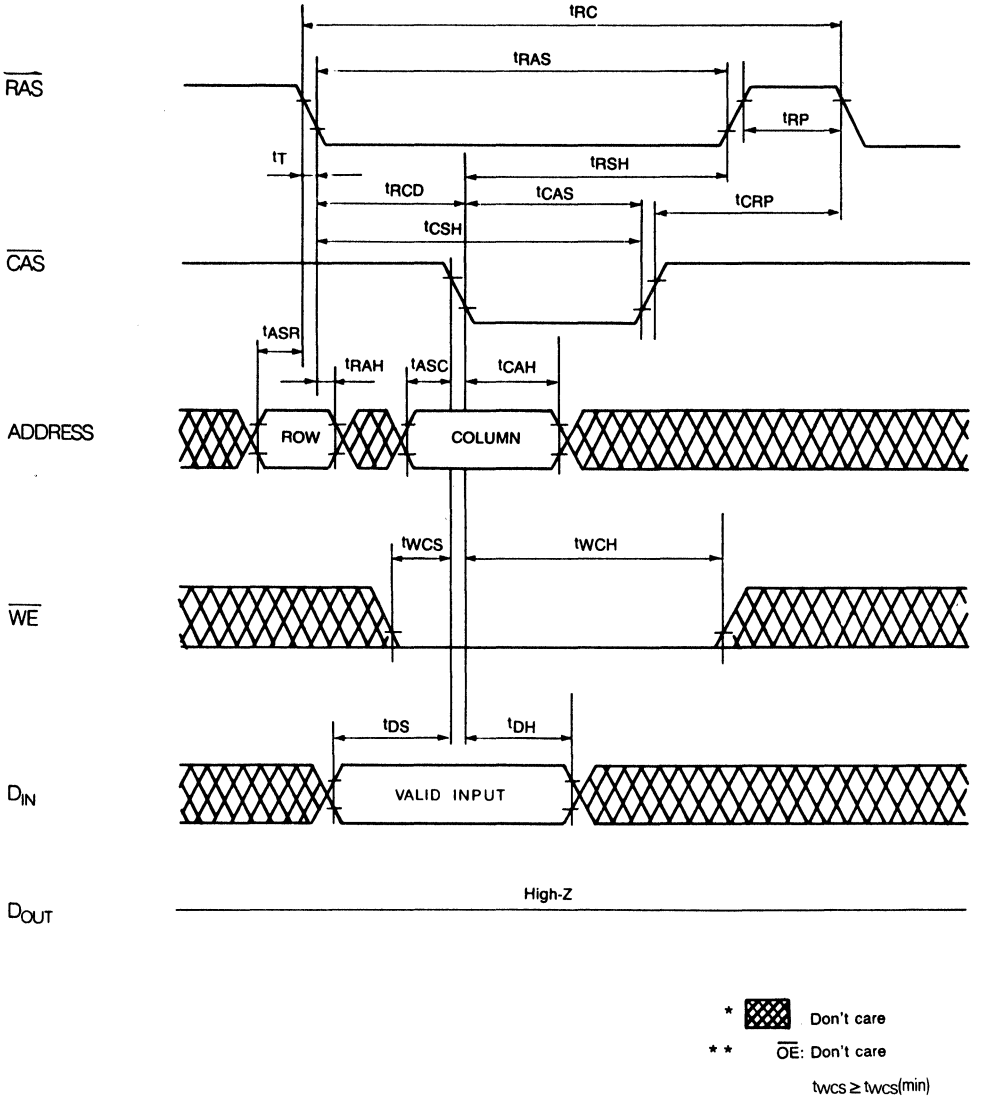


FIGURE 2. EARLY WRITE CYCLE

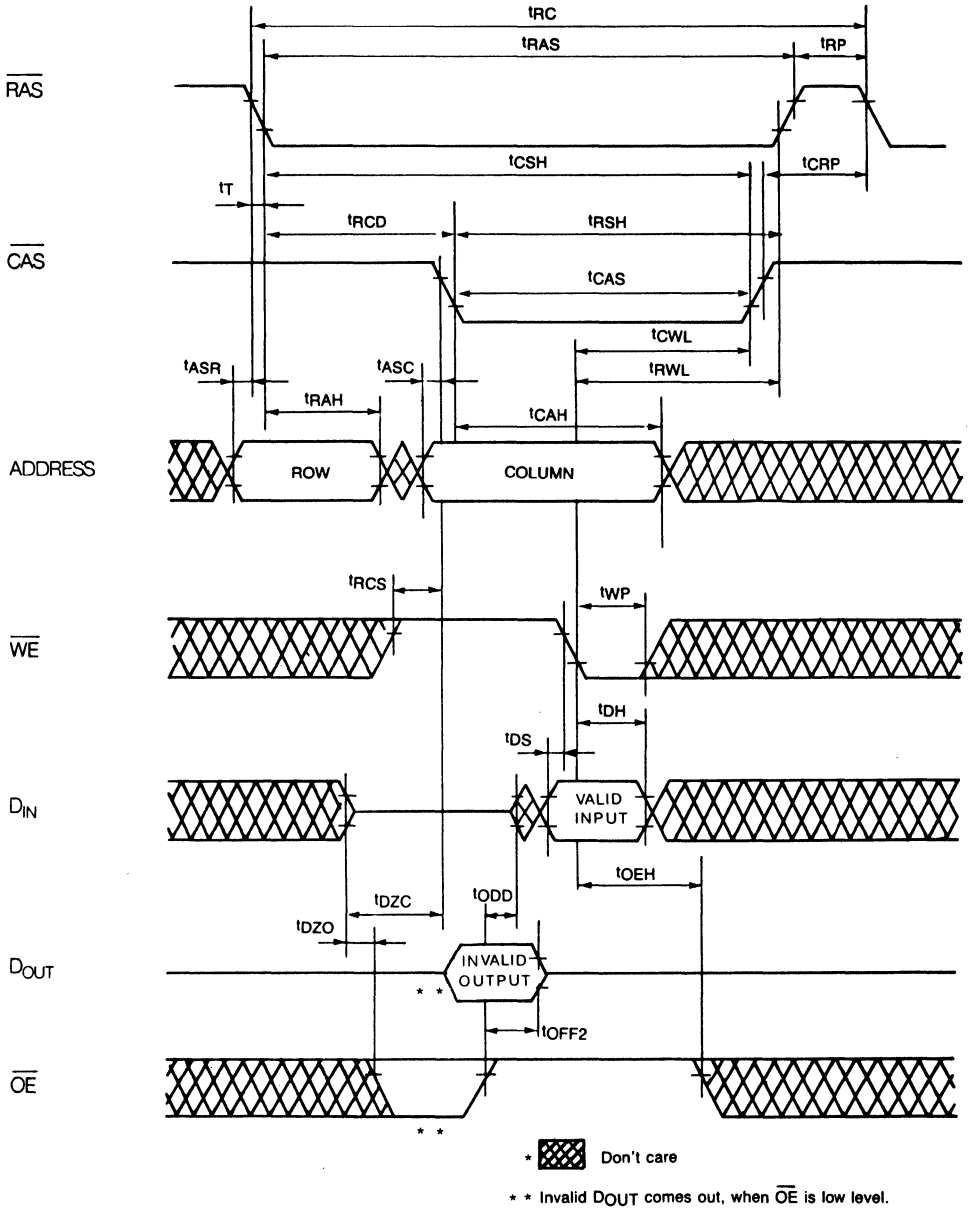


FIGURE 3. DELAYED WRITE CYCLE

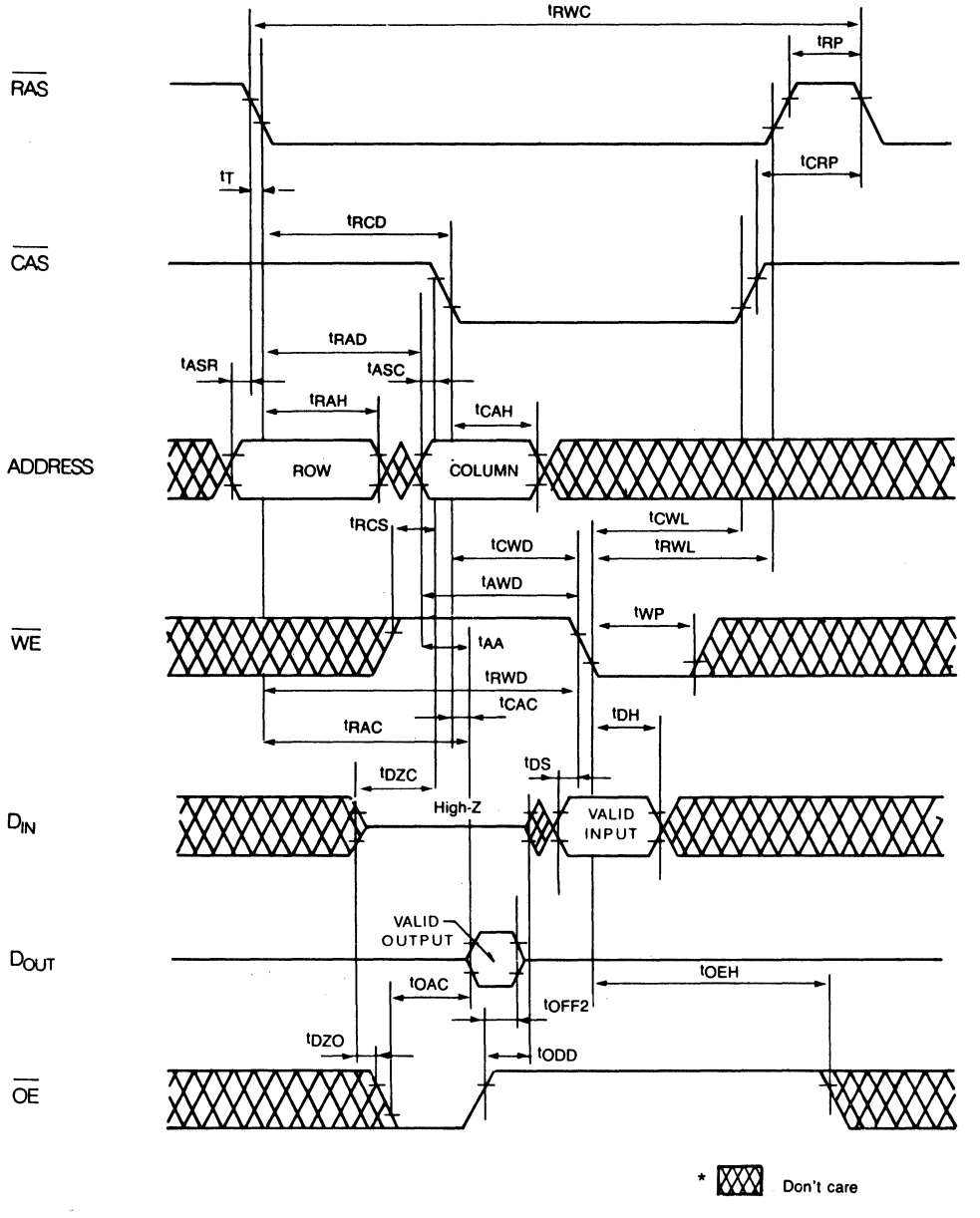


FIGURE 4. READ-MODIFY-WRITE CYCLE

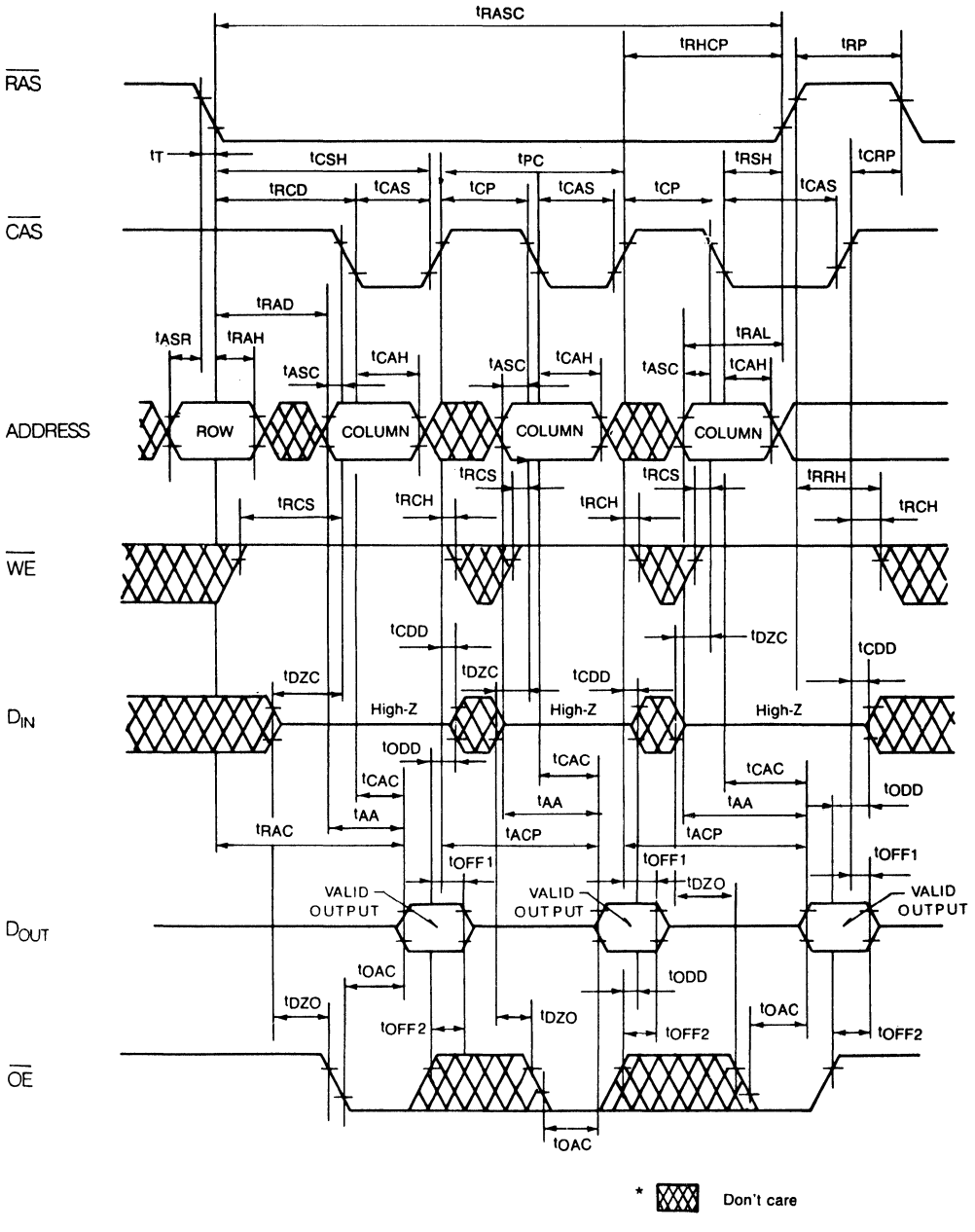


FIGURE 5. FAST PAGE MODE READ CYCLE

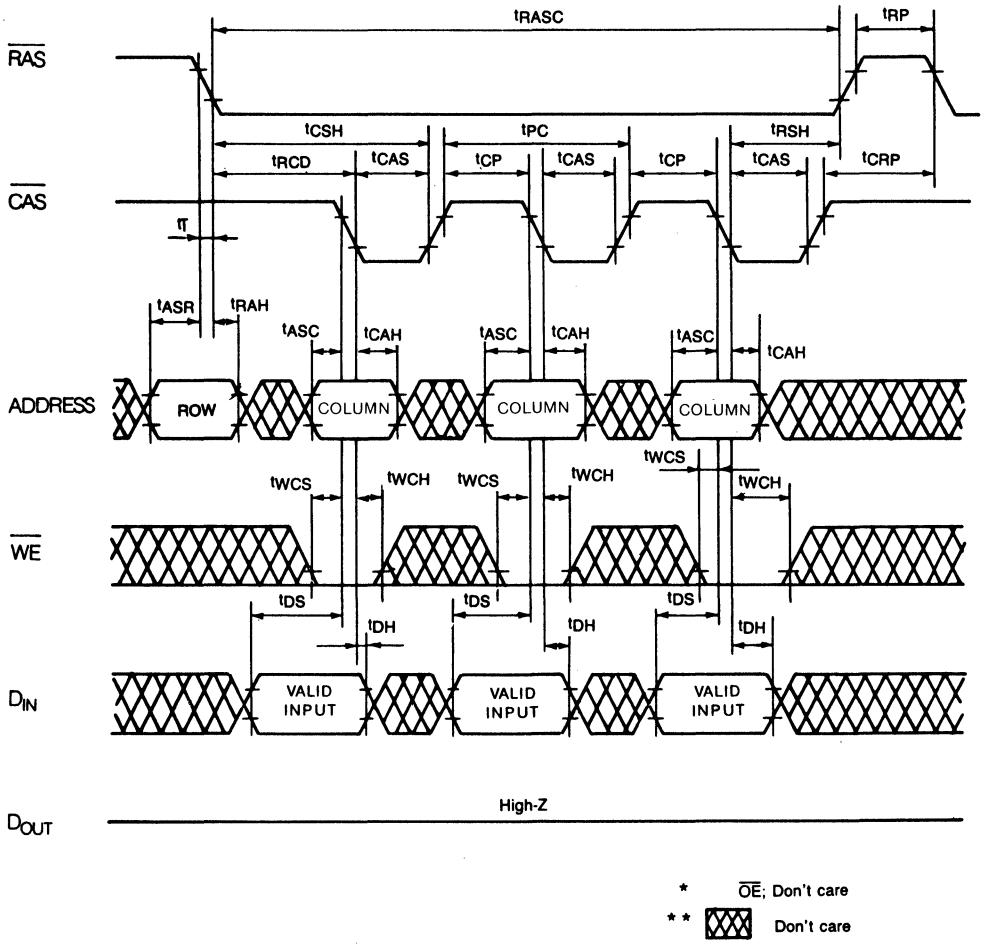


FIGURE 6. FAST PAGE MODE EARLY WRITE CYCLE

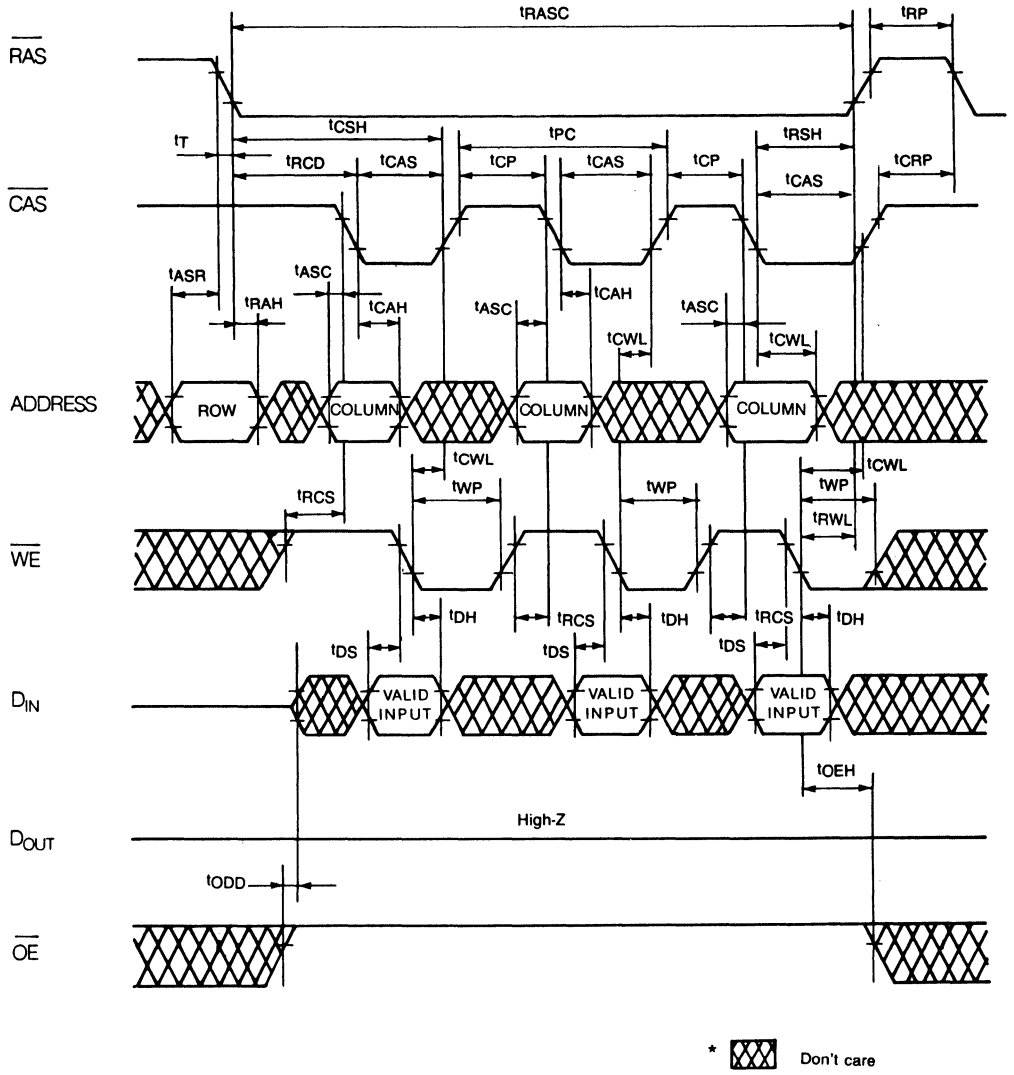


FIGURE 7. FAST PAGE MODE DELAYED WRITE CYCLE

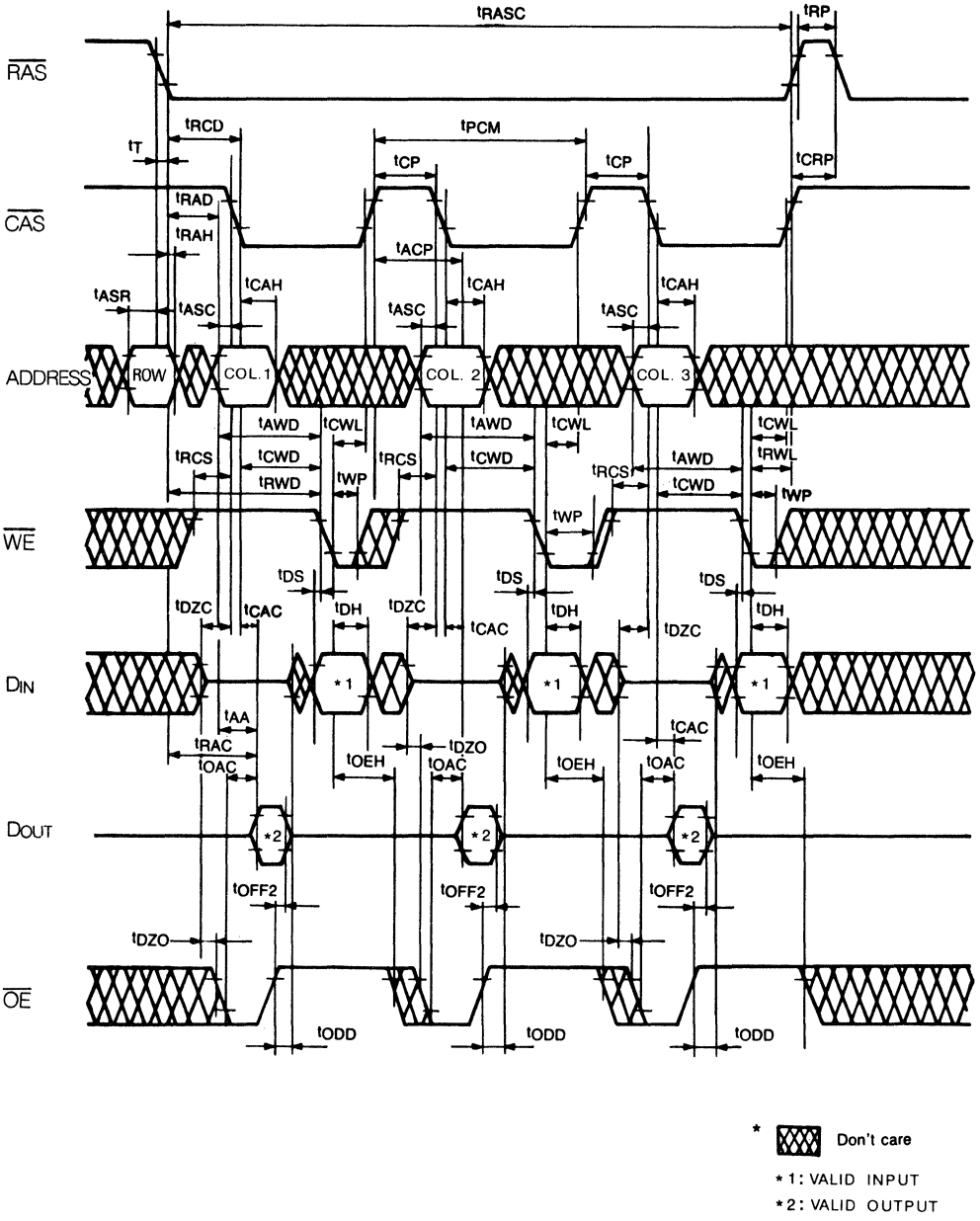


FIGURE 8. FAST PAGE MODE READ-MODIFY-WRITE CYCLE

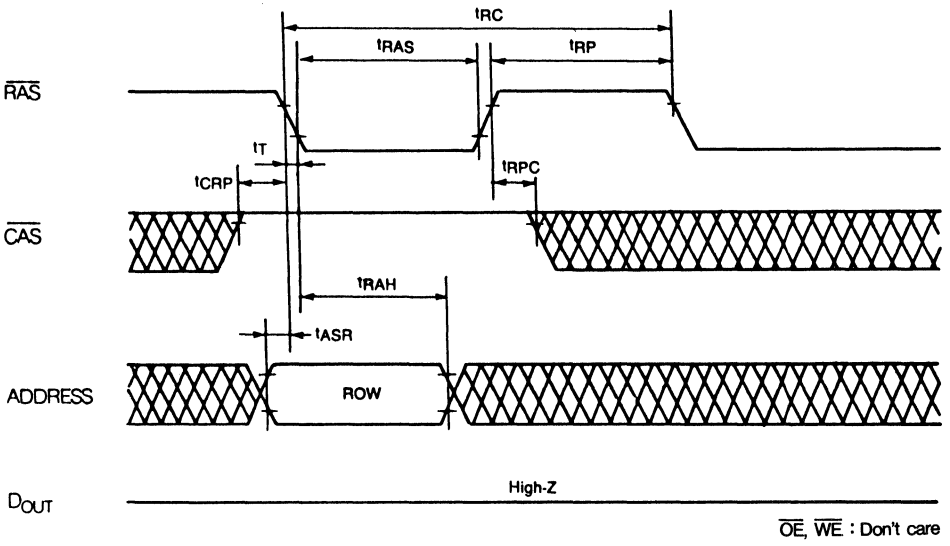


FIGURE 9. RAS-ONLY-REFRESH CYCLE

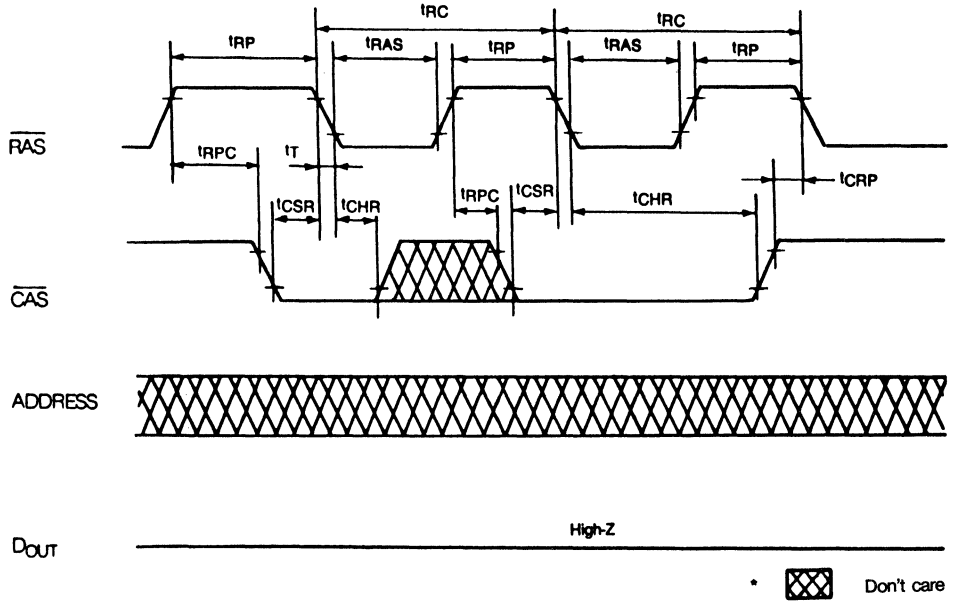


FIGURE 10. CAS BEFORE RAS REFRESH CYCLE

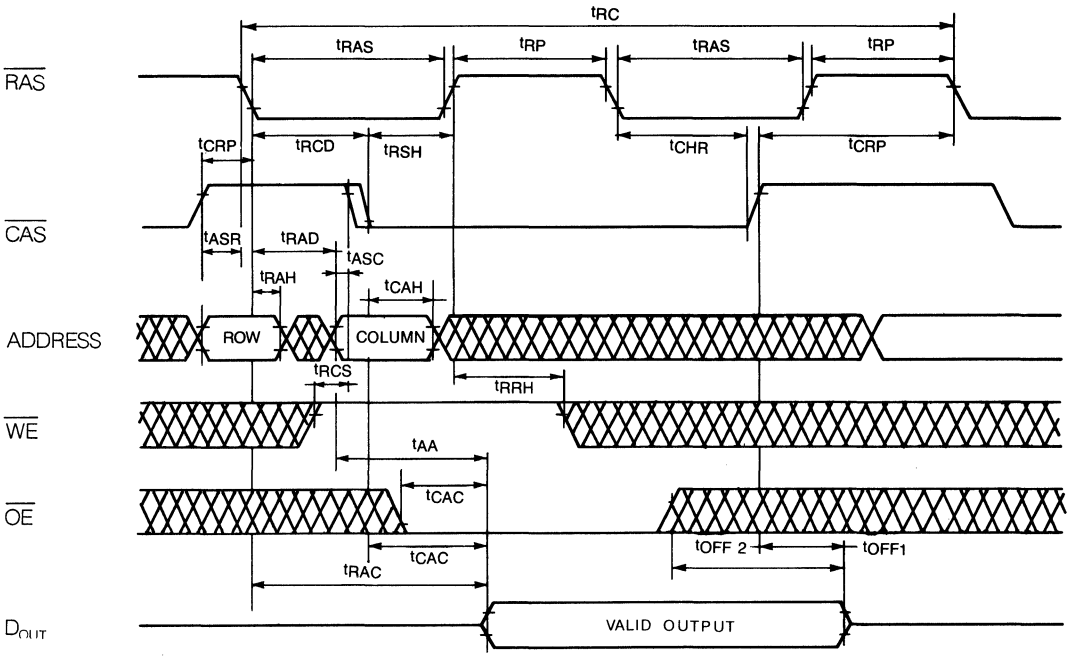


FIGURE 11. HIDDEN REFRESH CYCLE (READ)

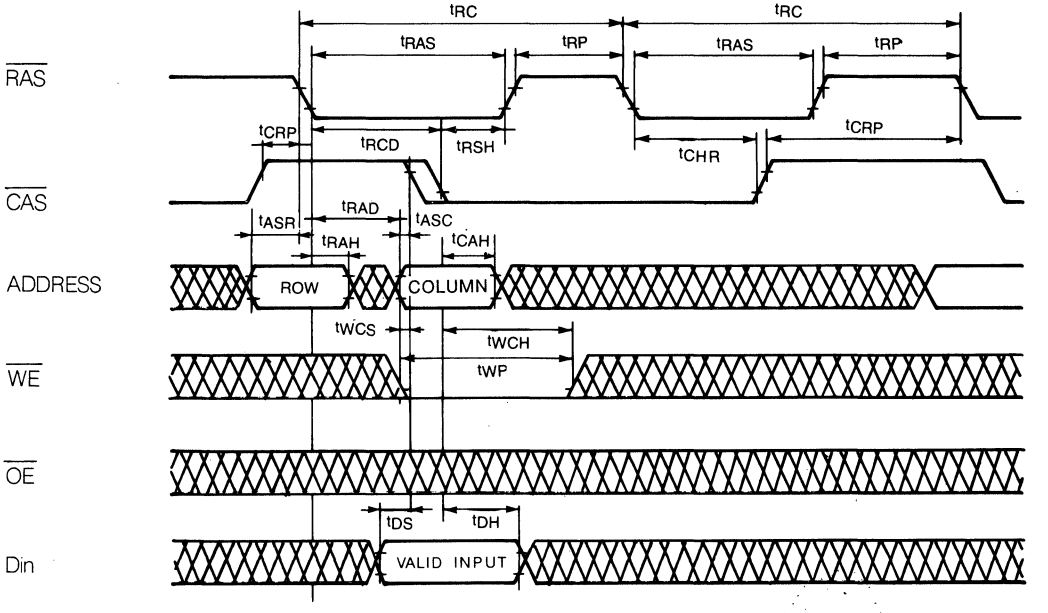
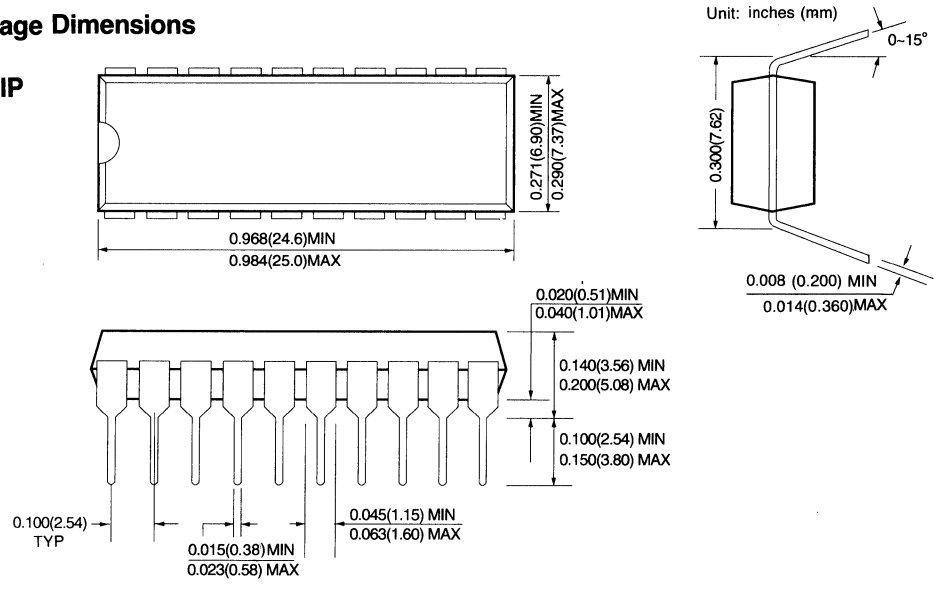


FIGURE 12. HIDDEN REFRESH CYCLE (WRITE)

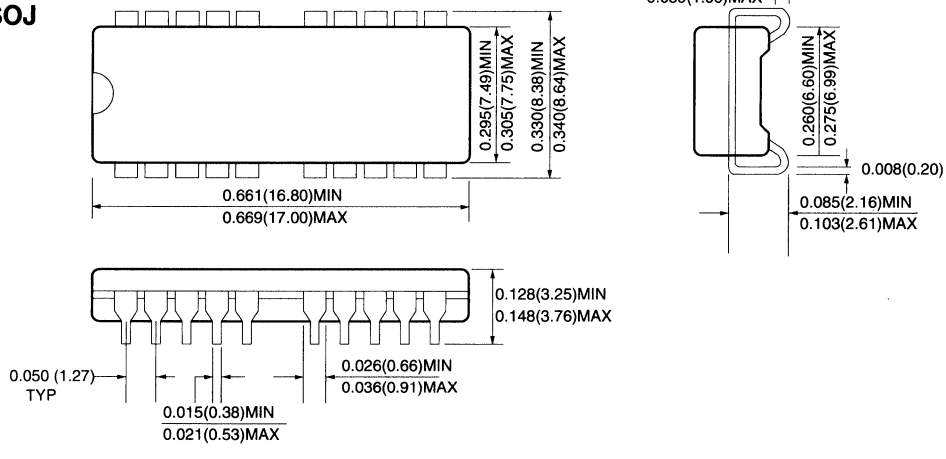
Package Dimensions

Unit: inches (mm)

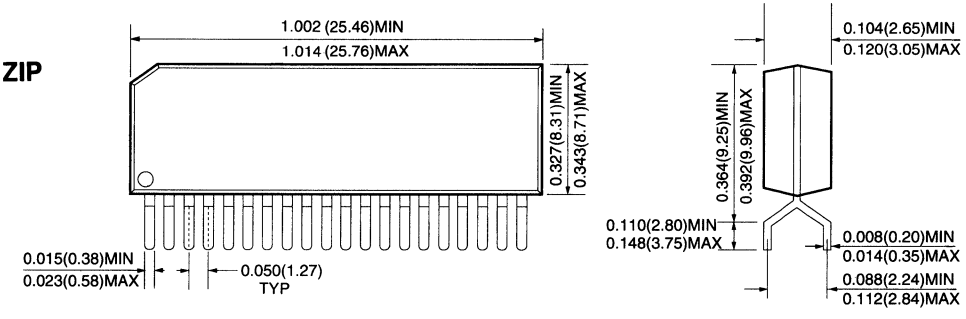
20 DIP



20 SOJ



20 ZIP



GoldStar
GOLDSTAR ELECTRON CO., LTD.

GM71C4100A/AL

4,194,304 WORDS×1 BIT
CMOS DYNAMIC RAM

Description

The GM71C4100A/AL is the new generation dynamic RAM organized 4,194,304×1 Bit. GM71C4100A/AL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C4100A/AL offers Fast Page Mode as a high speed access Mode. Multiplexed address inputs permit the GM71C4100A/AL to be packaged in a standard 300-mil 20-pin plastic SOJ, standard 400-mil 20-pin plastic ZIP, and standard 300-mil 20-pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

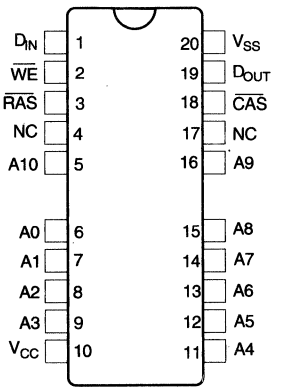
- 4,194,304×1 Bit Organization
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit:ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GM71C4100A/AL-60	60	15	110	40
GM71C4100A/AL-70	70	20	130	45
GM71C4100A/AL-80	80	20	150	50
GM71C4100A/AL-10	100	25	180	55

- Low Power
  Active: 605/550/495/440mW (MAX)
  Standby: 5.5mW (CMOS level:MAX)
  1.1mW (L-series)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and output TTL Compatible
- 1024 Refresh Cycles/16ms
- 1024 Refresh Cycles/128ms (L-series)
- Battery Back Up Operation (L-series)

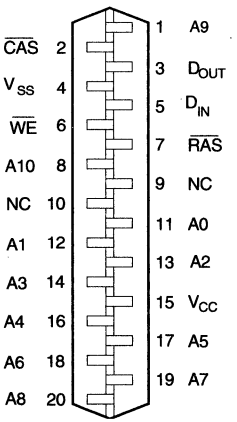
Pin Configuration

20 (26) SOJ



(TOP VIEW)

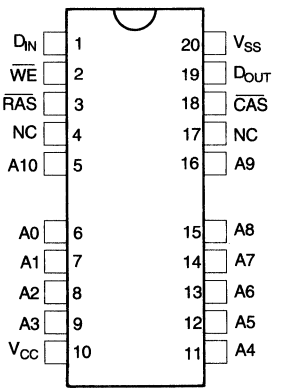
20 ZIP



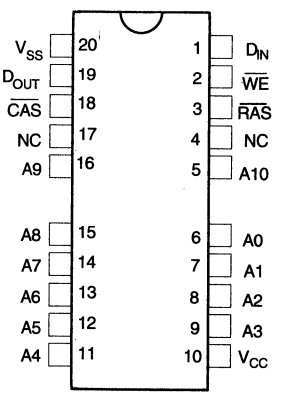
(BOTTOM VIEW)

20 (26) TSOP II

GM71C4100AT/ALT



GMM71C4100AR/ALR



(TOP VIEW)

Pin Description

Pin	Function	Pin	Function
A0~A10	Address Inputs	$\overline{CAS}$	Column Address Strobe
A0~A9	Refresh Address Inputs	$\overline{WE}$	Read/Write Enable
D_{IN}	Data-input	V_{CC}	Power (+5V)
D_{OUT}	Data-output	V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe	NC	No Connect

Ordering Information

Type No.	Access Time	PKG
GM71C4100AJ/ALJ-60 GM71C4100AJ/ALJ-70 GM71C4100AJ/ALJ-80 GM71C4100AJ/ALJ-10	60ns 70ns 80ns 100ns	300 Mil 20 (26) Pin Plastic SOJ
GM71C4100AZ/ALZ-60 GM71C4100AZ/ALZ-70 GM71C4100AZ/ALZ-80 GM71C4100AZ/ALZ-10	60ns 70ns 80ns 100ns	400 Mil 20 Pin Plastic ZIP
GM71C4100AT/ALT-60 GM71C4100AT/ALT-70 GM71C4100AT/ALT-80 GM71C4100AT/ALT-10	60ns 70ns 80ns 100ns	300 Mil 20 (26) Pin Plastic TSOP II (Normal Type)
GM71C4100AR/ALR-60 GM71C4100AR/ALR-70 GM71C4100AR/ALR-80 GM71C4100AR/ALR-10	60ns 70ns 80ns 100ns	300 Mil 20 (26) Pin Plastic TSOP II (Reverse Type)

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0~70	°C
T_{STG}	Storage Temperature (Plastic)	−55~125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−1.0~7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	−1.0~7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended Operating Conditions (T_A=0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	6.5	V
V_{IL}	Input Low Voltage	−2.0	—	0.8	V

DC Electrical Characteristics: (V_{CC}=5V±10%, T_A=0~70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT}=-5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT}=4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC}=t_{RC} min)	60ns	—	110	mA	1,2
		70ns	—	100		
		80ns	—	90		
		100ns	—	80		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$=V_{IH}, D_{OUT}=High-Z)		—	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$=V_{IH}, t_{RC}=t_{RC}min)	60ns	—	110	mA	2
		70ns	—	100		
		80ns	—	90		
		100ns	—	80		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$=V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC}=t_{PC} min)	60ns	—	110	mA	1,3
		70ns	—	100		
		80ns	—	90		
		100ns	—	80		
I_{CC5}	Standby Current (CMOS)		—	1	mA	
	Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$=V_{IH} $\overline{WE}$, Address D_{IN}=V_{IH} or V_{IL}, D_{OUT}=High-Z)		—	200	μA	4,5
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC}=t_{RC} min)	60ns	—	110	mA	
		70ns	—	100		
		80ns	—	90		
		100ns	—	80		
I_{CC7}	Battery Back Up Operating Current (Standby with CBR Refresh) (t_{RC}=125μs, t_{RAS}≤1μs, $\overline{WE}$=V_{IH}, $\overline{CAS}$=V_{IL}, Address and D_{IN}=V_{IH} or V_{IL}, D_{OUT}=High-Z)		—	300	μA	4,5
I_{CC8}	Standby Current $\overline{RAS}$=V_{IH} $\overline{CAS}$=V_{IL} D_{OUT}=Enable		—	5	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V≤V_{IN}≤7V)		-10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V≤V_{OUT}≤7V)		-10	10	μA	

Note) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} (max) is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$=V_{IL}
3. Address can be changed once or less while $\overline{CAS}$=V_{IH}
4. L Series
5. V_{CC}-0.2V≤V_{IH}≤6.5V, 0V≤V_{IL}≤0.2V

Capacitance (V_{CC}=5V ± 10%, T_A=25°C)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address, D_{IN})	—	5	pF	1
C_{I2}	Input Capacitance (Clocks)	—	7	pF	1
C_O	Output Capacitance (D_{OUT})	—	7	pF	1,2

Note 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC}=5V±10%, T_A=0~70°C, Note 1, 12, 15)

Test Conditions: Input rise and fall times: 5ns
Input timing reference levels: 0.8V, 2.4V
Output load: 2TTL Gate + C_L (100 pF) (Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C4100A/AL-60		GM71C4100A/AL-70		GM71C4100A/AL-80		GM71C4100A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	150	—	180	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	60	—	70	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	20	10,000	25	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	10	—	15	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	15	—	20	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	60	25	75	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	55	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	100	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	10	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	—	16	—	16	—	16	—	16	ms	
	Refresh Period (L-Series)	—	128	—	128	—	128	—	128	ms	

Read Cycle

Symbol	Parameter	GM71C4100A/AL-60		GM71C4100A/AL-70		GM71C4100A/AL-80		GM71C4100A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	—	80	—	100	ns	2,3,16
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	—	20	—	25	ns	3,4,14, 16
t_{AA}	Access Time from Column Address	—	30	—	35	—	40	—	45	ns	3,5,14, 16
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	0	—	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	0	—	0	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	45	—	ns	
t_{OFF}	Output Buffer Turn-off Delay Time	0	15	0	20	0	20	0	25	ns	6

Write Cycle

Symbol	Parameter	GM71C4100A/AL-60		GM71C4100A/AL-70		GM71C4100A/AL-80		GM71C4100A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	15	—	15	—	20	—	ns	
t_{WP}	Write Command Pulse Width	10	—	10	—	10	—	20	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	20	—	25	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Symbol	Parameter	GM71C4100A/AL-60		GM71C4100A/AL-70		GM71C4100A/AL-80		GM71C4100A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	130	—	155	—	175	—	210	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	60	—	70	—	80	—	100	—	ns	10
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	15	—	20	—	20	—	25	—	ns	10
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	30	—	35	—	40	—	45	—	ns	10

Refresh Cycle

Symbol	Parameter	GM71C4100A/AL-60		GM71C4100A/AL-70		GM71C4100A/AL-80		GM71C4100A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	10	—	10	—	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time in Normal Mode	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Symbol	Parameter	GM71C4100A/AL-60		GM71C4100A/AL-70		GM71C4100A/AL-80		GM71C4100A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	50	—	55	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	—	10	—	10	—	10	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	100,000	—	100,000	—	100,000	—	100,000	ns	13
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	—	45	—	50	ns	3,14,16
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	45	—	50	—	ns	

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	GM71C4100A/AL-60		GM71C4100A/AL-70		GM71C4100A/AL-80		GM71C4100A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	60	—	70	—	75	—	85	—	ns	
t_{CPW}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	35	—	40	—	45	—	50	—	ns	10

Test Mode Cycle

Symbol	Parameter	GM71C4100A/AL-60		GM71C4100A/AL-70		GM71C4100A/AL-80		GM71C4100A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{WS}	Test Mode $\overline{WE}$ Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{WH}	Test Mode $\overline{WE}$ Hold Time	10	—	10	—	10	—	10	—	ns	

Counter Test Cycle

Symbol	Parameter	GM71C4100A/AL-60		GM71C4100A/AL-70		GM71C4100A/AL-80		GM71C4100A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{CPT}	$\overline{CAS}$ Precharge Time in Counter Test Cycle	40	—	40	—	40	—	50	—	ns	

Notes :

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RCD}(max)$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : if $t_{WCS} \geq t_{WCS}(min)$ the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle ; if $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$ and $t_{CPW} \geq t_{CPW}(min)$, the cycle is a read modify write and the data output will contain data read from the selected cell: if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or a read modify write cycle.
12. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycels ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
13. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
14. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
15. Test mode operation specified in this data sheet is 8 bit test function controlled by control address bits — RA10, CA10 and CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of eight test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. Data output pin is D_{OUT} and data input pin is D_{IN}. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
16. In a test mode read cycle, the value of t_{RAC}, T_{AA}, t_{CAC} and t_{ACP} is delayed for 2nd to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

TIMING WAVEFORMS

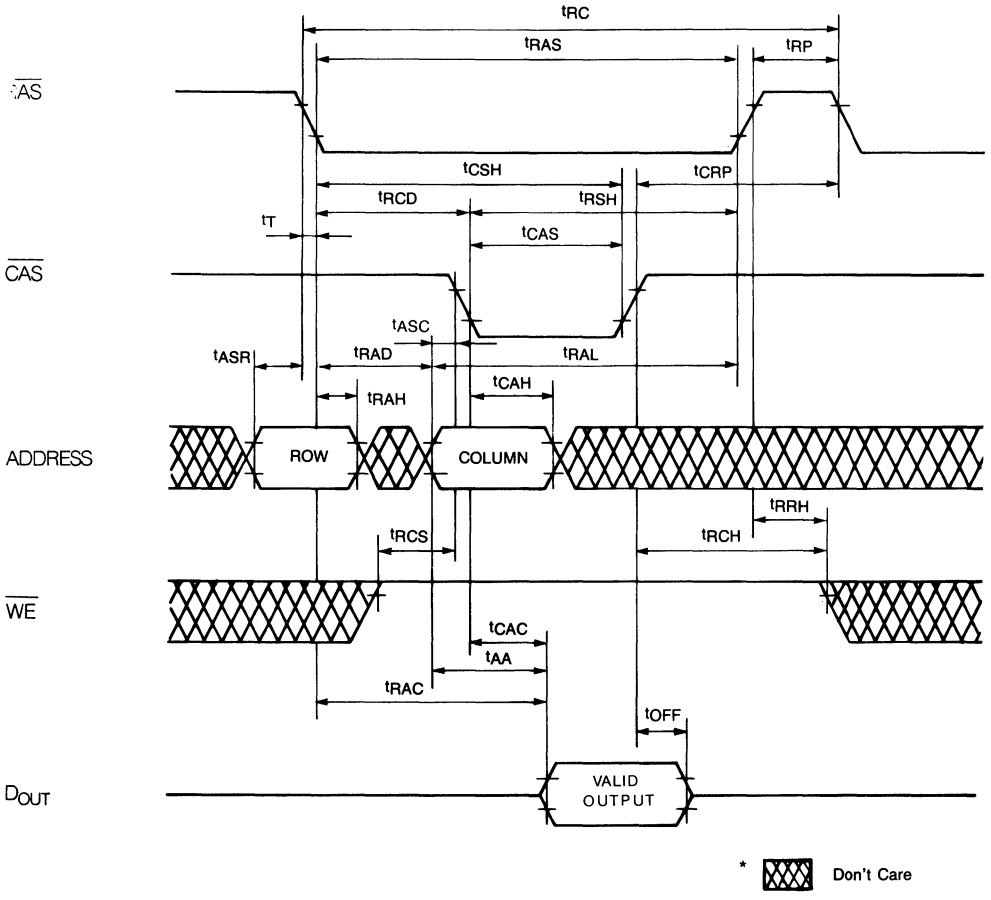


FIGURE 1. READ CYCLE

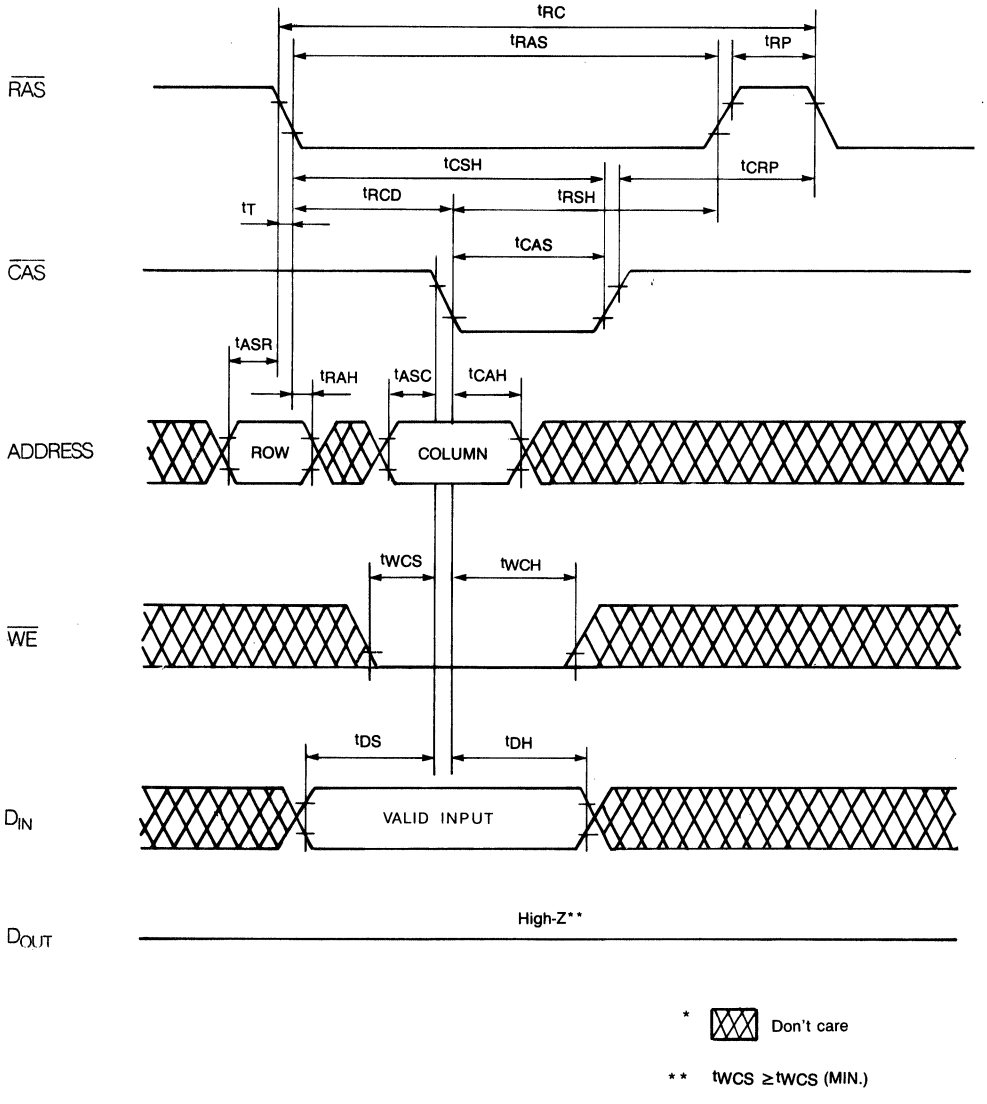


FIGURE 2. EARLY WRITE CYCLE

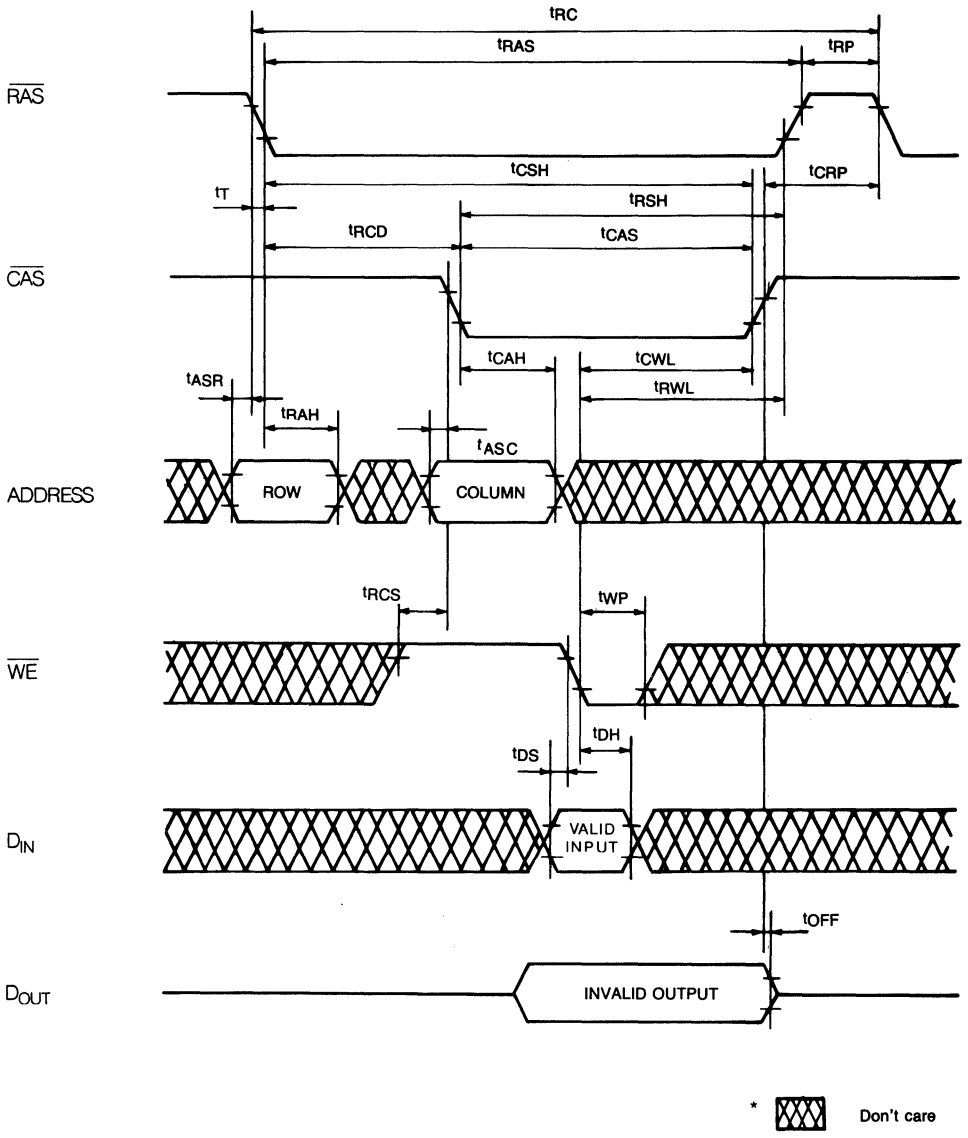


FIGURE 3. DELAYED WRITE CYCLE

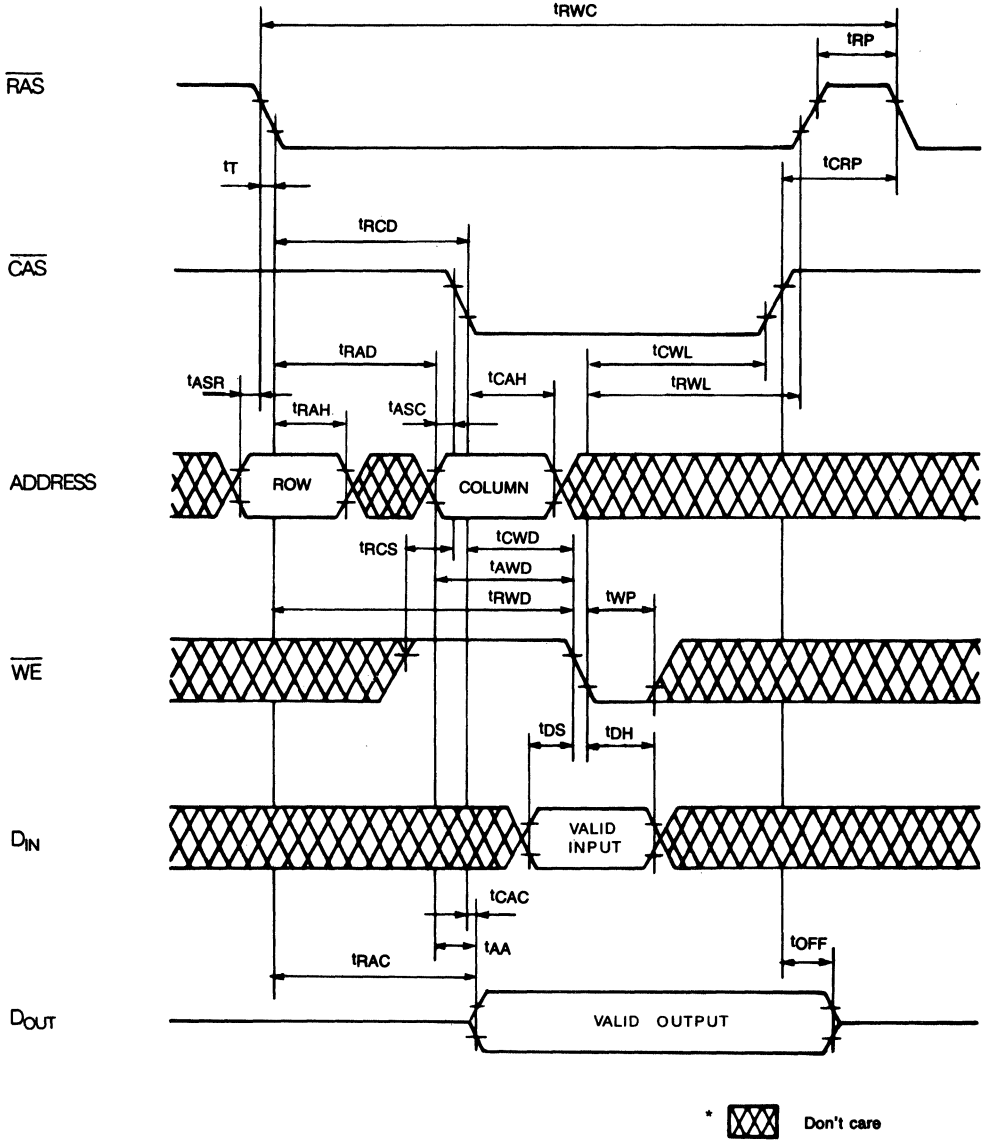


FIGURE 4. READ-MODIFY-WRITE CYCLE

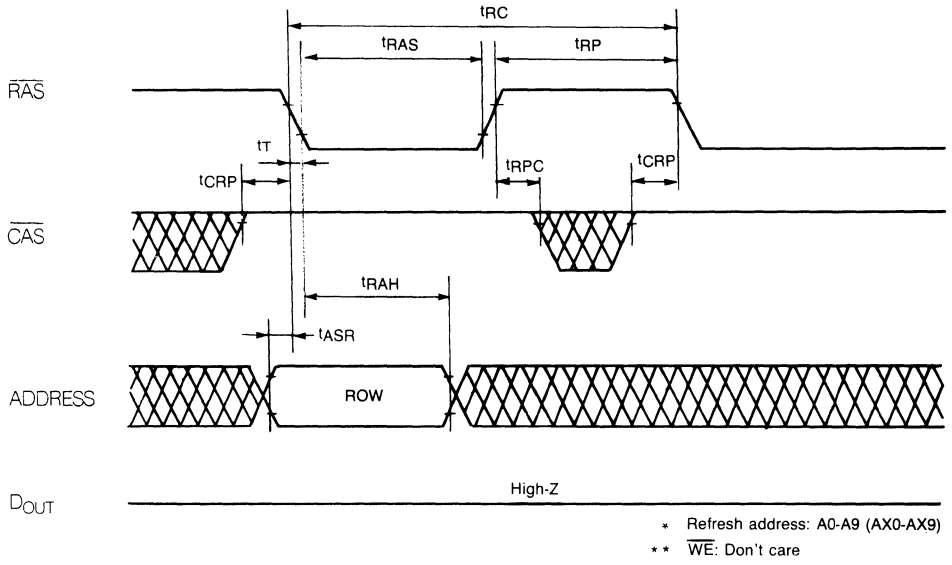


FIGURE 5. RAS-ONLY-REFRESH CYCLE

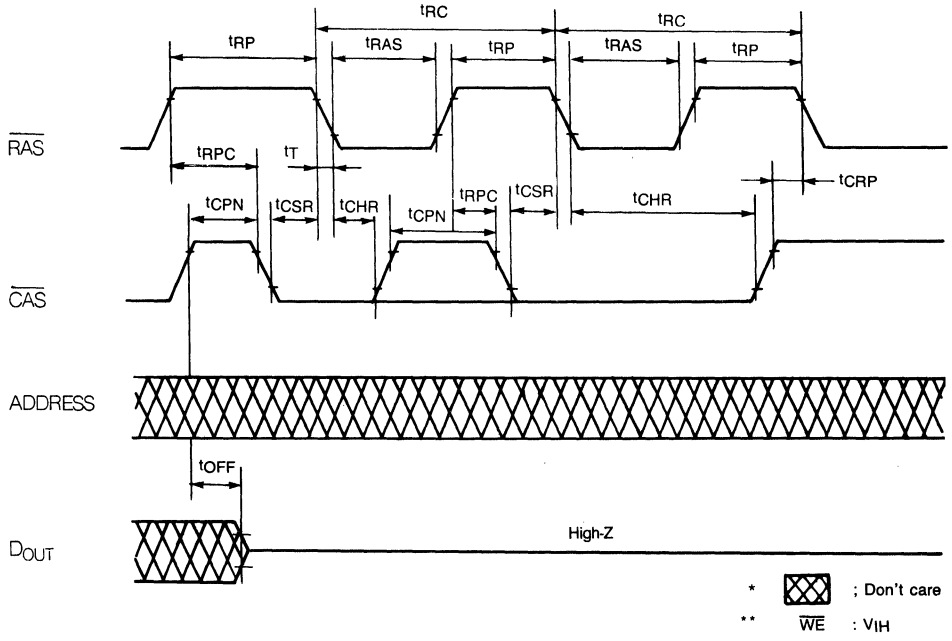


FIGURE 6. CAS-BEFORE-RAS REFRESH CYCLE

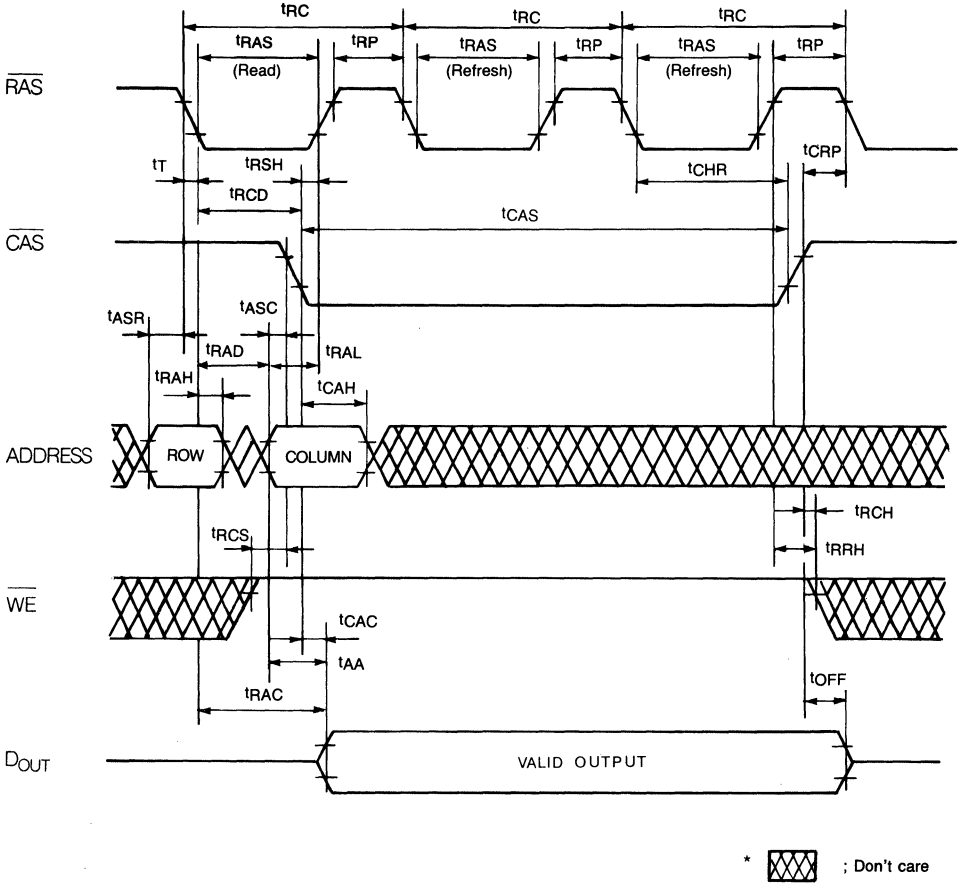


FIGURE 7. HIDDEN REFRESH CYCLE

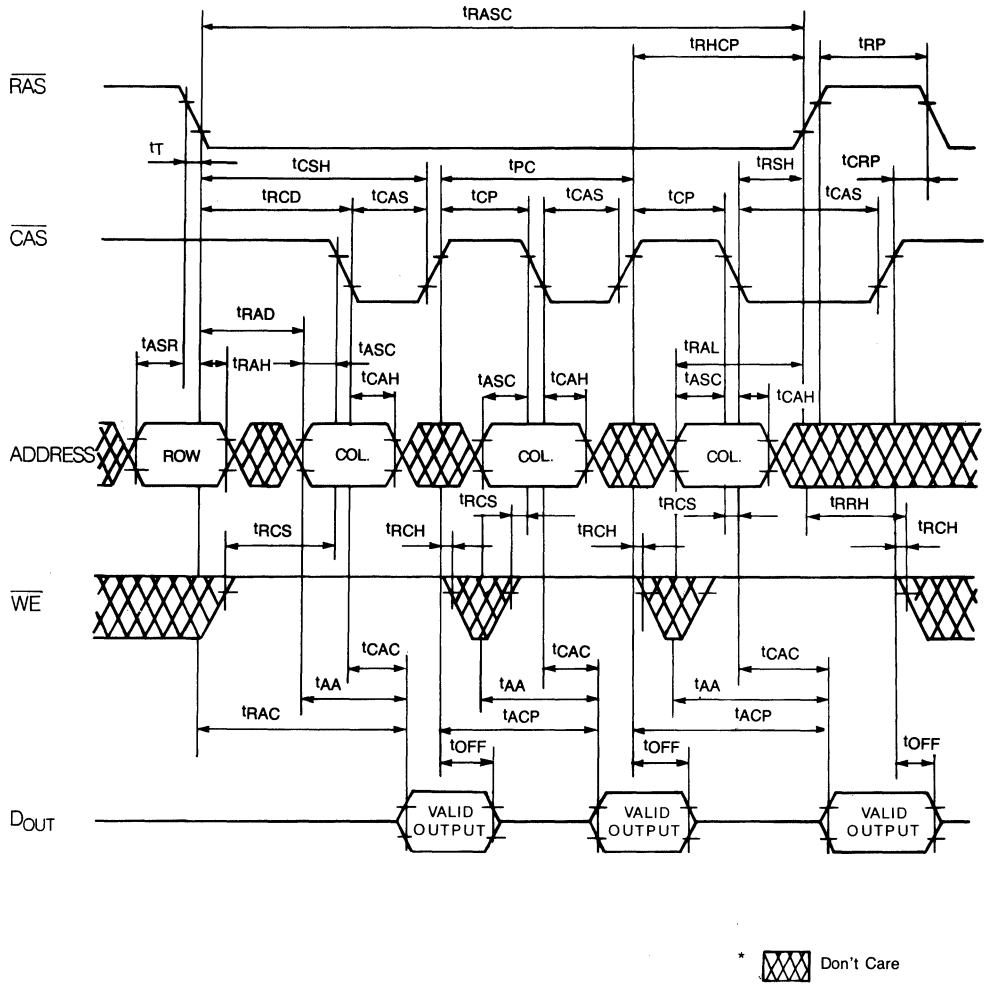


FIGURE 8. FAST PAGE MODE READ CYCLE

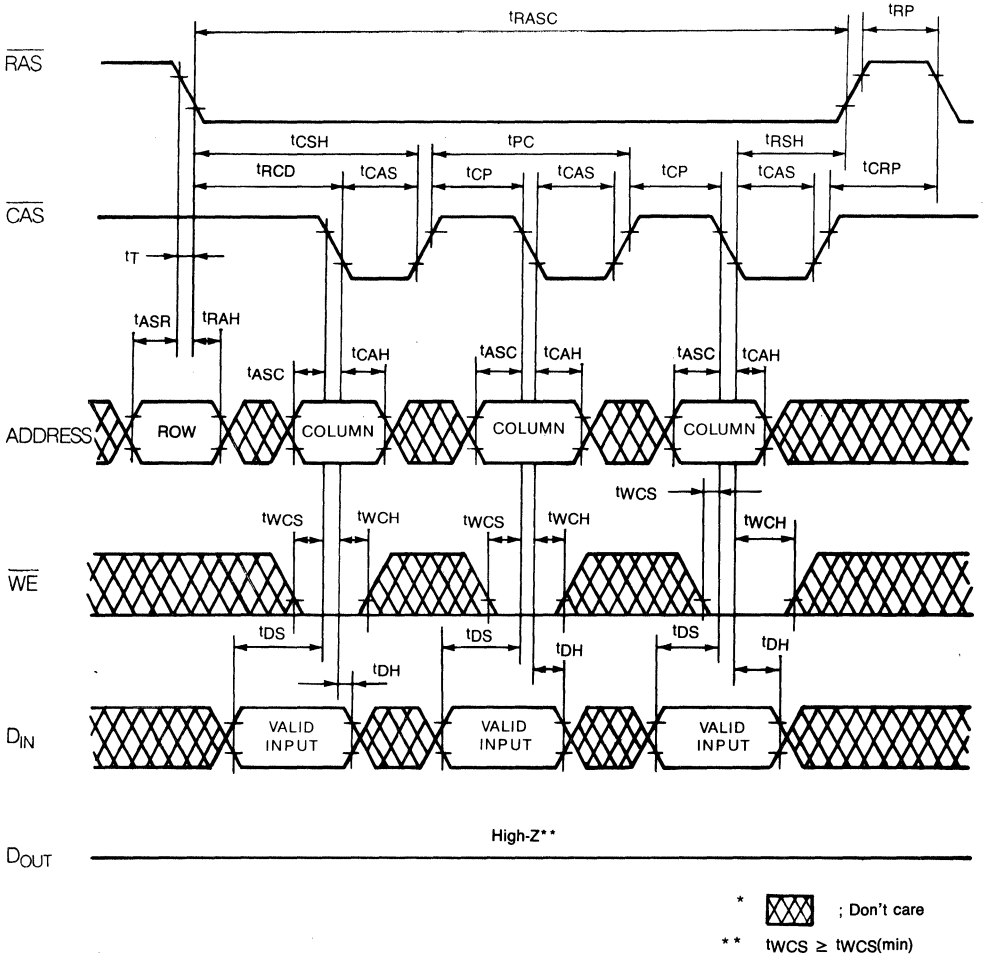


FIGURE 9. FAST PAGE MODE EARLY WRITE CYCLE

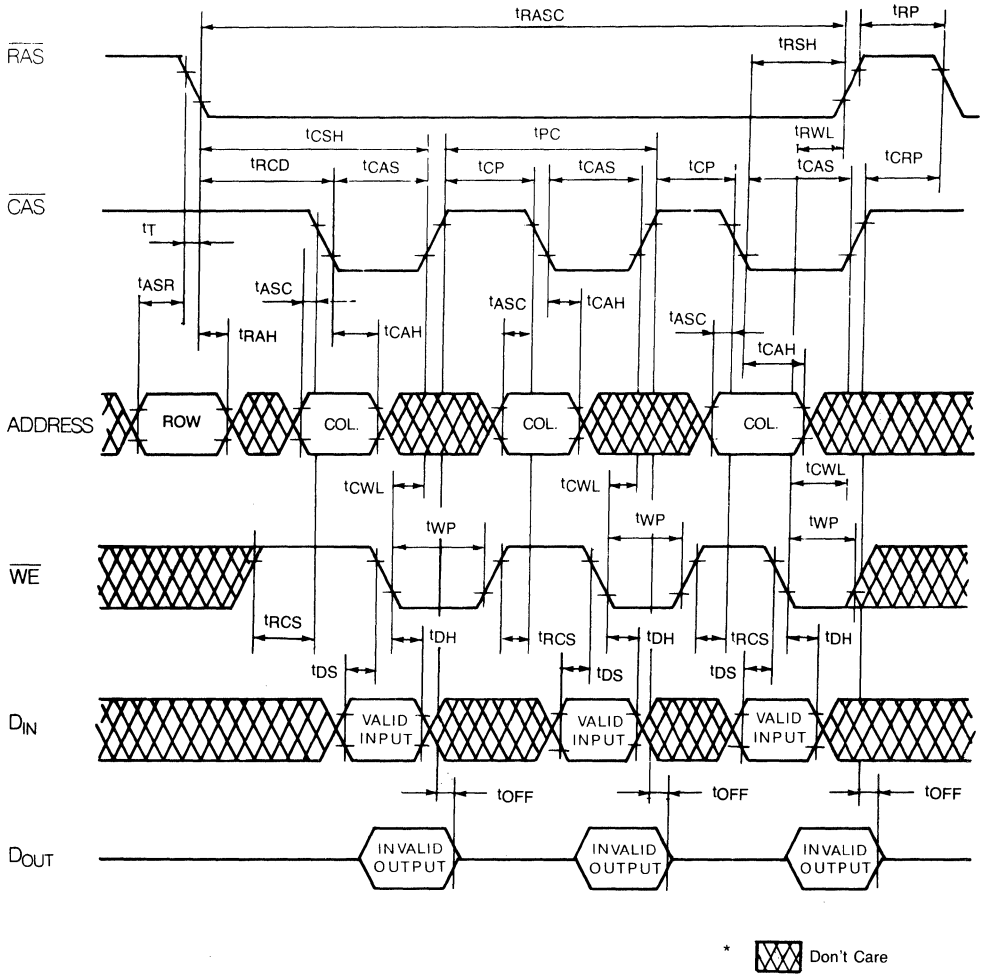


FIGURE 10. FAST PAGE MODE DELAYED WRITE CYCLE

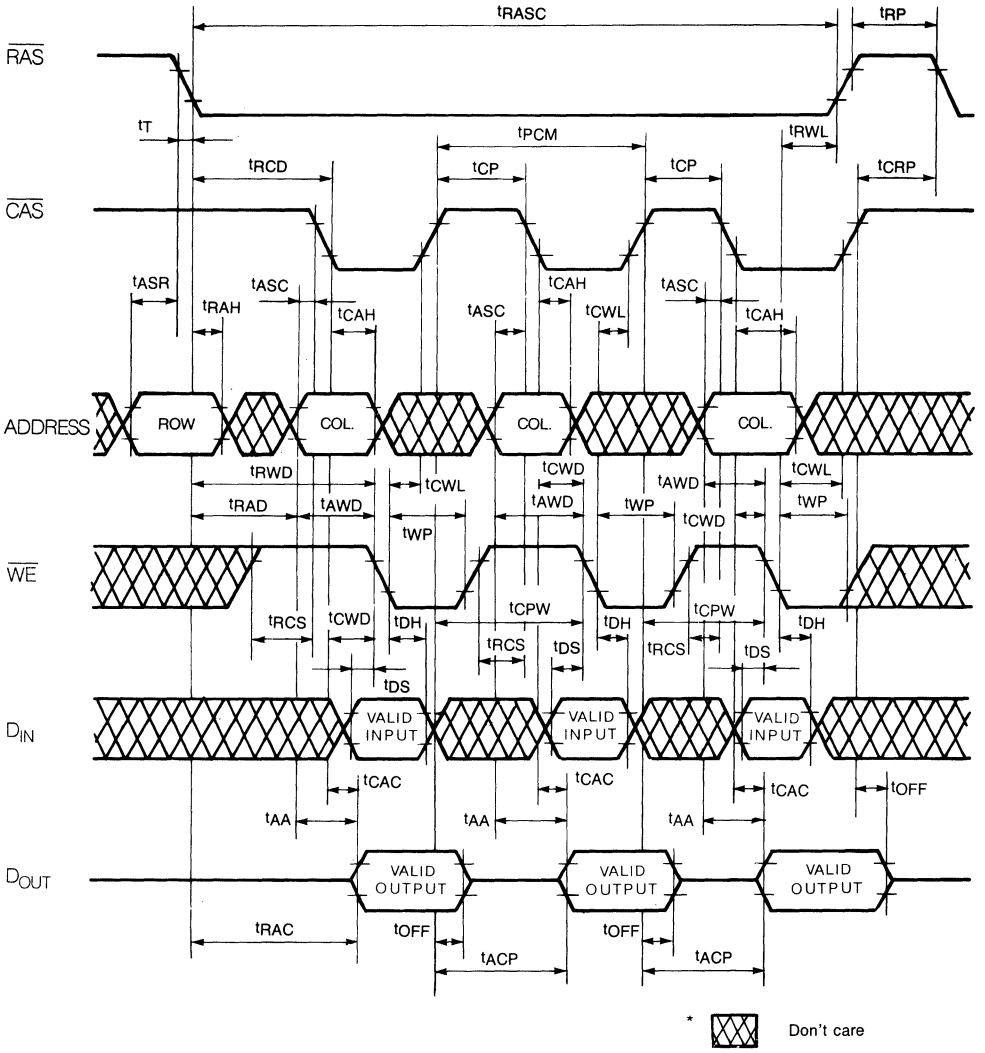


FIGURE 11. FAST PAGE MODE READ-MODIFY-WRITE CYCLE

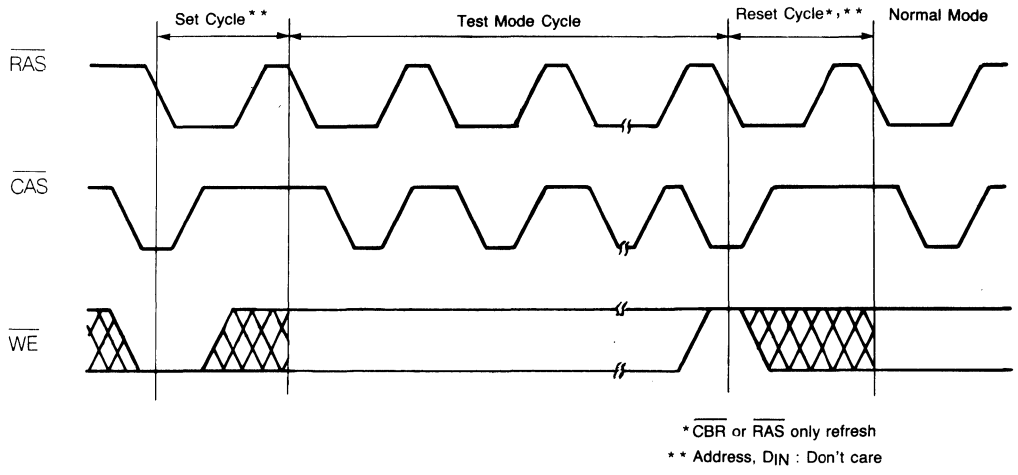


FIGURE 12. TEST MODE CYCLE

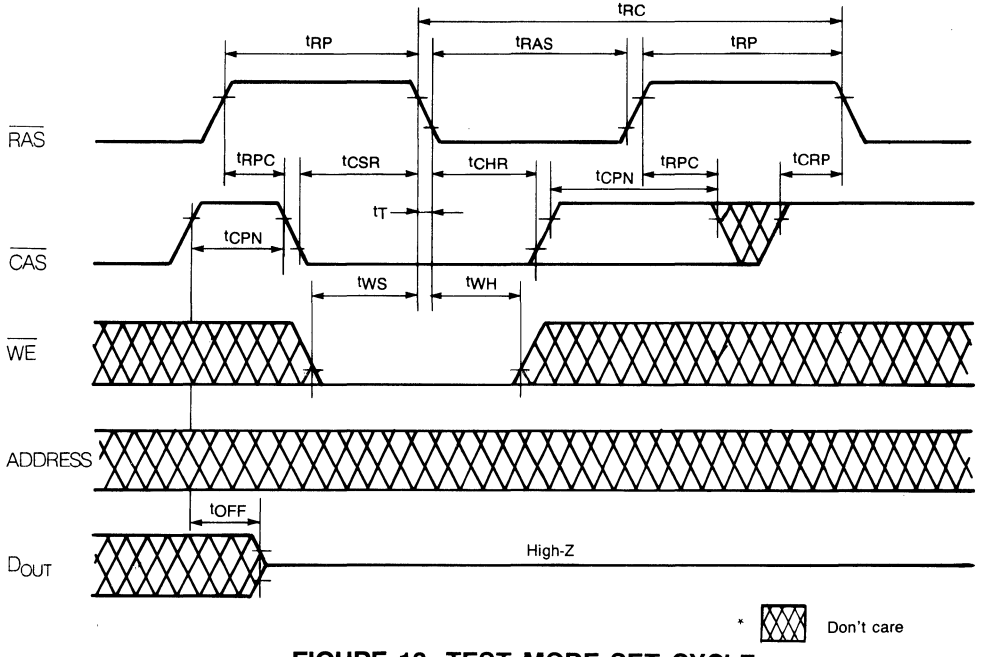


FIGURE 13. TEST MODE SET CYCLE

TEST MODE RESET CYCLE

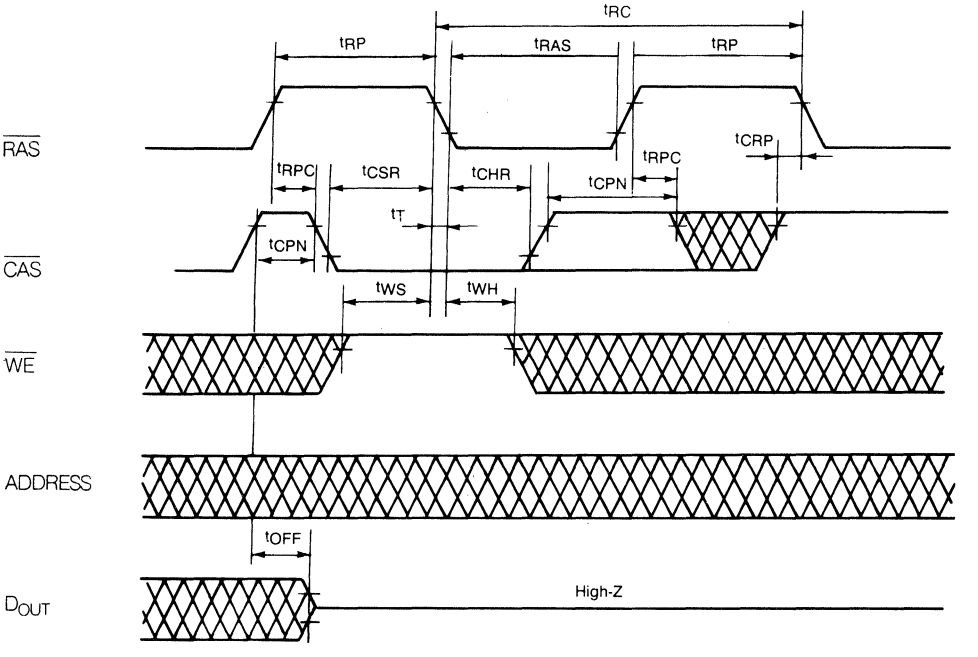


FIGURE 14. $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE

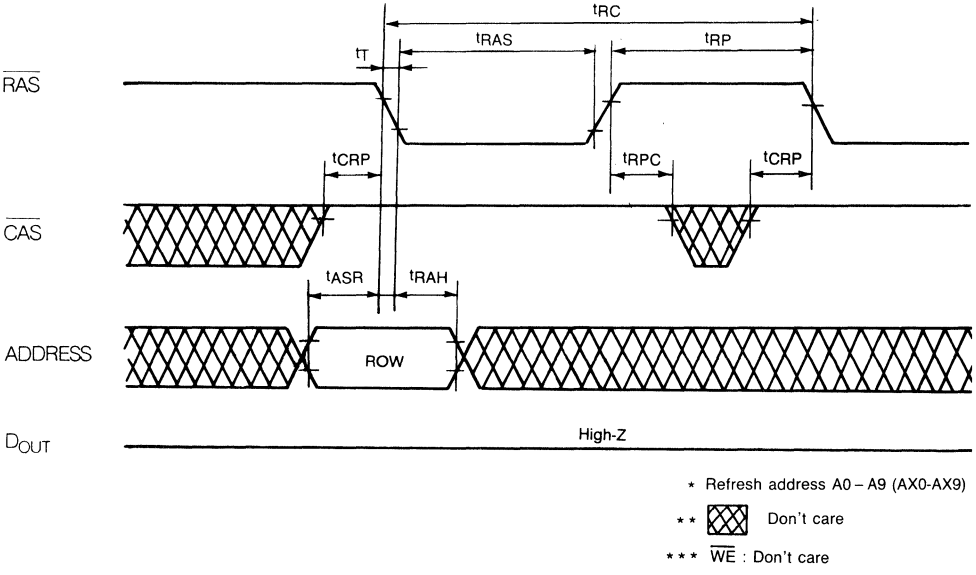


FIGURE 15. $\overline{RAS}$-ONLY REFRESH CYCLE

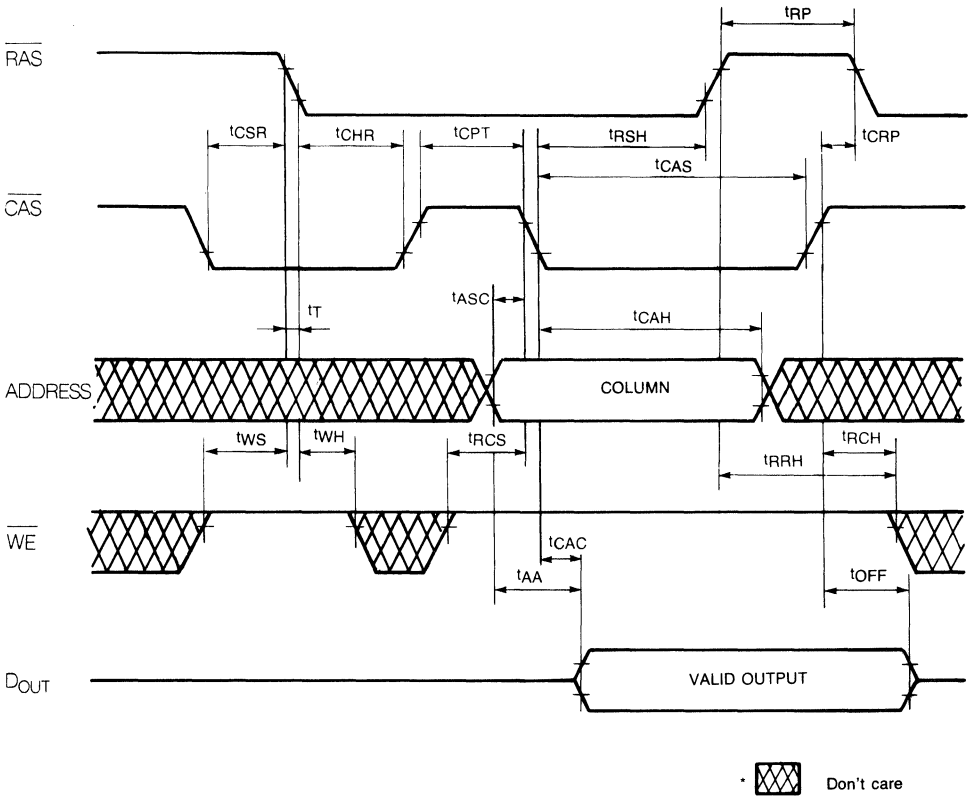


FIGURE 16. $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER CHECK CYCLE (READ)

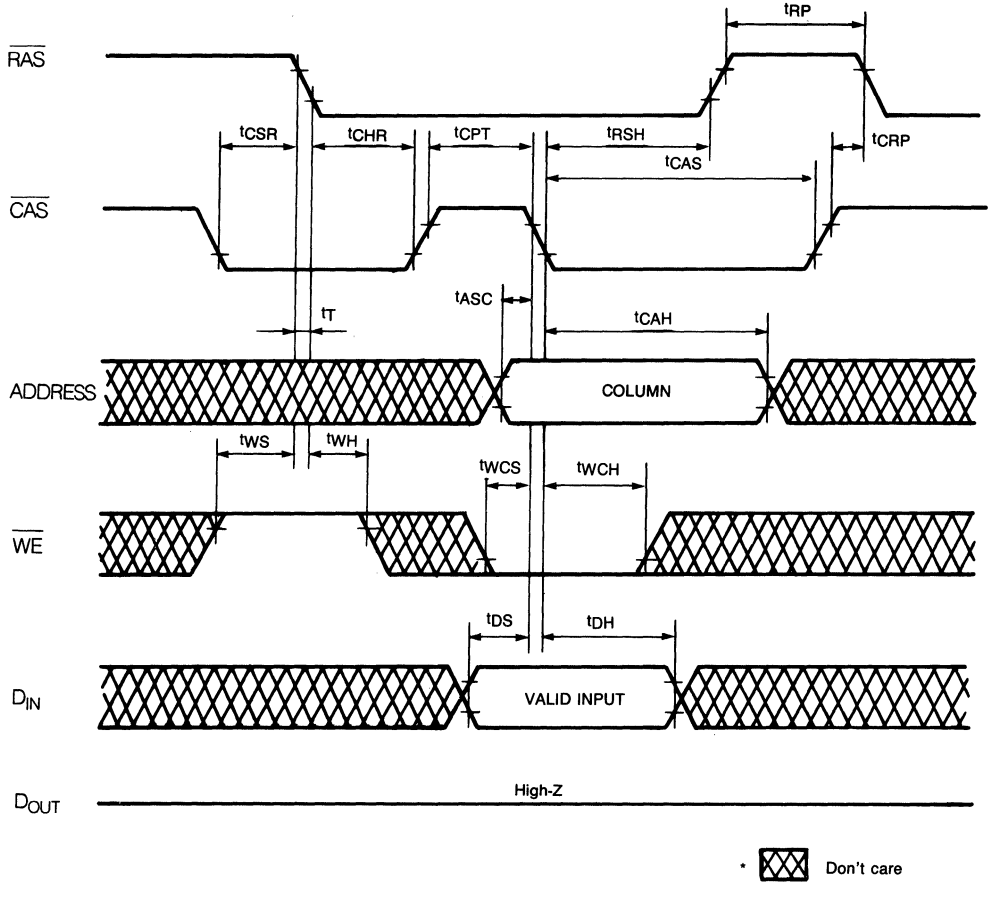
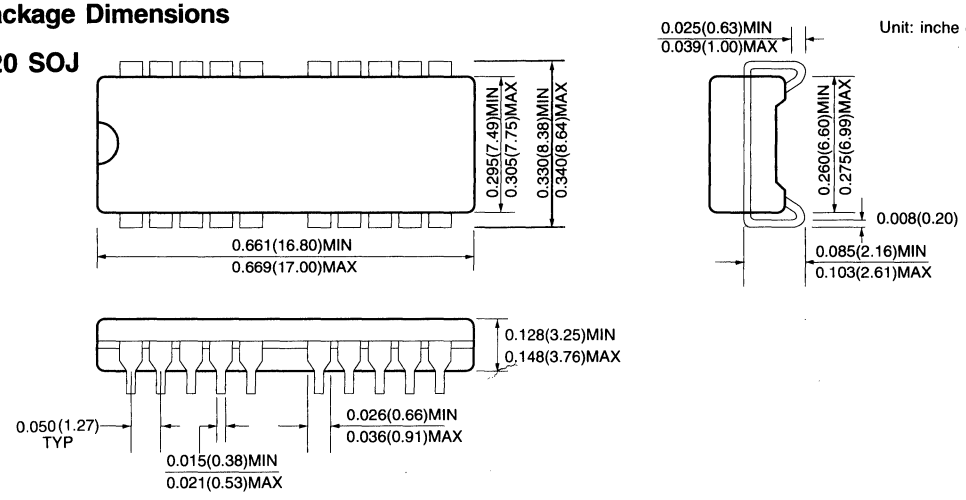


FIGURE 17. $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER CHECK CYCLE (WRITE)

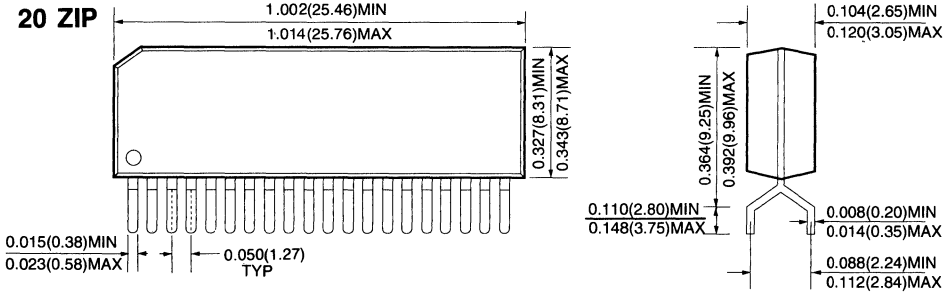
Package Dimensions

Unit: inche (mm)

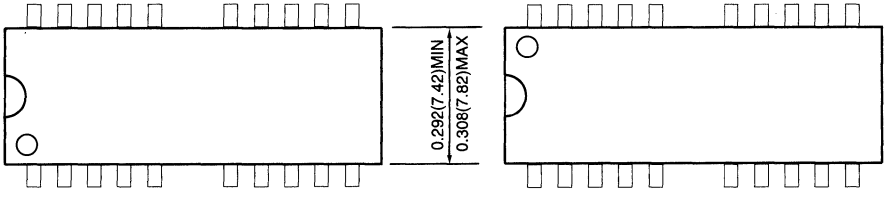
20 SOJ



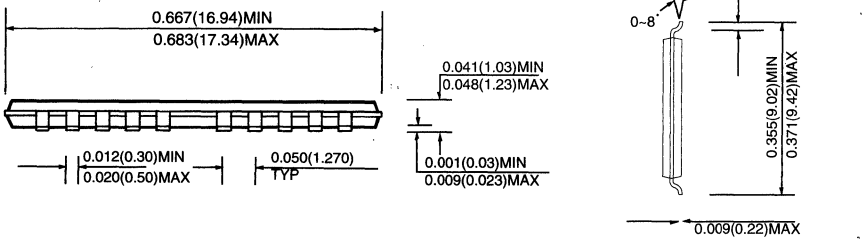
20 ZIP



20(26) TSOP (TYPE II)



GM71C4100AT/ALT **GM71C4100AR/ALR**



GM71C4400A/AL

1,048,576 WORDS×4 BIT
CMOS DYNAMIC RAM

Description

The GM71C4400A/AL is the new generation dynamic RAM organized 1,048,576×4 Bit. GM71C4400A/AL has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71C4400A/AL offers Fast Page Mode as a high speed access Mode. Multiplexed address inputs permit the GM71C4400A/AL to be packaged in a standard 300-mil 20-pin plastic SOJ, standard 400-mil 20-pin plastic ZIP, and standard 300-mil 20-pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment. System oriented features include single power supply of 5V ± 10% tolerance, direct interfacing capability with high performance logic families such as Schottky TTL.

Features

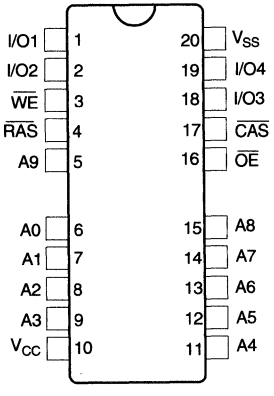
- 1,048,576 × 4 Bit Organization
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GM71C4400A/AL-60	60	15	110	40
GM71C4400A/AL-70	70	20	130	45
GM71C4400A/AL-80	80	20	150	50
GM71C4400A/AL-10	100	25	180	55

- Low Power
  Active: 605/550/495/440mW (MAX)
  Standby: 5.5mW (CMOS level: MAX)
  1.1mW (L-series)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16ms
- 1024 Refresh Cycles/128ms (L-series)
- Battery Back Up Operation (L-series)

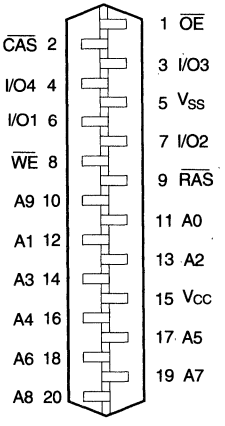
Pin Configuration

20 (26) SOJ



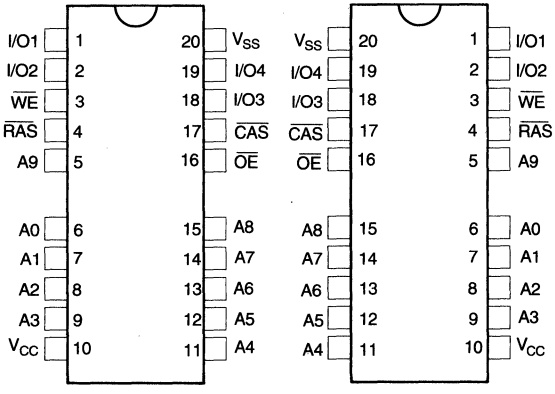
(TOP VIEW)

20 ZIP



(BOTTOM VIEW)

20 (26) TSOP II



(TOP VIEW)

Pin Description

Pin	Function	Pin	Function
A0 ~ A9	Address Inputs	$\overline{WE}$	Read/Write Enable
A0 ~ A9	Refresh Address Inputs	$\overline{OE}$	Output Enable
I/O1 ~ I/O4	Data-in/Data-out	V_{CC}	Power (+5V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe		

Ordering Information

Type No.	Access Time	PKG
GM71C4400AJ/ALJ-60 GM71C4400AJ/ALJ-70 GM71C4400AJ/ALJ-80 GM71C4400AJ/ALJ-10	60ns 70ns 80ns 100ns	300 Mil 20 (26) Pin Plastic SOJ
GM71C4400AZ/ALZ-60 GM71C4400AZ/ALZ-70 GM71C4400AZ/ALZ-80 GM71C4400AZ/ALZ-10	60ns 70ns 80ns 100ns	400 Mil 20 Pin Plastic ZIP
GM71C4400AT/ALT-60 GM71C4400AT/ALT-70 GM71C4400AT/ALT-80 GM71C4400AT/ALT-10	60ns 70ns 80ns 100ns	300 Mil 20 (26) Pin Plastic TSOP II (Normal Type)
GM71C4400AR/ALR-60 GM71C4400AR/ALR-70 GM71C4400AR/ALR-80 GM71C4400AR/ALR-10	60ns 70ns 80ns 100ns	300 Mil 20 (26) Pin Plastic TSOP II (Reverse Type)

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature (plastic)	−55 ~ 125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−1.0 ~ 7.0	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	−1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.0	W

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	6.5	V
V_{IL}	Input Low Voltage (I/O Pin)	−1.0	—	0.8	V
V_{IL}	Input Low Voltage (Others)	−2.0	—	0.8	V

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	110	mA	1,2
		70ns	—	100		
		80ns	—	90		
		100ns	—	80		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH}. D_{OUT} = High-Z)		—	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Refresh Mode ($\overline{RAS}$ Cycling. $\overline{CAS}$ = V_{IH}. t_{RC} = t_{RC}min)	60ns	—	110	mA	2
		70ns	—	100		
		80ns	—	90		
		100ns	—	80		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}. $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	60ns	—	110	mA	1,3
		70ns	—	100		
		80ns	—	90		
		100ns	—	80		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current		—	1	mA	
	($\overline{RAS}$, $\overline{CAS}$ = V_{IH} $\overline{WE}$, $\overline{OE}$, Address, D_{IN} = V_{IH} or V_{IL}. D_{OUT} = High-Z)		—	200	μA	4,5
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	110	mA	
		70ns	—	100		
		80ns	—	90		
		100ns	—	80		
I_{CC7}	Battery Back Up Operating Current (Standby with CBR Refresh) (t_{RC} = 125μs. $t_{RAS} \leq 1\mu s$. $\overline{WE}$ = V_{IH}. $\overline{CAS}$ = V_{IL}. $\overline{OE}$, Address and D_{IN} = V_{IH} or V_{IL}. D_{OUT} = High-Z)		—	300	μA	4,5
I_{CC8}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	5	mA	1
$I_{I(L)}$	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 7V$)		−10	10	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 7V$)		−10	10	μA	

Note) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} (max) is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}
4. L Series
5. V_{CC}-0.2V ≤ V_{IH} ≤ 6.5, 0V ≤ V_{IL} ≤ 0.2V

Capacitance (V_{CC}=5V ± 10%, T_A=25°C)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	—	5	pF	1
C_{I2}	Input Capacitance (Clocks)	—	7	pF	1
$C_{I/O}$	Output Capacitance (Data-In/Out)	—	10	pF	1,2

Note 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable D_{OUT}.

AC Characteristics (V_{CC}=5V±10%, T_A=0~70°C, Note 1, 14, 15, 16)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GM71C4400A/AL-60		GM71C4400A/AL-70		GM71C4400A/AL-80		GM71C4400A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	150	—	180	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	60	—	70	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	100	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	20	10,000	25	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	10	—	15	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	15	—	20	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	60	25	75	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	55	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	100	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	10	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	15	—	20	—	20	—	25	—	ns	
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	—	0	—	0	—	0	—	ns	
t_{DZC}	$\overline{CAS}$ Set-up Time from D_{IN}	0	—	0	—	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	—	16	—	16	—	16	—	16	ms	
	Refresh Period (L-Series)	—	128	—	128	—	128	—	128	ms	

Read Cycle

Symbol	Parameter	GM71C4400A/AL-60		GM71C4400A/AL-70		GM71C4400A/AL-80		GM71C4400A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	—	80	—	100	ns	2,3,17
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	—	20	—	25	ns	3,4,13, 17
t_{AA}	Access Time from Column Address	—	30	—	35	—	40	—	45	ns	3,5,13, 17
t_{OAC}	Access Time from $\overline{OE}$	—	15	—	20	—	20	—	25	ns	3,17
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	0	—	ns	18
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	0	—	0	—	ns	18
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	45	—	ns	
t_{OFF1}	Output Buffer Turn-off Delay Time	0	15	0	20	0	20	0	25	ns	6
t_{OFF2}	Output Buffer Turn-off Delay Time from $\overline{OE}$	0	15	0	20	0	20	0	25	ns	6
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	20	—	25	—	ns	

Write Cycle

Symbol	Parameter	GM71C4400A/AL-60		GM71C4400A/AL-70		GM71C4400A/AL-80		GM71C4400A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	15	—	15	—	20	—	ns	
t_{WP}	Write Command Pulse Width	10	—	10	—	10	—	20	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	20	—	25	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	15	—	15	—	20	—	ns	11

Read-Modify-Write Cycle

Symbol	Parameter	GM71C4400A/AL-60		GM71C4400A/AL-70		GM71C4400A/AL-80		GM71C4400A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	150	—	180	—	200	—	245	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80	—	95	—	105	—	135	—	ns	10
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	35	—	45	—	45	—	60	—	ns	10
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50	—	60	—	65	—	80	—	ns	10
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$	15	—	20	—	20	—	25	—	ns	

Refresh Cycle

Symbol	Parameter	GM71C4400A/AL-60		GM71C4400A/AL-70		GM71C4400A/AL-80		GM71C4400A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	10	—	10	—	ns	
t_{CPN}	$\overline{CAS}$ Precharge Time in Normal Mode	10	—	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Symbol	Parameter	GM71C4400A/AL-60		GM71C4400A/AL-70		GM71C4400A/AL-80		GM71C4400A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	50	—	55	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Recharge Time	10	—	10	—	10	—	10	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	100,000	—	100,000	—	100,000	—	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	—	45	—	50	ns	3,13,17
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	45	—	50	—	ns	
t_{CPW}	Fast Page Mode Read-Modify-Write Cycle $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	55	—	65	—	70	—	85	—	ns	
t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	80	—	95	—	100	—	110	—	ns	

Test Mode Cycle

Symbol	Parameter	GM71C4400A/AL-60		GM71C4400A/AL-70		GM71C4400A/AL-80		GM71C4400A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{WS}	Test Mode $\overline{WE}$ Set-up Time	0	—	0	—	0	—	0	—	ns	
t_{WH}	Test Mode $\overline{WE}$ Hold Time	10	—	10	—	10	—	10	—	ns	

Counter Test Cycle

Symbol	Parameter	GM71C4400A/AL-60		GM71C4400A/AL-70		GM71C4400A/AL-80		GM71C4400A/AL-10		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
t_{CPT}	$\overline{CAS}$ Precharge Time in Counter Test Cycle	40	—	40	—	40	—	50	—	ns	

Notes :

1. AC measurements assume $t_T = 5ns$.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD}(max)$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit. then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only : if $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle : if $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$ $t_{AWD} \geq t_{AWD}(min)$ and $t_{CPW} \geq t_{CPW}(min)$ the cycle is a read modify write and the data output will contain data read from the selected cell: if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or a read modify write cycle.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles is required.
15. In delayed write or read modify write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
16. Test mode operation specified in this data sheet is 2 bit test function controlled by control address bits ... CA0. This test mode operation can be performed by $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ (WCBR) refresh cycle. Refresh during test mode operation will be performed by normal read cycles or by WCBR refresh cycles. When the state of two test bits accord each other, the condition of the output data is high level. When the state of test bits do not accord, the condition of the output data is low level. In order to end this test mode operation, perform a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.
17. In a test mode read cycle, the value of t_{RAC}, t_{AA}, t_{CAC}, t_{OAC} and t_{ACP} is delayed for 2ns to 5ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

TIMING WAVEFORMS

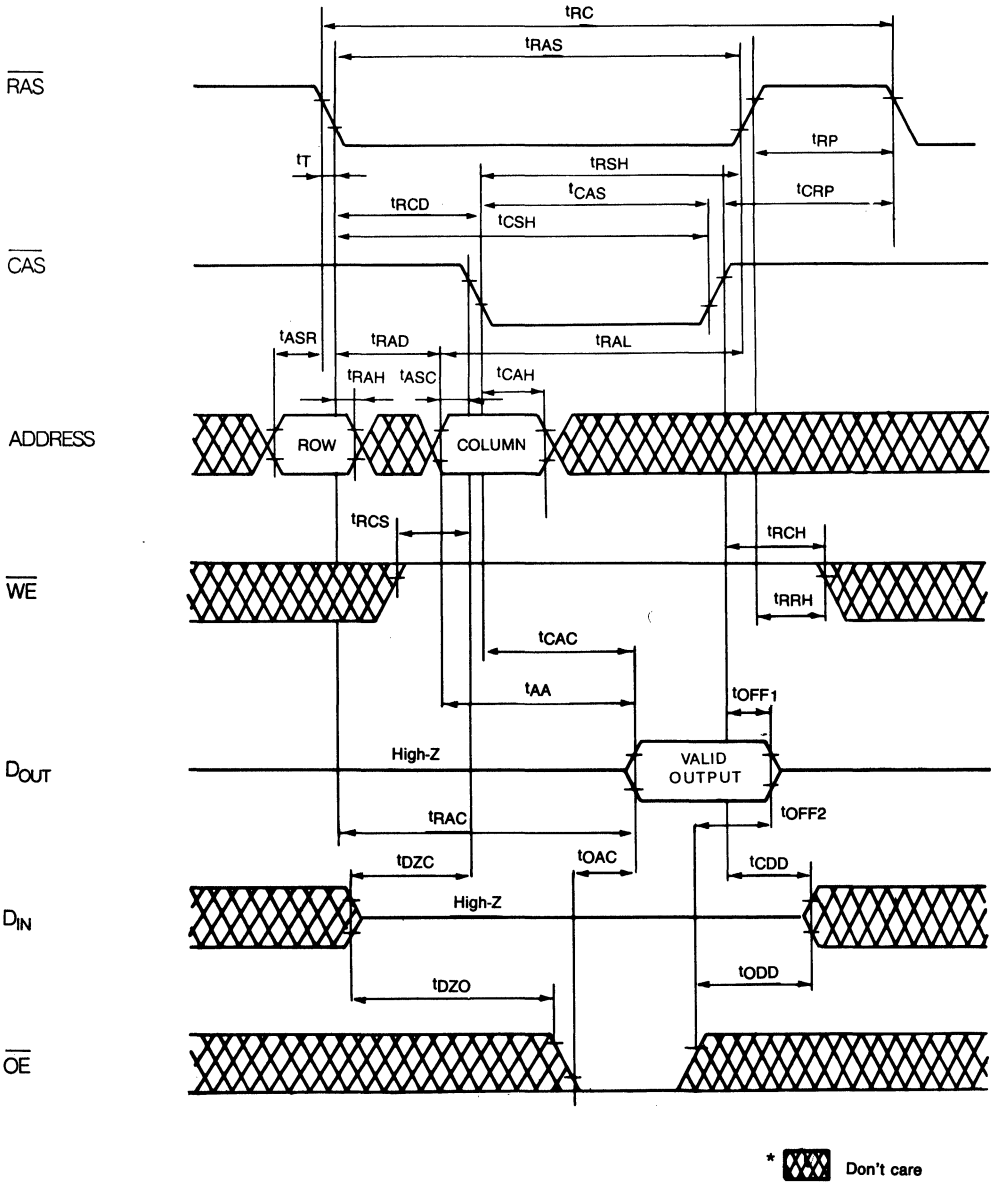


FIGURE 1. READ CYCLE

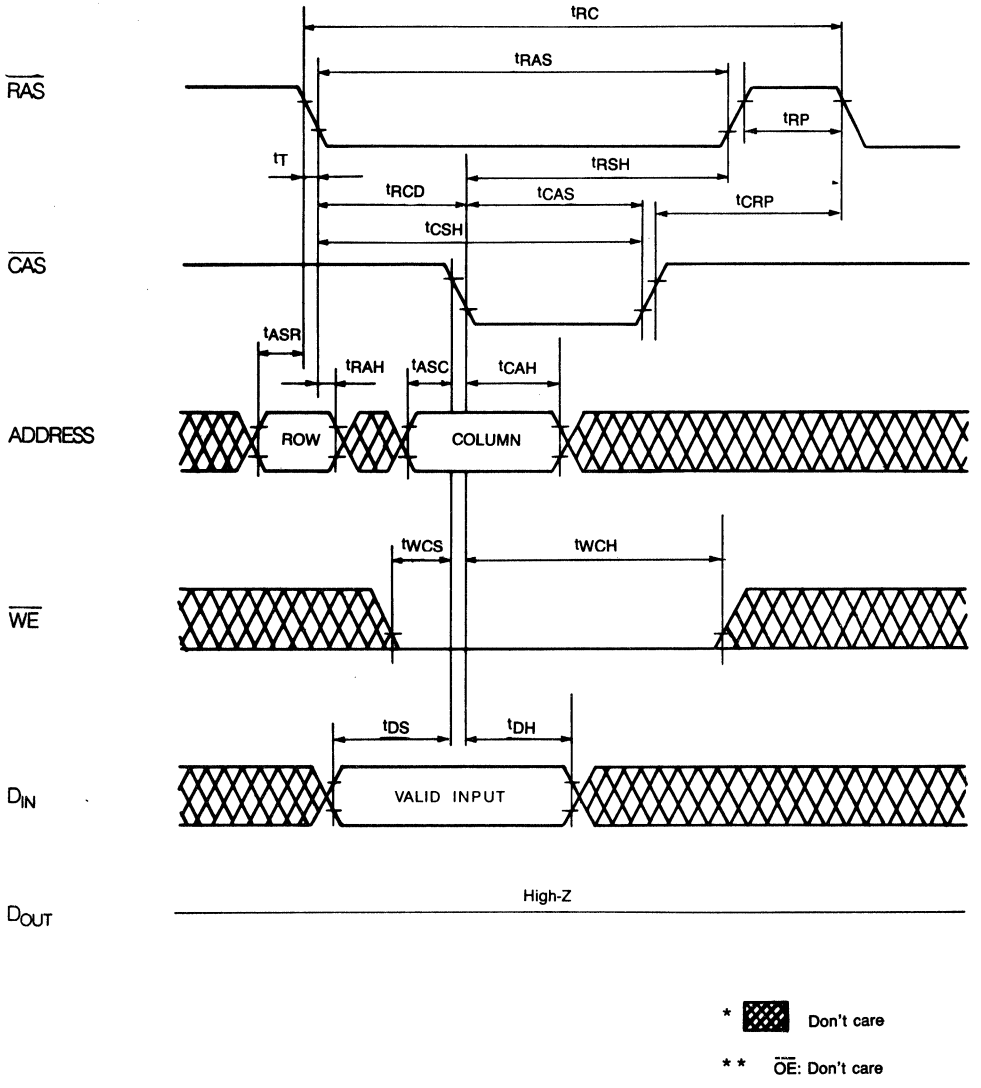


FIGURE 2. EARLY WRITE CYCLE

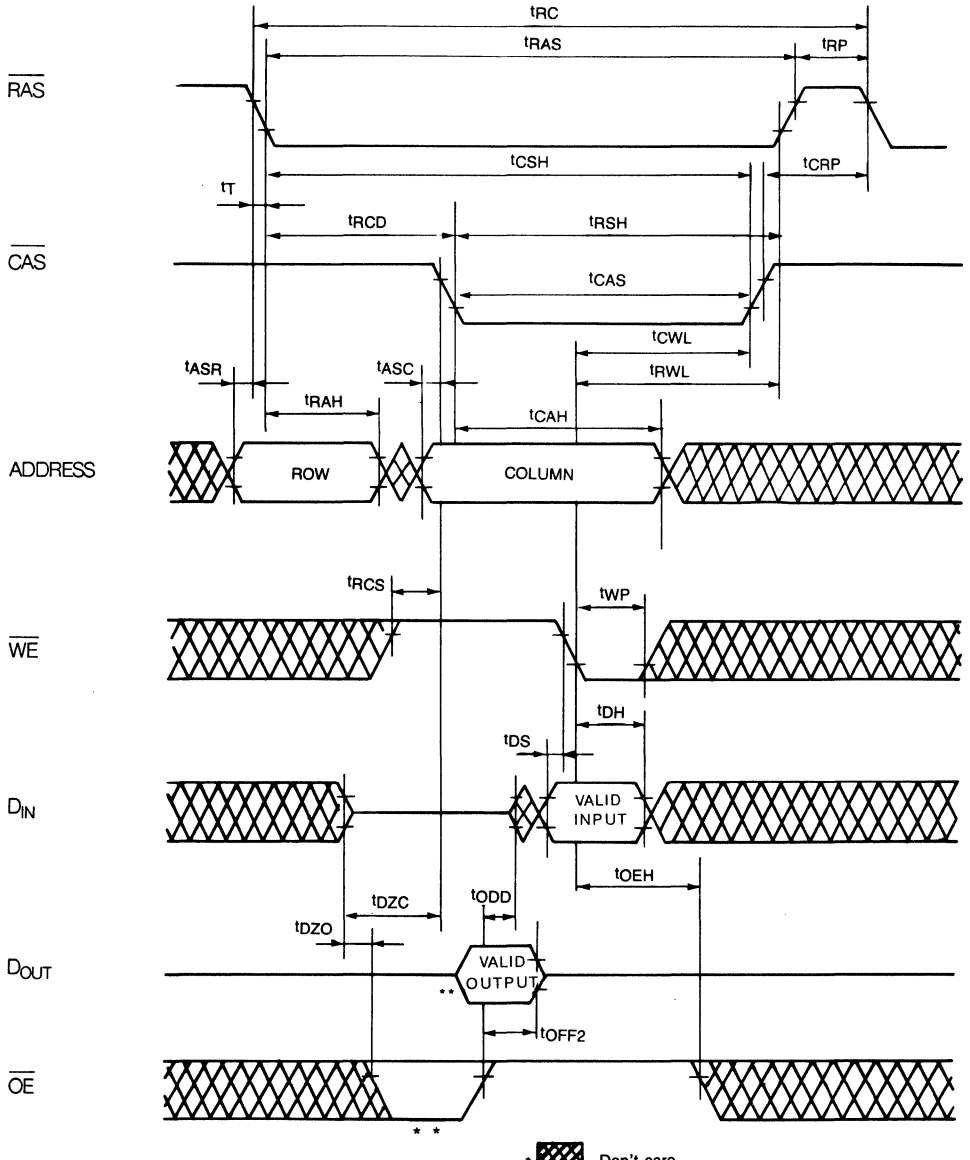


FIGURE 3. DELAYED WRITE CYCLE

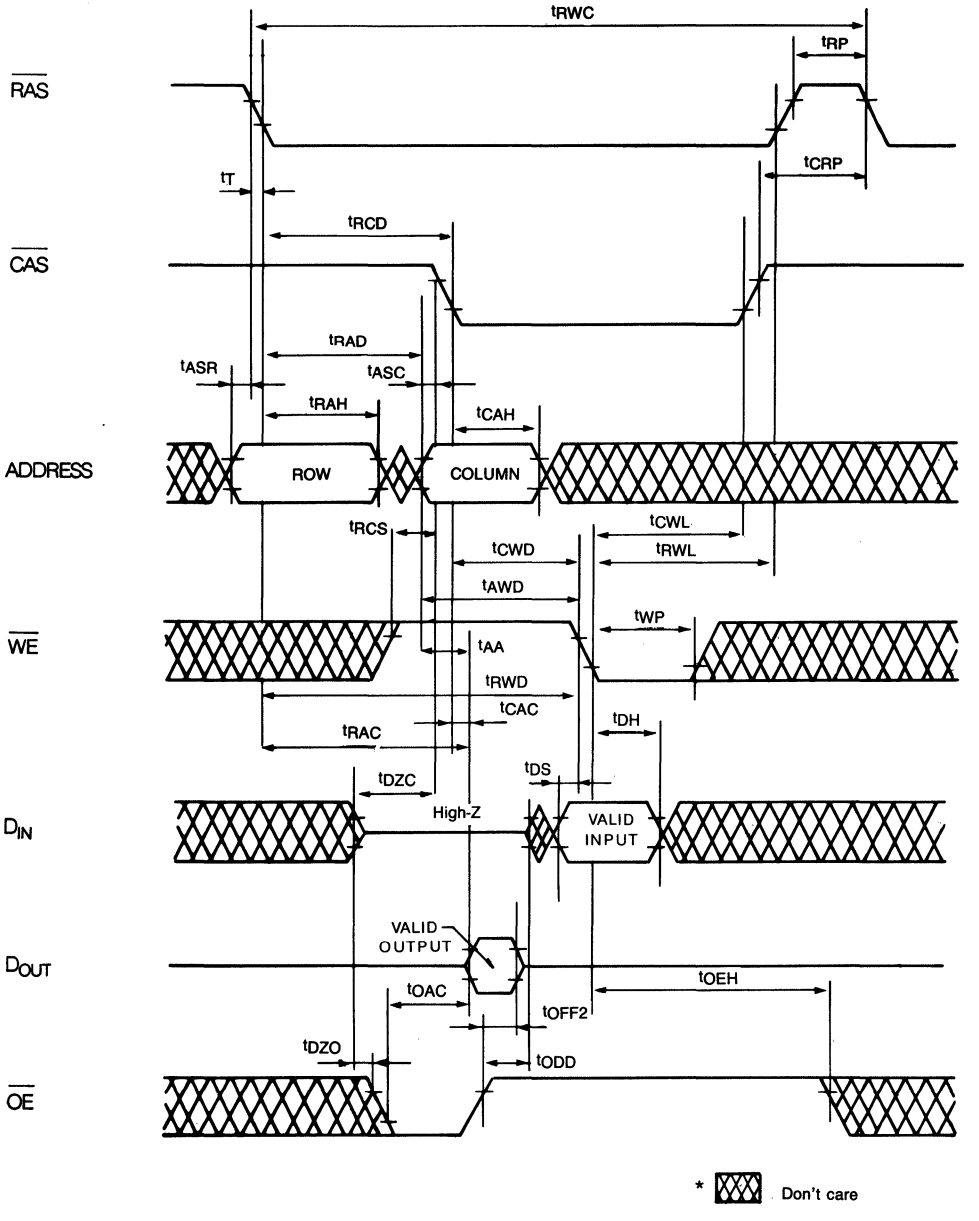


FIGURE 4. READ-MODIFY-WRITE CYCLE

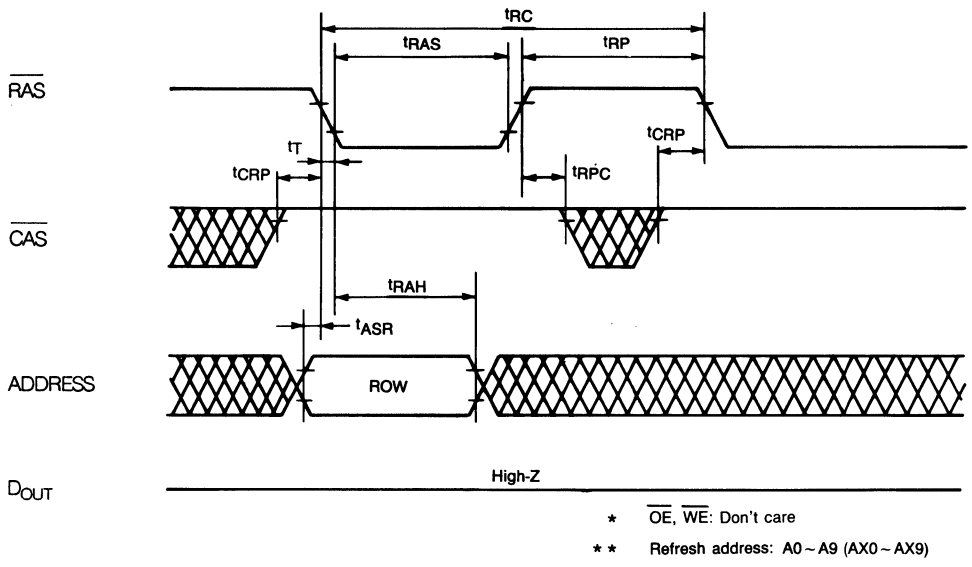


FIGURE 5. RAS-ONLY-REFRESH CYCLE

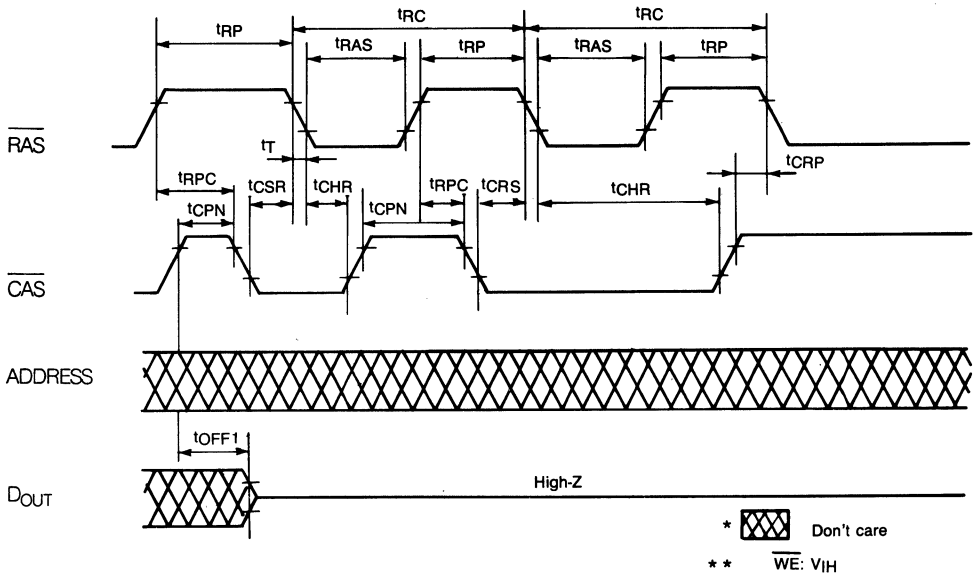


FIGURE 6. CAS-BEFORE-RAS REFRESH CYCLE

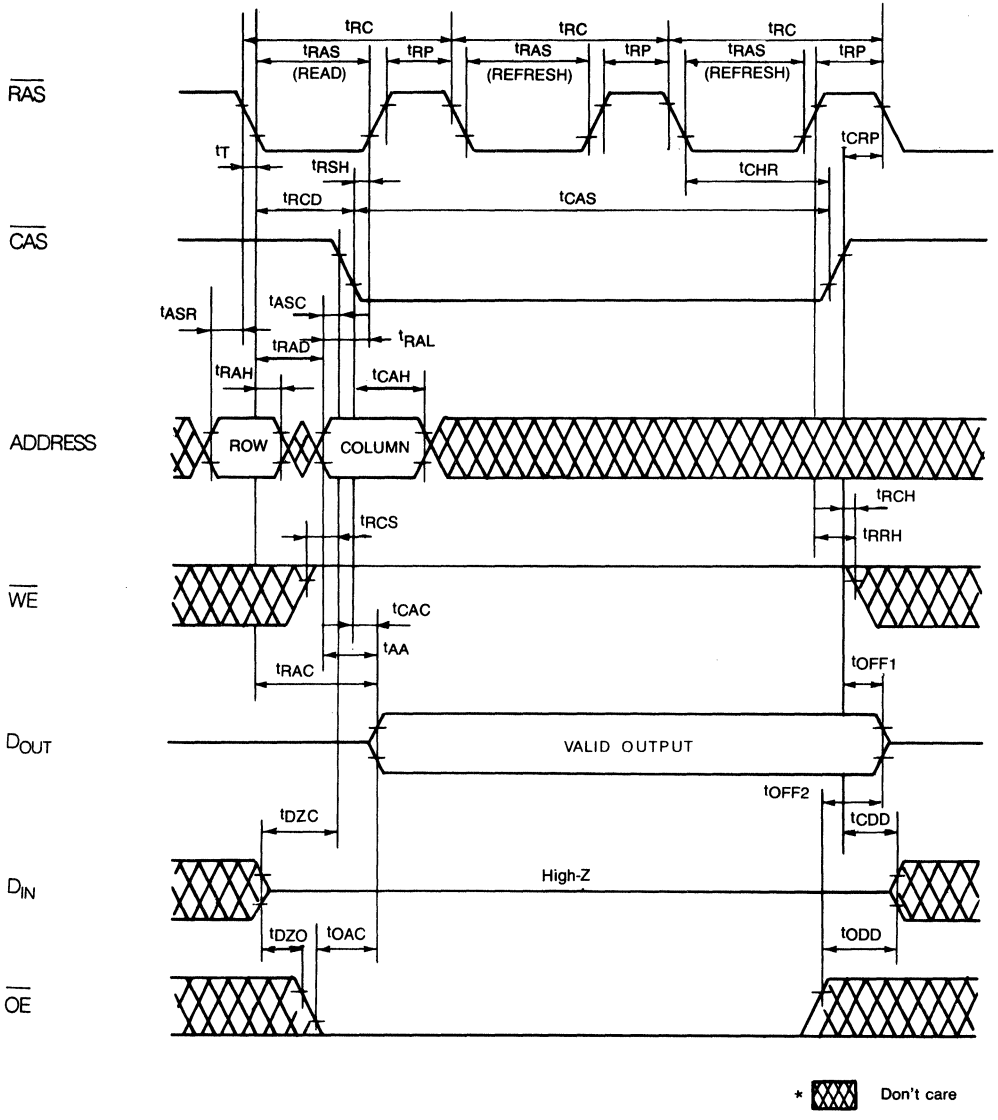


FIGURE 7. HIDDEN REFRESH CYCLE

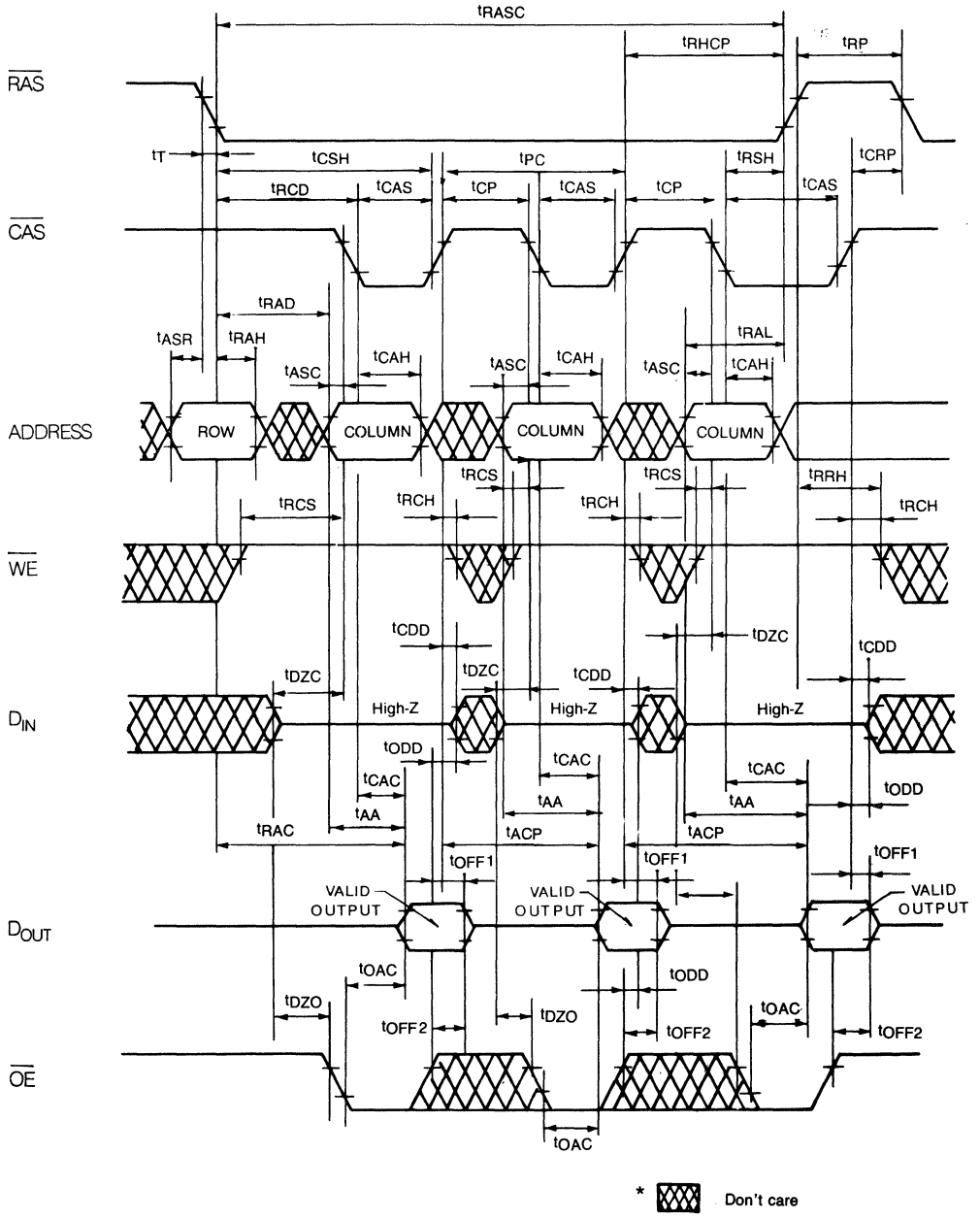


FIGURE 8. FAST PAGE MODE READ CYCLE

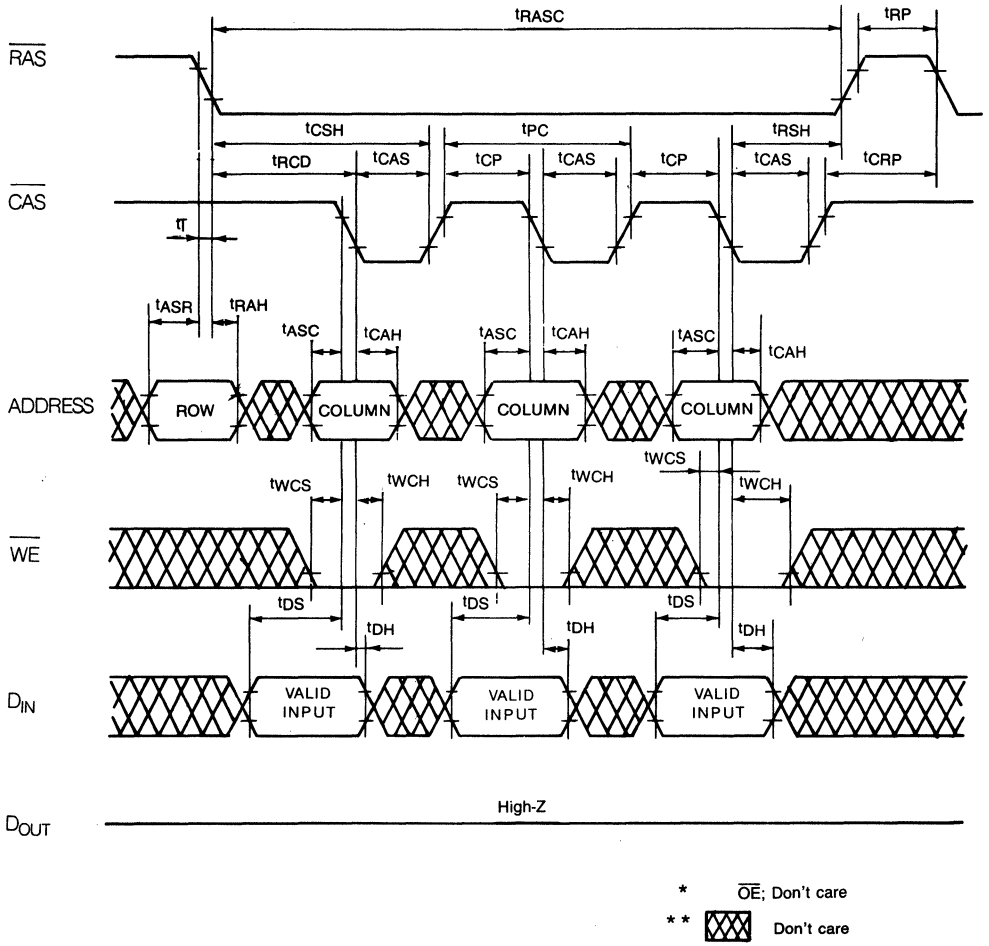


FIGURE 9. FAST PAGE MODE EARLY WRITE CYCLE

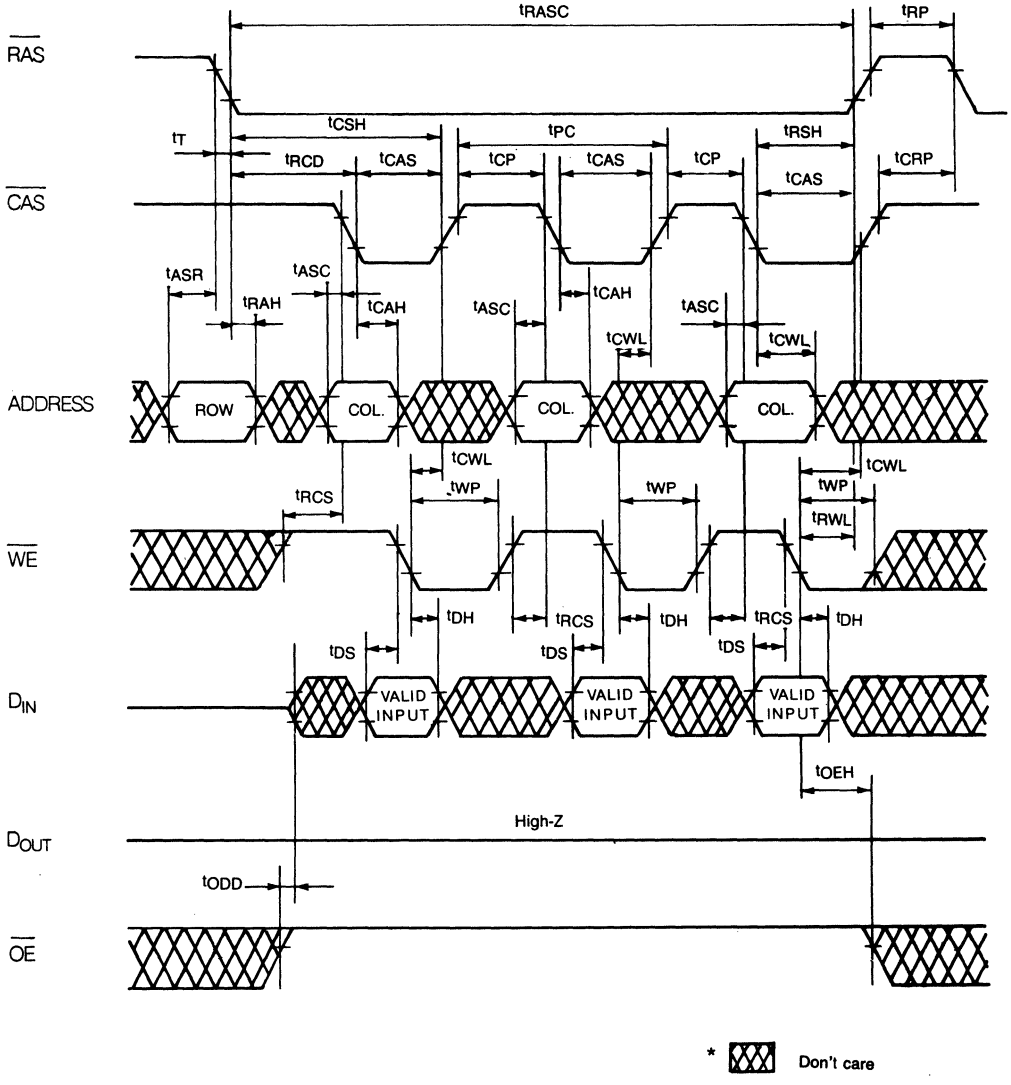


FIGURE 10. FAST PAGE MODE DELAYED WRITE CYCLE

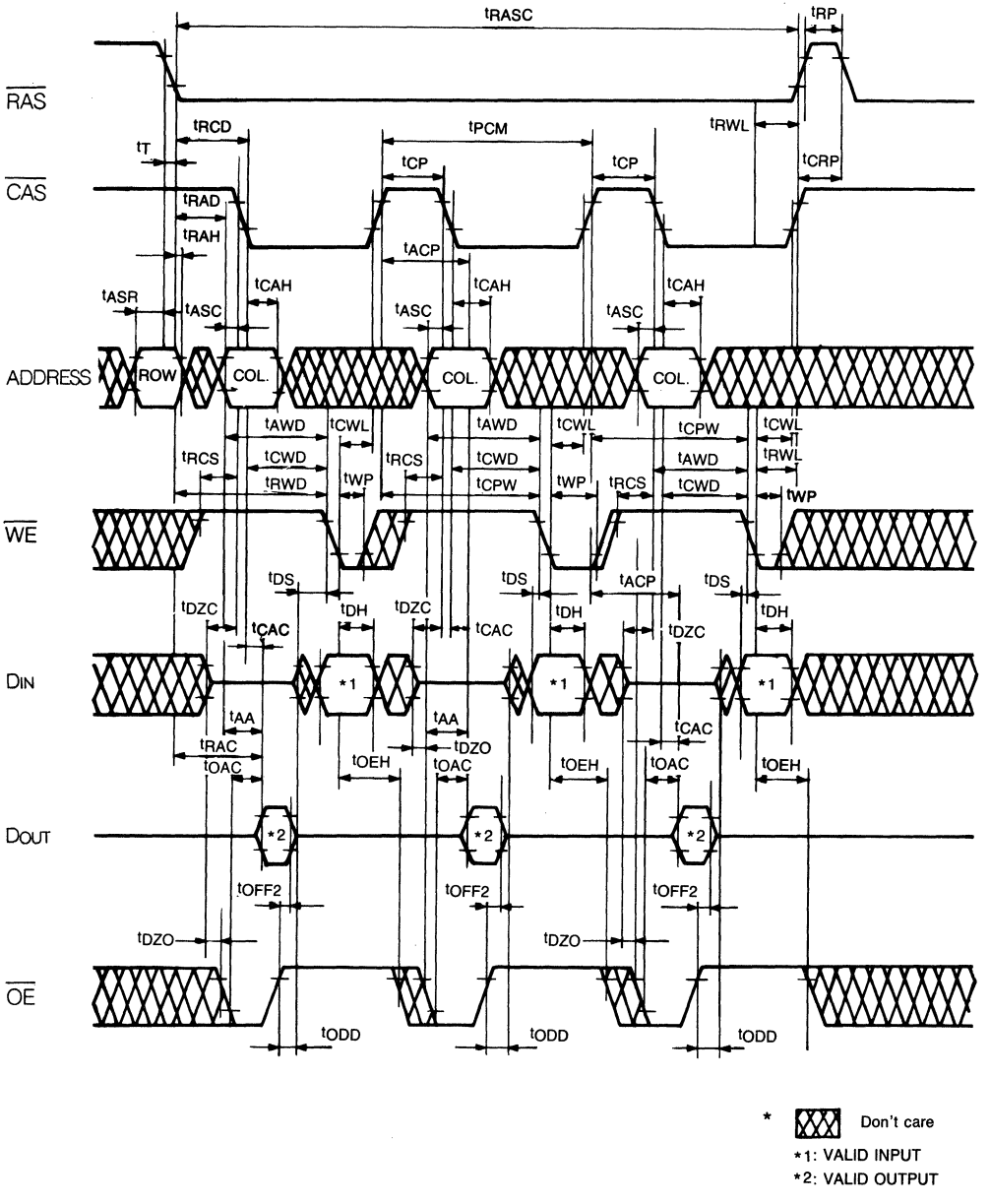


FIGURE 11. FAST PAGE MODE READ-MODIFY-WRITE CYCLE

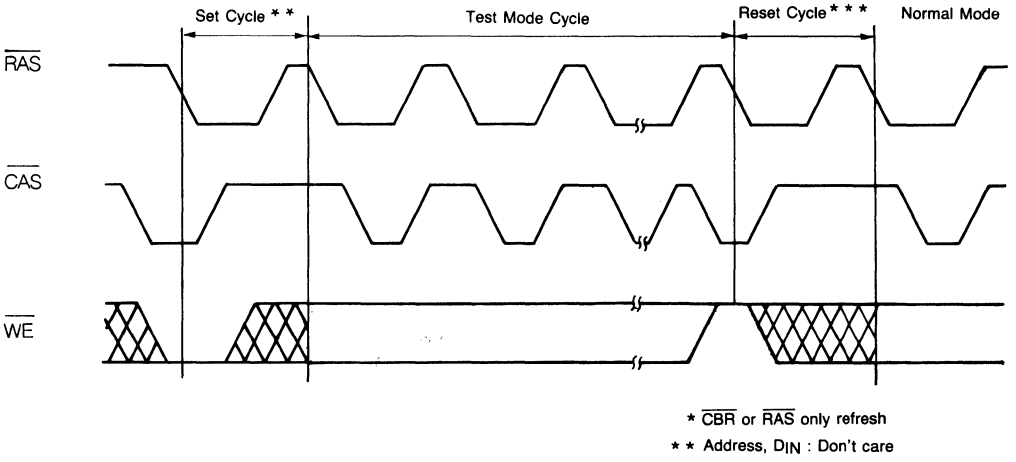


FIGURE 12. TEST MODE CYCLE

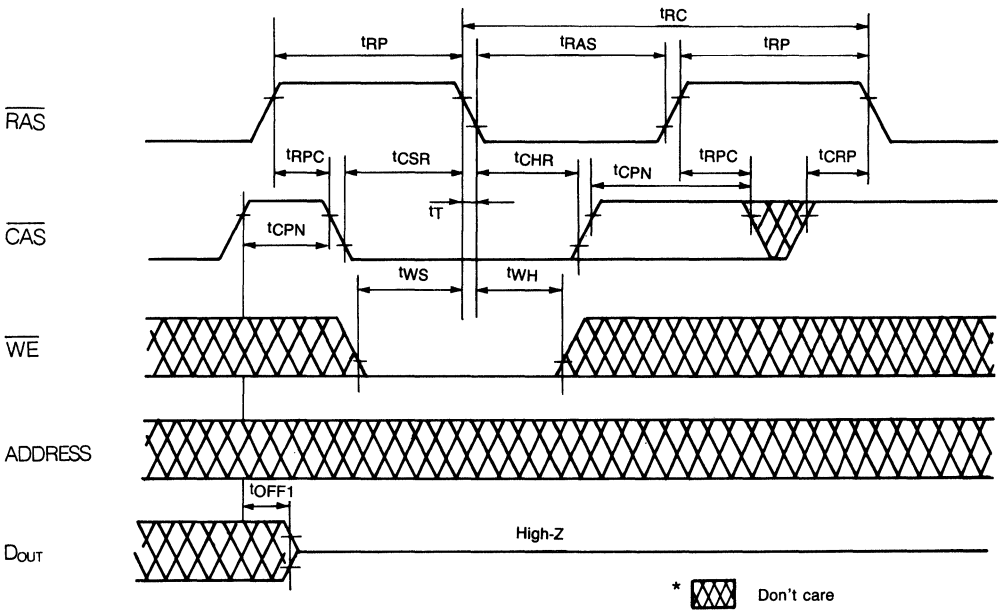


FIGURE 13. TEST MODE SET CYCLE

TEST MODE RESET CYCLE

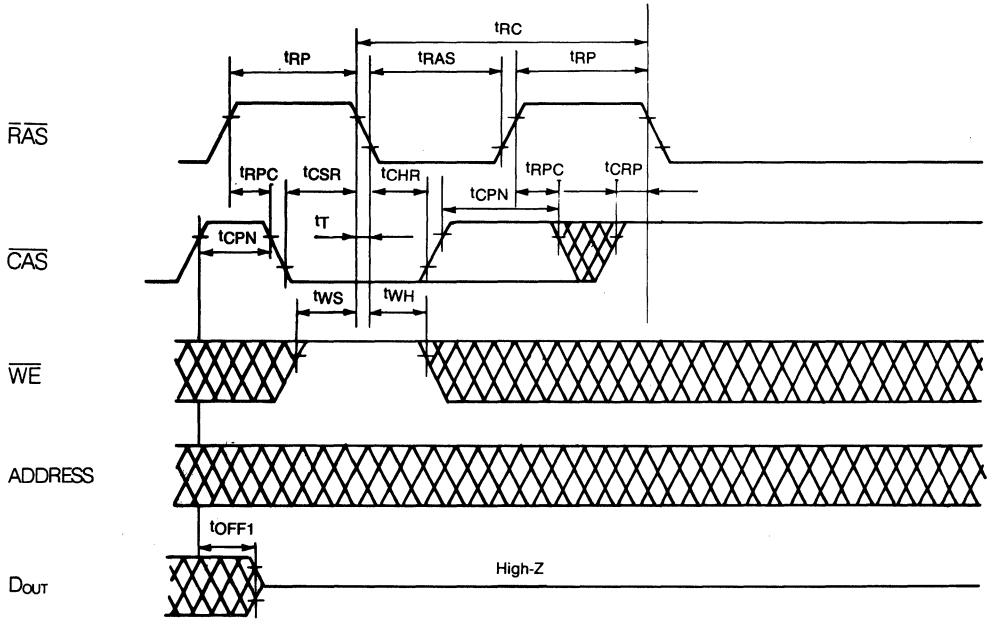


FIGURE 14. CAS-BEFORE RAS REFRESH CYCLE

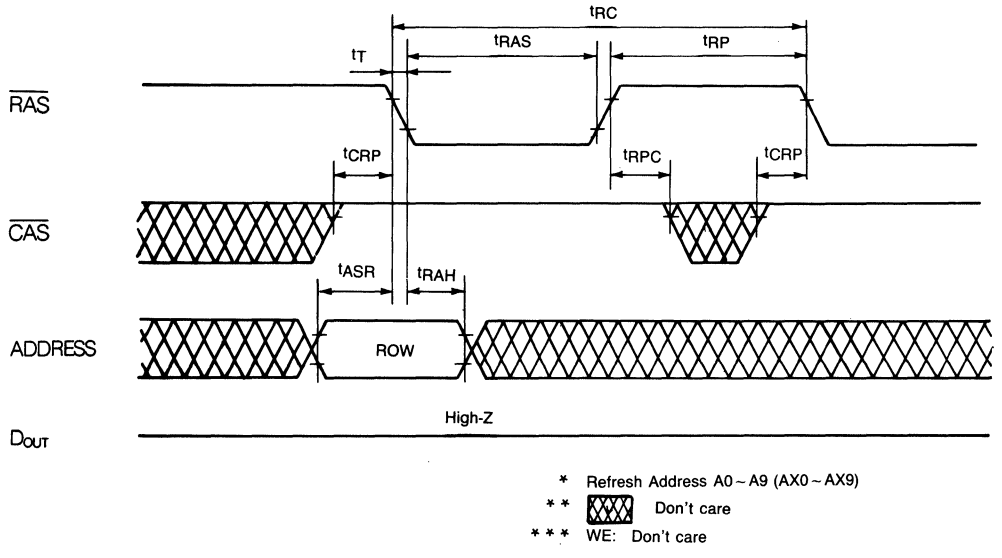


FIGURE 15. RAS-ONLY REFRESH CYCLE

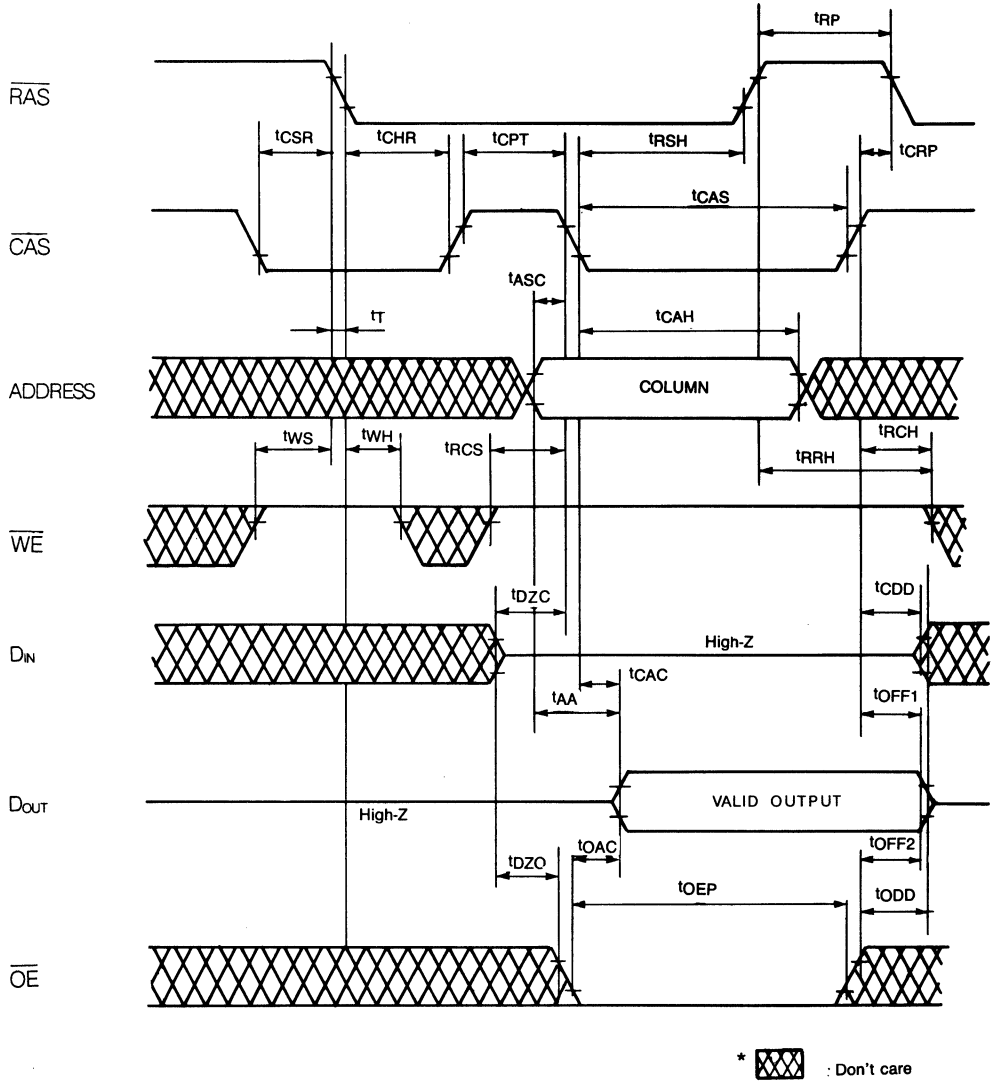


FIGURE 16. $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER CHECK CYCLE (READ)

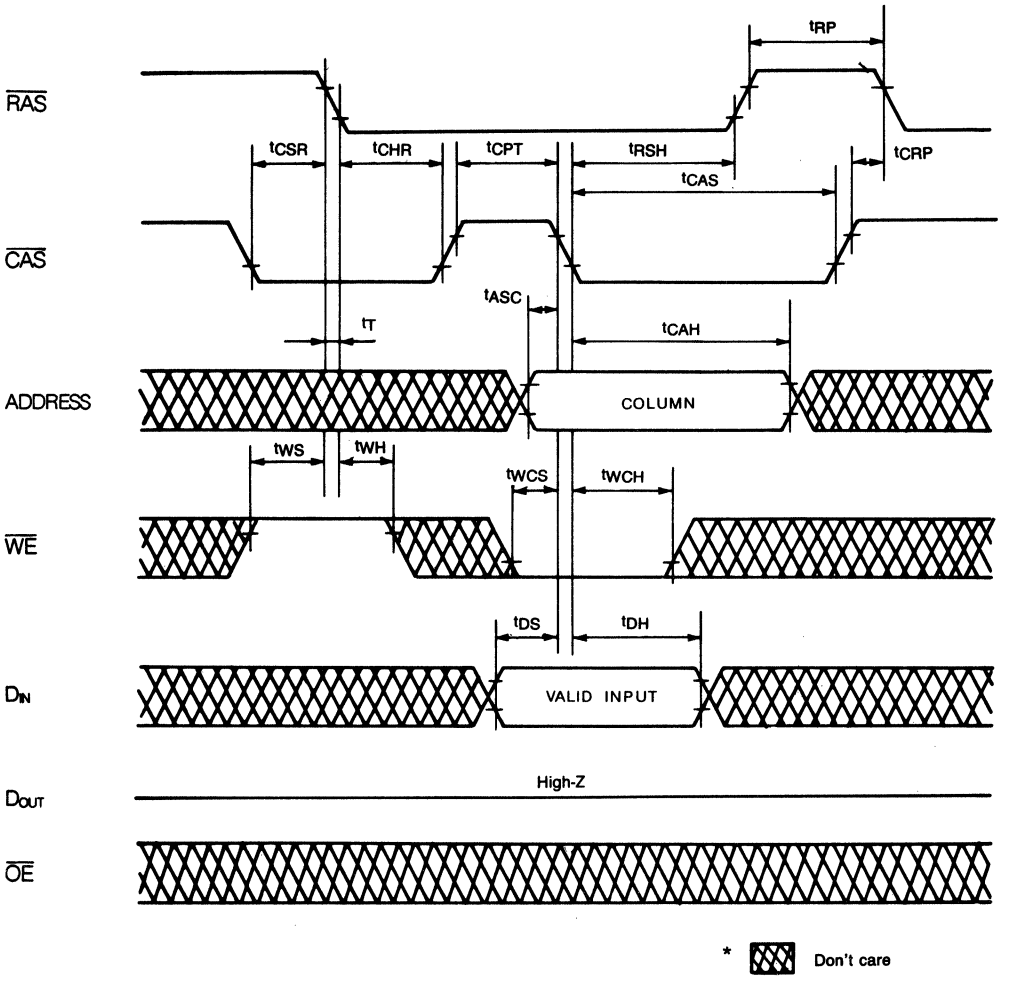
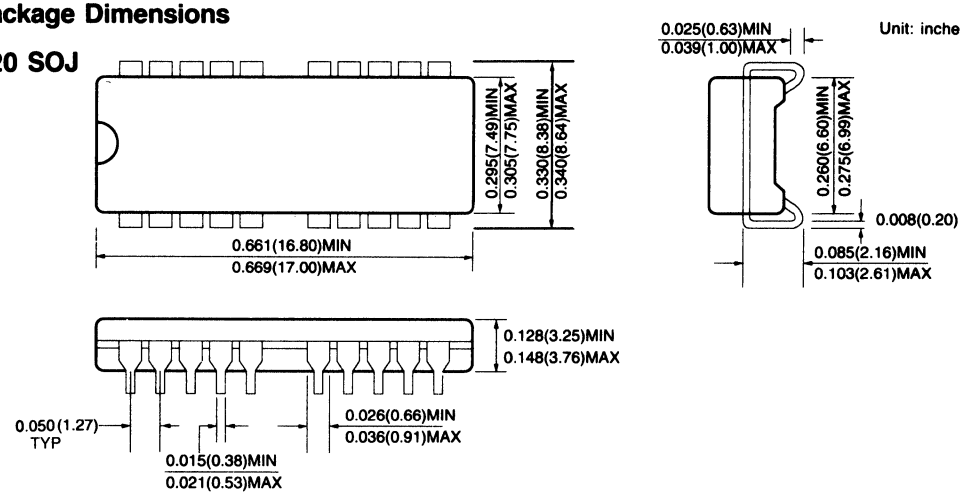


FIGURE 17. $\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH COUNTER CHECK CYCLE (WRITE)

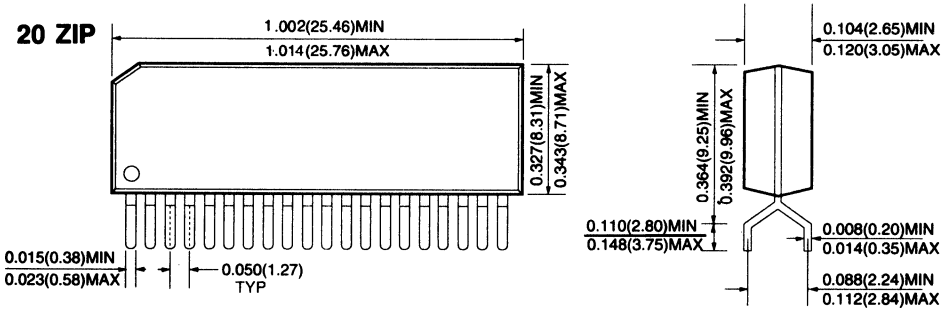
Package Dimensions

Unit: inche (mm)

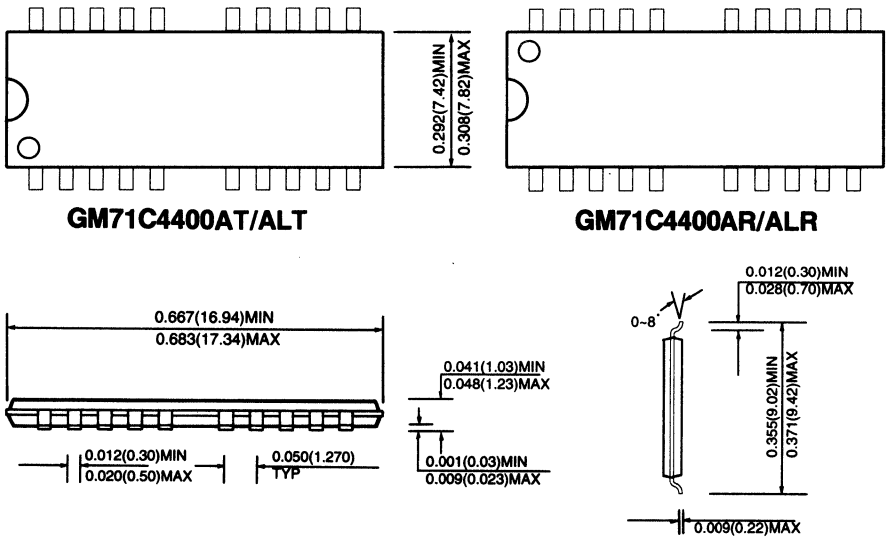
20 SOJ

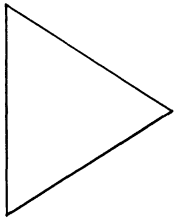


20 ZIP



20(26) TSOP (TYPE II)





GMM78256S–60/70/80/10

262,144 WORDS×8 BIT
CMOS DYNAMIC RAM MODULE

Description

The GMM78256S is a 256K×8 bits Dynamic RAM Module, mounted 2 pieces of 1M bit DRAM (GM71C4256ASJ, 256K×4) sealed in 20 pin SOJ package. The GMM78256S is a socket type memory module, suitable for easy interchange or addition of module. The GMM78256S provides common data inputs and outputs. It's module board has decoupling capacitors mounted under each DRAM.

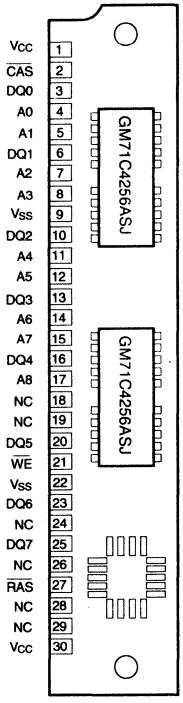
Features

- High Density Standard 30 Pin mounting 2 pcs of 1M DRAM GM71C4256ASJ (SOJ)
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit: ns)

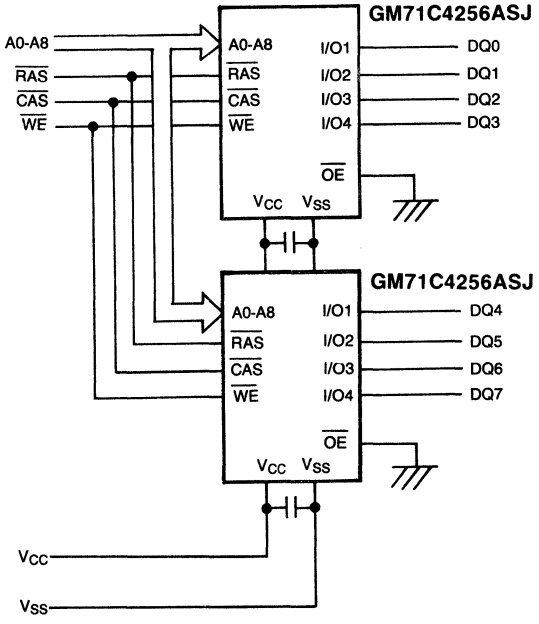
	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GM78256S-60	60	20	120	45
GM78256S-70	70	20	130	50
GM78256S-80	80	25	160	55
GM78256S-10	100	25	190	55

- Low Power
  Active: 990/880/770/660mW (MAX)
  Standby: 11mW (CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 512 Refresh Cycles/8ms

Pin Configuration (Top View)



Block Diagram



Pin Description

Pin	Function	Pin	Function
A0~A8	Address Inputs	$\overline{WE}$	Read/Write Enable
DQ0~DQ7	Data Input/Data Output	V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (+5V)
$\overline{CAS}$	Column Address Strobe	NC	No Connection

Note: 1. Common $\overline{CAS}$ control for eight common data-in and data-out lines.
2. The common control for one separate pair of data-in and data-out lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out.

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0~70	°C
T_{STG}	Storage Temperature (plastic)	-55~125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-1.0~7.0	V
V_{CC}	Power Supply Voltage	-1.0~7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	2.0	W

*Note: Stress greater than above listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions (T_A=0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	6.5	V	1
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	1

Note: 1. All voltages referenced to V_{SS}

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	180	mA	1,2
		70ns	—	160		
		80ns	—	140		
		100ns	—	120		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	4	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	—	180	mA	2
		70ns	—	160		
		80ns	—	140		
		100ns	—	120		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	60ns	—	160	mA	1,3
		70ns	—	140		
		80ns	—	120		
		100ns	—	100		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V)		—	2	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	160	mA	
		70ns	—	140		
		80ns	—	140		
		100ns	—	120		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	10	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V) All other Pins Not Under Test = 0V		−20	20	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		−10	10	μA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

AC Electrical Characterstics

Refer to the GM71C4256A/AL data sheet for AC Characteristics.
The GMM78256S writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$(min)).
Delayed write cycle is not available because of I/O common.

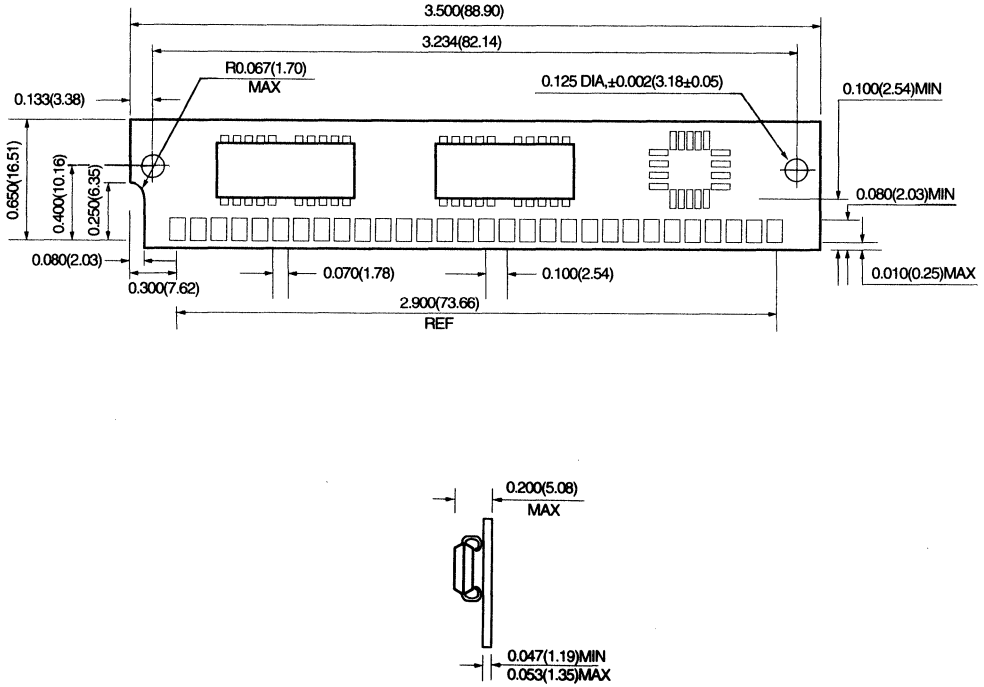
Capacitance (V_{CC} = 5V ± 10%, T_A = 25°C, f = 1MHz)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	—	30	pF	1
C_{I2}	Input Capacitance (Clocks)	—	36	pF	1,2
$C_{I/O}$	I/O Capacitance (DQ0 ~ DQ7)	—	17	pF	1,2

Note: 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

Package Dimensions

Unit: inches (mm)



Tolerance: ±0.005(0.13) unless otherwise specified.

GoldStar
GOLDSTAR ELECTRON CO., LTD.

GMM79256NS-70/80/10

262,144 WORDS×9 BIT
CMOS DYNAMIC RAM MODULE

Description

The GMM79256NS is a 256K×9 bits Dynamic RAM Module, mounted 2 pieces of 1M bit DRAM (GM71C4256ASJ, 256K×4) sealed in 20 pin SOJ package and a 256K bit DRAM (GM71C-256A, 256K×1) in 18 pin PLCC package. The GMM79256NS is a socket type memory module, suitable for easy interchange or addition of module. The GMM79256NS provides common data inputs and outputs, and also provides separate I/O on parity bit for parity check. It's module board has decoupling capacitors mounted under each DRAM.

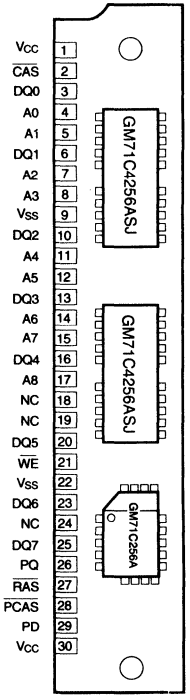
Features

- High Density Standard 30 pin mounting 2 pcs of 1M DRAM GM71C4256ASJ (SOJ) and a 256K DRAM GM71C256A(PLCC)
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit : ns)

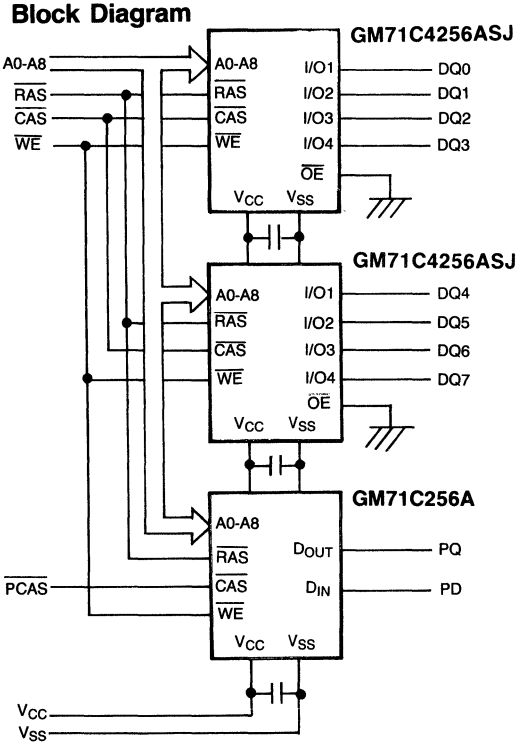
	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GMM79256NS-70	70	20	130	50
GMM79256NS-80	80	25	160	55
GMM79256NS-10	100	25	190	60

- Low Power
  Active: 1,265/1,100/935mW (MAX)
  Standby: 27.5mW (CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 512 Refresh Cycles/8ms

Pin Configuration (Top View)



Block Diagram



Pin Description

Pin	Function	Pin	Function
A0~A8	Address	$\overline{WE}$	Read/Write Enable
DQ0~DQ7	Data Input/Data Output	PD	Data in for Parity
$\overline{RAS}$	Row Address Strobe	PQ	Data out for Parity
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{PCAS}$	$\overline{CAS}$ for Parity	V_{CC}	Power (+5V)
NC	No Connection		

Note: 1. Common $\overline{CAS}$ control for eight common data-in and data-out lines.
2. The common control for one separate pair of data-in and data-out lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out.

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0~70	°C
T_{STG}	Storage Temperature	-55~125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-1.0~7.0	V
V_{CC}	Power Supply Voltage	-1.0~7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	3.0	W

*Note: Stress greater than above listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions (T_A=0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	6.5	V	1
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	1

Note: 1. All voltages referenced to V_{SS}

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	70ns	—	230	mA	1,2
		80ns	—	200		
		100ns	—	170		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	7.5	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	70ns	—	230	mA	2
		80ns	—	200		
		100ns	—	170		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	70ns	—	185	mA	1,3
		80ns	—	160		
		100ns	—	130		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V)		—	5	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	70ns	—	210	mA	
		80ns	—	200		
		100ns	—	170		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	14	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V) All other Pins Not Under Test = 0V	PD, $\overline{PCAS}$	−10	10	μA	
		ADDR., $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	−30	30		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		−10	10	μA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

Capacitance (V_{CC}=5V ± 10%, T_A=25°C, f=1MHz)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	—	30	pF	1
C_{I2}	Input Capacitance (Clocks)	—	36	pF	1,2
C_{I3}	Input Capacitance (PD)	—	10	pF	1
$C_{I/O}$	I/O Capacitance (DQ0~DQ7)	—	17	pF	1,2
C_O	Output Capacitance (PQ)	—	10	pF	1,2

Note 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable D_{OUT}.

AC Electrical Characterstics (V_{CC}=5V±10% T_A=0~70°C, Note 1, 14)

The GMM79256NS writes data only in early write cycle (twcs≥twcs (min)).
Delayed write cycle is not available because of I/O common.

Read, Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GMM79256NS-70		GMM79256NS-80		GMM79256NS-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	130	—	160	—	190	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	70	—	80	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10,000	80	10,000	100	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	25	10,000	25	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	15	—	15	—	15	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	20	—	20	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	55	25	75	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	20	40	20	55	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	25	—	25	—	30	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70	—	80	—	100	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	15	—	15	—	15	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	—	8	—	8	—	8	ms	

Read Cycle

Symbol	Parameter	GMM79256NS-70		GMM79256NS-80		GMM79256NS-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	70	—	80	—	100	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	25	—	25	ns	3,4
t_{AA}	Access Time from Column Address	—	35	—	40	—	45	ns	3,5
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	10	—	10	—	10	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35	—	40	—	45	—	ns	
t_{OFF}	Output Buffer Turn-off Delay Time	—	20	—	20	—	25	ns	6

Write Cycle

Symbol	Parameter	GMM79256NS-70		GMM79256NS-80		GMM79256NS-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	20	—	20	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	25	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	25	—	25	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	20	—	20	—	ns	11

Refresh Cycle

Symbol	Parameter	GMM79256NS-70		GMM79256NS-80		GMM79256NS-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	20	—	25	—	30	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

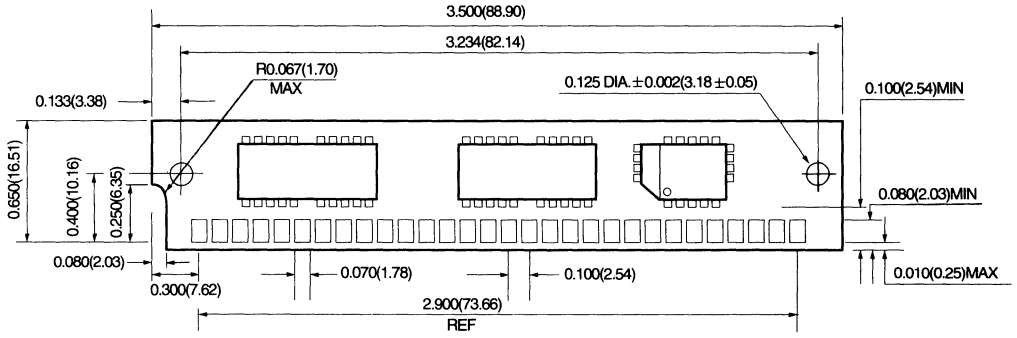
Symbol	Parameter	GMM79256NS-70		GMM79256NS-80		GMM79256NS-10		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast-Page Mode Cycle Time	50	—	55	—	55	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	—	15	—	20	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	100,000	—	100,000	—	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	45	—	50	—	55	ns	13
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45	—	50	—	50	—	ns	

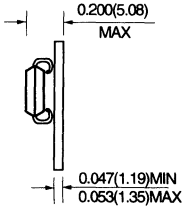
Notes :

1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RCD}(max)$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS} is not restrictive operating parameters. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

Package Dimensions

Unit: inches (mm)





Tolerance: ±0.005(0.13) unless otherwise specified.

GMM781000S-60/70/80/10

1,048,576 WORDS×8 BIT
CMOS DYNAMIC RAM MODULE

Description

The GMM781000S is 1M×8 Dynamic RAM Module organized as 1,048,576×8 bits and consists of eight 1M bit DRAM (GM71C1000SJ) in 20/26 pin small out-line J-form on a 30 pin single in-line package. GMM781000S is a socket type memory module, suitable for easy exchange or addition of module. The GMM781000S provides common data inputs and outputs. It's module board has decoupling capacitors mounted under each DRAM.

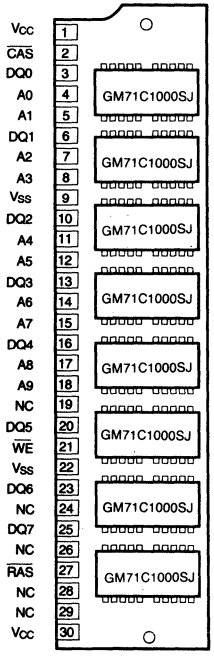
Features

- High Density JEDEC standard 30 pin mounting 8 pcs of 1M DRAM GM71C1000SJ (SOJ)
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time and Cycle Time (Unit: ns)

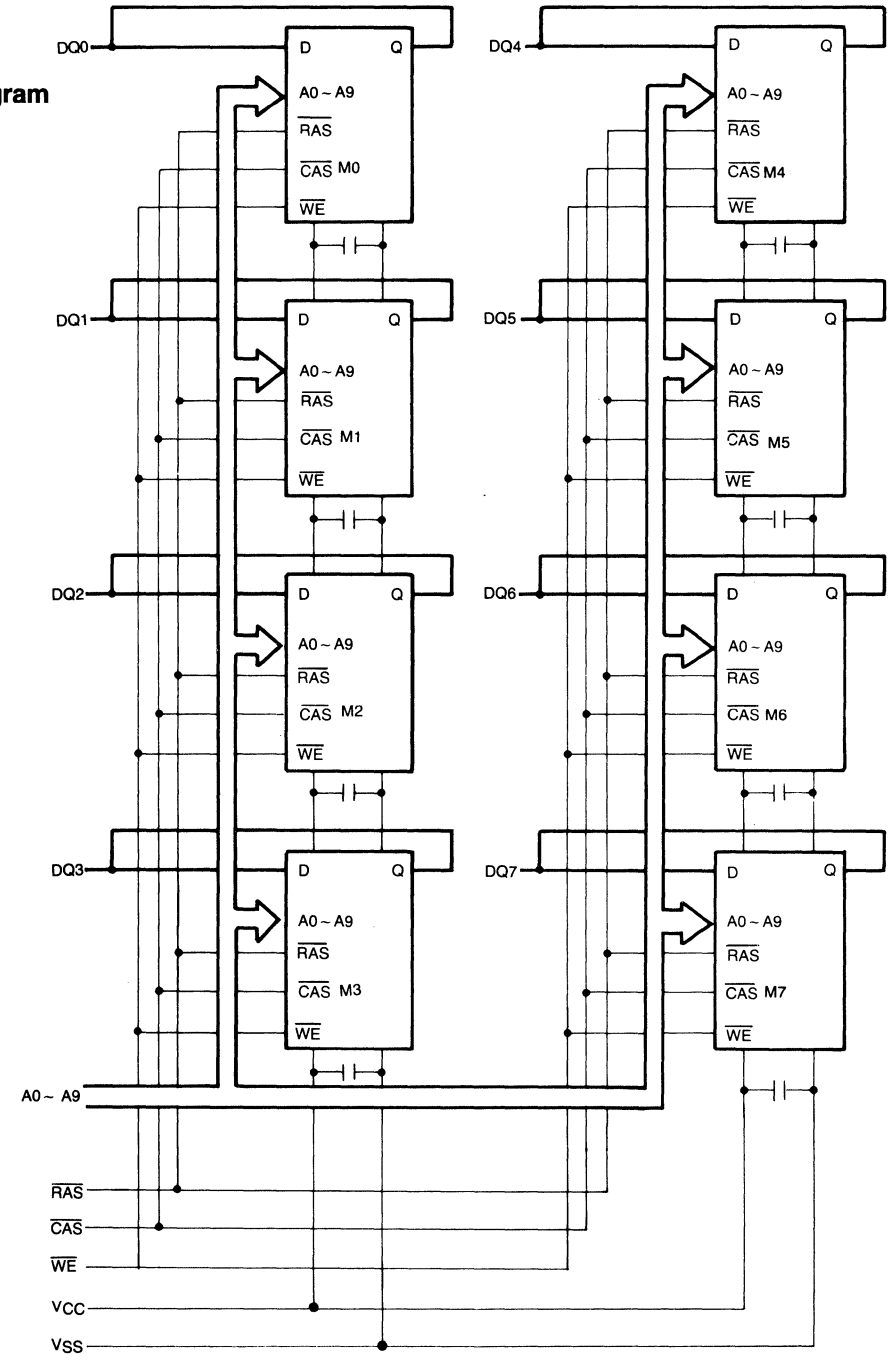
	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GMM781000S-60	60	20	120	45
GMM781000S-70	70	20	130	50
GMM781000S-80	80	25	160	55
GMM781000S-10	100	25	190	55

- Low Power
  Active: 3,960/3,520/3,080/3,640 mW (MAX)
  Standby: 44mW (CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 512 Refresh Cycles/8 ms

Pin Configuration (Top View)



Block Diagram



*M0-M7: GM71C1000SJ

Pin Description

Pin	Function	Pin	Function
A0~A9	Address	$\overline{WE}$	Read/Write Enable
DQ0~DQ7	Data Input/Data Output	V_{CC}	Power (+5V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	NC	No Connection

Note: 1. Common $\overline{CAS}$ control for eight common data-in and data-out lines.
2. The common control for one separate pair of data-in and data-out lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out.

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0~70	°C
T_{STG}	Storage Temperature	-55~125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-1.0~7.0	V
V_{CC}	Power Supply Voltage	-1.0~7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	8	W

*Note: Stress greater than above listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions (T_A=0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	6.5	V	1
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	1

Note: 1. All Voltages referenced to V_{SS}

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	720	mA	1,2
		70ns	—	640		
		80ns	—	560		
		100ns	—	480		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	16	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	—	720	mA	2
		70ns	—	640		
		80ns	—	560		
		100ns	—	480		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	60ns	—	640	mA	1,3
		70ns	—	560		
		80ns	—	400		
		100ns	—	400		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V)		—	8	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	640	mA	
		70ns	—	560		
		80ns	—	480		
		100ns	—	400		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	40	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V) All Other Pins Not Under Test = 0V		−80	80	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		−20	20	μA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

AC Electrical Characterstics

Refer to the GM71C1000/L data sheet for AC characteristics.
The GMM781000S writes data only in early write cycle (t_{WCS} ≥ t_{WCS} (min)).
Delayed write cycle is not available because of I/O common.

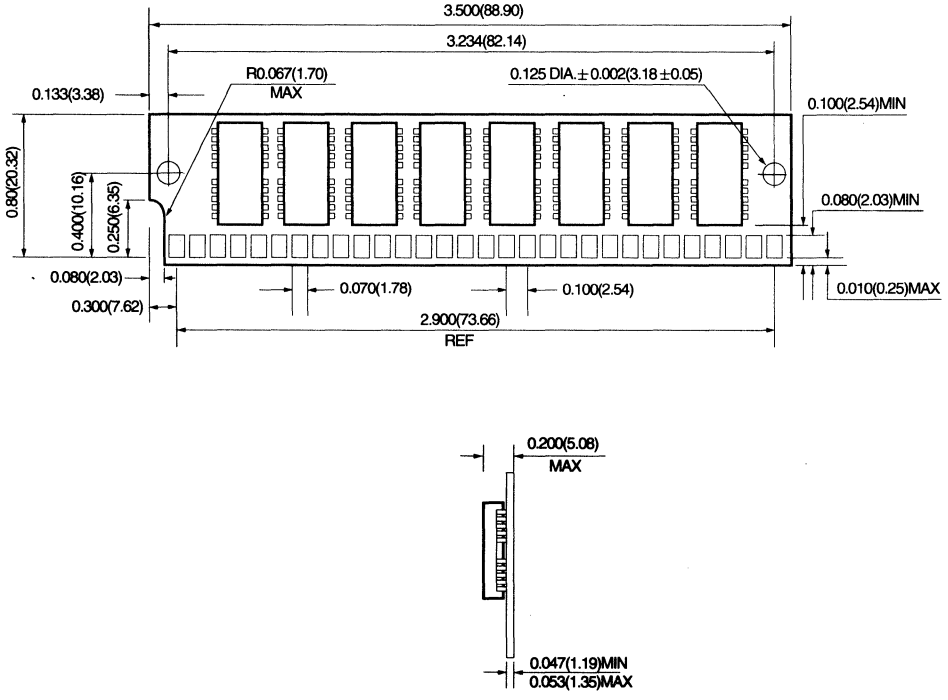
Capacitance (V_{CC}=5V ± 10%, T_A=25°C, f=1MHz)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	–	60	pF	1
C_{I2}	Input Capacitance (Clocks)	–	75	pF	1,2
$C_{I/O}$	I/O Capacitance (DQ0~DQ7)	–	17	pF	1,2

Note 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable D_{OUT}.

Package Dimensions

Unit: inches (mm)



Tolerence: ±0.005(0.13) unless otherwise specified.

GMM781000NS-60/70/80

1,048,576 WORDS×8 BIT
CMOS DYNAMIC RAM MODULE

Description

The GMM781000NS is a 1M×8 bits Dynamic RAM Module, mounted 2 pieces of 4M bit DRAM (GM71C4400AJ, 1M×4) sealed in 20 pin SOJ package. The GMM781000NS is a socket type memory module, suitable for easy interchange or addition of module. The GMM781000NS provides common data inputs and outputs.
It's module board has decoupling capacitors mounted for each DRAM.

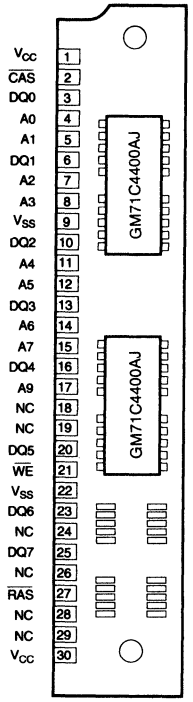
Features

- High Density Standard 30 pin mounting 2 pcs of 4M DRAM GM71C4400AJ (SOJ)
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit: ns)

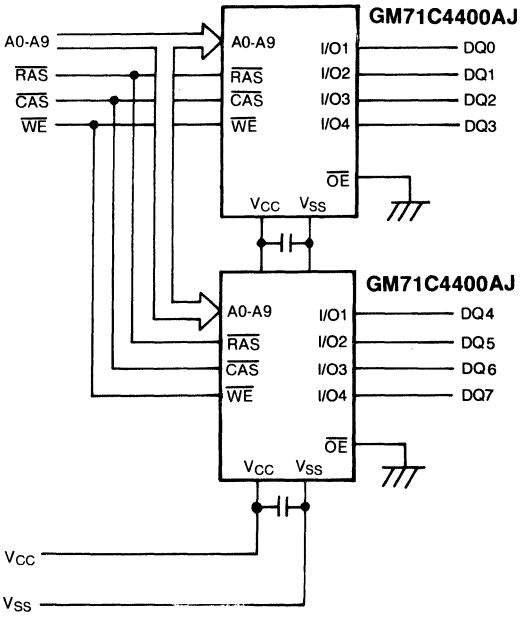
	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GMM781000NS-60	60	15	110	40
GMM781000NS-70	70	20	130	45
GMM781000NS-80	80	20	150	50

- Low Power
  Active: 1210/1100/990 mW (MAX)
  Standby: 11mW (CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16ms

Pin Configuration (Top View)



Block Diagram



Pin Description

Pin	Function	Pin	Function
A0~A9	Address	$\overline{WE}$	Read/Write Enable
DQ0~DQ7	Data Input/Data Output	V_{CC}	Power (+5V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	NC	No Connection

Note: 1. Common $\overline{CAS}$ control for eight common data-in and data-out lines.
2. The common control for one separate pair of data-in and data-out lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out.

Absolute Maximum Ratings*

Symbol	Parameter	Values	Unit
T_A	Ambient Temperature under Bias	0~70	°C
T_{STG}	Storage Temperature	-55~125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-1.0~7.0	V
V_{CC}	Power Supply Voltage	-1.0~7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	2.0	W

*Note: Stress greater than above under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions (T_A=0 ~ 70°C)

Symbol	Parameter	MIN	TYP	MAX	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	6.5	V	1
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	1

Note: 1 All voltages referenced to V_{SS}

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	220	mA	1,2
		70ns	—	200		
		80ns	—	180		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	4	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	—	220	mA	2
		70ns	—	200		
		80ns	—	180		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	60ns	—	220	mA	1,3
		70ns	—	200		
		80ns	—	180		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V)		—	2	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	220	mA	
		70ns	—	200		
		80ns	—	180		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	10	mA	1
$I_{I(L)}$	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 7V$) All Other Pins Not Under Test = 0V		−20	20	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 7V$)		−10	10	μA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

AC Electrical Characteristics

Refer to the GM71C4400A/AL data sheet for AC characteristics.
The GMM781000NS writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$(min)).
Delayed write cycle is not available because of I/O common.

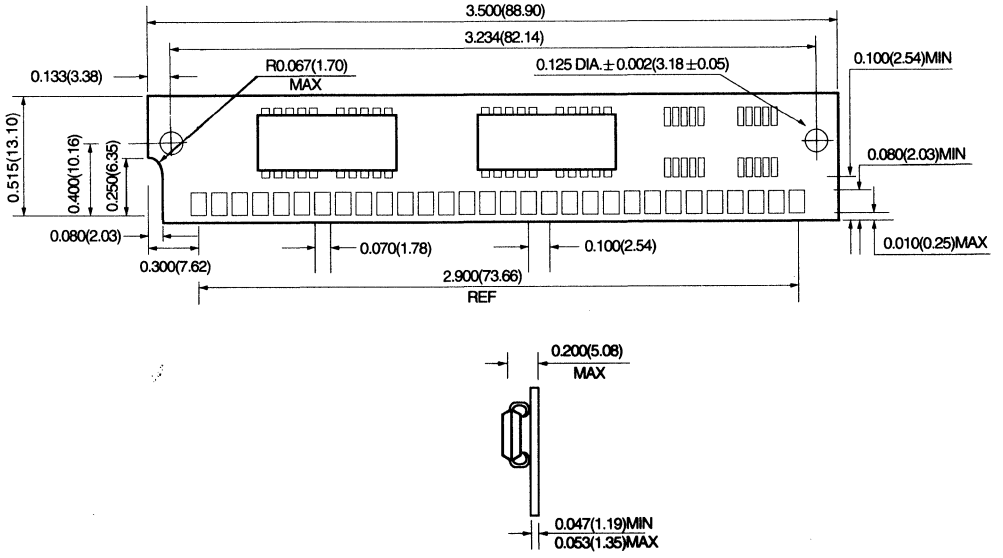
Capacitance(V_{CC} = 5V ± 10%, T_A = 25°C, f = 1MHz)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	—	20	pF	1
C_{I2}	Input Capacitance (Clocks)	—	20	pF	1,2
$C_{I/O}$	I/O Capacitance (DQ0 ~ DQ7)	—	17	pF	1,2

Note 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

Package Dimensions

Unit: inches (mm)



GMM791000S-60/70/80/10

1,048,576 WORDS×9 BIT
CMOS DYNAMIC RAM MODULE

Description

The GMM791000S is 1M×9 Dynamic RAM Module organized as 1,048,576×9 bits and consists of nine 1M bit DRAM (GM71C1000SJ) in 20/26 pin small out-line J-form on a 30 pin single in-line package. GMM791000S is a socket type memory module, suitable for easy exchange or addition of module. The GMM791000S provides common data inputs and outputs, and also provides separate I/O on parity bit for parity check. It's module board has decoupling capacitors mounted under each DRAM.

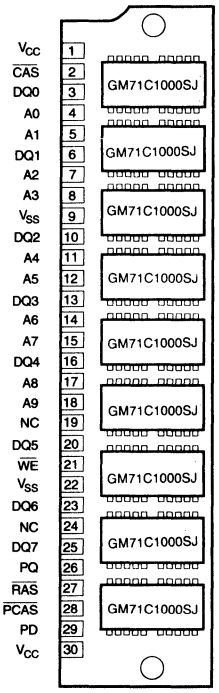
Features

- High Density JEDEC standard 30 pin mounting 9 pcs of 1M DRAM GM71C1000SJ (SOJ)
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit: ns)

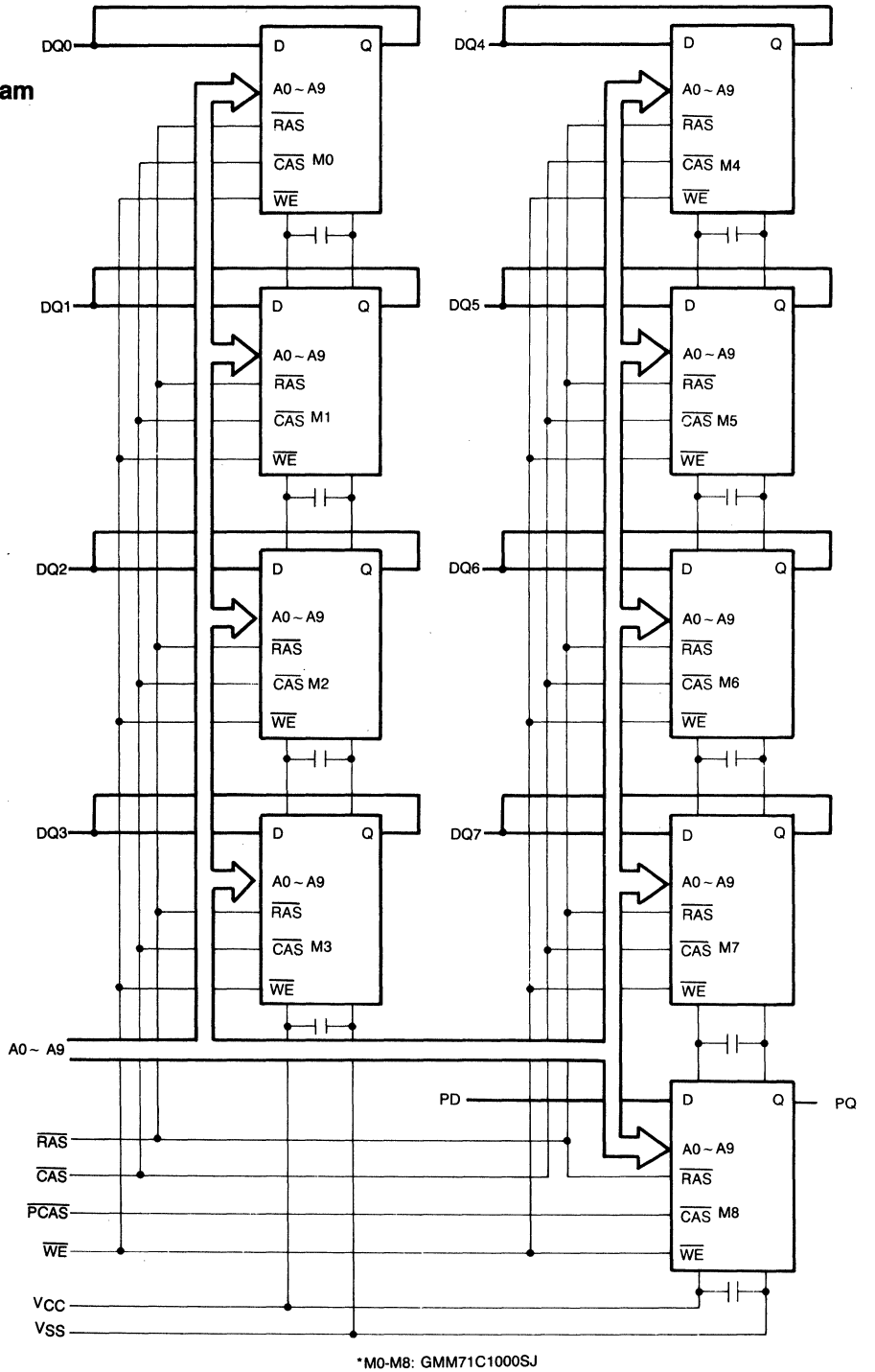
	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GMM791000S-60	60	20	120	45
GMM791000S-70	70	20	130	50
GMM791000S-80	80	25	160	55
GMM791000S-10	100	25	190	55

- Low Power
  Active: 4,455/3,960/3,465/2,970mW (MAX)
  Standby: 49.5mW (CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 512 Refresh Cycles/8ms

Pin Configuration (Top View)



Block Diagram



*M0-M8: GMM71C1000SJ

Pin Description

Pin	Function	Pin	Function
A0 ~ A9	Address	$\overline{WE}$	Read/Write Enable
DQ0 ~ DQ7	Data Input/Data Output	PD	Data In for Parity
$\overline{RAS}$	Row Address Strobe	PQ	Data Out for Parity
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{PCAS}$	$\overline{CAS}$ for Parity	V_{CC}	Power (+5V)
NC	No Connection		

Note: 1. Common $\overline{CAS}$ control for eight common data-in and data-out lines.
2. The common control for one separate pair of data-in and data-out lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out.

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature	−55 ~ 125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−1.0 ~ 7.0	V
V_{CC}	Power Supply Voltage	−1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	9	W

*Note: Stress greater than above listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	6.5	V	1
V_{IL}	Input Low Voltage	−1.0	—	0.8	V	1

Note: 1. All voltages referenced to V_{SS}

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	810	mA	1,2
		70ns	—	720		
		80ns	—	630		
		100ns	—	540		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	18	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	—	810	mA	2
		70ns	—	720		
		80ns	—	630		
		100ns	—	540		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	60ns	—	720	mA	1,3
		70ns	—	630		
		80ns	—	450		
		100ns	—	450		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V)		—	9	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	720	mA	
		70ns	—	630		
		80ns	—	540		
		100ns	—	450		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	45	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V) All Other Pins Not Under Test = 0V	PD, $\overline{PCAS}$	−10	10	μA	
		ADDR, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	−90	90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)	PQ	−10	10	μA	
		DQ	−20	20		

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

AC Electrical Characterstics

Refer to the GM71C1000/L data sheet for AC characteristics.
The GMM791000S writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$ (min)).
Delayed write cycle is not available because of I/O common.

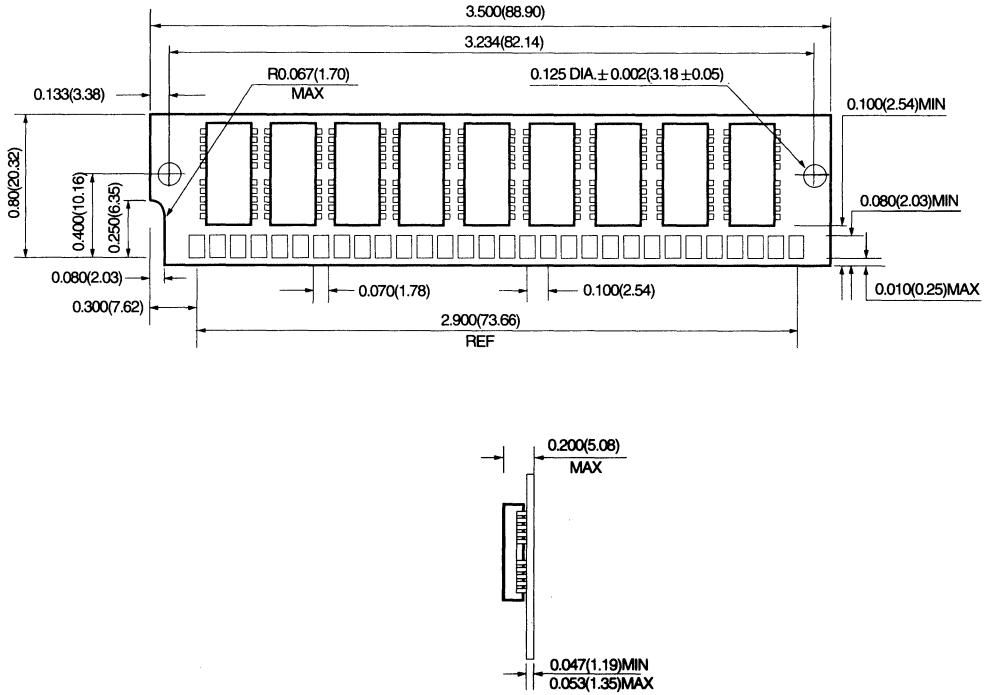
Capacitance (V_{CC} = 5V ± 10%, T_A = 25°C, f = 1MHz)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	—	60	pF	1
C_{I2}	Input Capacitance (Clocks)	—	75	pF	1,2
C_{I3}	Input Capacitance (PD)	—	10	pF	1
C_{I4}	Input Capacitance ($\overline{PCAS}$)	—	10	pF	1
$C_{I/O}$	I/O Capacitance (DQ0 ~ DQ7)	—	17	pF	1,2
C_O	Output Capacitance (PQ)	—	12	pF	1,2

Note 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

Package Dimensions

Unit: inches (mm)



Tolerance: ±0.005(0.13) unless otherwise specified.

GMM791000NS-60/70/80

1,048,576 WORDS×9 BIT
CMOS DYNAMIC RAM MODULE

Description

The GMM791000NS is a 1M×9 bits Dynamic RAM Module, mounted 2 pieces of 4M bit DRAM (GM71C4400AJ, 1M×4) sealed in 20 pin SOJ package and an 1M bit DRAM (GM 71C-1000SJ, 1M×1) in 20 pin SOJ package. The GMM791000NS is a socket type memory module, suitable for easy interchange or addition of module. The GMM791000NS provides common data inputs and outputs, and also provides separate I/O on parity bit for parity check. It's module board has decoupling capacitors mounted under each DRAM.

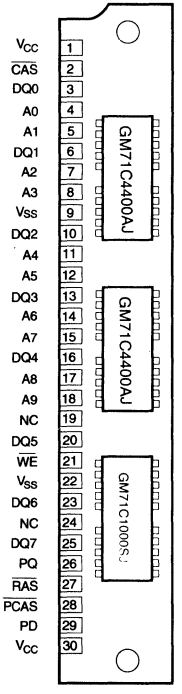
Features

- High Density Standard 30 pin mounting 2 pcs of 4M DRAM and an 1M DRAM
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit: ns)

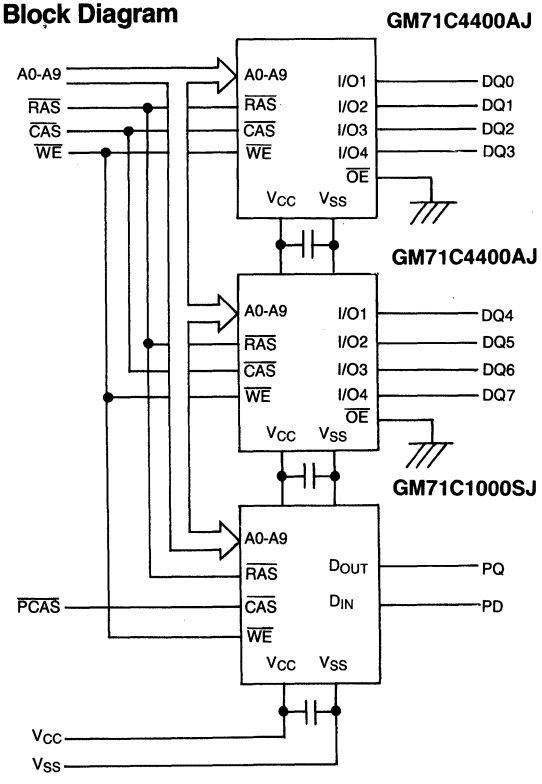
	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GMM791000NS-60	60	20	120	45
GMM791000NS-70	70	20	130	50
GMM791000NS-80	80	25	160	55

- Low Power
  Active: 1,705/1,540/1,375mW (MAX)
  Standby: 16.5mW (CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16ms

Pin Configuration (Top View)



Block Diagram



Pin Description

Pin	Function	Pin	Function
A0 ~ A9	Address	$\overline{WE}$	Read/Write Enable
DQ0 ~ DQ7	Data Input/Data Output	PD	Data In for Parity
$\overline{RAS}$	Row Address Strobe	PQ	Data Out for Parity
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{PCAS}$	$\overline{CAS}$ for Parity	V_{CC}	Power (+5V)
NC	No Connection		

Note: 1. Common $\overline{CAS}$ control for eight common data-in and data-out lines.
2. The common control for one separate pair of data-in and data-out lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out.

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature	−55 ~ 125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−1.0 ~ 7.0	V
V_{CC}	Power Supply Voltage	−1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	3.0	W

*Note: Stress greater than above listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Recommended Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	6.5	V	1
V_{IL}	Input Low Voltage	−1.0	—	0.8	V	1

Note: 1. All Voltages referenced to V_{SS}

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		Min	Max	Unit	Note
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	310	mA	1,2
		70ns	—	280		
		80ns	—	250		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	6	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	—	310	mA	2
		70ns	—	280		
		80ns	—	240		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	60ns	—	300	mA	1,3
		70ns	—	270		
		80ns	—	230		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V)		—	3	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	300	mA	
		70ns	—	270		
		80ns	—	240		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	15	mA	1
$I_{I(L)}$	Input Leakage Current Any Input ($0V \leq V_{IN} \leq 7V$) All Other Pins Not Under Test = 0V	PD, $\overline{PCAS}$	−10	10	μA	
		ADDR., $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	−30	30		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 7V$)		−10	10	μA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

Capacitance (V_{CC}=5V ± 10%, T_A=25°C, f=1MHz)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	—	25	pF	1
C_{I2}	Input Capacitance (Clocks)	—	25	pF	1,2
C_{I3}	Input Capacitance (PD)	—	10	pF	1
$C_{I/O}$	I/O Capacitance (DQ0 ~ DQ7)	—	15	pF	1,2
C_O	Output Capacitance (PQ)	—	10	pF	1,2

Note 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable D_{OUT}.

AC Electrical Characteristics (V_{CC}=5V±10%, T_A=0~70°C, Note 1, 14)

The GMM791000NS writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$(min)).
Delayed write cycle is not available because of I/O common.

Read, Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GMM791000NS-60		GMM791000NS-70		GMM791000NS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	120	—	130	—	160	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	50	—	70	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	12	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	20	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	22	55	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	17	40	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	—	16	—	16	—	16	ms	

Read Cycle

Symbol	Parameter	GMM791000NS-60		GMM791000NS-70		GMM791000NS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	—	80	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	20	—	25	ns	3,4
t_{AA}	Access Time from Column Address	—	30	—	35	—	40	ns	3,5
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	10	—	10	—	10	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	ns	
t_{OFF}	Output Buffer Turn-off Delay Time	—	20	—	20	—	20	ns	6

Write Cycle

Symbol	Parameter	GMM791000NS-60		GMM791000NS-70		GMM791000NS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	15	—	20	—	ns	
t_{WP}	Write Command Pulse Width	10	—	10	—	10	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	20	—	25	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	15	—	20	—	ns	11

Refresh Cycle

Symbol	Parameter	GMM791000NS-60		GMM791000NS-70		GMM791000NS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	15	—	15		20	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

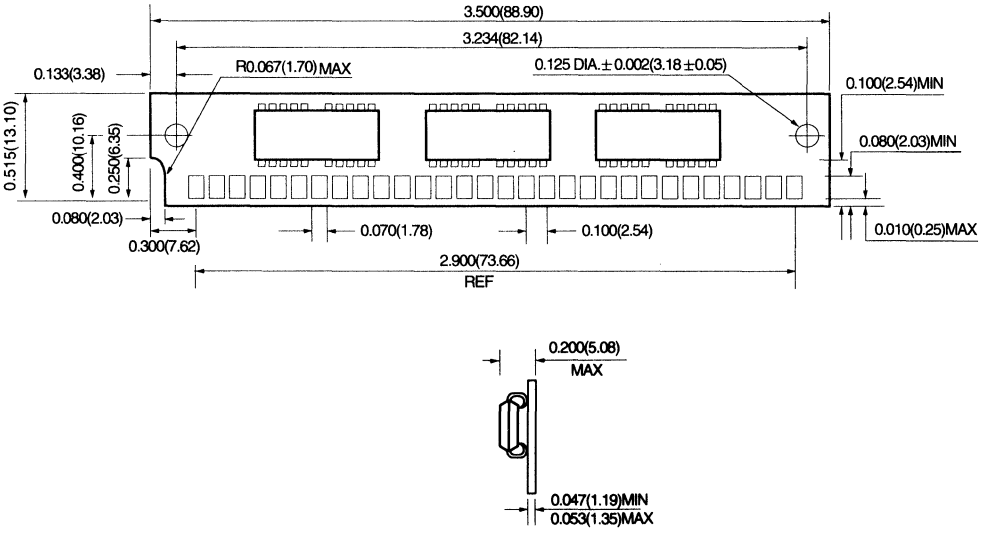
Symbol	Parameter	GMM791000NS-60		GMM791000NS-70		GMM791000NS-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	45	—	50	—	55	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	100,000	—	100,000	—	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	—	50	ns	13
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	50	—	ns	

Notes :

1. AC measurements assume $t_T = 5ns$.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RCD}(max)$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met. $t_{RAD}(max)$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS} is not restrictive operating parameters. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

Package Dimensions

Unit: inches (mm)



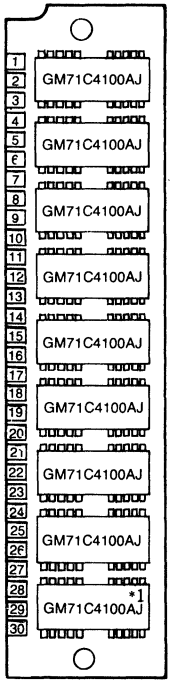
Tolerance: ±0.005(0.13) unless otherwise specified.

GMM784000S-60/70/80
4,194,304 WORDS×8 BIT
GMM794000S-60/70/80
4,194,304 WORDS×9 BIT
CMOS DYNAMIC RAM MODULE

Description

The GMM78(9)4000S is 4M×8(9) Dynamic RAM MODULE organized as 4,194,304×8(9) bits and consists of eight(nine) 4M bit DRAM(GM71C4100-AJ) in 20/26 pin small out-line J-form on a 30 pin single in-line package. These are a socket type memory module, suitable for easy interchange or addition of module, and provide common data inputs and outputs. It's module board has decoupling capacitors mounted under each DRAM. The GMM794000S provides separate I/O on parity bit for parity check.

Pin Configuration (Top View)



Features

- High Density JEDEC standard 30 pin mounting
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit: ns)

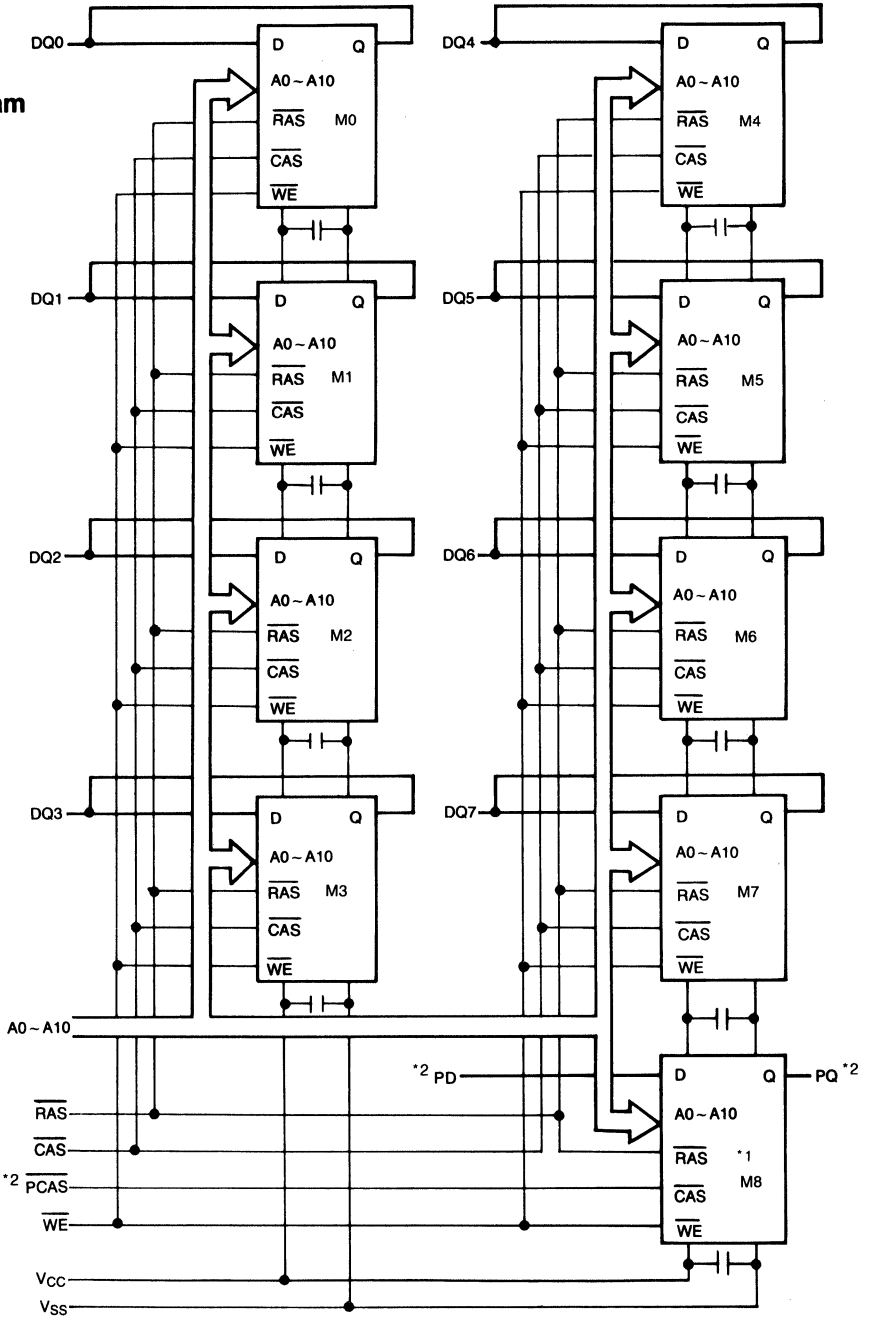
	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
GMM78(9)4000S-60	60	15	110	40
GMM78(9)4000S-70	70	20	130	45
GMM78(9)4000S-80	80	20	150	50

- Low Power
  Active
  — 4M×8: 4,840/4,400/3,960 mW(MAX)
  — 4M×9: 5,445/4,950/4,455 mW(MAX)
  Standby
  — 4M×8: 44.0 mW(CMOS level: MAX)
  — 4M×9: 49.5 mW(CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh, Hidden Refresh Capability
- All inputs and outputs TTL Compatible
- 1,024 Refresh Cycles/16ms

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	V_{SS}
3	DQ0	13	DQ3	23	DQ6
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ7
6	DQ1	16	DQ4	26	PQ*2
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	PCAS*2
9	V_{SS}	19	A10	29	PD*2
10	DQ2	20	DQ5	30	V_{CC}

*NOTE: 1. This component is not included in the GMM784000S.
2. In case of GMM784000S, Pin 26, 28 and Pin 29 are not connected.

Block Diagram



Note: 1. This component is not included in the GMM784000S.
2. In case of GMM784000S, PD, PQ and $\overline{\text{PCAS}}$ pin are not connected.
3. M0-M8: GM71C4100AJ

Pin Description

Pin	Function	Pin	Function
A0~A10	Address	$\overline{WE}$	Read/Write Enable
DQ0~DQ7	Data Input/Data Output	PD	Data in for Parity
$\overline{RAS}$	Row Address Strobe	PQ	Data out for Parity
$\overline{CAS}$	Column Address Strobe	V_{CC}	Power (+5V)
$\overline{PCAS}$	$\overline{CAS}$ for Parity	V_{SS}	Ground
NC	No Connection		

Note: 1. Common $\overline{CAS}$ controls for eight common data-in and data-out lines.
2. The common controls for one separate pair of data-in and data-out lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out.

Absolute Maximum Ratings*[1]

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0~70	°C
T_{STG}	Storage Temperature	-55~125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-1.0~7.0	V
V_{CC}	Power Supply Voltage	-1.0~7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	8/9*[2]	W

*Note: 1. Stress greater than above listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. In case of GMM794000S.

Recommended Operating Conditions (T_A=0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	6.5	V	1
V_{IL}	Input Low Voltage	-1.0	—	0.8	V	1

Note: 1. All Voltages referenced to V_{SS}

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		GMM784000S		GMM794000S		Unit	Note
			Min	Max	Min	Max		
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	880	—	990	mA	1,2
		70ns	—	800	—	900		
		80ns	—	720	—	810		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH}, D_{OUT} = High-Z)		—	16	—	18	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Refresh Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	—	880	—	990	mA	2
		70ns	—	800	—	900		
		80ns	—	720	—	810		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	60ns	—	880	—	990	mA	1,3
		70ns	—	800	—	900		
		80ns	—	720	—	810		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V, D_{OUT} = High-Z)		—	8	—	9	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	880	—	990	mA	
		70ns	—	800	—	900		
		80ns	—	720	—	810		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	40	—	45	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V) All Other Pins Not Under Test = 0V	PD, $\overline{PCAS}$	—	—	−10	10	μA	4
		ADDR., $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	−80	80	−90	90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)	PQ	—	—	−10	10	μA	4
		DQ	−20	20	−20	20		

Note) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}
4. In case of GMM794000S.

Capacitance (V_{CC}=5V ± 10%, T_A=25°C, f=1MHz)

Symbol	Parameter	Min	Max	Unit	Note
C_{I1}	Input Capacitance (Address)	—	60	pF	1
C_{I2}	Input Capacitance (Clocks)	—	75	pF	1,2
C_{I3}	Input Capacitance (PD)	—	10	PF	1,3
C_{I4}	Input Capacitance ($\overline{PCAS}$)	—	10	pF	1,3
$C_{I/O}$	I/O Capacitance (DQ0 ~ DQ7)	—	17	pF	1,2
C_O	Output Capacitance (PQ)	—	12	pF	1,2,3

Note: 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable D_{OUT}.
3. In case of GMM794000S.

AC Electrical Characteristics (V_{CC}=5V±10%, T_A=0 to +70°C, Note 1, 14)

The GMM78(9)4000S writes data only in early write cycle ($t_{WCS} \geq t_{WCS}$(min)).
Delayed write cycle is not available because of I/O common.

Read, Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GMM78(9)4000S-60		GMM78(9)4000S-70		GMM78(9)4000S-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	150	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	60	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	20	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	10	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	60	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	—	16	—	16	—	16	ms	

Read Cycle

Symbol	Parameter	GMM78(9)4000S-60		GMM78(9)4000S-70		GMM78(9)4000S-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	—	80	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	—	20	ns	3,4
t_{AA}	Access Time from Column Address	—	30	—	35	—	40	ns	3,5
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	ns	
t_{RRH}	Read Command Hold Time $\overline{RAS}$	0	—	0	—	0	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	ns	
t_{OFF}	Output Buffer Turn-off Time	0	15	0	20	0	20	ns	6

Write Cycle

Symbol	Parameter	GMM78(9)4000S-60		GMM78(9)4000S-70		GMM78(9)4000S-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	10	—	10	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	20	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	15	—	15	—	ns	11

Refresh Cycle

Symbol	Parameter	GMM78(9)4000S-60		GMM78(9)4000S-70		GMM78(9)4000S-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	10	—	ns	
t_{CPN}	$\overline{CAS}$ Precharge time in Normal Mode	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

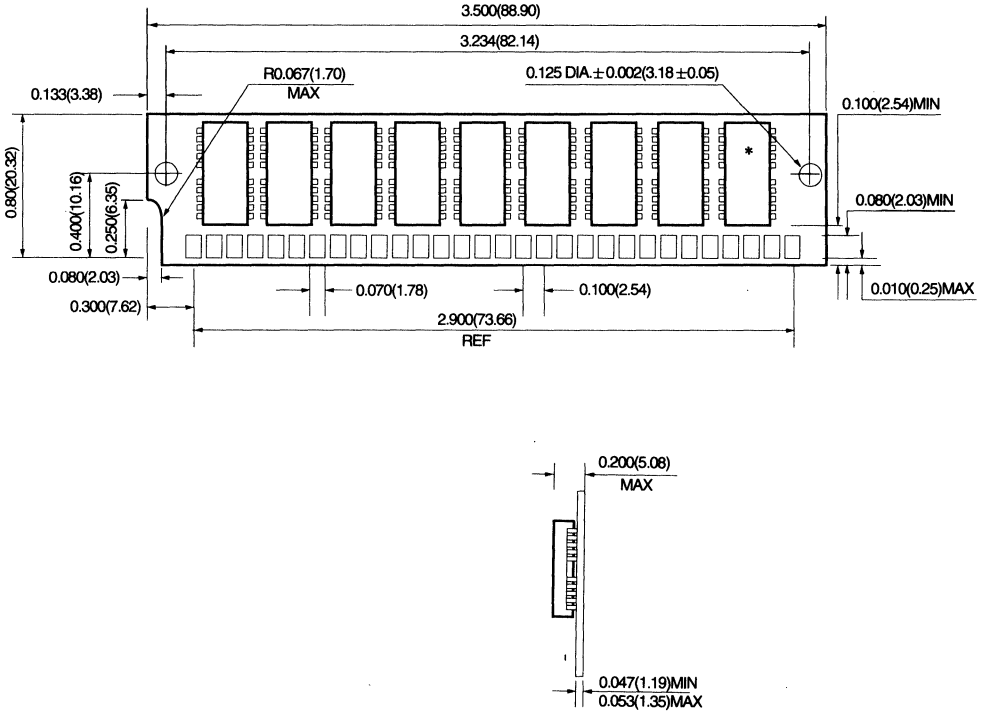
Symbol	Parameter	GMM78(9)4000S-60		GMM78(9)4000S-70		GMM78(9)4000S-80		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	50	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	100,000	—	100,000	—	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	—	45	ns	13
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	45	—	ns	

Notes :

1. AC measurements assume $t_T = 5ns$.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD}(max)$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RAD}(max)$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS} is not restrictive operating parameters. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

Package Dimensions

Unit: inches (mm)



Tolerance: ±0.005(0.13) unless otherwise specified.

*Note: There is no component in the GMM784000S.

GoldStar
GOLDSTAR ELECTRON CO., LTD.

GMM7321000SG-60/70/80
1,048,576 WORDS × 32 BIT
GMM7322000SG-60/70/80
2,097,152 WORDS × 32 BIT
CMOS DYNAMIC RAM MODULE

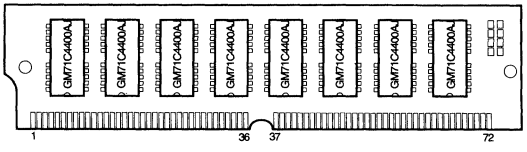
Description

The GMM7321000SG is a 1M×32 bits dynamic RAM MODULE which is assembled 8 pieces of 1M×4 bit DRAMs in 20/26 pin SOJ package on single side the printed circuit board with decoupling capacitors.

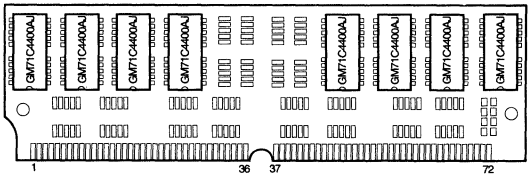
The GMM7322000SG is a 2M×32 bits dynamic RAM MODULE which is assembled 16 pieces of 1M×4 bit DRAMs in 20/26 pin SOJ package on both sides the printed circuit board with decoupling capacitors.

These are optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size. These provide common data inputs and outputs.

GMM7321000SG(Single Side)



GMM7322000SG(Both Side)



Features

- 72 pins Single In-Line Package (Gold plate)
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time

(Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
1M/2M×32-60	60	15	110	40
1M/2M×32-70	70	20	130	45
1M/2M×32-80	80	20	150	50

- Low Power
  Active
  — 1M×32: 4,840/4,400/3,960 mW(MAX)
  — 2M×32: 4,928/4,488/4,048 mW(MAX)
  Standby
  — 1M×32: 44 mW(CMOS level: MAX)
  — 2M×32: 88 mW(CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh Hidden Refresh
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16 ms

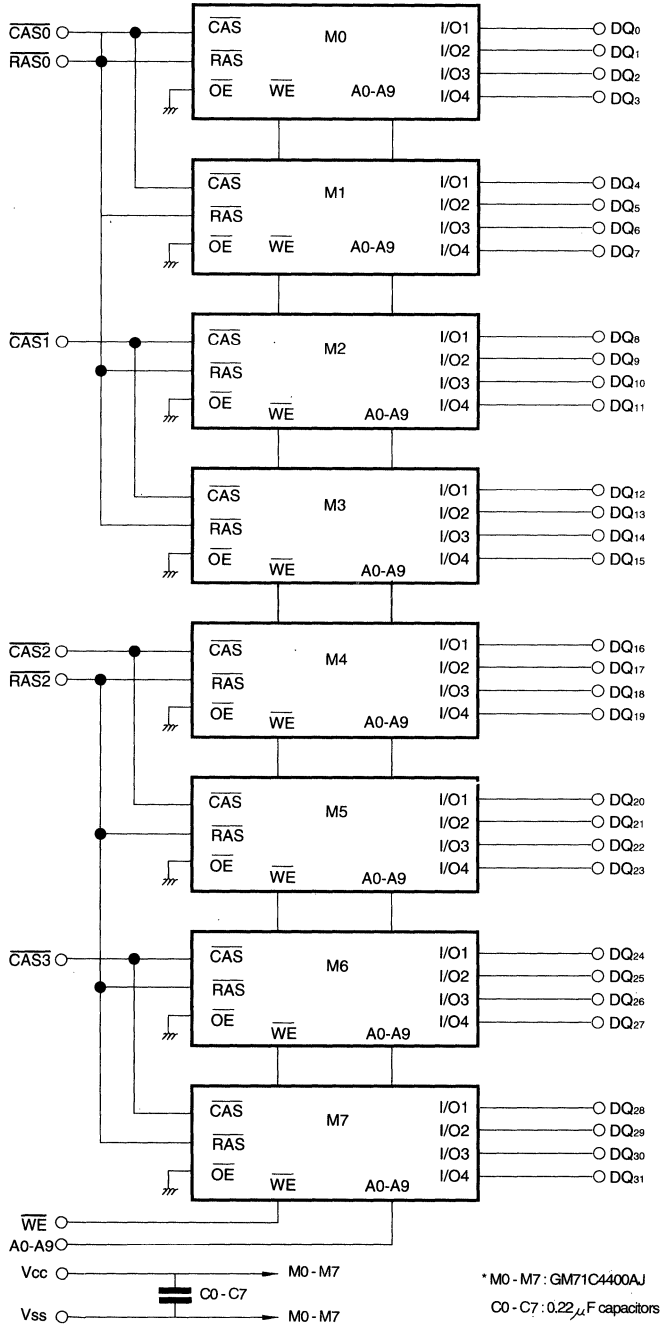
Pin Configuration (Top View)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	19	NC	37	NC	55	DQ_{11}
2	DQ_0	20	DQ_4	38	NC	56	DQ_{27}
3	DQ_{16}	21	DQ_{20}	39	V_{SS}	57	DQ_{12}
4	DQ_1	22	DQ_5	40	$\overline{CAS_0}$	58	DQ_{28}
5	DQ_{17}	23	DQ_{21}	41	$\overline{CAS_2}$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS_3}$	60	DQ_{29}
7	DQ_{18}	25	DQ_{22}	43	$\overline{CAS_1}$	61	DQ_{13}
8	DQ_3	26	DQ_7	44	$\overline{RAS_0}$	62	DQ_{30}
9	DQ_{19}	27	DQ_{23}	45	$\overline{RAS_1}$*1	63	DQ_{14}
10	V_{CC}	28	A_7	46	NC	64	DQ_{31}
11	NC	29	NC	47	WE	65	DQ_{15}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_8	67	PD_1
14	A_2	32	A_9	50	DQ_{24}	68	PD_2
15	A_3	33	$\overline{RAS_3}$*1	51	DQ_9	69	PD_3
16	A_4	34	$\overline{RAS_2}$	52	DQ_{25}	70	PD_4
17	A_5	35	NC	53	DQ_{10}	71	NC
18	A_6	36	NC	54	DQ_{26}	72	V_{SS}

*Note 1. In case of GMM7321000SG, Pin 33 and Pin 45 are no connection.

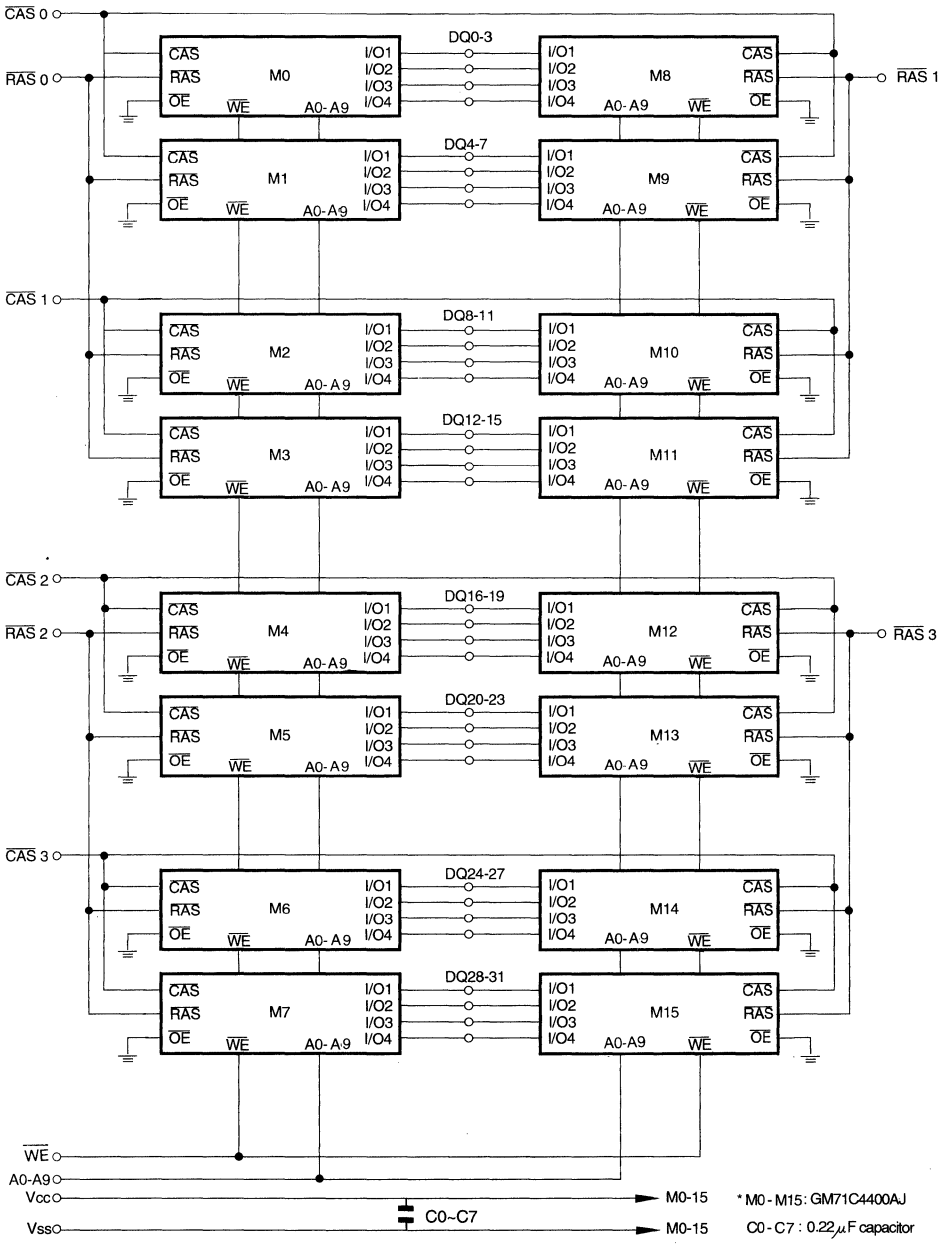
Block Diagram

- **GMM7321000SG**



Block Diagram

- **GMM7322000SG**



Pin Description

Pin	Function	Pin	Function
$A_0 \sim A_9$	Address Inputs	PD1 ~ PD4	Presence Detect
$DQ_0 \sim DQ_{31}$	Data Input/Output	V_{CC}	Power (+5V)
$\overline{RAS}0 \sim \overline{RAS}3$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}0 \sim \overline{CAS}3$	Column Address Strobe	NC	No Connection
$\overline{WE}$	Read/Write Enable		

Presence Detect Pins

• GMM7321000SG

Pin	60ns	70ns	80ns
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

• GM7322000SG

Pin	60ns	70ns	80ns
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

Absolute Maximum Ratings*[1]

Symbol	Parameter	Values	Unit
T_A	AmbientTemperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature	−55 ~ 125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−1.0 ~ 7.0	V
V_{CC}	Power Supply Voltage	−1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	8/16*[2]	W

*Note: 1. Stress greater than above under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. GMM732000SG

Recommended DC Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	MIN	TYP	MAX	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	6.5	V	1
V_{IL}	Input Low Voltage	−1.0	—	0.8	V	1

Note: 1 All voltages referenced to V_{SS}

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		GMM7321000SG		GMM7322000SG		Unit	Note
			Min	Max	Min	Max		
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	880	—	896	mA	1,2
		70ns	—	800	—	816		
		80ns	—	720	—	736		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	16	—	32	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	—	880	—	896	mA	2
		70ns	—	800	—	816		
		80ns	—	720	—	736		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	60ns	—	880	—	896	mA	1,3
		70ns	—	800	—	816		
		80ns	—	720	—	736		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V)		—	8	—	16	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	880	—	896	mA	
		70ns	—	800	—	816		
		80ns	—	720	—	736		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	40	—	80	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V) All Other Pins Not Under Test = 0V		−80	80	−160	160	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		−10	10	−20	20	μA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

Capacitance (V_{CC}=5V ± 10%, T_A=25°C, f=1MHz)

Symbol	Parameter	GMM7321000SG		GMM7322000SG		Unit	Notes
		Min	Max	Min	Max		
C_{I1}	Input Capacitance (A0~A9)	—	60	—	100	pF	1
C_{I2}	Input Capacitance ($\overline{WE}$)	—	75	—	132	pF	1,2
C_{I3}	Input Capacitance ($\overline{RAS}$0~$\overline{RAS}$3)	—	40	—	36	pF	1,2
C_{I4}	Input Capacitance ($\overline{CAS}$0~$\overline{CAS}$3)	—	30	—	36	pF	1,2
CDQ_1	Capacitance	—	17	—	30	pF	1,2

Note 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable D_{OUT}.

AC Electrical Characteristics (V_{CC}=5V±10%, T_A=0~70°C, Notes 1, 14)

Refer to the GM71C4400A/AL Data Sheet for Timing Waveforms.

Read, Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GMM732XXX-60		GMM732XXX-70		GMM732XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read/Write or Write Cycle Time	110	—	130	—	150	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	60	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	20	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	10	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	60	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	17	40	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	—	16	—	16	—	16	ms	

Read Cycle

Symbol	Parameter	GMM732XXX-60		GMM732XXX-70		GMM732XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	—	80	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	—	20	ns	3,4
t_{AA}	Access Time from Column Address	—	30	—	35	—	40	ns	3,5
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	0	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	ns	
t_{OFF}	Output Buffer Turn-off Time	—	15	—	20	—	20	ns	6

Write Cycle

Symbol	Parameter	GMM732XXX-60		GMM732XXX-70		GMM732XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	10	—	10	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	20	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	15	—	20	—	ns	11

Refresh Cycle

Symbol	Parameter	GMM732XXX-60		GMM732XXX-70		GMM732XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10		ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Symbol	Parameter	GMM732XXX-60		GMM732XXX-70		GMM732XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	50	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	100,000	—	100,000	—	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	—	45	13	
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	45	—	ns	

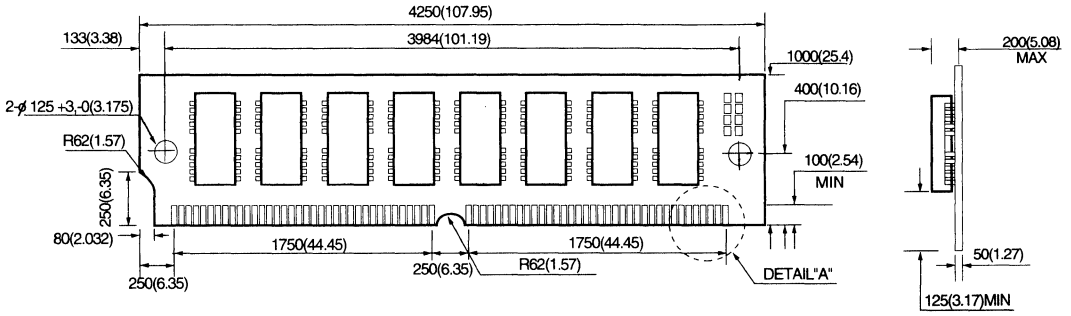
Notes :

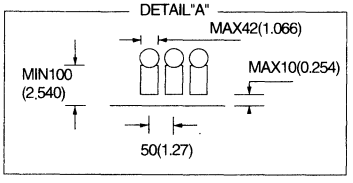
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD}(max)$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RAD}(max)$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, is not rrestrictive operating parameters. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in fast page mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimu of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

Package Dimensions

GMM7321000SG

Unit: mil (mm)





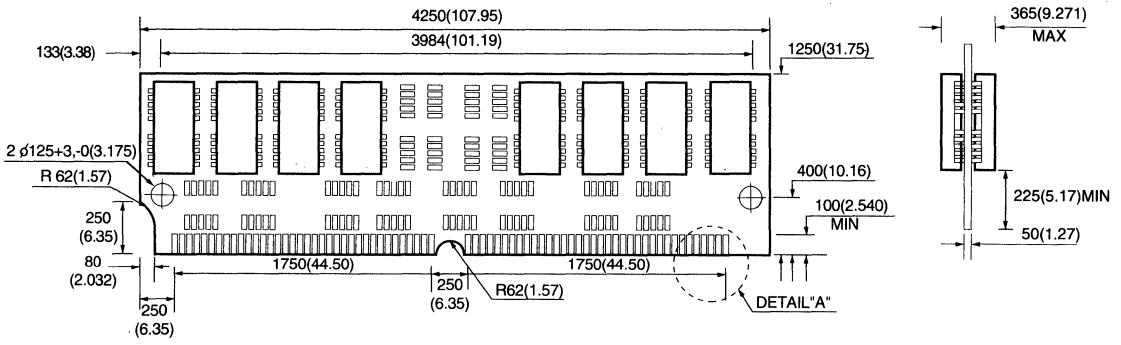
Tolerance : ±5(0.127) Unless otherwise Specified.

Package Dimensions

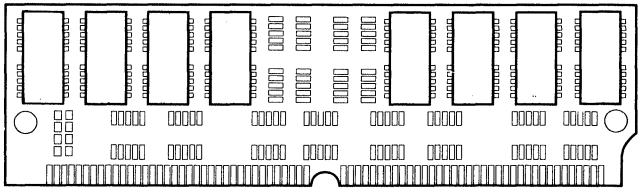
GMM7322000SG

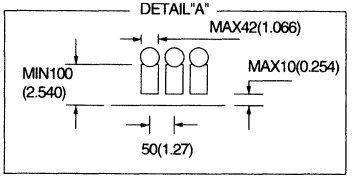
Unit: mil(mm)

(Front)



(Rear)





Tolerance : ±5(0.127) Unless otherwise Specified.

GMM7361000SG/SGS-60/70/80
1,048,576 WORDS×36 BIT
GMM7362000SG-60/70/80
2,097,152 WORDS×36 BIT
CMOS DYNAMIC RAM MODULE

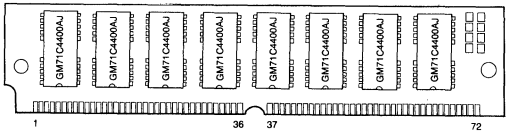
Description

The GMM7361000SG/SGS is a 1M×36 bits dynamic RAM MODULE which is assembled 8 pieces of 1M×4 bit DRAMs and 4 pieces of 1M×1 bit DRAMs in 20/26 pin SOJ package on both/single side the printed circuit board with decoupling capacitors.

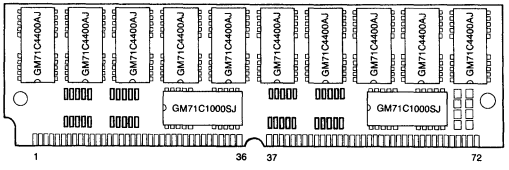
The GMM7362000SG is a 2M×36 bits dynamic RAM MODULE which is assembled 16 pieces of 1M×4 bit DRAMs and 8 pieces of 1M×1 bit DRAMs in 20/26 pin SOJ package on both sides the printed circuit board with decoupling capacitors.

These are optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size. These provide common data inputs and outputs.

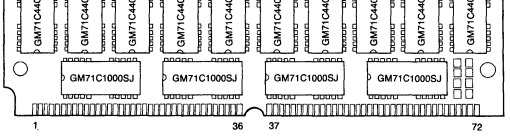
•GMM7361000SG (Both Side) *1



•GMM7361000SGS (Single Side)



•GMM7362000SG (Both Side) *2



Features

- 72 pins Single In-Line Package (Gold plate)
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
1M/2M×36-60	60	20	120	45
1M/2M×36-70	70	20	130	50
1M/2M×36-80	80	25	160	55

- Low Power
  Active
  — 1M×36: 6,820/6,160/5,500 mW(MAX)
  — 2M×36: 6,952/6,292/6,632 mW(MAX)
  Standby
  — 1M×36: 66 mW(CMOS level; MAX)
  — 2M×36: 138 mW(CMOS level; MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ Refresh Hidden Refresh
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16ms

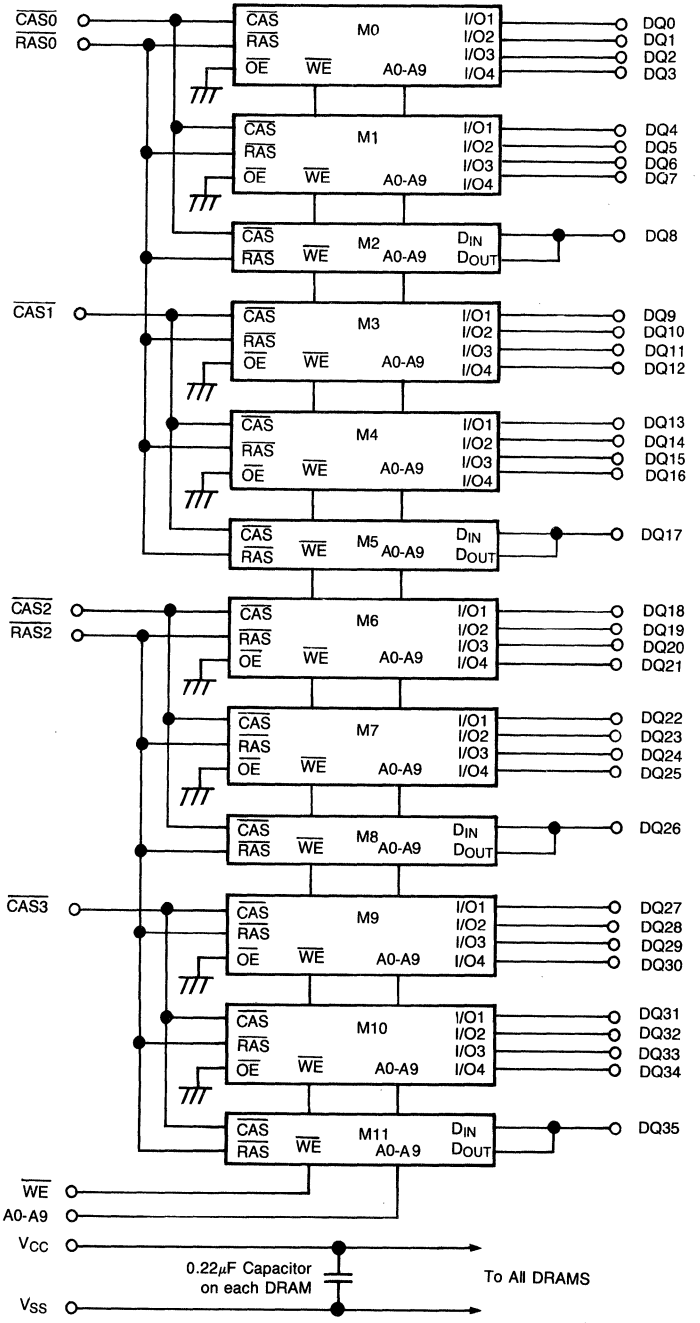
Pin Configuration (Top View)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	19	NC	37	DQ_{17}	55	DQ_{12}
2	DQ_0	20	DQ_4	38	DQ_{35}	56	DQ_{30}
3	DQ_{18}	21	DQ_{22}	39	V_{SS}	57	DQ_{13}
4	DQ_1	22	DQ_5	40	$\overline{CAS_0}$	58	DQ_{31}
5	DQ_{19}	23	DQ_{23}	41	$\overline{CAS_2}$	59	V_{CC}
6	DQ_2	24	DQ_6	42	$\overline{CAS_3}$	60	DQ_{32}
7	DQ_{20}	25	DQ_{24}	43	$\overline{CAS_1}$	61	DQ_{14}
8	DQ_3	26	DQ_7	44	$\overline{RAS_0}$	62	DQ_{33}
9	DQ_{21}	27	DQ_{25}	45	$\overline{RAS_1}$ *3	63	DQ_{15}
10	V_{CC}	28	A_7	46	NC	64	DQ_{34}
11	NC	29	NC	47	$\overline{WE}$	65	DQ_{16}
12	A_0	30	V_{CC}	48	NC	66	NC
13	A_1	31	A_8	49	DQ_9	67	PD_1
14	A_2	32	A_9	50	DQ_{27}	68	PD_2
15	A_3	33	$\overline{RAS_3}$ *3	51	DQ_{10}	69	PD_3
16	A_4	34	$\overline{RAS_2}$	52	DQ_{28}	70	PD_4
17	A_5	35	DQ_{26}	53	DQ_{11}	71	NC
18	A_6	36	DQ_8	54	DQ_{29}	72	V_{SS}

Note: 1. There are 4 pieces of 1M×1 bit DRAM on the rear side.
2. There are 8 pieces of 1M×4 bit DRAM and 2 pieces of 1M×1 bit DRAM on the rear side.
3. In case of GMM7361000SG/SGS, Pin 33 and Pin 45 are not connected.

Block Diagram

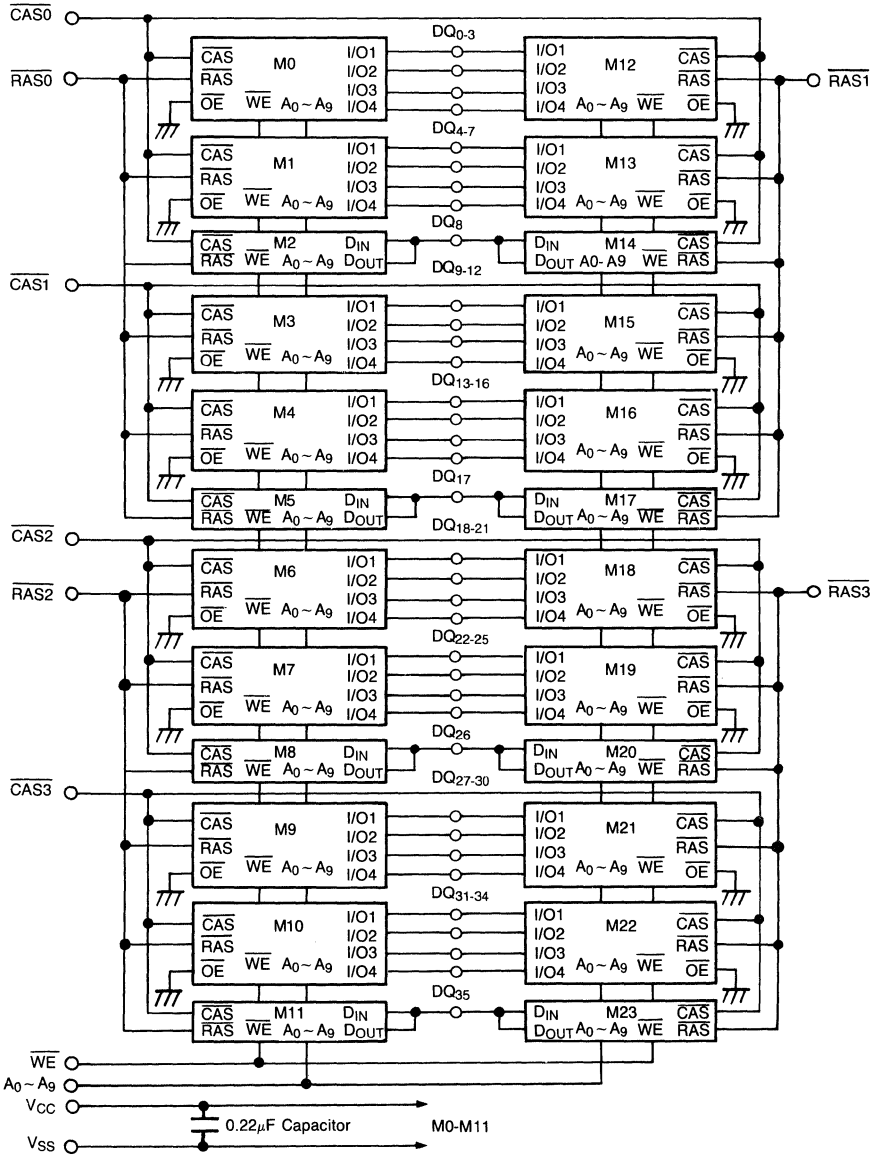
•GMM7361000SG/SGS



*Note: M2, M5, M8, M11 are GM71C1000SJ & others are GM71C4400AJ.

Block Diagram

•GMM7362000SG



*Note: M2, M5, M8, M11 M14, M17, M20, M23 are GM71C1000SJ & others are GM71C4400AJ.

Pin Description

Pin	Function	Pin	Function
$A_0 \sim A_9$	Address Inputs	PD1 ~ PD4	Presence Detect
$DQ_0 \sim DQ_{35}$	Data Input/Output	V_{CC}	Power (+5V)
$\overline{RAS0} \sim \overline{RAS3}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS0} \sim \overline{CAS3}$	Column Address Strobe	NC	No Connection
$\overline{WE}$	Read/Write Enable		

Presence Detect Pins

•GMM7361000SG/SGS

Pin	60ns	70ns	80ns
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

•GMM7362000SG

Pin	60ns	70ns	80ns
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

Absolute Maximum Ratings*1

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature	−55 ~ 125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−1.0 ~ 7.0	V
V_{CC}	Power Supply Voltage	−1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	12/24*2	W

*Note 1. Stress greater than above under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. GMM7362000SG

Recommended DC Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	6.5	V	1
V_{IL}	Input Low Voltage	−1.0	—	0.8	V	1

Note: 1. All Voltages referenced to V_{SS}

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		GMM7361000SG		GMM7362000SG		Unit	Notes
			Min	Max	Min	Max		
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	1240	—	1264	mA	1,2
		70ns	—	1120	—	1144		
		80ns	—	1000	—	1024		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	24	—	48	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min)	60ns	—	1240	—	1264	mA	2
		70ns	—	1120	—	1144		
		80ns	—	960	—	984		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	60ns	—	1200	—	1124	mA	1,3
		70ns	—	1080	—	1104		
		80ns	—	920	—	944		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V)		—	12	—	24	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	1200	—	1224	mA	
		70ns	—	1080	—	1104		
		80ns	—	960	—	984		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	60	—	120	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V) All Other Pins Not Under Test = 0V		−120	120	−240	240	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		−20	20	−20	20	μA	

Note) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

Capacitance (V_{CC}=5V ± 10%, T_A=25°C, f=1MHz)

Symbol	Parameter	GMM7361000SG		GMM7362000SG		Unit	Notes
		Min	Max	Min	Max		
C_{I1}	Input Capacitance (A0~A9)	—	88	—	140	pF	1
C_{I2}	Input Capacitance ($\overline{WE}$)	—	104	—	188	pF	1,2
C_{I3}	Input Capacitance ($\overline{RAS0}$~$\overline{RAS3}$)	—	42	—	42	pF	1,2
C_{I4}	Input Capacitance ($\overline{CAS0}$~$\overline{CAS3}$)	—	36	—	42	pF	1,2
CDQ_1	I/O Capacitance (DQ0~7, 9~16, 18~25, 27~34)	—	17	—	30	pF	1,2
CDQ_2	I/O Capacitance (DQ8, 17, 26, 35)	—	22	—	24	pF	1,2

Note 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$=V_{IH} to disable D_{OUT}.

AC Electrical Characteristics (V_{CC}=5V±10%, T_A=0 ~70°C, Notes 1,14)

The GMM736XXXX writes data only in early write cycle(t_{WCS} ≥ t_{WCS}(min)).
Delayed write cycle is not available because of I/O common.

Read, Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GMM736XXXX-60		GMM736XXXX-70		GMM736XXXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	120	—	130	—	160	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	50	—	50	—	70	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10,000	20	10,000	25	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	12	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	20	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	22	55	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	17	40	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	20	—	25	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	—	16	—	16	—	16	ms	

Read Cycle

Symbol	Parameter	GMM736XXXX-60		GMM736XXXX-70		GMM736XXXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	—	80	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	20	—	25	ns	3,4
t_{AA}	Access Time from Column Address	—	30	—	35	—	40	ns	3,5
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	10	—	10	—	10	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	ns	
t_{OFF}	Output Buffer Turn-off Time	—	20	—	20	—	20	ns	6

Write Cycle

Symbol	Parameter	GMM736XXXX-60		GMM736XXXX-70		GMM736XXXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	15	—	20	—	ns	
t_{WP}	Write Command Pulse Width	10	—	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	20	—	25	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	20	—	25	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	15	—	20	—	ns	11

Refresh Cycle

Symbol	Parameter	GMM736XXXX-60		GMM736XXXX-70		GMM736XXXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	15	—	15	—	20	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

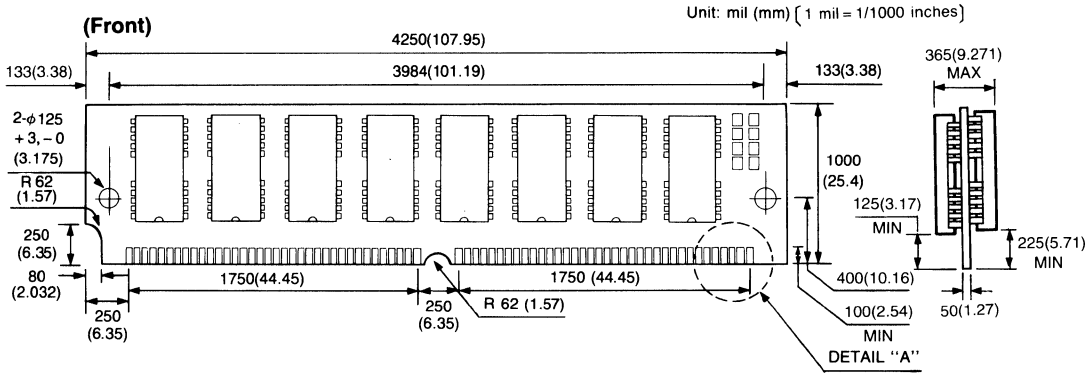
Symbol	Parameter	GMM736XXXX-60		GMM736XXXX-70		GMM736XXXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast-Page Mode Cycle Time	45	—	50	—	55	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	100,000	—	100,000	—	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	40	—	45	—	50	ns	13
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	—	45	—	50	—	ns	

Notes :

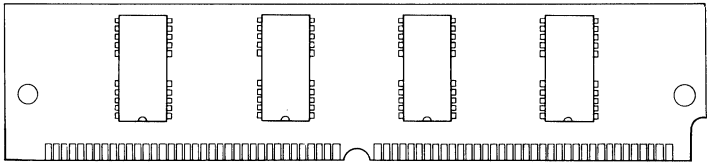
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the $t_{RCD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RCD}(max)$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the $t_{RAD}(max)$ limit insures that $t_{RAC}(max)$ can be met, $t_{RAD}(max)$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS} is not restrictive operating parameters. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
12. t_{RASC} is defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycels (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

Package Dimensions

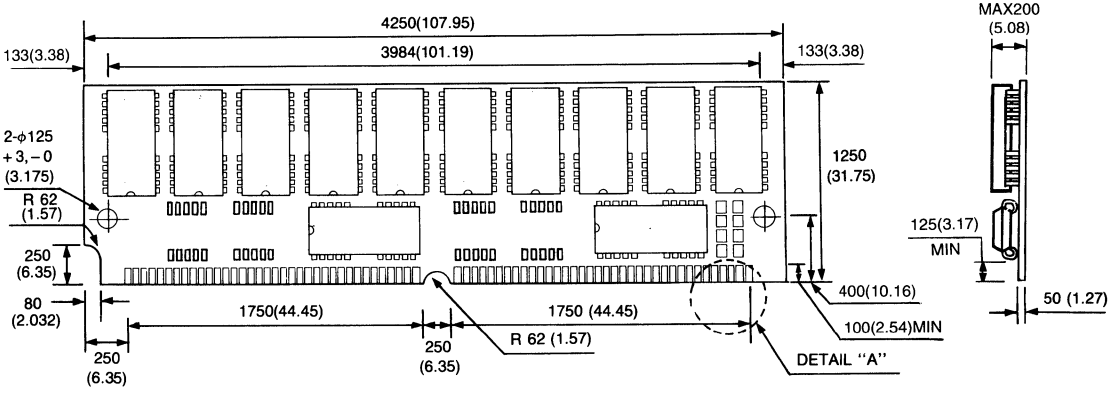
•GMM7361000SG



(Rear)

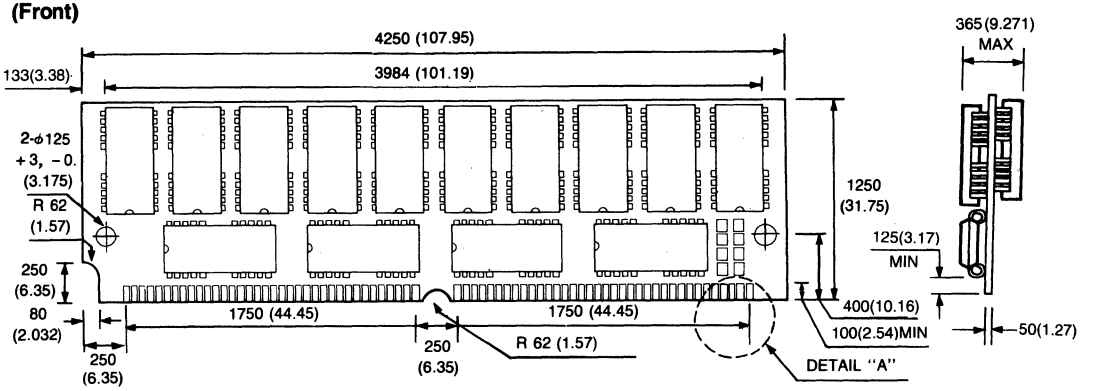


•GMM7361000SGS (There is no component on the rear side)

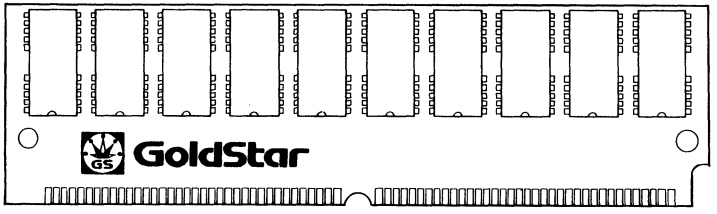


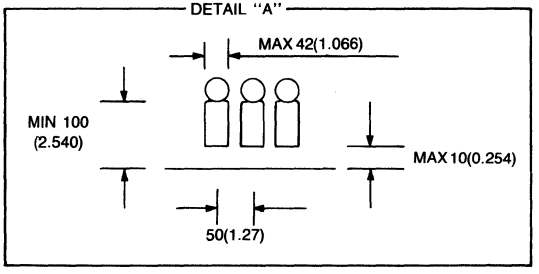
•GMM7362000SG

(Front)



(Rear)





Tolerance: ±5 (0.127) unless otherwise specified.

GMM7401000SG-60/70/80
1,048,576 WORDS × 40 BIT
GMM7402000SG-60/70/80
2,097,152 WORDS × 40 BIT
CMOS DYNAMIC RAM MODULE

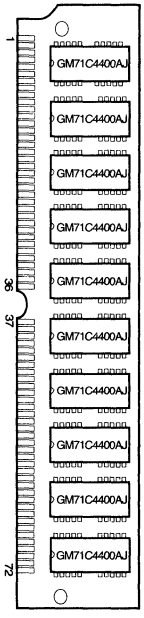
Description

The GMM7401000SG is a 1M×40 bits dynamic RAM MODULE which is assembled 10 pieces of 1M×4 bit DRAMs in 20/26 pin SOJ package on single side the printed circuit board with decoupling capacitors.

The GMM7402000SG is a 2M×40 bits dynamic RAM MODULE which is assembled 20 pieces of 1M×4 bit DRAMs in 20/26 pin SOJ package on both sides the printed circuit board with decoupling capacitors.

These are optimized for application to the systems which are required high density and large capacity such as main memory of the computers and an image memory systems, and to the others which are requested compact size. These provide common data inputs and outputs.

GMM7401000SG (Single side)
GMM7402000SG (Both side)



Features

- 72 pins Single In-Line Package (Gold plate)
- Fast Page Mode Capability
- Single Power Supply
- Fast Access Time & Cycle Time (Unit: ns)

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
1M/2M×40-60	60	15	110	40
1M/2M×40-70	70	20	130	45
1M/2M×40-80	80	20	150	50

- Low Power
  Active
  — 1M×40: 6,050/5,500/4,950 mW(MAX)
  — 2M×40: 6,160/5,610/5,060 mW(MAX)
  Standby
  — 1M×40: 55 mW(CMOS level: MAX)
  — 2M×40: 110 mW(CMOS level: MAX)
- $\overline{RAS}$ Only Refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden Refresh
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16 ms

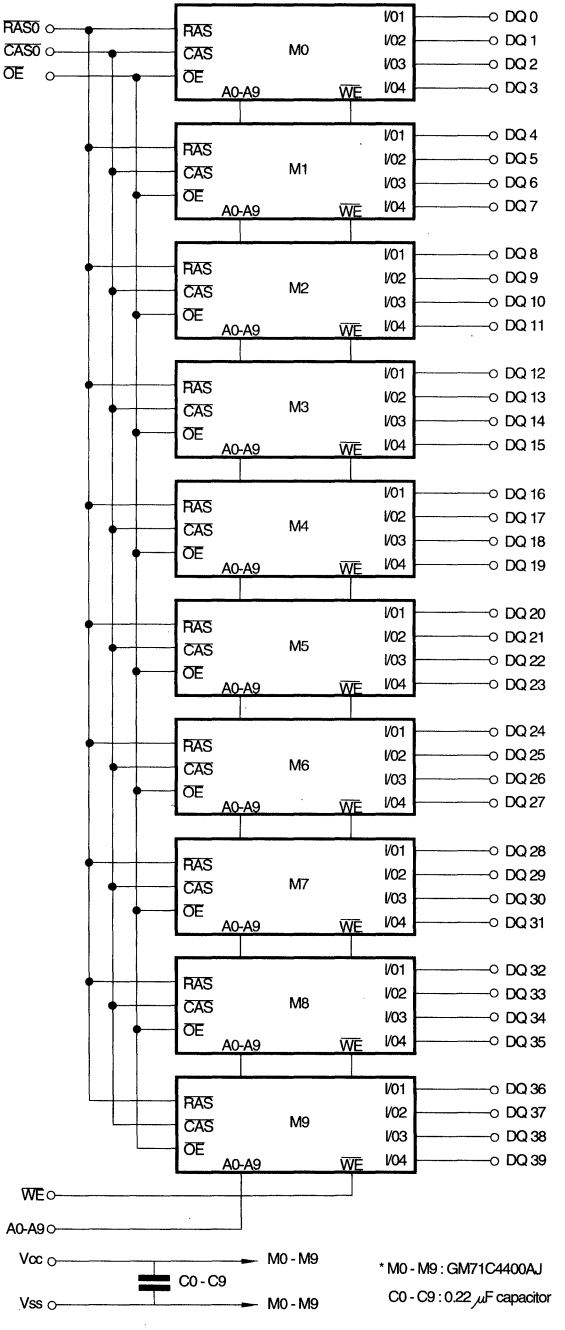
Pin Configuration (Top View)

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	19	$\overline{OE}$	37	DQ_{33}	55	DQ_{11}
2	DQ_0	20	DQ_4	38	DQ_{35}	56	DQ_{27}
3	DQ_{16}	21	DQ_{20}	39	V_{SS}	57	DQ_{12}
4	DQ_1	22	DQ_5	40	$\overline{CAS_0}$	58	DQ_{28}
5	DQ_{17}	23	DQ_{21}	41	NC	59	V_{CC}
6	DQ_2	24	DQ_6	42	NC	60	DQ_{29}
7	DQ_{18}	25	DQ_{22}	43	$\overline{CAS_1}$*1	61	DQ_{13}
8	DQ_3	26	DQ_7	44	$\overline{RAS_0}$	62	DQ_{30}
9	DQ_{19}	27	DQ_{23}	45	$\overline{RAS_1}$*1	63	DQ_{14}
10	V_{CC}	28	A_7	46	DQ_{37}	64	DQ_{31}
11	NC	92	DQ_{36}	47	$\overline{WE}$	65	DQ_{15}
12	A_0	30	V_{CC}	48	V_{SS}	66	DQ_{38}
13	A_1	31	A_8	49	DQ_8	67	PD_1
14	A_2	32	A_9	50	DQ_{24}	68	PD_2
15	A_3	33	NC	51	DQ_9	69	PD_3
16	A_4	34	NC	52	DQ_{25}	70	PD_4
17	A_5	35	DQ_{34}	53	DQ_{10}	71	DQ_{39}
18	A_6	36	DQ_{32}	54	DQ_{26}	72	V_{SS}

Note 1. In case of GMM7401000S, these are not connected.

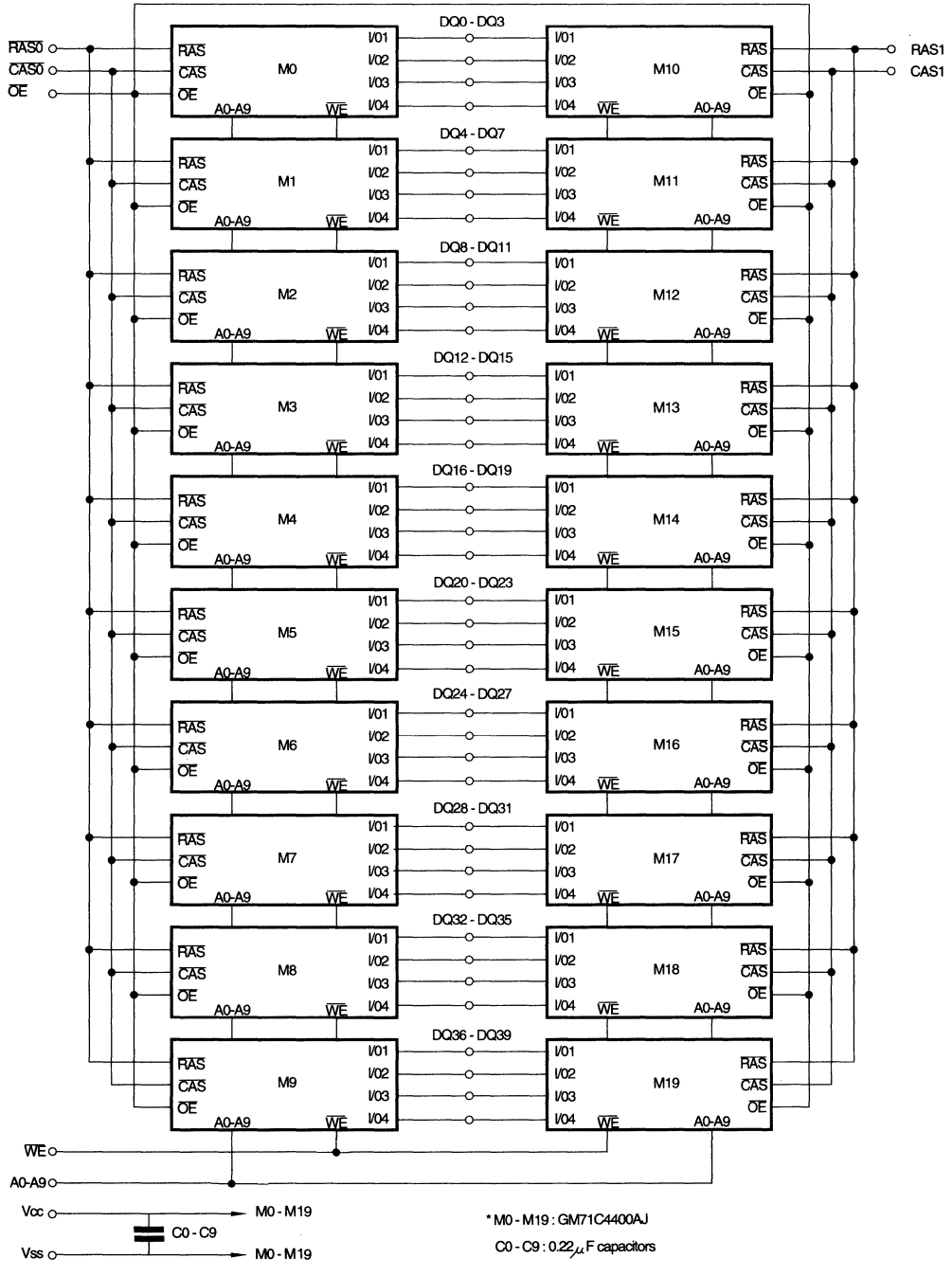
Block Diagram

•GMM7401000SG



Block Diagram

- **GMM7402000SG**



Pin Description

Pin	Function	Pin	Function
$A_0 \sim A_9$	Address Inputs	PD1 ~ PD4	Presence Detect
$DQ_0 \sim DQ_{39}$	Data Input/Output	V_{CC}	Power (+5V)
$\overline{RAS0}$, $\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS0}$, $\overline{CAS}$	Column Address Strobe	NC	No Connection
$\overline{WE}$	Read/Write Enable	$\overline{OE}$	Output Enable

Presence Detect Pins

• GMM7401000SG

Pin	60ns	70ns	80ns
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}	V_{SS}
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

• GM7402000SG

Pin	60ns	70ns	80ns
PD1	NC	NC	NC
PD2	NC	NC	NC
PD3	NC	V_{SS}	NC
PD4	NC	NC	V_{SS}

Absolute Maximum Ratings*[1]

Symbol	Parameter	Values	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature	−55 ~ 125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	−1.0 ~ 7.0	V
V_{CC}	Power Supply Voltage	−1.0 ~ 7.0	V
I_{OUT}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	10/20*[2]	W

*Note: 1. Stress greater than above under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. GMM7402000SG

Recommended DC Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	MIN	TYP	MAX	Unit	Note
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	6.5	V	1
V_{IL}	Input Low Voltage	−1.0	—	0.8	V	1

Note: 1. All voltages referenced to V_{SS}

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter		GMM7401000SG		GMM7402000SG		Unit	Note
			Min	Max	Min	Max		
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = −5mA)		2.4	V_{CC}	2.4	V_{CC}	V	
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = 4.2mA)		0	0.4	0	0.4	V	
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	60ns	—	1100	—	1120	mA	1,2
		70ns	—	1000	—	1020		
		80ns	—	900	—	920		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{IH})		—	20	—	40	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} min)	60ns	—	1100	—	1120	mA	2
		70ns	—	1000	—	1020		
		80ns	—	900	—	920		
I_{CC4}	Fast Page Mode Current Average Power Supply Current Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Address Cycling: t_{PC} = t_{PC} min)	60ns	—	1100	—	1120	mA	1,3
		70ns	—	1000	—	1020		
		80ns	—	900	—	920		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$, $\overline{CAS}$ = V_{CC} − 0.2V)		—	10	—	20	mA	
I_{CC6}	$\overline{CAS}$ before $\overline{RAS}$ Refresh Current (t_{RC} = t_{RC} min)	60ns	—	1100	—	1120	mA	
		70ns	—	1000	—	1020		
		80ns	—	900	—	920		
I_{CC7}	Standby Current $\overline{RAS}$ = V_{IH} $\overline{CAS}$ = V_{IL} D_{OUT} = Enable		—	50	—	100	mA	1
$I_{I(L)}$	Input Leakage Current Any Input (0V ≤ V_{IN} ≤ 7V) All Other Pins Not Under Test = 0V		−100	100	−200	200	μA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is Disabled, 0V ≤ V_{OUT} ≤ 7V)		−10	10	−20	20	μA	

Note: 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. Address can be changed less than three times while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

Capacitance (V_{CC} = 5V ± 10%, T_A = 25°C, f = 1MHz)

Symbol	Parameter	GMM7401000SG		GMM7402000SG		Unit	Notes
		Min	Max	Min	Max		
C_{I1}	Input Capacitance (A0 ~ A9)	—	85	—	130	pF	1
C_{I2}	Input Capacitance ($\overline{WE}$, $\overline{OE}$)	—	85	—	160	pF	1,2
C_{I3}	Input Capacitance ($\overline{RAS0}$, $\overline{RAS1}$)	—	85	—	90	pF	1,2
C_{I4}	Input Capacitance ($\overline{CAS0}$, $\overline{CAS1}$)	—	85	—	90	pF	1,2
CDQ_1	I/O Capacitance	—	20	—	25	pF	1,2

Note 1. Capacitance shall be measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable D_{OUT}.

AC Electrical Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C, Notes 1, 14)

Refer to the GM71C4400A/AL Data Sheet for Timing Waveforms.

Read, Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	GMM740XXX-60		GMM740XXX-70		GMM740XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RC}	Random Read/Write or Write Cycle Time	110	—	130	—	150	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	60	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10,000	70	10,000	80	10,000	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10,000	20	10,000	20	10,000	ns	
t_{ASR}	Row Address Set-up Time	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	10	—	ns	
t_{ASC}	Column Address Set-up Time	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	60	ns	8
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	17	40	ns	9
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	80	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	7
t_{REF}	Refresh Period	—	16	—	16	—	16	ms	

Read Cycle

Symbol	Parameter	GMM740XXX-60		GMM740XXX-70		GMM740XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	—	80	ns	2,3
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	—	20	ns	3,4
t_{AA}	Access Time from Column Address	—	30	—	35	—	40	ns	3,5
t_{RCS}	Read Command Set-up Time	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	ns	
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	0	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	40	—	ns	
t_{OFF}	Output Buffer Turn-off Time	—	15	—	20	—	20	ns	6

Write Cycle

Symbol	Parameter	GMM740XXX-60		GMM740XXX-70		GMM740XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{WCS}	Write Command Set-up Time	0	—	0	—	0	—	ns	10
t_{WCH}	Write Command Hold Time	15	—	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	10	—	10	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	20	—	ns	
t_{DS}	Data-in Set-up Time	0	—	0	—	0	—	ns	11
t_{DH}	Data-in Hold Time	15	—	15	—	20	—	ns	11

Refresh Cycle

Symbol	Parameter	GMM740XXX-60		GMM740XXX-70		GMM740XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$ Set-up Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)	10	—	10	—	10		ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	10	—	ns	

Fast Page Mode Cycle

Symbol	Parameter	GMM740XXX-60		GMM740XXX-70		GMM740XXX-80		Unit	Notes
		Min	Max	Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	50	—	ns	
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10	—	10	—	10	—	ns	
t_{RASC}	Fast Page Mode $\overline{RAS}$ Pulse Width	—	100,000	—	100,000	—	100,000	ns	12
t_{ACP}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	—	45	ns	13
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	45	—	ns	

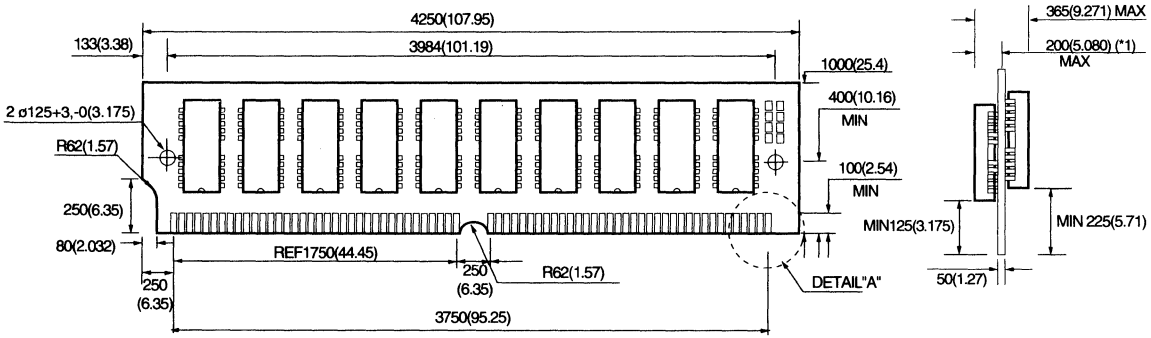
Notes :

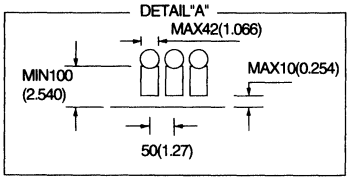
1. AC measurements assume t_T = 5ns.
2. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
5. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
6. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
8. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met, t_{RCD}(max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
9. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met, t_{RAD}(max) is specified as a reference point only, if t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
10. t_{WCS}, is not rrestrictive operating parameters. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles.
12. t_{RASC} defines $\overline{RAS}$ pulse width in Fast Page Mode cycles.
13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP}.
14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$ clock such as $\overline{RAS}$ only refresh). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.

Package Dimensions

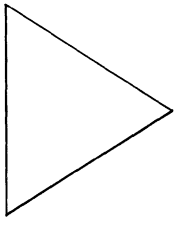
GMM7401000SG (*1)
GMM7402000SG

Unit: mil (mm)





Tolerance : ±5(0.127) Unless otherwise Specified.



GM53C261

65,536 WORDS × 4 BIT
CMOS MULTIPORT VIDEO RAM

Description

The GM53C261 is a high speed 65,536×4 bit multiport CMOS dynamic memory. The two ports, random access and serial access, are configured to offer optimum flexibility in graphics and other systems that require an interface between a processor and a high speed serial data channel such as a CRT or graphics display device.

The organization of the random access port of the GM53C261 is exactly like the GM71C464A, a 64K×4 CMOS DRAM. Additional functions such as transfer between RAM and SAM utilize otherwise unused states of the $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$ and $\overline{SE}$ signals sampled at the falling edge of $\overline{RAS}$ at the beginning of a cycle.

The Serial Access Memory (SAM) is organized as 256×4 bits that can be read or written at high speed. The contents of the SAM can be loaded into RAM, and the contents of a selected RAM row (256×4) can be loaded into SAM. Except when transferring data between one another, the SAM and RAM operate in an asynchronous manner. The transfer from RAM to SAM or SAM to RAM also refreshes the transferred row in the RAM.

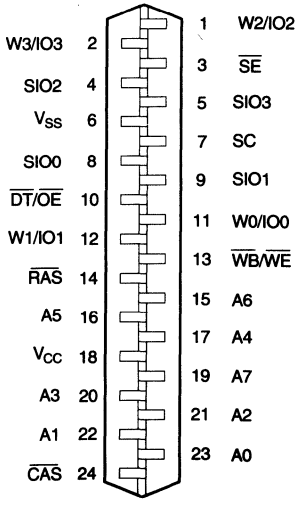
In a RAM to SAM load cycle, 8 bits are needed to specify which of the 256 rows is to be transferred. The state of the address lines at the falling edge of $\overline{CAS}$ is used to specify the starting point in the SAM where data is to be written or read. The static mechanization of the SAM (allowed by CMOS) does not require refreshing. The first access to SAM, either read or write, will be to the location specified at $\overline{CAS}$ time in the previous cycle, and subsequent accesses will continue in an increasing address direction.

Features

- Dual Port Accessibility
  RAM: 64K×4 Bit
  SAM : 256×4 Bit
- High Speed Access Time
  RAM: 80/100/120 ns
  SAM: 25/30/35 ns
- Min. Read/Write cycle time: 145/175/205 ns
  Min. Serial port cycle time: 30/35/40 ns
- Low power dissipation for GM53C261-12
  RAM port operating alone-50 mA
  SAM Port operating alone-35 mA
  RAM/SAM operating together-85 mA
- Low CMOS standby current-6 mA
- Fast page mode access, $\overline{RAS}$-only refresh, Hidden refresh and $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Bi-directional data transfer between RAM and SAM with real-time operation.
- Bit-masked Write function on RAM port for additional flexibility.
- 256 Refresh cycles/4 ms
- Standard package is 24 pin ZIP.

Pin Configuration

24 ZIP



(Bottom View)

Pin Description

Pin	Function	Pin	Function
A0 ~ A7	Address Inputs	SC	Serial Clock
W/IO0 ~ W/IO3	Write-Per-Bit Selection Input/ RAM Port Data Input/Output	$\overline{WB}/\overline{WE}$	Write-Per-Bit/Write Enable
		$\overline{DT}/\overline{OE}$	Data Transfer/Output Enable
SIO0 ~ SIO3	SAM Port Data Input/Output	$\overline{SE}$	SAM Port Enable
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power Supply
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground

Absolute Maximum Ratings*

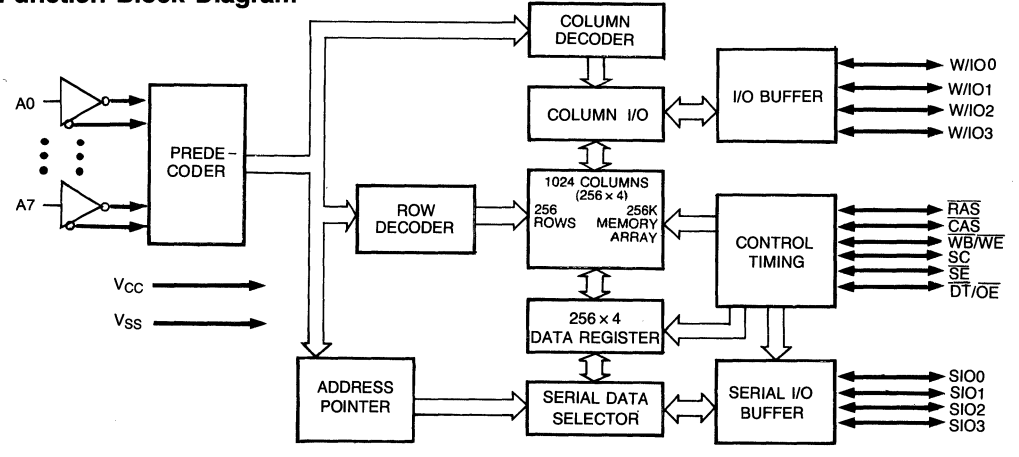
Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	−10 ~ 80	°C
T_{STG}	Storage Temperature	−55 ~ 125	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	1.0 ~ 7.0	V
V_{CC}	Voltage on V_{CC} relative to V_{SS}	1.0 ~ 7.0	V
I_{OUT}	Data Output Current	50	mA
P_D	Power Dissipation	1.0	W

*Note: Operation at or above "Absolute Maximum Ratings" can adversely affect device reliability.

Recommended Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	V_{CC}+1	V
V_{IL}	Input Low Voltage	−1	—	0.8	V

Function Block Diagram



Mode Selection

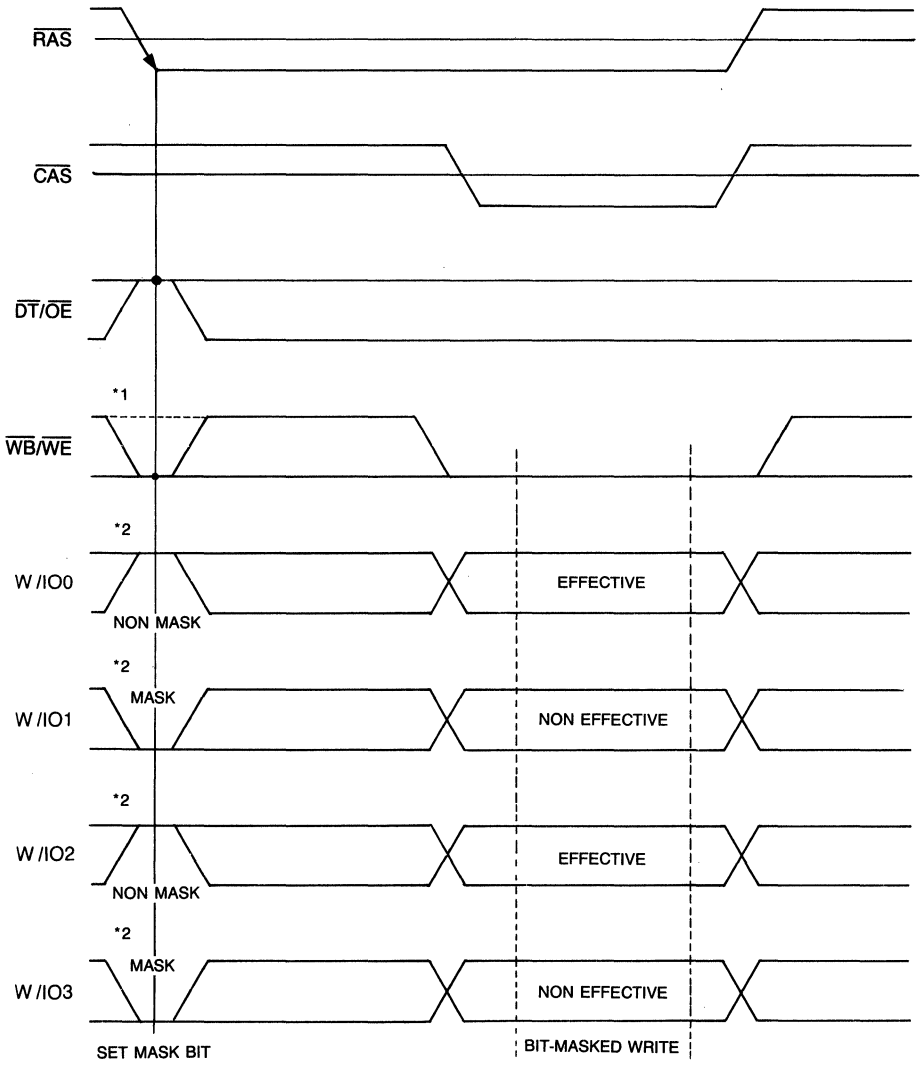
RAM Operation to be Performed	SAM Mode to be Entered	Control Signals (Sampled at the falling edge of $\overline{RAS}$					A0-A7 Sample Time	
		$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	W/IO 0-3	$\overline{RAS}$	$\overline{CAS}$
Read	Mode not affected	H	H	X	X	X	Row	Column Add.
Write	Mode not affected			H	X	X	Row	Column Add.
Bit Masked Write	Mode not affected			L	X	H*	Row	Column Add.
	Mode not affected			L	X	L*	Row	Column Add.
RAM→SAM Transfer	Output Mode		L	H	X	X	Row	SAM Start**
SAM→RAM Transfer	Input Mode			L	L	X	Row	SAM Start**
Pseudo Transfer	Input Mode			L	H	X	X	SAM Start**
$\overline{CAS}$-before-$\overline{RAS}$ or Hidden Refresh	Mode not affected	L	X	X	X	X	X	X

X = Don't care

* The state of the W/IO line is sampled at the falling edge of $\overline{RAS}$ to set the Write Bit Mask Resgister. If W/IO is high at the falling edge of $\overline{RAS}$, no masking action is taken and the corresponding data bit will be subject to change by a write operation. If W/IO is low at the falling edge of $\overline{RAS}$, the corresponding bit is masked and will not be altered by a write operation.

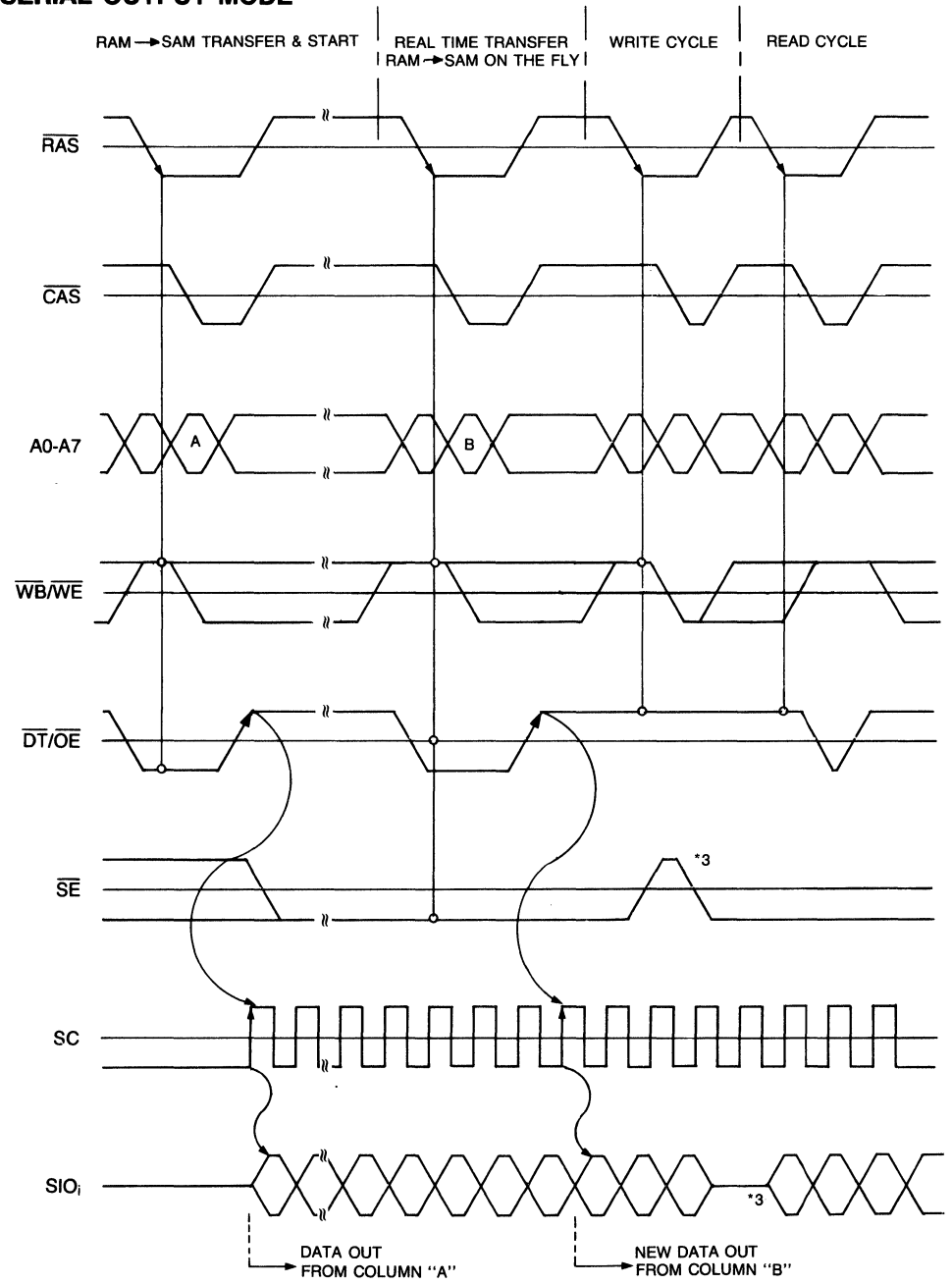
** The 8 address signals, A0-A7, are used to select the RAM row address that will be affected by a transfer to or from the SAM and the starting address for a SAM read or write operation. The falling edge of $\overline{RAS}$ strobes the row address, and the falling edge of $\overline{CAS}$ strobes the SAM starting address.

BIT MASKED WRITE



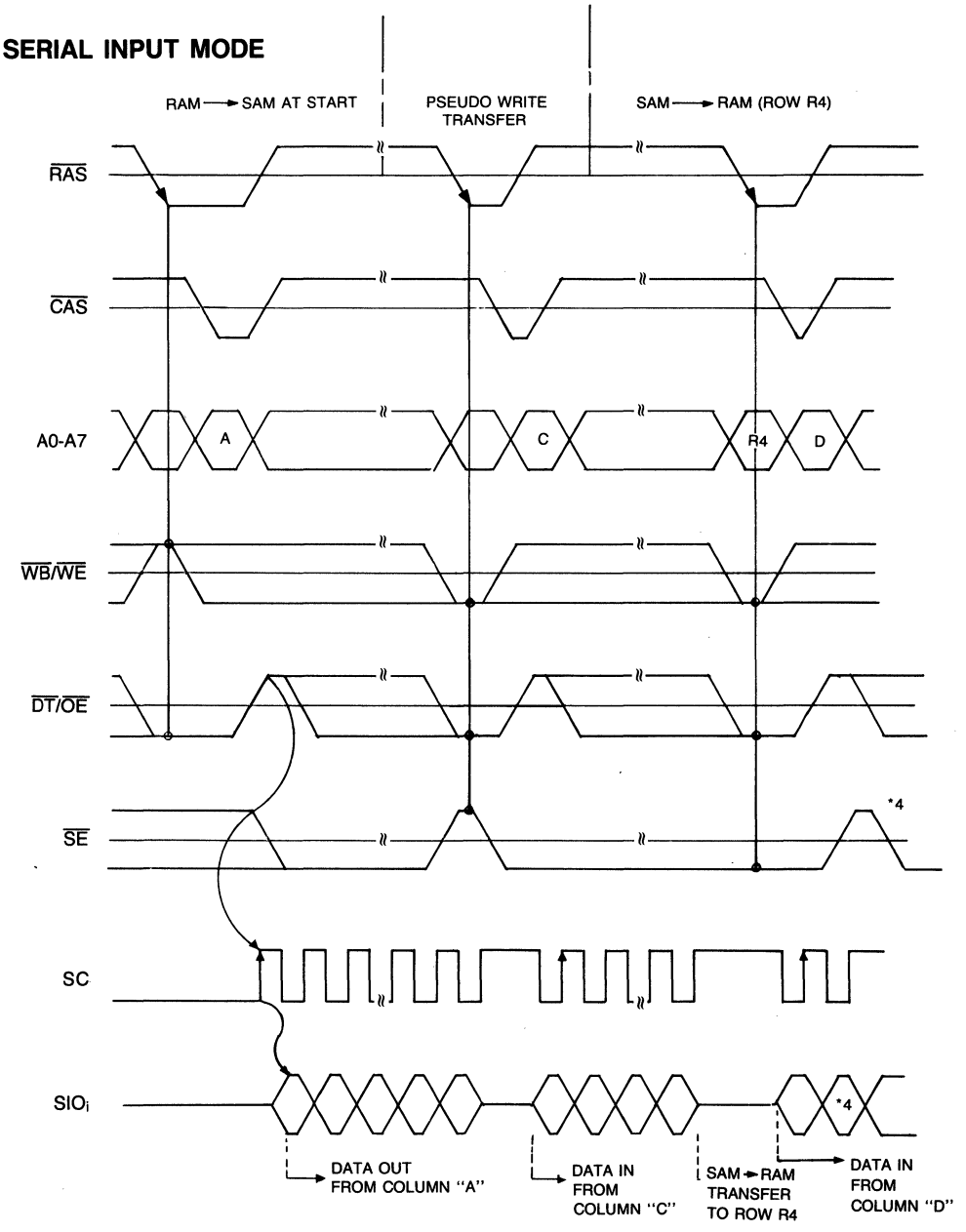
*1 If $\overline{WB}/\overline{WE}$ = "H" all 4 bits of data are written into RAM
*2 W/IO0-3 = "H" Non masked
W/IO0-3 = "L" Masked

SERIAL OUTPUT MODE



*3 If $\overline{SE}$ goes to "H" level, SIO_i enters the high impedance state, but the serial data selector continues to function.

SERIAL INPUT MODE



*4 If $\overline{SE}$ goes to "H" level, SIO_i input data is ignored, but the serial data selector continues to function

DC Characteristics (Note 1, 5)

$T_A = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter		Min	Max	Unit	Test Conditions	Notes
V_{LI}	Input Leakage Current (any input pin)		-10	10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$	
I_{LO}	Output Leakage Current (for High-Z State)		-10	10	μA	$V_{SS} \leq V_{OUT} \leq V_{CC}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{SE}$ at V_{IH}	
I_{CC1}	V_{CC} Supply Current	80ns	—	70	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port TTL Standby t_{RC}(min), SC = V_{IL}	2,3
		100ns	—	60			
		120ns	—	50			
I_{CC2}	V_{CC} Supply Current, TTL Standby			8	mA	RAM/SAM ports TTL Standby, $\overline{RAS}$, $\overline{CAS}$ at V_{IH}, I/O ≥ V_{SS}, SC = V_{IL}	
I_{CC3}	V_{CC} Supply Current $\overline{RAS}$-Only Refresh	80ns	—	70	mA	$\overline{RAS}$ Cycling, $\overline{CAS}$ at V_{IH} SAM port TTL Standby t_{RC}(min), SC = V_{IL}	2,3
		100ns	—	60			
		120ns	—	50			
I_{CC4}	V_{CC} Supply Current Page Mode Operation	80ns	—	60	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling SAM port TTL Standby t_{PC}(min), SC = V_{IL}	2,3
		100ns	—	50			
		120ns	—	40			
I_{CC5}	V_{CC} Supply Current $\overline{CAS}$-before-$\overline{RAS}$ Refresh	80ns	—	70	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling SAM port TTL Standby t_{PC}(min), SC = V_{IL}	2,3
		100ns	—	60			
		120ns	—	50			
I_{CC6}	V_{CC} Supply Current RAM/SAM Transfer Mode	80ns	—	75	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port TTL Standby t_{RC}(min), SC = V_{IL}	2,3
		100ns	—	65			
		120ns	—	55			
I_{CC7}	V_{CC} Supply Current Both Ports Active	80ns	—	120	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port Active. t_{RC}(min), t_{SCC}(min)	2,3
		100ns	—	100			
		120ns	—	85			
I_{CC8}	V_{CC} Supply Current SAM Only Operation	80ns	—	50	mA	$\overline{RAS}/\overline{CAS}$ at V_{IH}, I/O ≥ V_{SS}, SAM port Active. t_{SCC}(min)	2
		100ns	—	40			
		120ns	—	35			
I_{CC9}	V_{CC} Supply Current $\overline{RAS}$-Only Refresh and SAM Active	80ns	—	120	mA	$\overline{RAS}$ Cycling, $\overline{CAS}$ at V_{IH}, SAM port Active. t_{RC}(min), t_{SCC}(min)	2,3
		100ns	—	100			
		120ns	—	85			
I_{CC10}	V_{CC} Supply Current Page Mode Operation and SAM Active	80ns	—	110	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling SAM port Active. t_{PC}(min), t_{SCC}(min)	2,3
		100ns	—	90			
		120ns	—	75			
I_{CC11}	V_{CC} Supply Current $\overline{CAS}$-before-$\overline{RAS}$ Refresh and SAM Active	80ns	—	120	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port Active. t_{RC}(min), t_{SCC}(min)	2,3
		100ns	—	100			
		120ns	—	85			

DC Characteristics (Continued)

Symbol	Parameter		Min	Max	Unit	Test Conditions	Note
I_{CC12}	V_{CC} Supply Current RAM/SAM Transfer Mode and SAM Active	80ns	—	125	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port Active. t_{RC}(min), t_{SCC}(min)	2,3
		100ns	—	105			
		120ns	—	90			
I_{CC13}	V_{CC} Supply Current Both ports CMOS Standby	80ns	—	6	ma	$\overline{RAS}$, $\overline{CAS}$, $\overline{SE}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE} \geq V_{CC} - 0.5V$ $SC \leq 0.6V$	
		100ns	—	6			
		120ns	—	6			
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 4.2mA$	
V_{OH}	Output High Voltage		2.4		V	$I_{OH} = -5mA$	

Capacitance*

Symbol	Parameter	Typ	Max	Unit
C_{IN1}	Address Input Capacitance		5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$, SC, $\overline{DT}/\overline{OE}$ Capacitance		8	pF
C_{OUT}	I/O Capacitance		7	pF

*Note: Capacitance is sampled and not 100% tested.

AC Test Conditions

Input Rise Levels	0 to3.0V
Input Rise and Fall Times	5 ns between 0.8 and 2.4V
Input Timing Reference Levels	0.8 and 2.4V
Output Timing Reference Levels	0.8 and 2.4V
Output Load (RAM Port)	2 TTL and 100pF
Output Load (SAM Port)	2 TTL and 50pF

AC Characteristics (Note 1, 4, 5, 6)

$T_A = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$ unless otherwise specified.

Read, Write, Read-Modify-Write and Refresh Cycles

Symbol	Parameter	GM53C261-80		GM53C261-10		GM53C261-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	
t_{REF}	Refresh Interval (256 Cycles)		4		4		4	ms	
t_{RC}	Read or Write Cycle Time	145		175		205		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	80	37K	100	37K	120	37K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	55		65		75		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	80		100		120		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	25		30		35		ns	
t_{ASR}	Row Address Setup Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	15		15		15		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		10		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	55	25	70	25	85	ns	7
t_{ASC}	Column Address Setup Time	0		0		0		ns	
t_{CAH}	Column Address Hold Time	15		20		20		ns	
t_{RSH}	$\overline{RAS}$ Hold Time	25		30		35		ns	
t_{DHS}	$\overline{DT}$ High Setup Time	0		0		0		ns	
t_{DHH}	$\overline{DT}$ High Hold Time	20		20		20		ns	
t_{AR}	Column Address Hold Time from $\overline{RAS}$	60		70		80		ns	
t_{RAC}	$\overline{RAS}$ Access Time		80		100		120	ns	8,9
t_{CAC}	$\overline{CAS}$ Access Time		25		30		35	ns	9,10,11
t_{CAA}	Column Address Access Time		40		45		55	ns	9
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RRH}	Read Command Hold Time $\overline{RAS}$-Referenced	5		5		10		ns	12
t_{RCH}	Read Command Hold Time $\overline{CAS}$-Referenced	0		0		0		ns	12
t_{CAC}	$\overline{OE}$ Access Time		20		25		30	ns	9
t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to Output High-Z		20		25		30	ns	13
t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Output Low-Z	0		0		0		ns	
t_{OH}	Output Hold Time from $\overline{OE}$ or $\overline{CAS}$	0		0		0		ns	

Write Cycle

Symbol	Parameter	GM53C261-80		GM53C261-10		GM53C261-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25		30		35		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25		30		35		ns	
t_{WP}	Write Command Pulse Width	15		20		25		ns	
t_{WCS}	Write Command Setup Time	0		0		0		ns	14
t_{WCH}	Write Command Hold Time	15		20		25		ns	
t_{DS}	Data in Setup Time	0		0		0		ns	
t_{DH}	Data in Hold Time	15		20		25		ns	
t_{WBS}	Write Mask Setup Time	0		0		0		ns	
t_{WBH}	Write Mask Hold Time	20		20		20		ns	
t_{WS}	Write Mask Select Setup Time	0		0		0		ns	
t_{WH}	Write Mask Select Hold Time	20		20		20		ns	
t_{OEH}	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	10		10		15		ns	
t_{WCR}	Write Hold Time from $\overline{RAS}$	65		80		95		ns	
t_{DHR}	Data Hold Time from $\overline{RAS}$	65		80		95		ns	

Read-Modify-Write Cycle

Symbol	Parameter	GM53C261-80		GM53C261-10		GM53C261-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	205		245		285		ns	
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	140	37K	170	37K	200	37K	ns	
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	85		100		115		ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	110		135		160		ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	55		65		75		ns	14
t_{AWD}	Column Address to $\overline{WE}$ Delay	70		80		95		ns	
t_{OED}	$\overline{OE}$ to Data in Delay Time	20		25		30		ns	

Fast Page Mode Operation

Symbol	Parameter	GM53C261-80		GM53C261-10		GM53C261-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{PC}	Page Mode Cycle Time	55		60		70		ns	
t_{CP}	$\overline{CAS}$ Precharge Time	15		20		25		ns	
t_{CAP}	Access Time from Column Precharge		50		55		65	ns	15

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

Symbol	Parameter	GM53C261-80		GM53C261-10		GM53C261-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{CSR}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Setup Time	10		10		10		ns	
t_{CHR}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Hold Time	25		25		25		ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0		0		ns	

Read/Write, Pseudo Write Transfer and Serial Read/Write Cycle

Symbol	Parameter	GM53C261-80		GM53C261-10		GM53C261-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{SCC}	Serial Clock Cycle Time	30		35		40		ns	
t_{SCL}	SC Precharge Time	10		10		10		ns	
t_{SOO}	$\overline{SE}$ to Serial Out Setup Time	0		0		5		ns	
t_{SOH}	Serial Out Hold after SC High	0		0		5		ns	
t_{SCA}	Serial Output Access Time from SC		25		30		35	ns	16
t_{SOA}	Serial Output Access Time from $\overline{SE}$		20		25		30	ns	16
t_{SOZ}	Serial Output Disable Time from $\overline{SE}$ High		15		20		25	ns	13
t_{SCH}	SC Pulse Width	10		15		15		ns	
t_{SOE}	$\overline{SE}$ Pulse Width	10		10		10		ns	
t_{SOP}	$\overline{SE}$ Precharge Time	10		10		10		ns	
t_{DLS}	Transfer Command to $\overline{RAS}$ Setup Time	0		0		0		ns	
t_{RDH}	Transfer Command to $\overline{RAS}$ Hold Time	60		75		90		ns	
t_{CDH}	Transfer Command to $\overline{CAS}$ Hold Time	20		25		30		ns	
t_{SDD}	SC to Transfer Command Lead Time	10		15		20		ns	
t_{SDH}	SC Hold Time after $\overline{DT}$ High	10		10		10		ns	
t_{SZS}	Serial Data Input to $\overline{DT}$ High Delay Time		0		0		0	ns	
t_{DTP}	$\overline{DT}$ Precharge Time	20		25		30		ns	
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	65		75		85		ns	
t_{SWS}	Serial Write Enable Setup Time	10		10		10		ns	
t_{SWH}	Serial Write Enable Hold Time	10		15		20		ns	
t_{SWIS}	Serial Write Disable Setup Time	10		10		10		ns	
t_{SWIH}	Serial Write Disable Hold Time	10		15		20		ns	
t_{SRS}	SC to $\overline{RAS}$ Setup Time	10		20		20		ns	

AC Characteristics (Cont'd)

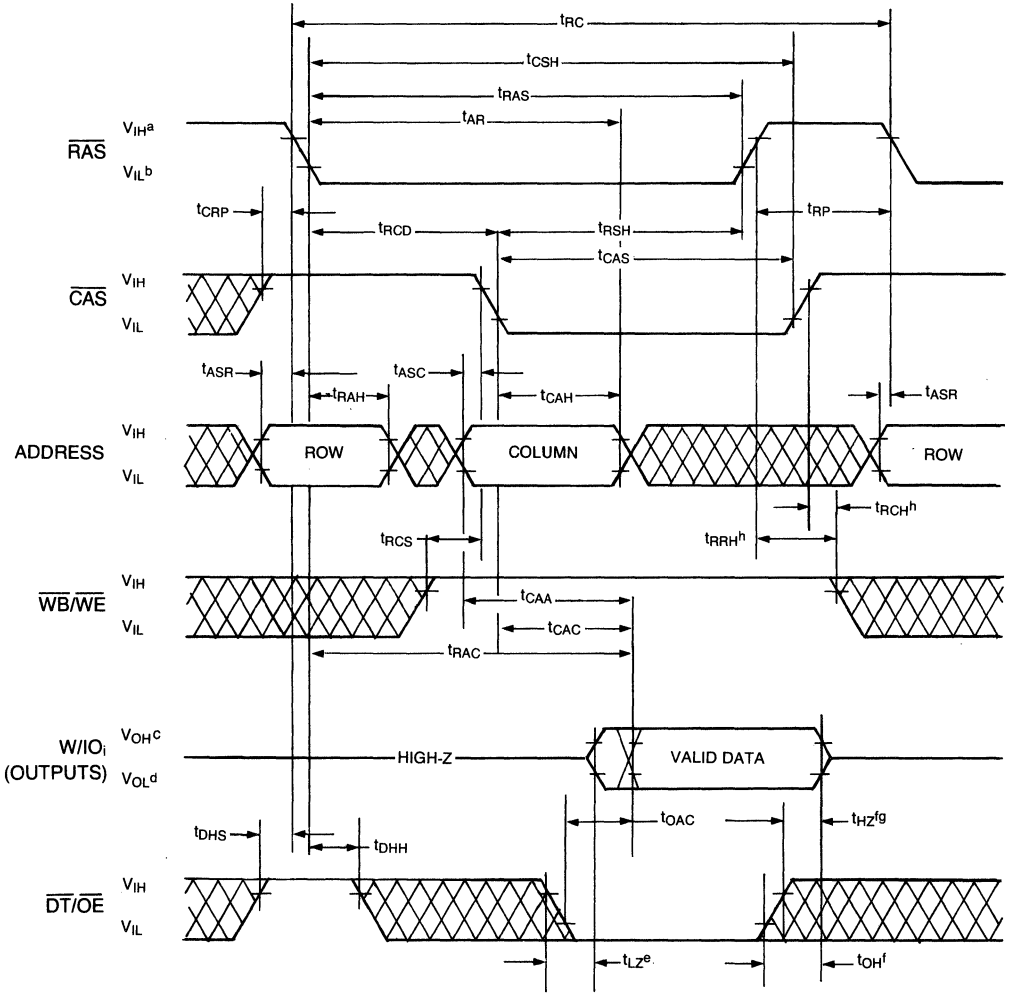
Read/Write, Pseudo Write Transfer and Serial Read/Write Cycle

Symbol	Parameter	GM53C261-80		GM53C261-10		GM53C261-12		Unit	Note
		Min	Max	Min	Max	Min	Max		
t_{ES}	Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Setup Time	0		0		0		ns	
t_{EH}	Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Hold time	20		20		20		ns	
t_{SIS}	Serial Data in Setup Time	0		0		0		ns	
t_{SIH}	Serial Data in Hold Time	10		10		10		ns	
t_{SDS}	SC to $\overline{DT}$ High Setup Time	0		0		0		ns	
t_{SCR}	SC to $\overline{RAS}$ Precharge Setup Time	0		0		0		ns	

Notes :

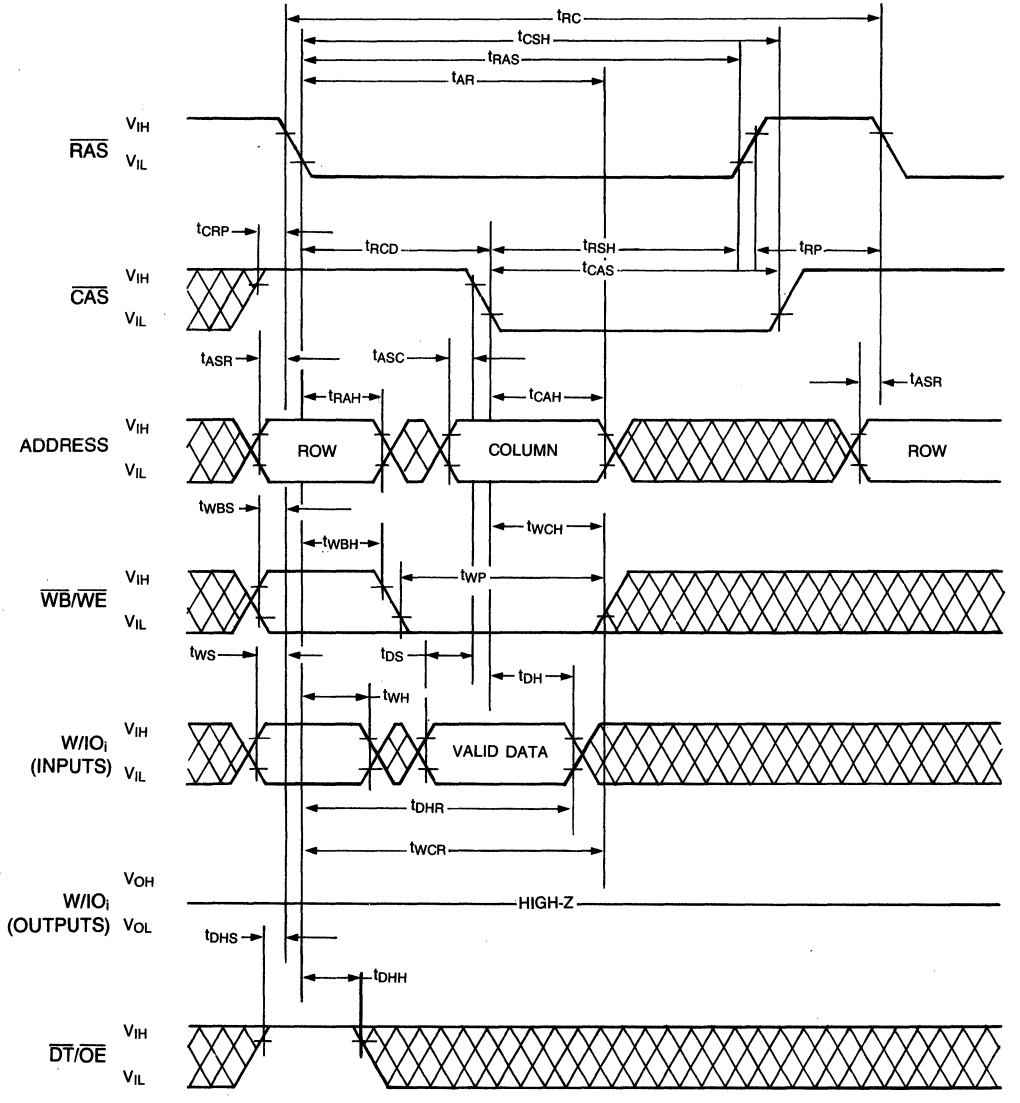
1. All voltages are referenced to V_{SS}.
2. I_{CC} is dependent on output loading when the device output is enabled. I_{CC} (max.) is measured with all outputs open.
3. I_{CC} is dependent on the number of address transitions while $\overline{CAS}$ is at V_{IH}. Specified I_{CC} (max.) is measured with a maximum of two transitions per address input per random cycle and one transition per address cycle in Fast Page Mode.
4. V_{IH} (min.) and V_{IL} (max.) are the reference levels for measuring input signal timing. Transition times are measured between V_{IH} (min.) and V_{IL} (max.)
5. An initial pause of 200μs and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks or upon Power Up. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
6. AC characteristics assume t_T=5 ns. All AC measurements are made with a load equivalent to two TTL inputs and either 50 or 100 pF in parallel. V_{IL} (min.) $\geq$ V_{SS} and V_{IH} (max.) $\leq$ V_{CC}.
7. t_{RCD} (max.) is for reference only t_{RCD} (min.) = t_{RAH} (min) + 2t_T + t_{ASC} (min.)
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If $t_{RCD} \geq t_{RCD}$ (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.)
9. Measured with a load equivalent to 2 TTL loads and 100pF in Parallel.
10. Assumes $t_{RCD} \geq t_{RCD}$ (max.).
11. If $t_{ASC} \leq (t_{CAA}$ (max.)-t_{CAC} (max.)-$t_T)$, access time is defined by t_{CAA} rather than t_{CAC}.
12. Either t_{RCH} or t_{RRH}must be satisfied.
13. An output disable time defines the time when the output reaches the open-circuit condition and is not referenced to output voltage levels.
14. t_{WCS}, t_{RWD} and t_{CWD} are specified for reference only. If $T_{WCS} \geq t_{WCS}$ (min.), the cycle is a $\overline{CAS}$ controlled write cycle (Early Write), and the I/O pins will be at High-Z during the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min.), and $t_{RWD} \geq t_{RWD}$ (min.), the cycle is a Read-Modify-Write cycle, and the I/Opins will reflect the data read from the addressed location. If any of the above conditions is not satisfied, the condition of the Data Out pins will be indeterminate.
15. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
16. Measured with a load equivalent to 2 TTL loads and 50 pF in parallel.

TIMING WAVEFORMS
READ CYCLE

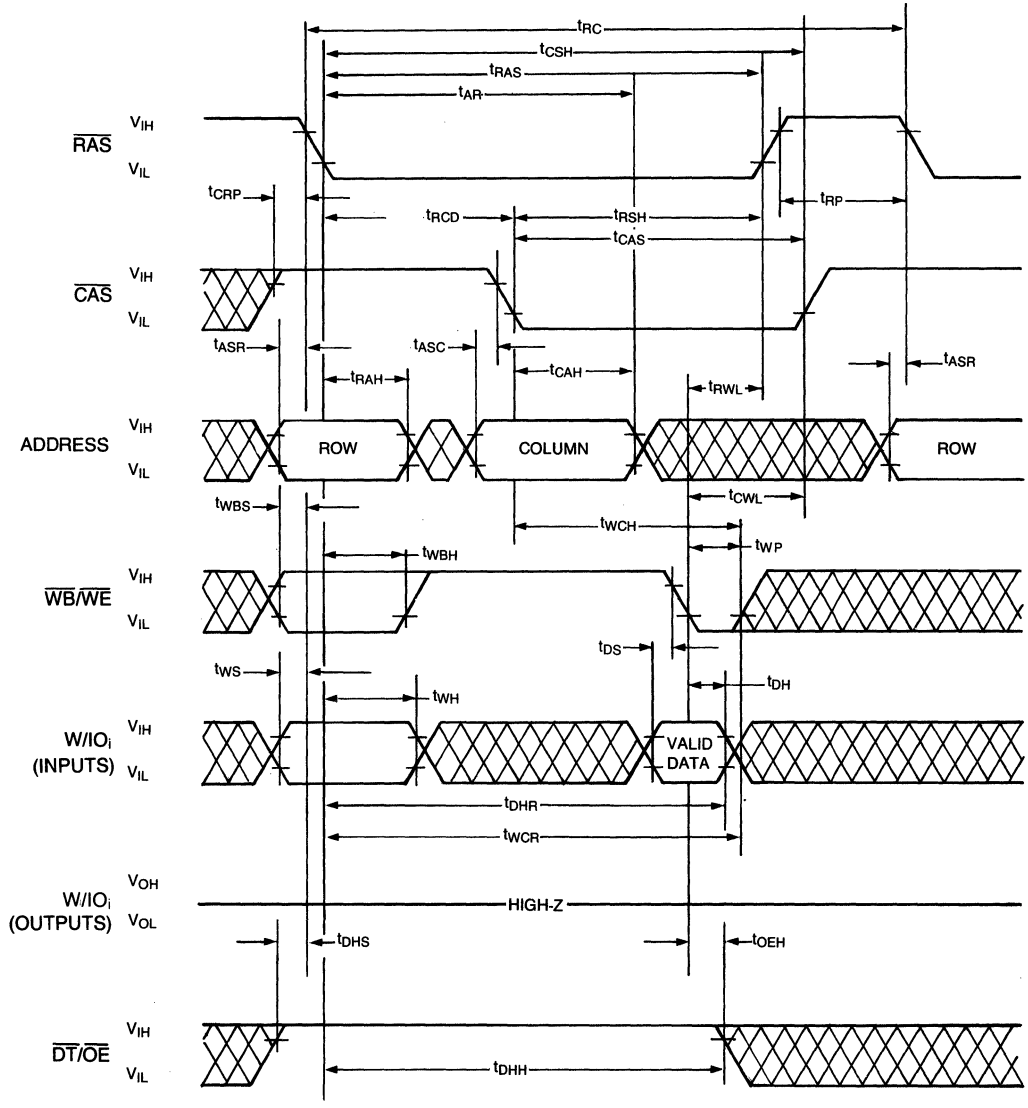


NOTES:
a., b. V_{IH} and V_{IL} (max) are reference levels for measuring timing of input signals.
c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.
e. t_{LZ} is referenced to the later or $\overline{CAS}$ and $\overline{OE}$ low transition.
f. t_{HZ} and t_{OH} are referenced to the earlier of $\overline{CAS}$ and $\overline{OE}$ High transition.
g. Transition is measured +500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).
h. Either t_{RCH} or t_{RRH} must be satisfied.

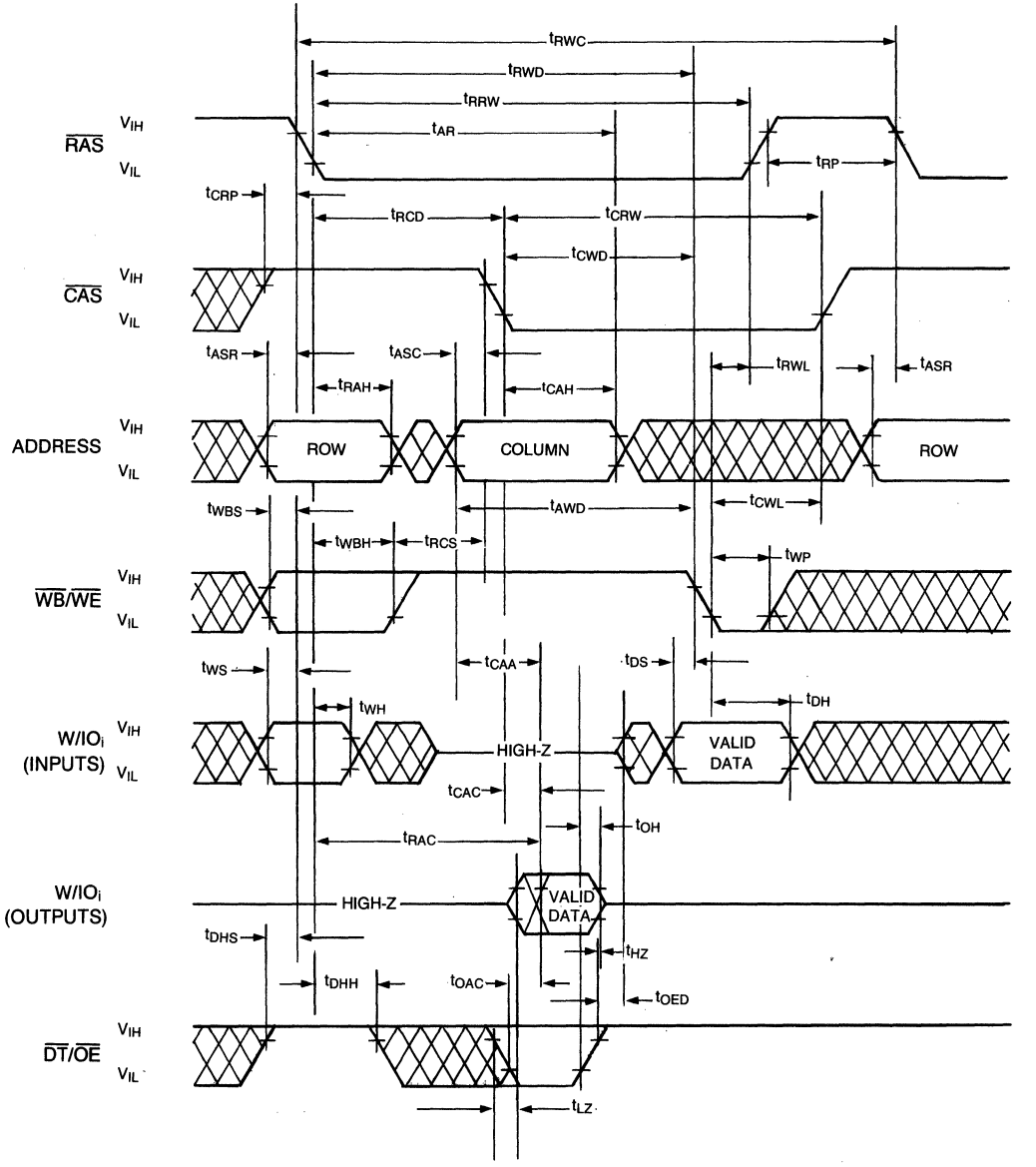
WRITE CYCLE (EARLY WRITE)



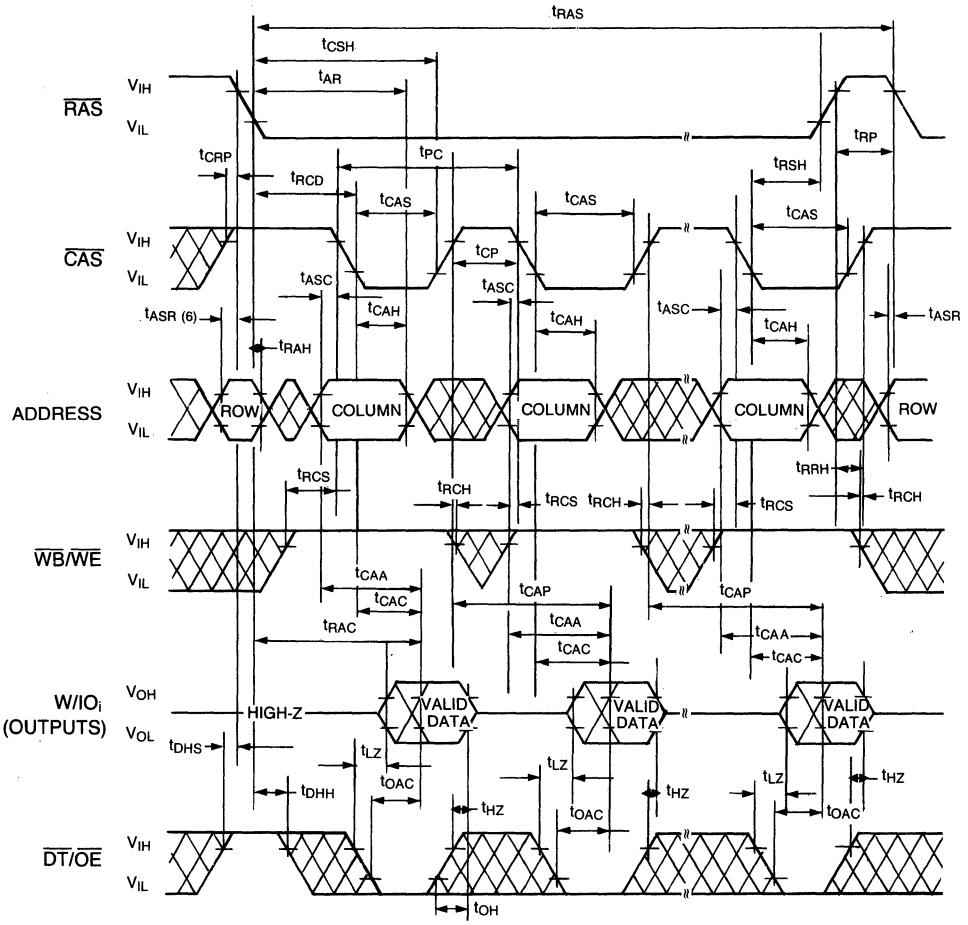
WRITE CYCLE (DELAYED WRITE)



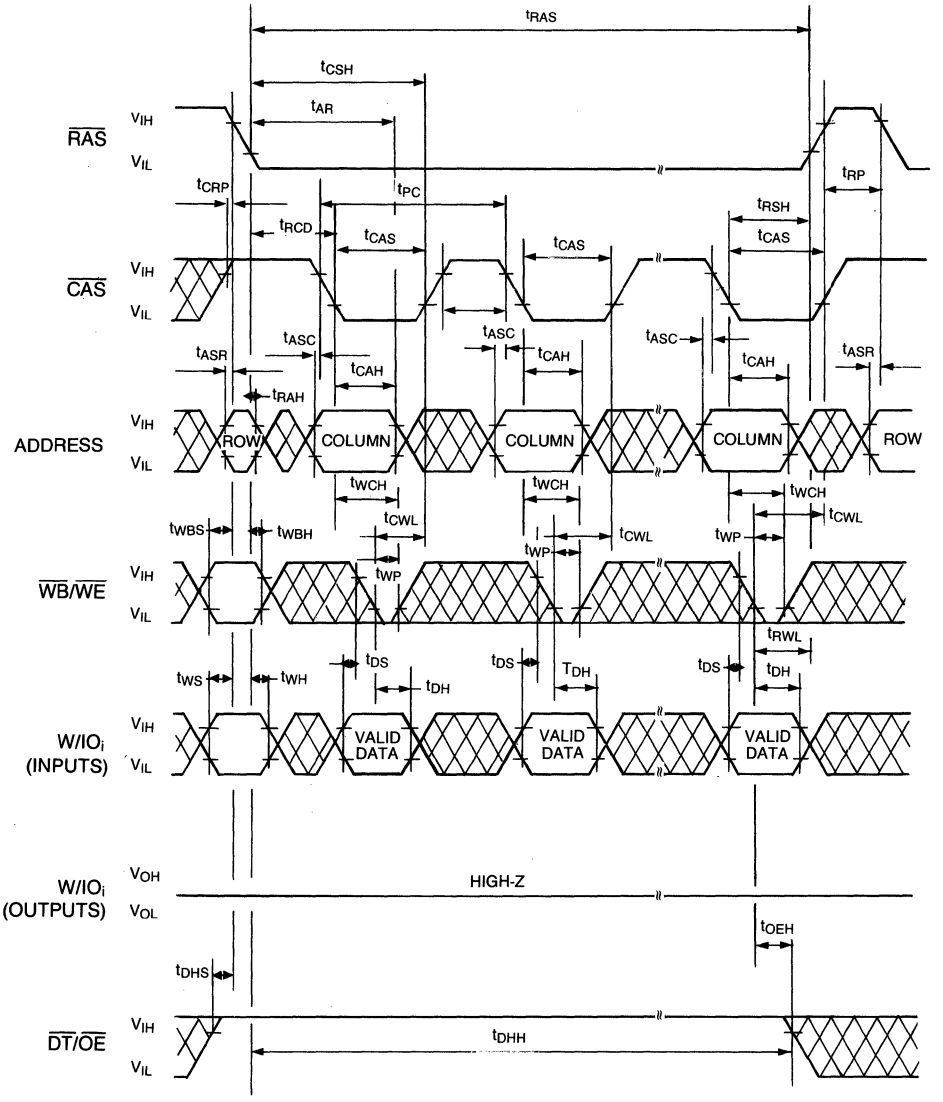
READ-MODIFY-WRITE CYCLE



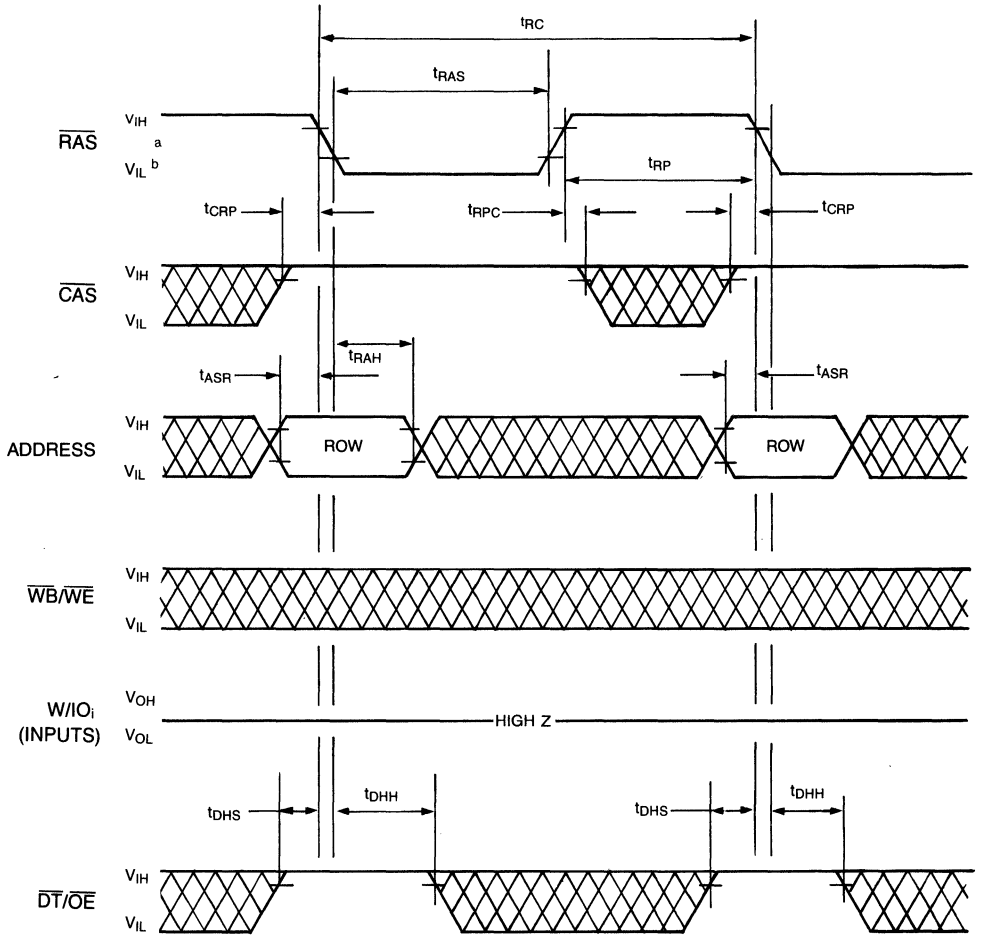
FAST PAGE MODE READ CYCLE



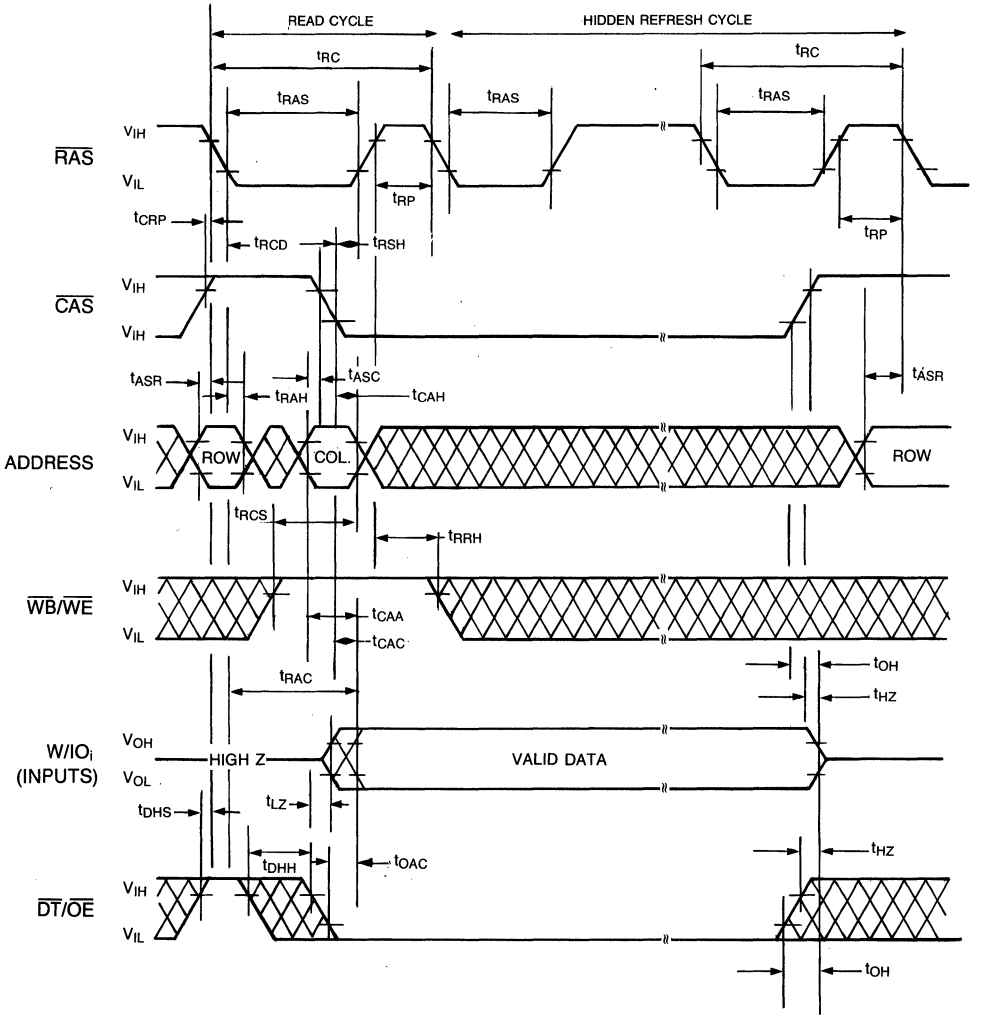
FAST PAGE MODE WRITE CYCLE



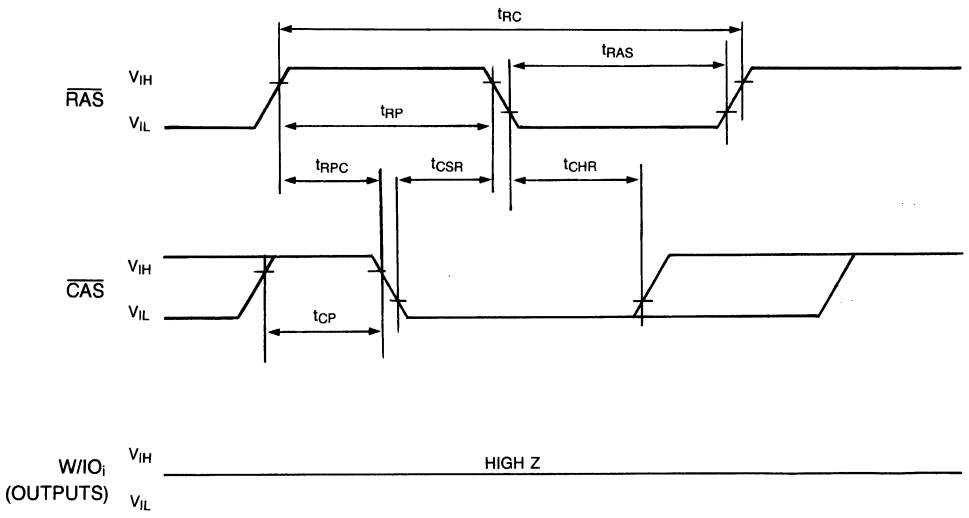
$\overline{RAS}$-ONLY REFRESH CYCLE



HIDDEN REFRESH CYCLE

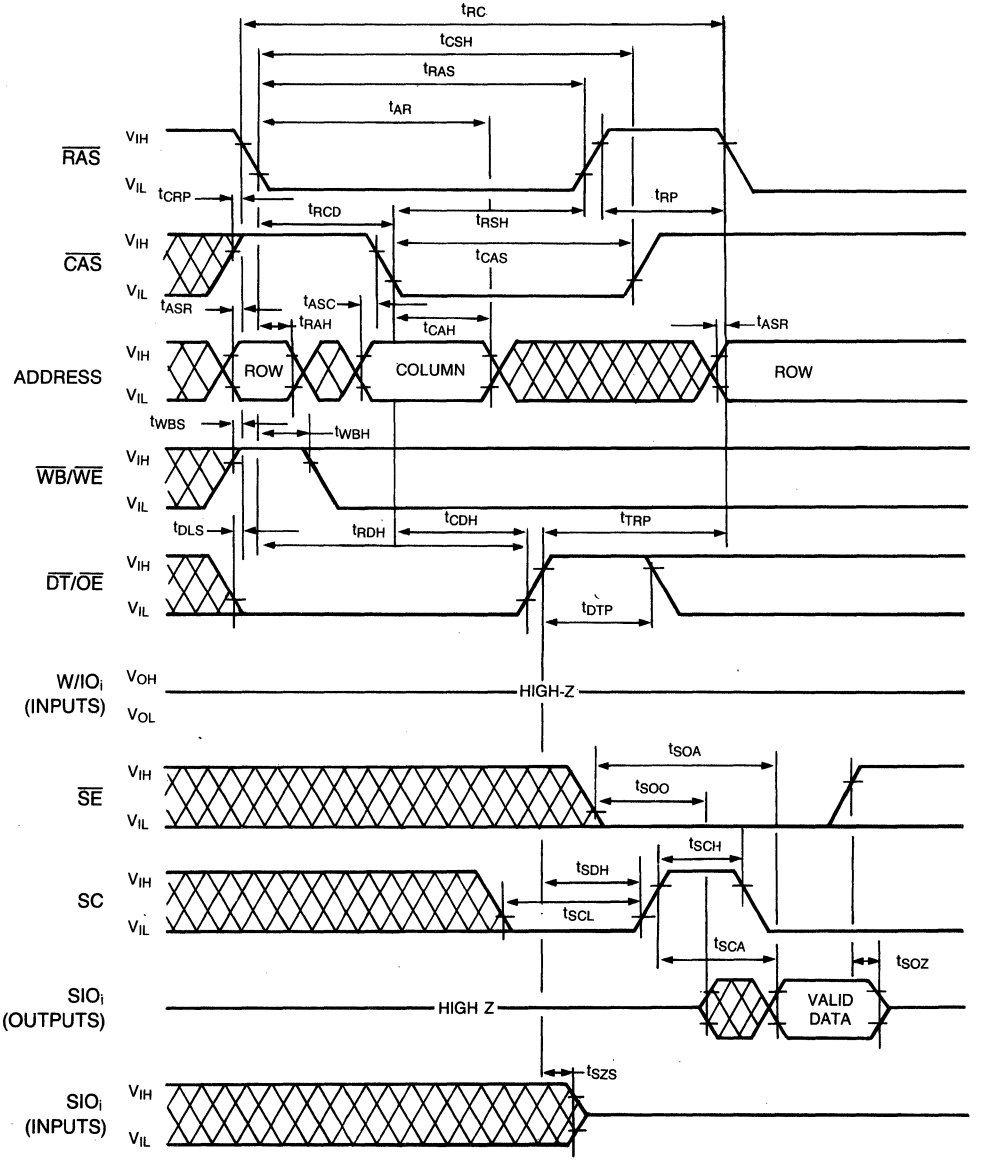


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



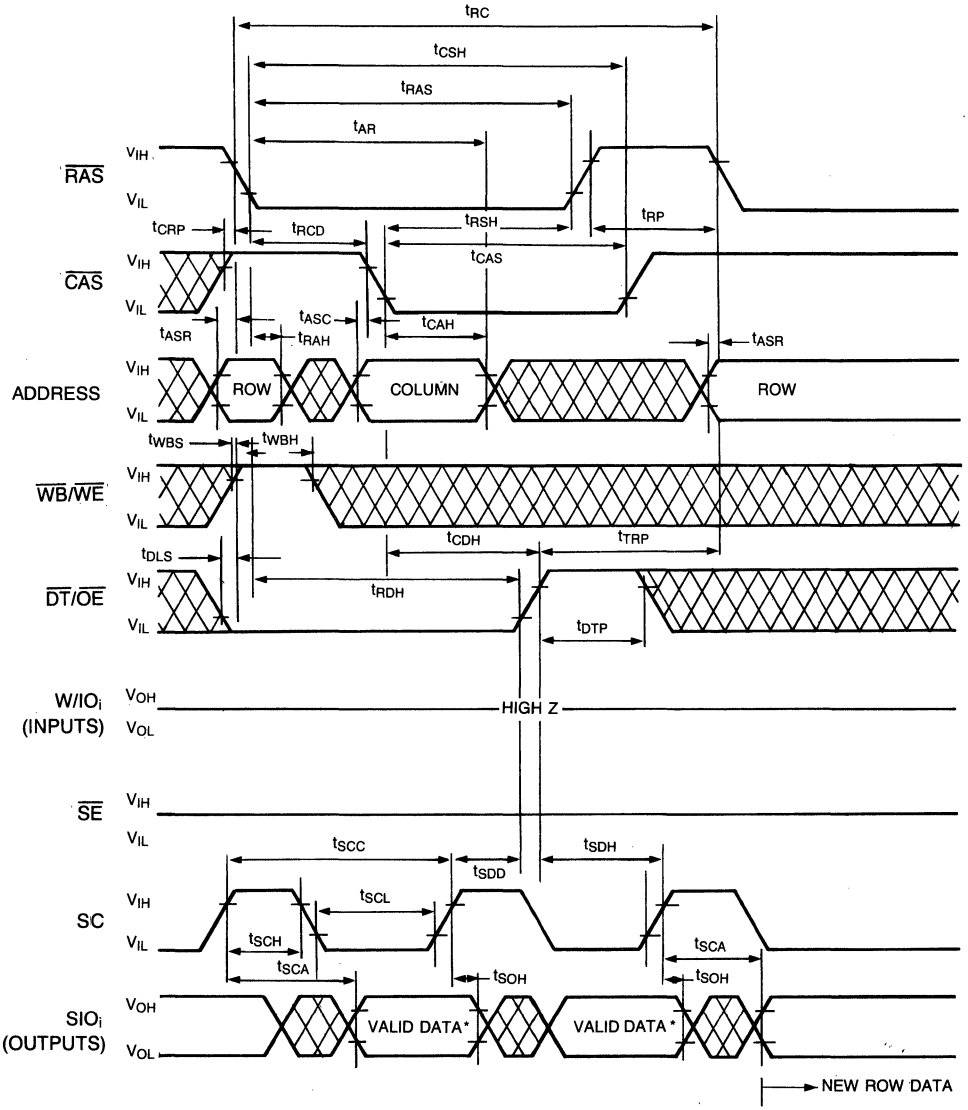
A0-A7 = DON'T CARE
$\overline{DT}/\overline{OE}$ = DON'T CARE
$\overline{WB}/\overline{WE}$ = DON'T CARE

READ TRANSFER CYCLE (RAM-SAM) SERIAL READ SETUP*

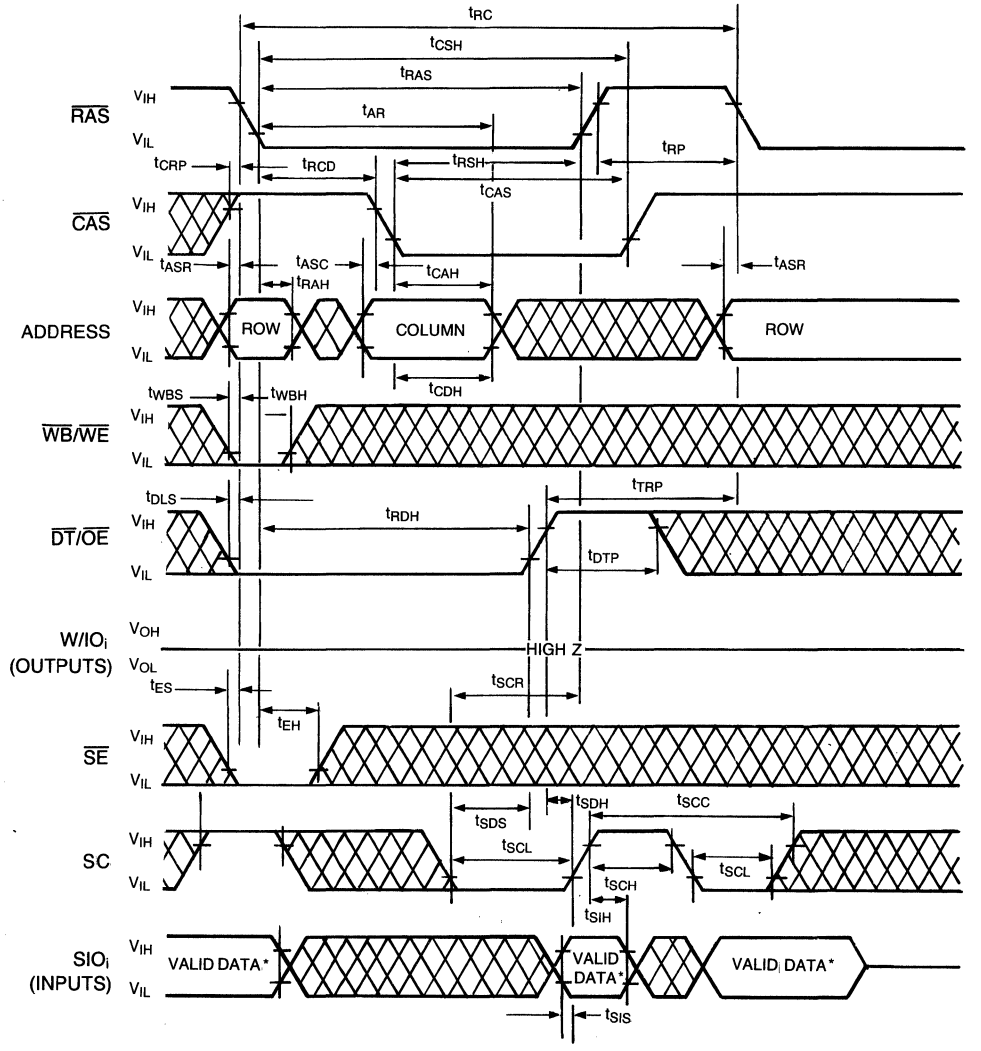


NOTE: *IN THE CASE THAT THE PREVIOUS TRANSFER IS WRITE TRANSFER.

REAL-TIME-READ TRANSFER CYCLE (RAM-SAM)

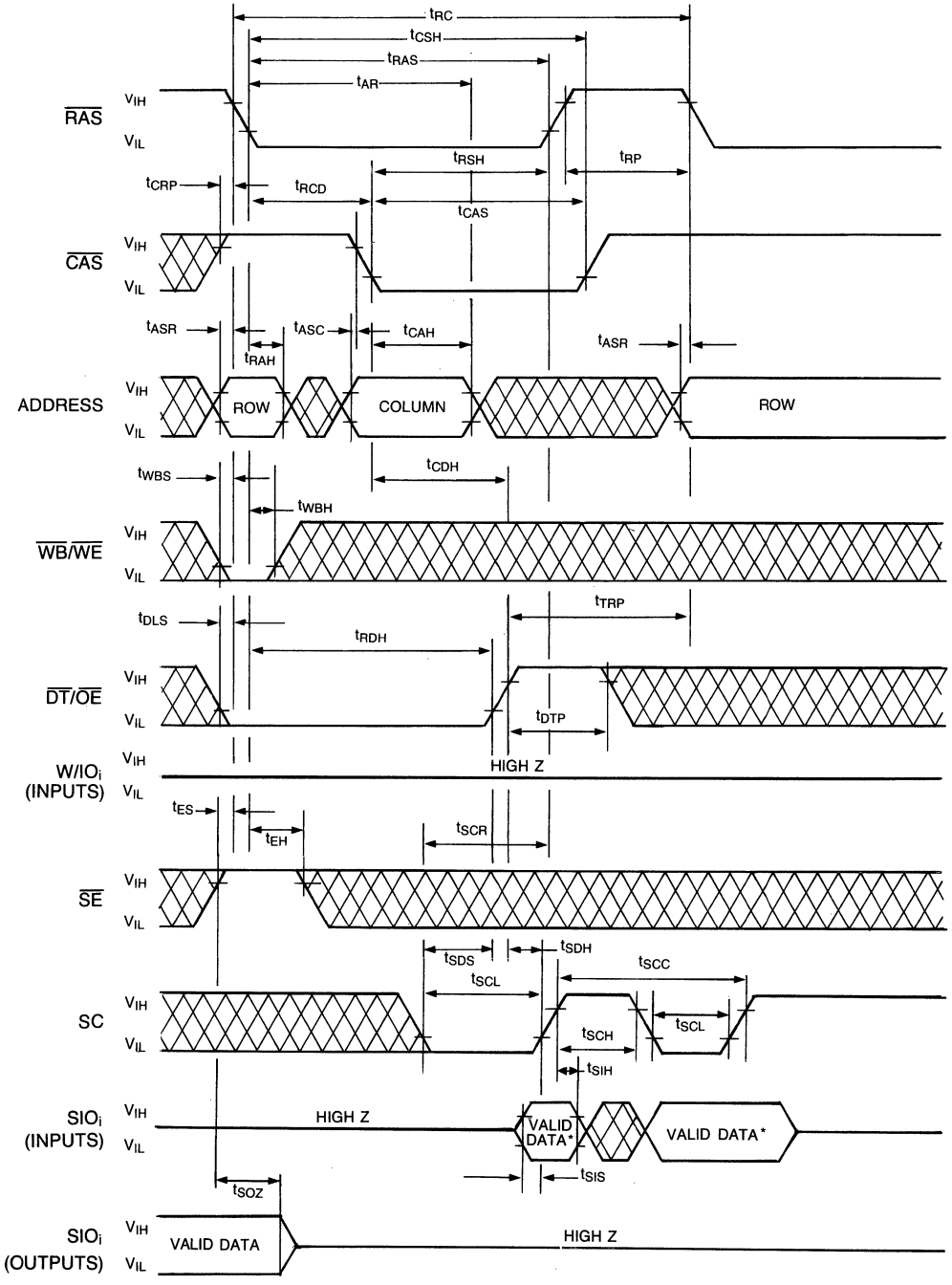


WRITE TRANSFER CYCLE (SAM-RAM)



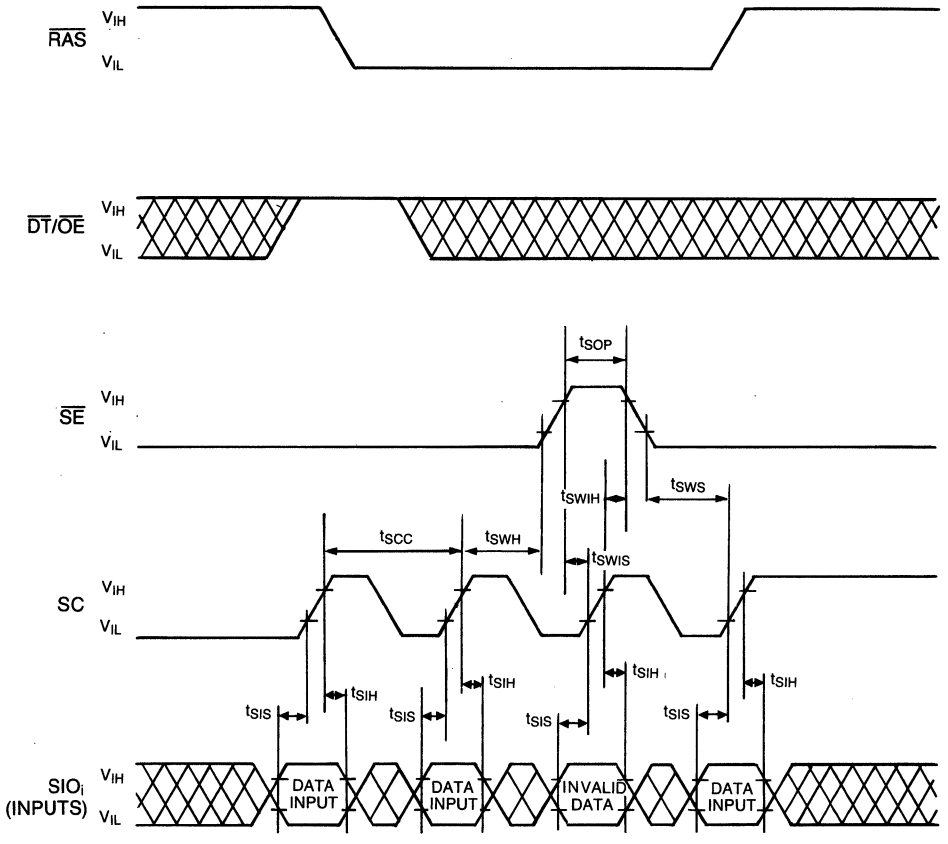
NOTE* IF $\overline{SE}$ IS "H" LEVEL, THE SERIAL INPUT DATA ARE NOT WRITTEN INTO THE DATA REGISTER, BUT THE SERIAL DATA SELECTOR CONTINUES TO FUNCTION.

PSEUDO WRITE TRANSFER CYCLE SERIAL WRITE SETUP

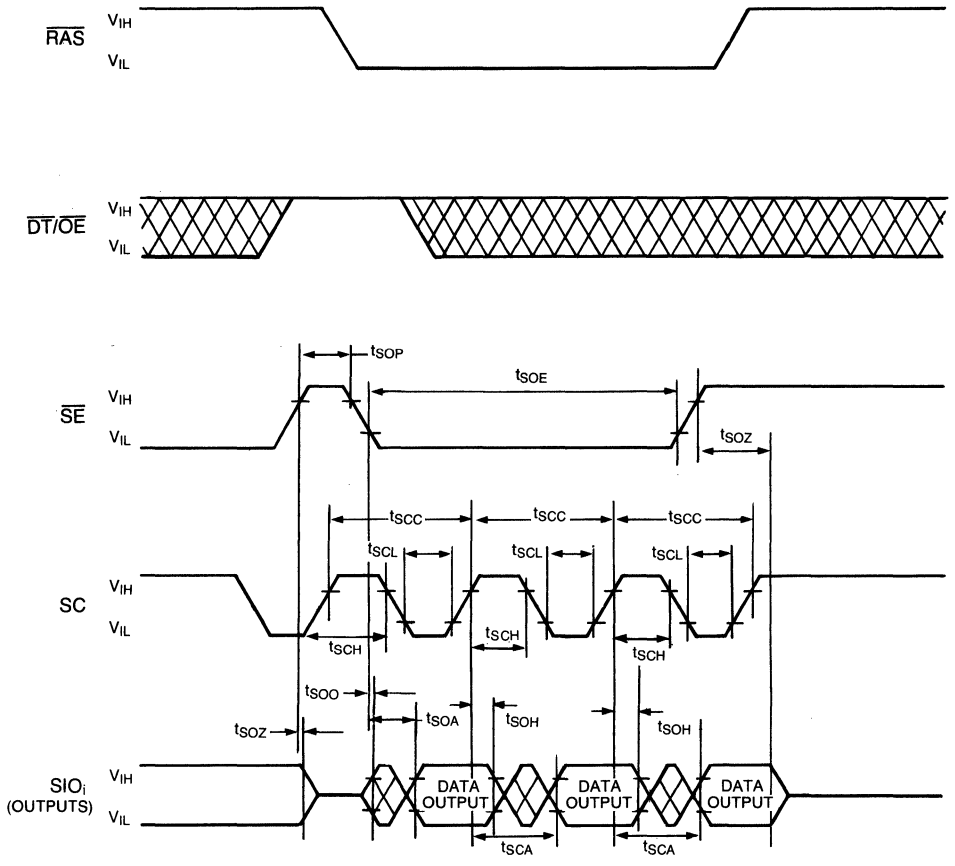


NOTE* IF $\overline{SE}$ IS "H" LEVEL, THE SERIAL INPUT DATA ARE NOT WRITTEN INTO THE DATA REGISTER, BUT THE SERIAL DATA SELECTOR IS WORKED.

SERIAL WRITE CYCLE



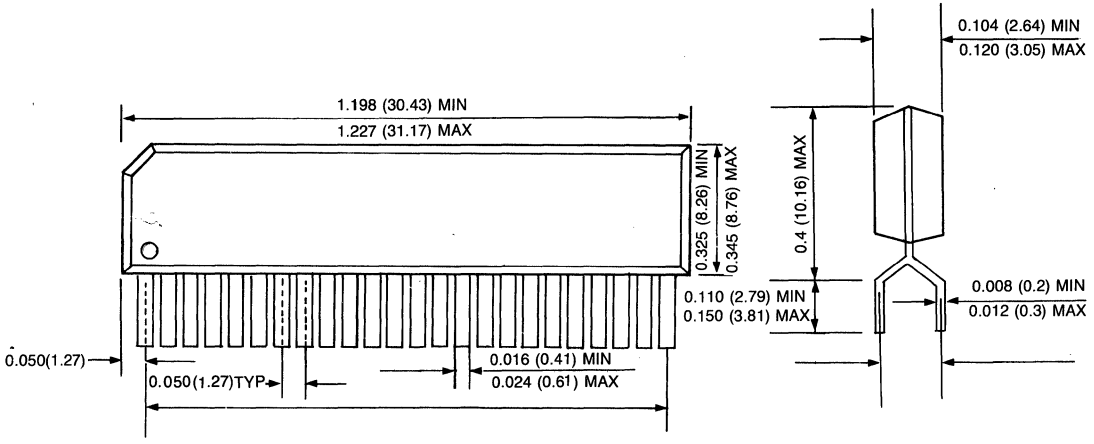
SERIAL READ CYCLE

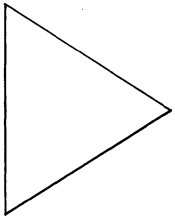


Package Dimensions

Unit: inches (mm)

24 ZIP





GM76C28A

2,048 WORDS × 8 BIT
CMOS STATIC RAM

Description

The GM76C28A is 2,048 words×8 bits asynchronous, static random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

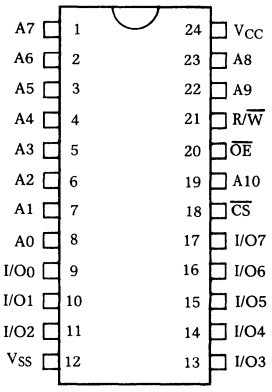
Features

- Access time: 100/120ns
- Low Power Consumption
  Standby: 1μA
  Operation: 25/30mA
- Complete static operation
- Single power supply: 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output with Wired-OR capability
- Non-volatile storage with back-up batteries
- Standard 24 DIP (600mil)/24 SOP (330mil)/ 24 DIP (300mil)

Pin Description

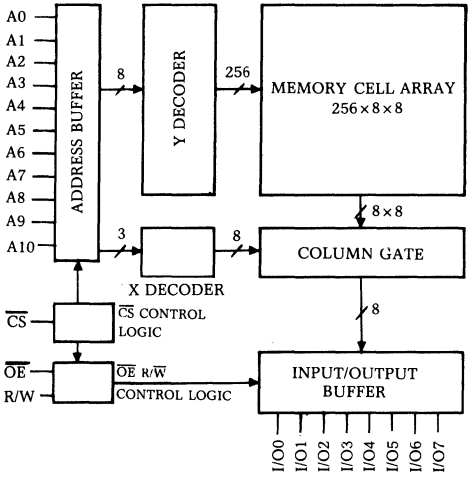
Pin	Function
A0~A10	Address Inputs
R/$\overline{W}$	Read/Write
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O0~7	Data Input/Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground

Pin Configuration



(Top View)

Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0~70	°C
T_{STG}	Storage Temperature	-65~150	°C
V_{IN}/V_{OUT}	Voltage on any Pin Relative to V_{SS}	-0.5~7.0	V
P_D	Power Dissipation	1.0	W

*Note: Operation at or above "Absolute Maximum Ratings" can adversely affect device reliability.

Recommended Operating Conditions (T_A=0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5	—	0.8	V

*All voltages are referenced to V_{SS} pin=0V.

Truth Table

$\overline{CS}$	$\overline{OE}$	R/$\overline{W}$	A0 to A10	DATA I/O	MODE	I_{CC}
H	—	—	—	Hi-Z	Unselected	I_{CCS1}, I_{CCS2}
L	L	H	Stable	Output Data	Read	I_{CC}
L	H	L	Stable	Input Data	Write	I_{CC}
L	L	L	Stable	Input Data	Write	I_{CC}

Note: — means "H", "L" or "Hi-Z"

Electrical Characteristics

DC Electrical Characteristics (V_{CC}=5V±10%, V_{SS}=0V, T_A=0~70°C)

Symbol	Parameter	Conditions	GM76C28A-10			GM76C28A-12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
V_{OL}	Low Level Output Voltage	I_{OL}=4.0mA			0.4			0.4	V
V_{OH}	High Level Output Voltage	I_{OH}=-1.0mA	2.4			2.4			V
I_{CC1}	Operating Supply Current	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA		30	60		25	50	mA
I_{CC2}		V_{IH}=3.5V, V_{IL}=0.6V, $I_{I/O}$=0mA		16			16		mA
I_{CC}	Average Operating Current	Min cycle, duty=100%, $I_{I/O}$=0mA		30	60		25	50	mA
I_{CCS1}	Standby Supply Current	$\overline{CS}$=V_{IH}		1.5	3.0		1.5	3.0	mA
I_{CCS2}		$\overline{CS}$=V_{CC}-0.2V		1	50		1	50	μA
$I_{I(L)}$	Input Leakage Current	V_{CC}=5.5V, V_I=0 to V_{CC}	-1		1	-1		1	μA
$I_{O(L)}$	Output Leakage Current	$\overline{CS}$=V_{IH}, or $\overline{OE}$=V_{IH}, $V_{I/O}$=0 to V_{CC}	-1		1	-1		1	μA

*Typical values are for reference with V_{CC}=5V and T_A=25°C assumed.

AC Electrical Characteristics:

Read Cycle ($V_{CC}=5V\pm10\%$, $T_A=0\sim70°C$)

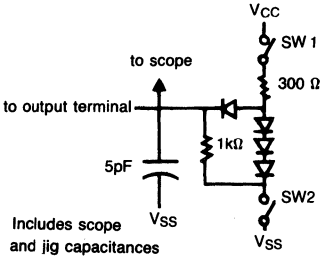
Symbol	Parameter	Conditions	GM76C28A-10		GM76C28A-12		Unit
			Min	Max	Min	Max	
t_{RC}	Read Cycle Time	*1	100		120		ns
t_{AA}	Address Access Time			100		120	ns
t_{ACS}	$\overline{CS}$ Access Time			100		120	ns
t_{CLZ}	$\overline{CS}$ Output Setup Time	*2	10		10		ns
t_{OE}	$\overline{OE}$ Access Time	*1		55		60	ns
t_{OLZ}	$\overline{OE}$ Output Setup Time	*2	5		10		ns
t_{CHZ}	$\overline{CS}$ Output Floating		0	40	0	40	ns
t_{OHZ}	$\overline{OE}$ Output Floating		0	40	0	40	ns
t_{OH}	Output Hold Time	*1	10		10		ns

Write Cycle: ($V_{CC}=5V\pm10\%$, $T_A=0\sim70°C$)

Symbol	Parameter	Conditions	GM76C28A-10		GM76C28A-12		Unit
			Min	Max	Min	Max	
t_{WC}	Write Cycle Time	1	100	—	120	—	ns
t_{CW}	Chip Select Time ($\overline{CS}$)		80	—	85	—	ns
t_{AW}	Address Enable Time		80	—	85	—	ns
t_{AS}	Address Setup Time		0	—	0	—	ns
t_{WP}	Write Pulse Width		65	—	70	—	ns
t_{OHZ}	$\overline{OE}$ Output Floating	*2	0	40	0	40	ns
t_{WHZ}	R/W Output Floating	*3	0	45	0	50	ns
t_{DW}	Input Data Setup Time	*1	45	—	50	—	ns
t_{WR}	Address Hold Time		0	—	0	—	ns
t_{DH}	Input Data Hold Time		0	—	0	—	ns
t_{OW}	R/W Output Setup Time	*3	5	—	10	—	ns

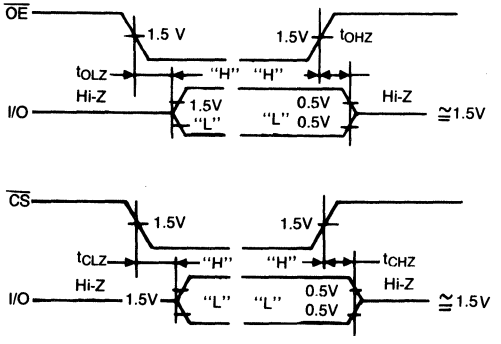
*1 Test conditions.
1. Input pulse level: 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Input/output timing reference level: 1.5V
4. Output load: 1 TTL + C_L = 100pF

*2 Test conditions.
1. Input pulse level: 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Test circuit

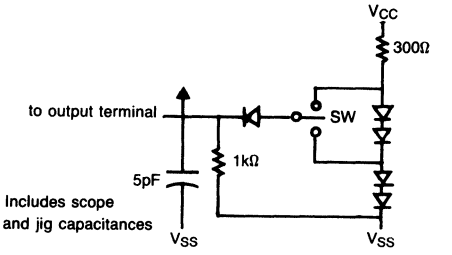


- Both SW1 and SW2 are closed when measuring t_{CHZ} or t_{OHZ}.
- SW1 is open and SW2 is closed when measuring Hi-Z-high of t_{CLZ} or t_{OLZ}
- SW1 is closed and SW2 is open when measuring Hi-Z-low t_{CLZ} or t_{OLZ}

Output turn-on turn-off time

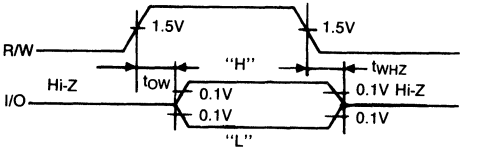


*3 Test conditions.
1. Input pulse level: 0.8V to 2.2V
2. $t_r = t_f = 10ns$
3. Test circuit

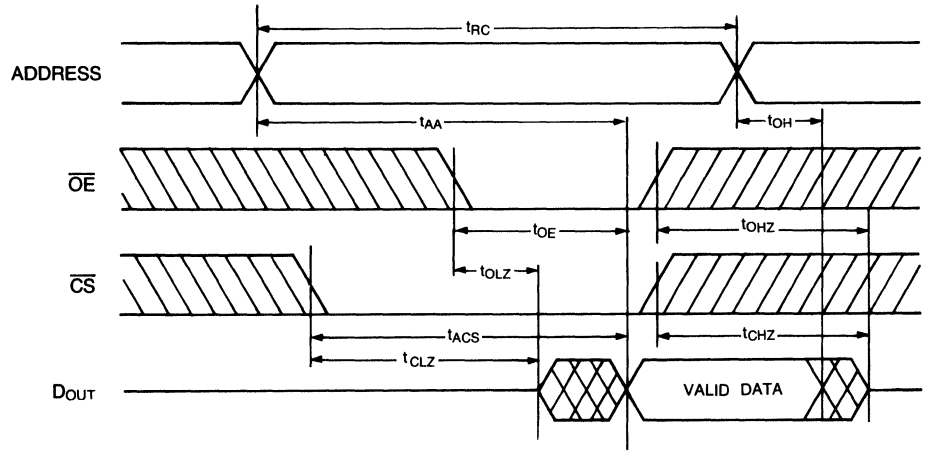


- SW is set to the V_{CC} side when measuring Hi-Z-high and high-Hi-Z of t_{OW} or t_{WHZ}
- SW is set to the V_{SS} side when measuring Hi-Z low and low-Hi-Z of t_{OW} or t_{WHZ}

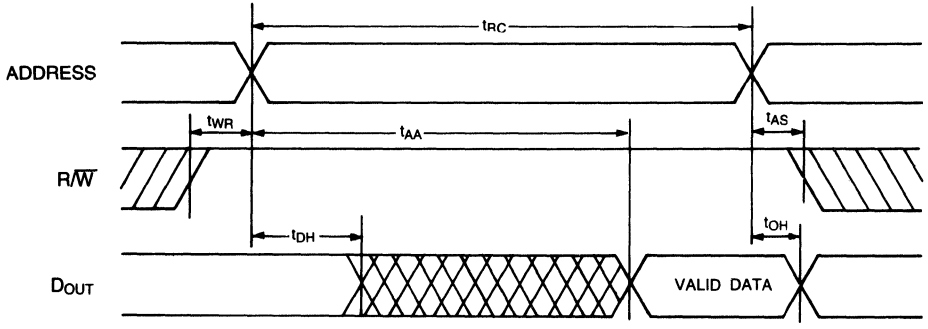
Output turn-on turn-off time



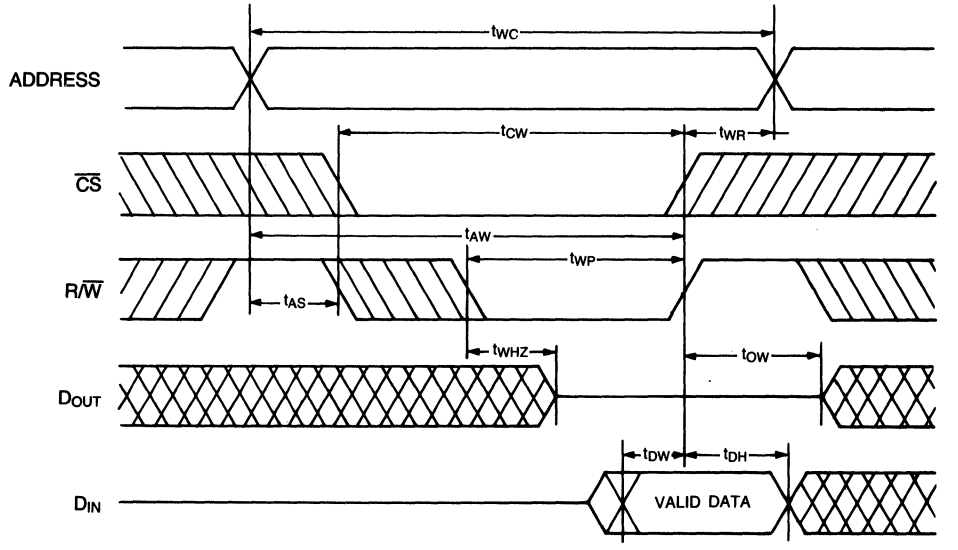
READ CYCLE 1 ($\overline{OE}$, $\overline{CS}$ CONTROL, R/$\overline{W}$ = HIGH)



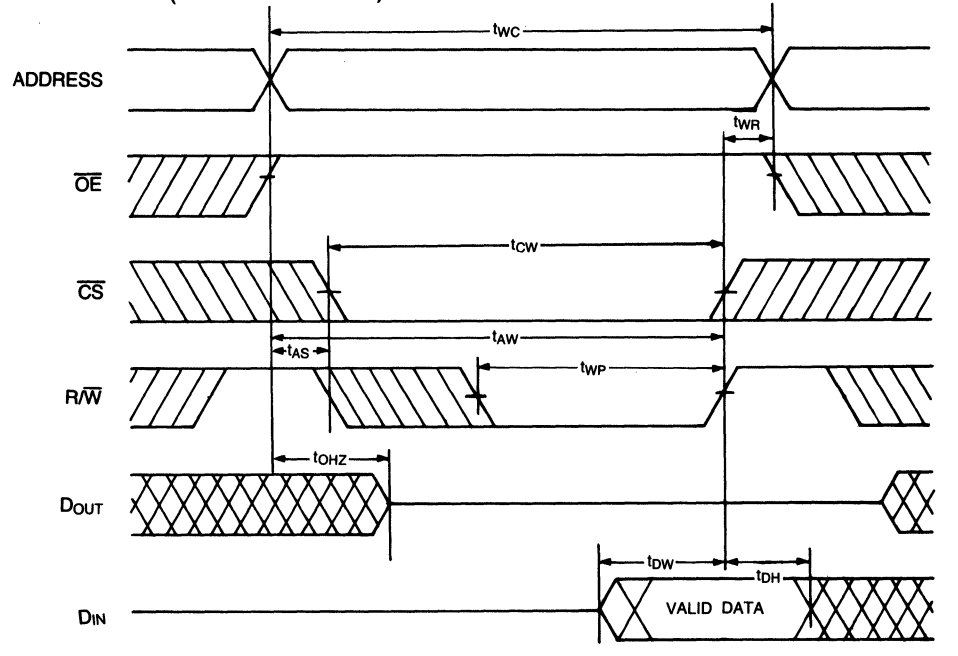
READ CYCLE 2 (R/$\overline{W}$ CONTROL, $\overline{OE}$ = LOW, $\overline{CS}$ = LOW)



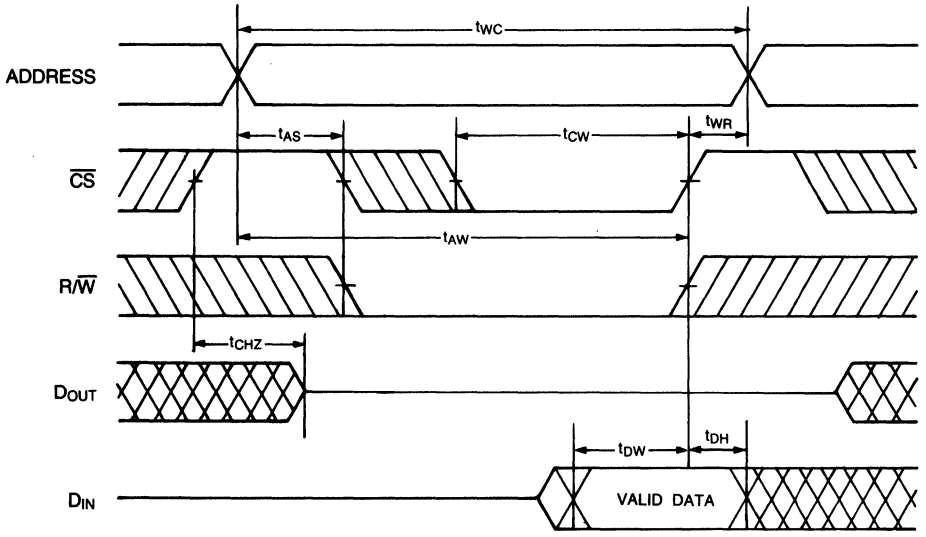
WRITE CYCLE 1 (R/$\overline{W}$ CONTROL, $\overline{OE}$ = LOW)



WRITE CYCLE 2 (R/$\overline{W}$ CONTROL)



WRITE CYCLE 3 ($\overline{CS}$ CONTROL, $\overline{OE}$ = LOW)



Capacitance ($f = 1MHz$, $T_A = 25°C$)

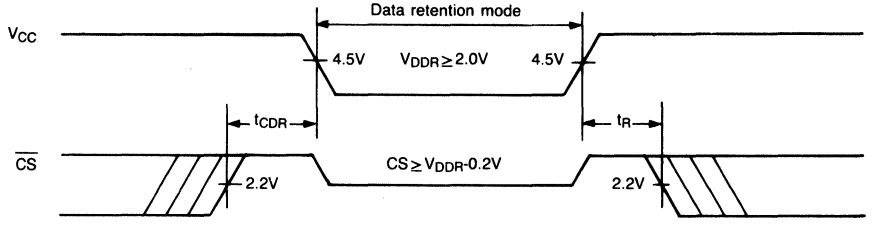
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_I	Input Capacitance	$V_I = 0V$		4	6	pF
$C_{I/O}$	I/O Capacitance	$V_{I/O} = 0V$		6	8	pF

Data Retention Characteristics ($T_A = 0 \sim 70°C$)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCR}	Data Retention Supply Voltage	$\overline{CS} \geq V_{CCR}-0.2V$	2.0	—	5.5	V
I_{CCR}	Data Retention Current	$V_{CC} = 3.0V$, $\overline{CS} \geq 2.8V$	—	-	25	μA
t_{CDR}	Chip Select Data Hold Time	Refer to the figure below	0	—	—	ns
t_R	Operation Recovery Time		t_{RC}*	—	—	ns

*t_{RC}: read cycle time

Data retention timing

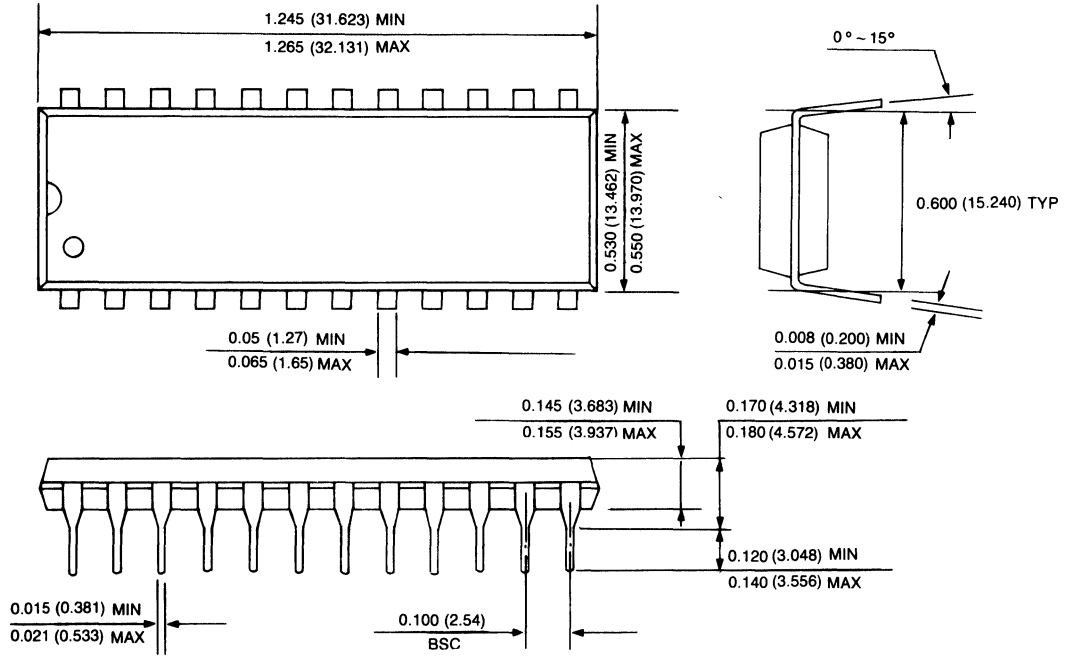


Note: When retaining data in standby mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

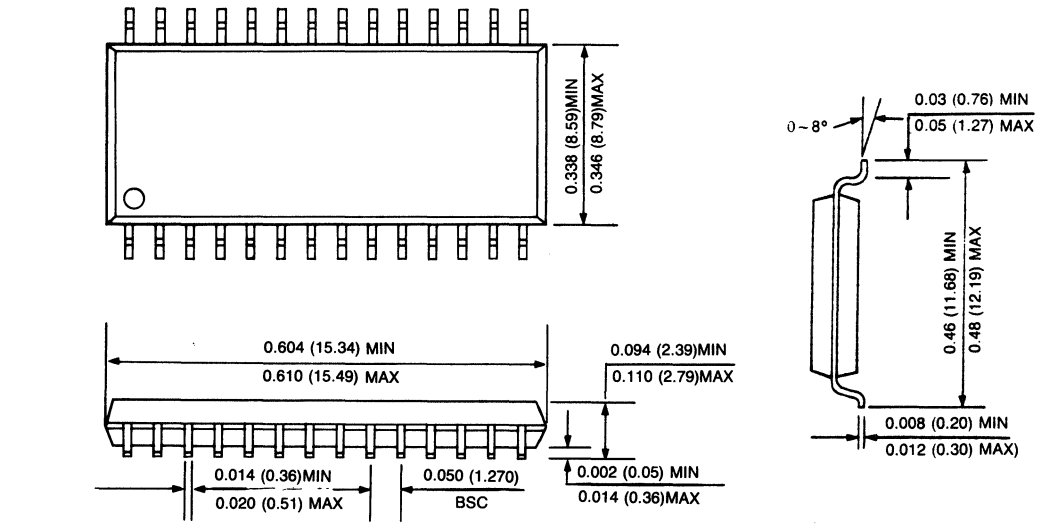
Package Dimensions

Unit: inches (mm)

24 DIP

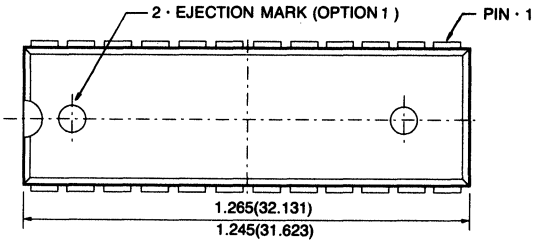


24 SOP

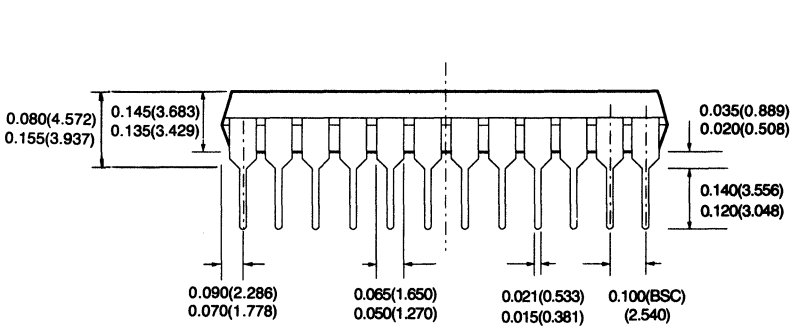


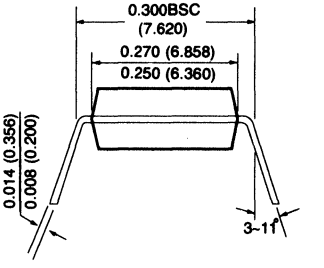
24 SKINNY

UNIT:INCH (mm) MAX/MIN



NOTE
1. LEAD FRAME, COPPER TTT
2. LEAD FINISH, SOLDER PLATED OR SOLDER COATED.
3. BACK EJECTOR PIN MARKED "KOREA"
4. BOTH PACKAGE LENGTH AND WIDTH DO NOT INCLUDE FLASH.
5. CONTROLLING DIMENSION; INCHES (mm)





GM76C88AL

8,192 WORDS × 8 BIT
CMOS STATIC RAM

Description

The GM76C88AL is 65,536 bit static random access memory organized as 8,192 words by 8 bits using CMOS technology and operated from a single 5V supply. Advanced Circuit techniques provide low power feature with a maximum operating current of 40mA and standby current of max. 100μA. Its very low standby power requirement makes it idel for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuits.

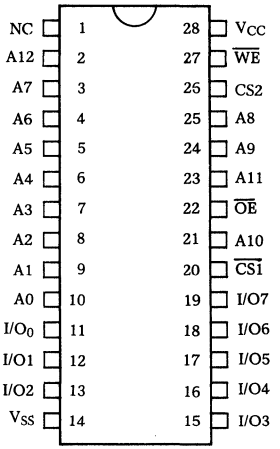
Features

- Access Time: 150ns.
- Low Power Consumption
  Standby: 2μA
  Operation: 3mA
- Completely Static RAM: No Clock or Timing Strobe Required
- Non-Volatile Storage with Back-Up Batteries
- 3-State Output with Wired-OR capability
- Directly TTL Compatible: All Inputs and Outputs
- Single +5V Operation (±10%)
- Standard 28 DIP and SOP capability

Pin Description

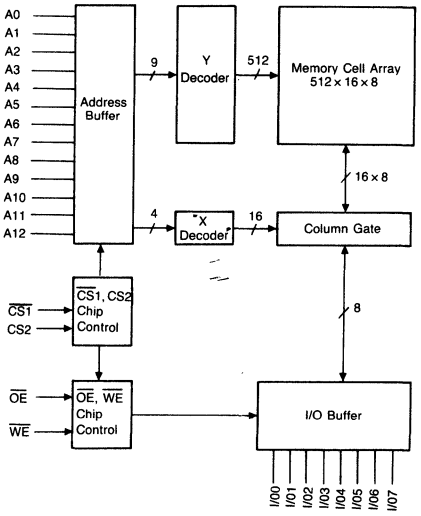
Pin	Function
A0 ~ A12	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$, CS2	Chip Select
$\overline{OE}$	Output Enable
I/O0 ~ I/O7	Data Inputs/Outputs
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

Pin Configuration



(Top View)

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0~70	°C
T_{STG}	Storage Temperature	-65~150	°C
T_{SOL}	Soldering Temperature and Time	260, 10 (at lead)	°C, S
V_{CC}	Supply Voltage	-0.5~7.0	V
V_{IN}	Input Voltage	-0.5~7.0	V
P_D	Power Dissipation	1.0	W

Recommended Operating Conditions (T_A=0~70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5	—	0.8	V

Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	A1 to A12	DATA I/O	MODE
H	X	—	—	—	Hi-Z	Unselected
—	L	—	—	—	Hi-Z	Unselected
L	H	X	L	Stable	Input Data	Write
L	H	L	H	Stable	Output Data	Read
L	H	H	H	Stable	Hi-Z	Output disable

Note: X means don't care. — means "H", "L" or "Hi-Z"

DC Electrical Characteristics (V_{CC}=5V±10%, T_A=0~70°C)

Symbol	Parameter	Conditions		GM76C88AL-15			Unit
				Min	Typ*1	Max	
V_{OH}	High Level Output Voltage	I_{OH}=-1.0mA		2.4	V_{CC}-0.1	—	V
V_{OL}	Low-Level Output Voltage	I_{OL}=4.0mA		—	0.2	0.4	V
I_{CC1}	Operating Supply Current	V_I=V_{IL}, V_{IH}	t_{RC}=1μs	—	6	10	mA
		$I_{I/O}$=0mA	t_{RC}=Min	—	25	40	
I_{CC2}		V_I=0.2V/V_{CC}-0.2V	t_{RC}=1μs	—	3	5	mA
		$I_{I/O}$=0mA	t_{RC}=Min	—	20	35	
I_{CCS1}	Standby Supply Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL}		—	1.5	3.0	mA
I_{CCS2}		$\overline{CS1}$=CS2≥V_{CC}-0.2V or CS2≤0.2V		—	2	100	μA
$I_{I(L)}$	Input Leakage Current	V_I=0 to V_{CC}		-1	—	1	μA
$I_{IO(L)}$	Output Leakage Current	$\overline{CS1}$=V_{IH} or CS2=V_{IL} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH} $V_{I/O}$=0 to V_{CC}		-1	—	1	μA

*1 Typical values are for T_A=25°C and V_{CC}=5.0V

AC Operating Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Read Cycle

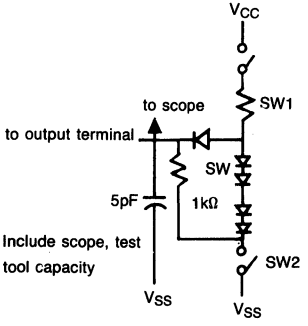
Symbol	Parameter	Conditions	GM76C88AL-15		Unit
			Min	Max	
t_{RC}	Read Cycle Time	*1	150	—	ns
t_{AA}	Address Access Time		—	150	ns
t_{ACS1}	Chip Select 1 Access Time		—	150	ns
t_{ACS2}	Chip Select 2 Access Time		—	150	ns
t_{OE}	Output enable access time		—	70	ns
t_{CLZ1}	Chip Select 1 Output Setup Time	*2	10	—	ns
t_{CHZ1}	Chip Select 1 Output Floating		—	70	ns
t_{CLZ2}	Chip Select 2 Output Setup Time		10	—	ns
t_{CHZ2}	Chip Select 2 Output Floating		—	70	ns
t_{OLZ}	Output Enable Output Setup Time		5	—	ns
t_{OHZ}	Output Enable Output Floating Time		—	60	ns
t_{OH}	Output Hold Time	*1	30	—	ns

Write Cycle

Symbol	Parameter	Conditions	GM76C88AL-15		Unit
			Min	Max	
t_{WC}	Write Cycle Time	*1	150	—	ns
t_{CW1}	Chip Select Time 1		120	—	ns
t_{CW2}	Chip Select Time 2		120	—	ns
t_{AW}	Address Enable Time		120	—	ns
t_{AS}	Address Setup Time		0	—	ns
t_{WP}	Write Pulse Width		100	—	ns
t_{WR}	Address Hold Time		0	—	ns
t_{DW}	Input Data Setup Time		60	—	ns
t_{DH}	Input data hold time	*3	0	—	ns
t_{WHZ}	R/W Output Floating		—	70	ns
t_{OW}	R/W Output Setup Time		10	—	ns

*1 Test Conditions
1. Input pulse level: 0.8V to 2.2V
2. tr = tf = 10ns
3. Input and output timing reference levels 1.5V
4. Output load $1_{TTL}+C_L$ = 100pF

*2 Test Conditions
1. Input pulse level: 0.8V to 2.2V
2. tr = tf = 10ns
3. Test circuit

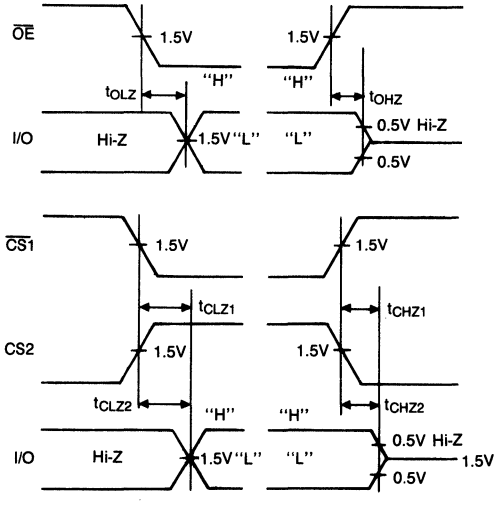


Test: t_{CHZ1}, t_{CHZ2}, t_{OHZ} Both SW1 and SW2 are close

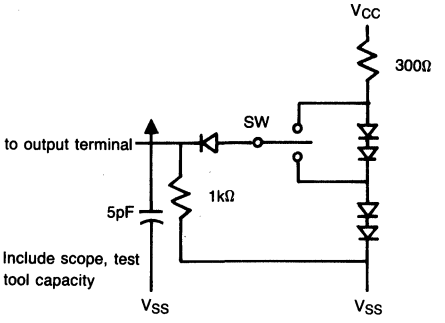
Test: t_{CLZ1}, t_{CLZ2}, t_{OLZ} "Hi-Z" to "H" SW1 is open, SW2 is close

Test: t_{CLZ1}, t_{CLZ2}, t_{OLZ} "Hi-Z" to "L" SW1 is close, SW2 is open

Output turn-on turn-off time



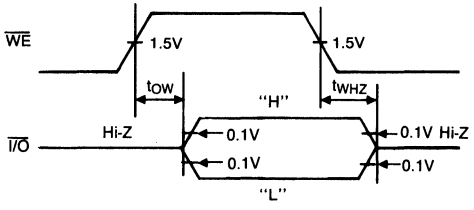
*3 Test Conditions
1. Input pulse level: 0.8V to 2.2V
2. tr = tf = 10ns
3. Test circuit



Test: t_{OW}, t_{WHZ} "Hi-Z" to "H" and "H" to "Hi-Z" SW is V_{DD} side

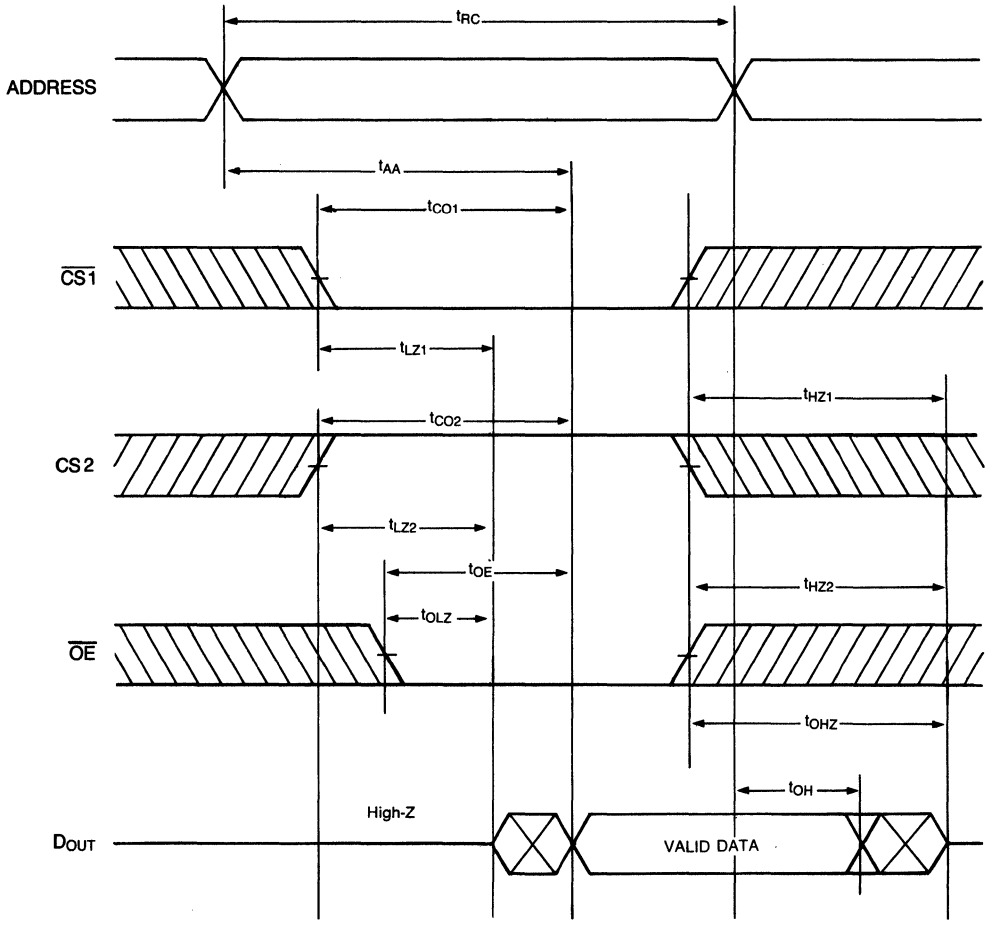
Test: t_{OW}, t_{WHZ} "Hi-Z" to "L" and "L" to "Hi-Z" SW is V_{SS} side

Output turn-on turn-off time



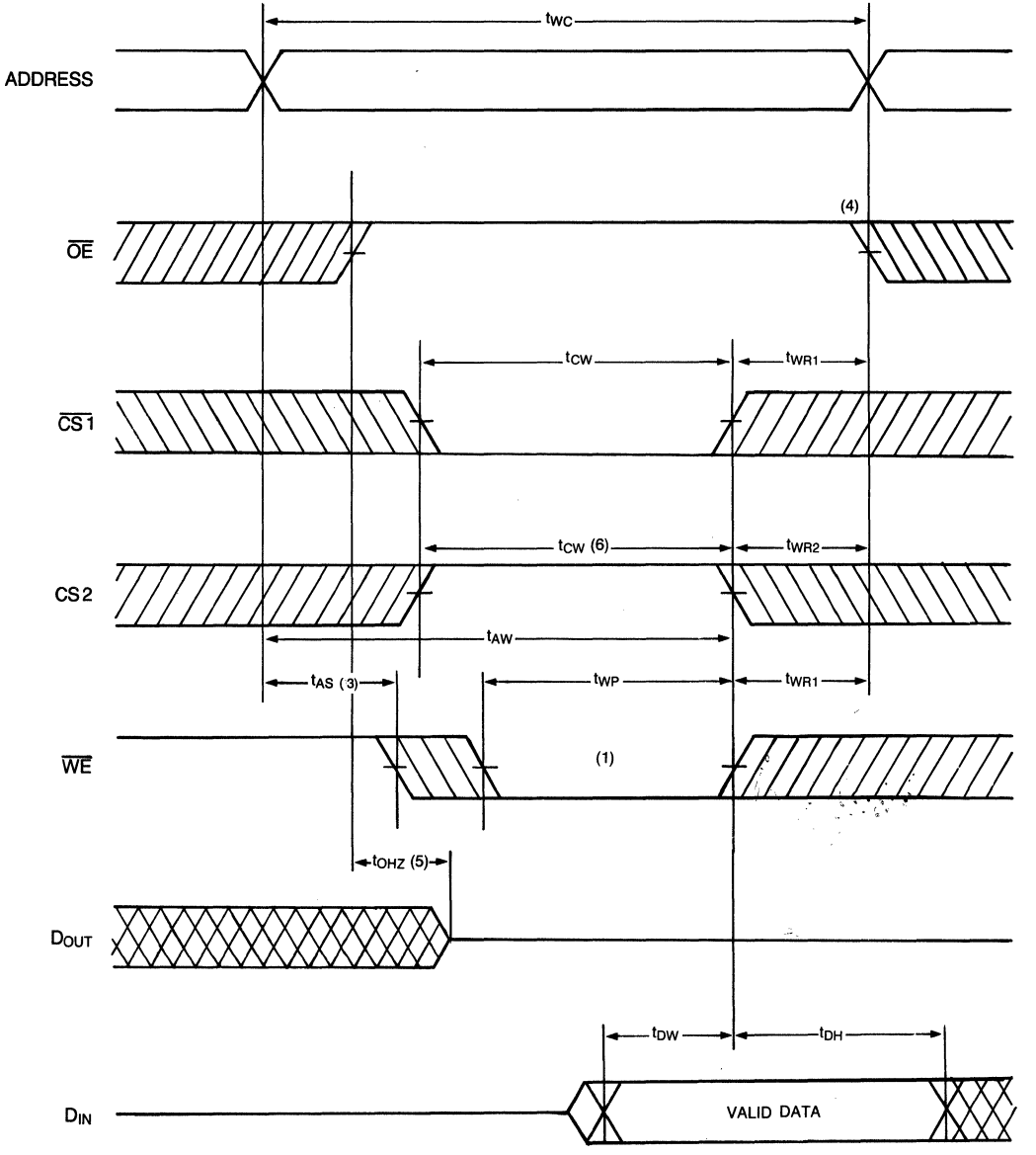
TIMING WAVEFORMS

READ CYCLE

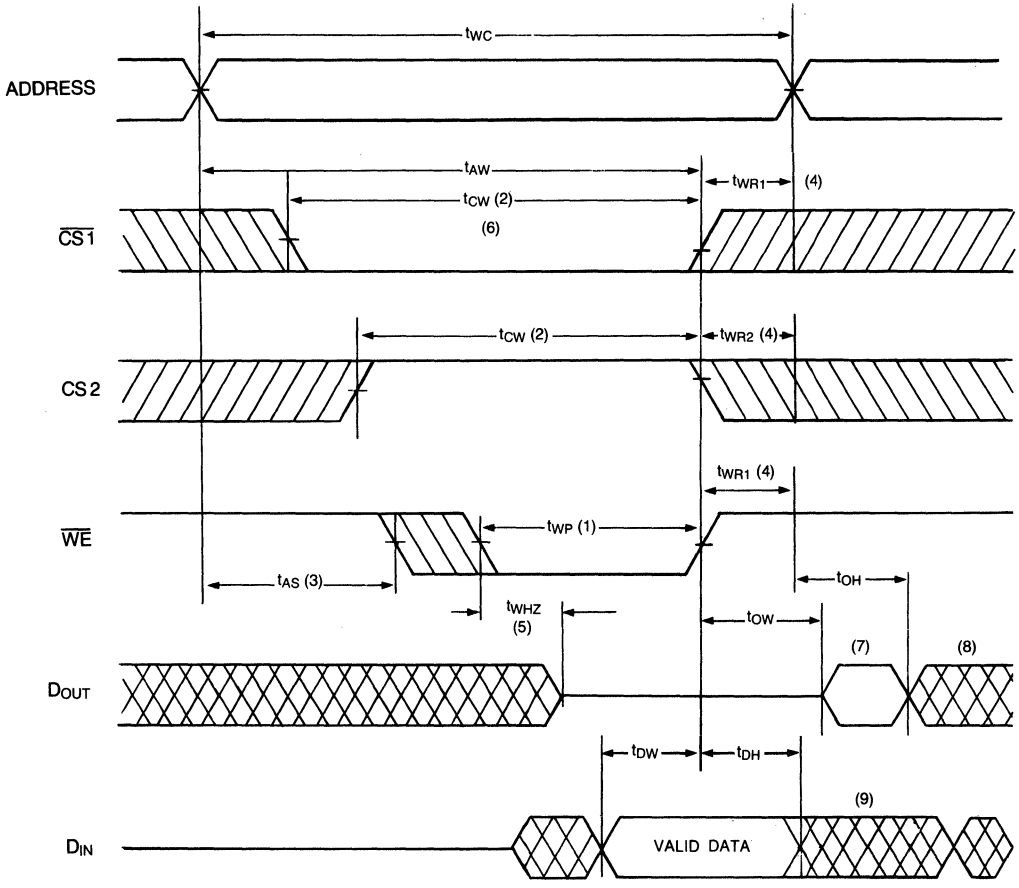


NOTE: 1) $\overline{WE}$ is high for Read Cycle

WRITE CYCLE (1) ($\overline{OE}$ clock)



WRITE CYCLE (2) ($\overline{OE}$ Low Fix)



NOTES :

1. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2 and a low $\overline{WE}$, A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high. CS2 going low and $\overline{WE}$ going high t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at $\overline{CS1}$ or $\overline{WE}$ going high t_{WR2} applies in case a write ends at CS2 going low.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If $\overline{CS1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low , the outputs remain in high impedance state.
7. D_{OUT} is the same phase of the latest written data in this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

Capacitance: (f=1MHz T_A=25°C)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_I=0V	—	6	pF
C_{OUT}	Output Capacitance	V_O=0V	—	8	

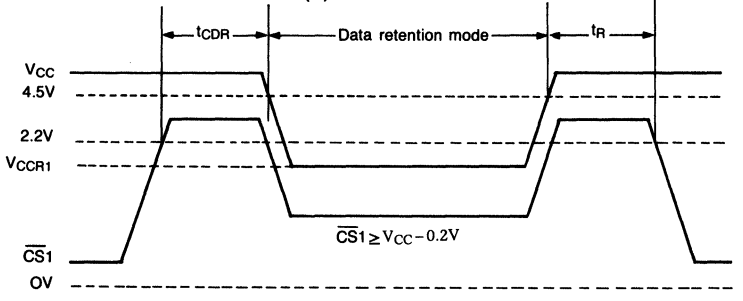
Note: This parameter is sampled and not 100% tested.

Data Retention Characteristics (T_A=0~70°C)

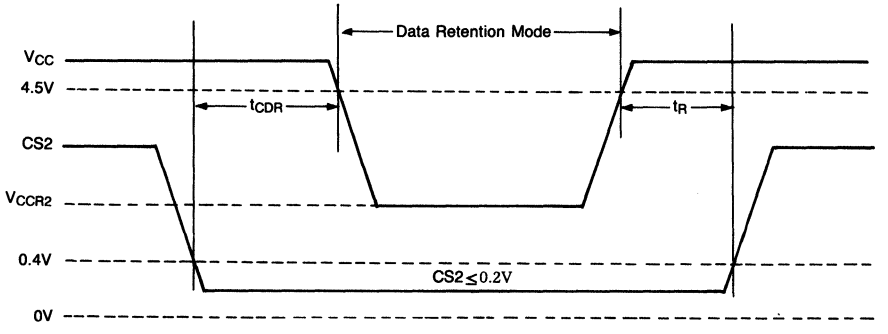
Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
V_{CCR}	Data Retention Supply Voltage	V_{CCR1}	$\overline{CS1} \geq V_{CC}$-0.2V, CS2$\geq V_{CC}$-0.2V or CS2$\leq$0.2V	2.0	—	—	V
		V_{CCR2}	CS2$\leq$0.2V	2.0	—	—	V
I_{CCR}	Data Retention Current	I_{CCR1}	V_{CC}=3.0V, $\overline{CS1} \geq V_{CC}$-0.2V CS2$\geq V_{CC}$-0.2V or CS2$\leq$0.2V	—	1	50*	μA
		I_{CCR2}	V_{CC}=3.0V, CS2$\leq$0.2V	—	1	50*	μA
t_{CDR}	Chip Select to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
t_R	Operation Recovery Time	t_R		t_{RC}**	—	—	ns

*V_{IL} min=−0.3V, 3μA max at T_A=0~40°C
**t_{RC}=Read Cycle Time

•Low V_{CC} Data Retention Mode: (1) $\overline{CS1}$ Controlled



•Low V_{CC} Data Retention Mode: (2) CS2 Controlled

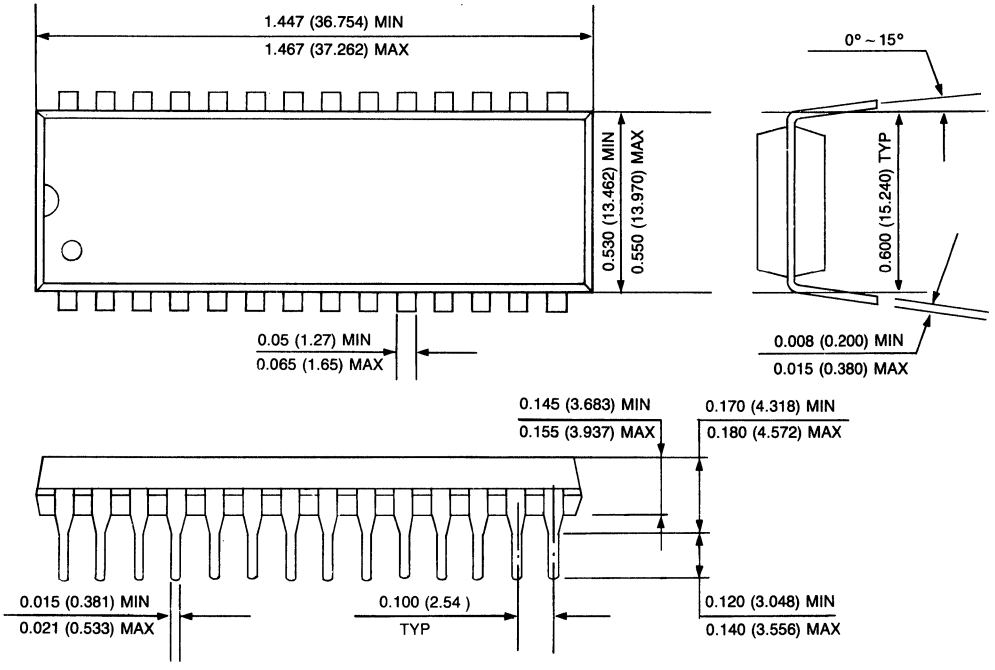


Note: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and D_{IN} buffer. If CS2 controls data retention mode, V_{IN} for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either CS2$\geq V_{CC}$-0.2V or CS2$\leq$0.2V. The other input levels (Address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

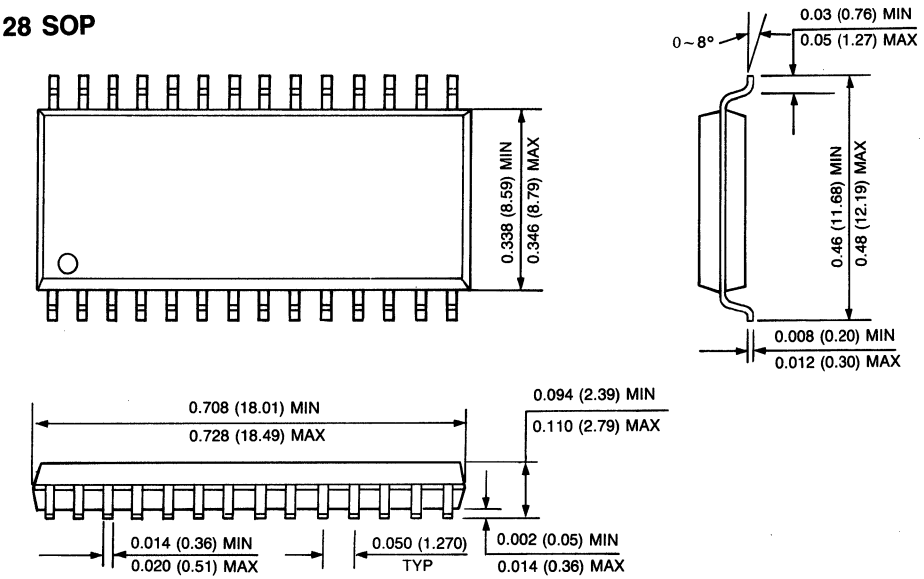
Package Dimensions

28 DIP

Unit: inches (mm)



28 SOP



GM76C256/L/LL

32,768 WORDS × 8 BIT
CMOS STATIC RAM

Description

The GM76C256/L/LL is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 70mA (max) at minimum cycle time of 85ns.

When $\overline{CS}$ is a logical high, the device is placed in low power standby mode in which standby current is 2mA (max).

The GM76C256/L/LL has two control inputs. Chip select ($\overline{CS}$) allows for device selection and data retention control, and output enable ($\overline{OE}$) provides fast memory access.

Thus the GM76C256/L/LL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The GM76C256/L/LL is offered in 28 pin DIP (600 mil) and SOP (330mil).

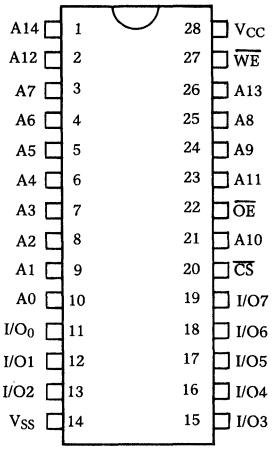
Features

- High Speed: Fast Access and Cycle Time 85/100 Max.
- Low Power Standby and Low Power Operation;
  Standby: 0.55mW Max. (Low Power Version)
  Standby: 0.17mW Max. (Low Low Power Version)
  Operation: 385mW Max.
- Completely Static RAM: No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Capability of Battery Back up Operation
- Standard 28 DIP and SOP

Pin Description

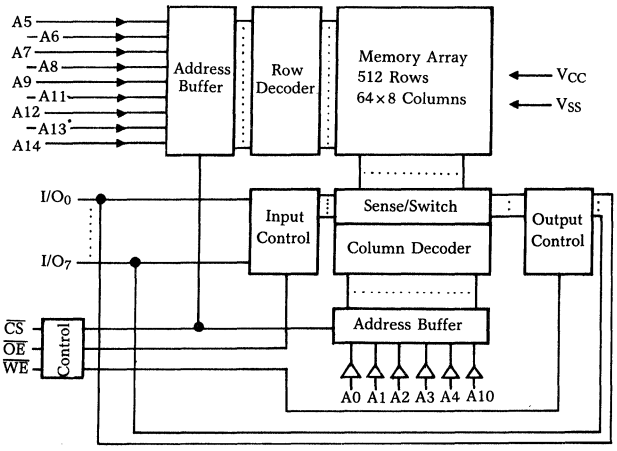
Pin	Function
A0~A14	Address Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS}$	Chip Select Input
I/O0~I/O7	Data Input/Output
V_{CC}	Power Supply +5V
V_{SS}	Ground

Pin Configuration



(Top View)

Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0~70	°C
T_{STG}	Storage Temperature	−65~150	°C
T_{SOL}	Soldering Temperature and Time	260, 10 (at lead)	°C, S
V_{CC}	Supply Voltage	−0.3~7.0	V
V_{IN}	Input Voltage	−0.3*~7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5~V_{CC}+0.5	V
P_D	Power Dissipation	1.0	W

*: −3.0V at pulse width 50ns Max.

Recommended Operating Conditions (T_A=0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{DR}	Data Retention Supply Voltage	2.0	—	5.5	V

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Outputs	Mode
H	X	X	High-Z	Deselect Power Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High-Z	Deselect

Note: X means don't care.

DC Electrical Characteristics: (V_{CC}=5V±10%, T_A=0~70°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH}=−1.0mA	2.4	—	—	V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA	—	—	0.4	V
$I_{I(L)}$	Input Leakage Current	$V_{SS} \le V_{IN} \le V_{CC}$	−2	−	+2	μA
$I_{O(L)}$	Output Leakage Current	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} or $\overline{OE}$=V_{IH}, $V_{SS} \le V_{OUT} \le V_{CC}$	−2	—	+2	μA
I_{CCS1}	Stand-by Power Supply Current	$\overline{CS}$=V_{IH}	—	—	2	mA
I_{CCS2}		$\overline{CS} \ge V_{CC}$−0.2V GM76C256 GM76C256L GM76C256LL	 — —	 2*	 1 100 30	 mA μA μA
I_{CC}	Operating Supply Current	$\overline{CS}$=V_{IL}, $V_{I/O}$=0mA	—	—	45	mA
I_{CC1}	Average Operating Power Supply Current	Min. Cycle, duty=100% $I_{I/O}$=0mA	—	—	70	mA

*TYP Values are measured at 25°C, V_{CC}=5V

AC Operating Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Read Cycle

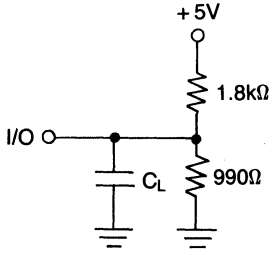
Symbol	Parameter	Conditions	GM76C256L-85		GM76C256L-10		Unit
			Min	Max	Min	Max	
t_{RC}	Read Cycle Time	*1	85	—	100	—	ns
t_{AA}	Address Access Time		—	85	—	100	ns
t_{ACS}	Chip Select Access Time		—	85	—	100	ns
t_{OE}	Output Enable to Output Valid		—	45	—	50	ns
t_{OH}	Output Hold from Address Change		5	—	10	—	ns
t_{CLZ}	Chip Selection to Output in Low-Z	*2	10	—	10	—	ns
t_{OLZ}	Output Enable to Output in Low-Z		5	—	5	—	ns
t_{CHZ}	Chip Deselection to Output in High-Z		0	30	0	35	ns
t_{OHZ}	Output Disable to Output in High-Z		0	30	0	35	ns

WriteCycle

Symbol	Parameter	Conditions	GM76C256L-85		GM76C256L-10		Unit
			Min	Max	Min	Max	
t_{WC}	Write Cycle Time	*1	85	—	100	—	ns
t_{CW}	Chip Selection to End of Write		75	—	80	—	ns
t_{AW}	Address Valid to End of Write		75	—	80	—	ns
t_{AS}	Address Setup Time		0	—	0	—	ns
t_{WP}	Write Pulse Width		60	—	60	—	ns
t_{WR}	Write Recovery Time		5	—	5	—	ns
t_{DW}	Data to Write Time Overlap		40	—	40	—	ns
t_{DH}	Data Hold from Write Time		0	—	0	—	ns
t_{WHZ}	Write to Output in High-Z	*2	0	30	0	35	ns
t_{OW}	Output Active from End of Write		5	—	5	—	ns

*1 Test Conditions

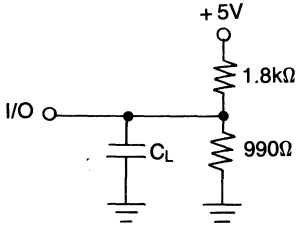
1. Input pulse level: 0.6V to 2.4V
2. tr = tf = 5ns
3. Input and output timing reference levels: 1.5V
4. Output load C_L = 100pF



C_L = 100pF (Includes Jig Capacitance)

*2 Test Conditions

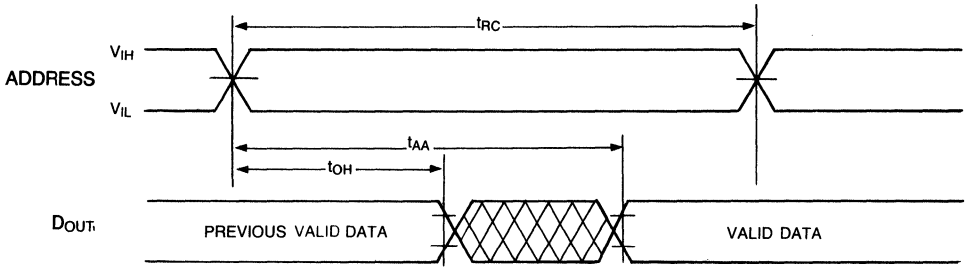
1. Input pulse level: 0.6V to 2.4V
2. tr = tf = 5ns
3. Input timing reference levels: 1.5V
4. Output timing reference levels:
   ±200mV (the level displaced from stable output voltage level)
5. Output load C_L = 5pF



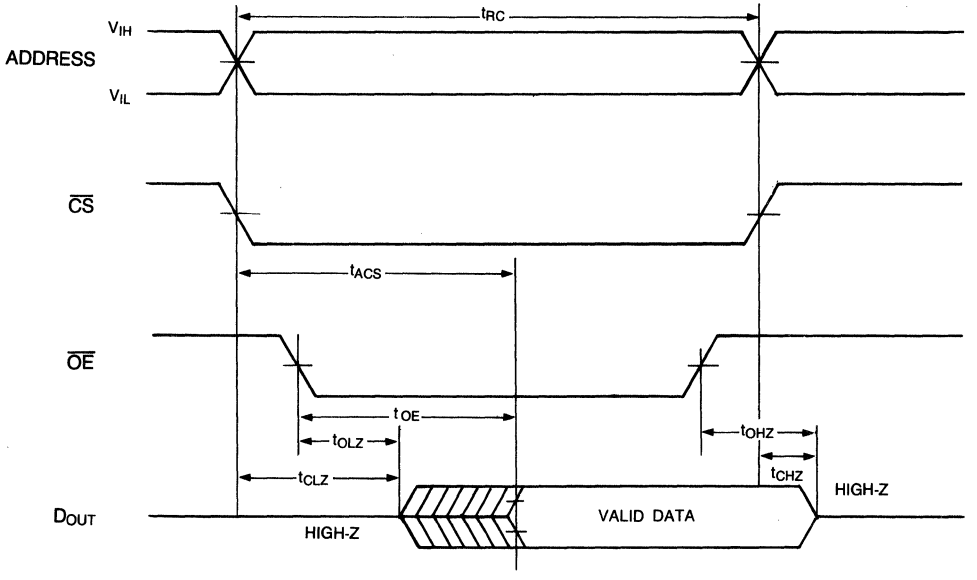
C_L = 5pF (Includes Jig Capacitance)

TIMING WAVEFORMS

Read Cycle 1 (Notes 1, 3)

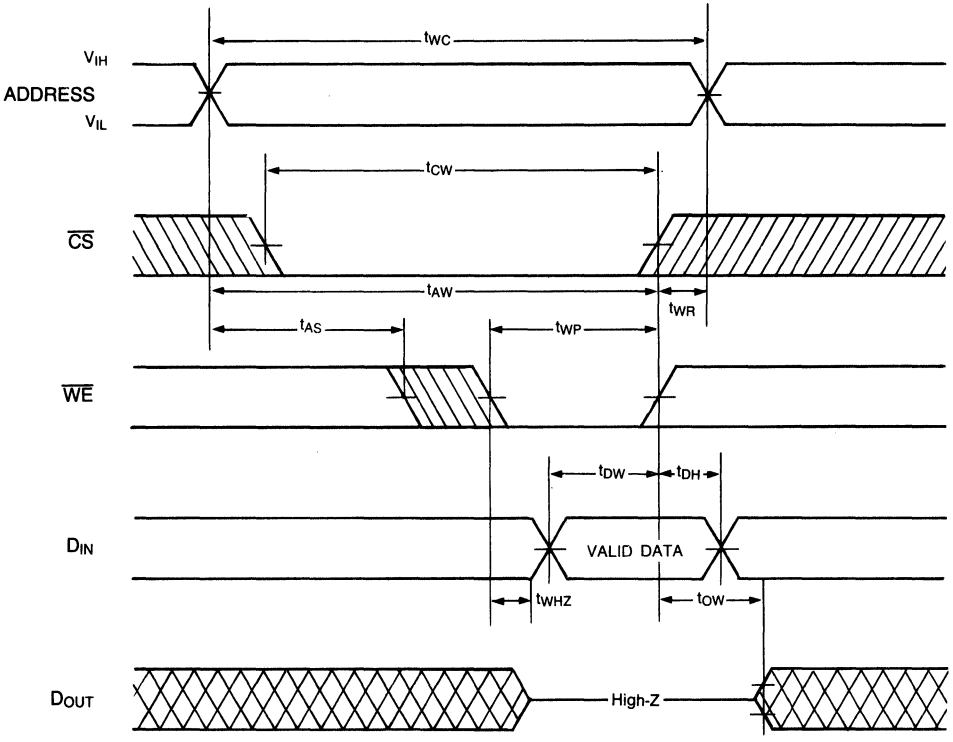


Read Cycle 2 (Notes 2, 3)

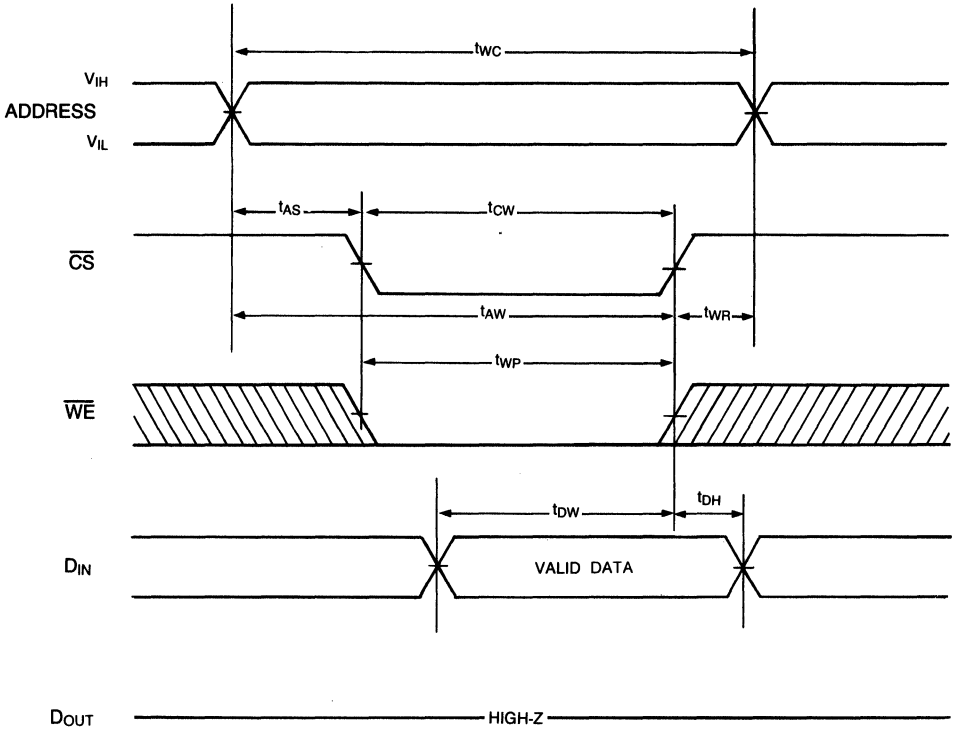


Notes:
1. Device is continuously selected. $\overline{OE}$, $\overline{CS}$ = V_{IL}
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{WE}$ is high for read cycle.

Write Cycle 1 ($\overline{WE}$ Controlled) (Note 1, 2)



Write Cycle 2 ($\overline{CS}$ Controlled) (Note 1, 2, 3)



Notes:
1. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. Data I/O is high impedance if $\overline{OE} = V_{IH}$
3. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1MHz $V_{CC} = 5.0V$	—	6	pF
C_{OUT}	Output Capacitance		—	8	

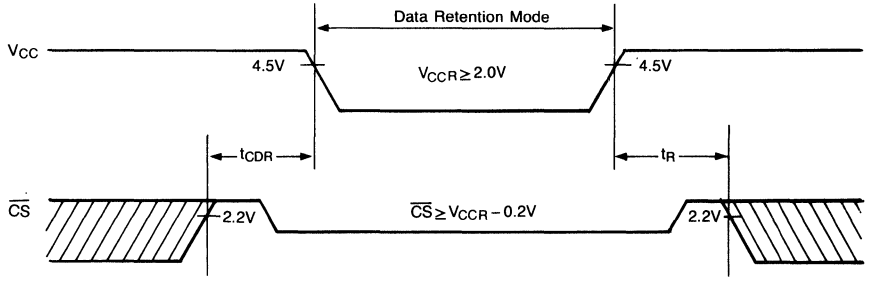
Note: Tested on a sample basis

Data Retention Characteristics: ($T_A = 0 \sim 70°C$)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CCR}	Date Retention Supply Voltage	$\overline{CS} \geq V_{CCR} - 0.2V$	2.0	—	5.5	V
I_{CCR}	Data Retention Current	$V_{CC} = 3.0V$, $\overline{CS} \geq 2.8V$	—	—	50	μA
t_{CDR}	Chip Select Data Hold Time	Refer to the figure below	0	—	—	ns
t_R	Operation Recovery Time		t_{RC}*	—	—	ns

Note*: Read Cycle Time

Data Retention Timing

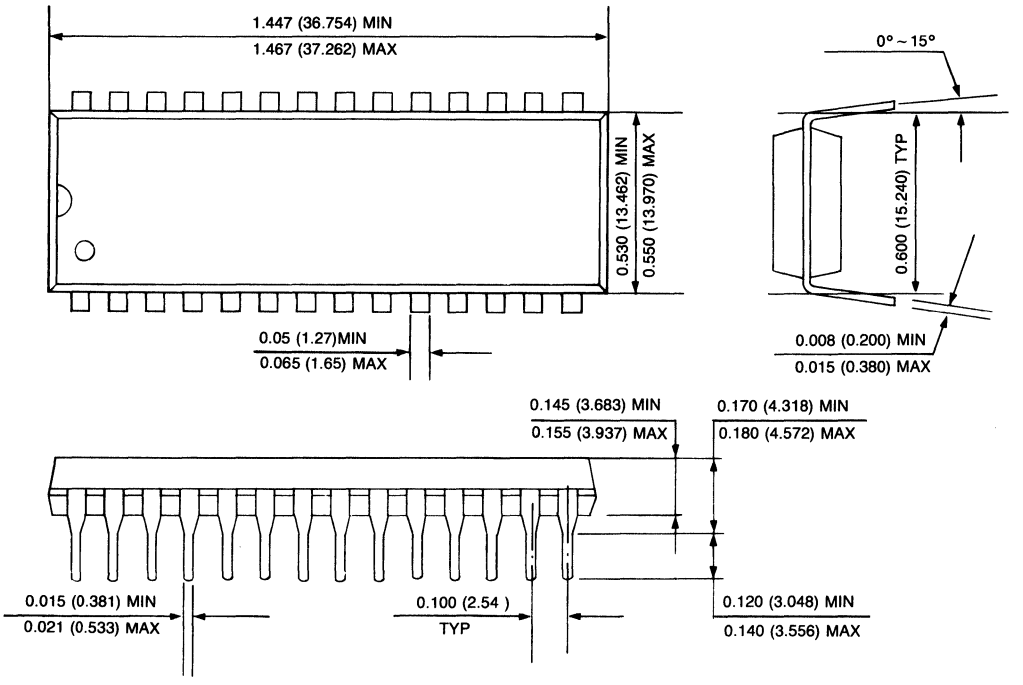


Note: When retaining data in standby mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

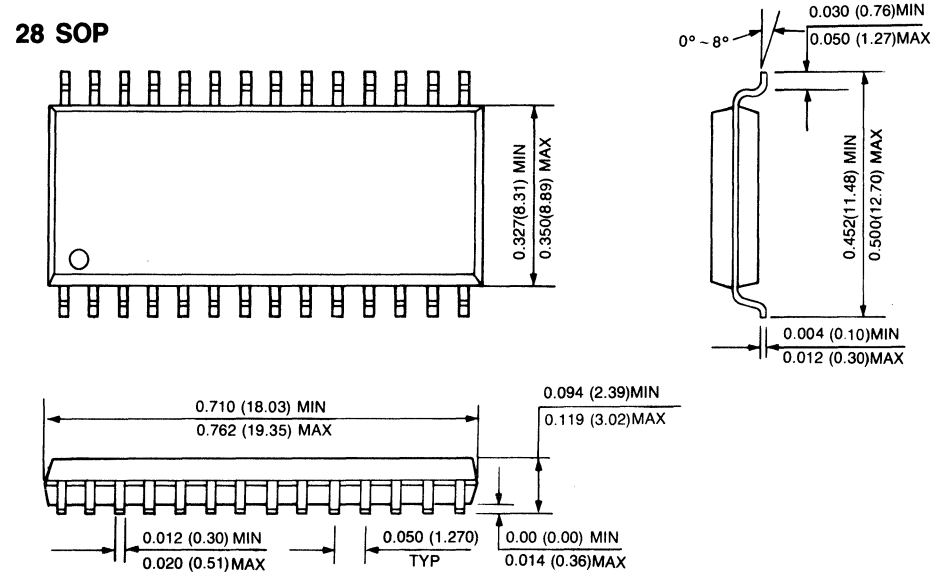
Package Dimensions

Unit: inches (mm)

28 DIP



28 SOP



GM76C256AL/ALL

32,768 WORDS × 8 BIT
CMOS STATIC RAM

Description

The GM76C256AL/ALL is a 262,144 bit static random access memory organized as 32,768 words by 8 bits using CMOS technology, and operated from a single 5V supply. Advanced circuit techniques provide both high speed and low power features with an operating current of 50mA (max) at minimum cycle time of 70ns.

When $\overline{CS}$ is a logical high, the device is placed in low power standby mode in which standby current is 1mA (max).

The GM76C256AL/ALL has two control inputs. Chip select ($\overline{CS}$) allows for device selection and data retention control, and output enable ($\overline{OE}$) provides fast memory access.

Thus the GM76C256AL/ALL is suitable for use in various microprocessor application systems where high speed, low power, and battery back up are required. The GM76C256AL/ALL is offered in 28 pin DIP (600 mil) and SOP (330mil).

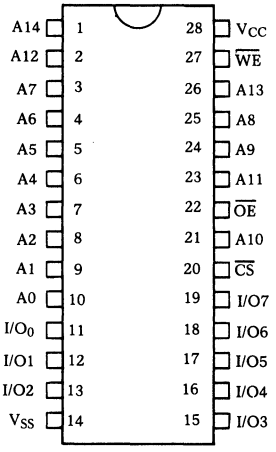
Features

- High Speed: Fast Access and Cycle Time 70/85/100ns Max.
- Low Power Standby and Low Power Operation; Stand by: 0.55mW Max. (Low Power Version) Stand by: 0.17mW Max. (Low Low Power Version)
  Operation: 275mW Max.
- Completely Static RAM: No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Capability of Battery Back up Operation
- Standard 28 DIP and SOP

Pin Description

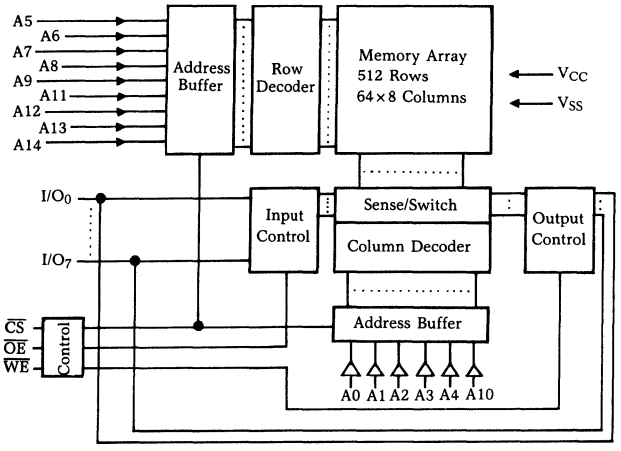
Pin	Function
A0 ~ A14	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{CS}$	Chip Select Input
I/O0 ~ I/O7	Data Input/Output
V_{CC}	Power Supply +5V
V_{SS}	Ground

Pin Configuration



(Top View)

Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature	−65 ~ 150	°C
T_{SOL}	Soldering Temperature and Time	260, 10 (at lead)	°C, S
V_{CC}	Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5 ~ V_{CC} + 0.5	V
P_D	Power Dissipation	1.0	W

*: −3.0V at pulse width 50ns Max.

Recommended Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{DR}	Data Retention Supply Voltage	2.0	—	5.5	V

Truth Table

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode
H	X	X	High Z	Deselect Power Down
L	H	L	Data Out	Read
L	L	X	Data In	Write
L	H	H	High Z	Deselect

Note: X means don't care

DC Electrical Characteristics: (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −1.0mA	2.2	—	—	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	—	—	0.4	V
$I_{I(L)}$	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$	−1	−	1	μA
$I_{O(L)}$	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, $V_{SS} \leq V_{OUT} \leq V_{CC}$	−1	—	1	μA
I_{CCS1}	Stand-by Power Supply Current	$\overline{CS}$ = V_{IH}	—	—	1	mA
I_{CCS2}		$\overline{CS} \geq V_{CC}$ − 0.2V GM76C256AL GM76C256ALL	— —	2* 1*	100 20	μA μA
I_{CC}	Operating Supply Current	$\overline{CS}$ = V_{IL}, $V_{I/O}$ = 0mA	—	7	15	mA
I_{CC1}	Average Operating Power Supply Current	Min. Cycle, duty = 100% $I_{I/O}$ = 0mA	—	—	50	mA

*TYP. Values are measured at 25°C, V_{CC} = 5V

AC Operating Characteristics (V_{CC}=5V±10%, T_A = 0 ~ 70°C)

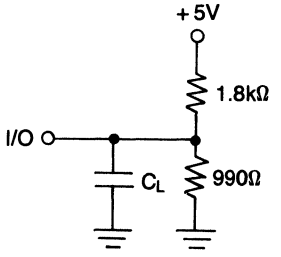
Read Cycle

Symbol	Parameter	Conditions	GM76C256AL-70		GM76C256AL-85		GM76C256AL-10		Unit
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	*1	70	—	85	—	100	—	ns
t_{AA}	Address Access Time		—	70	—	85	—	100	ns
t_{ACS}	Chip Select Access Time		—	70	—	85	—	100	ns
t_{OE}	Output Enable to Output Valid		—	35	—	45	—	50	ns
t_{OH}	Output Hold from Address Change		5	—	5	—	10	—	ns
t_{CLZ}	Chip Selection to Output in Low-Z	*2	10	—	10	—	10	—	ns
t_{OLZ}	Output Enable to Output in Low-Z		5	—	5	—	5	—	ns
t_{CHZ}	Chip Deselection to Output in High-Z		0	30	0	30	0	35	ns
t_{OHZ}	Output Disable to Output in High-Z		0	30	0	30	0	35	ns

Write Cycle

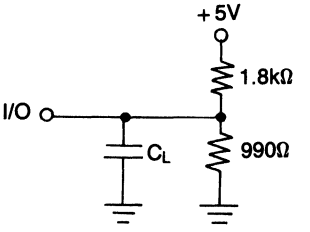
Symbol	Parameter	Conditions	GM76C256AL-70		GM76C256AL-85		GM76C256AL-10		Unit
			Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	*1	70	—	85	—	100	—	ns
t_{CW}	Chip Selection to End of Write		60	—	75	—	80	—	ns
t_{AW}	Address Valid to End of Write		60	—	75	—	80	—	ns
t_{AS}	Address Setup Time		0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width		50	—	60	—	60	—	ns
t_{WR}	Write Recovery Time		0	—	5	—	5	—	ns
t_{DW}	Data to Write Time Overlap		30	—	40	—	40	—	ns
t_{DH}	Data Hold from Write Time		0	—	0	—	0	—	ns
t_{WHZ}	Write to Output in High-Z	*2	0	25	0	30	0	35	ns
t_{OW}	Output Active from End of Write		5	—	5	—	5	—	ns

*1 Test Conditions
1. Input pulse level: 0.6V to 2.4V
2. tr = tf = 5ns
3. Input and output timing reference levels: 1.5V
4. Output load C_L = 100pF



C_L = 100pF (Includes Jig Capacitance)

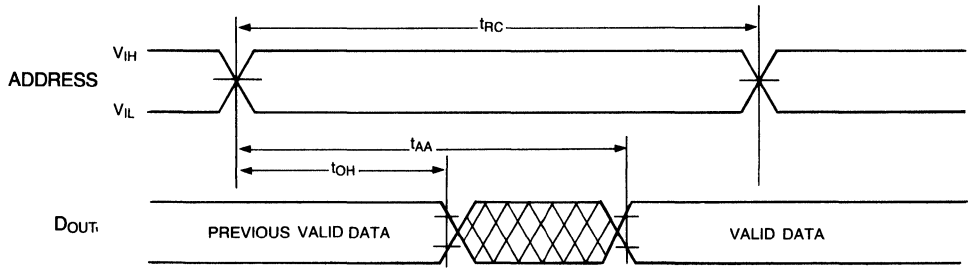
*2 Test Conditions
1. Input pulse level: 0.6V to 2.4V
2. tr = tf = 5ns
3. Input timing reference level: 0.8V to 2.2V.
4. Output timing reference levels: ±200mV (the level displace from stable output voltage level)
5. Output load C_L = 5pF



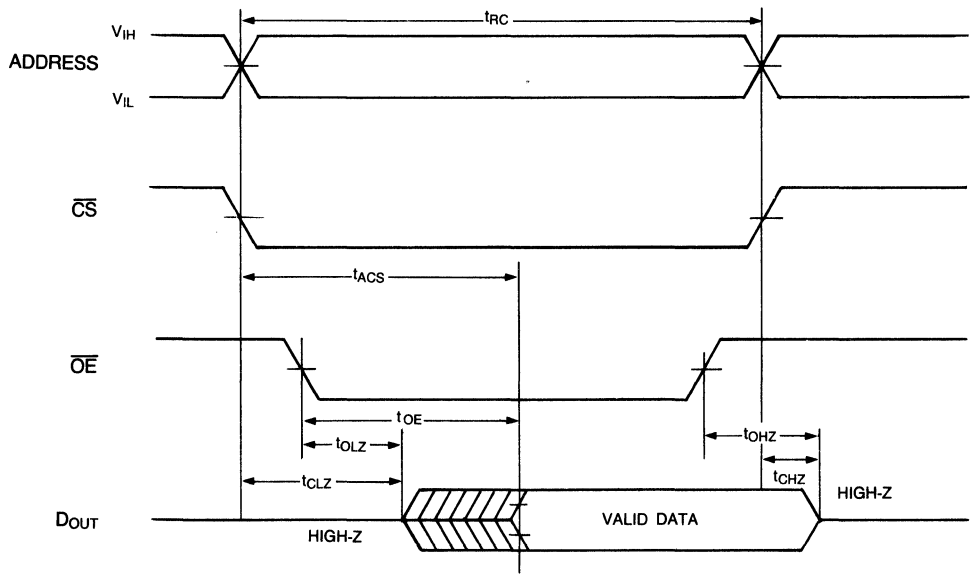
C_L = 5pF (Includes Jig Capacitance)

TIMING WAVEFORMS

Read Cycle 1 (Notes 1, 3)

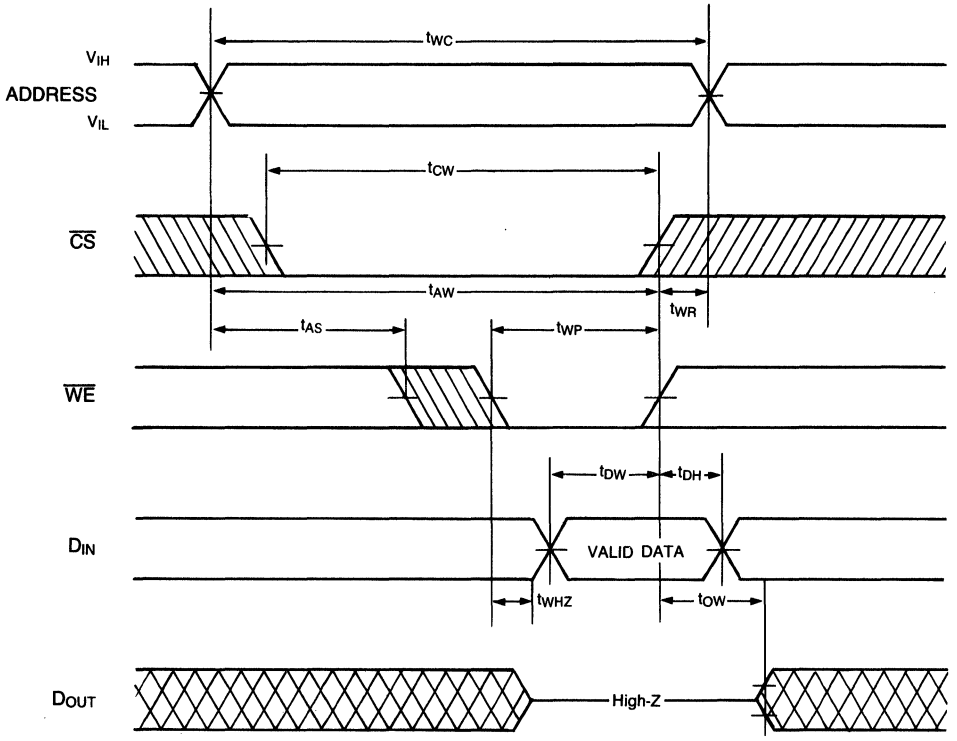


Read Cycle 2 (Notes 2, 3)

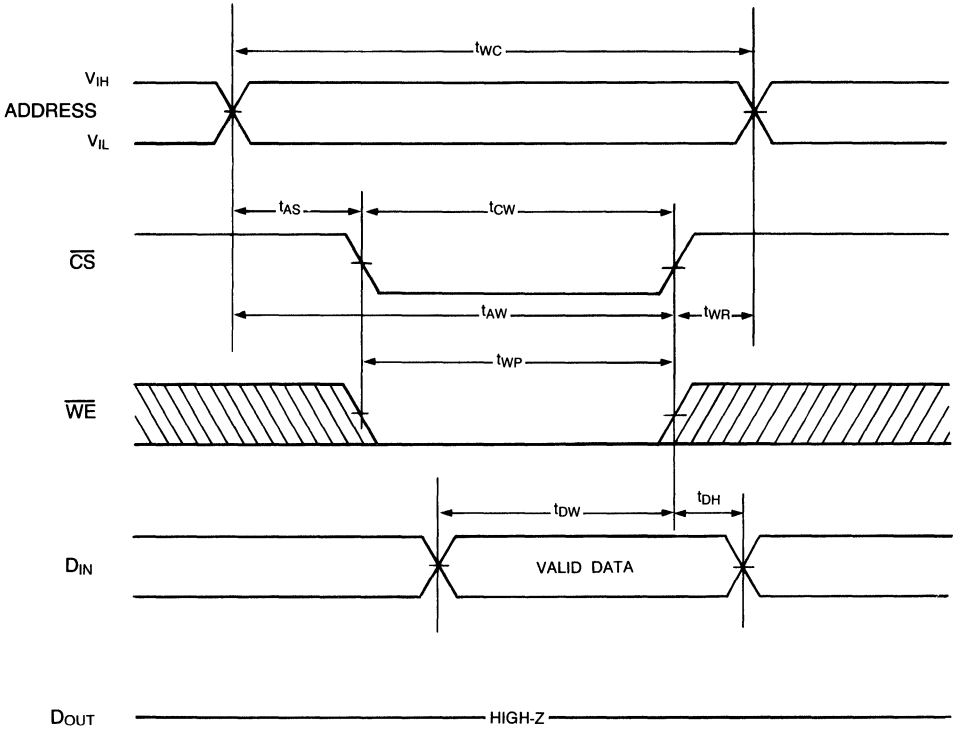


Notes:
1. Device is continuously selected. $\overline{OE}$, $\overline{CS}$ = V_{IL}
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. $\overline{WE}$ is high for read cycle.

Write Cycle 1 ($\overline{WE}$ Controlled) (Note 1, 2)



Write Cycle 2 ($\overline{CS}$ Controlled) (Note 1, 2, 3)



Notes:
1. The internal write time of the memory is defined by the overlap of $\overline{CS}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. Data I/O is high impedance if $\overline{OE} = V_{IH}$
3. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.

Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	T_A=25°C, f=1MHz V_{CC}=5.0V	—	6	pF
C_{OUT}	Output Capacitance		—	8	

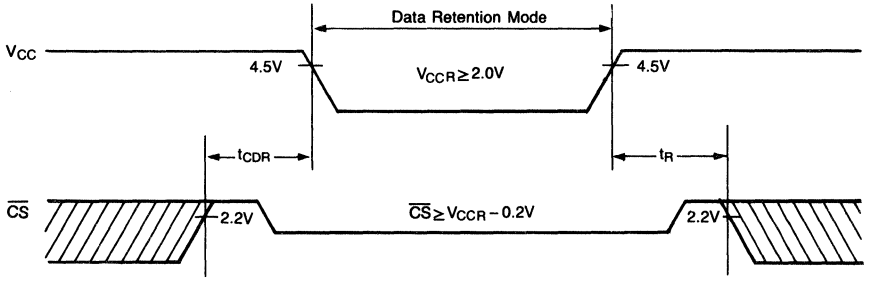
Note: Tested on a sample basis

Data Retention Characteristics: (T_A=0°~70°C)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{CCR}	Data Retention Supply Voltage	$\overline{CS} \geq V_{CC}-0.2V$		2.0	—	5.5	V
I_{CCR}	Data Retention Current	V_{CC}=3.0V $\overline{CS} \geq 2.8V$	AL	—	1**	50	μA
			ALL	—	0.5**	10	
t_{CDR}	Chip Select Data Hold Time	Refer to the figure below		0	—	—	ns
t_R	Operation Recovery Time			t_{RC}*	—	—	ns

Note* : Read Cycle Time
Note**: Typ, Values are measured at 25°C.

Data Retention Timing

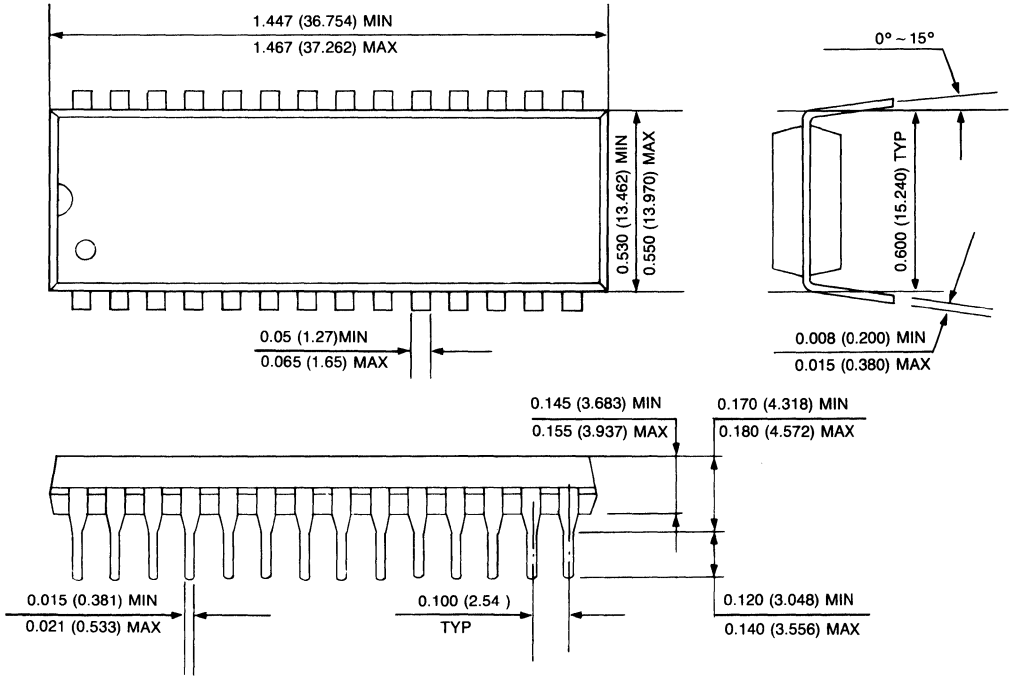


Note: When retaining data in standby mode, supply voltage can be lowered within a certain range. Read or write cycle cannot be performed while the supply voltage is low.

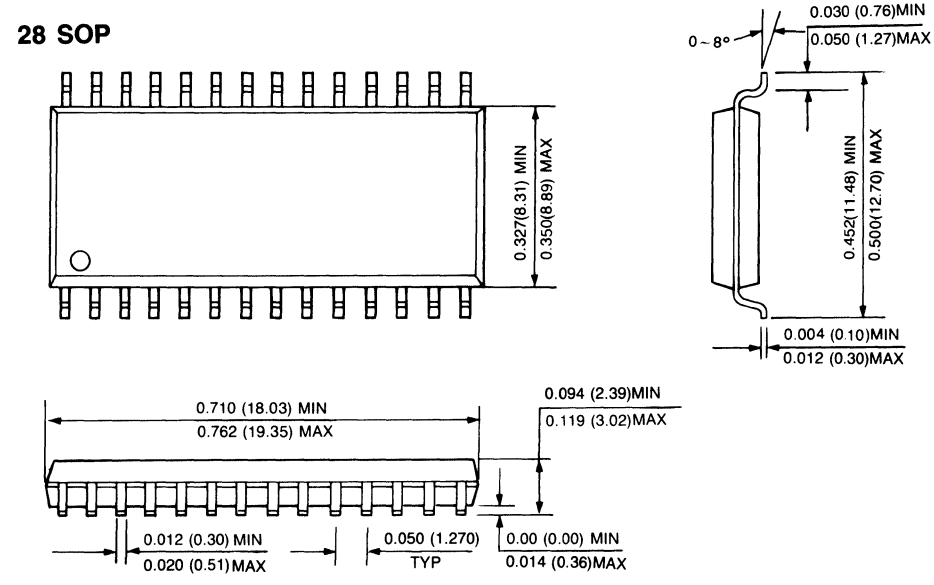
Package Dimensions

Unit: inches (mm)

28 DIP



28 SOP



GM76C8128/L/LL

131,072 WORDS×8 BIT
CMOS STATIC RAM

Description

The GM76C8128/L/LL is a 1,048,576 bits static random access memory organized as 131,072 words by 8 bits. Using a 0.8um advanced CMOS technology, it provides high speed operation with minimum cycle time of 70/85/100ns. The device is placed in a low power standby mode with $\overline{CS1}$ high or CS2 low and the output enable ($\overline{OE}$) allows fast memory access. Thus it is suitable for high speed and low power applications, especially where battery back-up is required.
The GM76C8128/L/LL is offered in a 32-pin DIP (600mil) and SOP (525 mil)

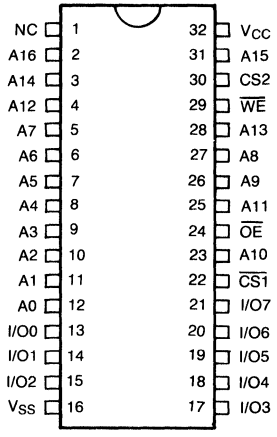
Features

- High Speed: Fast Access and Cycle Time 70/85/100ns Max.
- Low Power Standby and Low Power Operation.
  Standby: 5.5mW Max.
  Standby: 0.55mW Max. (Low Power Version)
  Standby: 0.275mW Max (Low Low Power Version)
- Operation: 385mW (Max)
- Completely Static RAM: No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Capability of Battery Back up Operation
- Single +5V Operation (±10%)
- Standard 32 DIP and SOP

Pin Description

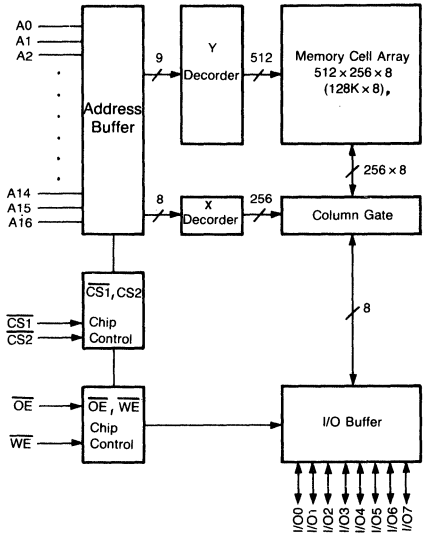
Pin	Function
A0~A16	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS1}$, CS2	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O0~I/O7	Data Inputs/Outputs
V_{CC}	Power Supply (+5V)
V_{SS}	Ground
NC	No Connection

Pin Configuration



(Top View)

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
T_A	Ambient Temperature under Bias	0 ~ 70	°C
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{SOL}	Soldering Temperature and Time	260, 10 (at lead)	°C, S
V_{CC}	Supply Voltage	−0.3 ~ 7.0	V
V_{IN}	Input Voltage	−0.3* ~ 7.0	V
$V_{I/O}$	Input and Output Voltage	−0.5 ~ V_{CC}+0.5	V
P_D	Power Dissipation	1.0	W

*: −3.0V at pulse width 50ns Max.

Recommended Operating Conditions (T_A = 0 ~ 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	−0.3	—	0.8	V
V_{DR}	Data Retention Supply Voltage	2.0	—	5.5	V

Truth Table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	A1 to A16	DATA I/O	Mode
L	H	L	H	stable	Output Data	Read
L	H	X	L	stable	Input Data	Write
L	H	H	H	stable	Hi-Z	Output Disable
H	X	X	X	—	Hi-Z	Standby
X	L	X	X	—	Hi-Z	

Note: X means don't care

DC Electrical Characteristics (V_{CC} = 5V ± 10%, T_A = 0 ~ 70°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{I(L)}$	Input Leakage Current	V_{IN} = 0 to V_{CC}	-1	—	+1	μA
$I_{O(L)}$	Output Leakage Current	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL} $\overline{OE}$ = V_{IH}, $V_{SS} \leq V_{OUT} \leq V_{CC}$	-1	—	+1	μA
I_{OH}	High Level Output Current	V_{OH} = 2.4V	-1.0	—	—	mA
I_{OL}	Low Level Output Current	V_{OL} = 0.4V	—	—	2.1	mA
I_{CC}	Operating Supply Current	$\overline{CS1}$ = V_{IL} or CS2 = V_{IH} V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0mA	—		35	mA
I_{CC1}	Average Operating Current	$\overline{CS1}$ = V_{IL} and CS2 = V_{IH} V_{IN} = V_{IH}/V_{IL} I_{OUT} = 0mA t_{cycle} = Min. cycle	—		70	mA
I_{CC2}		$\overline{CS1}$ = 0.2V, CS2 = V_{CC}-0.2V V_{IN} = V_{CC}-0.2V/0.2V I_{OUT} = 0mA t_{cycle} = 1μs	—	—	30	mA
I_{CCS1}	Standby Current	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}	—	—	3	mA
I_{CCS2}		$\overline{CS1}$ = V_{CC}-2V, CS2 = 0.2V V_{CC} = 2.0V ~ 5.5V GM76C8128 GM76C8128L GM76C8128LL	— — —	— 2* 2*	1 100 50	mA μA μA

*TYP. Values are measured at 25°C, V_{CC} = 5V

AC Operating Characteristics ($V_{CC}=5V\pm10\%$, $T_A=0\sim70°C$)

Read Cycle

Symbol	Parameter	GM76C8128/L-70		GM76C8128/L-85		GM76C8128/L-10		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	70	—	85	—	100	—	ns
t_{AA}	Address Access Time	—	70	—	85	—	100	ns
t_{ACS1}	Chip Select 1 Access Time	—	70	—	85	—	100	ns
t_{ACS2}	Chip Select 2 Access Time	—	70	—	85	—	100	ns
t_{OE}	Output Enable Access Time	—	35	—	45	—	50	ns
t_{CHZ1}	Chip Select 1 Output Setup Time	5	—	10	—	10	—	ns
t_{CHZ1}	Chip Select 1 Output Floating	—	25	—	30	—	35	ns
t_{CLZ2}	Chip Select 2 Output Setup Time	5	—	10	—	10	—	ns
t_{CHZ2}	Chip Select 2 Output Floating	—	25	—	30	—	35	ns
t_{OLZ}	Output Enable Output Setup Time	0	—	0	—	0	—	ns
t_{OHZ}	Output Enable Output Floating Time	—	25	—	30	—	35	ns
t_{OH}	Output Hold Time	10	—	10	—	10	—	ns

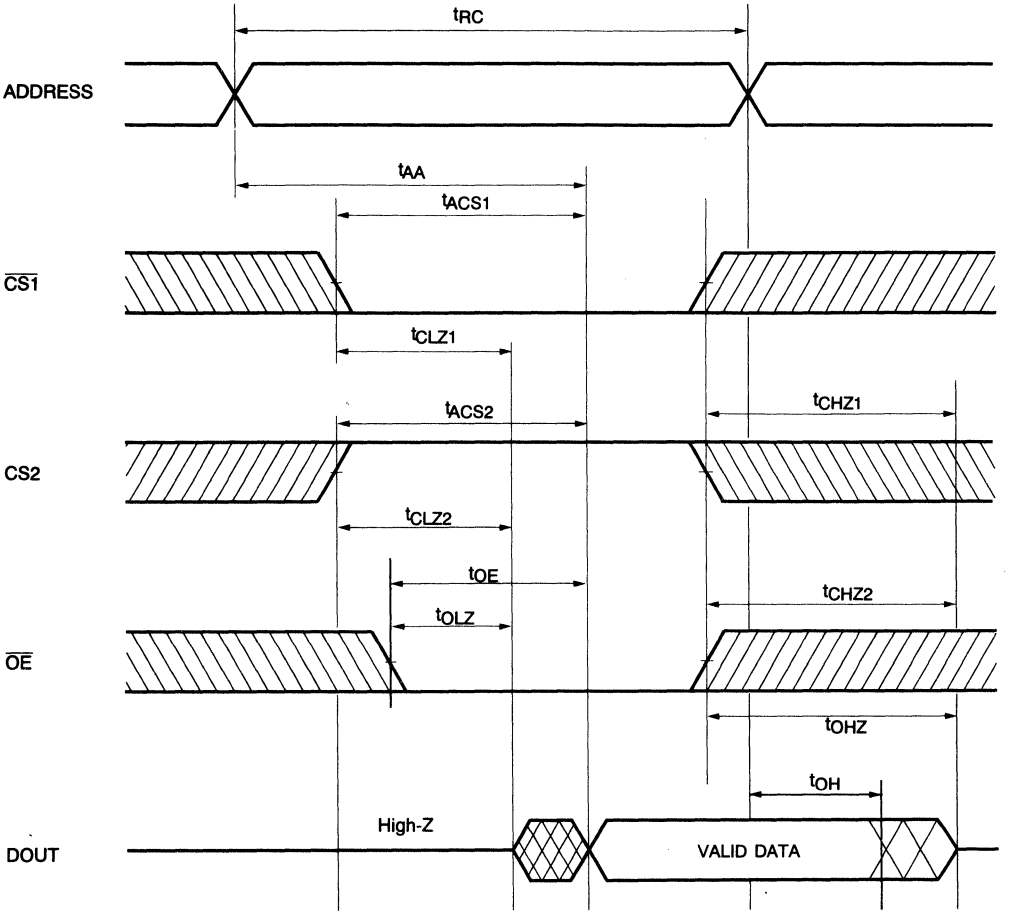
Write Cycle

Symbol	Parameter	GM76C8128/L-70		GM76C8128/L-85		GM76C8128/L-10		Unit
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	70	—	85	—	100	—	ns
t_{CW1}	Chip Select Time 1	65	—	75	—	80	—	ns
t_{CW2}	Chip Select Time 2	65	—	75	—	80	—	ns
t_{AW}	Address Enable Time	60	—	70	—	80	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	50	—	60	—	60	—	ns
t_{WR}	Address Hold Time	0	—	0	—	0	—	ns
t_{DW}	Input Data Setup Time	30	—	35	—	40	—	ns
t_{DH}	Input Data Hold Time	0	—	0	—	0	—	ns
t_{WHZ}	R/W Output Floating	—	25	—	30	—	35	ns
t_{OW}	R/W Output Setup Time	0	—	0	—	0	—	ns

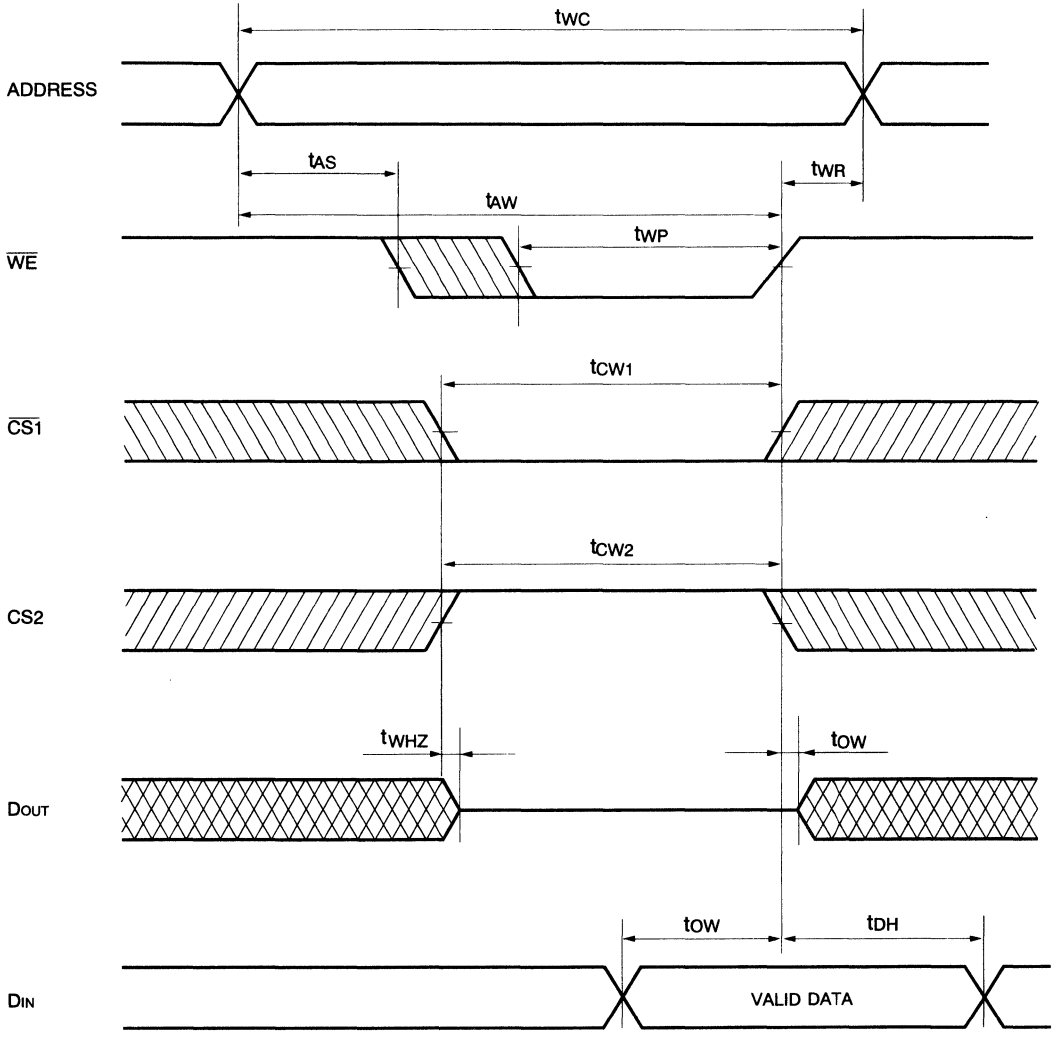
AC TEST CONDITIONS
- Output load: 100pF + 1TTL Gate
- Input pulse level: 0.6V to 2.4V
- Input and output timing reference levels 0.8V, 2.2V
- $tr=t_f=5ns$

TIMING WAVEFORMS

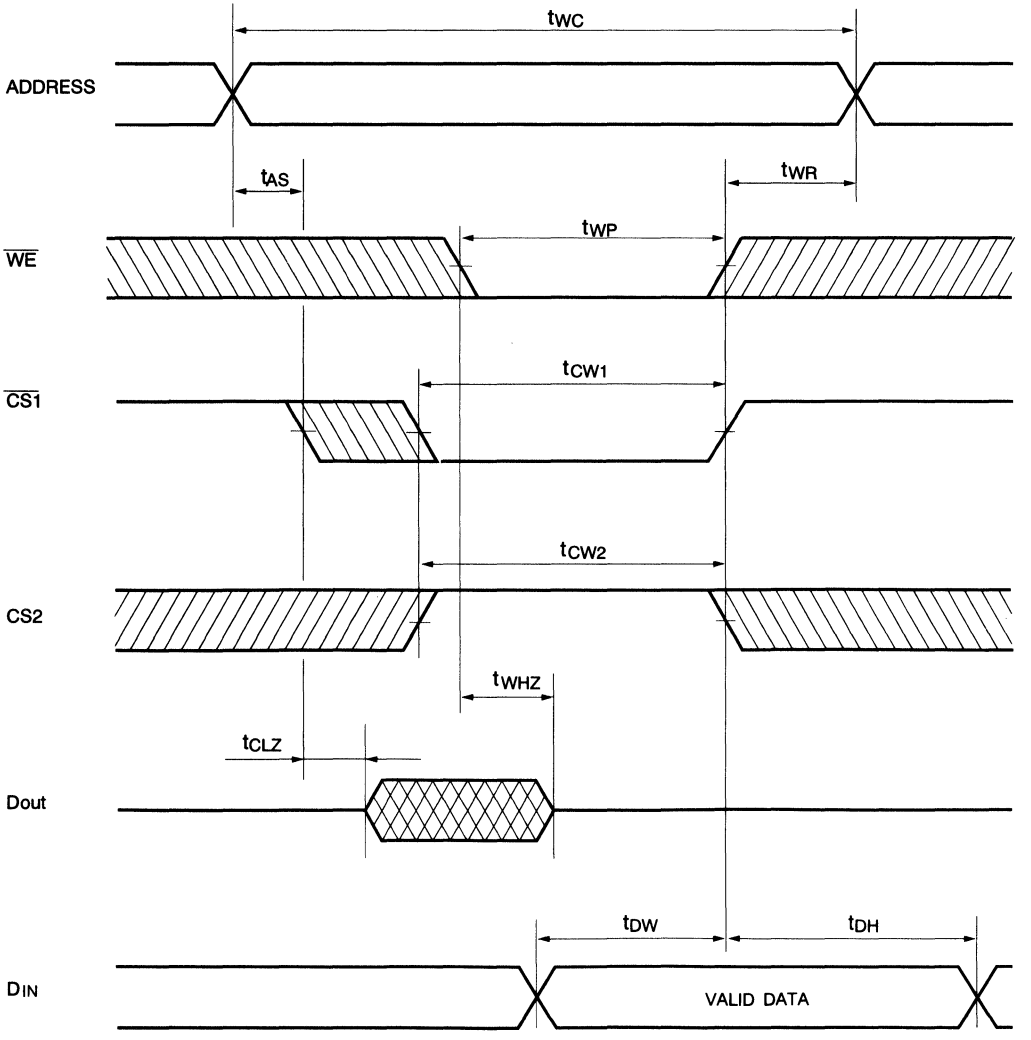
Read Cycle (Note 1)



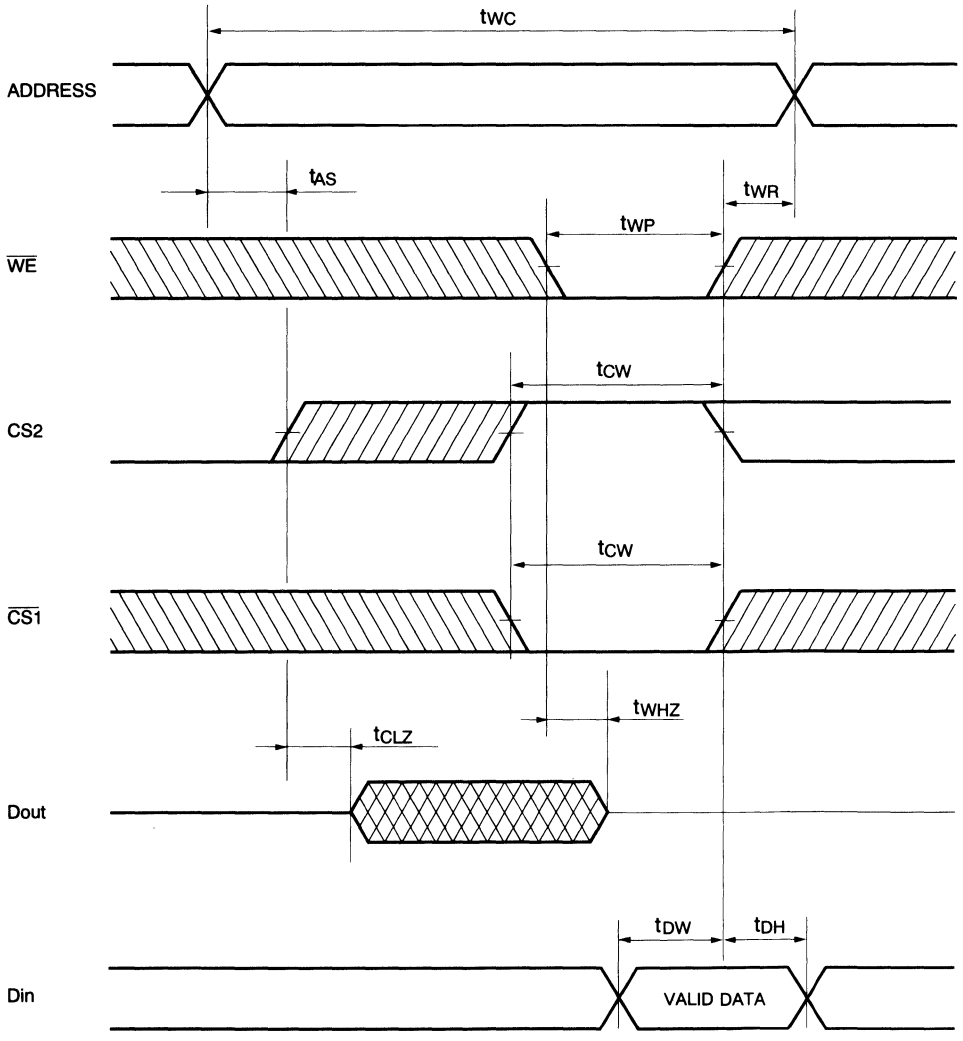
Write Cycle(1) ($\overline{WE}$ Controlled) (Notes 2,3,4)



Write Cycle (2)($\overline{CS1}$ Controlled) (Note 4)



Write Cycle (3)(CS2 Controlled) (Note 4)



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Assuming that $\overline{CS1}$ Low transition or CS2 High transition occurs coincident with or after $\overline{WE}$ Low transition. Outputs remain in a high impedance state.
3. Assuming that $\overline{CS1}$ High transition or CS2 Low transition occurs coincident with or prior to $\overline{WE}$ High transition. Outputs remain in a high impedance state.
4. Assuming that $\overline{OE}$ is high for write cycle. Outputs are in a high impedance state during this period.

Capacitance: (f = 1MHz, T_A = 25°C)

Symbol	Parameter	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_I = 0V	—	8	pF
C_{OUT}	Input Capacitance	V_O = 0V	—	8	pF

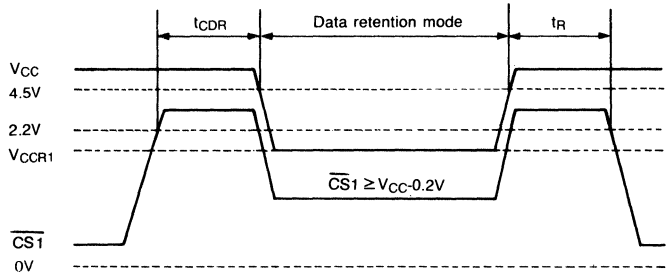
Note: This parameter is sampled and not 100% tested.

Data Retention Characteristics (T_A = 0 ~ 70°C)

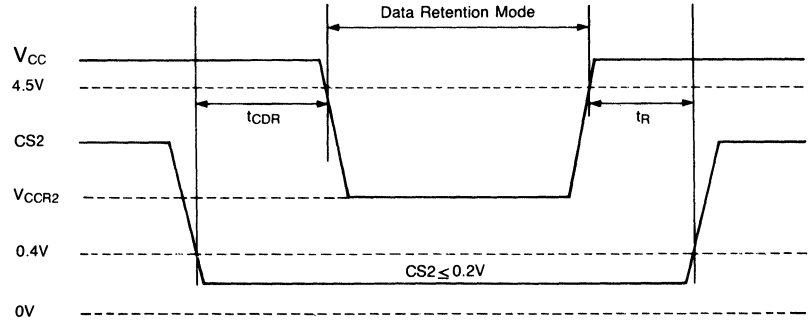
Symbol	Parameter			Min	Typ	Max	Unit
V_{CCR}	Data Retention Supply Voltage			2.0	—	5.5	V
I_{CCR}	Data Retention Current	V_{CC} = 3.0V	L	—	1	50*	μA
			LL	—	1	25	
t_{CDR}	Chip Select to Data Retention Time			0	—	—	ns
t_R	Operation Recovery Time			5	—	—	ns

*20μA max at T_A = 0 ~ 40°...

• Low V_{CC} Data Retention Mode: (1) $\overline{CS1}$ Controlled



• Low V_{CC} Data Retention Mode: (2) CS2 Controlled

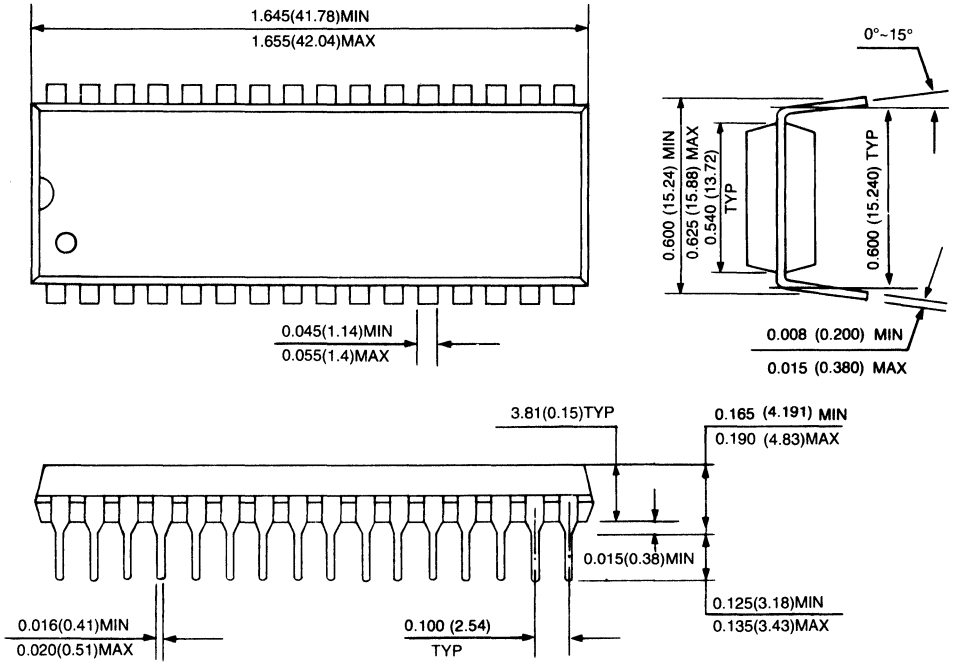


Note: In Data Retention Mode, CS2 controls the Address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$ and D_{IN} buffer. If CS2 controls data retention mode, V_{IN} for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, CS2 must satisfy either CS2 ≥ V_{CC}-0.2V or CS2 ≤ 0.2V. The other input levels (Address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the high impedance state.

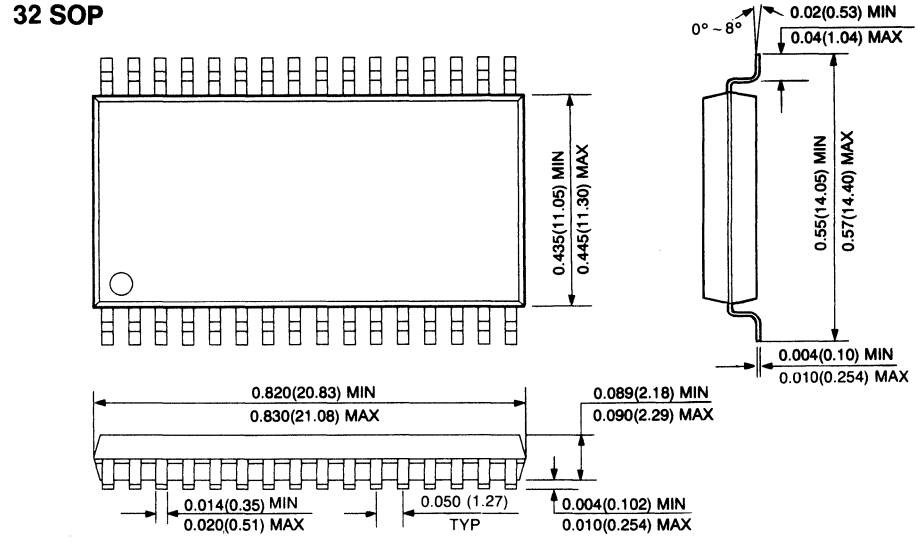
Package Dimensions

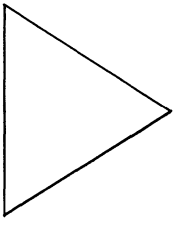
Unit: inches (mm)

32 DIP



32 SOP





GoldStar
GOLDSTAR ELECTRON CO., LTD.

GM231000

131,072 WORDS × 8 BIT
NMOS MASK ROM

Description

The GM231000 high-performance Read Only Memory is organized as 131,072 words by eight bits an access time of 200/250 ns. It is desgined to be compatible with all microprocessors and similar applications where high performance large-bit storage and simple interfacing are important considerations.

The GM231000 offers automatic power down controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains HIGH. This feature provides system level power savings of as much as 80%. Pin 20 can also be Mask Programmed as a $\overline{CS}$ or CS allowing two GM231024 ROM's to be wired-OR without external decoding.

This ROM is packaged in industry-standard 28 pin dual-in-line package and is available in ceramic or low-cost plastic.

Features

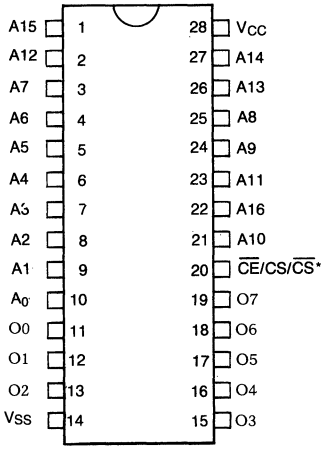
- 131,072×8 organization
- Single +5V Supply
- Access time 200/250 ns (Max)
- Totally static operation
- Completely TTL compatible
- Operating current 100 mA (Max)
- Standby current 20 mA (Max)
- Automatic power down ($\overline{CE}$)
  Programmable Chip Select
  3-state outputs for wired-OR expansion
- 28-pin industry-standard DIP (600 mil)
- EPROMs accepted as program data input

Pin Description

Pin	Function
A0~A16	Address Inputs
O0~O7	Data Outputs
CE	Chip Enable Input
CS/$\overline{CS}$	Chip Select Input
V_{CC}	Power Supply
V_{SS}	Ground

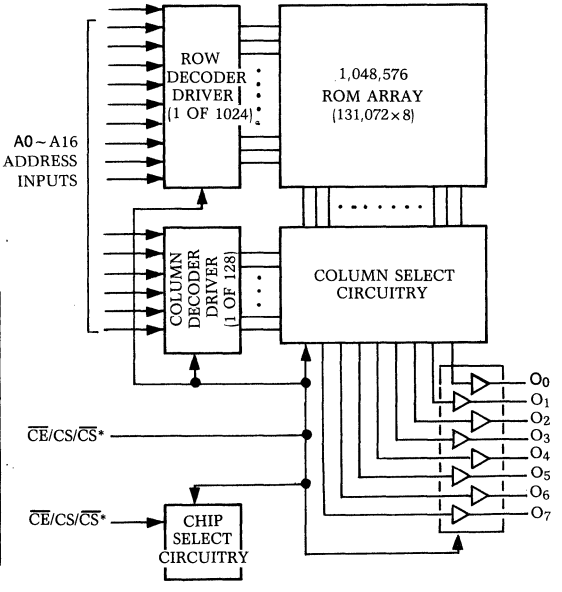
Pin Configuration

28 DIP (Top View)



*CHIP SELECT(CS) IS PROGRAMMABLE ACTIVE LOW OR ACTIVE HIGH.

Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Operating Temperature	0~70	°C
T_{STG}	Storage Temperature	−65~125	°C
V_{CC}	Supply Voltage Ground Potential	−0.5~7.0	V
V_{OUT}	Applied Output Voltage	−0.5~7.0	V
V_{IN}	Applied Input Voltage	−0.5~7.0	V
P_D	Power Dissipation	1.0	W

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics: ($V_{CC}=5V\pm10\%$, $V_{SS}=0V$, $T_A=0\sim70°C$)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	$I_{OH}=-1.0mA$	2.4		V
V_{OL}	Output Low Voltage	$I_{OL}=3.2mA$		0.4	V
V_{IH}	Input High Voltage		2.0		V
V_{IL}	Input Low Voltage		−0.5	0.8	V
I_{LI}	Input Leakage Current	$V_{IN}=0V$ to V_{CC}		10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0V$ to V_{CC}		10	μA
I_{CC}	Operating Supply Current	Note 1		100	mA
I_{SB}	Standby Supply Current	$\overline{CE}=V_{IH}$		20	mA
I_{OS}	Output Short Circuit Current	Note 2		90	mA

AC Operating Characteristics ($V_{CC}=5V\pm10\%$, $T_A=0\sim70°C$, GND=0V

Symbol	Parameter	GM231000-20		GM231000-25		Unit	Note
		Min	Max	Min	Max		
t_{RC}	Cycle Time	200		250		ns	
t_{AA}	Address Access Time		200		250	ns	
t_{OH}	Output Hold After Address Change	10		10		ns	
t_{ACE}	Clip Enable Access Time		200		250	ns	
t_{ACS}	Chip Select Access Time		85		100	ns	
t_{LZ}	Output LOW-Z Delay	10		10		ns	3
t_{HZ}	Output HIGH-Z Delay		85		100	ns	4

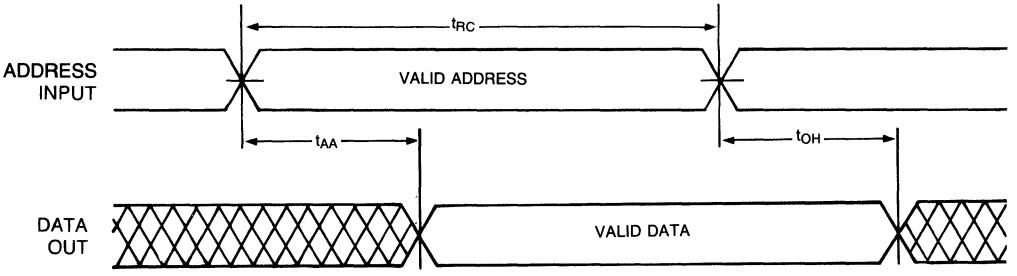
Capacitance ($T_A=25°C$, f=1.0 MHz, Note 5)

Symbol	Parameter	Conditions	Min	Max	Unit
C_I	Input Capacitance	$V_{IN}=0V$		5	pF
C_O	Output Capacitance	$V_{OUT}=0V$		5	pF

Notes:
1. Measured with device selected and outputs unloaded.
2. For a duration not to exceed 30 seconds.
3. Output LOW impedance delay (t_{LZ}) is measured from $\overline{CE}$ or CS going active.
4. Output HIGH impedance delay (t_{HZ}) is measured from $\overline{CE}$ or CS going inactive.
5. This parameter is periodically sampled and is not 100% tested.

TIMING WAVEFORMS

Propagation Delay From Address ($\overline{CE}$/CS/$\overline{CS}$ Active)



Propagation Delay From Chip Enable, Chip Select or Output Enable (Address Valid)

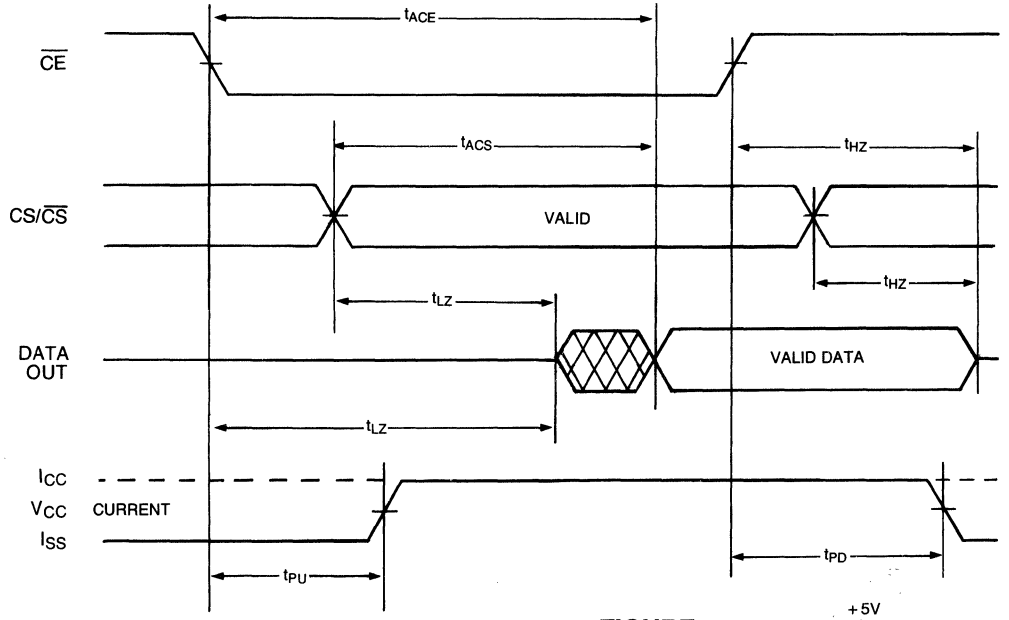
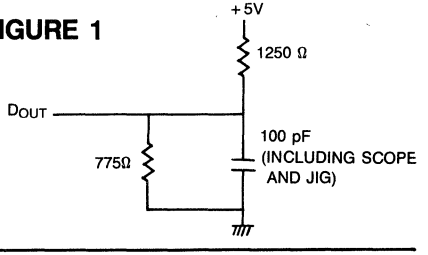


FIGURE 1



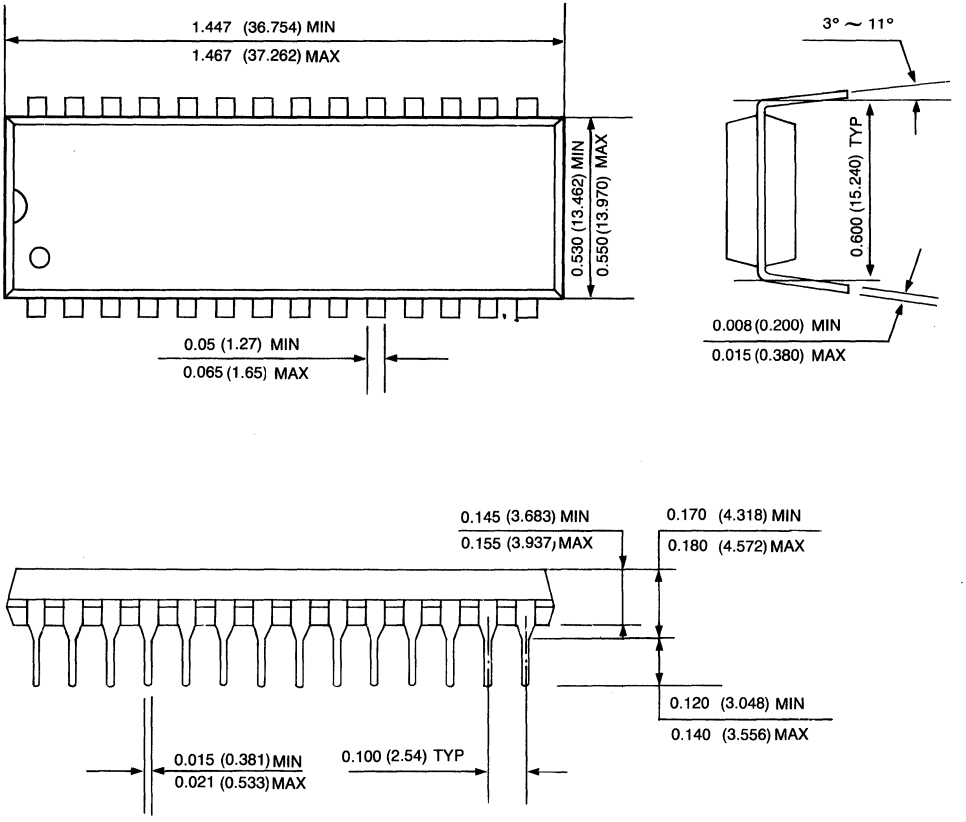
AC Test Conditions

Input Pulse Levels	0.8 to 2.2V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8 and 2.0V
Output Load	See Figure 1

Package Dimensions

28 DIP

Unit: inches (mm)



GM23C1000

131,072 WORDS×8 BIT
CMOS MASK ROM

Description

The GM23C1000 is a high performance read only memory organized as 131,072 words by 8 bits. It is designed to be compatible with all microprocessors and similar applications where high-performance large-bit storage and simple interfacing are important design considerations. The GM23C1000 offers automatic powerdown controlled by the Chip Enable CE/$\overline{CE}$ input. When CE/$\overline{CE}$ goes LOW/HIGH, the device will automatically power down and remain in a low power standby mode as long as CE/$\overline{CE}$ remains LOW/HIGH. Pin 20 may a so be mask programmed as CS/$\overline{CS}$ (active HIGH or LOW, but not powerdown) in order to eliminate bus contention in multiple bus micro-processor systems.

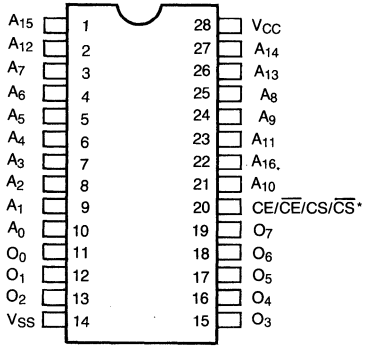
Features

- 131,072×8-bit organization
- Single +5V Power Supply
- Access times: 100/120 ns (Max.)
- Current
  Operating: 40 mA (Max.)
  Standby: 30μA (Max.)
- 3-state outputs for wired-OR expansion
- Mask programmed for Chip Enable (Powerdown) CE/$\overline{CE}$ or Chip Select CS/$\overline{CS}$
- Fully static operation
- TTL-compatible inputs and outputs
- 28-pin industry-standard DIP (600 mil)

Pin Description

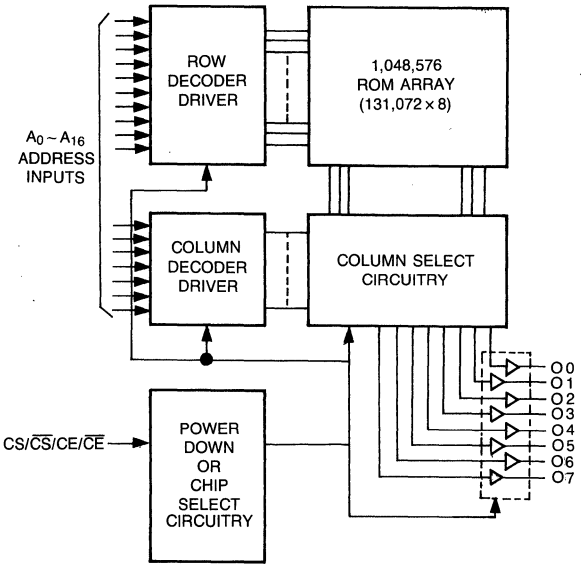
Pin	Function
A0~A16	Address Inputs
O0~O7	Data Outputs
CE/$\overline{CE}$	Chip Enable Input
CS/$\overline{CS}$	Chip Select Input
V_{CC}	Power Supply
V_{SS}	Ground

Pin Configuration
28 DIP (Top View)



*Chip Select (CS) is Programmable Active Low or Active High.

Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Operating Temperature	−10 ~ 80	°C
T_{STG}	Storage Temperature	−65 ~ 150	°C
V_{CC}	Supply Voltage to Ground Potential	−0.5 ~ 7.0	V
V_{OUT}	Output Voltage	−0.5 ~ V_{CC} + 0.5	V
V_{IN}	Input Voltage	−0.5 ~ V_{CC} + 0.5	V
P_D	Power Dissipation	300	mW
	Soldering Temp. & Time	250, 10	°C, sec

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics: (T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%, GND = 0V)

Symbol	Parameter	Conditions	Min.	Max.	Unit	Note
V_{OH}	Output High Voltage	I_{OH} = −1.0mA	2.4		V	
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA		0.4	V	
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V	
V_{IL}	Input Low Voltage		−0.5	0.8	V	
I_{LI}	Input Leakage Current	V_{IN} = 0V to V_{CC}		10	μA	
I_{LO}	Output Leakage Current	V_{OUT} = 0V to V_{CC}		10	μA	1
I_{CC}	Operating Current	1 cyc = 100ns		40	mA	2
I_{SB}	Standby Current	CE = V_{IH}, CE = V_{IL}		1.5	mA	
I_{SBI}	Standby Current	CE = V_{CC}-0.2V, CE = 0.2V		30	μA	

Capacitance:

Symbol	Parameter	Conditions	Min.	Max.	Unit	Note
C_I	Input Capacitance	T_A = 25°C		10	pF	—
C_O	Output Capacitance	f = 1.0 MHz		10	pF	3

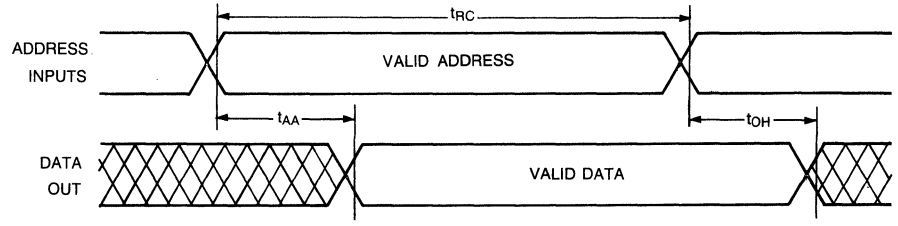
AC Characteristics ($T_A = 0°C \sim 70°C$, $V_{CC} = 5V \pm 10\%$, GND = 0V)

Symbol	Parameter	GM23C1000-10		GM23C1000-12		Unit	Note
		Min	Max	Min	Max		
t_{RC}	Read Cycle Time	100		120		ns	
t_{AA}	Address Access Time		100		120	ns	
t_{ACE}	Chip Enable Access Time		100		120	ns	
t_{ACS}	Chip Select Access Time		85		100	ns	
t_{OH}	Output Hold After Address Change	10		10		ns	
t_{LZ}	Output Low-Z Delay	10		10		ns	4
t_{HZ}	Output High-Z Delay		50		60	ns	5
t_{PU}	Power-Up Time	0		0		ns	
t_{PT}	Powerdown Time		50		60	ns	

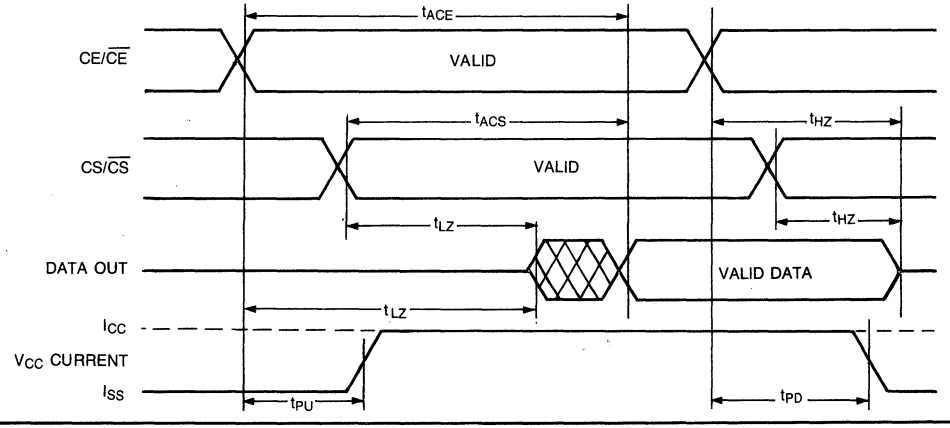
Notes:
1. CS/CE = V_{IL}, $\overline{CS}/\overline{CE}$ = V_{IH} (Output is unloaded).
2. $V_{IN} = V_{IH}/V_{IL}$. But CS/CE = V_{IH}. $\overline{CS}/\overline{CE} = V_{IL}$ (Output is unloaded).
3. This parameter is periodically sampled and is not 100% tested. All pins except pin under test tied to AC ground.
4. Output Low impedance delay (t_{LZ}) is measured from CE/$\overline{CE}$ or CS/$\overline{CS}$ going active.
5. Output High impedance delay (t_{HZ}) is measured from CE/$\overline{CE}$ or CS/$\overline{CS}$ going inactive.

Timing Waveforms

PROPAGATION DELAY FROM ADDRESS (CE/$\overline{CE}$ = ACTIVE, CS/$\overline{CS}$ = ACTIVE)



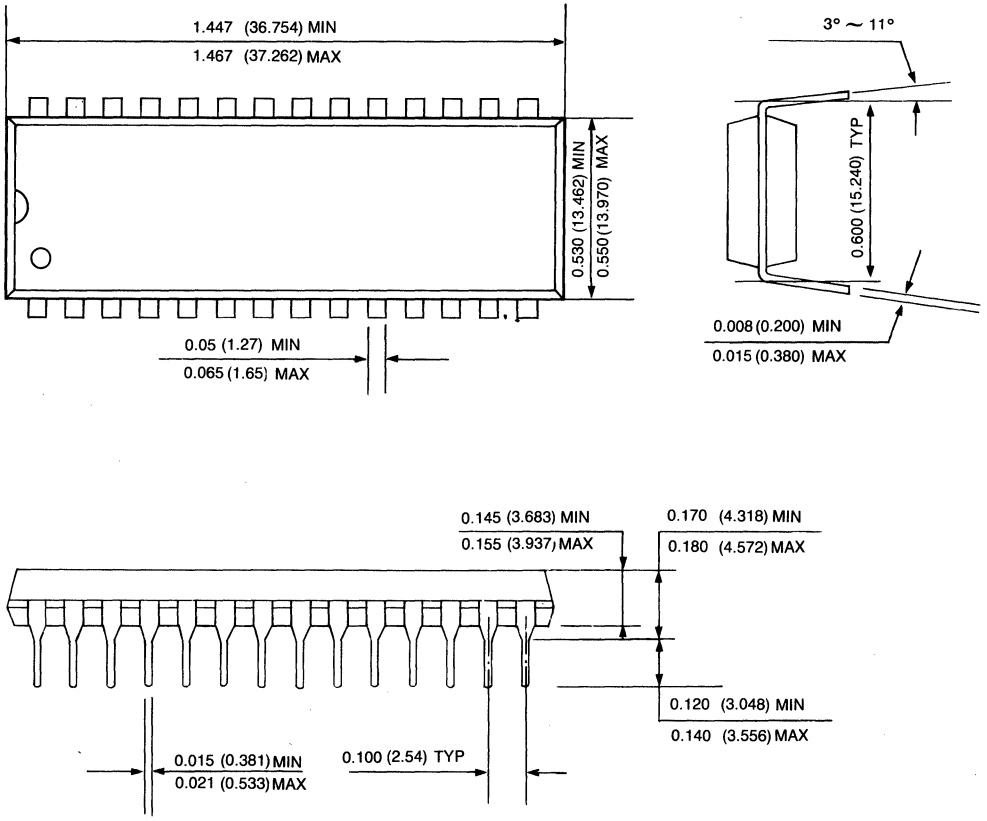
PROPAGATION DELAY FROM CHIP ENABLE, OR CHIP SELECT (ADDRESS VALID)



Package Dimensions

28 DIP

Unit: inches (mm)



GM23C4000

524,288 WORDS × 8 BIT
CMOS MASK ROM

Description

The GM23C4000 high-performance Read Only Memory is organized as 524,288 words by eight bits and has an access time of 150/200ns. It is designed to be compatible with all microprocessors and similar applications where high performance large-bit storage and simple interfacing are important considerations. The GM23C4000 offers automatic power down controlled by the Chip Enable ($\overline{CE}$) input. When $\overline{CE}$ goes HIGH, the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains HIGH. This feature provides system level power savings of as much as 80%. The GM23C4000 is packaged in a 32-DIP, provides polarity programmable $\overline{CE}$ and $\overline{OE}$, CS buffer as user option mode.

Features

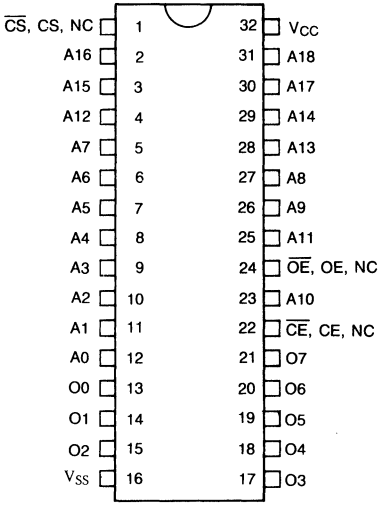
- 524,288 × 8 organization
- Single +5V Supply
- Access time 150/200ns (Max)
- Totally static operation
- Completely TTL compatible
- Operating current 60mA (Max)
- Standby current 100μA (Max)
- Automatic power down ($\overline{CE}$)
  Programmable Chip Select
  3-state outputs for wired-OR expansion
- 32-pin industry-standard DIP (600 mil)
- EPROMs accepted as program data input
- Polarity programmable chip enable and output enable, chip select pin

Pin Description

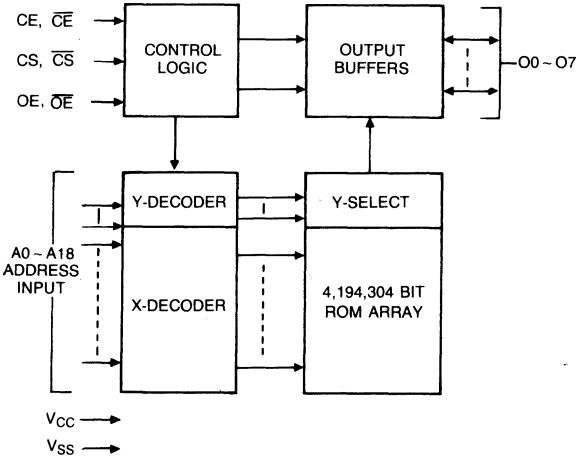
Pin	Function
A0 ~ A18	Address Inputs
O0 ~ O7	Data Output
$\overline{CS}$, CS, NC	Chip Select Input
$\overline{CE}$, CE, NC	Chip Enable Input
$\overline{OE}$, OE, NC	Output Enable Input
V_{CC}	Power Supply
V_{SS}	Ground

Pin Configuration

32 DIP (Top View)



Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Operating Temperature	0~70	°C
T_{STG}	Storage Temperature	-65~125	°C
V_{CC}	Supply Voltage Ground Potential	-0.5~7.0	V
V_{OUT}	Applied Output Voltage	-0.5~7.0	V
V_{IN}	Applied Input Voltage	-0.5~7.0	V
P_D	Power Dissipation	1.0	W

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics: ($V_{CC}=5V\pm10\%$, $T_A=0\sim70°C$)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Voltage	$I_{OH}=-400\mu A$	2.4		V
V_{OL}	Output Low Voltage	$I_{OL}=1.6mA$		0.4	V
V_{IH}	Input High Voltage		2.2	$V_{CC}+0.3$	V
V_{IL}	Input Low Voltage		-0.3	0.8	V
I_{LI}	Input Leakage Current	$V_{IN}=0V$ to V_{CC}		10	μA
I_{LO}	Output Leakage Current	$V_{OUT}=0V$ to V_{CC}		10	μA
I_{CC}	Operating Supply Current	Note 1		50	mA
I_{SB}	Standby Supply Current	$\overline{CE}=V_{IH}$		1	mA
I_{SB1}	Power-Down Supply Current	$\overline{CE}=V_{CC}\pm0.3V$		100	μA

AC Operating Characteristics ($V_{CC}=5V\pm10\%$, $T_A=0\sim70°C$)

Symbol	Parameter	GM23C4000-15		GM23C4000-20		Unit	Note
		Min	Max	Min	Max		
t_{RC}	Read Cycle Time	150		200		ns	
t_{AA}	Address Access Time		150		200	ns	
t_{OH}	Output Hold After Address Change	10		10		ns	
t_{ACE}	Chip Enable Access Time		150		200	ns	
t_{ACS}	Chip Select Access Time		75		90	ns	
t_{AOE}	Output Enable Access Time		75		90	ns	
t_{LZ}	Output LOW-Z Delay	10		10		ns	2
t_{HZ}	Output HIGH-Z Delay		85		90	ns	3

Capacitance ($T_A=25°C$, $f=1.0$ MHz, Note 4)

Symbol	Parameter	Conditions	Min	Max	Unit
C_I	Input Capacitance	$V_{IN}=0V$		15	pF
C_O	Output Capacitance	$V_{OUT}=0V$		25	pF

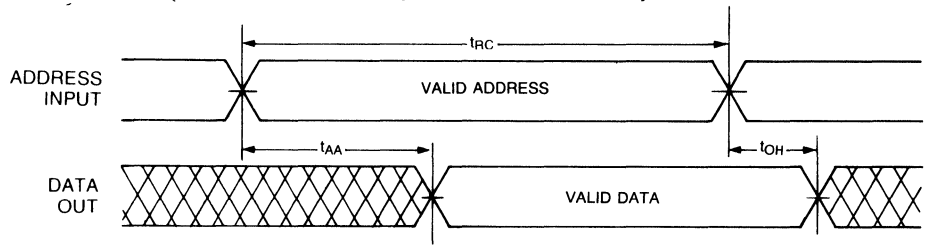
Notes:
1. Measured with device selected and outputs unloaded.
2. Output LOW impedance delay (t_{LZ}) is measured from $\overline{CE}$ going LOW.
3. Output HIGH impedance delay (t_{HZ}) is measured from $\overline{CE}$ going HIGH.
4. This parameter is periodically sampled and is not 100% tested.

Mode Selection

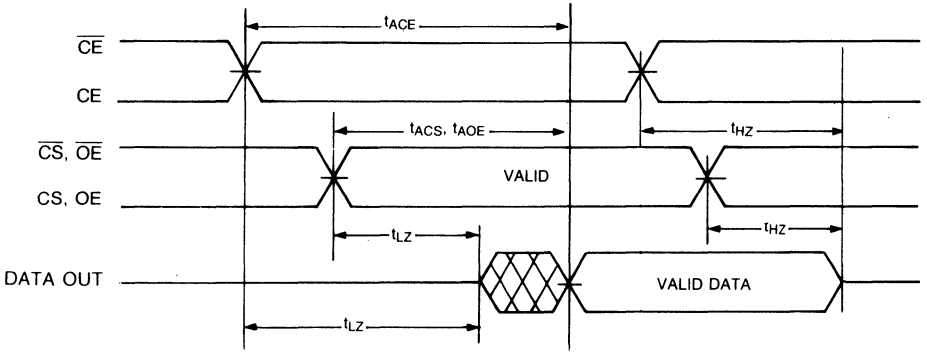
CE/$\overline{CE}$	OE/$\overline{OE}$	CS/$\overline{CS}$	Mode	Data	Power
L/H	X	X	Standby	High-Z	Standby
H/L	X	L/H	Operating	High-Z	Active
H/L	L/H	X	Operating	High-Z	Active
H/L	H/L	H/L	Operating	Dout	Active

TIMING WAVEFORMS

Propagation Delay From Address ($\overline{CE}$/$\overline{CS}$/$\overline{OE}$ = Active)



Propagation Delay From Chip Enable (Address Valid)



AC Test Conditions

Input Pulse Levels	0.4 to 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.5V
Output Timing Level	0.8 and 2.0V
Output Load	See Figure 1

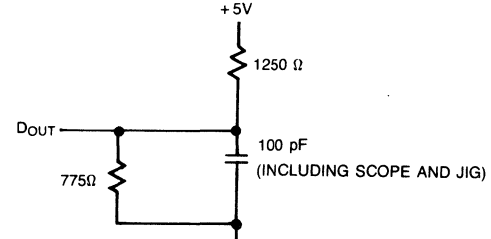
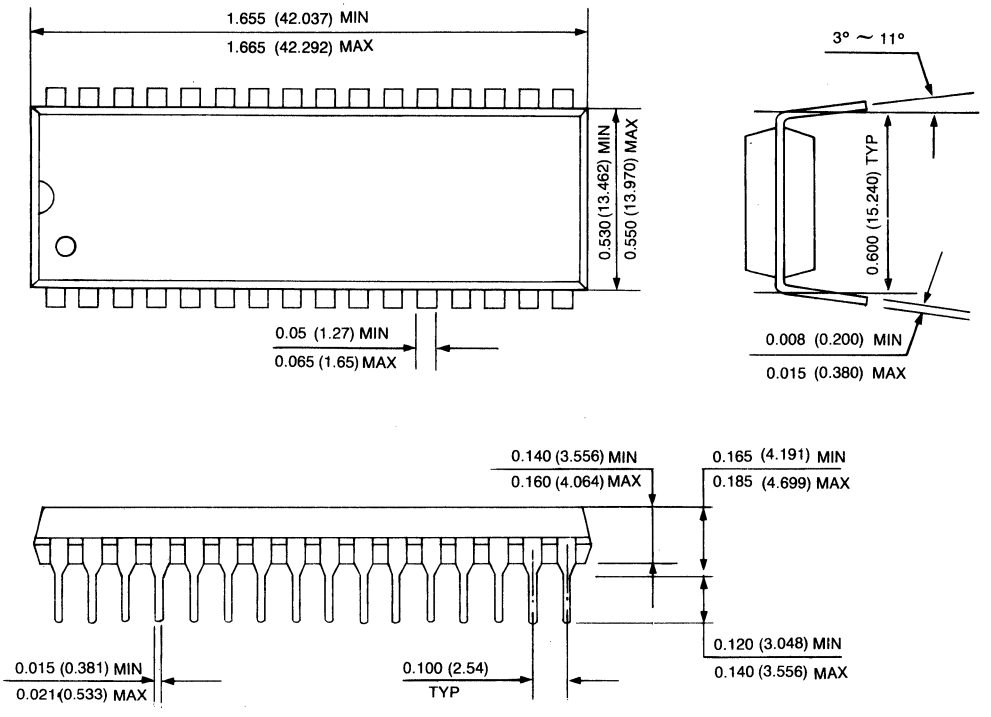


FIGURE 1

Package Dimensions

32 DIP

Unit: inches (mm)



GoldStar
GOLDSTAR ELECTRON CO., LTD.

GM23C4100

512K × 8 / 256K × 16 BIT
CMOS MASK ROM

Description

The GM23C4100 high performance read only memory is organized either as 524,288 × 8 bit (Byte Mode) or as 262,144 × 16 bit (Word Mode) followed by BHE mode select.

The GM23C4100 offers automatic power down controlled by the mark programmed CE or $\overline{CE}$ input. The low power feature allows the battery operation. The large size of 4M bit memory density is ideal for character generator, data or program memory in microprocessor application. This ROM is packaged in 40 pin DIP or 44 pin QFP.

Features

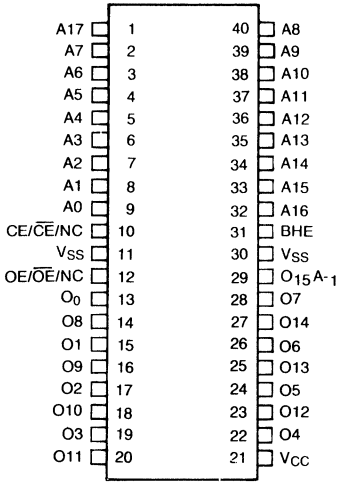
- Single +5V Power Supply
- TTL compatible
- High Speed: Maximum 150ns T_{AA}
- Programmable chip enable and output enable
- Low power consumption
  - Operating: 50mA maximum
  - Standby: 100μA maximum
- Byte or Word switchable by BHE pin (BHE can be switched on the fly or a DC signal)
- Package: 40 pin (600 mil) DIP or 44 pin QFP

Pin Description

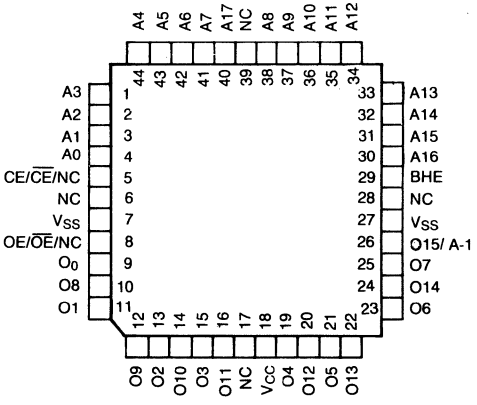
Pin	Function
A0 ~ A17	Address Inputs
O0 ~ O14	Data Outputs
O15/A-1	Output O_{15} (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$/NC	Chip Enable
OE/$\overline{OE}$/NC	Output Enable
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

Pin Configuration

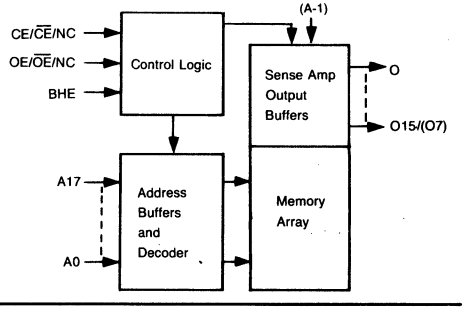
40 DIP (Top View)



44 QFP (Top View)



Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Ambient Operating Temperature	0~70	°C
T_{STG}	Storage Temperature (plastic)	-65~125	°C
V_{CC}	Voltage on any Pin Except Relative to V_{SS}	-0.5~7.0	V

*Operation at or above "Absolute Maximum Ratings" can adversely affect device reliability.

Recommended Operating Conditions (T_A = 0~70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3	—	0.8	V

DC Electrical Characteristics: (V_{CC}=5V±10%, V_{SS}=0V T_A=0 to 70°C)

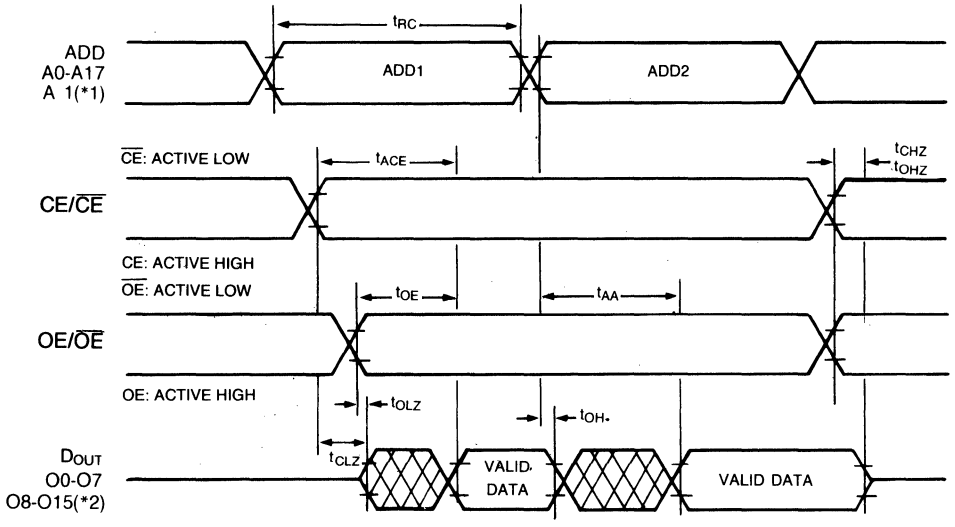
Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	Output High Level Voltage	I_{OH}=-400μA	2.4	—	V
V_{OL}	Output Low Level Voltage	I_{OL}=2.1mA	—	0.4	V
I_{CC}	Operating Current	$\overline{CE}$=$\overline{OE}$=V_{IL}, f=5.0MHz all I/O's=open	—	50	mA
I_{SB}	Standby Current (BIP)	$\overline{CE}$=I_{IH}, all I/O's=open	—	1	mA
I_{SB1}	Standby Current (CMOS)	$\overline{CE}$=V_{CC}, all I/O's=open	—	100	μA
I_{LI}	Input Leakage Current	V_{IN}=0 to V_{CC}	—	10	μA
I_{LO}	Output Leakage Current	V_{OUT}=0 to V_{CC}	—	10	μA

Mode Selection

CE/$\overline{CE}$	OE/$\overline{OE}$	BHE	O15/A-1	Mode	Data	Power
L/H	X	X	X	Standby	High-Z	Standby
H/L	L/H	X	X	Operating	High-Z	Active
H/L	H/L	H	Output	Operating	O0-O15:D_{OUT}	Active
	H/L	L	Input	Operating	O0-O7: D_{OUT} O8-O14:High-Z	Active

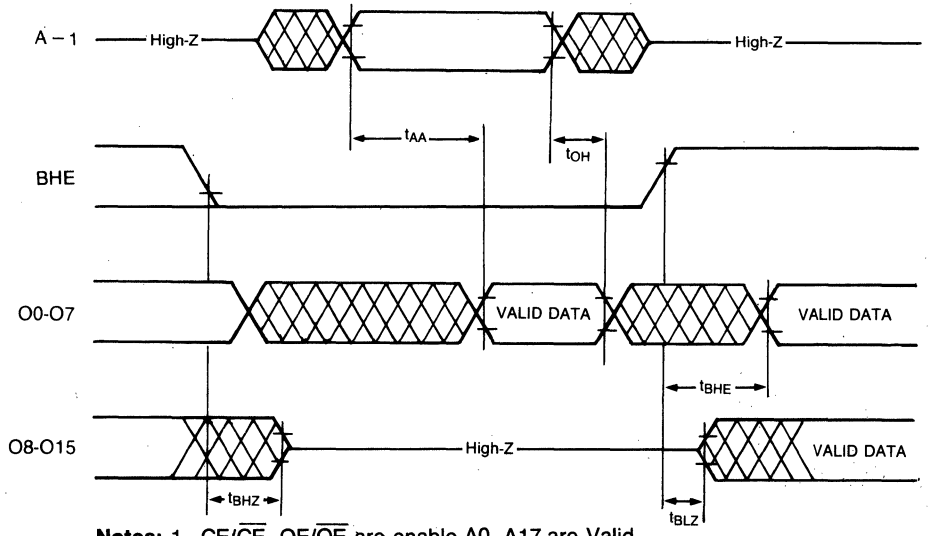
TIMING WAVEFORMS

(1) Word Mode (BHE = V_{IH})/Byte Mode (BHE = V_{IL})



(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})
(*2) Word Mode only. (BHE = V_{IH})

(2) Word Mode, Byte Mode Switch



Notes: 1. CE/$\overline{CE}$, OE/$\overline{OE}$ are enable A0 - A17 are Valid.
2. If BHE is high and $\overline{CE}$, $\overline{OE}$ is enable O15/A – 1 pin is in the output state.
3. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

AC Operating Characteristics ($V_{CC}=5V\pm10\%$, $T_A=0\sim70°C$)

Symbol	Parameter	GM23C4100-15		GM23C4100-20		Unit
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	150		200		ns
t_{ACE}	Chip Enable Access Time		150		200	ns
t_{AA}	Address Access Time		150		200	ns
t_{OE}	Output Enable Access Time		70		80	ns
t_{OHZ} t_{CHZ}	Output or Chip Disable to Output High-Z		60		70	ns
t_{OH}	Output Hold from Address Change	10		10		ns
t_{OLZ} t_{CLZ}	Output or Chip Enable to Output in Low-Z	10		10		ns
t_{BHE}	BHE Access Time		150		200	ns
t_{BHZ}	BHE Low to Output O8-O15 in High-Z		60		70	ns
t_{BLZ}	BHE High to Output O8-O15 in Low-Z	10		10		ns

*Test Condition
Input Pulse Level: 0.6V to 2.4V
Input Rise and Fall Times: 10ns
Input and Output Timing Levels: 0.8V and 2.0V
Output Loads: 1 TTL gate and $C_L=100pF$.

Capacitance* ($T_A=25°C$, $f=1.0MHz$)

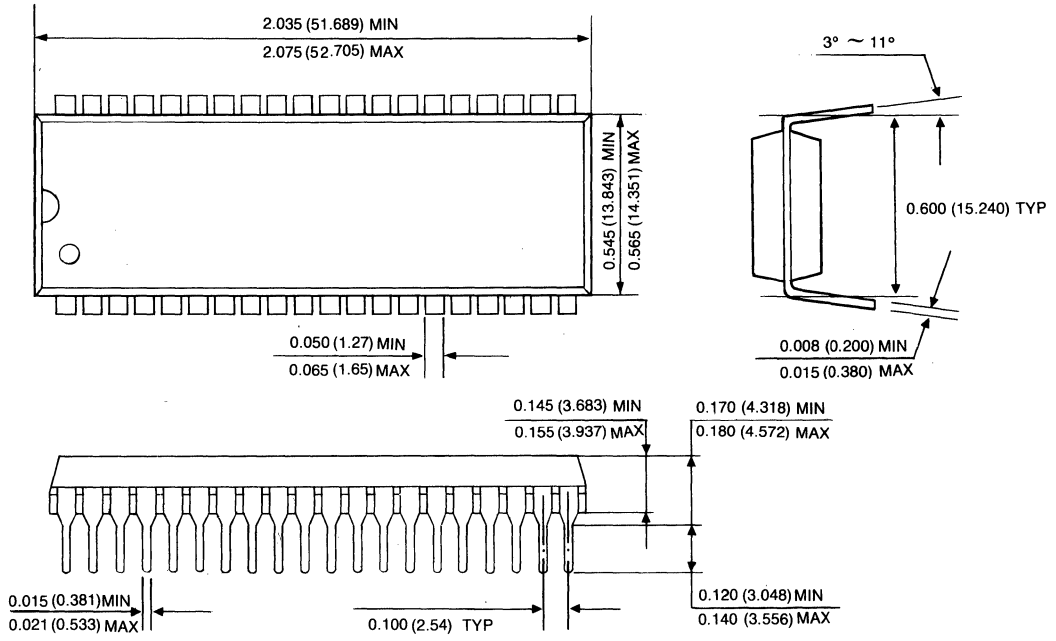
Symbol	Parameter	Test Conditions	Min	Max	Unit
C_O	Output Capacitance	$V_{OUT}=0V$		8.0	pF
C_I	Input Capacitance	$V_{IL}=0V$		8.0	pF

*Capacitance is periodically sampled and not 100% tested.

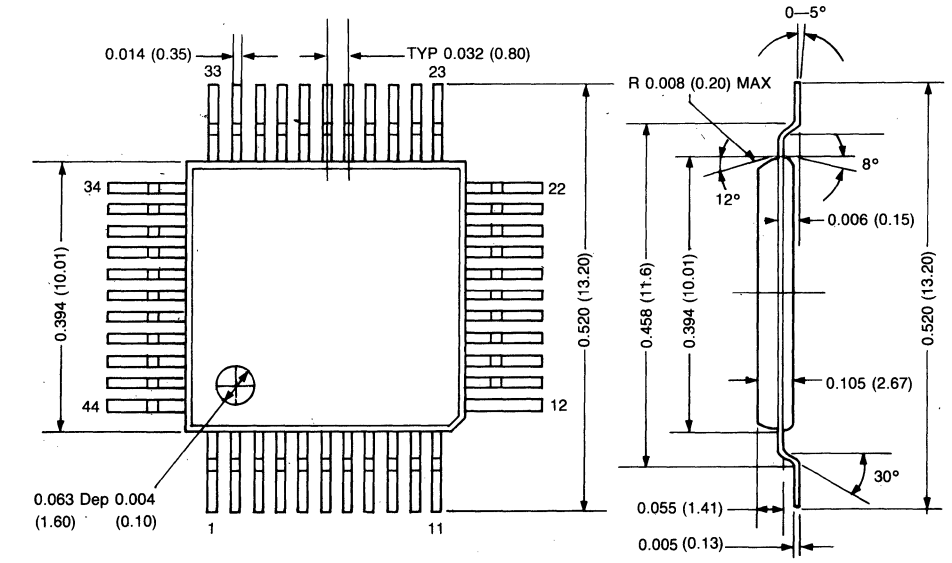
Package Dimensions

40 DIP

Unit: inches (mm)



44 QFP



GM23C8100

512K×16/1M × 8 BIT
CMOS MASK ROM

Description

The GM23C8100 high performance read only memory is organized either as 1,048,576×8 bit (Byte Mode) or as 524,288×16 bit (Word Mode) followed by BHE mode select.
The GM23C8100 offers automatic power down controlled by the mark programmed CE or $\overline{CE}$ input. The low power feature allows the battery operation. The large size of 8M bit memory density is ideal for character generator, data or program memory in microprocessor application. This ROM is packaged in 42 pin DIP.

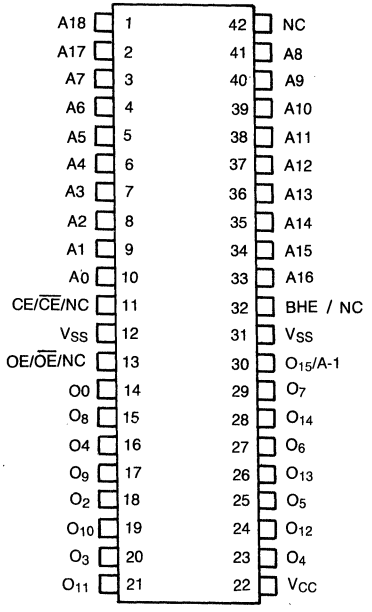
Features

- Single +5V Power Supply
- TTL compatible
- High Speed: Maximum 150ns/200ns
- Programmable chip enable and output enable
- Low power consumption
  Operating: 50mA maximum
  Standby: 30μA maximum
- Byte or Word switchable by BHE pin (BHE can be switched on the fly or a DC signal)
- Package: 42-pin plastic DIP

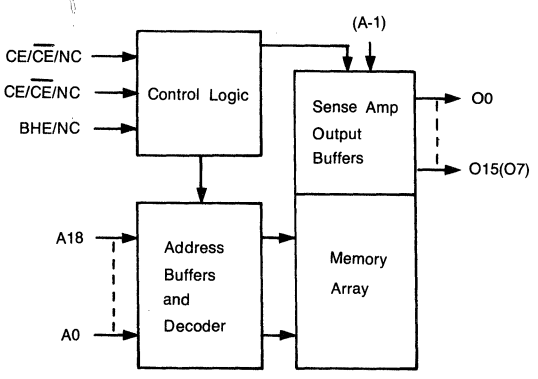
Pin Description

Pin	Function
A0 ~ A18	Address Inputs
O0 ~ O14	Data Outputs
O15/A-1	Output Data 15 (Word mode)/ LSB Address (Byte mode)
BHE	Word/Byte Selection
CE/$\overline{CE}$/NC	Chip Enable
OE/$\overline{OE}$/NC	Output Enable
V_{CC}	Supply Power (+5V)
V_{SS}	Ground
NC	No Connection

Pin Configuration
42 DIP (Top View)



Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Operating Temperature	0~70	°C
T_{STG}	Storage Temperature	-55~150	°C
V_{CC}	Supply Voltage	-0.3~7.0	V
V_{OUT}	Output Voltage	-0.3~V_{CC}+0.3	V
V_{IN}	Input Voltage	-0.3~V_{CC}+0.3	V

*Operation at or above "Absolute Maximum Ratings" can adversely affect device reliability.

Recommended Operating Conditions (T_A=0~70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2		V_{CC}+0.3	V
V_{IL}	Input Low Voltage	-0.3		0.8	V

DC Electrical Characteristics: (V_{CC}=5V±10%, V_{SS}=0V, T_A=0~70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH}=-1.0mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=2.1mA			0.4	V
I_{LI}	Input Leakage Current	V_{IN}=0 to V_{CC}			1	μA
I_{LO}	Output Leakage Current	V_{OUT}=0 to V_{CC}			1	μA
I_{SB}	Standby Current (BIP)	/CE Disabled (V_{IH}) All Output Open		0.1	1	mA
I_{SB1}	Standby Current (MOS)	/CE Disabled (V_{CC}-0.2V) All Output Open		5	30	μA
I_{CC}	Operating Current	T_{CYC}=MIN, /CE&/OE=V_{IL} All Input V_{IL}/V_{IH} All Output Open			50	mA

AC Characteristics

Symbol	Parameter	GM23C8100-15		GM23C8100-20		Unit
		Min	Max	Min	Max	
t_{RC}	Read Cycle Time	150		200		ns
t_{AA}	Address Access Time		150		200	ns
t_{ACE}	Chip Enable Access Time		150		200	ns
t_{OE}	Output Enable Access Time		70		80	ns
t_{BHE}	BHE Access Time		150		200	ns
t_{BHZ}	BHE Low To Output O_8-O_{15} In High-Z		60		70	ns
t_{BLZ}	BHE High To Output O_8-O_{15} In Low-Z	10		10		ns
t_{OHZ} t_{CHZ}	Output or Chip Disable To Output High-Z		60		70	ns
t_{OH}	Output Hold From Address Change	10		10		ns
t_{OLZ} t_{CLZ}	Output or Chip Enable To Output In Low-Z	10		10		ns

*TEST CONDITION

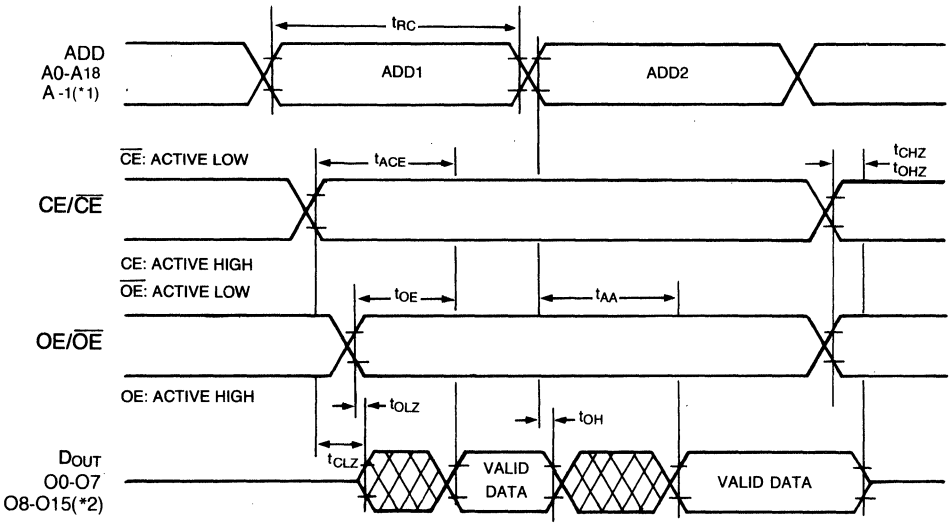
Input Pulse Levels ..... 0.6V to 2.2V
Input Rise and Fall Times 10ns
Output and Output Timing Levels ..... 0.8V to 2.0V
Output Loads ..... 1 TTL + 100 pF

Mode Selection

Mode	/CE,CE	/OE,OE	Byte	D0-D7	D8-D14	D15/A-1	Power
16 Bit Operating	L, H	L, H	H	Data Out			Active
8 Bit Operating	L, H	L, H	L	Out	High-Z	LSB	Active
Output Disable	L, H	H, L	X	High-Z	High-Z	High-Z	Active
Standby	H, L	X	X	High-Z	High-Z	High-Z	Standby

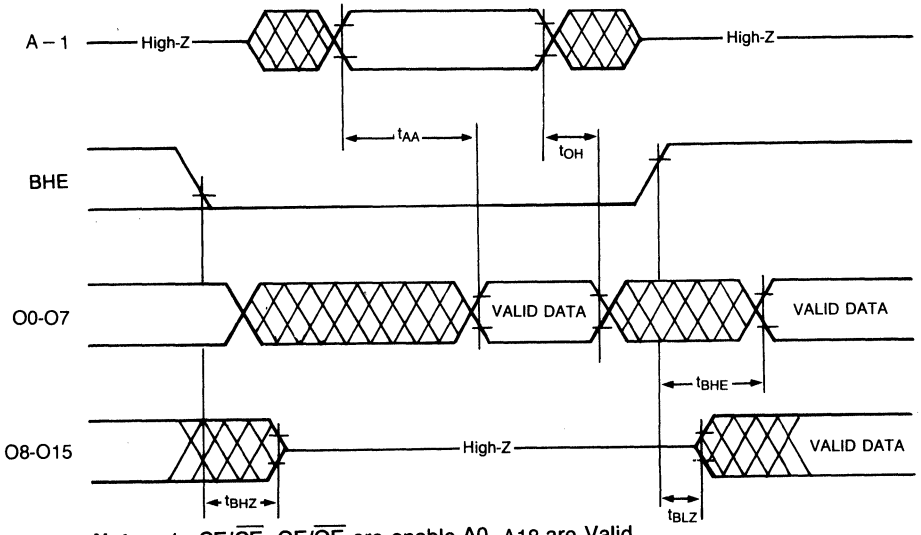
TIMING WAVEFORMS

(1) Word Mode (BHE = V_{IH})/Byte Mode (BHE = V_{IL})



(*1) Byte Mode only. A-1 is Least Significant Bit Address. (BHE = V_{IL})
(*2) Word Mode only. (BHE = V_{IH})

(2) Word Mode, Byte Mode Switch

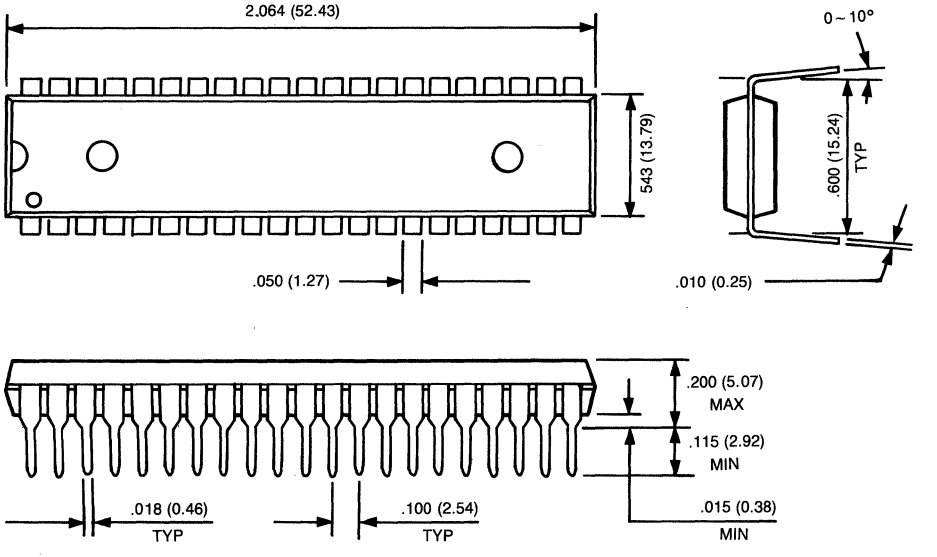


Notes: 1. CE/CE, OE/OE are enable A0 - A18 are Valid.
2. If BHE is high and CE, OE is enable O15/A – 1 pin is in the output state.
3. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

Package Dimensions

42 DIP

Unit: Inches (mm)



GM23C8000

1,048,576×8 BIT CMOS
MASK-PROGRAMMABLE ROM

General Description

The GM23C8000 is a 1048576 words by 8 bits EPROM-Compatible Read-Only-Memory. It is designed to be compatible with all microprocessors and similar applications where high performance large-bit storage and similar interfacing are important design considerations.

The GM23C8000 offers automatic powerdown controlled by the Chip Enable CE/$\overline{CE}$ input. When $\overline{CE}$ goes HIGH (CE goes LOW), the device will automatically power down and remain in a low power standby mode as long as $\overline{CE}$ remains HIGH (CE remains LOW). This feature provides system level power savings as much as 99%. An additional feature of GM23C8000 is the Output Enable. OE functions (may be mask programmed as OE/$\overline{OE}$/NC) in order to eliminate bus contention in multiple bus microprocessor systems.

Pin Description

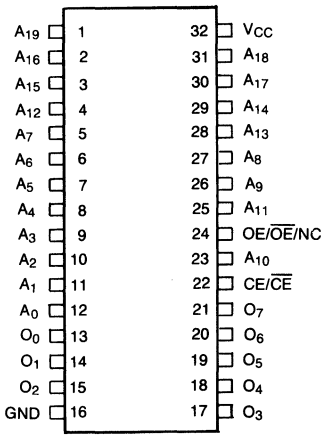
Pin No.	Symbol	Description
3-12, 23 25-29	A0~A15	Address Inputs
13-15, 17-21	O0-O7	Data Output
16	GND	Ground
32	V_{CC}	Power Supply
1	A19	Address Input
22	CE/$\overline{CE}$	Chip Enable Input
2	A16	Address Input
24	OE/$\overline{OE}$/NC	Output Enable
		Address Input
31	A18	Address Input
30	A17	Address Input

Notes
(1) This pin is user-definable as active high or active low.
(2) NC is "No Connection"

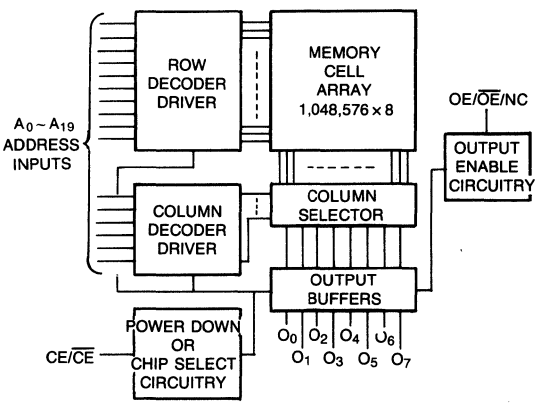
Features

- 1048576×8-bit organization
- Single +5V Power Supply
- Access times: 150 ns (max.)
- Current: Operating: 40 mA (max.)
  Standby: 30 μA (max.)
- 3-state outputs for wired OR expansion
- Fully static operation
- TTL-compatible inputs and outputs
- Mask programmed for CE/$\overline{CE}$, OE or OE or NC
- Available in 32 pin DIP package (GM23C8000) or in 32 pin SOP package (GM23C8000).

Pin Configuration



Block Diagram



Absolute Maximum Ratings*

Symbol	Parameter	Rating	Unit
T_A	Operating Temperature	−10 ~ +80	°C
T_{STG}	Storage Temperature	−65 ~ +150	°C
V_{CC}	Supply Voltage to Ground Potential	−0.5V ~ V_{CC} +0.5	V
V_{OUT}	Output Voltage	−0.5 ~ V_{CC} +0.5	V
V_{IN}	Input Voltage	−0.5 ~ V_{CC} +0.5	V
P_D	Power Dissipation	400	mV

*Comments
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extendes periods may attect device reliability.

Recommended DC Operating Conditions (T_A=0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage	−0.5		0.8	V

DC Electrical Characteristics: (V_{CC}=5.0V ± 10%, GND=0V, T_A=0 to 70°C)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	I_{OH} = −1.0mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2mA			0.4	V
I_{IH}	Input High Voltage		2.2		V_{CC} +0.3	V
V_{IL}	Input Low Voltage		−0.5		0.8	V
$I_{I(L)}$	Input Leakage Current	V_{IN} = 0V to V_{CC}			10	μA
$I_{O(L)}$	Output Leakage Current	V_{OUT} = 0V to V_{CC}			10	μA
I_{CC}	Operating Supply Current	$\overline{CE}$ = V_{IL}, CE = V_{IH}			40	mA
I_{SB}	Standby Supply Current	$\overline{CE}$ = V_{IH}, CE = V_{IL}			1.5	mA
I_{SB1}	Standby Supply Current	$\overline{CE}$ = V_{CC}-0.2V, CE = 0.2V			30	μA

Capacitance:

Symbol	Parameter	Conditions	Min.	Max.	Unit
C_I*	Input Capacitance	T_A = 25°C, f = 1.0MHz		10	pF
C_O*	Output Capacitance			10	pF

*This parameter is periodically sampled and is not 100% tested. All pins except pin under test tied to AC ground.

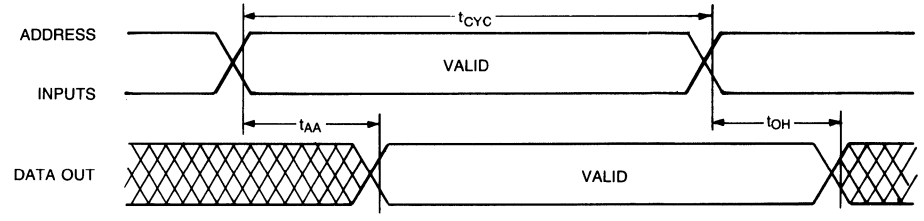
AC Operating Characteristics (T_A = 0°C to +70°C, V_{CC} = 5V ± 10%, GND = 0V)

Symbol	Parameter	GM23C8000		Unit
		Min	Max	
t_{CYC}	Cycle Time	150		ns
t_{AA}	Address Access Time		150	ns
t_{ACE}	Chip Enable Access Time		150	ns
t_{AOE}	Output Enable Access Time		75	ns
t_{OH}	Output Hold After Address Change	10		ns
t_{LZ}	Output Low Z Delay	10		ns
t_{HZ}	Output High Z Delay		85	ns
t_{PU}	Power-Up Time	0		ns
t_{PD}	Power-Down Time		85	ns

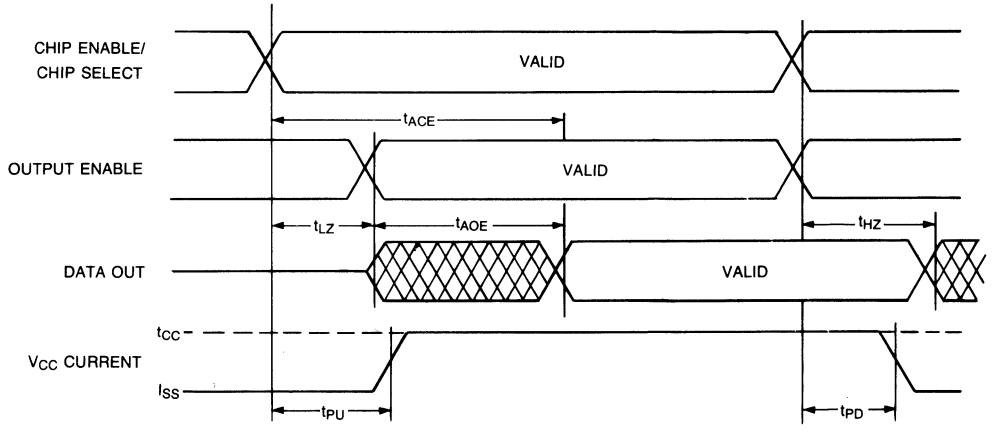
*t_{HZ} is specified from either OE/$\overline{OE}$ or CE/$\overline{CE}$ going disabled whichever occurs first.

Timing Waveforms

Propagation Delay From Address (CE/$\overline{CE}$ going enabled)

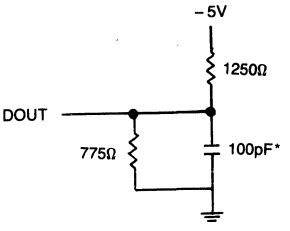


Propagation Delay From Chip Enable or Chip Select or Output Enable (Address Valid)



AC Test Conditions

Input Pulse Levels	0.4 to 2.4V
Input Rise and Fall Time	10ns
Timing Measurement	V_{IL}=0.8V V_{IH}=2.2V
Reference Level	V_{OL}=0.8V V_{OH}=2.0V
Output Load	See Fig. 1



*Including scope and 119

Fig. 1 Output Load Circuit

Truth Table (GM23C8000)

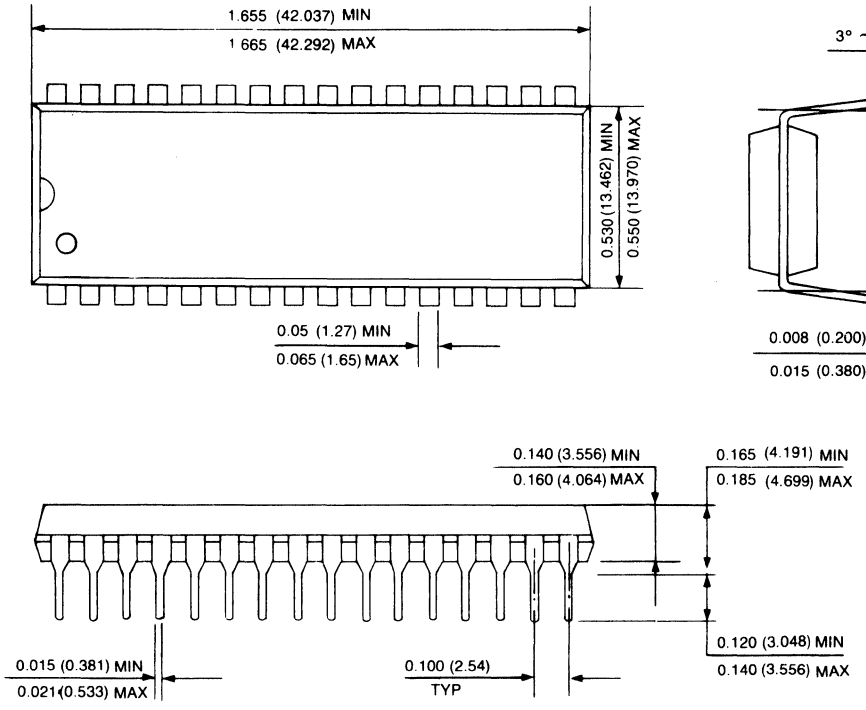
CE/CE	OE/OE	O_0–O_7	Mode
A	A	Output Data	Read
I	X	Hi–Z	Power Down
A	I	Hi–Z	Output Disable

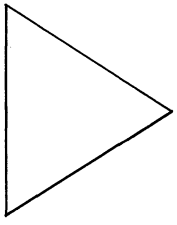
1. CE/CE, OE/OE/NC, are mask programmable which can be selected for active low, active high or no connection.
2. "A" means "Active" "I" means "Inactive" "X" means "Active" or "Inactive".
3. If OE/OE/NC is set to no-connection, the input level will be internally fixed at active level.

Package Dimensions

32 DIP

Unit: inches (mm)





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