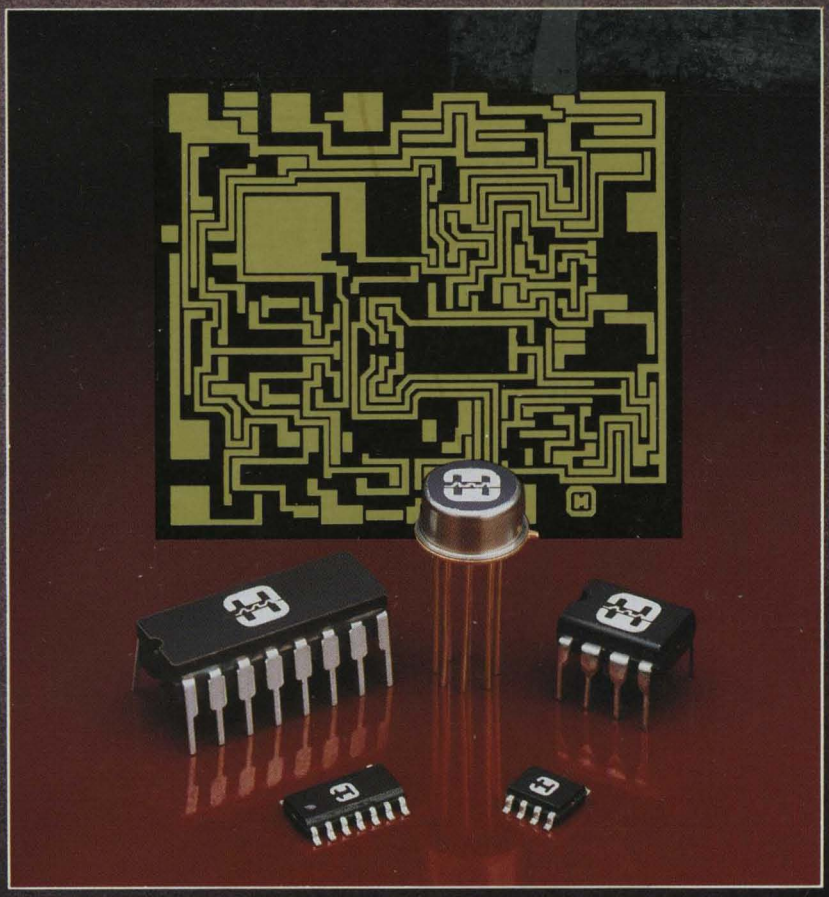

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Commercial Linear Product Cross Reference

DEVICE	HARRIS REPLACEMENT	(NOTE 1) PIN TO PIN	(NOTE 2) EE	HARRIS ADVANTAGE OR COMMENTS
3507J	HA2-2525-5	Yes	I	
3508J	HA2-2625-5	Yes	I	
3551J	HA2-5162-5	*	FE	Reduced Ibias/Greater Bandwidth
3551S	HA2-5160-2	*	FE	Reduced Ibias/Greater Bandwidth
3554AM	HFA1-0001-9	No	FE	Greater Bandwidth/Faster Ts/Lower Cost
3554BM	HFA1-0001-9	No	FE	Greater Bandwidth/Faster Ts/Lower Cost
3554SM	HFA1-0001-9	No	FE	Greater Bandwidth/Faster Ts/Lower Cost
AD301AH	CA0301AT	Yes	I	
AD301AN	CA0301AE	Yes	I	
AD3554AM	HFA1-0001-9	No	FE	Greater Bandwidth/Faster Ts/Lower Cost
AD3554BM	HFA1-0001-9	No	FE	Greater Bandwidth/Faster Ts/Lower Cost
AD3554SM	HFA1-0001-9	No	FE	Greater Bandwidth/Faster Ts/Lower Cost
AD389BD	HA1-5320-2	No	FE	Faster Acquisition/Reduced Droop
AD389KD	HA1-5320-5	No	FE	Faster Acquisition/Reduced Droop
AD507JH	HA2-2625-5	Yes	I	
AD507KH	HA2-2625-5	Yes	FE	
AD507SH	HA2-2620-2	Yes	I	
AD509JH	HA2-2525-5	Yes	I	Substitute HA2-2529-5
AD509KH	HA2-2525-5	Yes	FE	Substitute HA2-2529-5
AD509SH	HA2-2520-2	Yes	I	Substitute HA2-2529-2
AD515AJH	HA2-5180-5	Yes	FE	Enhanced ACs
AD515AKH	HA2-5180-5	Yes	FE	Improved ACs
AD518JH	HA2-2515-5	Yes	I	
AD518JN	HA3-2515-5	Yes	I	
AD518KH	HA2-2515-5	Yes	FE	
AD518SH	HA2-2510-2	Yes	I	
AD539JD	HA1-2547-5	No	FE	Enhanced Bandwidth
AD539KD	HA1-2547-5	No	FE	Enhanced Bandwidth
AD539SD	HA1-2547-9	No	FE	Enhanced Bandwidth
AD542JH	HA1-5170-5	*	FE	Enhanced ACs
AD542KH	HA2-5170-5	*	FE	Enhanced ACs
AD542LH	HA2-5170-5	*	FE	Enhanced ACs
AD542SH	HA2-5170-2	*	FE	Enhanced ACs
AD545JH	HA2-5180-5	Yes	FE	Enhanced ACs
AD54KH	HA2-5180-5	Yes	FE	Enhanced ACs
AD545LH	HA2-5180-5	Yes	FE	Enhanced ACs
AD545MH	HA2-5180-5	Yes	FE	Enhanced ACs
AD5539JN	HA3-2539-5	*	FE	
AD5539JQ	HA1-2539-5	*	FE	
AD5539SQ	HA1-2539-2	*	FE	
AD582KD	HA1-2425-5	No	FE	Faster Acquisition/Enhanced ACs
AD582SD	HA1-2420-2	No	FE	Faster Acquisition/Enhanced ACs
AD583KD	HA1-2425-5	Yes	FE	Faster Acquisition/Greater Iout
AD585AQ	HA1-5320-5	No	FE	Faster Acquisition/Reduced Droop
AD585SQ	HA1-5320-2	No	FE	Faster Acquisition/Reduced Droop
AD590IH	AD590IH	Yes	I	
AD590JH	AD590JH	Yes	I	

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Commercial Linear Product Cross Reference

DEVICE	HARRIS REPLACEMENT	(NOTE 1) PIN TO PIN	(NOTE 2) EE	HARRIS ADVANTAGE OR COMMENTS
AD741CH	CA0741CT	Yes	I	
AD741CN	CA0741CE	Yes	I	
AD741H	CA0741T	Yes	I	
AD821AQ	CA5160AE (PDIP)	*	FE	Reduced Ibias/Enhanced ACs
AD821AS	CA5160AE (PDIP)	*	FE	Reduced Ibias/Enhanced ACs
AD821JN	CA5160AE	*	FE	Reduced Ibias/Enhanced ACs
AD840JN	HA3-2540C-5	Yes	FE	
AD840JQ	HA1-2540C-5	Yes	FE	
AD840KN	HA3-2540-5	Yes	FE	
AD840KQ	HA1-2540-5	Yes	FE	
AD840SQ	HA1-2540-2	Yes	FE	
AD841JH	HA2-2541-5	Yes	FE	
AD841JQ	HA1-2541-5	Yes	FE	
AD841KH	HA2-2541-5	Yes	FE	
AD841KQ	HA1-2541-5	Yes	FE	
AD841SH	HA2-2541-2	Yes	FE	
AD841SQ	HA1-2541-2	Yes	FE	
AD842JH	HA2-2542-5	Yes	FE	
AD842JN	HA3-2542-5	Yes	FE	
AD842JQ	HA1-2542-5	Yes	FE	
AD842KH	HA2-2542-5	Yes	FE	
AD842KN	HA3-2542-5	Yes	FE	
AD842KQ	HA1-2542-5	Yes	FE	
AD842SH	HA2-2542-2	Yes	FE	
AD846AQ	HA1-5004-9	No	FE	Enhanced ACs/Greater Iout
AD846BQ	HA1-5004-9	No	FE	Enhanced ACs/GReater Iout
AD846SQ	HA1-5004-9	No	FE	Enhanced ACs/Greater Iout
AD847JN	HA3-2544C-5	Yes	FE	
AD847SQ	HA7-2544C-2	Yes	FE	
AD9610BH	HA1-5004-9	No	FE	Greater Bandwidth/Lower Cost Monolithic
ADLH0032CG	HA2-2542-5	*	FE	Monolithic/Lower Cost
ADLH0032G	HA2-2542-2	*	FE	Monolithic/Lower Cost
ADLH0033CG	HA2-5033-5	*	FE	Enhanced ACs/Monolithic/Lower Cost
ADLH0033G	HA2-5033-2	*	FE	Enhanced ACs/Monolithic/Lower Cost
ADOP27AH	HA2-5127A-2	Yes	E	Enhanced ACs/Reduced Icc
ADOP27AQ	HA7-5127A-2	Yes	E	Enhanced ACs/Reduced Icc
ADOP27EH	HA2-5127A-5	Yes	E	Enhanced ACs/Reduced Icc
ADOP27EQ	HA7-5127A-5	Yes	E	Enhanced ACs/Reduced Icc
ADOP27GH	HA2-5127-5	Yes	E	Enhanced ACs/Reduced Icc
ADOP27GQ	HA7-5127-5	Yes	E	Enhanced ACs/Reduced Icc
ADOP37AH	HA2-5137A-2	Yes	E	Enhanced ACs/Reduced Icc
ADOP37AQ	HA7-5137A-2	Yes	E	Enhanced ACs/Reduced Icc
ADOP37EH	HA2-5137A-5	Yes	E	Enhanced ACs/Reduced Icc
ADOP37EQ	HA7-5137A-5	Yes	E	Enhanced ACs/Reduced Icc
ADOP37GH	HA2-5137-5	Yes	E	Enhanced ACs/Reduced Icc
ADOP37GQ	HA7-5137-5	Yes	E	Enhanced ACs/Reduced Icc
AM-450-2	HA2-2505-5	Yes	E	Guaranteed DCs/ACs
AM-450-2M	HA2-2502-2	Yes	E	Guaranteed DCs/ACs
AM-452-2	HA2-2525-5	Yes	E	Guaranteed DCs/ACs
AM-452-2M	HA2-2522-2	Yes	E	Guaranteed DCs/ACs

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Commercial Linear Product Cross Reference

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AM-460-2	HA2-2605-5	Yes	E	Guaranteed DCs/ACs
AM-460-2M	HA2-2602-2	Yes	E	Guaranteed DCs/ACs
AM-462-2	HA2-2625-5	Yes	E	Guaranteed DCs/ACs
AM-462-2M	HA2-2620-2	Yes	E	Guaranteed DCs/ACs
AM-7650-1	ICL7650SCPD	Yes	FE	Almost Identical
AM-7650-2	ICL7650SCTV-1	Yes	FE	Almost Identical
BB3554AM	HFA1-0001-9	No	FE	Greater Bandwidth/Faster Ts/Lower Cost
BB3554BM	HFA1-0001-9	No	FE	Greater Bandwidth/Faster Ts/Lower Cost
BB3554SM	HFA1-0001-9	No	FE	Greater Bandwidth/Faster Ts/Lower Cost
CA3054	CA3054	Yes	I	SOIC Version Available
CA3059	CA3059	Yes	I	
CA3079	CA3079	Yes	I	
CA3146P	CA3146E	Yes	I	
CLC400AID	HFA1-0001-9	*	FE	Faster Transient Response
CLC400AJP	HFA3-0001-9	*	FE	Faster Transient Response
CLC401AID	HFA1-0005-9	*	FE	Faster Transient Response
CLC401AJP	HFA3-0005-9	*	FE	Faster Transient Response
EHA1-2539-2	HA1-2539-2	Yes	I	
EHA1-2539-5	HA1-2539-5	Yes	I	
EHA1-2540-2	HA1-2540-2	Yes	I	
EHA1-2540-5	HA1-2540-5	Yes	I	
EHA1-5190-2	HA1-5190-2	Yes	I	
EHA1-5195-5	HA1-5195-5	Yes	I	
EHA2-2500-2	HA2-2500-2	Yes	I	
EHA2-2502-2	HA2-2502-2	Yes	I	
EHA2-2505-5	HA2-2505-5	Yes	I	
EHA2-2510-2	HA2-2510-2	Yes	I	
EHA2-2512-2	HA2-2512-2	Yes	I	
EHA2-2515-5	HA2-2515-5	Yes	I	
EHA2-2520-2	HA2-2520-2	Yes	I	Substitute HA2-2529-2
EHA2-2522-2	HA2-2522-2	Yes	I	Substitute HA2-2529-2
EHA2-2525-5	HA2-2525-5	Yes	I	Substitute HA2-2529-5
EHA2-2600-2	HA2-2600-2	Yes	I	
EHA2-2602-2	HA2-2602-2	Yes	I	
EHA2-2605-5	HA2-2605-5	Yes	I	
EHA2-2620-2	HA2-2620-2	Yes	I	
EHA2-2622-2	HA2-2622-2	Yes	I	
EHA2-2625-5	HA2-2625-5	Yes	I	
EHA2-5190-2	HA2-5190-2	Yes	I	
EHA2-5195-5	HA2-5195-5	Yes	I	
EHA3-2539-5	HA3-2539-5	Yes	I	
EHA3-2540-5	HA3-2540-5	Yes	I	
EHA7-2500-2	HA7-2500-2	Yes	I	
EHA7-2502-2	HA7-2502-2	Yes	I	
EHA7-2505-5	HA7-2505-5	Yes	I	

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DEVICE	HARRIS REPLACEMENT	(NOTE 1) PIN TO PIN	(NOTE 2) EE	HARRIS ADVANTAGE OR COMMENTS
EHA7-2510-2	HA7-2510-2	Yes	I	
EHA7-2512-2	HA7-2512-2	Yes	I	
EHA7-2515-5	HA7-2515-5	Yes	I	
EHA7-2520-2	HA7-2520-2	Yes	I	
EHA7-2522-2	HA7-2522-2	Yes	I	
EHA7-2525-5	HA7-2525-5	Yes	I	
EHA7-2600-2	HA7-2600-2	Yes	I	
EHA7-2602-2	HA7-2602-2	Yes	I	
EHA7-2605-5	HA7-2605-5	Yes	I	
EHA7-2620-2	HA7-2620-2	Yes	I	
EHA7-2622-2	HA7-2622-2	Yes	I	
EHA7-2625-5	HA7-2625-5	Yes	I	
EL2003CH	HA2-5002-5	Yes	FE	Greater Slew Rate/Reduced Icc
EL2003CJ	HA7-5002-5	No	FE	Greater Slew Rate/Reduced Icc
EL2003CN	HA3-5002-5	No	FE	Greater Slew Rate/Reduced Icc
EL2003CPL	HA9P5002-9	No	FE	Greater Slew Rate/Reduced Icc
EL2003H	HA2-5002-2	Yes	FE	Greater Slew Rate/Reduced Icc
EL2003J	HA7-5002-2	No	FE	Greater Slew Rate/Reduced Icc
EL2005CG	HA2-5033-5	*	FE	Greater Bandwidth
EL2005G	HA2-5033-2	*	FE	Greater Bandwidth
EL2020CJ	HA1-5004-5	No	FE	Enhanced ACs/Iout
EL2020J	HA1-5004-9	No	FE	Enhanced ACs/Iout
EL2033CJ	HA7-5002-5	*	FE	Greater Slew Rate/Reduced Icc
EL2033CN	HA3-5002-5	*	FE	Greater Slew Rate/Reduced Icc
EL2033J	HA7-5002-2	*	FE	Greater Slew Rate/Reduced Icc
EL2039CJ	HA1-2539-5	Yes	FE	
EL2039CN	HA3-2539-5	Yes	FE	
EL2039J	HA1-2539-2	Yes	FE	
EL2040CJ	HA1-2540-5	Yes	FE	
EL2040CN	HA3-2540-5	Yes	FE	
EL2040J	HA1-2540-2	Yes	FE	
EL2041CG	HA2-2541-5	Yes	FE	
EL2041CJ	HA1-2541-5	Yes	FE	
EL2041G	HA2-2541-2	Yes	FE	
EL2041J	HA1-2541-2	Yes	FE	
EL2190G	HA2-5190-2	Yes	FE	
EL2190J	HA1-5190-2	Yes	FE	
EL2195CG	HA2-5195-5	Yes	FE	
EL2195CJ	HA1-5195-5	Yes	FE	
ELH0032CG	HA2-2542-5	*	FE	
ELH0032G	HA2-2542-2	*	FE	
ELH0033CG	HA2-5033-5	*	FE	Greater Bandwidth
ELH0033G	HA2-5033-2	*	FE	Greater Bandwidth
HOS-100AH	HA2-5033-2	*	FE	Greater Bandwidth/Lower Cost
HOS-100SH	HA2-5033-2	*	FE	Greater Bandwidth/Lower Cost
HOS050	HA2-2542-2	*	FE	Lower Cost
HOS050A	HA2-2542-2	*	FE	Lower Cost
HOS050C	HA2-2542-2	*	FE	Lower Cost

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DEVICE	HARRIS REPLACEMENT	(NOTE 1) PIN TO PIN	(NOTE 2) EE	HARRIS ADVANTAGE OR COMMENTS
ICL7611ACPA	ICL7611ACPA	Yes	I	
ICL7611ACTV	ICL7611ACTV	Yes	I	
ICL7611AMTV	ICL7611AMTV	Yes	I	
ICL7611BCPA	ICL7611BCPA	Yes	I	
ICL7611BCTV	ICL7611BCTV	Yes	I	
ICL7611BMTV	ICL7611BMTV	Yes	I	
ICL7611DCPA	ICL7611DCPA	Yes	I	
ICL7611DCSA	ICL7611DCBA	Yes	I	
ICL7611DCTV	ICL7611DCTV	Yes	I	
ICL7611DMTV	ICL7611DMTV	Yes	I	
ICL7612ACPA	ICL7612ACPA	Yes	I	
ICL7612ACTV	ICL7612ACTV	Yes	I	
ICL7612AMTV	ICL7612AMTV	Yes	I	
ICL7612BCPA	ICL7612BCPA	Yes	I	
ICL7612BCTV	ICL7612BCTV	Yes	I	
ICL7612BMTV	ICL7612BMTV	Yes	I	
ICL7612DCPA	ICL7612DCPA	Yes	I	
ICL7612DCSA	ICL7612DCBA	Yes	I	
ICL7612DCTV	ICL7612DCTV	Yes	I	
ICL7612DMTV	ICL7612DMTV	Yes	I	
ICL7621ACPA	ICL7621ACPA	Yes	I	
ICL7621ACTV	ICL7621ACTV	Yes	I	
ICL7621AMTV	ICL7621AMTV	Yes	I	
ICL7621BCPA	ICL7621BCPA	Yes	I	
ICL7621BCTV	ICL7621BCTV	Yes	I	
ICL7621BMTV	ICL7621BMTV	Yes	I	
ICL7621DCPA	ICL7621DCPA	Yes	I	
ICL7621DCSA	ICL7621DCBA	Yes	I	
ICL7621DCTV	ICL7621DCTV	Yes	I	
ICL7621DMTV	ICL7621DMTV	Yes	I	
ICL7631CCPE	ICL7631CCPE	Yes	I	
ICL7631ECPE	ICL7631ECPE	Yes	I	
ICL7641CCPD	ICL7641CCPD	Yes	I	
ICL7641ECPD	ICL7641ECPD	Yes	I	
ICL7642CCJD	ICL7642CCJD	Yes	I	
ICL7642CCPD	ICL7642CCPD	Yes	I	
ICL7642CMJD	ICL7642CMJD	Yes	I	
ICL7642ECJD	ICL7642ECJD	Yes	I	
ICL7642ECPD	ICL7642ECPD	Yes	I	
ICL7642EMJD	ICL7642EMJD	Yes	I	
ICL7650BCPA-1	ICL7650SCPA-1	Yes	FE	Reduced Vio/Ibias
ICL7650BCPD	ICL7650SCPD	Yes	FE	Reduced Vio/Ibias
ICL7650BCTV-1	ICL7650SCTV-1	Yes	FE	Reduced Vio/Ibias
ICL7652CPD	ICL7652SCPD	Yes	FE	Greater Slew Rate
ICL7652IJD	ICL7652SIPD	Yes	FE	Greater Slew Rate
ICL7660CPA	ICL7660SCPA	*	E	Reduced Icc
ICL7660CSA	ICL7660SIBA	*	E	Reduced Icc
ICL7660CTV	ICL7660SCTV	*	E	Reduced Icc
ICL7660IJA	ICL7660SIPA (PDIP)	*	E	Reduced Icc
ICL7660ITV	ICL7660SITV	*	E	Reduced Icc
ICL7660SMTV	ICL7660SMTV	*	E	Reduced Icc

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DEVICE	HARRIS REPLACEMENT	(NOTE 1) PIN TO PIN	(NOTE 2) EE	HARRIS ADVANTAGE OR COMMENTS
ICL7663ACPA	ICL7663SACPA	Yes	E	Wider Voltage Range/Reduced Rsat
ICL7663ACSA	ICL7663SCBA	Yes	E	Wider Voltage Range/Reduced Rsat
ICL7663AIJA	ICL7663SACJA	Yes	E	Wider Voltage Range/Reduced Rsat
ICL7663BCPA	ICL7663SCPA	Yes	E	Wider Voltage Range/Reduced Rsat
ICL7663BIJA	ICL7663SIJA	Yes	E	Wider Voltage Range/Reduced Rsat
ICL7663CPA	ICL7663SCPA	Yes	E	Wider Voltage Range/Reduced Rsat
ICL7663CSA	ICL7663SCBA	Yes	E	Wider Voltage Range/Reduced Rsat
ICL7663IJA	ICL7663SIJA	Yes	E	Wider Voltage Range/Reduced Rsat
ICL7665ACJA	ICL7665SACJA	Yes	I	
ICL7665ACPA	ICL7665SACPA	Yes	I	
ICL7665BCPA	ICL7665SCPA	Yes	E	Enhanced Supply Range/Tempco
ICL7665BCSA	ICL7665SCBA	Yes	E	Enhanced Supply Range/Tempco
ICL7665CJA	ICL7665SCJA	Yes	I	
ICL7665CPA	ICL7665SCPA	Yes	I	
ICL7665CSA	ICL7665SCBA	Yes	I	
ICM7242IPA	ICM7242IPA	Yes	FE	
ICM7555IPA	ICM7555IPA	Yes	FE	Wider Operating Voltage Range
ICM7555ITV	ICM7555ITV	Yes	FE	Wider Operating Voltage Range
ICM7555MTV	ICM7555MTV	Yes	FE	Wider Operating Voltage Range
ICM7556IPD	ICM7556IPD	Yes	FE	Wider Operating Supply Range
ICM7556MJD	ICM7556MJD	Yes	FE	Wider Operating Supply Range
KF347ACN	CA3410AE	Yes	FE	Reduced Ibias/Iio
KF347AIN	CA3410AE	Yes	FE	Reduced Ibias/Iio
KF347CN	CA3410E	Yes	FE	Reduced Ibias/Iio
KF347IN	CA3410E	Yes	FE	Reduced Ibias/Iio
KF351N	CA3140E	Yes	FE	Reduced Ibias/Iio
KS272ACN	CA5260AE	Yes	FE	Specified @ +5V Supply
KS272AIN	CA5260AE	Yes	FE	Specified @ +5V Supply
KS272CN	CA5260E	Yes	FE	Specified @ +5V Supply
KS272IN	CA5260E	Yes	FE	Specified @ +5V Supply
KS274CN	CA5470E	Yes	FE	Greater Band Width/Spec. @ +5V Supply
KS274IN	CA5470E	Yes	FE	Greater Band Width/Spec. @ +5V Supply
LF157H	CA3130AT	Yes	FE	Reduced Ibias
LF198AH	HA1-2420-2 (CDIP)	No	FE	Faster Acquisition
LF198H	HA1-2420-2 (CDIP)	No	FE	Faster Acquisition
LF347BN	CA3410AE	Yes	FE	Reduced Ibias
LF347N	CA3410E	Yes	FE	Reduced Ibias
LF351D	CA3140M	Yes	FE	Reduced Ibias/Iio
LF351H	CA3140T	Yes	FE	Reduced Ibias/Iio
LF351M	CA3140M	Yes	FE	Reduced Ibias/Iio
LF351N	CA3140E	Yes	FE	Reduced Ibias/Iio
LF351P	CA3140E	Yes	FE	Reduced Ibias/Iio
LF353N	CA3240E	Yes	FE	Reduced Ibias/Iio
LF353P	CA3240E	Yes	FE	Reduced Ibias/Iio
LF357AH	CA3130AT	Yes	FE	Reduced Ibias
LF357H	CA3130T	Yes	FE	Reduced Ibias/Iio
LF357M	CA3130M	Yes	FE	Reduced Ibias/Iio
LF357N	CA3130E	Yes	FE	Reduced Ibias/Iio

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DEVICE	HARRIS REPLACEMENT	(NOTE 1) PIN TO PIN	(NOTE 2) EE	HARRIS ADVANTAGE OR COMMENTS
LF398AH	HA1-2425-5 (CDIP)	No	FE	Faster Acquisition
LF398AN	HA3-2425-5	No	FE	Faster Acquisition
LF398H (CAN)	HA1-2425-5 (CDIP)	No	FE	Faster Acquisition
LF398N	HA3-2425-5	No	FE	Faster Acquisition
LF400CH	CA3100T	*	FE	Similar ACs
LF411CD	CA3140AM	Yes	FE	Reduced Ibias/Iio
LF411CH	CA3140AT	Yes	FE	Reduced Ibias/Iio
LF411CN	CA3140AE	Yes	FE	Reduced Ibias/Iio
LF411CP	CA3140AE	Yes	FE	Reduced Ibias/Iio
LF411MH	CA3140AT	Yes	FE	Reduced Ibias/Iio
LF412CD	CA3240AE	Yes	FE	Reduced Ibias/Iio
LF412CN	CA3140AE	Yes	FE	Reduced Ibias/Iio
LF412CP	CA3240AE	Yes	FE	Reduced Ibias/Iio
LH0002CH	HA2-5002-5	*	E	Enhanced ACs/DCs/Monolithic
LH0002CN	HA3-5002-5	No	E	Enhanced ACs/DCs/Monolithic
LH0002H	HA2-5002-2	*	E	Enhanced ACs/DCs/Monolithic
LH0022CD	CA3140AE (PDIP)	No	FE	Greater Bandwidth/Slew Rate
LH0022CH	CA3140AT	Yes	FE	Greater Bandwidth/Slew Rate
LH0032ACG	HA2-2542-S	Yes	FE	Monolithic/Lower Cost
LH0032AG	HA2-2542-2	Yes	FE	Monolithic/Lower Cost
LH0032CG	HA2-2542-5	Yes	FE	Monolithic/Lower Cost
LH0032G	HA2-2542-2	Yes	FE	Monolithic/Lower Cost
LH0033ACG	HA2-5033-5	*	FE	Greater Bandwidth/Monolithic/Lower Cost
LH0033AG	HA2-5033-2	*	FE	Monolithic/Lower Cost
LH0033CG	HA2-5033-5	*	FE	Greater Bandwidth/Monolithic/Lower Cost
LH0033CJ	HA3-5033-5	*	FE	Monolithic/Lower Cost
LH0033G	HA2-5033-2	*	FE	Monolithic/Lower Cost
LH0042CD	CA3140E (PDIP)	No	FE	Greater Bandwidth/Slew Rate
LH0042CD	CA3140T	Yes	FE	Greater Bandwidth/Slew Rate
LH4004CD	HA1-5004-5	No	FE	Monolithic/Lower Cost
LH4004D	HA1-5004-9	No	FE	Monolithic/Lower Cost
LH4161CH	HA2-2544-5	No	FE	PDIP Substitute is HA3-2544C-5
LH4161CJ	HA7-2544-5	No	FE	
LH4161H	HA2-2544-2	No	FE	
LH4161J	HA7-2544-2	No	FE	
LM101H	CA0101T	Yes	I	
LM124J	CA0124E (PDIP)	Yes	I	
LM139AJ	CA0139AF	Yes	I	
LM139DG	CA0139F	Yes	I	
LM139J	CA0139F	Yes	I	
LM143H	HA2-2640-2	*	FE	Enhanced ACs
LM1458DP	CA1458E	Yes	I	
LM1458H	CA1458T/LM1458H	Yes	I	
LM1458N	CA1458E/LM1458N	Yes	I	
LM1524DJ	CA1524F	Yes	I	
LM1558H	CA1558T/LM1558H	Yes	I	

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Commercial Linear Product Cross Reference

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LM158AH	CA0158AT	Yes	I	
LM158H	CA0158T	Yes	I	
LM193H	CA3290AT	Yes	FE	MOSFET Input
LM201H	CA0201T/LM201H	Yes	I	
LM224D	CA0224M	Yes	FE	
LM224J	CA0224E (PDIP)	Yes	FE	
LM224N	CA0224E	Yes	FE	
LM239AD	CA0239AM	Yes	I	
LM239AJ	CA0239AF	Yes	I	
LM239AN	CA0239AE	Yes	I	
LM239D	CA0239M	Yes	I	
LM239DG	CA0239F	Yes	I	
LM239DP	CA0239E	Yes	I	
LM239FP	CA0239M	Yes	I	
LM239J	CA0239F	Yes	I	
LM239N	CA0239E	Yes	I	
LM2524DN	CA2524E	Yes	I	
LM258AH	CA0258AT	Yes	I	
LM258D	CA0258M	Yes	I	
LM258H	CA0258T	Yes	I	
LM258N	CA0258E	Yes	I	
LM258PM	CA0258E	Yes	I	
LM2901D	LM2901M	Yes	I	
LM2901M	LM2901M	Yes	I	
LM2901N	CA3290AE	Yes	FE	MOSFET Input
LM2902D	LM2902M	Yes	FE	
LM2902N	LM2902N	Yes	FE	
LM2903N	CA3290AE	Yes	FE	MOSFET Input
LM2904D	CA2904M	Yes	I	
LM2904M	CA2904M	Yes	I	
LM2904N	CA2904E/LM2904N	Yes	I	
LM2904PM	CA2904E	Yes	I	
LM293H	CA3290AT	Yes	FE	MOSFET Input
LM301ADP	CA0301AE	Yes	I	
LM301AH	CA0301AT/LM301AH	Yes	I	
LM301AHD	CA0301AEX	Yes	I	
LM301AN	CA0301AE/LM301AN	Yes	I	
LM301AND	CA0301AEX	Yes	I	
LM301AP	CA0301AE	Yes	I	
LM3045J	CA3045	Yes	I	
LM3046D	CA3046M	Yes	FE	
LM3046N	CA3046E	Yes	I	
LM3080AN	CA3080AE	Yes	FE	
LM3080N	CA3080E	Yes	FE	
LM3086J	CA3086F	Yes	I	
LM3086M	CA3086M	Yes	I	
LM3086N	CA3086	Yes	I	

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Commercial Linear Product Cross Reference

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LM311H	CA0311T/LM311H	Yes	I	
LM311N	CA0311E/LM311N	Yes	I	
LM311ND	CA0311EX	Yes	I	
LM311PM	CA0311E	Yes	I	
LM3146M	CA3146M	Yes	I	Enhanced "A" Version Offered
LM3146N	CA3146E	Yes	I	Enhanced "A" Version Offered
LM324D	CA0324M	Yes	I	
LM324M	CA0324M	Yes	I	
LM324N	CA0324E/LM324N	Yes	I	
LM3302M	LM3302M	Yes	I	
LM3302N	CA3290E/LM3302N	Yes	I	
LM339AD	CA0339AM	Yes	I	
LM339ADP	CA0339AE	Yes	I	
LM339AFP	CA0339AM	Yes	I	
LM339AN	CA0339AE/LM339AN	Yes	I	
LM339D	CA0339M	Yes	I	
LM339DG	CA0339F	Yes	I	
LM339DP	CA0339E	Yes	I	
LM339FP	CA0339M	Yes	I	
LM339M	CA0339M	Yes	I	
LM339N	CA0339E/LM339N	Yes	I	
LM3401N	CA3401E	Yes	E	Greater Bandwidth
LM343H	HA2-2645-5	*	FE	Enhanced ACs
LM3524DN	CA3524E	Yes	I	
LM3524J	CA3524F	Yes	I	
LM3524N	CA3524E	Yes	I	
LM358AH	CA0358AT	Yes	I	
LM358AM	CA0358AM	Yes	I	
LM358AN	CA0358AE	Yes	I	
LM358D	CA0358M	Yes	I	
LM358H	CA0358T	Yes	I	
LM358M	CA0358M	Yes	I	
LM358N	CA0358E/LM358N	Yes	I	
LM358PM	CA0358E	Yes	I	
LM393H	CA3290AT	Yes	FE	MOSFET Input
LM393N	CA3290AE	Yes	FE	MOSFET Input
LM4250CH	LM4250CH	Yes	I	
LM4250CJ	LM4250CJ	Yes	I	
LM4250CN	LM4250CN	Yes	I	
LM4250H	LM4250H	Yes	FE	Almost Identical
LM4250J	LM4250J	Yes	FE	Almost Identical
LM555CH	CA0555CT/LM555CH	Yes	I	
LM555CM	CA0555CM	Yes	I	
LM555CN	CA0555CE/LM555CN	Yes	I	
LM555H	CA0555T	Yes	I	Guaranteed Drift/Accuracy
LM556CN	ICM7556IPD	Yes	FE	CMOS/Reduced Icc
LM604ACM	HA9P2406-5	No	FE	Enhanced ACs
LM604ACN	HA3-2406-5	No	FE	Enhanced ACs
LM604AMJ	HA1-2400-2	No	FE	Enhanced ACs
LM604CM	HA9P2406-5	No	FE	Enhanced ACs
LM604CN	HA3-2406-5	No	FE	Enhanced ACs

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LM6118J	HA7-5222-9	Yes	FE	Lower Vio
LM6161J	HA7-2544-2	*	FE	Guaranteed Differential Phase/Gain
LM6164J	HA1-5190-2	No	FE	Reduced Voltage Noise
LM6165J	HA1-2540-2	No	FE	Enhanced Slew Rate/Avol
LM6218AH LM6218AJ	HA2-5222-9 HA7-5222-9	No Yes	FE FE	Lower Vio Lower Vio
LM6361N	HA3-2544C-5	*	FE	Guaranteed Differential Phase/Gain
LM6364N	HA1-5195-5	No	FE	Reduced Voltage Noise
LM6365N	HA3-2540C-5	No	FE	Enhanced Slew Rate/Avol
LM723CH LM723CN LM723H	CA0723CT CA0723CE CA0723T/LM723H	Yes Yes Yes	I I I	
LM741CH LM741CN LM741H LM741PM	CA0741CT/LM741CH CA0741CE/LM741CN CA0741T/LM741H CA0741E	Yes Yes Yes Yes	I I I I	
LM747CH LM747CN LM747H	CA0747CT CA0747CE CA0747T	Yes Yes Yes	I I I	
LM748CH LM748CN LM748H LM748PM	CA0748CT/LM748CH CA0748CE CA0748T/LM748H CA0748E	Yes Yes Yes Yes	I I I I	
LMC555CH LMC555CM LMC555CN	ICM7555ITV ICM7555CBA ICM7555IPA	Yes Yes Yes	FE FE FE	Reduced Icc/Wider Supply Range Reduced Icc/Wider Supply Range Reduced Icc/Wider Supply Range
LMC668ACJ LMC668ACJ-8 LMC668ACN LMC668ACN-8	ICL7650SIJD ICL7650SIJA-1 ICL7650SIPD ICL7650SCPA-1	Yes Yes Yes Yes	E E E E	Enhanced DCs Enhanced DCs Enhanced DCs Enhanced DCs
LS204AT LS204CB LS204CM LS204CT LS204T	HA2-5102-2 HA3-5102-5 HA9P-5102-5 HA2-5102-5 HA2-5102-2	Yes Yes Yes Yes Yes	FE FE FE FE FE	Reduced Noise Voltage Reduced Noise Voltage Reduced Noise Voltage Reduced Noise Voltage Reduced Noise Voltage
LS404CB LS404CM LS404M	HA3-5104-5 HA9P-5104-5 HA9P-5104-9	Yes	FE FE FE	Reduced Noise Voltage Reduced Noise Voltage Reduced Noise Voltage
LS776CB LS776T	CA3440AE CA3440AT	Yes Yes	FE FE	MOS Input MOS Input
LT1001CH LT1001CJ8 LT1001MH LT1001MJ8	HA2-5177-5 HA7-5177-5 HA2-5177-2 HA7-5177-2	Yes Yes Yes Yes	FE FE FE FE	Enhanced ACs/Reduced Icc Enhanced ACs/Reduced Icc Enhanced ACs/Reduced Icc Enhanced ACs/Reduced Icc
LT1014ACJ LT1014AMJ LT1014CJ LT1014MJ	HA1-5134A-5 HA1-5134A-2 HA1-5134-5 HA1-5134-2	Yes Yes Yes Yes	FE FE FE FE	Reduced Vio/Enhanced ACs Reduced Vio/Enhanced ACs Reduced Vio/Enhanced ACs Reduced Vio/Enhanced ACs

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LT1022CH	HA2-5160-5	*	FE	Greater Bandwidth/Slew Rate
LT1022MH	HA2-5160-2	*	FE	Greater Bandwidth/Slew Rate
LT1037ACH	HA2-5137A-5	Yes	FE	Enhanced ACs/Reduced Icc
LT1037ACJ8	HA7-5137A-5	Yes	FE	Enhanced ACs/Reduced Icc
LT1037AMH	HA2-5137A-2	Yes	FE	Enhanced ACs/Reduced Icc
LT1037AMJ8	HA7-5137A-2	Yes	FE	Enhanced ACs/Reduced Icc
LT1037CH	HA2-5137-5	Yes	FE	Enhanced ACs/Reduced Icc
LT1037CJ8	HA7-5137-5	Yes	FE	Enhanced ACs/Reduced Icc
LT1037MH	HA2-5137-2	Yes	FE	Enhanced ACs/Reduced Icc
LT1037MJ8	HA7-5137-2	Yes	FE	Enhanced ACs/Reduced Icc
LT1055CH	HA2-5170-5	Yes	FE	Reduced Vio/Icc/Enhanced ACs
LT1055CN8	HA7-5170-5 (CDIP)	Yes	FE	Reduced Vio/Icc/Enhanced ACs
LT1055MH	HA2-5170-2	Yes	FE	Reduced Vio/Icc/Enhanced ACs
LT1056CH	HA2-5170-5	Yes	FE	Reduced Vio/Icc/Enhanced ACs
LT1056CN8	HA7-5170-5 (CDIP)	Yes	FE	Reduced Vio/Icc/Enhanced ACs
LT1056MH	HA2-5170-2	Yes	FE	Reduced Vio/Icc/Enhanced ACs
LT1524J	CA1524F	Yes	I	
LT3524J	CA3524F	Yes	I	
LT3524N	CA3524E	Yes	I	
LTC1044CH	ICL7660SITV	Yes	E	Reduced Icc/Wider Voltage Range
LTC1044CN8	ICL7660SIPA	Yes	E	Reduced Icc/Wider Voltage Range
LTC1044MH	ICL7660SMTV	Yes	E	Reduced Icc/Wider Voltage Range
LTC1052CJ	ICL7652SIJD	Yes	FE	Reduced Voltage Noise
LTC1052CN	ICL7652SIPD	Yes	FE	Reduced Voltage Noise
MA723CN	CA0723CE	Yes	I	
MA747CN	CA0747CE	Yes	I	
MA747N	CA0747E	Yes	I	
MA748CP	CA0748CE	Yes	I	
MAX460IGC	HA2-5033-5	*	FE	Greater Bandwidth
MAX460MGC	HA2-5033-2	*	FE	Greater Bandwidth
MAX610CP	HV3-1205/2405E-5	No	FE	Guaranteed Surge Protection
MAX611CP	HV3-1205/2405E-5	No	FE	Guaranteed Surge Protection
MAX612CP	HV3-1205/2405E-5	No	FE	Guaranteed Surge Protection
MAX663CPA	ICL7663SACPA	*	FE	Reduced Icc/Greater Voltage Range
MAX663CSA	ICL7663SCBA	*	FE	Reduced Icc/Greater Voltage Range
MAX663EJA	ICL7663SAIJA	*	FE	Reduced Icc/Greater Voltage Range
MAX663EPA	ICL7663SAIPA	*	FE	Reduced Icc/Greater Voltage Range
MAX663ESA	ICL7663SIBA	*	FE	Reduced Icc/Greater Voltage Range
MAX8211CPA	ICL8211CPA	Yes	FE	Bipolar/Wider Supply Range
MAX8211CSA	ICL8211CBA	Yes	FE	Bipolar/Wider Supply Range
MAX8211CTY	ICL8211CTY	Yes	FE	Bipolar/Wider Supply Range
MAX8212CPA	ICL8212CPA	Yes	FE	Bipolar/Wider Supply Range
MAX8212CSA	ICL8212CBA	Yes	FE	Bipolar/Wider Supply Range
MAX8212CTY	ICL8212CTY	Yes	FE	Bipolar/Wider Supply Range
MC1445P1D	CA0555CEX	Yes	I	
MC1455D	CA0555CM	Yes	I	
MC1455G	CA0555CT	Yes	I	
MC1455P1	CA0555CE	Yes	I	

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MC1458CD	CA1458M	Yes	I	
MC1458CN	CA1458E	Yes	I	
MC1458G	CA1458T	Yes	I	
MC1458N	CA1458E	Yes	FE	
MC1458P1	CA1458E	Yes	I	
MC1558G	CA1558T	Yes	I	
MC1558GDS	CA1558TX	Yes	I	
MC1558N	CA1558E	Yes	FE	
MC1723CG	CA0723CT	Yes	I	
MC1723CGD	CA0723CTX	Yes	I	
MC1723CP	CA0723CE	Yes	I	
MC1723CPD	CA0723CEX	Yes	I	
MC1723G	CA0723T	Yes	I	
MC1723GD	CA0723TX	Yes	I	
MC1741CG	CA0741CT	Yes	I	
MC1741CP1	CA0741CE	Yes	I	
MC1741CP1D	CA0741CEX	Yes	I	
MC1741G	CA0741T	Yes	I	
MC1776CD	ICL7611DCBA	Yes	FE	Lower Power Drain
MC1776CG	ICL7611BCTV	Yes	FE	Lower Power Drain
MC1776CP1	ICL7611BCPA	Yes	FE	Lower Power Drain
MC1776G	ICL7611BMTV	Yes	FE	Lower Power Drain
MC3302N	CA3290E	Yes	FE	MOSFET Input
MC3302P	LM3302N	Yes	I	
MC3303D	CA5470M	Yes	FE	MOS Input/Enhanced ACs
MC3303N	CA5470E	Yes	FE	MOS Input/Enhanced ACs
MC33071P	CA3140AE	Yes	FE	Reduced Ibias/Iio
MC33072P	CA3240AE	Yes	FE	Reduced Ibias/Iio
MC33074P	CA3410AE	Yes	FE	Reduced Ibias/Iio
MC34001BG	CA3140AT	Yes	FE	Reduced Ibias/Iio
MC34001BP	CA3140AE	Yes	FE	Reduced Ibias/Iio
MC34001G	CA3140T	Yes	FE	Reduced Ibias/Iio
MC34001P	CA3140E	Yes	FE	Reduced Ibias/Iio
MC34002BG	CA3240AT	Yes	FE	Reduced Ibias/Iio
MC34002BP	CA3240AE	Yes	FE	Reduced Ibias/Iio
MC34002G	CA3240T	Yes	FE	Reduced Ibias/Iio
MC34002P	CA34002E	Yes	FE	Reduced Ibias/Iio
MC3401P	CA3401E	Yes	FE	Greater Bandwidth
MC3403D	CA5470M	Yes	FE	MOS Input/Enhanced ACs
MC3403N	CA5470E	Yes	FE	MOS Input/Enhanced ACs
MC34071P	CA3140AE	Yes	FE	Reduced Ibias/Iio
MC34072P	CA3240AE	Yes	FE	Reduced Ibias/Iio
MC34074P	CA3410AE	Yes	FE	Reduced Ibias/Iio
MC3456L	ICM7556MJD	Yes	FE	CMOS/Reduced Icc
MC3456P	ICM7556IPD	Yes	FE	CMOS/Reduced Icc
MC3556L	ICM7556MJD	Yes	FE	CMOS/Reduced Icc
NE5230N	CA5160AE	No	FE	MOS Input

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NE5532AFE	HA7-5102-5	Yes	FE	Enhanced DCs/Reduced Icc
NE5532AN	HA3-5102-5	Yes	FE	Enhanced DCs/Reduced Icc
NE5532FE	HA7-5102-5	Yes	FE	Enhanced DCs/Reduced Icc
NE5532N	HA3-5102-5	Yes	FE	Enhanced DCs/Reduced Icc
NE5534AFE	HA7-5101-5	*	FE	Enhanced DCs
NE5534AN	HA3-5101-5	*	FE	Enhanced DCs
NE5534FE	HA7-5101-5	*	FE	Enhanced DCs
NE5534N	HA3-5101-5	*	FE	Enhanced DCs
NE5539D	HA9P-2539-5	*	FE	Specified @ ±15V Supplies
NE5539F	HA1-2539-5	*	FE	Specified @ ±15V Supplies
NE5539N	HA3-2539-5	*	FE	Specified @ ±15V Supplies
NE555D	CA0555CM	Yes	FE	
NE555DP	CA0555E	Yes	I	
NE555FP	CA0555M	Yes	I	
NE555N	CA0555CE/NE555N	Yes	FE	NE555N Brand Offered
NE556-1N	ICM7556IPD	Yes	FE	CMOS/Reduced Icc
NE556N	ICM7556IPD	Yes	FE	CMOS/Reduced Icc
OP-15CH	CA3140AT	Yes	FE	Reduced Ibias/Iio
OP-15GN8	CA3140AE	Yes	FE	Reduced Ibias/Iio
OP11AY	HA1-5134-2	Yes	FE	Enhanced ACs
OP11EY	HA1-5134-5	Yes	FE	Enhanced ACs
OP11FY	HA1-5104-5	Yes	FE	Enhanced ACs
OP20CJ	HA2-5141-2	Yes	FE	Enhanced ACs
OP20CZ	HA7-5141-2	Yes	FE	Enhanced ACs
OP20HJ	HA2-5141-5	Yes	FE	Enhanced ACs
OP20HP	HA3-5141-5	Yes	FE	Enhanced ACs
OP20HZ	HA7-5141-5	Yes	FE	Enhanced ACs
OP215GZ	CA3240AE (PDIP)	Yes	FE	
OP21GJ	HA2-5151-5	Yes	FE	Enhanced ACs
OP21GP	HA3-5151-5	Yes	FE	Enhanced ACs
OP220CJ	HA2-5142-2	Yes	FE	Enhanced ACs
OP220CZ	HA7-5142-2	Yes	FE	Enhanced ACs
OP220GJ	HA2-5142-5	Yes	FE	Enhanced ACs
OP220GZ	HA7-5142-5	Yes	FE	Enhanced ACs
OP221CJ	HA2-5152-2	Yes	FE	Enhanced ACs
OP221GJ	HA2-5152-5	Yes	FE	Enhanced ACs
OP221GZ	HA7-5152-5	Yes	FE	Enhanced ACs
OP22AJ	HA2-2720-2	Yes	FE	
OP22AZ	HA7-2720-2	Yes	FE	
OP22EJ	HA2-2725-5	Yes	FE	
OP22EZ	HA7-2725-5	Yes	FE	
OP22FZ	HA7-2725-5	Yes	FE	
OP22HZ	HA7-2725-5	Yes	FE	
OP271AZ	HA7-5102-2	Yes	FE	Lower Voltage Noise/Greater Bandwidth
OP271EZ	HA7-5102-5	Yes	FE	Lower Voltage Noise/Greater Bandwidth
OP271FZ	HA7-5102-5	Yes	FE	Lower Voltage Noise/Greater Bandwidth
OP271GP	HA3-5102-5	Yes	FE	Lower Voltage Noise/Greater Bandwidth
OP271GS	HA9P-5102-9	Yes	FE	Lower Voltage Noise/Greater Bandwidth

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OP27AH	HA2-5127A-2	Yes	E	Enhanced ACs/Reduced Icc
OP27AJ	HA2-5127A-2	Yes	E	Enhanced ACs/Reduced Icc
OP27AJ8	HA7-5127A-2	Yes	E	Enhanced ACs/Reduced Icc
OP27AZ	HA7-5127A-2	Yes	E	Enhanced ACs/Reduced Icc
OP27CH	HA2-5127-2	Yes	E	Enhanced ACs/Reduced Icc
OP27CJ	HA2-5127-2	Yes	E	Enhanced ACs/Reduced Icc
OP27CJ8	HA7-5127-2	Yes	E	Enhanced ACs/Reduced Icc
OP27CZ	HA7-5127-2	Yes	E	Enhanced ACs/Reduced Icc
OP27EH	HA2-5127A-5	Yes	E	Enhanced ACs/Reduced Icc
OP27EJ	HA2-5127A-5	Yes	E	Enhanced ACs/Reduced Icc
OP27EJ8	HA7-5127A-5	Yes	E	Enhanced ACs/Reduced Icc
OP27EZ	HA7-5127A-5	Yes	E	Enhanced ACs/Reduced Icc
OP27GH	HA2-5127-5	Yes	E	Enhanced ACs/Reduced Icc
OP27GJ	HA2-5127-5	Yes	E	Enhanced ACs/Reduced Icc
OP27GJ8	HA7-5127-5	Yes	E	Enhanced ACs/Reduced Icc
OP27GZ	HA7-5127-5	Yes	E	Enhanced ACs/Reduced Icc
OP37AH	HA2-5137A-2	Yes	E	Enhanced ACs/Reduced Icc
OP37AJ	HA2-5137A-2	Yes	E	Enhanced ACs/Reduced Icc
OP37AJ8	HA7-5137A-2	Yes	E	Enhanced ACs/Reduced Icc
OP37AZ	HA7-5137A-2	Yes	E	Enhanced ACs/Reduced Icc
OP37CH	HA2-5137-2	Yes	E	Enhanced ACs/Reduced Icc
OP37CJ	HA2-5137-2	Yes	E	Enhanced ACs/Reduced Icc
OP37CJ8	HA7-5137-2	Yes	E	Enhanced ACs/Reduced Icc
OP37CZ	HA7-5137-2	Yes	E	Enhanced ACs/Reduced Icc
OP37EH	HA2-5137A-5	Yes	E	Enhanced ACs/Reduced Icc
OP37EJ	HA2-5137A-5	Yes	E	Enhanced ACs/Reduced Icc
OP37EJ8	HA7-5137A-5	Yes	E	Enhanced ACs/Reduced Icc
OP37EZ	HA7-5137A-5	Yes	E	Enhanced ACs/Reduced Icc
OP37GH	HA2-5137-5	Yes	E	Enhanced ACs/Reduced Icc
OP37GJ	HA2-5137-5	Yes	E	Enhanced ACs/Reduced Icc
OP37GJ8	HA7-5137-5	Yes	E	Enhanced ACs/Reduced Icc
OP37GZ	HA7-5137-5	Yes	E	Enhanced ACs/Reduced Icc
OP400AY	HA1-5134A-2	Yes	FE	
OP400EY	HA1-5134A-5	Yes	FE	
OP400FY	HA1-5134-5	Yes	FE	
OP41EJ	CA3193AT	Yes	FE	Reduced Vio/Noise Voltage
OP41FJ	CA3193T	Yes	FE	Reduced Vio/Noise Voltage
OP41GP	CA3193E	Yes	FE	Reduced Vio/Noise Voltage
OP420BY	HA1-5144-2	Yes	FE	Enhanced ACs
OP420CY	HA1-5144-2	Yes	FE	Enhanced ACs
OP420HY	HA1-5144-5	Yes	FE	Enhanced ACs
OP421BY	HA1-5154-2	Yes	FE	Enhanced ACs
OP421CY	HA1-5154-2	Yes	FE	Reduced Icc/Greater Bandwidth
OP421HY	HA1-5154-5	Yes	FE	Reduced Icc/Greater Bandwidth
OP42AJ	HA2-5170-2	Yes	FE	Enhanced DCs
OP42AZ	HA7-5170-2	Yes	FE	Enhanced DCs
OP42EJ	HA2-5170-5	Yes	FE	Enhanced DCs
OP42EZ	HA7-5170-5	Yes	FE	Enhanced DCs
OP42FJ	HA2-5170-5	Yes	FE	Enhanced DCs
OP42FZ	HA7-5170-5	Yes	FE	Enhanced DCs
OP43BJ	HA2-5180-2	*	FE	Reduced Ibias/Greater Bandwidth
OP43GP	HA7-5180-5	*	FE	Reduced Ibias/Greater Bandwidth

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Commercial Linear Product Cross Reference

DEVICE	HARRIS REPLACEMENT	(NOTE 1) PIN TO PIN	(NOTE 2) EE	HARRIS ADVANTAGE OR COMMENTS
OP470AY	HA1-5104-2	Yes	FE	
OP470EY	HA1-5104-5	Yes	FE	
OP470FY	HA1-5104-5	Yes	FE	
OP470GP	HA3-5104-5	Yes	FE	
OP470GS	HA9P5104-5	Yes	FE	
OP47AD	HA7-5147A-2	Yes	E	Greater Bandwidth/Min Acl=10
OP47AT	HA2-5147A-2	Yes	E	Greater Bandwidth/Min Acl=10
OP47CD	HA7-5147-2	Yes	E	Greater Bandwidth/Min Acl=10
OP47CT	HA2-5147-2	Yes	E	Greater Bandwidth/Min Acl=10
OP47EN	HA7-5147A-5 (CDIP)	Yes	E	Greater Bandwidth/Min Acl=10
OP47GN	HA7-5147-5 (CDIP)	Yes	E	Greater Bandwidth/Min Acl=10
OP62AJ	HA2-5221-9	*	FE	Greater Slew Rate
OP62AZ	HA7-5221-9	*	FE	Greater Slew Rate
OP62EJ	HA2-5221-9	*	FE	Greater Slew Rate
OP62EZ	HA7-5221-9	*	FE	Greater Slew Rate
OP62FJ	HA2-5221-9	*	FE	Greater Slew Rate
OP62FZ	HA7-5221-9	*	FE	Greater Slew Rate
OP63AJ	HA2-5221-9	*	FE	Reduced Vio
OP63AZ	HA7-5221-9	*	FE	Reduced Vio
OP63EJ	HA2-5221-9	*	FE	Reduced Vio
OP63EZ	HA7-5221-9	*	FE	Reduced Vio
OP63FJ	HA2-5221-9	*	FE	Reduced Vio
OP63FZ	HA7-5221-9	*	FE	Reduced Vio
OP64AJ	HA2-5221-9	*	FE	Reduced Vio
OP64AZ	HA7-5221-9	*	FE	Reduced Vio
OP64EJ	HA2-5221-9	*	FE	Reduced Vio
OP64EZ	HA7-5221-9	*	FE	Reduced Vio
OP64FJ	HA2-5221-9	*	FE	Reduced Vio
OP64FZ	HA7-5221-9	*	FE	Reduced Vio
OP65AJ	HA2-2548-9	*	FE	Lower Vio/Guaranteed Ts
OP65AZ	HA7-2548-9	*	FE	Lower Vio/Guaranteed Ts
OP65EJ	HA2-2548-9	*	FE	Lower Vio/Guaranteed Ts
OP65EZ	HA7-2548-9	*	FE	Lower Vio/Guaranteed Ts
OP65FJ	HA2-2548-9	*	FE	Lower Vio/Guaranteed Ts
OP65FZ	HA7-2548-9	*	FE	Lower Vio/Guaranteed Ts
OP65GP	CA3450E	No	FE	Greater Bandwidth /Slew Rate
OP77BJ	HA2-5177-2	Yes	FE	Greater Bandwidth/Reduced Icc
OP77BZ	HA7-5177-2	Yes	FE	Greater Bandwidth/Reduced Icc
OP77FJ	HA2-5177-5	Yes	FE	Greater Bandwidth/Reduced Icc
OP77FZ	HA7-5177-5	Yes	FE	Greater Bandwidth/Reduced Icc
OP80FJ	CA5420AT	*	FE	Single Supply Operation
OP80GJ	CA5420T	*	FE	Single Supply Operation
OP80GP	CA5420E	*	FE	Single Supply Operation
OPA111AM	HA2-5180-5	Yes	FE	Reduced Ibias/Enhanced ACs
OPA111BM	HA2-5180-5	Yes	FE	Enhanced ACs
OPA111SM	HA2-5180-2	Yes	FE	Reduced Ibias/Enhanced ACs
OPA121KP	CA3140AE	*	FE	MOS Input/Enhanced ACs
OPA2111KM	HA2-5102-5	Yes	FE	Greater Bandwidth
OPA2111KP	HA3-5102-5	Yes	FE	Greater Bandwidth

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OPA27AJ	HA2-5127A-2	Yes	E	Enhanced ACs/Reduced Icc
OPA27AZ	HA7-5127A-2	Yes	E	Enhanced ACs/Reduced Icc
OPA27CJ	HA2-5127-2	Yes	E	Enhanced ACs/Reduced Icc
OPA27CZ	HA7-5127-2	Yes	E	Enhanced ACs/Reduced Icc
OPA27EJ	HA2-5127A-5	Yes	E	Enhanced ACs/Reduced Icc
OPA27EZ	HA7-5127A-5	Yes	E	Enhanced ACs/Reduced Icc
OPA27GJ	HA2-5127-5	Yes	E	Enhanced ACs/Reduced Icc
OPA27GZ	HA7-5127-5	Yes	E	Enhanced ACs/Reduced Icc
OPA37AJ	HA2-5137A-2	Yes	E	Enhanced ACs/Reduced Icc
OPA37AZ	HA7-5137A-2	Yes	E	Enhanced ACs/Reduced Icc
OPA37CJ	HA2-5137-2	Yes	E	Enhanced ACs/Reduced Icc
OPA37CZ	HA7-5137-2	Yes	E	Enhanced ACs/Reduced Icc
OPA37EJ	HA2-5137A-5	Yes	E	Enhanced ACs/Reduced Icc
OPA37EZ	HA7-5137A-5	Yes	E	Enhanced ACs/Reduced Icc
OPA37GJ	HA2-5137-5	Yes	E	Enhanced ACs/Reduced Icc
OPA37GZ	HA7-5137-5	Yes	E	Enhanced ACs/Reduced Icc
OPA404AG	HA1-5114-5	Yes	FE	Lower Voltage Noise/Enhanced ACs
OPA404BG	HA1-5114-5	Yes	FE	Lower Voltage Noise/Enhanced ACs
OPA404KP	HA3-5114-5	Yes	FE	Lower Voltage Noise/Enhanced ACs
OPA404KU	HA9P-5114-5	Yes	FE	Lower Voltage Noise/Enhanced ACs
OPA404SG	HA1-5114-2	Yes	FE	Lower Voltage Noise/Enhanced ACs
OPA445AP	HA7-2645-5	Yes	FE	
OPA445BM	HA2-2640-2	Yes	FE	
OPA445SM	HA2-2640-2	Yes	FE	
OPA620KG	HFA7-0005-5	*	FE	Enhanced ACs
OPA620KP	HFA3-0005-5	*	FE	Enhanced ACs
OPA620LG	HFA7-0005-5	*	FE	Enhanced ACs
OPA620SG	HFA7-0005-9	*	FE	Enhanced ACs
OPA621KG	HFA7-0002-5	*	FE	Lower Voltage Noise/Temco
OPA621KP	HFA3-0002-5	*	FE	Lower Voltage Noise/Temco
OPA621LG	HFA7-0002-5	*	FE	Lower Voltage Noise/Temco
OPA621SG	HFA7-0002-9	*	FE	Lower Voltage Noise/Temco
OPA633AH	HA2-5033-2	Yes	I	
OPA633KP	HA3-5033-5	Yes	I	
OPA633SH	HA2-5033-5	Yes	FE	
PM139AY	CA0139AF	Yes	I	
PM139Y	CA0139F	Yes	I	
PM741CJ	CA0741CT	Yes	I	
PM741J	CA0741T	Yes	I	
RC3403AN	CA5470E	Yes	FE	MOS Input/Enhanced ACs
RC4741D	HA1-4741-2	Yes	E	Guaranteed ACs
RC4741M	HA9P-4741-5	Yes	E	Guaranteed ACs
RC5532AN	HA3-5102-5	Yes	FE	Enhanced DCs/Reduced Icc
RC5532N	HA3-5102-5	Yes	FE	Enhanced DCs/Reduced Icc
RC5534AN	HA3-5101-5	Yes	FE	Enhanced DCs/Reduced Icc
RC5534N	HA3-5101-5	*	FE	Enhanced DCs/Reduced Icc
RC741N	CA0741CE	Yes	I	
RC747N	CA0747CE	Yes	I	
RC747T	CA0747CT	Yes	I	

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RM5334T	HA2-5101-2	*	FE	Reduced Icc
RM5532AD	HA7-5102-2	Yes	FE	Reduced Icc
RM5532AT	HA2-5102-2	Yes	FE	Reduced Icc
RM5532D	HA7-5102-2	Yes	FE	Reduced Icc
RM5532T	HA2-5102-2	Yes	FE	Reduced Icc
RM5534AD	HA7-5101-2	*	FE	Reduced Icc
RM5534AT	HA2-5101-2	*	FE	Reduced Icc
RM5534D	HA7-5101-2	*	FE	Reduced Icc
RM741T	CA0741T	Yes	I	Specified From 0-70 Degrees C
RM747T	CA0747T	Yes	I	
RV741T	CA0741CT	Yes	FE	Specified From 0-70 Degrees C
SA5230N	CA5160AE	No	FE	MOS Input
SA556-1N	ICM7556IPD	Yes	FE	CMOS/Reduced Icc
SA556N	ICM7556IPD	Yes	FE	CMOS/Reduced Icc
SA723CN	CA0723CE	Yes	I	
SA747CN	CA0747CE	Yes	FE	
SE5532AFE	HA7-5102-2	Yes	FE	Reduced Icc
SE5532FE	HA7-5102-2	Yes	FE	Reduced Icc
SE5534AFE	HA7-5101-2	*	FE	Reduced Ibias/Iio
SE5534FE	HA7-5101-2	*	FE	Reduced Ibias/Iio
SE5539F	HA1-2539-2	*	FE	Specified @ ±15V Supplies
SE555CN	CA0555E	Yes	FE	
SE556-1CN	ICM7556MJD	Yes	FE	CMOS/Reduced Icc
SE556-1F	ICM7556MJD	Yes	FE	CMOS/Reduced Icc
SE556F	ICM7556MJD	Yes	FE	CMOS/Reduced Icc
SG1524CF	CA1524F	Yes	FE	
SG1524CN	CA1524E	Yes	FE	
SG1524J	CA1524F	Yes	I	
SG1536T	HA2-2640-2	*	FE	Reduced Vio/Enhanced ACs
SG1536Y	HA7-2640-2	*	FE	Reduced Vio/Enhanced ACs
SG2524CF	CA2524F	Yes	FE	
SG2524CN	CA2524E	Yes	FE	
SG301AT	CA0301AT	Yes	FE	Almost Identical
SG3045J	CA3045	Yes	FE	
SG3049T	CA3049T	Yes	FE	Greater Bandwidth/Reduced Noise
SG3083	CA3083	Yes	I	
SG3183D	CA3183M	Yes	FE	Identical Specs @ 25 Degrees C
SG3183N	CA3183E	Yes	FE	Identical Specs @ 25 Degrees C
SG3524CF	CA3524F	Yes	FE	
SG3524CN	CA3524E	Yes	FE	
SG3524J	CA3524F	Yes	I	
SG3524N	CA3524E	Yes	I	
SG741CN	CA0741CE	Yes	I	
SG741T	CA0741T	Yes	I	

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SHC5320KH	HA1-5320-5	Yes	I	
SHC5320SH	HA1-5320-2	Yes	I	
SHC85	HA1-2425-5	No	FE	Enhanced ACs
SHC85ET	HA1-2420-2	No	FE	Enhanced ACs
SHM-20C	HA1-5320-5	Yes	FE	Guaranteed Acquisition Time
SHM-20M	HA1-5320-2	Yes	FE	Guaranteed Acquisition Time
SHM-IC-1	HA1-2425-5	Yes	FE	Almost Identical
SHM-IC-1M	HA1-2420-2	Yes	FE	Almost Identical
SI7652DJ	ICL7652SIPD	Yes	E	Enhanced ACs/Gain
SI7652DK	ICL7652SIPD (PDIP)	Yes	E	Enhanced ACs/Gain
SI7660AA	ICL7660SMTV	*	E	Greater Vout Efficiency/Reduced Icc
SI7660BA	ICL7660SITV	*	E	Greater Vout Efficiency/Reduced Icc
SI7660CA	ICL7660SCTV	*	E	Greater Vout Efficiency/Reduced Icc
SI7660CJ	ICL7660SCPA	*	E	Greater Vout Efficiency/Reduced Icc
SI7660DY	ICL7660SIBA	*	E	Greater Vout Efficiency/Reduced Icc
SL3045CDG14	CA3045	Yes	FE	
SL3046CDP14	CA3046E	Yes	FE	
SL3127CDG16	CA3127F	Yes	FE	SOIC Version Available
SMP10AY	HA1-2420-2	*	FE	Faster Acquisition/Lower Droop
SMP10BY	HA1-2420-2	*	FE	Faster Acquisition/Lower Droop
SMP10EY	HA1-2425-5	*	FE	Faster Acquisition/Lower Droop
SMP10FY	HA1-2425-5	*	FE	Faster Acquisition/Lower Droop
SMP11AY	HA1-2420-2	*	FE	Faster Acquisition/Lower Droop
SMP11BY	HA1-2420-2	*	FE	Faster Acquisition/Lower Droop
SMP11EY	HA1-2425-5	*	FE	Faster Acquisition/Lower Droop
SMP11FY	HA1-2425-5	*	FE	Faster Acquisition/Lower Droop
SP1-2541-5	HA1-2541-5	Yes	I	
SP1-2541-2	HA1-2541-2	Yes	I	
SP1-2542-2	HA1-2542-2	Yes	I	
SP1-2542-5	HA1-2542-5	Yes	I	
SP1-5330-2	HA1-5330-2	Yes	I	
SP1-5330-5	HA1-5330-5	Yes	I	
SP2-2500-2	HA2-2500-2	Yes	I	
SP2-2502-2	HA2-2502-2	Yes	I	
SP2-2505-5	HA2-2505-5	Yes	I	
SP2-2510-2	HA2-2510-2	Yes	I	
SP2-2512-2	HA2-2512-2	Yes	I	
SP2-2515-5	HA2-2515-5	Yes	I	
SP2-2520-2	HA2-2520-2	Yes	I	Substitute HA2-2529-2
SP2-2522-2	HA2-2522-2	Yes	I	Substitute HA2-2529-2
SP2-2525-5	HA2-2525-5	Yes	I	Substitute HA2-2529-5
SP2-2541-2	HA2-2541-2	Yes	I	
SP2-2541-5	HA2-2541-5	Yes	I	
SP2-2542-2	HA2-2542-2	Yes	I	
SP2-2542-5	HA2-2542-5	Yes	I	
SP2-2600-2	HA2-2600-2	Yes	I	
SP2-2602-2	HA2-2602-2	Yes	I	
SP2-2605-5	HA2-2605-5	Yes	I	

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SP2-2620-2	HA2-2620-2	Yes	I	
SP2-2622-2	HA2-2622-2	Yes	I	
SP2-2625-5	HA2-2625-5	Yes	I	
SP3-2505-5	HA3-2505-5	Yes	I	
SP3-2515-5	HA3-2515-5	Yes	I	
SP3-2525-5	HA3-2525-5	Yes	I	Substitute HA3-2529-5
SP3-2542-5	HA3-2542-5	Yes	I	
SP3-2605-5	HA3-2605-5	Yes	I	
SP3-2625-5	HA3-2625-5	Yes	I	
SP7-2500-2	HA7-2500-2	Yes	I	
SP7-2502-2	HA7-2502-2	Yes	I	
SP7-2505-5	HA7-2505-5	Yes	I	
SP7-2510-2	HA7-2510-2	Yes	I	
SP7-2512-2	HA7-2512-2	Yes	I	
SP7-2515-5	HA7-2515-5	Yes	I	
SP7-2520-2	HA7-2520-2	Yes	I	Substitute HA7-2529-2
SP7-2522-2	HA7-2522-2	Yes	I	Substitute HA7-2529-2
SP7-2525-5	HA7-2525-5	Yes	I	Substitute HA7-2529-5
SP7-2600-2	HA7-2600-2	Yes	I	
SP7-2602-2	HA7-2602-2	Yes	I	
SP7-2605-5	HA7-2605-5	Yes	I	
SP7-2620-2	HA7-2620-2	Yes	I	
SP7-2622-2	HA7-2622-2	Yes	I	
SP7-2625-5	HA7-2625-5	Yes	I	
TCA520BN	CA5130AE	*	FE	MOS Input/Enhanced ACs
TCA520TD	CA5130M	*	FE	MOS Input/Enhanced ACs
TLC251ACP	CA3440AE	*	FE	
TLC251CP	CA3440E	*	FE	
TLC252ACD	CA5260AM	Yes	FE	Specified @ +5V Supply
TLC252ACP	CA5260AE	Yes	FE	Specified @ +5V Supply
TLC252CD	CA5260M	Yes	FE	Specified @ +5V Supply
TLC252CP	CA5260E	Yes	FE	Specified @ +5V Supply
TLC254CD	CA5470M	Yes	FE	Specified @ +5V Supply
TLC254CN	CA5470E	Yes	FE	Specified @ +5V Supply
TLC2652CP	ICL7652SCPD	Yes	FE	Reduced Ibias/Iio
TLC2652IN	ICL7652SIPD	Yes	FE	Reduced Ibias/Iio
TLC272ACD	CA5260AM	Yes	FE	Greater Vout Range/Reduced Icc
TLC272ACP	CA5260AE	Yes	FE	Greater Vout Range/Reduced Icc
TLC272AID	CA5260AM	Yes	FE	Greater Vout Range/Reduced Icc
TLC272AIP	CA5260AE	Yes	FE	Greater Vout Range/Reduced Icc
TLC272CD	CA5260M	Yes	FE	Greater Vout Range/Reduced Icc
TLC272CP	CA5260E	Yes	FE	Greater Vout Range/Reduced Icc
TLC272ID	CA5260M	Yes	FE	Greater Vout Range/Reduced Icc
TLC272IP	CA5260E	Yes	FE	Greater Vout Range/Reduced Icc
TLC272MJG	CA5260E (PDIP)	Yes	FE	Greater Vout Range/Reduced Icc
TLC274CD	CA5470M	Yes	FE	Greater Vout/Bandwidth/Slew Rate
TLC274CN	CA5470E	Yes	FE	Greater Vout/Bandwidth/Slew Rate
TLC274ID	CA5470M	Yes	FE	Greater Vout/Bandwidth/Slew Rate
TLC274IN	CA5470E	Yes	FE	Greater Vout/Bandwidth/Slew Rate
TLC274MJ	CA5470E (PDIP)	Yes	FE	Greater Vout/Bandwidth/Slew Rate

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TLC27M2ACD	CA5260AM	Yes	FE	Greater Vout/Bandwidth/Slew Rate
TLC27M2ACP	CA5260AE	Yes	FE	Greater Vout/Bandwidth/Slew Rate
TLC27M2AID	CA5260AM	Yes	FE	Greater Vout/Bandwidth/Slew Rate
TLC27M2AIP	CA5260AE	Yes	FE	Greater Vout/Bandwidth/Slew Rate
TLC27M2CD	CA5260M	Yes	FE	Greater Vout/Bandwidth/Slew Rate
TLC27M2CP	CA5260E	Yes	FE	Greater Vout/Bandwidth/Slew Rate
TLC27M2ID	CA5260M	Yes	FE	Greater Vout/Bandwidth/Slew Rate
TLC27M2IP	CA5260E	Yes	FE	Greater Vout/Bandwidth/Slew Rate
TLC27M2MJG	CA5260E (PDIP)	Yes	FE	Greater Vout/Bandwidth/Slew Rate
TLC555CD	ICM7555CBA	Yes	FE	Reduced Icc
TLC555IP	ICM7555IPA	Yes	FE	Reduced Icc
TLC556CN	ICM7556IPD	Yes	FE	Reduced Icc
TLC556IN	ICM7556IPD	Yes	FE	Reduced Icc
TLC556MJ	ICM7556MJD	Yes	FE	Reduced Icc
TLE2021	HA-5151		FE	Greater Slew Rate
TLE2022	HA-5152		FE	Greater Slew Rate
TLE2024	HA-5154		FE	Greater Slew Rate
TP1321	HA-5195	Yes	FE	
TP1322	HA-2520	Yes	FE	
TP1326	HA-2600	Yes	FE	
TP1332	HA-2645	Yes	FE	
TP1339	HA-2620	No	FE	
TP1341	HA-2540	Yes	FE	
TP1342	HA-2539	Yes	FE	
TP1344	HA-5160	Yes	FE	
TP1345	HA-5162	Yes	FE	
TP1346	H1-5180	Yes		
TP4856	HA1-2420/25	Yes	I	Guaranteed Acquisition Time
TP4866	HA1-5320	Yes	FE	Guaranteed Acquisition Time
TSC426CPA	ICL7667CPA	Yes	FE	Almost Identical
TSC426MJA	ICL7667MJA	Yes	FE	Almost Identical
TSC7650ACPA	ICL7650SCPA-1	Yes	FE	Reduced Tempco/Voltage Noise
TSC7650ACPD	ICL7650SCPD	Yes	FE	Reduced Tempco/Voltage Noise
TSC7650AIJA	ICL7650SIJA-1	Yes	FE	Reduced Tempco/Voltage Noise
TSC7650AIJD	ICL7650SIJD	Yes	FE	Reduced Tempco/Voltage Noise
TSC7652CPD	ICL7652SCPD	Yes	FE	
TSC7652IJD	ICL7652SIPD (PDIP)	Yes	FE	
TSC7660	ICL7660	*	FE	
TSC7662	ICL7662	*	FE	
µA741CL	CA0741CT	Yes	I	
µA741CP	CA0741CE	Yes	I	
µA741HM	CA0741T	Yes	I	
UC0P01CN	CA3140AE	Yes	FE	MOSFET Input
UC0P01GJ	CA3140AE (PDIP)	Yes	FE	MOSFET Input
UC0P02EN	CA3493E	*	FE	Reduced Tempco
UC1524J	CA1524F	Yes	I	
UC2524J	CA2524F	Yes	I	
UC2524N	CA2524E	Yes	I	

NOTES: 1. A "*" in this column indicates that primary pins are pin-to-pin, but secondary or optional function pins are not.

2. Electrical equivalency; denoted by the following: I = Identical, FE = Functional Equivalent, E = Enhanced Harris product meets all competitor specifications and exceeds several.

Commercial Linear Product Cross Reference

DEVICE	HARRIS REPLACEMENT	(NOTE 1) PIN TO PIN	(NOTE 2) EE	HARRIS ADVANTAGE OR COMMENTS
UC3524J	CA3524F	Yes	I	
UC3524N	CA3524E	Yes	I	
VI-7660-1	ICL7660SCPA	*	E	Greater Vout Efficiency/Reduced Icc
VI-7660-2	ICL7660SCTV	*	E	Greater Vout Efficiency/Reduced Icc
XR-1458CP	CA1458E	Yes	I	
XR-1524M	CA1524F	Yes	I	
XR-2242CP	ICM7242IPA	Yes	FE	Greatly Reduced Icc
XR-2524N	CA2524F	Yes	I	
XR-2524P	CA2524E	Yes	I	
XR-3403CP	CA5470E	Yes	FE	MOS Input/Enhanced ACs
XR-3524N	CA3524F	Yes	I	
XR-3524P	CA3524E	Yes	I	
XR-4558CP	CA1458E	Yes	I	
XR-4739CN	HA7-5102-5	No	FE	Enhanced ACs/DCs
XR-4739CP	HA3-5102-5	No	FE	Enhanced ACs/DCs
XR-4741CN	HA1-4741-5	Yes	E	Guaranteed Channel Separation
XR-4741CP	HA3-4741-5	Yes	E	Guaranteed Channel Separation
XR-4741M	HA1-4741-2	Yes	E	Guaranteed Channel Separation
XR-5532AN	HA7-5102-5	Yes	FE	Reduced Vio/Ibias
XR-5532AP	HA3-5102-5	Yes	FE	Reduced Vio/Ibias
XR-5532N	HA7-5102-5	Yes	FE	Reduced Vio/Ibias
XR-5532P	HA3-5102-5	Yes	FE	Reduced Vio/Ibias
XR-5534ACN	HA7-5101-5	*	FE	Greater Avol/Reduced Vio
XR-5534ACP	HA3-5101-5	*	FE	Greater Avol/Reduced Vio
XR-5534AM	HA7-5101-2	*	FE	Greater Avol
XR-5534CN	HA7-5101-5	*	FE	Greater Avol/Reduced Vio
XR-5534CP	HA3-5101-5	*	FE	Greater Avol/Reduced Vio
XR-5534M	HA7-5101-2	*	FE	Greater Avol
XR-555CP	CA0555CE	Yes	FE	
XR-8038CN	ICL8038CCJD	Yes	FE	Reduced Supply Current
XR-8038CP	ICL8038CCPD	Yes	FE	Reduced Supply Current
XR-8038M	ICL8038AMJD	Yes	FE	Reduced Supply Current
XR-8038N	ICL8038BCJD	Yes	FE	Reduced Supply Current

NOTES: 1. A "*" in this column indicates that primary pins are pin-to-pin, but secondary or optional function pins are not.

2. Electrical equivalency; denoted by the following: I = Identical, FE = Functional Equivalent, E = Enhanced Harris product meets all competitor specifications and exceeds several.

LINEAR 2

POWER CONTROL CIRCUITS

		PAGE
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POWER CONTROL CIRCUITS DATA SHEETS		
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ICL 8211	Programmable Voltage Detector	2-147
ICL 8212	Programmable Voltage Detector	2-147

Selection Guide

POWER-SUPPLY SUPERVISORY CIRCUITS

Type	Function	Description	Package Number of Pins*
ICL7663S	Programmable micro-power positive voltage regulator	Low-power, high-efficiency device (I_Q = 4μA max.) that accepts an input of 1 to 16V and provides an adjustable output over the same range at up to 40mA load. T_A Range: 0 to +70°C, -25 to +85°C. Line and load regulation and ESP protection (>2000V).	BA, JA, PA, TV
ICL7680	-5V to ±15V voltage converter/regulator	Boost-type switched-mode converter inverter chip to convert +5 to ±15V regulated outputs. Features current limiting protection with external shut down. T_A Range: 0 to +70°C.	JE, PE
ICL7660S	Voltage converter	Performs supply voltge conversion from positive to negative. Input range is +1.5V to +10V resulting in complementary output voltages of -1.5V to -12V. Can be connected as a voltge doubler to generate output voltage of -18.6V. T_A Range: 0 to +70°C, -55 to +125°C. ICL7660S improved version of ICL7660. Has extended supply voltage range, lower supply current, and ESD protection (>2000V).	BA, PA, TV
ICL7662S	Voltage converter	Similar to the ICL7660 in its operation, except the output voltages are -4.5V to -20V. Doubler output 22.6V.	PA, TV
ICL7665S ICL7665	Programmable micro-power under/over voltage detector	Contains two individually programmable voltage comparators and requires only 3μA supply current. Intended for battery-operated systems that require low or high voltage warnings, etc. Open drain outputs for interfacing. T_A Range: 0 to +70°C, -25 to +85°C. ICL7665S improved ICL7665. For features, see ICL7663S.	BA, JA, PA, TV
ICL8211	Programmable voltage level detector	Contains a 1.15V reference, a comparator, a hysteresis output and a non-inverting main-output. Provides a 7mA current-limited output sink when voltage on threshold terminal is <1.15V. T_A Range: 0 to +70°C, -55 to +125°C.	BA, JA, PA, TV
ICL8212	Programmable voltage level detector	Similar in operation to the ICL8211 except that its main output is inverting as opposed to non-inverting. Requires a voltage in excess of 1.15V to switch its output on (no current limit). T_A Range: Same as ICL8211.	
ICL7667	Dual power MOSFET driver	TTL-compatible high-speed CMOS driver designed to provide high output current (1.5A) and voltage (up to +15V) for driving the gates of power MOSFETs in high-frequency switched-mode power converters. T_A Range: 0 to +70°C, -55 to +125°C.	BA, JA, PA, TV
HV-250/255	MOSFET drivers	Complementary power. Wide supply range (20V to 450V). High peak output current of 2A. High switching speed 200ns. New product in development.	-
HV-350/355		Totem pole N-channel power MOSFET driver. Wide supply range (20V to 450V). High peak output current of 2A. High switching speed of 200ns. New product in development.	-
ICL7673	Automatic battery backup switch	Automatically switches between a main power supply (eg., +5V) and a battery back-up supply, when the main supply is removed. Wide supply range: 2.5V to 15V. T_A Range: 0 to +70°C, -25 to +85°C.	BA, PA, TV
ICL7675 ICL7676	Switched-mode power-supply controller set	Two-chip set provides required control circuitry for a 50W - 150W isolated-type flyback-type switching power supply. ICL7675 primary side controller provides main power-switch drive. ICL7676 secondary side controller monitors the regulated output. T_A Range: 0 to +70°C, -25 to +85°C, -55 to +125°C.	JA, PA
ICL7677	CMOS power fail detector	Used on primary side of power supply with opto isolators transmitting the fault indication to the equipment on the secondary side. Also used on secondary side to drive TTL/CMOS logic at fault indicating outputs. T_A Range: 0 to +70°C, - 25 to +85°C, -55 to +125°C.	JN, PN

*See Packaging Section

Selection Guide

SPECIAL PURPOSE CIRCUITS

Type	Description	Features
ICL8069	Low voltage reference	1.2V temperature compensated voltage reference uses band-gap principal for excellent stability and low noise at reverse currents down to 50μA. 0 to 70°C and -55 to +125°C temperature ranges (metal only). Temperature coefficients of 0.005 and 0.01/°C.

Type	Description	V_I Range V	V_O Range V	I_O (Max) mA	Load Regulation % V_O (Max)	$V_I - V_O$ V (Min)	Short-Circuit Current Limit mA (Typ)	Package Number of Pins*
CA3085	Voltage regulators	7.5 to 30	1.8 to 26	12**	0.1	4	96	8T,
CA3085A		7.5 to 40	1.7 to 36	100	0.15	4	96	8S,
CA3085B		7.5 to 50	1.7 to 46	100	0.15	3.5	96	8E
CA723		9.5 to 40	2 to 37	150	0.03	3	65	10T
CA723C		9.5 to 40	2 to 37	150	0.03	3	65	14E
		**This value may be extended to 100mA; however, regulation is not specified beyond 12mA. Operating temperature range (T_A): -55 to +125°C. Electrical characteristics at T_A = 25°C						

Type	Description	V^+ Range V	V_O Range V	Load Regulation % V_O (Typ)	Ripple Rejection dB (Typ)	Total Standby Current Is (mA) (Max)	$V_{CE\ SAT}$ V (Typ)
CA1524	Regulating	8 to 40	4.8 to 5.2	0.2	66	10	0.8
CA2524	pulse-width	8 to 40	4.8 to 5.2	0.2	66	10	0.8
CA3524	modulators	8 to 40	4.6 to 5.4	0.2	66	10	0.8
		Electrical characteristics at V^+ = 20V, f = 20kHZ. T_A = -55 to +125°C for CA1524; 0 to +70°C for CA2524, CA3534. 16-lead dual-in-line (E) & (F) packages. Short-circuit current limit: 100mA typ. Temperature stability: 1% max.					

Type	Description	AC Input Voltage @ 50-60 & 400Hz (VAC)	Max. DC Supply Volts (V)	Max. Input Current (μA)	Sensor Range (R_X) kΩ	Control Current to Thyristor Gate (mA)
CA3059	Zero voltage switches	24 120 208/230 277	14	1	2 to 100	Up to 124 with internal supply; up to 240 with one external supply
CA3079			10	2	2 to 50	
		Electrical characteristics at T_A = 25°C. 14-lead dual-in-line (E) package. Operating temperature range (T_A): -55 to +125°C.				

Type	Description	Input Voltage Range (Vrms)	Input Frequency Range (Hz)	Max. Ouput Current (mA)	Variable Output Voltage (V)	Line and Load Regulation	
HV-1205	Monolithic Power Supplies	18-132	48-440	50	5-24	<5%	Surge Protection per IEEE 587 Category A & B Using MOV
HV-2405E		18-264	48-440	50	5-24	<5%	

*See Packaging Section

Selection Guide

SPECIAL PURPOSE CIRCUITS (Continued)

Type	Description	Features	I_{CEX} Max. (V_{CE} = 50V) µA	$V_{CE\ SUS}$ Min. (I_C = 100mA) V	V_{CE} (sat) Max. (I_C = 600mA) V	I^+ Max. I_C = 700mA V_{CC} + 5.5V mA	I_R Max. (V_R = 50V) µA	t_{PHL}, t_{PLH} Max. µs	Package Number of Pins*
		Inverting Types							
CA3262	Quad-gated power drivers (interface low-level logic to high-current loads)	Independent over-current limiting for each output • (0.7 min. A). Independent over-temperature limiting for each output (155 typ. °C)	100#	25#	0.7△	80□ 5■	100	10	16E
CA3272**			100#	35#	0.6△	60□	100	10	28Q
CA3242		Overload protection circuitry	100△	25△	0.8#	80□ 5■	100	20	16E
		Non Inverting Types							
CA3252		Input latch with external feedback resistor	100△	25△	0.7#	80□ 5■	100	30	16E
		□All outputs ON # V_{IN} = 0.8V △ V_{IN} = 2.4V **w/fault mode flag ■All outputs OFF • V_{OUT} = 4.5V to 24.5V Electrical characteristics at T_A = +25°C, V_{CC} = 5V; T_A range: -40 to +85°C							

Type	Description	Characteristics			Limits Min.	Limits Typ.	Limits Max.	Units
CA3169	Solenoid and motor driver (½H drive)	Output leakage current (Pin 2 or Pin 3)			-110	±0.5	110	µA
		Quiescent current (Pin 1):	Input terminals shorted	V_{CC} = 14V	-	70	100	mA
			Input terminals open		-	17	40	
		Overvoltage shutdown circuit (Pin 1)	Upper trip point		20	25	27	V
			Lower trip point		18	21.4	23	
		Source output short circuit current (Pin 2-G)			0.65	1.11	2.6	A
		Sink output (I_{SINK} 600mA) output saturation voltage			-	0.3	0.85	V
		Operating temperature range: -40 to +85°C. Electrical characteristics at T_A = 25°C, V_{CC} = 10.5V to 18V Versa V1 TO-220 style package						

Type	Description	Characteristics	CA3020	CA3020A	Units
CA3020	Multipurpose wideband power amplifiers	Maximum power output (P_O) at THD = 10%	550	1000	mA
CA302A		Sensitivity (C_{IN})	35	45	mA
		Power gain (Gp)	75	75	dB
		Input resistance (R_{IN})	55	55	kΩ
		Signal-to-noise ration (I/N)	70	66	dB
		Total harmonic distortion at 150mW (THD)	3.1	3.3	%
		Bandwidth (-3dB point) (BW)	8	8	MHz
		Operating temperature range (T_A): -55 to +125°C Typical electrical characteristics at T_A = +25°C 12-lead (T) package			

*See Packaging Section

May 1990

Voltage Regulators

For Regulated Output Voltage Adjustable from 2 V to 37 V at Output Currents up to 150 mA without External Pass Transistors

Features:

- *Up to 150 mA output current*
- *Positive and negative voltage regulation*
- *Regulation in excess of 10 a with suitable pass transistors*
- *Input and output short-circuit protection*
- *Load and line regulation: 0.03%*
- *Direct replacement for 723 and 723C industry types*
- *Adjustable output voltage: 2 to 37 V*

Applications:

- *Series and shunt voltage regulator*
- *Floating regulator*
- *Switching voltage regulator*
- *High-current voltage regulator*
- *Temperature controller*

The CA723 and CA723 are silicon monolithic integrated circuits designed for service as voltage regulators at output voltages ranging from 2 to 37 volts at currents up to 150 milliamperes.

Each type includes a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and a current-limiting circuit. They also provide independently accessible inputs for adjustable current limiting and remote shutdown and, in addition, feature low standby current drain, low temperature drift, and high ripple rejection.

The CA723 and CA723C may be used with positive and negative power supplies in a wide variety of series, shunt, switching, and floating regulator applications. They can provide regulation at load currents greater than 150 milliamperes and in excess of 10 amperes with the use of suitable n-p-n or p-n-p external pass transistors.

The CA723 and CA723C are supplied in the 10-lead TO-5-style package (T suffix), and the 14-lead dual-in-line plastic package (E suffix), and are direct replacements for industry types 723, 723C, μA723, and μA723C in packages with similar terminal arrangements. They are also available in chip form ("H" suffix).

All types are rated for operation over the full military-temperature range of -55°C to +125°C.

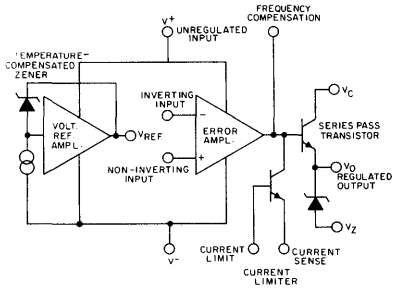


Figure 1 - Functional diagram of the CA723 and CA723C.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between V^+ and V^- Terminals)	40	V
PULSE VOLTAGE FOR 50-ms PULSE WIDTH (Between V^+ and V^- Terminals)	50	V
DIFFERENTIAL INPUT–OUTPUT VOLTAGE	40	V
DIFFERENTIAL INPUT VOLTAGE:		
Between Inverting and Non-Inverting Inputs	±5	V
Between Non-Inverting Input and V^-	8	V
CURRENT FROM ZENER DIODE TERMINAL (V_Z)	25	mA
CURRENT FROM VOLTAGE REFERENCE TERMINAL (V_{REF})	15	mA

DEVICE DISSIPATION:		
Up to T_A = 25°C –		
CA723T, CA723CT	800	mW
CA723E, CA723CE	1000	mW
Above T_A = 25°C –		
CA723T, CA723CT Derate linearly	6.3	mW/°C
CA723E, CA723CE Derate linearly	8.3	mW/°C
AMBIENT TEMPERATURE RANGE (All Types):		
Operating	–55 to +125	°C
Storage	–65 to +150	°C
LEAD TEMPERATURE (During Soldering):		
At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max.	+265	°C

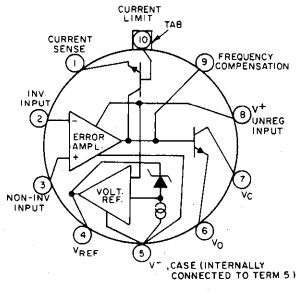


Fig. 2 – Terminal arrangement of the CA723T and CA723CT in the TO-5 style package.

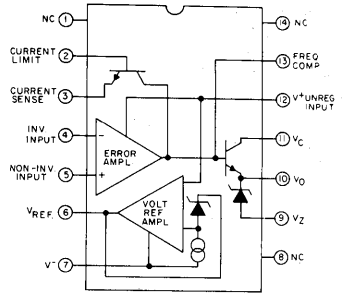


Fig. 3 – Terminal arrangement of the CA723E and CA723CE in the dual-in-line plastic package.

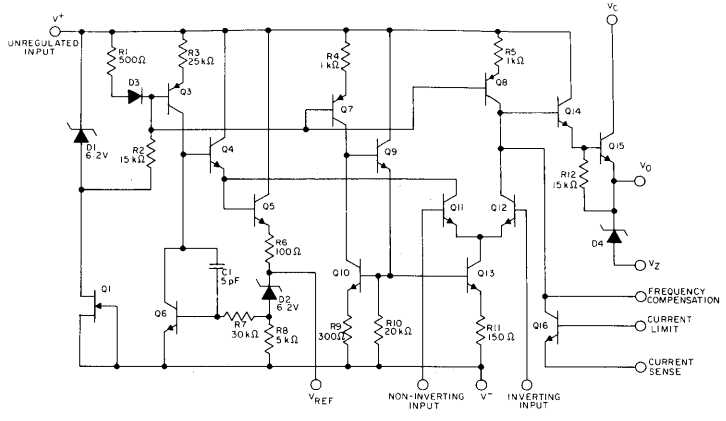


Fig. 4 – Equivalent schematic diagram of the CA723 and CA723C.

ELECTRICAL CHARACTERISTICS at T_A = 25 C, $V^+ = V_C = V_I$ = 12 V, V^- = 0, V_O = 5 V, I_L = 1 mA, C_1 = 100 pF, C_{REF} = 0, R_{SCP} = 0, unless otherwise specified. Divider impedance $\frac{R_1R_2}{R_1+R_2}$ at non-inverting input, Term. 5, = 10 kΩ (see Fig. 23).

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA723			CA723C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Quiescent Regulator Current, I_Q	I_L = 0, V_I = 30 V	–	2.3	3.5	–	2.3	4	mA
Input Voltage Range, V_I		9.5	–	40	9.5	–	40	V
Output Voltage Range, V_O		2	–	37	2	–	37	V
Differential Input-Output Voltage, V_I–V_O		3	–	38	3	–	38	V
Reference Voltage, V_{REF}		6.95	7.15	7.35	6.8	7.15	7.5	V
Line Regulation (See Note 1)	V_I = 12 to 40 V	–	0.02	0.2	–	0.1	0.5	%V_O
	V_I = 12 to 15 V	–	0.01	0.1	–	0.01	0.1	
	V_I = 12 to 15 V, T_A = −55 to +125°C	–	–	0.3	–	–	–	
	V_I = 12 to 15 V, T_A = 0 to 70°C	–	–	–	–	–	0.3	
Load Regulation (See Note 1)	I_L = 1 to 50 mA	–	0.03	0.15	–	0.03	0.2	%V_O
	I_L = 1 to 50 mA, T_A = −55 to +125°C	–	–	0.6	–	–	–	
	I_L = 1 to 50 mA, T_A = 0 to 70°C	–	–	–	–	–	0.6	
Output-Voltage Temp. Coefficient, $\triangle V_O$	T_A = −55 to +125°C	–	0.002	0.015	–	–	–	%/°C
	T_A = 0 to 70°C	–	–	–	–	0.003	0.015	
Ripple Rejection (See Note 2)	f = 50 Hz to 10 kHz	–	74	–	–	74	–	dB
	f = 50 Hz to 10 kHz, C_{REF} = 5 μF	–	86	–	–	86	–	

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA723			CA723C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Short-Circuit Limiting Current, I_{LIM}	R_{SCP} = 10 Ω, V_O = 0	–	65	–	–	65	–	mA
Equivalent Noise RMS Output Voltage, V_N (See Note 2)	BW = 100 Hz to 10 kHz, C_{REF} = 0	–	20	–	–	20	–	μV
	BW = 100 Hz 10 kHz, C_{REF} = 5 μF	–	2.5	–	–	2.5	–	

Note 1: Line and load regulation specifications are given for condition of a constant chip temperature. For high-dissipation conditions, temperature drifts must be separately taken into account.

Note 2: For C_{REF}, see Fig. 23.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723

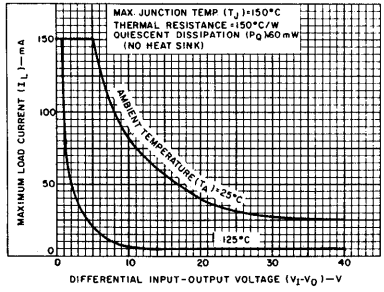


Fig. 5 – Max. load current vs differential input-output voltage.

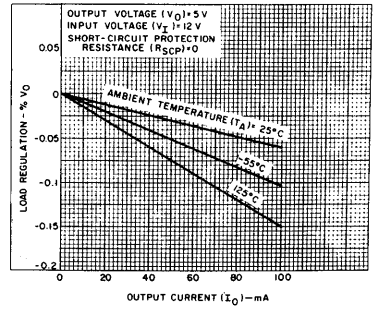


Fig. 6 – Load regulation without current limiting.

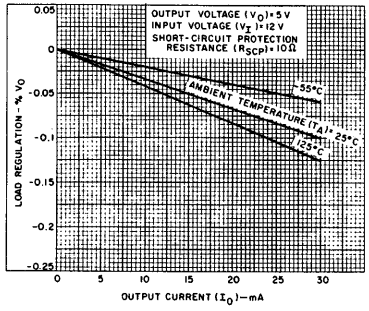


Fig. 7 – Load regulation with current limiting.

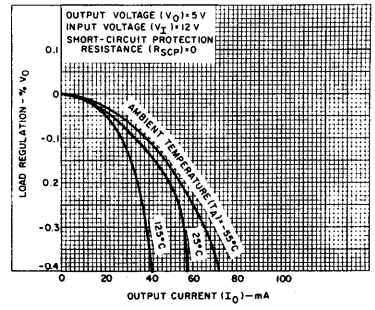


Fig. 8 – Load regulation with current limiting.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723 (Cont'd)

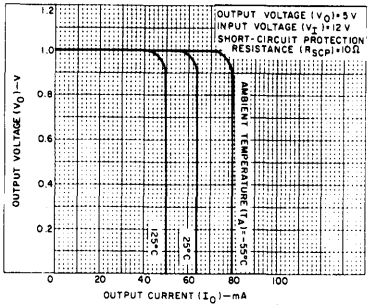


Fig. 9 – Current limiting characteristics.

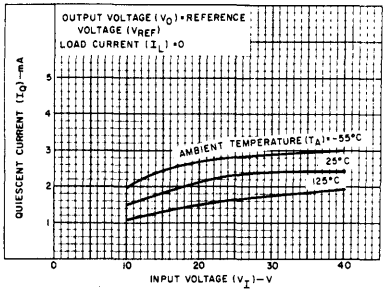


Fig. 10 – Quiescent current vs. input voltage.

TYPICAL CHARACTERISTICS CURVES FOR TYPE CA723C

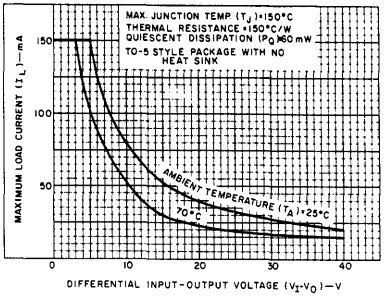


Fig. 11 – Max. load current vs differential input-output voltage CA723CT.

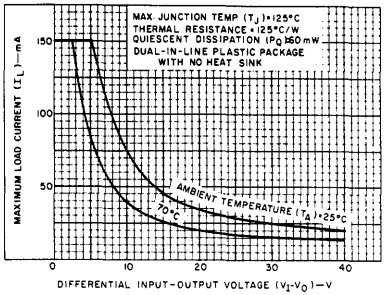


Fig. 12 – Max. load current vs differential input-output voltage for CA723CE.

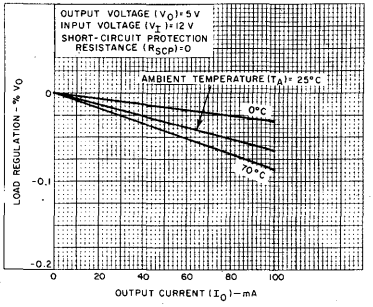


Fig. 13 – Load regulation without current limiting.

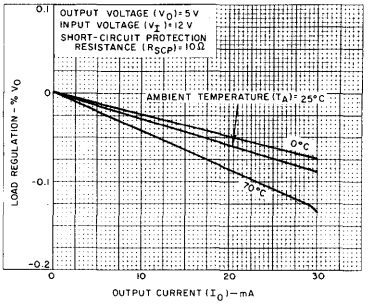


Fig. 14 – Load regulation with current limiting.

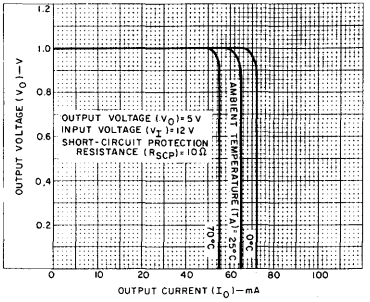


Fig. 15 – Current limiting characteristics.

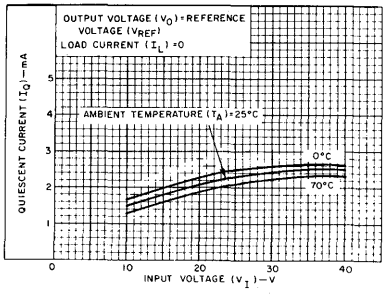


Fig. 16 – Quiescent current vs. input voltage.

TYPICAL CHARACTERISTICS CURVES FOR TYPES CA723 AND CA723C

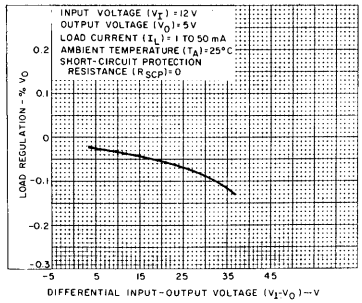


Fig. 17 — Load regulation vs. differential input-output voltage.

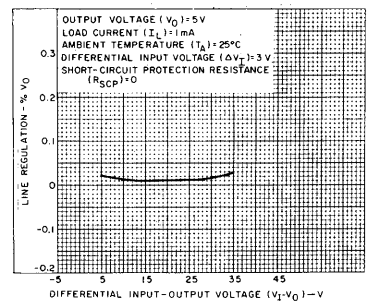


Fig. 18 — Line regulation vs. differential input-output voltage.

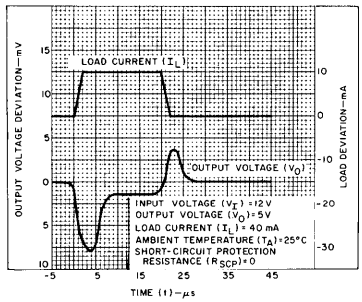


Fig. 19 — Line transient response.

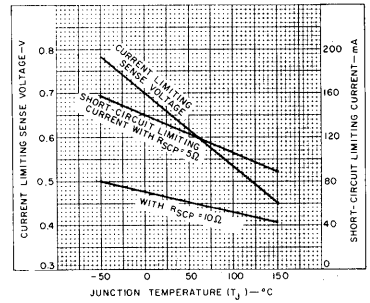


Fig. 20 — Current limiting characteristics vs. junction temperature.

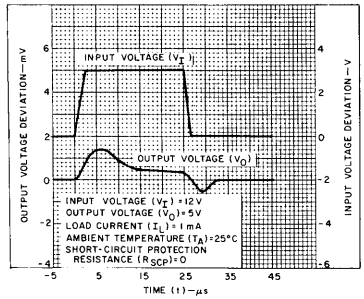


Fig. 21 — Load transient response.

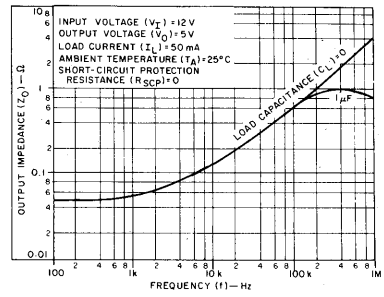
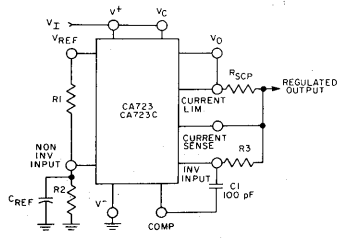


Fig. 22 — Output impedance vs. frequency.

TYPICAL APPLICATION CIRCUITS

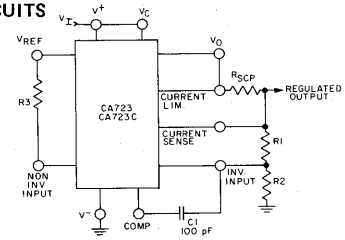


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 50 mA)	1.5 mV

Note: R3 = $\frac{R1\ R2}{R1+R2}$ for minimum temperature drift

Fig. 23 — Low-voltage regulator circuit (V_O = 2 to 7 volts).



CIRCUIT PERFORMANCE DATA:

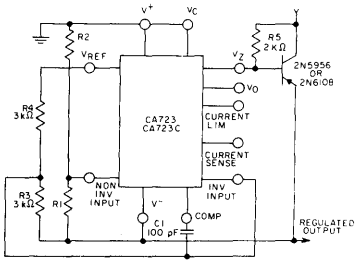
REGULATED OUTPUT VOLTAGE	15 V
LINE REGULATION (ΔV_I = 3 V)	1.5 mV
LOAD REGULATION (ΔI_L = 50 mA)	4.5 mV

Note: R3 = $\frac{R1\ R2}{R1+R2}$ for minimum temperature drift

R3 may be eliminated for minimum component count.

Fig. 24 — High-voltage regulator circuit (V_O = 7 to 37 volts).

TYPICAL APPLICATION CIRCUITS (Cont'd)

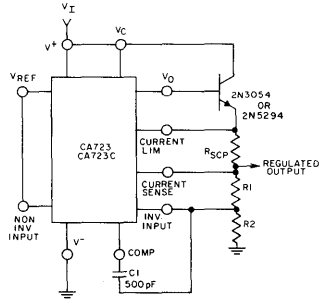


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	−15	V
LINE REGULATION (ΔV_I = 3 V)	1	mV
LOAD REGULATION (ΔI_L = 100 mA)	2	mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

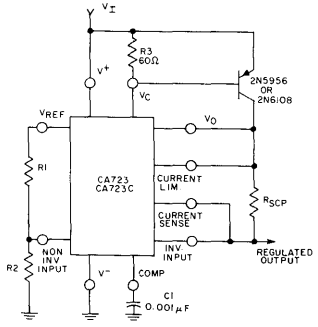
Fig. 25 – Negative-voltage regulator circuit.



CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	15	V
LINE REGULATION (ΔV_I = 3 V)	1.5	mV
LOAD REGULATION (ΔI_L = 1 A)	15	mV

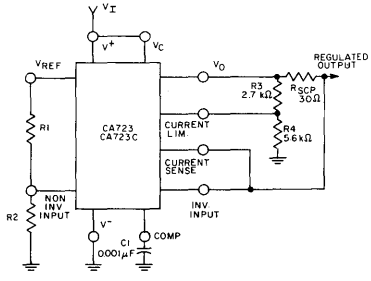
Fig. 26 – Positive-voltage-regulator circuit (with external n-p-n pass transistor).



CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5	V
LINE REGULATION (ΔV_I = 3 V)	0.5	mV
LOAD REGULATION (ΔI_L = 1 A)	5	mV

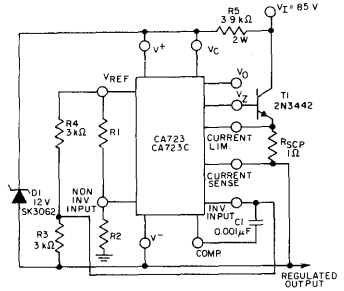
Fig. 27 – Positive voltage-regulator circuit (with external p-n-p pass transistor).



CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	5	V
LINE REGULATION (ΔV_I = 3 V)	0.5	mV
LOAD REGULATION (ΔI_L = 10 mA)	1	mV
SHORT-CIRCUIT CURRENT	20	mA

Fig. 28 – Foldback current-limiting circuit.

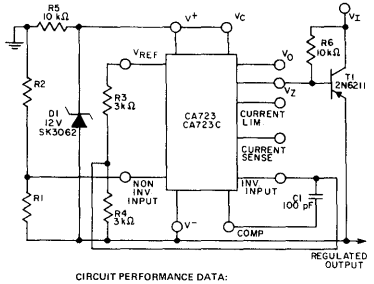


Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	50	V
LINE REGULATION (ΔV_I = 20 V)	15	mV
LOAD REGULATION (ΔI_L = 50 mA)	20	mV

Fig. 29 – Positive-floating regulator circuit.



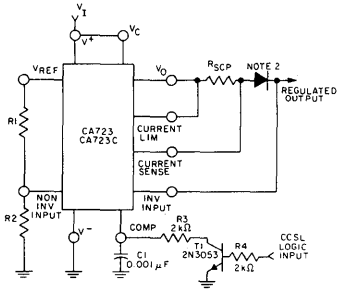
CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE	−100	V
LINE REGULATION (ΔV_I = 20 V)	30	mV
LOAD REGULATION (ΔI_L = 100 mA)	20	mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

Fig. 30 – Negative-floating regulator circuit.

TYPICAL APPLICATION CIRCUITS (Cont'd)

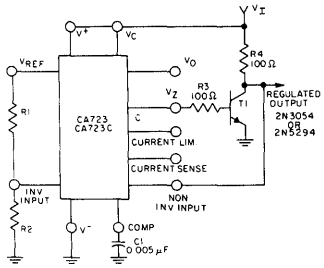


CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE . . .	5 V
LINE REGULATION (ΔV_I = 3 V)	0.5 mV
LOAD REGULATION (ΔI_L = 50 mA). . .	1.5 mV

Note 1: A current limiting transistor may be used for shutdown if current limiting is not required.
Note 2: Add a diode if V_O > 10 V.

Fig. 31 – Remote shutdown regulator circuit with current limiting.



CIRCUIT PERFORMANCE DATA:

REGULATED OUTPUT VOLTAGE . . .	5 V
LINE REGULATION (ΔV_I = 10 V) . . .	0.5 mV
LOAD REGULATION (ΔI_L = 100 mA) . .	1.5 mV

Note: For applications employing the TO-5 style package and where V_Z is required, an external 6.2-volt zener diode should be connected in series with V_O (Terminal 6).

Fig. 32 – Shunt regulator circuit.

May 1990

Regulating Pulse Width Modulator

Features:

- *Complete PWM power control circuitry*
- *Separate outputs for single-ended or push-pull operation*
- *Line and load regulation of 0.2% typ.*
- *Internal reference supply with 1% max. oscillator and reference voltage variation over full temperature range*
- *Standby current of less than 10 mA*
- *Frequency of operation beyond 100 kHz*
- *Variable-output dead time of 0.5 to 5 μs*
- *Low VCE(sat) over the temperature range*

Applications:

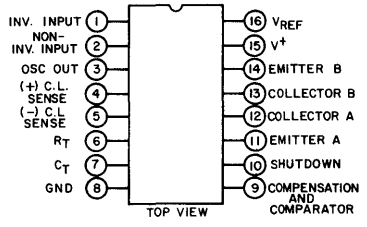
- *Positive and negative regulated supplies*
- *Dual-output regulators*
- *Flyback converters*
- *DC-DC transformer-coupled regulating converters*
- *Single-ended DC-DC converters*
- *Variable power supplies*

The CA1524, CA2524, and CA3524 are silicon monolithic integrated circuits designed to provide all the control circuitry for use in a broad range of switching regulator circuits.

The CA1524, CA2524, and CA3524 have all the features of the industry types SG1524, SG2524, and SG3524, respectively. A block diagram of the CA1524 series is shown in Fig. 1. The circuit includes a zener voltage reference, transconductance error amplifier, precision R-C oscillator, pulse-width modulator, pulse-steering flip-flop, dual alternating output switches, and current-limiting and shutdown circuitry. This device can be used for switching regulators of either polarity, transformer-coupled dc-dc converter, transformerless voltage doublers, dc-ac power inverters, highly efficient variable power supplies, and polarity converter, as well as other power-control applications.

The CA1524 is specified for the military temperature range of -55°C to +125°C.

The CA2524 and CA3524 are speciifed for the commmercial temperature range of 0°C to 70°C. All types operate over a supply voltage range of 8 to 40 V, have a rated operating temperature range of -55°C to +125°C, and are supplied in 16-lead, dual-in-line plastic packages (E suffix, and dual-in-line frit-seal hermetic packages (F suffix)). The CA3524 is available in chip form (H suffix).



TERMINAL ASSIGNMENT

MAXIMUM RATING, *Absolute-Maximum Values*

INPUT VOLTAGE (BETWEEN VIN AND GROUND TERMINALS)	40 V
OPERATING VOLTAGE RANGE (VIN TO GROUND)	8 to 40 V
OUTPUT CURRENT EACH OUTPUT: (TERMINAL 11, 12 OR 13, 14)	100 mA
OUTPUT CURRENT (REFERENCE REGULATOR)	50 mA
OSCILLATOR CHARGING CURRENT	5 mA
DEVICE DISSIPATION:	
Up to TA = 25°C	1 W
Above TA = 25°C	Derate linearly 8 mW/°C
OPERATING TEMPERATURE RANGE	-55 to +125°C
STORAGE TEMPERATURE RANGE	-65 to +150°C

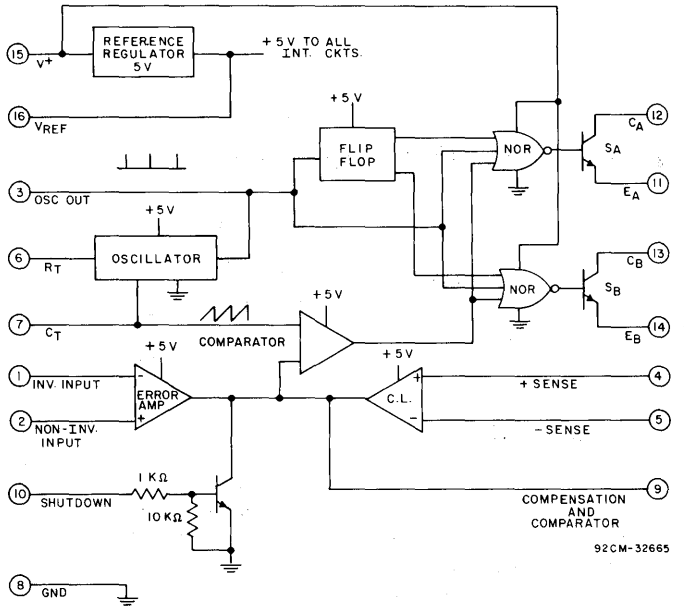


Fig. 1 - Functional block diagram of CA1524 series.

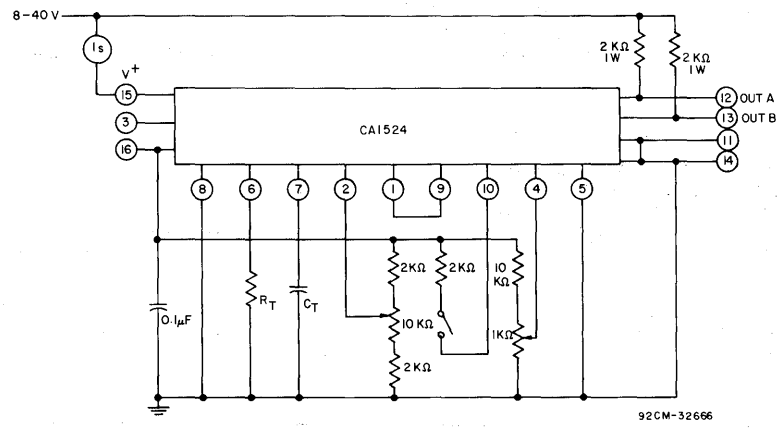
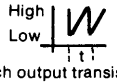


Fig. 2 - Open loop test circuit for CA1524 series.

ELECTRICAL CHARACTERISTICS at T_A=-55 to +125°C for CA1524, 0 to +70°C for the CA2524 and CA3524; V+=20 V and f=20 kHz, unless otherwise stated.

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA1524, CA2524			CA3524			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Reference Section:								
Output Voltage		4.8	5	5.2	4.6	5	5.4	V
Line Regulation	V+=8 to 40 V	—	10	20	—	10	30	mV
Load Regulation	I_L=0 to 20 mA	—	20	50	—	20	50	mV
Ripple Rejection	f=120 Hz, T_A=25°C	—	66	—	—	66	—	dB
Short Circuit Current Limit	V_{REF}=0, T_A=25°C	—	100	—	—	100	—	mA
Temperature Stability	Over Operating Temperature Range	—	0.3	1	—	0.3	1	%
Long Term Stability	T_A=25°C	—	20	—	—	20	—	mV/khr
Oscillator Section:								
Maximum Frequency	C_T=0.001 μF, R_T=2 KΩ	—	300	—	—	300	—	kHz
Initial Accuracy	R_T and C_T constant	—	5	—	—	5	—	%
Voltage Stability	V+=8 to 40 V, T_A=25°C	—	—	1	—	—	1	%
Temperature Stability	Over Operating Temperature Range	—	—	2	—	—	2	%
Output Amplitude	Terminal 3, T_A=25°C	—	3.5	—	—	3.5	—	V
Output Pulse Width (Pin 3)	C_T=0.01 μF, T_A=25°C	—	0.5	—	—	0.5	—	μs
* Ramp Voltage Low	Pin 7	—	0.6	—	—	0.6	—	V
* Ramp Voltage High	Pin 7	—	3.5	—	—	3.5	—	V
Capacitor Charging Current Current Range	Pin 7 (5-2 V_{BE})/RT	0.03	—	2	0.03	—	2	mA
Timing Resistance Range	Pin 6	1.8	—	120	1.8	—	120	KΩ
Charging Capacitor Range	Pin 7	0.001	—	0.1	0.001	—	0.1	μF
Dead Time Expansion Capacitor on Pin 3 (when a small osc. cap is used)	Pin 3	100	—	1000	100	—	1000	pF
Error Amplifier Section:								
Input Offset Voltage	V_{CM}=2.5 V	—	0.5	5	—	2	10	mV
Input Bias Current	V_{CM}=2.5 V	—	1	10	—	1	10	μA
Open Loop Voltage Gain		72	80	—	60	80	—	dB
Common Mode Voltage	T_A=25°C	1.8	—	3.4	1.8	—	3.4	V
Common Mode Rejection Ratio	T_A=25°C	—	70	—	—	70	—	dB
Small Signal Bandwidth	A_V= 0 dB, T_A=25°C	—	3	—	—	3	—	MHz
Output Voltage	T_A=25°C	0.5	—	3.8	0.5	—	3.8	V
Amplifier Pole		—	250	—	—	250	—	Hz
Pin 9 Shutdown Current	External Sink	—	200	—	—	200	—	μA
Comparator Section:								
Duty Cycle	% Each Output On	0	—	45	0	—	45	%
Input Threshold	Zero Duty Cycle	—	1	—	—	1	—	V
Input Threshold	Max. Duty Cycle	—	3.5	—	—	3.5	—	V
Input Bias Current		—	1	—	—	1	—	μA
Current Limiting Section:								
Sense Voltage For 25% Output Duty Cycle	Terminal 9=2 V with Error Amplifier Set for Max Out, T_A=25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.		—	0.2	—	—	0.2	—	mV/°C
Common Mode Voltage		-1	—	+1	-1	—	+1	V
Rolloff Pole of R51 C3 + Q64		—	300	—	—	300	—	Hz

*Ramp voltage at Pin 7 

where t = OSC period in microseconds
$t \cong R_T C_T$ with C_T in microfarads and R_T in ohms.

Output frequency at each output transistor is half OSC frequency when each output is used separately and is equal to the OSC frequency when each output is connected in parallel.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA1524, CA2524			CA3524			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Section: (Each Output)								
Collector-Emitter Voltage		40	—	—	40	—	—	V
Collector Leakage Current	V_{CE}=40 V	—	0.1	50	—	0.1	50	μA
Saturation Voltage	V+=40 V, I_C=50 mA	—	0.8	2	—	0.8	2	V
Emitter Output Voltage	V+=20 V	17	18	—	17	18	—	V
Rise Time	R_C=2 KΩ, T_A=25°C	—	0.2	—	—	0.2	—	μs
Fall Time	R_C=2 KΩ, T_A=25°C	—	0.1	—	—	0.1	—	μs
Total Standby Current:* I_S	V+=40 V	—	4	10	—	4	10	mA

*Excluding oscillator charging current, error and current limit dividers, and with outputs open.

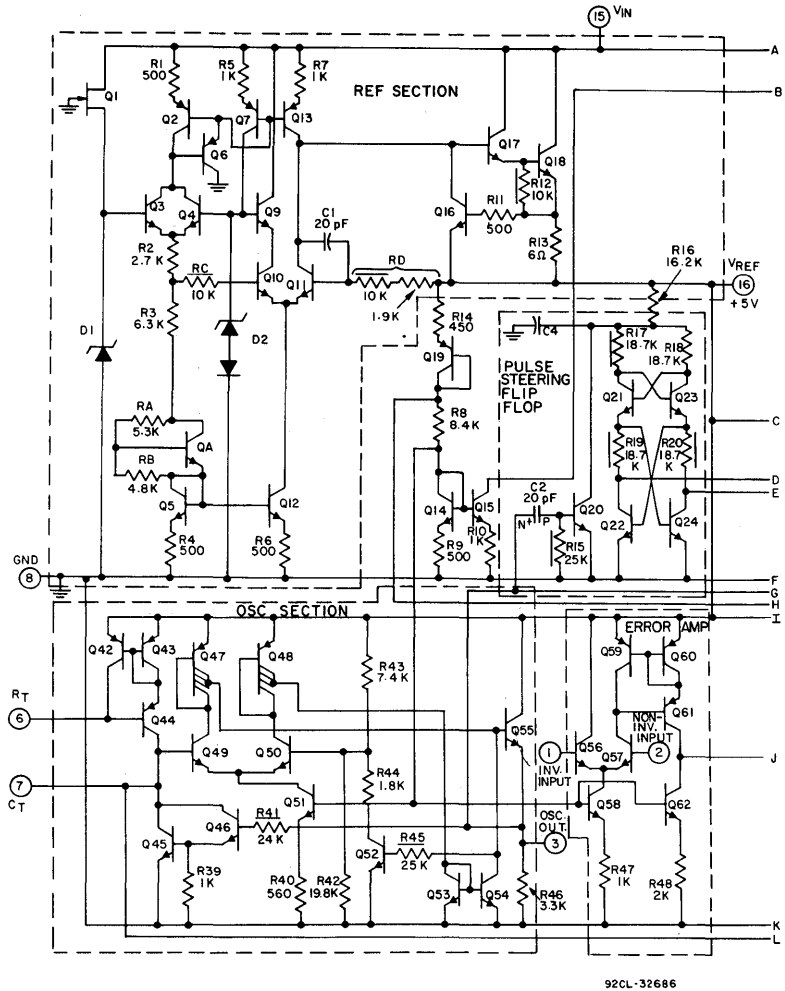


Fig. 3 - Schematic diagram.

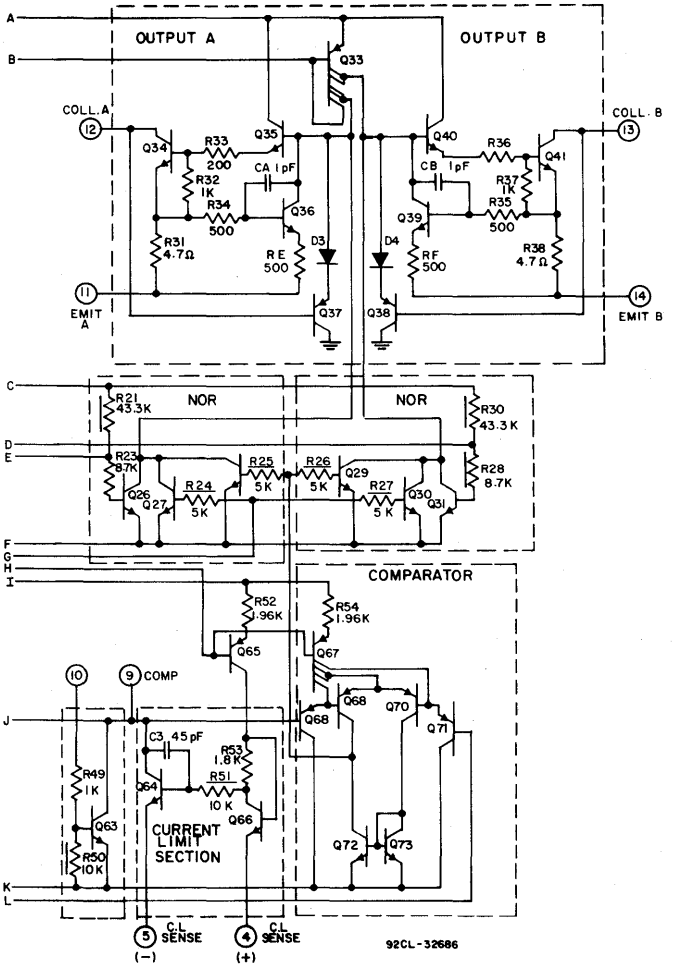


Fig. 3 - Schematic diagram (cont'd).

CIRCUIT DESCRIPTION

Voltage Reference Section

The CA1524 series contains an internal series voltage regulator employing a zener reference to provide a nominal 5-volt output, which is used to bias all internal timing and control circuitry. The output of this regulator is available at terminal 16 and is capable of supplying up to 50-mA output current.

Fig. 4 shows the temperature variation of the reference voltage with supply voltages of 8 to 40 volts and load currents up to 20 mA. Load regulation and line regulation curves are shown in Figs. 5 and 6, respectively.

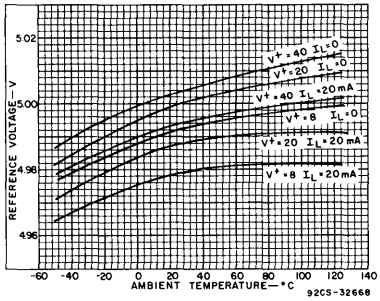


Fig. 4 - Typical reference voltage as a function of ambient temperature.

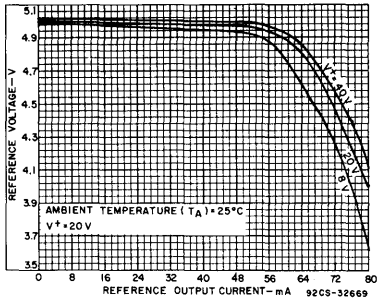


Fig. 5 - Typical reference voltage as a function of reference output current.

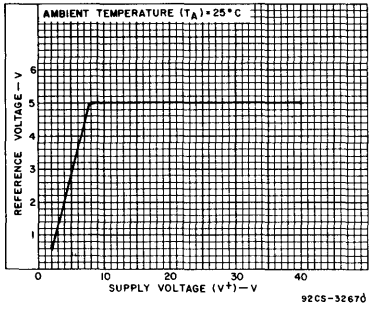


Fig. 6 - Typical reference voltage as a function of supply voltage.

Oscillator Section

Transistors Q42, Q43 and Q44, in conjunction with an external resistor R_T, establishes a constant charging current into an external capacitor C_T to provide a linear ramp voltage at terminal 7. The ramp voltage has a value that ranges from 0.6 to 3.5 volts and is used as the reference for the comparator in the device. The charging current is equal to $(5-2V_{BE})/R_T$ or approximately $3.6/R_T$ and should be kept within the range of 30 μA to 2 mA by varying R_T. The discharge time of C_T determines the pulse width of the oscillator output pulse at terminal 3. This pulse has a practical range of 0.5 μs to 5 μs for a capacitor range of 0.001 to 0.1 μF. The pulse has two internal uses: as a dead-time control of blanking pulse to the output stages to assure that both outputs cannot be on simultaneously and as a trigger pulse to the internal flip-flop which controls the switching of the output between the two output channels. The output dead-time relationship is shown in Fig. 7. Pulse widths less than 0.5 μs may allow false triggering of one output by removing the blanking pulse prior to a stable state in the flip-flop.

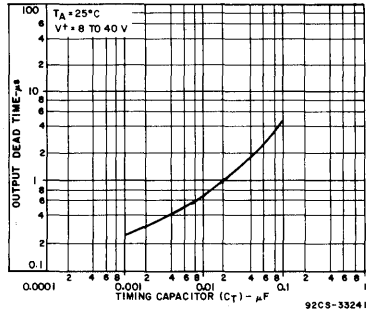


Fig. 7 - Typical output stage dead time as a function of timing capacitor value.

If a small value of C_T must be used, the pulse width can be further expanded by the addition of a shunt capacitor in the order of 100 pF but no greater than 1000 pF, from terminal 3 to ground. When the oscillator output pulse is used as a sync input to an oscilloscope, the cable and input capacitances may increase the pulse width slightly. A 2-KΩ resistor at terminal 3 will usually provide sufficient decoupling of the cable. The upper limit of the pulse width is determined by the maximum duty cycle acceptable.

The oscillator period is determined by R_T and C_T, with an approximate value of $t=R_TC_T$, where R_T is in ohms, C_T is in μF, and t is in μs. Excess lead lengths, which produce stray capacitances, should be avoided in connecting R_T and C_T to their respective terminals. Fig. 8 provides curves for selecting these values for a wide range of oscillator periods. For series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle with the output stage frequency the same as the oscillator frequency. Since the outputs are separate, push-pull and flyback applications are possible. The flip-flop divides the frequency such that the duty cycle of each output is 0-45% and the overall frequency is half that of the oscillator. Curves of the output duty cycle as a function of the voltage at terminal 9 are shown in Fig. 10. To synchronize two or more CA1524's, one must be designated as master, with

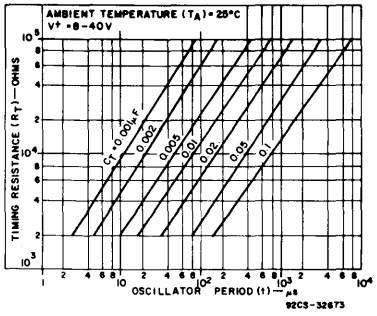


Fig. 8 - Typical oscillator period as a function of R_T and C_T.

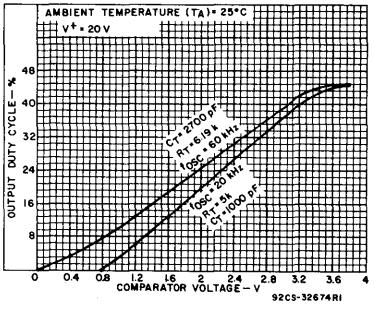


Fig. 10 - Typical duty cycle as a function of comparator voltage (at terminal 9).

R_TC_T set for the correct period. Each of the remaining units (slaves) must have a C_T of ½ the value used in the master and approximately a 10% longer R_TC_T period than the master. Connecting terminal 3 together on all units assures that the master output pulse, which occurs first and has a wider pulse width, will reset the slave units.

Error Amplifier Section

The error amplifier consists of a differential pair (Q56, Q57) with an active load (Q61 and Q62) forming a differential transconductance amplifier. Since Q61 is driven by a constant current source, Q62, the output impedance R_{out}, terminal 9, is very high (≅ 5 MΩ).

The gain is:

$$A_V = g_m R = 8\, I_C\, R/2KT = 10^4,$$

where $R = \frac{R_{out}\, R_L}{R_{out}+R_L}$, $R_L = \infty$, $A_V \propto 10^4$

Since R_{out} is extremely high, the gain can be easily reduced from a nominal 10^4 (80 dB) by the addition of an external shunt resistor from terminal 9 to ground as shown in Fig. 9.

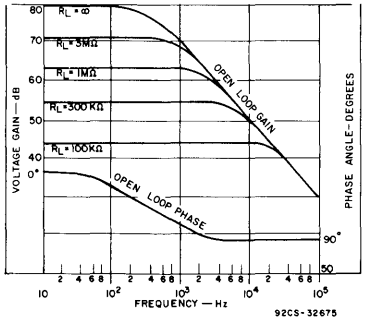


Fig. 9 - Open-loop error amplifier response characteristics.

The output amplifier terminal is also used to compensate the system for ac stability. The frequency response and phase shift curves are shown in Fig. 10. The uncompensated amplifier has a single pole at approximately 250 Hz and a unity gain cross-over at 3 MHz.

Since most output filter designs introduce one or more additional poles at a lower frequency, the best network to stabilize the system is a series RC combination at terminal 9 to ground. This network should be designed to introduce a zero to cancel out one of the output filter poles. A good starting point to determine the external poles is a 1000-pF capacitor and a variable series 50-KΩ potentiometer from terminal 9 to ground. The compensation point is also a convenient place to insert any programming signal to override the error amplifier. Internal shutdown and current limiting are also connected at terminal 9. Any external circuit that can sink 200 μA can pull this point to ground and shut off both output drivers.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and will be stable in either the inverting or non-inverting mode. Input common-mode limits must be observed; if not, output signal inversion may result. The internal 5-volt reference can be used for conventional regulator applications if divided as shown in Fig. 11. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

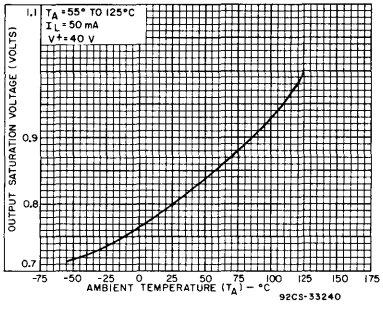


Fig. 11 - Typical output saturation voltage as a function of ambient temperature.

Output Section

The CA1524 series outputs are two identical n-p-n transistors with both collectors and emitters uncommitted. Each output transistor has antisaturation circuitry that enables a fast transient response for the wide range of oscillator frequencies. Current limiting of the output section is set at 100 mA for each output and 100 mA total if both outputs are paralleled. Having both emitters and collectors available provides the versatility to drive either n-p-n or p-n-p external transistors. Curves of the output saturation voltage as a function of temperature and output current are shown in Figs. 11 and 12, respectively.

There are a number of output configurations possible in the application of the CA1524 to voltage regulator circuits which fall into three basic classifications:

1. Capacitor-diode coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

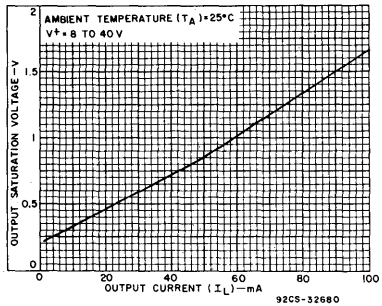


Fig. 12 - Typical output saturation voltage as a function of output current.

Device Application Suggestions

For higher currents, the circuit of Fig. 13 may be used with an external p-n-p transistor and bias resistor. The internal regulator may be bypassed for operation from a fixed 5-volt supply by connecting both terminals 15 and 16 to the input voltage, which must not exceed 6 volts.

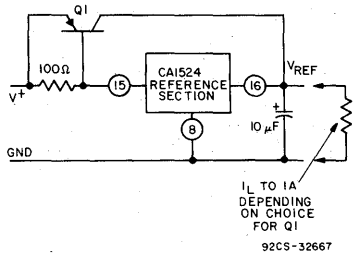


Fig. 13 - Circuit for expanding the reference current capability.

The internal 5-volt reference can be used for conventional regulator applications if divided as shown in Fig. 14. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

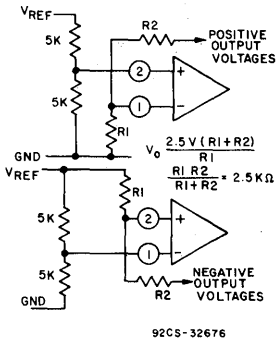


Fig. 14 - Error amplifier biasing circuits.

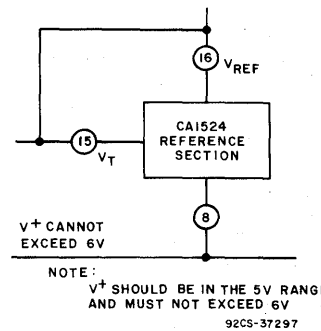


Fig. 15 - Circuit to allow external bypass of the reference regulation.

To provide an expansion of the dead time without loading the oscillator, the circuit of Fig. 16 may be used.

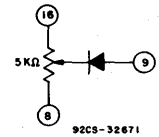


Fig. 16 - Circuit for expansion of dead time, without using a capacitor on pin 3 or when a low value oscillator capacitor is used.

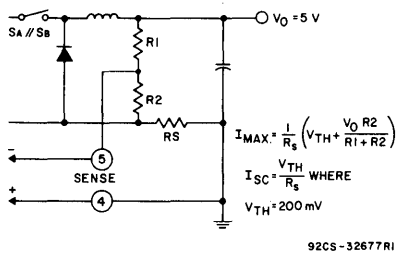


Fig. 17 - Foldback current-limiting circuit used to reduce power dissipation under shorted output conditions.

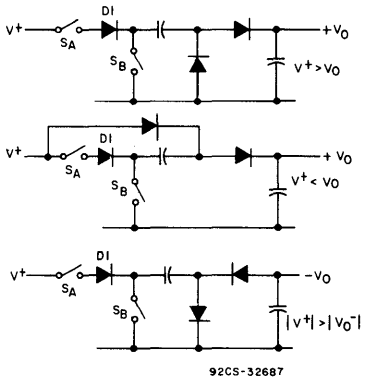


Fig. 18 - Capacitor-diode coupled voltage multiplier output stages. (Note: Diode D1 is necessary to prevent reverse emitter-base breakdown of transistor switch S_A).

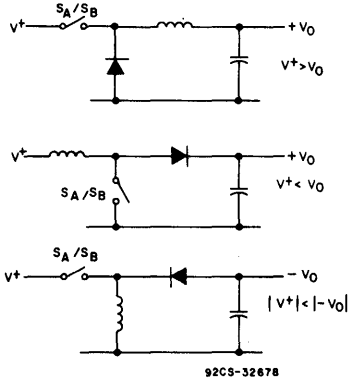


Fig. 19 - Single-ended inductor circuits where the two outputs of the 1524 are connected in parallel.

Table I - Input vs. Output voltage, and Feedback Resistor Values for I_L=40 mA (For capacitor-diode output circuit in Fig. 21)

V_O (V)	R2 (KΩ)	V+ (Min.) (V)
-0.5	6	8
-2.5	10	9
-3	11	10
-4	13	11
-5	15	12
-6	17	13
-7	19	14
-8	21	15
-9	23	16
-10	25	17
-11	27	18
-12	29	19
-13	31	20
-14	33	21
-15	35	22
-16	37	23
-17	39	24
-18	41	25
-19	43	26
-20	45	27

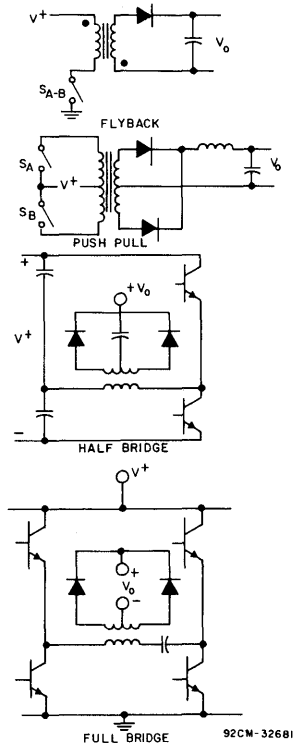


Fig. 20 - Transformer-coupled outputs.

APPLICATIONS*

A capacitor-diode output filter is used in Fig. 22 to convert +15 V dc to -5 V dc at output currents up to 50 mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table I gives the required minimum input voltage and feedback resistor values, R2, for an output voltage.

Capacitor-Diode Output Circuit

A capacitor-diode output filter is used in Fig. 21 to convert +15 V dc to -5 V dc at output currents up to 50 mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table I gives the required minimum input voltage and feedback resistor values, R2, for an output voltage range of -0.5 V to -20 V with an output current of 40 mA.

Single-Ended Switching Regulator

The CA1524 in the circuit of Fig. 22 has both output stages connected in parallel to produce an effective 0-90% duty cycle. Transistor Q1 is pulsed on and off by these output stages. Regulation is achieved from the feedback provided by R1 and R2 to the error amplifier which adjusts the on-time of the output transistors according to the load current being drawn. Various output voltages can be obtained by adjusting R1 and R2. The use of an output inductor requires an R-C phase compensation network to stabilize the system. Current limiting is set at 1.9 amperes by the sense resistor R3.

*For additional information on the application of this device and a further explanation of the circuits below, see RCA Application Note ICAN-6915 "Application of the CA1524 series PWM IC".

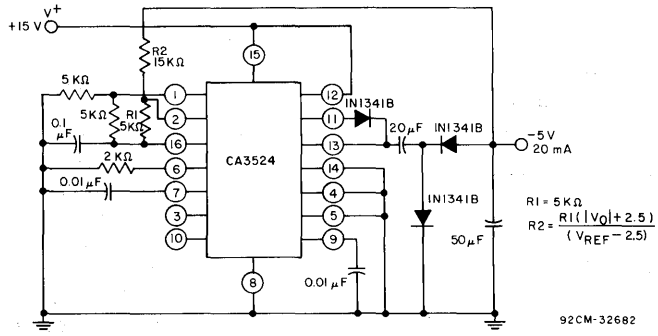


Fig. 21 - Capacitor-diode output circuit.

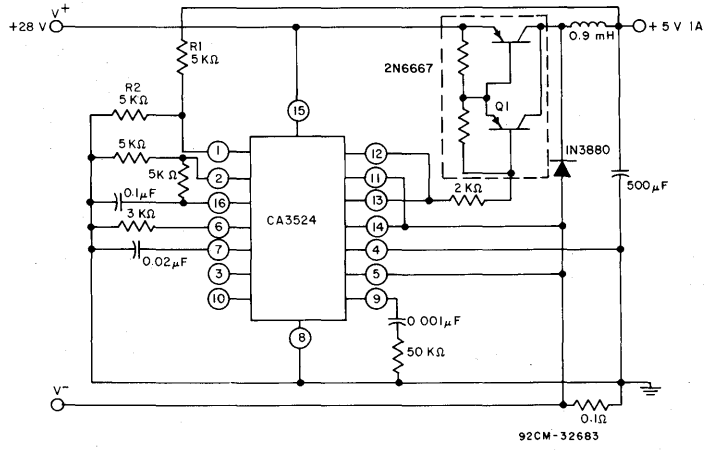


Fig. 22 - Single-ended LC switching regulator circuit.

Flyback Converter

Fig. 23 shows a flyback converter circuit for generating a dual 15-volt output at 20 mA from a 5-volt regulated line. Reference voltage is provided by the input and the internal reference generator is unused. Current limiting in this circuit is accomplished by sensing current in the primary line and resetting the soft-start circuit.

Push-Pull Converter

The output stages of the CA1524 provide the drive for transistors Q1 and Q2 in the push-pull application of Fig. 24. Since the internal flip-flop divides the oscillator frequency by two, the oscillator must be set at twice the output frequency. Current limiting for this circuit is done in the primary of transformer T1 so that the pulse width will be reduced if transformer saturation should occur.

Low-Frequency Pulse Generator

Fig. 25 shows the CA1524 being used as a low-frequency pulse generator. Since all components (error amplifier, oscillator, oscillator reference regulator, output transistor drivers) are on the IC, a regulated 5-V (or 2.5-V) pulse of 0%-45% (or 0%-90%) on time is possible over a frequency range of 150 to 500 Hz. Switch S1 is used to go from a 5-V output pulse (S1 closed) to a 2.5-V output pulse (S1 open) with a duty cycle range of 0% to 45%. The output frequency will be roughly half of the oscillator frequency when the output transistors are not connected in parallel (75 Hz to 250 Hz, respectively). Switch S2 will allow both output stages to be paralleled for an effective duty cycle of 0%-90% with the output frequency range from 150 to 500 Hz. The frequency is adjusted by R1; R2 controls duty cycle.

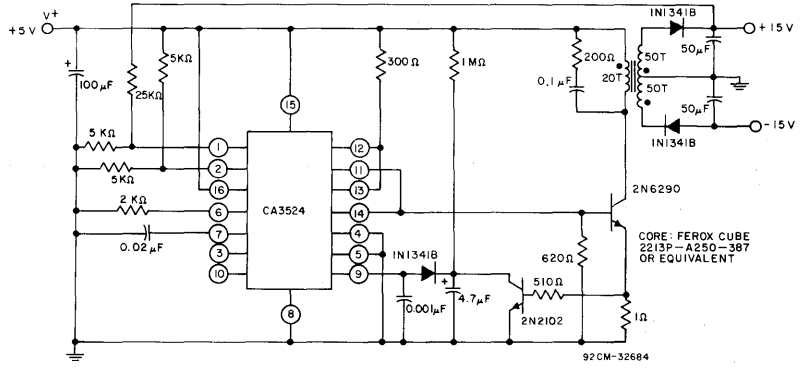


Fig. 23 - Flyback converter circuit.

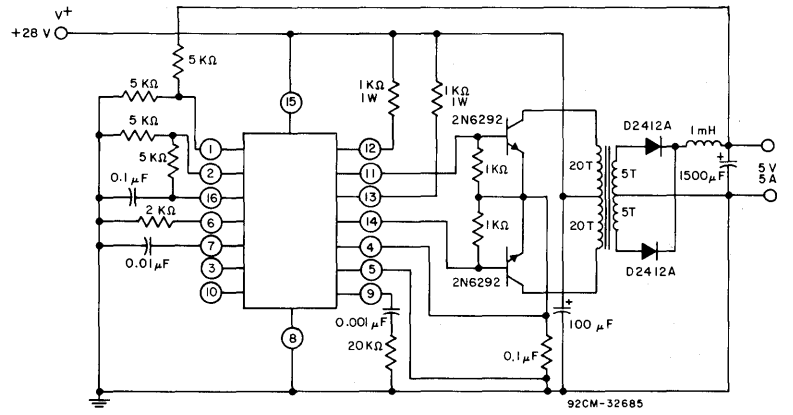


Fig. 24 - Push-pull transformer-coupled converter.

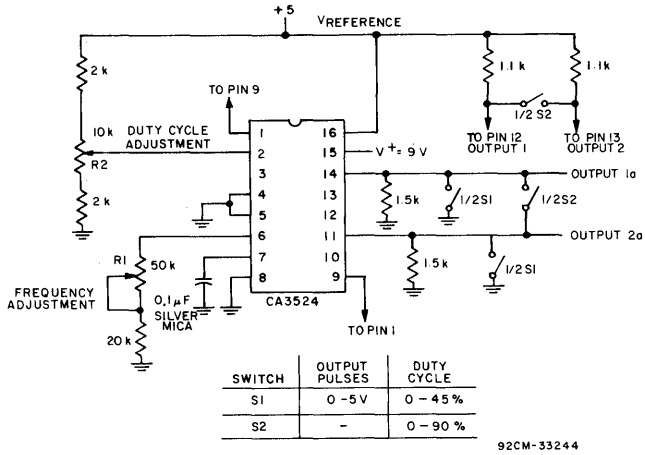


Fig. 25 - Low-frequency pulse generator.

The Variable Switcher

The circuit diagram of the CA1524, used as a variable-output-voltage power supply is shown in Fig. 26. By connecting the two output transistors in parallel, the duty cycle is doubled, i.e., 0-90%.

As the reference voltage level is varied, the feedback voltage will track that level and cause the output voltage to change according to the change in reference voltage.

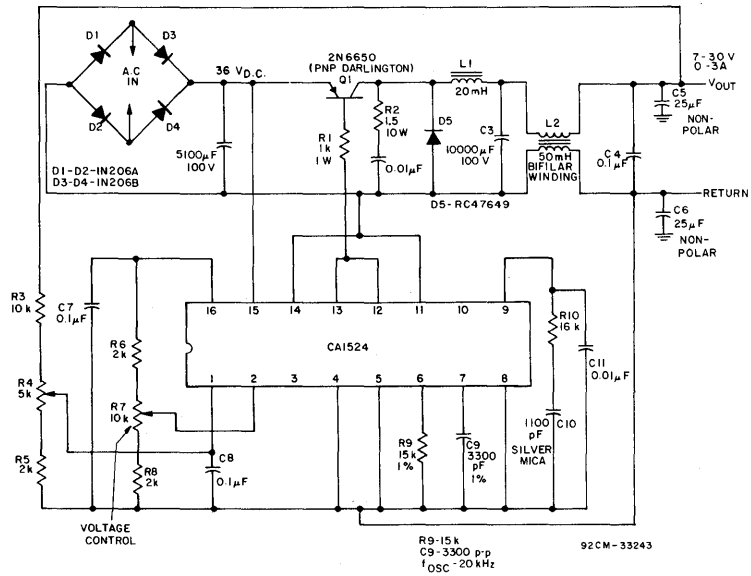


Fig. 26 - The CA1524 used as a 0-5 A, 7-30 V laboratory supply.

Digital Readout Scale

The CA1524 can be used as the driving source for an electronic scale application. The circuit shown in Figs. 27 and 28 uses half (Q2) of the CA1524 output in a low-voltage switching regulator (2.2 V) application to drive the LED's displaying the weight. The remaining output stage (Q1) is used as a driver for the sampling plates PL1 and PL2. Since the CA1524 contains a 5-volt internal regulator and a wide operating range of 8 to 40 volts, a single 9-volt battery can power the total system. The two plates, PL1 and PL2, are driven with opposite phase signals (frequency held constant but duty cycle may change) from the pulse-width modulator IC (CA1524). The sensor, S, is located between the two plates. Plates PL1, S and PL2 form an effective capacitance bridge-type divider network. As plate S is moved according to the object's weight, a change in capacitance is noted between PL1, S and PL2. This change is reflected as a voltage to the ac amplifier (CA3160). At the null position the signals from PL1 and PL2 as detected by S are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal at S becomes greater. The CA3160 ac amplifier provides a buffer for the small signal change noted at S. The output of the CA3160 is converted to a dc voltage by a peak-to-peak detector. A peak-to-peak detector is needed, since the duty cycle of the sampled waveform is subject to change. The detector output is filtered further and displayed via the CA3161E and CA3162E digital readout system, indicating the weight on the scale.

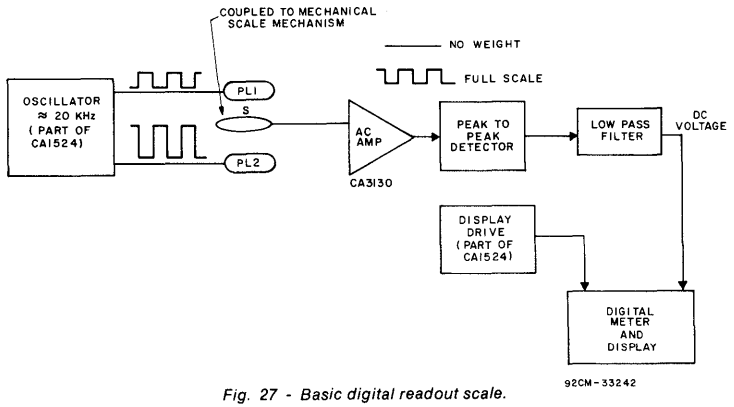


Fig. 27 - Basic digital readout scale.

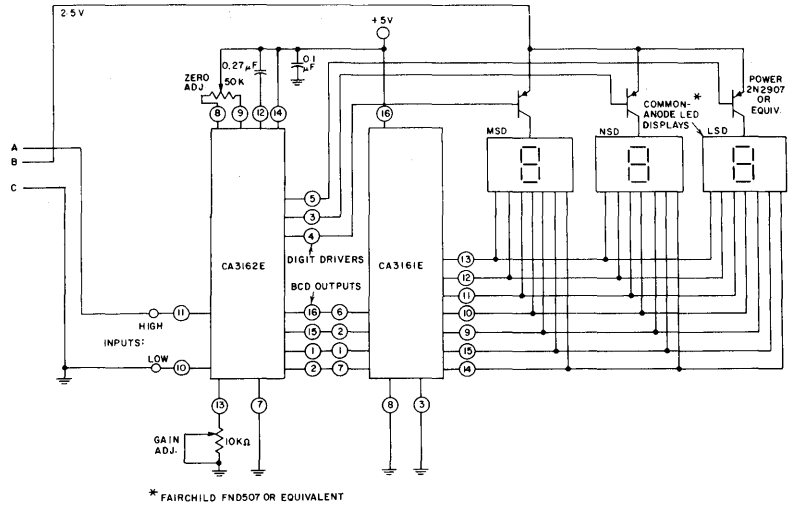


Fig. 28 - Schematic diagram of digital readout scale (cont'd).

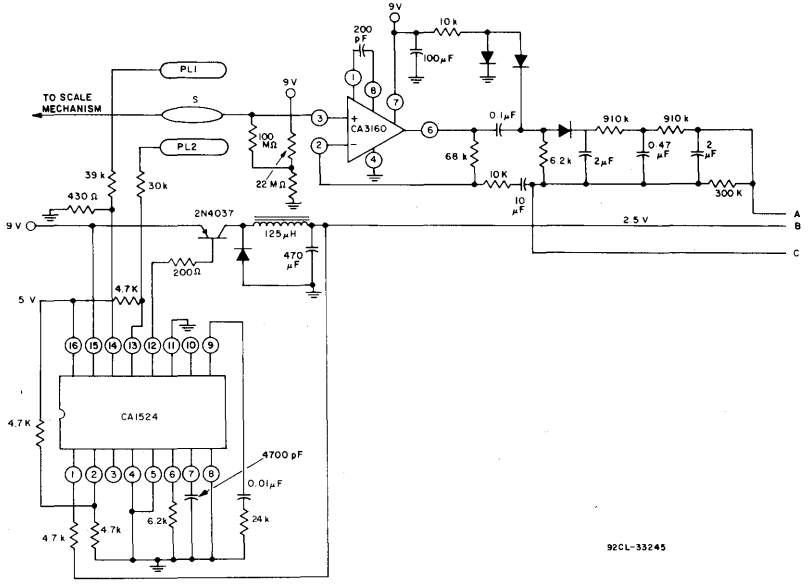
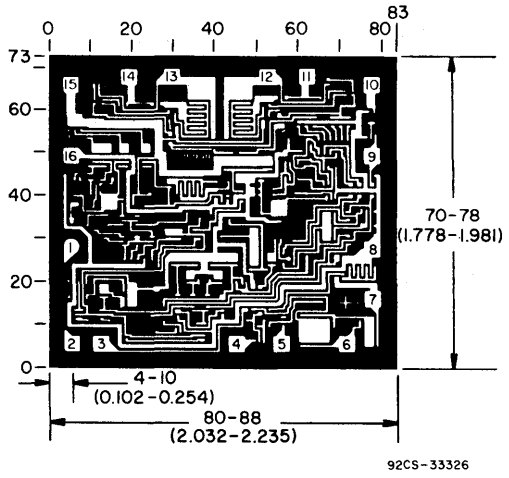


Fig. 28 - Schematic diagram of digital readout scale.



Dimensions and pad layout for CA3524H chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

May 1990

Zero-Voltage Switches

For 50/60 and 400 Hz Thyristor Control Applications

Features:

- *Relay control*
- *Valve control*
- *Synchronous switching of flashing lights*
- *On-off motor switching*
- *Differential comparator with self-contained power supply for industrial applications*
- *Photosensitive control*
- *Power one-shot control*
- *Heater control*
- *Lamp control*

The CA3059 and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24 V, 120 V, 208/230 V, and 277 V at 50/60 and 400 Hz. Each of the zero-voltage switches incorporates 4 functional blocks (see Fig. 1) as follows:

1. Limiter-Power Supply - Permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier - Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector - Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit - Provides high-current pulses to the gate of the power controlling thyristor.

In addition, the CA3059 provides the following important auxiliary functions (see Fig. 1).

1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

For an explanation of these functions see Operating Considerations. For detailed application information, see companion Application Note ICAN-6182, "Features and Applications of Integrated-Circuit Zero-Voltage Switches (CA3059 and CA3079)".

The CA3059 and CA3079 are supplied in 14-lead dual-in-line plastic packages. The CA3079 is also available in chip form (H suffix).

Features	CA3059	CA3079
■ *24 V, 120 V, 208/230 V, 277 V at 50/60, or 400 Hz operation*	√	√
■ *Differential Input*	√	√
■ *Low Balance Input Current (max.) -μA*	1	2
■ *Built-in Protection Circuit for opened or shorted sensor (Terminal 14)*	√	
■ *Sensor Range (Rx) -kΩ*	2 to 100	2 to 50
■ *DC Mode (Terminal 12)*	√	
■ *External Trigger (Terminal 6)*	√	
■ *External Inhibit (Terminal 1)*	√	
■ *DC Supply Volts (max.)*	14	10
■ *Operating Temperature Range - °C*	-55 to +125	

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C*

DC SUPPLY VOLTAGE (BETWEEN TERMS. 2 AND 7):
- CA3059 ..... 14 V
- CA3079 ..... 10 V

DC SUPPLY VOLTAGE, (BETWEEN TERMS. 2 AND 8):
- CA3059 ..... 14 V
- CA3079 ..... 10 V

PEAK SUPPLY CURRENT (TERMS. 5 AND 7) ..... ± 50 mA

OUTPUT PULSE CURRENT (TERM. 4) ..... 150 mA

POWER DISSIPATIONS:
- Up to TA = 55° C - CA3059, CA3079 ..... 700 mW
- Above TA = 55° C - CA3059, CA3079 ..... Derate linearly 6.67 mW/° C

AMBIENT TEMPERATURE RANGE:
- Operating ..... -55 to +125° C
- Storage ..... -65 to +150° C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL NO.	1 Note 3	2	3	4	5 Note 1	6 Note 3	7	8	9	10	11	12 Note 3	13	14 Note 2,3	MAXIMUM CURRENT RATINGS I_{IN} mA	MAXIMUM CURRENT RATINGS I_{OUT} mA
1 Note 3		*	*	*	*	15 0	10 -2	*	*	*	*	*	*	*	10	0.1
2			0 -15	0 -15	2 -14	0 -14	0▲ -14	0▲ -14	0 -14	0 -14	0 -14	* .	0 -14	0 -14	150	10
3				0 -15	*	*	*	*	*	*	*	*	*	*	*	*
4					*	2 -10	*	*	*	*	*	*	*	*	0.1	150
5 Note 1						*	7 -7	*	*	*	*	*	*	*	50	10
6 Note 3							14 0	*	*	*	*	*	*	*	*	*
7								*	14 0	*	20 0	2.5 -2.5	14 0	6 -6	*	*
8									10 0	*	*	*	*	*	0.1	2
9										*	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12 Note 3													*	*	50	50
13														*	*	*
14 Note 3															2	2

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to −10 volts.

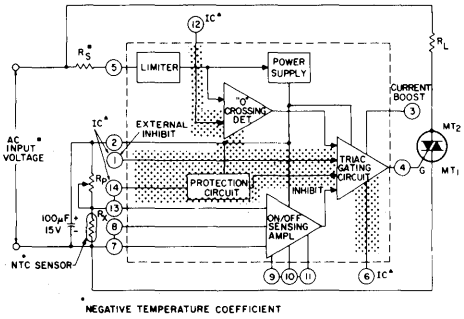
Note 1 – Resistance should be inserted between Terminal 5 and external supply or line voltage for limiting current into Terminal 5 to less than 50 mA.

Note 2 – Resistance should be inserted between Terminal 14 and external supply for limiting current into Terminal 14 to less than 2 mA.

Note 3 – For the CA3079 indicated terminal is internally connected and, therefore, should not be used.

▲For CA3079 (0 to −10 V).

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.



AC Input Voltage (50/60 or 400 Hz) V AC	Input Series Resistor (R_S) k Ω	Dissipation Rating for R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE:

Circuitry, within shaded areas, not included in CA3079

- See chart
- ▲ IC = Internal Connection - - DO NOT USE (Terminal Restriction applies only to CA3079).

Fig. 1 - Functional block diagram of CA3059 and CA3079.

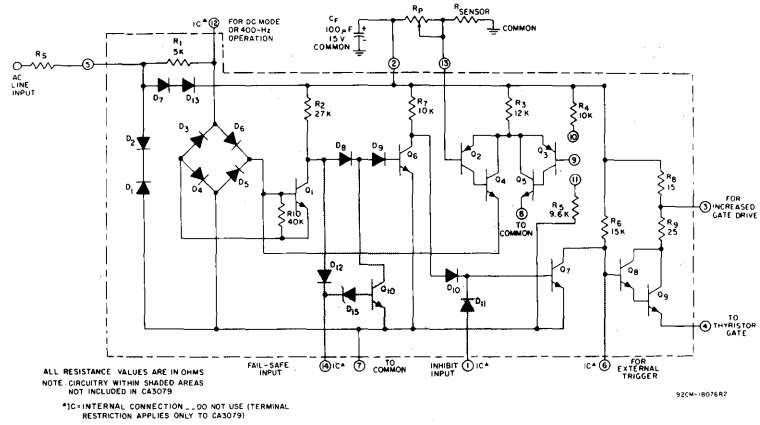


Fig. 2 - Schematic diagram of CA3059 and CA3079

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise)

All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS $T_A = 25^oC$ (Unless Indicated Otherwise)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)●					
DC Supply Voltage, V_S					
Inhibit Mode					
At 50/60 Hz	R_S = 8 kΩ, I_L = 0	6.1	6.5	7	V
At 400 Hz	R_S = 10 kΩ, I_L = 0	–	6.8	–	V
At 50/60 Hz	R_S = 5 kΩ, I_L = 2 mA	–	6.4	–	V
Pulse Mode					
At 50/60 Hz	R_S = 8 kΩ, I_L = 0	6	6.4	7	V
At 400 Hz	R_S = 10 kΩ, I_L = 0	–	6.7	–	V
At 50/60 Hz	R_S = 5 kΩ, I_L = 2 mA	–	6.3	–	V
At 50/60 Hz (CA3058) *See Fig. 3*	R_S = 8 kΩ, I_L = 0; T_A = −55 to +125°C	5.5	–	7.5	V

ELECTRICAL CHARACTERISTICS (For all types, unless indicated otherwise) (Cont'd)
All voltages are measured with respect to Terminal 7.

CHARACTERISTIC	TEST CONDITIONS $T_A = 25^oC$ (Unless Indicated Otherwise)	LIMITS			UNITS
		Min.	Typ.	Max.	
For Operating at 120 V rms, 50-60 Hz (AC Line Voltage)•					
Gate Trigger Current, I_{GT}[4] *See Figs. 4, 5(a)*	Terms. 3 and 2 connected, V_{GT} = 1 V	–	105	–	mA
Peak Output Current (Pulsed), I_{OM}[4] With Internal Power Supply	Term. 3 open, Gate Trigger Voltage (V_{GT}) = 0	50	84	–	mA
	Terms. 3 and 2 connected, Gate Trigger Voltage (V_{GT})=0	90	124	–	mA
	Term. 3 open, V^+=12 V, V_{GT}=0	–	170	–	mA
With External Power Supply *See Figs. 5, 6*	Terms. 3 and 2 connected, V^+=12 V, V_{GT} = 0	–	240	–	mA
Inhibit Input Ratio, V_9/V_2 *See Fig. 7*	Voltage Ratio of Term. 9 to 2	0.465	0.485	0.520	–
Total Gate Pulse Duration:* For positive dv/dt, t_P 50-60 Hz	C_{EXT} = 0	70	100	140	μs
400 Hz	C_{EXT} = 0, R_{EXT} = ∞	–	12	–	μs
For negative dv/dt, t_N 50-60 Hz	C_{EXT} = 0	70	100	140	μs
400 Hz *See Fig. 8*	C_{EXT} = 0, R_{EXT} = ∞	–	10	–	μs
Pulse Duration After Zero Crossing (50-60 Hz): For positive dv/dt, t_{P1}	C_{EXT} = 0	–	50	–	μs
For negative dv/dt, t_{N1} *See Fig. 8*	R_{EXT} = ∞	–	60	–	μs
Output Leakage Current, I_4 Inhibit Mode: *See Fig. 9*		–	0.001	10	μA
Input Bias Current, I_I CA3059		–	220	1000	nA
CA3079 *See Fig. 10*		–	220	2000	nA
Common-Mode Input Voltage Range, V_{CMR}	Terms. 9 and 13 connected	–	1.5 to 5	–	V
Sensitivity, $\Delta V_{13}^{\neq}$ (Pulse Mode) *See Figs. 5(a), 12*	Term. 12 open	–	6	–	mV

≠ Required voltage change at Term. 13 to either turn OFF the triac when ON or turn ON the triac when OFF.

* Pulse duration in 50 Hz applications is approximately 15% longer than shown in Fig. 8(b).

• The values given in the Electrical Characteristics Chart at 120 V also apply for operation at input voltages of 208/230 V, and 277 V, except for Pulse Duration. However, the series resistor (RS) must have the indicated value, shown in the chart in Fig. 1, for the specified input voltage.

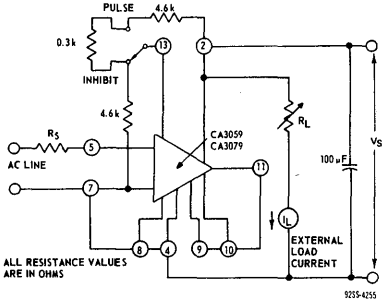


Fig. 3(a)—DC supply voltage test circuit for CA3059 and CA3079.

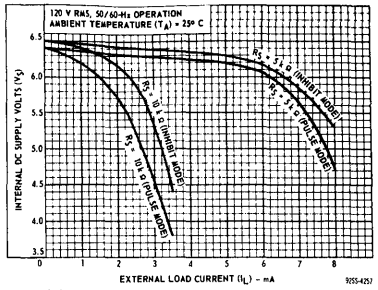


Fig. 3(c)—DC supply voltage vs. external load current for CA3059 and CA3079.

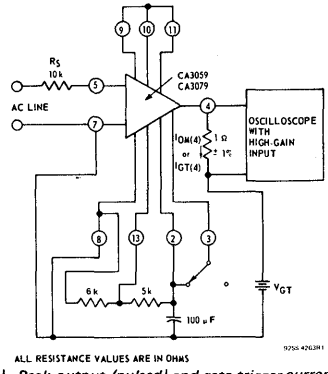


Fig. 5(a)—Peak output (pulsed) and gate trigger current with internal power supply test circuit for CA3059 and CA3079.

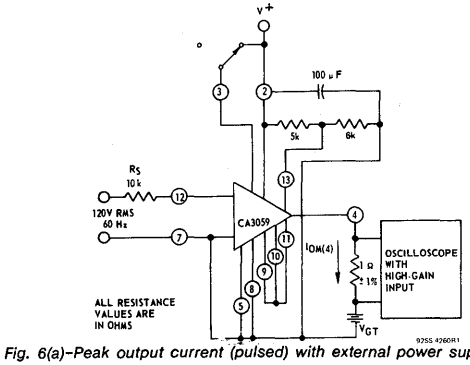


Fig. 6(a)-Peak output current (pulsed) with external power supply test curcuit for CA3059.

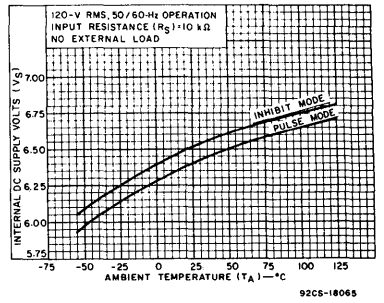


Fig. 3(b)—DC supply voltage vs. ambient temperature for CA3059 and CA3079.

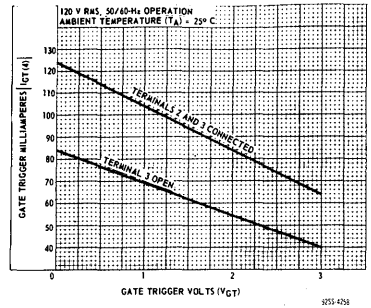


Fig. 4—Gate trigger current vs. gate trigger voltage for CA3059 and CA3079.

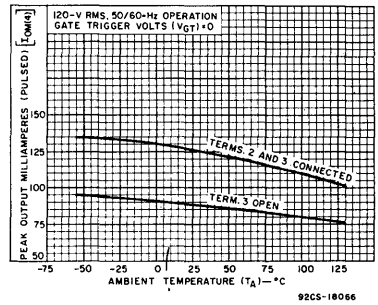


Fig. 5(b)—Peak output current (pulsed) vs. ambient temperature for CA3059 and CA3079.

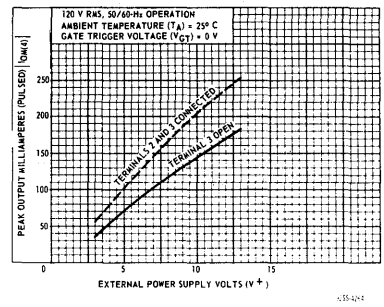


Fig. 6(b)—Peak output current (pulsed) vs. external power supply voltage for CA3059.

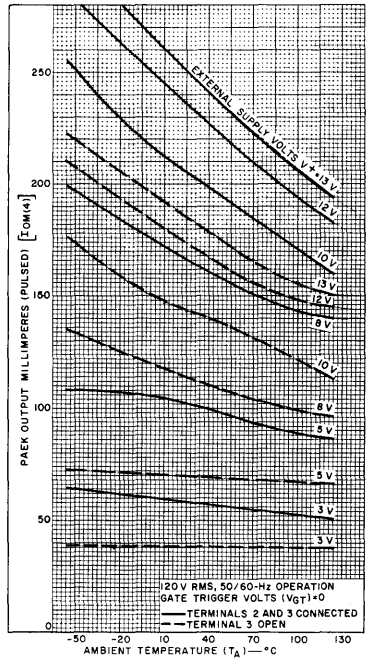


Fig. 6(c) – Peak output current (pulsed) vs ambient temperature for CA3059.

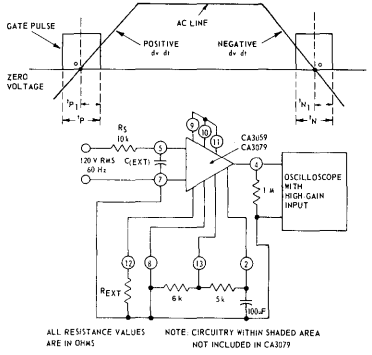


Fig. 8(a) – Gate pulse duration test circuit with associated waveform for CA3059 and CA3079.

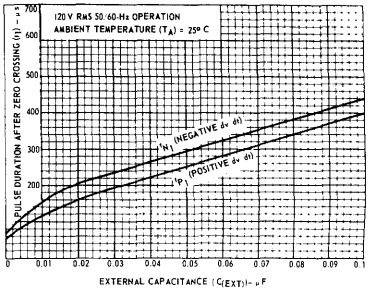


Fig. 8(c) – Pulse duration after zero crossing vs external capacitance for CA3059 and CA3079.

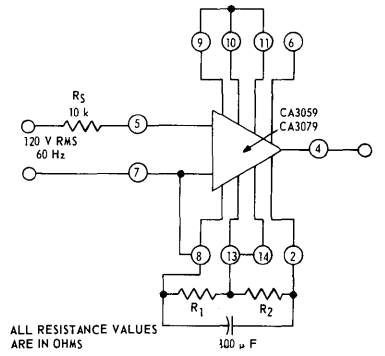


Fig. 7(a) – Input inhibit voltage ration test circuit for CA3059 and CA3079.

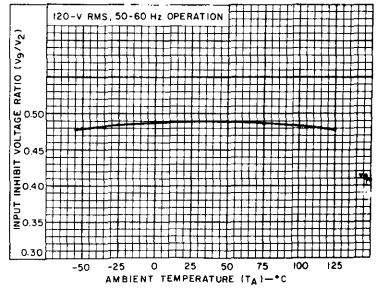


Fig. 7(b) – Input inhibit voltage ratio vs ambient temperature for CA3059 and CA3079.

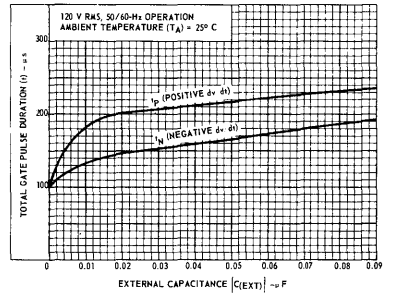


Fig. 8(b) – Total gate pulse duration vs external capacitance for CA3059 and CA3079.

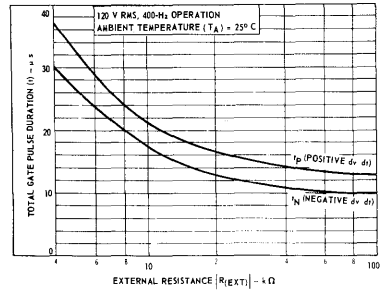


Fig. 8(d) – Total gate pulse duration vs external resistance for CA3059.

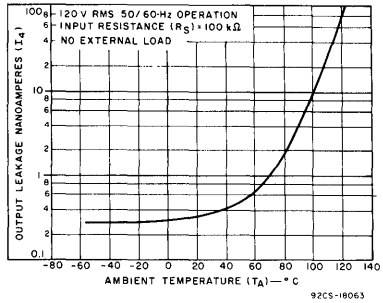


Fig. 9—Output leakage current (inhibit mode) vs. ambient temperature for CA3059 and CA3079.

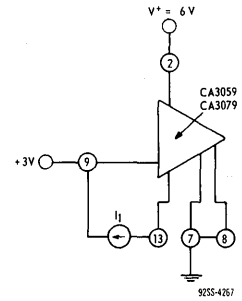
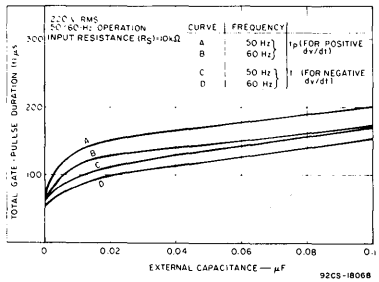
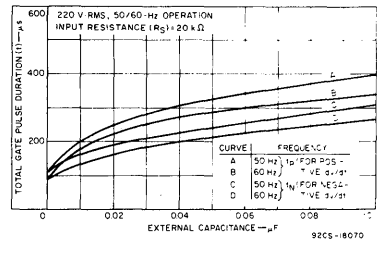


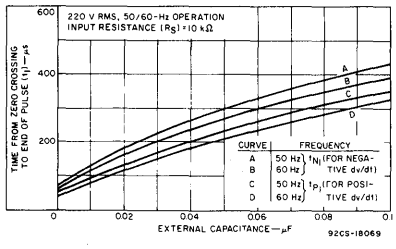
Fig. 10—Input bias current test circuit for CA3059 and CA3079.



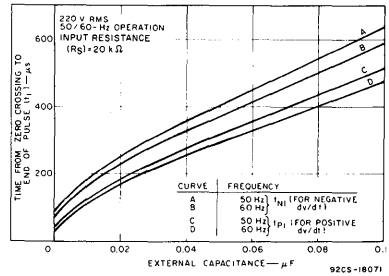
(a)



(b)



(c)



(d)

Fig. 11—Relative pulse width and location of zero crossing for 220-volt operation for CA3059 and CA3079.

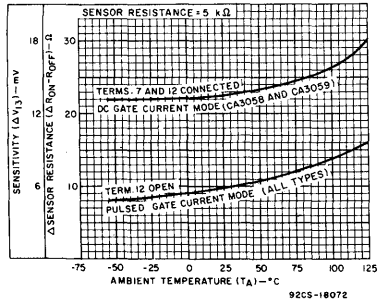


Fig. 12—Sensitivity vs. ambient temperature for CA3059 and CA3079.

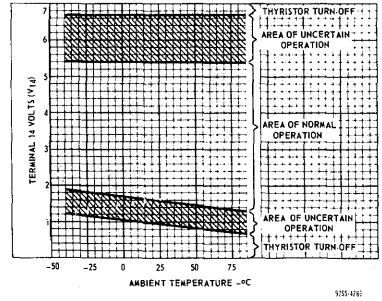


Fig. 13—Operating regions for built-in protection circuit for CA3059.

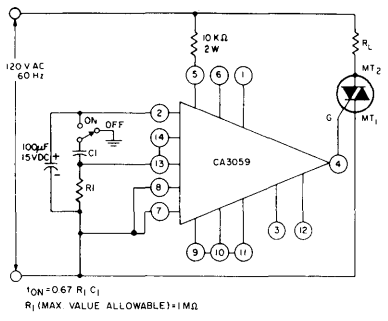


Fig. 14—Line-operated one-shot timer.

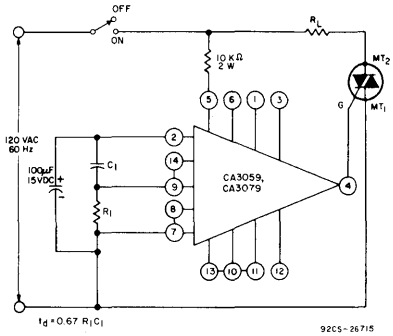


Fig. 15—Line-operated thyristor control time delay turn-on circuit.

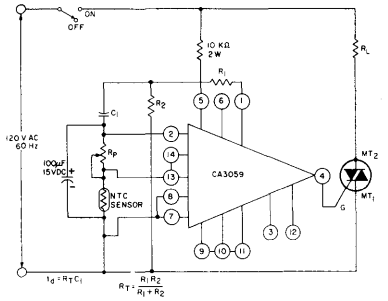


Fig. 16—On/off temperature control circuit with delayed turn-on.

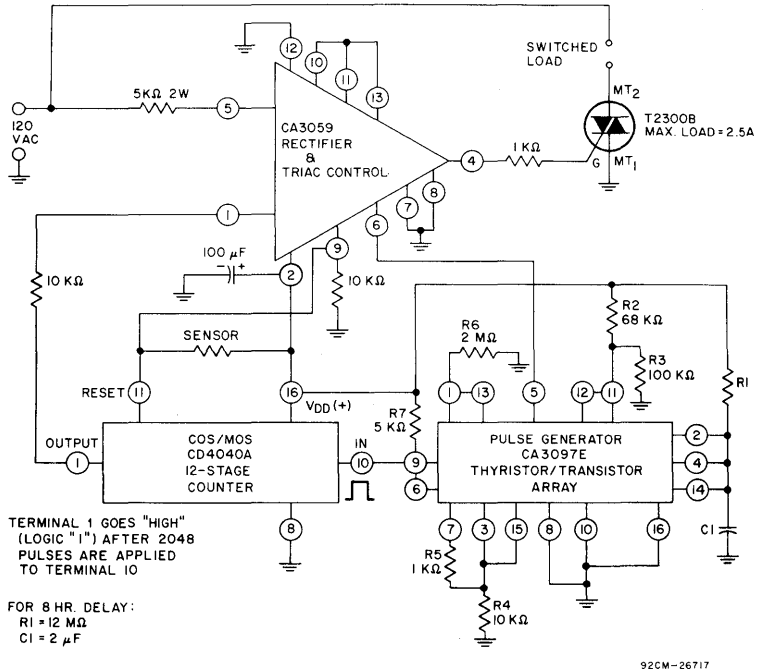


Fig. 17(a)—Line-operated IC timer for long time periods.

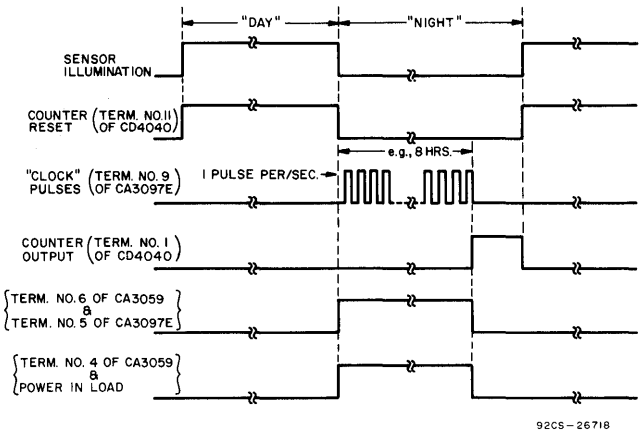


Fig. 17(b)—Timing diagram for Fig. 17(a).

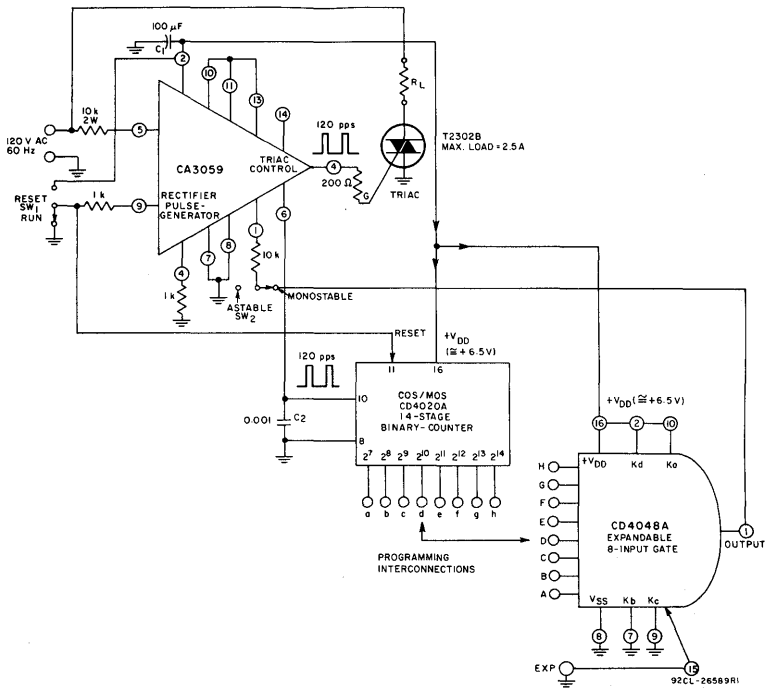


Fig. 18(a)—Programmable ultra-accurate line-operated timer. (Programmable over the range from 0.5333 seconds to 2 minutes, 16 seconds in 0.5333-second increments)

Time Periods (t = 0.5333 s)	1 t	2 t	4 t	8 t	16 t	32 t	64 t	128 t	t_o
Terminals									
CD4020A	a	b	c	d	e	f	g	h	
CD4048A	A	B	C	D	E	F	G	H	
	C	NC	NC	NC	NC	NC	NC	NC	1 t
	NC	C	NC	NC	NC	NC	NC	NC	2 t
	C	C	NC	NC	NC	NC	NC	NC	3 t
	NC	NC	C	NC	NC	NC	NC	NC	4 t
	C	NC	C	NC	NC	NC	NC	NC	5 t
	NC	C	C	NC	NC	NC	NC	NC	6 t
	C	C	C	NC	NC	NC	NC	NC	7 t
	NC	NC	NC	C	NC	NC	NC	NC	8 t
	C	NC	NC	C	NC	NC	NC	NC	9 t
	NC	C	NC	C	NC	NC	NC	NC	10 t
	C	C	NC	C	NC	NC	NC	NC	11 t
	NC	NC	C	C	NC	NC	NC	NC	12 t
	C	NC	C	C	NC	NC	NC	NC	13 t
	NC	C	C	C	NC	NC	NC	NC	14 t
	C	C	C	C	NC	NC	NC	NC	15 t
	C	C	C	C	NC	C	C	NC	111 t
	NC	NC	NC	NC	C	C	C	NC	112 t
	C	NC	NC	NC	C	C	C	NC	113 t
	C	C	C	C	C	C	C	C	255 t

Notes:

t_o = Total time delay = $n_1\,t + n_2\,t + \ldots n_n t$.

C = Connect. For example, interconnect terminal a of the CD4020A and terminal A of the CD4048A.

NC = No Connection. For example, terminal b of the CD4020A open and terminal B of the CD4048A connected to $+V_{DD}$ bus.

Fig. 18(b)—"Programming" table for Fig. 18(a).

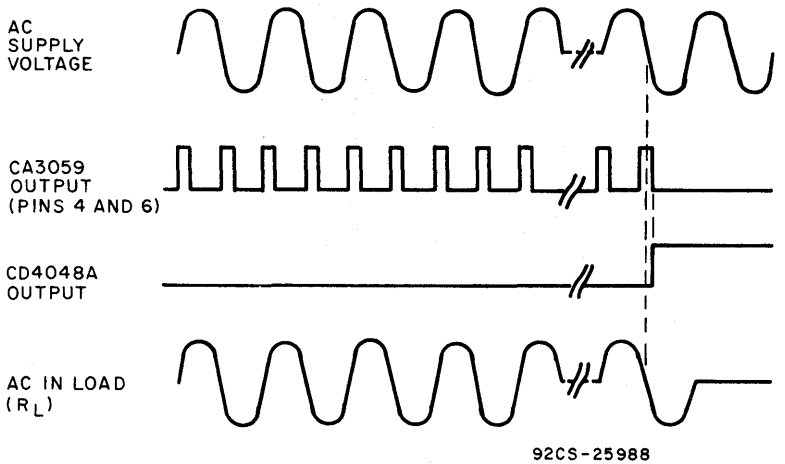


Fig. 18(c)—Timing diagram for Fig. 18(a).

OPERATING CONSIDERATIONS

Power Supply Considerations for CA3059 and CA3079

The CA3059 and CA3079 are intended for operation as self-powered circuits with the power supplied from an AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figs. 3(b) and 3(c).

Power Supply Considerations for CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Fig. 5 for the peak output current characteristics). When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Fig. 5(a).

Operation of Built-in Protection for the CA3059

A special feature of the CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in Fig. 1. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2 mA with a 5 kΩ dropping resistor.
2. Set the value of R_P and sensor resistance (R_X) between 2 kΩ and 100 kΩ.
3. The ratio of R_X to R_P, typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Fig. 13.

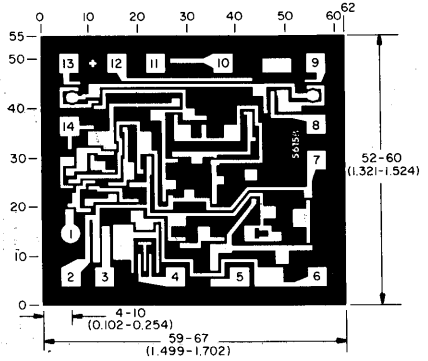
External Inhibit Function for the CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2 V at 10 μA will remove drive from the thyristor. This required level is compatible with DTL or T^2L logic. A logical 1 activates the inhibit function.

DC Gate Current Mode for the CA3059

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.

For a list of RCA thyristors, see RCA Thyristor Data Bulletin, File No. 406, dated 5-75.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid gradations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for CA3059H.

May 1990

Positive Voltage Regulators

For Regulated Voltages from 1.7 V to 46 V at Currents up to 100 mA

Features:

- *Up to 100 mA output current*
- *Input and output short-circuit protection*
- *Load and line regulation: 0.025%*
- *Pin compatible with LM100 Series*
- *Adjustable output voltage*

Applications:

- *Shunt voltage regulator*
- *Current regulator*
- *Switching voltage regulator*
- *High-current voltage regulator*
- *Combination positive and negative voltage regulator*
- *Dual tracking regulator*

The CA3085, CA3085A, and CA3085B are silicon monolithic integrated circuits designed specifically for service as voltage regulators at output voltages ranging from 1.7 to 46 volts at currents up to 100 milliamperes.

A block diagram of the CA3085 Series is shown in Fig. 1. The diagram shows the connecting terminals that provide access to the regulator circuit components. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

The CA3085A and CA3085B have output current capabilities up to 100 mA and the CA3085 up to 12 mA without the use of external pass transistors. However, all the devices can provide voltage regulation at load currents greater than 100 mA with the use of suitable external pass transistors. The CA3085 Series has an unregulated input voltage ranging from 7.5 to 30 V (CA3085), 7.5 to 40 V (CA3085A), and 7.5 to 50 V (CA3085B) and a minimum regulated output voltage of 26 V (CA3085), 36 V (CA3085A), and 46 V (CA3085B).

The CA3085A is unilaterally interchangeable with the CA3055.

These types are supplied in the 8-lead TO-5 style package (CA3085, CA3085A, CA3085B, and the 8-lead TO-5 with dual-in-line formed leads ("DIL-CAN", CA3085S, CA3085AS, CA3085BS). The CA3085 is also supplied in the 8-lead dual-in-line plastic package ("MINI-DIP", CA3085E), and in chip form (CA3085H).

TYPE	VIN RANGE V	VOUT RANGE V	MAX. IOUT mA	MAX. LOAD REGULATION % VOUT
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

*This value may be extended to 100 mA; however, regulation is not specified beyond 12 mA.

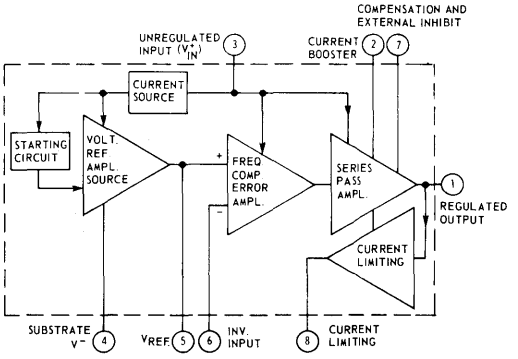


Figure 1 - Block diagram of CA3085 Series.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES at T_A = 25°C

POWER DISSIPATION: WITHOUT HEAT SINK	WITH HEAT SINK (TO-5 ONLY)
up to T_A = 55°C ..... 630 mW	up to T_C = 55°C .... 1.6 W
above T_A = 55°C derate linearly @6.67 mW/°C	above T_C = 55°C .... derate linearly at 16.7 mW/°C

TEMPERATURE RANGE:

Operating ..... −55 to +125°C
Storage ..... −65 to +150°C

UNREGULATED INPUT VOLTAGE:

CA3085 ..... 30 V
CA3085A ..... 40 V
CA3085B ..... 50 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. ..... +265°C

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal No. 7 and horizontal Terminal No. 1 is +3 to −10 volts.

MAXIMUM VOLTAGE RATINGS

TERMINAL No.	5	6	7	8	1	2	3	4
5	–	+5 −5	•	•	•	•	•	+10 0
6	–	–	•	•	•	•	•	•
7	–	–	–	+3 −10	+3 −10	•	•	+‡ 0
8	–	–	–	–	+5 −1	•	•	•
1	–	–	–	–	–	+10 −‡	0 −‡	+‡ 0
2	–	–	–	–	–	–	0 –	+‡ 0
3	–	–	–	–	–	–	–	+‡ 0
4	–	–	–	–	–	–	–	Substrate & Case

*Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

‡30 V for CA3085
40 V for CA3085A
50 V for CA3085B

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
5	10	1.0
6	1.0	−0.1
7	1.0	−1.0
8	0.1	10
1	20	150
2	150	60
3	150	60
4	–	–

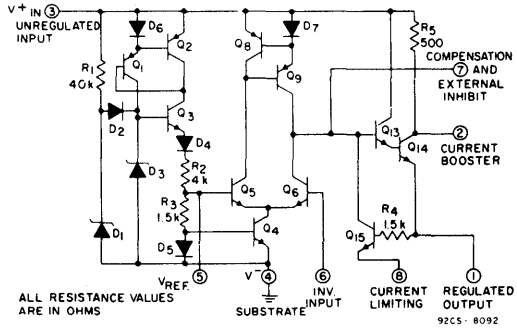


Fig.2—Schematic diagram of CA3085 Series.

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS: Test Circuit Fig. No.	TEST CONDITIONS: T_A = 25°C (Unless indicated otherwise)		CA3085 MIN.	CA3085 TYP.	CA3085 MAX.	CA3085A MIN.	CA3085A TYP.	CA3085A MAX.	CA3085B MIN.	CA3085B TYP.	CA3085B MAX.	UNITS
Reference Voltage	V_{REF}	4	V^+_{IN} = 15V		1.4	1.6	1.8	1.5	1.6	1.7	1.5	1.6	1.7	V
Quiescent Regulator Current	$I_{quiescent}$	4	V^+_{IN} = 30V		–	3.3	4.5	—	–	–	–	–	–	mA
			V^+_{IN} = 40V		–	–	–	–	3.65	5	–	–	–	
			V^+_{IN} = 50V		–	–	–	–	–	–	–	4.05	7	
Input Voltage Range	$V_{IN(range)}$	–	–		7.5	–	30	7.5	–	40	7.5	–	50	V
Maximum Output Voltage	$V_{O(max.)}$	4	V^+_{IN} = 30, 40, 50V#; R_L = 365Ω; Term. No. 6 to Gnd.		26	27	–	36	37	–	46	47	–	V
Minimum Output Voltage	$V_{O(min.)}$	4	V^+_{IN} = 30V		–	1.6	1.8	–	1.6	1.7	–	1.6	1.7	V
Input-Output Voltage Differential	V_{IN}-V_{OUT}	–	–		4	–	28	4	–	38	3.5	–	48	V
Limiting Current	I_{LIM}	7	V^+_{IN} = 16V, V^+_{OUT} = 10V R_{SCP}* = 6Ω		–	96	120	–	96	120	–	96	120	mA
Load Regulation●	–	–	I_L = 1 to 100mA, R_{SCP} = 0		–	–	–	–	0.025	0.15	–	0.025	0.15	%V_{OUT}
		–	I_L = 1 to 100mA, R_{SCP} = 0 T_A = 0°C to +70°C		–	–	–	–	0.035	0.6	–	0.035	0.6	
		–	I_L = 1 to 12mA, R_{SCP} = 0		–	0.003	0.1	–	–	–	–	–	–	
Line Regulation▲	–	–	I_L = 1mA, R_{SCP} = 0		–	0.025	0.1	–	0.025	0.075	–	0.025	0.04	%/V
		–	I_L = 1mA, R_{SCP} = 0 T_A = 0°C to +70°C		–	0.04	0.15	–	0.04	0.1	–	0.04	0.08	
Equivalent Noise Output Voltage	V_{NOISE}	11	V^+_{IN} = 25V	C_{REF} = 0	–	0.5	–	–	0.5	–	–	0.5	–	mV p-p
				C_{REF} = 0.22μF	–	0.3	–	–	0.3	–	–	0.3	–	
Ripple Rejection	–	12	V^+_{IN} = 25V f = 1kHz	C_{REF} = 0	–	50	–	–	50	–	45	50	–	dB
				C_{REF} = 2μF	–	56	–	–	56	–	50	56	–	
Output Resistance	r_o	12	V^+_{IN} = 25V, f = 1kHz		–	0.075	1.1	–	0.075	0.3	–	0.075	0.3	Ω
Temperature Coefficient of Reference and Output Voltages	$\Delta V_{REF}/\Delta V_o$	–	I_L = 0, V_{REF} = 1.6V		–	0.0035	–	–	0.0035	–	–	0.0035	–	%/°C
Load Transient Recovery Time: Turn On	t_{ON}	16	V^+_{IN} = 25V, +50mA Step		–	1	–	–	1	–	–	1	–	μs
Turn Off	t_{OFF}		V^+_{IN} = 25V, −50mA Step		–	3	–	–	3	–	–	3	–	μs
Line Transient Recovery Time: Turn On	t_{ON}	–	V^+_{IN} = 25V, f = 1kHz, 2V Step		–	0.8	–	–	0.8	–	–	0.8	–	μs
Turn Off	t_{OFF}	–			–	0.4	–	–	0.4	–	–	0.4	–	μs

30V (CA3085), 40V(CA3085A), 50V(CA3085B)

* R_{SCP}: Short-circuit protection resistance

● Load Regulation = $\frac{\Delta V_{OUT}}{V_{OUT(initial)}} \times 100\%$

▲ Line Regulation = $\frac{(\Delta V_{OUT})}{[V_{OUT(initial)}]\ (\Delta V_{IN})} \times 100\%$

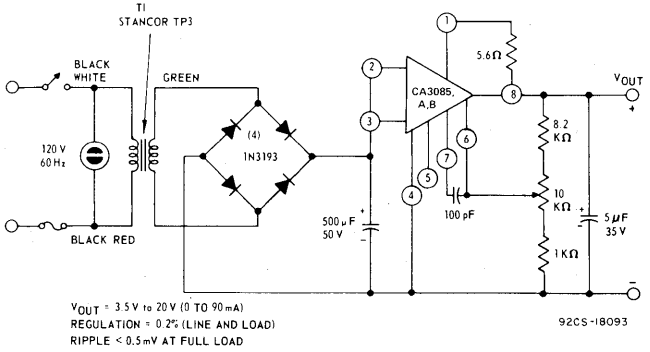
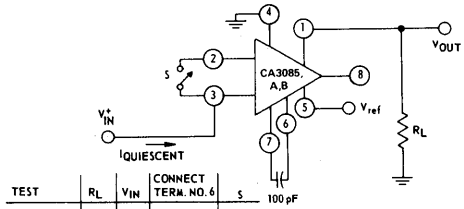


Fig.3—Application of the CA3085 Series in a typical power supply.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES



TEST	R_L	V_{IN}	CONNECT TERM. NO. 6	S
$V_{REF.}$	∞	+1.6	OPEN	OPEN
$I_{QUIESCENT}$	∞	+40	OPEN	OPEN
V_{OUT} (MAX.)	365Ω	+40	GROUND	CLOSED
V_{OUT} (MIN.)	10k	+30	TERM. NO. 1	OPEN

Fig.4—Test circuit for V_{REF}, $I_{quiescent}$, V_{OUT}(max.), V_{OUT}(min.).

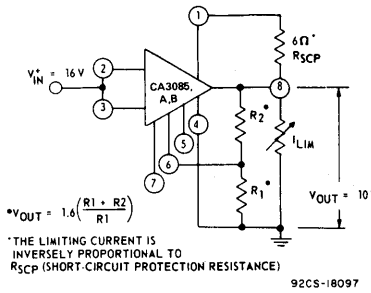


Fig.7—Test circuit for limiting current

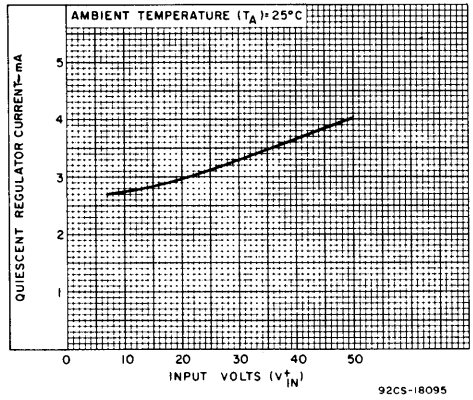


Fig.5—$I_{quiescent}$ vs. V^+_{IN}.

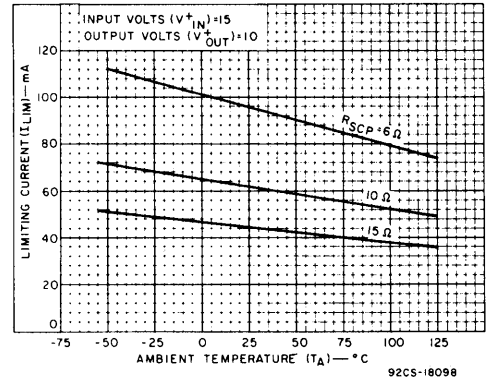


Fig.8—I_{LIM} vs. T_A.

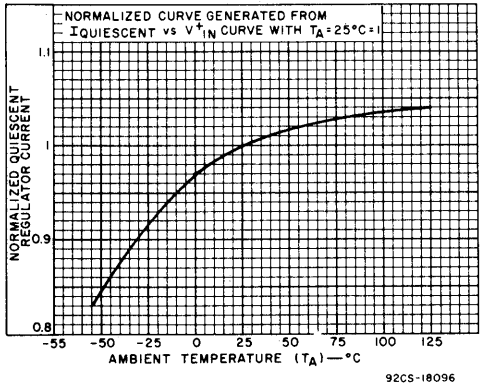


Fig.6—Normalized $I_{quiescent}$ vs. T_A.

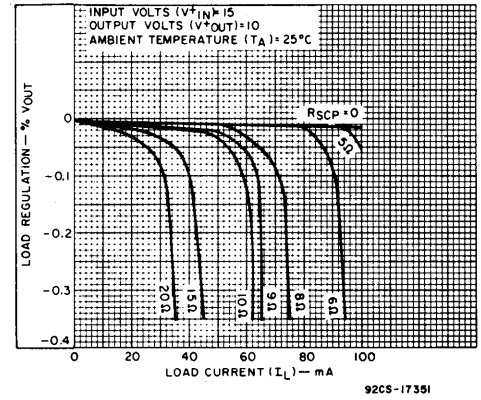


Fig.9—Load regulation characteristics.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES

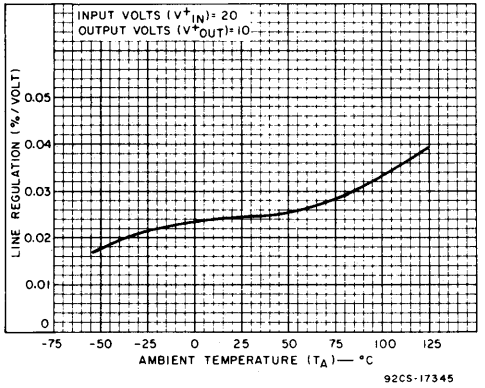


Fig.10—Line regulation temperature characteristics.

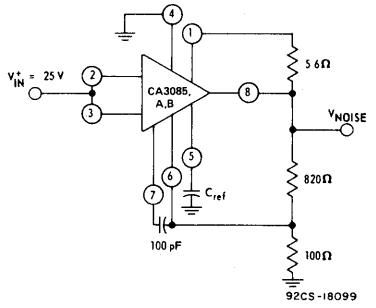


Fig.11—Test circuit for noise voltage.

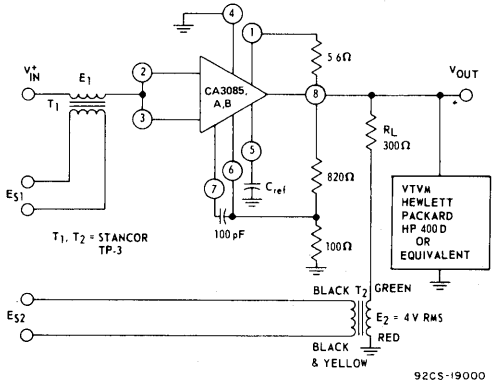


Fig.12—Test circuit for ripple rejection and output resistance.

TEST PROCEDURES FOR TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

Output Resistance

Conditions:

1. V_{IN} = +25 V, C_{REF} = 0, Short E_1
2. Set E_{S2} at 1 kHz so that E_2 = 4 V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate R_{OUT} from $R_{OUT} = V_{OUT}(R_L/E_2)$

Ripple Rejection — I

Conditions:

1. V_{IN} = +25 V, C_{REF} = 0, Short E_2
2. Set E_{S1} at 1 kHz so that E_1 = 3 V rms
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or equivalent
4. Calculate Ripple Rejection from 20 log (E_1/V_{OUT})

Ripple Rejection — II

Conditions:

1. Repeat Ripple Rejection I with C_{REF} = 2 μF

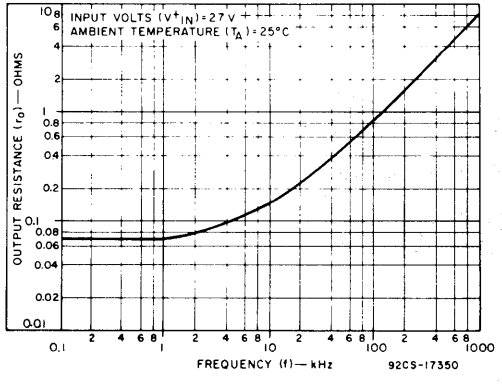


Fig.13—r_o vs. f.

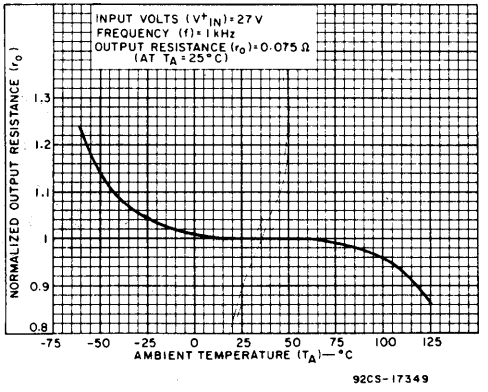


Fig.14—Normalized r_o vs. T_A.

TEST CIRCUIT AND TYPICAL CHARACTERISTICS CURVES FOR CA3085 SERIES

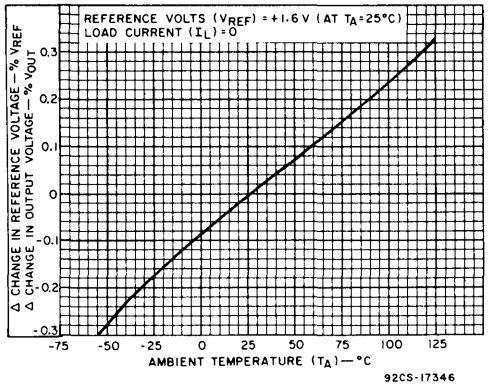


Fig.15—Temperature coefficient of V_{REF} and V_{OUT}.

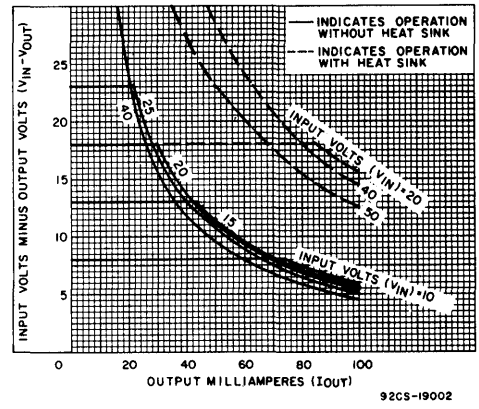


Fig.17—Dissipation limitation (V_{IN}–V_{OUT} vs. I_{OUT}).

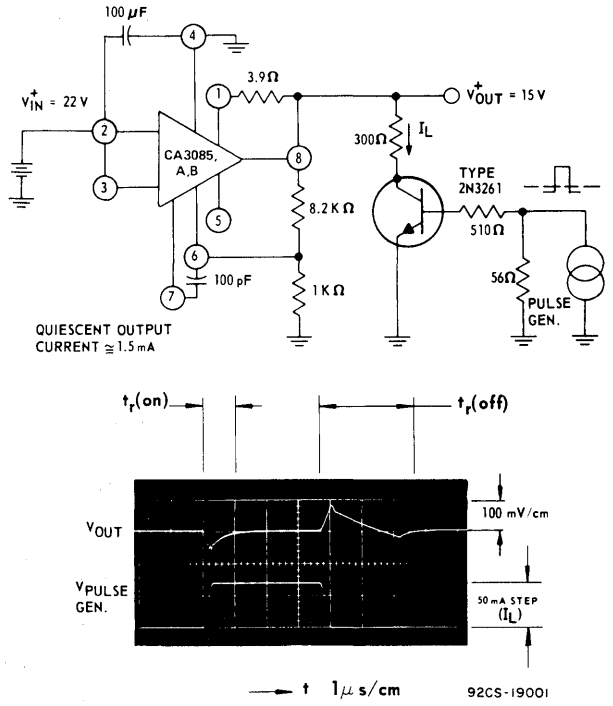


Fig.16—Turn-on and turn-off recovery time test circuit with associated waveforms.

TYPICAL REGULATOR CIRCUITS USING THE CA3085 SERIES

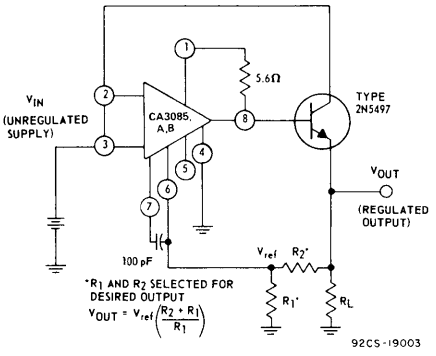


Fig.18—Typical high-current voltage regulator circuit.

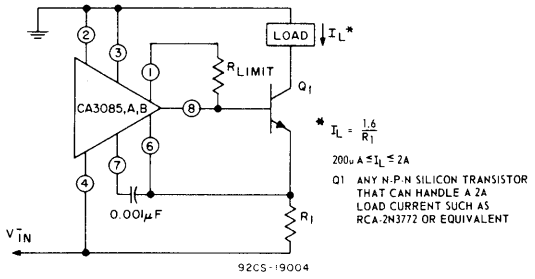


Fig.19—Typical current regulator circuit.

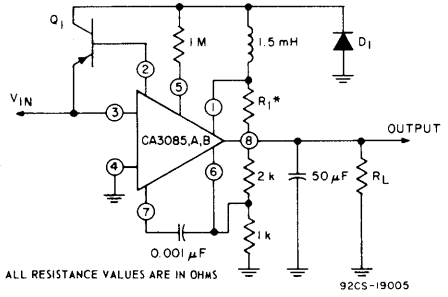
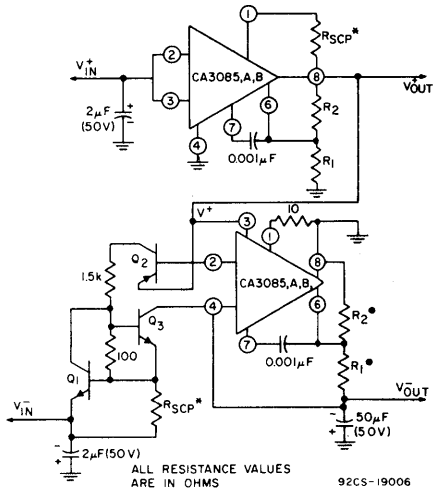


Fig.20—Typical switching regulator circuit.



ALL RESISTANCE VALUES ARE IN OHMS

Q1 RCA-2N2102 OR EQUIVALENT

Q2 ANY P-N-P SILICON TRANSISTOR (RCA-2N5322 OR EQUIVALENT)

Q3 ANY N-P-N SILICON TRANSISTOR THAT CAN HANDLE THE DESIRED LOAD CURRENT (RCA-2N3772 OR EQUIVALENT)

$*V_{OUT} = \left(\frac{R_1 + R_2}{R_1}\right)$

*R_{SCP}: SHORT-CIRCUIT PROTECTION RESISTANCE

Fig.21—Combination positive and negative voltage regulator circuit.

HARRIS

HV-1205

May 1990

Single Chip Power Supply

Features

- Direct AC to DC Conversion
- Wide Input Voltage Range 18Vrms-132Vrms
- Wide Input Frequency Range 48Hz-440Hz
- Guaranteed Output Current 50mA
- Output Voltage ..... 5V to 24V
- Line and Load Regulation ..... <5%
- Surge Protection per IEEE 587 Category A & B Using MOV

Applications

- Compact, Low Cost, Power Supply for Non-Isolated Applications
- High Efficiency Regulator for 26 VAC Systems
- Battery Back-Up Systems
- Dual Output Supply for OFF-LINE Motor Controls

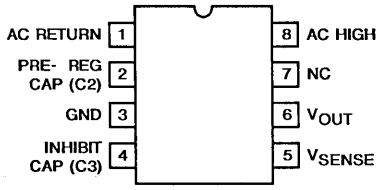
Description

The HV-1205 is a single chip power supply that can supply 5V to 24V at 50mA output current. Just a few inexpensive external components are needed to provide a compact, light weight, cost effective power supply. The HV-1205 replaces a transformer, rectifier, and voltage regulator. This chip is made in the new Harris High Voltage Dielectric Isolation Process. This high breakdown process (400V) allows a patented switching circuit to draw current from the AC line only as necessary to supply the load. The HV-1205 operates from -40°C to +85°C (with no derating necessary due to package power dissipation). The HV-1205 is available in an 8 Pin Plastic Mini-DIP.

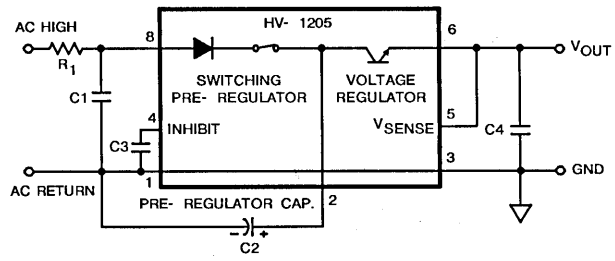
CAUTION: This Product Does Not Provide Isolation From the AC Line

Pinout

HV3-1205 (PLASTIC MINI-DIP)
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

Voltage Between Pin 1 and 8, Continuous Vrms 132Vrms
Voltage Between Pin 1 and 8, Peak 400V
Voltage Between Pin 2 and 6 ..... 15V
Input Current, Peak 1.1A
Output Current ..... Short Circuit Protected
Output Voltage 30V
Maximum Junction Temperature..... +150°C

Operating Temperature Range

HV3-1205-9..... -40°C to +85°C
HV3-1205-5..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +175°C

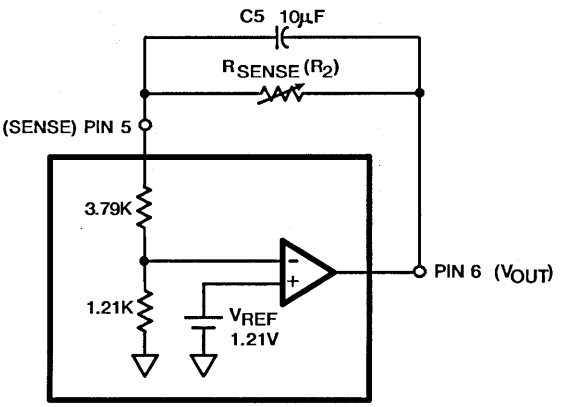
Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Plastic DIP	82	16

Electrical Specifications Unless Otherwise Specified: V_{IN} =120Vrms at 60Hz, C1 = 0.05µF, C2 = 470µF, C3 = 150pF, V_{OUT} = 5V, I_{OUT} = 50mA, Source Impedance, R_1 = 150Ω. Parameters are Guaranteed at the Specific V_{IN} and Frequency Conditions, Unless Otherwise Specified. See Functional Diagrams for Component Location.

PARAMETER	V_{IN}	TEMP	HV-1205-9 -40°C to +85°C			HV-1205-5 0°C to +75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage (At Preset 5V)	120V	+25°C	4.75	5.0	5.25	4.75	5.0	5.25	V
	120V	Full	4.65	5.0	5.35	4.65	5.0	5.35	V
Output Voltage TC	120V	Full	-	0.02	-	-	0.02	-	%/°C
Output Ripple (Vp-p) (C4 = 1µF, f = 60Hz)	120V	+25°C	-	10	-	-	10	-	mV
	120V	Full	-	20	-	-	20	-	mV
Line Regulation	80Vrms to 132Vrms	+25°C	-	-	15	-	-	20	mV
		Full	-	-	30	-	-	40	mV
Load Regulation (I_{OUT} = 5mA to 50mA)	120V	+25°C	-	-	15	-	-	20	mV
	120V	Full	-	-	30	-	-	40	mV
Output Current	120V	Full	0	-	50	0	-	50	mA
Short Circuit Current Limit	120V	Full	55	95	-	55	95	-	mA
Drop-Out Voltage	Pin 2 - Pin 6	+25°C	-	2.2	-	-	2.2	-	V
Quiescent Current Post Regulator	11V_{DC} to 30V_{DC} On Pin 2	+25°C	-	2	-	-	2	-	mA

Equivalent Circuit For Output Voltage Adjustment

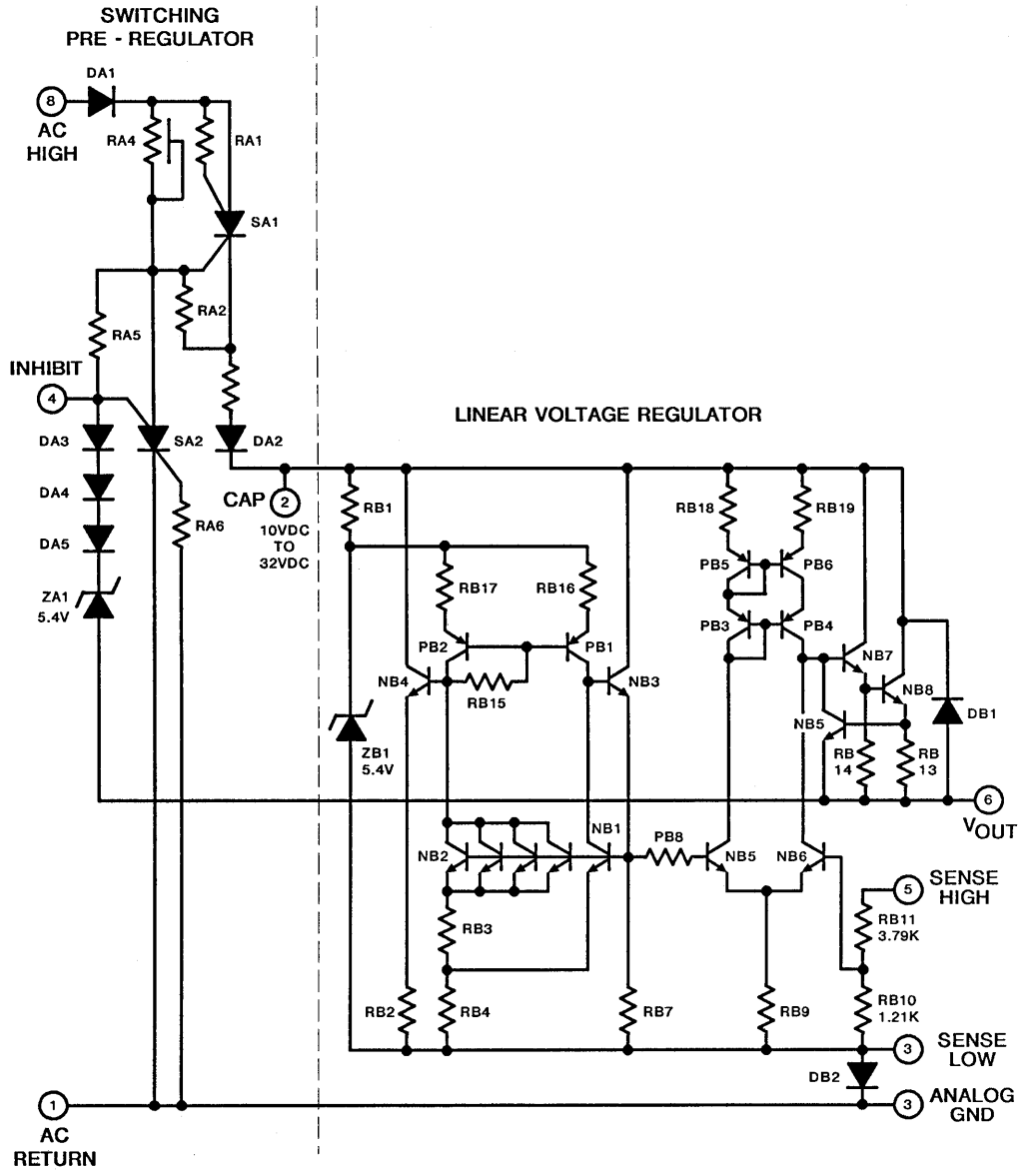
$K = \frac{V_{OUT} - 5V}{}$ Where K is the Approximate Value of Resistor Between Pin 5 and Pin 6 (in KΩ), V_{OUT} is the Desired Output Voltage. See Graph.



R_{SENSE} IS ZERO OHMS FOR 5V_{OUT}

FIGURE 1.

Schematic


SWITCHING
PRE - REGULATOR
LINEAR VOLTAGE REGULATOR
8
AC
HIGH
DA1
RA4
RA1
SA1
RA2
RA5
INHIBIT
4
DA3
SA2
DA2
DA4
DA5
ZA1
5.4V
RA6
CAP
2
10VDC
TO
32VDC
RB1
RB17
RB16
PB2
PB1
NB4
NB3
RB15
ZB1
5.4V
RB18
RB19
PB5
PB6
PB3
PB4
NB7
NB8
DB1
NB5
RB
14
RB
13
6
VOUT
NB1
PB8
NB2
NB5
NB6
5
SENSE
HIGH
RB11
3.79K
RB3
RB2
RB4
RB7
RB9
RB10
1.21K
3
SENSE
LOW
DB2
3
ANALOG
GND
1
AC
RETURN

Application Information

How The HV-1205 Works

The HV-1205 converts AC voltage into regulated DC voltage to power low voltage components such as integrated circuits. This is accomplished in two stages on the monolithic chip. First, the pre-regulator momentarily connects a large capacitor to the AC high line until it charges to about 6V above the selected output voltage. The pre-regulator then switches to a blocking mode and stays in that blocking mode until the next line cycle begins. The large capacitor supplies power to the series pass regulator, providing DC current to power the user's circuit. Providing current to the post regulator causes the large cap to discharge at a rate dependent on load current. Each line cycle refreshes the charge on the electrolytic capacitor. For a detailed explanation of HV-1205 operation see Application Note 558.

Input Voltage

The HV-1205 operates over a wide range of input voltages. Most applications will use the 120Vrms line from the power grid. A standard circuit for this application is shown in Figure 2. Much smaller input voltages can be used. The size of the external components used will be determined by the output voltage and current required and the input voltage available. Several graphs have been provided to help choose component values for a specific application. The section below called Component Selection discusses trade-offs related to component sizing.

Input Frequency

The HV-1205 is designed to operate from 48Hz to 440Hz. Higher operating frequency in possible. Keep in mind that the HV-1205 will refresh C2 once per line cycle.

Setting Output Voltage

The HV-1205 can be set to provide a regulated output voltage anywhere from 5V to 24V_{DC}. Refer to Figures 4, 5 and 6 for several ways of adjusting output voltage. Any time an output voltage greater than 5V is chosen, a 10µF capacitor between the output and the sense pin is required. That capacitor allows C2 to charge gradually.

As seen in Figure 1, output voltage is set by feedback to the sense pin. The output will rise to the voltage necessary to keep the sense pin at 5V. For a 5V output, pins 5 and 6 are shorted together. There are three ways to increase the output voltage beyond 5V. The simplest method is to increase the feedback resistor by adding an external resistor between pins 5 and 6. The disadvantage is that the internal circuit resistors have a tolerance of approximately ±15% which limits the accuracy of the predicted output (see graph). The internal thin film resistors have low temperature coefficients.

An external voltage divider as shown in Figure 5 improves the accuracy as long as the external resistors are much lower in value than those of the internal divider. Approximately 1mA flows into pin 5. If a potentiometer is used as the divider, an additional resistor between the lower leg and ground will insure that the output never exceeds its maximum rated voltage.

A zener diode between pins 5 and 6, as shown in Figure 6, sets the output voltage above 5V by the zener's breakdown voltage at 1mA. This voltage has the accuracy and tolerance of the zener. An added advantage is that two outputs are now available, pin 5 at 5V and pin 6 at V_Z + 5V. All the current from the 5V supply flows through the reference diode. The sum of both output currents should not exceed 50mA.

Output Current

Any current draw up to 50mA continuous is acceptable. More current can be drawn momentarily. Care should be taken to make sure C2 is not discharged below the dropout voltage and that the duty cycle of the excess current is low enough to not cause a package power dissipation problem. The output is current limited as shown in the graph to protect against shorted loads.

Component Selection

One of the most powerful features of the HV-1205 is its flexibility. One standard configuration allows enormous variation in input voltage and output current while still maintaining a regulated output. For example, with R_1 = 150Ω, C2 = 470µF and V_{OUT} = 5V, the HV-1205 will provide a regulated 50mA output when input voltage is anywhere from 132V_{AC} down to about 28V_{AC}. The designer can choose components tailored to his application in order to save cost, space, power dissipation etc.

Below is a list of external components, description of their purpose, and a recommended value. This is a full list of possible components all of which may not be required for an intended application. Most designs will use a subset of this list.

F1: Fuse. Opens the connections to the power line should chip fail. Recommended value = 1/4A, 2AG similar to Littlefuse 225.250®.

R_1: Source Resistance. Limits current into HV-1205. Needs to be large enough to limit inrush current when C2 is discharged fully. V_{PEAK}/R_1 = 1.1A Maximum. R_1 will dissipate power as shown in the graphs. The equation for Pd in R_1 is: Pd = $1.33\sqrt{\pi R_1 V_{PEAK}(I_{OUT})^3}$. Low average output currents would allow for source resistors with lower Pd ratings. Similarly, lower V_{AC} or smaller value R_1 will cause less dissipation in R_1. Sizing of R_1 should be tailored to the intended application keeping in mind not to let the maximum inrush current be exceeded. Should an external method of limiting inrush current be used (such as NTC resistors) then the value of R_1 and its associated heat could be reduced. Recommended value = 150Ω.

C1: Snubber Capacitor. R_1 and C1 form a low pass filter thereby limiting the rate of voltage rise at the input of the HV-1205. Recommended value = 0.05µF, AC rated.

MOV: Surge suppressor. Metal Oxide Varistor clamps voltage to a level that the HV-1205 can handle. Recommended value = V130LA20 or equivalent.

Littlefuse 225.250® is a Registered Trademark of Tracor, Inc.

Application Information (Continued)

C2: Pre-Regulator capacitor. This capacitor is charged once each line cycle. The post-regulator portion of HV-1205 is powered by C2 for most of the line cycle. Normally the smallest C2 that will supply the load current (see graph) is used. Using a large C2 will supply temporary high load currents or normal load current during a short power loss. Using a larger C2 will reduce ripple at Pin 2, the input to the post regulator, which will reduce output ripple. C2 should have a ripple current rating consistent with the application. Small capacitors with high ESR may not store enough charge to maintain load current. See graph. Recommended value = 470µF, voltage rating should be about 10V greater than chosen V_{OUT}.

C3: Inhibit capacitor. Keeps the HV-1205 from turning on during input transients. If sized too large, HV-1205 will never turn on. If sized too small, no protection from transients is offered. For 60Hz (or 50Hz) use the recommended value of 150pF, voltage rating should be at about 10V greater than V_{OUT}. For 400Hz use 47pF.

C4: Output filter capacitor. At least 1µF is required to maintain stability of the output stage. Larger values will not reduce ripple but will reduce spiking which may occur on the output coincident with the HV-1205 going into blocking mode. 100µF reduces the spike amplitude to about 25mVp-p.

R2: Feedback component. A resistor or diode that causes a voltage drop between the SENSE and OUTPUT pins and thereby adjusting the output voltage. See voltage adjustment equivalent circuit. Also see graph for approximate resistor value.

C5: Sense Capacitor. Used to ramp up C2 voltage at power up. Charging C2 rapidly to higher output voltages without C5 in place could damage the HV-1205. A large C5 can be used to delay power up of the load circuit (when V_{OUT} is greater than 5V). Recommended value, 10µF.

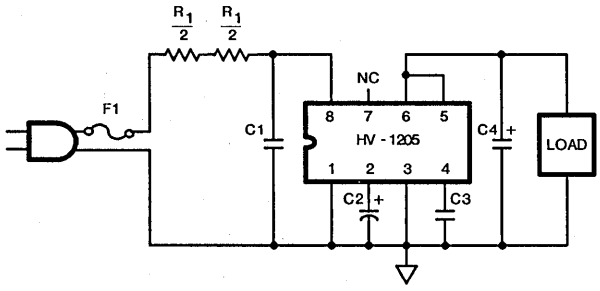


FIGURE 2. HV-1205 STANDARD +5V APPLICATION

V_{OUT} ADJUSTMENT

FIGURE 4 METHOD		FIGURE 5 METHOD		FIGURE 6 METHOD	
R_2	V_O	R_A/R_B	V_O	V_Z*	V_O
0	5V	0/00	5V	-	5V
1K	6V	160/1K	6V	1V	6V
3K	8V	510/1K	8V	3V	8V
5K	10V	820/1K	10V	5V	10V
7K	12V	1.2K/1K	12.2V	7V	12V
9K	14V	1.5K/1K	14V	9V	14V
11K	16V	1.8K/1K	15.8V	11V	16V
13K	18V	2.2K/1K	18.2V	13V	18V
15K	20V	2.4K/1K	19.4V	15V	20V
17K	22V	3.0K/1K	23V	17V	22V
19K	24V	3.17K/1K	24V	19V	24V

*V_Z @ 1mA

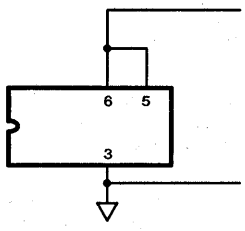


FIGURE 3. V_{OUT} = +5V

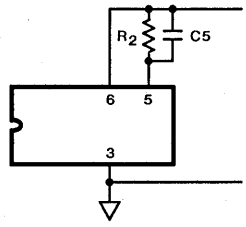


FIGURE 4. V_{OUT} > +5V

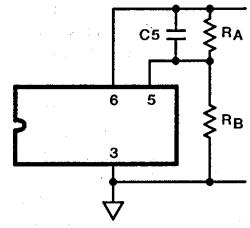


FIGURE 5. V_{OUT} > +5V

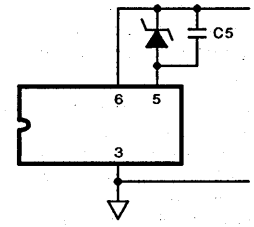
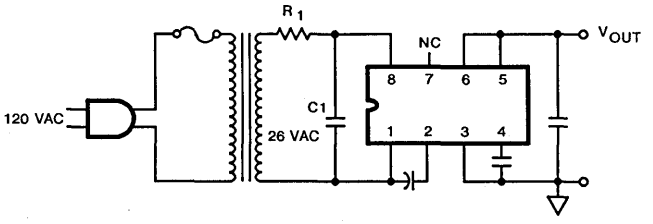


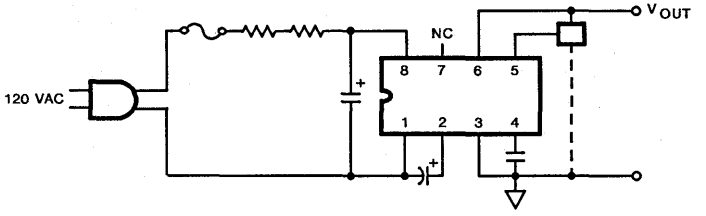
FIGURE 6. V_{OUT} > +5V

Application Information (Continued)

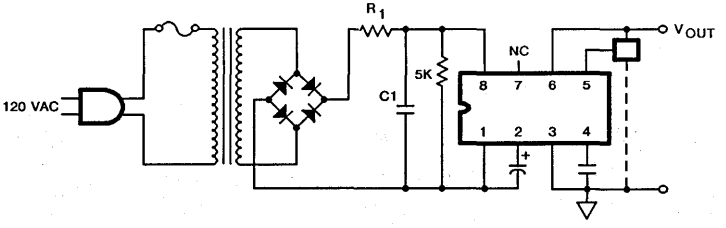
OPERATION FROM TRANSFORMER SECONDARY (+5V_{OUT})



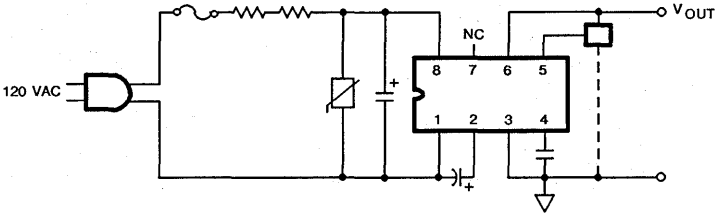
OPERATION WITH V_{OUT} > 5V



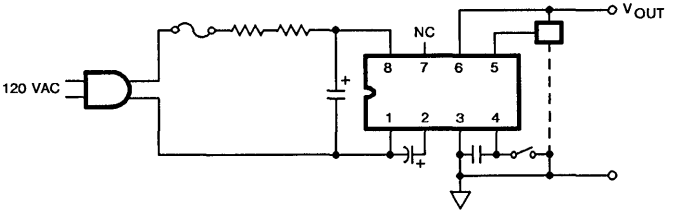
OPERATION FROM A BRIDGE RECTIFIER



SURGE PROTECTION USING MOV



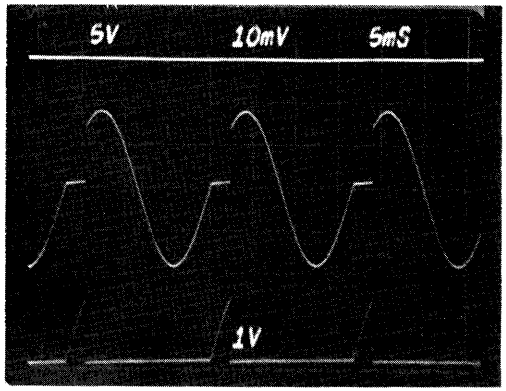
USING SWITCH TO TURN OFF OUTPUT



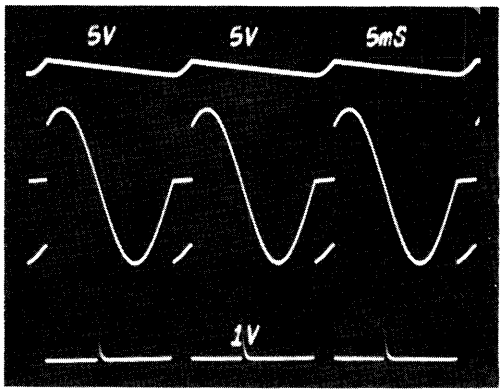
HV-1205 Waveforms

Unless Otherwise Specified: $T_A = +25^oC$, $V_{AC} = 120Vrms$, f = 60Hz, $R_1 = 150\Omega$, C1 = 0.05µF, C2 = 470µF, C3 = 150pF, C4 = 1µF, $V_{OUT} = 5V$

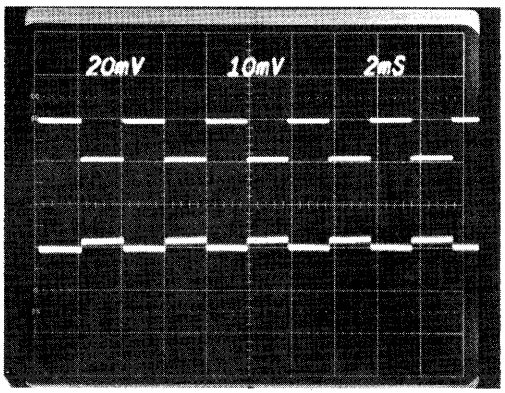
Top Trace: Regulated $5V_{OUT}$
Middle Trace: Input Voltage at Pin 8, AC HIGH (100V/Div)
Bottom Trace: Current into Pin 8, (0.5A/Div)



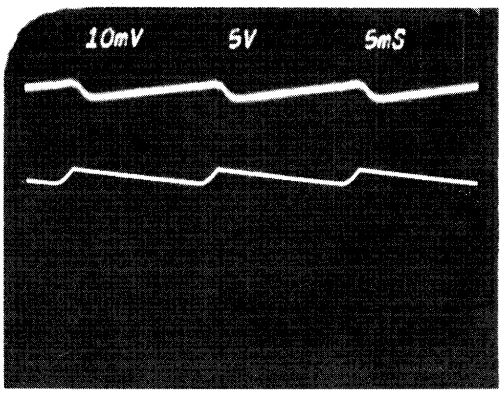
Top Trace: Pre-Regulator Capacitor Voltage, C2 (5V/Div) @ Approximately 11VDC
Middle Trace: Input Voltage at Pin 8, AC HIGH (100V/Div)
Bottom Trace: Inhibit Capacitor Voltage (5V/Div)



Top Trace: Load Current Step (50mA/Div)
Bottom Trace: Output Voltage (20mV/Div) @ 5VDC

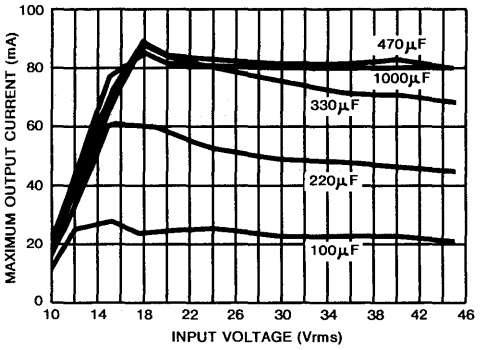


Top Trace: Ripple on Regulated 5V Out with 50mA Out (10mV/Div)
Bottom Trace: Ripple on C2, Input to Linear Regulator. C2 = 470µF (5V/Div)

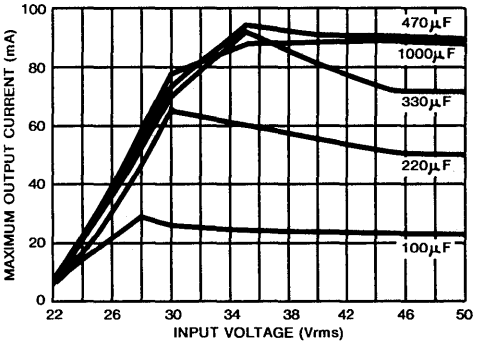


Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{AC} = 120Vrms, f = 60Hz, R_1 = 150Ω, C1 = 0.05µF, C2 = 470µF, C3 = 150pF, C4 = 1µF, V_{OUT} = 5V

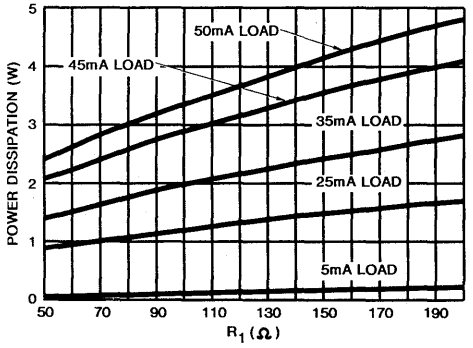
MAXIMUM OUTPUT CURRENT FOR 5V REGULATED OUTPUT vs. INPUT VOLTAGE AND PRE-REGULATOR CAPACITOR SIZE (C2)
R_1 = 24Ω



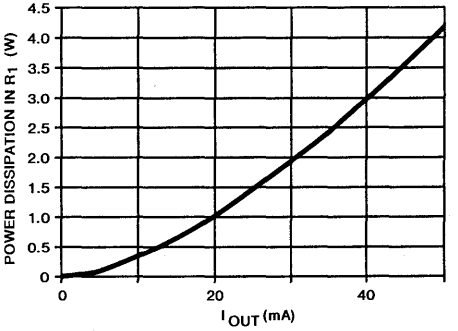
MAXIMUM OUTPUT CURRENT FOR 24V REGULATED OUTPUT vs. INPUT VOLTAGE AND PRE-REGULATOR CAPACITOR SIZE (C2)
R_1 = 24Ω



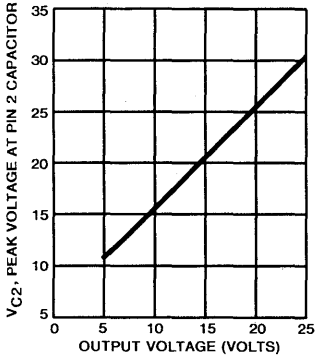
Pd IN R_1 vs. R_1 VALUE
Vrms = 120V



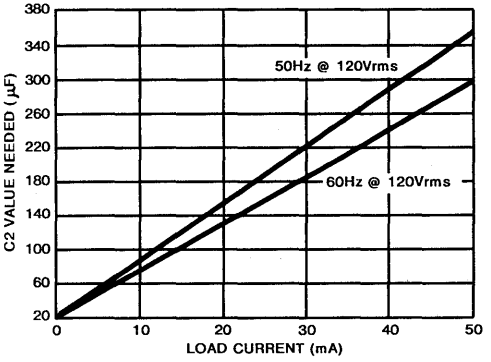
Pd IN R_1 vs. I_{OUT}
120Vrms, R_1 = 150Ω



PEAK C2 VOLTAGE vs. OUTPUT VOLTAGE

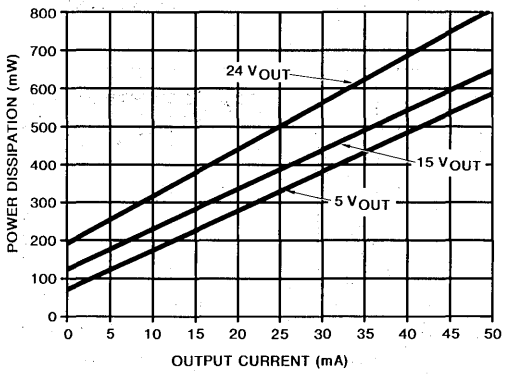


MINIMUM C2 VALUE vs. LOAD CURRENT

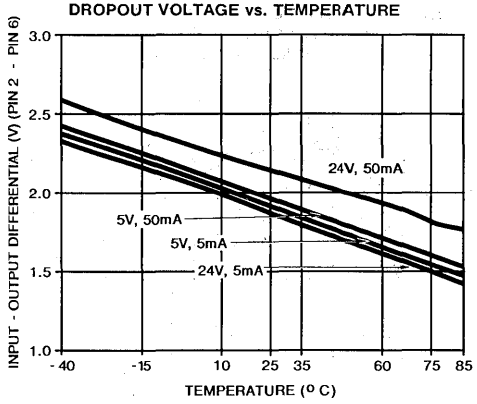


Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{AC} = 120Vrms, f = 60Hz, R_1 = 150Ω, C1 = 0.05µF, C2 = 470µF, C3 = 150pF, C4 = 1µF, V_{OUT} = 5V

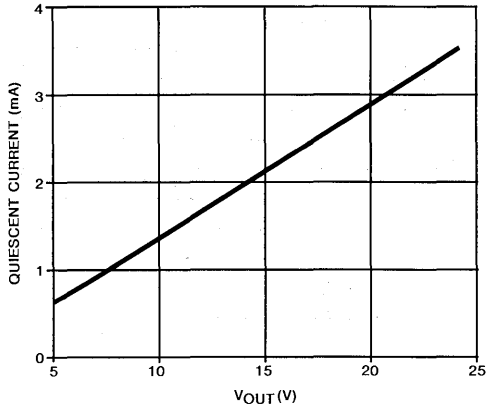
CHIP POWER DISSIPATION vs. OUTPUT CURRENT



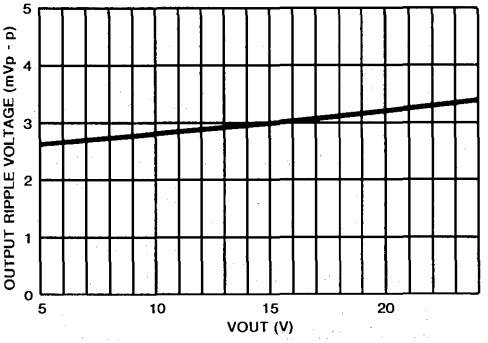
DROPOUT VOLTAGE vs. TEMPERATURE



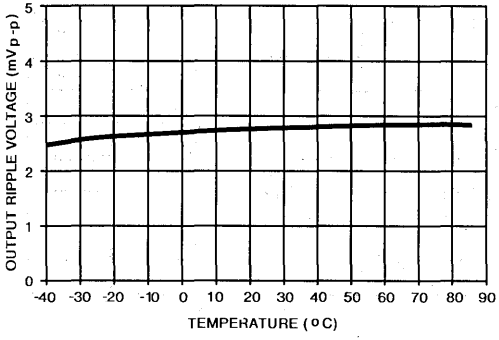
QUIESCENT CURRENT vs. OUTPUT VOLTAGE @ = +25°C
I_{OUT} = 5mA to 50mA



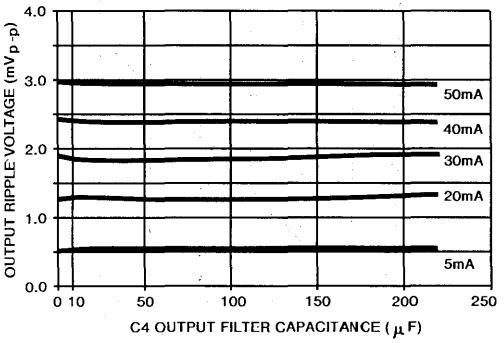
OUTPUT RIPPLE VOLTAGE vs. OUTPUT VOLTAGE
I_{OUT} = 50mA



OUTPUT RIPPLE VOLTAGE vs. TEMPERATURE
C4 = 1µF



OUTPUT RIPPLE VOLTAGE vs. LOAD CAPACITANCE AND OUTPUT CURRENT

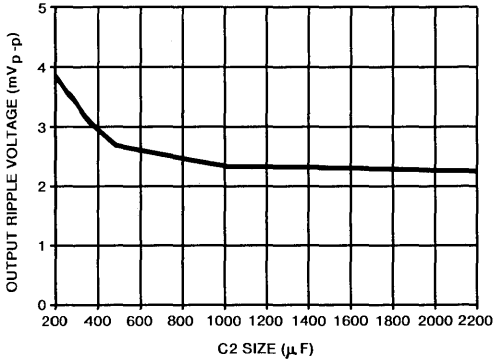


Typical Performance Curves

Unless Otherwise Specified: T_A = +25°C, V_{AC} = 120Vrms, f = 60Hz, R_1 = 150Ω, C1 = 0.05µF, C2 = 470µF, C3 = 150pF, C4 = 1µF, V_{OUT} = 5V

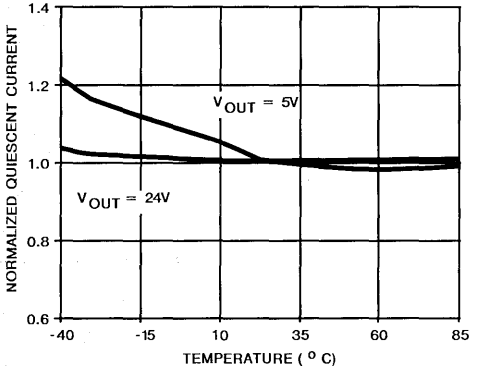
OUTPUT RIPPLE VOLTAGE vs. C2 SIZE

I_{OUT} = 50mA, V_{OUT} = 5V



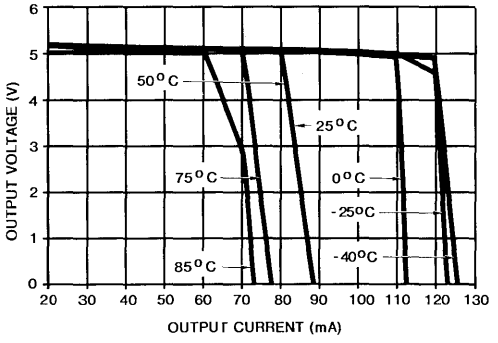
NORMALIZED QUIESCENT CURRENT vs. TEMPERATURE

Actual Quiescent Current at +25°C: V_{OUT} = 24V: 3.42mA
V_{OUT} = 5V: 0.41mA



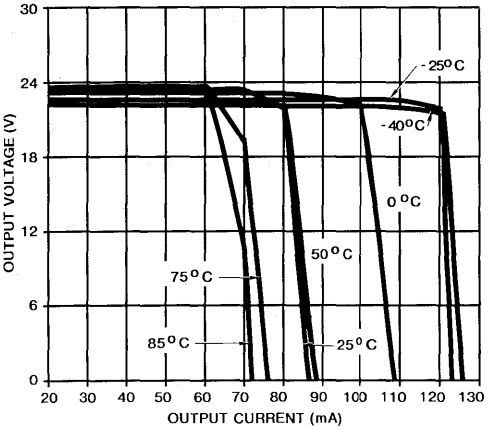
OUTPUT CURRENT LIMIT ($5V_{OUT}$)

50mA is the Maximum Specified Output Current



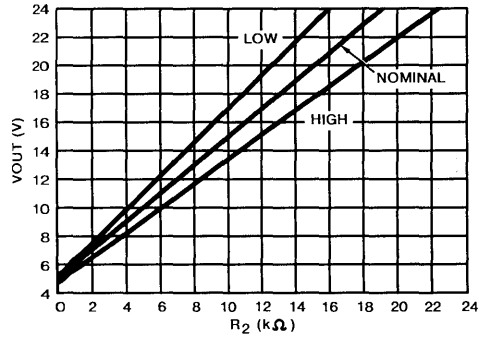
OUTPUT CURRENT LIMIT ($24V_{OUT}$)

50mA is the Maximum Specified Output Current

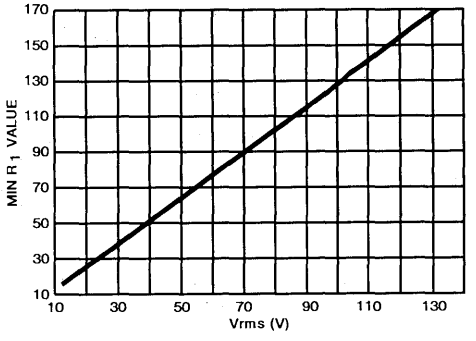


V_{OUT} vs. R_2 WITH TOLERANCES

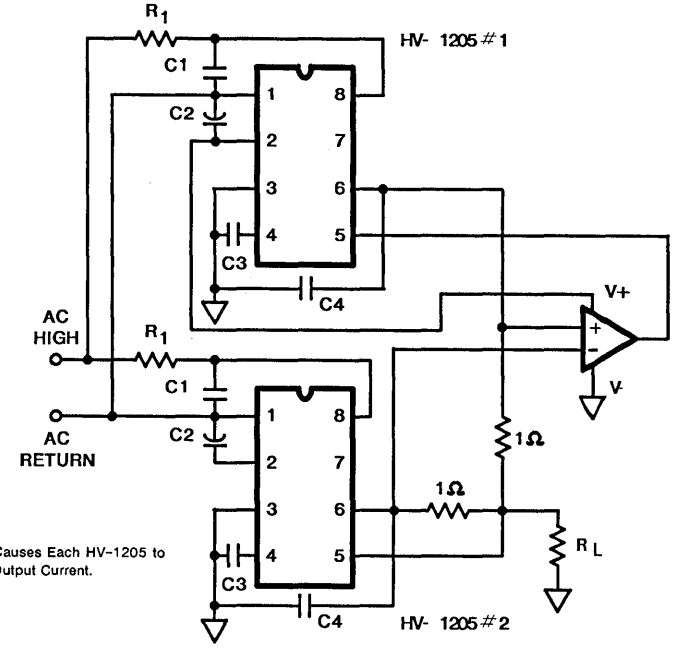
Internal Resistors 15% High or Low



MINIMUM ALLOWABLE R_1 FOR INPUT VOLTAGE

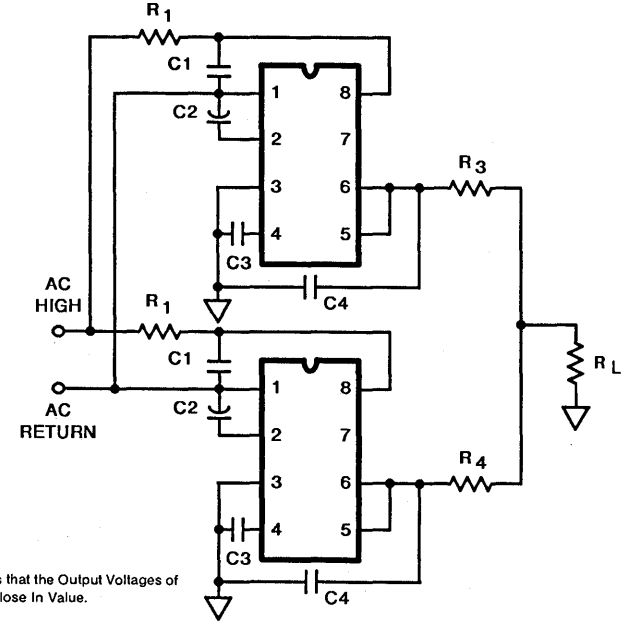


HV-1205 Parallel Operation (Method #1)



NOTE: Operational Amplifier Causes Each HV-1205 to Contribute Equally to Output Current.

HV-1205 Parallel Operation (Method #2)



$$\Delta I_{OUT} = \frac{\Delta V_{OUT}}{R_3}$$

$R_3 = R_4$

NOTE: This Method Requires that the Output Voltages of Each HV-1205 are Close In Value.

HV-2405E

May 1990

Single Chip Power Supply

Features

- Direct AC to DC Conversion
- Wide Input Voltage Range 18Vrms-264Vrms
- Wide Input Frequency Range 48Hz-440Hz
- Guaranteed Output Current 50mA
- Output Voltage ..... 5V to 24V
- Line and Load Regulation ..... <5%
- Surge Protection per IEEE 587 Category A & B Using MOV or Gas Discharge Tube

Applications

- Compact, Low Cost, Power Supply for Non-Isolated Applications
- High Efficiency Regulator for HVAC 26V Control Systems
- Battery Back-Up Systems
- Dual Output Supply for OFF-LINE Motor Controls
- Housekeeping Supply for Switch-Mode Power Supplies

Ordering Information

PART NUMBER	OPERATING TEMPERATURE RANGE	PACKAGE DESCRIPTION
HV3-2405E-5	0°C to +75°C	8 Lead Plastic Mini-DIP
HV3-2405E-9	-40°C to +85°C	8 Lead Plastic Mini-DIP

CAUTION: This Product Does Not Provide Isolation From the AC Line

Description

The HV-2405E is a single chip power supply that can supply 5V to 24V at 50mA output current. Just a few inexpensive external components are needed to provide a compact, light weight, cost effective power supply. The HV-2405E replaces a transformer, rectifier, and voltage regulator. This chip is made in the new Harris High Voltage Dielectric Isolation Process. This high breakdown process (500V) allows a patented switching circuit to draw current from the AC line only as necessary to supply the load.

The wide input voltage range makes the HV-2405E an excellent choice for use in equipment which must operate from either 240V or 120V. Unlike competitive AC-DC convertors, the HV-2405E can use the same external components for operation from either voltage. In addition the HV-2405E can be connected across any two phases of a 3-phase system (208Vrms)*. This great flexibility in input voltage allows a single design for worldwide use.

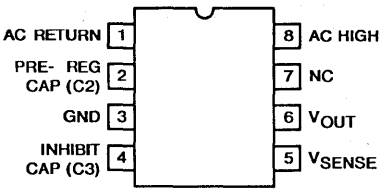
The HV-2405E is pin for pin compatible with the HV-1205 but allows twice the input voltage. Additionally, the output and sense pins are connected through a zener diode to limit output voltage should the sense pin to output connection become open.

Further flexibility can be obtained from the HV-2405E by using it with other Harris chips. For example, the high efficiency ICL-7660S and ICL-7662 provide positive to negative voltage conversion. For automatic switch-over to battery back-up use the ICL 7673. Harris also offers a line of extremely low power op amps.

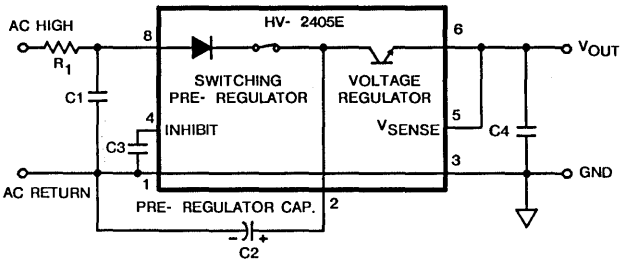
*** CAUTION: When used in this mode, GND and AC RETURN operate at high voltage with respect to earth ground.**

Pinout

HV3-2405E (PLASTIC MINI-DIP)
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

Voltage Between Pin 1 and 8, Continuous Vrms 264Vrms
Voltage Between Pin 1 and 8, Peak 500V
Voltage Between Pin 2 and 6 ..... 10V
Input Current, Peak 2.5A
Output Current ..... Short Circuit Protected
Output Voltage 30V
Maximum Junction Temperature..... +150°C

Operating Temperature Range

HV3-2405E-9 ..... -40°C to +85°C
HV3-2405E-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +175°C

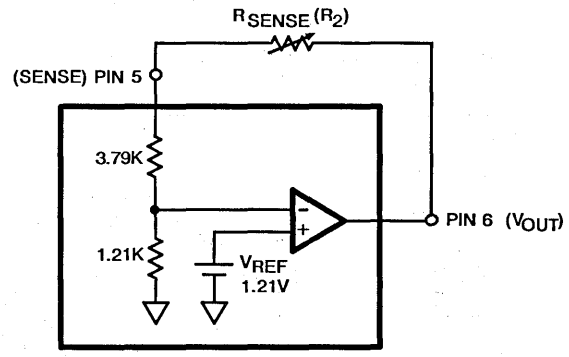
Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Plastic DIP	82	16

Electrical Specifications Unless Otherwise Specified: V_{IN} = 264Vrms at 50Hz, C1 = 0.05µF, C2 = 470µF, C3 = 150pF, V_{OUT} = 5V, I_{OUT} = 50mA, Source Impedance, R_1 = 150Ω. Parameters are Guaranteed at the Specific V_{IN} and Frequency Conditions, Unless Otherwise Specified. See Functional Diagrams for Component Location.

PARAMETER	V_{IN}	TEMP	HV-2405E-9 -40°C to +85°C			HV-2405E-5 0°C to +75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage (At Preset 5V)	264V	+25°C	4.75	5.0	5.25	4.75	5.0	5.25	V
	264V	Full	4.65	5.0	5.35	4.65	5.0	5.35	V
Output Voltage TC	264V	Full	-	0.02	-	-	0.02	-	%/°C
Output Ripple (Vp-p) (C4 = 1µF, f = 50Hz)	264V	+25°C	-	22	-	-	22	-	mV
	264V	Full	-	24	-	-	24	-	mV
Line Regulation	80Vrms to 264Vrms	+25°C	-	10	15	-	10	20	mV
		Full	-	15	30	-	15	40	mV
Load Regulation (I_{OUT} = 5mA to 50mA)	264V	+25°C	-	-	15	-	-	20	mV
	264V	Full	-	-	30	-	-	40	mV
Output Current	264V	Full	0	-	50	0	-	50	mA
Short Circuit Current Limit	264V	Full	55	95	-	55	95	-	mA
Drop-Out Voltage	Pin 2 - Pin 6	+25°C	-	2.2	-	-	2.2	-	V
Quiescent Current Post Regulator	11V_{DC} to 30V_{DC} On Pin 2	+25°C	-	2	-	-	2	-	mA

Equivalent Circuit For Output Voltage Adjustment

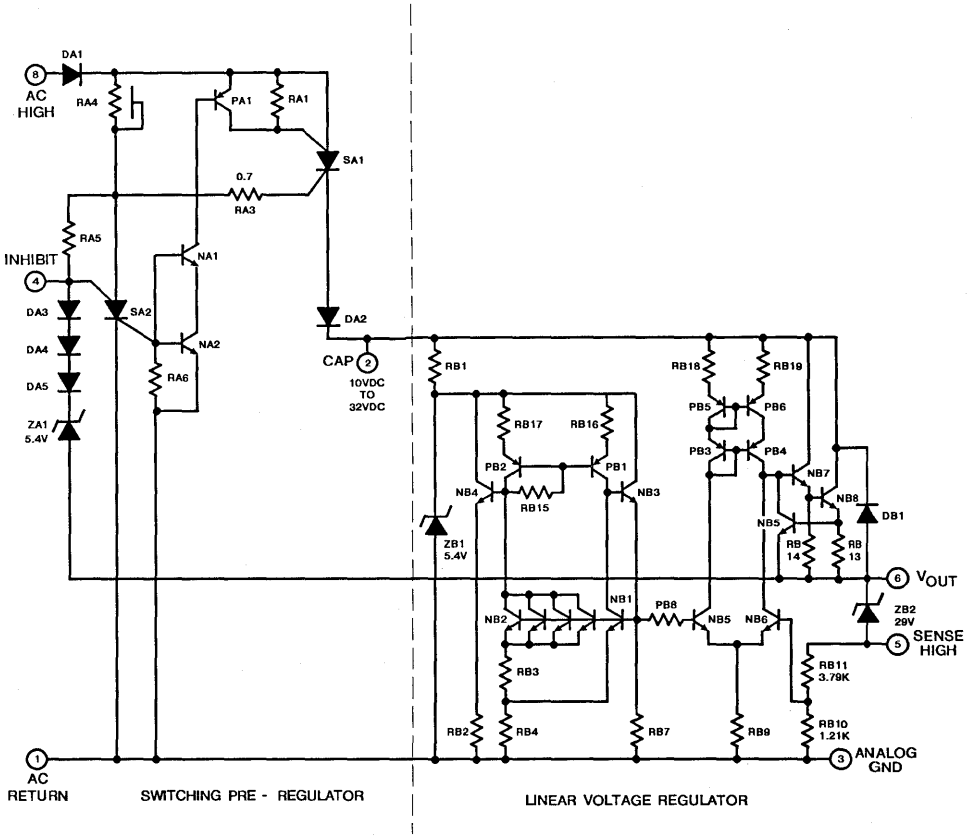
$K = \frac{V_{OUT} - 5V}{3.79K}$ Where K is the Approximate Value of Resistor Between Pin 5 and Pin 6 (in KΩ), V_{OUT} is the Desired Output Voltage. See Graph.



R_{SENSE} IS ZERO OHMS FOR 5V OUTPUT

FIGURE 1.

Schematic



Patent pending on the above circuit.

Application Information

How The HV-2405E Works

The HV-2405E converts AC voltage into regulated DC voltage to power low voltage components such as integrated circuits. This is accomplished in two stages on the monolithic chip. First, the pre-regulator momentarily connects a large capacitor to the AC high line until it charges to about 6V above the selected output voltage. The pre-regulator then switches to a blocking mode and stays in that blocking mode until the next line cycle begins. The large capacitor supplies power to the series pass regulator, providing DC current to power the user's circuit. Providing current to the post regulator causes the large cap to discharge at a rate dependent on load current. Each line cycle refreshes the charge on the electrolytic capacitor.

Input Voltage

The HV-2405E operates over a wide range of input voltages. Most applications will use the 240Vrms or 120Vrms line from the power grid. A standard circuit for this application is shown in Figure 2. Much smaller input voltages can be used. The size of the external components used will be determined by the output voltage and current required and the input voltage available. Several graphs have been provided to help choose component values for a specific application. The section below called Component Selection discusses trade-offs related to component sizing.

Input Frequency

The HV-2405E is designed to operate from 48Hz to 440Hz. Higher operating frequency is possible. Keep in mind that the HV-2405E will refresh C2 once per line cycle.

Setting Output Voltage

The HV-2405E can be set to provide a regulated output voltage anywhere from 5V to 24V_{DC}. Refer to Figures 4, 5 and 6 for several ways of adjusting output voltage.

As seen in Figure 1, output voltage is set by feedback to the sense pin. The output will rise to the voltage necessary to keep the sense pin at 5V. For a 5V output, pins 5 and 6 are shorted together. There are three ways to increase the output voltage beyond 5V. The simplest method is to increase the feedback resistor by adding an external resistor between pins 5 and 6. The disadvantage is that the internal circuit resistors have a tolerance of approximately ±15% which limits the accuracy of the predicted output (see graph). The internal thin film resistors have low temperature coefficients.

An external voltage divider as shown in Figure 5 improves the accuracy as long as the external resistors are much lower in value than those of the internal divider. Approximately 1mA flows into pin 5.

A zener diode between pins 5 and 6, as shown in Figure 6, sets the output voltage above 5V by the zener's breakdown voltage at 1mA. This voltage has the accuracy and tolerance of the zener. An added advantage is that two outputs are now available, pin 5 at 5V and pin 6 at V_Z + 5V. All the current from the 5V supply flows through the reference diode. The sum of both output currents should not exceed 50mA.

The HV-2405E has an internal zener diode to clamp the output above the 24V maximum but below a damaging level.

Output Current

Any current draw up to 50mA continuous is acceptable. More current can be drawn momentarily. Care should be taken to make sure C2 is not discharged below the dropout voltage and that the duty cycle of the excess current is low enough to not cause a package power dissipation problem. The output is current limited as shown in the graph to protect against shorted loads.

Component Selection

One of the most powerful features of the HV-2405E is its flexibility. One standard configuration allows enormous variation in input voltage and output current while still maintaining a regulated output. For example, with R_1 = 150Ω, C2 = 470µF and V_{OUT} = 5V, the HV-2405E will provide a regulated 50mA output when input voltage is anywhere from 264V_{AC} down to about 28V_{AC}. The designer can choose components tailored to his application in order to save cost, space, power dissipation etc.

Below is a list of external components, description of their purpose, and a recommended value. This is a full list of possible components all of which may not be required for an intended application. Most designs will use a subset of this list.

F1: Fuse. Opens the connections to the power line should chip or C2 fail. Recommended value = 1/2A, 2AG similar to Littlefuse 225.500®.

R_1: Source Resistance. Limits current into HV-2405E. Needs to be large enough to limit inrush current when C2 is discharged fully. V_{PEAK}/R_1 = 2.5A Maximum. R_1 will dissipate power as shown in the graphs. The equation for Pd in R_1 is:
$Pd = 1.33 \sqrt{\pi R_1 V_{PEAK}(I_{OUT})^3}$.
Low average output currents would allow for source resistors with lower Pd ratings. Similarly, lower V_{AC} or smaller value R_1 will cause less dissipation in R_1. Sizing of R_1 should be tailored to the intended application keeping in mind not to let the maximum inrush current be exceeded. Should an external method of limiting inrush current be used (such as NTC resistors) then the value of R_1 and its associated heat could be reduced. Recommended value = 150Ω.

C1: Snubber Capacitor. R_1 and C1 form a low pass filter thereby limiting the rate of voltage rise at the input of the HV-2405E. Recommended value = 0.05µF, AC rated.

MOV: Surge suppressor. Metal Oxide Varistor clamps voltage to a level that the HV-2405E can handle. Recommended value = V130LA20 or equivalent for 120V applications and gas tube which arcs over at less than 500V for 240V applicatons.

Littlefuse 225.500® is a Registered Trademark of Tracor, Inc.

Application Information (Continued)

C2: Pre-Regulator capacitor. This capacitor is charged once each line cycle. The post-regulator portion of HV-2405E is powered by C2 for most of the line cycle. Normally the smallest C2 that will supply the load current (see graph) is used. Using a large C2 will supply temporary high load currents or normal load current during a short power loss. Using a larger C2 will reduce ripple at Pin 2, the input to the post regulator, which will reduce output ripple. C2 should have a ripple current rating consistent with the application. Small capacitors with high ESR may not store enough charge to maintain load current. See graph. Recommended value = 470µF, voltage rating should be about 10V greater than chosen V_{OUT}.

C3: Inhibit capacitor. Keeps the HV-2405E from turning on during input transients. If sized too large, HV-2405E will never turn on. If sized too small, no protection from transients is offered. For 50Hz or 60Hz use the recommended value of 150pF, voltage rating should be at about 10V greater than V_{OUT}.

C4: Output filter capacitor. At least 1µF is required to maintain stability of the output stage. Larger values will not reduce ripple but will reduce spiking which may occur on the output coincident with the HV-2405E going into blocking mode.

R2: Feedback component. A resistor or zener diode that causes a voltage drop between the SENSE and OUTPUT pins and thereby adjusting the output voltage. See voltage adjustment equivalent circuit. Also see graph for approximate resistor value. About 1mA flows through this component.

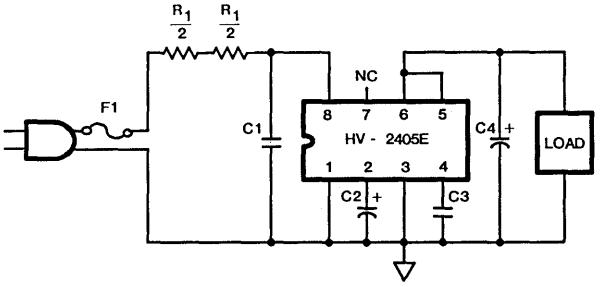


FIGURE 2. HV-2405E STANDARD +5V APPLICATION

V_{OUT} ADJUSTMENT

FIGURE 4 METHOD		FIGURE 5 METHOD		FIGURE 6 METHOD	
R_2	V_O	R_A/R_B	V_O	V_Z*	V_O
0	5V	0/Open	5V	-	5V
1K	6V	160/1K	6V	1V	6V
3K	8V	510/1K	8V	3V	8V
5K	10V	820/1K	10V	5V	10V
7K	12V	1.2K/1K	12.2V	7V	12V
9K	14V	1.5K/1K	14V	9V	14V
11K	16V	1.8K/1K	15.8V	11V	16V
13K	18V	2.2K/1K	18.2V	13V	18V
15K	20V	2.4K/1K	19.4V	15V	20V
17K	22V	3.0K/1K	23V	17V	22V
19K	24V	3.17K/1K	24V	19V	24V

*V_Z @ 1mA

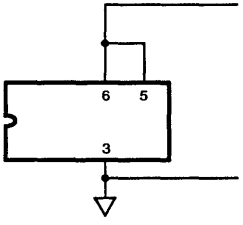


FIGURE 3. V_{OUT} = +5V

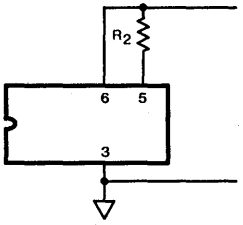


FIGURE 4. V_{OUT} > +5V

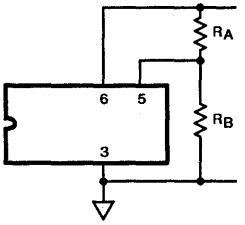


FIGURE 5. V_{OUT} > +5V

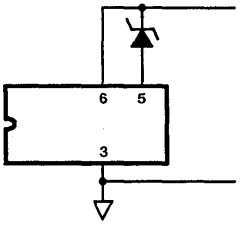
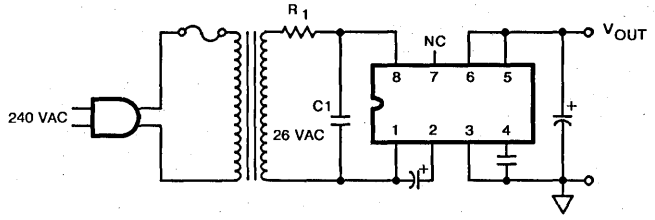


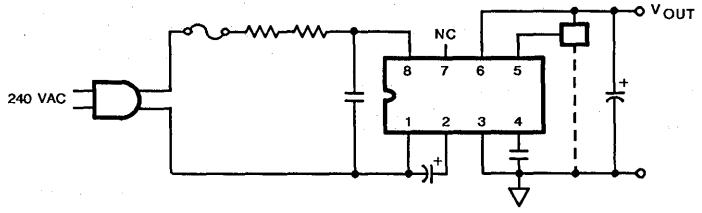
FIGURE 6. V_{OUT} > +5V

Application Information (Continued)

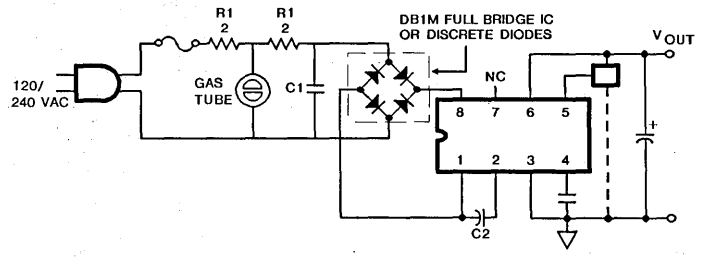
OPERATION FROM TRANSFORMER SECONDARY (+5V_{OUT})



OPERATION WITH V_{OUT} > 5V

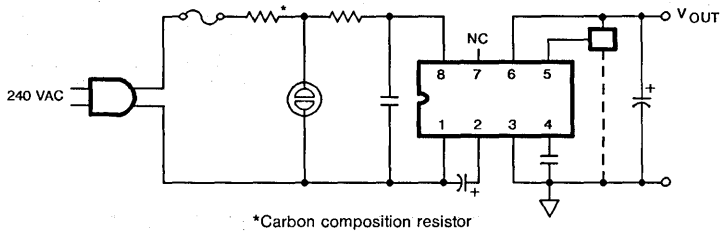


OPERATION FROM A BRIDGE RECTIFIER



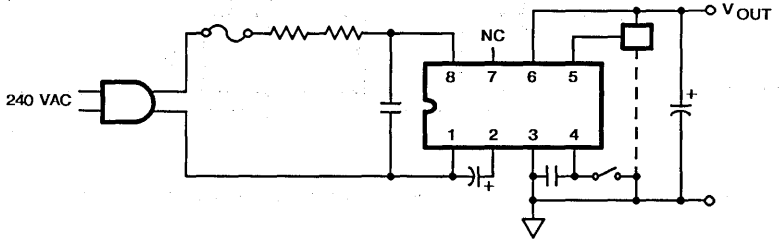
* τ formed by R1*C1 assures that V_{C1} is an AC waveform.

SURGE PROTECTION USING GAS TUBE



*Carbon composition resistor

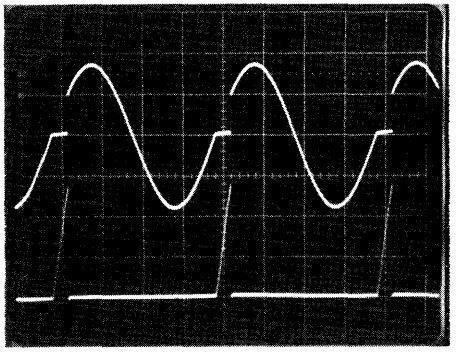
USING SWITCH TO TURN OFF OUTPUT



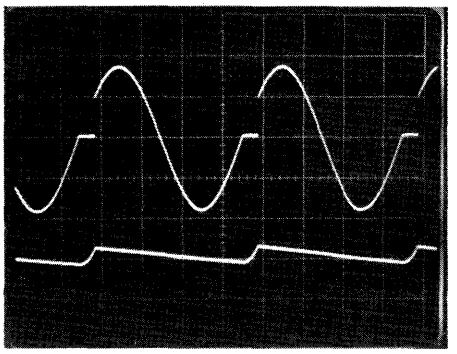
HV-2405E Waveforms

Unless Otherwise Specified: T_A = +25°C, V_{AC} = 240Vrms, f = 50Hz, R_1 = 150Ω, C1 = 0.05µF, C2 = 470µF, C3 = 150pF, C4 = 1µF, V_{OUT} = 5V @ 50mA, 5ms/div

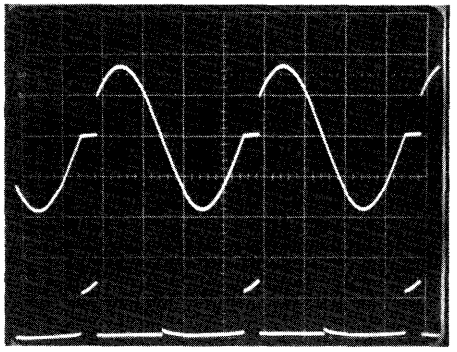
Top Trace: Input Voltage at Pin 8, AC High (200V/Div)
Bottom Trace: Current into Pin 8, (0.5A/Div)



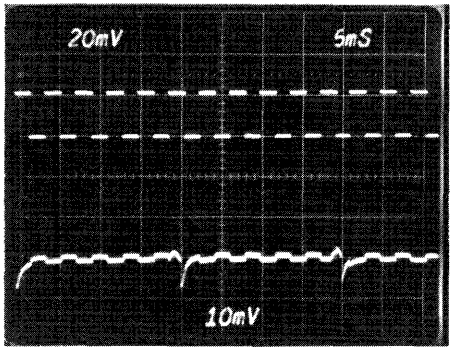
Top Trace: Input Voltage at Pin 8, AC High (200V/Div)
Bottom Trace: Pre-Regulator Capacitor Voltage, C2 (5V/Div) @ Approximately 10V DC



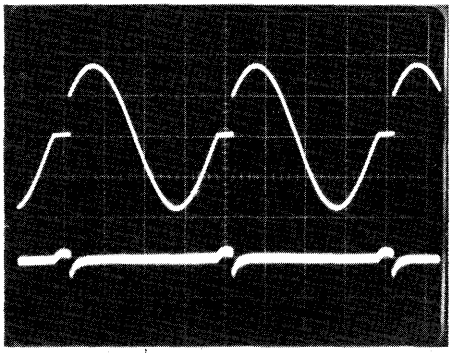
Top Trace: Input Voltage at Pin 8, AC High (200V/Div)
Bottom Trace: Inhibit Capacitor Voltage (10V/Div)



Top Trace: Load Current Step (50mA/Div)
Bottom Trace: Output Voltage (20mV/Div) @ 5VDC

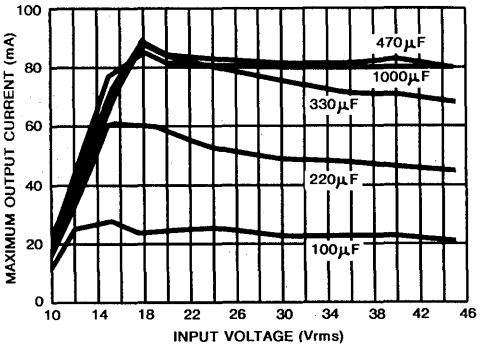


Top Trace: Input Voltage at Pin 8, AC High (200V/Div)
Bottom Trace: Ripple or Switch Spike on Regulator 5V DC Output (50mV/Div)
This is Worst Case Ripple due to Worst Case Operating Conditions
(High Line Voltage, Minimum R1 Value, Maximum I_{OUT})

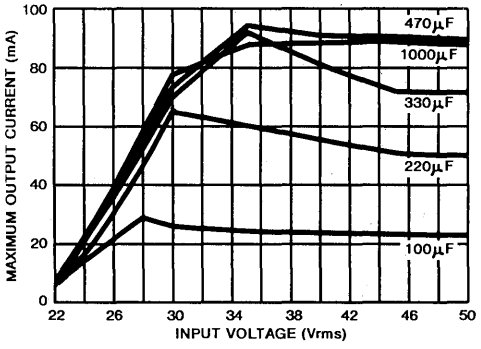


Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{AC} = 240Vrms, f = 50Hz, R_1 = 150Ω, C1 = 0.05µF, C2 = 470µF, C3 = 150pF, C4 = 1µF, V_{OUT} = 5V

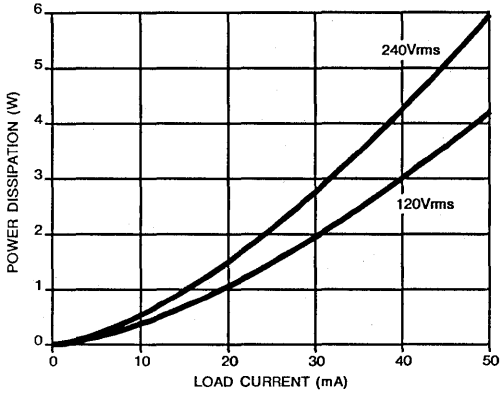
MAXIMUM OUTPUT CURRENT FOR 5V REGULATED OUTPUT vs. INPUT VOLTAGE AND PRE-REGULATOR CAPACITOR SIZE (C2)
R_1 = 24Ω



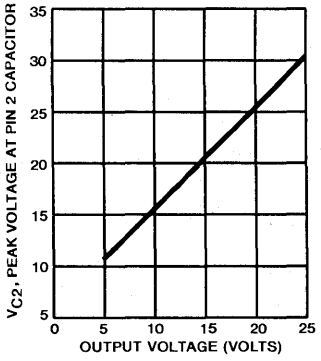
MAXIMUM OUTPUT CURRENT FOR 24V REGULATED OUTPUT vs. INPUT VOLTAGE AND PRE-REGULATOR CAPACITOR SIZE (C2)
R_1 = 24Ω



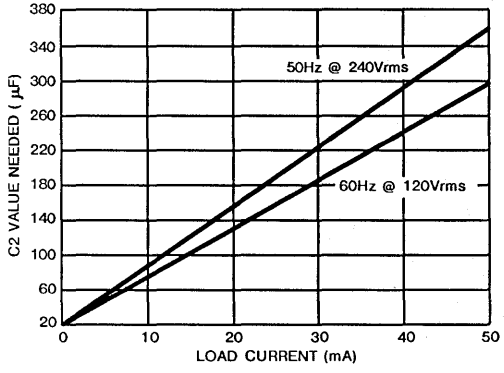
Pd IN R_1 vs. I_{OUT}
R_1 = 150Ω, VAC = 120V/240V



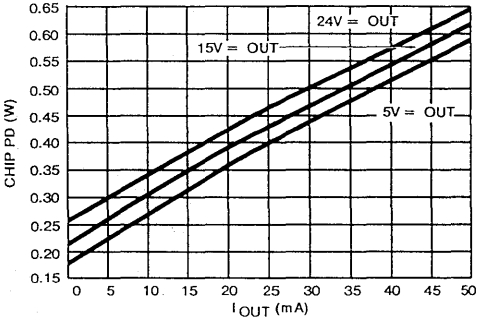
PEAK C2 VOLTAGE vs. OUTPUT VOLTAGE



MINIMUM C2 VALUE vs. LOAD CURRENT

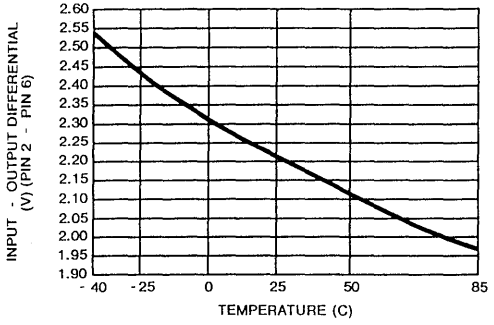


CHIP POWER DISSIPATION vs. OUTPUT CURRENT

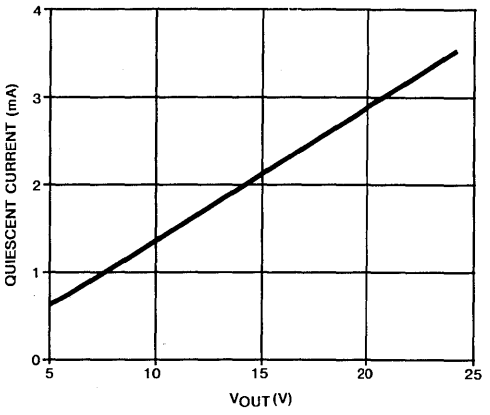


Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{AC} = 240Vrms, f = 50Hz, R_1 = 150Ω, C1 = 0.05µF, C2 = 470µF, C3 = 150pF, C4 = 1µF, V_{OUT} = 5V

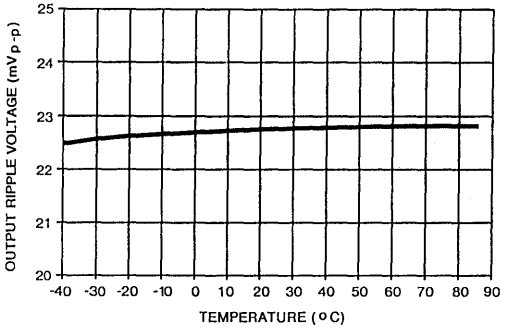
DROPOUT VOLTAGE vs. TEMPERATURE



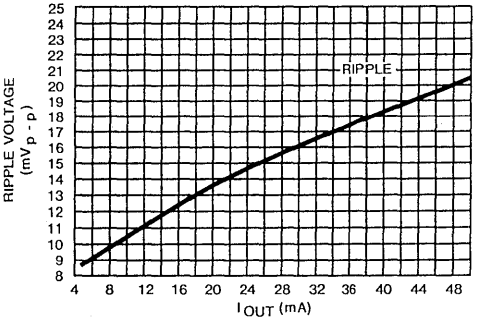
QUIESCENT CURRENT vs. OUTPUT VOLTAGE @ = +25°C
I_{OUT} = 5mA to 50mA



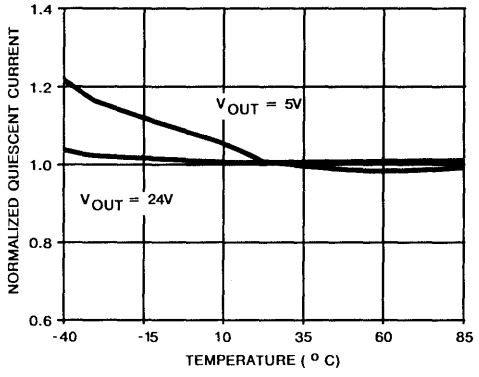
OUTPUT RIPPLE VOLTAGE vs. TEMPERATURE
C4 = 1µF



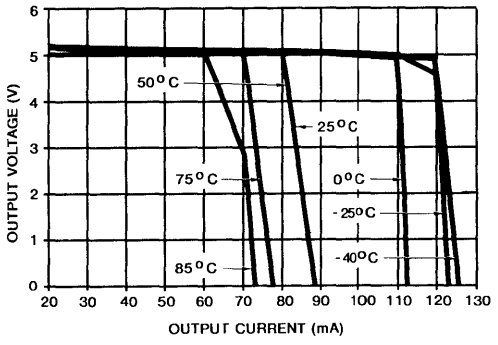
OUTPUT RIPPLE VOLTAGE vs. LOAD CURRENT



NORMALIZED QUIESCENT CURRENT vs. TEMPERATURE
Actual Quiescent Current at +25°C: V_{OUT} = 24V: 3.42mA
V_{OUT} = 5V: 0.41mA

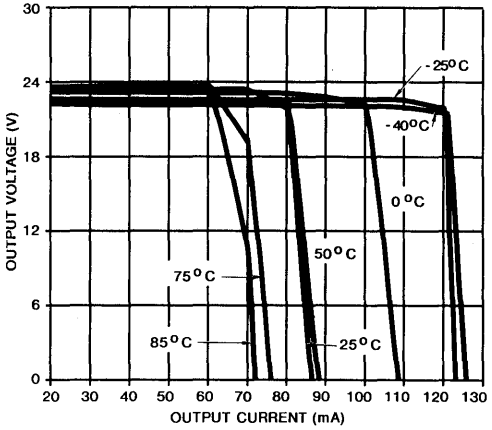


OUTPUT CURRENT LIMIT ($5V_{OUT}$)
50mA is the Maximum Specified Output Current

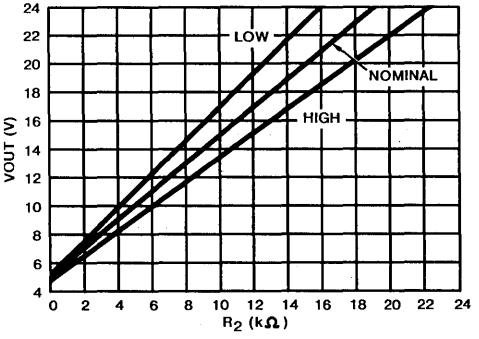


Typical Performance Curves Unless Otherwise Specified: T_A = +25°C, V_{AC} = 240Vrms, f = 50Hz, R_1 = 150Ω, C1 = 0.05µF, C2 = 470µF, C3 = 150pF, C4 = 1µF, V_{OUT} = 5V

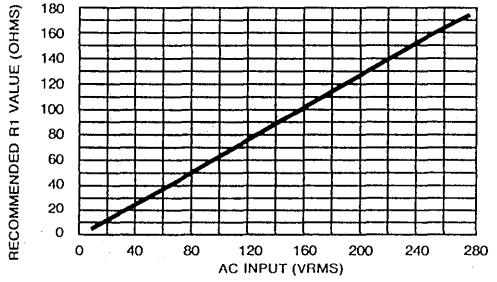
OUTPUT CURRENT LIMIT ($24V_{OUT}$)
50mA is the Maximum Specified Output Current



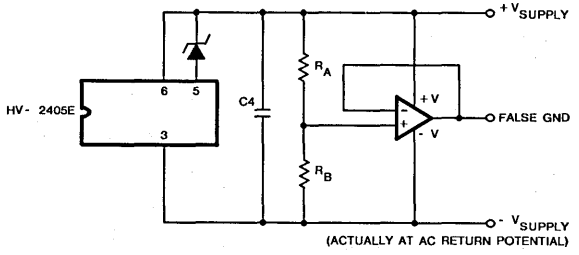
V_{OUT} vs. R_2 WITH TOLERANCES
Internal Resistors 15% High or Low



MINIMUM RECOMMENDED R_1 FOR NOMINAL INPUT VOLTAGE

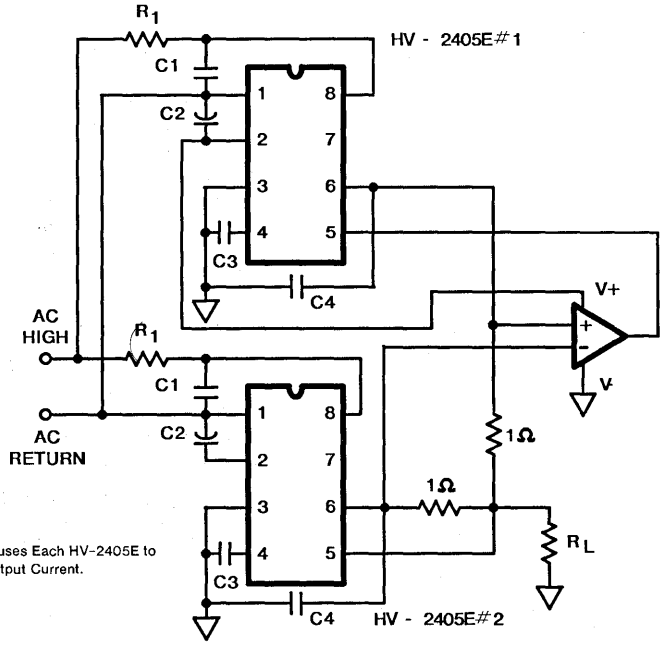


CREATING SYNTHESIZED ± SUPPLIES USING FALSE GROUND



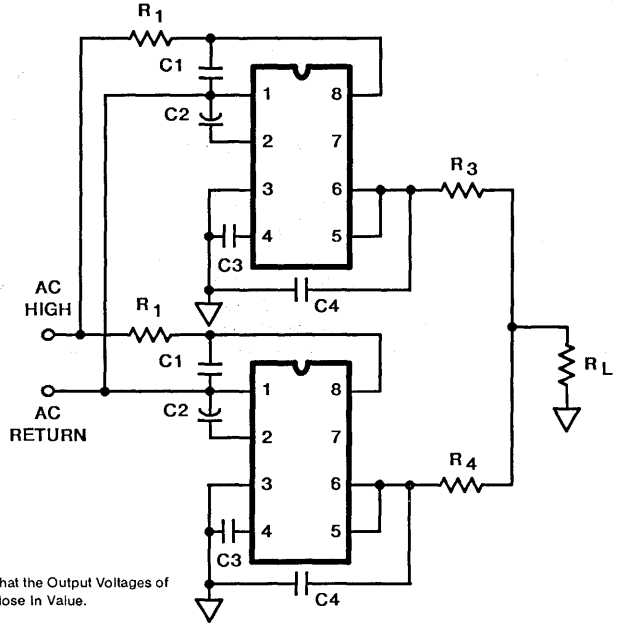
NOTES:
1. RA, RB voltage divider sets voltage of false ground anywhere between VOUT of HV-2405E and ground.
2. RA and RB should be large values (e.g. 470K)
3. Circuits powered with this method must ALL be referred to "False Gnd"
4. Op amp must be able to source/sink load current
5. Example: RA = 470K, RB = 470K, VOUT set to 24V. +VSUPPLY would be ≈ +12V
   -VSUPPLY would be ≈ -12V

HV-2405E Parallel Operation (Method #1)



NOTE: Operational Amplifier Causes Each HV-2405E to Contribute Equally to Output Current.

HV-2405E Parallel Operation (Method #2)



$$\Delta I_{OUT} = \frac{\Delta V_{OUT}}{R_3}$$

$R_3 = R_4$

NOTE: This Method Requires that the Output Voltages of Each HV-2405E are Close In Value.

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

ICL7660
CMOS Voltage Converter

GENERAL DESCRIPTION

The Harris ICL7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7660 performs supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complementary output voltages of −1.5V to −10.0V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660 can also be connected to function as a voltage doubler and will generate output voltages up to +18.6V with a +10V input.

Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latchup.

An enhanced direct replacement for this part, the ICL7660S, is now available and should be used for all new designs.

FEATURES

- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication ($V_{OUT} = (-) nV_{IN}$)**
- **99.9% Typical Open Circuit Voltage Conversion Efficiency**
- **98% Typical Power Efficiency**
- **Wide Operating Voltage Range 1.5V to 10.0V**
- **Easy to Use — Requires Only 2 External Non-Critical Passive Components**
- **No External Diode Over Full Temperature and Voltage Range**

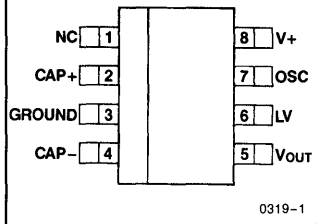
APPLICATIONS

- **On Board Negative Supply for Dynamic RAMs**
- **Localized μ-Processor (8080 Type) Negative Supplies**
- **Inexpensive Negative Supplies**
- **Data Acquisition Systems**

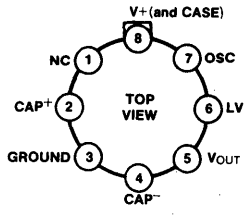
ORDERING INFORMATION

Part Number	Temp. Range	Package
ICL7660CTV	0° to +70°C	TO-99
ICL7660CBA	0°C to +70°C	8 PIN SOIC
ICL7660CPA	0° to +70°C	8 PIN MINI DIP
ICL7660MTV*	−55° to +125°C	TO-99

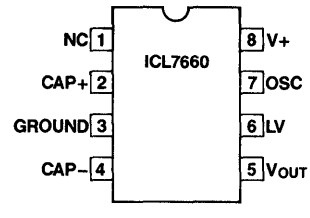
*Add /883B to part number if 883B processing is required.



(Outline Dwg BA)
8 LEAD S.O.



(Outline Dwg TV)
8 LEAD TO-99



(Outline Dwg PA)
8 LEAD MiniDIP

Figure 1: Pin Configurations

302063-005

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 10.5V
LV and OSC Input Voltage
(Note 1) ..... −0.3V to (V+ +0.3V) for V+ <5.5V
(V+ −5.5V) to (V+ +0.3V) for V+ >5.5V
Current into LV (Note 1) ..... 20μA for V+ >3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) ..... Continuous
Power Dissipation (Note 2)
ICL7660CTV 500mW
ICL7660CPA 300mW
ICL7660MTV 500mW

Operating Temperature Range
ICL7660M ..... −55°C to +125°C
ICL7660C ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature
(Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

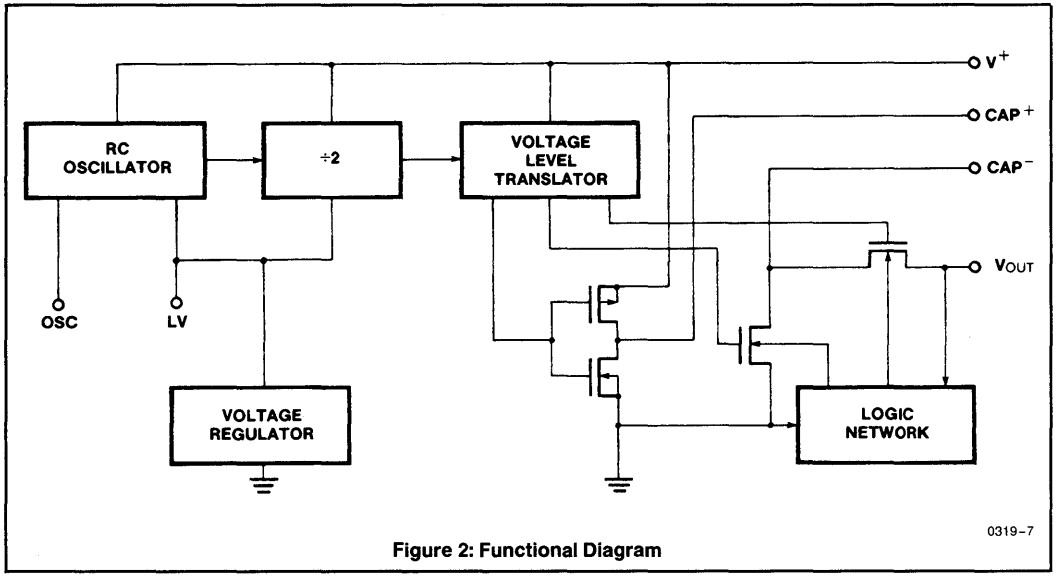


Figure 2: Functional Diagram

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $T_A = 25°C$, $C_{OSC} = 0$, Test Circuit Figure 3 (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
I^+	Supply Current	$R_L = \infty$		170	500	μA
V_L^+	Supply Voltage Range – Lo	$MIN \leq T_A \leq MAX$, $R_L = 10k\Omega$, LV to GROUND	1.5		3.5	V
V_H^+	Supply Voltage Range – Hi	$MIN \leq T_A \leq MAX$, $R_L = 10k\Omega$, LV Open	3.0		10.0	V

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $T_A = 25°C$, $C_{OSC} = 0$, Test Circuit Figure 3 (unless otherwise specified) (Continued)

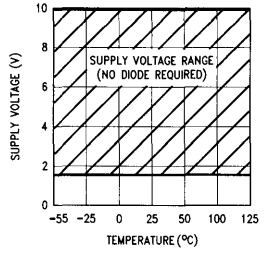
Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
R_{OUT}	Output Source Resistance	$I_{OUT} = 20mA$, $T_A = 25°C$		55	100	Ω
		$I_{OUT} = 20mA$, $0°C \le T_A \le +70°C$			120	Ω
		$I_{OUT} = 20mA$, $-55°C \le T_A \le +125°C$			150	Ω
		$V^+ = 2V$, $I_{OUT} = 3mA$, LV to GROUND $0°C \le T_A \le +70°C$			300	Ω
		$V^+ = 2V$, $I_{OUT} = 3mA$, LV to GROUND, $-55°C \le T_A \le +125°C$			400	Ω
f_{OSC}	Oscillator Frequency			10		kHz
P_{Ef}	Power Efficiency	$R_L = 5k\Omega$	95	98		%
$V_{OUT\ Ef}$	Voltage Conversion Efficiency	$R_L = \infty$	97	99.9		%
Z_{OSC}	Oscillator Impedance	$V^+ = 2$ Volts		1.0		MΩ
		$V = 5$ Volts		100		kΩ

Notes: 1. Connecting any input terminal to voltages greater than V+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7660.

2. Derate linearly above 50°C by 5.5mW/°C.

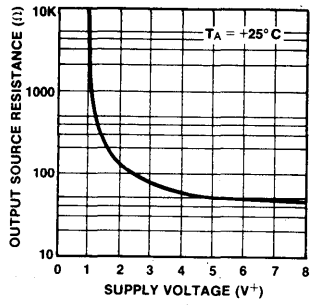
TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3)

OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE



0319-8

OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



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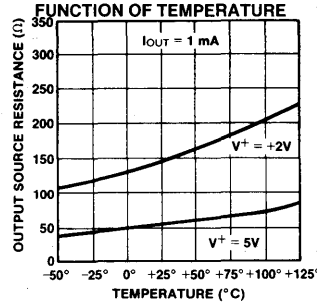
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE

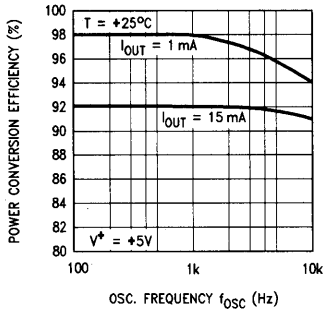


0319-10

NOTE: All typical values have been characterized but are not tested.

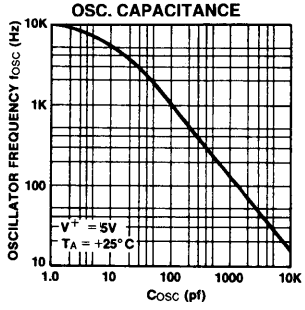
TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3) (Continued)

POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY



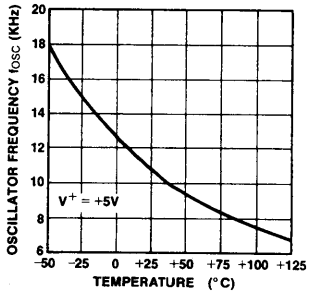
0319-11

FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE



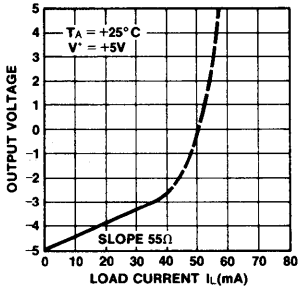
0319-12

UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE



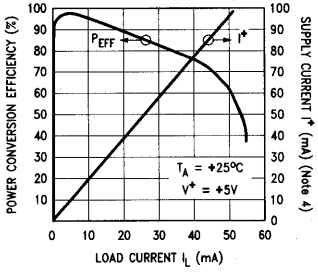
0319-13

OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



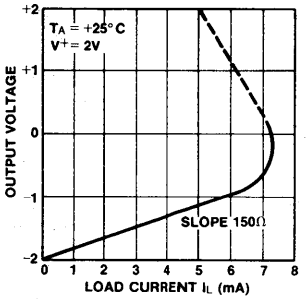
0319-14

SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



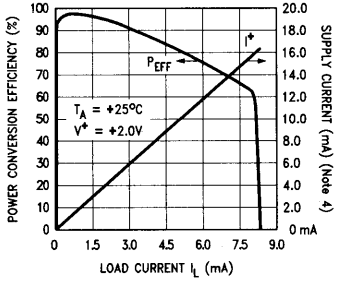
0319-15

OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



0319-16

SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

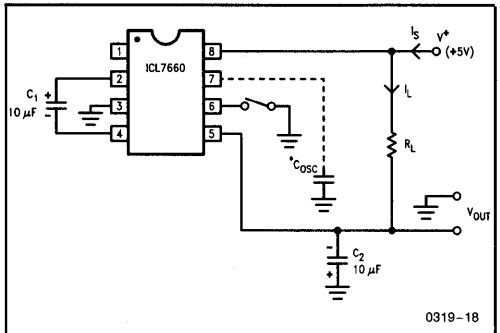


0319-17

NOTE 4. These curves include in the supply current that current fed directly into the load R_L from V^+ (see Figure 3). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660, to the negative side of the load. Ideally, $V_{OUT} \cong 2\ V_{IN}$, $I_S \cong 2\ I_L$, so $V_{IN} \bullet I_S \cong V_{OUT} \bullet I_L$.

2 POWER CONTROL CIRCUITS

NOTE: All typical values have been characterized but are not tested.



NOTE: 1. For large values of C_{OSC} (>1000pF) the values of C_1 and C_2 should be increased to 100µF.

Figure 3: ICL7660 Test Circuit

DETAILED DESCRIPTION

The ICL7660 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10µF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2. The ICL7660 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660, the 4 switches of Figure 4 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

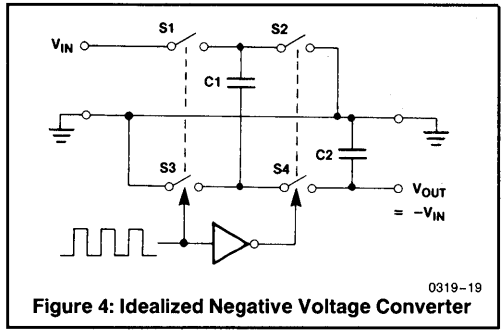


Figure 4: Idealized Negative Voltage Converter

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage converter can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power.

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660 approaches these conditions for negative voltage conversion if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

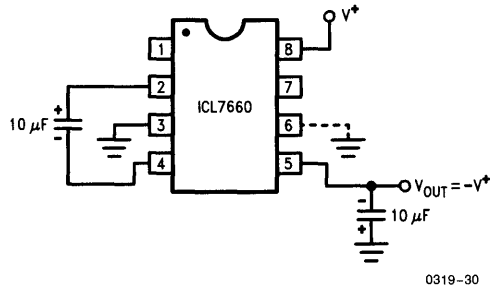
$$E = \tfrac{1}{2} C_1 (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 4) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

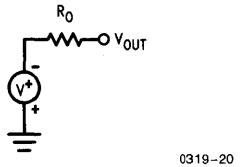
DO'S AND DON'TS

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
3. Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
4. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660 and the + terminal of C_2 must be connected to GROUND.
5. Add capacitor (~ 0.1µF, disc) from pin 8 to ground to limit rate of rise of input voltage to approximately 2V/µs.

NOTE: All typical values have been characterized but are not tested.



a) Configuration



b) Thevenin Equivalent

Figure 5: Simple Negative Converter

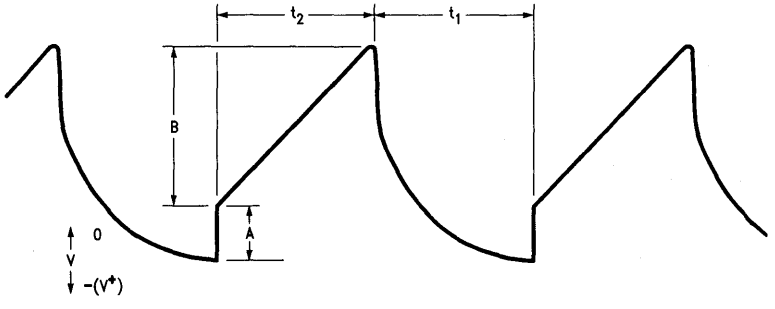


Figure 6: Output Ripple

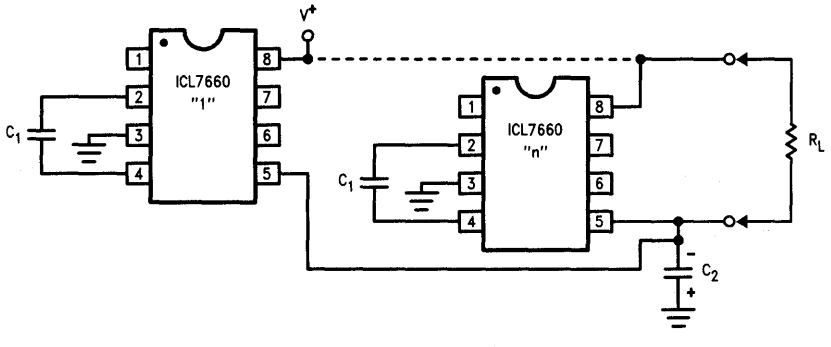


Figure 7: Paralleling Devices

NOTE: All typical values have been characterized but are not tested.

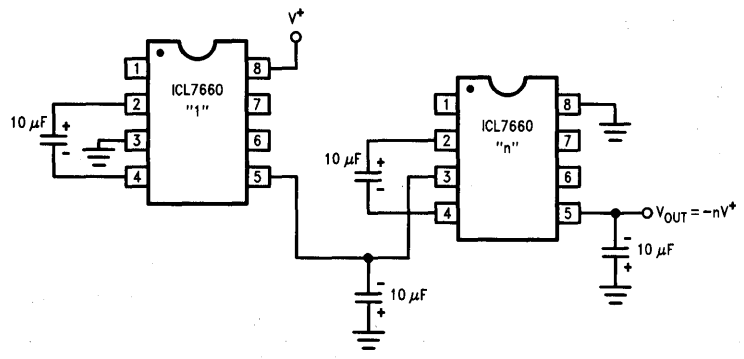


Figure 8: Cascading Devices for Increased Output Voltage

TYPICAL APPLICATIONS

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660 for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +1.5V to +10.0 volts is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 3.5 volts.

The output characteristics of the circuit in Figure 5a can be approximated by an ideal voltage source in series with a resistance as shown in Figure 5b. The voltage source has a value of $-V^+$. The output impedance (R_o) is a function of the ON resistance of the internal MOS switches (shown in Figure 4), the switching frequency, the value of C1 and C2, and the ESR (equivalent series resistance) of C1 and C2. A good first order approximation for R_o is:

$$R_o \cong 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) + \frac{1}{(f_{PUMP})(C1)} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2},\ R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four R_{SWX} terms as R_{SW}, we see that:

$$R_o \cong 2(R_{SW}) + \frac{1}{(f_{PUMP})(C1)} + 4(ESR_{C1}) + ESR_{C2}$$

R_{SW}, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 23Ω @ 25°C and 5V. Careful selection of C1 and C2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \bullet C1)$ component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \bullet C1)$ term, but may have the side effect of a net increase in output impedance when C1 > 10 µF and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where f_{OSC} = 10 kHz and C = C1 = C2 = 10 µF:

$$R_o \cong 2(23) + \frac{1}{(5 \bullet 10^3)(10^{-5})} + 4(ESR_{C1}) + ESR_{C2}$$

$$R_o \cong 46 + 20 + 5(ESR_C)$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \bullet C1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 101. Segment A is the voltage drop across the ESR of C2 at the instant it goes from being charged by C1 (current flow into C2) to being discharged through the load (current flowing out of C2). The magnitude of this current change is 2•Iout, hence the total drop is 2•Iout•eSR_{C2} volts. Segment B is the voltage change across C2 during time t_2, the half of the cycle when C2 supplies current to the load. The drop at B is Iout•t2/C2 volts. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{ripple} \cong \left[\frac{1}{2(f_{PUMP})(C2)} + 2(ESR_{C2})\right] Iout$$

Again, a low ESR capacitor will result in a higher performance output.

Paralleling Devices

Any number of ICL7660 voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\text{ (of ICL7660)}}{n\text{ (number of devices)}}$$

NOTE: All typical values have been characterized but are not tested.

Cascading Devices

The ICL7660 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\,(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660 R_{OUT} values.

Changing the ICL7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 9. In order to prevent possible device latchup, a 100kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be ½ of the clock frequency. Output transitions occur on the positive-going edge of the clock.

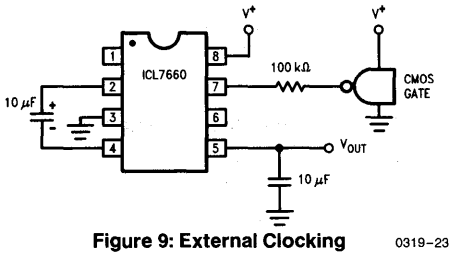


Figure 9: External Clocking 0319-23

It is also possible to increase the conversion efficiency of the ICL7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 10. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10µF to 100µF).

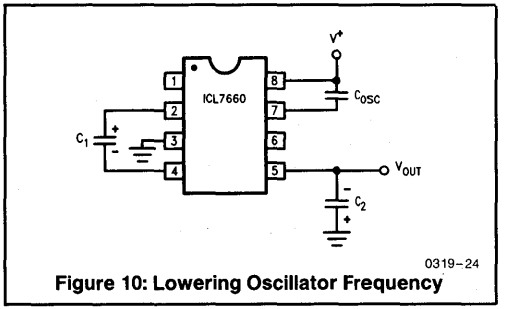


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Figure 10: Lowering Oscillator Frequency

Positive Voltage Doubling

The ICL7660 may be employed to achieve positive voltage doubling using the circuit shown in Figure 11. In this application, the pump inverter switches of the ICL7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10mA it will be approximately 60 ohms.

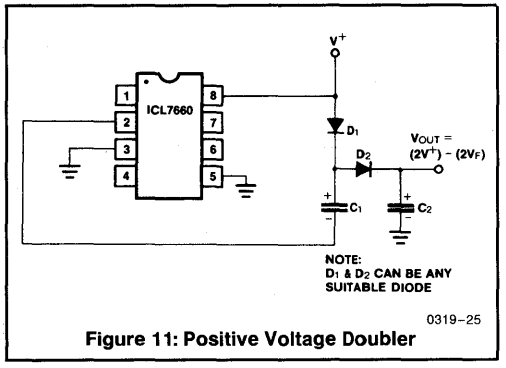

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Figure 11: Positive Voltage Doubler

2 POWER CONTROL CIRCUITS

NOTE: All typical values have been characterized but are not tested.

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 12 combines the functions shown in Figures 5 and 11 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and −5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

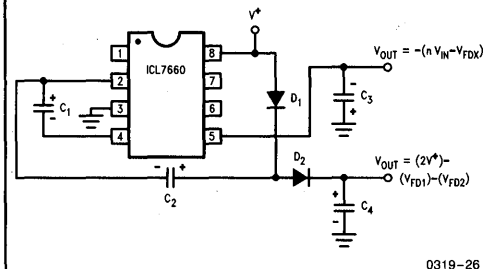


Figure 12: Combined Negative Voltage Converter and Positive Doubler

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 13. The combined load will be evenly shared between the two sides. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 8, +15V can be converted (via +7.5, and −7.5) to a nominal −15V, although with rather high series output resistance (~250Ω).

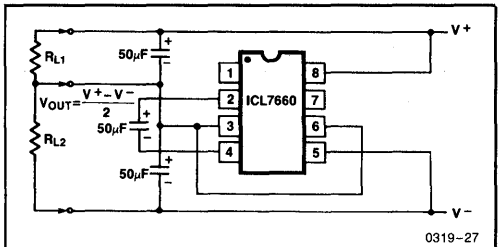


Figure 13: Splitting A Supply in Half

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660 can be a problem, particularly if the load current varies substantially. The circuit of Figure 14 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7660, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

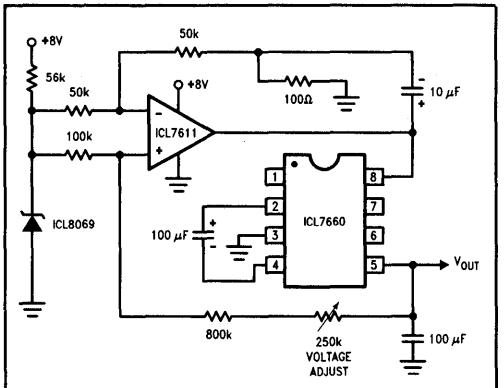


Figure 14: Regulating the Output Voltage

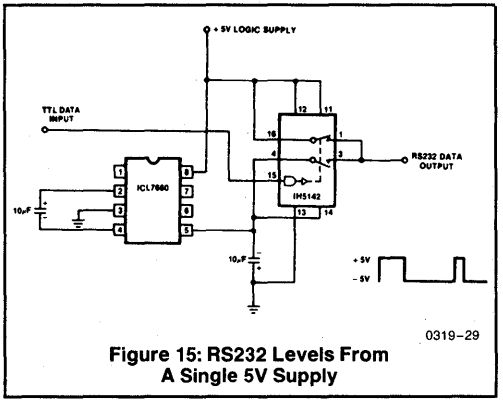


Figure 15: RS232 Levels From A Single 5V Supply

OTHER APPLICATIONS

Further information on the operation and use of the ICL7660 may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter".

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICL7660S
Super Voltage Converter

GENERAL DESCRIPTION

The ICL7660S Super Voltage Converter is a monolithic CMOS voltage conversion IC that guarantees significant performance advantages over other similar devices. It is a direct replacement for the industry-standard ICL7660 offering an ***extended*** operating supply voltage range up to 12V, with ***lower*** supply current. ***No external diode*** is needed for the ICL7660S. In addition, a ***Frequency Boost pin*** has been incorporated to enable the user to achieve lower output impedance despite using smaller capacitors. All improvements are highlighted in ***bold italics*** in the Electrical Characteristics section. ***Critical parameters are guaranteed over the entire commercial, industrial and military temperature ranges.***

The ICL7660S performs supply voltage conversion from positive to negative for an input range of 1.5V to 12V, resulting in complementary output voltages of −1.5V to −12V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660S can be connected to function as a voltage doubler and will generate up to 22.8V with a 12V input. It can also be used as a voltage multiplier or voltage divider.

The chip contains a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be over-driven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (3.5V to 12V), the LV pin is left floating to prevent device latchup.

FEATURES

- ***Guaranteed Lower*** **Max Supply Current for *All* Temperature Ranges**
- ***Guaranteed Wider*** **Operating Voltage Range —1.5V to 12V**
- ***No External Diode*** **Over Full Temperature and Voltage Range**
- **Boost Pin (Pin 1) for Higher Switching Frequency**
- ***Guaranteed*** **Minimum Power Efficiency of 96%**
- ***Improved*** **Minimum Open Circuit Voltage Conversion Efficiency of 99%**
- **Improved SCR Latchup Protection**
- **Simple Conversion of +5V Logic Supply to ±5V Supplies**
- **Simple Voltage Multiplication $V_{OUT} = (-)nV_{IN}$**
- **Easy to Use—Requires Only 2 External Non-Critical Passive Components**
- ***Improved*** **Direct Replacement for Industry-Standard ICL7660 and Other Second-Source Devices**

APPLICATIONS

- **Simple Conversion of +5V to ±5V Supplies**
- **Voltage Multiplication $V_{OUT} = \pm nV_{IN}$**
- **Negative Supplies for Data Acquisition Systems & Instrumentation**
- **RS232 Power Supplies**
- **Supply Splitter, $V_{OUT} = \pm V_S/2$**

ORDERING INFORMATION

Part Number	Temp. Range	Package
ICL7660SCBA	0°C to +70°C	8-Pin SOIC
ICL7660SCPA	0°C to +70°C	8-Pin Minidip
ICL7660SIBA	−25°C to +85°C	8-Pin SOIC
ICL7660SCTV	0°C to +70°C	TO-99
ICL7660SIPA	−25°C to +85°C	8-Pin Minidip
ICL7660SITV	−25°C to +85°C	TO-99
ICL7660SMTV*	−55°C to +125°C	TO-99

*Add /883B to part number if 883B processing is required.

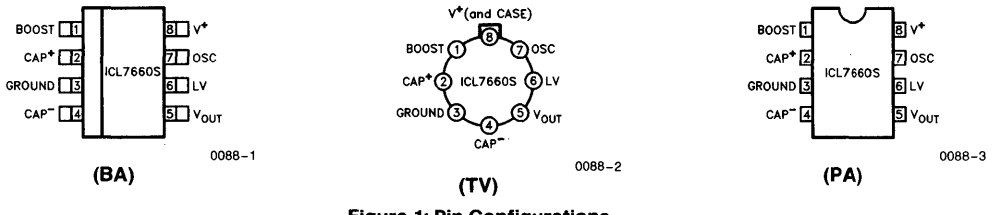


Figure 1: Pin Configurations

302163-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 13.0V

LV and OSC Input Voltage
(Note 1) ..... −0.3V to (V^+ + 0.3V) for $V^+ < 5.5V$
.....(V^+ − 5.5V) to (V^+ + 0.3V) for $V^+ > 5.5V$

Current into LV (Note 1).....20 μA for $V^+ > 3.5V$

Output Short Duration ($V_{SUPPLY} \leq 5.5V$).....Continuous

Power Dissipation (Note 2)
ICL7660SCTV.....500 mW
ICL7660SCPA .....300 mW
ICL7660SCBA .....300 mW
ICL7660SITV .....500 mW
ICL7660SIPA .....300 mW
ICL7660SIBA .....300 mW
ICL7660SMTV .....500 mW

Operating Temperature Range
ICL7660SM..... −55°C to +125°C
ICL7660SI..... −25°C to +85°C
ICL7660SC .....0°C to +70°C

Storage Temperature Range ..... −65°C to +150°C

Lead Temperature
(Soldering, 10 sec).....300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

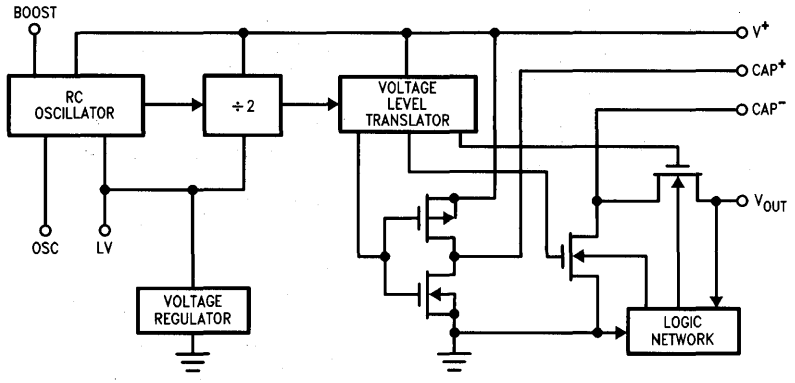


Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

$V^+ = 5V$, $T_A = 25°C$, OSC = Free running, Test Circuit Figure 3 (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
I+	***Supply Current*** (Note 3)	$R_L = \infty$, 25°C		***80***	***160***	µA
		$0°C < T_A < +70°C$			***180***	
		$-25°C < T_A < +85°C$			***180***	
		$-55°C < T_A < +125°C$			***200***	
V_H^+	***Supply Voltage Range—Hi*** (Note 4)	$R_L = 10K$, LV Open $T_{min} < T_A < T_{max}$	3.0		***12***	V
V_L^+	Supply Voltage Range—Lo	$R_L = 10K$, LV to GROUND $T_{min} < T_A < T_{max}$	1.5		3.5	V
R_{OUT}	***Output Source Resistance***	$I_{OUT} = 20$ mA, $T_A = 25°C$		60	100	Ω
		$I_{OUT} = 20$ mA, $0°C < T_A < +70°C$			120	
		$I_{OUT} = 20$ mA, $-25°C < T_A < +85°C$			120	
		$I_{OUT} = 20$ mA, $-55°C < T_A < +125°C$			150	
		$I_{OUT} = 3$ mA, $V^+ = 2V$, LV = GND, $0°C < T_A < +70°C$			***250***	
		$I_{OUT} = 3$ mA, $V^+ = 2V$, LV = GND, $-25°C < T_A < +85°C$			***300***	
		$I_{OUT} = 3$ mA, $V^+ = 2V$, LV = GND, $-55°C < T_A < +125°C$			400	
f_{OSC}	***Oscillator Frequency***	$C_{OSC} = 0$, Pin 1 Open or GND	***5***	10		kHz
		Pin 1 = V^+		***35***		
PEff	***Power Efficiency***	$R_L = 5$ kΩ	***96***	98		%
		$T_{min} < T_A < T_{max}$	***95***	***97***		
V_{OUT} Eff	***Voltage Conversion Efficiency***	$R_L = \infty$	***99***	99.9		%
Z_{OSC}	Oscillator Impedance	$V^+ = 2V$		1		MΩ
		$V^+ = 5V$		100		kΩ

NOTE 1: Connecting any terminal to voltages greater than V^+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of ICL7660s.

2: Derate linearly above 50°C by 5.5 mW/°C.

3: In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of 5 pF.

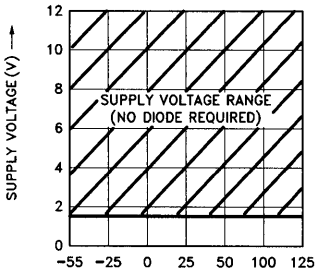
4: The Harris ICL7660S can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.

5: All significant improvements over the industry-standard ICL7660 are highlighted in ***bold italics.***

NOTE: All typical values have been characterized but are not tested.

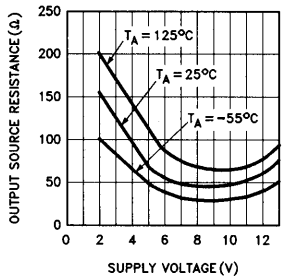
TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3)

OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE



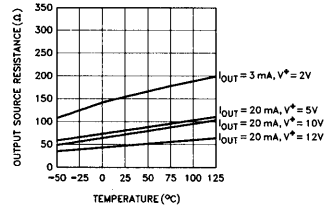
0088-5

OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



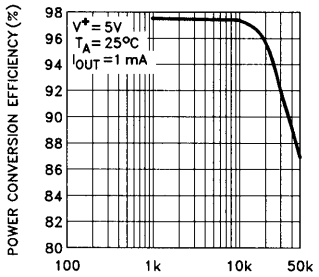
0088-6

OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



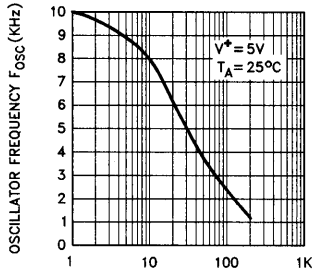
0088-7

POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY



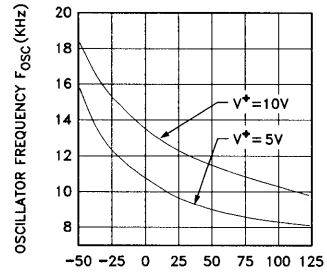
0088-8

FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE



0088-9

UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

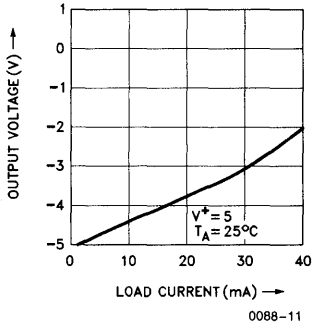


0088-10

NOTE: All typical values have been characterized but are not tested.

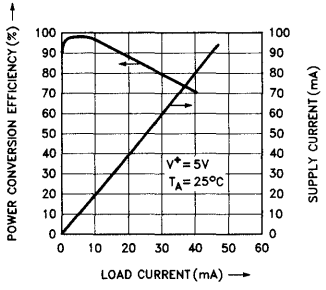
TYPICAL PERFORMANCE CHARACTERISTICS (Circuit of Figure 3) (Continued)

OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



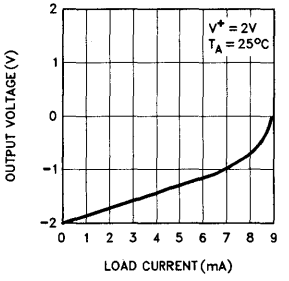
0088-11

SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



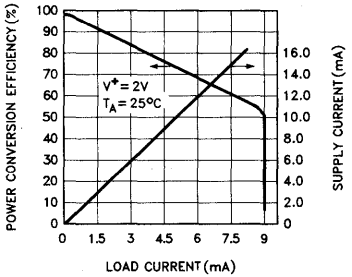
0088-12

OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



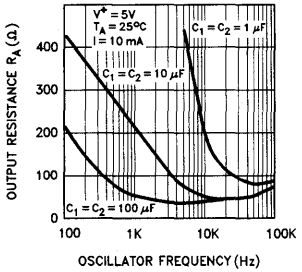
0088-13

SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



0088-14

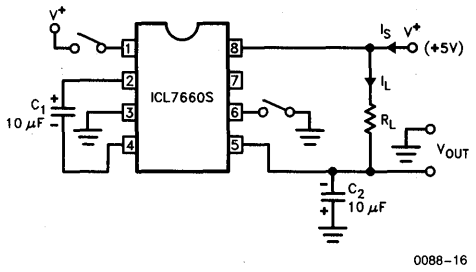
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY



0088-15

NOTE 4: These curves include in the supply current that current fed directly into the load R_L from V^+ (see Figure 3). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660S, to the negative side of the load. Ideally, $V_{OUT} \cong 2\ V_{IN}$, $I_S \cong 2\ I_L$, so $V_{IN} \bullet I_S \cong V_{OUT} \bullet I_L$.

NOTE: All typical values have been characterized but are not tested.



NOTE 1: For large values of C_{OSC} (>1000pF) the values of C_1 and C_2 should be increased to 100μF.

Figure 3: ICL7660S Test Circuit

DETAILED DESCRIPTION

The ICL7660S contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10μF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2. The ICL7660S approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7660S, the 4 switches of Figure 4 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT}=V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660S by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660S is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

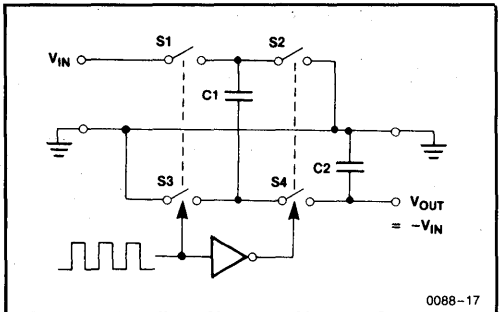


Figure 4: Idealized Negative Voltage Converter

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage converter can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power.

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660S approaches these conditions for negative voltage conversion if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E=\tfrac{1}{2}C_1(V_1^2-V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 4) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DO'S AND DON'TS

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
3. Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including startup are okay.
4. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660S and the + terminal of C_2 must be connected to GROUND.

NOTE: All typical values have been characterized but are not tested.

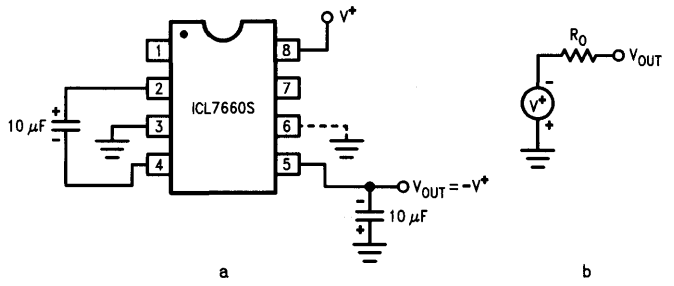


Figure 5: Simple Negative Converter and its Output Equivalent

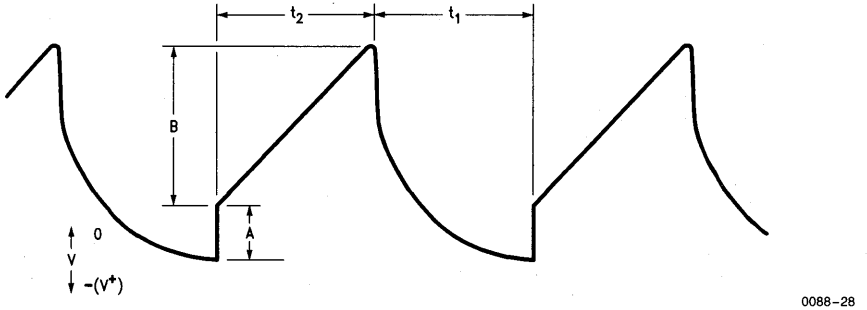


Figure 6: Output Ripple

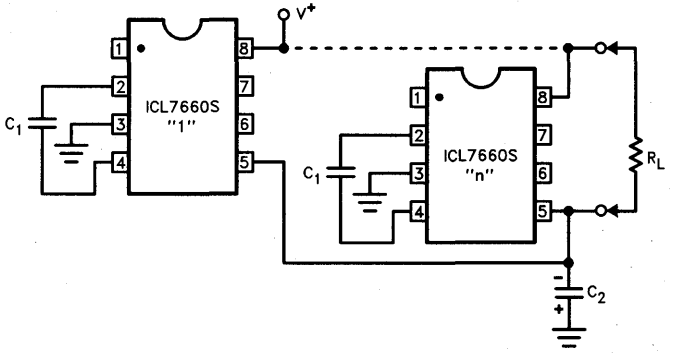
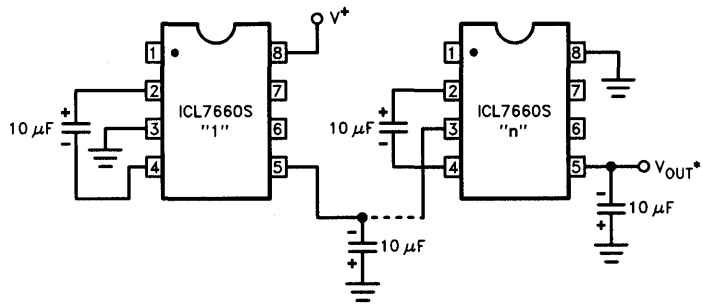


Figure 7: Paralleling Devices

NOTE: All typical values have been characterized but are not tested.



*NOTE 1: $V_{OUT} = -nV^+$ for $1.5V \leq V^+ \leq 12V$.

Figure 8: Cascading Devices for Increased Output Voltage

TYPICAL APPLICATIONS

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660S for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +1.5V to +12V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 3.5 volts.

The output characteristics of the circuit in Figure 5a can be approximated by an ideal voltage source in series with a resistance as shown in Figure 5b. The voltage source has a value of −(V+). The output impedance (R_o) is a function of the ON resistance of the internal MOS switches (shown in Figure 4), the switching frequency, the value of C1 and C2, and the ESR (equivalent series resistance) of C1 and C2. A good first order approximation for R_o is:

$$R_o \cong 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) + \frac{1}{f_{PUMP} \times C1} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2},\ R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four R_{SWX} terms as R_{SW}, we see that:

$$R_o \cong 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C1} + 4 \times ESR_{C1} + ESR_{C2}\ \Omega$$

R_{SW}, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 23Ω @ 25°C and 5V. Careful selection of C1 and C2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \times C1)$ component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \times C1)$ term, but may have the side effect of a net increase in output impedance when C1 > 10 μF and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where f_{OSC} = 10 kHz and C = C1 = C2 = 10 μF:

$$R_o \cong 2 \times 23 + \frac{1}{(5 \times 10^3 \times 10 \times 10^{-6})} + 4 \times ESR_{C1} + ESR_{C2}$$

$$R_o \cong 46 + 20 + 5 \times ESR_C\ \Omega$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \times C1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 6. Segment A is the voltage drop across the ESR of C2 at the instant it goes from being charged by C1 (current flowing into C2) to being discharged through the load (current flowing out of C2). The magnitude of this current change is $2 \times I_{OUT}$, hence the total drop is $2 \times I_{OUT} \times ESR_{C2}$ volts. Segment B is the voltage change across C2 during time t_2, the half of the cycle when C2 supplies current to the load. The drop at B is $I_{OUT} \times t_2/C2$ volts. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{ripple} \cong \left(\frac{1}{2 \times f_{PUMP} \times C2} + 2 \times ESR_{C2}\right) \times I_{OUT}$$

Again, a low ESR capacitor will result in a higher performance output.

Paralleling Devices

Any number of ICL7660S voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ (\text{of ICL7660S})}{n\ (\text{number of devices})}$$

Cascading Devices

The ICL7660S may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN}),$$

NOTE: All typical values have been characterized but are not tested.

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660S R_{OUT} values.

Changing the ICL7660S Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to alter the oscillator frequency. This can be achieved simply by one of several methods described below.

By connecting the Boost Pin (Pin 1) to V^+, the oscillator charge and discharge current is increased and, hence, the oscillator frequency is increased by approximately 3½ times. The result is a decrease in the output impedance and ripple. This is of major importance for surface-mount applications where capacitor size and cost are critical. Smaller capacitors, e.g. 0.1 μF, can be used in conjunction with the Boost Pin in order to achieve similar output currents compared to the device free running with $C_1 = C_2 = 10$ μF or 100 μF. (Refer to graph of Output Source Resistance as a Function of Oscillator Frequency).

Increasing the oscillator frequency can also be achieved by overdriving the oscillator from an external clock, as shown in Figure 9. In order to prevent device latchup, a 100 kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be ½ of the clock frequency. Output transitions occur on the positive-going edge of the clock.

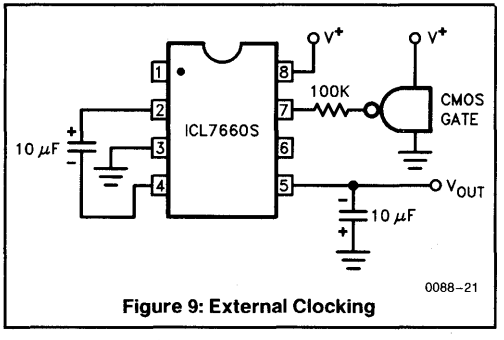


Figure 9: External Clocking

It is also possible to increase the conversion efficiency of the ICL7660S at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 10. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10μF to 100μF).

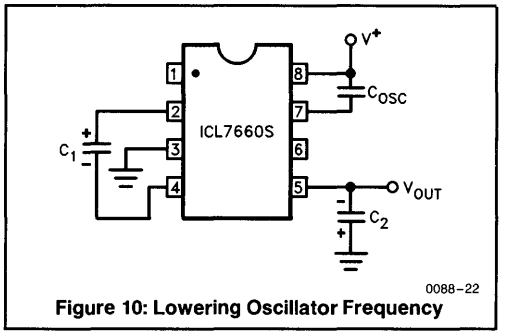
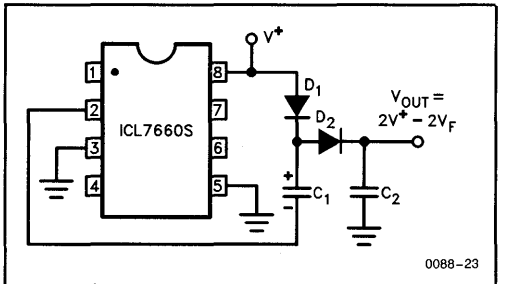


Figure 10: Lowering Oscillator Frequency



NOTE: D_1 & D_2 can be any suitable diode.

Figure 11: Positive Voltage Doubler

Positive Voltage Doubling

The ICL7660S may be employed to achieve positive voltage doubling using the circuit shown in Figure 11. In this application, the pump inverter switches of the ICL7660S are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5$ volts and an output current of 10mA it will be approximately 60 ohms.

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 12 combines the functions shown in Figures 5 and 11 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and −5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

NOTE: All typical values have been characterized but are not tested.

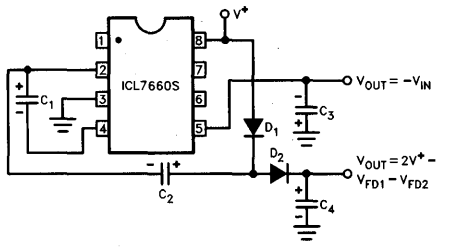


Figure 12: Combined Negative Voltage Converter and Positive Doubler

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 13. The combined load will be evenly shared between the two sides, and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 8, +15V can be converted (via +7.5, and −7.5) to a nominal −15V, although with rather high series output resistance (~250Ω).

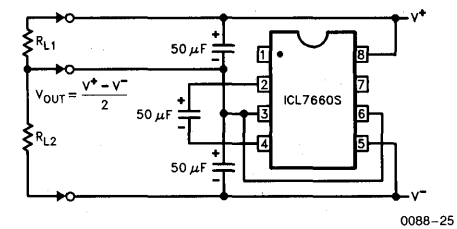


Figure 13: Splitting A Supply in Half

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660S can be a problem, particularly if the load current varies substantially. The circuit of Figure 14 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660S's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7660S, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

OTHER APPLICATIONS

Further information on the operation and use of the ICL7660S may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter".

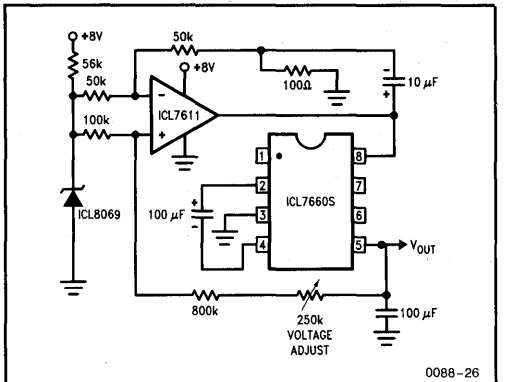


Figure 14: Regulating the Output Voltage

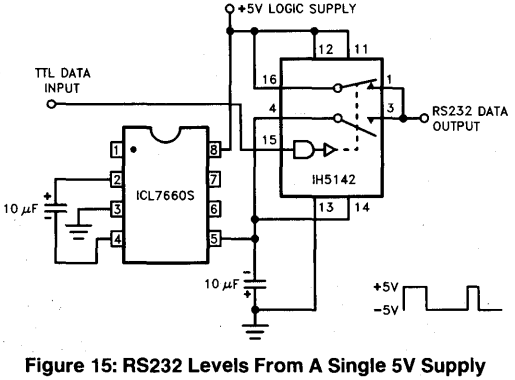


Figure 15: RS232 Levels From A Single 5V Supply

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICL7662
CMOS Voltage Converter

GENERAL DESCRIPTION

The Harris ICL7662 is a monolithic high-voltage CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7662 performs supply voltage conversion from positive to negative for an input range of +4.5V to +20.0V, resulting in complementary output voltages of −4.5V to −20V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7662 can also function as a voltage doubler, and will generate output voltages up to +38.6V with a +20V input.

Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 15.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+10 to +20V), the LV pin is left floating to prevent device latchup.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7662CTV	0°C to +70°C	TO-99
ICL7662CPA	0°C to +70°C	8 PIN MINI DIP
ICL7662MTV*	−55°C to +125°C	TO-99

*Add /883B to Part Number for 883B Processing.

FEATURES

- **No External Diode Needed Over Entire Temperature Range**
- **Pin Compatible With ICL7660**
- **Simple Conversion of +15V Supply to −15V Supply**
- **Simple Voltage Multiplication ($V_{OUT}=(-)\,nV_{IN}$)**
- **99.9% Typical Open Circuit Voltage Conversion Efficiency**
- **96% Typical Power Efficiency**
- **Wide Operating Voltage Range 4.5V to 20.0V**
- **Easy to Use — Requires Only 2 External Non-Critical Passive Components**

APPLICATIONS

- **On Board Negative Supply for Dynamic RAMs**
- **Localized μ-Processor (8080 Type) Negative Supplies**
- **Inexpensive Negative Supplies**
- **Data Acquisition Systems**
- **Up to −20V for Op Amps**

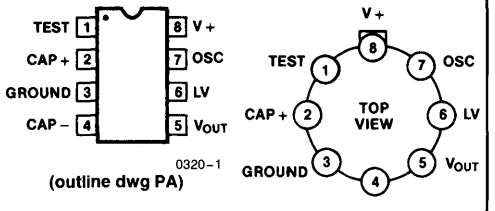


Figure 1: Pin Configurations

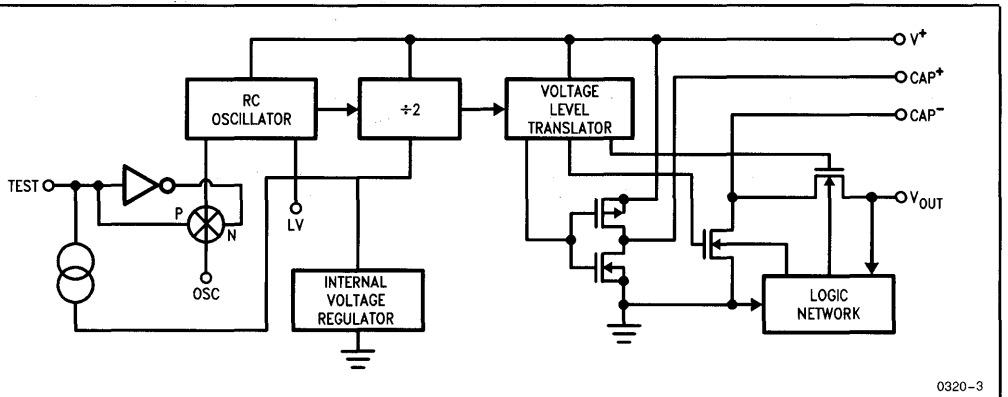


Figure 2: Functional Diagram

302064-005

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 22V
Oscillator Input Voltage (Note 1) .....
−0.3V to (V+ +0.3V) for V+ <10V
(V+ −10V) to (V+ +0.3V) for V+ >10V
Current into LV (Note 1) ..... 20μA for V+ >10V
Output Short Duration ..... Continuous

Power Dissipation (Note 2)
ICL7662CTY 500mW
ICL7662CPA 300mW
ICL7662MTY 500mW
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

$V^+ = 15V$, $T_A = 25°C$, $C_{OSC} = 0$, unless otherwise stated. Test Circuit Figure 3.

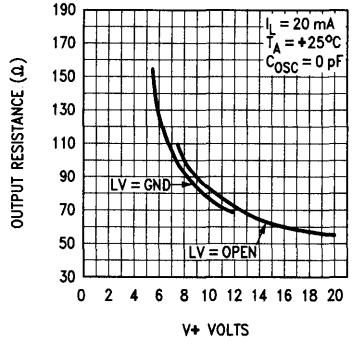
Symbol	Parameter	Test Conditions		Limits			Units
				Min	Typ	Max	
V^+L	Supply Voltage Range-Lo	$R_L = 10k\Omega$, LV = GND	Min < T_A < Max	4.5		11	V
V^+H	Supply Voltage Range-Hi	$R_L = 10k\Omega$, LV = Open	Min < T_A < Max	9		20	V
I^+	Supply Current	$R_L = \infty$, LV = Open	$T_A = 25°C$		.25	.60	mA
			$0°C < T_A < +70°C$		.30	.85	
			$-55°C < T_A < +125°C$		.40	1.0	
R_o	Output Source Resistance	$I_o = 20mA$, LV = Open	$T_A = 25°C$		60	100	Ω
			$0°C < T_A < +70°C$		70	120	
			$-55°C < T_A < +125°C$		90	150	
I^+	Supply Current	$V^+ = 5V$,	$T_A = 25°C$		20	150	μA
		$R_L = \infty$, LV = GND	$0°C < T_A < +70°C$		25	200	
			$-55°C < T_A < +125°C$		30	250	
R_o	Output Source Resistance	$V^+ = 5V$,	$T_A = 25°C$		125	200	Ω
		$I_o = 3mA$, LV = GND	$0°C < T_A < +70°C$		150	250	
			$-55°C < T_A < +125°C$		200	350	
F_{osc}	Oscillator Frequency				10		kHz
P_{eff}	Power Efficiency	$R_L = 2K\Omega$	$T_A = 25°C$	93	96		%
			Min < T_A < Max	90	95		
V_{OEf}	Voltage Conversion Effic.	$R_L = \infty$	Min < T_A < Max	97	99.9		%
I_{osc}	Oscillator Sink or Source Current	$V^+ = 5V$ ($V_{osc} = 0V$ to $+5V$)			0.5		μA
		$V^+ = 15V$ ($V_{osc} = +5V$ to $+15V$)			4.0		

NOTES: 1. Connecting any terminal to voltages greater than V^+ or less than ground may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7662.
2. Derate linearly above 50°C by 5.5mW/°C.
3. Pin 1 is a Test pin and is not connected in normal use. When the TEST pin is connected to V^+, an internal transmission gate disconnects any external parasitic capacitance from the oscillator which would otherwise reduce the oscillator frequency from its nominal value.

NOTE: All typical values have been characterized but are not tested.

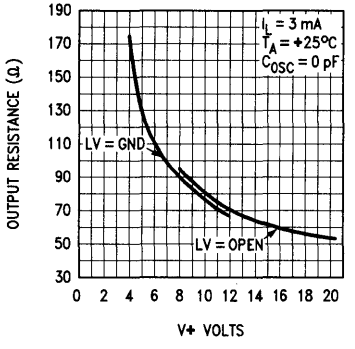
TYPICAL PERFORMANCE CHARACTERISTICS (See Test Circuit of Figure 3)

OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



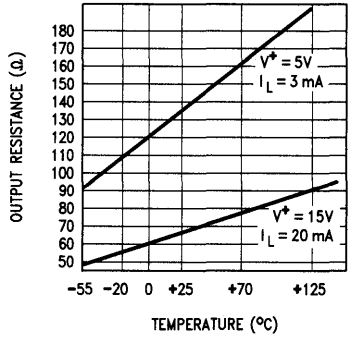
0320-4

OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



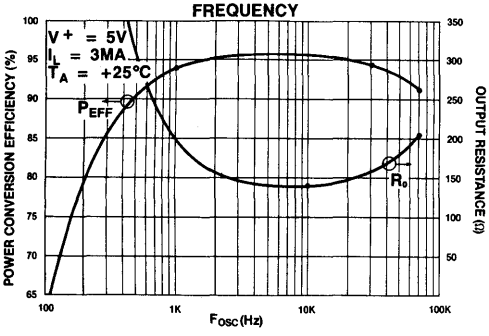
0320-5

OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



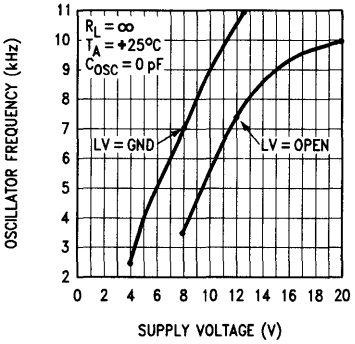
0320-6

POWER CONVERSION EFFICIENCY AND OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY



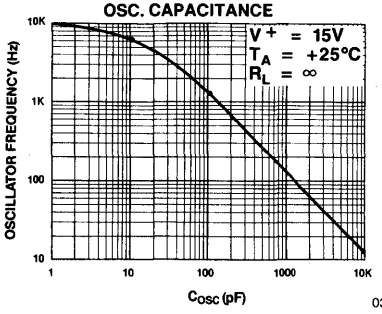
0320-7

OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



0320-8

FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE

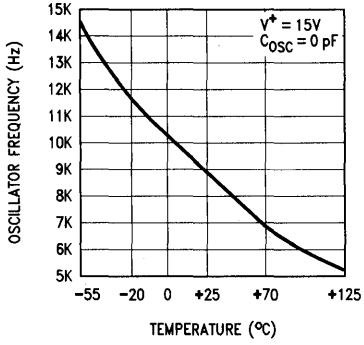


0320-9

NOTE: All typical values have been characterized but are not tested.

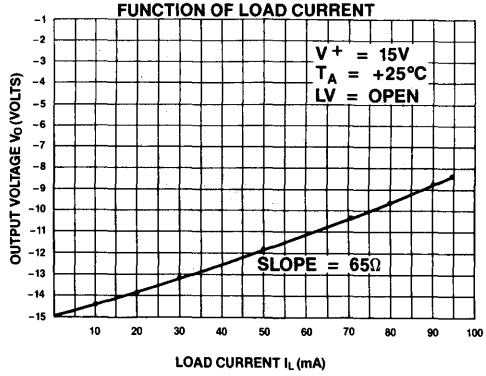
TYPICAL PERFORMANCE CHARACTERISTICS (See Test Circuit of Figure 3) (Continued)

UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE



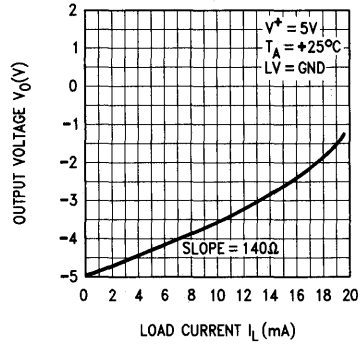
0320-10

OUTPUT VOLTAGE AS A FUNCTION OF LOAD CURRENT



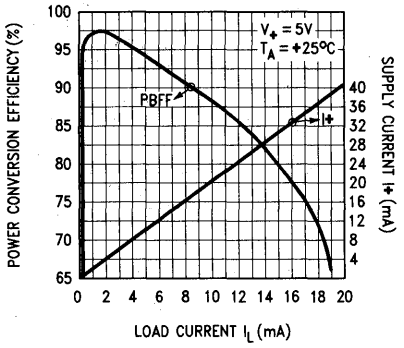
0320-11

OUTPUT VOLTAGE AS A FUNCTION OF LOAD CURRENT



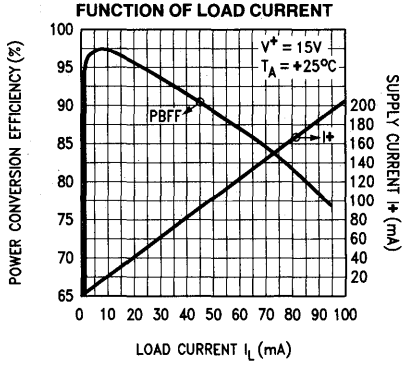
0320-12

SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



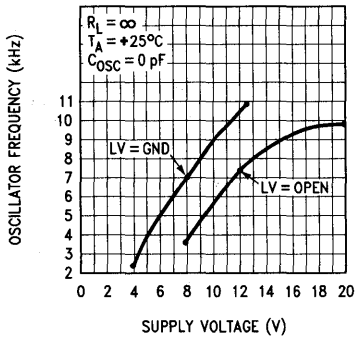
0320-13

SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



0320-14

FREQUENCY OF OSCILLATION AS A FUNCTION OF SUPPLY VOLTAGE

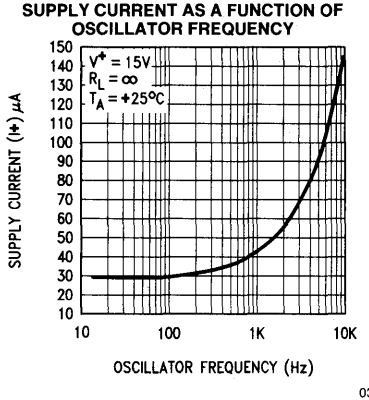


0320-15

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

(See Test Circuit of Figure 3) (Continued)



NOTE 4.

Note that these curves include in the supply current that current fed directly into the load R_L from V^+ (see Figure 3). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7662, to the negative side of the load. Ideally, $V_{LOAD} \cong 2V_{IN}$, $I_S \cong 2\ I_L$, so $V_{IN} \bullet I_S \cong V_{LOAD} \bullet I_L$

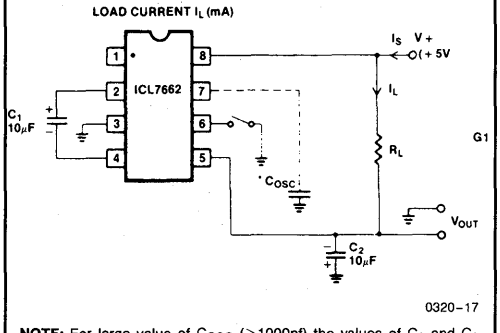
CIRCUIT DESCRIPTION

The ICL7662 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10μF polarized electrolytic capacitors. The mode of operation of the device may be best understood by considering Figure 4, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2. The ICL7662 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7662, the 4 switches of Figure 4 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7662 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7662 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 11 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.



NOTE: For large value of C_{OSC} (>1000pf) the values of C_1 and C_2 should be increased to 100μF.

Figure 3: ICL7662 Test Circuit

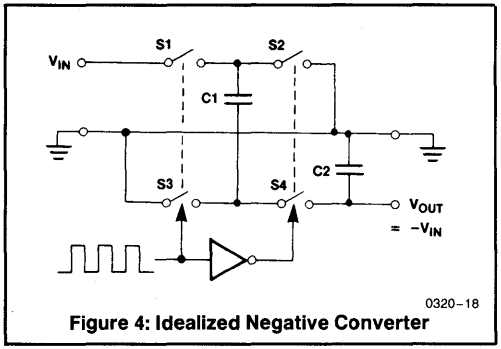


Figure 4: Idealized Negative Converter

NOTE: All typical values have been characterized but are not tested.

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7662 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = \tfrac{1}{2} C_1 (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 4) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DO'S AND DON'TS

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 11 volts.
3. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7662 and the + terminal of C_2 must be connected to GROUND.

TYPICAL APPLICATIONS

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7662 for generation of negative supply voltages. Figure 5 shows typical connections to provide a negative supply where a positive supply of +4.5V to 20.0V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 11 volts.

The output characteristics of the circuit in Figure 5a can be approximated by an ideal voltage source in series with a resistance as shown in Figure 5b. The voltage source has a value of −(V+). The output impedance (R_o) is a function of the ON resistance of the internal MOS switches (shown in Figure 4), the switching frequency, the value of C1 and C2, and the ESR (equivalent series resistance) of C1 and C2. A good first order approximation for R_o is:

$$R_o \cong 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) + \frac{1}{f_{PUMP} \times C1} + ESR_{C2}$$

$$\left(f_{PUMP} = \frac{f_{OSC}}{2},\ R_{SWX} = \text{MOSFET switch resistance}\right)$$

Combining the four R_{SWX} terms as R_{SW}, we see that:

$$R_o \cong 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C1} + 4 \times ESR_{C1} + ESR_{C2}\ \Omega$$

R_{SW}, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 24Ω @ 25°C and 15V, and 53Ω @ 25°C and 5V. Careful selection of C1 and C2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \times C1)$ component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \times C1)$ term, but may have the side effect of a net increase in output impedance when C1 > 10 μF and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where f_{OSC} = 10 kHz and C = C1 = C2 = 10 μF:

$$R_o \cong 2 \times 23 + \frac{1}{(5 \times 10^3 \times 10 \times 10^{-6})} + 4 \times ESR_{C1} + ESR_{C2}$$

$$R_o \cong 46 + 20 + 5 \times ESR_C\ \Omega$$

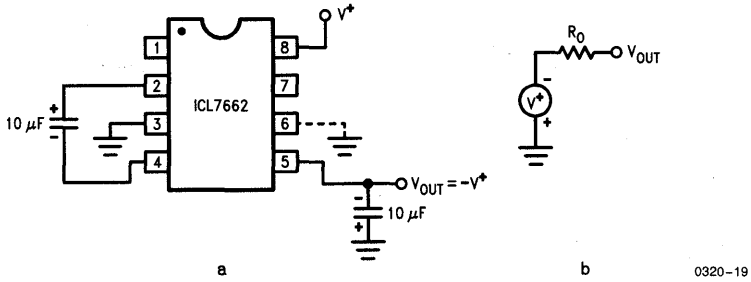


Figure 5: Simple Negative Converter and Its Output Equivalent

NOTE: All typical values have been characterized but are not tested.

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \times C1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 6. Segment A is the voltage drop across the ESR of C2 at the instant it goes from being charged by C1 (current flowing into C2) to being discharged through the load (current flowing out of C2). The magnitude of this current change is $2 \times I_{OUT}$, hence the total drop is $2 \times I_{OUT} \times ESR_{C2}$ volts. Segment B is the voltage change across C2 during time t_2, the half of the cycle when C2 supplies current to the load. The drop at B is $I_{OUT} \times t_2/C2$ volts. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{ripple} \cong \left(\frac{1}{2 \times f_{PUMP} \times C2} + 2 \times ESR_{C2}\right) \times I_{OUT}$$

Again, a low ESR capacitor will result in a higher performance output.

Paralleling Devices

Any number of ICL7662 voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately

$$R_{OUT} = \frac{R_{OUT}\text{ (of ICL7662)}}{\text{n (number of devices)}}$$

Cascading Devices

The ICL7662 may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\,(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7662 R_{OUT} values.

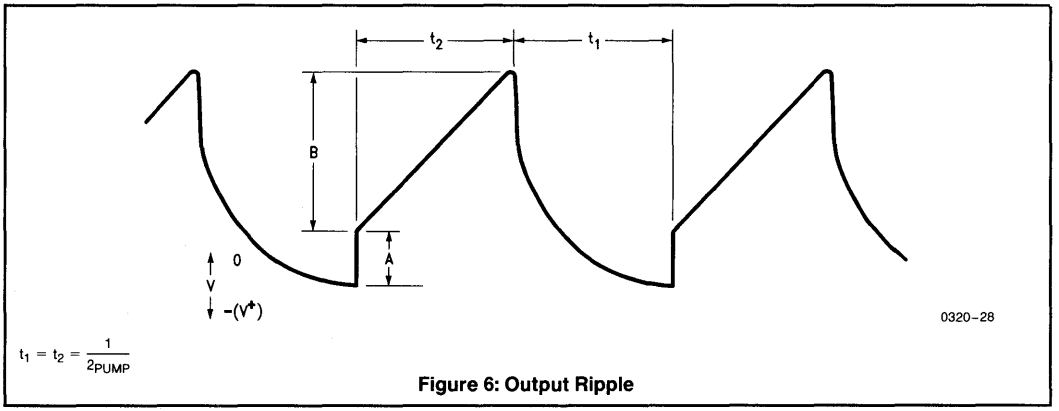


Figure 6: Output Ripple

NOTE: All typical values have been characterized but are not tested.

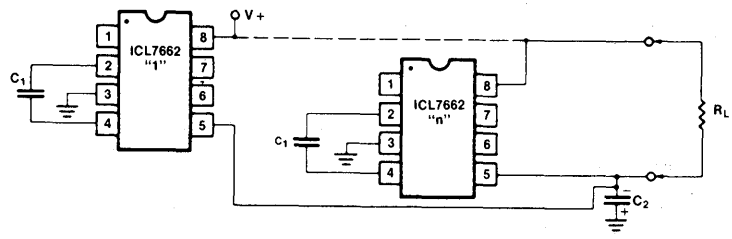


Figure 7: Paralleling Devices

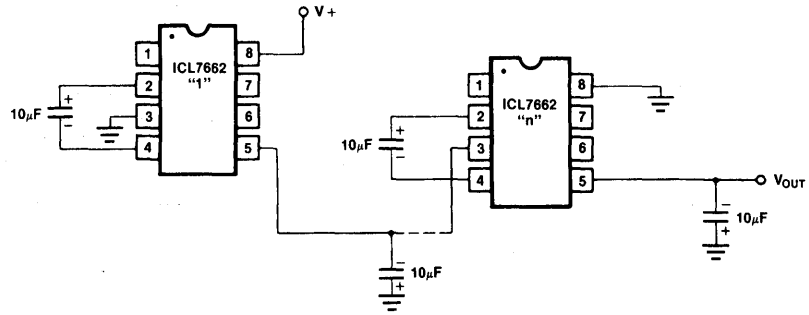


Figure 8: Cascading Devices for Increased Output Voltage

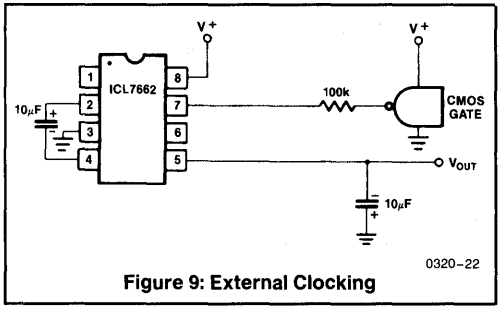


Figure 9: External Clocking

Changing the ICL7662 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 9. In order to prevent possible device latchup, a 100kΩ resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be ½ of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the ICL7662 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 10. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V^+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10μF to 100μF).

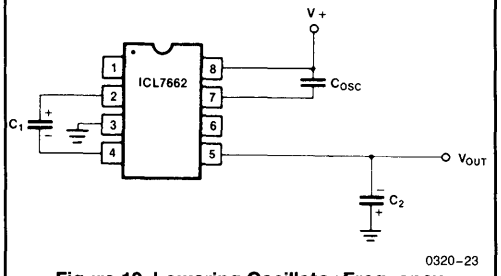


Figure 10: Lowering Oscillator Frequency

NOTE: All typical values have been characterized but are not tested.

Positive Voltage Doubling

The ICL7662 may be employed to achieve positive voltage doubling using the circuit shown in Figure 11. In this application, the pump inverter switches of the ICL7662 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2V^+) - (2V_F)$ or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 15$ volts and an output current of 10mA it will be approximately 70 ohms.

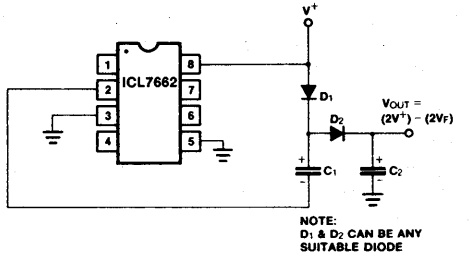


Figure 11: Positive Voltage Doubler

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 12 combines the functions shown in Figures 5 and 11 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and −5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

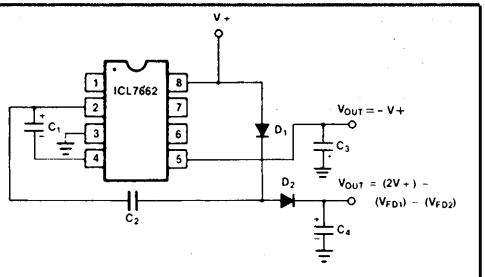


Figure 12: Combined Negative Converter and Positive Doubler

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 13. The combined load will be evenly shared between the two sides and, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 8, +30V can be converted (via +15V, and −15V) to a nominal −30V, although with rather high series output resistance (~250Ω).

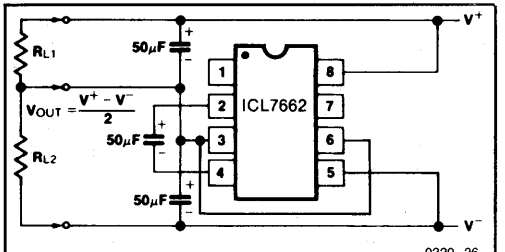


Figure 13: Splitting A Supply in Half

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7662 can be a problem, particularly if the load current varies substantially. The circuit of Figure 14 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7662's output does not respond instantaneously to a change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7662, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

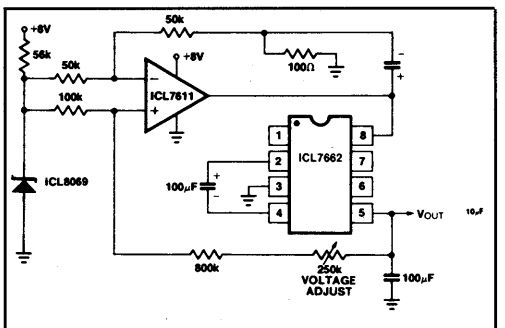


Figure 14: Regulating the Output Voltage

OTHER APPLICATIONS

Further information on the operation and use of the ICL7662 may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter".

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICL7663S

CMOS Programmable Micropower Positive Voltage Regulator

GENERAL DESCRIPTION

The Harris ICL7663S Super Programmable Micropower Voltage Regulator is a low power, high efficiency positive voltage regulator which accepts 1.6V to 16V inputs and provides adjustable outputs from 1.3V to 16V at currents up to 40 mA.

It is a direct replacement for the industry standard ICL7663B offering ***wider*** operating voltage and temperature ranges, ***improved*** output accuracy (ICL7663SA), ***better*** temperature coefficient, ***guaranteed*** maximum supply current, and ***guaranteed*** line and load regulation. All improvements are highlighted in ***bold italics*** in the electrical characteristics section. ***Critical parameters are guaranteed over the entire commercial and industrial temperature ranges.*** The ICL7663S/SA programmable output voltage is set by two external resistors. The 1% reference accuracy of the ICL7663SA eliminates the need for trimming the output voltage in most applications.

The ICL7663S is well suited for battery powered supplies, featuring 4 μA quiescent current, low V_{IN} to V_{OUT} differential, output current sensing and logic input level shutdown control. In addition, the ICL7663S has a negative temperature coefficient output suitable for generating a temperature compensated display drive voltage for LCD displays.

The ICL7663S is available in either an 8-pin plastic, CERDIP, or SOIC package.

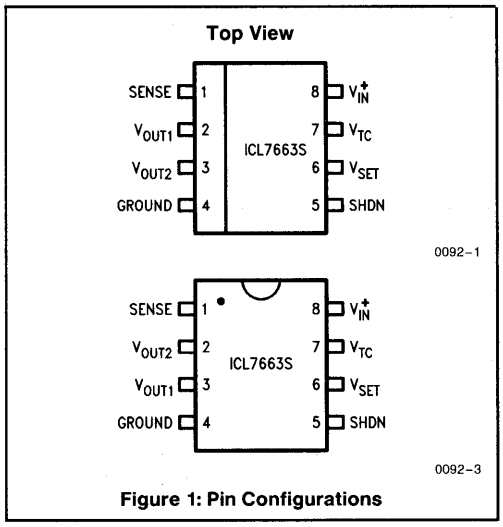


Figure 1: Pin Configurations

FEATURES

- ***Guaranteed*** **10 μA Maximum Quiescent Current over *All* Temperature Ranges**
- ***Wider*** **Operating Voltage Range—1.6V to 16V**
- ***Guaranteed*** **Line and Load Regulation over *Entire* Operating Temperature Range *Optional***
- **1% Output Voltage Accuracy (ICL7663SA)**
- **Output Voltage Programmable from 1.3V to 16V**
- ***Improved*** **Temperature Coefficient of Output Voltage**
- **40 mA Minimum Output Current with Current Limiting**
- **Output Voltages with Programmable Negative Temperature Coefficients**
- **Output Shutdown via Current-Limit Sensing or External Logic Level**
- **Low Input-to-Output Voltage Differential**
- **Improved Direct Replacement for Industry Standard ICL7663B and Other Second-Source Products**

APPLICATIONS

- **Low-Power Portable Instrumentation**
- **Pagers**
- **Handheld Instruments**
- **LCD Display Modules**
- **Remote Data Loggers**
- **Battery-Powered Systems**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7663SCBA	0°C to +70°C	8 Lead SOIC
ICL7663SCPA		8 Lead Minidip
ICL7663SCJA		8 Lead CERDIP
ICL7663SACPA		8 Lead Minidip
ICL7663SACJA		8 Lead CERDIP
ICL7663SIBA	−25°C to +85°C	8 Lead SOIC
ICL7663SIPA		8 Lead Minidip
ICL7663SIJA		8 Lead CERDIP
ICL7663SAIPA		8 Lead Minidip
ICL7663SAIJA		8 Lead CERDIP

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage ..... +18V
Any Input or Output Voltage (Note 1)
(Terminals 1, 2, 3, 5, 6, 7) ..... (V_{IN} + 0.3) to (GND − 0.3)V
Output Source Current
(Terminal 2) ..... 50 mA
(Terminal 3) ..... 25 mA
Output Sinking Current
(Terminal 7) ..... −10 mA
Lead Temperature (Soldering, 10 sec.) ..... 300°C
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
ICL7663SC ..... 0°C to +70°C
ICL7663SI ..... −25°C to +85°C
Total Power Dissipation (Note 2)
SOIC ..... 200 mW
Minidip ..... 200 mW
CERDIP ..... 500 mW

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

Specifications below applicable to both ICL7663S and ICL7663SA unless otherwise stated. V^+_{IN} = 9V, V_{OUT} = 5V, T_A = 25°C, unless otherwise stated. See Test Circuit, Figure 3.

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V^+_{IN}	***Input Voltage***	***ICL7663S***				
		T_A = 25°C	1.5		***16***	V
		0°C < T_A < +70°C	1.6		***16***	V
		−25°C < T_A < +85°C	1.6		***16***	
		ICL7663SA				
		0°C < T_A < +70°C	***1.6***		***16***	V
		−25°C < T_A < +85°C	***1.6***		***16***	
I_Q	***Quiescent Current***	1.4V ≤ V_{OUT} ≤ 8.5V, No Load				
		V^+_{IN} = 9V, 0°C < T_A < 70°C			***10***	µA
		−25°C < T_A < +85°C			***10***	
		V^+_{IN} = 16V, 0°C < T_A < +70°C			***12***	µA
		−25°C < T_A < +85°C			***12***	
V_{SET}	***Reference Voltage***	I_{OUT1} = 100 µA, V_{OUT} = V_{SET}				
		ICL7663S T_A = 25°C	1.2	1.3	1.4	V
		ICL7663SA T_A = 25°C	***1.275***	***1.29***	***1.305***	V
$\frac{\Delta V_{SET}}{\Delta T}$	***Temperature Coefficient***	0°C < T_A < +70°C		***100***		ppm
		−25°C < T_A < +85°C		***100***		ppm
$\frac{\Delta V_{SET}}{V_{SET}, \Delta V_{IN}}$	***Line Regulation***	2V < V_{IN} < 15V				
		0°C < T_A < +70°C		0.03	***0.03***	%/V
		−25°C < T_A < +85°C		0.03	***0.3***	%/V
I_{SET}	***V_{SET} Input Current***	0°C < T_A < +70°C		0.01	***10***	nA
		−25°C < T_A < +85°C		0.01	***10***	nA

NOTE: 1. Connecting any terminal to voltages greater than (V^+_{IN} + 0.3V) or less than (GND − 0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663S power-up.

2. Derate linearly above 50°C at 5 mW/°C for Plastic Minidip, 7.5 mW/°C for TO-99 can, and 10 mW/°C for CERDIP.

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

Specifications below applicable to both ICL7663S and ICL7663SA unless otherwise stated. V^+_{IN} = 9V, V_{OUT} = 5V, T_A = 25°C, unless otherwise stated. See Test Circuit, Figure 3.

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
I_{SHDN}	Shutdown Input Current			±0.01	10	nA
V_{SHDN}	Shutdown Input Voltage	V_{SHDN} HI: Both V_{OUT} Disabled V_{SHDN} LO: Both V_{OUT} Enable	1.4		 0.3	V V
I_{SENSE}	Sense Pin Input Current			0.01	10	nA
V_{CL}	Sense Pin Input Threshold			0.5		V
R_{SAT}	***Input-Output Saturation Resistance (Note 3)***	V^+_{IN} = 2V, I_{OUT1} = 1 mA V^+_{IN} = 9V, I_{OUT1} = 2 mA V^+_{IN} = 15V, I_{OUT1} = 5 mA		***170*** ***50*** ***35***	***350*** ***100*** ***70***	Ω Ω Ω
$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	***Load Regulation***	1 mA < I_{OUT2} < 20 mA 50 µA < I_{OUT1} < 5 mA		1 2	***3*** ***10***	Ω Ω
I_{OUT2}	***Available Output Current (V_{OUT2})***	3V ≤ V_{IN} ≤ 16V, V_{IN} − V_{OUT2} = 1.5V	***40***			mA
V_{TC}	Negative Tempco Output (Note 4)	Open-Circuit Voltage		0.9		V
I_{TC}		Maximum Sink Current	0	8	2.0	mA
$\frac{\Delta V_{TC}}{\Delta T}$	Temperature Coefficient	Open Circuit		+2.5		mV/°C
$I_{L(MIN)}$	Minimum Load Current	(Includes V_{SET} Divider) T_A = 25°C 0°C < T_A < +70°C −25°C < T_A < +85°C		 0.2 0.2	***1.0*** ***5.0*** ***5.0***	µA µA µA

NOTE: 3. This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5 mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.

4. This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET}, a negative coefficient results in the output voltage. See Figure 5 for details. Pin will not source current.

5. All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V.

6. All significant improvements over the industry standard ICL7663 are highlighted in ***bold italics***.

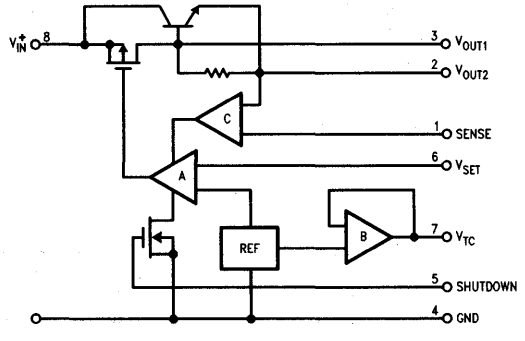
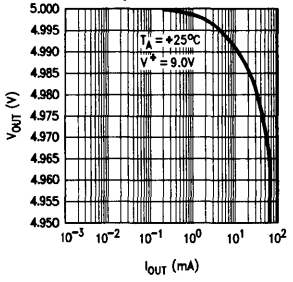


Figure 2: ICL76635 Functional Diagram

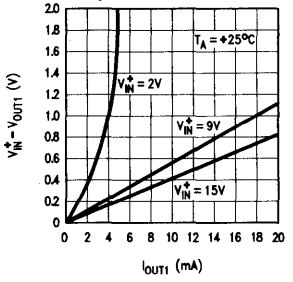
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

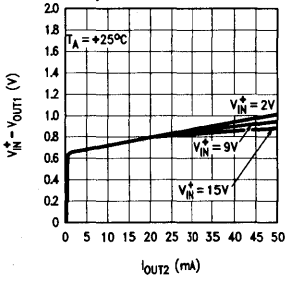
V_{OUT2} Output Voltage as a Function of Output Current



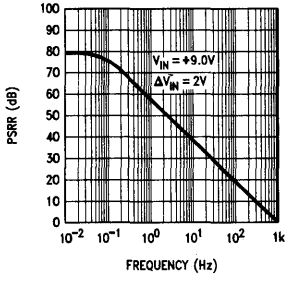
V_{OUT1} Input-Output Differential vs Output Current



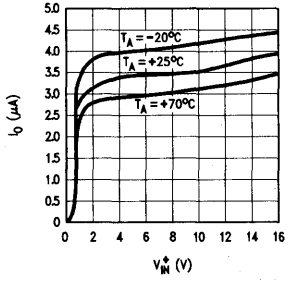
V_{OUT2} Input-Output Differential vs Output Current



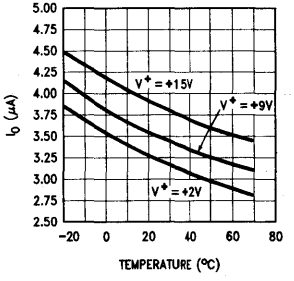
Input Power Supply Rejection Ratio



Quiescent Current as a Function of Input Voltage



Quiescent Current as a Function of Temperature



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DETAILED DESCRIPTION

The ICL7663S is a CMOS integrated circuit incorporating all the functions of a voltage regulator plus protection circuitry on a single monolithic chip. Referring to the functional diagram (Figure 2), the main blocks are a bandgap-type voltage reference, an error amplifier, and an output driver with both PMOS and NPN pass transistors.

The bandgap output voltage, trimmed to 1.29V ± 15 mV for the ICL7663SA, and the input voltage at the V_{SET} terminal are compared in amplifier A. Error amplifier A drives a P-channel pass transistor which is sufficient for low (under about 5 mA) currents. The high current output is passed by an NPN bipolar transistor connected as a follower. This configuration gives more gain and lower output impedance.

Logic-controlled shutdown is implemented via a N-channel MOS transistor. Current-sensing is achieved with comparator C, which functions with the V_{OUT2} terminal. The ICL7663S has an output (V_{TC}) from a buffer amplifier (B), which can be used in combination with amplifier A to generate programmable-temperature-coefficient output voltages.

The amplifier, reference and comparator circuitry all operate at bias levels well below 1 μA to achieve extremely low quiescent current. This does limit the dynamic response of the circuits, however, and transients are best dealt with outside the regulator loop.

BASIC OPERATION

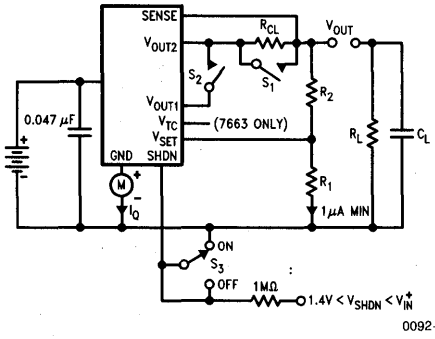
The ICL7663S is designed to regulate battery voltages in the 5V to 15V region at maximum load currents of about 5 mA to 30 mA. Although intended as low power devices, power dissipation limits must be observed. For example, the power dissipation in the case of a 10V supply regulated down to 2V with a load current of 30 mA clearly exceeds the power dissipation rating of the Minidip:

$$(10 - 2)\,(30)\,(10^{-3}) = 240\,\text{mW}$$

The circuit of Figure 4 illustrates proper use of the device.

CMOS devices generally require two precautions: every input pin must go somewhere, and maximum values of applied voltages and current limits must be rigorously observed. Neglecting these precautions may lead to, at the least, incorrect or nonoperation, and at worst, destructive device failure. To avoid the problem of latchup, do not apply inputs to any pins before supply voltage is applied.

NOTE: All typical values have been characterized but are not tested.



NOTE: 1. S_1 when closed disables output current limiting.

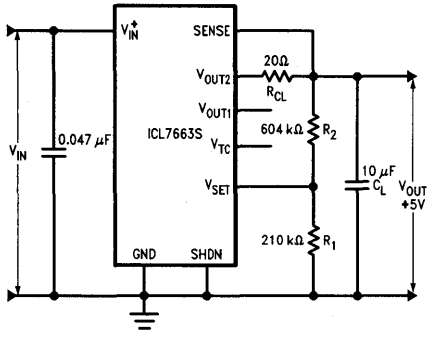
2: Close S_2 for V_{OUT1}, open S_2 for V_{OUT2}.

3: $V_{OUT} = \frac{R_2 + R_1}{R_1} V_{SET}$.

4: I_Q quiescent current is measured at GND pin by meter M.

5: S_3 when ON, permits normal operation, when OFF, shuts down both V_{OUT1} and V_{OUT2}.

Figure 3: ICL7663S Test Circuit



$$V_{OUT} = \frac{R_2 + R_1}{R_1} V_{SET} = 5V$$

$$I_{CL} = \frac{V_{CL}}{R_{CL}} = 25\ mA$$

Figure 4: Positive Regulator with Current Limit

Input Voltages—The ICL7663S accepts working inputs of 1.5V to 16V. When power is applied, the rate-of-rise of the input may be hundreds of volts per microsecond. This is potentially harmful to the regulators, where internal operating currents are in the nanoampere range. The 0.047 μF capacitor on the device side of the switch will limit inputs to a safe level around 2 V/μs. Use of this capacitor is suggested in all applications. In severe rate-of-rise cases, it may be advisable to use an RC network on the SHutDowN pin to delay output turn-on. Battery charging surges, transients, and assorted noise signals should be kept from the regulators by RC filtering, zener protection, or even fusing.

Output Voltages—The resistor divider R_2/R_1 is used to scale the reference voltage, V_{SET}, to the desired output using the formula $V_{OUT} = (1 + R_2/R_1)\ V_{SET}$. Suitable arrangements of these resistors, using a potentiometer, enables exact values for V_{OUT} to be obtained. In most applications the potentiometer may be eliminated by using the ICL7663SA. The ICL7663SA has V_{SET} voltage guaranteed to be 1.29V ±15 mV and when used with ±1% tolerance resistors for R_1 and R_2 the initial output voltage will be within ±2.7% of ideal.

The low leakage current of the V_{SET} terminal allows R_1 and R_2 to be tens of megohms for minimum additional quiescent drain current. However, some load current is required for proper operation, so for extremely low-drain applications it is necessary to draw at least 1 μA. This can include the current for R_2 and R_1.

Output voltages up to nearly the V_{IN} supply may be obtained at low load currents, while the low limit is the reference voltage. The minimum input-output differential in each regulator is obtained using the V_{OUT1} terminal. The input-output differential increases to 1.5V when using V_{OUT2}.

Output Currents—Low output currents of less than 5 mA are obtained with the least input-output differential from the V_{OUT1} terminal (connect V_{OUT2} to V_{OUT1}). Where higher currents are needed, use V_{OUT2} (V_{OUT1} should be left open in this case).

High output currents can be obtained only as far as package dissipation allows. It is strongly recommended that output current-limit sensing be used in such cases.

Current-Limit Sensing—The on-chip comparator (C in Figure 2) permits shutdown of the regulator output in the event of excessive current drain. As Figure 4 shows, a current-limiting resistor, R_{CL}, is placed in series with V_{OUT2} and the SENSE terminal is connected to the load side of R_{CL}. When the current through R_{CL} is high enough to produce a voltage drop equal to V_{CL} (0.5V) the voltage feedback is bypassed and the regulator output will be limited to this current. Therefore, when the maximum load current (I_{LOAD}) is determined, simply divide V_{CL} by I_{LOAD} to obtain the value for R_{CL}.

Logic-Controllable Shutdown—When equipment is not needed continuously (e.g., in remote data-acquisition systems), it is desirable to eliminate its drain on the system until it is required. This usually means switches, with their unreliable contacts. Instead, the ICL7663S can be shut down by a logic signal, leaving only I_Q (under 4 μA) as a drain on the power source. Since this pin must not be left open, it should be tied to ground if not needed. A voltage of less than 0.3V for the ICL7663S will keep the regulator ON, and a voltage level of more than 1.4V but less than V^+_{IN} will turn the outputs OFF. If there is a possibility that the control signal could exceed the regulator input (V^+_{IN}) the current from this signal should be limited to 100 μA maximum by a high-value (1 MΩ) series resistor. This situation may occur when the logic signal originates from a system powered separately from that of the regulator.

NOTE: All typical values have been characterized but are not tested.

Additional Circuit Precautions—This regulator has poor rejection of voltage fluctuations from AC sources above 10 Hz or so. To prevent the output from responding (where this might be a problem), a reservoir capacitor across the load is advised. The value of this capacitor is chosen so that the regulated output voltage reaches 90% of its final value in 20 ms. From

$$I = C\frac{\Delta V}{\Delta t}, C = I_{OUT}\frac{(20 \times 10^{-3})}{0.9\,V_{OUT}} = 0.022\frac{I_{OUT}}{V_{OUT}}$$

In addition, where such a capacitor is used, a current-limiting resistor is also suggested (see "Current-Limit Sensing").

Producing Output Voltages with Negative Temperature Coefficients—The ICL7663S has an additional output which is 0.9V relative to GND and has a tempco of +2.5 mV/°C. By applying this voltage to the inverting input of amplifier A (i.e., the V_{SET} pin), output voltages having negative TC may be produced. The TC of the output voltage is controlled by the R_2/R_3 ratio (see Figure 5 and its design equations).

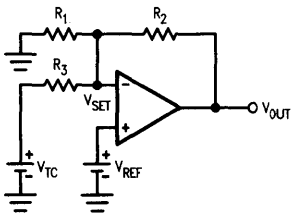
APPLICATIONS

Boosting Output Current with External Transistor

The maximum available output current from the ICL7663S is 40 mA. To obtain output currents greater than 40 mA, an external NPN transistor is used connected as shown in Figure 6.

Generating a Temperature Compensated Display Drive Voltage

Temperature has an important effect in the variation of threshold voltage in multiplexed LCD displays. As temperature rises, the threshold voltage goes down. For applications where the display temperature varies widely, a temperature compensated display voltage, V_{DISP}, can be generated using the ICL7663S. This is shown in Figure 7 for the ICM7233 triplexed LCD display driver.



EQ. 1: $V_{OUT} = V_{SET}\left(1 + \frac{R_2}{R_1}\right) + \frac{R_2}{R_3}(V_{SET} - V_{TC})$

EQ. 2: $TC\,V_{OUT} = -\frac{R_2}{R_3}(TC\,V_{TC})$ in mV/°C

Where: V_{SET} = 1.3V
V_{TC} = 0.9V
TCV_{TC} = +2.5 mV/°C

Figure 5. Generating Negative Temperature Coefficients

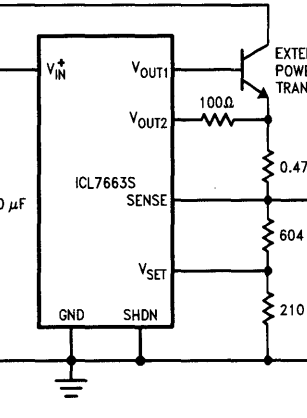


Figure 6: Boosting Output Current with External Transistor

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

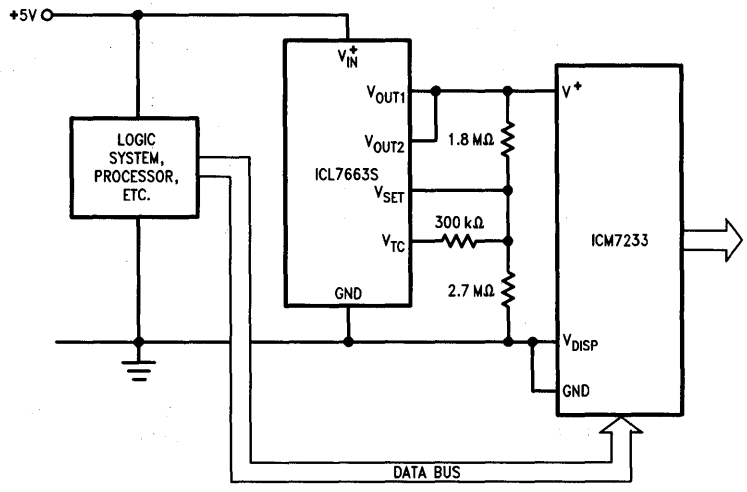


Figure 7: Generating a Multiplexed LCD Display Drive Voltage

NOTE: All typical values have been characterized but are not tested.

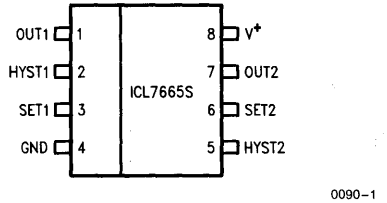
HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICL7665S
CMOS Micropower Over/Under Voltage Detector

GENERAL DESCRIPTION

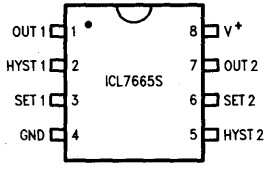
The ICL7665S Super CMOS Micropower Over/Under Voltage Detector contains two low power, individually programmable voltage detectors on a single CMOS chip. Requiring typically 3 μA for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction. The trip points and hysteresis of the two voltage detectors are individually programmed via external resistors. An internal bandgap-type reference provides an accurate threshold voltage while operating from any supply in the 1.6V to 16V range.

The Harris ICL7665S, Super Programmable Over/Under Voltage Detector is a direct replacment for the industry standard ICL7665B offering ***wider*** operating voltage and temperature ranges, ***improved*** threshold accuracy (ICL7665SA), and temperature coefficient, and ***guaranteed*** maximum supply current. All improvements are highlighted in bold italics in the electrical characteristics section. ***All critical parameters are guaranteed over the entire commercial and industrial temperature ranges.***



0090-1

Outline dwg (BA)



0090-3

Outline dwg (PA)

Figure 1: Pin Configurations

FEATURES

- **Guaranteed 10 μA Maximum Quiescent Current over Temperature**
- **Guaranteed Wider Operating Voltage Range over Entire Operating Temperature Range**
- **2% Threshold Accuracy (ICL7665SA)**
- **Dual Comparator with Precision Internal Reference**
- **100 ppm/°C Temperature Coefficient of Threshold Voltage**
- ***Improved* Direct Replacement for Industry-Standard ICL7665B and Other Second-Source Devices**
- **Up to 20 mA Output Current Sinking Ability**
- **Individually Programmable Upper and Lower Trip Voltages and Hysteresis Levels**

APPLICATIONS

- **Pocket Pagers**
- **Portable Instrumentation**
- **Charging Systems**
- **Memory Power Back-Up**
- **Battery-Operated Systems**
- **Portable Computers**
- **Level Detectors**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7665SCBA	0°C to +70°C	8 Lead SOIC
ICL7665SCPA	0°C to +70°C	8 Lead Minidip
ICL7665SCJA	0°C to +70°C	8 Lead CERDIP
ICL7665SACPA	0°C to +70°C	8 Lead Minidip
ICL7665SACJA	0°C to +70°C	8 Lead CERDIP
ICL7665SIBA	-25°C to +85°C	8 Lead SOIC
ICL7665SIPA	-25°C to +85°C	8 Lead Minidip
ICL7665SIJA	-25°C to +85°C	8 Lead CERDIP
ICL7665SAIPA	-25°C to +85°C	8 lead Minidip
ICL7665SAIJA	-25°C to +85°C	8 Lead CERDIP

302167-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 2) ..... −0.3V to +18V
Output Voltages OUT1 and OUT2 (with respect to GND) (Note 2) ..... −0.3V to +18V
Output Voltages HYST1 and HYST2 (with respect to V+) (Note 2) ..... −0.3V to +18V
Input Voltages SET1 and SET2 (Note 2) ..... (GND − 0.3V) to (V+ + 0.3V)
Maximum Sink Output OUT1 and OUT2 ..... 25 mA
Maximum Source Output Current HYST1 and HYST2 ..... −25 mA

Lead Temperature (Soldering, 10 sec) ..... +300°C
Storage Temperature Range ..... −65°C to 150°C
Operating Temperature Range
ICL7665SC ..... 0°C to +70°C
ICL7665SI ..... −25°C to +85°C
Total Power Dissipation (Note 1)
SOIC ..... 200 mW
Minidip ..... 200 mW
CERDIP ..... 500 mW

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

The specifications below are applicable to both the ICL7665S and ICL7665SA unless otherwise stated. $V^+ = 5V$, $T_A = +25°C$, Test Circuit Figure 3 unless otherwise stated.

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V^+	***Operating Supply Voltage***	ICL7665S				
		$T_A = 25°C$	1.6		16	V
		$0°C \le T_A \le +70°C$	1.8		16	V
		$-25°C \le T_A \le +85°C$	1.8		16	V
		ICL7665SA				
		$0°C \le T_A \le +70°C$	***1.8***		16	V
		$-25°C \le T_A \le +85°C$	***1.8***		16	V
I^+	***Supply Current***	$GND \le V_{SET1}, V_{SET2} \le V^+$				
		All Outputs Open Circuit				
		$0°C \le T_A \le +70°C$				V
		$V^+ = 2V$		2.5	10	μA
		$V^+ = 9V$		2.6	10	μA
		$V^+ = 15V$		2.9	***10***	μA
		$-25°C \le T_A \le +85°C$				
		$V^+ = 2V$		2.5	***10***	μA
		$V^+ = 9V$		2.6	***10***	μA
		$V^+ = 15V$		***2.9***	***10***	μA
	Input Trip Voltage	ICL7665S				
V_{SET1}			1.15	1.3	1.45	V
V_{SET2}			1.2	1.3	1.4	V
		ICL7665SA				
V_{SET1}			***1.275***	***1.30***	***1.325***	V
V_{SET2}			***1.225***	***1.30***	***1.375***	V
$\frac{\Delta V_{SET}}{\Delta T}$	***Temperature Coefficient of V_{SET}***	ICL7665S		***200***		ppm
		ICL7665SA		***100***		ppm
$\frac{\Delta V_{SET}}{\Delta V_S}$	Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{2HYST2} = 1\ M\Omega$ $2V \le V^+ \le 10V$		0.03		%/V
I_{OLK}	Output Leakage Currents of OUT and HYST	$V_{SET} = 0V$ or $V_{SET} \ge 2V$		10	200	nA
I_{HLK}				−10	−100	nA
I_{OLK}		$V^+ = 15V, T_A = 70°C$			2000	nA
I_{HLK}					−500	
	Output Saturation Voltages	$V_{SET1} = 2V, I_{OUT1} = 2\ mA$				
V_{OUT1}		$V^+ = 2V$		0.2	0.5	V
V_{OUT1}		$V^+ = 5V$		0.1	0.3	V
V_{OUT1}		$V^+ = 15V$		0.06	0.2	V

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

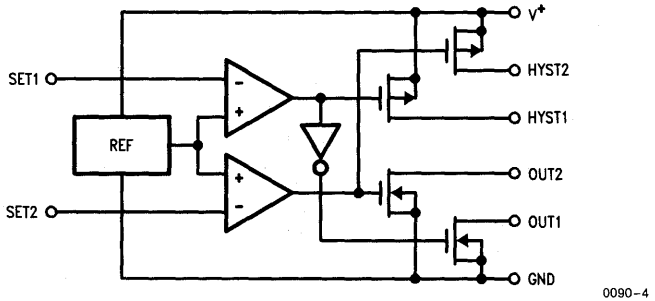
The specifications below are applicable to both the ICL7665S and ICL7665SA unless otherwise stated. $V^+ = 5V$, $T_A = +25°C$, Test Circuit Figure 3 unless otherwise stated. (Continued)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
	Output Saturation Voltages	$V_{SET1} = 2V$, $I_{HYST1} = -0.5$ mA				
V_{HYST1}		$V^+ = 2V$		−0.15	−0.30	V
V_{HYST1}		$V^+ = 5V$		−0.05	−0.15	V
V_{HYST1}		$V^+ = 15V$		−0.02	−0.10	V
	Output Saturation Voltages	$V_{SET2} = 0V$, $I_{OUT2} = 2$ mA				
V_{OUT2}		$V^+ = 2V$		0.2	0.5	V
V_{OUT2}		$V^+ = 5V$		0.15	0.3	V
V_{OUT2}		$V^+ = 15V$		0.11	0.25	V
	Output Saturation Voltages	$V_{SET2} = 2V$				
V_{HYST2}		$V^+ = 2V$, $I_{HYST2} = -0.2$ mA		−0.25	−0.8	
V_{HYST2}		$V^+ = 5V$, $I_{HYST2} = -0.5$ mA		−0.43	−1.0	
		$V^+ = 15V$, $I_{HYST2} = -0.5$ mA		−0.35	−0.8	V
I_{SET}	V_{SET} Input Leakage Current	$GND \le V_{SET} \le V^+$		0.01	10	nA
ΔV_{SET}	***Δ Input for Complete Output Change***	$R_{OUT} = 4.7$ kΩ, $R_{HYST} = 20$ kΩ				
		$V_{OUT}LO = 1\% V^+$, $V_{OUT}HI = 99\% V^+$				
		ICL7665S		1.0		mV
		ICL7665SA		0.1		mV
$V_{SET1}-V_{SET2}$	Difference in Trip Voltages	R_{OUT}, $R_{HYST} = 1$ MΩ		±5	±50	mV
	Output/Hysteresis Difference	R_{OUT}, $R_{HYST} = 1$ MΩ				
		ICL7665S		±1		mV
		ICL7665SA		***±0.1***		mV

NOTE 1: Derate above +25°C ambient temperature at 4 mW/°C.

2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than ($V^+ + 0.3V$) or less than (GND − 0.3V) may cause destructive device latchup. For these reasons, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665S be turned on first. If this is not possible, currents into inputs and/or outputs must be limited to ±0.5 mA and voltages must not exceed those defined above.

3: All significant improvements over the industry-standard ICL7665 are highlighted in bold italics.



CONDITIONS*

$V_{SET1} > 1.3V$, OUT1 switch ON	HYST1 switch ON
$V_{SET1} < 1.3V$, OUT1 switch OFF	HYST1 switch OFF
$V_{SET2} > 1.3V$, OUT2 switch OFF	HYST2 switch ON
$V_{SET2} < 1.3V$, OUT2 switch ON	HYST2 switch OFF

*See Operating Characteristics for exact thresholds.

Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

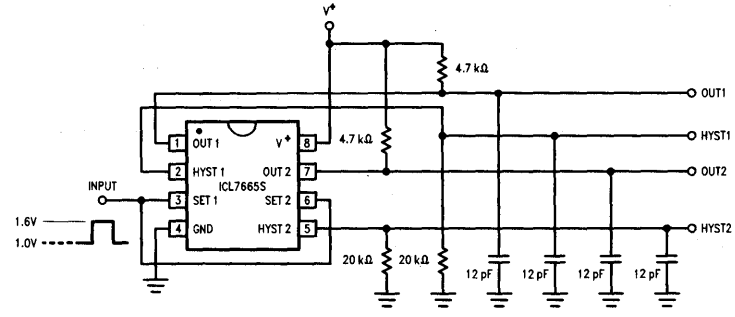


Figure 3: Test Circuits

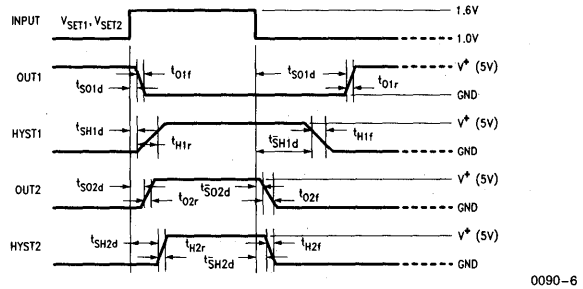


Figure 4: Switching Waveforms

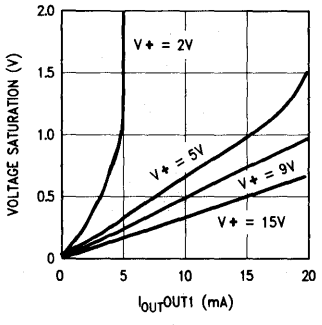
A.C. ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
t_{SO1d} t_{SH1d} t_{SO2d} t_{SH2d}	Output Delay Times Input Going HI	V_{SET} Switched between 1.0V to 1.6V R_{OUT} = 4.7 kΩ, C_L = 12 pF R_{HYST} = 20 kΩ, C_L = 12 pF		85 90 55 55		µs
t_{SO1d} t_{SH1d} t_{SO2d} t_{SH2d}	Input Going LO	V_{SET} Switched between 1.6V to 1.0V R_{OUT} = 4.7 kΩ, C_L = 12 pF R_{HYST} = 20 kΩ, C_L = 12 pF		75 80 60 60		µs
t_{O1r} t_{O2r} t_{H1r} t_{H2r}	Output Rise Times	V_{SET} Switched between 1.0V to 1.6V R_{OUT} = 4.7 kΩ, C_L = 12 pF R_{HYST} = 20 kΩ, C_L = 12 pF		0.6 0.8 7.5 0.7		µs
t_{O1f} t_{O2f} t_{H1f} t_{H2f}	Output Fall Times	V_{SET} Switched between 1.0V to 1.6V R_{OUT} = 4.7 kΩ, C_L = 12 pF R_{HYST} = 20 kΩ, C_L = 12 pF		0.6 0.7 4 1.8		µs

NOTE: All typical values have been characterized but are not tested.

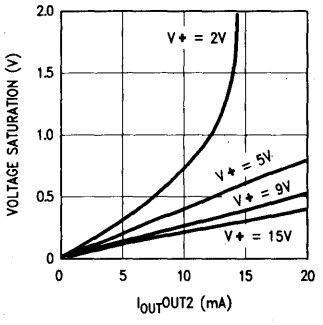
Typical Performance Characteristics

OUT1 Saturation Voltage as a Function of Output Current



0090-7

OUT2 Saturation Voltage as a Function of Output Current



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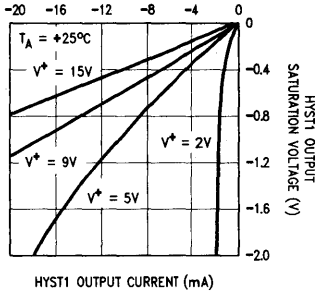
HYST1 Output Saturation Voltage vs HYST1 Output Current



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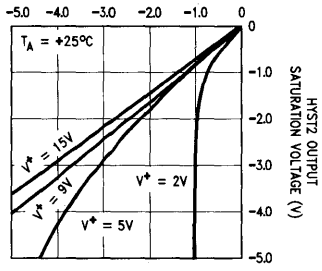
HYST2 Output Saturation Voltage vs HYST2 Output Current



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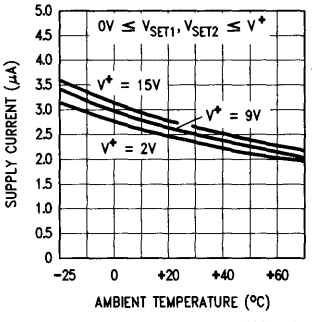
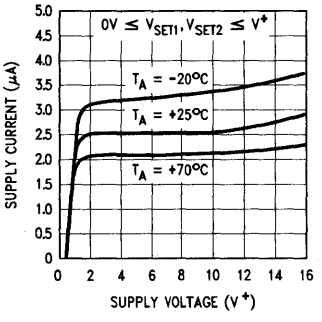
Supply Current as a Function of Ambient Temperature



0090-11

Supply Current as a Function of Supply Voltage



0090-12

DETAILED DESCRIPTION

As shown in the Functional Diagram, Figure 2, the ICL7665S consists of two comparators which compare input voltages on the SET1 and SET2 terminals to an internal 1.3V band-gap reference. The outputs from the two comparators drive open-drain N-channel transistors for OUT1 and OUT2, and open-drain P-channel transistors for HYST1 and HYST2 outputs. Each section, the Under-Voltage Detector and the Over-Voltage Detector, is independent of the other, although both use the internal 1.3V reference. The offset voltages of the two comparators will normally be unequal so V_{SET1} will generally not quite equal V_{SET2}.

The input impedances of the SET1 and SET2 pins are extremely high, and for most practical applications can be ignored. The four outputs are open-drain MOS transistors, and when ON behave as low resistance switches to their respective supply rails. This minimizes errors in setting-up the hysteresis, and maximizes the output flexibility. The operating currents of the bandgap reference and the comparators are around 100 nA each.

PRECAUTIONS

Junction-isolated CMOS devices like the ICL7665S have an inherent SCR or 4-layer PNPN structure distributed throughout the die. Under certain circumstances, this can be triggered into a potentially destructive high-current mode. This latchup can be triggered by forward-biasing an input or output with respect to the power supply, or by applying excessive supply voltages. In very-low current analog circuits, such as the ICL7665S, this SCR can also be triggered by applying the input power supply extremely rapidly ("instantaneously"), e.g. through a low impedance battery and an ON/OFF switch with short lead lengths. The rate-of-rise of the supply voltage can exceed 100 V/μs in such a circuit. A low-impedance capacitor (e.g., 0.05 μF disc ceramic) between the V^+ and GrouND pins of the ICL7665S can be used to reduce the rate-of-rise of the supply voltage in battery applications. In line-operated systems, the rate-of-rise of the supply is limited by other considerations, and is normally not a problem.

NOTE: All typical values have been characterized but are not tested.

If the SET voltages must be applied before the supply voltage V^+, the input current should be limited to less than 0.5 mA by appropriate external resistors, usually required for voltage setting anyway. A similar precaution should be taken with the outputs if it is likely that they will be driven by other circuits to levels outside the supplies at any time. See M011 for some other protection ideas.

SIMPLE THRESHOLD DETECTOR

Figure 5 shows the simplest connection of the ICL7665S for threshold detection. From the graph (b), it can be seen that at low input voltages OUT1 is OFF, or high, while OUT2 is ON, or low. As the input rises (e.g., at power-on) toward V_{NOM} (usually the eventual operating voltage), OUT2 goes high on reaching V_{TR2}. If the voltage rises above V_{NOM} as much as V_{TR1}, OUT1 goes low. The equations giving V_{SET1} and V_{SET2} are from Figure 5(a):

$$V_{SET1} = V_{IN}\frac{R_{11}}{(R_{11}+R_{21})};\ V_{SET2} = V_{IN}\frac{R_{12}}{(R_{12}+R_{22})}$$

Since the voltage to trip each comparator is nominally 1.3V, the value V_{IN} for each trip point can be found from

$$V_{TR1} = V_{SET1}\frac{(R_{11}+R_{21})}{R_{11}} = 1.3\frac{(R_{11}+R_{21})}{R_{11}} \text{ for detector 1}$$

and

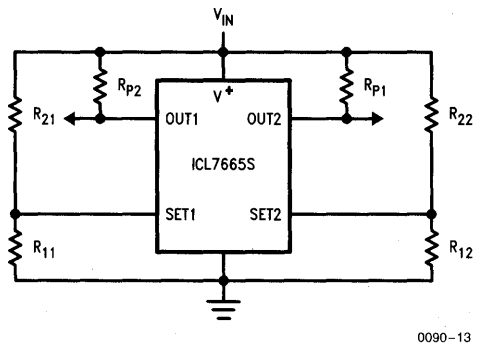
$$V_{TR2} = V_{SET2}\frac{(R_{12}+R_{22})}{R_{12}} = 1.3\frac{(R_{12}+R_{22})}{R_{12}} \text{ for detector 2}$$

Either detector may be used alone, as well as both together, in any of the circuits shown here.

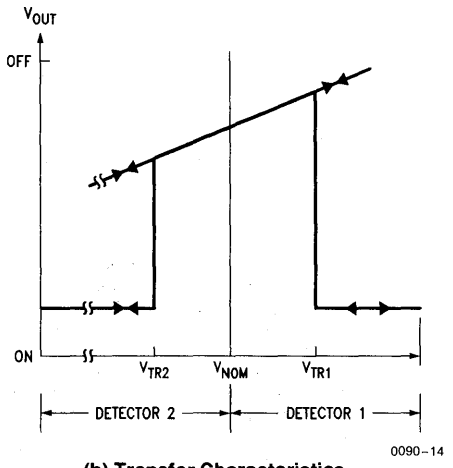
When V_{IN} is very close to one of the trip voltages, normal variations and noise may cause it to wander back and forth across this level, leading to erratic output ON and OFF conditions. The addition of hysteresis, making the trip points slightly different for rising and falling inputs, will avoid this condition.

THRESHOLD DETECTOR WITH HYSTERESIS

Figure 6(a) shows how to set up such hysteresis, while Figure 6(b) shows how the hysteresis around each trip point produces switching action at different points depending on whether V_{IN} is rising or falling (the arrows indicate direction of change). The HYST outputs are basically switches which short out R_{31} or R_{32} when V_{IN} is above the respective trip point. Thus if the input voltage rises from a low value, the trip point will be controlled by R_{1n}, R_{2n}, and R_{3n}, until the trip point is reached. As this value is passed, the detector changes state, R_{3n} is shorted out, and the trip point becomes controlled by only R_{1n} and R_{2n}, a lower value. The input will then have to fall to this new point to restore the



(a) Circuit Configuration

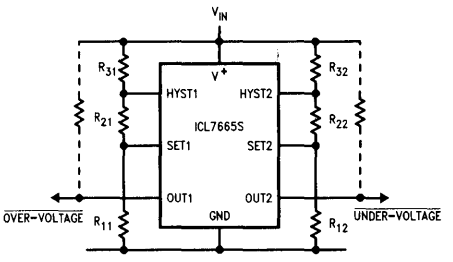


(b) Transfer Characteristics

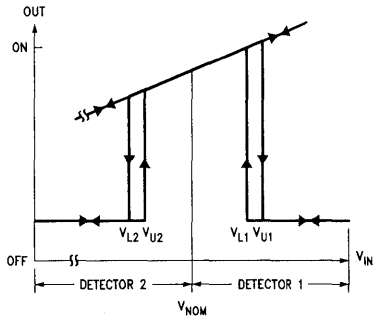
Figure 5: Simple Threshold Detector

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS



(a) Circuit Configuration



(b) Transfer Characteristics

Figure 6: Threshold Detector with Hysteresis

Table 1: Set-Point Equations

a) NO HYSTERESIS

$$\text{Over-Voltage } V_{TRIP} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$

$$\text{Over-Voltage } V_{TRIP} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$

b) HYSTERESIS PER FIGURE 6A

$$V_{U1} = \frac{R_{11} + R_{21} + R_{31}}{R_{11}} \times V_{SET1}$$

Over-Voltage V_{TRIP}

$$V_{L1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$

$$V_{U2} = \frac{R_{12} + R_{22} + R_{32}}{R_{12}} \times V_{SET2}$$

Under-Voltage V_{TRIP}

$$V_{L2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$

c) HYSTERESIS PER FIGURE 7

$$V_{U1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$$

Over-Voltage V_{TRIP}

$$V_{L1} = \frac{R_{11} + \dfrac{R_{21}R_{31}}{R_{21} + R_{31}}}{R_{11}} \times V_{SET1}$$

$$V_{U2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$$

Over-Voltage V_{TRIP}

$$V_{L2} = \frac{R_{12} + \dfrac{R_{22}R_{32}}{R_{22} + R_{32}}}{R_{12}} \times V_{SET2}$$

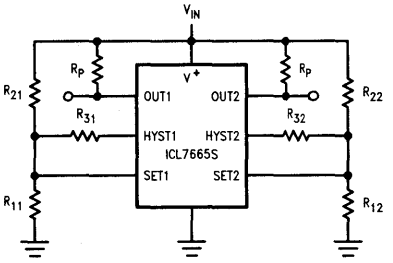


Figure 7: An Alternative Hysteresis Circuit

NOTE: All typical values have been characterized but are not tested.

THRESHOLD DETECTOR WITH HYSTERESIS (Continued)

initial comparator state, but as soon as this occurs, the trip point will be raised again.

An alternative circuit for obtaining hysteresis is shown in Figure 7. In this configuration, the HYST pins put the extra resistor in parallel with the upper setting resistor. The values of the resistors differ, but the action is essentially the same. The governing equations are given in Table 1. These ignore the effects of the resistance of the HYST outputs, but these can normally be neglected if the resistor values are above about 100 kΩ.

APPLICATIONS

Single Supply Fault Monitor

Figure 8 shows an over/under-voltage fault monitor for a single supply. The over-voltage trip point is centered around 5.5V and the under-voltage trip point is centered around 4.5V. Both have some hysteresis to prevent erratic output ON and OFF conditions. The two outputs are connected in a wired OR configuration with a pullup resistor to generate a power OK signal.

Multiple Supply Fault Monitor

The ICL7665S can simultaneously monitor several supplies when connected as shown in Figure 9. The resistors are chosen such that the sum of the currents through R_{21A}, R_{21B}, and R_{31} is equal to the current through R_{11} when the two input voltages are at the desired low voltage detection point. The current through R_{11} at this point is equal to 1.3 V/R_{11}. The voltage at the V_{SET} input depends on the voltage of both supplies being monitored. The trip voltage of one supply while the other supply is at the nominal voltage will be different than the trip voltage when both supplies are below their nominal voltages.

The other side of the ICL7665S can be used to detect the absence of negative supplies. The trip points for OUT1 depend on both the negative supply voltages and the actual voltage of the +5V supply.

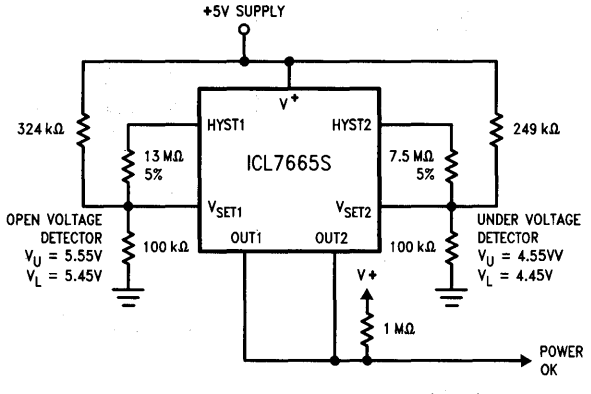


Figure 8: Fault Monitor for a Single Supply

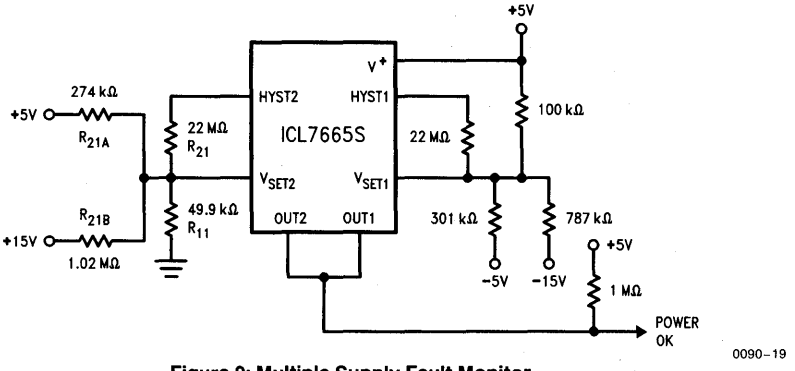


Figure 9: Multiple Supply Fault Monitor

NOTE: All typical values have been characterized but are not tested.

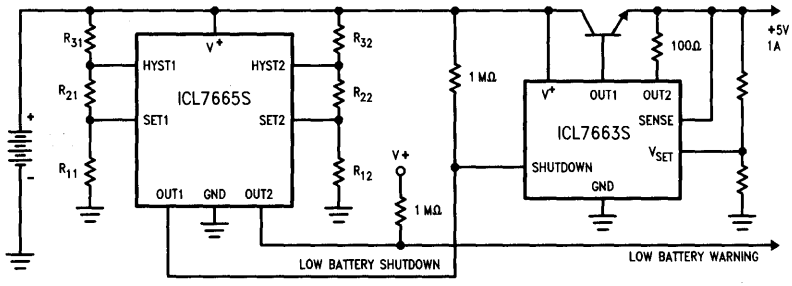


Figure 10: Low Battery Warning and Low Battery Disconnect

Combination Low Battery Warning and Low Battery Disconnect

When using rechargeable batteries in a system, it is important to keep the batteries from being overdischarged. The circuit shown in Figure 10 provides a low battery warning and also disconnects the low battery from the rest of the system to prevent damage to the battery. OUT1 is used to shutdown the ICL7663S when the battery voltage drops to the value where the load should be disconnected. As long as V_{SET1} is greater than 1.3V, OUT1 is low, but when V_{SET1} drops below 1.3V, OUT1 goes high, shutting off the ICL7663S. OUT2 is used for low battery warning. When V_{SET2} is greater than 1.3V, OUT2 is high and the low battery warning is on. When V_{SET2} drops below 1.3V, OUT2 is low and the low battery warning goes off. The trip voltage for low battery warning can be set higher than the trip voltage for shutdown to give advance low battery warning before the battery is disconnected.

Power Fail Warning and Powerup/Powerdown Reset

Figure 11 shows a power fail warning circuit with powerup/powerdown reset. When the unregulated DC input is above the trip point, OUT1 is low. When the DC input drops below the trip point, OUT1 shuts OFF and the power fail warning goes high. The voltage on the input of the 7805 decays at a rate of I_{OUT}/C. Since the 7805 will continue to provide 5V out at 1A until V_{IN} is less than 7.3V, this circuit will provide a certain amount of warning before the 5V output begins to drop.

The ICL7665S OUT2 is used to prevent a microprocessor from writing spurious data to a CMOS battery backup memory by causing OUT2 to go low when the 7805 5V output drops below the ICL7665S trip point.

Simple High/Low Temperature Alarm

Figure 12 illustrates a simple high/low temperature alarm which uses the ICL7665S with an NPN transistor. The voltage at the top of R_1 is determined by the V_{BE} of the transistor and the position of R_1's wiper arm. This voltage has a negative temperature coefficient. R_1 is adjusted so that V_{SET2} equals 1.3V when the NPN transistor's temperature reaches the temperature selected for the high temperature alarm. When this occurs, OUT2 goes low. R_2 is adjusted

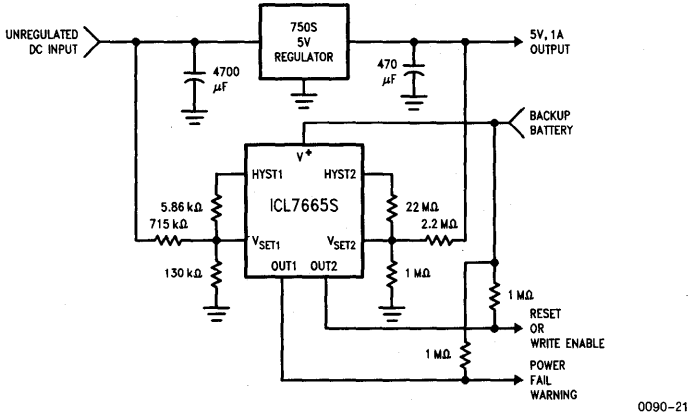


Figure 11: Power Fail Warning and Powerup/Powerdown Reset

NOTE: All typical values have been characterized but are not tested.

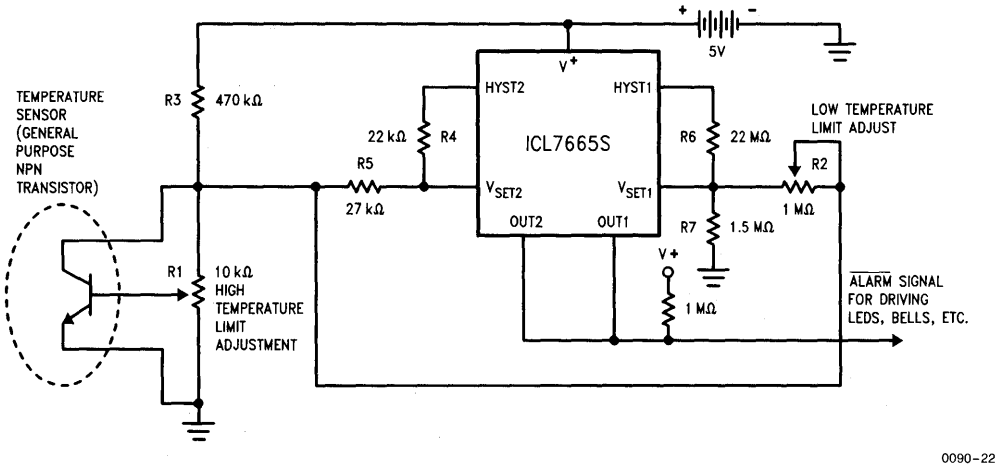


Figure 12: Simple High/Low Temperature Alarm

so that V_{SET1} equals 1.3V when the NPN transistor's temperature reaches the temperature selected for the low temperature alarm. When the temperature drops below this limit, OUT1 goes low.

AC Power Fail and Brownout Detector

Figure 13 shows a circuit that detects AC undervoltage by monitoring the secondary side of the transformer. The capacitor, C_1, is charged through R_1 when OUT1 is OFF. With a normal 110 VAC input to the transformer, OUT1 will discharge C_1 once every cycle, approximately every 16.7 ms. When the AC input voltage is reduced, OUT1 will stay OFF, so that C_1 does not discharge. When the voltage on C_1 reaches 1.3V, OUT2 turns OFF and the power fail warning goes high. The time constant, R_1C_1, is chosen such that it takes longer than 16.7 ms to charge C_1 1.3V.

For a more comprehensive AC power fail circuit, refer to Harris' new ICL7677 monolithic power fail detector.

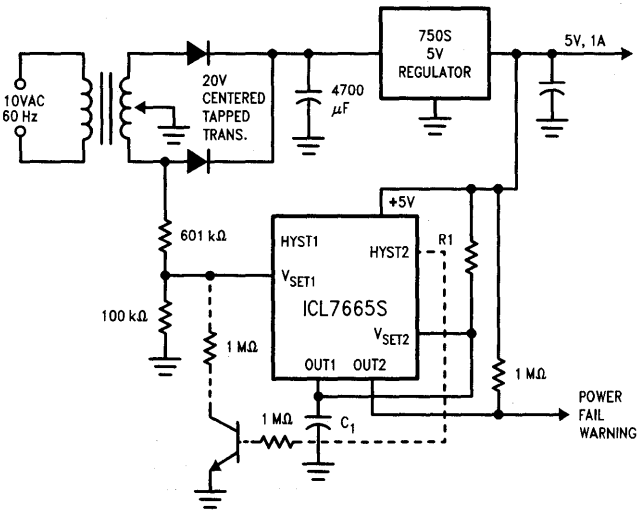


Figure 13: AC Power Fail and Brownout Detector

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICL7667
Dual Power MOSFET Driver

GENERAL DESCRIPTION

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters. The ICL7667's high current outputs minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitance. The ICL7667's inputs are TTL compatible and can be directly driven by common pulse-width modulation control IC's.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7667CBA	0°C to +70°C	8-Pin SOIC
ICL7667CPA		8-Pin Plastic
ICL7667CJA		8-Pin Cerdip
ICL7667CTV		TO-99 Can
ICL7667MTV*	−55°C to +125°C	TO-99 Can
ICL7667MJA*		8-Pin Cerdip

*Add /883B to Part Number for 883B processing.

FEATURES

- **Fast Rise and Fall Times**
  - **— 30ns With 1000pF Load**
- **Wide Supply Voltage Range**
  - **— V_{CC} = 4.5 to 15V**
- **Low Power Consumption**
  - **— 4mW With Inputs Low**
  - **— 120mW With Inputs High**
- **TTL/CMOS Input Compatible Power Driver**
  - **— R_{OUT} = 7Ω typ**
- **Direct Interface With Common PWM Control IC's**
- **Pin Equivalent to DS0026/DS0056; TSC426**

TYPICAL APPLICATIONS

- **Switching Power Supplies**
- **DC/DC Converters**
- **Motor Controllers**

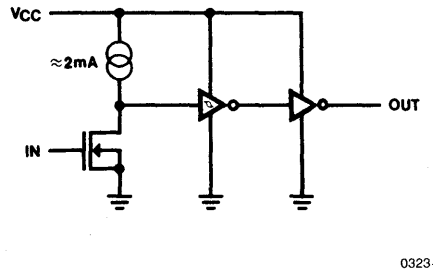
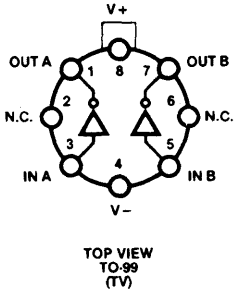


Figure 1: Functional Diagram



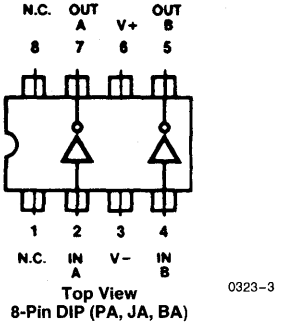


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Figure 2: Pin Configurations

302068-004

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+ to V^- 15V
Input Voltage ..... $(V^- - 0.3V)$ to $(V^+ + 0.3V)$
Package Dissipation, $T_A = 25°C$ 500mW
Linear Derating Factors

TO-99	Plastic	Cerdip
6.7mW/°C	5.6mW/°C	6.7mW/°C
above 50°C	above 36°C	above50°C

Storage Temperature ..... −65°C to +150°C
Operating Temperature Range
ICL7667C ..... 0°C to +70°C
ICL7667M ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

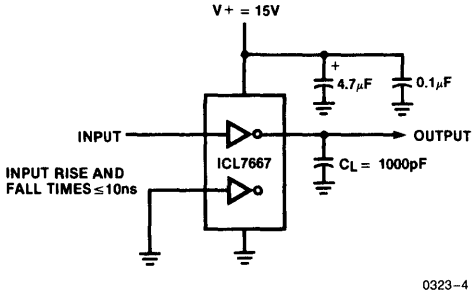
ELECTRICAL CHARACTERISTICS (STATIC)

Symbol	Parameter	Test Conditions	ICL7667C,M $T_A = 25°C$			ICL7667M $-55°C \le T_A \le +125°C$			Units
			Min	Typ	Max	Min	Typ	Max	
V_{IH}	Logic 1 Input Voltage	$V_{CC} = 4.5V$	2.0			2.0			V
V_{IH}	Logic 1 Input Voltage	$V_{CC} = 15V$	2.0			2.0			V
V_{IL}	Logic 0 Input Voltage	$V_{CC} = 4.5V$			0.8			0.5	V
V_{IL}	Logic 0 Input Voltage	$V_{CC} = 15V$			0.8			0.8	V
I_{IL}	Input Current	$V_{CC} = 15V$, $V_{IN} = 0V$ and 15V	−0.1		0.1	−0.1		0.1	μA
V_{OH}	Output Voltage High	$V_{CC} = 4.5V$ and 15V	$V_{CC} - 0.05$	V_{CC}		$V_{CC} - 0.1$			V
V_{OL}	Output Voltage Low	$V_{CC} = 4.5V$ and 15V		0	0.05			0.1	V
R_{OUT}	Output Resistance	$V_{IN} = V_{IL}$, $I_{OUT} = -10$ mA, $V_{CC} = 15V$		7	10			12	Ω
R_{OUT}	Output Resistance	$V_{IN} = V_{IH}$, $I_{OUT} = 10$mA, $V_{CC} = 15V$		8	12			13	Ω
I_{CC}	Power Supply Current	$V_{CC} = 15V$, $V_{IN} = 3V$ both inputs		5	7			8	mA
I_{CC}	Power Supply Current	$V_{CC} = 15V$, $V_{IN} = 0V$ both inputs		150	400			400	μA

ELECTRICAL CHARACTERISTICS (DYNAMIC)

Symbol	Parameter	Test Conditions	ICL7667C,M $T_A = 25°C$			ICL7667M $-55°C \le T_A \le +125°C$			Units
			Min	Typ	Max	Min	Typ	Max	
T_{D2}	Delay Time	Figure 3		35	50			60	ns
T_R	Rise Time	Figure 3		20	30			40	ns
T_F	Fall Time	Figure 3		20	30			40	ns
T_{D1}	Delay Time	Figure 3		20	30			40	ns

NOTE: All typical values have been characterized but are not tested.



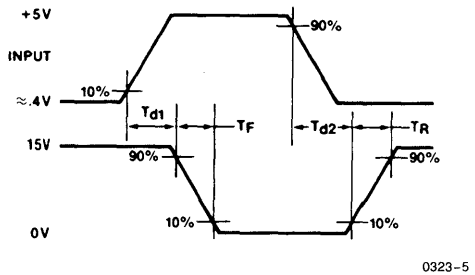
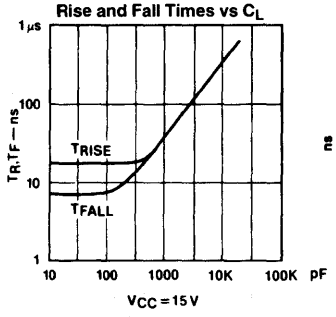
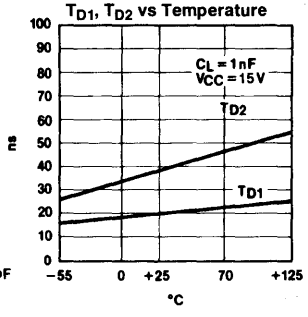
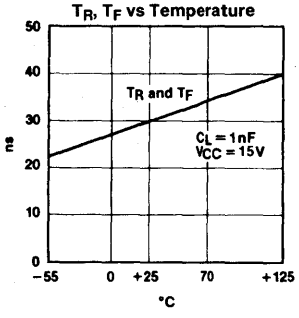


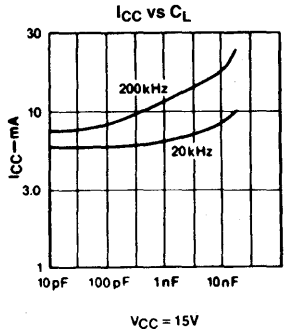
Figure 3: Test Circuit

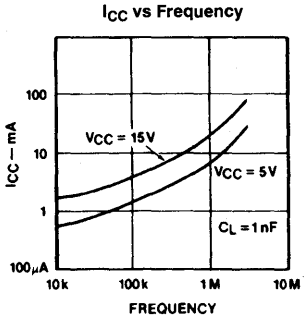
Typical Performance Characteristics

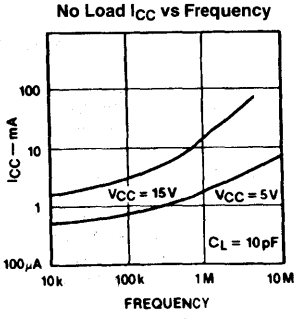












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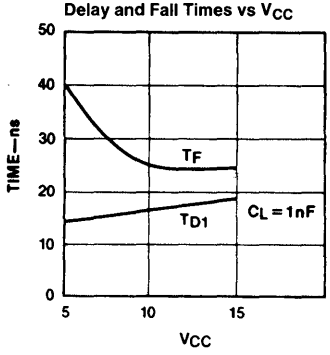
NOTE: All typical values have been characterized but are not tested.

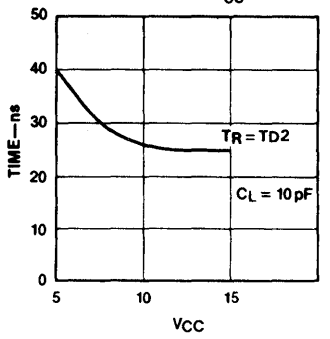
Typical Performance Characteristics (Continued)

Delay and Fall Times vs V_{CC}



0323-12

Rise Time vs V_{CC}



0323-13

DETAILED DESCRIPTION

The ICL7667 is a dual high-power CMOS inverter whose inputs respond to TTL levels while the outputs can swing as high as 15V. Its high output current enables it to rapidly charge and discharge the gate capacitance of power MOSFETs, minimizing the switching losses in switchmode power supplies. Since the output stage is CMOS, the output will swing to within millivolts of both ground and V_{CC} without any external parts or extra power supplies as required by the DS0026/56 family. Although most specifications are at $V_{CC} = 15V$, the propagation delays and specifications are almost independent of V_{CC}.

In addition to power MOS drivers, the ICL7667 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge-pump voltage inverters.

INPUT STAGE

The input stage is a large N-channel FET with a P-channel constant-current source. This circuit has a threshold of about 1.5V, relatively independent of the V_{CC} voltage. This means that the inputs will be directly compatible with TTL over the entire 4.5 – 15V V_{CC} range. Being CMOS, the inputs draw less than 1μA of current over the entire input voltage range of ground to V_{CC}. The quiescent current or no load supply current of the ICL7667 is affected by the input voltage, going to nearly zero when the inputs are at the 0 logic level and rising to 7mA maximum when both inputs are at the 1 logic level. A small amount of hysteresis, about 50 – 100mV at the input, is generated by positive feedback around the second stage.

OUTPUT STAGE

The ICL7667 output is a high-power CMOS inverter, swinging between ground and V_{CC}. At $V_{CC} = 15V$, the output impedance of the inverter is typically 7Ω. The high peak current capability of the ICL7667 enables it to drive a 1000pF load with a rise time of only 40ns. Because the output stage impedance is very low, up to 300mA will flow through the series N- and P-channel output devices (from V_{CC} to ground) during output transitions. This crossover current is responsible for a significant portion of the internal power dissipation of the ICL7667 at high frequencies. It can be minimized by keeping the rise and fall times of the input to the ICL7667 below 1μs.

APPLICATION NOTES

Although the ICL7667 is simply a dual level-shifting inverter, there are several areas to which careful attention must be paid.

GROUNDING

Since the input and the high current output current paths both include the ground pin, it is very important to minimize any common impedance in the ground return. Since the ICL7667 is an inverter, any common impedance will generate negative feedback, and will degrade the delay, rise and fall times. Use a ground plane if possible, or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close to the ICL7667 as is possible.

BYPASSING

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors that has a low impedance over a wide frequency range should be used. A 4.7μF tantalum capacitor in parallel with a low inductance 0.1μF capacitor is usually sufficient bypassing.

OUTPUT DAMPING

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

1) Reduce inductance by making printed circuit board traces as short as possible.
2) Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.
3) Use a 10 to 30Ω resistor in series with the output of the ICL7667. Although this reduces ringing, it will also slightly increase the rise and fall times.
4) Use good bypassing techniques to prevent supply voltage ringing.

NOTE: All typical values have been characterized but are not tested.

POWER DISSIPATION

The power dissipation of the ICL7667 has three main components:

1) Input inverter current loss
2) Output stage crossover current loss
3) Output stage I^2R power loss

The sum of the above must stay within the specified limits for reliable operation.

As noted above, the input inverter current is input voltage dependent, with an I_{CC} of 0.2mA maximum with a logic 0 input and 6mA maximum with a logic 1 input.

The output stage crowbar current is the current that flows through the series N- and P-channel devices that form the output. This current, about 300mA, occurs only during output transitions. **Caution:** The inputs should never be allowed to remain between V_{IL} and V_{IH} since this could leave the output stage in a high current mode, rapidly leading to destruction of the device. If only one of the drivers is being used, be sure to tie the unused input to a ground. **NEVER** leave an input floating. The average supply current drawn by the output stage is frequency dependent, as can be seen in I_{CC} vs. Frequency graph in the Typical Characteristics Graphs.

The output stage I^2R power dissipation is nothing more than the product of the output current times the voltage drop across the output device. In addition to the current drawn by any resistive load, there will be an output current due to the charging and discharging of the load capacitance. In most high frequency circuits the current used to charge and discharge capacitance dominates, and the power dissipation is approximately

$$P_{AC} = CV_{CC}^2f$$

Where C = Load Capacitance

f = Frequency

In cases where the load is a power MOSFET and the gate drive requirements are described in terms of gate charge, the ICL7667 power dissipation will be

$$P_{AC} = Q_GV_{CC}f$$

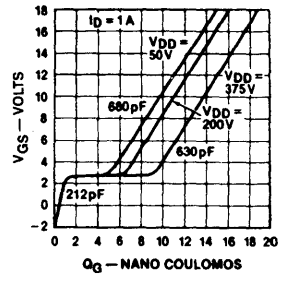
Where Q_G = Charge required to switch the gate, in Coulombs.

f = Frequency

POWER MOS DRIVER CIRCUITS

POWER MOS DRIVER REQUIREMENTS

Because it has a very high peak current output, the ICL7667 excels at driving the gate of power MOS devices. The high current output is important since it minimizes the time the power MOS device is in the linear region. Figure 4 is a typical curve of charge vs. gate voltage for a power MOSFET. The flat region is caused by the Miller capacitance, where the drain-to-gate capacitance is multiplied by the voltage gain of the FET. This increase in capacitance occurs while the power MOSFET is in the linear region and is dissipating significant amounts of power. The very high current output of the ICL7667 is able to rapidly overcome this high capacitance and quickly turns the MOSFET fully on or off.



0323-14

Figure 4: MOSFET Gate Dynamic Characteristics

DIRECT DRIVE OF MOSFETs

Figure 6 shows interfaces between the ICL7667 and typical switching regulator ICs. Note that unlike the DS0026, the ICL7667 does not need a dropping resistor and speed-up capacitor between it and the regulator IC. The ICL7667, with its high slew rate and high voltage drive can directly drive the gate of the MOSFET. The 1527 IC is the same as the 1525 IC, except that the outputs are inverted. This inversion is needed since ICL7667 is an inverting buffer.

TRANSFORMER COUPLED DRIVE OF MOSFETs

Transformers are often used for isolation between the logic and control section and the power section of a switching regulator. The high output drive capability of the ICL7667 enables it to directly drive such transformers. Figure 6 shows a typical transformer coupled drive circuit. PWM ICs with either active high or active low outputs can be used in this circuit, since any inversion required can be obtained by reversing the windings on the secondaries.

BUFFERED DRIVERS FOR MULTIPLE MOSFETs

In very high power applications which use a group of MOSFETs in parallel, the input capacitance may be very large and it can be difficult to charge and discharge quickly. Figure 8 shows a circuit which works very well with very large capacitance loads. When the input of the driver is zero, Q1 is held in conduction by the lower half of the ICL7667 and Q2 is clamped off by Q1. When the input goes positive, Q1 is turned off and a current pulse is applied to the gate of Q2 by the upper half of the ICL7667 through the transformer, T1. After about 20ns, T1 saturates and Q2 is held on by its own C_{gs} and the bootstrap circuit of C1, D1 and R1. This bootstrap circuit may not be needed at frequencies greater than 10kHz since the input capacitance of Q2 discharges slowly.

NOTE: All typical values have been characterized but are not tested.

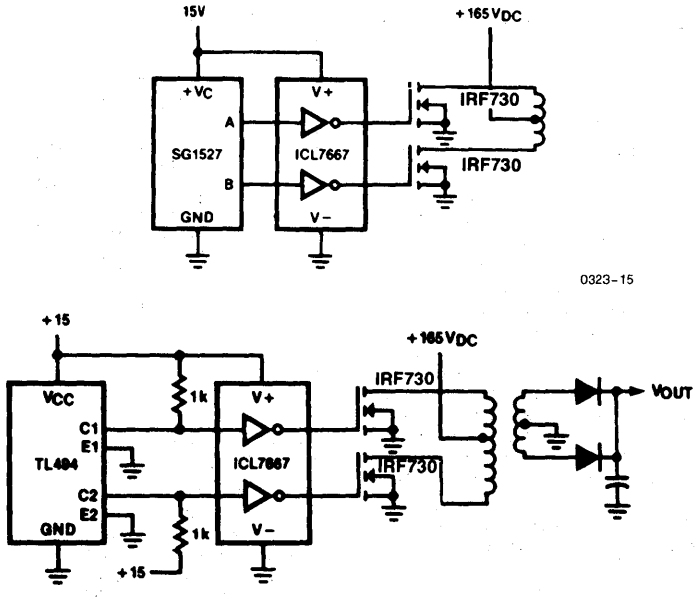


Figure 5: Direct Drive of MOSFET Gates

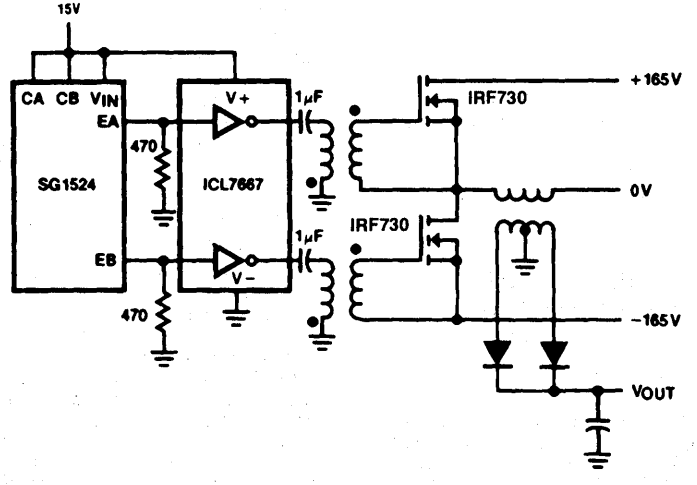


Figure 6: Transformer Coupled Drive Circuit

NOTE: All typical values have been characterized but are not tested.

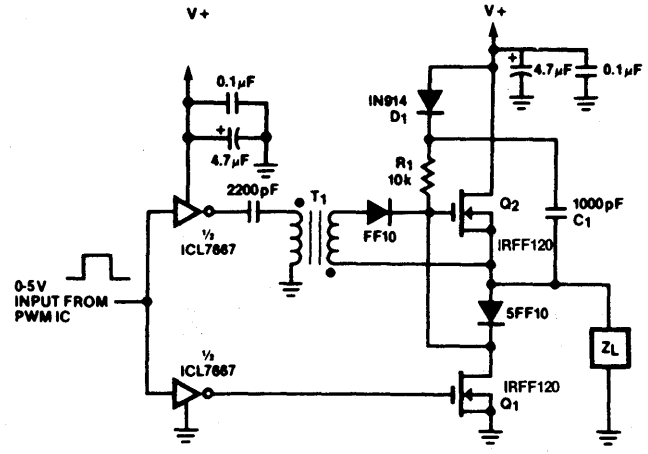
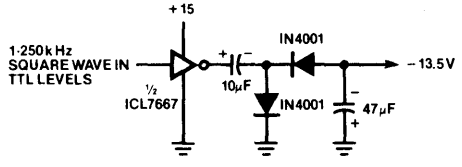


Figure 7: Very High-Speed Driver



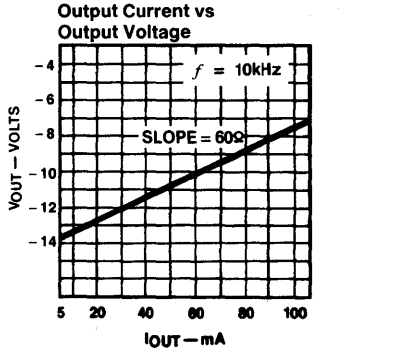


Figure 8: Voltage Inverter

NOTE: All typical values have been characterized but are not tested.

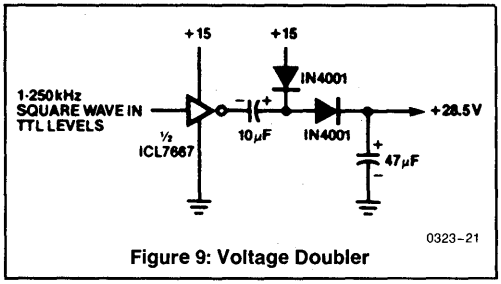


Figure 9: Voltage Doubler

OTHER APPLICATIONS

RELAY AND LAMP DRIVERS

The ICL7667 is suitable for converting low power TTL or CMOS signals into high current, high voltage outputs for relays, lamps and other loads. Unlike many other level translator/driver ICs, the ICL7667 will both source and sink current. The continuous output current is limited to 200mA by the I^2R power dissipation in the output FETs.

CHARGE PUMP OR VOLTAGE INVERTERS AND DOUBLERS

The low output impedance and wide V_{CC} range of the ICL7667 make it well suited for charge pump circuits. Figure 8 shows a typical charge pump voltage inverter circuit and a typical performance curve. A common use of this circuit is to provide a low current negative supply for analog circuitry or RS232 drivers. With an input voltage of +15V, this circuit will deliver 20mA at −12.6V. By increasing the size of the capacitors, the current capability can be increased and the voltage loss decreased. The practical range of the input frequency is 500Hz to 250kHz. As the frequency goes up, the charge pump capacitors can be made smaller, but the internal losses in the ICL7667 will rise, reducing the circuit efficiency.

Figure 9, a voltage doubler, is very similar in both circuitry and performance. A potential use of Figure 8 would be to supply the higher voltage needed for EEPROM or EPROM programming.

CLOCK DRIVER

Some microprocessors (such as the 68XX and 65XX families) use a clock signal to control the various LSI peripherals of the family. The ICL7667's combination of low propagation delay, high current drive capability and wide voltage swing make it attractive for this application. Although the ICL7667 is primarily intended for driving power MOSFET gates at 15V, the ICL7667 also works well as a 5V high-speed buffer. Unlike standard 4000 series CMOS, the ICL7667 uses short channel length FETs and the ICL7667 is only slightly slower at 5V than at 15V.

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICL7673
Automatic Battery Back-up Switch

GENERAL DESCRIPTION

The Harris ICL7673 is a monolithic CMOS battery backup circuit that offers unique performance advantages over conventional means of switching to a backup supply. The ICL7673 is intended as a low-cost solution for the switching of systems between two power supplies; main and battery backup. The main application is keep-alive-battery power switching for use in volatile CMOS RAM memory systems and real time clocks. In many applications this circuit will represent a low insertion voltage loss between the supplies and load. This circuit features low current consumption, wide operating voltage range, and exceptionally low leakage between inputs. Logic outputs are provided that can be used to indicate which supply is connected and can also be used to increase the power switching capability of the circuit by driving external PNP transistors.

FEATURES

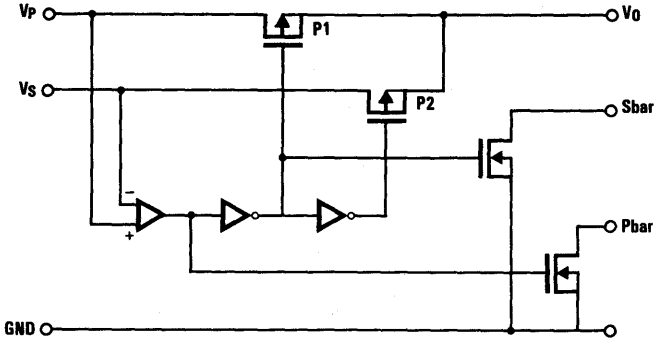
- **Automatically Connects Output to The Greater Of Either Input Supply Voltage**
- **If Main Power to External Equipment Is Lost, Circuit Will Automatically Connect Battery Backup**
- **Reconnects Main Power When Restored**
- **Logic Indicator Signaling Status Of Main Power**
- **Low Impedance Connection Switches**
- **Low Internal Power Consumption**
- **Wide Supply Range: 2.5 to 15 Volts**
- **Low Leakage Between Inputs**
- **External Transistors May Be Added If Very Large Currents Need to Be Switched**

APPLICATIONS

- **On Board Battery Backup for Real-Time Clocks, Timers, or Volatile RAMs**
- **Over/Under Voltage Detector**
- **Peak Voltage Detector**
- **Other Uses:**
  —Portable Instruments, Portable Telephones, Line Operated Equipment

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7673CPA	0°C to +70°C	8-pin minidip
ICL7673CBA	0°C to +70°C	8-pin SOIC



$V_P > V_S$, P_1 SWITCH ON AND P_{bar} SWITCH ON
$V_S > V_P$, P_2 SWITCH ON AND S_{bar} SWITCH ON

Figure 1: Functional Diagram

302070-005

NOTE: All typical values have been characterized but are not tested.

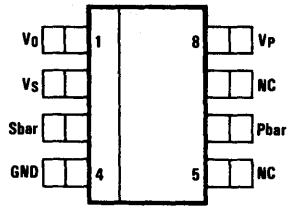
ABSOLUTE MAXIMUM RATINGS

Input Supply (V_P or V_S) Voltage .... (GND − 0.3) to +18V
Output Voltages P_{bar} and S_{bar} ..... (GND − 0.3) to +18V
Peak Current
  Input V_P (@ V_P = 5V) (note 1) 38mA
  Input V_S (@ V_S = 3V) 30mA
  P_{bar} or S_{bar} 150mA
Continuous Current
  Input V_P (@ V_P = 5V) (note 1) 38mA
  Input V_S (@ V_S = 3V) 30mA
  P_{bar} or S_{bar} 50mA

Package Dissipation 300mW
Derate ..... 6.1mW/°C
Operating Temperature Range:
  ICL7673C ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1. Derate above 25°C by 0.38mA/°C.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



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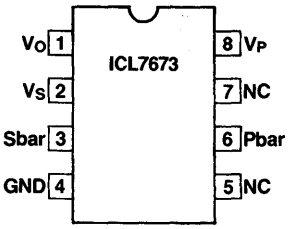
(Outline Dwg BA)
8-LEAD SOIC



0324-4

(Outline Dwg PA)
8-LEAD Minidip

Figure 2: Pin Configurations

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_P	INPUT VOLTAGE	V_S = 0 volts I load = 0mA	2.5	–	15	V
V_S		V_P = 0 volts I load = 0mA	2.5	–	15	
I^+	QUIESCENT SUPPLY CURRENT	V_P = 0 volts V_S = 3 volts I load = 0mA	–	1.5	5	μA
$R_{ds(on)P1}$	SWITCH RESISTANCE P1 (NOTE 2)	V_P = 5 volts V_S = 3 volts I load = 15mA	–	8	15	Ω
		@ T_A = 85°C	–	16	–	
		V_P = 9 volts V_S = 3 volts I load = 15mA	–	6	–	Ω
		V_P = 12 volts V_S = 3 volts I load = 15mA	–	5	–	Ω

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$T_{C(P1)}$	TEMPERATURE COEFFICIENT OF SWITCH RESISTANCE P1	V_P = 5 volts V_S = 3 volts I load = 15mA	–	0.5	–	%/°C
$R_{ds(on)P2}$	SWITCH RESISTANCE P2 (NOTE 2)	V_P = 0 volts V_S = 3 volts I load = 1mA	–	40	100	Ω
		@ T_A = 85°C	–	60	–	
		V_P = 0 volts V_S = 5 volts I load = 1mA	–	26	–	Ω
		V_P = 0 volts V_S = 9 volts I load = 1mA	–	16	–	Ω
$T_{C(P2)}$	TEMPERATURE COEFFICIENT OF SWITCH RESISTANCE P2	V_P = 0 volts V_S = 3 volts I load = 1mA	–	0.7	–	%/°C
$I_{L(PS)}$	LEAKAGE CURRENT (V_P to V_S)	V_P = 5 volts V_S = 3 volts I load = 10mA	–	0.01	20	nA
		@ T_A = 85°C	–	35	–	
$I_{L(SP)}$	LEAKAGE CURRENT (V_S to V_P)	V_P = 0 volts V_S = 3 volts I load = 1mA	–	0.01	50	nA
		@ T_A = 85°C	–	120	–	
$V_{O\ Pbar}$	OPEN DRAIN OUTPUT SATURATION VOLTAGES	V_P = 5 volts V_S = 3 volts I sink = 3.2mA I load = 0mA	–	85	400	mV
		@ T_A = 85°C	–	120	–	
		V_P = 9 volts V_S = 3 volts I sink = 3.2mA I load = 0mA	–	50	–	mV
		V_P = 12 volts V_S = 3 volts I sink = 3.2mA I load = 0mA	–	40	–	mV
$V_{O\ Sbar}$		V_P = 0 volts V_S = 3 volts I sink = 3.2mA I load = 0mA	–	150	400	mV
		@ T_A = 85°C	–	210	–	
		V_P = 0 volts V_S = 5 volts I sink = 3.2mA I load = 0mA	–	85	–	mV
		V_P = 0 volts V_S = 9 volts I sink = 3.2mA I load = 0mA	–	50	–	mV

NOTE: All typical values have been characterized but are not tested.

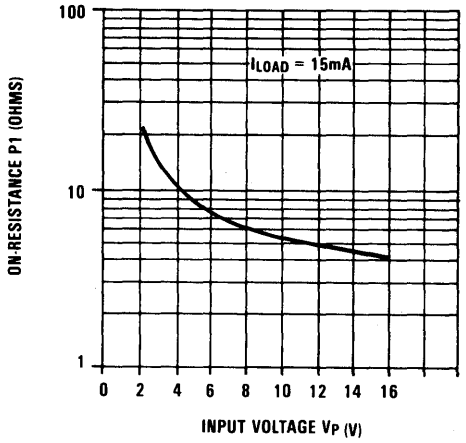
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$I_{L\ Pbar}$	OUTPUT LEAKAGE CURRENTS OF Pbar AND Sbar	V_P = 0 volts V_S = 15 volts I load = 0mA	–	50	500	nA
		@ T_A = 85°C	–	900	–	
$I_{L\ Sbar}$		V_P = 15 volts V_S = 0 volts I load = 0mA	–	50	500	nA
		@ T_A = 85°C	–	900	–	
$V_P - V_S$	SWITCHOVER UNCERTAINTY FOR COMPLETE SWITCHING OF INPUTS AND OPEN DRAIN OUTPUTS.	V_S = 3 volts I sink = 3.2mA I load = 0mA	–	±10	±50	mV

NOTE 2. The minimum input to output voltage can be determined by multiplying the load current by the switch resistance.

TYPICAL PERFORMANCE CHARACTERISTICS

ON-RESISTANCE SWITCH P1 AS A FUNCTION OF INPUT VOLTAGE V_P



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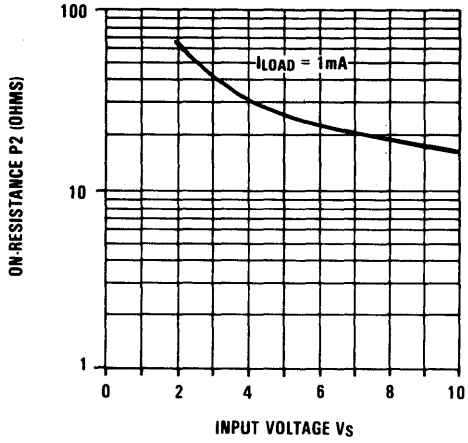
ON-RESISTANCE SWITCH P2 AS A FUNCTION OF INPUT VOLTAGE V_S



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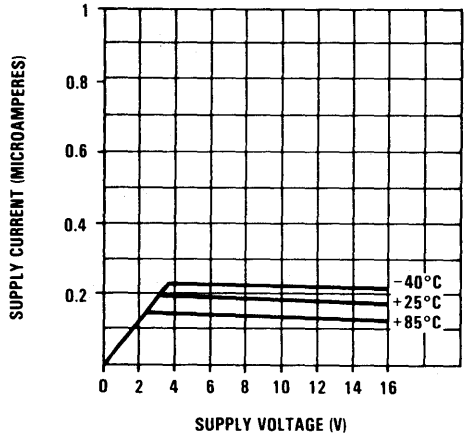
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



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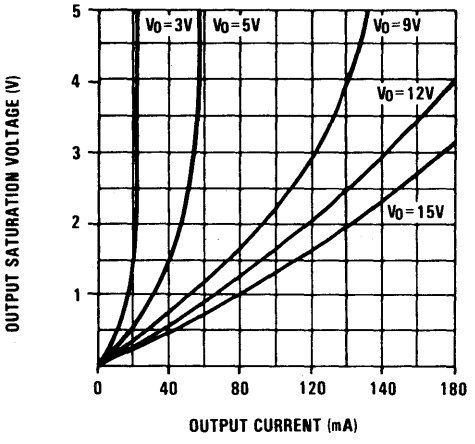
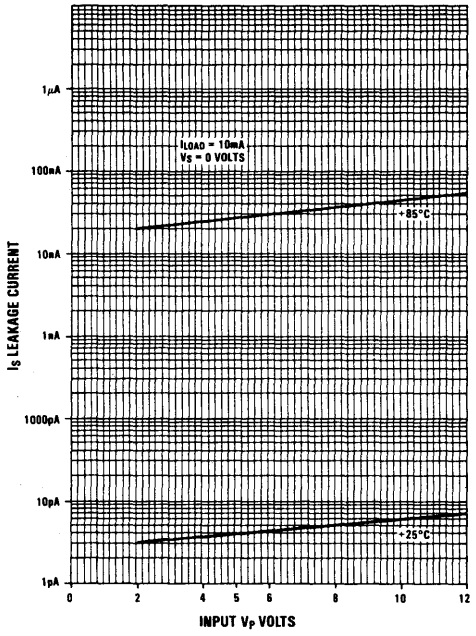
Pbar OR Sbar SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



0324-8

I_S LEAKAGE CURRENT V_P to V_S AS A FUNCTION OF INPUT VOLTAGE



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DETAILED DESCRIPTION

As shown in the functional diagram (Figure 1), the ICL7673 includes a comparator which senses the input voltages V_P and V_S. The output of the comparator drives the first inverter and the open-drain N-channel transistor P_{bar}. The first inverter drives a large P-channel switch, P1, a second inverter, and another open-drain N-channel transistor, S_{bar}. The second inverter drives another large P-channel switch P2. The ICL7673, connected to a main and a backup power supply, will connect the supply of greater potential to its output. The circuit provides break-before-make switch action as it switches from main to backup power in the event of a main power supply failure. For proper operation, inputs V_P and V_S must not be allowed to float, and, the difference in the two supplies must be greater than 50 millivolts. The leakage current through the reverse biased parasitic diode of switch P2 is very low.

OUTPUT VOLTAGE

The output operating voltage range is 2.5 to 15 volts. The insertion loss between either input and the output is a function of load current, input voltage, and temperature. This is due to the P-channels being operated in their triode region, and, the ON-resistance of the switches is a function of output voltage V_O. The ON-resistance of the P-channels have positive temperature coefficients, and therefore as temperature increases the insertion loss also increases. At low load currents the output voltage is nearly equal to the greater of the two inputs. The maximum voltage drop across switch P1 or P2 is 0.5 volts, since above this voltage the body-drain parasitic diode will become forward biased. Complete switching of the inputs and open-drain outputs typically occurs in 50 microseconds.

NOTE: All typical values have been characterized but are not tested.

INPUT VOLTAGE

The input operating voltage range for V_P or V_S is 2.5 to 15 volts. The input supply voltage (V_P or V_S) slew rate should be limited to 2 volts per microsecond to avoid potential harm to the circuit. In line-operated systems, the rate-of-rise (or fall) of the supply is a function of power supply design. For battery applications it may be necessary to use a capacitor between the input and ground pins to limit the rate-of-rise of the supply voltage. A low-impedance capacitor such as a 0.047μF disc ceramic can be used to reduce the rate-of-rise.

STATUS INDICATOR OUTPUTS

The N-channel open drain output transistors can be used to indicate which supply is connected, or can be used to drive external PNP transistors to increase the power switching capability of the circuit. When using external PNP power transistors, the output current is limited by the beta and thermal characteristics of the power transistors. The application section details the use of external PNP transistors.

APPLICATIONS

A typical discrete battery backup circuit is illustrated in Figure 3. This approach requires several components, substantial printed circuit board space, and high labor cost. It also consumes a fairly high quiescent current. The ICL7673 battery backup circuit, illustrated in Figure 4, will often replace such discrete designs and offer much better performance, higher reliability, and lower system manufacturing cost. A trickle charge system could be implemented with an additional resistor and diode as shown in Figure 5. A complete low power AC to regulated DC system can be implemented using the ICL7673 and ICL7663S micropower voltage regulator as shown in Figure 6.

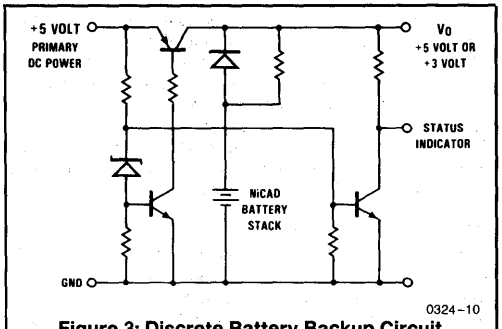


Figure 3: Discrete Battery Backup Circuit

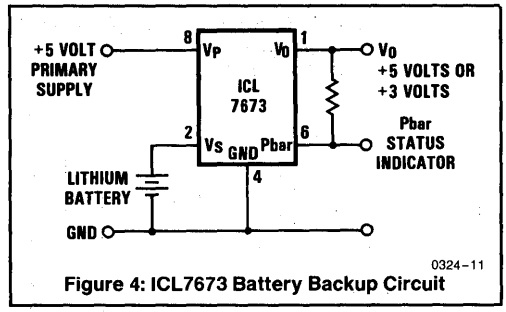


Figure 4: ICL7673 Battery Backup Circuit

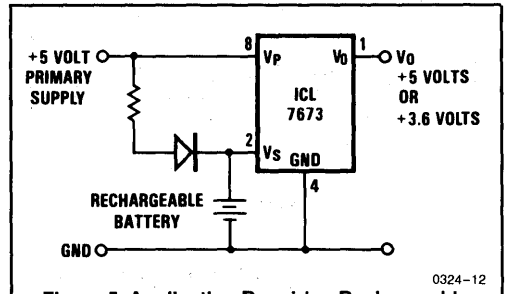


Figure 5: Application Requiring Rechargeable Battery Backup

Applications for the ICL7673 include volatile semiconductor memory storage systems, real-time clocks, timers, alarm systems, and over/under voltage detectors. Other systems requiring DC power when the master AC line supply fails can also use the ICL7673.

A typical application, as illustrated in Figure 7, would be a microprocessor system requiring a 5 volt supply. In the event of primary supply failure, the system is powered down, and a 3 volt battery is employed to maintain clock or volatile memory data. The main and backup supplies are connected to V_P and V_S, with the circuit output V_O supplying power to the clock or volatile memory. The ICL7673 will sense the main supply, when energized, to be of greater potential than V_S and connect, via its internal MOS switches, V_P to output V_O. The backup input, V_S will be disconnected internally. In the event of main supply failure, the circuit will sense that the backup supply is now the greater potential, disconnect V_P from V_O, and connect V_S.

Figure 8 illustrates the use of external PNP power transistors to increase the power switching capability of the circuit. In this application the output current is limited by the beta and thermal characteristics of the power transistors.

If hysteresis is desired for a particular low power application, positive feedback can be applied between the input V_P and open drain output S_{bar} through a resistor as illustrated in Figure 9. For high power applications hysteresis can be applied as shown in Figure 10.

The ICL7673 can also be used as a clipping circuit as illustrated in Figure 11. With high impedance loads the circuit output will be nearly equal to the greater of the two input signals.

NOTE: All typical values have been characterized but are not tested.

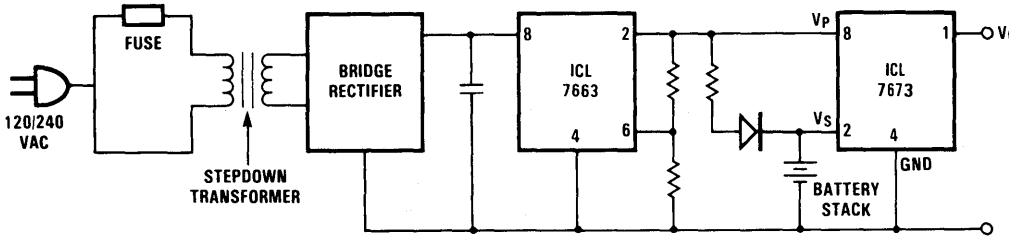


Figure 6: Power Supply for Low Power Portable AC to DC Systems

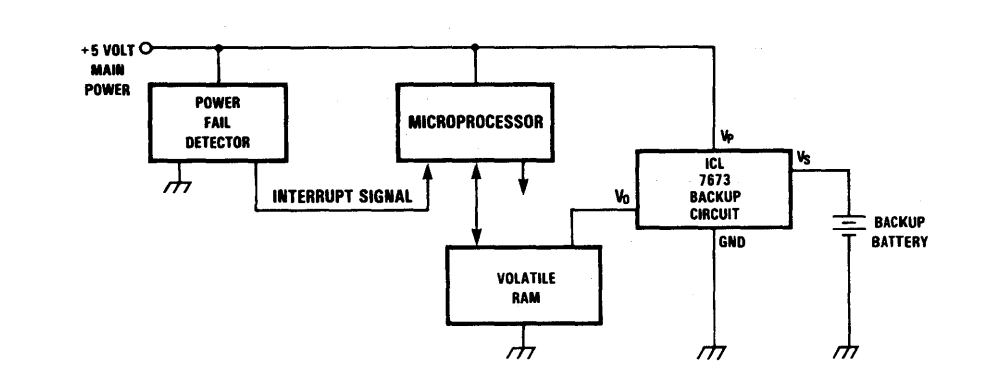


Figure 7: Typical Microprocessor Memory Application

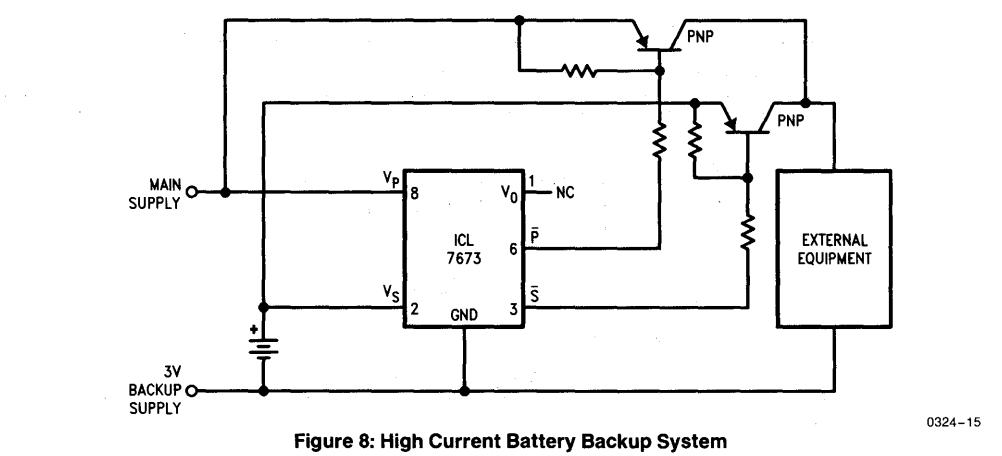


Figure 8: High Current Battery Backup System

NOTE: All typical values have been characterized but are not tested.

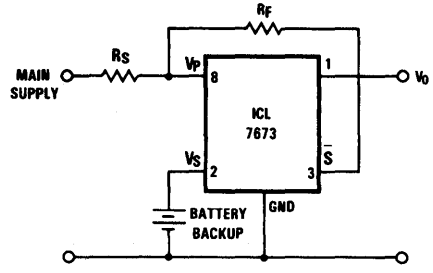


Figure 9: Low Current Battery Backup System With Hysteresis

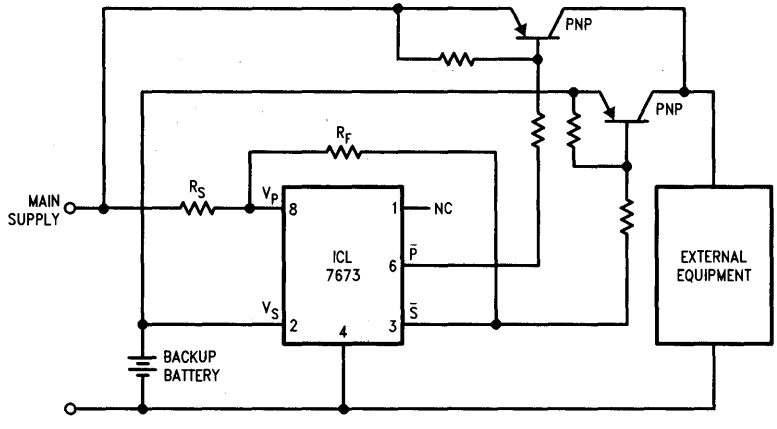


Figure 10: High Current Backup System With Hysteresis

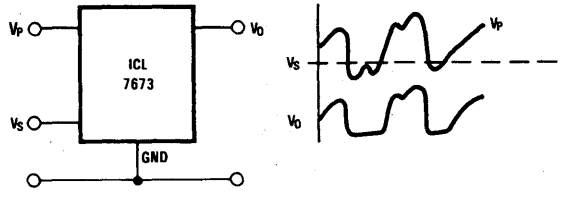


Figure 11: Clipping Circuits

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICL7675/ICL7676
Switched-Mode Power Supply Controller Set

GENERAL DESCRIPTION

The ICL7675/7676 two-chip set provides the necessary control circuitry for regulation of a single-ended, transformer coupled, flyback type switching power supply. Specifically designed to operate in this type of configuration, the Harris controller chip set is trimmed to provide a regulated 5V output.

The two chips comprise a primary side controller and a secondary side controller. Referring to Figure 3, the output of the primary side controller drives the power MOSFET switch in the primary leg of the transformer. The switch is always turned off at a time corresponding to the falling edge of the internal system clock at a frequency of 50kHz. Following an initial soft-start cycle, the switch is turned on at a time corresponding to a pulse received from the secondary side controller via a pulse transformer. The secondary side controller detects the power switch turn-off at the secondary of the transformer and initiates a time-out sequence with a duration directly proportional to the output voltage being sensed. A pulse generated at the end of the time-out period is fed back through the pulse transformer to the primary side controller, thereby completing the control loop.

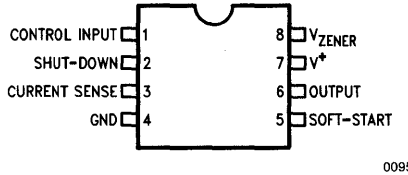
Power for the primary side controller may be taken from the high voltage DC input to the power transformer via a resistor which feeds current to the on-chip zener diode. This eliminates the need for a separate power supply for the controller. Excessive current in the power MOSFET switch is detected at one end of a resistor in series with the source of the MOSFET, forcing the primary side controller into the soft-start mode.

FEATURES

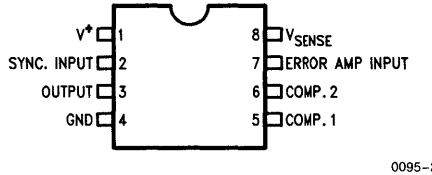
- **Output Voltage of 5V ± 5% Under All Conditions**
- **Simple Low Current Pulse Transformer Feedback**
- **Power Switch Over-Current Protection**
- **Soft-Start**
- **No Off-Chip Trimming Required**
- **Minimum External Components**
- **Low Supply Current**
- **Output Duty Cycle—5% to 75%**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7675CPA	0°C to +70°C	8 Lead MINIDIP
ICL7675CJA	0°C to +70°C	8 Lead CERDIP
ICL7675IPA	−25°C to +85°C	8 Lead MINIDIP
ICL7675MJA	−55°C to +125°C	8 Lead CERDIP
ICL7676CPA	0°C to +70°C	8 Lead MINIDIP
ICL7676MJA	−55°C to +125°C	8 Lead CERDIP



ICL7675
Package Outline (PA, JA)



ICL7676
Package Outline (PA, JA)

Figure 1: Pin Configurations

302072-002

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

ICL7675

Supply Voltage (V^+ to GND) 16V
Voltage on any pin ..... (V^+ + 0.3) to (GND − 0.3) V

ICL7676

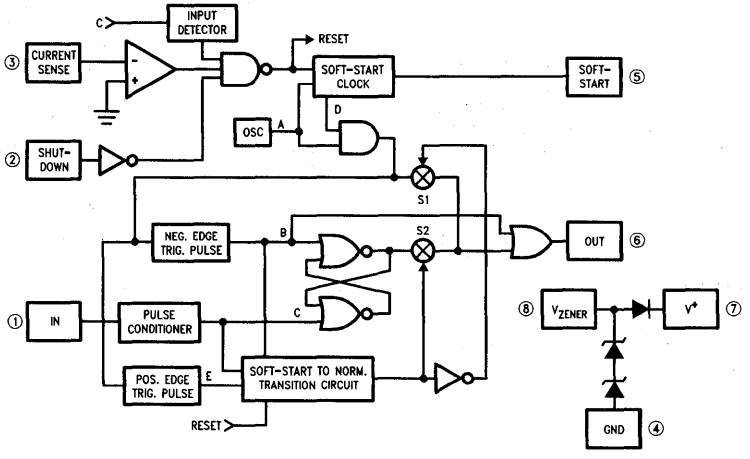
Supply Voltage (V_{sense} to GND) 16V
Voltage on any pin ..... (V_{sense} + 0.3) to (GND − 0.3) V

ICL7675 & ICL7676

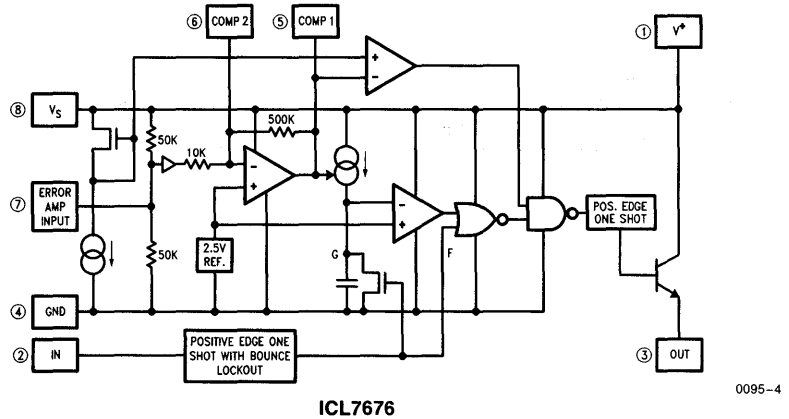
Lead Temperature (Soldering, 10 sec) ..... 300°C
Storage Temperature Range ..... −65°C to +150°C

Operating Temperature Range
ICL767XC ..... 0°C to +70°C
ICL767XI ..... −25°C to +85°C
ICL767XM ..... −55°C to +125°C
Continuous Total Power Dissipation (T_A = 25°C)
CERDIP Package ..... 500 mW
Plastic Package ..... 375 mW

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



ICL7675



ICL7676

Figure 2: Functional Diagrams

NOTE: All typical values have been characterized but are not tested.

ICL7675
ELECTRICAL CHARACTERISTICS

Unless otherwise stated: Pins 1, 2, 3, and 4 are connected to GND; Pin 7 is connected to V^+; all other pins are open; $V^+ = 13.5V$

Parameter	Test Conditions	Limits												Units
		$T_A = +25°C$			$0°C < T_A < +70°C$			$-25°C < T_A < +85°C$			$-55°C < T_A < +125°C$			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Oscillator: Frequency		42		58	41		59	40		60	38		62	kHz
Temp. Stability						0.1			0.1			0.1		%/°C
Output: Fall Time (Note 1)	R_O = 10M, C_O = 500 pF		100	150			170			180			200	ns
Rise Time (Note 1)	R_O = 10M, C_O = 500 pF		100	150			170			180			200	ns
Voltage	Output Low, $I_O = -5$ mA		0.2	0.3			0.33			0.35			0.40	V
	Output High, $I_O = +5$ mA	12.8			12.8			12.7			12.6			V
Control Input: Leakage Current			0.01	10			50			50			100	nA
Threshold		9.5		11.0	9.0		11.0	8.5		11.5	8.5		12.0	V
Shut-Down: Leakage Current			0.01	10			50			50			100	nA
Threshold		9.5		11.5	9.4		11.8	9.3		12.0	9.2		12.5	V
Soft-Start: Time-out	Open Pin		8											ms
Current Limiting: Sense Voltage		420		600	390		630	370		640	300		700	mV
Sense Voltage Temperature Coefficient						0.6			0.6			0.6		mV/°C
V_{zener}: Forward Voltage (Pin 8)		13.5	13.8	14.3										V
Forward Voltage Temperature Coefficient						7			7			7		mV/°C
V^+ Supply Voltage (Pin 7)			13.2											V
Supply Current	No Output Load			1.2			1.3			1.4			1.5	mA

NOTE 1: This parameter is guaranteed by design and is not tested in production.

NOTE: All typical values have been characterized but are not tested.

ICL7676
ELECTRICAL CHARACTERISTICS

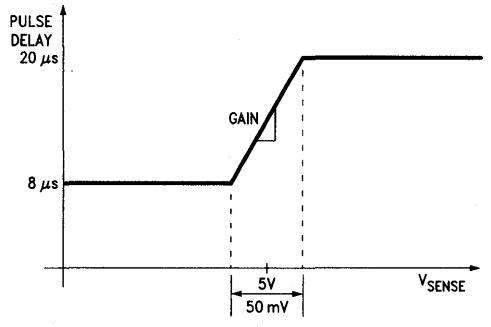
Unless otherwise stated: Pins 2 and 4 are connected to GND; Pins 1 and 8 are connected to V_{sense}; all other pins are open; $V^+ = 5V$

Parameter	Test Conditions	Limits									Units
		$T_A = +25°C$			$0°C < T_A < +70°C$			$-55°C < T_A < +125°C$			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Power Supply: Output Voltage	15 μs Pulse Delay (Note 2)	4.9		5.1							V
Temp. Stability						100			100		mV
Sync Input: Threshold		1.2		2.4	1.2		2.4	1.2		2.4	V
Leakage			0.01	10			50			100	nA
Output: Voltage	Output High	4.35			4.3			4.1			V
Pulse Current		15			14			10			mA
Pulse Width		0.55		1.0	0.5		1.0	0.25		1.0	μs
Min. Pulse Delay	50kHz Clock at Input			9			9			12	μs
Max. Pulse Delay	50kHz Clock at Input	20			20			20			μs
Gain	Time-Out/V_{sense}	90	140		70			50			μs/V
V_{sense} Input Current (Note 3)	$V_{sense} = 5.0V$, No Load			1.0			1.1			1.5	mA

NOTE 2: This corresponds to a 25% duty cycle at the output of the ICL7675.

3: This parameter is equivalent to device supply current.

TYPICAL PERFORMANCE CHARACTERISTICS



Pulse Delay vs V_{sense}

NOTE: All typical values have been characterized but are not tested.

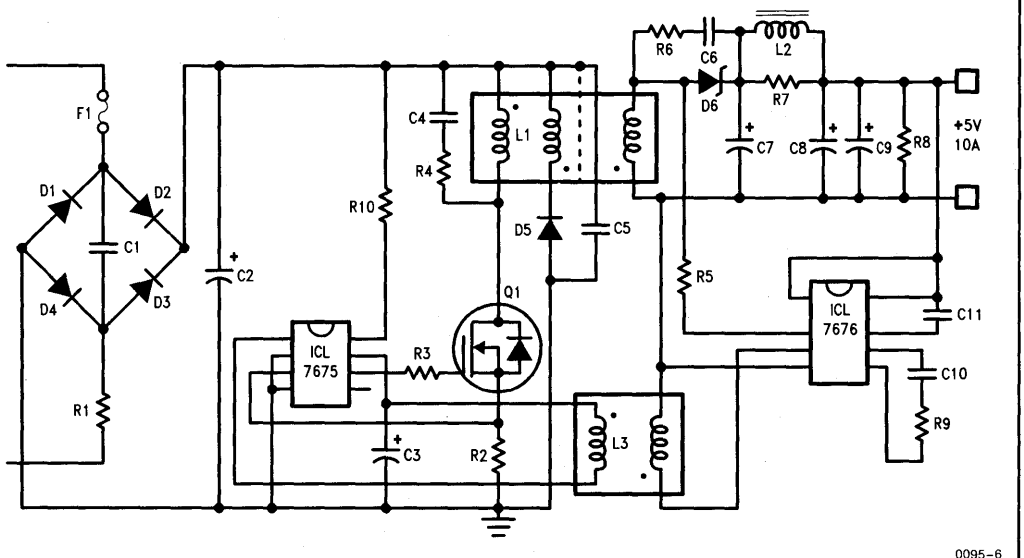


Figure 3: System Schematic

C1	0.022 μF/400V	R1	Thermistor	D1-4	1N4004
C2	330 μF/200V	R2	.47Ω/2W	D5	1N4937
C3	470 μF/16V	R3	10Ω/.125W	D6	MBR1035
C4	180 pF/500V	R4	1.5 kΩ/2W		
C5	0.022 μF/400V	R5	10 kΩ/.25W	L1	Lp = 5.1 mH
C6	39 pF/500V	R6	10Ω/.5W		n = 1/14
C7	11,000 μF/6.3V	R7	3.9Ω/.5W	L2	20 μH
C8	4.7 μF/16V	R8	10Ω/5W	L3	47 μH
C9	.047 μF/10V	R9	68 kΩ/.25W		n = 1/3
C10	2200 pF/500V	R10	75 kΩ/.5W	Q1	GE IRF821
C11	270 pF/500V				

Table 1: Example Component Values for SMPS System

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

Refer to the system schematic (Figure 3), timing diagram (Figure 4) and the individual controller functional diagrams (Figure 2) for the following discussion.

Secondary Side Controller

The secondary side controller, ICL7676, is required to provide an output pulse that will cause the primary side controller, ICL7675, to turn the MOSFET power switch on in the primary leg of the power supply transformer. This pulse must occur at a time such that the resultant switch duty cycle causes the output of the power supply to be regulated at precisely 5V. The circuit accomplishes this by amplifying the difference between a fraction of the output voltage and an internally generated reference voltage and using that output to control a ramp generator. When the output of the ramp generator reaches the reference voltage level, a comparator triggers a monostable giving a fixed width pulse at the output of the controller. A positive transition at the power supply transformer secondary, corresponding to power switch turn-off, triggers a one-shot with a bounce lock-out feature that prevents any false triggering due to excessive ringing at this node. The output of this one-shot resets the ramp generator by turning on a MOS transistor across the ramp capacitor. Also, if the ramp voltage has not reached the comparator threshold, the one-shot triggers the output monostable. This ensures that a pulse is sent to the primary side controller every cycle. Variations in the output voltage are detected and cause an increase or decrease in the current supplied to the ramp capacitor. This causes a change in the capacitor ramp rate at point G in Figure 2 and a consequent change in the time when the comparator threshold crossover occurs, generating an output pulse from the ICL7676. The output pulse's position is thereby modulated relative to the input trigger in direct proportion to the power supply voltage. The direction of change is such that when the resultant duty cycle at the output of the ICL7675 corrects the power supply voltage, a negative feedback control loop is formed that maintains the desired output voltage.

Primary Side Controller

The primary side controller, ICL7675, must process the incoming pulse from the secondary side controller, ICL7676, and combine this with the internally generated oscillator waveform to produce a driving signal for the MOSFET switch. Initially, however, a soft-start circuit determines the driving signal waveform. Therefore, there must also be a circuit which directs the orderly transition from soft-start to normal operation. When the power supply is first turned on, a power-up-reset circuit initializes the soft-start clock and sets switch S1 on and switch S2 off, as shown in Figure 2. The soft-start's slowly increasing duty cycle waveform is fed through an AND gate and through switch S1 to the output buffer. Meanwhile, the transition circuit continuously monitors the relative position in time between the incoming pulse from the secondary side controller and the leading edge from the clock waveform. When the duty cycle of the soft-start clock has increased to the point where its positive edge occurs earlier than the input pulse, then the transition circuit gives control of the output switch drive to the feedback loop by turning off S1 and turning on S2. Now the negative edge of the clock resets the flip-flop, turning off the power switch, and the input pulse sets the flip-flop, turning on the power switch. The negative edge of the soft-start clock is synchronized to the negative edge of the oscillator and occurs at a fixed frequency of 50kHz. The soft-start clock's output duty cycle gradually increases from zero to 100%, but when ANDed with the 75% duty cycle waveform of the oscillator, the maximum duty cycle of the resultant waveform is limited to 75% as well.

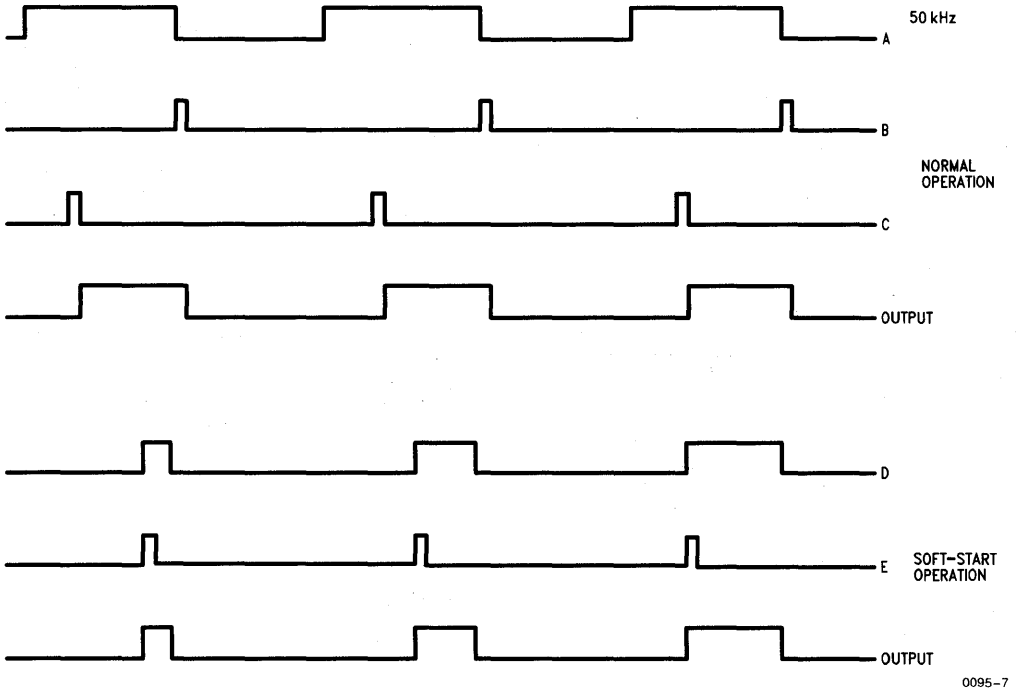
Soft-Start Cycle

The soft-start cycle time is fixed at about 15 ms. It can be increased somewhat by adding capacitance to pin 5. If no pulse is received from the secondary side controller, the primary side controller will reset, initiating the soft-start sequence. It will continue to recycle through the soft-start sequence until a pulse is received. As long as a pulse is received within one eighth cycle after the falling edge of the system clock, an approximately 0.5 μs pulse will appear at the output to drive the power switch. This allows for delays in the feedback loop which might cause the controlling pulse to arrive late.

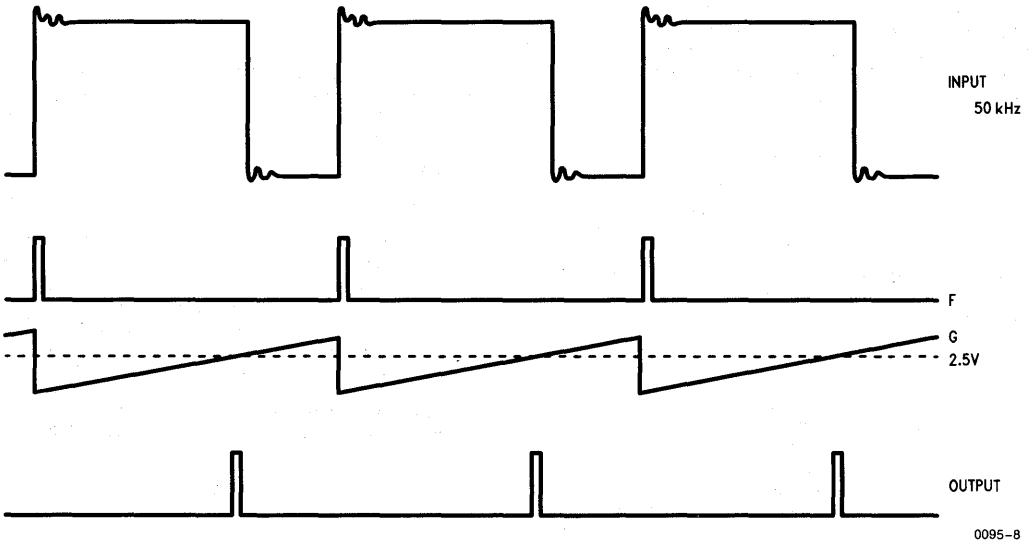
Other Features

The external resistor R2, connected between the I_{sense} pin and ground and placed in series with the power MOSFET switch, senses an over-current fault condition, tripping a comparator which shuts down the output. After the fault condition has been removed, the power supply will pass through the soft-start cycle before returning to normal operation. There is also a shut-down pin that when forced high will shut down the output. An on-chip zener diode and rectifying diode combination, connected through a dropping resistor to the high DC input voltage of the power supply, provides power to the circuit.

NOTE: All typical values have been characterized but are not tested.



ICL7675 Timing Diagram



ICL7676 Timing Diagram

Figure 4: 7675/7676 Timing Diagrams

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

Refer to the system schematic (Figure 3) for the following discussion of a flyback converter.

The input bridge rectifier and filter circuit converts the 115V AC line to 163V DC. The unregulated high voltage DC is applied across a GE IRF 821 Power FET (Q1) and the primary of transformer L1. The Power FET acts as a switch, opening and closing in response to the gate drive signal from the output of the ICL7675 controller. When Q1 opens, the energy stored in L1 is transferred to the secondary and through diode D6 into C7. This is characteristic of the flyback converter. The ICL7676 monitors the voltage across C7 and sends a variable time delay pulse through pulse transformer L3 to the ICL7675 with a delay proportional to the voltage sensed. The ICL7675 translates the pulse into a variable duty-cycle 50kHz output signal which drives the gate of the Power FET Q1 "ON" and "OFF" thereby closing the negative feedback loop.

The flyback converter topology is best suited for power levels below 150W due to the high ripple current produced across capacitor C7. This topology is favored because of its simplicity. Output voltage control is achieved by varying the ratio of ON to OFF time for Q1, and can be expressed as follows:

$$V_0 = V_{C2}\,N\frac{t_{on}}{t_{off}} - V_{D6} - I_0R_S$$

where:

V_{C2} = Voltage across C2
V_{D6} = Forward drop across D6
I_0 = Output current
R_S = Output series resistance
N = Turns ratio of L1 (secondary/primary)

This applies for continuous mode operation where the current in L1 never falls to zero during a clock cycle. For light loads, discontinuous conduction may occur. The primary inductance of L1 required to assure continuous mode operation at a light load $I_{0(min)}$ is:

$$L_p = \frac{t^2_{on(min)} \times V^2_{C1(max)} \times f}{2(V_0 + V_{D6} + I_0R_S)\,I_{0(min)}}$$

For $I_{0(min)}$ = 10% of full load at high line:

$$L_p = \frac{(6 \times 10^{-6})^2 \times (185)^2 \times (50 \times 10^3)}{(2)\,(6)\,(1)} = 5.1\text{ mH}$$

This inductance can be obtained on a gapped ferrite 'E' core which offers an excellent (performance)/(cost) ratio. The air gap is required to prevent saturation at low line and maximum current.

Neglecting voltage spikes due to leakage inductance, drain to source voltage stress for Q1 is:

$$V_{ds} = \frac{V_0 + V_{D6} + I_0R_S}{N} + V_{C2}$$

A turns ratio N = 1/14 limits V_{ds} to a safe value at high line. A catch winding clamps voltage spikes across the Power FET at turn off. The winding should be bifilar wound with the primary to minimize leakage inductance. An electrostatic shield will improve isolation between primary and secondary.

The network composed of L2 and C8 at the output provides additional filtering by attenuating high frequency spikes and ripple. The corner frequency for the LC filter is approximately 20kHz which effectively attenuates 50kHz and higher order harmonics. Inductor L2 is shunted by 3.9Ω R7 to reduce the output "Q" and minimize output ringing. For critical damping: $R = \sqrt{L/C}$. Diode D6 is a fast recovery Schottky doide. It has a low V_d and is snubbed by resistor R6 and capacitor C6 to limit the dV/dt and overshoot. The diode D5 is also a fast recovery diode which is connected to the catch winding of transformer L1. This protects the power FET Q1 from potentially damaging voltage spikes.

Switching Losses

Power FETs behave like ideal switches and are very well suited for high frequency switching power supply applications. The fast turn-on and turn-off of the power MOSFET results in very low switching losses. In this application the turn-off losses are essentially zero, due in part to the presence of snubber network C4 and R4. And the worst case turn-on losses are less than two watts.

Energy: $W = \int_0^t V_{ds}(t)\,I_d(t)\,dt$

where: $V_{ds}(t) = 10^9\,t$

$I_d(t) = 12.5 \times 10^6\,t$

$W = 12.5 \times 10^{15} \int_0^{200\text{ ns}} t^2\,dt$

Integrating:

$$W = 12.5 \times 10^{15}\frac{t^3}{3} \qquad \text{where: } t = 200 \times 10^{-9}$$

and Power:

$$P = W \times F \qquad \text{where: } F = 50\text{ kHz}$$

$$\text{Power} = 12.5 \times 10^{15}\left[\frac{(2 \times 10^{-7})^3}{3}\right] 5 \times 10^4$$

$$= 1.67\text{ Watts}$$

Because the power MOSFET has very high current gain it can be driven directly from the ICL7675. This is highly advantageous because it simplifies the circuitry and reduces overall system manufacturing costs.

Control Loop Design

The control loop for a transformer coupled flyback converter is similar to the boost converter from which it is derived. The presence of an LC resonant filter with its steep 180 degree phase rolloff and a right-half plane zero in the loop transfer function makes frequency compensation a non-trivial exercise. However, the design of the control loop can be made easier if not simpler with the proper tools. The mathematical equation representing the power mesh equivalent transfer function may be reduced to a model which can be entered into SPICE, a widely used circuit simulation program, or any other simulation software being used. The equation for the modulator-power mesh portion of the control loop may be expressed as:

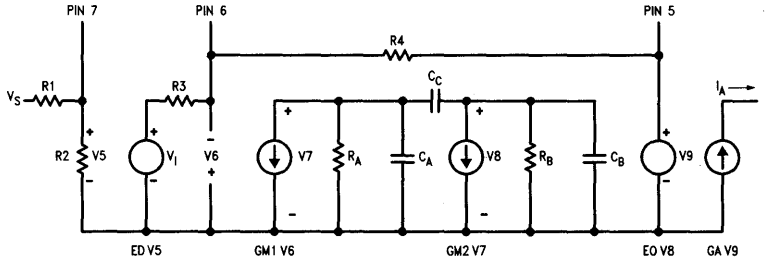
$$\frac{V_0}{D(1-D)}\left[1 - \frac{sn^2DL_p}{(1-D)^2\,R_0}\right]\frac{T(1-D)^2}{C_rV_{ref}}$$

NOTE: All typical values have been characterized but are not tested.

where:

- D = Duty cycle
- n = Transformer turns ratio
- L_p = Primary inductance
- R_0 = Load resistance
- T = Clock period
- C_r = Internal ramp capacitance = 40 pF
- V_{ref} = Internal reference voltage = 2.5V

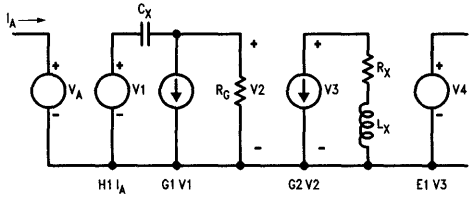
A model representing this equation is shown in Figure 5B. Combined with the output filter shown in Figure 5C, and the error amp shown in Figure 5A, a computer simulation can be used to determine the optimum combination of components for a stable design that still provides adequate response to external disturbances. Note that in the output filter, the effective primary inductance and inductor series resistance are multiplied by $n^2/(1-D)^2$. In the example here, a combination of lead compensation provided by C11 and lag compensation provided by R9 and C10 gave the desired response.



Valid for frequencies < 200 kHz

GM1 = 0.4 MV	R_B = 500 kΩ	R1 = 50 kΩ	E0 = ED = 1
GM2 = 0.15 MV	C_B = 20 pF	R2 = 50 kΩ	GA = 6.67 μV
R_A = 1.0 MΩ	C_C = 10 pF	R3 = 11.94 kΩ	
C_A = 4 pF		R4 = 500 kΩ	

Figure 5A: Error Amp Model



$$\frac{V4}{I_A} = \frac{E1 \times G1 \times G2 \times H1 \times R_G \left[1 - s\frac{C_X}{G1}\right]\left(R_X + s L_X\right)}{1 + s R_G C_X}$$

$$R_G = G1 = R_X = G2 = H1 = 1$$

$$C_X = L_X = \frac{n^2 D L_p}{(1-D)^2}$$

$$E1 = \frac{V_0}{D(1-D)} \times \frac{T(1-D)^2}{C_r V_{ref}}$$

Figure 5B: Control Loop Model

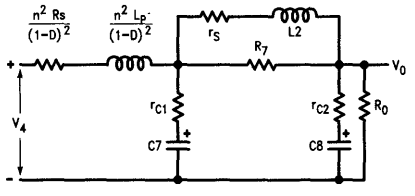


Figure 5C: Output Filter Model

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICL7680

±5V to ±15V Dual Switching Regulator

GENERAL DESCRIPTION

The Harris ICL7680 voltage regulator provides the necessary control circuitry for independent regulation of both a single-ended, boost type and boost-buck (inverting) type switched-mode power supply. Specifically designed to operate in these two configurations, the ICL7680 is trimmed to provide both a +15V and −15V output with a +5V input voltage.

The internal circuitry is divided into two similar sections sharing a common voltage reference and oscillator: one for the boost stage and another for the inverting stage. Each section contains an error amplifier, comparator, and output logic which provide a standard pulse-width modulated output drive to an external transistor switch. The boost section senses the positive power supply output voltage via an internal thin film resistor divider which is trimmed for +15V. This voltage is user adjustable by adding an external resistor. Similarly, the inverting section senses the negative power supply output voltage at the input of an inverting amplifier that is trimmed for −15V.

The output logic provides the proper phase to drive an N-channel MOSFET on the boost side and a P-channel MOSFET on the inverting side. Although bipolar devices could be used, the chip is optimized for MOSFET drive and these devices will give higher efficiency.

For overcurrent protection, an internal comparator senses the voltage across an external resistor between the chip input supply pin and the current sense pin, shutting the circuit down for a voltage exceeding the limit.

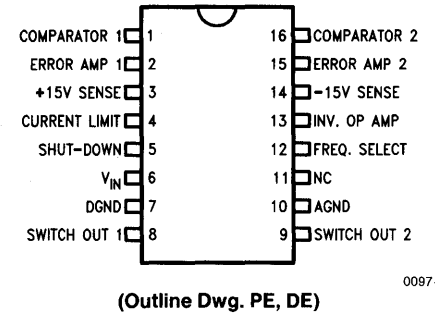
Oscillator frequencies of 25 kHz, 50 kHz, or 100 kHz can be set with the three-state frequency select pin connected to GND, left open, or connected to V_{in} respectively.

FEATURES

- **Dual Output Voltages of ±15V±5% Under All Conditions**
- **Output Voltage Externally Adjustable**
- **Input Current Sensing**
- **Three Frequency Oscillator, Selectable with a Single Pin**
- **No Off-Chip Trimming Required**
- **Minimum External Components**
- **Low Supply Current**
- **Built-In Latchup Protection**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7680CPE	0°C to +70°C	16 Pin Plastic
ICL7680IPE	−25°C to +85°C	16 Pin Plastic
ICL7680IDE	−25°C to +85°C	16 Pin Ceramic
ICL7680MDE	−55°C to +125°C	16 Pin Ceramic



(Outline Dwg. PE, DE)

Figure 1: Pin Configuration

HARRIS SEMICONDUCTOR, 2450 Walsh Avenue, Santa Clara, Ca. 95051

NOTE: All typical values have been characterized but are not tested.

302090-002
April 1988

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{in} to GND) 7V
Voltage on Any Pin ..... (V_{in} + 0.3) to (GND − 0.3)V
(Except Pin 3 and Pin 14)
Voltage on Pin 3 ..... +30V to −0.3V
Voltage on Pin 14 ..... +0.3V to −30V
Lead Temperature (Soldering, 10 sec) ..... 300°C
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
ICL7680C ..... 0°C to +70°C
ICL7680I ..... −25°C to +85°C
ICL7680M ..... −55°C to +125°C
Continuous Total Power Dissipation (T_A = 25°C)
Ceramic Package ..... 500 mW
Plastic Package ..... 375 mW

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

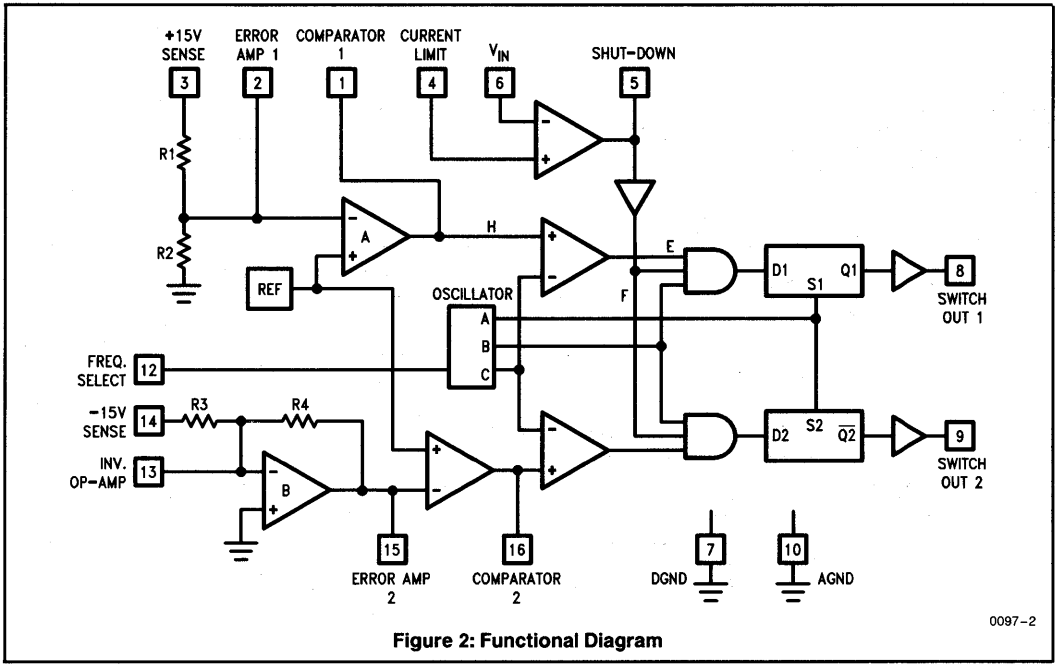


Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified: V_{in} = 5V, Pins 3, 7, 10, and 14 are connected to GND; Pin 4 is connected to V_{in}; all other pins are open.

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = 0°C to +70°C			T_A = −25°C to +85°C			T_A = −55°C to +125°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{REG}	Regulation Voltage	Duty Cycle 30, 70%	14.6		15.4	14.55		15.45	14.5		15.5	14.4		15.6	V
SWITCH OUTPUTS															
V_L	Low Voltage	No Load I_{sink} = 20 mA			0.1 1.0			0.1 1.3			0.1 1.5			0.1 1.6	V V
V_H	High Voltage	No Load I_{sink} = 20 mA	4.9 3.5			4.9 3.4			4.9 3.4			4.9 3.3			V V
D_{max1}	Max Duty Cycle 1	+15V Sense = 0V	80		90	80		90	80		90	80		90	%
D_{min2}	Min Duty Cycle 2	−15V Sense = 0V	10		20	10		20	10		20	10		20	%
t_f	Fall Time	R_0 = 10 MΩ, C_0 = 500 pF		70											ns
t_r	Rise Time	R_0 = 10 MΩ, C_0 = 500 pF		70											ns
SENSE INPUTS															
R_{in}	Input Resistance		110	140		109			107			105			kΩ
OP-AMP, ERROR AMPS, AND CURRENT LIMIT INPUTS															
I_{LK}	Leakage Current	Pin Voltage = 0V, V_{in}		0.01	120			145			170			220	nA
SHUT-DOWN (Bi-Directional)															
	Overdrive Input Current	Pin Voltage = 0V to V_{in}		−25	−35			−40			−45			−50	μA
V_{IL}	Input Low Voltage				0.8			0.8			0.8			0.8	V
V_{IH}	Input High Voltage		3.1			3.1			3.1			3.1			V
V_{OL}	Output Low Voltage	I_{sink} = 200 μA			0.45			0.5			0.55			0.6	V
V_{OH}	Output High Voltage	I_{source} = 10 μA	4.75	4.85		4.7			4.65			4.6			V
CURRENT LIMITING															
V_{sense}	Sense Voltage	Shut-Down Low	115		175	110		180	105		185	100		190	mV
OSCILLATOR															
f	Frequency	Pin 12 = GND Pin 12 = Open Pin 12 = V_{in}		28 55 100											kHz
	Frequency Select Input Current	Pin Voltage = 0V Pin Voltage = V_{in}	−1	−0.5	0 15	−1		0 16	−1		0 18	−1		0 20	μA μA
	Freq. Stability with Temperature	(Note 1)						10			10			10	%
	Freq. Stability with Voltage	V_{in} = 4V to 6V		0.5											%
SUPPLY															
V_{in}	Input Voltage Range	Functional Oper.	4		6	4		6	4		6	4		6	V
I_{in}	Supply Current	No Load		1.2	1.7			1.8			1.9			2.0	mA

NOTE 1: Parameter guaranteed by design and characterization, but not tested over temperature.

NOTE: All typical values have been characterized but are not tested.

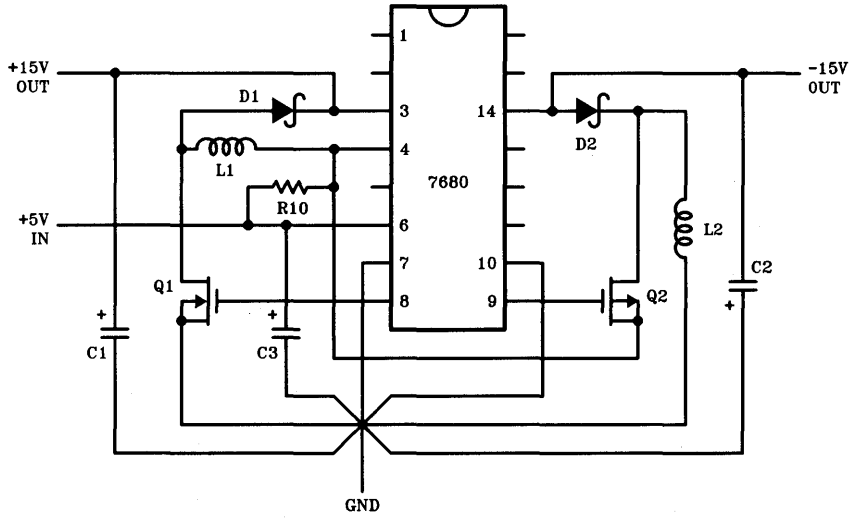


Figure 3: System Schematic for Discontinuous Mode

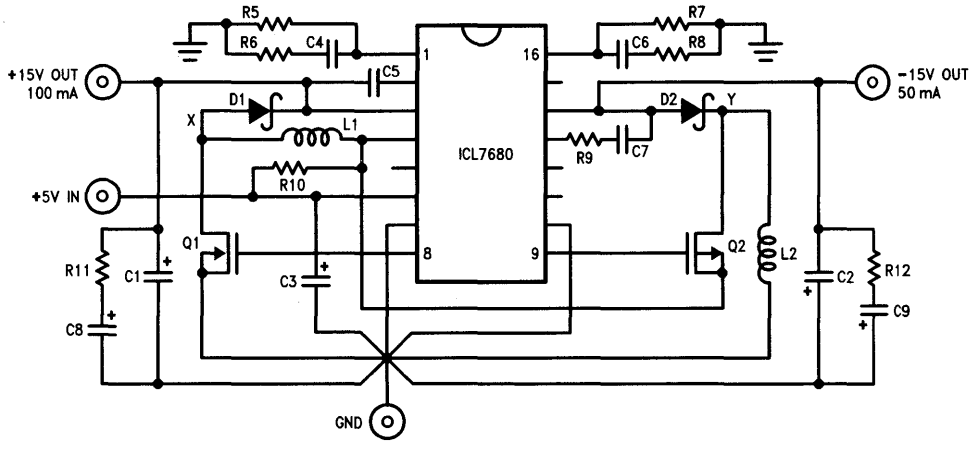


Figure 4: System Schematic for Continuous Mode

2 POWER CONTROL CIRCUITS

NOTE: All typical values have been characterized but are not tested.

Table 1: Example Component Values for SMPS System

C1	150 μF/75V	R5	750 kΩ/.25W	D1-2	1N5818
C2	150 μF/75V	R6	51 kΩ/.25W	L1-2	75 μH (Discontinuous Mode)
C3	10 μF/16V	R7	750 kΩ/.25W	L1-2	750 μH (Continuous Mode)
C4	0.01 μF/50V	R8	51 kΩ/.25W		93 turns, 22 ga. wire on Magnetics 55204 core
C5	0.001 μF/50V	R9	12 kΩ/.25W		Supertex
C6	0.01 μF/50V	R10	0.15Ω/.25W	Q1	TN0204N2
C7	0.001 μF/50V	R11	2.2Ω/.5W	Q2	TP0204N2
C8	470 μF/25V	R12	2.2Ω/.5W		
C9	470 μF/25V				

DETAILED DESCRIPTION

Refer to the system schematic (Figures 3 and 4) and the regulator functional diagram (Figure 2) for the following discussion.

Control Circuits

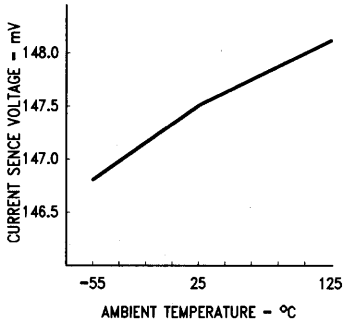
The ICL7680 is divided into two sections: one for the +15V regulator and another for the −15V regulator. The output of the boost circuit is connected to the +15V sense pin (3) where it is divided down to about 1.25V and applied to one input of an error amplifier (A). Here it is compared to the internal 1.25V reference, resulting in an error voltage which appears at the amplifier output. A pulse width modulated signal is produced by comparing the output of the error amp to a sawtooth waveform generated in the oscillator circuit. Variations in the error amp output cause the duty cycle at the output of the comparator to change. After some signal conditioning in the output logic circuitry, the PWM signal appears at the output pin where it can be connected to the boost circuit power switch. The duty cycle varies in direct proportion to voltage changes at the +15V sense pin (3) connected to the power supply output. The direction of change is such that when the voltage increases, duty cycle decreases, thus forming a negative feedback control loop. Changes in output voltage may occur due to fluctuations in either input voltage or load current. If the output voltage magnitude drops, for example, the effective duty ratio is increased until the output rises to the proper level, providing continuous regulation.

The −15V section operates similarly except that the buck-boost circuit output is applied to the −15V sense pin (14) at the input of an inverting op-amp (B) which provides +1.25V at its output. The op-amp (B) has an input common-mode range which includes ground.

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

CURRENT SENSE VOLTAGE vs. AMBIENT TEMPERATURE



0097-10

Oscillator

Oscillator frequencies of 25 kHz, 50 kHz, or 100 kHz can be selected with pin 12 connected to GND, left open, or connected to V_{in} respectively.

An internal sync pulse resets the output latch which only recognizes one input transition between each pulse. This provides immunity to noise at the output of the error amp which would otherwise cause multiple transitions at the output of the PWM comparator.

A sawtooth waveform with a peak to peak amplitude of two times the reference voltage, or 2.5V, provides one of the inputs for each of the PWM comparators at point C. The sawtooth waveform is also applied to a third comparator with a reference input, giving an output clock with a duty cycle of 85% at point B. When ANDed with either of the pulse width modulator outputs, this sets the upper duty cycle limit for the overall system. This limit is necessary during start-up conditions.

Other Features

A current limit comparator is also provided to monitor the input current of the supply through an external resistor, R10, between V_{in} (pin 6) and pin 4. If the IR drop across the resistor exceeds the limit, the output of the comparator at pin 5 will go low, turning off the switch drive output. Pin 5 can also be overdriven to shut down the circuit by other means.

APPLICATIONS

Refer to the power supply system schematic (Figures 3 and 4) for the following discussion of the boost and boost-buck converter.

When Q1 is off, current flows from the input source and energy is stored in L1. During this time, diode D1 is reverse biased, capacitor C1 supplies the output current, and the stored energy is somewhat depleted. When Q1 turns off, an inductive voltage step appears across L1 since current in an inductor cannot change instantaneously, making point X positive relative to V_{in}. Diode D1 becomes forward biased, and the current initially flowing through L1 and Q1 now continues flowing via diode D1 into output capacitor C1 and to the load, restoring the energy lost when C1 alone was driving the load. The magnitude of the inductive voltage step across L1 when Q1 opens depends on the switch duty cycle which is controlled by the ICL7680. The larger the duty cycle, the greater the peak current and energy stored in L1; hence, the higher the inductive voltage impulse across L1 necessary to transfer that energy out during the switch off time.

The duty cycle can be expressed as:

$$D = \frac{V_O + V_D - V_{in}}{V_O + V_D - V_S}$$

where: D = Duty cycle
V_O = Power supply output voltage = 15V
V_{in} = Power supply input voltage ≅ 5V
V_D = Forward diode voltage drop
V_S = Switch "on" voltage
$= \left[\frac{I_O}{1-D}\right] R_{DS(on)}$ for MOSFET
$= V_{CE(SAT)}$ for Bipolar

2 POWER CONTROL CIRCUITS

NOTE: All typical values have been characterized but are not tested.

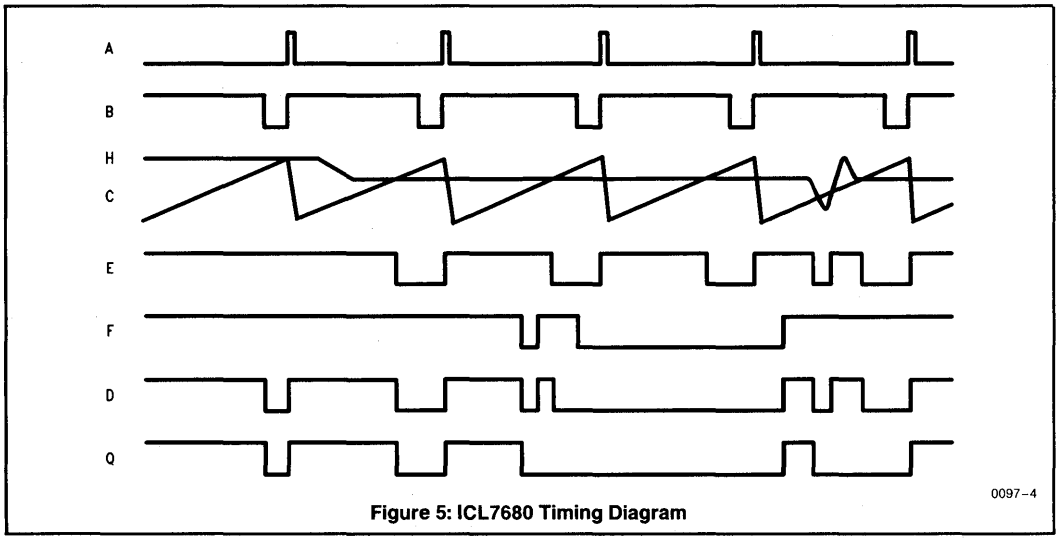


Figure 5: ICL7680 Timing Diagram

This applies for continuous mode operation where the current in L1 never falls to zero during a clock cycle. For light loads, discontinuous conduction may occur. The inductance of L1 required to assure continuous mode operation at a light load of $I_{O(min)}$ is:

$$L1 = \frac{V_O D_{min} (1 - D_{min})^2}{2 I_{O(min)} f}$$

The −15V section of the circuit behaves similarly except that the inductive voltage step at point Y is negative because of the reversed orientation of Q2 and L2. This negative inductive step forward biases diode D2 and allows the current initially flowing through Q2 and L2 to continue flowing through D2 out of capacitor C2 and out of the load. Again, the magnitude of the inductive voltage step across L2 depends on switch duty cycle which is controlled by the ICL7680. The duty cycle here can be expressed as:

$$D = \frac{V_D + |V_O|}{V_{in} + V_D + |V_O| - V_S}$$

The inductance of L2 required to assure continuous mode operation at light load $I_{O(min)}$ is:

$$L2 = \frac{(V_D + |V_O|) (1 - D_{min})^2}{2 I_{O(min)} f}$$

Component Selection

Power MOSFETs are recommended for the switching transistors because of their superior efficiency, especially with the low 5V input. Efficiencies close to 90% should be easily obtainable with these devices. To help determine the correct part to use, the voltage stress and current for Q1 and Q2 are given below. Also, since the gate is being driven with a 5V signal, a device with low V_{th} (threshold voltage) must be selected to ensure sufficient drive for turn on. Devices that fit into this category include the Supertex TN01A (N-ch) and TP02A/TP06A (P-ch) series and the RCA RFL1N (N-ch) series of MOSFETs. Alternatively, a bipolar configuration, such as shown in Figure 6, may be used in place of Q2 in Figures 3 and 4. This approach results in a system efficiency of about 80%.

The drain to source voltage stress for Q1 is:

$$V_{DS} = V_D + V_O$$

The drain to source voltage stress for Q2 is:

$$V_{DS} = V_D + V_{in} + |V_O|$$

The average "on" current in both Q1 and Q2 is:

$$I_{ON} = \frac{I_O}{1 - D}$$

Schottky diodes such as the 1N5818 with their lower forward voltage drop and high speed will also give improved efficiency. The average current in the diode is just I_O, and the reverse voltage stress is about V_O for D1 and ($|V_O|$ + V_{in}) for D2.

The peak-to-peak output voltage ripple for both topologies can be shown to be approximately:

$$\Delta V_O = \frac{D_{max} I_O}{f \bullet C}$$

This equation can be used to compute the minimum value of capacitor required to maintain a given percentage of voltage ripple at the output. It must be remembered, however, that the equivalent series resistance (esr) of the output capacitor can contribute significantly to the voltage ripple and

NOTE: All typical values have been characterized but are not tested.

must also be taken into account. The ripple contribution from esr for the low inductor current ripple in continuous mode conduction can be given by:

$$\Delta V_O = esr \bullet I_O \frac{1}{1-D}$$

This value should be added to the contribution from the output capacitor given above to give the total output voltage ripple. An equivalent series resistance of only 0.1Ω can dominate the total ripple at the output.

Finally, as shown in the last section and in Figure 9, any inductor series resistance R_S is multiplied by a factor $1/(1-D)^2$. For the large duty cycles encountered in this circuit this can have a significant effect on efficiency, and therefore R_S should be kept to a minimum.

Control Loop Design

The control loop for the boost and boost-buck converters is described below. The presence of an LC resonant filter with its steep 180 degree phase rolloff and a right-half plane zero in the loop transfer function makes frequency compensation a non-trivial exercise. However, the design of the control loop can be made easier if not simpler with the proper tools. The mathematical equation representing the small-signal output to control voltage transfer function may be reduced to a model which can be entered into any simulation software being used, such as SPICE, a widely used circuit simulation program. The equation for the modulator-power mesh portion of the control loop in the boost converter may be expressed as:

$$\frac{V_O}{(1-D)}\left[1 - \frac{sL}{(1-D)^2 R_O}\right]\frac{1}{V_m}$$

Similarly, the equation for the boost-buck converter may be written as:

$$\frac{V_O}{D(1-D)}\left[1 - \frac{sDL}{(1-D)^2 R_O}\right]\frac{1}{V_m}$$

where:

D = Duty cycle
L = Inductance
R_O = Load resistance
V_m = Internal reference voltage = 2.5V

A model representing these equations is shown in Figure 8. Combined with the output filter shown in Figure 9, and the error amp shown in Figure 7, a computer simulation can be used to determine the optimum combination of components for a stable design that still provides adequate response to external disturbances.

Note that in the output filter, the effective primary inductance and inductor series resistance are multiplied by $1/(1-D)^2$. For the boost converter example, a combination of lead compensation provided by C5 and lag compensation provided by R6 and C4 gave the desired response. The buck-boost converter has identical lag compensation provided by C6 and R8; however, the lead compensation requires a series combination of C7 and R9 which appears across R3 (Figure 2) within the ICL7680. Both R5 and R7 load the output of each error amplifier, reducing the DC gain. The output resistance of the error amp is given by R_B in Figure 7 as 4.6 MΩ. Finally, the C8/R11 and C9/R12 networks at both outputs provide damping which lessens the severity of the LC phase rolloff.

Line and Load Regulation

Line and load regulation can be approximated by 1/(loop gain) which for the boost converter can be expressed as:

$$\frac{2(1-D)}{a_o}$$

For the buck-boost converter, the expression becomes:

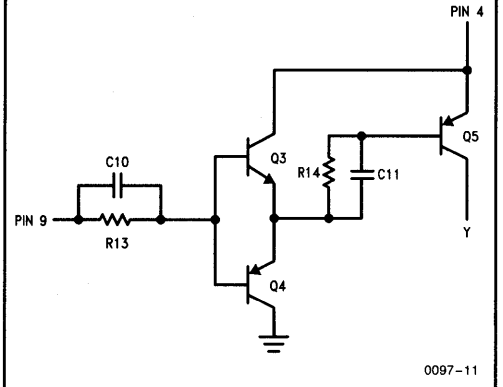
$$\frac{2D(1-D)}{a_o}$$

where: a_o = error amp gain
= $Gm_2 (R_B \parallel R_{EXT})$
= (0.66E-3) (4.6 Meg ∥ R_{EXT}), see Figure 7.

A value of around 0.2% is typical for the system shown in Figure 4.

Discontinuous Conduction

As stated earlier, the above analysis assumes continuous mode conduction where the inductor current never falls to zero. The converter can also be operated in what is called discontinuous conduction mode where the inductor current becomes zero for a portion of the clock cycle. This can occur from either a light load current or small inductor value or a combination of both. The advantage of this mode of operation is that the order of the system is reduced by one giving a single pole response, thereby easing loop stability design. The disadvantage is a higher input current surge and more severe ripple problems at the input and output, particularly with high ESR capacitors. An example of a system configuration for the discontinuous case is shown in Figure 3.

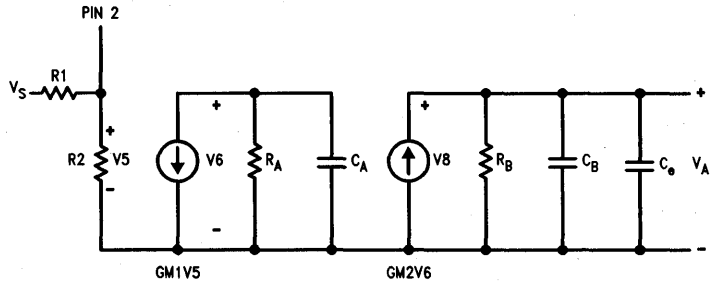


R13: 220Ω Q3: 2N2222A
R14: 100Ω Q4: 2N2907A
C10: 470 pF Q5: 2N3467 or 2N5022
C11: 100 pF f_{max} = mid frequency

This configuration can be used to extend operation of the −15V supply to 100 mA.

Figure 6: Configuration to Replace Q2 In Figures 3 and 4

NOTE: All typical values have been characterized but are not tested.



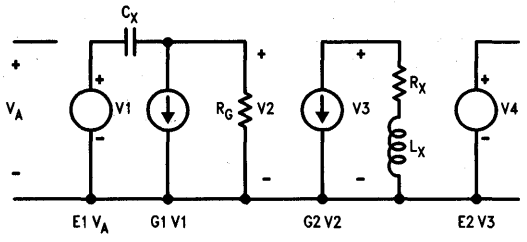
Valid for frequencies < 200 kHz

GM1 = 1
GM2 = 0.66×10^{-3}
R1 = 138 kΩ
R2 = 12.5 kΩ

R_A = 1Ω
C_A = 0.17 μF
R_B = 4.6 MΩ
C_B = 4 pF

C_e = Package capacitance + external loading capacitance

Figure 7: Error Amp Model



$$\frac{V4}{V_A} = \frac{E1 \times E2 \times G1 \times G2 \times RG \left[1 - s\frac{C_X}{G1}\right]\left(R_x + sL_X\right)}{1 + s\,R_G\,C_X}$$

$R_G = G1 = R_X = G2 = E2 = 1$

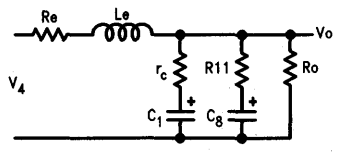
$$C_X = L_X = \frac{L}{(1-D)^2\,R_O} \quad \text{Boost}$$

$$C_X = L_X = \frac{D \times L}{(1-D)^2\,R_O} \quad \text{Buck-boost}$$

$$E1 = \frac{V_O}{(1-D)} \times \frac{1}{V_m} \quad \text{Boost}$$

$$E1 = \frac{V_O}{D(1-D)} \times \frac{1}{V_m} \quad \text{Buck-boost}$$

Figure 8: Control Loop Model



$$R_e = \frac{R_s + D \times R_t + (1-D)\,R_d + D\,(1-D)\,r_C}{(1-D)^2}$$

$$L_e = \frac{L}{(1-D)^2}$$

R_S = Inductor Series Resistance
R_t = MOSFET "ON" Resistance
R_d = Diode "ON" Resistance
r_C = Capacitor Series Resistance

Figure 9: Output Filter Model

NOTE: All typical values have been characterized but are not tested.

ICL8211/ICL8212
Programmable Voltage Detectors

GENERAL DESCRIPTION

The Harris ICL8211/8212 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

Specifically, the ICL8211 provides a 7mA current limited output sink when the voltage applied to the 'THRESHOLD' terminal is less than 1.15 volts (the internal reference). The ICL8212 requires a voltage in excess of 1.15 volts to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

FEATURES

- **High Accuracy Voltage Sensing and Generation: Internal Reference 1.15 Volts Typical**
- **Low Sensitivity to Supply Voltage and Temperature Variations**
- **Wide Supply Voltage Range: Typ. 1.8 to 30 Volts**
- **Essentially Constant Supply Current Over Full Supply Voltage Range**
- **Easy to Set Hysteresis Voltage Range**
- **Defined Output Current Limit — ICL8211 High Output Current Capability — ICL8212**

APPLICATIONS

- **Low Voltage Sensor/Indicator**
- **High Voltage Sensor/Indicator**
- **Non Volatile Out-of-Voltage Range Sensor/Indicator**
- **Programmable Voltage Reference or Zener Diode**
- **Series or Shunt Power Supply Regulator**
- **Fixed Value Constant Current Source**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL8211CPA	0°C to +70°C	8 lead Mini DIP
ICL8211CBA	0°C to +70°C	8 lead SOIC
ICL8211CTY	0°C to +70°C	TO-99 Can
ICL8211MTY*	−55°C to +125°C	TO-99 Can
ICL8212CPA	0°C to +70°C	8 lead Mini DIP
ICL8212CBA	0°C to +70°C	8 lead SOIC
ICL8212CTY	0°C to +70°C	TO-99 Can
ICL8212MTY*	−55°C to +125°C	TO-99 Can

* Add /883B to part number if 883B processing is required.

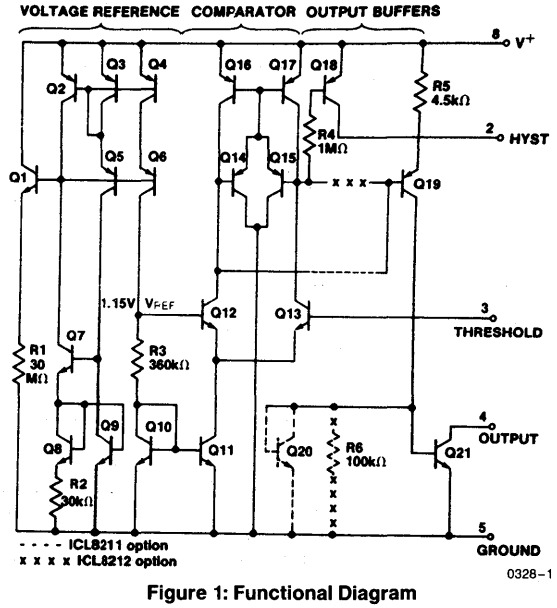


Figure 1: Functional Diagram

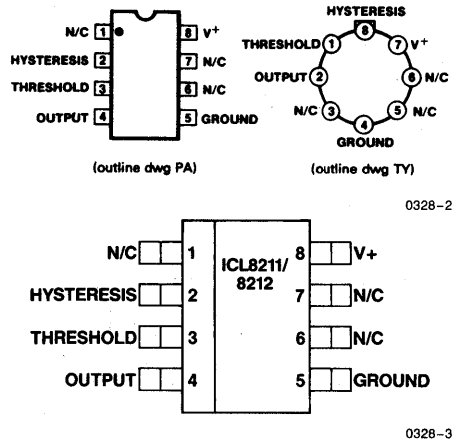


Figure 2: Pin Configurations

303200-004

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ..... −0.5 to +30 volts
Output Voltage ..... −0.5 to +30 volts
Hysteresis Voltage ..... +0.5 to −10 volts
Threshold Input Voltage .....
+30 to −5 volts with respect to GROUND and
+0 to −30 volts with respect to V^+
Current into Any Terminal ..... ±30mA

Power Dissipation (Note 1 & 2) 300mW
Operating Temperature Range:
ICL8211M/8212M ..... −55°C to +125°C
ICL8211C/8212C ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE 1: Rating applies for case temperatures to 125°C to ICL8211MTY/8212MTY products. Derate linearly at −10mW/°C for ambient temperatures above 100°C.

NOTE 2: Derate linearly above 50°C by −10mW/°C for ICL8211C/8212C products. The threshold input voltage may exceed +7 volts for short periods of time. However for continuous operation this voltage must be maintained at a value less than 7 volts.

ELECTRICAL CHARACTERISTICS ($V^+ = 5V$, $T_A = 25°C$ unless otherwise specified)

Symbol	Parameter	Test Conditions		ICL8211			ICL8212			Units
				Min	Typ	Max	Min	Typ	Max	
I^+	Supply Current	$2.0 < V^+ < 30$ $V_{TH} = 1.3V$ $V_{TH} = 0.9V$		 10 50	 22 140	 40 250	 50 10	 110 20	 250 40	 µA µA
V_{TH}	Threshold Trip Voltage	$I_{OUT} = 4mA$ $V_{OUT} = 2V$	$V^+ = 5V$ $V^+ = 2V$ $V^+ = 30V$	0.98 0.98 1.00	1.15 1.145 1.165	1.19 1.19 1.20	1.00 1.00 1.05	1.15 1.145 1.165	1.19 1.19 1.20	V V V
V_{THP}	Threshold Voltage Disparity Between Output & Hysteresis Output	$I_{OUT} = 4mA$ $I_{HYST} = 7\mu A$	$V_{OUT} = 2V$ $V_{HYST} = 3V$		−8.0			−0.5		mV
V_{SUPPLY}	Guaranteed Operating Supply Voltage Range (Note 5)	+25°C 0 to +70°C		2.0 2.2		30 30	2.0 2.2		30 30	V V
V_{SUPPLY}	Minimum Operating Supply Voltage Range	+25°C +125°C −55°C			1.8 1.4 2.5			1.8 1.4 2.5		V V V
$\Delta V_{TH}/\Delta T$	Threshold Voltage Temperature Coefficient	$I_{OUT} = 4mA$ $V_{OUT} = 2V$			±200			±200		ppm/°C
$\Delta V_{TH}/\Delta V^+$	Variation of Threshold Voltage with Supply Voltage	$\Delta V^+ = 10\%$ at $V^+ = 5V$			1.0			1.0		mV
I_{TH}	Threshold Input Current	$V_{TH} = 1.15V$ $V_{TH} = 1.00V$			100 5	250		100 5	250	nA nA
I_{OLK}	Output Leakage Current	$V_{OUT} = 30V$ $V_{OUT} = 30V$ $V_{OUT} = 5V$ $V_{OUT} = 5V$	$V_{TH} = 0.9V$ $V_{TH} = 1.3V$ $V_{TH} = 0.9V$ $V_{TH} = 1.3V$			 10 1			10 1 	µA µA µA µA
V_{SAT}	Output Saturation Voltage	$I_{OUT} = 4mA$	$V_{TH} = 0.9V$ $V_{TH} = 1.3V$		0.17	0.4		0.17	0.4	V V
I_{OH}	Max Available Output Current	(Note 3 & 4) $V_{OUT} = 5V$	$V_{TH} = 0.9V$ $V_{TH} = 1.3V$	4	7.0	12	 15	 35		mA mA
I_{LHYS}	Hysteresis Leakage Current	$V^+ = 10V$ $V_{HYST} = GROUND$	$V_{TH} = 1.0V$			0.1			0.1	µA
$V_{HYS\ (max)}$	Hysteresis Sat Voltage	$I_{HYST} = -7\mu A$ measured with respect to V^+	$V_{TH} = 1.3V$		−0.1	−0.2		−0.1	−0.2	V
$I_{HYS\ (max)}$	Max Available Hysteresis Current		$V_{TH} = 1.3V$	−15	−21		−15	−21		µA

NOTES: 3. The maximum output current of the ICL8211 is limited by design to 15mA under any operating conditions. The output voltage may be sustained at any voltage up to +30V as long as the maximum power dissipation of the device is not exceeded.

4. The maximum output current of the ICL8212 is not defined, and systems using the ICL8212 must therefore ensure that the output current does not exceed 30mA and that the maximum power dissipation of the device is not exceeded.

5. Threshold Trip Voltage is 0.80V(min) to 1.30V(max). At $I_{OUT} = 3$ mA.

NOTE: All typical values have been characterized but are not tested.

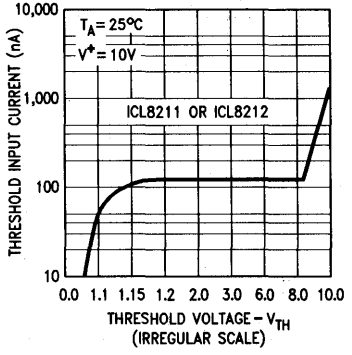
ELECTRICAL CHARACTERISTICS ICL8211MTY/8212MTY ($V^+ = 5V$, $T_A = -55°C$ to $+125°C$)

Symbol	Parameter	Test Conditions	ICL8211			ICL8212			Units
			Min	Typ	Max	Min	Typ	Max	
I^+	Supply Current	$2.8 < V^+ < 30$ $V_T = 1.3V$ $V_T = 0.8V$			 100 350			 350 100	 μA μA
V_{TH}	Threshold Trip Voltage	$I_{OUT} = 2mA$ $V_{OUT} = 2V$ $V^+ = 2.8V$ $V^+ = 30V$	 0.80 0.80		 1.30 1.30	 0.80 0.80		 1.30 1.30	 V V
V_{SUPPLY}	Guaranteed Operating Supply Voltage Range	(Note 5)	2.8		30	2.8		30	V
I_{TH}	Threshold Input Current	$V_{TH} = 1.15V$			400			400	nA
I_{OLK}	Output Leakage Current	$V_{OUT} = 30V$ $V_{TH} = 0.8V$ $V_{TH} = 1.3V$			 20			20	μA μA
V_{SAT}	Output Saturation Voltage	$I_{OUT} = 3mA$ $V_{TH} = 0.8V$ $V_{TH} = 1.3V$			0.5			 0.5	V V
I_{OH}	Max Available Output Current	(Note 3 & 4) $V_{TH} = 0.8V$ $V_{OUT} = 5V$ $V_{TH} = 1.3V$	3		15	 9			mA mA
I_{LHYS}	Hysteresis Leakage Current	$V^+ = 10V$ $V_{TH} = 0.8V$ $V_{HYST} = GROUND$			0.2			0.2	μA
$V_{HYS(max)}$	Hysteresis Saturation Voltage	$I_{HYST} = -7\mu A$ $V_{TH} = 1.3V$ measured with respect to V^+			0.3			0.3	V
$I_{HYS(max)}$	Max Available Hysteresis Current	$V_{TH} = 1.3V$	10			10			μA

NOTE: All typical values have been characterized but are not tested.

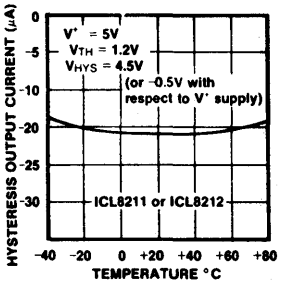
TYPICAL PERFORMANCE CHARACTERISTICS COMMON TO ICL8211 AND ICL8212

THRESHOLD INPUT CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



0328-4

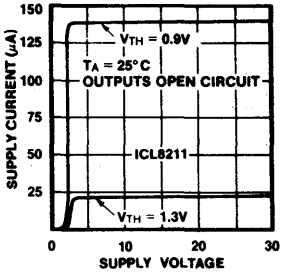
HYSTERESIS OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE



0328-5

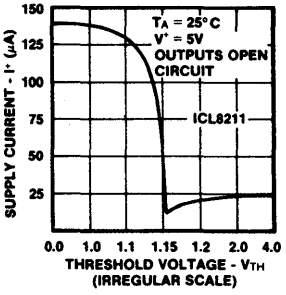
TYPICAL PERFORMANCE CHARACTERISTICS ICL8211 ONLY

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



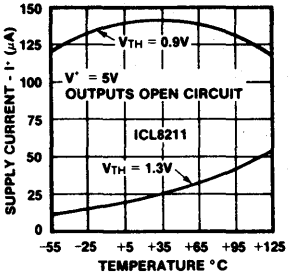
0328-6

SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



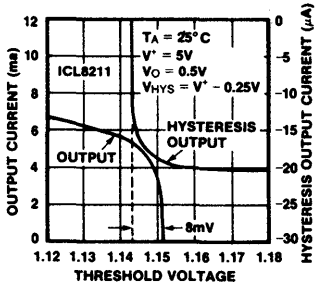
0328-7

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



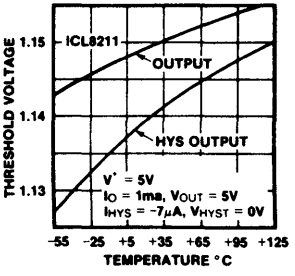
0328-8

OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



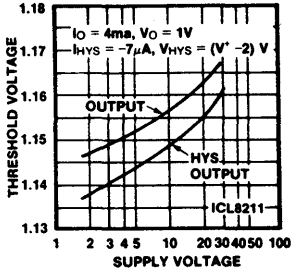
0328-9

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



0328-10

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE

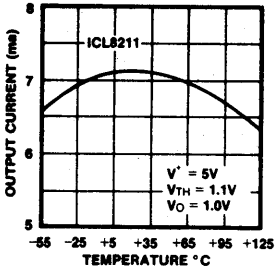


0328-11

NOTE: All typical values have been characterized but are not tested.

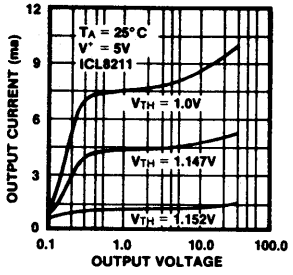
TYPICAL PERFORMANCE CHARACTERISTICS ICL8211 ONLY (Continued)

OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE



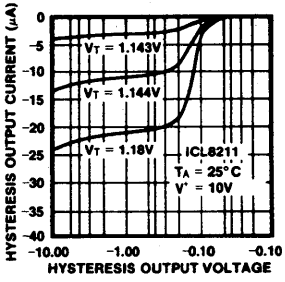
0328-12

OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



0328-13

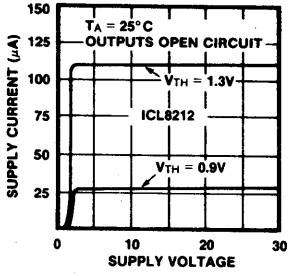
HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



0328-23

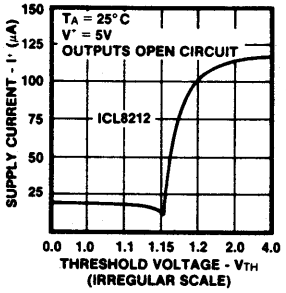
TYPICAL PERFORMANCE CHARACTERISTICS ICL8212 ONLY

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



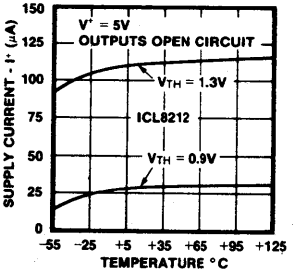
0328-15

SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



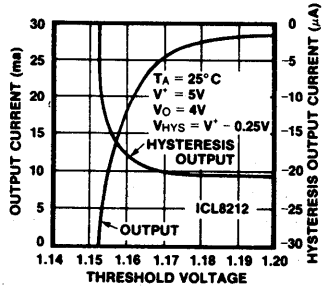
0328-16

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



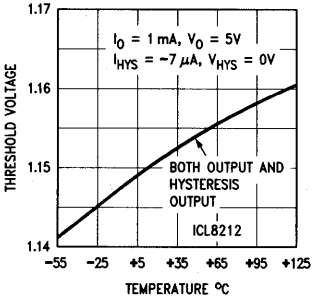
0328-17

OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



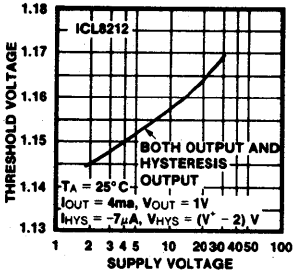
0328-18

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



0328-19

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE

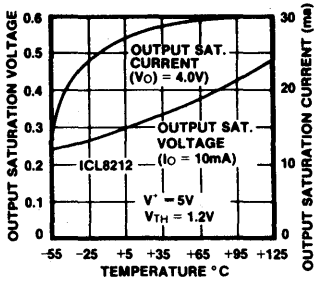


0328-20

NOTE: All typical values have been characterized but are not tested.

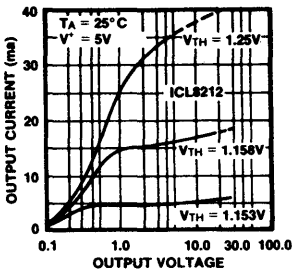
TYPICAL PERFORMANCE CHARACTERISTICS ICL8212 ONLY (Continued)

OUTPUT SATURATION VOLTAGE AND CURRENT AS A FUNCTION OF TEMPERATURE



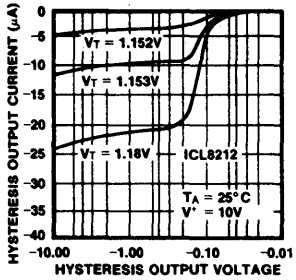
0328-21

OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



0328-22

HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



0328-14

DETAILED DESCRIPTION

The ICL8211 and ICL8212 use standard linear bipolar integrated circuit technology with high value thin film resistors which define extremely low value currents.

Components Q_1 thru Q_{10} and R_1, R_2 and R_3 set up an accurate voltage reference of 1.15 volts. This reference voltage is close to the value of the bandgap voltage for silicon and is highly stable with respect to both temperature and supply voltage. The deviation from the bandgap voltage is necessary due to the negative temperature coefficient of the thin film resistors (−5000 ppm per °C).

Components Q_2 thru Q_9 and R_2 make up a constant current source; Q_2 and Q_3 are identical and form a current mirror. Q_8 has 7 times the emitter area of Q_9, and due to the current mirror, the collector currents of Q_8 and Q_9 are forced to be equal and it can be shown that the collector current in Q_8 and Q_9 is

$$I_C\ (Q_8 \text{ or } Q_9) = \frac{1}{R_2} \times \frac{kT}{q} \ln 7$$

or approximately 1µA at 25°C

Where k = Boltzman's constant

q = charge on an electron

and T = absolute temperature in °K

Transistors Q_5, Q_6, and Q_7 assure that the V_{CE} of Q_3, Q_4, and Q_9 remain constant with supply voltage variations. This ensures a constant current supply free from variations.

The base current of Q_1 provides sufficient start up current for the constant source; there being two stable states for this type of circuit — either ON as defined above, or OFF if no start up current is provided. Leakage current in the transistors is not sufficient in itself to guarantee reliable startup.

Q_4 is matched to Q_3 and Q_2; Q_{10} is matched to Q_9. Thus the I_C and V_{BE} of Q_{10} are identical to that of Q_9 or Q_8. To generate the bandgap voltage, it is necessary to sum a voltage equal to the base emitter voltage of Q_9 to a voltage proportional to the difference of the base emitter voltages of two transistors Q_8 and Q_9 operating at two current densities.

$$\text{Thus } 1.15 = V_{BE}\ (Q_9 \text{ or } Q_{10}) + \frac{R_3}{R_2} \times \frac{kT}{q} \ln 7$$

$$\text{which provides } \frac{R_3}{R_2} = 12 \text{ (approx.)}$$

The total supply current consumed by the voltage reference section is approximately 6µA at room temperature. A voltage at the THRESHOLD input is compared to the reference 1.15 volts by the comparator consisting of transistors Q_{11} thru Q_{17}. The outputs from the comparator are limited to two diode drops less than V^+ or approximately 1.1 volts. Thus the base current into the hysteresis output transistor is limited to about 500nA and the collector current of Q_{19} to 100µA.

In the case of the ICL8211, Q_{21} is proportioned to have 70 times the emitter area of Q_{20} thereby limiting the output current to approximately 7mA, whereas for the ICL8212 almost all the collector current of Q_{19} is available for base drive to Q_{21}, resulting in a maximum available collector current of the order of 30mA. It is advisable to externally limit this current to 25mA or less.

APPLICATIONS

The ICL8211 and ICL8212 are similar in many respects, especially with regard to the setup of the input trip conditions and hysteresis circuitry. The following discussion describes both devices, and where differences occur they are clearly noted.

General Information

THRESHOLD INPUT CONSIDERATIONS

Although any voltage between −5V and V^+ may be applied to the THRESHOLD terminal, it is recommended that the THRESHOLD voltage does not exceed about +6 volts since above that voltage the threshold input current increases sharply. Also, prolonged operation above this voltage will lead to degradation of device characteristics.

NOTE: All typical values have been characterized but are not tested.

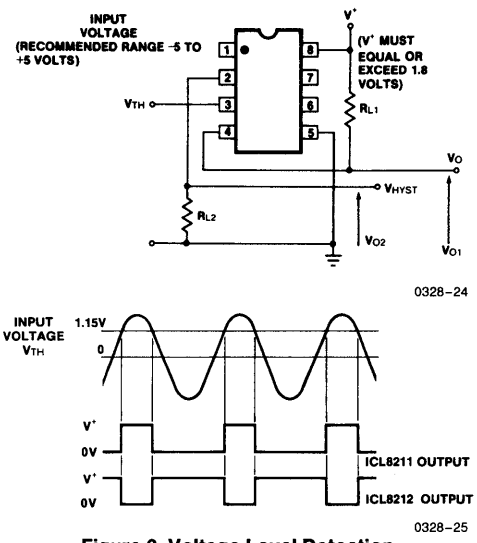


Figure 3: Voltage Level Detection

The outputs change states with an input THRESHOLD voltage of approximately 1.15 volts. Input and output waveforms are shown in Figure 3 for a simple 1.15 volt level detector.

The HYSTERESIS output is a low current output and is intended primarily for input threshold voltage hysteresis applications. If this output is used for other applications it is suggested that output currents be limited to 10μA or less.

The regular OUTPUT's from either the ICL8211 or ICL8212 may be used to drive most of the common logic families such as TTL or C-MOS using a single pullup resistor. There is a guaranteed TTL fanout of 2 for the ICL8211 and 4 for the ICL8212.

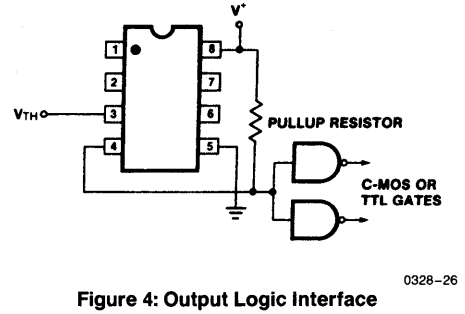


Figure 4: Output Logic Interface

A principal application of the ICL8211 is voltage level detection, and for that reason the OUTPUT current has been limited to typically 7mA to permit direct drive of an LED connected to the positive supply without a series current limiting resistor.

On the other hand the ICL8212 is intended for applications such as programmable zener references, and voltage regulators where output currents well in excess of 7mA are desirable. Therefore, the output of the ICL8212 is not current limited, and if the output is used to drive an LED, a series current limiting resistor must be used.

In most applications an input resistor divider network may be used to generate the 1.15V required for V_{TH}. For high accuracy, currents as large as 50μA may be used, however for those applications where current limiting may be desirable, (such as when operating from a battery) currents as low as 6μA may be considered without a great loss of accuracy. 6μA represents a practical minimum, since it is about this level where the device's own input current becomes a significant percentage of that flowing in the divider network.

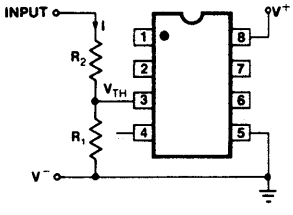


Figure 5: Input Resistor Network Considerations

Case 1. High accuracy required, current in resistor network unimportant Set $I = 50\mu A$ for $V_{TH} = 1.15$ volts $\therefore R_1 \rightarrow 20k\Omega$.

Case 2. Good accuracy required, current in resistor network important Set $I = 7.5\mu A$ for $V_{TH} = 1.15$ volts $\therefore R_1 \rightarrow 150k\Omega$.

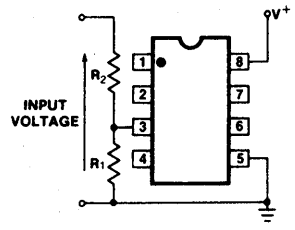
SETUP PROCEDURES FOR VOLTAGE LEVEL DETECTION

Case 1. Simple voltage detection — no hysteresis

Unless an input voltage of approximately 1.15 volts is to be detected, resistor networks will be used to divide or multiply the unknown voltage to be sensed. Figure 7 shows procedures on how to set up resistor networks to detect INPUT VOLTAGES of any magnitude and polarity.

For supply voltage level detection applications the input resistor network is connected across the supply terminals as shown in Figure 8.

NOTE: All typical values have been characterized but are not tested.



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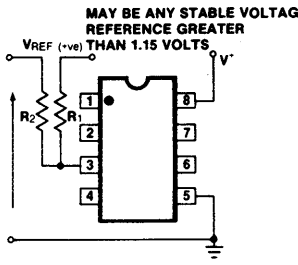
Input voltage to change the output states

$$= \frac{(R_1 + R_2)}{R_1} \times 1.15 \text{ volts}$$

Figure 6: Range of Input Voltage Greater Than + 1.15 Volts



0328-29

Range of input voltage less than + 1.15 volts.
Input voltage to change the output states

$$= \frac{(R_1 + R_2) \times 1.15}{R_1} - \frac{R_2 V_{REF}}{R_1}$$

Figure 7: Input Resistor Network Setup Procedures

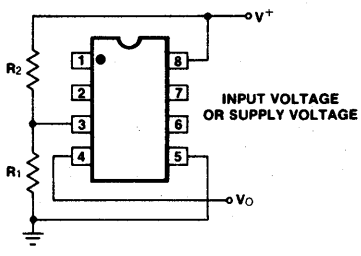


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Figure 8: Combined Input and Supply Voltages

Case 2. Use of the HYSTERESIS function

The disadvantage of the simple detection circuits is that there is a small but finite input range where the outputs are neither totally 'ON' nor totally 'OFF'. The principle behind hysteresis is to provide positive feedback to the input trip point such that there is a voltage difference between the input voltage necessary to turn the outputs ON and OFF.

The advantage of hysteresis is especially apparent in electrically noisy environments where simple but positive voltage detection is required. Hysteresis circuitry, however, is not limited to applications requiring better noise performance but may be expanded into highly complex systems with multiple voltage level detection and memory applications — refer to specific applications section.

There are two simple methods to apply hysteresis to a circuit for use in supply voltage level detection. These are shown in Figure 9.

The circuit (a) of Figure 9 requires that the full current flowing in the resistor network be sourced by the HYSTERESIS output, whereas for circuit (b) the current to be sourced by the HYSTERESIS output will be a function of the ratio of the two trip points and their values. For low values of hysteresis, circuit (b) is to be preferred due to the offset voltage of the hysteresis output transistor.

A third way to obtain hysteresis (ICL8211 only) is to connect a resistor between the OUTPUT and the THRESHOLD terminals thereby reducing the total external resistance between the THRESHOLD and GROUND when the OUTPUT is switched on.

Practical Applications

a) Low Voltage Battery Indicator (Figure 10)

This application is particularly suitable for portable or remote operated equipment which requires an indication of a depleted or discharged battery. The quiescent current taken by the system will be typically 35μA which will increase to 7mA when the lamp is turned on. R_3 will provide hysteresis if required.

b) Non-Volatile Low Voltage Detector (Figure 11)

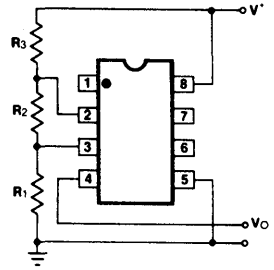
In this application the high trip voltage V_{TR2} is set to be above the normal supply voltage range. On power up the initial condition is A. On momentarily closing switch S_1 the operating point changes to B and will remain at B until the supply voltage drops below V_{TR1}, at which time the output will revert to condition A. Note that state A is always retained if the supply voltage is reduced below V_{TR1} (even to zero volts) and then raised back to V_{NOM}.

c) Non-Volatile Power Supply Malfunction Recorder (Figures 12 and 13)

In many systems a transient or an extended abnormal (or absence of a) supply voltage will cause a system failure. This failure may take the form of information lost in a volatile semiconductor memory stack, a loss of time in a timer or even possible irreversible damage to components if a supply voltage exceeds a certain value.

It is, therefore, necessary to be able to detect and store the fact that an **out-of-operating range** supply voltage condition has occurred, even in the case where a supply voltage may have dropped to zero. Upon power up to the normal operating voltage this record must have been retained and easily interrogated. This could be important in the case of a transient power failure due to a faulty component or intermittent power supply, open circuit, etc., where direct observation of the failure is difficult.

NOTE: All typical values have been characterized but are not tested.



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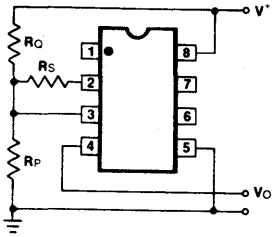
Low trip voltage

$$V_{TR1} = \left[\frac{(R_1 + R_2 \times 1.15}{R_1)} + 0.1\right] \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_1 + R_2 + R_3)}{R_1} \times 1.15 \text{ volts}$$



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Low trip voltage

$$V_{TR1} = \left[\frac{R_Q R_S}{(R_Q + R_S)} + RP\right] \times \frac{1}{R_P} \times 1.15 \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_P + R_Q)}{R_P} \times 1.15 \text{ volts}$$

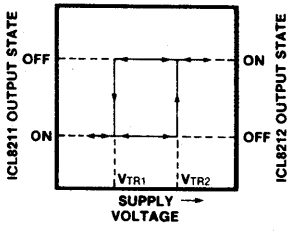

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Figure 9: Two alternative voltage detection circuits employing hysteresis to provide pairs of well defined trip voltages.

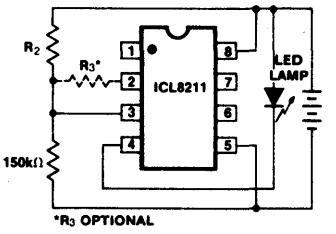

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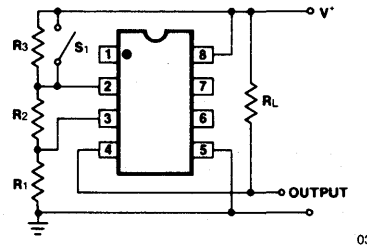
Figure 10: Low Voltage Battery Indicator



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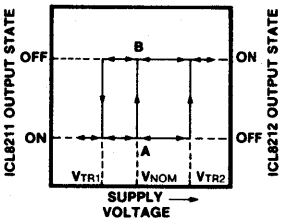
(a)



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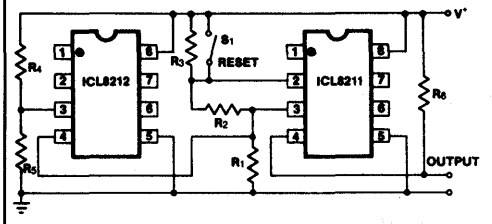
(b)

Figure 11: Non-Volatile Low Voltage Indicator



0328-37

Figure 12: Non-Volatile Power Supply Malfunction Recorder

2 POWER CONTROL CIRCUITS

NOTE: All typical values have been characterized but are not tested.

A simple circuit to record an out of range voltage excursion may be constructed using an ICL8211, an ICL8212 plus a few resistors. This circuit will operate to 30 volts without exceeding the maximum ratings of the I.C.'s. The two voltage limits defining the in range supply voltage may be set to any value between 2.0 and 30 volts.

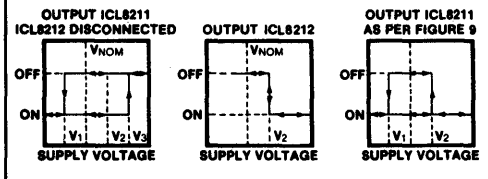


Figure 13: Output States of the ICL8211 and ICL8212 as a Function of the Supply Voltage

The ICL8212 is used to detect a voltage, V_2, which is the upper voltage limit to the operating voltage range. The ICL8211 detects the lower voltage limit of the operating voltage range, V_1. Hysteresis is used with the ICL8211 so that the output can be stable in either state over the operating voltage range V_1 to V_2 by making V_3 — the upper trip point of the ICL8211 much higher in voltage than V_2.

The output of the ICL8212 is used to force the output of the ICL8211 into the ON state above V_2. Thus there is no value of the supply voltage that will result in the output of the ICL8211 changing from the ON state to the OFF state. This may be achieved only by shorting out R_3 for values of supply voltage between V_1 and V_2.

d) Constant Current Sources (Figure 14)

The ICL8212 may be used as a constant current source of value of approximately 25μA by connecting the THRESHOLD terminal to GROUND. Similarly the ICL8211 will provide a 130μA constant current source. The equivalent parallel resistance is in the tens of megohms over the supply voltage range of 2 to 30 volts. These constant current sources may be used to provide biasing for various circuitry including differential amplifiers and comparators. See Typical Operating Characteristics for complete information.

e) Programmable Zener Voltage Reference (Figure 15)

The ICL8212 may be used to simulate a zener diode by connecting the OUTPUT terminal to the V_Z output and using a resistor network connected to the THRESHOLD terminal to program the zener voltage

$$V_{zener} = \frac{(R_1 + R_2)}{R_1} \times 1.15 \text{ volts.}$$

Since there is no internal compensation in the ICL8212 it is necessary to use a large capacitor across the output to prevent oscillation.

Zener voltages from 2 to 30 volts may be programmed and typical impedance values between 300μA and 25mA will range from 4 to 7Ω. The knee is sharper and occurs at a significantly lower current than other similar devices available.

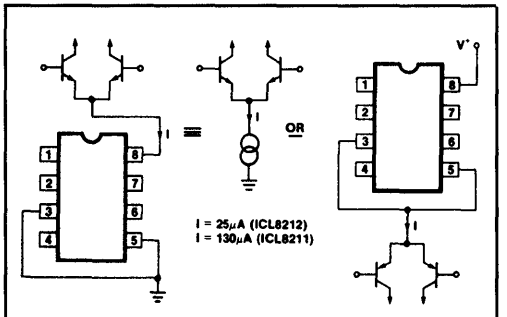


Figure 14: Constant Current Source Applications

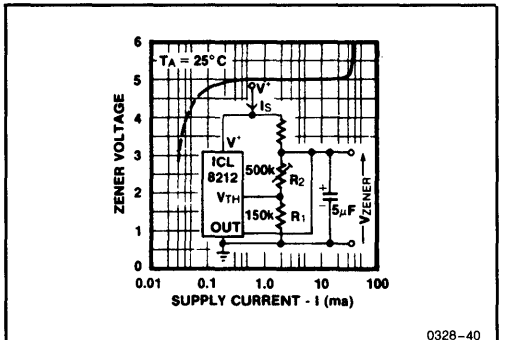


Figure 15: Programmable Zener Voltage Reference

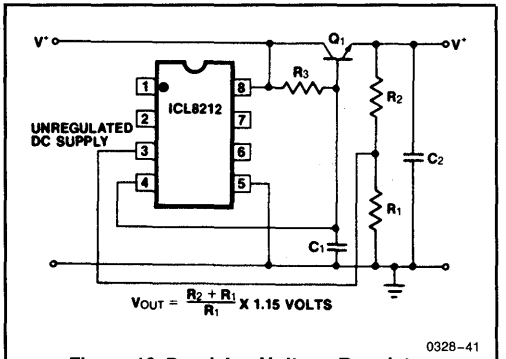


Figure 16: Precision Voltage Regulator

f) Precision Voltage Regulator (Figure 16)

The ICL8212 may be used as the controller for a highly stable series voltage regulator. The output voltage is simply programmed, using a resistor divider network R_1 and R_2. Two capacitors C_1 and C_2 are required to ensure stability since the ICL8212 is uncompensated internally.

NOTE: All typical values have been characterized but are not tested.

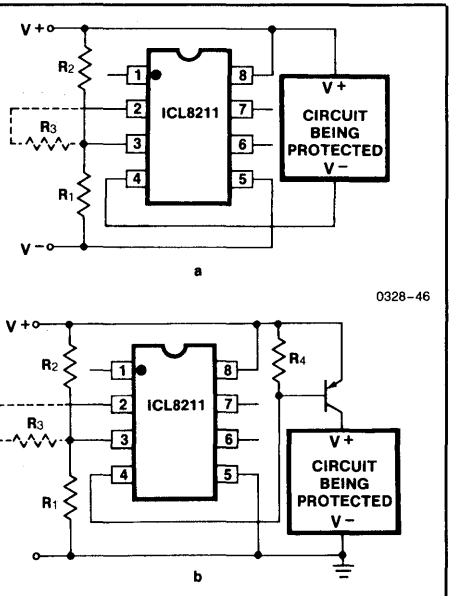


Figure 17: High Voltage Dump Circuits

This regulator may be used with lower input voltages than most other commercially available regulators and also consumes less power for a given output control current than any commercial regulator. Applications would therefore include battery operated equipment especially those operating at low voltages.

g) High Supply Voltage Dump Circuit (Figure 17)

In many circuit applications it is desirable to remove the power supply in the case of high voltage overload. For circuits consuming less than 5mA this may be achieved using an ICL8211 driving the load directly. For higher load currents it is necessary to use an external pnp transistor or darlington pair driven by the output of the ICL8211. Resistors R_1 and R_2 set up the disconnect voltage and R_3 provides optional voltage hysteresis if so desired.

h) Frequency Limit Detector (Figure 18)

Simple frequency limit detectors providing a GO/NO-GO output for use with varying amplitude input signals may be conveniently implemented with the ICL8211/8212. In the application shown, the first ICL8212 is used as a zero crossing detector. The output circuit consisting of R_3, R_4 and C_2 results in a slow output positive ramp. The negative range is much faster than the positive range. R_5 and R_6 provide hysteresis so that under all circumstances the second ICL8212 is turned on for sufficient time to discharge C_3. The time constant of R_7 C_3 is much greater than R_4 C_2. Depending upon the desired output polarities for low and high input frequencies, either an ICL8211 or an ICL8212 may be used as the output driver.

This circuit is sensitive to supply voltage variations and should be used with a stabilized power supply. At very low frequencies the output will switch at the input frequency.

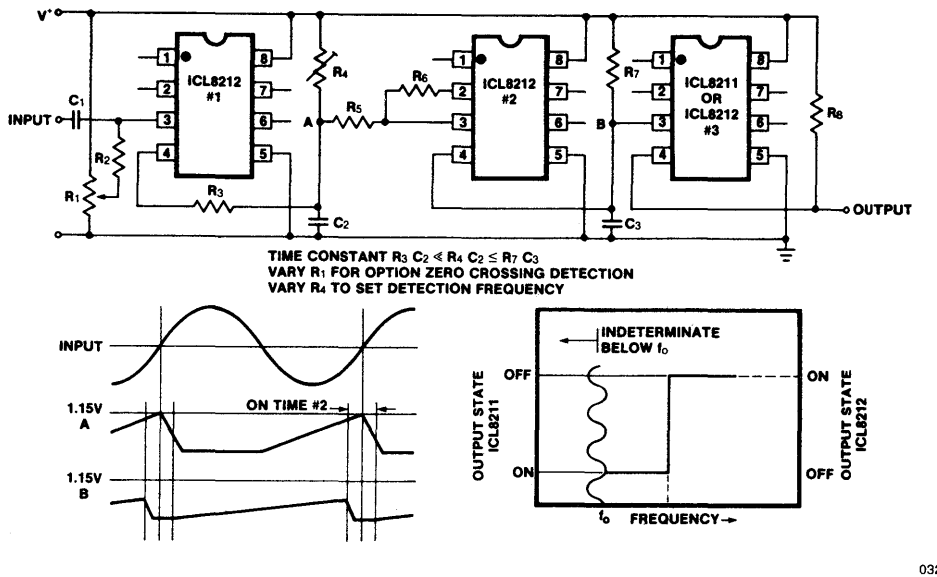
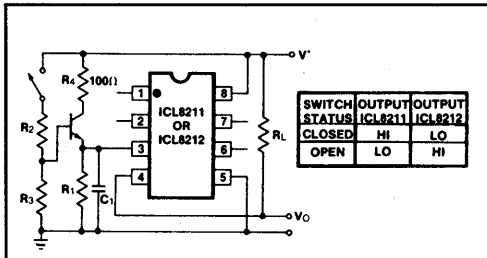


Figure 18: Frequency Limit Detector

NOTE: All typical values have been characterized but are not tested.

i) Switch Bounce Filter (Figure 19)

Single pole single throw (SPST) switches are less costly and more available than single pole double throw (SPDT) switches. SPST switches range from push button and slide types to calculator keyboards. A major problem with the use of switches is the mechanical bounce of the electrical contacts on closure. Contact bounce times can range from a fraction of a millisecond to several tens of milliseconds depending upon the switch type. During this contact bounce time the switch may make and break contact several times. The circuit shown in Figure 19 provides a rapid charge up of C_1 to close to the positive supply voltage (V^+) on a switch closure and a corresponding slow discharge of C_1 on a switch break. By proportioning the time constant of R_1 C_1 to approximately the manufacturer's bounce time the output as terminal #4 of the ICL8211/8212 will be a single transition of state per desired switch closure.



SWITCH STATUS	OUTPUT ICL8211	OUTPUT ICL8212
CLOSED	HI	LO
OPEN	LO	HI

0328-44

Figure 19: Switch Bounce Filter

j) Low Voltage Power Disconnect (Figure 20)

There are some classes of circuits that require the power supply to be disconnected if the power supply voltage falls below a certain value. As an example, the National LM199 precision reference has an on chip heater which malfunctions with supply voltages below 9 volts causing an excessive device temperature. The ICL8212 may be used to detect a power supply voltage of 9 volts and turn the power supply off to the LM199 heater section below that voltage.

For further applications, see A027 "Power Supply Design using the ICL8211 and ICL8212."

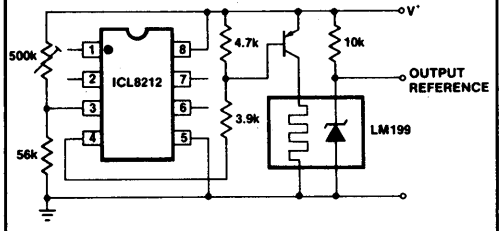


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Figure 20: Low Voltage Power Supply Disconnect

NOTE: All typical values have been characterized but are not tested.

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PRECISION: Min/Max Limits @ +25°C, Unless Otherwise Specified

DEVICE	OFFSET VOLTAGE (mV)	V_{IO} DRIFT (typ) (μV/°C)	BIAS CURRENT (nA)	OFFSET CURRENT (nA)	CMRR (dB)	PSRR (dB)	GBWP (MHz)	SLEW RATE (V/μs)	A_{VOL} (dB)	SUPPLY CURRENT (mA)
SINGLE										
ICL7605	0.005	0.01	1.5	-	100	110	-	-	90	5.0
ICL7606	0.005	0.01	1.5	-	100	110	-	-	90	5.0
ICL7650S	0.005	0.02	0.01	0.005	120	120	2.0	2.5	135	3.0
ICL7652S	0.005	0.01	0.03	0.040	120	120	0.5	1.0	135	2.5
HA-5127A	0.025	0.20	40.0	35.0	114	86	8.5	10.0	120	3.5
HA-5130	0.025	0.40	2.0	2.0	110	100	2.5	0.8	120	1.3
HA-5137A	0.025	0.20	40.0	35.0	114	100	63.0	20.0	120	3.5
HA-5147A	0.025	0.20	40.0	35.0	114	100	120.0	35.0	120	3.5
HA-5177A	0.025	0.10	2.0	2.0	120	110	2.0	0.8	134	1.7
HA-5177	0.060	0.20	6.0	6.0	110	110	1.4	0.8	126	1.7
HA-5135	0.075	0.40	4.0	4.0	106	94	2.5	0.8	120	1.7
HA-5137	0.100	0.40	80.0	75.0	100	96	63.0	20.0	117	3.5
HA-5147	0.100	0.40	80.0	75.0	100	96	140.0	35.0	117	3.5
CA3193A	0.200	1.00	20.0	5.0	110	100	1.2	0.25	110	3.5
HA-5170	0.300	2.0	0.01	0.03	85	85	8.0	8.0	109	2.5
CA3493	0.500	1.0	40.0	10.0	100	100	1.2	0.25	100	3.5
DUAL										
HA-5222	0.8	0.5	80	50	86	86	100.0	25.0	106	8.00
CA158A	2.0	7.0	50	10	70	65	1.0	0.5	94	1.20
HA-5102	2.0	3.0	200	75	86	86	60.0	3.0	100	5.00
HA-5112	2.0	3.0	200	75	86	86	60.0	20.0	100	5.00
ICL7621	2.0	10.0	0.05	0.03	76	80	1.4	1.6	80	2.50
CA3280	3.0	5.0	5000	700	80	86	9.0	125.0	94	4.80
CA258A	3.0	7.0	80	15	70	65	1.0	0.5	94	1.20
HA-5152	3.0	3.0	250	50	80	80	1.3	6.0	94	0.25
CA358A	3.0	7.0	100	30	65	65	1.0	0.5	88	1.20
TRIPLE										
ICL8023	6.0	-	30	10	70	76	0.27	0.16	94	0.09
ICL7631	10.0	-	0.05	0.03	70	80	1.40	1.60	80	2.50
QUAD										
HA-5134A	0.1	0.3	25.0	25.0	115	110	4.0	0.75	123	8.00
HA-5114	2.5	3.0	200.0	75.0	86	86	60.0	20.0	100	6.50
HA-5104	2.5	3.0	200.0	75.0	86	86	60.0	3.0	100	6.50
HA-5154	3.0	3.0	250.0	50.0	80	80	1.3	6.0	94	0.25
HA-5144	6.0	3.0	100.0	10.0	77	77	0.4	0.8	86	0.15
CA224	7.0	7.0	250.0	50.0	65	65	1.0	0.5	88	2.00
CA324	7.0	7.0	250.0	50.0	65	65	1.0	0.5	86	2.00
CA2902	7.0	7.0	250.0	50.0	65	65	1.0	0.5	86	2.00
CA3410A	8.0	10.0	0.03	0.01	80	80	5.4	10.0	86	10.0

Selection Guide

LOW BIAS CURRENT: Min/Max Limits @ +25°C, Unless Otherwise Specified

DEVICE	BIAS CURRENT (nA)	OFFSET CURRENT (nA)	OFFSET VOLTAGE (mV)	CM RANGE (±V)	A_{VOL} (dB)	GBWP (typ) (MHz)	SLEW RATE (typ) (V/μs)	CMRR (dB)	PSRR (dB)	CURRENT SUPPLY (mA)
SINGLE										
CA5420A	0.001	0.0005	5.0	3.7	85	0.5	0.5	75	75	0.50
HA-5180	0.001	0.0002	3.0	10.0	106	2.0	7.0	90	85	1.00
CA5420	0.002	0.0010	10.0	3.7	85	0.5	0.5	70	70	0.50
ICL8007A	0.004	0.002	30.0	10.0	86	1.0	6.0	86	75	6.00
CA3420	0.005	0.004	10.0	1.0	80	0.5	0.5	55	60	0.65
CA3420A	0.005	0.004	5.0	1.0	86	0.5	0.5	60	70	0.65
CA5130A	0.010	0.005	4.0	2.5	90	4.0	10.0	75	60	0.10
CA5160A	0.010	0.005	4.0	2.5	90	4.0	10.0	75	60	0.10
ICL7650	0.010	0.005	0.005	2.0	120	2.0	2.5	110	120	3.50
ICL7650S	0.010	0.005	0.005	3.5	135	2.0	2.5	120	120	3.00
CA5130	0.015	0.010	10.0	2.5	85	4.0	10.0	70	55	0.10
CA5160	0.015	0.010	10.0	2.5	85	4.0	10.0	70	55	0.10
ICL8007	0.020	0.005	20.0	10.0	86	1.0	6.0	70	70	5.20
CA3130A	0.030	0.020	5.0	10.0	94	15.0	9.0	80	80	15.00
DUAL										
CA5260	0.015	0.01	15.0	11.0	80	3.0	5.0	70	70	2.0
CA5260A	0.015	0.01	4.0	2.5	83	3.0	5.0	80	75	2.0
CA3260A	0.03	0.02	5.0	13.0	94	4.0	10.0	80	76	15.5
CA3240A	0.04	0.02	5.0	13.0	86	4.5	9.0	70	76	12.0
CA3240	0.05	0.03	15.0	12.0	86	4.5	9.0	70	76	12.0
CA3260	0.05	0.03	15.0	10.0	94	4.0	10.0	70	70	15.5
ICL7621	0.05	0.03	2.0	12.0	80	1.4	1.6	76	80	2.5
CA158A	50.0	10.0	2.0	13.0	94	1.0	0.5	70	65	1.2
TRIPLE										
ICL7631	0.05	0.03	10.0	4.2	80	1.40	1.60	70	80	2.50
ICL8023	30.0	10.0	6.0	12.0	94	0.27	0.16	70	76	0.09
QUAD										
CA5470	0.01	0.005	22.0	3.5	80	14.0	5.0	55	60	10.0
CA3410A	0.03	0.01	8.0	12.5	86	5.4	10.0	80	80	10.0
CA3410	0.04	0.03	15.0	12.5	86	5.4	10.0	70	70	12.0
ICL7641	0.05	0.03	10.0	4.2	80	1.4	1.60	70	80	2.5
ICL7642	0.05	0.03	10.0	4.2	80	1.4	1.60	70	80	2.5
HA-5134A	25.0	25.0	0.1	10.0	123	4.0	0.75	115	110	8.0

Selection Guide

WIDEBAND: Min/Max Limits @ +25°C, Unless Otherwise Specified

DEVICE	GBWP (typ) (MHz)	FPBW (MHz)	SLEW RATE (typ) (V/μs)	A_{VOL} (dB)	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA)
SINGLE										
HFA-0002	1000	4.50	250	98	10	0.7	700	105	90	15.0
HA-2539	600	8.70	600	80	10	10.0	20000	60	60	25.0
HA-2540	400	5.50	400	80	10	10.0	20000	60	60	25.0
HFA-0001	350	53.00	1000	43	1	15.0	50000	45	35	75.0
HFA-0005	300	22.00	420	43	1	15.0	50000	45	40	40.0
CA3450	170	6.56	330	60	1	15.0	350	50	60	35.0
HA-2548	150	1.91	120	114	5	0.9	50	80	86	18.0
HA-5190	150	5.00	200	83	5	5.0	15000	74	70	28.0
HA-5195	150	5.00	200	83	5	5.0	15000	74	70	28.0
HA-5147	140	0.45	35	117	10	0.1	80	100	96	3.5
HA-5147A	120	0.45	35	120	10	0.03	40	114	100	3.5
HA-2620	100	0.40	35	100	5	4.0	15	80	80	3.7
HA-2622	100	0.32	35	98	5	5.0	25	74	74	4.0
HA-2625	100	0.32	35	98	5	5.0	25	74	74	4.0
HA-5101	100	0.10	10	120	1	3.0	200	80	80	6.0
HA-5111	100	0.63	50	120	10	3.0	200	80	80	6.0
HA-5160	100	1.60	120	97	10	3.0	0.05	74	74	8.0
HA-5162	100	1.10	70	90	10	15.0	0.065	70	70	8.0
HA-5221	100	0.24	25	106	1	0.75	80	86	86	8.0
DUAL										
HA-5222	100.0	0.24	25	106	1	0.8	80.0	86	86	8.0
HA-5102	60.0	0.02	3	100	1	2.0	200.0	86	86	5.0
HA-5112	60.0	0.19	20	100	10	2.0	200.0	86	86	5.0
CA3280	9.0	1.99	125	94	1	3.0	5000.0	80	86	4.8
CA3280A	9.0	1.99	125	94	1	0.5	5000.0	94	94	4.8
CA3240	4.5	0.14	9	86	1	15.0	0.05	70	76	12.0
CA3240A	4.5	0.14	9	86	1	5.0	0.04	70	76	12.0
CA3260	4.0	0.16	10	94	1	15.0	0.05	70	70	15.5
CA3260A	4.0	0.16	10	94	1	5.0	0.03	80	76	15.5
CA5260	3.0	0.10	5	80	1	15.0	0.02	70	70	2.0
CA5260A	3.0	0.10	5	83	1	4.0	0.02	80	75	2.0
TRIPLE										
ICL7631	1.40	0.032	1.60	80	1	10.0	0.05	70	80	2.5
ICL8023	0.27	0.002	0.16	94	1	6.0	30.0	70	76	0.1
QUAD										
HA-5104	60.0	0.02	3.0	100	1	2.5	200.0	86	86	6.5
HA-5114	60.0	0.19	20.0	100	10	2.5	200.0	86	86	6.5
HA-2400	40.0	0.20	30.0	94	1	9.0	200.0	80	74	6.0
HA-2404	40.0	0.20	30.0	94	1	9.0	200.0	80	74	6.0
HA-2405	40.0	0.20	30.0	94	1	9.0	250.0	74	74	6.0
HA-2406	30.0	0.24	20.0	92	1	10.0	250.0	74	74	7.0
CA5470	14.0	0.01	5.0	80	1	22.0	0.01	55	60	10.0
CA3410	5.4	0.16	10.0	86	1	15.0	0.04	70	70	12.0
CA3410A	5.4	0.16	10.0	86	1	8.0	0.03	80	80	10.0
HA-5134A	4.0	0.02	0.8	123	1	0.1	25.0	115	110	8.0

Selection Guide

HIGH SLEW RATE: Min/Max Limits @ +25°C, Unless Otherwise Specified

DEVICE	SLEW RATE (typ) (V/μs)	GBWP (typ) (MHz)	FPBW (MHz)	A_{VOL} (dB)	MINIMUM STABLE GAIN	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	CMRR (dB)	PSRR (dB)	SUPPLY CURRENT (mA)
SINGLE										
HFA-0001	1000	350	4.5	43	1	15.0	50000	45	35	75.0
HA-2539	600	600	8.7	80	10	10.0	20000	60	60	25.0
HFA-0005	420	300	22.0	43	1	15.0	50000	45	40	40.0
HA-2540	400	400	5.5	80	10	10.0	20000	60	60	25.0
HA-2542	350	70	4.7	80	2	10.0	35000	70	70	35.0
CA3450	330	170	6.6	60	1	15.0	350	50	60	35.0
HA-2541	250	40	3.0	80	1	2.0	25000	70	70	40.0
HFA-0002	250	1000	4.5	98	10	0.7	700	105	90	15.0
HA-5190	200	150	5.0	83	5	5.0	15000	74	70	28.0
HA-5195	200	150	5.0	83	5	5.0	15000	74	70	28.0
HA-2529	150	20	2.1	80	3	5.0	200	80	80	6.0
HA-2544	150	50	3.2	71	1	15.0	15000	75	70	12.0
HA-2520	120	20	1.5	80	3	8.0	200	80	80	6.0
HA-2522	120	20	1.2	78	3	10.0	250	74	74	6.0
HA-2525	120	20	1.2	78	3	10.0	250	74	74	6.0
HA-2548	120	150	1.91	114	5	0.9	50	80	86	18.0
HA-5160	120	100	1.600	97	10	3	0.05	74	74	8
DUAL										
CA3280	125	9.0	1.99	94	1	3.0	5000	80	86	4.8
CA3280A	125	9.0	1.99	94	1	0.5	5000	94	94	4.8
HA-5222	25	100	0.24	106	1	0.75	80	86	86	8.0
HA-5112	20	60	0.19	100	10	2.0	200	86	86	5.0
CA3260	10	4.0	0.16	94	1	15.0	0.05	70	70	15.5
CA3260A	10	4.0	0.16	94	1	5.0	0.03	80	76	15.5
CA3240	9.0	4.5	0.14	86	1	15.0	0.05	70	76	12.0
CA3240A	9.0	4.5	0.14	86	1	5.0	0.04	70	76	12.0
HA-5152	6.0	1.3	0.10	94	1	3.0	250	80	80	0.25
CA5260A	5.0	3.0	0.10	83	1	4.0	0.015	80	75	2.0
TRIPLE										
ICL7631	1.6	1.4	0.032	80	1	10.0	0.05	70	80	2.5
ICL8023	0.16	0.27	0.002	94	1	6.0	30.0	70	76	0.09
QUAD										
HA-2400	30	40	0.20	94	1	9.0	200	80	74	6
HA-2404	30	40	0.20	94	1	9.0	200	80	74	6
HA-2405	30	40	0.20	94	1	9.0	250	74	74	6
HA-2406	20	30	0.24	92	1	10.0	250	74	74	7
HA-5114	20	60	0.191	100	10	2.5	200	86	86	6.5
CA3410	10	5.4	0.159	86	1	15.0	0.04	70	70	12
CA3410A	10	5.4	0.159	86	1	8.0	0.03	80	80	10
HA-5154	6.0	1.3	0.095	94	1	3.0	250	80	80	0.25
CA5470	5.0	14	0.01	80	1	22.0	0.01	55	60	10

Selection Guide

LOW POWER: Min/Max Limits @ +25°C, Unless Otherwise Specified

DEVICE	SUPPLY CURRENT (mA)	MAX V+, V- (±V)	SLEW RATE (typ) (V/µs)	GBWP (typ) (MHz)	CM RANGE (±V)	OUTPUT VOLTAGE SWING (±V)	OUTPUT CURRENT (mA)	OFFSET VOLTAGE (mV)	BIAS CURRENT (nA)	PSRR (dB)
SINGLE										
LM4250	0.011	18.0	-	-	13.5	12.0	-	5.0	10.0	74
CA3440	0.017	12.5	0.03	0.063	3.5	3.0	15.0	10.0	0.050	70
CA3440A	0.017	12.5	0.03	0.063	3.5	3.0	15.0	5.0	0.040	70
CA3078A	0.02	18.0	1.5	0.002	5.5	5.1	12.0	3.5	12.0	70
ICL7611A	0.02	9.0	0.02	0.044	4.4	4.9	8.0	2.0	0.05	80
ICL7612A	0.02	9.0	0.02	0.044	5.3	4.9	8.0	2.0	0.05	80
ICL8021	0.03	18.0	0.16	0.270	12.0	12.0	10.0	6.0	30.0	76
CA5130	0.10	8.0	10.0	4.0	2.5	2.5	4.0	10.0	0.015	55
CA5130A	0.10	8.0	10.0	4.0	2.5	2.5	4.0	4.0	0.010	60
CA5160	0.10	8.0	10.0	4.0	2.5	2.5	4.0	10.0	0.015	55
CA5160A	0.10	8.0	10.0	4.0	2.5	2.5	4.0	4.0	0.010	60
CA3078	0.13	7.0	1.5	0.002	5.5	5.1	12.0	4.5	170.0	70
HA-5141	0.15	17.5	0.8	0.40	10.0	10.0	4.5	6.0	100.0	77
HA-5151	0.25	17.5	6.0	1.30	10.0	10.0	4.5	3.0	250.0	80
CA3094	0.40	12.0	50.0	30.0	12.0	14.9	100.0	5.0	5000.0	70
CA3094A	0.40	18.0	50.0	30.0	12.0	14.9	100.0	5.0	5000.0	70
CA3094B	0.40	22.0	50.0	30.0	12.0	14.9	100.0	5.0	5000.0	70
DUAL										
HA-5142	0.15	17.5	0.8	0.4	10.0	10.0	4.5	6.0	100.0	77
ICL7621A	0.25	9.0	0.2	0.5	4.2	4.9	8.0	2.0	0.05	80
HA-5152	0.25	17.5	6.0	1.3	10.0	10.0	4.5	3.0	250.0	80
CA158A	1.2	13.0	0.5	1.0	13.0	13.0	20.0	2.0	50.0	65
CA258A	1.2	6.5	0.5	1.0	13.0	13.0	20.0	3.0	80.0	65
CA2904	1.2	6.5	0.5	1.0	13.0	13.0	20.0	7.0	250.0	50
CA258	1.2	6.5	0.5	1.0	13.0	13.0	20.0	5.0	150.0	65
CA358	1.2	13.0	0.5	1.0	13.0	13.0	20.0	7.0	250.0	65
CA158	1.2	16.0	0.5	1.0	13.0	13.0	20.0	5.0	150.0	65
CA358A	1.2	13.0	0.5	1.0	13.0	13.0	20.0	3.0	100.0	65
CA124	2.0	16.0	0.5	1.0	13.0	26.0	10.0	5.0	150.0	65
CA5260	2.0	8.0	5.0	3.0	2.5	3.0	1.75	15.0	0.015	70
TRIPLE										
ICL8023	0.09	18.0	0.16	0.27	12.0	12.0	10.0	6.0	30.0	76
ICL7631	2.50	9.0	1.60	1.40	4.2	4.5	8.0	10.0	0.05	80
QUAD										
ICL7642	0.02	9.0	0.02	0.04	4.2	4.5	8.0	10.0	0.05	80
HA-5144	0.15	17.5	0.8	0.4	10.0	10.0	4.5	6.0	100.0	77
HA-5154	0.25	17.5	6.0	1.3	10.0	10.0	4.5	3.0	250.0	80
CA224	2.00	16.0	0.5	1.0	13.0	13.0	10.0	7.0	250.0	65
CA324	2.00	16.0	0.5	1.0	13.0	13.0	10.0	7.0	250.0	65
ICL7641	2.50	9.0	1.6	1.4	4.2	4.5	8.0	10.0	0.05	80

Operational Amplifiers

CA101, CA201, CA301A, LM201*, LM301A*

May 1990

Operational Amplifiers

For Commercial, Industrial, and Military Applications

Features:

- *Short-circuit protection and latch-free operation*
- *Unity-gain phase compensation with a single 30-pF capacitor*
- *Replacement for industry types 101, 201, 301A*
- *CA301A Slew Rate (Summing ampl.) 10 V/μs*

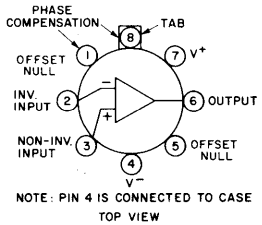
Applications:

- *Long-interval integrator*
- *Timers*
- *Sample-and-hold circuits*
- *Summing amplifiers*
- *Multivibrators*
- *Comparators*
- *Instrumentation*
- *AC/DC converters*
- *Inverting amplifiers*
- *Sine- & square-wave generators*
- *Capacitance multipliers & simulated inductors*

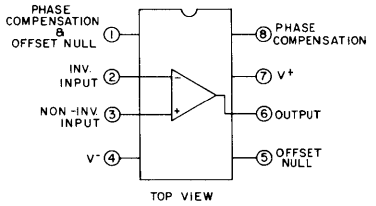
The CA101, CA201, and CA301A are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These types, which are externally phase compensated, permit a choice of operation for optimum high-frequency performance at a selected gain; unity-gain compensation can be obtained with a single 30-pF capacitor.

All types are available in 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads ("DIL-CAN", S suffix). The CA301A is also available in the 8-lead dual-in-line plastic package ("MINI-DIP", E suffix), and in chip form (H suffix).



(a) TO-5 Style package for all types
T-Suffix
S-Suffix



(b) Plastic package for CA301A
E-Suffix

Figure 1 - Functional diagrams.

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

Maximum Ratings, *Absolute Maximum Values at T_A = 25° C:*

DC SUPPLY VOLTAGE (Between V+ and V⁻ Terminals):
- CA101, CA201 ..... 44 V
- CA301A ..... 36 V

DC INPUT VOLTAGE ..... ±15 V
(For supply voltages less than ±15 V, the Input Voltage rating is equal to the DC Supply Voltage)

DIFFERENTIAL INPUT VOLTAGE ..... ±30 V

OUTPUT SHORT-CIRCUIT DURATION ..... Indefinite*

DEVICE DISSIPATION:
- UP TO T_A = 75° C ..... 500 mW
- Above T_A = 75° C Derate linearly at ..... 6.67 mW/° C

AMBIENT TEMPERATURE RANGE:
- Operating —
  - CA101 ..... -55 to +125° C
  - CA201, CA301A ..... 0 to +70° C
- Storage (All types) ..... -65 to +150° C

LEAD TEMPERATURE (During Soldering):
- At a distance 1/16" ± 1/32" (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

* At $T_A \leq$ 70° C and $T_C \leq$ 125° C (CA101); $T_A \leq$ 55° C and $T_C \leq$ 70° C (CA201, CA301A).

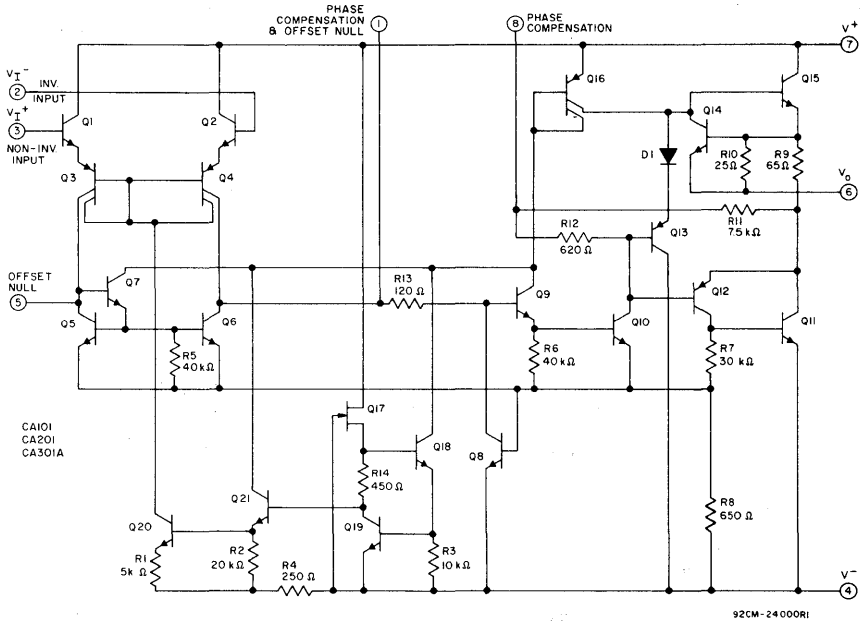


Fig. 2 - Schematic diagram.

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	TEST CONDITIONS Δ	LIMITS									UNITS
	Supply Voltage (V±) = 5 to 15 V	CA101			CA201			CA301A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage V_{IO}	T_A=25°C $R_S \leq 10k\Omega$	—	1	5	—	2	7.5	—	—	—	mV
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	—	2	7.5	
	$R_S \leq 10k\Omega$	—	—	6	—	—	10	—	—	—	
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	—	—	10	
Average Temperature Coefficient of Input Offset Voltage αV_{IO}	$R_S \leq 10k\Omega$	—	6	—	—	10	—	—	—	—	μV/°C
	$R_S \leq 50\Omega$	—	3	—	—	6	—	—	—	—	
		—	—	—	—	—	—	—	6	30	
Average Temperature Coefficient of Input Offset Current αI_{IO}	-55°C to +25°C	—	—	—	—	—	—	—	—	—	nA/°C
	0°C to +25°C	—	—	—	—	—	—	—	0.02	0.6	
	+25°C to +70°C	—	—	—	—	—	—	—	0.01	0.3	
	+25°C to +125°C	—	—	—	—	—	—	—	—	—	
Input Offset Current I_{IO}	T_A = 0°C	—	—	—	—	150	750	—	—	—	nA
	T_A = 25°C	—	40	200	—	100	500	—	3	50	
	T_A = 70°C	—	—	—	—	50	400	—	—	—	
	T_A = 125°C	—	10	200	—	—	—	—	—	—	
		—	—	—	—	—	—	—	—	70	
	T_A = -55°C	—	100	500	—	—	—	—	—	—	
Input Bias Current I_{IB}	T_A = -55°C	—	0.28	1.5	—	—	—	—	—	—	μA
	T_A = 0°C	—	—	—	—	0.32	2	—	—	—	
	T_A = 25°C	—	0.12	0.5	—	0.25	1.5	—	0.07	0.25	
		—	—	—	—	—	—	—	—	0.3	
Supply Current $I_\pm$	T_A=25°C $V_\pm$=15V	—	—	—	—	—	—	—	1.8	3	mA
	$V_\pm$=20V	—	1.8	3	—	1.8	3	—	—	—	
	T_A=125°C $V_\pm$=20V	—	1.2	2.5	—	—	—	—	—	—	
Open-Loop Differential Voltage Gain A_{OL}	T_A=25°C $V_\pm$=15V V_O=±10V $R_L \geq 2k\Omega$	50	160	—	20	150	—	25	160	—	V/mW
	$V_\pm$=15V V_O=±10V $R_L \geq 2k\Omega$	25	—	—	15	—	—	15	—	—	
Input Resistance R_I	T_A=25°C	0.3	0.8	—	0.1	0.4	—	0.5	2	—	MΩ
Output Voltage Swing V_{OPP}	$V_\pm$=15V R_L=10kΩ	±12	±14	—	±12	±14	—	±12	±14	—	V
	$V_\pm$=15V R_L=2kΩ	±10	±13	—	±10	±13	—	±10	±13	—	
Common-Mode Input-Voltage Range V_{ICR}	$V_\pm$=15V	±12	—	—	±12	—	—	±12	—	—	V
	$V_\pm$=20V	—	—	—	—	—	—	—	—	—	
Common-Mode Rejection Ratio CMRR	$R_S \leq 10k\Omega$	70	90	—	65	90	—	—	—	—	dB
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	70	90	—	
Supply-Voltage Rejection Ratio PSRR	$R_S \leq 10k\Omega$	70	90	—	70	90	—	—	—	—	dB
	$R_S \leq 50k\Omega$	—	—	—	—	—	—	70	90	—	

Δ Characteristics applicable over operating temperature range (T_A) as shown below, unless otherwise specified:
CA101: -55 to +125°C; CA201, CA301A: 0 to 70°C

TYPICAL STATIC CHARACTERISTICS

TYPE CA101

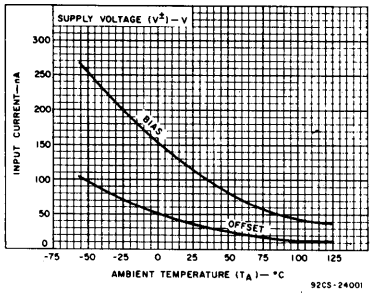


Fig. 3 - Input current (I_{IO}, I_{IB}) vs. temperature.

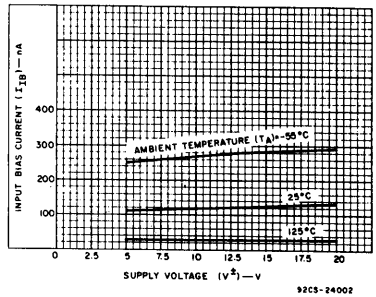


Fig. 4 - Input bias current vs. supply voltage.

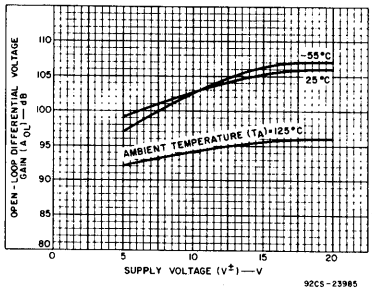


Fig. 5 - Voltage gain vs. supply voltage.

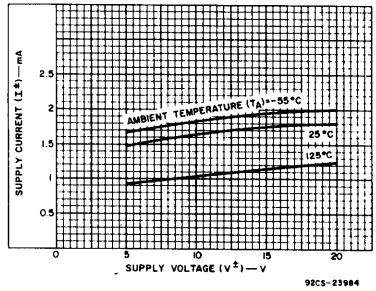


Fig. 6 - Supply characteristics.

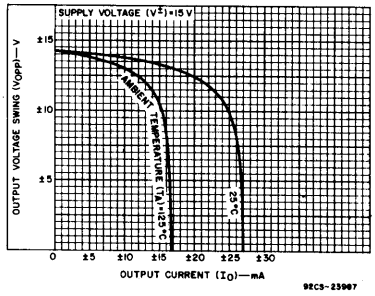


Fig. 7 - Output characteristics.

TYPE CA201

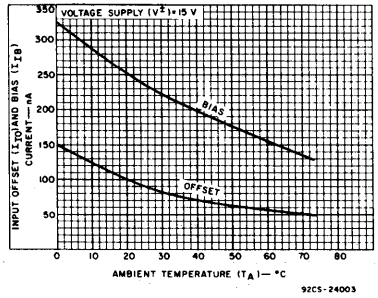


Fig. 8 - Input current (I_{IO}, I_{IB}) vs. temperature.

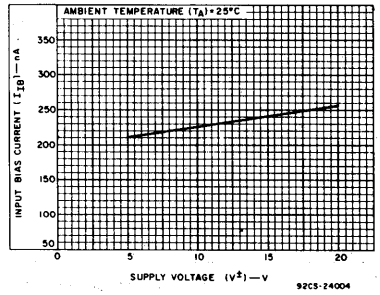


Fig. 9 - Input bias current (I_{IB}) vs. supply voltage.

TYPICAL STATIC CHARACTERISTICS (Cont'd)

TYPE CA201

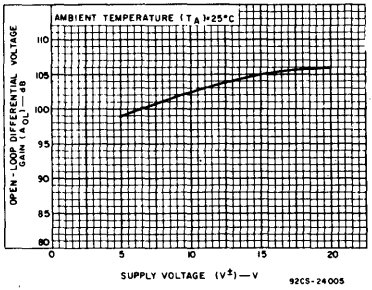


Fig. 10 - Voltage gain vs. supply voltage.

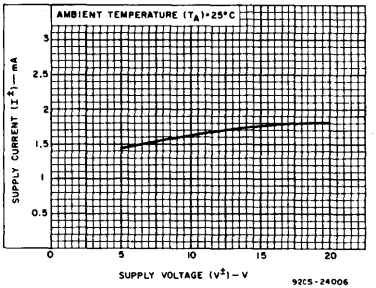


Fig. 11 - Supply characteristics.

TYPE CA301A

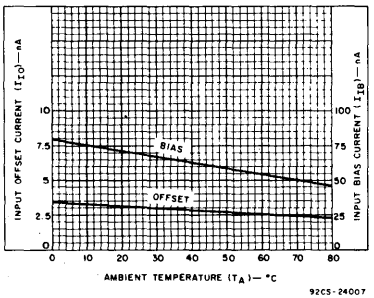


Fig. 12 - Input current (I_{IO}, I_{IB}) vs. temperature.

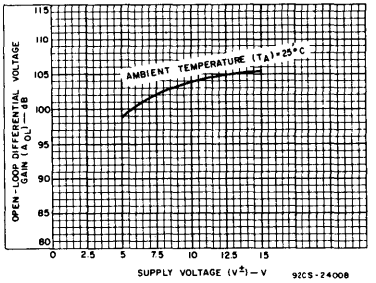


Fig. 13 - Voltage gain vs. supply voltage.

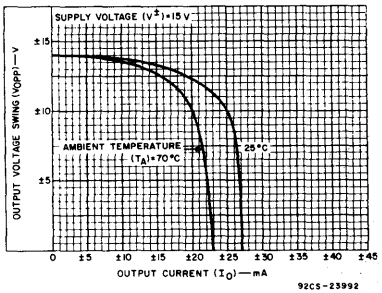


Fig. 14 - Output characteristics.

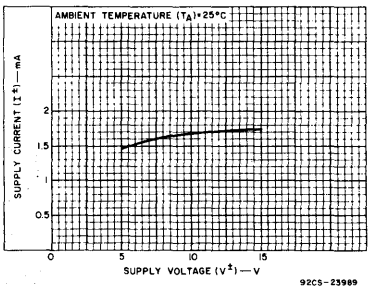


Fig. 15 - Supply characteristics.

TYPICAL DYNAMIC CHARACTERISTICS
TYPES CA101, CA201, CA301A

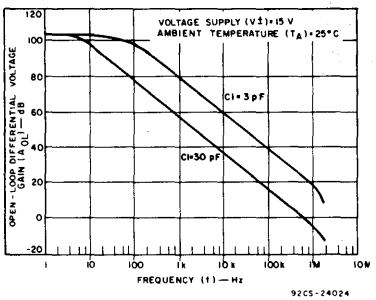


Fig. 16 - Voltage gain vs. frequency.

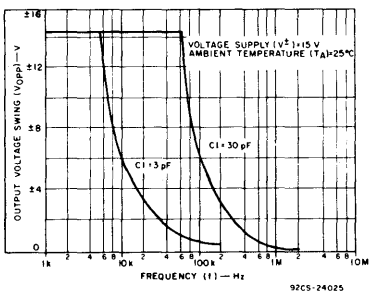


Fig. 17 - Output voltage swing vs. frequency.

TYPICAL DYNAMIC CHARACTERISTICS (Cont'd) FOR TYPES CA101, CA201 AND CA301A

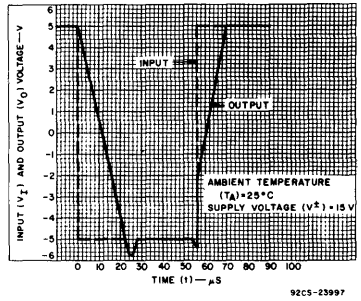


Fig. 18 - Voltage follower pulse response.

TYPE CA301A

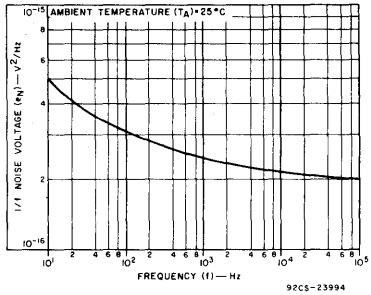


Fig. 19 - 1/f noise voltage vs. frequency.

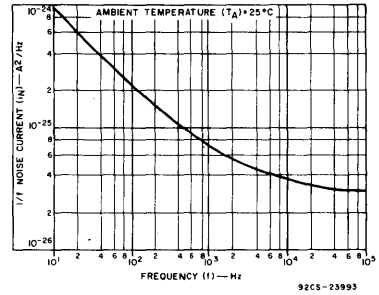
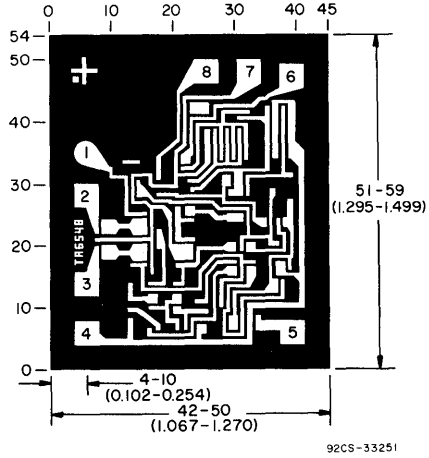


Fig. 20 - 1/f noise current vs. frequency.



Dimensions and pad layout for CA301H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Operational Amplifiers

CA124, CA224, CA324, CA2902, LM324*, LM2902*

May 1990

Quad Operational Amplifiers

For Commercial, Industrial, and Military Applications

Features:

- *Operation from single or dual supplies*
- *Unity-gain bandwidth - 1 MHz (typ.)*
- *DC voltage gain - 100 dB (typ.)*
- *Input bias current - 45 nA (typ.)*
- *Input offset voltage - 2 mV (typ.)*
- *Input offset current -*
  5 nA (typ.) for CA224, CA324, CA2902, LM324, LM2902
  3 nA (typ.) for CA124
- *Replacement for industry types 124, 224, 324*

Applications:

- *Summing amplifiers*
- *Multivibrators*
- *Oscillators*
- *Transducer amplifiers*
- *DC gain blocks*

The CA124, CA224, CA324, CA2902, LM324, and LM2902 consist of four independent, high-gain operational amplifiers on a single monolithic substrate. An on-chip capacitor in each of the amplifiers provides frequency compensation for unity gain. These devices are designed specially to operate from either single or dual supplies, and the differential voltage range is equal to the power-supply voltage. Low power drain and an input common-mode voltage range from 0 V to V+ -1.5 V (single-supply operation) make these devices suitable for battery operation.

The CA124, CA224, CA324, CA2902, LM324 and LM2902 are supplied in both 14-lead dual-in-line plastic (E suffix) and 14-lead (150 mil) small outline (M suffix) packages. These devices are also available in chip form (H suffix).

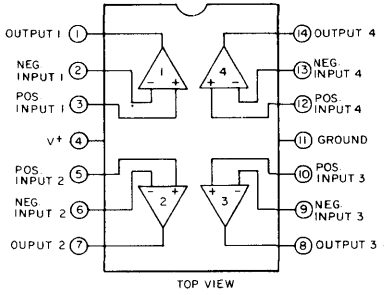


Figure 1 - Functional diagram.

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

File Number **796**

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

SUPPLY VOLTAGE	32 V or ±16 V
DIFFERENTIAL INPUT VOLTAGE	±32 V
INPUT VOLTAGE	−0.3 V to +32 V
INPUT CURRENT ($V_I < -0.3$ V)†	50 mA
OUTPUT SHORT CIRCUIT TO GROUND ($V^+ \leq 15$ V)*	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+265°C

*The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device.

†This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V dc.

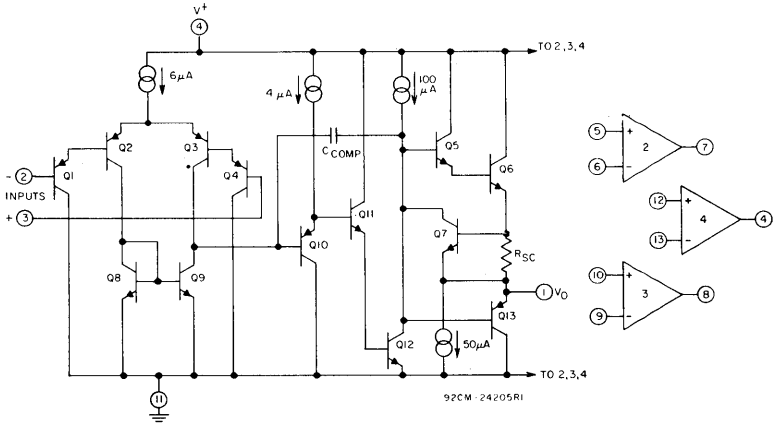


Fig. 2—Schematic diagram—one of four operational amplifiers.

ELECTRICAL CHARACTERISTICS (Values Apply For Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	CA124 LIMITS			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	5	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+–1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+=30 V	0	–	V^+–1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	3	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	150	nA
Output Current (Source), I_O	V_I^+=+1 V, V_I^-=0 V, V^+=15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+=0 V, V_I^-=1 V, V^+=15 V	10	20	–	mA
	V_I^+=0 V, V_I^-=1 V, V_O=200 mV	12	50	–	μA
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	94	100	–	dB
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f=1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –55 to +125°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	7	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	100	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	–	300	nA
Total Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.8	2	mA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V	0	–	V^+–2	V
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	88	–	–	dB
Output Voltage Swing: High-Level, V_{OH}	R_L=2 kΩ, V^+=30 V	26	–	–	V
	R_L=10 kΩ	27	28	–	
Low-Level, V_{OL}	R_L=10 kΩ	–	5	20	mV
Output Current: Source, I_O	V_I^+=1 V_{DC}, V_I^-=0, V^+=15 V	10	20	–	mA
Sink, I_O	V_I^-=1 V_{DC}, V_I^+=0, V^+=15 V	5	8	–	mA
Differential Input Voltage	Note 2	–	–	V^+	V

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltage and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ - 1.5 V, but either or both inputs can go to +32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode voltage range (0 V to V^+ - 1.5 V).

ELECTRICAL CHARACTERISTICS (Values apply for each operational amplifier)

CHARACTERISTIC	TEST CONDITIONS	CA224, CA324 LIMITS			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+–1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+= 30 V	0	–	V^+–1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	V_I^+=+1 V, V_I^-=0 V, V^+=15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+=0 V, V_I^-=1 V, V^+=15 V	10	20	–	mA
	V_I^+=0 V, V_I^-=1 V, V_O=200 mV	12	50	–	μA
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	88	100	–	dB
Common-Mode Rejection Ratio, CMRR	DC	65	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –40 to +85°C (CA224), T_A = 0 to 70°C (CA324)				
Input Offset Voltage, V_{IO}	Note 3	–	–	9	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	150	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	–	500	nA
Total Supply Current, I^+	R_L =∞ On All Ampl.	–	0.8	2	mA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V	0	–	V^+–2	V
Large-Signal Voltage Gain, A	$R_L \geq 2$ kΩ, V^+=15 V (For large V_O swing)	83	–	–	dB
Output Voltage Swing: High-Level, V_{OH}	R_L = 2 kΩ, V^+ = 30 V	26	–	–	V
	R_L = 10 kΩ	27	28	–	
Low-Level, V_{OL}	R_L = 10 kΩ	–	5	20	mV
Output Current: Source, I_O	V_I^+=1 V_{DC}, V_I^-=0, V^+=15 V	10	20	–	mA
Sink, I_O	V_I^-=1 V_{DC}, V_I^+=0, V^+=15 V	5	8	–	mA
Differential Input Voltage	Note 2	–	–	V^+	V

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltage and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go to +32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

ELECTRICAL CHARACTERISTICS (Values apply for each operational amplifier)

CHARACTERISTIC	TEST CONDITIONS	2902 LIMITS			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = -40 to +85°C (CA2902)				
Input Offset Voltage, V_{IO}	Note 3	-	-	10	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	-	7	-	µV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	-	45	200	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		-	10	-	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	-	40	500	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 26 V, Note 2	0	-	V^+ -2	V
Supply Current, I^+	$R_L = \infty$ On All Ampl.	-	0.7	1.2	mA
	$R_L = \infty$, V^+ = 26 V	-	1.5	3	
Large-Signal Voltage Gain, A	R_L > 2 kΩ, V^+ = 15 V (For large V_O swing)	83	-	-	dB
Output Voltage Swing:					
High-Level, V_{OH}	R_L = 2 kΩ, V^+ = 26 V	22	-	-	V
	R_L = 10 kΩ	23	28	-	
Low-Level, V_{OL}	R_L = 10 kΩ	-	5	100	mV
Output Current:					
Source, I_O	V_I^+ = 1 V_{DC}, V_I^- = 0, V^+ = 15 V	10	20	-	mA
Sink, I_O	V_I^- = 1 V_{DC}, V_I^+ = 0, V^+ = 15 V	5	8	-	mA
Differential Input Voltage	Note 2	-	-	V^+	V

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because the current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltage and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ - 1.5 V, but either or both inputs can go to +32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V; and over the full input common-mode voltage range (0 V to V^+ - 1.5 V).

TYPICAL CHARACTERISTICS CURVES

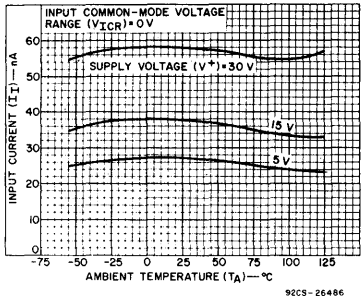


Fig. 3—Input current vs. ambient temperature.

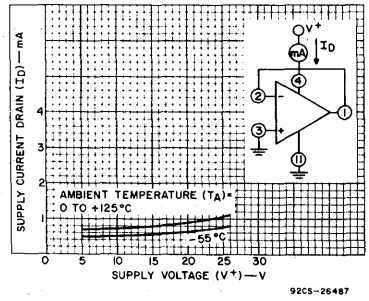


Fig. 4—Supply current drain vs. supply voltage.

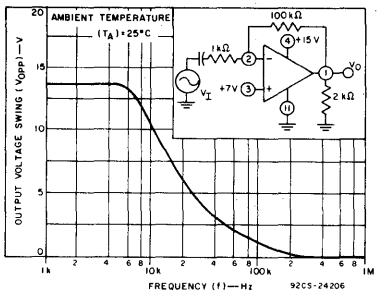


Fig. 5—Large-signal frequency response.

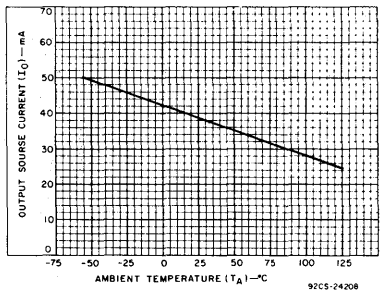


Fig. 6—Output current vs. ambient temperature.

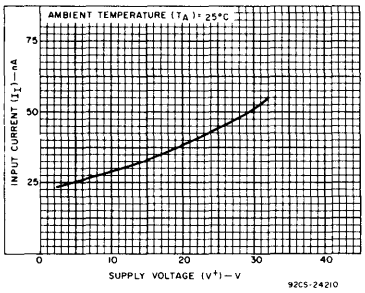


Fig. 7—Input current vs. supply voltage.

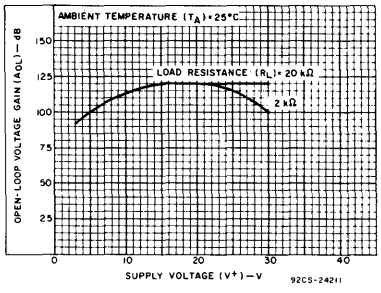


Fig. 8—Voltage gain vs. supply voltage.

TYPICAL CHARACTERISTICS CURVES (CONT'D)

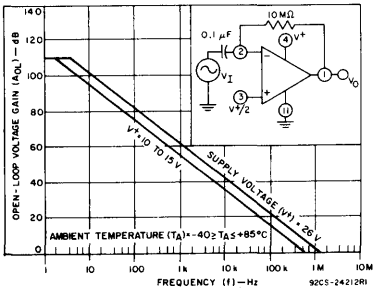


Fig. 9—Open-loop frequency response.

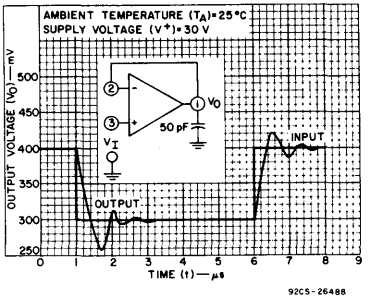


Fig. 10—Voltage follower pulse response (small signal).

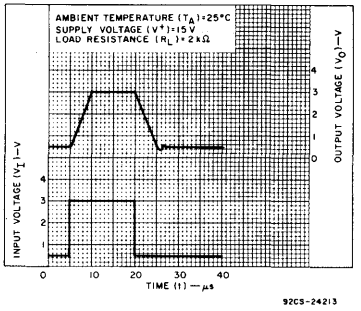


Fig. 11—Voltage follower pulse response.

Operational Amplifiers

CA158, CA158A, CA258, CA258A, CA358, CA358A, CA2904, LM358*, LM2904*

May 1990

Dual Operational Amplifiers

For Commercial, Industrial, and Military Applications

Features:

- *Internal frequency compensation for unity gain*
- *High dc voltage gain – 100 dB typ.*
- *Wide bandwidth at unity gain – 1 MHz typ.*
- *Wide power supply range:*
  Single supply 3 to 30 V
  Dual supplies ± 1.5 to ± 15 V
- *Low supply current – 1.5 mA typ.*
- *Low input bias current*
- *Low input offset voltage and current*
- *Input common-mode voltage range includes ground*
- *Differential input voltage range equal to V+ range*
- *Large output voltage swing – 0 to V+ –1.5V*

The CA158, CA158A, CA258, CA258A, CA358, CA358A and CA2904 types consist of two independent, high gain, internally frequency compensated operational amplifiers which are designed specifically to operate from a single power supply over a wide range of voltages. They may also be operated from split power supplies. The supply current is basically independent of the supply voltage over the recommended voltage range.

These devices are particularly useful in interface circuits with digital systems and can be operated from the single common 5 Vdc power supply. They are also intended for transducer amplifiers, dc gain blocks and many other conventional op amp circuits which can benefit from the single power supply capability.

The CA158, CA158A, CA258, CA258A, CA358, CA358A, and CA2904 types are supplied in 8-lead Small Outline packages (M suffix), 8-lead dual-in-line plastic packages (MINI-DIP, E suffix), 8-lead TO-5 style packages with standard leads (T suffix), and with dual-in-line formed leads (DIL-CAN, S suffix). The CA358 is also supplied in chip form (H suffix).

The CA158, CA158A, CA258, CA258A, CA358, CA358A, and CA2904 types are an equivalent to or a replacement for the industry types 158, 158A, 258, 258A, 358, 358A, and CA2904.

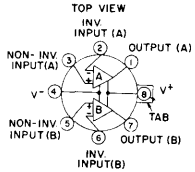


Figure 1 – Functional diagram for CA158, CA258, and CA358 S- and T-suffix types.

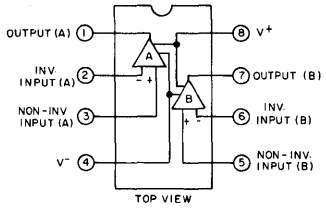


Figure 2 – Functional diagram for CA158, CA258, CA358, and CA2904 E-suffix and M-suffix types.

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

SUPPLY VOLTAGE, V^+:	
CA2904	26 V or ± 13 V
Other Types	32 V or ± 16 V
DIFFERENTIAL INPUT VOLTAGE:	
All Types	± 32 V
INPUT VOLTAGE	−0.3 V to V^+ V
INPUT CURRENT ($V_I < -0.3$ V) +	50 mA
OUTPUT SHORT CIRCUIT TO GROUND	
($V^+ \leq 15$ V)*	Continuous
DEVICE DISSIPATION:	
Up to $T_A = 55^oC$	630 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/^{o}C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to + 125^{o}C
Storage	−65 to + 150^{o}C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	+ 300 ^{o}C

+ This input current will only exist when the voltage at any of the input leads is driven negative. This current is due to the collector-base junction of the input p-n-p transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral n-p-n parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This transistor action is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3 V dc.

* The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

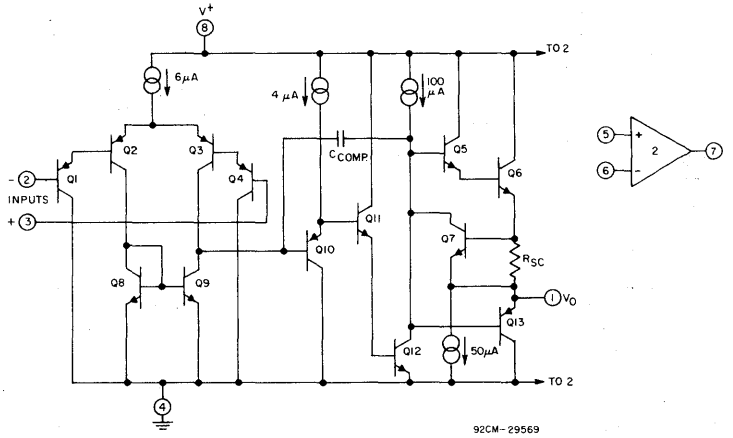


Fig.3 – Schematic diagram – one of two operational amplifiers.

ELECTRICAL CHARACTERISTICS (Values Apply For Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA158A (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	1	2	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	2	10	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	20	50	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geqslant$ 2 kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –55 to +125°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	4	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	15	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	30	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	200	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	100	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA258A (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	1	3	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	2	15	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	40	80	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –25 to +85°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	4	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_s = 0	–	7	15	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	30	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	200	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	100	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_s = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of thedevice. Destructive dissipation can result from simultaneous short circuits on both amplifiers

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA358A (E. T. S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	3	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	100	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	25	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	65	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = 0 to +70°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	5	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	20	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	75	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	300	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	200	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ – 1.5 V, but either or both inputs can go the + 32 V without damage.

NOTE 3: V_O = 1.4 V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V^+ – 1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at $V^+ > 15$ V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA158 (E, T, S) CA258 (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	5	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	3	30	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	150	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V^+ = 15 V (For large V_O swing)	50	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	70	85	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = –55 to + 125°C (CA158); T_A = –25 to +85°C (CA258)				
Input Offset Voltage, V_{IO}	Note 3	–	–	7	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	100	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	300	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ -1.5 V, but either or both inputs can go the +32 V without damage.

NOTE 3: V_O = 1.4, V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V+ -1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at V^+ > 15 V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA358 (E, T, S)			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 2 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15 V	10	20	–	mA
	V_I^+ = 0 V, V_I^- = 1 V, V_O = 200 mV	12	50	–	μA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geqslant$ 2 kΩ, V^+ = 15 V (For large V_O swing)	25	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	65	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	65	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = 0 to +70°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	9	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	–	150	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	500	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ -1.5 V, but either or both inputs can go the +32 V without damage.

NOTE 3: V_O = 1.4, V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V+ -1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at V^+ > 15 V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

ELECTRICAL CHARACTERISTICS (Values Apply for Each Operational Amplifier)

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA2904E			UNITS
	Supply Voltage (V^+) = 5 V Unless Otherwise Specified	Min.	Typ.	Max.	
	T_A = 25°C				
Input Offset Voltage, V_{IO}	Note 3	–	2	7	mV
Output Voltage Swing, V_{OPP}	R_L = 10 kΩ	0	–	V^+ –1.5	V
Input Common-Mode Voltage Range, V_{ICR}	Note 2, V^+ = 30 V	0	–	V^+ –1.5	V
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	5	50	nA
Input Bias Current, I_{IB}	I_I^+ or I_I^-, Note 1	–	45	250	nA
Output Current (Source), I_O	V_I^+ = +1 V, V_I^- = 0 V, V^+ = 15 V	20	40	–	mA
Output Current (Sink), I_O	V_I^+ = 0 V, V_I^- = 1 V, V^+=15.V	10	20	–	mA
Short Circuit Output Current	R_L = 0 (to Ground) Note 4	–	40	60	mA
Large Signal Voltage Gain, A_{OL}	$R_L \geqslant$ 2 kΩ, V^+ = 15 V (For large V_O swing)	—	100	–	V/mV
Common-Mode Rejection Ratio, CMRR	DC	50	70	–	dB
Power Supply Rejection Ratio, PSRR	DC	50	100	–	dB
Amplifier-to-Amplifier Coupling	f = 1 to 20 kHz (Input referred)	–	–120	–	dB
	T_A = -40 to +85°C				
Input Offset Voltage, V_{IO}	Note 3	–	–	10	mV
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 0	–	7	–	μV/°C
Input Offset Current, I_{IO}	$I_I^+ - I_I^-$	–	45	200	nA
Temperature Coefficient of Input Offset Current, αI_{IO}		–	10	–	pA/°C
Input Bias Current, I_{IB}	I_I^+ or I_I^-	–	40	500	nA
Input Common-Mode Voltage Range, V_{ICR}	V^+ = 30 V, Note 2	0	–	V^+–2	V
Supply Current, I^+	R_L = ∞ On All Ampl.	–	0.7	1.2	mA
	R_L = ∞, V^+ = 30 V	–	1.5	3	

NOTE 1: Due to the p-n-p input stage the direction of the input current is out of the IC. No loading change exists on the input lines because this current is essentially constant, independent of the state of the output.

NOTE 2: The input signal voltages and the input common-mode voltage should not be allowed to go negative by more than 0.3 V. The positive limit of the common-mode voltage range is V^+ -1.5 V, but either or both inputs can go the +32 V without damage.

NOTE 3: V_O = 1.4, V_{DC}, R_S = 0 Ω with V^+ from 5 V to 30 V, and over the full input common-mode voltage range (0 V to V+ -1.5 V).

NOTE 4: The maximum output current is approximately 40 mA independent of the magnitude of V^+. Continuous short circuits at V^+ > 15 V can cause excessive power dissipation and eventual destruction. Short circuits from the output to V^+ can cause overheating and eventual destruction of the device. Destructive dissipation can result from simultaneous short circuits on both amplifiers.

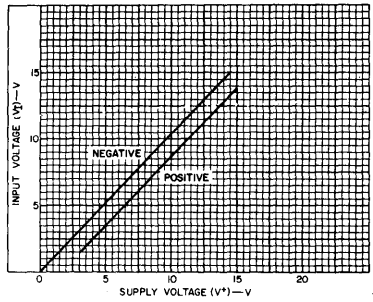


Fig. 4 – Input voltage range as a function of supply voltage.

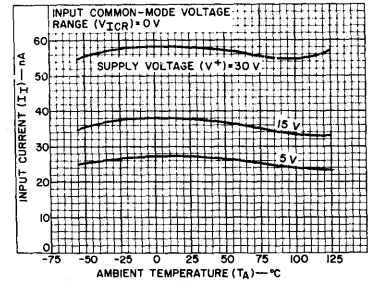


Fig. 5 – Input current as a function of ambient temperature.

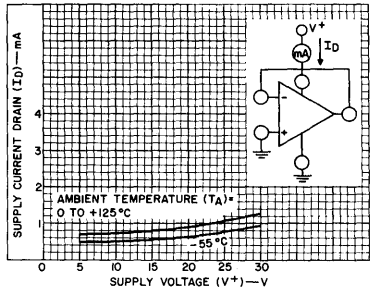


Fig. 6 – Supply current drain as a function of supply voltage.

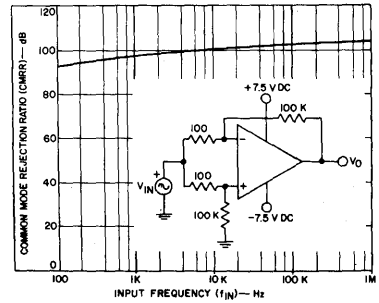


Fig. 7 – Common mode rejection ratio as a function of input frequency.

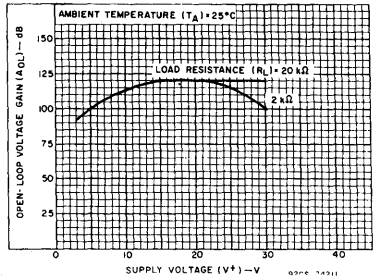


Fig. 8 – Voltage gain as a function of supply voltage.

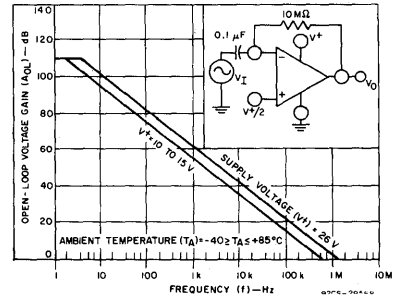


Fig. 9 – Open-loop frequency response.

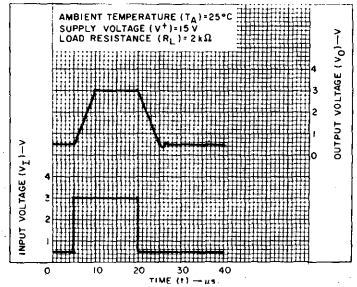


Fig. 10 – Voltage follower pulse response.

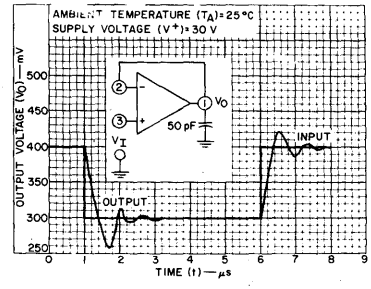


Fig. 11 – Voltage follower pulse response (small signal).

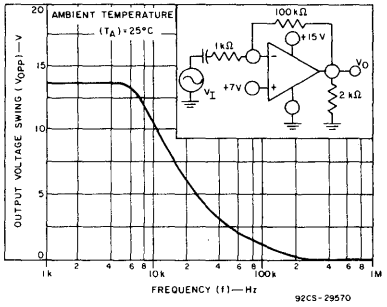


Fig. 12 – Large-signal frequency response.

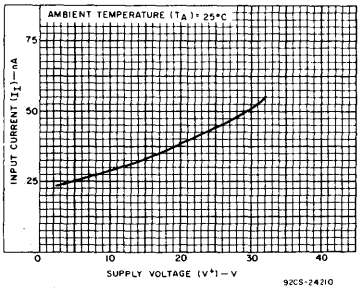


Fig. 13 – Input current as a function of supply voltage.

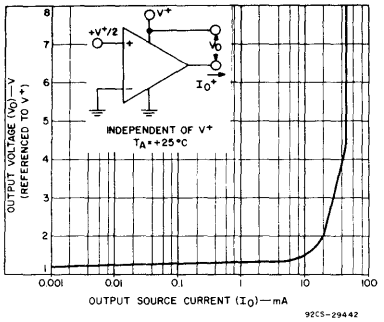


Fig. 14 – Output source current characteristics.

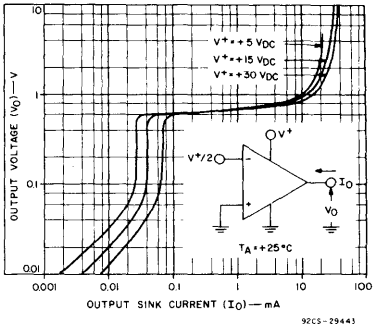


Fig. 15 – Output sink current characteristics.

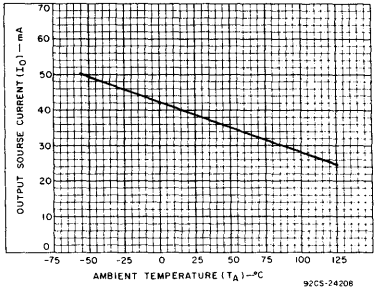
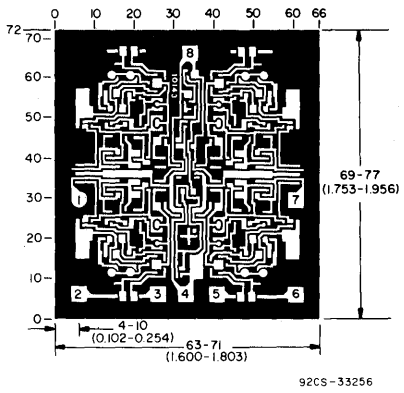


Fig. 16 – Output current as a function of ambient temperature.

ORDERING INFORMATION

These packages are identified by Suffix Letters indicated in the chart shown below. When ordering these devices, it is important that the appropriate suffix letter be affixed to the type number of the device required.

PACKAGE	SUFFIX LETTERS	TYPES
8-Lead Dual-In-Line Plastic with	E	CA158, A CA258, A CA358, A CA2904
8-Lead TO-5 Style with Standard Leads	T	CA158, A CA258, A CA358, A
8-Lead TO-5 Style with Dual-In-Line Formed Leads	S	



Dimensions and pad layout for CA358H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

May 1990

Operational Amplifiers

High-Gain Single and Dual Operational Amplifiers
For Military, Industrial and Commercial Applications

Features:

- *Input bias current (all types): 500 nA max.*
- *Input offset current (all types): 200 nA max.*

Applications:

- *Comparator*
- *DC amplifier*
- *Integrator or differentiator*
- *Multivibrator*
- *Narrow-band or band-pass filter*
- *Summing amplifier*

The CA1458, CA1558 (dual types); CA741C, CA741 (single-types); CA747C, CA747 (dual types); and CA748C, CA748 (single types) are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These monolithic silicon integrated-circuit devices provide output short-circuit protection and latch-free operation. These types also feature wide common-mode and differential-mode signal ranges and have low-offset voltage nulling capability when used with an appropriately valued potentiometer. A 5-megohm potentiometer is used for offset nulling types CA748C, CA748 (See Fig. 10); a 10-kilohm potentiometer is used for offset nulling types CA741C, CA741, CA747CE, CA747E (See Fig. 9); and types CA1458, CA1558, CA747CT, have no specific terminals for offset nulling. Each type consists of a differential-input amplifier that effectively drives a gain and level-shifting stage having a complementary emitter-follower output.

The manufacturing process make it possible to produce IC operational amplifiers with low-burst ("popcorn") noise characteristics. Type CA6741, a low-noise version of the CA741, gives limit specifications for burst noise in the data bulletin, File No. 530. Contact your Sales Representative for information pertinent to other operational amplifier types that meet low-burst noise specifications.

This operational amplifier line also offers the circuit designer the option of operation with internal or external phase compensation.

Types CA748C and CA748, which are externally phase compensated (terminals 1 and 8) permit a choice of operation for improved bandwidth and slew-rate capabilities. Unity gain with external phase compensation can be obtained with a single 30-pF capacitor. All the other types are internally phase-compensated.

TYPE NO.	NO. OF AMPL.	PHASE COMP.	OFFSET VOLTAGE NULL	MINIMUM AOL	MAXIMUM VIO (mV)	OPERATING TEMPERATURE RANGE (°C)
CA1458	Dual	Int.	No	20k	6	0 to 70▲
CA1558	Dual	Int.	No	50k	5	-55 to 125
CA741C	Single	Int.	Yes	20k	6	0 to 70▲
CA741	Single	Int.	Yes	50k	5	-55 to +125
CA747C	Dual	Int.	Yes*	20k	6	0 to 70▲
CA747	Dual	Int.	Yes*	50k	5	-55 to +125
CA748C	Single	Ext.	Yes	20k	6	0 to 70▲
CA748	Single	Ext.	Yes	50k	5	-55 to +125

* In the 14-lead dual-in-line plastic package only.

▲ All types in any package style can be operated over the temperature range of -55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

ORDERING INFORMATION

When ordering any of these types, it is important that the appropriate suffix letter for the package required be affixed to the type number. For example: If a CA1458 in a straight-lead TO-5 style package is desired, order CA1458T.

TYPE NO.	PACKAGE TYPE AND SUFFIX LETTER							FIG. NO.
	TO-5 STYLE			PLASTIC		CHIP	BEAM-LEAD	
	8L	10L	DIL-CAN	8L	14L			
CA1458	T		S	E		H		1d, 1h
CA1558	T		S	E				1d, 1h
CA741C	T		S	E		H		1a, 1e
CA741	T		S	E			L	1a, 1e
CA747C		T			E	H		1b, 1f
CA747		T			E			1b, 1f
CA748C	T		S	E		H		1c, 1g
CA748	T		S	E				1c, 1g

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^\circ C$:*

DC Supply Voltage (between V^+ and V^- terminals):
- CA741C, CA747C▲, CA748C, CA1458▲ . . . . . 36 V
- CA741, CA747▲, CA748, CA1558▲ . . . . . 44 V

Differential Input Voltage . . . . . ±30 V
DC Input Voltage* . . . . . ±15 V
Output Short-Circuit Duration . . . . . Indefinite
Device Dissipation:
- Up to 70°C (CA741C, CA748C) . . . . . 500 mW
- Up to 75°C (CA741, CA748) . . . . . 500 mW
- Up to 30°C (CA747) . . . . . 800 mW
- Up to 25°C (CA747C) . . . . . 800 mW
- Up to 30°C (CA1558) . . . . . 680 mW
- Up to 25°C (CA1458) . . . . . 680 mW

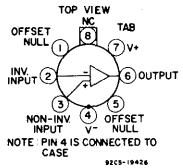
For Temperatures Indicated Above . . . . . Derate linearly 6.67 mW/°C
Voltage between Offset Null and V^- (CA741C, CA741, CA747CE) . . . . . ±0.5 V
Ambient Temperature Range:
- Operating – CA741, CA747E, CA748, CA1558 . . . . . −55 to +125 °C
- CA741C, CA747C, CA748C, CA1458 . . . . . 0 to +70 °C†
- Storage . . . . . −65 to +150 °C

Lead Temperature (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . 265 °C

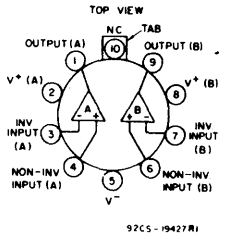
* If Supply Voltage is less than ± 15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

▲ Voltage values apply for each of the dual operational amplifiers.

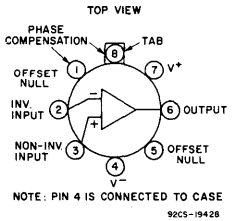
† All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.



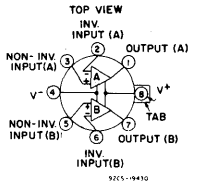
1a.–CA741CS,CA741CT,CA741S, & CA741T with internal phase compensation.



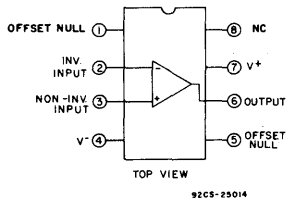
1b.–CA747CT and CA747T with internal phase compensation.



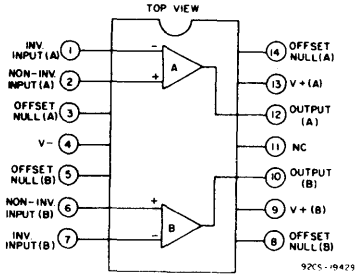
1c.–CA748CS, CA748CT,CA748S, and CA748T with external phase compensation.



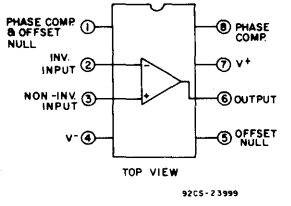
1d.–CA1458S,CA1458T,CA1558S, and CA1558T and internal phase compensation.



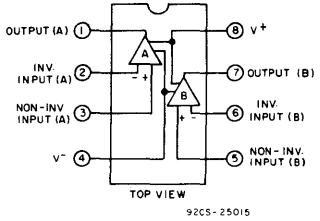
1e.–CA741C and CA741E with internal phase compensation.



1f.–CA747CE and CA747E with internal phase compensation.



1g.–CA748CE and CA748E with external phase compensation.



1h.–CA1458E and CA1558E with internal phase compensation.

Fig. 1 – Functional diagrams.

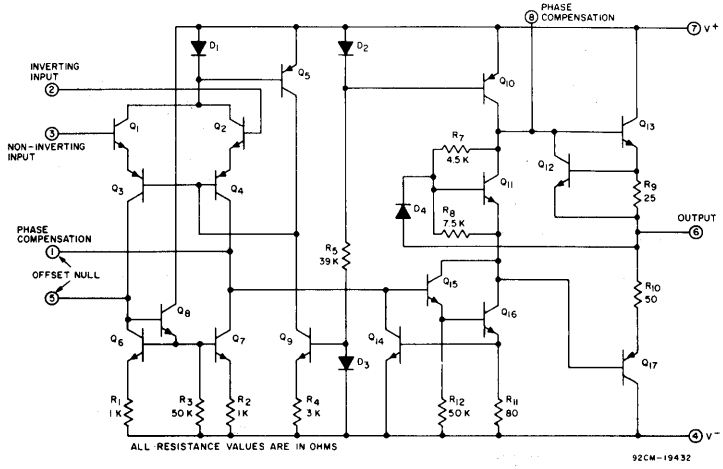


Fig.2—Schematic diagram of operational amplifier with external phase compensation for CA748C and CA748.

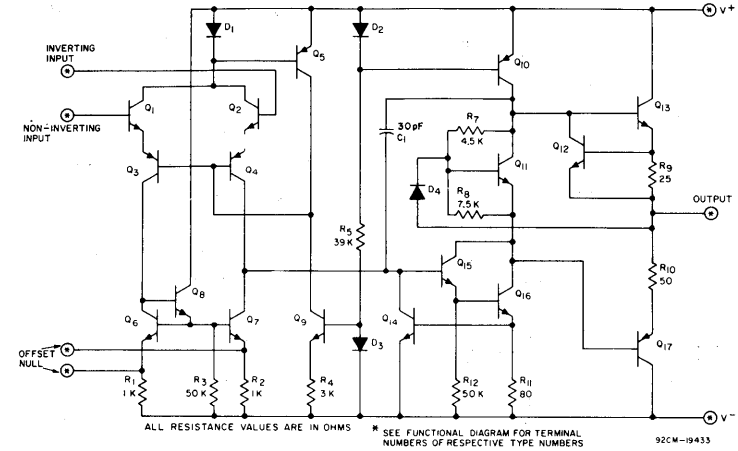


Fig.3—Schematic diagram of operational amplifiers with internal phase compensation for CA741C, CA741, and for each amplifier of the CA747C, CA747, CA1458, and CA1558.

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	TEST CONDITIONS $V\pm$ = ±15 V •	TYP. VALUES ALL TYPES	UNITS
Input Capacitance, C_I		1.4	pF
Offset Voltage Adjustment Range		±15	mV
Output Resistance, R_O		75	Ω
Output Short-Circuit Current		25	mA
Transient Response: Rise Time, t_r	Unity gain, V_I = 20 mV, R_L = 2 kΩ, $C_L \leqslant$ 100 pF	0.3	μs
Transient Response: Overshoot		5	%
Slew Rate, SR: Closed-loop	$R_L \geqslant$ 2 kΩ	0.5	V/μs
Slew Rate, SR: Open-loop▲		40	V/μs

▲ Open-loop slew rate applies only for types CA748C and CA748.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, V^+ = 15 V, V^- = −15 V	Ambient Temperature, T_A	LIMITS CA741C CA747C* CA748C CA1458* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S \leqslant$ 10 kΩ	25 °C	–	2	6	mV
		0 to 70 °C	–	–	7.5	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		0 to 70 °C	–	–	300	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		0 to 70 °C	–	–	800	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geqslant$ 2 kΩ, V_O = ±10 V	25 °C	20,000	200,000	–	
		0 to 70 °C	15,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		25 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leqslant$ 10 kΩ	25 °C	70	90	–	dB
Supply-Voltage Rejection Ratio, PSRR	$R_S \leqslant$ 10 kΩ	25 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geqslant$ 10 kΩ	25 °C	±12	±14	–	V
	$R_L \geqslant$ 2 kΩ	25 °C	±10	±13	–	
		0 to 70 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
Device Dissipation, P_D		25 °C	–	50	85	mW

* Values apply for each section of the dual amplifiers.

ELECTRICAL CHARACTERISTICS

For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, $V^+ = 15$ V, $V^- = -15$ V		LIMITS CA741 CA747* CA748 CA1558*			UNITS
		Ambient Temperature, T_A	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}	$R_S = \leq 10\,k\Omega$	25 °C	–	1	5	mV
		−55 to +125 °C	–	1	6	
Input Offset Current, I_{IO}		25 °C	–	20	200	nA
		−55 °C	–	85	500	
		+125 °C	–	7	200	
Input Bias Current, I_{IB}		25 °C	–	80	500	nA
		−55 °C	–	300	1500	
		+125 °C	–	30	500	
Input Resistance, R_I			0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq 2\,k\Omega$ $V_O = \pm 10$ V	25 °C	50,000	200,000	–	
		−55 to +125 °C	25,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}		−55 to +125 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	70	90	–	dB
Supply Voltage Rejection Ratio, PSRR	$R_S \leq 10\,k\Omega$	−55 to +125 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq 10\,k\Omega$	−55 to +125 °C	±12	±14	–	V
	$R_L \geq 2\,k\Omega$	−55 to +125 °C	±10	±13	–	
Supply Current, $I^{\pm}$		25 °C	–	1.7	2.8	mA
		−55 °C	–	2	3.3	
		+125 °C	–	1.5	2.5	
Device Dissipation, P_D		25 °C	–	50	85	mW
		−55 °C	–	60	100	
		+125 °C	–	45	75	

* Values apply for each section of the dual amplifiers.

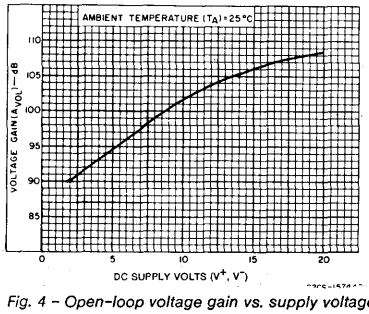


Fig. 4 – Open-loop voltage gain vs. supply voltage for all types except CA748 and CA748C.

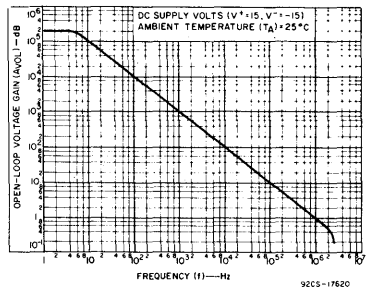


Fig.5–Open-loop voltage gain vs. frequency for all types except CA748 and CA748C.

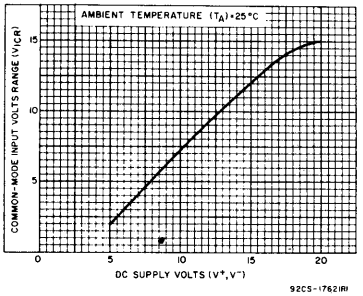


Fig.6—Common-mode input voltage range vs. supply voltage for all types.

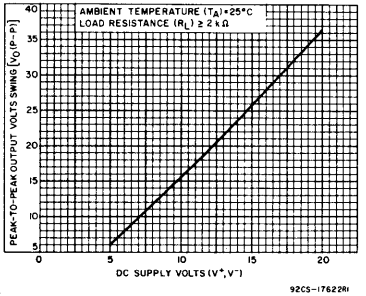


Fig.7—Peak-to-peak output voltage vs. supply voltage for all types except CA748 and CA748C.

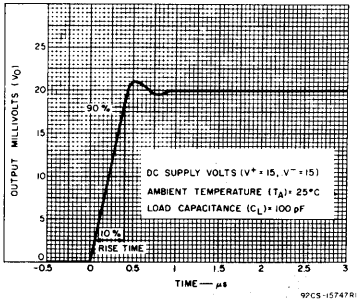


Fig. 8 – Output voltage vs. transient response time for CA741C and CA741.

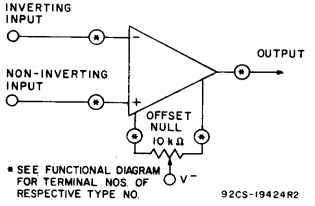


Fig.9—Voltage offset null circuit for CA741C, CA741, CA747CE, and CA747E.

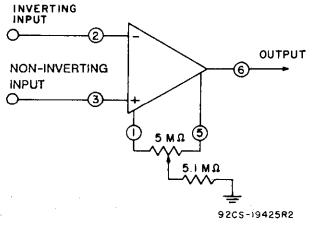


Fig.10—Voltage-offset null circuit for CA748C and CA748.

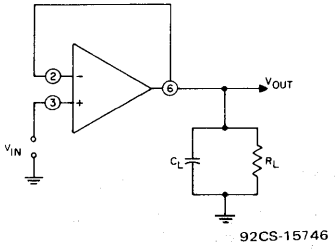
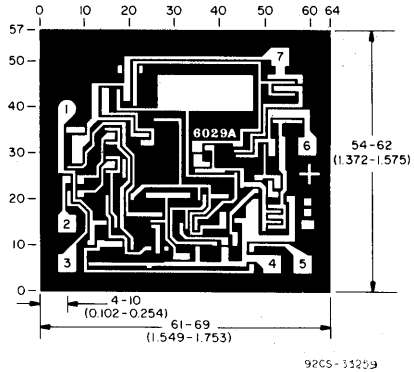


Fig.11—Transient response test circuit for all types.

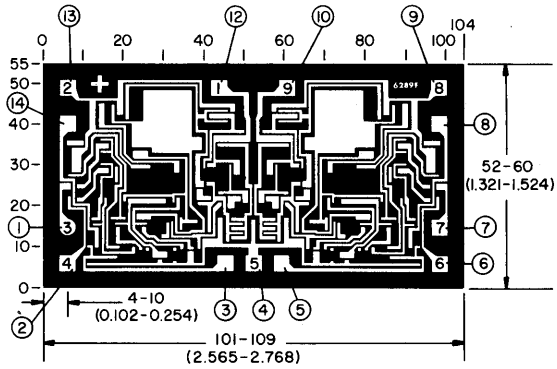
CHIP PHOTOS

Dimensions and Pad Layouts

CA741CH

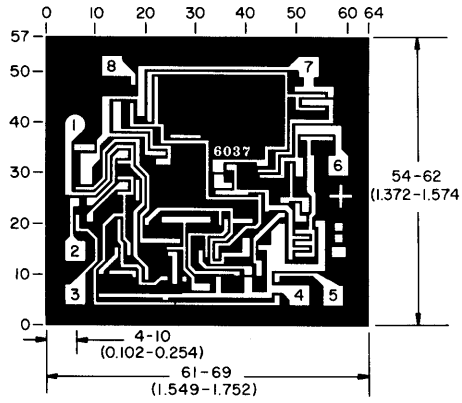


CA747CH

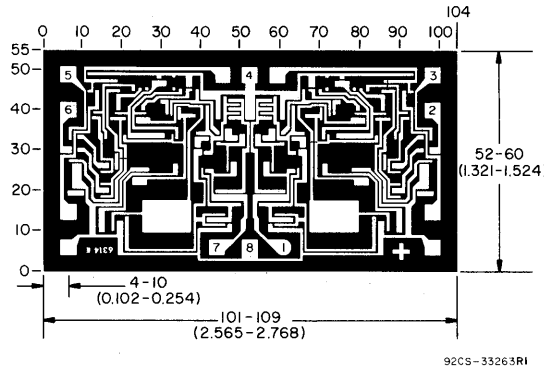


NOTE: NOS. IN PADS ARE FOR 10-LEAD TO-5
NOS. OUTSIDE OF CHIP ARE FOR 14-LEAD DIP

92CM-33260



CA748CH



CA1458H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Operational Amplifiers

CA3010, CA3015, CA3029, CA3030

May 1990

Operational Amplifiers

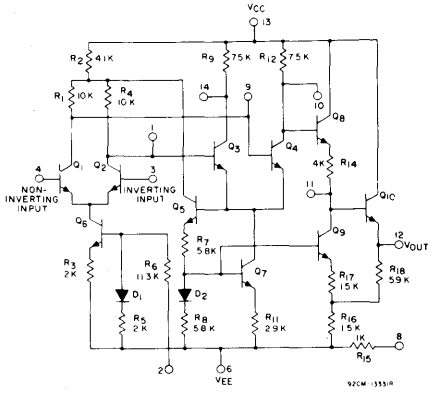
Features:

- *All types are electrically identical within their voltage groups*
- *For use in telemetry, data-processing, instrumentation, and communication equipment*
- *Built-in temperature stability from -55°C to +125°C for TO-5 style; 0°C to +70°C for plastic dual-in-line packages*

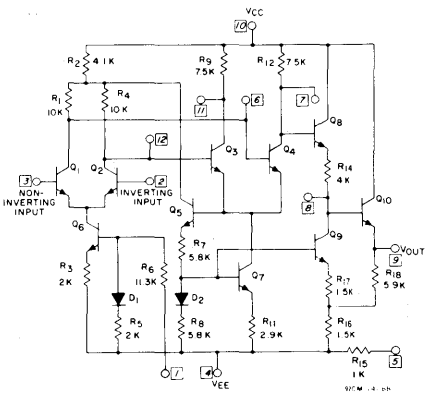
Applications:

- *Narrow-band and band-pass amplifier*
- *Operational functions*
- *Feedback amplifier*
- *DC and video amplifier*
- *Multivibrator*
- *Oscillator*
- *Comparator*
- *Servo driver*
- *Balanced modulator-driver*

6-Volt Types	12-Volt Types	Package
CA3010	CA3015	12-Lead TO-5 Style
CA3029	CA3030	14-Lead Plastic Dual-In-Line



CA3029
CA3030



CA3010
CA3015

Figure 1 - Schematic diagrams.

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010	CA3029	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010	CA3029	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 CA3029 4 & 9 (CA3010)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.4, CA3010 (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015	CA3030	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015	CA3030	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 CA3030 4 & 9 (CA3015)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.4, CA3015 (Substrate) DO NOT GROUND				

	CA3010 CA3015	CA3029 CA3030
OPERATING TEMPERATURE RANGE	-55°C to +125°C	-40°C to +85°C
STORAGE TEMPERATURE RANGE	-65°C to +150°C	-65°C to +150°C

	CA3015 CA3030	CA3010 CA3029
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V	-4 V to +1 V
MAXIMUM DEVICE DISSIPATION	600 mW	300 mW

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 CA3029, CA3030 Terminal No.5 (CA3010, CA3015) Not Connected Unless Otherwise Specified	Test Circuit	CA3010 CA3029			CA3015 CA3030			Units	Typical Characteristic Curves
			Fig.	Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	1.08 -	5 -	- -	- 1.37	- 5	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.54 -	5 -	- -	- 1.07	- 5	μA	2
Input Bias Current	I_{IB}	= +6V = -6V = +12V = -12V	5	- -	5.3 -	12 -	- -	- 9.6	- 24	μA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_D	= +6 V = -6 V = +12V = -12V	4	- -	30 -	- -	- -	- 175	- -	mW	none
		[5] shorted to [9] V_{CC} = +6V V_{EE} = -6V 8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		- -	102 -	- -	- -	- 500	- -		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Common-Mode Rejection Ratio	CMRR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	4 -	6.75 -	- -	- 12	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	10 -	14 -	- -	- 5	- 7.8	- -	kΩ	13
Output Impedance	Z_{OUT}	= +6V = -6V = +12V = -12V	15	- -	200 -	- -	- -	- 92	- -	Ω	16
Common-Mode Input-Voltage Range	V_{ICR}	= +6V = -6V = +12V = -12V	11	0.5 to -4 -	- -	- -	- 0.65 to -8	- -	- -	V	none

LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. ..... +265°C

TYPICAL STATIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029, CA3030
Italic Numbers in Square Boxes are for CA3010, CA3015.

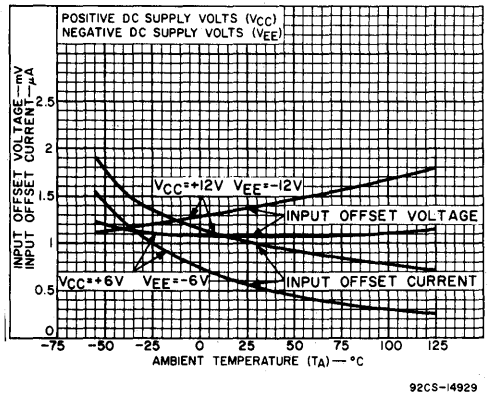


Fig. 2 — Input offset voltage and current.

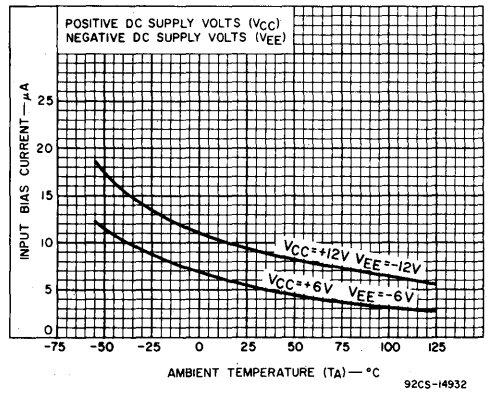


Fig. 3 — Input bias current.

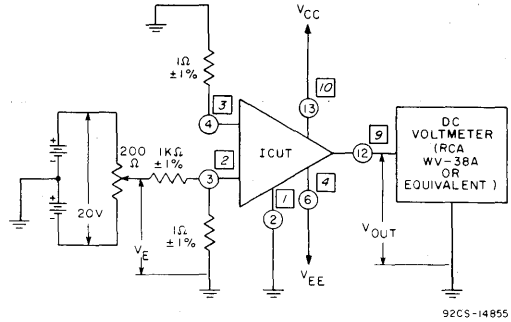


Fig. 4 — Input offset voltage, input offset voltage sensitivity, and device dissipation test circuit

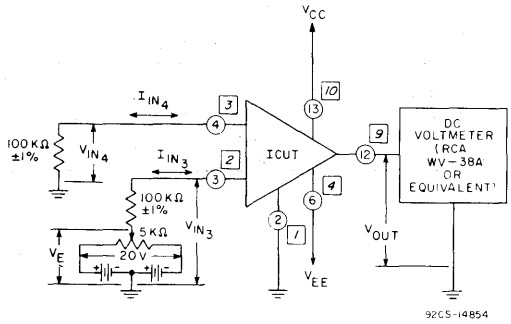


Fig. 5 — Input offset current and input bias current test circuit.

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\ (\text{Step 2}) - V_{OUT}\ (\text{Step 3})}{2\ \text{volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal (13) or *10*

I_E = Direct Current out of Terminal (6) or *4*

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}.
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN_4}}{100\ k\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\ k\Omega$$

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029, CA3030
Italic Numbers in Square Boxes are for CA3010, CA3015.

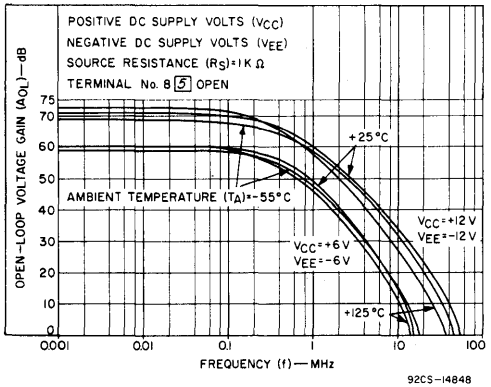


Fig. 6 — Open-loop voltage gain vs. frequency for CA3010, CA3015,

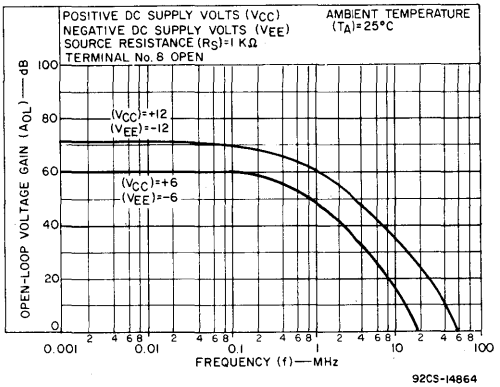
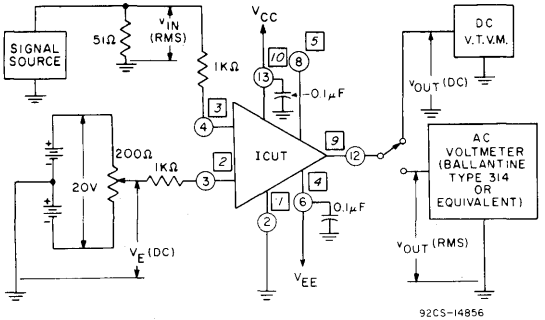


Fig. 7 — Open-loop voltage gain vs. frequency for CA3029 and CA3030



Procedure:

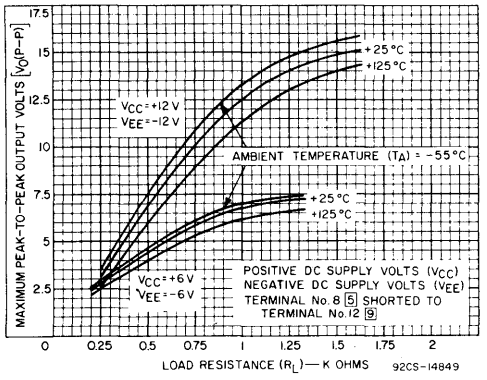
1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz.

$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz.
4. Measure Open-Loop Bandwidth at -3 dB Point.
   Reference Level = A_{OL} at 1 kHz.

Fig.8

Fig. 8 — Open-loop differential voltage gain, maximum peak-to-peak output voltage, and open-loop bandwidth at -3 dB point test circuit



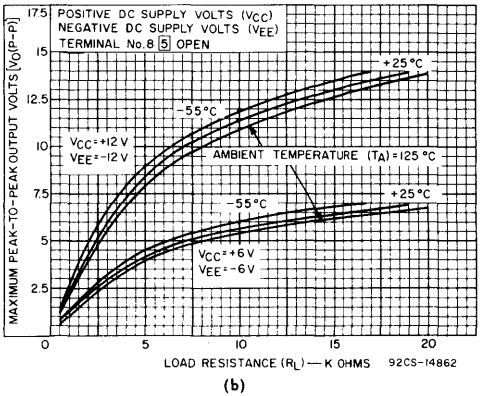


Fig. 9 — Maximum peak-to-peak output voltage vs. load resistance for CA3010, CA3015

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029, CA3030,
Italic Numbers in Square Boxes are for CA3010, CA3015.

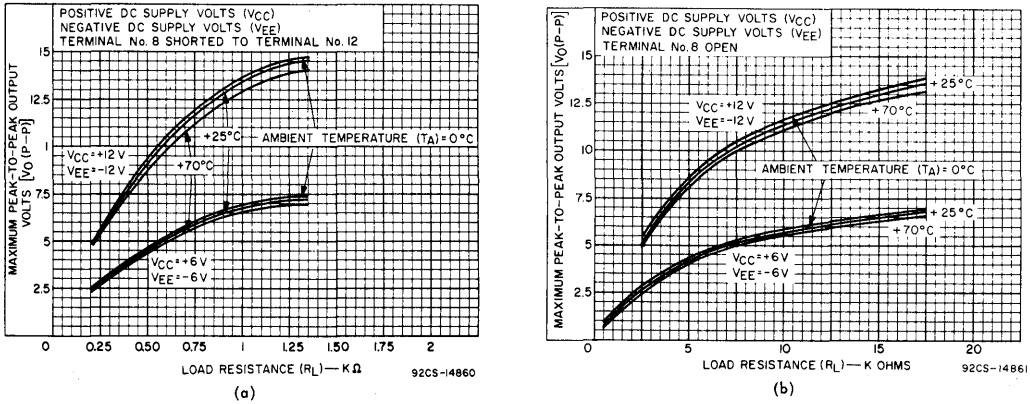
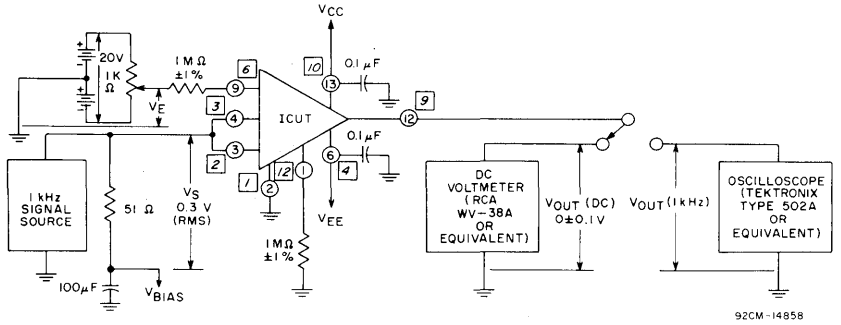


Fig. 10 — Maximum peak-to-peak output voltage vs. load resistance for CA3029 and CA3030



Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for V_{OUT}(DC) = 0 ± 0.1 V.
2. Apply 1-kHz sinusodial input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$

$$A_{CM} \text{ in dB} = -20 \log_{10} V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$CMR \text{ in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB}.$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

Fig. 11 — Common-mode rejection ratio and common-mode input-voltage-range test circuit.

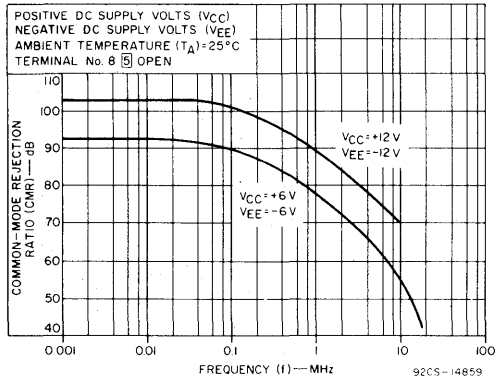


Fig. 12 — Common-mode rejection ratio vs. frequency.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029, CA3030
Italic Numbers in Square Boxes are for CA3010, CA3015.

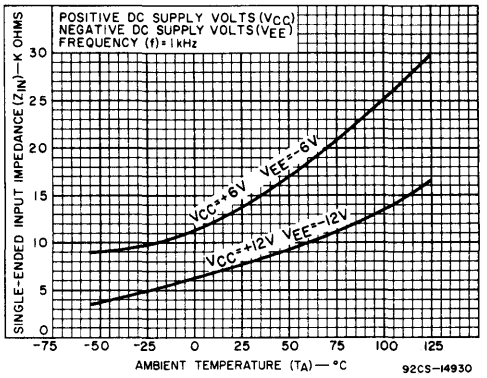


Fig. 13 — Single-ended input impedance vs. temperature.

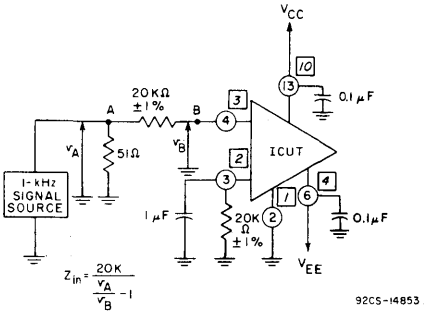
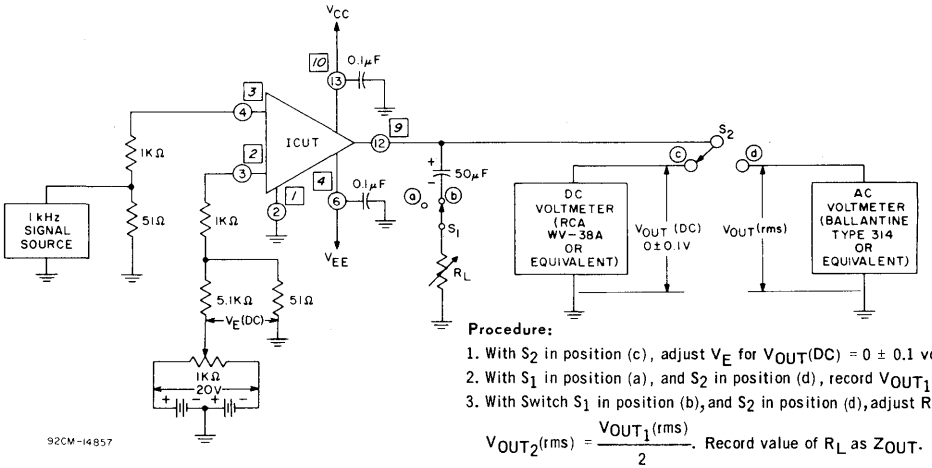


Fig. 14 — Single-ended input impedance test circuit.



Procedure:

1. With S_2 in position (c), adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record $V_{OUT_1}(rms)$.
3. With Switch S_1 in position (b), and S_2 in position (d), adjust R_L until $V_{OUT_2}(rms) = \frac{V_{OUT_1}(rms)}{2}$. Record value of R_L as Z_{OUT}.

Fig. 15 — Output impedance test circuit.

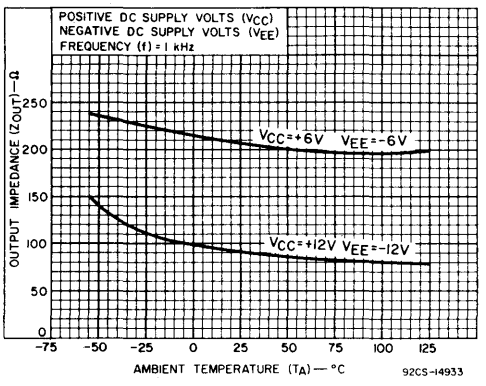


Fig. 16 — Output impedance vs. temperature.

NOT RECOMMENDED FOR NEW DESIGNS SEE CA741

Operational Amplifiers

CA3010A, CA3015A, CA3029A, CA3030A

May 1990

Operational Amplifiers

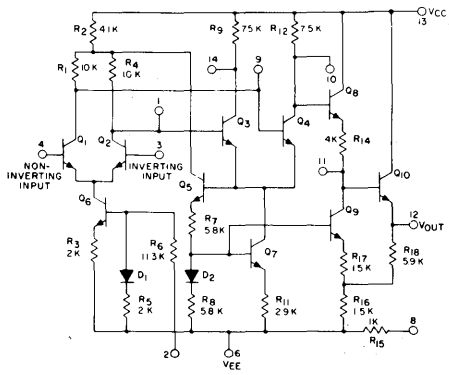
Features:

- *These new types have all the desirable features and characteristics of their prototypes plus lower noise figures and improved input characteristics for offset voltage, offset current, bias current, and impedance*
- *All types are electrically identical within their voltage groups*
- *For use in telemetry, data-processing, instrumentation, and communication equipment*
- *Built-in temperature stability from -55°C to +125°C for TO-5 style, and ceramic dual-in-line packages; 0°C to +70°C for plastic dual-in-line packages*

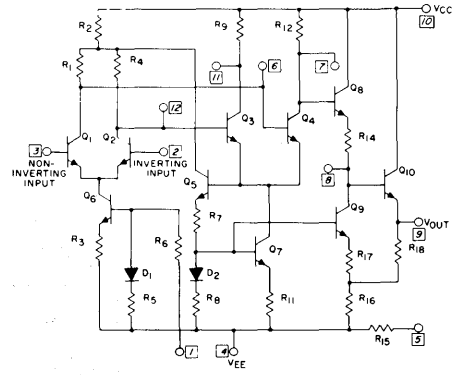
Applications:

- *Narrow-band and band-pass amplifier*
- *Operational functions*
- *Feedback amplifier*
- *DC and video amplifier*
- *Multivibrator*
- *Oscillator*
- *Comparator*
- *Servo driver*
- *Scaling adder*
- *Balanced modulator-driver*

6-VOLT TYPES	12-VOLT TYPES	PACKAGE
CA3010A	CA3015A	12-Lead TO-5 Style
CA3029A	CA3030A	14-Lead Plastic Dual-In-Line (TO-116)



CA3029A, CA3030A



CA3010A, CA3015A

Figure 1 - Schematic diagrams.

File Number **310**

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, T_A = 25°C

Voltage or current limits shown for each terminal can be applied under the indicated voltage or other circuit conditions for other terminals

All voltages are with respect to ground (common terminal of Positive and Negative DC Supplies)

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3010A	CA3029A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3010A	CA3029A	
1	2	-8 V	0 V	4 10	6 13	-8 +6
2	3	-4 V	+1 V	1 3 4 10	2 4 6 13	0 0 -6 +6
3	4	-4 V	+1 V	1 2 4 10	2 3 6 13	0 0 -6 +6
-	5	NO CONNECTION				
4	6	-10 V	0 V	1 10	2 13	0 +6
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 200 Ω Between Terminals 6 & 12 CA3029A, 4 & 9 (CA3010A)	6 13	-6 +6
10	13	0 V	+10 V	1 4	2 6	0 -6
11	14	0 V	+7 V	1 4 10	2 6 13	0 -6 +6
CASE		Internally connected to Terminal No.4, CA3010A (Substrate) DO NOT GROUND				

Terminal		Voltage or Current Limits		Circuit Conditions		
CA3015A	CA3030A	Negative	Positive	Terminal		Voltage
12	1	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
				CA3015A	CA3030A	
1	2	-16 V	0 V	4 10	6 13	-16 +12
2	3	-8 V	+1 V	1 3 4 10	2 4 6 13	0 0 -12 +12
3	4	-8 V	+1 V	1 2 4 10	2 3 6 13	0 0 -12 +12
-	5	NO CONNECTION				
4	6	-20 V	0 V	1 10	2 13	0 +12
-	7	NO CONNECTION				
5	8	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
6	9	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
7	10	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
8	11	DO NOT APPLY VOLTAGE FROM AN EXTERNAL SOURCE TO THIS TERMINAL				
9	12	30 mA		4 10 400 Ω Between Terminals 6 & 12 CA3030A, 4 & 9 (CA3015A)	6 13	-12 +12
10	13	0 V	+20 V	1 4	2 6	0 -12
11	14	0 V	+14 V	1 4 10	2 6 13	0 -12 +12
CASE		Internally connected to Terminal No.4, CA3015A (Substrate) DO NOT GROUND				

	CA3010A CA3015A	CA3029A CA3030A
OPERATING TEMPERATURE RANGE	-55°C to +125°C	-40°C to +80°C
STORAGE TEMPERATURE RANGE	-65°C to +200°C	-65°C to +150°C

	CA3030A CA3015A	CA3029A CA3010A
MAXIMUM SIGNAL VOLTAGE	-8 V to +1 V	-4 V to +1 V
MAXIMUM DEVICE DISSIPATION	600 mW	300 mW

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristics	Symbols	Special Test Conditions Terminal No.8 CA3029A, CA3030A, Terminal No.5 (CA3010A, CA3015A) Not Connected Unless Otherwise Specified	Test Circuit Fig.	CA3010A CA3029A Min.	CA3010A CA3029A Typ.	CA3010A CA3029A Max.	CA3015A CA3030A Min.	CA3015A CA3030A Typ.	CA3015A CA3030A Max.	Units	Typical Characteristic Curves Fig.
STATIC CHARACTERISTICS:											
Input Offset Voltage	V_{IO}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	4	- -	0.9 -	2 -	- -	- 1	- 2	mV	2
Input Offset Current	I_{IO}	= +6V = -6V = +12V = -12V	5	- -	0.3 -	1.5 -	- -	- 0.5	- 1.6	μA	2
Input Bias Current	I_{IB}	= +6V = -6V = +12V = -12V	5	- -	2.5 -	4 -	- -	- 4.7	- 6	μA	3
Input Offset Voltage Sensitivity: Positive	$\Delta V_{IO}/\Delta V_{CC}$	= +6V = -6V = +12V = -12V	4	- -	0.10 -	1 -	- -	- 0.096	- 0.5	mV/V	none
Negative	$\Delta V_{IO}/\Delta V_{EE}$	= +6V = -6V = +12V = -12V		- -	0.26 -	1 -	- -	- 0.156	- 0.5		
Device Dissipation	P_D	= +6 V = -6 V = +12V = -12V	4	- -	40 -	- -	- -	- 175	- -	mW	none
		[5] shorted to [9] V_{CC} = +6V, V_{EE} = -6V 8 shorted to 12 V_{CC} = +12V, V_{EE} = -12V		- -	102 -	- -	- -	- 500	- -		
DYNAMIC CHARACTERISTICS: All tests at f = 1 kHz except BW_{OL}											
Open-Loop Differential Voltage Gain	A_{OL}	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	8	57 -	60 -	- -	- 66	- 70	- -	dB	6 & 7
Open-Loop Bandwidth at -3 dB Point	BW_{OL}	= +6V = -6V = +12V = -12V	8	200 -	300 -	- -	- 200	- 320	- -	kHz	6 & 7
Slew Rate	SR	V_{CC} = +6V V_{EE} = -6V R_S = 1 kΩ = +12V = -12V	none	- -	3 -	- -	- -	- 7	- -	V/μs	none
Common-Mode Rejection Ratio	CMR	V_{CC} = +6V, V_{EE} = -6V = +12V = -12V	11	70 -	94 -	- -	- 80	- 103	- -	dB	12
Maximum Output-Voltage Swing	$V_{O(P-P)}$	= +6V = -6V = +12V = -12V	8	4 -	6.75 -	- -	- 12	- 14	- -	V_{P-P}	9 & 10
Input Impedance	Z_{IN}	= +6V = -6V = +12V = -12V	14	15 -	20 -	- -	- 7.5	- 10	- -	kΩ	13
Output Impedance	Z_{OUT}	= +6V = -6V = +12V = -12V	15	- -	160 -	- -	- -	- 85	- -	Ω	16
Common-Mode Input-Voltage Range	V_{ICR}	= +6V = -6V = +12V = -12V	11	+0.5 to -4 -	- -	- -	- +0.65 to -8	- -	- -	V	none
Noise Figure	NF	V_{CC} = +3V, V_{EE} = -3V R_S = 1 kΩ = +6V = -6V = +9V = -9V = +12V = -12V	18	- - - -	6.3 8.3 - -	9 12 - -	- - - -	6.3 8.3 10 11	9 12 14 16	dB	17

LEAD TEMPERATURE (During Soldering): ALL TYPES

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)
from case for 10 seconds max. ..... +265°C

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029A, CA3030A
Italic Numbers in Square Boxes are for CA3010A, CA3015A.

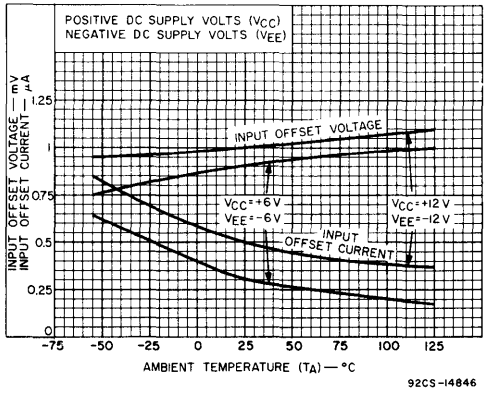


Fig. 2 — Input offset voltage and current

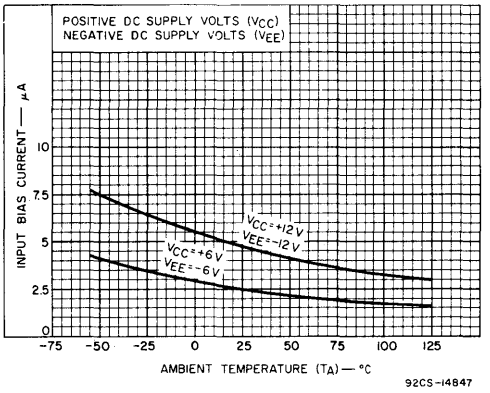


Fig. 3 — Input bias current

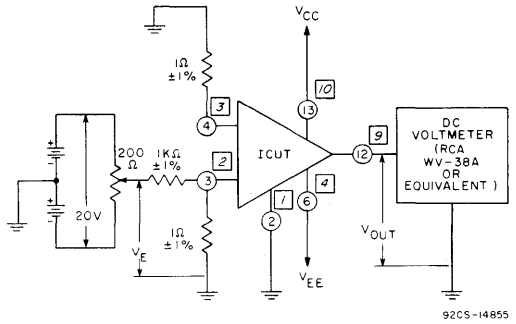


Fig. 4 — Input offset voltage, input offset voltage sensitivity, and and device dissipation test circuit.

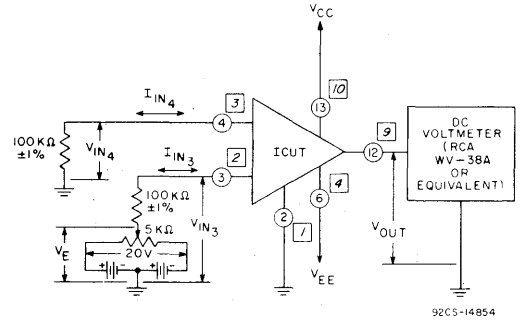


Fig. 5 — Input offset current and input bias current test circuit.

Procedure:

Input Offset Voltage

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Measure V_E and record Input Offset Voltage in millivolts as $V_E/1000$.

Input Offset Voltage Sensitivity

1. Adjust V_E for a DC Output Voltage (V_{OUT}) of 0 ± 0.1 volts.
2. Increase $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
3. Decrease $|V_{CC}|$ by 1 volt and record output voltage (V_{OUT}).
4. Divide the diference between V_{OUT} measured in steps 2 and 3 by the change in V_{CC} in steps 2 and 3.

$$\frac{V_{OUT}}{V_{CC}} = \frac{V_{OUT}\text{ (Step 2) - }V_{OUT}\text{ (Step 3)}}{2\text{ volts}}$$

5. Refer the reading to the input by dividing by Open Loop Voltage Gain (A_{OL}).

$$V_{IO}/V_{CC} = \frac{V_{OUT}/V_{CC}}{A_{OL}}$$

6. Repeat procedures 1 through 5 for the Negative Supply (V_{EE}).
7. Device Dissipation

$P_T = V_{CC}I_C + V_{EE}I_E$

I_C = Direct Current into Terminal 13 or *10*

I_E = Direct Current out of Terminal 6 or *4*

Procedure:

Input Bias Current and Input Offset Current

1. Adjust V_E for $|V_{OUT}| < 0.1$ V DC.
2. Measure and record V_E and V_{IN_4}
3. Calculate the Input Bias Current using the following equation:

$$I_{I4} = \frac{V_{IN_4}}{100\text{ k}\Omega}$$

4. Calculate the Input Offset Current using the following equation:

$$I_{IO} = V_E/100\text{ k}\Omega$$

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029A, CA3030A,
Italic Numbers in Square Boxes are for CA3010A, CA3015A.

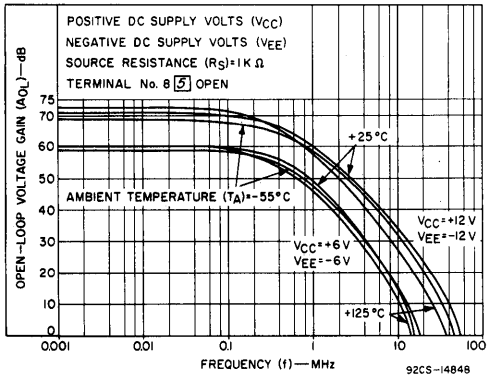


Fig. 6 — Open loop voltage gain vs. frequency for CA3015A, CA3016A

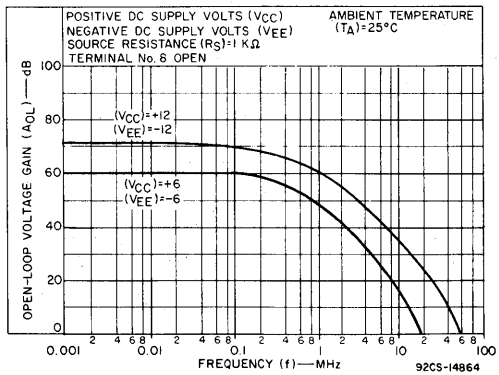
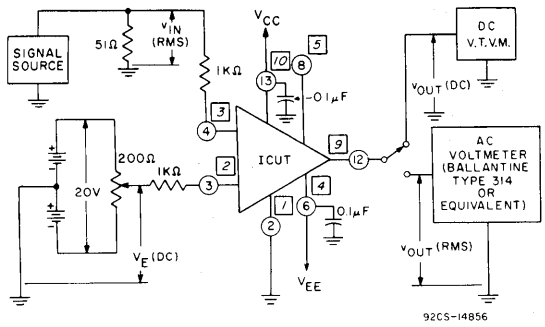


Fig. 7 — Open loop voltage gain vs. frequency for CA3029A and CA3030A.



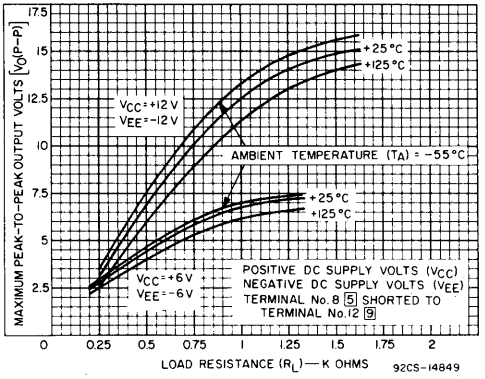
Procedure:

1. Adjust V_E for V_{OUT} = ±0.1 V DC.
2. Measure Open-Loop Differential Voltage Gain (A_{OL}) at f = 1 kHz

$$A_{OL} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$$

3. Measure Maximum Peak-to-Peak Output Voltage at f = 1 kHz
4. Measure Open-Loop Bandwidth at -3 dB Point
   Reference Level = A_{OL} at 1 kHz

Fig. 8 — Open-loop differential voltage gain, maximum peak-to-peak output voltage, and open-loop bandwidth at -3 point test circuit.



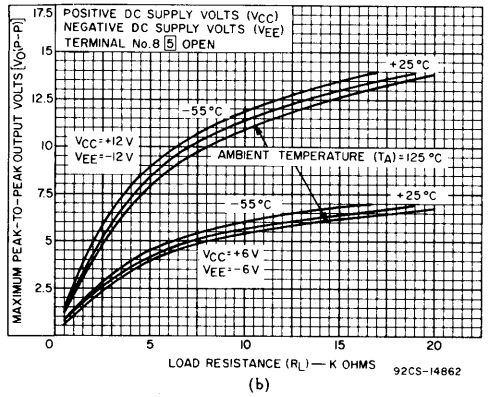


Fig. 9 — Maximum peak-to-peak output voltage vs. load resistance for CA3010A, CA3015A

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029A, CA3030A,
Italic Numbers in Square Boxes are for CA3010A, CA3015A.

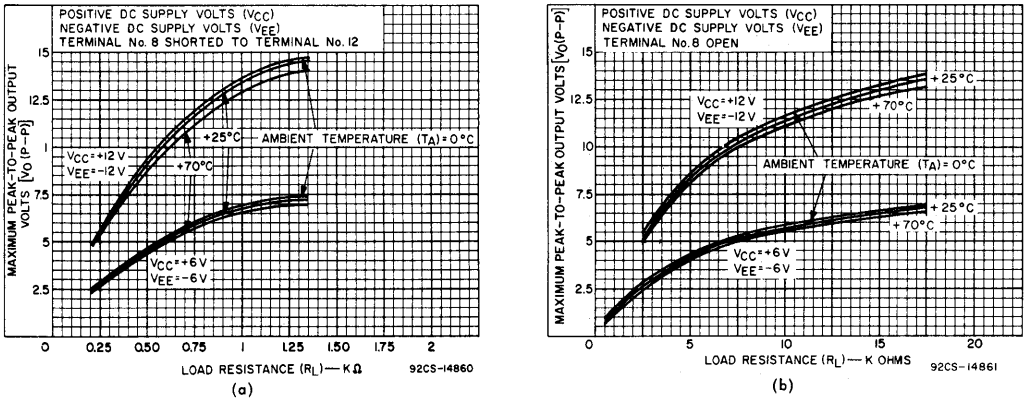
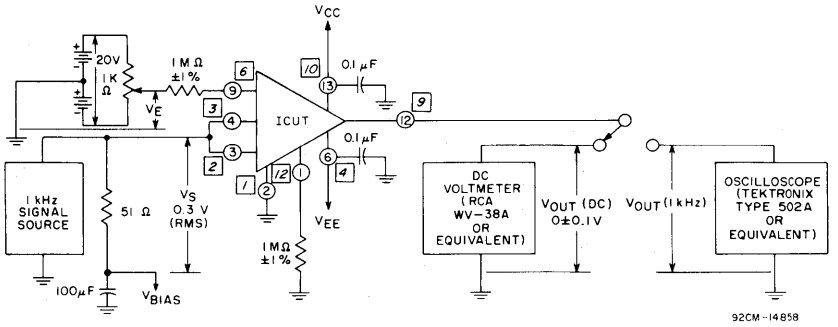


Fig. 10 — Maximum peak-to-peak output voltage vs. load resistance for CA3029A and CA3030A.



Procedures:

Common-Mode Rejection Ratio:

1. Set V_{BIAS} = 0. Adjust V_E for V_{OUT}(DC) = 0 ± 0.1 V.
2. Apply 1-kHz sinusodial input signal and adjust for V_S = 0.3 V (RMS).
3. Measure and record the RMS value of V_{OUT}. An oscilloscope is used for this measurement so that the output signal may be visually separated.from noise output.
4. Calculate Common-Mode Voltage Gain:

$$A_{CM} = V_{OUT}/V_S$$

$$A_{CM} \text{ in dB} = -20 \log_{10} V_S/V_{OUT}$$

5. Calculate Common-Mode Rejection Ratio:

$$CMR \text{ in dB} = A_{DIFF} \text{ in dB} - A_{CM} \text{ in dB.}$$

Common-Mode Input-Voltage Range:

1. Calculate and record CMR for various positive and negative values of V_{BIAS} within the maximum limits shown on Page 2. The Common-Mode Input-Voltage Range limits are those values of V_{BIAS} at which CMR is 6 dB less than that calculated in Step 5 of the procedure given above.

Fig. 11 — Common-mode rejection ratio and common-mode input-voltage-range test circuit.

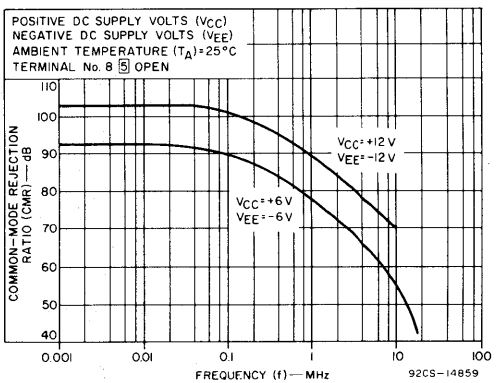


Fig. 12 — Common-mode rejection ratio vs. frequency.

TYPICAL DYNAMIC CHARACTERISTICS AND TEST CIRCUITS

Terminal Numbers in Circles are for CA3029A, CA3030A
Italic Numbers in Square Boxes are for CA3010A, CA3015A.

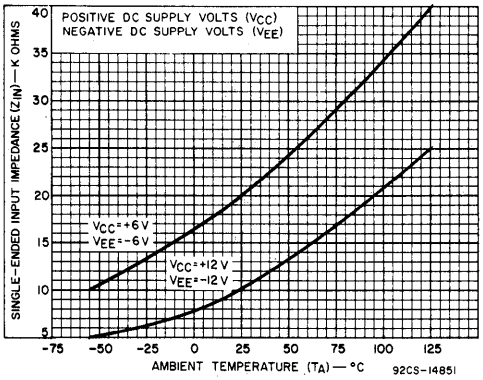


Fig. 13 — Single-ended input impedance vs. temperature.

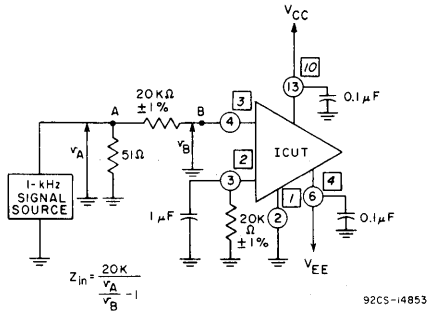
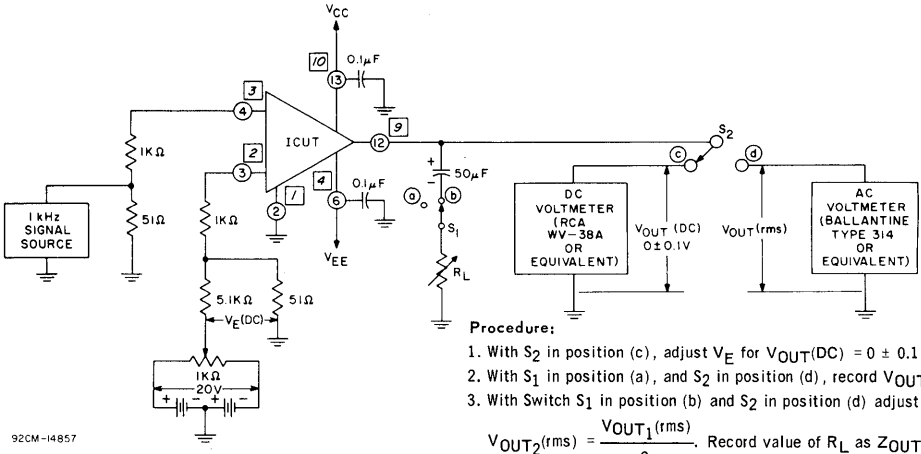


Fig. 14 — Single-ended input impedance test circuit.



Procedure:

1. With S_2 in position (c), adjust V_E for $V_{OUT}(DC) = 0 \pm 0.1$ volt.
2. With S_1 in position (a), and S_2 in position (d), record $V_{OUT_1}(rms)$.
3. With Switch S_1 in position (b) and S_2 in position (d) adjust R_L until $V_{OUT_2}(rms) = \frac{V_{OUT_1}(rms)}{2}$. Record value of R_L as Z_{OUT}.

Fig. 15 — Output impedance test circuit.

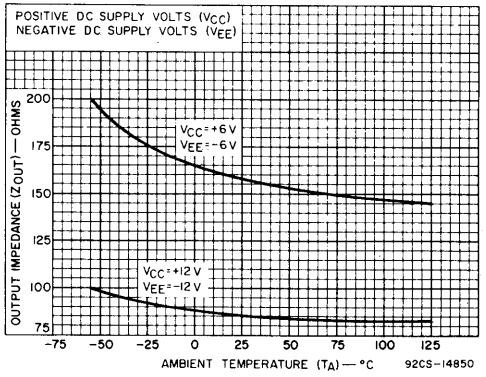


Fig. 16 — Output impedance vs. temperature.

May 1990

Multipurpose Wide-Band Power Amplifiers

For Military, Industrial, and Commercial Equipment at Frequencies up to 8 MHz

Features:

- *High power output-class B amplifier...*
  CA3020-0.5 W typ. at VCC = +9 V
  CA3020A-1.0 W typ. at VCC +12 V
- *Wide frequency range...*
  Up to 8 MHz with resistive loads
- *High power gain...*
  75 dB typ.
- *Single power supply for class B operation with transformer...*
  CA3020-3 to 9 V
  CA3020A-3 to 12 V
- *Built-in temperature-tracking voltage regulator provides stable operation over - 55°C to +125°C temperature range*

Applications:

- *AF power amplifiers for portable and fixed sound and communications systems*
- *Servo-control amplifiers*
- *Wide-band linear mixers*
- *Video power amplifiers*
- *Transmission-line driver amplifiers (balanced and unbalanced)*
- *Fan-in and fan-out amplifiers for computer logic circuits*
- *Lamp-control amplifiers*
- *Motor-control amplifiers*
- *Power multivibrators*
- *Power switches*
- *Companion Application Note, ICAN-5766, "Application of CA3020 and CA3020A Integrated Circuit Multipurpose Wide-Band Power Amplifiers"*

3 OPERATIONAL AMPLIFIERS

The CA3020 and CA3020A are integrated-circuit, multi-stage, multipurpose, wide-band power amplifiers on a single monolithic silicon chip. They employ a highly versatile and stable direct-coupled circuit configuration featuring wide frequency range, high voltage and power gain, and high power output. These features plus inherent stability over a wide temperature range make the CA3020 and CA3020A extremely useful for a wide variety of applications in military, industrial, and commercial equipment.

The CA3020 and CA3020A are particularly suited for service as class B power amplifiers. The CA3020A can provide a maximum power output of 1 watt from a 12-volt dc supply with a typical power gain of 75 dB. The CA3020 provides 0.5-watt power output from a 9-volt supply with the same power gain.

These types are supplied in hermetically sealed TO-5 style 12-lead packages.

SCHEMATIC DIAGRAM FOR CA3020 AND CA3020A

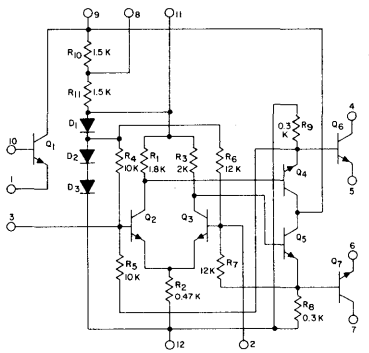


Figure 1

The resistance values included on the schematic diagram have been supplied as a convenience to assist Equipment Manufacturers in optimizing the selection of "outboard" components of equipment designs. The values shown may vary as much as ± 30%.

Harris reserves the right to make any changes in the Resistance Values provided such changes do not adversely affect the published performance characteristics of the device.

ABSOLUTE-MAXIMUM RATINGS:

DISSIPATION:

WITHOUT HEAT SINK	WITH HEAT SINK
At T_A = 25°C . . . . . 1 W	At T_C = 25°C . . . . . 2 W
Above T_A = 25°C . . . . . derate linearly 6.7 mW/°C	At T_C = 25°C to T_C = 55°C . . . . . 2 W
	Above T_C = 55°C . . derate linearly 16.7 mW/°C

TEMPERATURE RANGE:

Operating . . . . . -55°C to +125°C

Storage . . . . . -65°C to +150°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range of the vertical terminal 1 with respect to terminal 12 is 0 to +10 volts.

TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
1		*	*	*	*	*	*	*	▲ 0 -10/-12	+3 Note 1	*	+10 0
2			*	*	*	*	*	*	*	*	*	+2 -2
3				*	*	*	*	*	*	*	*	+2 -2
4					▲ +18/+25 0	*	*	*	*	*	*	▲ +18/+25 0
5						*	*	*	*	*	*	+3 Note 2
6							▲ 0 -18/-25	*	*	*	*	+3 Note 2
7								*	*	*	*	▲ +18/+25 0
8									Note 3	*	*	Note 3 0
9										+10 0	Note 1 0	+10/+12 0
10											*	+10 0
11												*
12												REF. SUB-STRATE

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	-	20
2	-	-
3	-	-
4	300	-
5	-	300
6	-	300
7	300	-
8	-	-
9	20	-
10	1	-
11	20	-
12	-	-

Note 1: This voltage is established by the maximum current rating.

Note 2: The emitters of Q_6 and Q_7 may be returned to a negative voltage supply through emitter resistors. Current into terminal No.9 should not be exceeded and the total device dissipation should not be exceeded.

Note 3: Terminal No.8 may be connected to terminals Nos.9, 11, or 12.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

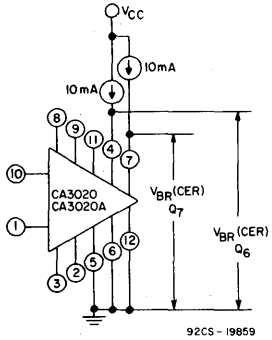
▲ Higher value is for CA3020A.

ELECTRICAL CHARACTERISTICS AT $T_A = 25°C$

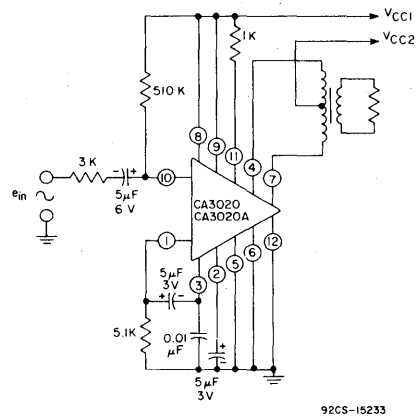
CHARACTERISTICS	SYMBOLS	TEST CONDITIONS			LIMITS CA3020			LIMITS CA3020A			UNITS
		CIRCUIT AND PROCEDURE	DC SUPPLY VOLTAGE								
		FIG.	V_{CC1}	V_{CC2}	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Collector-to-Emitter Breakdown Voltage, Q_6 & Q_7 at 10 mA	$V_{(BR)CER}$	2a	-	-	18	-	-	25	-	-	V
Collector-to-Emitter Breakdown Voltage, Q_1 at 0.1 mA	$V_{(BR)CEO}$	-	-	-	10	-	-	10	-	-	V
Idle Currents, Q_6 & Q_7	I_4 IDLE I_7 IDLE	8	9.0	2.0	-	5.5	-	-	5.5	-	mA
Peak Output Currents, Q_6 & Q_7	I_4PK I_7PK	8	9.0	2.0	140	-	-	180	-	-	mA
Cutoff Currents, Q_6 & Q_7	I_4 CUTOFF I_7 CUTOFF	8	9.0	2.0	-	-	1.0	-	-	1.0	mA
Differetial Amplifier Current Drain	I_{CC1}	8	9.0	9.0	6.3	9.4	12.5	6.3	9.4	12.5	mA
Total Current Drain	I_{CC1} + I_{CC2}	8	9.0	9.0	8.0	21.5	35.0	14.0	21.5	30.0	mA
Differential Amplifier Input Terminal Voltages	V_2 V_3	8	9.0	2.0	-	1.11	-	-	1.11	-	V
Regulator Terminal Voltage	V_{11}	8	9.0	2.0	-	2.35	-	-	2.35	-	V
Q, Cutoff (Leakage) Currents: Collector-to-Emitter	I_{CEO}	-	10.0	-	-	-	100	-	-	100	μA
Emitter-to-Base	I_{EBO}		3.0	-	-	-	0.1	-	-	0.1	
Collector-to-Base	I_{CBO}		3.0	-	-	-	0.1	-	-	0.1	
Forward Current Transfer Ratio, Q_1 at 3 mA	h_{FE1}	-	6.0	-	30	75	-	30	75	-	
Bandwidth at -3 dB Point	BW	9	6.0	6.0	-	8	-	-	8	-	MHz
Maximum Power Output	$P_{O(MAX)}$	10	6.0	6.0	200	300[a]	-	200	300[a]	-	mW
			9.0	9.0	400	550[a]	-	400	550[a]	-	
			9.0	12.0	-	-	-	800	1000[b]	-	
Sensitivity for P_{OUT} = 400 mW	e_{IN}	10	9.0	9.0	-	35[a]	55	-	-	-	mV
Sensitivity for P_{OUT} = 800 mW	e_{IN}	10	9.0	12.0	-	-	-	-	50[b]	100	mV
Input Resistance---- Terminal 3 to Ground	R_{IN3}	11	6.0	6.0	-	1000	-	-	1000	-	Ω
Junction-to-Case Thermal Resistance	θ_{J-C}	-	-	-	-	-	60	-	-	60	°C/W

a R_{CC} = 130 Ω

b R_{CC} = 200 Ω



a. Collector-to-Emitter Breakdown Voltage (Q_6 and Q_7) Circuit



b. Typical Audio Amplifier Circuit Utilizing the CA3020 or CA3020A As An Audio Preamplifier and Class B Power Amplifier

Fig.2

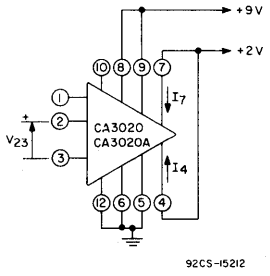
TYPICAL PERFORMANCE DATA*

An External Radiator is Recommended for High Ambient Temperature Operation

CHARACTERISTICS	SYMBOLS	CA3020	CA3020A	UNITS
Power Supply Voltage	V_{CC_1}	9.0	9.0	V
	V_{CC_2}	9.0	12.0	
Zero Signal Current Diff. Ampl.	I_{CC_1}	15	15	mA
Zero Signal Current Output Ampl.	I_{CC_2}	24	24	
Maximum Signal Current Diff. Ampl.	I_{CC_1}	16	16.6	mA
Maximum Signal Current Output Ampl.	I_{CC_2}	125	140	
Maximum Power Output at THD = 10%	P_O	550	1000	mW
Sensitivity	e_{IN}	35	45	mV
Power Gain	G_P	75	75	dB
Input Resistance	R_{IN}	55	55	kΩ
Efficiency	η	45	55	%
Signal-to-Noise Ratio	S/N	70	66	dB
THD at 150 mW level		3.1	3.3	%
Test Signal Frequency from 600Ω Generator		1000	1000	Hz
Equivalent Collector-to-Collector Load Resistance	R_{CC}	130	200	Ω

* Refer to Figs.8 through 12 for Measurement and Symbol Information.

TYPICAL TRANSFER CHARACTERISTICS



a. Test Setup

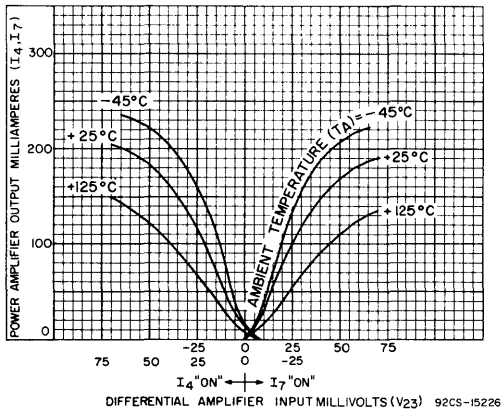
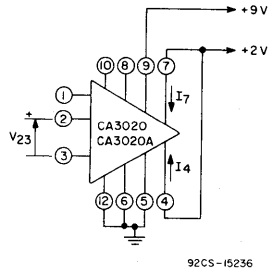


Fig.3 b. Characteristics with R_{10} shorted out



a. Test Setup

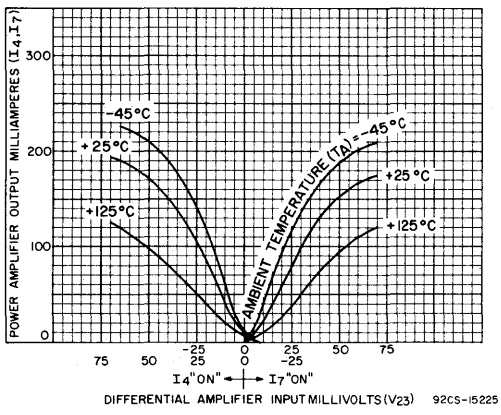
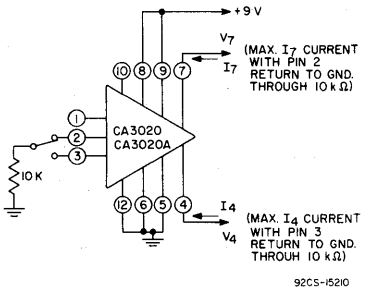


Fig.4 b. Characteristics with R_{10} in circuit

"MINIMUM DRIVE" TYPICAL CURRENT-VOLTAGE SATURATION CURVE



a. Test Setup

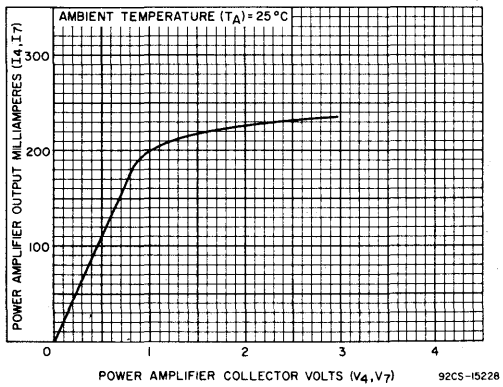
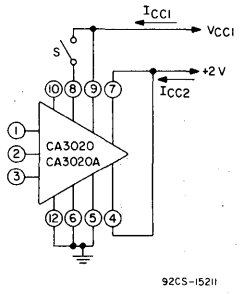
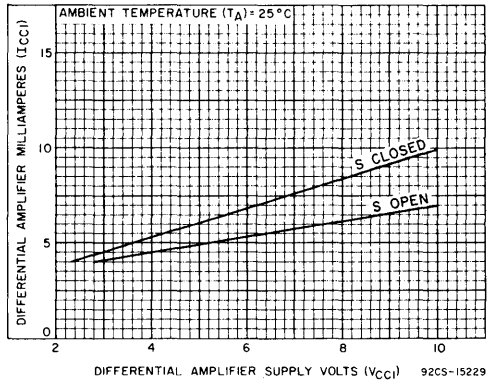


Fig.5 b. Characteristic

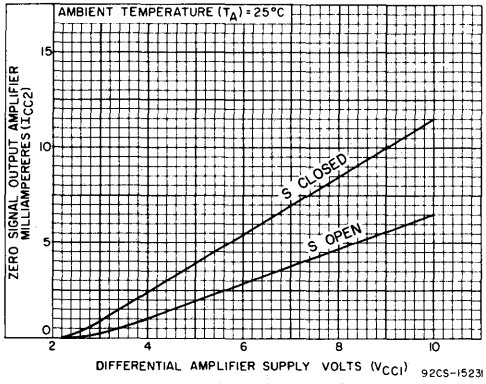
ZERO SIGNAL AMPLIFIER CURRENT vs DIFFERENTIAL AMPLIFIER SUPPLY VOLTAGE



a. Test Setup



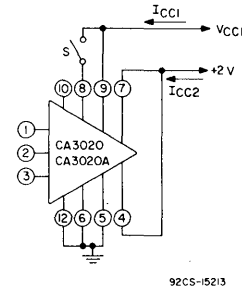
b. Differential Amplifier Characteristics



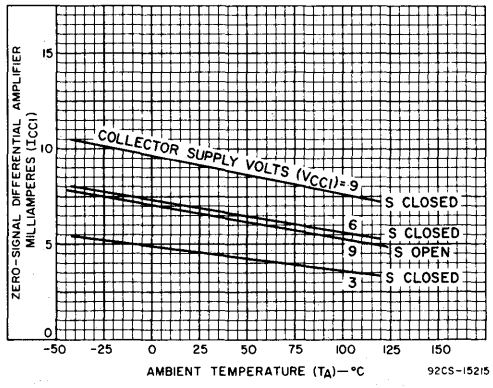
c. Output Amplifier Characteristics

Fig.6

ZERO SIGNAL AMPLIFIER CURRENT
vs AMBIENT TEMPERATURE

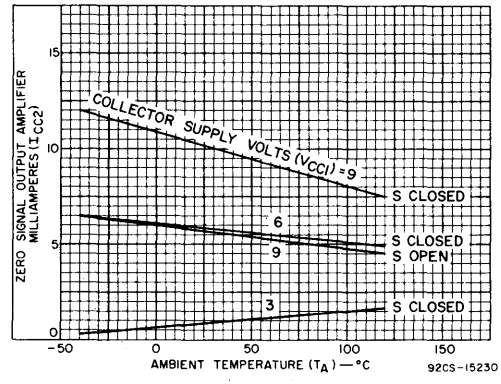


a. Test Setup



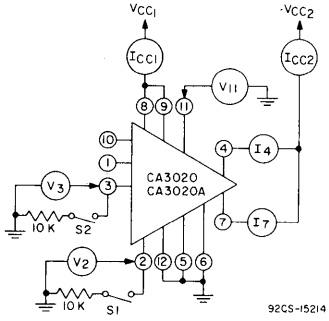
b. Differential Amplifier Characteristics

Fig.7



c. Output Amplifier Characteristics

STATIC CURRENT AND VOLTAGE TEST CIRCUIT



CURRENTS OR VOLTAGES	S1	S2
$I_{4\text{-IDLE}}$	open	open
$I_{7\text{-IDLE}}$	open	open
$I_{4\text{-PEAK}}$	open	close
$I_{7\text{-PEAK}}$	close	open
$I_{4\text{-CUTOFF}}$	close	open
$I_{7\text{-CUTOFF}}$	open	close

CURRENTS OR VOLTAGES	S1	S2
I_{CC1}	open	open
I_{CC2}	open	open
V_2	open	open
V_3	open	open
V_{11}	open	open

Fig.8

MEASUREMENT OF BANDWIDTH AT -3 dB POINTS

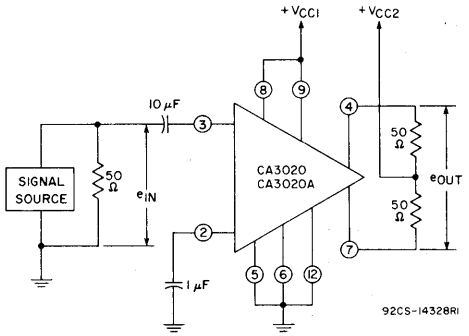
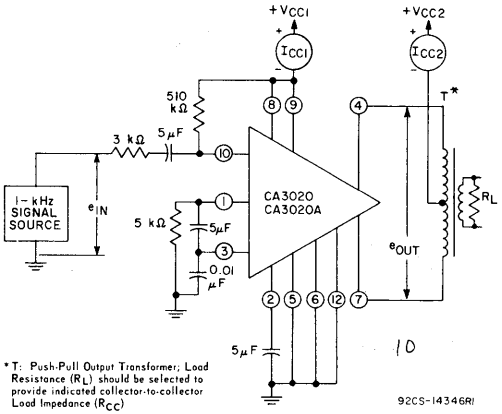


Fig.9

PROCEDURES:

1. Apply desired value of V_{CC_1} and V_{CC_2}
2. Apply 1 kHz input signal and adjust for e_{IN} = 5 mV (rms)
3. Record the resulting value of e_{OUT} in dB (reference value)
4. Vary input-signal frequency, keeping e_{IN} constant at 5 mV, and record frequencies above and below 1 kHz at which e_{OUT} decreases 3 dB below reference value.
5. Record bandwidth as frequency range between -3 dB points.

MEASUREMENTS OF ZERO-SIGNAL DC CURRENT DRAIN, MAXIMUM-SIGNAL DC CURRENT DRAIN, MAXIMUM POWER OUTPUT, CIRCUIT EFFICIENCY, SENSITIVITY, AND TRANSDUCER POWER GAIN



PROCEDURES:

Zero-Signal DC Current Drain

1. Apply desired Value of V_{CC_1} and V_{CC_2} and reduce e_{IN} to 0V
2. Record resulting values of I_{CC_1} and I_{CC_2} in mA as Zero-Signal DC Current Drain.

Fig.10

Maximum-Signal DC Current Drain, Maximum Power Output, Circuit Efficiency, Sensitivity, and Transducer Power Gain

1. Apply desired value of V_{CC_1} and V_{CC_2} and adjust e_{IN} to the value at which the Total Harmonic Distortion in the output of the amplifier = 10%
2. Record resulting value of I_{CC_1} and I_{CC_2} in mA as Maximum-Signal DC Current Drain
3. Determine resulting amplifier power output in watts and record as Maximum Power Output (P_{OUT})
4. Calculate Circuit Efficiency (η) in % as follows:

$$\eta = 100 \frac{P_{OUT}}{V_{CC_1} I_{CC_1} + V_{CC_2} I_{CC_2}}$$

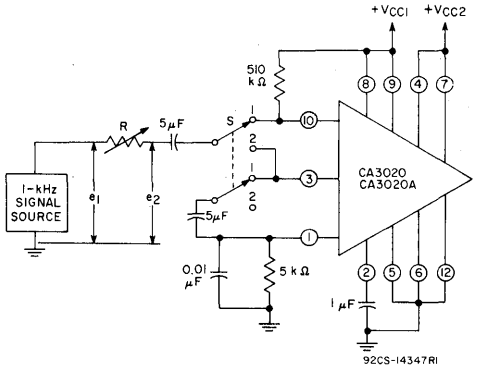
where P_{OUT} is in watts, V_{CC_1} and V_{CC_2} are in volts, and I_{CC_1} and I_{CC_2} are in amperes.

5. Record value of e_{IN} in mV (rms) required in Step 1 as Sensitivity (e_{IN})
6. Calculate Transducer Power Gain (G_p) in dB as follows:

$$G_p = 10 \log_{10} \frac{P_{OUT}}{P_{IN}}$$

where P_{IN} (in mW) $= \dfrac{e_{IN}^2}{3000 + R_{IN(10)}}$

MEASUREMENT OF INPUT RESISTANCE



PROCEDURES:

Input Resistance Terminal 10 to Ground ($R_{IN_{10}}$)

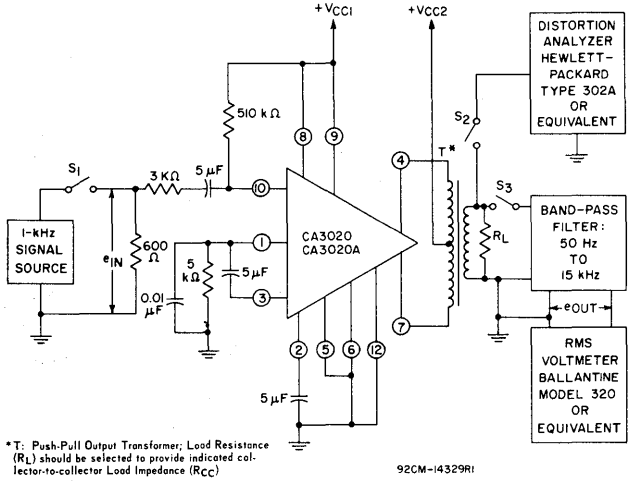
1. Apply desired value of V_{CC_1} and V_{CC_2} and set S in Position 1
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as $R_{IN_{10}}$

Input Resistance Terminal 3 to Ground (R_{IN_3})

1. Apply desired value of V_{CC_1} and V_{CC_2} set S in Position 2
2. Adjust 1-kHz input for desired signal level of measurement
3. Adjust R for $e_2 = e_1/2$
4. Record resulting value of R as R_{IN_3}

Fig.11

MEASUREMENT OF SIGNAL-TO-NOISE RATIO AND TOTAL HARMONIC DISTORTION



*T: Push-Pull Output Transformer; Load Resistance (R_L) should be selected to provide indicated collector-to-collector Load Impedance (R_{CC})

PROCEDURES:

Signal-to-Noise Ratio

1. Close S_1 and S_3; open S_2
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for an amplifier output of 150mW and record resulting value of E_{OUT} in dB as e_{OUT_1} (reference value)
4. Open S_1 and record resulting value of e_{OUT} in dB as e_{OUT_2}
5. Signal-to-Noise Ratio (S/N) = $20\log_{10}\frac{e_{OUT_1}}{e_{OUT_2}}$.

Total Harmonic Distortion

1. Close S_1 and S_2; open S_3
2. Apply desired values of V_{CC_1} and V_{CC_2}
3. Adjust e_{IN} for desired level amplifier output power
4. Record Total Harmonic Distortion (THD) in %

Fig.12

May 1990

Operational Transconductance Amplifier Arrays

Features:

- *Low power consumption - as low as 100 mW per amplifier*
- *Independent biasing for each amplifier*
- *High forward transconductance*
- *Programmable range of input characteristics*
- *Low input bias and input offset current*
- *High input and output impedance*
- *No effect on device under output short-circuit conditions*
- *Zener diode bias regulator*

Applications:

- *For low power conventional operational amplifier applications*
- *Active filters*
- *Comparators*
- *Gyrators*
- *Mixers*
- *Modulators*
- *Multiplexers*
- *Multipliers*
- *Strobing and gating functions*
- *Sample and hold functions*

The CA3060 monolithic integrated circuit consists of an array of three independent Operational Transconductance Amplifiers.* This type of amplifier has the generic characteristics of an operational voltage amplifier with the exception that the forward gain characteristic is best described by transconductance rather than voltage gain (open-loop voltage gain is the product of the transconductance and the load resistance, $g_m R_L$). When operated into a suitable load resistor and with provisions for feedback, these amplifiers are well suited for a wide variety of operational-amplifier and related applications. In addition, the extremely high output impedance makes these types particularly well suited for service in active filter.

The three amplifiers in the CA3060 are identical push-pull Class A types which can be independently biased to achieve a wide range of characteristics for specific application. The electrical characteristics of each amplifier are a function of the amplifier bias current(I_{ABC}). This feature offers the system designer maximum flexibility with regard to output current capability, power consumption, slew rate, input resistance. input bias current, and input offset current. The linear variation of the parameters with respect to bias and the ability to maintain a constant dc level between input and output of each amplifier also makes the CA3060 suitable for a variety of non-linear applications such as mixers, multipliers, and modulators.

In addition, the CA3060 incorporates a unique Zener diode regulator system that permits current regulation below supply voltages normally associated with such systems.

The CA3060 is supplied in a 16-lead dual-in-line plastic package (E suffix) and in chip form (H suffix). This device is operational from -40°C to +85°C.

*Generic applications of the OTA are described in ICAN-6668. For improved input operating ranges, refer to CA3080 and CA3280 data bulletins (File Nos. 475 and 1174) and application notes ICAN-6668 and ICAN-6818.

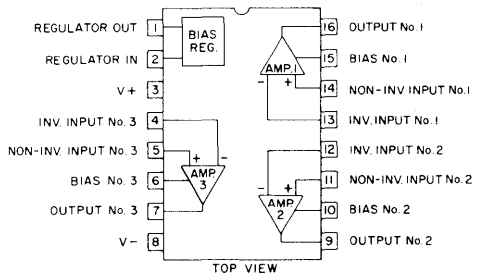


Fig. 1 - Functional block diagram for the CA3060.

ELECTRICAL CHARACTERISTICS at T_A = 25° C, V+ = 15 V, V- = -15 V

CHARACTERISTIC	SYMBOL	TYPICAL CHARACTERISTICS CURVE Fig.	LIMITS Amplifier Bias Current I_{ABC} = 1 A TYP.	I_{ABC} = 10 A TYP.	I_{ABC} = 100 μA MIN.	TYP.	MAX.	UNITS
STATIC CHARACTERISTICS								
Input Offset Voltage	V_{IO}	3	1	1	—	1	5	mV
Input Offset Current	I_{IO}	4	3	30	—	250	1000	nA
Input Bias Current	I_{IB}	5a,b	33	300	—	2500	5000	nA
Peak Output Current	I_{OM}	6a,b	2.3	26	150	240	—	μA
Peak Output Voltage:								
Positive	V_{OM+}	7	13.6	13.6	12	13.6	—	V
Negative	V_{OM-}		14.7	14.7	12	14.7	—	
Amplifier Supply Current (each amplifier)	I_A	8a,b	8.5	85	—	850	1200	μA
Power Consumption (each amplifier)	P	—	0.26	2.6	—	26	36	mW
Input Offset-Voltage Sensitivity■:								
Positive	$\Delta V^{IO}/\Delta V+$	—	1.5	2	—	2	150	uV/V
Negative	$\Delta V^{IO}/\Delta V-$		20	20	—	30	150	
Amplifier Bias Voltage*	V_{ABC}	9	0.54	0.60	—	0.66	—	V
DYNAMIC CHARACTERISTICS (at 1 kHz unless specified otherwise)								
Forward Transconductance (large signal)	921	10a,b	1.55	18	30	102	—	mmho
Common-Mode Rejection Ratio	CMRR	—	110	110	70	90	—	dB
Common-Mode Input Voltage Range	V_{ICR}	—	+12 to -12 min. +13 to -14 typ.	+12 to -12 min. +13 to -14 typ.	+12 to -12 min. +13 to -14 typ.			V
Slew Rate (Test ckt., Fig. 13)	SR	—	0.1	1	—	•	—	V/μs
Open-Loop (g_{21}) Bandwidth	BW_{OL}	11	20	45	—	110	—	kHz
Input Impedance Components:								
Resistance	R_I	12	1600	170	10	20	—	kΩ
Capacitance at 1 MHz	C_I	—	2.7	2.7	—	2.7	—	pF
Output Impedance Components:								
Resistance	R_O	14	200	20	—	2	—	MΩ
Capacitance at 1 MHz	C_O	—	4.5	4.5	—	4.5	pF	
ZENER BIAS REGULATOR CHARACTERISTICS (at T_A = 25° C, I_Z = 0.1 mA)				MIN.	TYP.	MAX.		
Voltage	V_Z	15	Temp. Coeff. = 3mV/° C	6.2	6.7	7.9		V
Impedance	Z_Z	—			200	300		

*Temperature-Coefficient; -2.2 mV/° C (at V_{ABC} = 0.54 V, I_{ABC} = 1 μA; -2.1 mV/° C (at V_{ABC} = 0.060 V, I_{ABC} = 10 μA); -1.9 mV/° C (at V_{ABC} = 0.66 V, I_{ABC} = 100 μA)

■ Conditions for Input Offset Voltage and Supply Sensitivity:

(a) Bias current derived from the regulator with an appropriate resistor connected from terminal No. 1 to the bias terminal on the amplifier under test — V+ is reduced to 13 volts for V+ sensitivity
V- is reduced to -13 volts for V- sensitivity

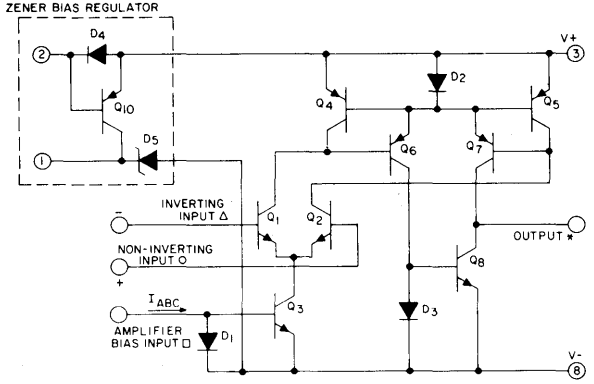
(b) V+ sensitivity in $\mu V/V = \frac{\text{Voffset - Voffset for +13 V and -15 V supplies}}{\text{1 volt}}$

V- sensitivity in $\mu V/V = \frac{\text{Voffset - Voffset for +13 V and -15 V supplies}}{\text{1 volt}}$

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25° C.:*

DC SUPPLY VOLTAGE (BETWEEN V+ and V- TERMINALS)	36V (±18V)
DIFFERENTIAL INPUT VOLTAGE (EACH AMPLIFIER)	±5V
DC INPUT VOLTAGE	V+ to V-
INPUT SIGNAL CURRENT (EACH AMPLIFIER)	±1mA
AMPLIFIER BIAS CURRENT (EACH AMPLIFIER)	2 mA
Bias Regulator Input Current	-5mA
OUTPUT SHORT-CIRCUIT DURATION*	No limitation
DEVICE DISSIPATION	
Up to T_A = 75° C	490mW
Above T_A 75° C	Derate linearly 6.67 mW/° C
TEMPERATURE RANGE	
Operating	-55° C to +125° C
Storage	-65 to +150° C
LEAD TEMPERATURE (During Soldering)	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10s max.	+300° C

*Short circuit may be applied to ground or to either supply



Δ INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 13, 12 AND 4, RESPECTIVELY

O NON-INVERTING INPUT OF AMPLIFIERS 1, 2, AND 3 IS TERMINAL Nos. 14, 11, AND 5, RESPECTIVELY

* OUTPUT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 16, 9, AND 7, RESPECTIVELY

□ AMPLIFIER BIAS CURRENT OF AMPLIFIERS 1, 2, AND 3 IS ON TERMINAL Nos. 15, 10, AND 6, RESPECTIVELY

92CS-15860R1

Fig. 2 — Simplified schematic diagram showing bias regulator and one operational transconductance amplifier for the CA3060.

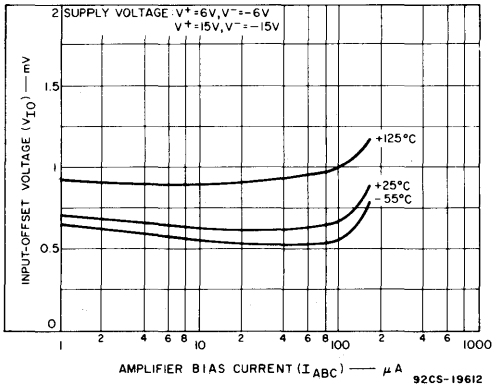


Fig.3—Input offset voltage vs. amplifier bias current.

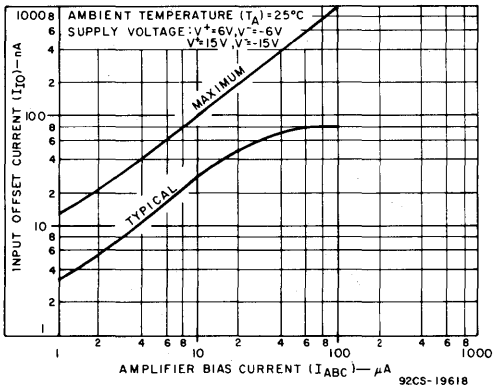


Fig.4—Input offset current vs. amplifier bias current.

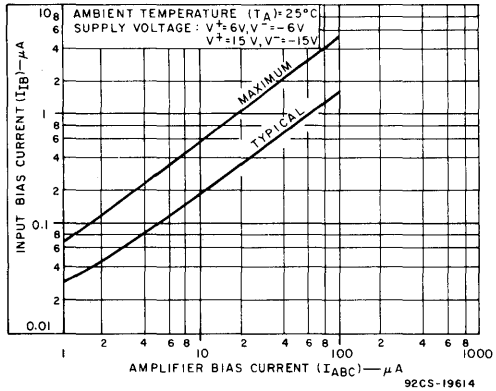


Fig.5a—Input bias current vs. amplifier bias current

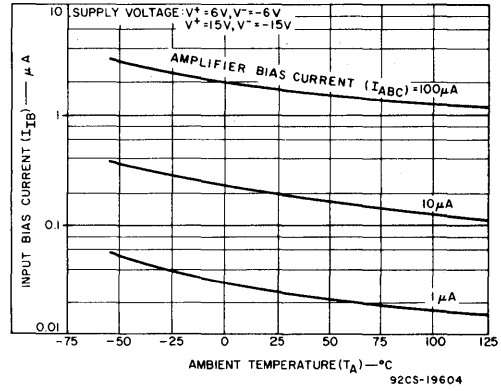


Fig.5b—Input bias current vs. ambient temperature.

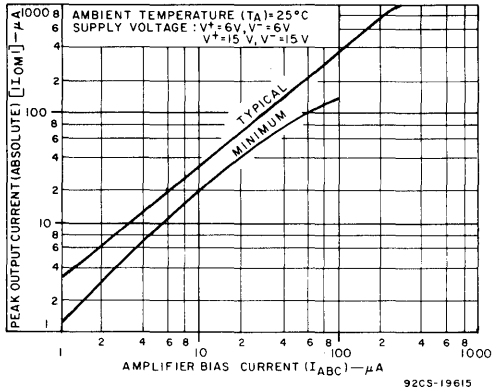


Fig.6a—Peak output current vs. amplifier bias current.

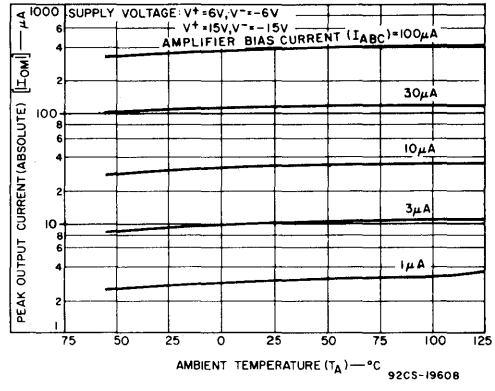


Fig.6b—Peak output current vs. ambient temperature.

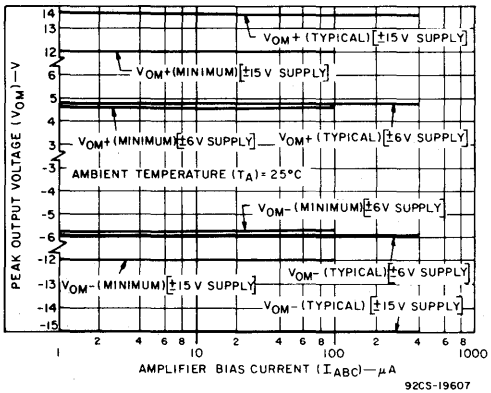


Fig.7—Peak output voltage vs. amplifier bias current.

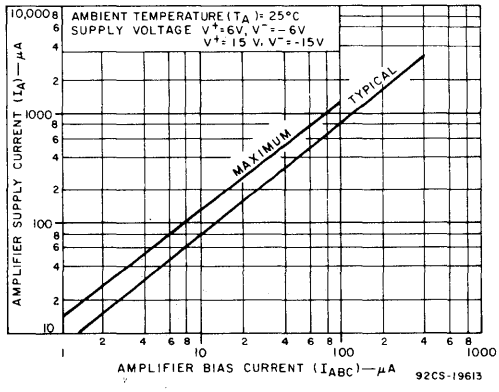


Fig.8a—Amplifier supply current (each amplifier) vs. amplifier bias current.

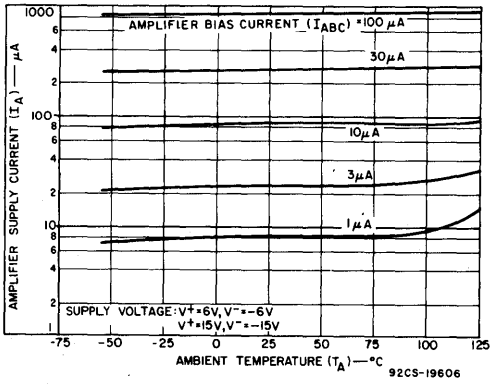


Fig.8b—Amplifier supply current (each amplifier) vs. ambient temperature.

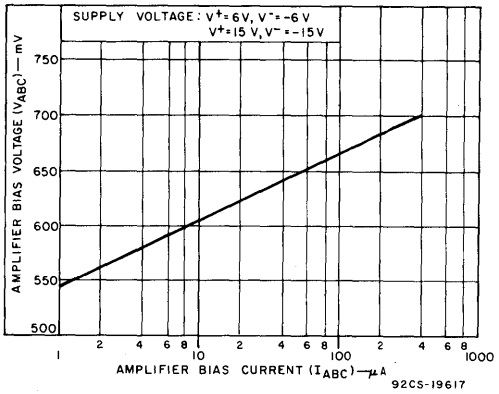


Fig.9—Amplifier bias voltage vs. amplifier bias current.

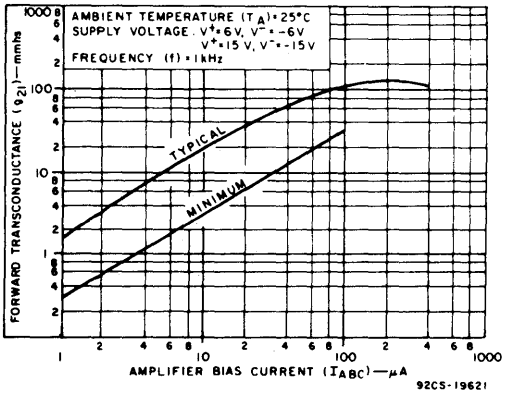


Fig.10a—Forward transconductance vs. amplifier bias current.

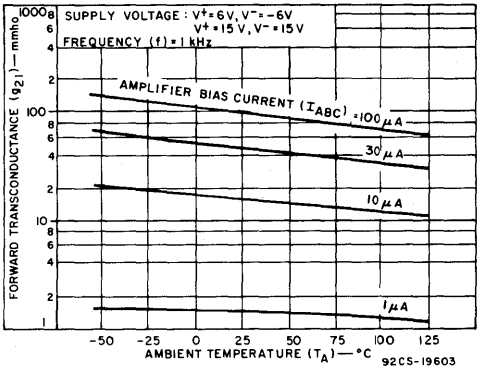


Fig.10b—Forward transconductance vs. ambient temperature.

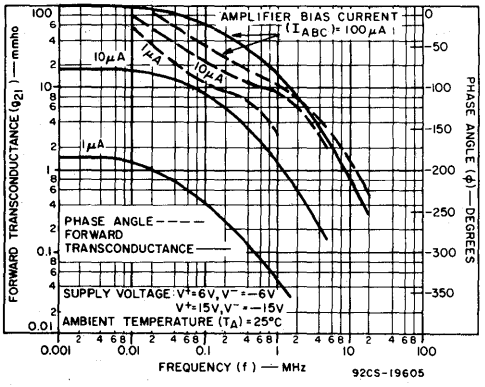


Fig.11—Forward transconductance vs. frequency.

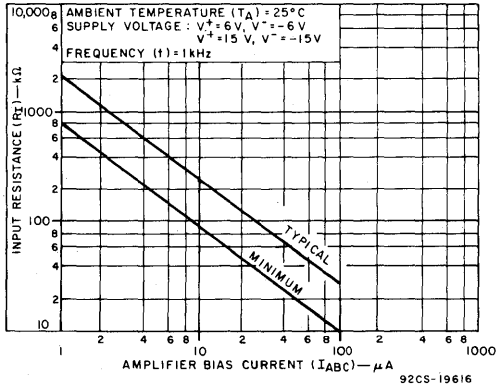
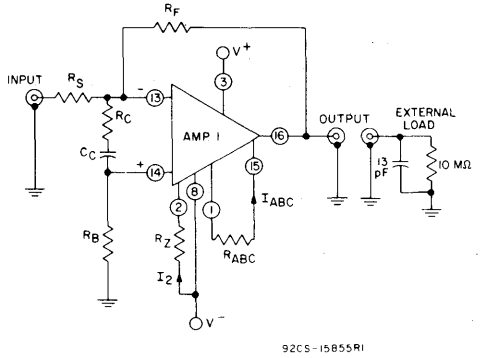


Fig.12—Input resistance vs. amplifier bias current.



V_Z is measured between terminals 1 and 8.

V_{ABC} is measured between terminals 15 and 8.

$$R_Z = \frac{[(V^+)-(V^-)-0.7]}{I_2}, \quad R_{ABC} = \frac{V_Z - V_{ABC}}{I_{ABC}}$$

Supply Voltage: for both ±6 V and ±15 V.

TYPICAL SLEW RATE TEST CIRCUIT PARAMETERS

I_{ABC}	SLEW RATE	I_2	R_{ABC}	R_S	R_F	R_B	R_C	C_C
μA	V/μs	μA	ohms					μF
100	8	200	62 k	100k	100k	51k	100	0.02
10	1	200	620k	1M	1M	510k	1k	0.005
1	0.1	2	6.2M	10M	10M	5.1M	∞	0

Fig. 13—Slew rate test circuit for amplifier No. 1 of CA3060.

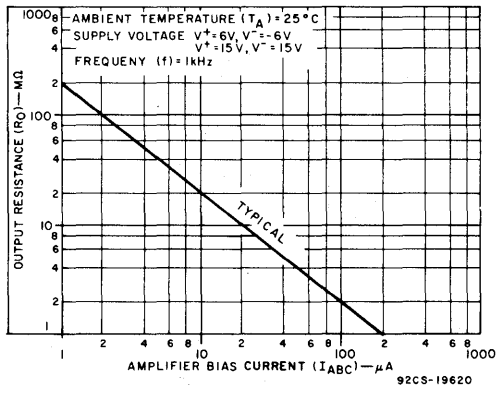


Fig. 14—Output resistance vs. amplifier bias current.

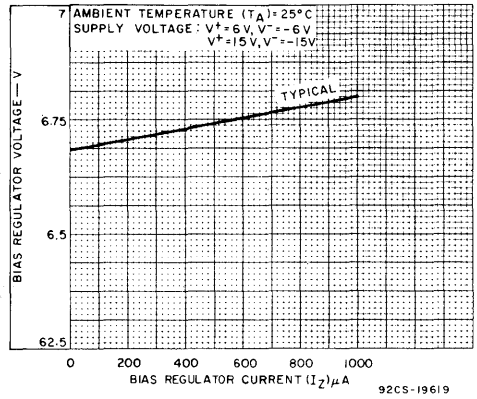


Fig. 15—Bias regulator voltage vs. bias regulator current.

OPERATING CONSIDERATIONS

The CA3060 consists of three operational amplifiers similar in form and application to conventional operational amplifiers but sufficiently different from the standard operational amplifier (op-amp) to justify some explanation of their characteristics. The amplifiers incorporated in the CA3060 are best described by the term Operational Transconductance Amplifier (OTA). The characteristics of an ideal OTA are similar to those of an ideal op-amp except that the OTA has an extremely high output impedance. Because of this inherent characteristic the output signal is best defined in terms of current which is proportional to the difference between the voltages of the two input terminals. Thus, the transfer characteristic is best described in terms of transconductance rather than voltage gain. Other than the difference given above, the characteristics tabulated on pages 3 and 4 of this data bulletin are similar to those of any typical op-amp.

The OTA circuitry incorporated in the CA3060 (See Fig. 16) provides the equipment designer with a wider variety of circuit arrangements than does the standard op-amp; because as the curves in the data bulletin indicate, the user may select the optimum circuit conditions for a specific application simply by varying the bias conditions of each amplifier. If low power consumption, low bias, and low offset current, or high input impedance are primary design requirements, then low current operating conditions may be selected. On the other hand, if operation into a moderate load impedance is the primary consideration, then higher levels of bias may be used.

Bias Considerations for Op-Amp Applications

The operational transconductance amplifiers allow the circuit designer to select and control the operating conditions of the circuit merely by the adjustment of the input bias current I_{ABC}. This enables the designer to have complete control over transconductance, peak output current and total power consumption independent of supply voltage.

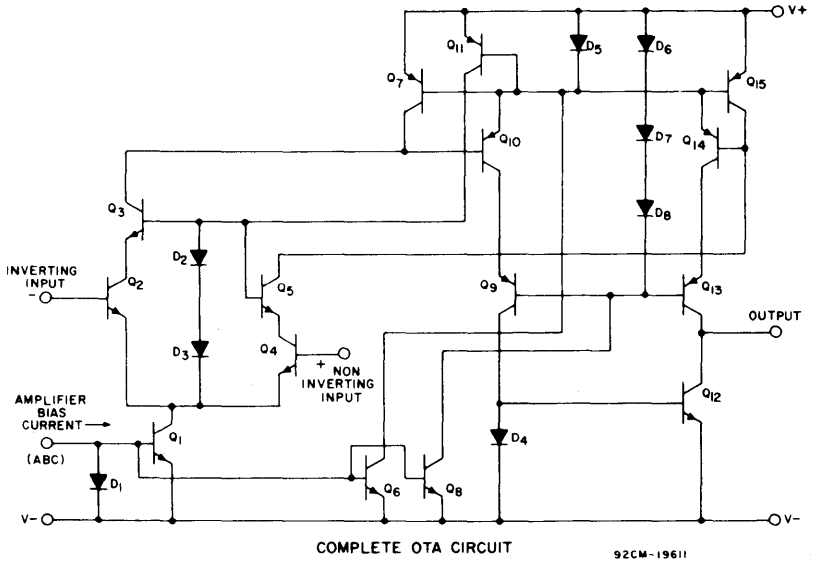


Fig. 16—Complete schematic diagram showing bias regulator and one of the three operational transconductance amplifiers.

In addition, the high output impedance makes these amplifiers ideal for applications where current summing is involved.

The design of a typical operational amplifier circuit (See Fig. 17) would proceed as follows:

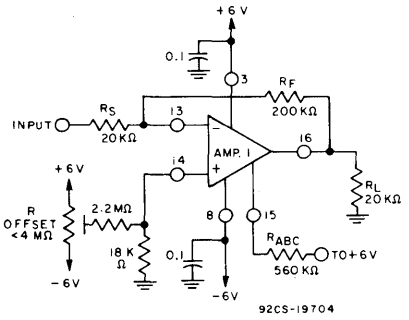


Fig. 17—20-dB amplifier using the CA3060.

Circuit Requirements
Closed loop voltage gain = 10 (20 dB)
Offset voltage adjustable to zero
Current drain as low as possible
Supply voltage = ±6 V
Maximum input voltage = ±50 mV
Input resistance = 20 kΩ
Load resistance = 20 kΩ
Device: CA3060

Calculation

1. Required transconductance g_{21}.
   Assume that the open loop gain A_{OL} must be at least ten times the closed loop gain. Therefore, the forward transconductance required is given by

$$g_{21} = A_{OL}/R_L$$

$$= 100/18\ k\Omega$$

$$\cong 5.5\ mmho$$

(R_L = 20 kΩ in parallel with 200 kΩ

≅ 18 kΩ)

2. Selection of suitable amplifier bias current.
   The amplifier bias current is selected from the minimum value curve of transconductance (Fig. 10a) to assure that the amplifier will provide sufficient gain. For the required g_{21} of 5.5 mmho an amplifier bias current I_{ABC} of 20 μA is suitable.

3. Determination of Output Swing Capability.
   For a loop gain of 10 the output swing is ±0.5 V and the peak load current 25 μA. However, the amplifier must also supply the necessary current through the feedback resistor and for R_S = 20 kΩ than R_F = 200 kΩ if A_{OL} = 10. Therefore, the feedback loading = 0.5/200 kΩ = 2.5 μA.

   The total amplifier current output requirements are, therefore, ±27.5 μA. Referring to the data given in Fig. 6a we see that for an amplifier bias current of 20 μA the amplifier output current is ±40 μA. This is obviously adequate and it is not necessary to change the amplifier bias current I_{ABC}.

4. Calculation of bias resistance.
   For minimum supply current drain the amplifier bias current I_{ABC} should be fed directly from the supplies and not from the bias regulator. The value of the resistor R_{ABC} may be directly calculated using Ohm's law.

$$R_{ABC} = \frac{V_{SUP} - V_{ABC}}{I_{ABC}}$$

$$R_{ABC} = \frac{12 - 0.63}{20 \times 10^{-6}}$$

$$= 568.5\ k\Omega \text{ or} \cong 560\ k\Omega$$

5. Calculation of offset adjustment circuit.
   In order to reduce the loading effect of the offset adjustment circuit on the power supply, the offset control should be arranged to provide the necessary offset current. The source resistance of the non-inverting input is made equal to the source resistance of the inverting input.

   i.e. $\frac{20 \times 200 \times 10^6 \text{ ohms}}{220 \times 10^3} \cong 18\ k\Omega$

Because the maximum offset voltage is 5 mV and an additional increment due to the offset current (Fig. 4) flowing through the source resistance

(i.e. $200 \times 10^{-9} \times 18 \times 10^3$ volts), therefore,

the Offset Voltage Range = 5 mV + 3.6 mV = ±8.6 mV

The current necessary to provide this offset is

$$\frac{8.6 \times 10^{-3}}{18 \times 10^3} \text{ or } 0.48\ \mu A$$

With a supply voltage of ±6 V, this current can be provided by a 10 MΩ resistor. However, the stability of such a resistor is often questionable and a more realistic value of 2.2 MΩ was used in the final circuit.

OTHER CONSIDERATIONS

Capacitance Effects

The CA3060 is designed to operate at such low power levels that high impedance circuits must be employed. In designing such circuits, particularly feedback amplifiers, stray circuit capacitance must always be considered because of its adverse effect on frequency response and stability. For example a 10-kΩ load with a stray capacitance of 15 pF has a time constant of 1 MHz. Fig. 18 illustrates how a 10-kΩ 15-pF load modifies the frequency characteristic.

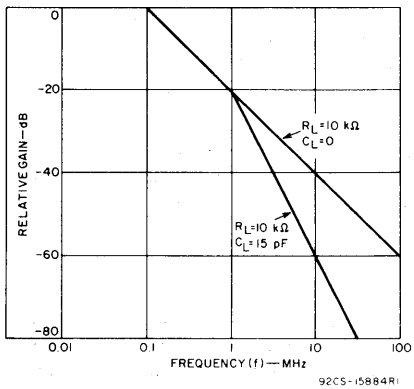


Fig. 18—Effect of capacitive loading on frequency response.

Capacitive loading also has an effect on slew rate; because the peak output current is established by the amplifier bias current, I_{ABC} (see Fig. 6a), the maximum slew rate is limited to the maximum rate at which the capacitance can be charged by the I_{OM}. Therefore,

$$SR = dV/dt = I_{OM}/C_L$$

where C_L is the total load capacitance including strays. This relationship is shown graphically in Fig. 19. When measuring slew rate for this data bulletin, care was taken to keep the total capacitive loading to 13 pF.

Phase Compensation

In many applications phase compensation will not be required for the amplifiers of the CA3060. When needed, compensation may easily be accomplished by a simple RC network at the input of the amplifier as shown in Fig. 13. The values given in Fig. 13 provide stable operation for the critical unity gain condition, assuming that capacitive loading on the output is 13 pF or less. Input phase compensation is recommended in order to maintain the highest possible slew rate.

In applications such as integrators, two OTAs may be cascaded to improve current gain. Compensation is best accomplished in this case with a shunt capacitor at the output of the first amplifier. The high gain following compensation assures a high slew rate.

APPLICATIONS

Having determined the operating points of the CA3060 amplifiers, they can now function in the same manner as conventional op-amps, and thus, are well suited for most op-amp applications, including inverting and non-inverting amplifiers, integrators, differentiators, summing amplifiers etc.

TRI-LEVEL COMPARATOR

Tri-level comparator circuits are an ideal application for the CA3060 since it contains the requisite three amplifiers. A tri-level comparator has three adjustable limits. If either the upper or lower limit is exceeded, the appropriate output is activated until the input signal returns to a selected intermediate limit. Tri-level comparators are particularly suited to many industrial control applications.

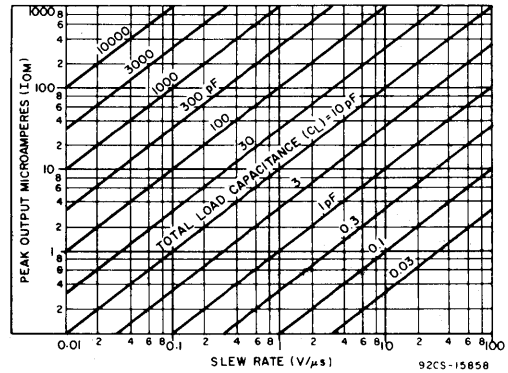


Fig. 19—Effect of load capacitance on slew rate.

Circuit Description

Fig. 20 shows the block diagram of a tri-level comparator using the CA3060. Two of the three amplifiers are used to compare the input signal with the upper-limit and lower-limit reference voltages. The third amplifier is used to compare the input signal with a selected value of intermediate-limit reference voltage. By appropriate selection or resistance ratios this intermediate-limit may be set to any voltage between the upper-limit and lower-limit values. The output of the upper-limit and lower-limit comparator sets the corresponding upper or lower-limit flip-flop. The activated flip-flop retains its state until the third comparator (intermediate-limit) in the CA3060 initiates a reset function, thereby indicating that the signal voltage has returned to the intermediate-limit selected. The flip-flops employ two CA3086 transistor-array IC's, with circuitry to provide separate "SET" and "POSITIVE OUTPUT" terminals.

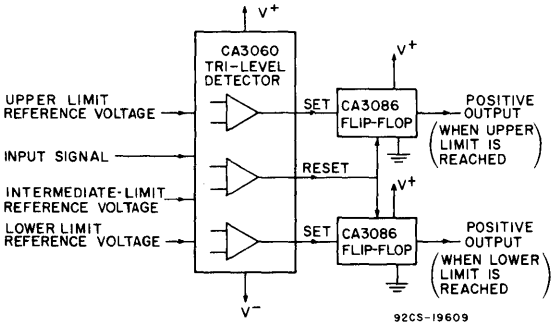


Fig.20—Functional block diagram of a tri-level comparator.

The circuit diagram of a tri-level comparator appears in Fig. 21. Power is provided for the CA3060 via terminals 3 and 8 by ±6-volt supplies and the built-in regulator provides amplifier-bias-current (I_{ABC}) to the three amplifiers via terminal 1. Lower-limit and upper-limit reference voltages are selected by appropriate adjustment of potentiometers R1 and R2, respectively. When resistors R3 and R4 are equal in value (as shown), the intermediate-limit reference voltage is automatically established at a value midway between the lower-limit and upper-limit values. Appropriate variation of resistors R3 and R4 permits selection of other values of intermediate-limit voltages. Input signal (E_S) is applied to the three comparators via terminals 5, 12, and 14. The "SET" output lines trigger the appropriate flip-flop whenever the input signal reaches a limit value. When the input signal returns to an intermediate-value, the common flip-flop "RESET" line is energized. The loads in the circuits, shown in Fig. 21 are 5-V, 25-mA lamps.

Active Filters – Using the CA3060 as a Gyrator

The high output impedance of the OTAs makes the CA3060 ideally suited for use as a gyrator in active filter applications. Fig. 22 shows two OTAs of the CA3060 connected as a gyrator in an active filter circuit. The OTAs in this circuit can make a 3-μF capacitor function as a floating 10-kilohenry inductor across Terminals A and B. The measured Q of 13 (at a frequency of 1 Hz) of this inductor compares favorably with a calculated Q of 16. The 20-kilohm to 2-megohm attenuators in this circuit extend the dynamic range of the OTA by a factor of 100. The 100-kilohm potentiometer, across V+ and V⁻, tunes the inductor by varying the g_{21} of the OTAs, thereby changing the gyration resistance.

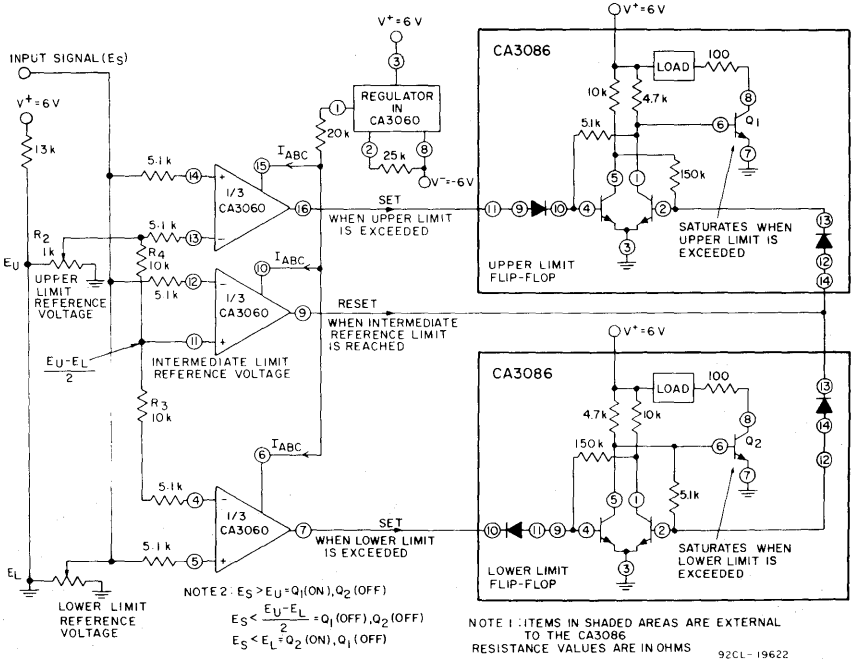


Fig.21—Tri-level comparator circuit.

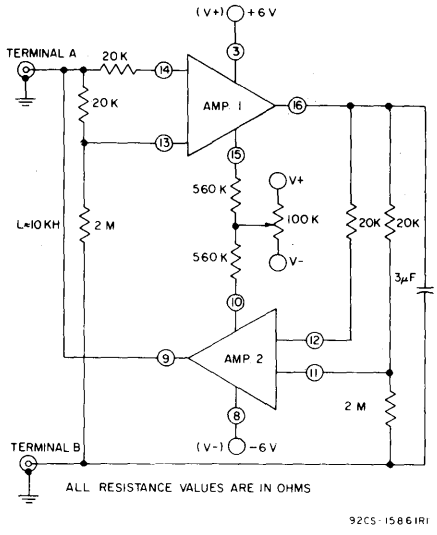


Fig.22—Two operational transconductance amplifiers of the CA3060 connected as a gyrator in an active filter circuit.

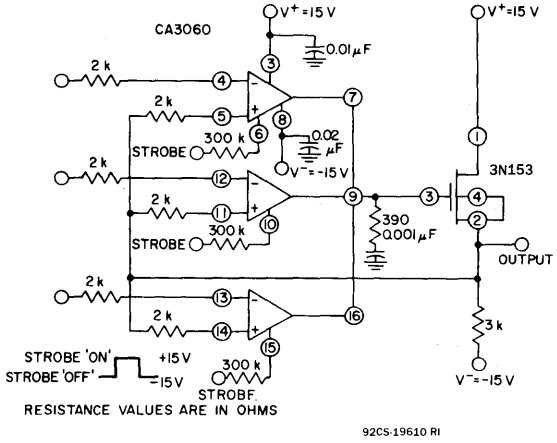


Fig.23—Three-channel multiplexer.

THREE CHANNEL MULTIPLEXER

Fig. 23 shows a schematic of a three channel multiplexer using a single CA3060 and a 3N153 MOS/FET as a buffer and power amplifier.

When the CA3060 is connected as a high-input impedance voltage follower, and strobe "ON," each amplifier is activated and the output swings to the level of the input of that amplifier. The cascade arrangement of each CA3060 amplifier with the MOS/FET provides an open loop voltage gain in excess of 100 dB, thus assuring excellent accuracy in the voltage follower mode with 100% feedback.

Operation at ±6 volts is also possible with several minor changes. First, the resistance in series with amplifier bias current (I_{ABC}) terminal of each amplifier should be decreased to maintain 100 μA of strobe—"ON" current at this lower supply voltage. Second, the drain resistance for the MOS/FET should be decreased to maintain the same value of source current. The low cost dual-gate protected MOS/FET, RCA-40841, may be used when operating at the low supply voltage.

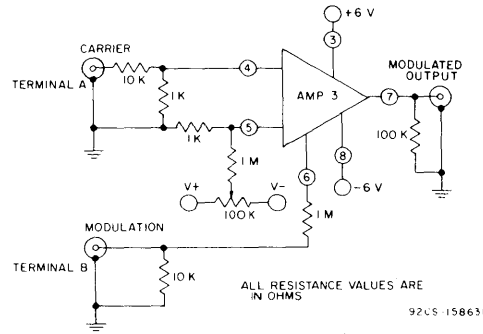
The phase compensation network consists of a single 390Ω resistor and a 1000-pF capacitor, located at the interface of the CA3060 output and the MOS/FET gate. The bandwidth of the system is 1.5 MHz and the slew rate is 0.3 volts/μsec. The system slew rate is directly proportional to the value of the phase compensation capacitor. Thus, with higher gain settings where lower values of phase compensation capacitors are possible, the slew rate is proportionally increased.

NON LINEAR APPLICATIONS

AM Modulator (Two-Quadrant Multiplier)

Fig. 24 shows Amplifier No. 3 of the CA3060 used in an AM modulator or 2-quadrant multiplier circuit. When modulation is applied to the amplifier bias input, Terminal B, and the carrier frequency to the differential input, Terminal A, the waveform, shown in Fig. 24, is obtained. Fig. 24 is a result of adjusting the input offset control to balance the circuit so that no modulation can occur at the output without a carrier input. The linearity of the modulator is indicated by the solid trace of the superimposed modulating frequency. The maximum depth of modulation is determined by the ratio of the peak input modulating voltage to V^-.

The two-quadrant multiplier characteristic of this modulator is easily seen if modulation and carrier are reversed as shown in Fig. 24. The polarity of the output must follow that of the differential input; therefore, the output is positive only during, the positive half cycle of the modulation and negative only in the second half cycle. Note, that both the input and output signals are referenced to ground. The output signal is zero when either the differential input or I_{ABC} are zero.



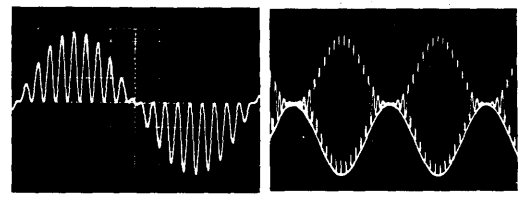


Fig.24—Two-quadrant multiplier circuit using the CA3060 with associated waveforms.

Four-Quadrant Multiplier

The CA3060 is also useful as a four-quadrant multiplier. A block diagram of such a multiplier, utilizing Amplifier Nos. 1, 2, and 3, is shown in Fig. 25 and a typical circuit is shown in Fig. 26. The multiplier consists of a single CA3060 and, as in the two-quadrant multiplier, exhibits no level shift between input and output. In Fig. 25, Amplifier No. 1 is connected as an inverting amplifier for the X-input signal. The output current of Amplifier No. 1 is calculated as follows:

$$I_O(1) = [-V_X]\ [g_{21}(1)] \qquad \text{(Eq.3)}$$

Ampl. No. 2 is a non-inverting amplifier so that

$$I_O(2) = [+V_X]\ [g_{21}(2)] \qquad \text{(Eq. 4)}$$

Because the amplifier output impedances are high, the load current is the sum of the two output currents, for an output voltage

$$V_O = V_X R_L\ [g_{21}(2) - g_{21}(1)] \qquad \text{(Eq. 5)}$$

The transconductance is approximately proportional to the amplifier bias current; therefore, by varying the bias current the g_{21} is also controlled. Amplifier No. 2 bias current is proportional to the Y-input signal and is expressed as

$$I_{ABC(2)} \approx \frac{(V\text{-}) + V_Y}{R_1} \qquad \text{(Eq. 6)}$$

Hence,

$$g_{21}(2) \approx k\ [\ (V\text{-}) + V_Y\ ]. \qquad \text{(Eq. 7)}$$

Bias for Amplifier No. 1 is derived from the output of Amplifier No. 3 which is connected as a unity-gain inverting amplifier. $I_{ABC(1)}$, therefore, varies inversely with V_Y. And by the same reasoning as above

$$g_{21}(1) \approx k\ \ [(V\text{-}) - V_Y]\ . \qquad \text{(Eq. 8)}$$

Combining equation 5, 7, and 8 yields:

$$V_O \approx V_X \cdot k \cdot R_L \left\{[(V\text{-}) + V_Y] - [(V\text{-}) - V_Y]\right\} \text{ or}$$

$$V_O \approx 2\,k\,R_L\,V_X\,V_Y$$

Fig. 26 shows the actual circuit including all the adjustments associated with differential input and an adjustment for equalizing the gains of Amplifiers No. 1 and No. 2. Adjustment of the circuit is quite simple. With both the X and Y voltages at zero, connect Terminal 10 to Terminal 8. This procedure disables Amplifier No. 2 and permits adjusting the offset voltage of Amplifier No. 1 to zero by means of the 100-kΩ potentiometer. Next, remove the short between Terminals 10 and 8 and connect Terminal 15 to Terminal 8. This step disables Amplifier No. 1 and permits Amplifier No. 2 to be zeroed with the other potentiometer. With AC signals on both the X and Y input, R3 and R11 are adjusted for symmetrical output signals. Fig. 27 shows the output waveform with the multiplier adjusted. The voltage waveform in Fig. 27a shows suppressed carrier modulation of 1-kHz carrier with a triangular wave.

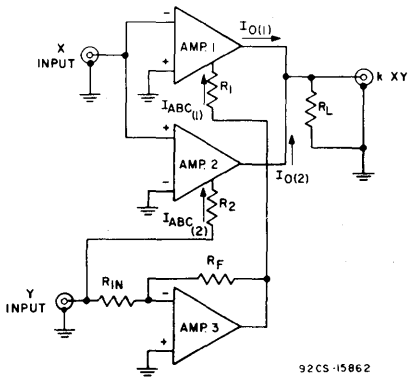


Fig.25—Four-quadrant multiplier using the CA3060.

Figures 27b and 27c, respectively, show the squaring of a triangular wave and a sine wave. Notice that in both cases the outputs are always positive and return to zero after each cycle.

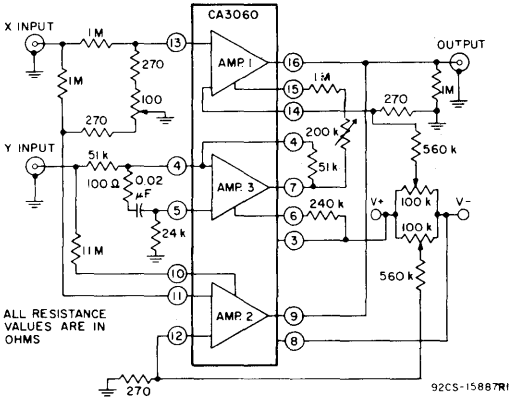


Fig.26—Typical four-quadrant multiplier circuit.

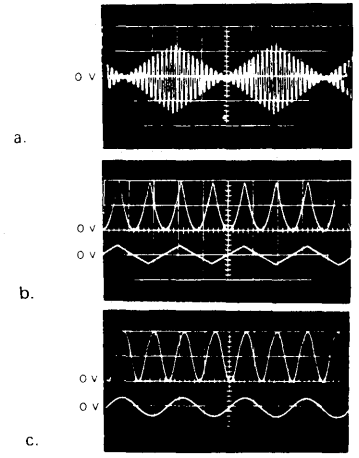


Fig.27—Voltage waveforms of four-quadrant multiplier circuit.

May 1990

Micropower Operational Amplifier

Features:

- *Low standby power: as low as 700nW*
- *Wide supply voltage range: ±0.75 to ±15 V*
- *High peak output current: 6.5 mA min.*
- *Adjustable quiescent current*
- *Output short-circuit protection*

Applications:

- *Portable electronics*
- *Medical electronics*
- *Instrumentation*
- *Telemetry*
- *Intrusion alarms*

The CA3078 and CA3078A are high-gain monolithic operational amplifiers which can deliver milliamperes of current yet only consume microwatts of standby power. Their operating points are externally adjustable and frequency compensation may be accomplished with one external capacitor. The CA3078 and CA3078A provide the designer with the opportunity to tailor the frequency response and improve the slew rate without sacrificing power. Operation with a single 1.5-volt battery is a practical reality with these devices.

The CA3078A is a premium device having a supply voltage range of V± = 0.75 to V± = 15 V and an operating temperature range of -25°C to +125°C. The CA3078 has the same lower supply voltage limit but the upper limit is V+ = +6 V and V- = -6 V. The operating temperature range is from 0°C to +70°C.

The CA3078 and CA3078A are supplied in the 8-lead Small Outline package (M suffix), the standard 8-lead TO-5 package ("T" suffix), the 8-lead dual-in-line formed-lead "DIL-CAN" package ("S" suffix), or the 8-lead dual-in-line plastic "MINI-DIP" package ("E" suffix).

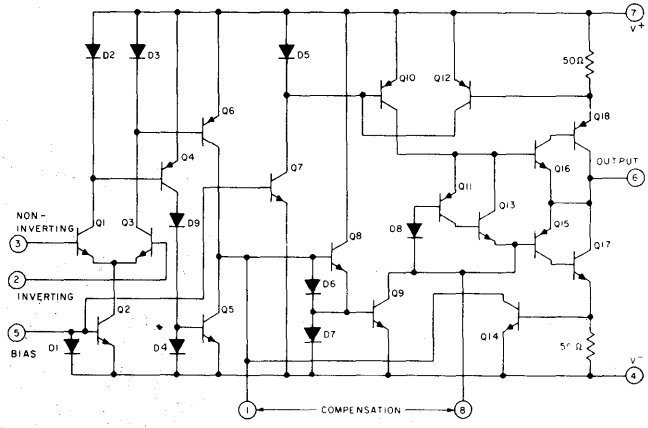


Fig. 1 - Schematic diagram of the CA3078 and CA3078A.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

	CA3078A	CA3078
DC Supply Voltage (between V^+ and V^- terminal	36 V	14 V
Differential Input Voltage	±6 V	±6 V
DC Input Voltage	V^+ to V^-	V^+ to V^-
Input Signal Current	0.1 mA	0.1 mA
Output Short-Circuit Duration*	No Limitation	No Limitation
Device Dissipation	150 mW (up to 125°C)	500 mW (up to 70°C)
Temperature Range:		
Operating	−55 to +125°C	0 to +70°C
Storage	−65 to +150°C	−65 to +150°C
Lead Temperature (During Soldering):		
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10s max.	+300°C	+300°C

* Short circuit may be applied to ground or to either supply.

ELECTRICAL CHARACTERISTICS For Equipment Design

CHARACTERISTICS SYMBOLS	TEST CONDITIONS			CA3078A LIMITS					CA3078 LIMITS					UNITS
				R_{SET} = 5.1 MΩ					R_{SET} = 1 MΩ					
				T_A = 25°C			T_A = −55 to 125°C		T_A = 25°C			T_A = 0 to 70°C		
	V^+ & V	R_S kΩ	R_L kΩ	MIN.	TYP.	MAX.	MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
V_{IO}	6	≤10	–	–	0.70	3.5	–	4.5	–	1.3	4.5	–	5	mV
V_{IO}		–	–	–	0.50	2.5	–	5.0	–	6	32	–	40	nA
I_{IB}		–	–	–	7	12	–	50	–	60	170	–	200	nA
A_{OL}		–	≥10	92	100	–	90	–	88	92	–	86	–	dB
I_Q		–	–	–	20	25	–	45	–	100	130	–	150	μA
P_D		–	–	–	240	300	–	540	–	1200	1560	–	1800	μW
V_{OM}		–	≥10	±5.1	±5.3	–	±5	–	±5.1	±5.3	–	±5	–	V
V_{ICR}		≤10	–	–	−5.5 to +5.8	–	−5 to +5	–	–	−5.5 to +5.8	–	−5 to +5	–	V
CMRR		≤10	–	80	115	–	–	–	80	110	–	–	–	dB
I_{OM}^+ or I_{OM}^-		–	–	–	12	–	6.5	30	–	12	–	6.5	30	mA
$\Delta V_{IO}/\Delta V^+$		≤10		76	105	–	–	–	76	93	–	–	–	μV/V
$\Delta V_{IO}/\Delta V^-$			–	76	105	–	–	–	76	93	–	–	–	
				R_{SET} = 13 MΩ,										
V_{IO}	15	≤10	–	–	1.4	3.5	–	4.5	–	–	–	–	–	mV
A_{OL}		–	≥10	92	100	–	88	–	–	–	–	–	–	dB
I_Q		–	–	–	20	30	–	50	–	–	–	–	–	μA
P_D		–	–	–	600	750	–	1350	–	–	–	–	–	μW
V_{OM}		–	≥10	±13.7	±14.1	–	±13.5	–	–	–	–	–	–	V
CMRR		≤10	–	80	106	–	–	–	–	–	–	–	–	dB
I_{IB}		–	–	–	7	14	–	55	–	–	–	–	–	nA
I_{IO}		–	–	–	0.50	2.7	–	5.5	–	–	–	–	–	nA

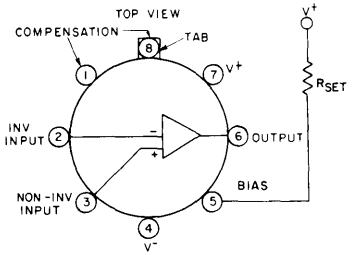
ELECTRICAL CHARACTERISTICS, *at $T_A = 25°C$*

Typical Values Intended Only for Design Guidance

CHARACTERISTICS SYMBOLS	TYPICAL VALUES				UNITS
	CA3078A		CA3078		
	$V^+ = +1.3$ V, $V^- = -1.3$ V $R_{SET} = 2$ MΩ	$V^+ = +0.75$ V, $V^- = -0.75$ V $R_{SET} = 10$ MΩ	$V^+ = +1.3$ V, $V^- = -1.3$ V $R_{SET} = 2$ MΩ	$V^+ = +0.75$ V, $V^- = -0.75$ V $R_{SET} = 10$ MΩ	
V_{IO}	0.7	0.9	1.3	1.5	mV
I_{IO}	0.3	0.054	1.7	0.5	nA
I_{IB}	3.7	0.45	9	1.3	nA
A_{OL}	84	65	80	60	dB
I_Q	10	1	10	1	μA
P_D	26	1.5	26	1.5	μW
V_{OPP}	1.4	0.3	1.4	0.3	V
V_{ICR}	−0.8 to +1.1	−0.2 to +0.5	−0.8 to +1.1	−0.2 to +0.5	V
CMRR	100	90	100	90	dB
$I_{OM}^{\pm}$	12	0.5	12	0.5	mA
$\Delta V_{IO}/\Delta V^{\pm}$	20	50	20	50	μV/V

Typical Values Intended Only for Design Guidance *at $T_A = 25°C$ and $V^+ = +6$ V, $V^- = -6$ V*

CHARACTERISTICS SYMBOLS	TEST CONDITIONS	CA3078A		CA3078	UNITS
		$R_{SET} = 5.1$ MΩ	$R_{SET} = 1$ MΩ	$R_{SET} = 1$ MΩ	
$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ kΩ	5	6	6	μV/°C
$\Delta V_{IO}/\Delta T_A$	$R_S \leq 10$ kΩ	6.3	70	70	pA/°C
BW_{OL}	3dB pt.	0.3	2	2	kHz
SR	See Figs. 20, 21	0.027	0.04	0.04	V/μs
		0.5	1.5	1.5	
–	10% to 90% Rise Time	3	2.5	2.5	μs
R_I		7.4	1.7	0.87	MΩ
R_O		1	0.8	0.8	kΩ
e_N(10 Hz)	$R_S = 0$	40	–	25	$nV/\sqrt{Hz}$
i_N(10 Hz)	$R_S = 1$ MΩ	0.25	–	1	$pA/\sqrt{Hz}$



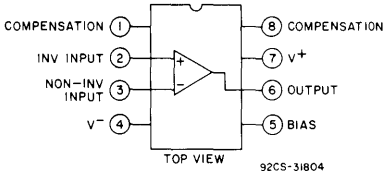


Fig. 2 – Functional diagrams.

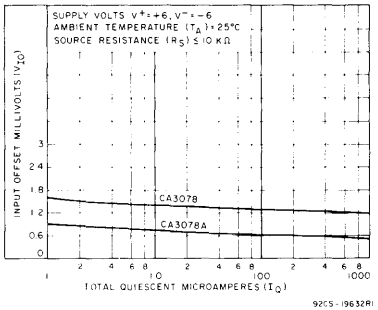


Fig. 3 – Input offset voltage vs. total quiescent current.

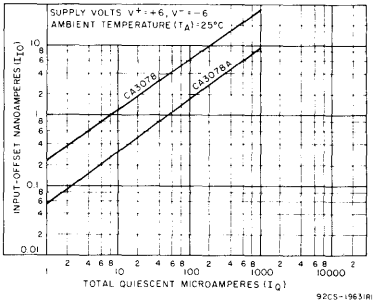


Fig. 4 – Input offset current vs. total quiescent current.

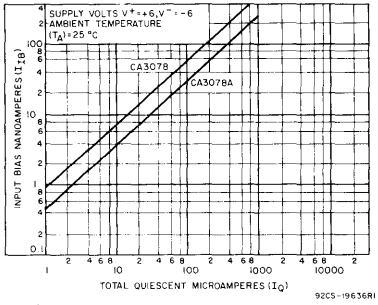


Fig. 5 – Input bias current vs. total quiescent current.

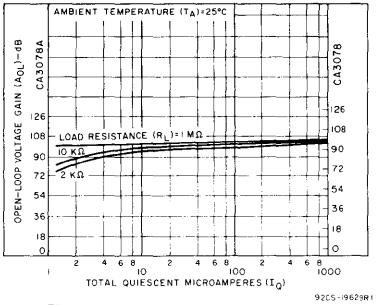


Fig. 6 – Open-loop voltage gain vs. total quiescent current.

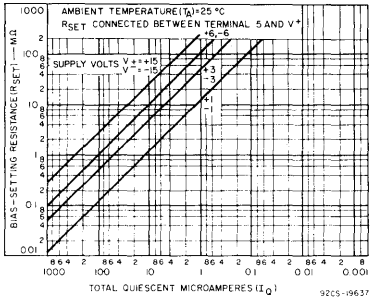


Fig. 7 – Bias-setting resistance vs. total quiescent current.

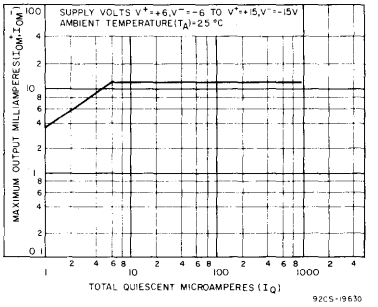


Fig. 8 – Maximum output current vs. total quiescent current.

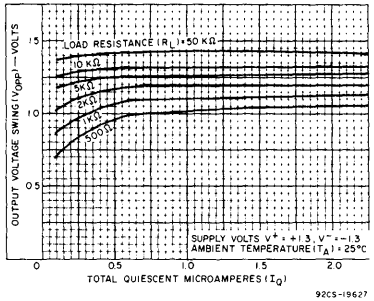


Fig. 9 – Output voltage swing vs. total quiescent current.

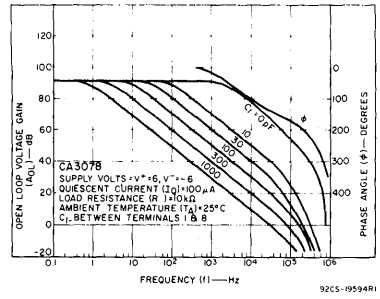


Fig. 10 – Open-loop voltage gain vs. frequency for I_Q = 100 μA – CA3078.

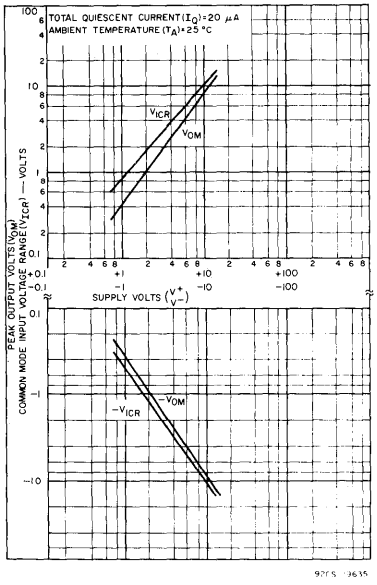


Fig. 11 – Output and common-mode voltage vs. supply voltage.

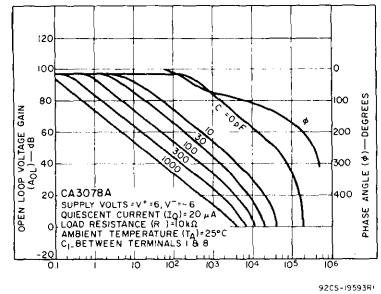


Fig. 12 – Open-loop voltage gain vs. frequency for I_Q = 20 μA – CA3078.

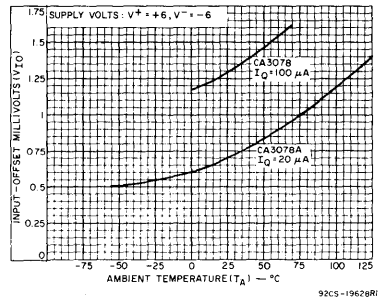


Fig. 13 – Input offset voltage vs. temperature.

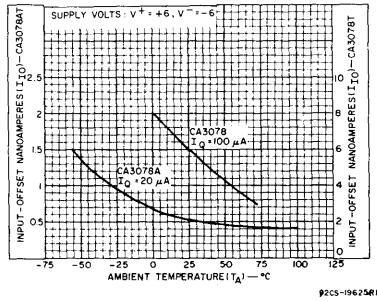


Fig. 14 – Input offset current vs. temperature.

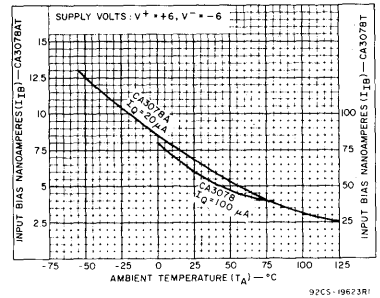


Fig. 15 – Input bias current vs. temperature.

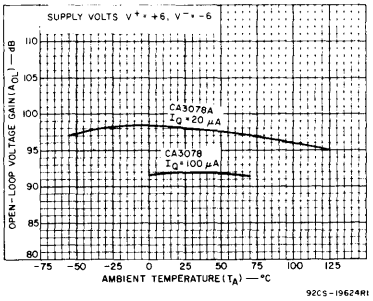


Fig. 16 – Open-loop voltage gain vs. temperature.

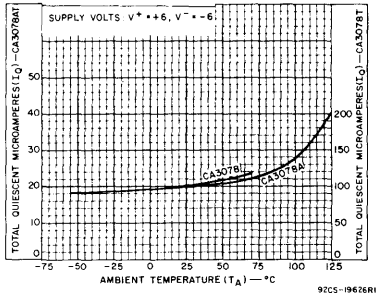


Fig. 17 – Total quiescent current vs. temperature.

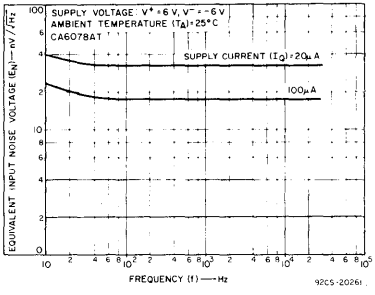


Fig. 18 – Quivalent input noise voltage vs. frequency.

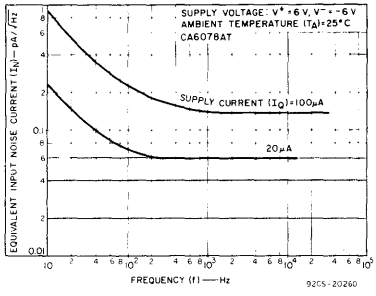


Fig. 19 – Equivalent input noise current vs. frequency.

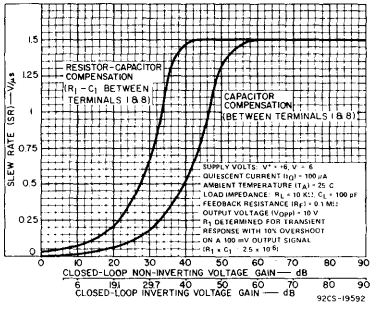


Fig. 20 – Slew rate vs. closed-loop gain for I_Q = 100 μA – CA3078.

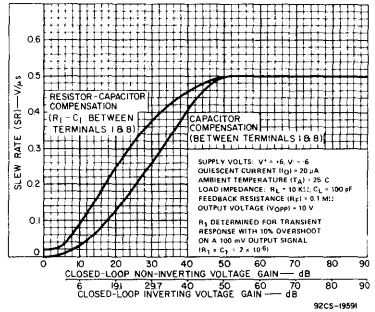


Fig. 21 – Slew rate vs. closed-loop gain for I_Q = 20 μA – CA3078.

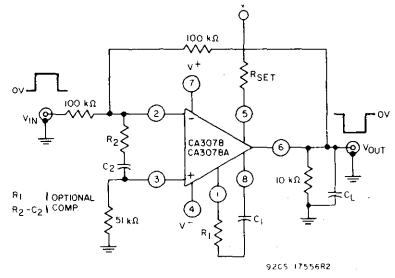


Fig. 22 – Transient response and slew-rate, unity gain (inverting) test circuit.

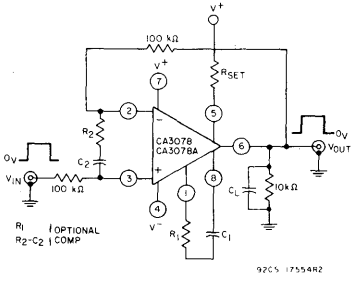


Fig. 23 – Slew-rate, unity gain (non-inverting) test circuit.

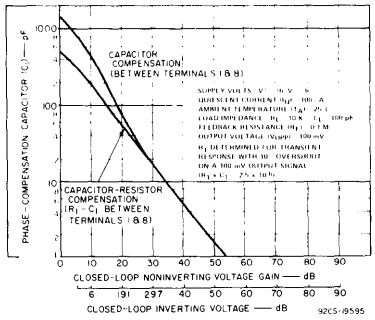


Fig. 24 – Phase compensation capacitance vs. closed-loop gain – CA3078.

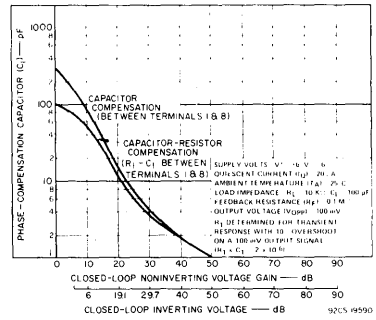


Fig. 25 – Phase compensation capacitance vs. closed-loop gain – CA3078A.

Table I – Unity-gain slew rate vs. compensation – CA3078 and CA3078A

SUPPLY VOLTS: $V^+ = 6$, $V^- = -6$	TRANSIENT RESPONSE: 10% OVERSHOOT FOR AN OUTPUT VOLTAGE OF 100 mV
OUTPUT VOLTAGE (V_O) = ±5 V	AMBIENT TEMPERATURE (T_A) = 25°C
LOAD RESISTANCE (R_L) = 10 kΩ	

COMPENSATION TECHNIQUE	UNITY GAIN (INVERTING) Fig. 22					UNITY GAIN (NON-INVERTING) Fig. 23				
	R1	C1	R2	C2	SLEW RATE	R1	C1	R2	C2	SLEW RATE
CA3078 – I_Q = 100 μA	kΩ	pF	kΩ	μF	V/μs	kΩ	pF	kΩ	μF	V/μs
Single Capacitor	0	750	∞	0	0.0085	0	1500	∞	0	0.0095
Resistor & Capacitor	3.5	350	∞	0	0.04	5.3	500	∞	0	0.024
Input	∞	0	0.25	0.306	0.67	∞	0	0.311	0.45	0.67
CA3078A – I_Q = 20 μA										
Single Capacitor	0	300	∞	0	0.0095	0	800	∞	0	0.003
Resistor & Capacitor	14	100	∞	0	0.027	34	125	∞	0	0.02
Input	∞	0	0.644	0.156	0.29	∞	0	0.77	0.4	0.4

OPERATING CONSIDERATIONS

Compensation Techniques

The CA3078A and CA3078 can be phase-compensated with one or two external components depending upon the closed-loop gain, power consumption, and speed desired. The recommended compensation is a resistor in series with a capacitor connected from terminal 1 to terminal 8. Values of the resistor and capacitor required for compensation as a function of closed loop gain are shown in Figs. 24 and 25. These curves represent the compensation necessary at quiescent currents of 100 μA and 20 μA, respectively, for a transient response with 10% overshoot. Figs. 20 and 21 show the slew rates that can be obtained with the two different compensation techniques. Higher speeds can be achieved with input compensation, but this increases noise output. Compensation can also be accomplished with a single capacitor connected from terminal 1 to terminal 8, with speed being sacrificed for simplicity. Table I gives an indication of slew rates that can be obtained with various compensation techques at quiescent currents of 100 μA and 20 μA.

Single Supply Operation

The CA3078A and CA3078 can operate from a single supply with a minimum total supply voltage of 1.5 volts. Figs. 27 and 28 show the CA3078A or CA3078 in inverting the non-inverting 20-dB amplifier configurations utilizing a 1.5-volt type "AA" cell for a supply. The total power consumption for

either circuit is approximately 675 nanowatts. The output voltage swing in this configuration is 300 mV p-p with a 20 kΩ load.

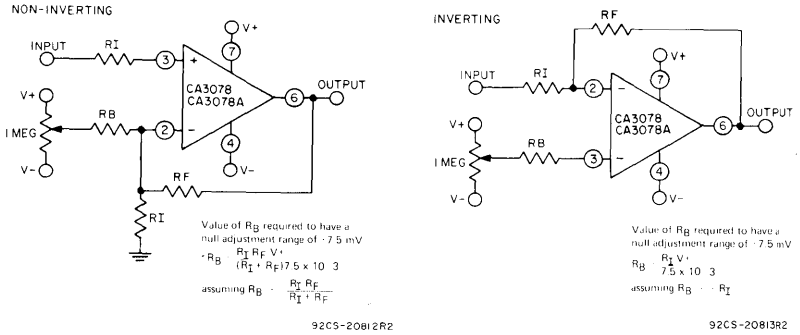


Fig. 26 – Offset voltage null circuits.

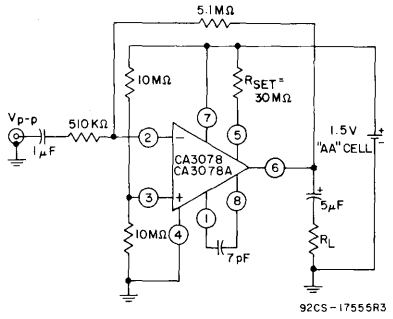


Fig. 27 – Inverting 20-dB amplifier circuit.

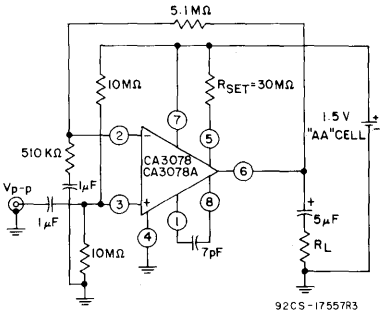


Fig. 28 – Non inverting 20-dB amplifier circuit.

May 1990

Operational Transconductance Amplifiers (OTA's)

Gatable-Gain Blocks

Features:

- *Slew rate (unity gain, compensated): 50 V/μs*
- *Adjustable power consumption: 10μW to 30 mW*
- *Flexible supply voltage range: ±2 V to ±15 V*
- *Fully adjustable gain: 0 to $g_m R_L$ limit*
- *Tight g_m spread: CA3080 (2:1), CA3080A (1.6:1)*
- *Extended g_m linearity: 3 decades*

Applications:

- *Sample and hold*
- *Multiplex*
- *Voltage follower*
- *Multiplier*
- *Comparator*

The CA3080 and CA3080A types are Gatable-Gain Blocks which utilize the unique operational-transconductance-amplifier (OTA) concept described in Application Note ICAN-6668, "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

The CA3080 and CA3080A types have differential input and a single-ended, push-pull, class A output. In addition, these types have an amplifier bias input which may be used either for gating or for linear gain control. These types also have a high output impedance and their transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

The CA3080 and CA3080A types are notable for their excellent slew rate (50 V/μs), which makes them especially useful for multiplex and fast unity-gain voltage followers. These types are especially applicable for multiplex applications because power is consumed only when the devices are in the "ON" channel state.

The CA3080A is rated for operation over the full military-temperature range (-55 to +125°C) and its characteristics are specifically controlled for applications such as sample-hold, gain-control, multiplex, etc. Operational transconductance amplifiers are also useful in programmable power-switch applications, e.g., as described in Application Note ICAN-6048, "Some Applications of a Programmable Power Switch/Amplifier" (CA3094, CA3094A, CA3094B).

These types are supplied in the 8-lead Small Outline package (CA3080M, CA3080AM), the 8-lead TO-5-style package (CA3080, CA3080A), and in the 8-lead TO-5-style package with dual-in-line formed leads ("DIL-CAN", CA3080S, CA3080AS). The CA3080 is also supplied in the 8-lead dual-in-line plastic ("MINI-DIP") package (CA3080E, CA3080AE), and in chip form (CA3080H).

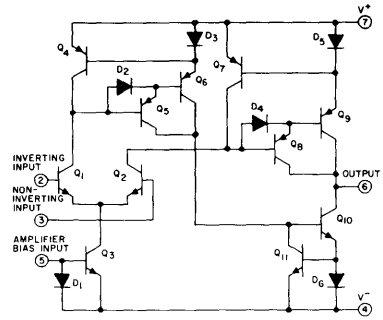


Figure 1- Schematic diagram for CA3080 and CA3080.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS $V^+ = 15\ V, V^- = -15\ V$, $I_{ABC} = 500\ \mu A$, $T_A = 25^oC$ (unless indicated otherwise)	CA3080, CA3080E, CA3080S LIMITS			UNITS
			Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}		–	0.4	5	mV
		$T_A = 0$ to 70^oC	–	–	6	
Input Offset Current	I_{IO}		–	0.12	0.6	μA
Input Bias Current	I_I		–	2	5	μA
		$T_A = 0$ to 70^oC	–	–	7	
Forward Transconductance (large signal)	g_m		6700	9600	13000	μmho
		$T_A = 0$ to 70^oC	5400	–	–	
Peak Output Current	$\lvert I_{OM} \rvert$	$R_L = 0$	350	500	650	μA
		$R_L = 0$, $T_A = 0$ to 70^oC	300	–	–	
Peak Output Voltage:		$R_L = \infty$				V
Positive	V^+_{OM}		12	13.5	–	
Negative	V^-_{OM}		−12	−14.4	–	
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity:						μV/V
Positive	$\Delta V_{IO}/\Delta V^+$		–	–	150	
Negative	$\Delta V_{IO}/\Delta V^-$		–	–	150	
Common-Mode Rejection Ratio	CMRR		80	110	–	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I		10	26	–	kΩ

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

			CA3080, CA3080E, CA3080S	
Input Offset Voltage	V_{IO}	$I_{ABC} = 5\ \mu A$	0.3	mV
Input Offset Voltage Change	$\lvert \Delta V_{IO} \rvert$	$I_{ABC} = 500\ \mu A$ to $I_{ABC} = 5\ \mu A$	0.2	mV
Peak Output Current	I_{OM}	$I_{ABC} = 5\ \mu A$	5	μA
Peak Output Voltage:		$I_{ABC} = 5\ \mu A$		V
Positive	V^+_{OM}		13.8	
Negative	V^-_{OM}		−14.5	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	0.08	nA
		$I_{ABC} = 0$, $V_{TP} = 36\ V$	0.3	
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4\ V$	0.008	nA
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:				V/μs
Maximum (uncompensated)	SR		75	
Unity Gain (compensated)			50	
Open-Loop Bandwidth	BW_{OL}		2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz	0.024	pF
Propagation Delay	t_{PHL}, t_{PLH}	$I_{ABC} = 500\ \mu A$	45	ns

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC		TEST CONDITIONS $V^+ = 15$ V, $V^- = -15$ V, $I_{ABC} = 500\ \mu A$, $T_A = 25^oC$ (unless indicated otherwise)	CA3080A, CA3080AE, CA3080AS LIMITS			UNITS
			Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	$I_{ABC} = 5\ \mu A$	–	0.3	2	mV
			–	0.4	2	
		$T_A = -55$ to $+125^oC$	–	–	5	
Input Offset Voltage Change	$\lvert\Delta V_{IO}\rvert$	$I_{ABC} = 500\ \mu A$ to $I_{ABC} = 5\ \mu A$	–	0.1	3	mV
Input Offset Current	I_{IO}		–	0.12	0.6	μA
Input Bias Current	I_I		–	2	5	μA
		$T_A = -55$ to $+125^oC$	–	–	8	
Forward Transconductance (large signal)	g_m		7700	9600	12000	μmho
		$T_A = -55$ to $+125^oC$	4000	–	–	
Peak Output Current	$\lvert I_{OM}\rvert$	$I_{ABC} = 5\ \mu A$, $R_L = 0$	3	5	7	μA
		$R_L = 0$	350	500	650	
		$R_L = 0, T_A = -55$ to $+125^oC$	300	–	–	
Peak Output Voltage:						V
Positive	V^+_{OM}	$I_{ABC} = 5\ \mu A$, $R_L = \infty$	12	13.8	–	
Negative	V^-_{OM}		−12	−14.5	–	
Positive	V^+_{OM}	$R_L = \infty$	12	13.5	–	
Negative	V^-_{OM}		−12	−14.4	–	
Amplifier Supply Current	I_A		0.8	1	1.2	mA
Device Dissipation	P_D		24	30	36	mW
Input Offset Voltage Sensitivity:						$\mu V/V$
Positive	$\lvert\Delta V_{IO}/\Delta V^+\rvert$		–	–	150	
Negative	$\lvert\Delta V_{IO}/\Delta V^-\rvert$		–	–	150	
Magnitude of Leakage Current		$I_{ABC} = 0$, $V_{TP} = 0$	–	0.08	5	nA
		$I_{ABC} = 0$, $V_{TP} = 36$ V	–	0.3	5	
Differential Input Current		$I_{ABC} = 0$, $V_{DIFF} = 4$ V	–	0.008	5	nA
Common-Mode Rejection Ratio	CMRR		80	110	--	dB
Common-Mode Input-Voltage Range	V_{ICR}		12 to −12	13.6 to −14.6	–	V
Input Resistance	R_I		10	26	–	kΩ

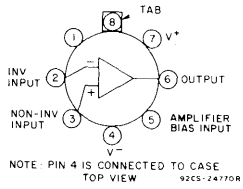
ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

			CA3080A, CA3080AE, CA3080AS	
Amplifier Bias Voltage	V_{ABC}		0.71	V
Slew Rate:				V/μs
Maximum (uncompensated)	SR		75	
Unity Gain (compensated)			50	
Open-Loop Bandwidth	BW_{OL}	–	2	MHz
Input Capacitance	C_I	f = 1 MHz	3.6	pF
Output Capacitance	C_O	f = 1 MHz	5.6	pF
Output Resistance	R_O		.15	MΩ
Input-to-Output Capacitance	$C_{I\text{-}O}$	f = 1 MHz	0.024	pF
Input Offset Voltage Temperature Drift	$\Delta V_{IO}/\Delta T$	$I_{ABC} = 100\ \mu A$, $T_A = -55$ to $+125^oC$	3	$\mu V/^oC$
Propagation Delay	t_{PHL}, t_{PLH}	$I_{ABC} = 500\ \mu A$	45	ns

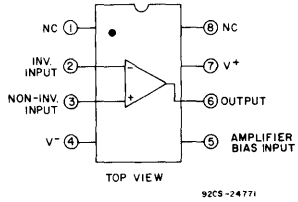
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (Between V^+ and V^- terminals)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE	V^+ to V^-
INPUT SIGNAL CURRENT	1 mA
AMPLIFIER BIAS CURRENT	2 mA
OUTPUT SHORT-CIRCUIT DURATION*	Indefinite
DEVICE DISSIPATION	125 mW
TEMPERATURE RANGE:	
Operating	
CA3080, CA3080E, CA3080S	0 to + 70 °C
CA3080A, CA3080AE, CA3080AS	−55 to + 125 °C
Storage	−65 to + 150 °C
LEAD TEMPERATURE (During Soldering):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 265 °C

* Short circuit may be applied to ground or to either supply.



TO-5 Style Package



Plastic Package (E Suffix)

Fig.2 – Functional diagrams.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS FOR THE CA3080 AND CA3080A

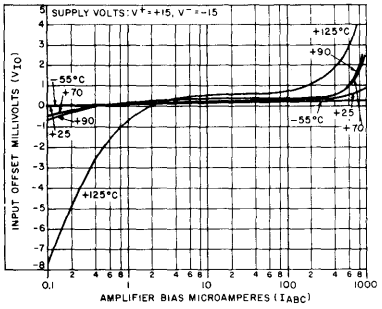


Fig.3 – Input offset voltage as a function of amplifier bias current.

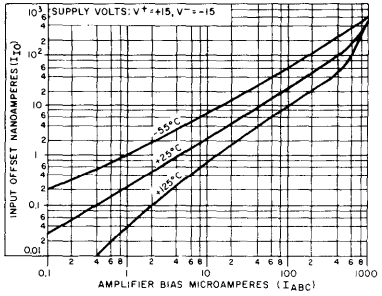


Fig.4 – Input offset current as a function of amplifier bias current.

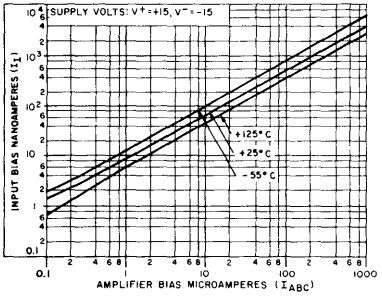


Fig.5 – Input bias current as a function of amplifier bias current.

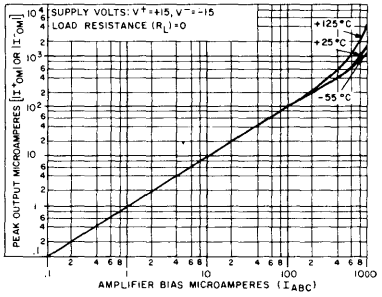


Fig.6 – Peak output current as a function of amplifier bias current.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

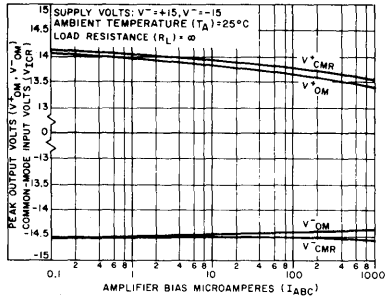


Fig.7 – Peak output voltage as a function of amplifier bias current.

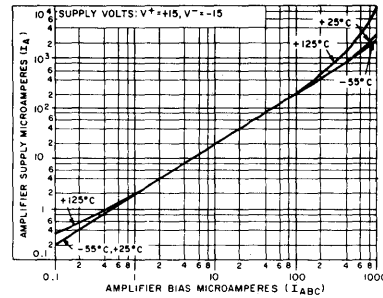


Fig.8 – Amplifier supply current as a function of amplifier bias current.

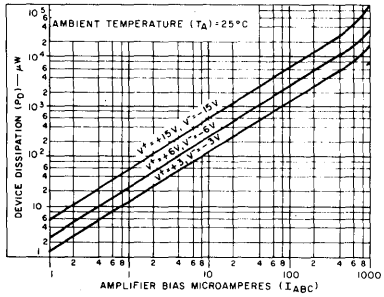


Fig.9 – Total power dissipation as a function of amplifier bias current.

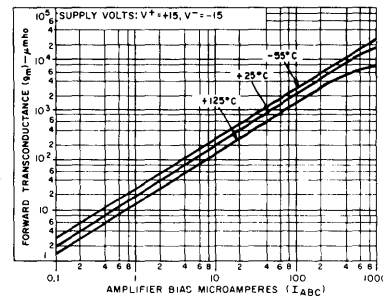


Fig.10 – Transconductance as a function of amplifier bias current.

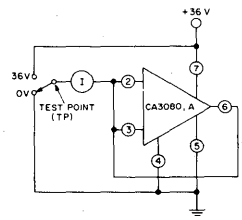


Fig.11 – Leakage current test circuit.

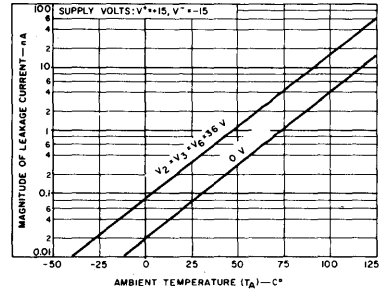


Fig.12 – Leakage current as a function of temperature.

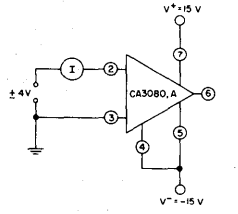


Fig.13 – Differential input current test circuit.

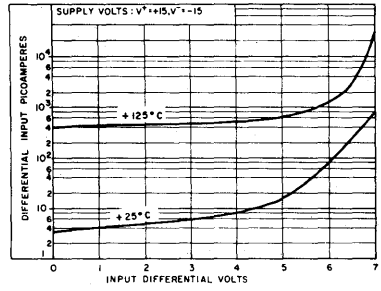


Fig.14 – Input current as a function of input differential voltage.

TYPICAL CHARACTERISTICS CURVES AND TEST CIRCUITS (Cont'd)

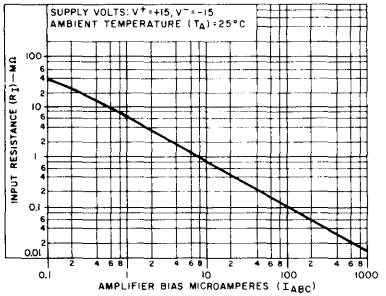


Fig. 15 – Input resistance as a function of amplifier bias current.

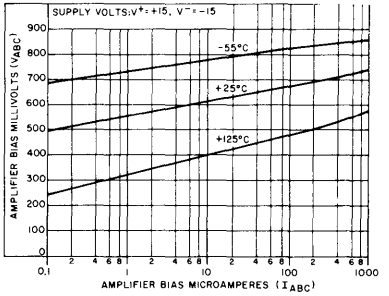


Fig. 16 – Amplifier bias voltage as a function of amplifier bias current.

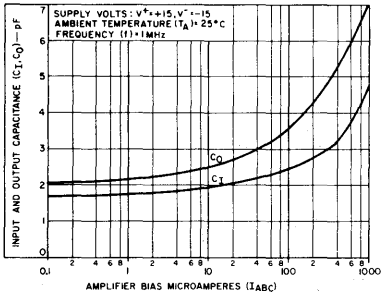


Fig. 17 – Input and output capacitance as a function of amplifier bias current.

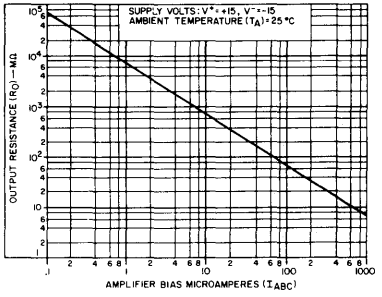


Fig. 18 – Output resistance as a function of amplifier bias current.

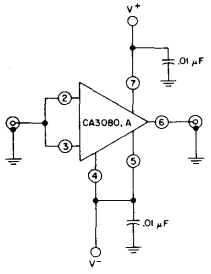


Fig. 19 – Input-to-output capacitance test circuit.

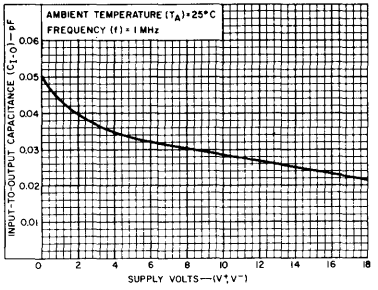
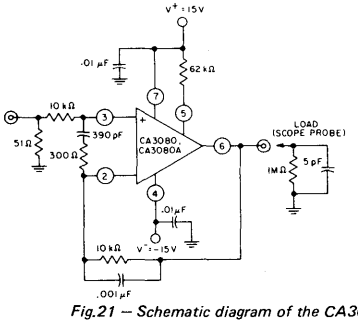


Fig. 20 – Input-to-output capacitance as a function of supply voltage.

APPLICATIONS



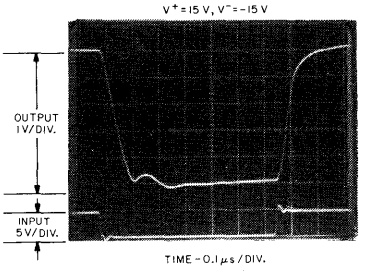


Fig. 21 – Schematic diagram of the CA3080 and CA3080A in a unity-gain voltage follower configuration and associated waveform.

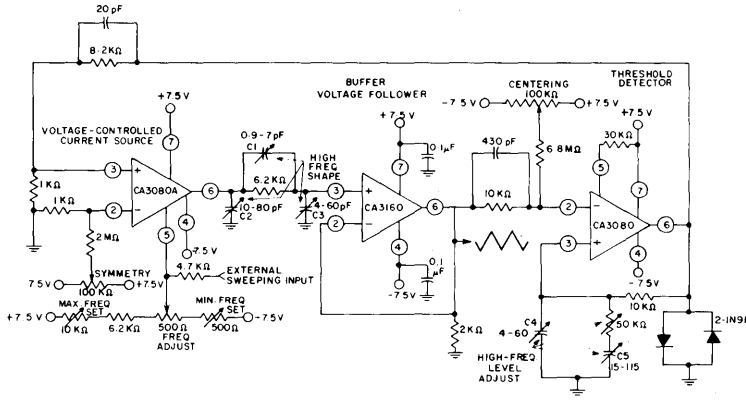
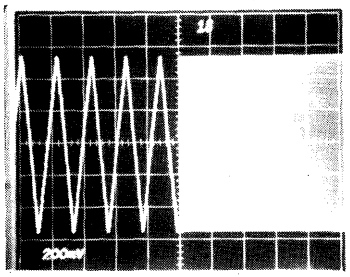
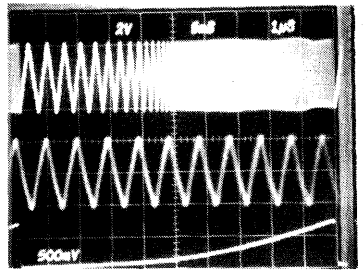


Fig.22 – 1,000,000/1 single-control function generator – 1 MHz to 1 Hz.



(a) – Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.



(b) – Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

Fig.23 – Function generator dynamic characteristics waveforms.

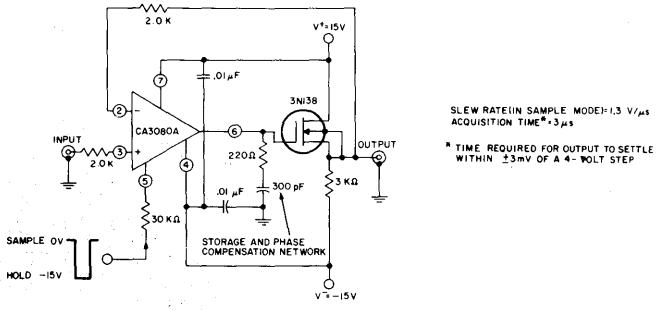


Fig.24 – Schematic diagram of the CA3080A in a sample-hold configuration.

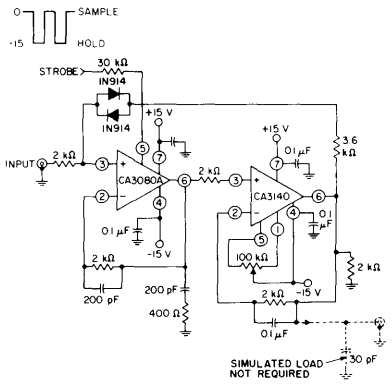
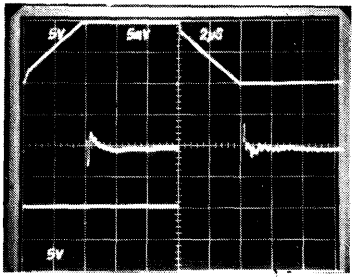
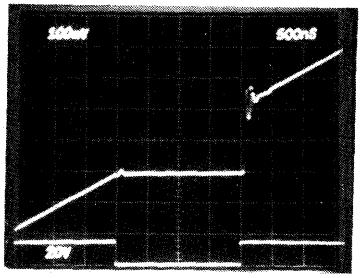


Fig.25 – Sample- and hold circuit.



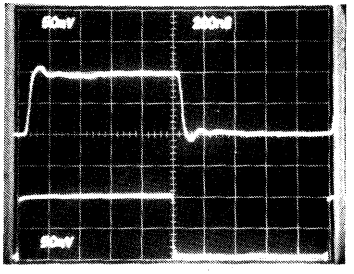
LARGE-SIGNAL RESPONSE AND SETTLING TIME
TOP TRACE: OUTPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)
BOTTOM TRACE: INPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)
CENTER TRACE: DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13
(5 mV/DIV. AND 2 μs/DIV.)

Fig.26 – Large-signal response and settling time for circuit shown in Fig.25.



SAMPLING RESPONSE
TOP TRACE: SYSTEM OUTPUT
(100 mV/DIV. AND 500 ns/DIV.)
BOTTOM TRACE: SAMPLING SIGNAL
(20 V/DIV. AND 500 ns/DIV.)

Fig.27 – Sampling response for circuit shown in Fig. 25.



TOP TRACE: OUTPUT
(50 mV/DIV. AND 200 ns/DIV.)
BOTTOM TRACE: INPUT
(50 mV/DIV. AND 200 ns/DIV.)

Fig.28 – Input and output response for circuit shown in Fig. 25.

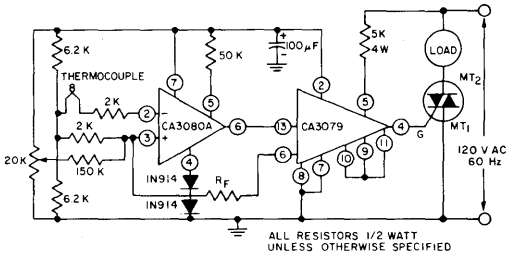


Fig.29 – Thermocouple temperature control with CA3079 zero voltage switch as the output amplifier.

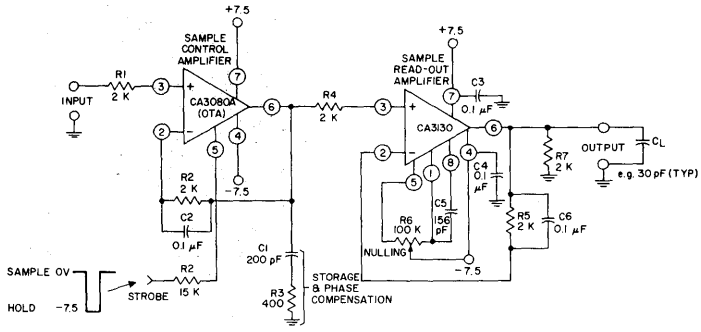
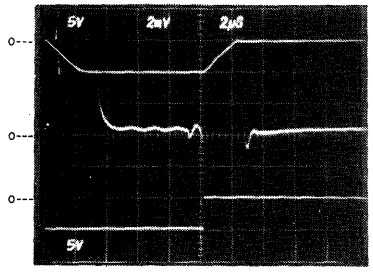
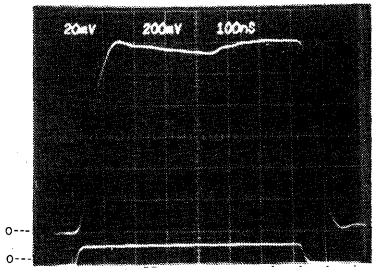


Fig.30 – Schematic diagram of the CA3080A in a sample-hold circuit with BiMos output amplifier.



TOP TRACE: OUTPUT—5 V/DIV. & 2 μs/DIV.
CENTER TRACE: DIFFERENTIAL COMPARISON OF INPUT & OUTPUT—2 mV/DIV. & 2 μs/DIV.
BOTTOM TRACE: INPUT—5 V/DIV. & 2 μs/DIV.

Fig.31 – Large-signal response for circuit shown in Fig. 30.



TOP TRACE: OUTPUT—20 mV/DIV. & 100 ns/DIV.
BOTTOM TRACE: INPUT—200 mV/DIV. & 100 ns/DIV.

Fig.32 – Small-signal response for circuit shown in Fig. 30.

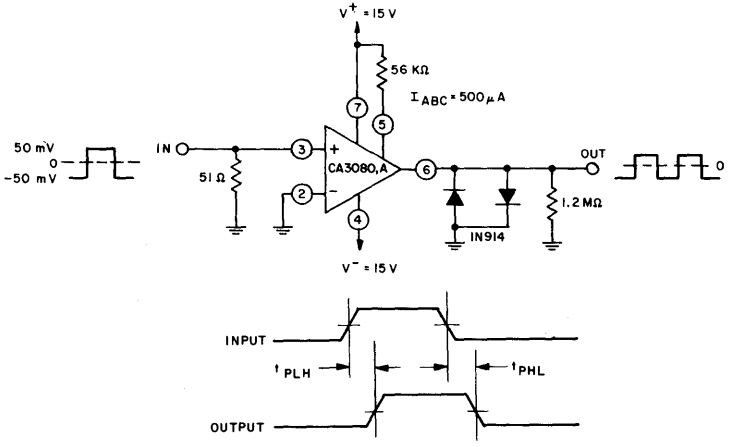


Fig. 33 - Propagation delay test circuit and associated waveforms.

May 1990

Programmable Power Switch/Amplifier

For Control & General-Purpose Applications

CA3094T, S, E:	For Operation Up to 24 Volts
CA3094AT, S, E:	For Operation Up to 36 Volts
CA3094BT, S:	For Operation Up to 44 Volts

Features:

- *Designed for single or dual power supply*
- *Programmable: strobing, gating, squelching, AGC capabilities*
- *Can deliver 3 watts (avg.) or 10 W (peak) to external load (in switching mode)*
- *High-power, single-ended class A amplifier will deliver power output of 0.6 watt (1.6 W device dissipation)*
- *Total harmonic distortion (THD) @ 0.6 W in class A operation - 1.4% typ.*

Applications:

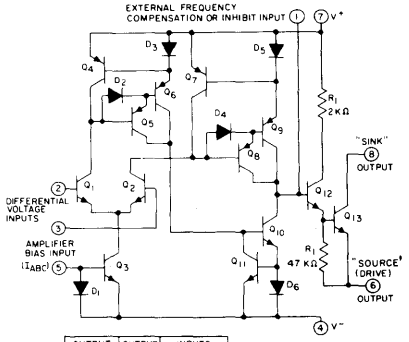
- *Error-signal detector: temperature control with thermistor sensor; speed control for shunt wound dc motor*
- *Over-current, over-voltage, over-temperature protectors*
- *Dual-tracking power supply with CA3085*
- *Wide-frequency-range oscillator*
- *Analog timer*
- *Level detector*
- *Alarm systems*
- *Voltage follower*
- *Ramp-voltage generator*
- *High-power comparator*
- *Ground-fault interrupter (GFI) circuits*

The CA3094 is a differential-input power-control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional-control output signal up to 100 mA. This signal is sufficient to directly drive high-current thyristors, relays, dc loads, or power transistors. The CA3094 has the generic characteristics of the CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100 mA.

The gain of the differential input stage is proportional to the amplifier bias current (I_{ABC}), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I_{ABC} of 100 mA, a one-millivolt change at the input will change the output from 0 to 100 mA (typical).

The CA3094 is intended for operation up to 24 volts and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24 volts is a primary design requirement (see Figs. 28, 29 and 30 in Applications Section). The CA3094A and CA3094B are like the CA3094 but are intended for operation up to 36 and 44 volts, respectively (single or dual supply).

These types are available in 8-lead TO-5 style packages with standard leads ("T" suffix) and with dual-in-line formed leads "DIL-CAN" ("S" suffix). Type CA3094 is also available in an 8-lead dual-in-line plastic package "MINI-DIP" ("E" suffix), and in chip form ("H" suffix).



OUTPUT MODE	OUTPUT TERM	INPUTS	
		INV	NON-INV
"SOURCE"	6	2	3
"SINK"	8	3	2

Fig. 1 - Schematic diagram of CA3094.

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	LIMITS Min.	Typ.	Max.	UNITS
INPUT PARAMETERS					
Input Offset Voltage V_{IO}	T_A = 25°C	–	0.4	5	mV
	T_A = 0 to 70°C	–	–	7	mV
Input-Offset-Voltage Change $\lvert\Delta V_{IO}\rvert$	Change in V_{IO} Between I_{ABC} = 100 μA and I_{ABC} = 5 μA	–	1	8	mV
Input Offset Current I_{IO}	T_A = 25°C	–	0.02	0.2	μA
	T_A = 0 to 70°C	–	–	0.3	μA
Input Bias Current I_I	T_A = 25°C	–	0.2	0.50	μA
	T_A = 0 to 70°C	–	–	0.70	μA
Device Dissipation P_D	I_{out} = 0	8	10	12	mW
Common-Mode Rejection Ratio CMRR		70	110	–	dB
Common-Mode Input–Voltage Range V_{ICR}	V^+ = 30 V High	27	28.8	–	V
	V^+ = 30 V Low	1.0	0.5	–	V
	V^+ = 15 V	+12	+13.8	–	V
	V^- = 15 V	−14	−14.5	–	V
Unity Gain-Bandwidth	I_C = 7.5 mA, V_{CE} = 15 V, I_{ABC} = 500 μA	–	30	–	MHz
Open-Loop Bandwidth At −3 dB Point BW_{OL}	I_C = 7.5 mA, V_{CE} = 15 V, I_{ABC} = 500 μA	–	4	–	kHz
Total Harmonic Distortion (Class A Operation) THD	P_D = 220 mW	–	0.4	–	%
	P_D = 600 mW	–	1.4	–	
Amplifier Bias Voltage (Terminal (No.5 to Terminal No.4) V_{ABC}		–	0.68	–	V
Input Offset Voltage Temperature Coefficient $\Delta V_{IO}/\Delta T$		–	4	–	μV/°C
Power-Supply Rejection $\Delta V_{IO}/\Delta V$		–	15	150	μV/V
1/F Noise Voltage E_N	f = 10 Hz, I_{ABC} = 50 μA	–	18	–	$\eta V/\sqrt{Hz}$
1/F Noise Current I_N	f = 10 Hz, I_{ABC} = 50 μA	–	1.8	–	$pA/\sqrt{Hz}$
Differential Input Resistance R_I	I_{ABC} = 20 μA	0.50	1	–	MΩ
Differential Input Capacitance C_I	f = 1 MHz, V^+ = 30 V	–	2.6	–	pF

ELECTRICAL CHARACTERISTICS at T_A = 25°C For Equipment Design

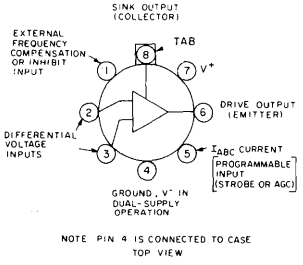
CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
	Single Supply V^+ = 30 V Dual Supply V^+ = 15 V, V^- = 15 V I_{ABC} = 100 μA Unless Otherwise Specified	Min.	Typ.	Max.	
OUTPUT PARAMETERS (Differential Input Voltage = 1V)					
Peak Output Voltage: (Terminal No. 6)	V^+ = 30 V				
With Q13 "ON" V^+OM	R_L = 2 kΩ to ground	26	27	–	V
With Q13 "OFF" V^-OM		–	0.01	0.05	V
Peak Output Voltage: (Terminal No. 6)	V^+ = +15 V, V^- = -15 V			0.5	
Positive V^+OM	R_L = 2 kΩ to −15 V	+11	+12	–	V
Negative V^-OM		–	−14.99	−14.95	V
Peak Output Voltage: (Terminal No. 8)	V^+ = 30 V				
With Q13 "ON" V^+OM	R_L = 2 kΩ to 30 V	29.95	29.99	–	V
With Q13 "OFF" V^-OM		–	0.040	–	V
Peak Output Voltage: (Terminal No. 8)	V^+ = 15 V, V^- = – 15 V				
Positive V^+OM	R_L = 2 kΩ to + 15 V	+14.95	+14.99	–	V
Negative V^-OM		–	14.96	–	V
Collector-to-Emitter Saturation Voltage (Terminal No. 8) $V_{CE(sat)}$	V^+ = 30 V I_C = 50 mA Terminal No.6 grounded	–	0.17	0.80	V
Output Leakage Current (Terminal No. 6 to Terminal No. 4)	V^+ = 30 V	–	2	10	μA
Composite Small-Signal Current Transfer Ratio (Beta) (Q_{12} and Q_{13}) h_{fe}	V^+ = 30 V V_{CE} = 5 V I_C = 50 mA	16,000	100,000	–	
Output Capacitance:	f = 1 MHz				
Terminal No. 6 C_O	All Remaining	–	5.5	–	pF
Terminal No. 8	Terminals Tied to	–	17	–	pF
	Terminal No. 4				
TRANSFER PARAMETERS					
Voltage Gain A	V^+ = 30 V I_{ABC} = 100 μA ΔV_{out} = 20 V R_L = 2 kΩ	20,000 86	100,000 100	– –	V/V dB
Forward Transconductance To Terminal No. 1 g_m		1650	2200	2750	μmhos
Slew Rate:					
Open Loop:					
Positive Slope	I_{ABC} = 500 μA	–	500	–	V/μs
Negative Slope	R_L = 2 kΩ	–	50	–	V/μs
Unity Gain (Non-Inverting, Compensated)	I_{ABC} = 500 μA R_L = 2 kΩ	–	0.7	–	V/μs

MAXIMUM RATINGS, *Absolute-Maximum Values:*

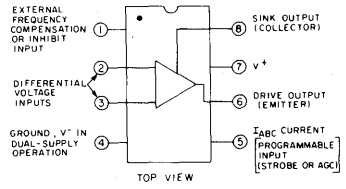
	CA3094	CA3094A	CA3094B	
DC SUPPLY VOLTAGE:				
Dual Supply	± 12 V	± 18 V	± 22 V	V
Single Supply	24 V	36 V	44 V	V
DC DIFFERENTIAL INPUT VOLTAGE (Terminals 2 and 3)	± 5*			V
DC COMMON-MODE INPUT VOLTAGE	Term. 4 ≤ Term. 2 & 3 ≤ Term. 7			
PEAK INPUT SIGNAL CURRENT (Terminals 2 and 3)	± 1			mA
PEAK AMPLIFIER BIAS CURRENT (Terminal 5)	2			mA
OUTPUT CURRENT:				
Peak	300			mA
Average	100			mA
DEVICE DISSIPATION:				
Up to T_A = 55°C:				
Without heat sink	630			mW
With heat sink	1.6			W
Above T_A = 55°C:				
Without heat sink derate linearly	6.67			mW/°C
With heat sink derate linearly	16.7			mW/°C
THERMAL RESISTANCE (Junction to Air)	140			°C/W
AMBIENT TEMPERATURE RANGE:				
Operating	−55 to +125			°C
Storage	−65 to +150			°C
LEAD TEMPERATURE (DURING SOLDERING): At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max.	+ 300			°C

*Exceeding this voltage rating will not damage the device unless the peak input signal current (1 mA) is also exceeded.

FUNCTIONAL DIAGRAMS



TO-5 Style Package



Plastic Package

TYPICAL CHARACTERISTICS CURVES

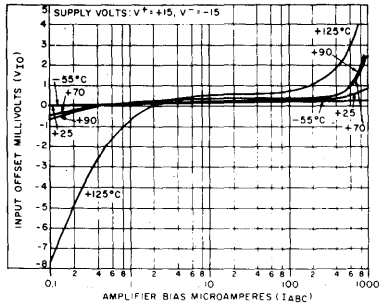


Fig.2 — Input offset voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

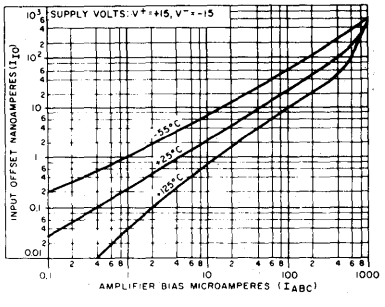


Fig.3 — Input offset current vs. amplifier bias current (I_{ABC}, terminal No.5).

TYPICAL CHARACTERISTICS CURVES (Cont'd)

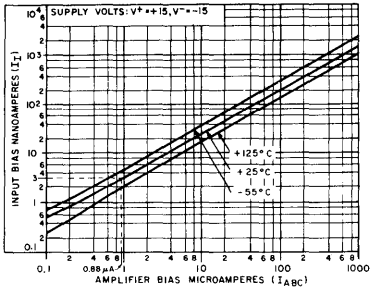


Fig.4 – Input bias current vs. amplifier bias current (I_{ABC}, terminal No.5).

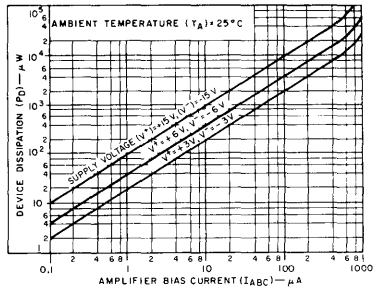


Fig.5 – Device dissipation vs. amplifier bias current (I_{ABC}, terminal No.5).

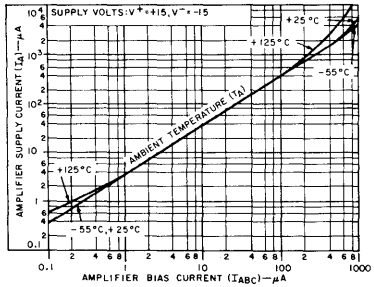


Fig.6 – Amplifier supply current vs. amplifier bias current (I_{ABC}, terminal No.5).

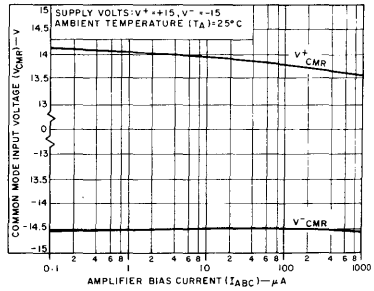


Fig.7 – Common mode input voltage vs. amplifier bias current (I_{ABC}, terminal No.5).

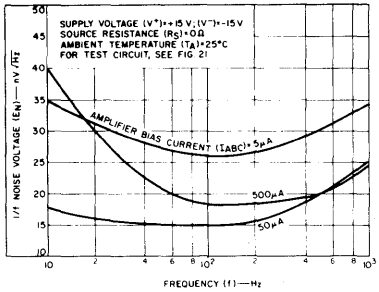


Fig.8 – I/F Noise voltage vs. frequency.

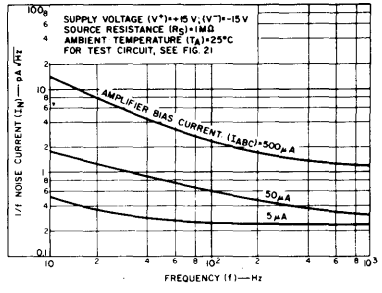


Fig.9 – I/F Noise current vs. frequency.

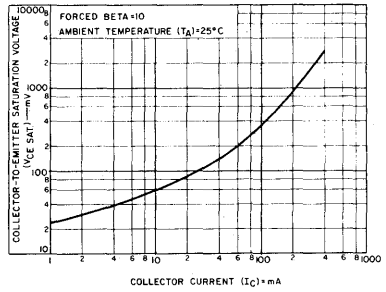


Fig.10 – Collector-emitter saturation voltage vs. collector current of output transistor Q_{13}.

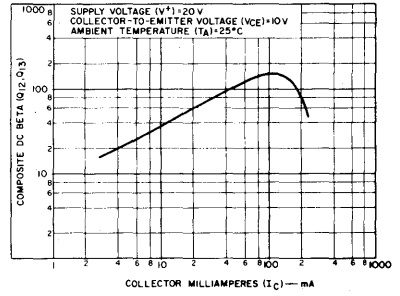


Fig.11 – Composite dc beta vs. collector current of Darlington-connected output transistors (Q_{12}, Q_{13}).

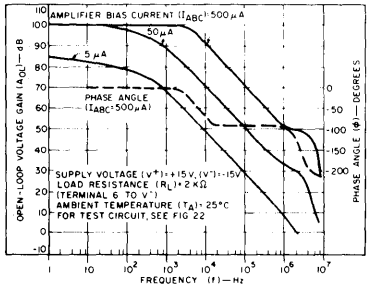


Fig. 12 – Open-loop voltage gain vs. frequency.

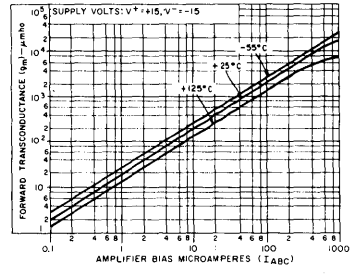


Fig. 13 – Forward transconductance vs amplifier bias current.

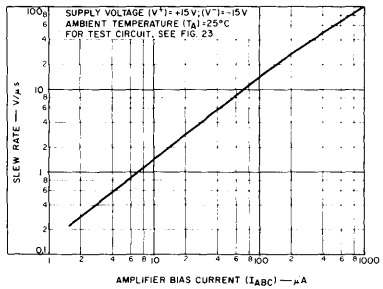


Fig. 14 – Slew rate vs amplifier bias current.

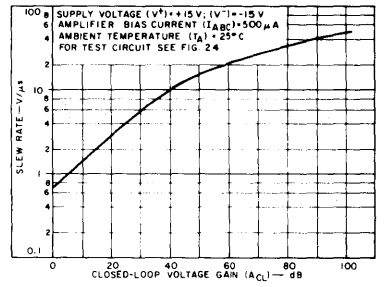


Fig. 15 – Slew rate vs closed-loop voltage gain.

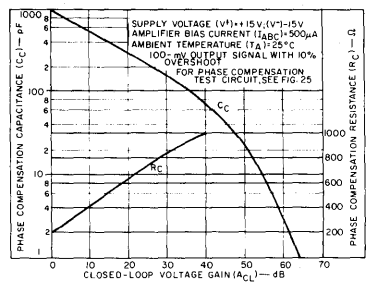


Fig. 16 – Phase compensation capacitance and resistance vs closed-loop voltage gain.

OPERATING CONSIDERATIONS

The "Sink" Output (terminal No.8) and the "Drive" Output (terminal No.6) of the CA3094 are not inherently current (or power) limited. Therefore, if a load is connected between terminal No.6 and terminal No.4 (V^- or ground), it is important to connect a current-limiting resistor between terminal 8 and terminal No.7 (V^+) to protect transistor Q_{13} under shorted load conditions. Similarly, if a load is connected between terminal No.8 and terminal No.7, the current-limiting resistor should be connected between terminal No.6 and terminal No.4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100-ohm current-limiting resistor be inserted between terminal No.7 and the V^+ supply.

TEST CIRCUITS

I/F Noise Measurement Circuit

When using the CA3094, A, or B audio amplifier circuits, it is frequently necessary to consider the noise performance of the device. Noise measurements are made in the circuit shown in Fig.21. This circuit is a 30-dB, non-inverting amplifier with emitter-follower output and phase compensation from terminal No.2 to ground. Source resistors (Rs) are set to 0.Ω or 1 MΩ for E noise and I noise measurements, respectively. These measurements are made at frequencies of 10, Hz, 100 Hz, and 1 kHz with a 1-Hz measurement bandwidth. Typical values for 1/f noise at 10 Hz and 50 μA I_{ABC} are E_n = 18 nV/$\sqrt{Hz}$ and I_N = 1.8 pA/$\sqrt{Hz}$.

TEST CIRCUITS

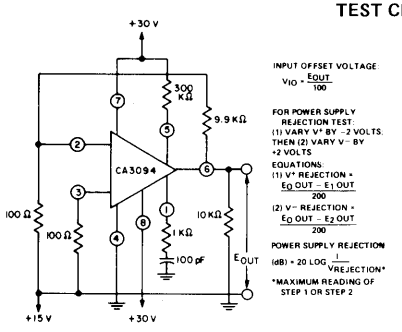


Fig.17 – Input offset voltage and power-supply rejection test circuit.

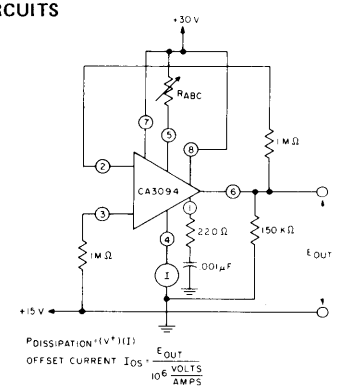


Fig.18 – Input offset current test circuit.

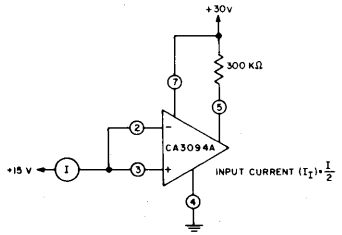


Fig.19 – Input bias current test circuit.

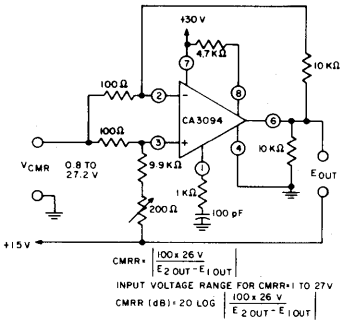
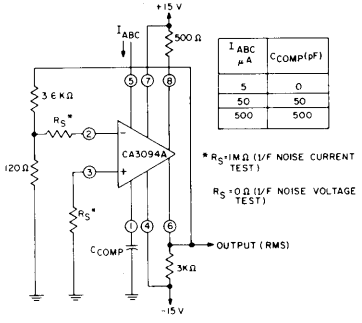
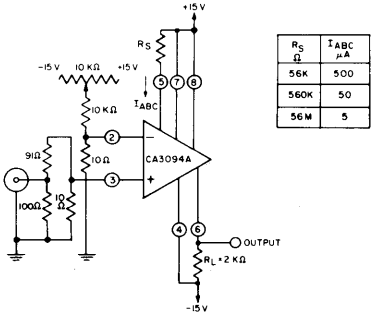


Fig.20 – Common-mode range and rejection ratio test circuit.



IABC μA	CCOMP (pF)
5	0
50	50
500	500

Fig.21 – I/F noise test circuit.



RS Ω	IABC μA
56K	500
560K	50
56M	5

Fig.22 – Open-loop gain vs frequency test circuit.

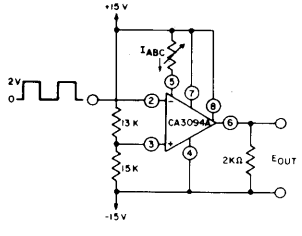


Fig.23 – Open-loop slew rate vs I_{ABC} test circuit.

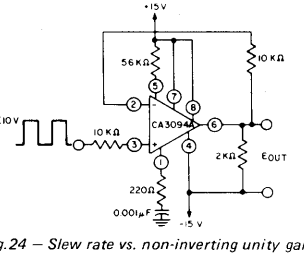
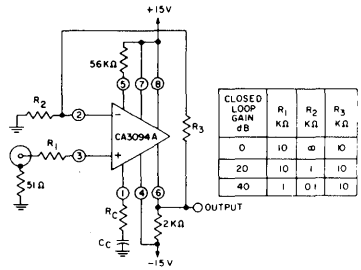


Fig.24 – Slew rate vs. non-inverting unity gain test circuit.

TEST CIRCUITS (Cont'd)



CLOSED LOOP GAIN dB	R1 KΩ	R2 KΩ	R3 KΩ
0	10	∞	10
20	10	1	10
40	1	0.1	10

Fig.25 – Phase compensation test circuit.

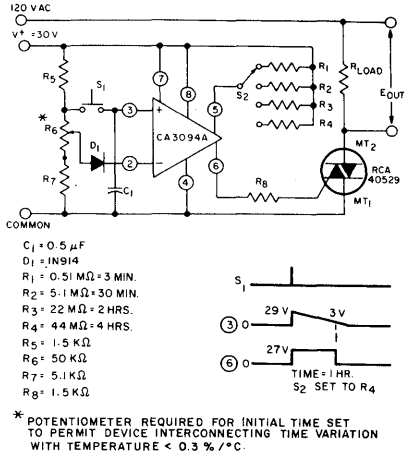


Fig.26 – Presettable analog timer.

TYPICAL APPLICATIONS

For Additional Application Information, refer to Application Note ICAN-6048 "Some Applications of a Programmable Power/ Switch Amplifier IC".

Design Considerations

The selection of the optimum amplifier bias current (I_{ABC}) depends on –

1. The Desired Sensitivity – the higher the I_{ABC}, the higher the sensitivity – i.e., a greater-drive current capability at the output for a specific voltage change at the input.
2. Required Input Resistance – the lower the I_{ABC}, the higher the input resistance.

If the desired sensitivity and requred input resistance are not known and are to be experimentally determined, or the anticipated equipment design is sufficiently flexible to tolerate a wide range of these parameters, it is recommended that the equipment designer begin his calculations with an I_{ABC} of 100 μA, since the CA3094 is characterized at this value of amplifier bias current.

The CA3094 is extremely versatile and can be used in a wide variety of applications.

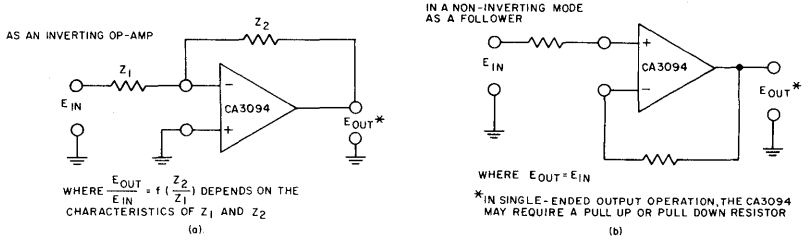
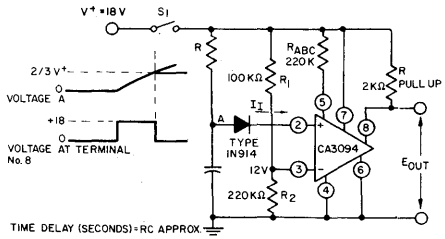


Fig.27 – Application of the CA3094: (a) as an inverting op-amp, and (b) in a non-inverting mode, as a follower.



Problem: To calculate the maximum value of R required to switch a 100-mA output current comparator

Given: $I_{ABC} = 5\ \mu A$, $R_{ABC} = 3.6\ M\Omega \approx \frac{18\ V}{5\ \mu A}$

$I_1 = 500$ nA @ $I_{ABC} = 100\ \mu A$ (from Fig.4)

$I_1 = 5\ \mu A$ can be determined by drawing a line on Fig.4 through $I_{ABC} = 100\ \mu A$ and $I_B = 500$ nA parallel to the typical $T_A = 25^oC$ curve.

Then: $I_1 = 33$ nA @ $I_{ABC} = 5\ \mu A$

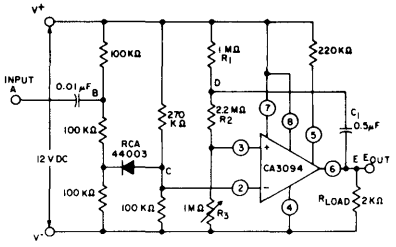
$$R_{max} = \frac{18-12\ volts}{33nA} = 180\ M\Omega\ @\ T_A = 25^oC$$

$R_{max} = 180\ M\Omega \times 2/3^* = 120\ M\Omega$ @ $T_A = -55^oC$

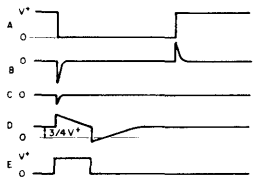
* Ratio of I_1 at $T_A = +25^oC$ to I_1 at $T_A = -55^oC$ for any given value of I_{ABC}.

Fig.28 – RC timer.

TYPICAL APPLICATIONS (Cont'd)



On a negative-going transient at input (A), a negative pulse at C will turn "on" the CA3094, and the output (E) will go from a low to a high level.



At the end of the time constant determined by C_1, R_1, R_2, R_3, the CA3094 will return to the "off" state and the output will be pulled low by R_{LOAD}. This condition will be independent of the interval when input A returns to a high level.

Fig.29 – RC timer triggered by external negative pulse.

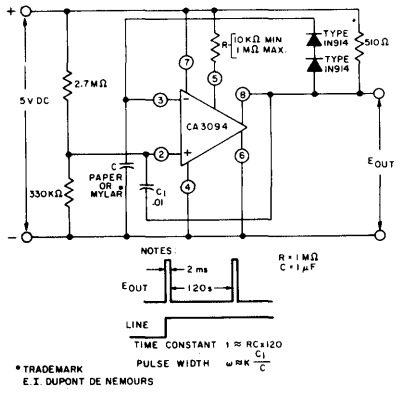


Fig.30 – Free-running pulse generator.

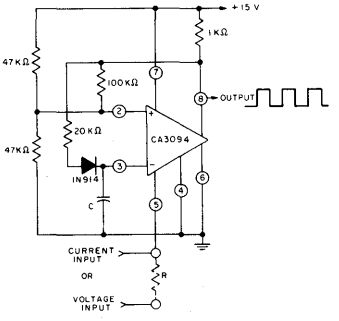


Fig.31 – Current or voltage-controlled oscillator.

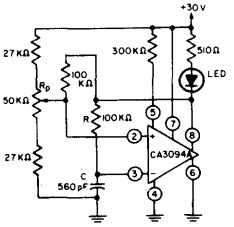


Fig.32 – Single-supply astable multivibrator.

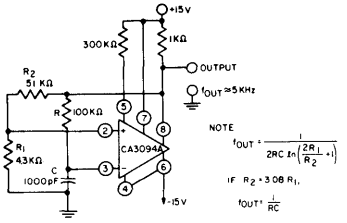


Fig.33 – Dual-supply astable multivibrator.

TYPICAL APPLICATIONS (Cont'd)

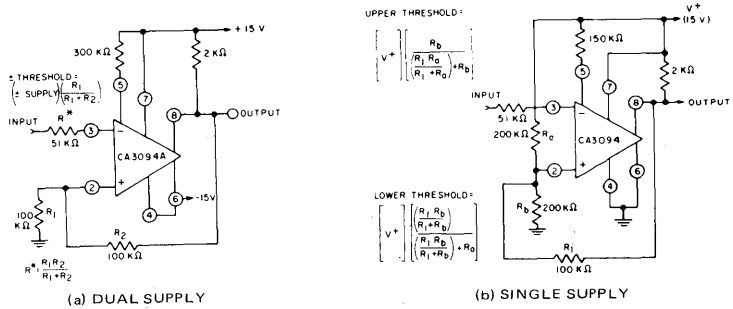


Fig.34 – Comparators (threshold detectors) –dual- and single-supply types.

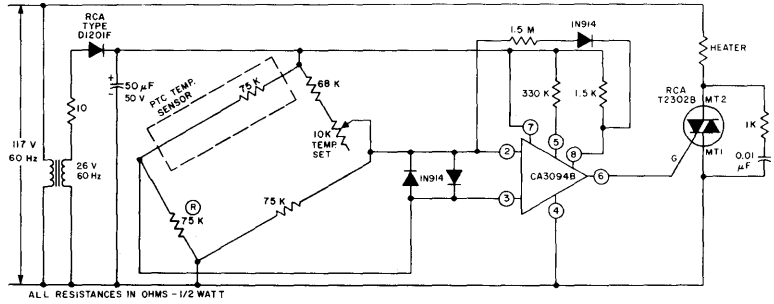


Fig.35 – Temperature controller.

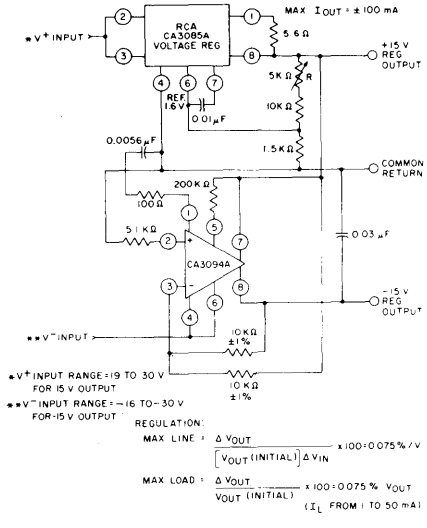


Fig.36 – Dual-voltage tracking regulator.

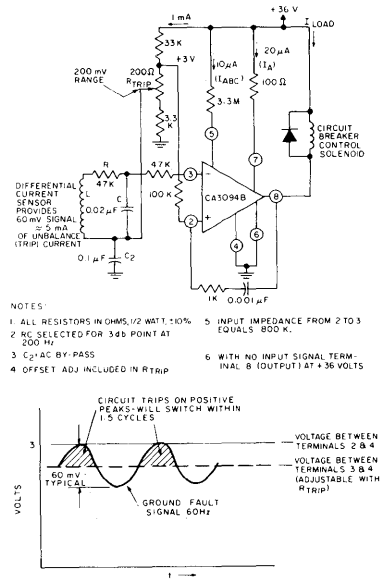
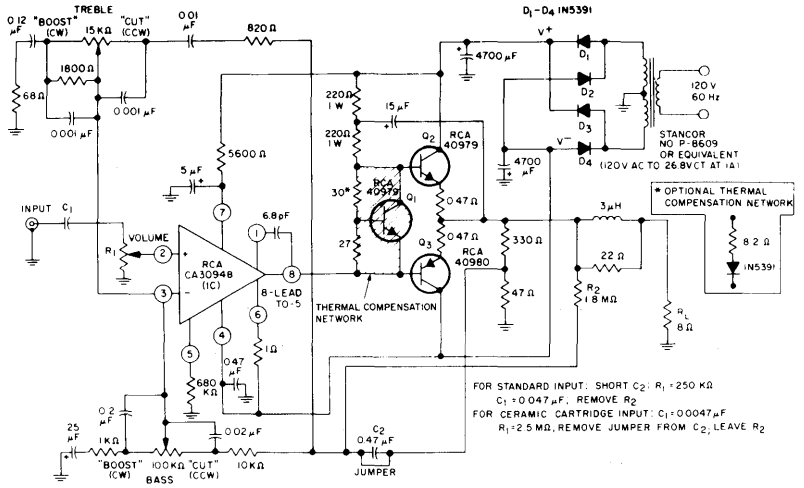


Fig.37 – Ground fault interrupter (GFI) and waveform pertinent to ground fault detector.



TYPICAL PERFORMANCE DATA
For 12-W Audio Amplifier Circuit

Power Output (8Ω load, Tone Control set at "Flat")		
Music (at 5% THD, regulated supply)	15	W
Continuous (at 0.2% IMD, 60 Hz & 2 kHz mixed in a 4:1 ratio, unregulated supply) See Fig. 8 In ICAN-6048	12	W
Total Harmonic Distoration		
At 1 W, unregulated supply	0.05	%
At 12 W, unregulated supply	0.57	%
Voltage Gain	40	dB
Hum and Noise (Below continuous Power Output)	83	dB
Input Resistance	250	kΩ
Tone Control Range	See Fig. 9 In ICAN-6048	

Fig.38 — 12-watt amplifier circuit featuring true complementary-symmetry output stage with CA3094 in driver stage.

May 1990

Wideband Operational Amplifier

Features:

- *High open-loop gain at video frequencies - 42 dB typ. at 1 MHz*
- *High unity-gain crossover frequency (f_T) - 38 MHz typ.*
- *Wide power bandwidth - V_O = 18 Vp-p typ. at 1.2 MHz*
- *High slew rate - 70 V/μs (typ.) in 20 dB amplifier, 25 V/μs (typ.) in unity-gain amplifier*
- *Fast settling time - 0.6 μs typ.*
- *High output current - ±15 mA min.*
- *LM118, 748/LM101 pin compatibility*
- *Single capacitor compensation*
- *Offset null terminals*

Applications:

- *Video amplifiers*
- *Fast peak detectors*
- *Meter-driver amplifiers*
- *High-frequency feedback amplifiers*
- *Video pre-drivers*
- *Oscillators*
- *Multivibrators*
- *Voltage-controlled oscillator*
- *Fast comparators*

The CA3100 is a large-signal wideband, high-speed operational amplifier which has a unity gain cross-over frequency (f_T) of approximately 38 MHz and an open-loop, 3 dB corner frequency of approximately 110 kHz. It can operate at a total supply voltage of from 14 to 36 volts (±7 to ±18 volts when using split supplies) and can provide at least 18 Vp-p and 30 mA p-p at the output when operating from ±15 volt supplies. The CA3100 can be compensated with a single external capacitor and has dc offset adjust terminals for those applications requiring offset null. (See Fig. 15).

The CA3100 circuit contains both bipolar and PMOS transistors on a single monolithic chip.

These devices are supplied in either the 8-lead Small Outline style package (M suffix), the standard 8-lead TO-5 style package (T suffix), 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" package (S suffix), or in the 8-lead dual-in-line plastic package "Mini-DIP" (E suffix). They are also available in chip form (H suffix).

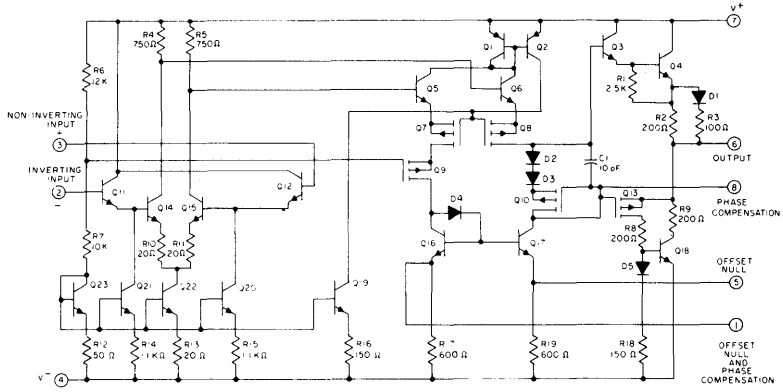
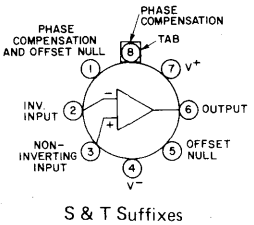


Figure 1 - Schematic diagram for CA3100.

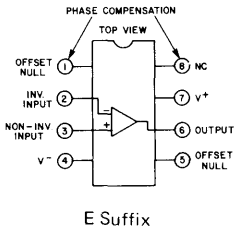
ELECTRICAL CHARACTERISTICS, *At T_A = 25°C:*

CHARACTERISTICS	TEST CONDITIONS SUPPLY VOLTAGE (V^+,V^-)=15 V UNLESS OTHERWISE SPECIFIED	LIMITS			UNITS
		MIN.	TYP.	MAX.	
STATIC					
Input Offset Voltage, V_{IO}	V_O = 0 ± 0.1 V	–	±1	±5	mV
Input Bias Current, I_{IB}	V_O = 0 ± 1 V	–	0.7	2	μA
Input Offset Current, I_{IO}		–	±0.05	±0.4	μA
Low-Frequency Open-Loop Voltage Gain, A_{OL}•	V_O = ±1 V Peak, F = 1 kHz	56	61	–	dB
Common-Mode Input Voltage Range, V_{ICR}	CMRR ≥ 76 dB	±12	+14 −13	–	V
Common-Mode Rejection Ratio, CMRR	V_I Common Mode = ±12 V	76	90	–	dB
Maximum Output Voltage: Positive, V_{OM}^+	Differential Input Voltage = 0 ± 0.1 V	+9	+11	–	V
Negative, V_{OM}^-	R_L = 2 KΩ	−9	−11	–	
Maximum Output Current: Positive, I_{OM}^+	Differential Input Voltage = 0 ± 0.1 V	+15	+30	–	mA
Negative, I_{OM}^-	R_L = 250 Ω	−15	−30	–	
Supply Current, I^+	V_O = 0 ± 0.1 V, R_L ≥ 10 KΩ	–	8.5	10.5	mA
Power-Supply Rejection Ratio, PSRR	ΔV^+ = ± 1 V, ΔV^- = ± 1 V	60	70	–	dB
DYNAMIC					
Unity-Gain Crossover Frequency, f_T	C_C = 0, V_O = 0.3 V (P-P)	–	38	–	MHz
1-MHz Open-Loop Voltage Gain, A_{OL}	f = 1 MHz, C_C = 0, V_O = 10 V (P-P)	36	42	–	dB
Slew Rate, SR: 20-dB Amplifier	A_V = 10, C_C = 0, V_I = 1 V (Pulse)	50	70	–	V/μs
Follower Mode	A_V = 1, C_C = 10 pF, V_I = 10 V (Pulse)	–	25	–	
Power Bandwidth, PBW▲: 20-dB Amplifier	A_V = 10, C_C = 0, V_O = 18 V (P-P)	0.8	1.2	–	MHz
Follower Mode	A_V = 1, C_C = 10 pF, V_O = 18 V (P-P)	–	0.4	–	
Open-Loop Differential Input Impedance, Z_I	F = 1 MHz	–	30	–	KΩ
Open-Loop Output Impedance, Z_O	F = 1 MHz	–	110	–	Ω
Wideband Noise Voltage Referred to Input, e_N(Total)	BW = 1 MHz, R_S = 1 KΩ	–	8	–	μV_{RMS}
Settling Time, t_s To Within ±50 mV of 9 V Output Swing	R_L = 2 KΩ, C_L = 20 pF	–	0.6	–	μs

▲ Power Bandwidth = $\frac{\text{Slew Rate}}{\pi V_O \text{ (P-P)}}$ • Low-frequency dynamic characteristic



S & T Suffixes



E Suffix

TERMINAL ASSIGNMENTS

MAXIMUM RATINGS, *Absolute-Maximum Values:*

Supply Voltage (between V+ and V− terminals)	36	V
Differential Input Voltage	±12	V
Input Voltage to Ground*	±15	V
Offset Terminal to V− Terminal Voltage	±0.5	V
Output Current	50	mA●
Device Dissipation:		
Up to T_A = 55°C	630	mW
Above T_A = 55°C	6.67	mW/°C
Ambient Temperature Range:		
Operating:		
E Type	−40 to +85	°C
S and T Types	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265	°C

* If the supply voltage is less than ±15 volts, the maximum input voltage to ground is equal to the supply voltage.

● CA3100S, CA3100T does not contain circuitry to protect against short circuits in the output.

TYPICAL CHARACTERISTIC CURVES

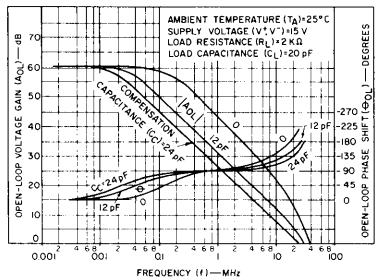


Fig. 2 – Open-loop gain, open-loop phase shift vs. frequency.

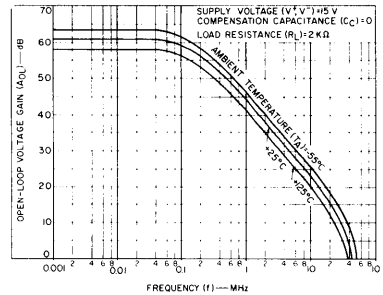


Fig. 3 – Open-loop gain vs. frequency and temperature.

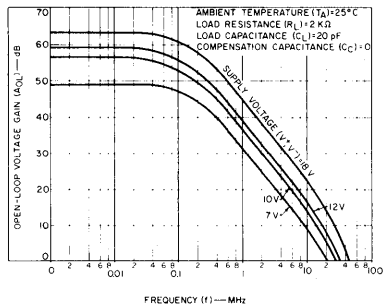


Fig. 4 – Open-loop gain vs. frequency and supply voltage.

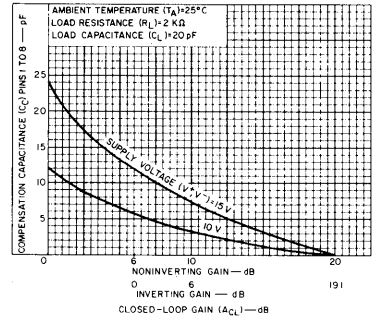


Fig. 5 – Required compensation capacitance vs. closed-loop gain.

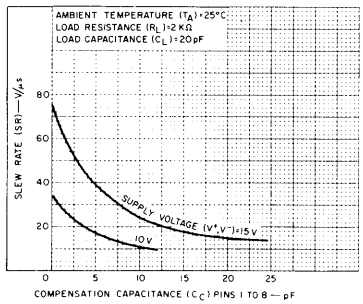


Fig. 6 – Slew rate vs. compensation capacitance.

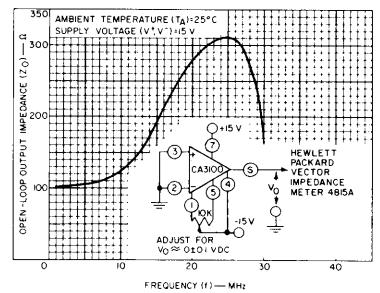


Fig. 7 – Typical open-loop output impedance vs. frequency.

TYPICAL CHARACTERISTIC CURVES (Cont'd)

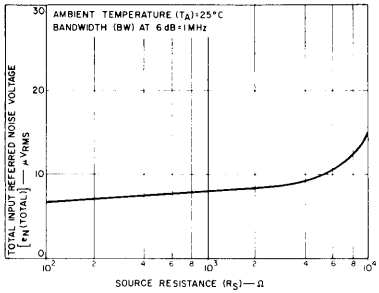


Fig. 8 – Wideband input noise voltage vs. source resistance.

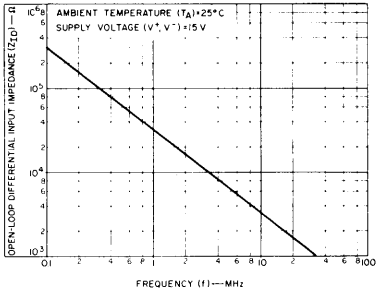


Fig. 9 – Typical open-loop differential input impedance vs. frequency.

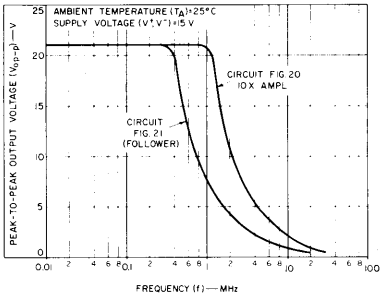


Fig. 10 – Maximum output voltage swing vs. frequency.

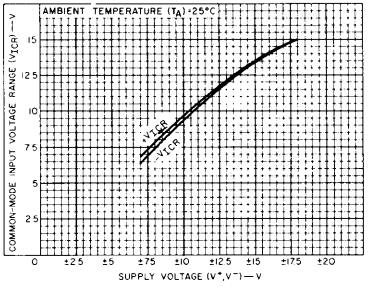


Fig. 11 – Common-mode input voltage range vs. supply voltage.

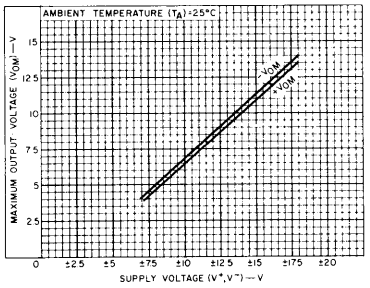


Fig. 12 – Maximum output voltage vs. supply voltage.

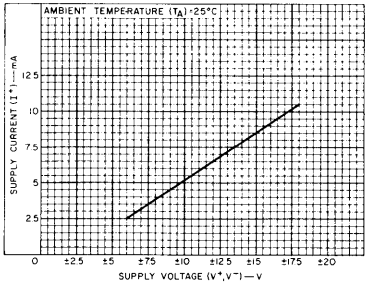


Fig. 13 – Supply current vs. supply voltage.

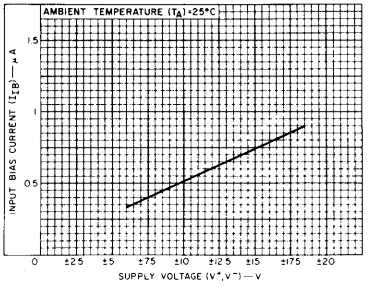


Fig. 14 – Input bias current vs. supply voltage.

TEST CIRCUITS

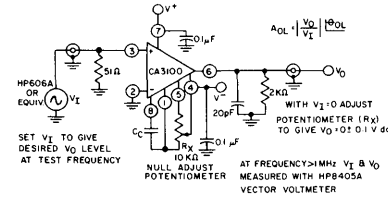


Fig. 15 – Open-loop voltage gain test circuit.

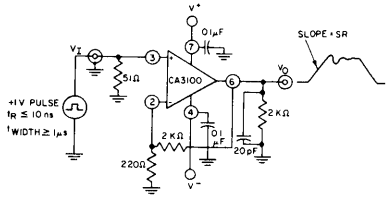


Fig. 16 – Slew rate in 10X amplifier test circuit.

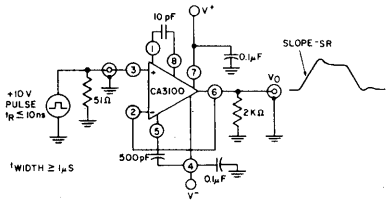


Fig. 17 – Follower slew rate test circuit.

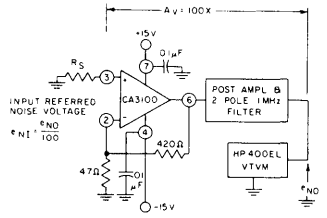


Fig. 18 – Wideband input noise voltage test circuit.

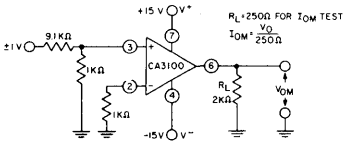


Fig. 19 – Output voltage swing (V_{OM}), output current swing (I_{OM}) test circuit.

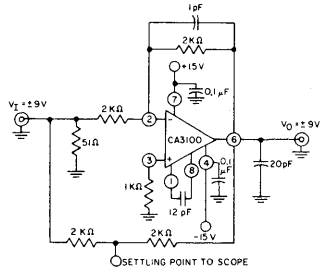


Fig. 20 – Settling time test circuit.

TYPICAL APPLICATIONS

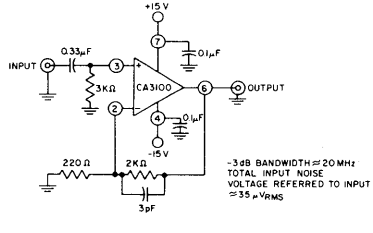


Fig. 21 – 20 dB video amplifier.

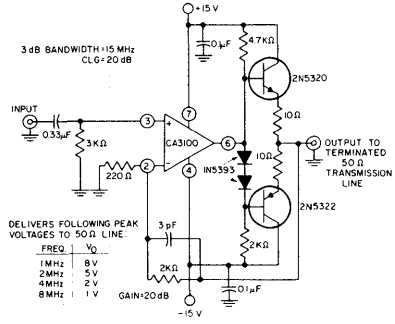


Fig. 22 – 20 dB video line driver.

TYPICAL APPLICATIONS (Cont'd)

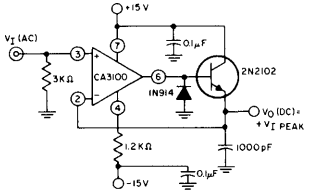


Fig. 23 – Fast positive peak detector.

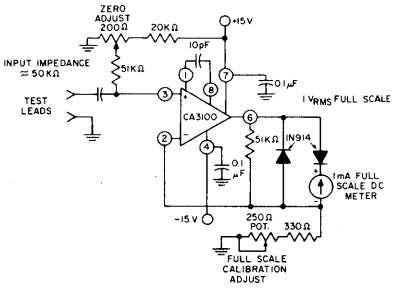


Fig. 24 – 1 MHz meter-driver amplifier.

May 1990

BiMOS Operational Amplifiers

With MOSFET Input/CMOS Output

Features:

- *MOSFET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 x 10^{12}Ω) typ.
  very low I_I = 5 pA typ. at 15 V operation
  = 2 pA typ. at 5 V operation
- *Ideal for single-supply applications*
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *CMOS output stage permits signal swing to either (or both) supply rails*

Applications:

- *Ground-referenced single supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *High-input-impedance comparators (ideal interface with digital CMOS)*
- *High-input-impedance wideband amplifiers*
- *Voltage followers (e.g. follower for single-supply D/A converter)*
- *Voltage regulators (permits control of output voltage down to zero volts)*
- *Peak detectors*
- *Single-supply full-wave precision rectifiers*
- *Photo-diode sensor amplifiers*

CA3130A and CA3130 are integrated-circuit operation amplifiers that combine the advantage of both CMOS and biploar transistors on a monolithic chip.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

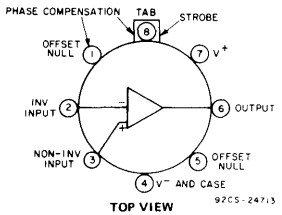
A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3130 Series circuits operate at supply voltges ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

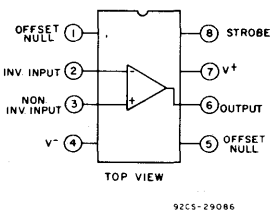
The CA3130 Series is supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA3130 is available in chip form (H suffix). The CA3130 and CA3130A are also available in the Mini-DIP 8-lead dual-in-line plastic package (E suffix), and in the 8-lead Small Outline package (M suffix). All types operate over the full military-temperature range of -55°C to +125°C. The CA3130A offers superior input characteristics over those of the CA3130.

ELECTRICAL CHARACTERISTICS at T_A=25°C, V^+=15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS						Units
	CA3130A (T,S,E)			CA3130 (T,S,E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$, $V^{\pm}$=±7.5 V	–	2	5	–	8	15	mV
Input Offset Current, $\|I_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.5	20	–	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	–	5	30	–	5	50	pA
Large-Signal Voltage Gain, A_{OL}	50 k	320 k	–	50 k	320 k	–	V/V
V_O=10 V_{p-p}, R_L=2 kΩ	94	110	–	94	110	–	dB
Common-Mode Rejection Ratio, CMRR	80	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR}	0	−0.5 to 12	10	0	−0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	–	32	150	–	32	320	μV/V
Maximum Output Voltage:							V
At R_L=2 kΩ V_{OM}^+	12	13.3	–	12	13.3	–	
At R_L=2 kΩ V_{OM}^-	–	0.002	0.01	–	0.002	0.01	
At R_L=∞ V_{OM}^+	14.99	15	–	14.99	15	–	
At R_L=∞ V_{OM}^-	–	0	0.01	–	0	0.01	
Maximum Output Current: I_{OM}^+ (Source) @ V_O = 0 V	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O = 15 V	12	20	45	12	20	45	mA
Supply Current, I^+: V_O=7.5 V, R_L=∞	–	10	15	–	10	15	mA
V_O = 0 V, R_L = ∞	–	2	3	–	2	3	mA
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$*	–	10	–	–	10	–	μV/°C



S and T Suffixes



E Suffix

Fig. 1 – Functional diagrams for the CA3130 series.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS: $V^+ = +7.5$ V, $V^- = -7.5$ V, $T_A = 25^oC$ (Unless Otherwise Specified)	CA3130A CA3130 (T,S,E)	UNITS
Input Offset Voltage Adjustment Range	10 kΩ across Terms. 4 and 5 or 4 and 1	±22	mV
Input Resistance, R_I		1.5	TΩ
Input Capacitance, C_I	f = 1 MHz	4.3	pF
Equivalent Input Noise Voltage, e_n	BW = 0.2 MHz, R_S = 1 MΩ*	23	μV
Unity Gain Crossover Frequency, f_T	C_C = 0	15	MHz
	C_C = 47 pF	4	
Slew Rate, SR: Open Loop	C_C = 0	30	V/μs
Closed Loop	C_C = 56 pF	10	
Transient Response: Rise Time, t_r	C_C = 56 pF, C_L = 25 pF, R_L = 2 kΩ (Voltage Follower)	0.09	μs
Overshoot		10	%
Settling Time (4 V_{p-p} Input to <0.1%)		1.2	μs

* Although a 1-MΩ source is used for this test, the equivalent input noise remains constant for values of R_S up to 10 MΩ.

CHARACTERISTIC	TEST CONDITIONS: $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$ (Unless Otherwise Specified)	CA3130A (T,S,E)	CA3130 (T,S,E)	UNITS
Input Offset Voltage, V_{IO}		2	8	mV
Input Offset Current, I_{IO}		0.1	0.1	pA
Input Current, I_I		2	2	pA
Common-Mode Rejection Ratio, CMRR		90	80	dB
Large-Signal Voltage Gain, A_{OL}	V_O = 4 V_{p-p}, R_L = 5 kΩ	100 k	100 k	V/V
		100	100	dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.8	0 to 2.8	V
Supply Current, I^+	V_O = 5 V, R_L = ∞	300	300	μA
	V_O = 2.5 V, R_L = ∞	500	500	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	μV/V

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) . . . . . 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE . . . . . ±8 V
COMMON-MODE DC
INPUT VOLTAGE . . . (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT . . . . . 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK −
UP TO 55°C . . . . . 630 mW
ABOVE 55°C . . . . Derate linearly 6.67 mW/°C
WITH HEAT SINK −
UP TO 90°C . . . . . 1 W
ABOVE 90°C . . . Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
OPERATING (all types) . . . . . −55 to + 125°C
STORAGE (all types) . . . . . −65 to + 150°C
OUTPUT SHORT-CIRCUIT.
DURATION * . . . . . INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH
(1.59 ± 0.79 mm) FROM CASE
FOR 10 SECONDS MAX. . . . . +265°C

*Short circuit may be applied to ground or to either supply.

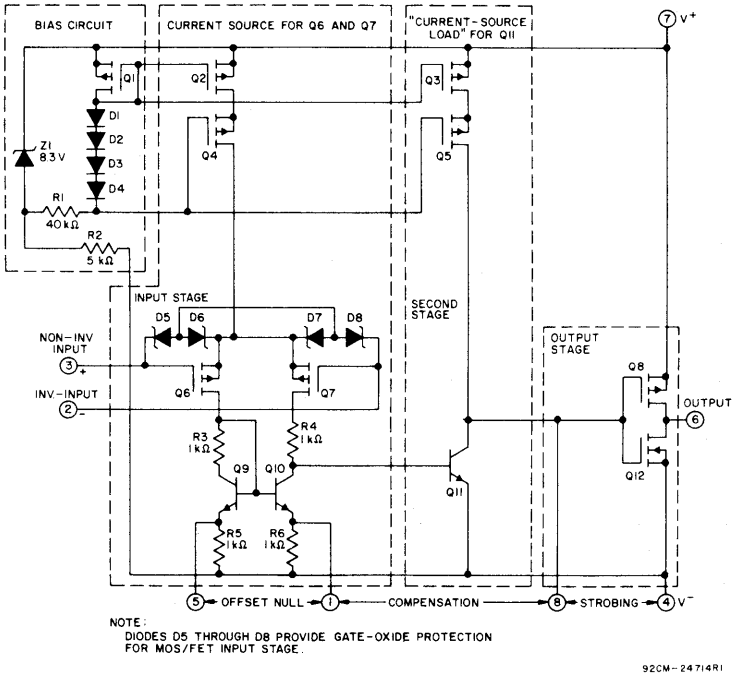


Fig. 2 – Schematic diagram of the CA3130 Series.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3130 Series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA3130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

Input Stages—The circuit of the CA3130 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

Second-Stage—Most of the voltage gain in the CA3130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit—At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes nonconductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage, Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage—The output stage consists of a drain-loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

†For general information on the characteristics of CMOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "CMOS Transistor Array".

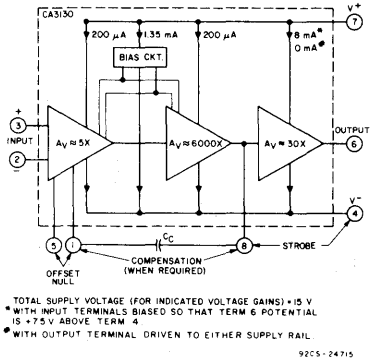


Fig. 3 – Block diagram of the CA3130 Series.

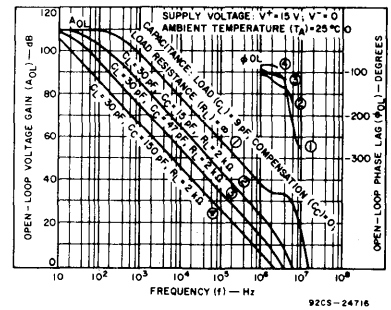


Fig. 4 – Open-loop voltage gain and phase shift vs. frequency for various values of C_L, C_C, and R_L.

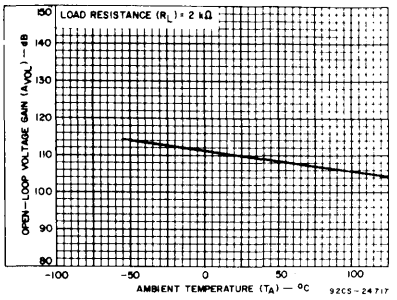


Fig. 5 — Open-loop gain vs. temperature.

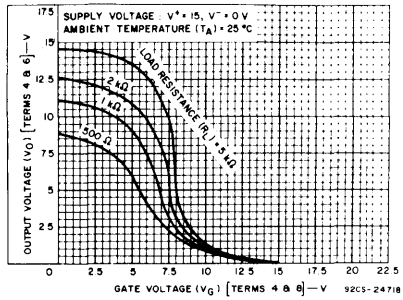


Fig. 6 — Voltage transfer characteristics of CMOS output stage.

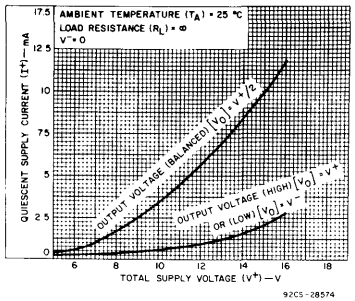


Fig. 7 — Quiescent supply current vs. supply voltage.

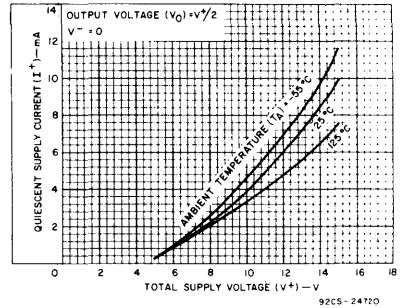


Fig. 8 — Quiescent supply current vs. supply voltage at several temperatures.

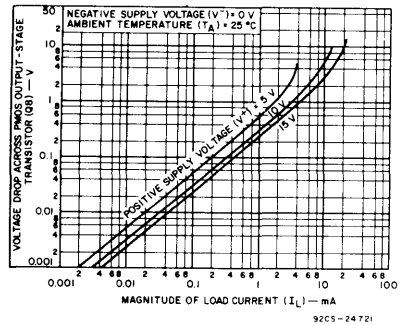


Fig. 9 — Voltage across PMOS output transistor (Q8) vs. load current.

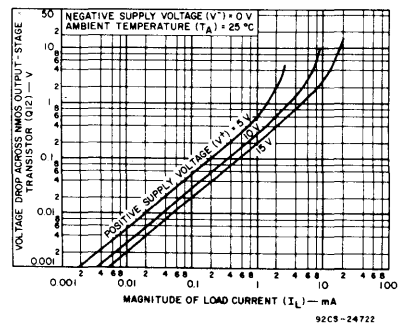


Fig. 10 — Voltage across NMOS output transistor (Q12) vs. load current.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3130 Series Op-Amps is typically 5 pA at T_A=25°C when terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig.11 contains data showing the variation of input current as a function of common-mode input voltage at T_A = 25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied

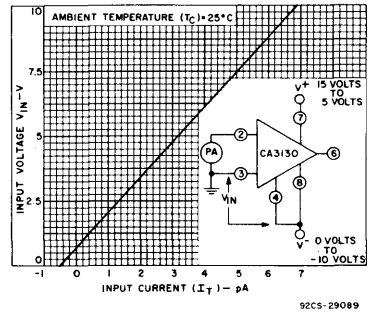


Fig.11 — Input current vs. common-mode voltage.

voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA3130 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig.12 provides data on the typical variation of input bias current as a function of temperature in the CA3130.

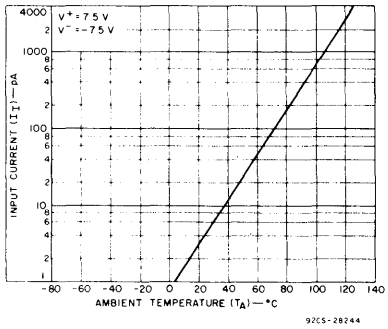


Fig.12 – Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terms. 2 and 3. Fig.13 shows typical data pertinent to shifts in offset voltage encountered with CA3130 devices (TO-5 package) during life testing. At lower temperatures (TO-5 and plastic), for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

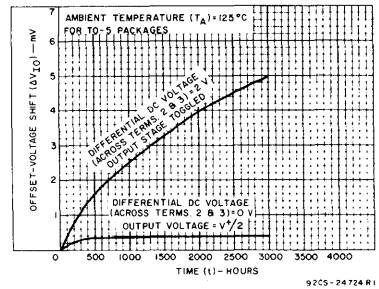


Fig.13 – Typical incremental offset-voltage shift vs. operating life.

Power-Supply Considerations

Because the CA3130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 14a and 14b show the CA3130 connected for both dual- and single-supply operation.

Dual-supply operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e.,

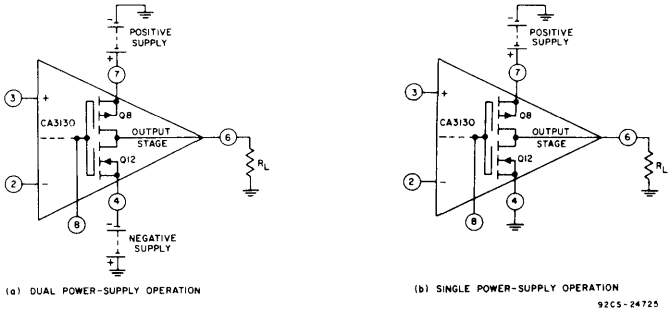


Fig.14 – CA3130 output stage in dual and single power-supply operation.

the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 14a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L=\infty$, by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig.14b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is a $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3130 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23 μV when the test-circuit amplifier of Fig. 15 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

TYPICAL APPLICATIONS

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3130, are particularly suited to service as voltage followers. Fig. 16 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 17, together with related waveforms. This follower circuit is

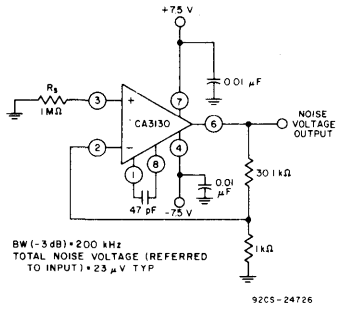
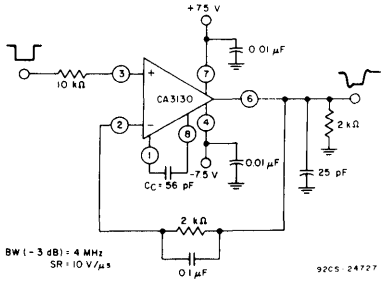
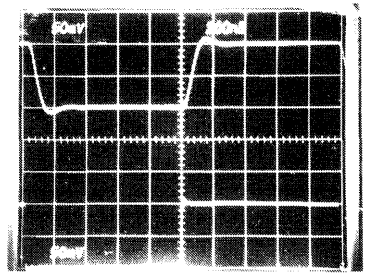
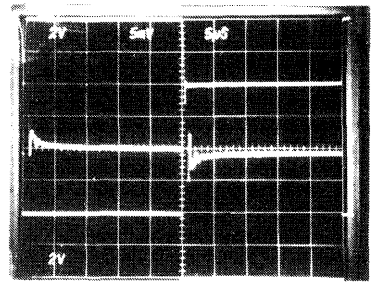


Fig.15 – Test-circuit amplifier (30-dB gain) used for wideband noise measurements.





Top Trace: Output
Bottom Trace: Input
(a) Small-signal response (50 mV/div. and 200 ns/div.)



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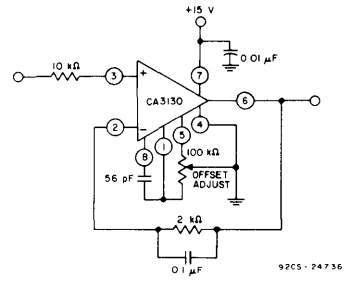
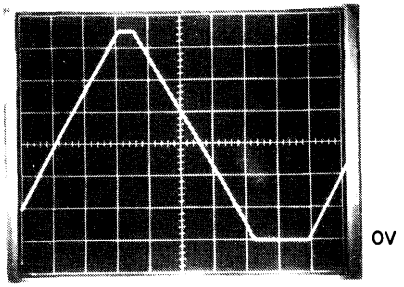
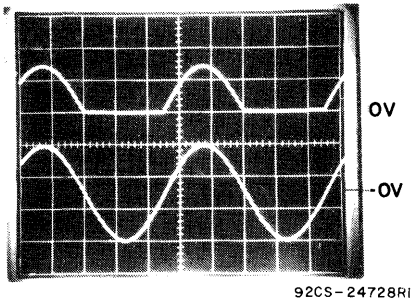
Top Trace: Output signal (2 V/div. and 5 μs/div.)
Center Trace: Difference signal (5 mV/div. and 5 μs/div.)
Bottom Trace: Input signal (2 V/div. and 5 μs/div.)
(b) Input-output difference signal showing settling time (Measurement made with Tektronix 7A13 differential amplifier)

Fig. 16 – Split-supply voltage follower with associated waveforms.





(a) Output-waveform with input-signal ramping (2 V/div. and 500 μs/div.)



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Top Trace: Output (5 V/div. and 200 μs/div.)
Bottom Trace: Input (5 V/div. and 200 μs/div.)
(b) Output-waveform with ground-reference sine-wave input

Fig. 17 – Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080).

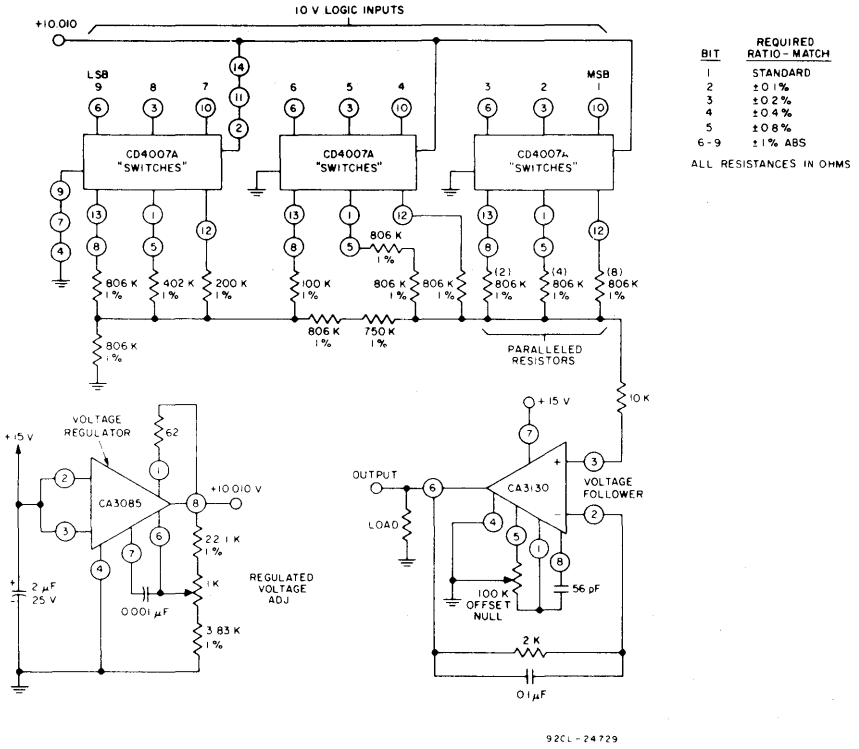
linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 17a with input-signal ramping. The waveforms in Fig. 17b show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 17b also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3130 in a single-supply voltage-follower application.

9-Bit COS/MOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig.18 This system combines the concepts of multiple-switch CMOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 18.

of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with varia-



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS

ALL RESISTANCES IN OHMS

Fig. 18-9-bit DAC using CMOS digital switches and CA3130.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly

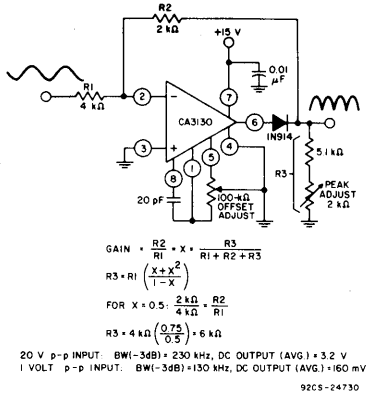
tions of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

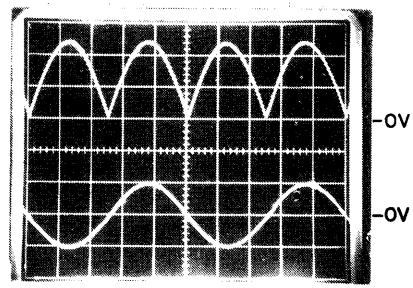
Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

The absolute-value circuit using the CA3130 is shown in Fig. 19. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a

*"Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC", Application Note ICAN-6080.

negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3130 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 19 is satisfied, the full-wave output is symmetrical.





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Top Trace: Output signal (2 V/div.)
Bottom Trace: Input signal (10 V/div.)
Time base on both traces: 0.2 ms/div.

Fig. 19 — Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

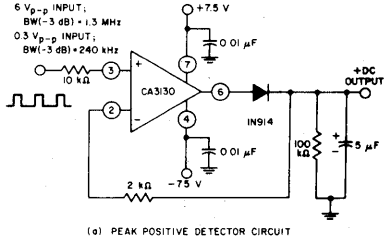
Peak Detectors

Peak-detector circuits are easily implemented with the CA3130, as illustrated in Fig. 20 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA3130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in an active "pull-down" mode so that the intrinsic capacitance can be discharged more expeditiously.

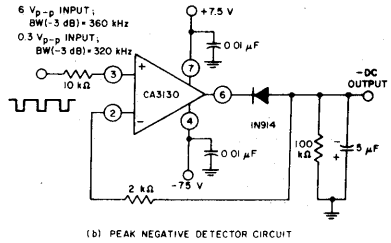
Error-Amplifier in Regulated-Power Supplies

The CA3130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Fig. 21 shows the schematic diagram of a 40-mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zeners to provide supply-voltage for the CA3130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier. Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.

Fig. 22 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous ad-



(a) PEAK POSITIVE DETECTOR CIRCUIT



(b) PEAK NEGATIVE DETECTOR CIRCUIT

92CS-24751

Fig. 20 — Peak-detector circuits.

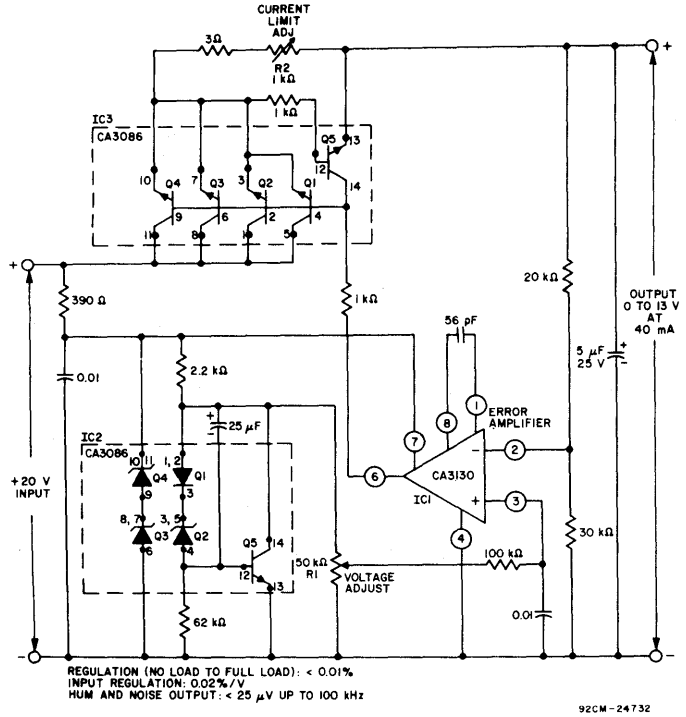


Fig. 21–Voltage regulator circuit (0 to 13 V at 40 mA).

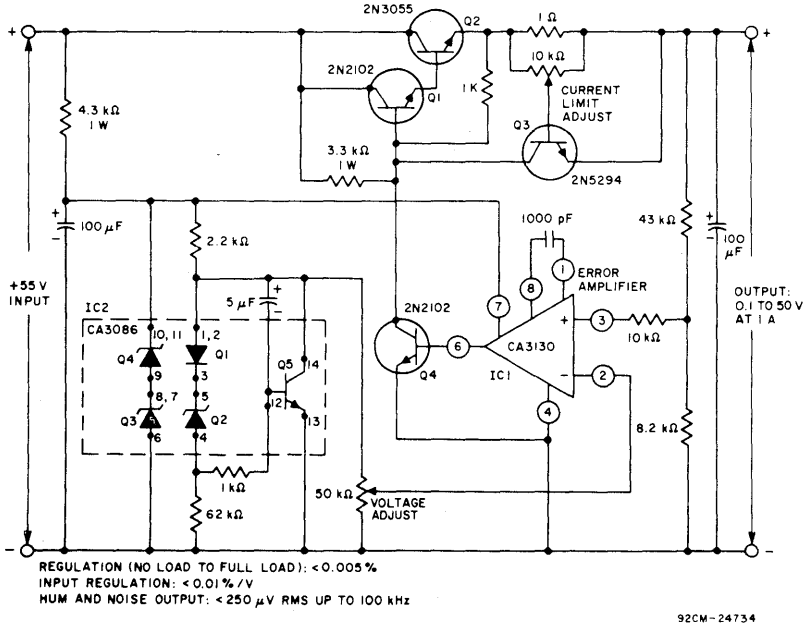


Fig.22 – Voltage regulator circuit (0.1 to 50 V at 1 A).

justment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA3130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on" and "off" periods, is shown in Fig. 23. Resistors R1 and R2 are used to bias the CA3130 to the mid-point of the supply-voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

Function Generator

Fig. 24 contains a schematic diagram of a function generator using the CA3130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_O, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA3130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA3130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

*See File No. 475 and ICAN-6668.

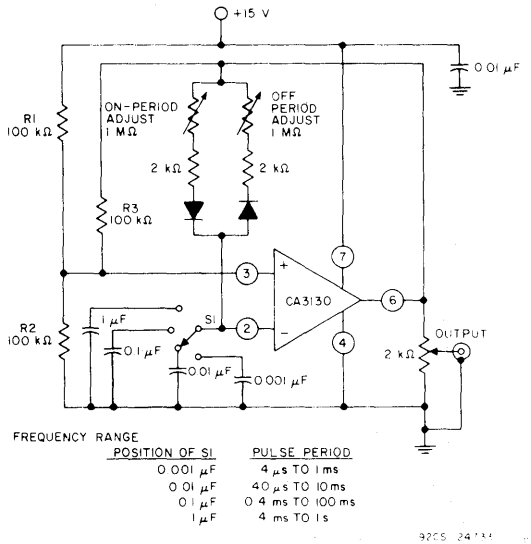


Fig. 23 — Pulse generator (astable multivibrator) with provisions for independent control of "ON" and "OFF" periods.

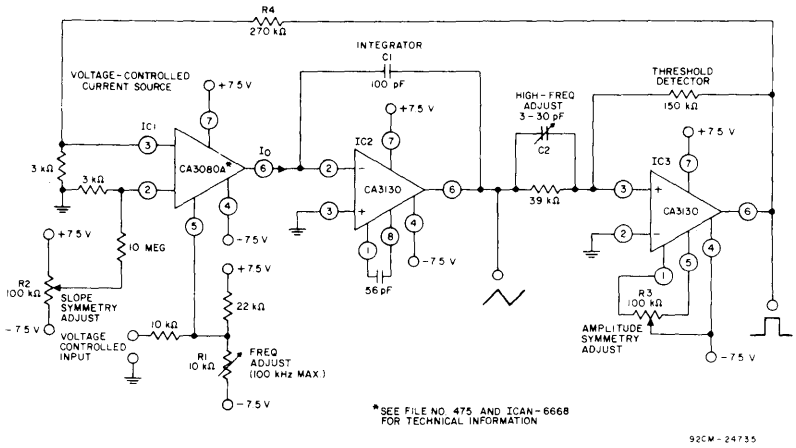


Fig. 24 – Function generator (frequency can be varied 1,000,000/1 with a single control).

Operation with Output-Stage Power-Booster

The current-sourcing and -sinking capability of the CA3130 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 25, three CMOS transistor-pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA3130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA3130 output stage by about 2.5X.

The amplifier circuit in Fig. 25 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (–3 dB) is 50 kHz.

*See File No. 619 for technical information.

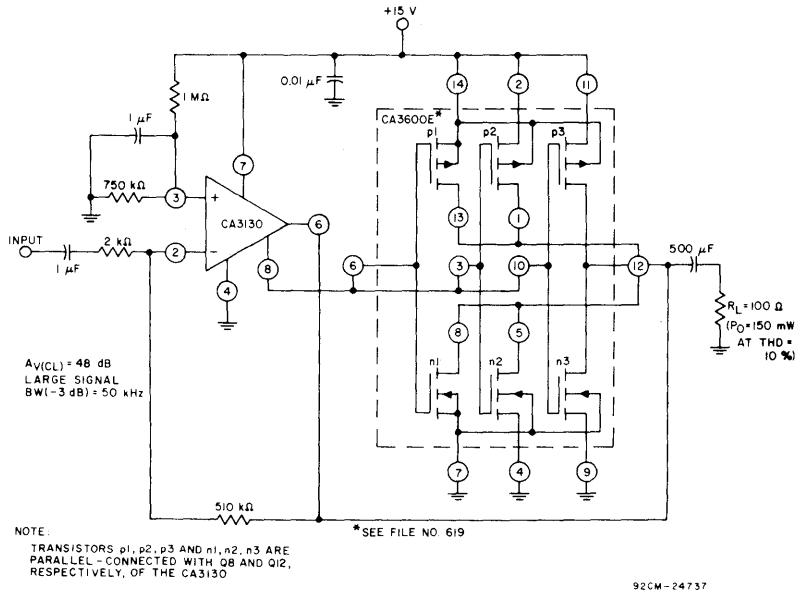


Fig. 25 - CMOS transistor array (CA3600E) connected as power-booster in the output stage of the CA3130.

May 1990

BiMOS Operational Amplifiers

With MOSFET Input/Biploar Output

Features:

- *MOSFET Input Stage*
  (a) Very high input impedance (Z_{IN}) -1.5 TΩ typ.
  (b) Very low input current (I_I) -10 pA typ. at ±15 V
  (c) Wide common-mode input-voltage range (VICR) - can be swung 0.5 volt below negative supply-voltage rail
  (d) Output swing complements input common-mode range
- *Directly replaces industry type 741 in most applications*

Applications:

- *Ground-referenced single-supply amplifiers in automobile and portable instrumentation*
- *Sample and hold amplifiers*
- *Long-duration timers/multivibrators (microseconds-minutes-hours)*
- *Photocurrent instrumentation*
- *Peak detectos*
- *Active filters*
- *Comparators*
- *Interface in 5 V TTL systems and other low-supply voltage systems*
- *All standard operational amplifier applications*
- *Function generators*
- *Tone controls*
- *Power supplies*
- *Portable instruments*
- *Intrusion alarm systems*

The CA3140A and CA3140 are integrated-circuit operational amplifiers that combine the advantages of high-voltage PMOS transistors with high-voltage biploar transistors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA3130 CMOS operational amplifiers and the versaility of the 741 series of industry-standard operational amplifiers.

The CA3140A and CA3140 BiMOS operational amplifiers feature gate-protected MOSFET (PMOS) transistors in the input circuit to provide very-high-input impedance, very-low-input current, and high-speed performance. The CA3140A and CA3140 operate at supply voltage from 4 to 36 volts (either single or dual supply). These operational amplifiers are internally phase-compensated to achieve stable operation in unity-gain follower operation, and, additionally, have access terminal for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset-voltage nulling. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load-terminal short-circuiting to either supply-rail or to ground.

The CA3140 Series has the same 8-lead terminal pin-out used for the "741" and other industry-standard operational amplifiers. They are supplied in either the standard 8-lead TO-5 style package (T suffix), or in the 8-lead dual-in-line formed-lead TO-5 style package "DIL-CAN" (S suffix). The CA3140 is available in chip form (H suffix). The CA3140A and CA3140 are also available in an 8-lead Small Outline package (M suffix) and in an 8-lead dual-in-line plastic package (MINI-DIP - E suffix). The CA3140A and CA3140 are intended for operation at supply voltage up to 36 volts (±18 volts). All types can be operated safely over the temperature range from -55°C to +125°C.

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V, $T_A = 25^oC$	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage Adjustment Resistor		Typ.Value of Resistor Between Term. 4 and 5 or 4 and 1 to Adjust Max. V_{IO}	18	4.7	kΩ
Input Resistance	R_1		1.5	1.5	TΩ
Input Capacitance	C_I		4	4	pF
Output Resistance	R_O		60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 39)	e_n	BW = 140 kHz, R_S = 1 MΩ	48	48	μV
Equivalent Input Noise Voltage (See Fig.10)	e_n	f = 1 kHz, R_S = 100 Ω	40	40	$nV/\sqrt{Hz}$
		f = 10 kHz, R_S = 100 Ω	12	12	$nV/\sqrt{Hz}$
Short-Circuit Current to Opposite Supply: Source	I_{OM^+}		40	40	mA
Sink	I_{OM^-}		18	18	mA
Gain-Bandwidth Product, (See Figs. 5 &18)	f_T		4.5	4.5	MHz
Slew Rate, (See Fig.6)	SR		9	9	V/μs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low			220	220	μA
Transient Response: Rise Time	t_r	$R_L = 2$ kΩ, $C_L = 100$ pF	0.08	0.08	μs
Overshoot (See Fig. 37)	t_r	$R_L = 2$ kΩ, $C_L = 100$ pF	10	10	%
Settling Time at 10 V_{p-p}, 1 mV (See Fig.17)	t_s	$R_L = 2$ kΩ, $C_L = 100$ pF, Voltage Follower	4.5	4.5	μs
Settling Time at 10 V_{p-p}, 10 mV (See Fig.17)	t_s	$R_L = 2$ kΩ, $C_L = 100$ pF, Voltage Follower	1.4	1.4	μs

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At $V^+ = 15$ V, $V^- = 15$ V, $T_A = 25^oC$ Unless Otherwise Specified

CHARACTERISTIC	LIMITS						UNITS
	CA3140A			CA3140			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	–	2	5	–	5	15	mV
Input Offset Current, $\|I_{IO}\|$	–	0.5	20	–	0.5	30	pA
Input Current, I_I	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}● (See Figs. 4,18)	20 k	100 k	–	20 k	100 k	–	V/V
	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR (See Fig.9)	–	32	320	–	32	320	μV/V
	70	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR} (See Fig.20)	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	11	V
Power-Supply Rejection Ratio, PSRR $\Delta V_{IO}/\Delta V$ (See Fig.11)	–	100	150	–	100	150	μV/V
	76	80	–	76	80	–	dB
Max. Output Voltage■ V_{OM}^+ (See Figs.13,20) V_{OM}^-	+12	13	–	+12	13	–	V
	−14	−14.4	–	−14	−14.4	–	
Supply Current, I^+ (See Fig.7)	–	4	6	–	4	6	mA
Device Dissipation, P_D	–	120	180	–	120	180	mW
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$	–	6	–	–	8	–	μV/°C
Max. Output Voltage,★ V_{OM}^+	–	–	–	–	–	–	V
V_{OM}^-	–	–	–	–	–	–	

● At $V_O = 26V_{p\text{-}p}$, +12V, −14V and $R_L = 2\ k\Omega$.

■ At $R_L = 2\ k\Omega$.

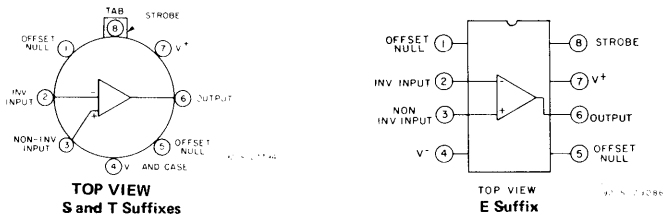


Fig. 1 – Functional diagrams of the CA3140 series.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

CA3140, CA3140A

DC SUPPLY VOLTAGE
(BETWEEN V^+ AND V^- TERMINALS) ..... 36 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ± 8 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8 V) to (V^- -0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK -
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate linearly 6.67 mW/°C
WITH HEAT SINK -
UP TO 55°C ..... 1 W
ABOVE 55°C ..... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING (ALL TYPES) ..... -55 to +125°C
STORAGE (ALL TYPES) ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION* ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)
FROM CASE FOR 10 SECONDS MAX. ..... +265°C

* Short circuit may be applied to ground or to either supply.

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE
At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$

CHARACTERISTIC		CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage	$\|V_{IO}\|$	2	5	mV
Input Offset Current	$\|I_{IO}\|$	0.1	0.1	pA
Input Current	I_I	2	2	pA
Input Resistance		1	1	TΩ
Large-Signal Voltage Gain	A_{OL}	100 k	100 k	V/V
(See Figs.4,18)		100	100	dB
Common-Mode Rejection Ratio,	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range	V_{ICR}	−0.5	−0.5	V
(See Fig.20)		2.6	2.6	
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	100	100	μV/V
		80	80	dB
Maximum Output Voltage	V_{OM}^+	3	3	V
(See Figs.13,20)	V_{OM}^-	0.13	0.13	
Maximum Output Current:				
Source	I_{OM}^+	10	10	mA
Sink	I_{OM}^-	1	1	
Slew Rate (See Fig.6)		7	7	V/μs
Gain-Bandwidth Product (See Fig.5)	f_T	3.7	3.7	MHz
Supply Current (See Fig.7)	I^+	1.6	1.6	mA
Device Dissipation	P_D	8	8	mW
Sink Current from Term. 8 to Term. 4 to Swing Output Low		200	200	μA

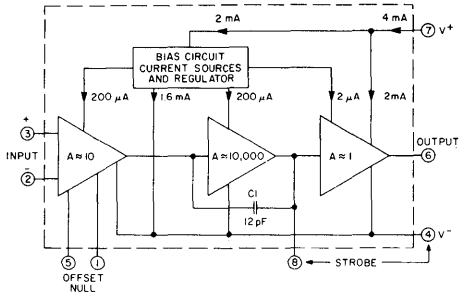


Fig.2 – Block diagram of CA3140 series.

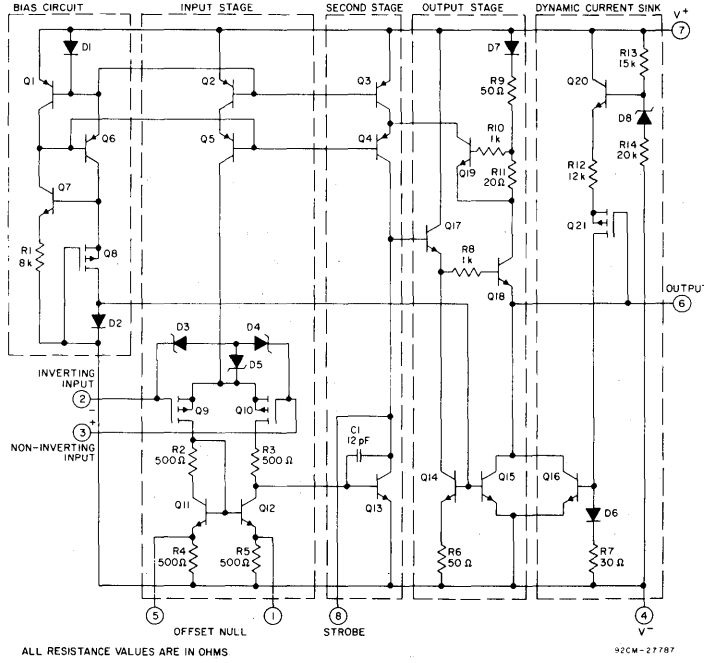


Fig.3 – Schematic diagram of CA3140 series.

CIRCUIT DESCRIPTION

Fig.2 is a block diagram of the CA3140 Series PMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant-current flow circuits in the first and second stages. The CA3140 includes an on-chip phase-compensating capacitor that is sufficient for the unity gain voltage-follower configuration.

Input Stages – The schematic circuit diagram of the CA3140 is shown in Fig.3. It consists of a differential-input stage using PMOS field-effect transistors (Q9, Q10) working into a mirror pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror-pair transistors also function as a differen-

tial-to-single-ended converter to provide base-current drive to the second-stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10-kΩ potentiometer connected across terminals 1 and 5 and with its slider arm connected to terminal 4. Cascode-connected bipolar transistors Q2, Q5 are the constant-current source for the input stage. The base-biasing circuit for the constant-current source is described subsequently. The small diodes D3, D4, D5 provide gate-oxide protection against high-voltage transients, e.g., static electricity.

Second Stage – Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode-connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll-off) can be accomplished, when desired, by simply connecting a small capacitor between terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (terminal 4) by mechanical or electrical means, the output terminal 6 swings low, i.e., approximately to terminal 4 potential.

Output Stage – The CA3140 Series circuits employ a broadband output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q17, Q18) is established by transistors (Q14, Q15) whose base-currents are "mirrored" to current flowing through diode D2 in the bias circuit section. When the CA3140 is operating such that output terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

When the CA3140 is operating such that output terminal 6 is sinking current to the V– bus, transistor Q16 is the current-sinking element. Transistor Q16 is mirror-connected to D6, R7, with current fed by way of Q21, R12, and Q20. Transistor Q20, in turn, is biased by current-flow through R13, zener D8, and R14. The dynamic current-sink is controlled by voltage-level sensing. For purposes of explanation, it is assumed that output terminal 6 is quiescently established at the potential mid-point between the V+ and V– supply rails. When output-current sinking-mode operation is required, the collector potential of transistor Q13 is driven below its quiescent level, thereby causing Q17, Q18 to decrease the output voltage at terminal 6. Thus, the gate terminal of PMOS transistor Q21 is displaced toward the V– bus, thereby reducing the channel resistance of Q21. As a consequence, there is an incremental increase in current flow through Q20, R12, Q21, D6, R7, and the base of Q16. As a result, Q16 sinks current from terminal 6 in direct response to the incremental change in output voltage caused by Q18. This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q18. Short-circuit protection of the output circuit is provided by Q19, which is driven into conduction by the high voltage drop developed across R11 under output short-circuit conditions. Under these conditions, the collector of Q19 diverts current from Q4 so as to reduce the base-current drive from Q17, thereby limiting current flow in Q18 to the short-circuited load terminal.

Bias Circuit – Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R1. The function of the bias circuit is to establish and maintain constant-current flow through D1, Q6, Q8 and D2. D1 is a diode-connected transistor mirror-connected in parallel with the base-emitter junctions of Q1, Q2, and Q3. D1 may be considered as a current-sampling diode that senses the emitter current of Q6 and automatically adjusts the base current of Q6 (via Q1) to maintain a constant current through Q6, Q8, D2. The base-currents in Q2, Q3 are also determined by constant-current flow D1. Furthermore, current in diode-connected transistor D2 establishes the currents in transistors Q14 and Q15.

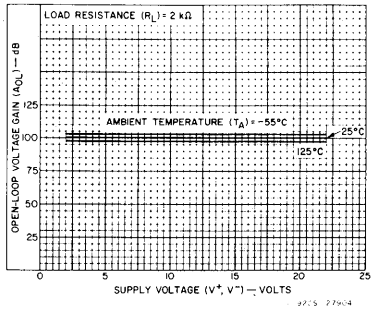


Fig.4 – Open-loop voltage gain vs supply voltage and temperature.

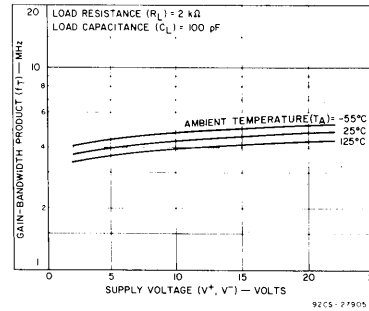


Fig.5 – Gain-bandwidth product vs supply voltage and temperature.

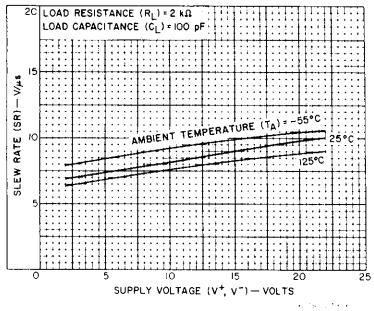


Fig.6 – Slew rate vs supply voltage andtemperature.

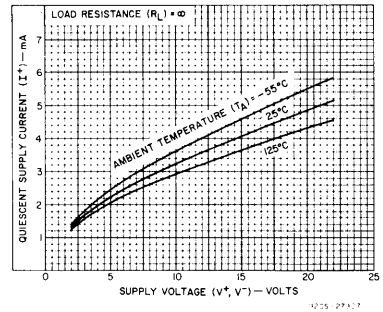


Fig.7 – Quiescent supply current vs supply voltage and temperature.

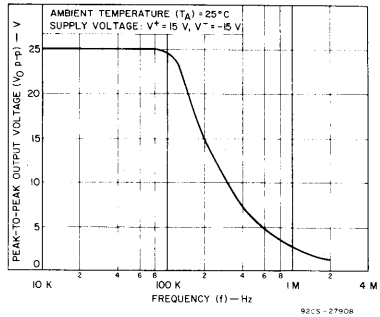


Fig.8 – Maximum output voltage swing vs frequency.

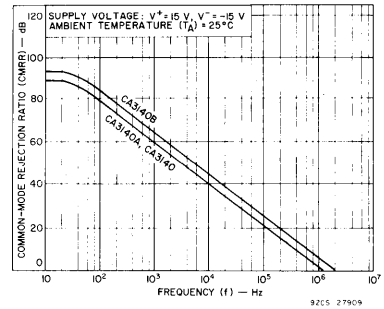


Fig.9 – Common-mode rejection ratio vs frequency.

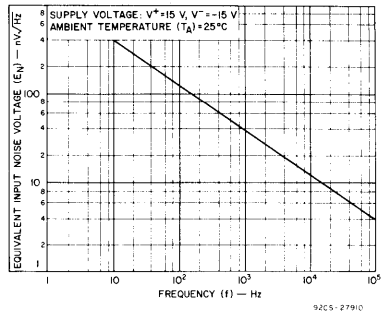


Fig.10 – Equivalent input noise voltage vs frequency.

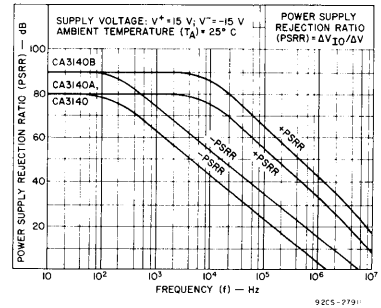


Fig.11 – Power supply rejection ratio vs frequency.

APPLICATIONS CONSIDERATIONS

Wide dynamic range of input and output characteristics with the most desirable high input-impedance characteristic is achieved in the CA3140 by the use of an unique design based upon the PMOS-Bipolar process. Input-common-mode voltage range and output-swing capabilities are complementary, allowing operation with the single supply down to four volts.

The wide dynamic range of these parameters also means that this device is suitable for many single-supply applications, such as, for example, where one input is driven below the potential of terminal 4 and the phase sense of the output signal must be maintained — a most important consideration in comparator applications.

OUTPUT CIRCUIT CONSIDERATIONS

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2-volt zener diode connected to terminal 8 as shown in Fig.12. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the CA3140. These voltages are independent of the operating supply voltage.

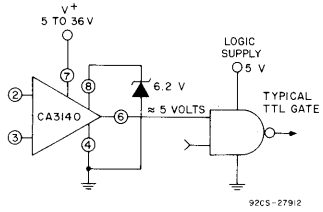


Fig.12 — Zener clamping diode connected to terminals 8 and 4 to limit CA3140 output swing to TTL levels.

Fig.13 shows output current-sinking capabilities of the CA3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

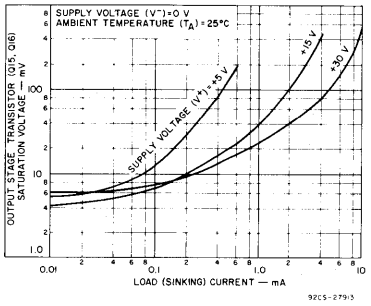


Fig.13 — Voltage across output transistors Q15 and Q16 vs load current.

Fig.16 show some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

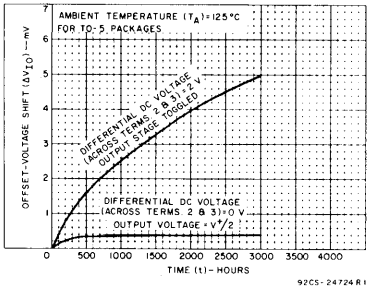


Fig.14 — Typical incremental offset-voltage shift vs operating life.

OFFSET-VOLTAGE NULLING

The input-offset voltage can be nulled by connecting a 10-kΩ potentiometer between terminals 1 and 5 and returning its wiper arm to terminal 4, see Fig.15a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig.15b, to optimize its utilization range are given in the table "Typical Electrical Characteristics" shown in this bulletin.

An alternate system is shown in Fig.15c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

LOW-VOLTAGE OPERATION

Operation at total supply voltages as low as 4 volts is possible with the CA3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low-voltage limitation occurs when the upper extreme of the input common-mode voltage range extends down to the voltage at terminal 4. This limit is reached at a total

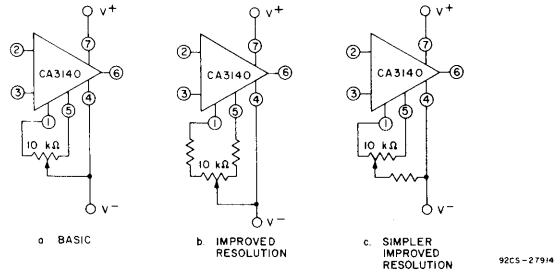


Fig. 15 – Three offset-voltage nulling methods.

supply voltage just below 4 volts. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Fig.20 shows these characteristics and shows that with 2-volt dual supplies, the lower extreme of the input common-mode voltage range is below ground potential.

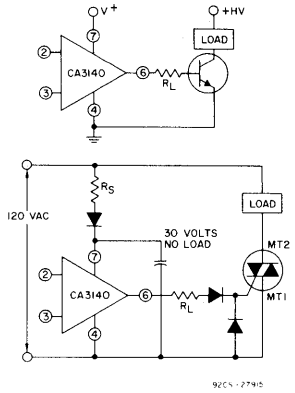


Fig. 16 – Methods of utilizing the $V_{CE}(sat)$ sinking-current capability of the CA3140 series.

BANDWIDTH AND SLEW RATE

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between terminals 1 and 8 can reduce the open-loop −3 dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Fig.17 shows the typical settling time required to reach 1 mV or 10 mV of the final value for various levels of large signal inputs for the voltage-follower and inverting unity-gain amplifiers. The exceptionally fast setting time characteristics are largely due to the high combination of high gain and wide bandwidth of the CA3140; as shown in Fig. 18.

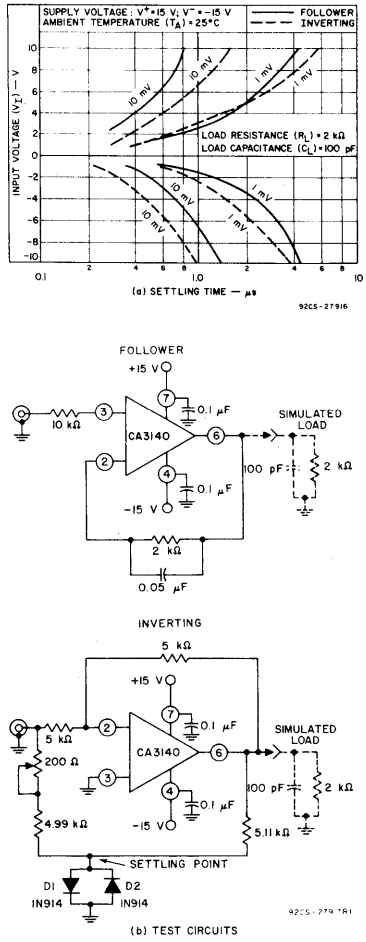


Fig. 17 – Input voltage vs settling time.

INPUT CIRCUIT CONSIDERATIONS

As mentioned previously, the amplifier inputs can be driven below the terminal 4 potential, but a series current-limiting re-

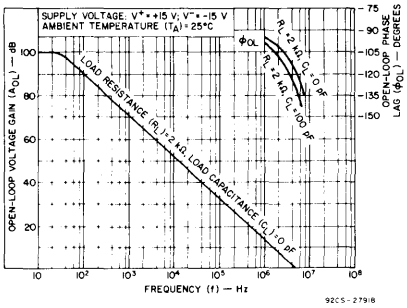


Fig.18 — Open-loop voltage gain and phase lag vs frequency.

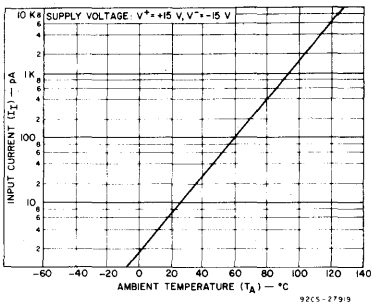


Fig.19 — Input current vs ambient temperature.

sistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig.19 shows typical input-terminal current versus ambient temperature for the CA3140.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Fig.14 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of 125°C (for TO-5); at lower temperatures (TO-5 and plastic), for example, at 85°C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetircal, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar a transistor input stage.

SUPER SWEEP FUNCTION GENERATOR

A function generator having a wide tuning range is shown in Fig.21. The 1,000,000/1

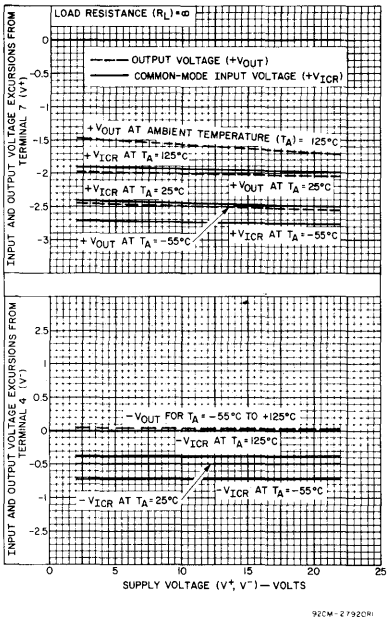


Fig.20 — Output-voltage-swing capability and common-mode input-voltage range vs supply voltage and temperature.

adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting read-out amplifier of the triangular signal developed across the integrating capacitor network connected to the output of the CA3080A current source.

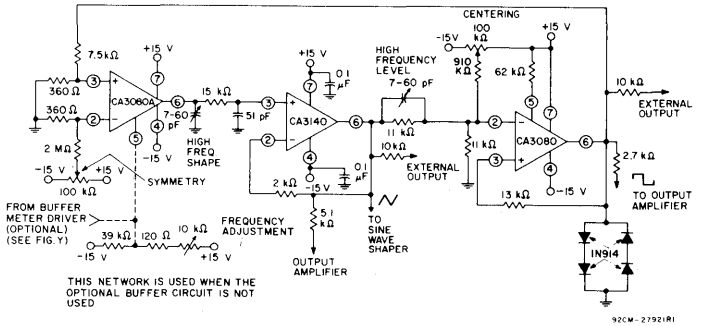
Buffered triangular output signals are then applied to a second CA3080 functioning as a high-speed hysteresis switch. Output from the switch is returned directly back to the

input of the CA3080A current source, thereby, completing the positive feedback loop.

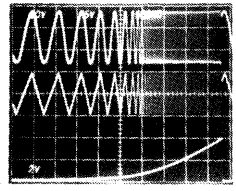
The triangular output level is determined by the four 1N914 level-limiting diodes of the second CA3080 and the resistor-divider network connected to terminal No.2 (input) of the CA3080. These diodes establish the input trip level to this switching stage and, therefore, indirectly determine the amplitude of the output triangle.

Compensation for propagation delays around the entire loop is provided by one adjustment on the input of the CA3080. This adjustment, which provides for a constant generator amplitude output, is most easily made while the generator is sweeping. High-frequency ramp linearity is adjusted by the single 7-to-60 pF capacitor in the output of the CA3080A.

It must be emphasized that only the CA-3080A is characterized for maximum output linearity in the current-generator function.



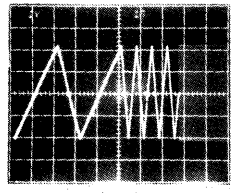
(a) Circuit



TOP TRACE: OUTPUT AT JUNCTION OF 2.7 Ω AND 51 Ω RESISTORS
5 V/DIV AND 500 ms/DIV
CENTER TRACE: EXTERNAL OUTPUT OF TRIANGULAR FUNCTION GENERATOR
2 V/DIV AND 500 ms/DIV
BOTTOM TRACE: OUTPUT OF "LOG" GENERATOR
10 V/DIV AND 500 ms/DIV

92CS-27922

(b1) Function generator sweeping



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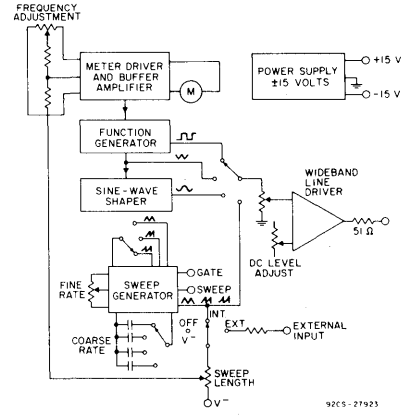


(c) Interconnections

1V/DIV and 1 sec/DIV

Three tone test signals, highest frequency ⩾ 0.5 MHz. Note the slight assymmetry at the three-second/cycle signal. This assymmetry is due to slightly different positive and negative integration from the CA3080A and from the pc board and component leakages at the 100-pA level.

(b2) Function generator with fixed frequencies

Fig.21 – Function generator.

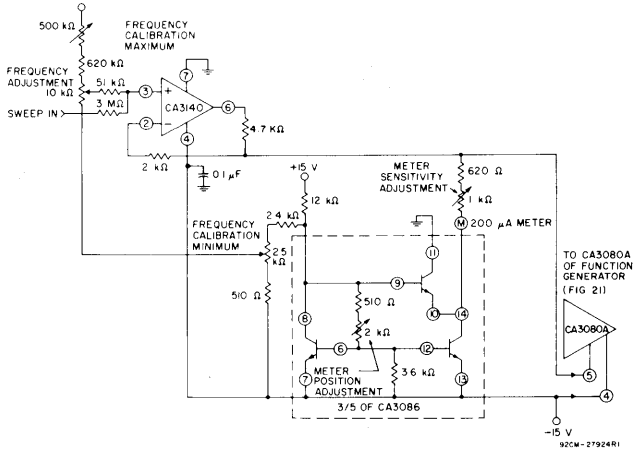


Fig. 22 – Meter driver and buffer amplifier.

METER DRIVER AND BUFFER AMPLIFIER

Fig. 22 shows the CA3140 connected as a meter driver and buffer amplifier. Low driving impedance is required of the CA-3080A current source to assure smooth operation of the Frequency Adjustment Control. This low-driving impedance requirement is easily met by using a CA3140 connected as a voltage follower. Moreover, a meter may be placed across the input to the CA3080A to give a logarithmic analog indication of the function generators frequency.

Analog frequency readout is readily accomplished by the means described above because the output current of the CA3080A varies approximately one decade for each 60-mV change in the applied voltage, V_{ABC} (voltage between terminals 5 and 4 of the CA3080A of the function generator). Therefore, six decades represent 360-mV change in V_{ABC}.

Now, only the reference voltage must be established to set the lower limit on the meter. The three remaining transistors from the CA3086 Array used in the sweep generator are used for this reference voltage. In addition, this reference generator arrangement tends to track ambient temperature variations, and thus compensates for the effects of the normal negative temperature coefficient of the CA3080A V_{ABC} terminal voltage.

Another output voltage from the reference generator is used to insure temperature tracking of the lower end of the Frequency Adjustment Potentiometer. A large series resistance simulates a current source, assuring similar temperature coefficients at both ends of the Frequency Adjustment Control.

To calibrate this circuit, set the Frequency Adjustment Potentiometer at its low end. Then adjust the Minimum Frequency Calibration Control for the lowest frequency. To establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necesary.

Two adjustments are used for the meter. The meter sensitivity control sets the meter-scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects 1/6 of full scale for each decade change in frequency.

SINE-WAVE SHAPER

The circuit shown in Fig. 23 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero-crossing slope is established by the 10-kΩ potentiometer connected between terminals 2 and 6 of the CA3140 and the 9.1-kΩ resistor and 10-kΩ potentiometer from terminal 2 to ground. Two break points are established by diodes D_1 through D_4. Positive feedback via D_5 and D_6 establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage-follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine-wave generator. The initial slope is adjusted with the potentiometer R_1, followed by an adjustment of R_2. The final slope is established by adjusting R_3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessarv

SWEEPING GENERATOR

Fig. 24 shows a sweeping generator. Three CA3140's are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

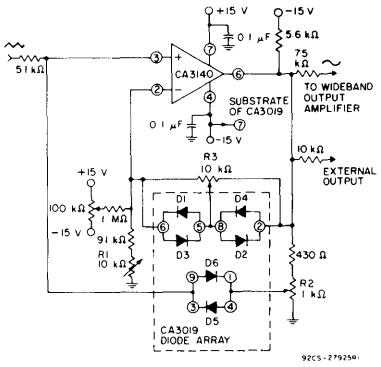


Fig. 23 – Sine-wave shaper.

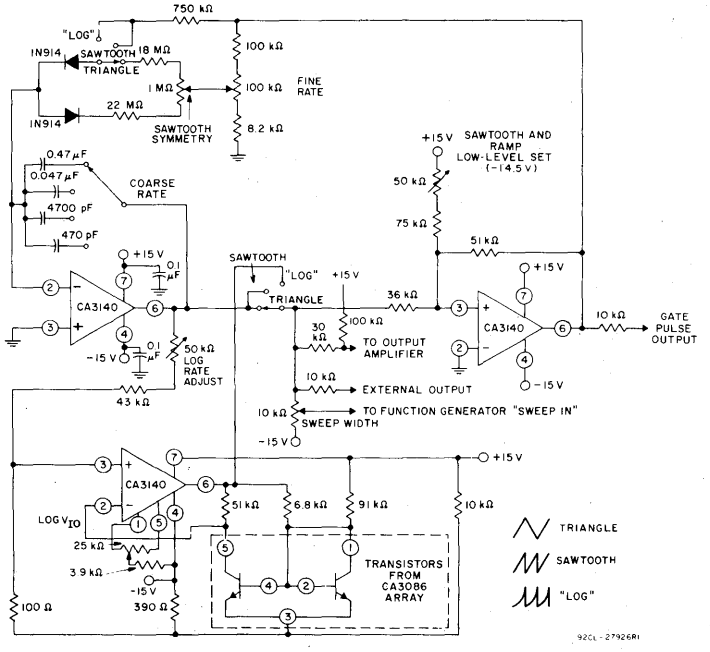


Fig. 24 – Sweeping generator.

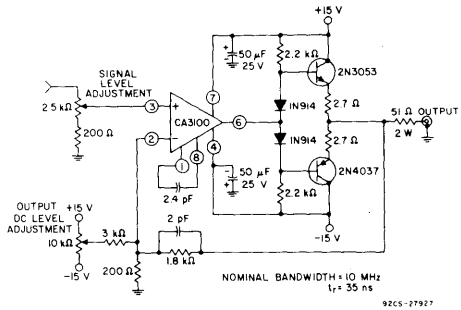


Fig. 25 – Wideband output amplifier.

WIDEBAND OUTPUT AMPLIFIER

Fig. 25 shows a high-slew-rate, wideband amplifier suitable for use as a 50-ohm transmission-line driver. This circuit, when used in conjunction with the function generator and sine-wave shaper circuits shown in Figs. 21 and 23 provides 18 volts peak-to-peak output open-circuited, or 9 volts peak-to-peak output when terminated in 50 ohms. The slew rate required of this amplifier is 28 volts/μs (18 volts peak-to-peak x π x 0.5 MHz).

POWER SUPPLIES

High input-impedance, common-mode capability down to the negative supply and high output-drive current capability are key factors in the design of wide-range output-voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0 to 24 volts.

Unlike many regulator systems using comparators having a bipolar transistor-input stage, a high-impedance reference-voltage divider from a single supply can be used in connection with the CA3140 (see Fig. 26).

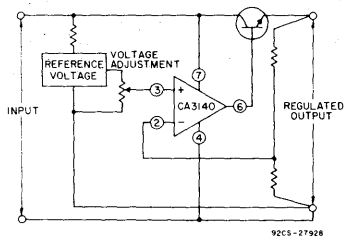


Fig. 26 – Basic single-supply voltage regulator showing voltage-follower configuration.

Essentially, the regulators, shown in Figs. 27 and 28, are connected as non-inverting power operational amplifiers with a gain of 3.2. An 8-volt reference input yields a maximum output voltage slightly greater than 25 volts. As a voltage follower, when the reference input goes to 0 volts the output will be 0 volts. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high I_{CBO} levels will also prevent the output voltage from reaching zero because there is a finite voltage drop (V_{CE}sat) across the output of the CA3140 (see Fig.13). This saturation voltage level may indeed set the lowest voltage obtainable.

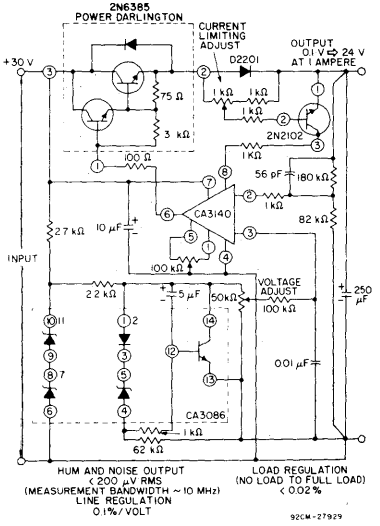


Fig. 27 – Regulated power supply.

The high impedance presented by terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the CA3140 in the event of unusual input or output transients on the supply-rail.

Figs. 27 and 28, show circuits in which a D2201 high-speed diode is used for the current sensor. This diode was chosen for its slightly higher forward-voltage drop characteristic thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1 ampere at 1 volt forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small-signal reference amplifier in the proximity of the current-sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode. In spite of those limitations, the current limiting point can easily be adjusted over the range from 10 mA to 1 ampere with a single adjustment potentiometer. If the temperature stability of the current-limiting system is a serious consideration, the more usual current-sampling resistor-type of circuitry should be employed.

A power Darlington transistor (in a heat sink TO-3 case), is used as the series-pass element for the conventional current-limiting system, Fig. 27, because high-power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat-sink VERSAWATT transistor is used as the series-pass element in the foldback current system, Fig.28, since dissipation levels will only approach 10 watts. In this system, the D2201 diode is used for current sampling. Foldback is provided by the 3 kΩ and 100 kΩ divider network connected to the base of the current-sensing transistor.

Both regulators, Figs. 27 and 28, provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200 μV as read with a meter having a 10-MHz bandwidth.

Fig.31 (a) shows the turn ON and turn OFF characteristics of both regulators. The slow turn-on rise is due to the slow rate of rise of the reference voltage. Fig. 29 (b) shows the transient response of the regulator with the switching of a 20-Ω load at 20 volts output.

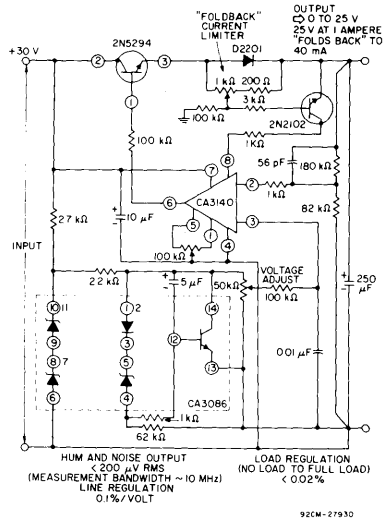
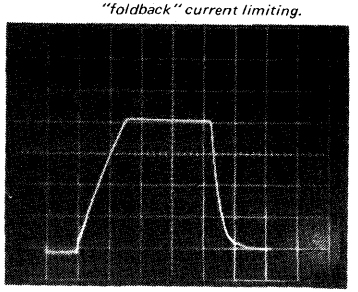


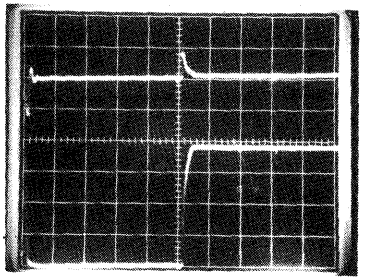
Fig. 28 – Regulated power supply with "foldback" current limiting.



(a)

SUPPLY TURN-ON AND TURN-OFF CHARACTERISTICS
(5 VOLTS / DIV AND 1 s/DIV.)

92CS-27882



(b)

TRANSIENT RESPONSE
TOP TRACE : OUTPUT VOLTAGE
(200 mV/DIV AND 5 μs/DIV)
BOTTOM TRACE COLLECTOR OF LOAD SWITCHING TRANSISTOR,
LOAD = 1 AMPERE
(5 VOLTS/DIV AND 5 μs/DIV)

92CS-27881

Fig. 29 – Waveforms of dynamic characteristics of power supply currents shown in Figs. 29 and 30.

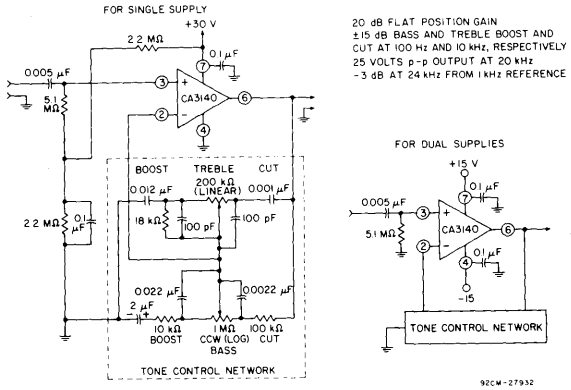


Fig. 30 – Tone control circuit using CA3130 series (20-dB midband gain).

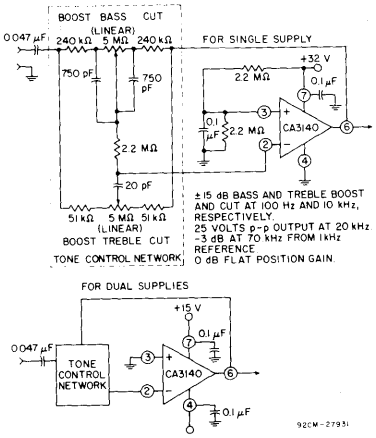


Fig. 31 – Baxandall tone control circuit using CA3140 series.

TONE CONTROL CIRCUITS

High-slew-rate, wide-bandwidth, high-output voltage capability and high input impedance are all characteristics required of tone-control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figs. 30 and 31.

The first circuit, shown in Fig. 31, is the Baxandall tone-control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small-size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are ± 15 dB at 100 Hz and 10 kHz, respectively. Full peak-to-peak output is available up to at least 20 kHz due to the high slew rate of the CA3140. The amplifier gain is −3 dB down from its "flat" position at 70 kHz.

Fig. 30 shows another tone-control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20-dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from terminal No.3 to ground. A detailed analysis of this circuit is given in "An IC Operational Transconductance Amplifier (OTA) With Power Capability" by L, Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No.3, August, 1972.

WIEN BRIDGE OSCILLATOR

Another application of the CA3140 that makes excellent use of its high input-impedance, high-slew-rate, and high-voltage qualities is the Wien Bridge sine-wave oscillator. A basic Wien Bridge oscillator is shown in Fig. 32. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = 1/2\pi RC$ and the gain required for oscillation, A_{OSC} is equal to 3. Note that if C_2 is increased by a factor of four and R_2 is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus per-

mitting a potentially higher operating frequency closer to the gain-bandwidth product of the CA3140.

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, R_S, is commonly replaced with some variable resistance element. Thus, through some control means, the value of R_S is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance is made to increase as the output amplitude is increased are a few of the elements often utilized.

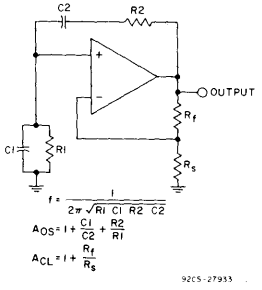


Fig. 32 – Basic Wien bridge oscillator circuit using an operational amplifier.

Fig. 33 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor (R_f of Fig. 32). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1-μF polycarbonate capacitors and 22 MΩ for the frequency determining network, the operating frequency is 0.007 Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180 kHz will reach a slew rate of approximately 9 volts/μs when its amplitude is 16 volts peak-to-peak.

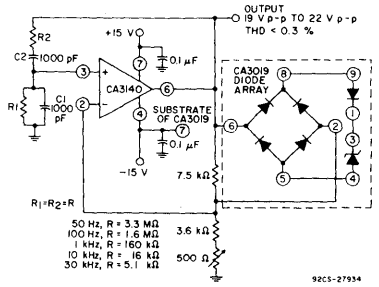


Fig. 33 – Wien bridge oscillator circuit using CA3140 series.

SIMPLE SAMPLE-AND-HOLD SYSTEM

Fig. 34 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The CA3080A serves as both input buffer amplifier and low feed-through transmission switch.* System offset nulling is accomplished with the CA3140 via its offset nulling terminals. A typical simulated load of 2 kΩ and 30 pF is shown in the schematic.

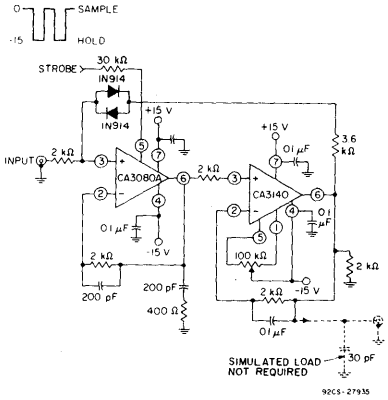
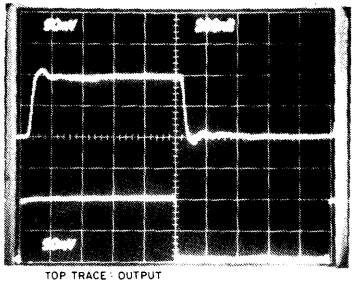


Fig. 34 – Sample- and hold circuit.

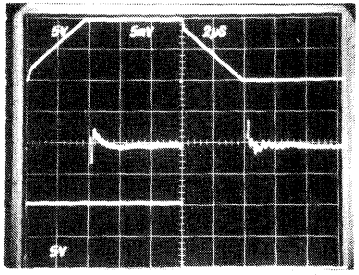
In this circuit, the storage compensation capacitance (C_1) is only 200 pF. Larger value capacitors provide longer "hold" periods but with slower slew rates. The slew rate $\frac{dv}{dt} = \frac{i}{c} = 0.5$ mA/200 pF = 2.5 V/μs.

* ICAN-6668 "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

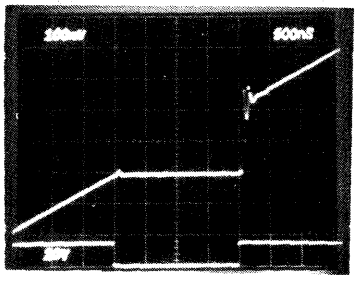
Pulse "droop" during the hold interval is 170 pA/200 pF which is = 0.85 μV/μs; (i.e., 170 pA/200 pF). In this case, 170 pA represents the typical leakage current of the CA3080A when strobed off. If C_1 were increased to 2000 pF, the "hold-droop" rate will decrease to 0.085 μV/μs, but the slew rate would decrease to 0.25 V/μs. The parallel diode network connected between terminal 3 of the CA3080A and terminal 6 of the CA3140 prevents large input-signal feed-through across the input terminals of the CA3080A to the 200 pF storage capacitor when the CA3080A is strobed off. Fig. 35 shows dynamic characteristic waveforms of this sample-and-hold system.



TOP TRACE: OUTPUT
(50 mV/DIV. AND 200 ns/DIV.)
BOTTOM TRACE: INPUT
(50 mV/DIV. AND 200 ns/DIV.)
92CS-27883



LARGE-SIGNAL RESPONSE AND SETTLING TIME
TOP TRACE: OUTPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)
BOTTOM TRACE: INPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)
CENTER TRACE: DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13
(5 mV/DIV. AND 2 μs/DIV.) 92CS-27884



SAMPLING RESPONSE
TOP TRACE: SYSTEM OUTPUT
(100 mV/DIV. AND 500 ns/DIV.)
BOTTOM TRACE: SAMPLING SIGNAL
(20 V/DIV. AND 500 ns/DIV.)
92CS-27885

Fig. 35 – Sample- and hold system dynamic characteristics waveforms.

CURRENT AMPLIFIER

The low input-terminal current needed to drive the CA3140 makes it ideal for use in current-amplifier applications such as the one shown in Fig. 36.● In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100 nA, with values shown, the load current presented to the supply will be 100 μA; a much easier current to measure in many systems.

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output-load capacitance and the potential oscillation in this situation. Essentially, the necessary high-frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

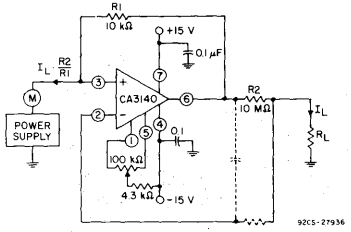


Fig. 36 – Basic current amplifier for low-current measurement systems.

Fig. 37 shows a single-supply, absolute-value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No.6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3140 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 37 is satisfied, the full-wave output is symmetrical.

● "Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308 – "Negative Immittance Converter Circuits".

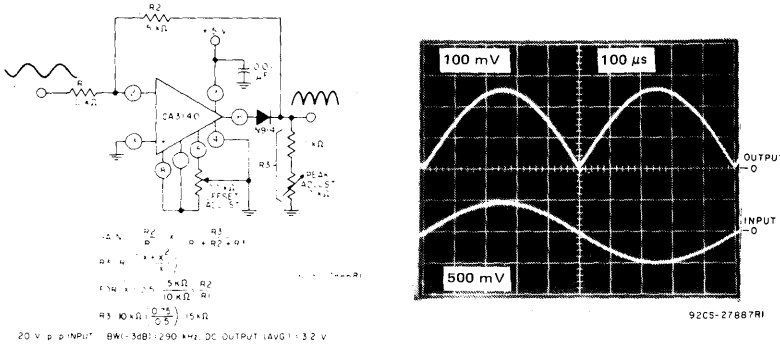
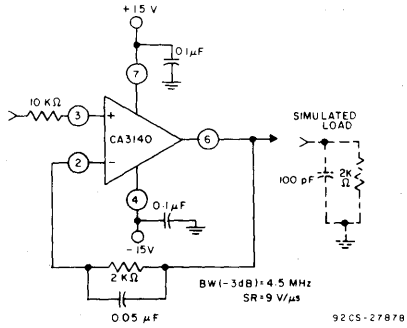
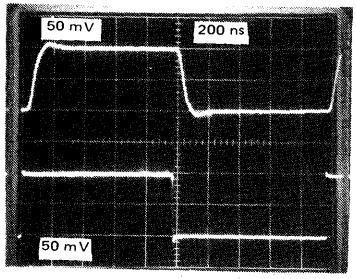
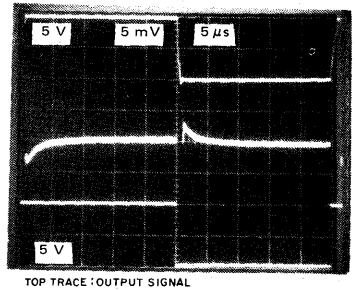


Fig. 37 – Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.





TOP TRACE: OUTPUT
(50 mV/DIV AND 200 ns/DIV)
BOTTOM TRACE: INPUT
(50 mV/DIV AND 200 ns/DIV)
(a) SMALL-SIGNAL RESPONSE
(50 mV/DIV AND 200 ns/DIV)
92CS-27879



TOP TRACE: OUTPUT SIGNAL
(5 V/DIV. AND 5 µs/DIV.)
CENTER TRACE: DIFFERENCE SIGNAL
(5m V/DIV. AND 5 µs/DIV.)
BOTTOM TRACE: INPUT SIGNAL
(5V/DIV. AND 5 µs/DIV)
(b) INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME (MEASUREMENT MADE WITH TEKTRONIX 7A13 DIFFERENTIAL AMPLIFIER)
92CS-27880

Fig. 38 – Split-supply voltage-follower test circuit and associated waveforms.

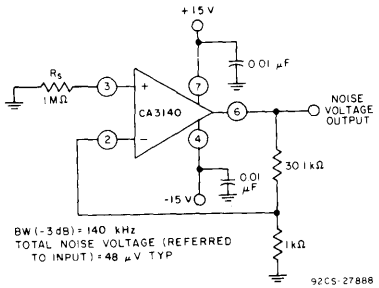
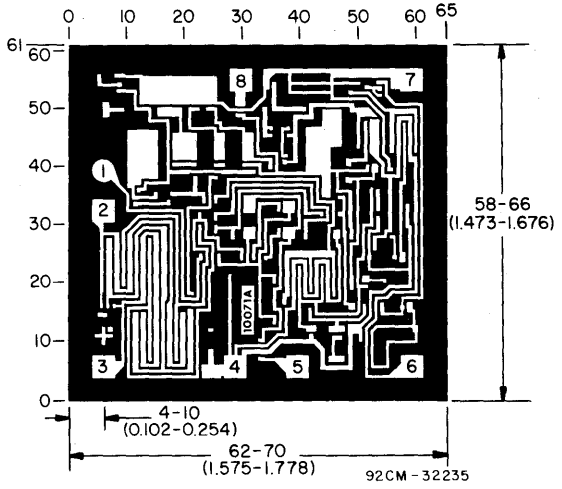


Fig. 39 – Test circuit amplifier (30-dB gain) used for wideband noise measurement.



Dimensions and pad layout for CA3140H.

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

May 1990

BiMOS Operational Amplifiers

With MOSFET Input/CMOS Output

Features:

- *MOSFET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 x 10^{12}Ω) typ.
  very low I_I = 5 pA typ. at 15 V operation
  = 2 pA typ. at 5 V operation
- *Common-mode input voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *CMOS output stage permits signal swing to either (or both) supply rails*

Applications:

- *Ground referenced single supply amplifiers*
- *Fast sample hold amplifiers*
- *Long duration timers/monostables*
- *High input impedance wideband amplifiers*
- *Voltage followers (e.g. follower for single supply D/A converter)*
- *Wien-Bridge oscillators*
- *Voltage controlled oscillators*
- *Photo diode sensor amplifiers*

The CA3160A and CA3160 are integrated circuit operational amplifiers that combine the advantage of both CMOS and biploar transistors on a monolithic chip. The CA3160 series are frequency compensated versions of the popular CA3130 series.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common-mode input voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

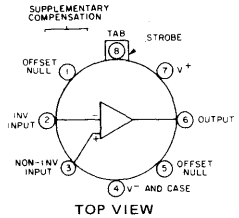
A complementary symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3160 Series circuits operate at supply voltges ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies, and have terminals for adjustment of offset voltage for applications requiring offset null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA3160 Series is supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA3160 is available in chip form (H suffix). The CA3160 and CA3160A are also available in the Mini-DIP 8-lead dual-in-line plastic package (Mini-DIP-E suffix). All types operate over the full military temperature range of -55°C to +125°C. The CA3160A offers superior input characteristics over those of the CA3160.

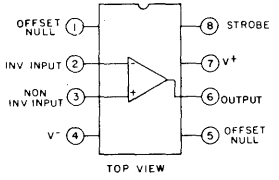
ELECTRICAL CHARACTERISTICS at T_A=25°C, V^+=15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS						Units
	CA3160A (T, S, E)			CA3160 (T, S, E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$, $V^{\pm}$=±7.5 V	–	2	5	–	6	15	mV
Input Offset Current, $\|I_{IO}\|$, $V^{\pm}$=±7.5 V	–	0.5	20	–	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	–	5	30	–	5	50	pA
Large-Signal Voltage Gain, A_{OL}	50 k	320 k	–	50 k	320 k	–	V/V
V_O=10 $V_{p\text{-}p}$, R_L=2 kΩ	94	110	–	94	110	–	dB
Common-Mode Rejection Ratio, CMRR	80	95	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR}	0	−0.5 to 12	10	0	−0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	–	32	150	–	32	320	μV/V
Maximum Output Voltage:							
At R_L=2 kΩ V_{OM}^+	12	13.3	–	12	13.3	–	V
At R_L=2 kΩ V_{OM}^-	–	0.002	0.01	–	0.002	0.01	V
At R_L=∞ V_{OM}^+	14.99	15	–	14.99	15	–	V
At R_L=∞ V_{OM}^-	–	0	0.01	–	0	0.01	V
Maximum Output Current: I_{OM}^+ (Source) @ V_O = 0 V	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O = 15 V	12	20	45	12	20	45	mA
Supply Current, I^+: V_O=7.5 V, R_L=∞	–	10	15	–	10	15	mA
V_O = 0 V, R_L = ∞	–	2	3	–	2	3	mA
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$*	–	6	–	–	8	–	μV/°C



TOP VIEW

S and T Suffixes



TOP VIEW

E Suffix

CA3160 Series devices have an on-chip frequency-compensation network. Supplementary phase-compensation or frequency roll-off (if desired) can be connected externally between terminals 1 and 8.

Fig. 1 – Functional diagrams of the CA3160 Series.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS		CA3160/ CA3160A (T, S, E)	UNITS
	V^+ = +7.5 V V^- = −7.5 V T_A = 25°C (Unless Otherwise Specified)			
Input Offset Voltage Adjustment Range	10 kΩ across Terms. 4 and 5 or 4 and 1		±22	mV
Input Resistance, R_I			1.5	TΩ
Input Capacitance, C_I	f = 1 MHz		4.3	pF
Equivalent Input Noise Voltage, e_n	BW= 0.2 MHz	R_S=1 MΩ R_S=10MΩ	40 50	μV
Equivalent Input Noise Voltage, e_n	R_S= 100 Ω	1 kHz 10 kHz	72 30	$nV\sqrt{Hz}$
Unity Gain Crossover Frequency, f_T			4	MHz
Slew Rate, SR:			10	V/μs
Transient Response: Rise Time, t_r	C_L - 25 pF R_L = 2 kΩ (Voltage Follower)		0.09	μs
Overshoot			10	%
Settling Time (4 V_{p-p} Input to <0.1%)			1.8	μs

CHARACTERISTIC	TEST CONDITIONS	CA3160A (T, S, E)	CA3160 (T, S, E)	UNITS
	V^+ = 5 V V^- = 0 V T_A = 25°C (Unless Otherwise Specified)			
Input Offset Voltage, V_{IO}		2	6	mV
Input Offset Current, I_{IO}		0.1	0.1	pA
Input Current, I_I		2	2	pA
Common-Mode Rejection Ratio, CMRR		90	80	dB
Large-Signal Voltage Gain, A_{OL}	V_O = 4 V_{p-p} R_L = 5 kΩ	100 k	100 k	V/V
		100	100	dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.8	0 to 2.8	V
Supply Current, I^+	V_O = 5 V, R_L = ∞	300	300	μA
	V_O = 2.5 V, R_L = ∞	500	500	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	μV/V

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) . . . . . 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE . . . . . ±8 V
COMMON-MODE DC
INPUT VOLTAGE . . . (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT . . . . . 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK −
UP TO 55°C . . . . . 630 mW
ABOVE 55°C . . . . Derate linearly 6.67 mW/°C
WITH HEAT SINK −
UP TO 90°C . . . . . 1 W
ABOVE 90°C . . . . Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
OPERATING (All Types) . . . . −55 to +125°C
STORAGE (All Types) . . . . . −65 to +150°C
OUTPUT SHORT-CIRCUIT
DURATION* . . . . . INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH
(1.59 ± 0.79 MM) FROM CASE
FOR 10 SECONDS MAX. . . . . +265°C

*Short circuit may be applied to ground or to either supply.

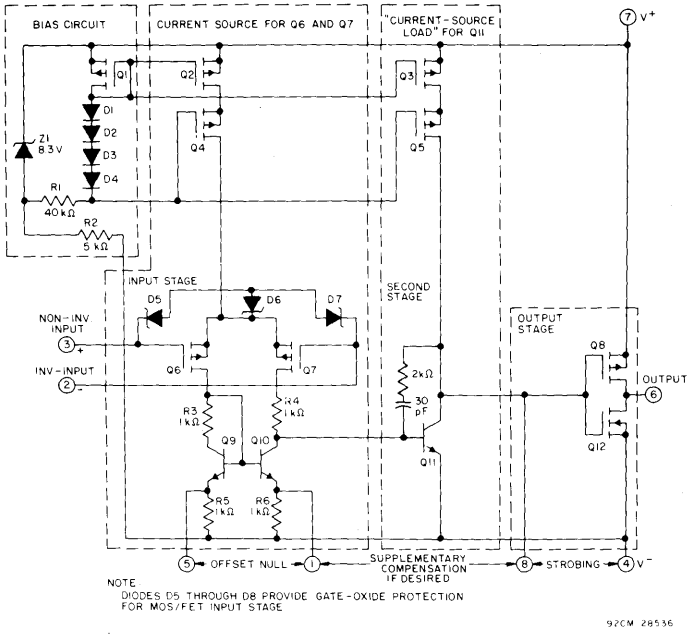


Fig.2 – Schematic diagram of the CA3160 Series.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA3160 series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA3160 series circuits are ideal for single-supply operation. Three class A amplifier stages, having the individual gain capability and current consumption shown in Fig.3, provide the total gain of the CA3160. A biasing circuit provides two potentials for common use in the first and second stages. Terminals 8 and 1 can be used to supplement the internal phase compensation network if additional phase compensation or frequency roll-off is desired. Terminals 8 and 4 can also be used to strobe the output stage into a low quiescent current state. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply-rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

Input Stages – The circuit of the CA3160 is shown in Fig.2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4, are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D7 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

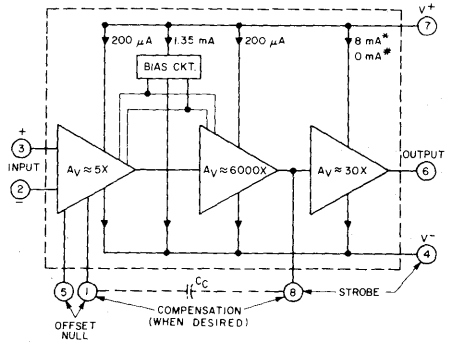
Second-Stage – Most of the voltage gain in the CA3160 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is described later. Miller Effect compensation (roll off) is accomplished by means of the 30-pF capacitor and 2-kΩ resistor connected between the base and collector of transistor Q11. These internal components provide sufficient compensation for unity gain operation in most applications. However, additional compensation, if desired, may be used between Terminals 1 and 8.

Bias-Source Circuit – At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Terminal 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage – The output stage consists of a drain-loaded inverting amplifier using COS/MOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig.6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

† For general information on the characteristics CMOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "CMOS Transistor Array".



TOTAL SUPPLY VOLTAGE (FOR INDICATED VOLTAGE GAINS) = 15 V.
*WITH INPUT TERMINALS BIASED SO THAT TERM 6 POTENTIAL IS +7.5 V ABOVE TERM. 4.
#WITH OUTPUT TERMINAL DRIVEN TO EITHER SUPPLY RAIL.

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Fig. 3 – Block diagram of the CA3160 Series.

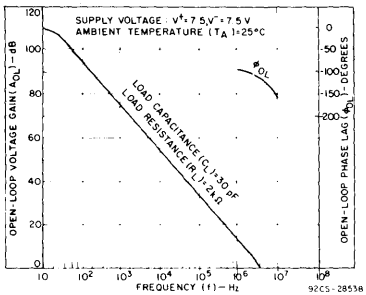


Fig.4 – Open-loop voltage gain and phase shift vs. frequency.

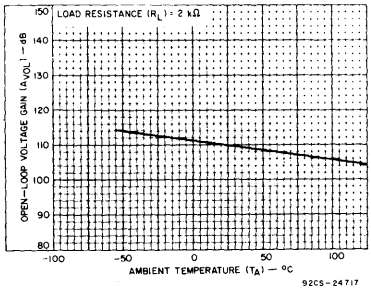


Fig.5 – Open-loop gain vs. temperature.

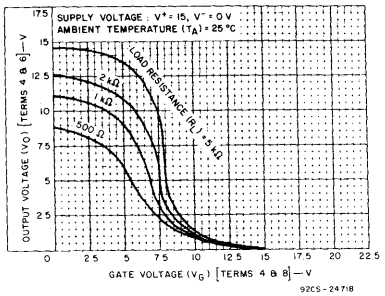


Fig.6 – Voltage transfer characteristics of COS/MOS output stage.

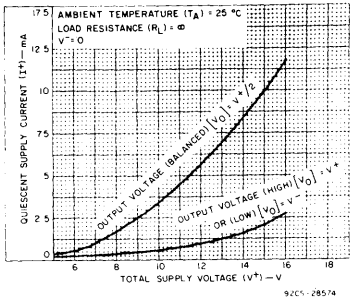


Fig.7 – Quiescent supply current vs. supply voltage.

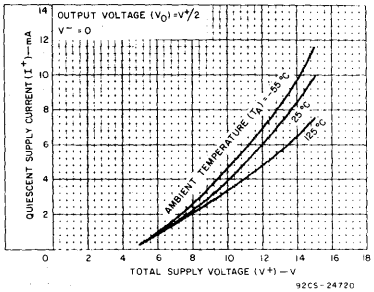


Fig.8 – Quiescent supply current vs. supply voltage at several temperatures.

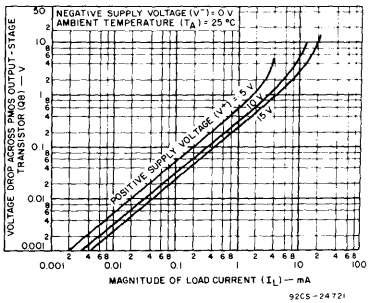


Fig.9 – Voltage across PMOS output transistor (Q8) vs. load current.

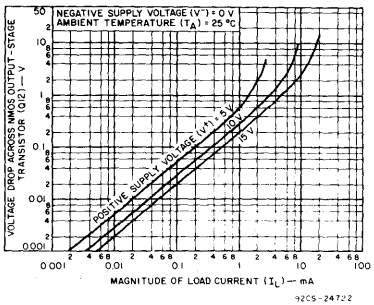


Fig.10 – Voltage across NMOS output transistor (Q12) vs. load current.

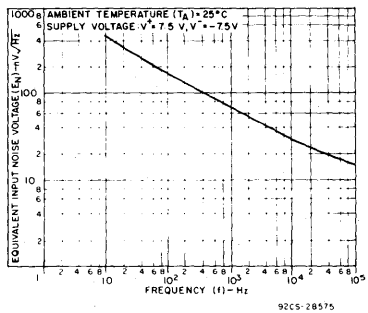


Fig.11 – Equivalent noise voltage vs. frequency.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA3160 Series Op-Amps is typically 5 pA at T_A=25°C when Terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig. 12 contains

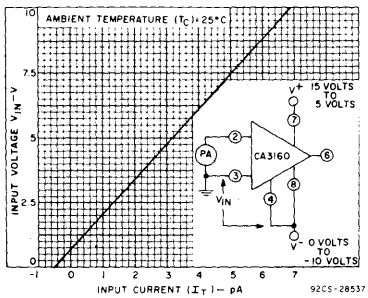


Fig. 12 – Input current vs. common-mode voltage.

data showing the variation of input current as a function of common-mode input voltage at T_A=25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA3160 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Input-Current Variation with Temperature

The input current of the CA3160 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig. 13 provides data on the typical variation of input bias current as a function of temperature in the CA3160.

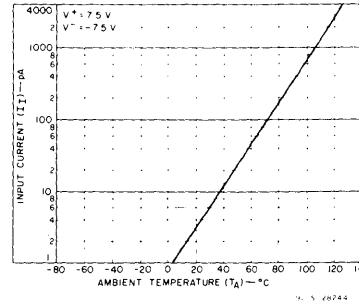


Fig. 13 – Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA3160. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA3160 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terminals 2 and 3. Fig. 14 shows typical data pertinent to shifts in offset voltage encountered with CA3160 devices in TO-5 packages during life testing. At lower temperatures (TO-5 and plastic) for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those en-

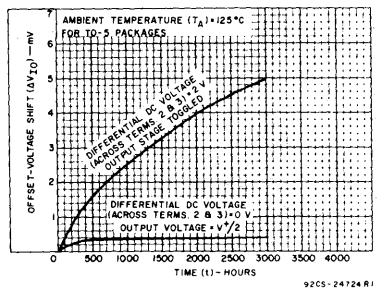
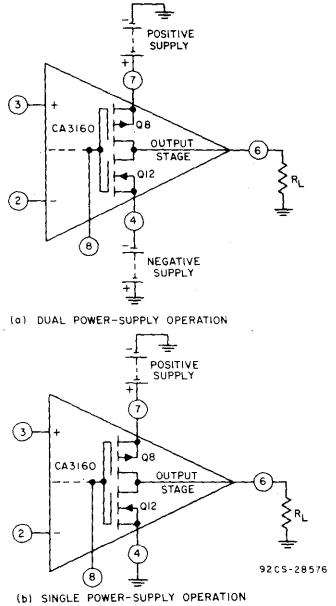


Fig. 14 – Typical incremental offset-voltage shift vs. operating life.

countered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output state is "toggled", e.g., as in comparator applications.

Power-Supply Considerations

Because the CA3160 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 15(a) and 15(b) show the CA3160 connected for both dual- and single-supply operation.



(a) DUAL POWER-SUPPLY OPERATION

(b) SINGLE POWER-SUPPLY OPERATION

Fig. 15 – CA3160 output stage in dual and single power-supply operation.

Dual-supply operation: When the output voltage at Terminal 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA3160 operated under these conditions.

Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA3160, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 15(a) shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L=\infty$, by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Terminal 6 and ground in the circuit of Fig. 15(b). Let it further be assumed again that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is a $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA3160 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 40 μV when the test-circuit amplifier of Fig. 16 is operated at a total supply voltage of 15 volts. This value of

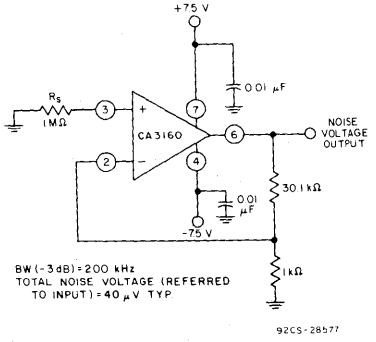
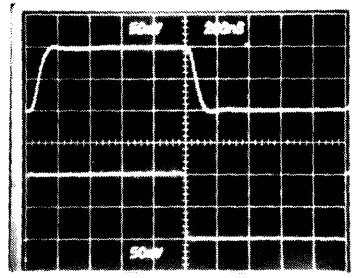
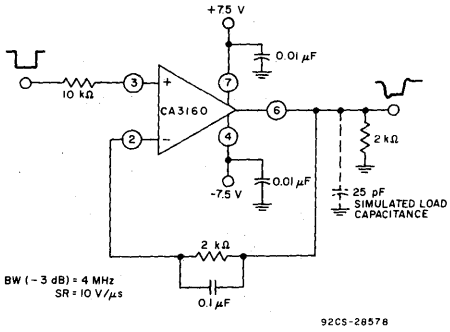


Fig. 16 – Test-circuit amplifier (30-dB gain) used for wideband noise measurements.

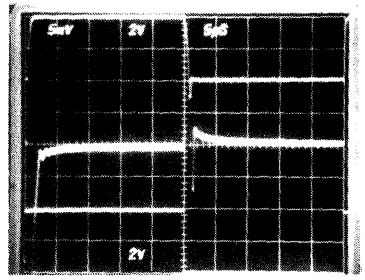
total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.



(b) Small Signal Response
Top Trace: Output
Bottom Trace: Input



(a)



(c) Input-Output Difference Signal Showing Settling Time
Top Trace: Output Signal
Center Trace: Difference Signal 5 mV/div
Bottom Trace: Input Signal

Fig.17 – Split-supply voltage follower with associated waveforms.

TYPICAL APPLICATIONS

Voltage Followers

Operational amplifiers with very high input resistances, like the CA3160, are particularly suited to service as voltage followers. Fig.17 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA3160 in a split-supply configuration.

A voltage follower, operated from a single-supply, is shown in Fig.18 together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig.18b with input-signal ramping. The waveforms in Fig.18c show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig.18c also shows the manner in which the COS/MOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA3160 in a single-supply voltage-follower application.

9-Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig.19. This system combines the concepts of multiple-switch CMOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA3160 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 19.

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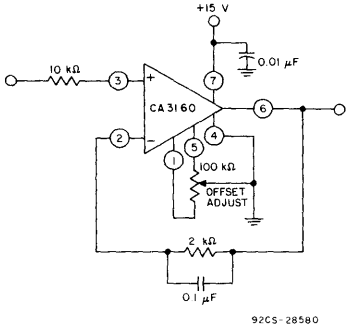
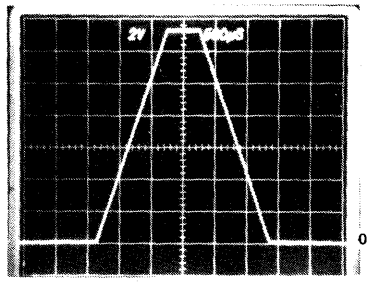
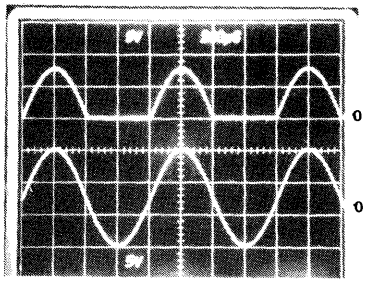
* "Digital-to-Analog Conversion Using the RCA-CD4007A COS/MOS IC", Application Note ICAN-6080.



(a)



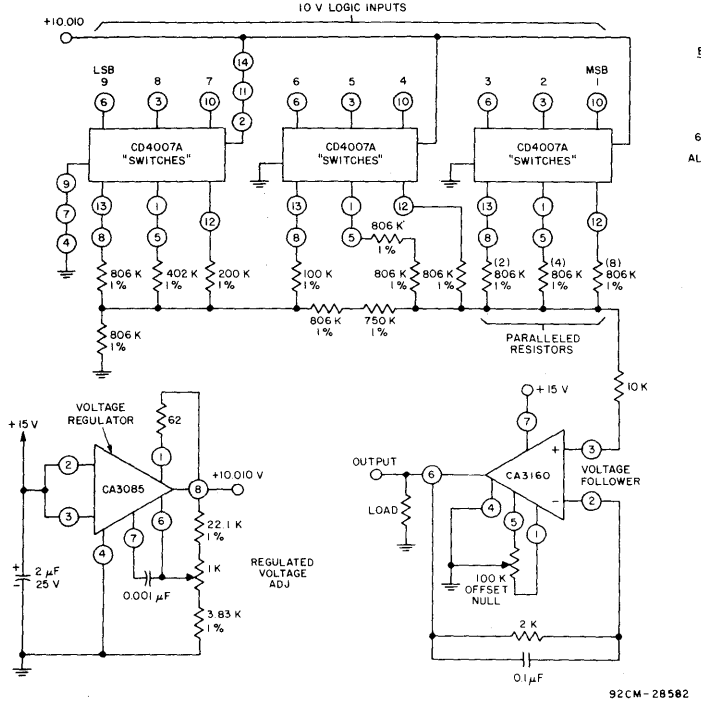
(b) Output signal with input-signal ramping.



92CS-28581R1

(c) Output-Waveform with Ground-Reference
Sine-Wave Input
Top Trace: Output
Bottom Trace: Input

Fig.18 – Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig.9 in ICAN-6080.)



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS.

ALL RESISTANCES IN OHMS

Fig.19 – 9-bit DAC using CMOS digital switches and CA3160.

The circuit uses an R/2R voltage-ladder network, with the output-potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA3160 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the COS/MOS building blocks simplifies the design of DAC systems tailored to particular needs.

Error-Amplifier in Regulated Power Supplies

The CA3160 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero.

The circuit shown in Fig.20 uses a CA3160 as an error amplifier in a continuously adjustable 1-ampere power supply. One of the key features of this circuit is its ability to regulate down to the vicinity of zero volts with only one dc power supply input.

An RC network, connected between the base of the output drive transistor and the input voltage, prevents "turn-on overshoot", a condition typical of many operational-amplifier regulator circuits. As the amplifier becomes operational, this RC network ceases to have any influence on the regulator performance.

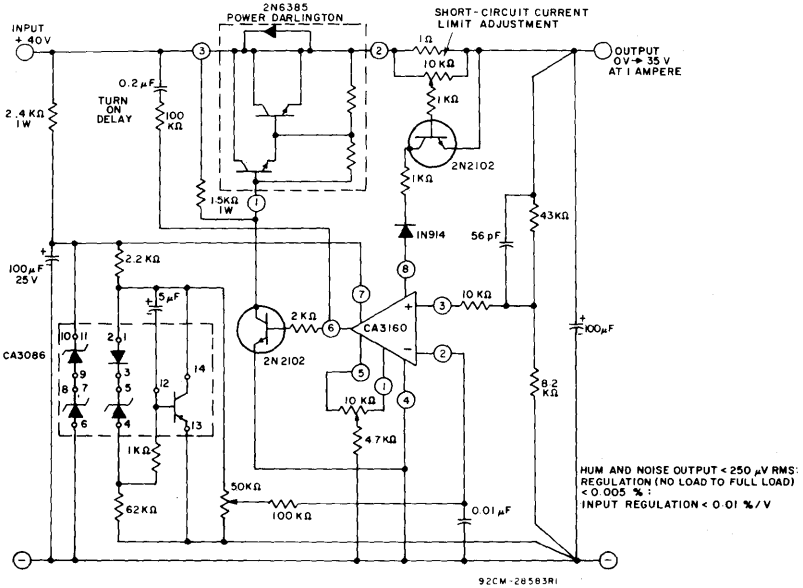


Fig.20 – Voltage regulator circuit (0.1 to 35 V at 1 A).

Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Fig.21. The oscillator operates with a tracking error in the order of 0.02 percent and a temperature coefficient of 0.01%/°C. A multivibrator (A_1) generates pulses of constant amplitude (V) and width (T_2). Since the output (terminal 6) of A_1 (a CA3130) can swing within about 10 millivolts of either supply-rail, the output pulse amplitude (V) is essentially equal to V+. The average output voltage ($E_{avg} = V\ T_2/T_1$) is applied to the non-inverting input terminal of comparator A_2 via an integrating network R_3, C_2. Comparator A_2 operates to establish circuit conditions such that $E_{avg} = V1$. This circuit condition is accomplished by feeding an output signal from terminal 6 of A_2 through R_4, D_4 to the inverting terminal (terminal 2) of A_1, thereby adjusting the multivibrator interval, T_3.

Voltmeter With High Input Resistance

The voltmeter circuit shown in Fig.22 illustrates an application in which a number of the CA3160 characteristics are exploited. Range-switch SW1 is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to Terminal 2 via 10 KΩ current-limiting resistor. The circuit is powered by a single 8.4-volt mercury battery. With zero input signal, the circuit consumes somewhat less than 500 microamperes plus the meter current required to indicate a given voltage. Thus, at full-scale input, the total supply current rises to slightly more than 1500 microamperes.

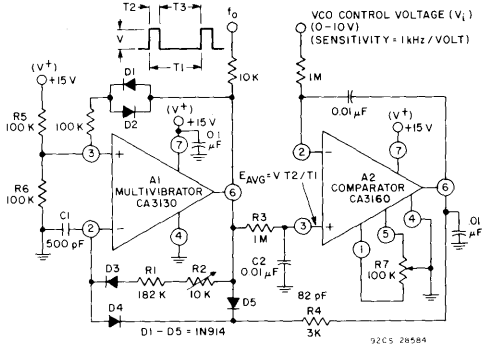


Fig.21 – Voltage-controlled oscillator.

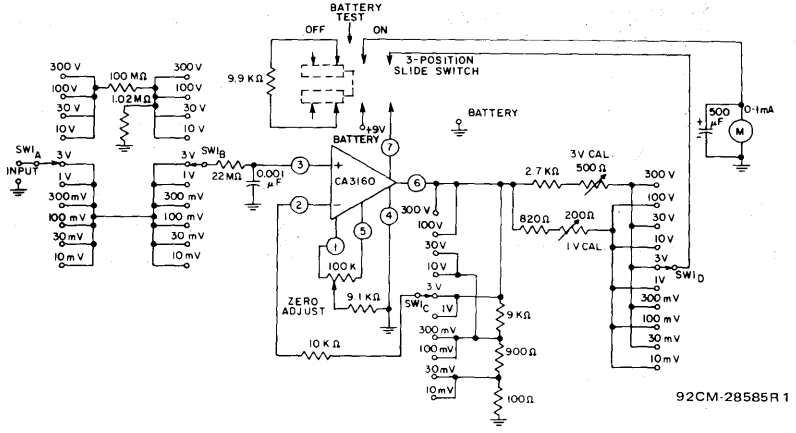


Fig.22 – High-input-resistance DC voltmeter.

Function Generator

A function generator having a wide tuning range is shown in Fig.23. The adjustment range, in excess of 1,000,000/1, is accomplished by a single potentiometer. Three operational amplifiers are utilized: a CA3160 as a voltage follower, a CA3080 as a high-speed comparator, and a second CA3080A as a programmable current source. Three variable capacitors C1, C2, and C3 shape the triangular signal between 500 kHz and 1 MHz. Capacitors C4, C5, and the trimmer potentiometer in series with C5 maintain essentially constant (±10%) amplitude up to 1 MHz.

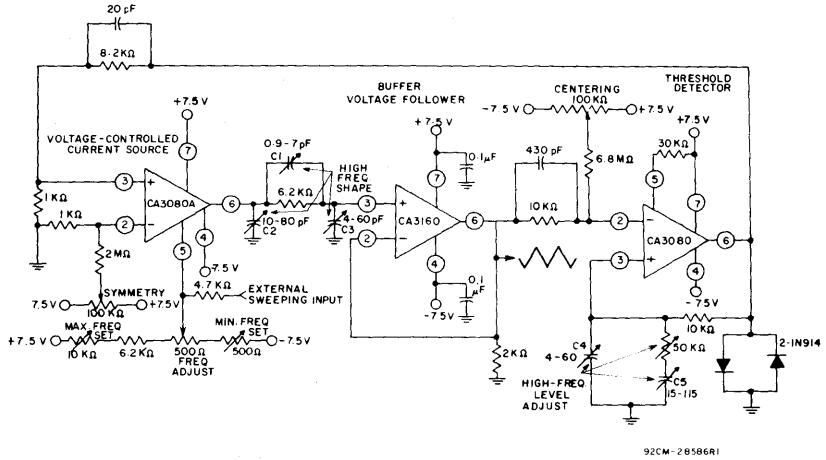
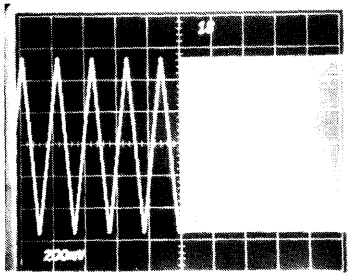
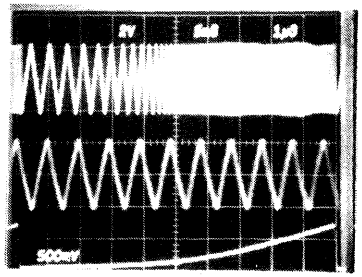


Fig.23(a) – 1,000,000/1 single-control function generator – 1 MHz to 1 Hz.



(b) – Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.

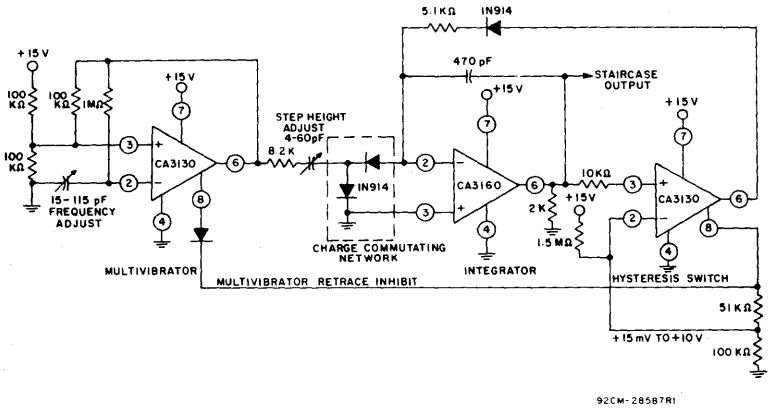


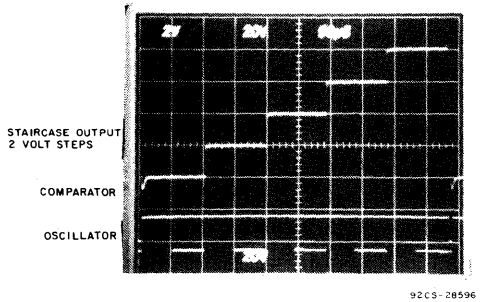
92CS-28588

(c) – Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

Staircase Generator

Fig. 24 shows a staircase generator circuit utilizing three CMOS operational amplifiers. Two CA3130's are used; one as a multivibrator, the other as a hysteresis switch. The third amplifier, a CA3160, is used as a linear staircase generator.





(b) – Staircase Generator Waveform
Top Trace: Staircase Output
2 Volt Steps
Center Trace: Comparator
Bottom Trace: Oscillator

Picoammeter Circuit

Fig. 25 is a current-to-voltage converter configuration utilizing a CA3160 and CA3140 to provide a picoampere meter for ±3 pA full-scale meter deflection. By placing Terminals 2 and 4 of the CA3160 at ground potential, the CA3160 input is operated in the "guarded mode". Under this operating condition, even slight leakage resistance present between Terminals 3 and 2 or between Terminals 3 and 4 would result in zero voltage across this leakage resistance, thus substantially reducing the leakage current.

If the CA3160 is operated with the same voltage on input Terminals 3 and 2 as on Terminal 4, a further reduction in the input current to the less than one picoampere level can be achieved as shown in Fig. 12.

To further enhance the stability of this circuit, the CA3160 can be operated with its output (Terminal 6) near ground, thus markedly reducing the dissipation by reducing the supply current to the device.

The CA3140 stage serves as a X100 gain stage to provide the required plus and minus output swing for the meter and feedback network. A 100-to-1 voltage divider network consisting of a 9.9-KΩ resistor in series with a 100-ohm resistor sets the voltage at the 10-KMΩ resistor (in series with Terminal 3) to ±30 mV full-scale deflection. This 30-mV signal results from ±3 volts appearing at the top of the voltage divider network which also drives the meter circuitry.

By utilizing a switching technique in the meter circuit and in the 9.9 KΩ and 100-ohm network similar to that used in voltmeter circuit shown in Fig. 22, a current range of 3 pA to 1 nA full scale can be handled with the single 10-KMΩ resistor.

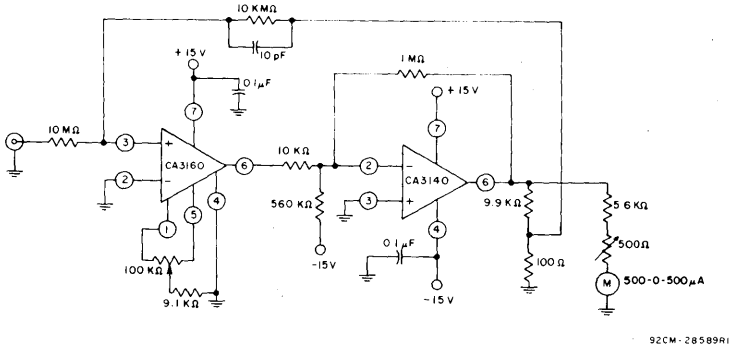


Fig.25 – Current-to-voltage converter to provide a picoammeter with ± 3 pA full-scale deflection.

Single-Supply Sample-and-Hold System

Fig. 26 shows a single-supply sample-and-hold system using a CA3160 to provide a high input impedance and an input-voltage range of 0 to 10 volts. The output from the input buffer integrator network is coupled to a CA3080A. The CA3080A functions as a strobeable current source for the CA3140 output integrator and storage capacitor. The CA3140 was chosen because of its low output impedance and constant gain-bandwidth product. Pulse "droop" during the hold interval can be reduced to zero by adjusting the 100-KΩ bias-voltage potentiometer on the positive input of the CA3140. This zero adjustment sets the CA3080A output voltage at its zero current position. In this sample-and-hold circuit it is essential that the amplifier bias current be reduced to zero to minimize output signal current during the hold mode. Even with 320 mV at the amplifier bias circuit terminal (5) at least ± 100 pA of output current will be available.

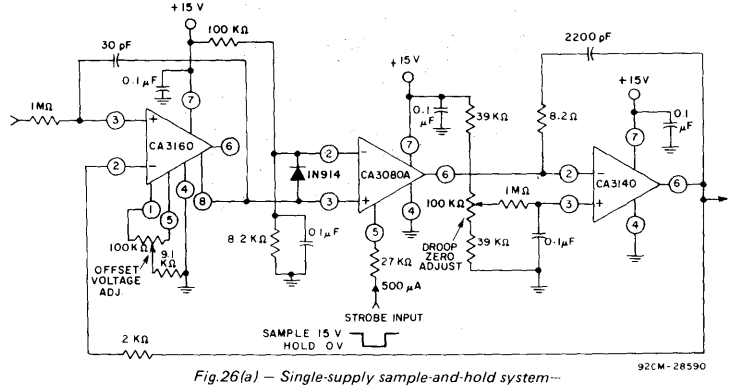
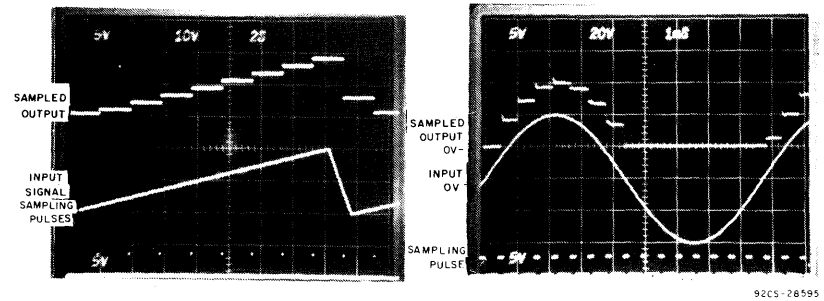


Fig.26(a) – Single-supply sample-and-hold system– input 0-to-10 volts.



(b) – Sample-and-hold waveform.
Top Trace: Sampled Output
Center Trace: Input Signal
Bottom Trace: Sampling Pulses

(c) – Sample-and-hold waveform.
Top Trace: Sampled Output
Center Trace: Input
Bottom Trace: Sampling Pulse

Wien Bridge Oscillator

A simple, single-supply Wien Bridge oscillator using a CA3160 is shown in Fig. 27. A pair of parallel-connected 1N914 diodes comprise the gain-setting network which standardizes the output voltage at approximately 1.1 volts. The 500-ohm potentiometer is adjusted so that the oscillator will always start and the oscillation will be maintained. Increasing the amplitude of the voltage may lower the threshold level for starting and for sustaining the oscillation, but will introduce more distortion.

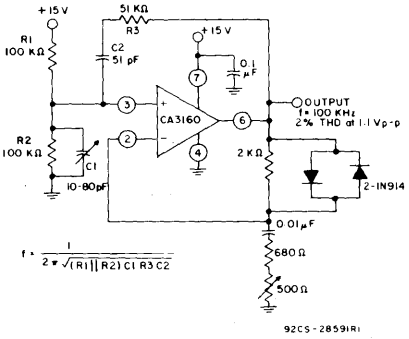


Fig.27 – Single-supply Wien Bridge oscillator.

Operation with Output-Stage Power-Booster

The current sourcing and sinking capability of the CA3160 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 28, three CMOS transistor-pairs in a single CA3600 IC array are shown parallel-connected with the output stage in the CA3160. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA3160 output stage by about 2.5X.

The amplifier circuit in Fig. 28 employs feedback to establish a closed-loop gain of 20 dB. The typical large-signal-bandwidth (−3 dB) is 190 kHz.

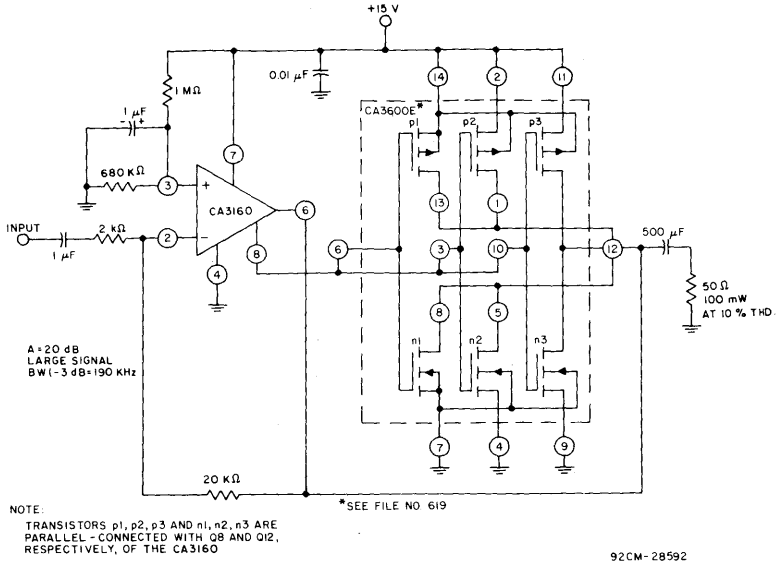


Fig.28 – CMOS transistor array (CA3600E) connected as power booster in the output stage of the CA3160.

Operational Amplifiers

CA3193A, CA3193

May 1990

BiMOS Precision Operational Amplifiers

Features:

- *Low V_{IO}: 200 μV max. (CA3193A)*
  500 μV max. (CA3193A)
- *Low $\Delta V_{IO}/\Delta T$: 3 μV/°C max. (CA3193A)*
  5 μV/°C max. (CA3193)
- *Low I_{IO} and I_I*
- *Low $\Delta I_{IO}/\Delta T$: 150 pA/°C max. (CA3193)*
- *Low $\Delta I_I/\Delta T$: 3.7 nA/°C max. (CA3193)*

Applications:

- *Thermocouple preamplifiers*
- *Strain-gauge bridge amplifiers*
- *Summing amplifiers*
- *Differential amplifiers*
- *Bilateral current sources*
- *Log amplifiers*
- *Differential voltmeters*
- *Precision voltage references*
- *Active filters*
- *Buffers*
- *Integrators*
- *Sample-and-hold circuits*
- *Low frequency filters*

The CA3193A and CA3193 are ultra-stable, precision instrumentation, operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The CA3193A and CA3193 amplifiers are internally phase compensated and provide a gain bandwidth product of 1.2 MHz. They are pin compatible with the industry 741 series and many other IC op amps, and may be used as replacements for 741 series types in most applications.

The CA3193A and CA3193 can also be used as functional replacements for op-amp types 725, 108A, OP-5, OP-7, LM11 and LM714 in many applications where nulling is not employed. Because of their low offset voltage and low offset voltage-versus-temperature coefficient the CA3193A and CA3193 amplifiers have a wider range of applications than most op amps and are particularly well suited ofr use as thermocouple amplifiers, high gain filters, buffer, strain gauge bridge amplifiers and precision voltage references.

The three types in the CA3193 series are functionally identical. The CA3193 and CA3193A operate from supply voltage of ±3.5 V to ±18 V and have operating temperature ranges of -25°C to +85°C and 0°C to +70°C, respectively.

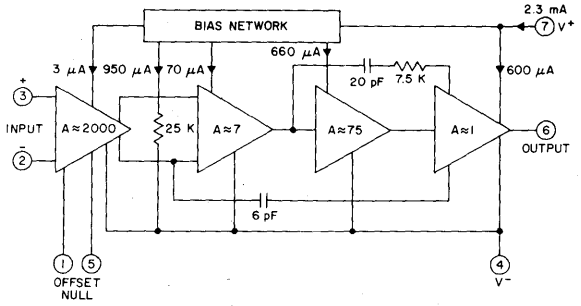


Figure 1 - Block diagram of CA3193A and CA3193.

File Number **1249**

Absolute-Maximum Ratings, *Absolute-Maximum Values at T_A =25° C*

	CA3193	CA3193A
DC Supply Voltage	± 18	± 18
Differential-Mode Input Voltage	± 5	± 5
Common-Mode DC Input Voltage	(V^+ -4), V^-	(V^+ -4), V^-
Input Terminal Current	1	1
Device Dissipation		
Without Heat Sink		
Up to 55° C	630	630
Above 55° C	Derate Linearly 6.67	
Temperature Range	0 to 70	-25 to 85
Output Short-Circuit Duration*	Indefinite	Indefinite
Lead Temperature (During Soldering) at distance of 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	±265	±265

* Short circuit may be applied to ground or to either supply.

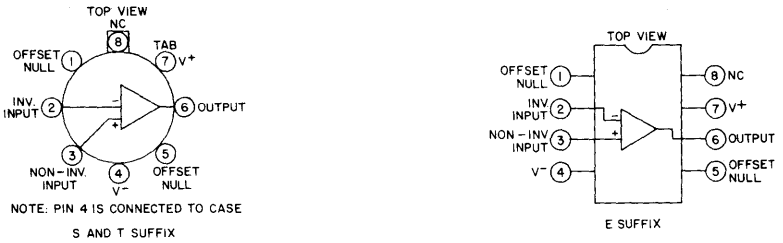


Fig. 2 - Functional diagram of CA3193A and CA3193.

The CA3193A and CA3193 types are supplied in standard 8-lead TO-5 style (T suffix), 8-lead dual-in-line formed lead TO-5-style (DIL-CAN-S suffix) and 8-lead dual-in-line plastic (Mini-DIP-E suffix) packages.

Circuit Description

The block diagram of the CA3193 amplifier, Fig. 1 shows the voltage gain and supply current for each of its four amplifier stages. Simplified and complete schematic diagrams of the CA3193 amplifier are shown in Figs. 3 and 4, respectively.

A quad of physically cross-connected n-p-n transistors comprise the input-stage differential pair (Q1, Q2 in Figs. 3 and 4); this arrangement contributes to the low input offset-voltage characteristics of the amplifier. The ultra-high gain provided in the first stage ensures that subsequent stages cannot significantly influence the overall offset-voltage characteristics of the amplifier. High load impedances for the input-stage differential pair (Q1, Q2) are provided by the cascode-connected p-n-p transistors Q3, Q5 and Q4, Q6, thereby contributing to the high gain developed in the stage.

The second stage of the amplifier consists of a differential amplifier employing PMOS/FETs (Q7, Q8 in Figs. 3 and 4) with appropriate drain loading. Since Q7 and Q8 are MOS/FETs, their loading on the first stage is quite low, thereby making an additional contribution to the high gain developed in the first stage. The second stage is also configured to convert its differential signal to a single-ended output signal by means of current mirror D9, Q30 (Figs. 3 and 4) to drive subsequent gain stage.

The third stage of the amplifier consists of Darlington-connected n-p-n transistors (Q17, Q19 in Figs. 3 and 4), driving the quasi-complementary Class AB output stage (Q14 and Q15, Q16 in Figs. 3 and 4). Output-stage short-circuit protection is activated by voltage drops developed across the 60-ohm resistors adjacent to the output terminal (R9 and R10, Fig. 4). When the voltage drop developed across either of these resistors reaches a potential equal to 1 V_{BE}, the respective protective transistor (Q12 or Q13) is activated and shunts the base drive from the bases of the output stage transistors (Q14 and Q15, Q16).

Internal frequency compensation for the CA3193 amplifier is provided by two internal networks, a 6-pF capacitor connected between the input-stage transistor collectors and the node between the third and output stages and a second network, consisting of a 20-pF capacitor in series with a 7.5 kΩ resistor connected between the input and output nodes of the third stage.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 15$ V and $V^- = 15$ V unless otherwise specified.

CHARACTERISTIC	LIMITS						UNITS
	CA3193A			CA3193			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	140	200	—	300	500	μV
V_{IO} @ Max.Temp.	—	—	380	—	—	725	μV
Input Offset Voltage Temp.Coefficient, $\Delta V_{IO}/\Delta T$ (Over specified temperature range for each device)	—	1	3	—	1	5	μV/°C
Input Offset Current, I_{IO}	—	3	5	—	5	10	nA
$\|I_{IO}\|$ @ Max.Temp.	—	—	11	—	—	17	nA
Input Offset Current Temp. Coefficient, $\Delta I_{IO}/\Delta T$ (Over specified temperature range for each device)	—	0.03	0.10	—	0.04	0.15	nA/°C
Input Bias Current, I_I	—	10	20	—	20	40	nA
$\|I_B\|$ @ Max.Temp.	—	—	83	—	—	207	nA
Input Bias Current Temp. Coefficient, $\Delta I_I/\Delta T$	—	0.10	1.18	—	0.15	3.70	nA/°C
Input Noise Voltage, e_n p-p (0.1 to 10 Hz)	—	0.36	—	—	0.36	—	μV p-p
Input Noise Voltage Density, e_n							
$f_O = 10$ Hz	—	25	—	—	25	—	
$f_O = 100$ Hz	—	25	—	—	25	—	
$f_O = 1000$ Hz	—	24	—	—	24	—	nV/
$f_O = 10$ kHz	—	24	—	—	24	—	$\sqrt{Hz}$
$f_O = 100$ kHz	—	22	—	—	22	—	
Input Noise Current, i_n p-p (0.1 to 10 Hz)	—	12	20	—	12	20	pA p-p
Input Noise Current Density, i_n							
$f_O = 10$ Hz	—	0.83	—	—	0.83	—	
$f_O = 100$ Hz	—	0.80	—	—	0.80	—	
$f_O = 1000$ Hz	—	0.75	—	—	0.75	—	pA/
$f_O = 10$ kHz	—	0.72	—	—	0.72	—	$\sqrt{Hz}$
$f_O = 100$ kHz	—	0.60	—	—	0.60	—	

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 15$ V and $V^- = 15$ V (Cont'd) unless otherwise specified.

CHARACTERISTIC	LIMITS						UNITS
	CA3193A			CA3193			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Common-Mode Input Voltage Range, V_{ICR}	−12	−13.5 to 11.5	10	−12	−13.5 to 11.5	10	V
Common-Mode Rejection Ratio, ($V_{CM} = V_{ICR}$)	110	115	—	100	110	—	dB
		1.78	3.16		3.16	10	μV/V
Power Supply Rejection Ratio, PSRR, $\Delta V_{IO}/\Delta V \pm$	100	130	—	100	130	—	dB
		0.316	10		0.316	10	μV/V
Maximum Output Voltage Swing ($R_L \geq 2$ KΩ)	±13.0	±13.5	—	±13.0	±13.5	—	V
Large-Signal Voltage Gain ($V_O = \pm 10$)							
$R_L \geq 1$ KΩ	—	—	—	—	—	—	
$R_L \geq 2$ KΩ	110	115	—	100	110	—	dB
$R_L \geq 10$ KΩ	—	125	—	—	115	—	
Short-Circuit Output Current to the Opposite Rail, I_{OM}^+, I_{OM}^-	−25	±7	25	−25	±7	25	mA
Slew Rate, SR ($R_L \geq 2$ KΩ; Unity Gain Voltage Follower)	—	0.25	—	—	0.25	—	V/μs
Gain-Bandwidth Product, f_t $A_{OL} = 0$ dB $R_L = 2$ kΩ $C_L = 100$ pF $V_{IN} = 20$ $f = 1$ kHz	—	1.20	—	—	1.20	—	MHz
Small-Signal Transient Response, t_r ($V_{IN} =$ 20 mV p-p, f = 1 kHz	—	0.29	—	—	0.29	—	μs
Supply Current, $R_L = \infty$ $V^+ = 15$, $V^- = -15$	—	2.3	3.5	—	2.3	3.5	mA
Temperature Range	−25	—	85	0	—	70	°C

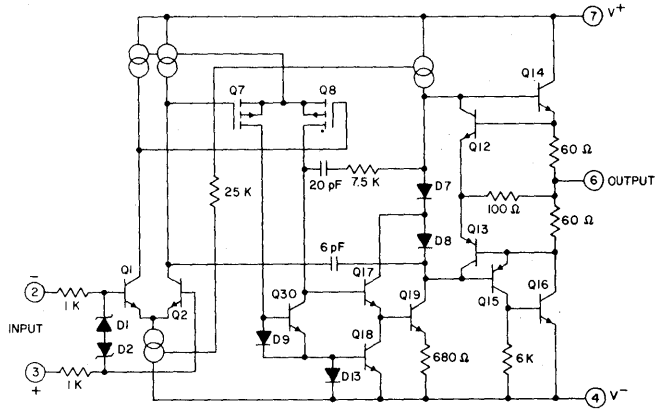


Fig. 3 - CA3193 simplified schematic diagram.

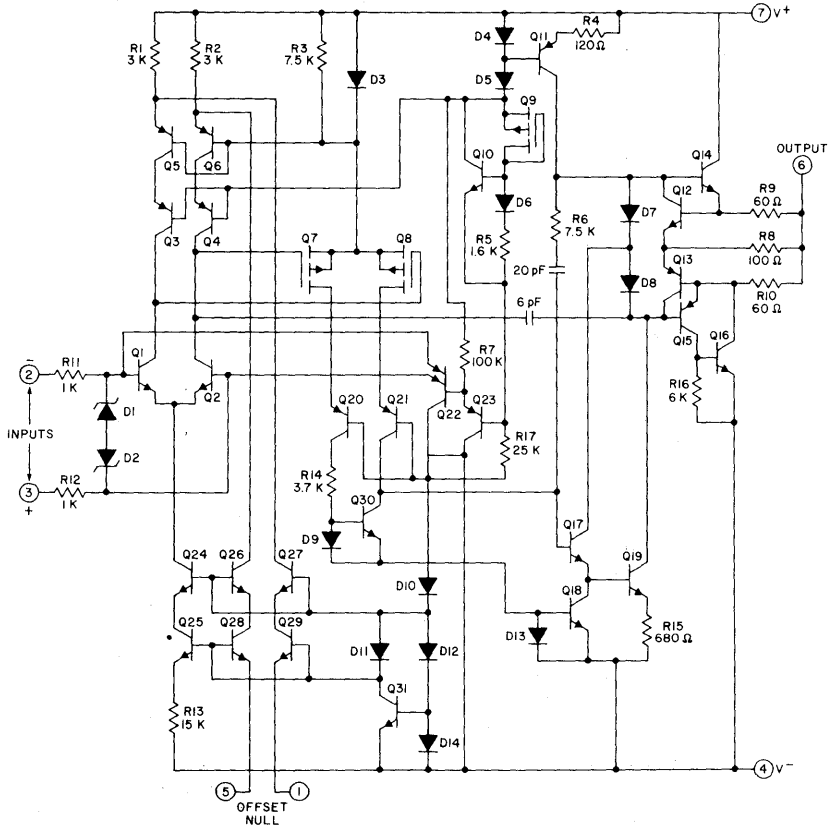


Fig. 4 - Schematic diagram of CA3193A and CA3193.

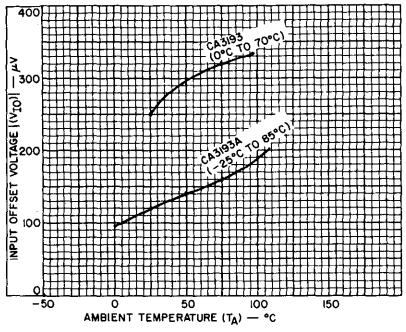


Fig. 5 - Typical input offset-voltage temperature characteristic for CA3193 series.

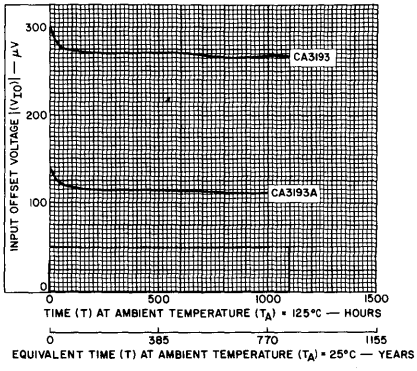


Fig. 6 - Input offset voltage vs. time.

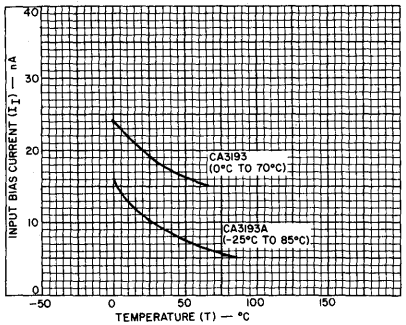


Fig. 7 - Typical input bias current vs. temperature.

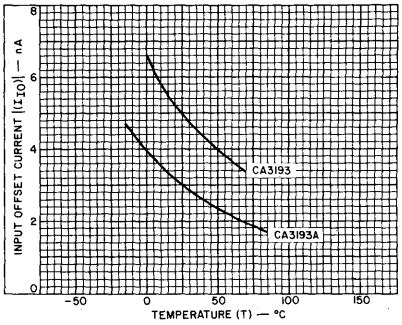


Fig. 8 - Typical input offset current vs. temperature.

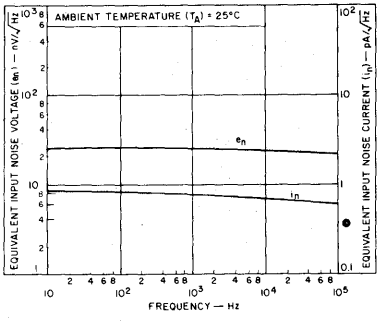


Fig. 9 - Input noise voltage and current density vs. frequency.

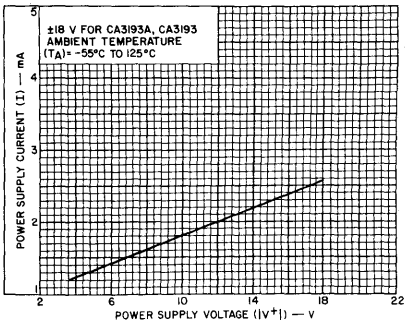


Fig. 10 - Power supply voltage (V^+, V^-) vs. supply current.

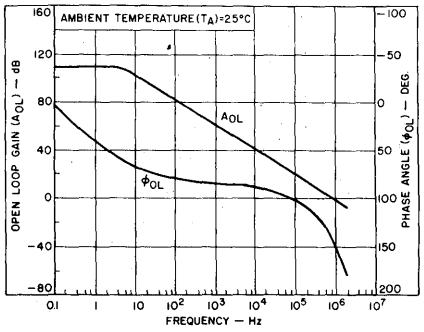


Fig. 11 - Open-loop gain and phase-shift response for CA3193B.

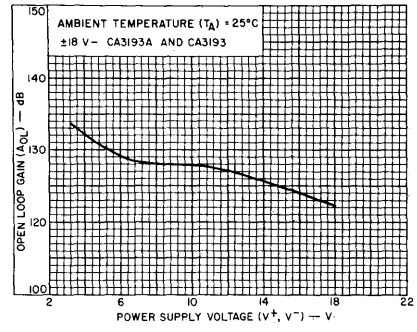
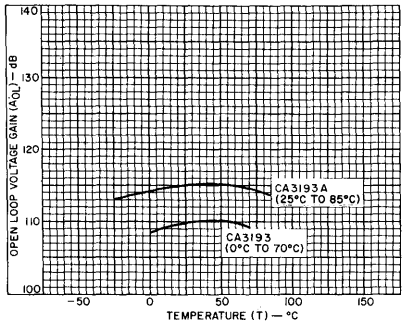


Fig. 12 - Open-loop gain vs. power-supply voltage.



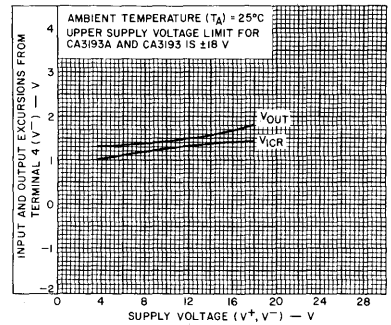


Fig. 13 - Open-loop gain vs. temperature for CA3193 series.

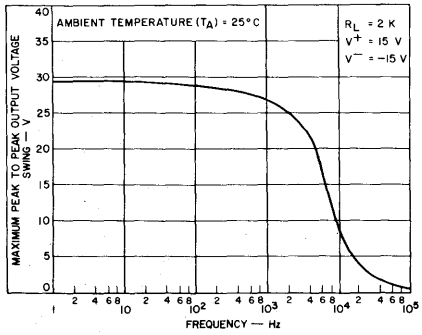


Fig. 14 - Maximum undistorted output voltage vs. frequency.

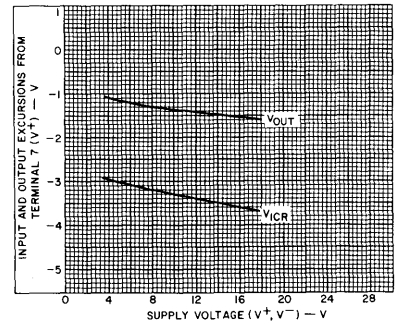


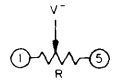
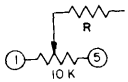
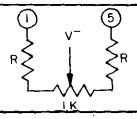
Fig. 15 - Output-voltage-swing capability and common-mode input-voltage vs. supply voltage.

Offset Voltage Nulling

The input offset voltage can be nulled to zero by any of the three methods shown in the table below. A 10K potentiometer between terminals 1 and 5, with its wiper returned to V⁻, will provide a gross nulling for all types. For finer nulling, either of the other two circuits shown below may be used, thus providing simpler improved resolution for all types.

CAUTION: The CA3193 amplifiers will be damaged if they are plugged into op-amp circuits employing nulling with respect to the V⁺ supply bus.

Offset Voltage Nulling

Offset Nulling Circuits			
Type	**Resistor R Value**	**Resistor R Value**	**Resistor R Value**
CA3193A CA3193	10K 10K	50K 20K	10K 5K
	Gross Offset Adjustment	Finer Offset Adjustments	

TEST CIRCUITS

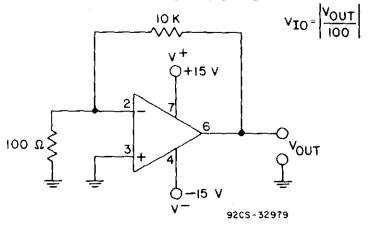
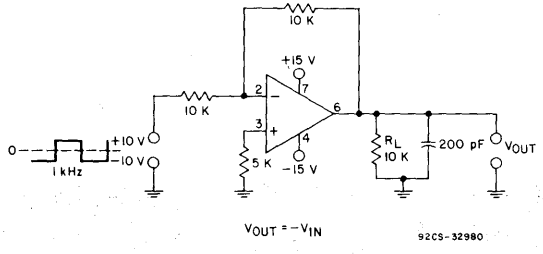
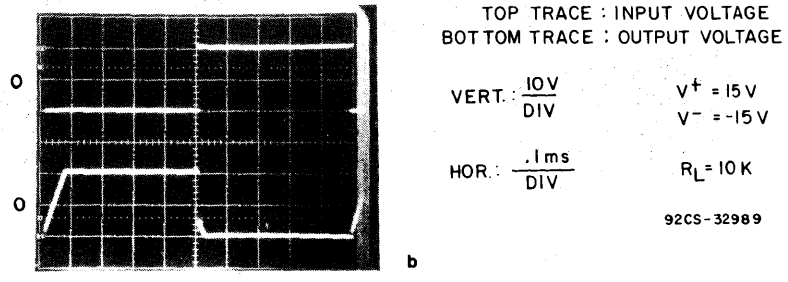


Fig. 16 - Input offset voltage test circuit.

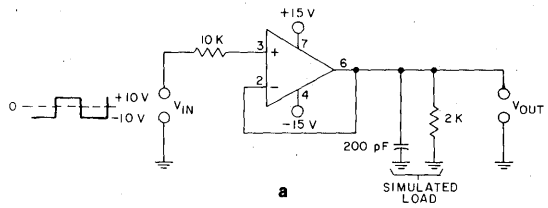


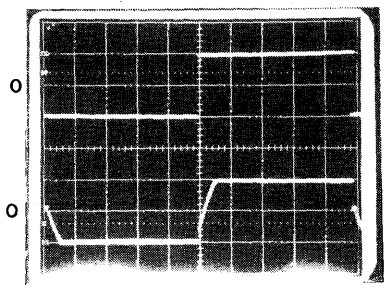
a



b

Fig. 17 - Inverting amplifier (a) test circuit (b) response to 1-kHz, 20-V p-p square wave.





TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT: $\frac{10\ V}{DIV}$

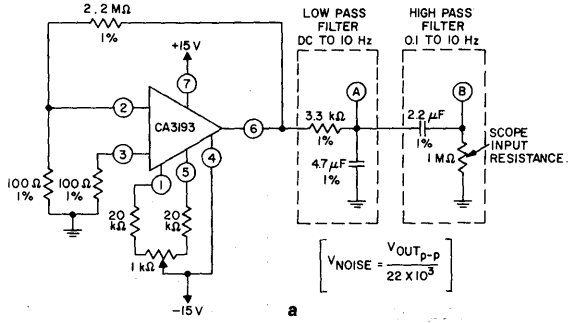
HOR : $\frac{.1\ ms}{DIV}$

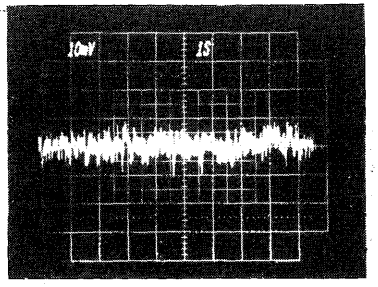
$V+ = 15\ V$

$V^- = 15\ V$

$R_L = 2K$

Fig. 18 - Voltage follower (a) test circuit (b) response to 20-V p-p, 1-kHz square-wave input.





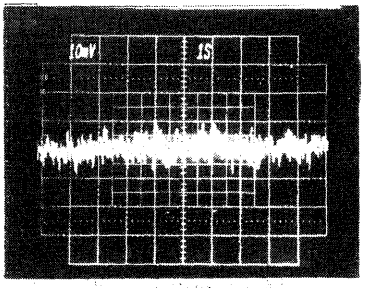
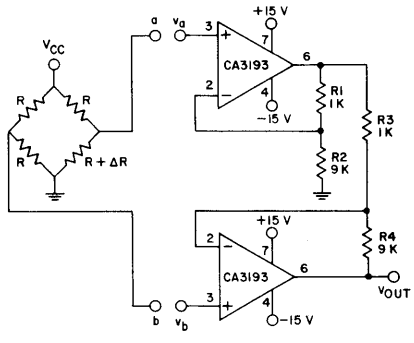


Fig. 19 - Low frequency noise (a) test circuit - 0.1 to 10 Hz (b) output A waveform - 0 to 10 Hz noise (c) output B waveform - 0 to 10 Hz noise.

APPLICATION CIRCUITS



$$V_{OUT} = -v_a\left(\frac{R2}{R1}+1\right)\frac{R4}{R3} + v_b\left(\frac{R4}{R3}+1\right)$$

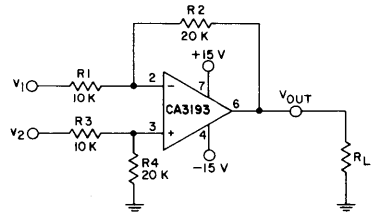
FOR IDEAL RESISTORS WITH $\frac{R1}{R2} = \frac{R3}{R4}$

$$V_{OUT} = v_b - v_a\left(\frac{R4}{R3}+1\right)$$

$$A = \frac{V_{OUT}}{v_b - v_a} = \left(\frac{R4}{R3}+1\right)$$

FOR VALUES ABOVE $V_{OUT} = (v_b - v_a)(10)$

Fig. 20 - Typical two-op amp bridge-type differential amplifier.



ALL RESISTANCE VALUES ARE IN OHMS

$$V_{OUT} = v_2\left(\frac{R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right) - v_1\left(\frac{R2}{R1}\right)$$

IF R4 = R2, R3 = R1 AND $\frac{R2}{R1} = \frac{R4}{R3}$

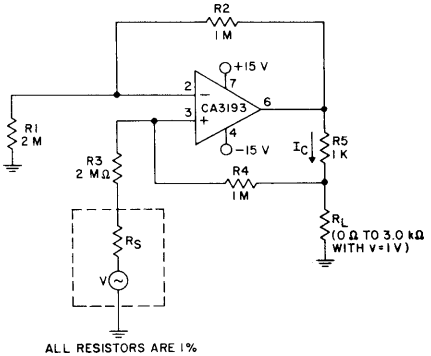
THEN $V_{OUT} = (v_2 - v_1)\left(\frac{R2}{R1}\right)$

FOR VALUES ABOVE $V_{OUT} = 2(v_2 - v_1)$

IF A_V IS TO BE MADE 1 AND IF R1 = R3 = R4 = R
WITH R2 = 0.999 R (0.1% MISMATCH IN R2)

THEN $V_{OCM} = 0.0005\ V_{IN}$ OR CMRR = 66 dB
THUS, THE CMRR OF THIS CIRCUIT IS LIMITED BY
THE MATCHING OR MISMATCHING OF THIS NETWORK
RATHER THAN THE AMPLIFIER.

Fig. 21 - Differential amplifier (simple subtractor) using CA3193.



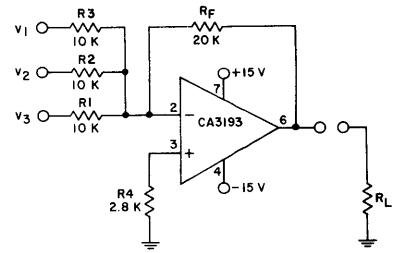
ALL RESISTORS ARE 1%

IF R1 = R3 AND R2 ≈ R4 + R5 THEN

I_L IS INDEPENDENT OF VARIATIONS IN R_L
FOR R_L VALUES OF 0 Ω TO 3 kΩ WITH v = 1 V

$$I_L = \frac{v}{R3}\frac{R4}{R5} = \frac{v}{(2\,M)(1K)} = \frac{v}{2K} = 500\ \mu A$$

Fig. 22 - Using CA3193 as a bilateral current source.



$$V_{OUT} = -\left(\frac{R_F}{R1}v_1 + \frac{R_F}{R2}v_2 + \frac{R_F}{R3}v_3\right)$$

$$V_{OUT} = -(2v_1 + 2v_2 + 2v_3)$$

ALL RESISTANCE VALUES ARE IN OHMS

Fig. 23 - Typical summing amplifier application.

The CA3193 is an excellent choice for use with thermocouples. In Fig. 24, the CA3193 amplifies the signal generated 500 times. The three 22-megohm resistors will provide full-scale output if the thermocouple opens.

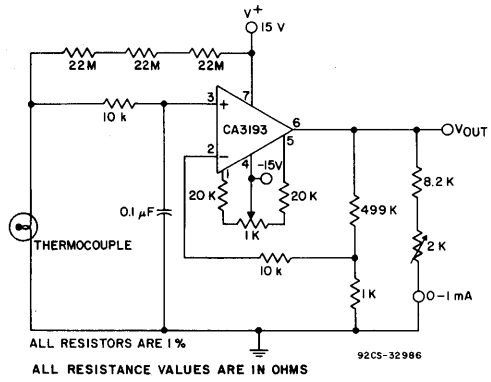


Fig. 24 - The CA3193 used in a thermocouple circuit.

May 1990

Dual BiMOS Operational Amplifiers

With MOSFET Input, Bipolar Output

Features:

- *Dual version of CA3140*
- *Internally compensated*
- *MOSFET input stage*
  - *(a) Very high input impedance (Z_{IN}): 1.5 TΩ typ.*
  - *(b) Very low input current (I_I): 10 pA typ. at ±15 V*
  - *(c) Wide common-mode input voltage range (V_{ICR}): can be swung 0.5 volt below negative supply voltage rail*
- *Directly replaces industry type 741 in most applications*

Applications:

- *Ground referenced single supply amplifiers in automobile and portable instrumentation*
- *Sample and hold amplifiers*
- *Long duration timers/multivibrators (microseconds- minutes-hours)*
- *Photocurrent instrumentation*
- *Active filters*
- *Intrusion alarm systems*
- *Comparators*
- *Instrumentation amplifiers*
- *Function generators*
- *Power supplies*

The CA3240A and CA3240 are dual versions of the popular CA3140 series integrated circuit operational amplifiers. They combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOSFET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range (typically to 0.5 V below the negative supply rail). The bipolar output transistors allow a wide output voltge swing and provide a high output current capability.

The CA3240A and CA3240 are supplied in the 8-lead dual-in-line plastic package (Mini-DIP, E suffix), and in the 14-lead dual-in-line plastic package (E1 suffix). They are pin-compatible with the industry standard 747 and 1458 operational amplifiers in similar packages. The CA3240A and CA3240 have an operating temperature range of -40 to +85°C. The offset null feature is available only when these types are supplied in the 14-lead dual-in-line plastic package (E1 suffix). The CA3240 is also available in chip form (H suffix).

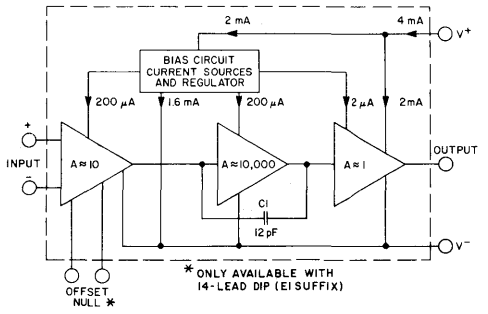


Figure 1 - Block diagram of one-half CA3240 series.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V
OPERATING VOLTAGE RANGE	4 to 36 V or ±2 to ±18 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT	1 mA
DEVICE DISSIPATION:	
UP TO 55°C	630 mW
ABOVE 55°C	Derate linearly 6.67 mW/°C
TEMPERATURE RANGE:	
OPERATING	−40 to +85°C
STORAGE	−65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION●	UNLIMITED
LEAD TEMPERATURE (DURING SOLDERING):	
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265°C

● Short circuit may be applied to ground or to either supply. Temperatures and/or supply voltages must be limited to keep dissipation within maximum rating.

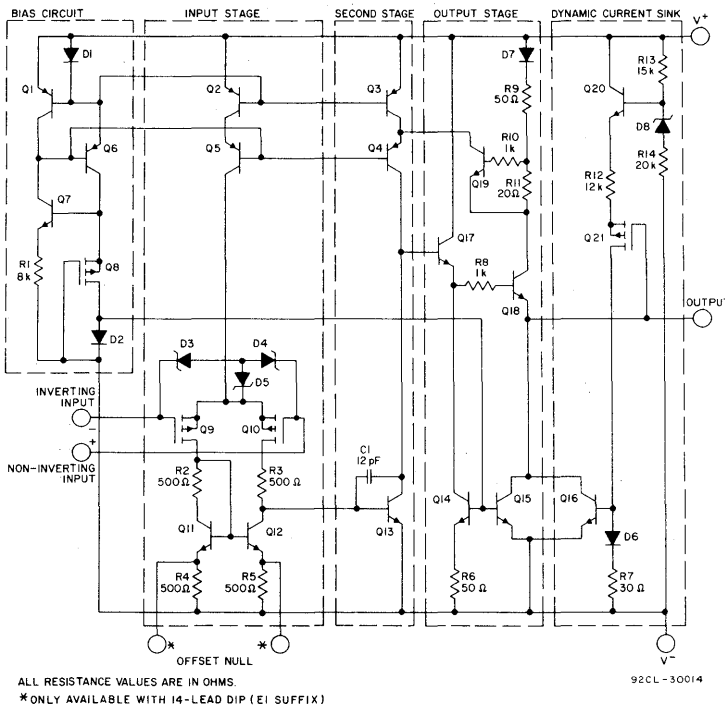


Fig. 2 – Schematic diagram of one-half CA3240 series.

Circuit Description

The schematic diagram of one amplifier section of the CA3240 is shown in Fig. 2. It consists of a differential amplifier stage using PMOS transistors Q9 and Q10 with gate-to-source protection against static discharge damage provided by zener diodes D3, D4, and D5. Constant current bias is applied to the differential amplifier from transistors Q2 and Q5 connected as a constant-current source. This assures a high common-mode rejection ratio. The output of the differential amplifier is coupled to the base of gain stage transistor Q13 by means of an n-p-n current mirror that supplies the required differential-to-single-ended conversion. Provision for offset null for types in the 14-lead plastic package (E1 suffix) is provided through the use of this current mirror.

The gain stage transistor Q13 has a high-impedance active load (Q3 and Q4) to provide maximum open-loop gain. The collector of Q13 directly drives the base of the compound emitter-follower output stage. Pull-down for the output stage is provided by two independent circuits: (1) constant-current-connected transistors Q14 and Q15 and (2) dynamic current-sink transistor Q16 and its associated circuitry. *The level of pull-down current is constant at about 1 mA for Q15 and varies from 0 to 18 mA for Q16 depending on the magnitude of the voltage between the output terminal and V^+.* The dynamic current sink becomes active whenever the output terminal is more negative than V^+ by about 15 V. When this condition exists, transistors Q21 and Q16 are turned on causing Q16 to sink current from the output terminal to V^-. This current always flows when the output is in the linear region, either from the load resistor or from the emitter of Q18 if no load resistor is present. The purpose of this dynamic sink is to permit the output to go within 0.2 V (V_{CE}(sat)) of V^- with a 2-kΩ load to ground. *When the load is returned to V^+, it may be necessary to supplement the 1 mA of current from Q15 in order to turn on the dynamic current sink (Q16).* This may be accomplished by placing a resistor (approx. 2 kΩ) between the output and V^-

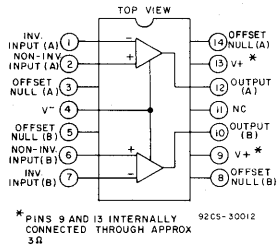
ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At V^+ = 15 V, V^- = 15 V, T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC	LIMITS						UNITS
	CA3240A			CA3240			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\lvert V_{IO}\rvert$	–	2	5	–	5	15	mV
Input Offset Current, $\lvert I_{IO}\rvert$	–	0.5	20	–	0.5	30	pA
Input Current, I_I	–	10	40	–	10	50	pA
Large-Signal Voltage Gain, A_{OL}●	20 k	100 k	–	20 k	100 k	–	V/V
(See Figs. 4, 19)	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR	–	32	320	–	32	320	μV/V
(See Fig. 9)	70	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR} (See Fig. 16)	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	11	V
Power-Supply Rejection Ratio, $\frac{\Delta V_{IO}}{\Delta V}$ PSRR	–	100	150	–	100	150	μV/V
(See Fig. 11)	76	80	–	76	80	–	dB
Maximum Output Voltage,■ V_{OM}^+	+12	13	–	+12	13	–	V
(See Figs. 22, 16) V_{OM}^-	−14	−14.4	–	−14	−14.4	–	
Maximum Output Voltage,† V_{OM}^-	0.4	0.13	–	0.4	0.13	–	V
Supply Current, (See Fig. 7) For Both Amps. I^+	–	8	12	–	8	12	mA
Total Device Dissipation, P_D	–	240	360	–	240	360	mW

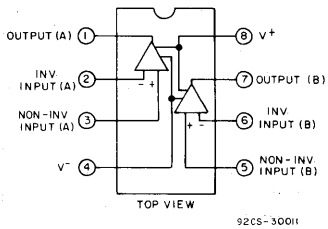
● At V_O = 26 V_{p-p}, +12 V, −14 V and R_L = 2 kΩ.
■ At R_L = 2 kΩ.
† At V^+ = 5 V, V^- = GND, I_{Sink} = 200 μA.

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS $V^+ = +15$ V, $V^- = -15$ V, $T_A = 25^oC$	TYPICAL VALUES CA3240A	TYPICAL VALUES CA3240	UNITS
Input Offset Voltage Adjustment Resistor (E1 Package Only)		Typ. Value of Resistor Between Terms. 4 and 3(5) or Between 4 and 14(8) to Adjust Max. V_{IO}	18	4.7	kΩ
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I		4	4	pF
Output Resistance	R_O		60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 21)	e_n	BW=140 kHz, R_S = 1 MΩ	48	48	μV
Equivalent Input Noise Voltage (See Fig. 10)	e_n	f= 1 kHz, R_S= 100 Ω	40	40	$nV/\sqrt{Hz}$
		f=10 kHz, R_S= 100 Ω	12	12	$nV/\sqrt{Hz}$
Short-Circuit Current to Opposite Supply Source	I_{OM}^+		40	40	mA
Sink	I_{OM}^-		11	11	mA
Gain-Bandwidth Product (See Figs. 5 and 19)	f_T		4.5	4.5	MHz
Slew Rate (See Fig. 6)	SR		9	9	V/μs
Transient Response: Rise Time	t_r	R_L=2 kΩ, C_L=100 pF	0.08	0.08	μs
Overshoot (See Fig. 20)	t_r	R_L=2 kΩ, C_L=100 pF	10	10	%
Settling Time at 10 V_{p-p}, (See Fig. 17) 1 mV	t_s	R_L=2 kΩ, C_L=100 pF, Voltage Follower	4.5	4.5	μs
Settling Time at 10 V_{p-p}, (See Fig. 17) 10 mV	t_s	R_L=2 kΩ, C_L=100 pF, Voltage Follower	1.4	1.4	μs
Crosstalk		f = 1 kHz	120	120	dB



E1 Suffix
Pin compatible with the industry-standard 747



E Suffix
Pin compatible with the industry-standard 1458

Fig. 3 — Functional diagrams.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At V^+ = 15 V, V^- = 15 V, T_A = −40 to +85°C Unless Otherwise Specified

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage,	$\lvert V_{IO}\rvert$	3	10	mV
Input Offset Current,♦	$\lvert I_{IO}\rvert$	32	32	pA
Input Current,♦	I_I	640	640	pA
Large-Signal Voltage Gain, (See Figs. 4, 19)	A_{OL}●	63 k	63 k	V/V
		96	96	dB
Common-Mode Rejection Ratio, (See Fig. 9)	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range, (See Fig. 16)	V_{ICR}	−15 to +12.3	−15 to +12.3	V
Power-Supply Rejection Ratio, (See Fig. 11)	$\frac{\Delta V_{IO}/\Delta V}{PSRR}$	150	150	μV/V
		76	76	dB
Maximum Output Voltage,■ (See Figs. 16, 22)	V_{OM}^+	12.4	12.4	V
	V_{OM}^-	−14.2	−14.2	
Supply Current, (See Fig. 7) For Both Amps.	I^+	8.4	8.4	mA
Total Device Dissipation,	P_D	252	252	mW
Temperature Coefficient of Input Offset Voltage,	$\Delta V_{IO}/\Delta T$	15	15	μV/°C

● At V_O = 26 $V_{p\text{-}p}$, +12 V, −14 V and R_L = 2 kΩ.
■ At R_L = 2 kΩ.
♦ At T_A = 85°C

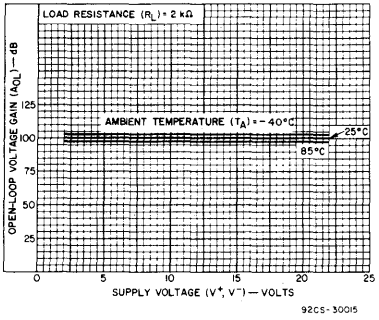


Fig. 4 — Open-loop voltage gain as a function of supply voltage and temperature.

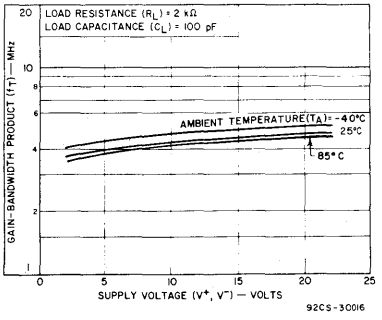


Fig. 5 — Gain-bandwidth product as a function of supply voltage and temperature.

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE
At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3240A	CA3240	
Input Offset Voltage,	$\|V_{IO}\|$	2	5	mV
Input Offset Current,	$\|I_{IO}\|$	0.1	0.1	pA
Input Current,	I_I	2	2	pA
Input Resistance		1	1	TΩ
Large-Signal Voltage Gain, (See Figs. 4, 19)	A_{OL}	100 k	100 k	V/V
		100	100	dB
Common-Mode Rejection Ratio,	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range, (See Fig. 22)	V_{ICR}	−0.5	−0.5	V
		2.6	2.6	
Power-Supply Rejection Ratio,	PSRR	31.6	31.6	μV/V
		90	90	dB
Maximum Output Voltage,	V_{OM}^+	3	3	V
(See Figs. 16,22)	V_{OM}^-	0.3	0.3	
Maximum Output Current: Source,	I_{OM}^+	20	20	mA
Sink	I_{OM}^-	1	1	
Slew Rate (See Fig. 6)		7	7	V/μs
Gain-Bandwidth Product, (See Fig. 5)	f_T	4.5	4.5	MHz
Supply Current, (See Fig. 7)	I^+	4	4	mA
Device Dissipation,	P_D	20	20	mW

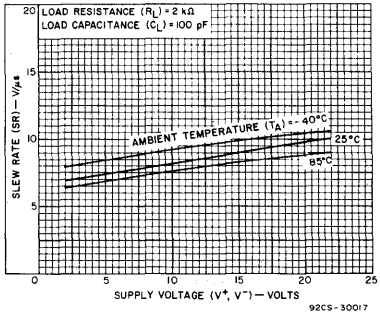


Fig. 6 — Slew rate as a function of supply voltage and temperature.

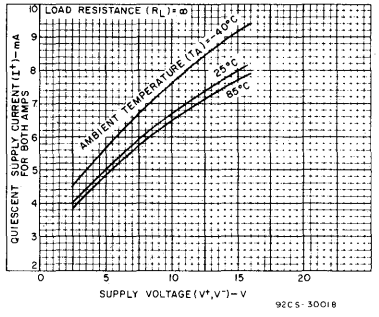


Fig. 7 — Quiescent supply current as a function of supply voltage and temperature.

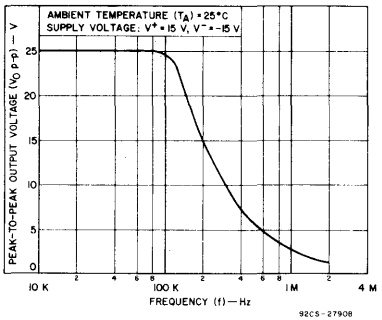


Fig. 8 — Maximum output voltage swing as a function of frequency.

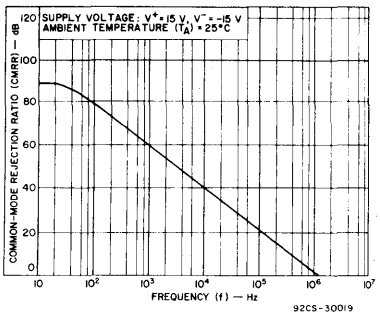


Fig. 9 — Common-mode rejection ratio as a function of frequency.

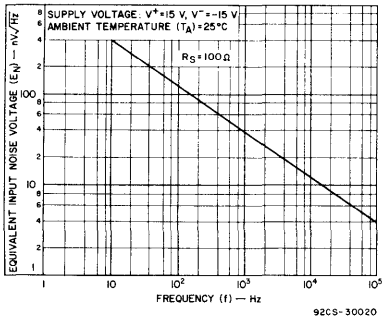


Fig. 10 — Equivalent input noise voltage as a function of frequency.

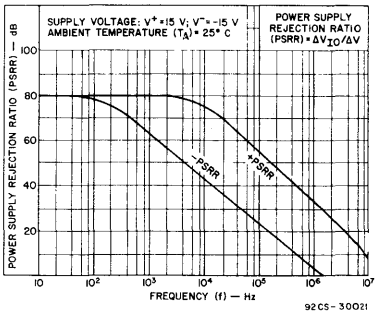


Fig. 11 — Power supply rejection ratio as a function of frequency.

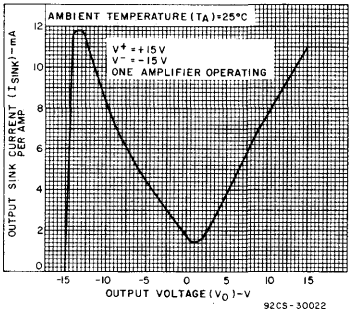


Fig. 12 — Output sink current as a function of output voltage.

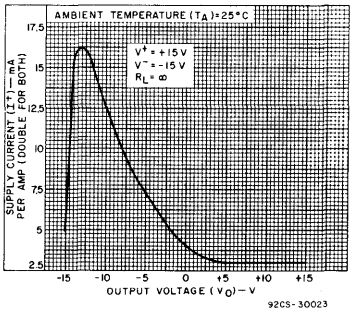


Fig. 13 — Supply current as a function of output voltage.

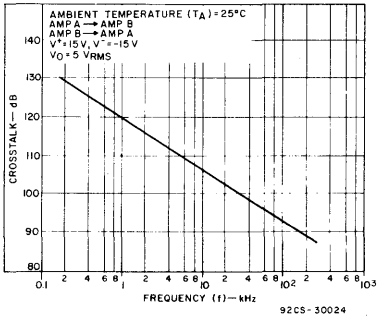


Fig. 14 — Crosstalk as a function of frequency.

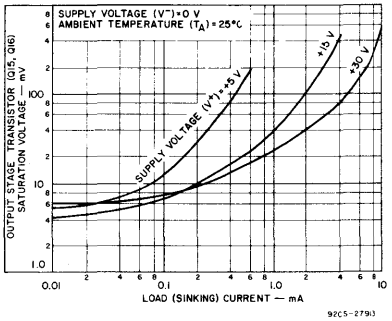


Fig. 15 — Voltage across output transistors Q15 and Q16 as a function of load current.

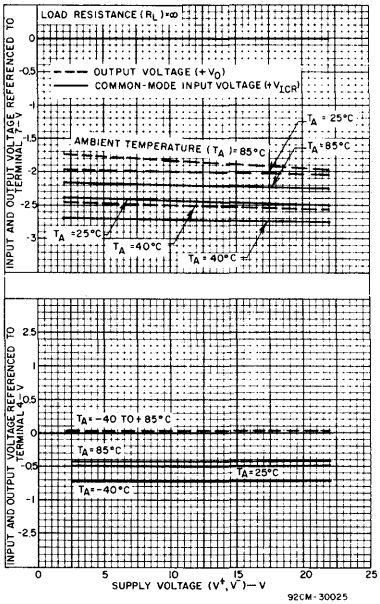


Fig. 16 — Output-voltage-swing capability and common-mode input-voltage range as a function of supply voltage and temperature.

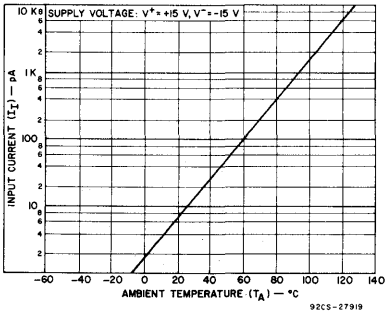


Fig. 18 — Input current as a function of ambient temperature.

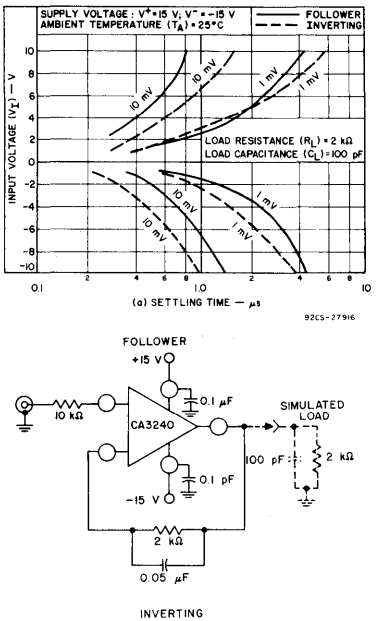


Fig. 17 — Input voltage as a function of settling time.

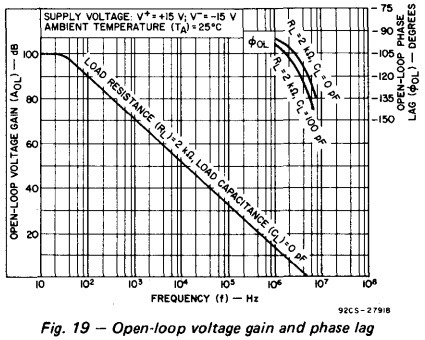
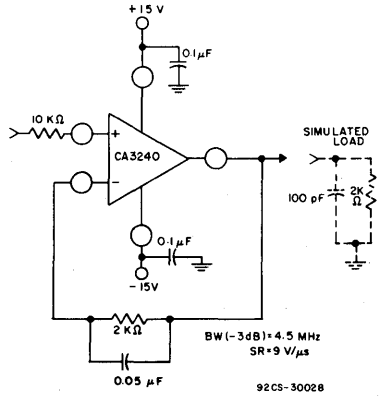
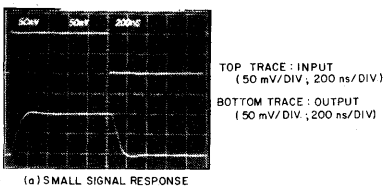
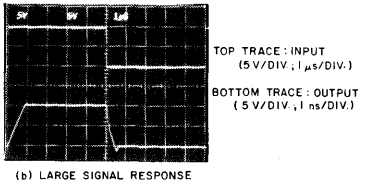


Fig. 19 — Open-loop voltage gain and phase lag as a function of frequency.





(a) SMALL SIGNAL RESPONSE



(b) LARGE SIGNAL RESPONSE

92CS-30029

Fig. 20 – Split-supply voltage-follower test circuit and associated waveforms.

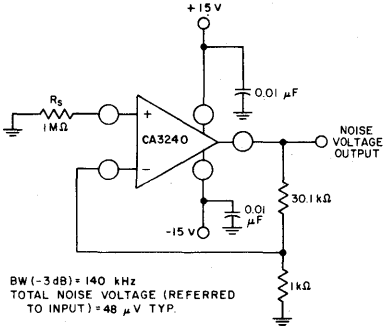


Fig. 21 – Test-circuit amplifier (30-dB gain) used for wideband noise measurement.

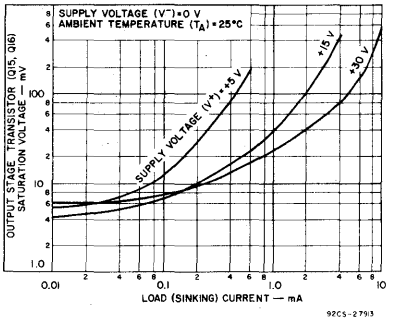


Fig. 22 – Voltage across output transistors Q15 and Q16 as a function of load current.

APPLICATIONS CONSIDERATIONS

Output Circuit Considerations

Fig. 22 shows output current-sinking capabilities of the CA3240 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

Fig. 23 shows some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

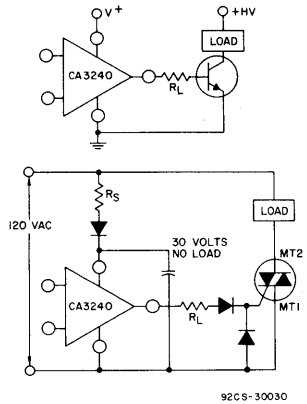


Fig. 23 — Methods of utilizing the $V_{CE}(sat)$ sinking-current capability of the CA3240 series.

Input Circuit Considerations

As indicated by the typical VICR, this device will accept inputs as low as 0.5 V below V^-. However, a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3240 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig. 24 shows typical input-terminal current versus ambient temperature for the CA3240.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

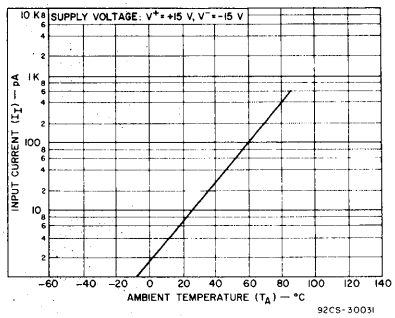


Fig. 24 — Input current as a function of ambient temperature.

Offset-Voltage Nulling

The input-offset voltage of the CA3240AE1 and CA3240E1 can be nulled by connecting a 10-kΩ potentiometer between Terminals 3 and 14 or 5 and 8 and returning its wiper arm to Terminal 4, see Fig. 25a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig. 25b, to optimize its utilization range are given in the table "Electrical Characteristics For Design Guidance" shown in this bulletin.

An alternate system is shown in Fig. 25c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

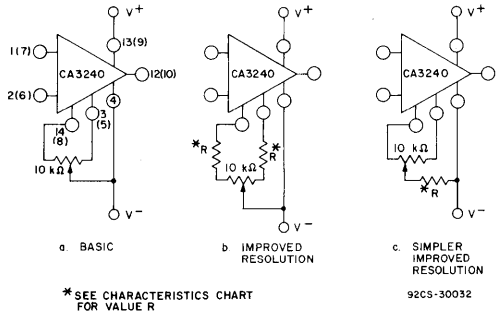


Fig. 25 – Three offset-voltage nulling methods. (CA3240AE1, CA3240E1 only.)

TYPICAL APPLICATIONS

On/Off Touch Switch

The on/off touch switch shown in Fig. 26 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the "on" plate is touched, current flows between the two halves of the grid causing a positive shift in the output voltage (Term. 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at Terminal 7 of the CA3240E, the triac is turned on and held on by the CA3059 and its associated positive feedback circuitry (51-kΩ resistor and 36-kΩ/42-kΩ voltage divider). When the positive pulse occurs at Terminal 1 (CA3240E), the triac is turned off and held off in a similar manner. Note that power for the CA3240E is supplied by the CA3059 internal power supply.

The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while allowing sufficiently high circuit impedance to provide protection against electrical shock.

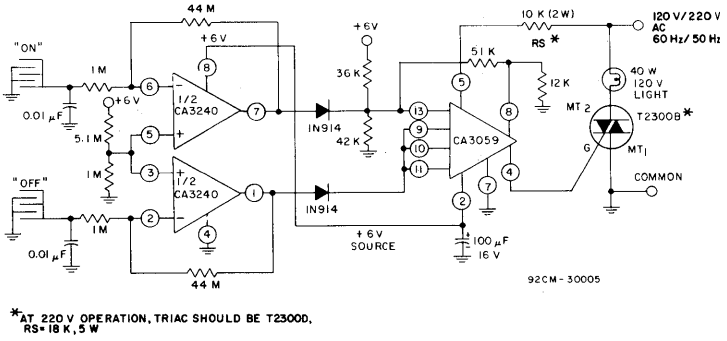


Fig. 26 – On/off touch switch.

Dual Level Detector (window comparator)

Fig. 27 illustrates a simple dual liquid level detector using the CA3240E as the sensing amplifier. This circuit operates on the principle that most liquids contain enough ions in solution to sustain a small amount of current flow between two electrodes submersed in the liquid. The current, induced by an 0.5-V potential applied between two halves of a PC board grid, is converted to a voltage level by the CA3240E in a circuit similar to that of the on/off touch switch shown in Fig. 26. The changes in voltage for both the upper and lower level sensors are processed by the CA3140 to activate an LED whenever the liquid level is above the upper sensor or below the lower sensor.

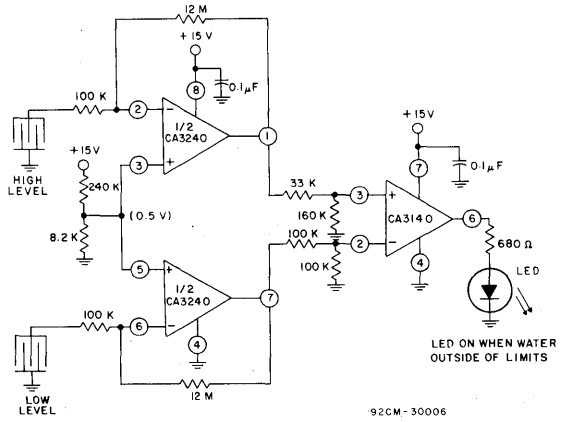


Fig. 27 – Dual level detector.

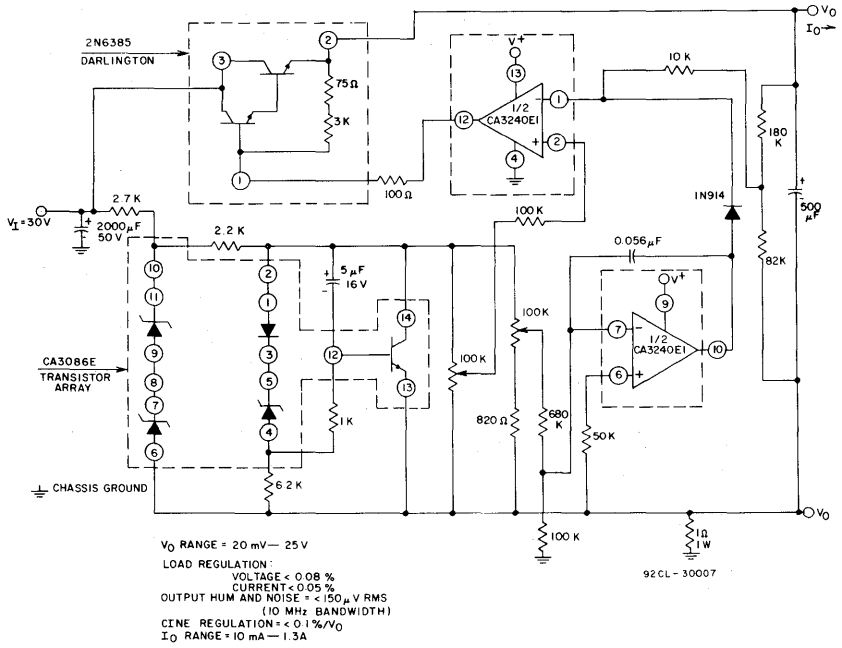


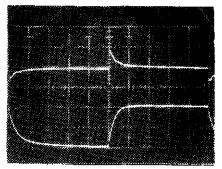
Fig. 28 – Constant-voltage/constant-current power supply.

Constant-Voltage/Constant-Current Power Supply

The constant-voltage/constant-current power supply shown in Fig. 28 uses the CA3240E as a voltage-error and current-sensing amplifier. The CA3240E is ideal for this application because its input common-mode voltage-range includes ground, allowing the supply to adjust from 20 mV to 25 V without requiring an additional negative input voltage. Also, the ground reference capability of the CA-3240E allows it to sense the voltage across the 1-Ω current-sensing resistor in the negative output lead of the power supply. The CA3086 transistor array functions as a reference for both constant-voltage and constant-current limiting. The 2N6385 power Darlington is used as the pass element and may be required to dissipate as much as 40 W. Fig. 29 shows the transient response of the supply during a 100-mA to 1-A load transition.

Precision Differential Amplifier

Fig. 30 shows the CA3240E in the classical precision differential amplifier circuit. The CA3240E is ideally suited for biomedical applications because of its extremely high input impedance. To insure patient safety, an extremely high electrode series resistance is required to limit any current that might result in patient discomfort in the event of a fault condition. In this case, 10-MΩ resistors have been used to limit the current to less than 2 μA without affecting the performance of the circuit. Fig. 31 shows a typical electrocardiogram waveform obtained with this circuit.



TRANSIENT RESPONSE

TOP TRACE: OUTPUT VOLTAGE (500 mV/cm AND 5 μs/cm)
BOTTOM TRACE: COLLECTOR OF LOAD SWITCHING TRANSISTOR LOAD = 100 mA TO 1A (5 V/cm AND 5 μs/cm)

92CS-30034

Fig. 29 – Transient response.

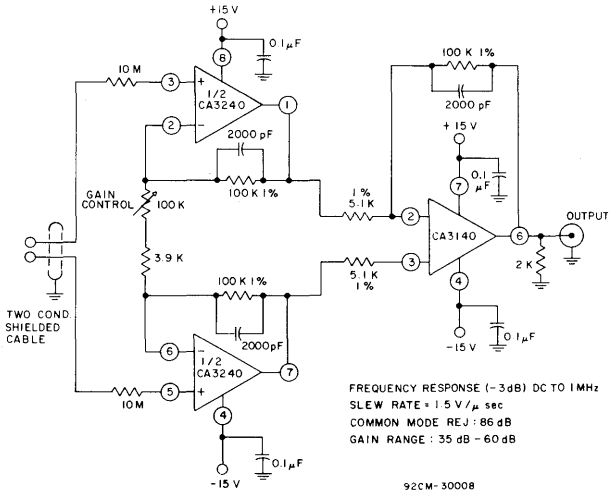
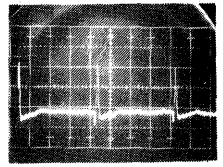


Fig. 30 – Precision differential amplifier.



TYPICAL ELECTROCARDIOGRAM WAVEFORM

VERTICAL : 1.0 mV/DIV
(AMPLIFIER GAIN = 100 X)
(SCOPE SENSITIVITY = 0.1V/DIV.
HORIZONTAL : > 0.2 SEC/DIV (UNCAL)

92CS-30033

Fig. 31 – Typical electrocardiogram waveform.

Differential Light Detector

In the circuit shown in Fig. 32, the CA3240E converts the current from two photo diodes to voltage, and applies 1 V of reverse bias to the diodes. The voltages from the CA3240E outputs are subtracted in the second stage (CA3140) so that only the difference is amplified. In this manner, the circuit can be used over a wide range of ambient light conditions without circuit component adjustment. Also, when used with a light source, the circuit will not be sensitive to changes in light level as the source ages.

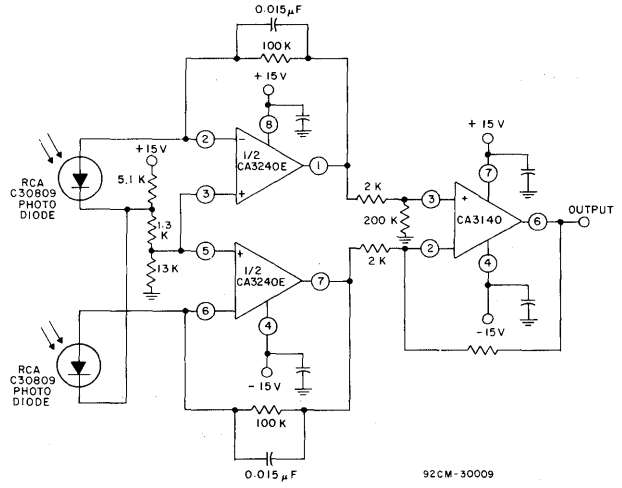


Fig. 32 – Differential light detector.

May 1990

BiMOS Operational Amplifiers

With MOSFET Input/CMOS Output

Features:

- *MOSFET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 x 10^{12}Ω) typ.
  very low I_I = 5 pA typ. at 15 V operation
  = 2 pA typ. at 5 V operation
- *Ideal for single supply applications*
- *Common-mode input voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *CMOS output stage permits signal swing to either (or both) supply rails*

Applications:

- *Ground referenced single supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long duration timers/monostables*
- *Ideal interface with digital CMOS*
- *High input impedance wideband amplifiers*
- *Voltage followers (e.g. follower for single supply D/A converter)*
- *Voltage regulators (permits control of output voltage down to zero volts)*
- *Wien-Bridge oscillators*
- *Voltage controlled oscillators*
- *Photo diode sensor amplifiers*

CA3260A and CA3260 are integrated circuit operation amplifiers that combine the advantage of both CMOS and bipoar transistors on a monolithic chip. The CA3260 series circuits are dual versions of the popular CA3160 series.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input voltage capability down to 0.5 volt below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor pair, capable of swinging the output voltage to within 10 millivolts of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA3260 Series circuits operate at supply voltages ranging from 4 to 16 volts, or ±2 to ±8 volts when using split supplies.

The CA3260 Series is supplied in standard 8-lead TO-5 style packages (T suffix) and 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA3260 is available in chip form (H suffix).

The CA3260 and CA3260A are also available in the 8-lead dual-in-line plastic package (Mini-DIP E suffix). All types operate over the full military temperature range of -55°C to +125°C. The CA3260A offers superior input characteristics over those of the CA3260.

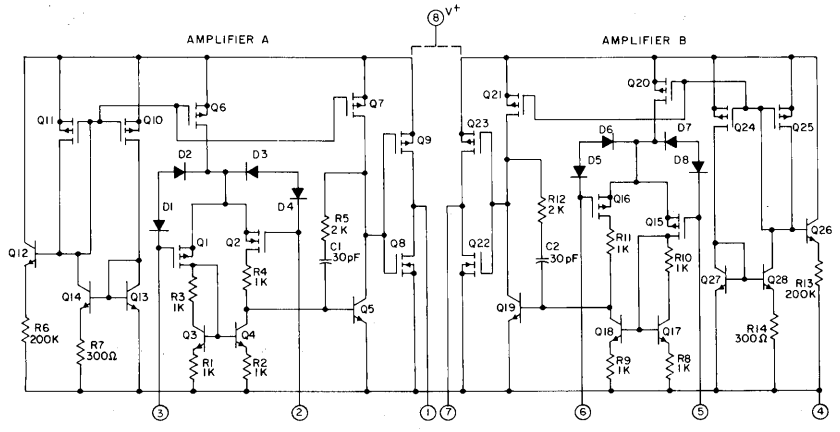
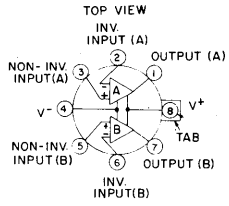
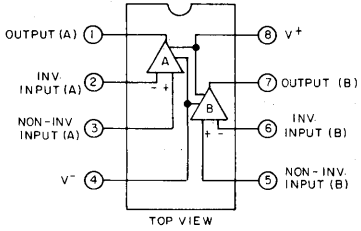


Fig. 1 - Schematic diagram of CA3260 series.



S and T Suffixes
Pin compatible with the industry-standard 1458



E Suffix
Pin compatible with the industry-standard 1458

Fig. 2 - Functional diagrams for the CA3260 Series.

ELECTRICAL CHARACTERISTICS for Each Amplifier at T_A=25°C, V^+=15 V, V^-=0 V (Unless otherwise specified)

CHARACTERISTIC	LIMITS						UNITS
	CA3260A (T,S,E)			CA3260 (T,S,E)			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\lvert V_{IO} \rvert$, $V^{\pm}$=±7.5 V	—	2	5	—	6	15	mV
Input Offset Current, $\lvert I_{IO} \rvert$, $V^{\pm}$=±7.5 V	—	0.5	20	—	0.5	30	pA
Input Current, I_I $V^{\pm}$=±7.5 V	—	5	30	—	5	50	pA
Large-Signal Voltage Gain, A_{OL}	50 k	320 k	—	50 k	320 k	—	V/V
V_O=10 V_{p-p}, R_L=10 kΩ	94	110	—	94	110	—	dB
Common-Mode Rejection Ratio, CMRR	80	95	—	70	90	—	dB
Common-Mode Input Voltage Range, V_{ICR}	0	-0.5 to 12	10	0	-0.5 to 12	10	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$=±7.5 V	—	32	150	—	32	320	μV/V
Maximum Output Voltage:							V
At R_L=10 kΩ V_{OM}^+	11	13.3	—	11	13.3	—	
At R_L=10 kΩ V_{OM}^-	—	0.002	0.01	—	0.002	0.01	
At R_L=∞ V_{OM}^+	14.99	15	—	14.99	15	—	
At R_L=∞ V_{OM}^-	—	0	0.01	—	0	0.01	
Maximum Output Current, I_{OM}^+ (Source) @ V_O=7.5 V	12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O=7.5 V	12	20	45	12	20	45	
Total Supply Current, I^+ R_L=∞ V_O(Ampli.A)=V_O (Ampli.B)=7.5 V	—	9	15.5	—	9	15.5	mA
V_O (Ampli.A)=V_O (Ampli.B)=0 V	—	1.2	3	—	1.2	3	
V_O (Ampli.A)=0 V V_O(Ampli.B)=7.5 V	—	5	8.5	—	5	8.5	
Input Offset Voltage Temp.Drift, $\Delta V_{IO}/\Delta T$	—	6	—	—	8	—	μV/°C
Crosstalk f=1 kHz	—	120	—	—	120	—	dB

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals)..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE..... (V^+ +8 V) to (V^- -0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK —
UP TO 55°C..... 630 mW
ABOVE 55°C ... Derate linearly 6.67 mW/°C
WITH HEAT SINK —
UP TO 90°C..... 1 W
ABOVE 90°C ... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING (All Types) ..... -55 to +125°C
STORAGE (All Types) ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT
DURATION*..... INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
At distance 1/16 ± 1/32 in.
(1.59 ± 0.79 mm) from case
for 10 s max. ..... +265°C

*Short circuit may be applied to ground or to either supply.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS	CA3260A (T, S, E)	CA3260 (T, S, E)	UNITS
V^+=+7.5 V, V^-=-7.5 V, T_A=25°C (Unless Otherwise Specified)				
Input Resistance, R_I		1.5	1.5	TΩ
Input Capacitance, C_I	f=1 MHz	4.3	4.3	pF
Unity Gain Crossover Frequency, f_T		4	4	MHz
Slew Rate, SR		10	10	V/μs
Transient Response: Rise Time, t_r	C_L=25 pF, R_L=2 kΩ (Voltage Follower)	0.09	0.09	μs
Overshoot		10	10	%
Settling Time (4 V_{p-p} Input to < 0.1%)		1.8	1.8	μs
V^+=5 V, V^-=0 V, T_A=25°C (Unless Otherwise Specified)				
Input Offset Voltage, V_{IO}		2	6	mV
Input Offset Current, I_{IO}		0.1	0.1	pA
Input Current, I_I		2	2	pA
Common-Mode Rejection Ratio, CMRR		70	60	dB
Large-Signal Voltage Gain, A_{OL}	V_O=4 V_{p-p}, R_L=20 kΩ	100 k 100	100 k 100	V/V dB
Common-Mode Input Voltage Range, V_{ICR}		0 to 2.5	0 to 2.5	V
Supply Current, I^+	V_O=5 V, R_L=∞	1	1	mA
	V_O=2.5 V, R_L=∞	1.2	1.2	
Power Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^+$		200	200	μV/V

May 1990

Dual Variable Operational Amplifiers

Features:

- *Low initial input-offset voltage: 500 μV max. (CA3280A)*
- *Low offset-voltage change versus I_{ABC}: <500 μV typ. for all types*
- *Low offset-voltage drift: 5 μV/C max. (CA3280A)*
- *Excellent matching of the two amplifiers for all characteristics*
- *Internal current-driven linearizing diodes reduce the external input current to an offset component*

Applications:

- *Voltage-controlled amplifiers*
- *Voltage-controlled oscillators*
- *Multipliers*
- *Demodulators*
- *Sample and hold*
- *Instrumentation amplifiers*
- *Function generators*
- *Triangle wave-to-sine wave converters*
- *Comparators*
- *Audio preamplifiers*

The CA3280 and CA3280A types consist of two variable operational amplifiers that are designed to substantially reduce the initial input offset voltage and the offset-voltage variation with respect to changes in programming current. This design results in reduced "AGC thump," an objectionable characteristic of many AGC systems. Inter-digitation, or crosscoupling, of critical portions of the circuit reduces the amplifier dependence upon thermal and processing variables.

The CA3280 has all the generic characteristics of an operational voltage amplifier except that the forward transfer

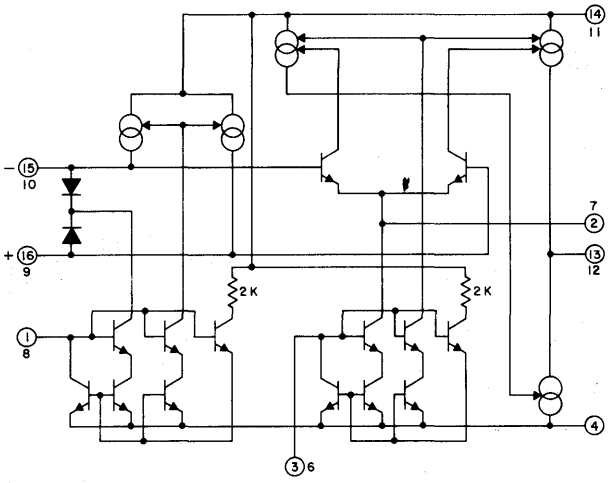


Figure 1 - Functional diagram of ½ CA3280.

characteristic is best described by transconductance rather than voltage gain, and the output is current, not voltage. The magnitude of the output current is equal to the product of transconductance and the input voltage. This type of operational transconductance amplifier was first introduced by RCA in 1969*, and it has since gained wide acceptance as a gateable, gain-controlled building block for instrumentation and audio applications, such as linearization of transducer outputs, standardization of widely changing signals for data processing, multiplexing, instrumentation amplifiers operating from the nanopower range to high current and highspeed comparators.

The operating-temperature ranges are -55 to +125° C for the CA3280A, and 0 to +70° C for the CA3280.

The CA3280 and CA3280A are supplied in the 16-lead dual-in-line plastic package (E suffix), in the 16-lead dual-in-line frit-seal ceramic package (F suffix, and are also supplied in chip form (H suffix).

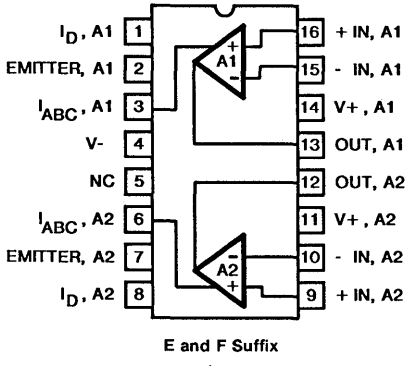
*"OTA Obsoletes Op Amp," by C.F. Wheatley and H.A. Wittlinger, NEC Proceedings, December, 1969.

For additional application information on this device and on OTA's in general, please refer to Application Notes: ICAN-6818, ICAN-6668, and ICAN-6077.

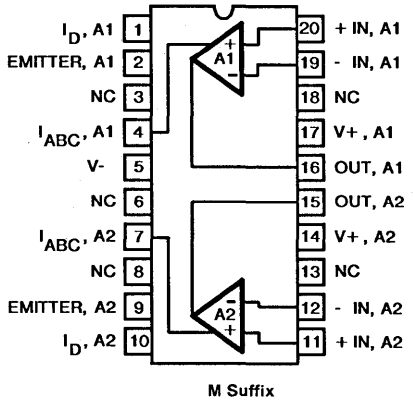
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (BETWEEN V+ AND V- TERMINALS)	36 V
DIFFERENTIAL INPUT VOLTAGE	±5 V
DC INPUT VOLTAGE RANGE	V+ to V-
INPUT SIGNAL CURRENT AT $I_D = 0$	100 μA
AMPLIFIER BIAS CURRENT	10 mA
OUTPUT SHORT CIRCUIT DURATION*	Indefinite
LINEARIZING DIODE BIAS CURRENT, I_D	5 mA
PEAK INPUT CURRENT WITH LINEARIZING DIODE	$\pm I_D$
POWER DISSIPATION, P_D:	
Either Amplifier	600 mW
Total Package	750 mW
Above 55° C	Derate linearly at 6.67 mW/° C
AMBIENT TEMPERATURE RANGE, T_A:	
Operating:	
CA3280	0 to +70° C
CA3280A	-55 to +125° C
Storage, All Types	-65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ±1/32 in. (1.59 ±0.79 mm) from case for 10 sec. max	+265° C

*Short circuit may be applied to ground or to either supply.



E and F Suffix



M Suffix

CA3280 Terminal Assignments

ELECTRICAL CHARACTERISTICS at T_A = 25°C, $V^{\pm}$ = 15 V (Unless Otherwise Stated)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA3280			CA3280A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, V_{IO}	I_{ABC}=1 mA	–	–	3	–	–	0.5	mV
	I_{ABC}=100μA	–	0.7	3	–	0.25	0.5	
	I_{ABC}=10μA	–	–	3	–	–	0.5	
	I_{ABC}=1mA to 10μA T_A=full temp. range	–	0.8	4	–	0.8	1.5	
Input Offset Voltage Change, $\lvert\Delta V_{IO}\rvert$	I_{ABC}=1μA to 1mA	–	0.5	1	–	0.5	1	mV
	I_{ABC}=100μA T_A=full temp. range	–	5	–	–	3	5	μV/°C
Amplifier Bias Voltage, V_{ABC}	I_{ABC}=100μA	–	1.2	–	–	1.2	–	V
Peak Output Voltage: Positive VOM^+	I_{ABC}=500μA	12	13.7	–	12.5	13.7	–	V
Negative VOM^-		12	−14.3	–	−13.3	−14.3	–	
Positive VOM^+	I_{ABC}=5μA	12	13.9	–	12.5	13.9	–	
Negative VOM^-		12	−14.5	–	−13.5	−14.5	–	
Common-Mode Input Voltage Range, V_{ICR}	I_{ABC}=100μA	−13	–	13	−13	–	13	V
Noise Voltage, e_N: 10 Hz	I_{ABC}=500μA	–	20	–	–	20	–	nV/$\sqrt{Hz}$
1 kHz		–	8	–	–	8	–	μV/$\sqrt{Hz}$
10 kHz		–	7	–	–	7	–	nV/$\sqrt{Hz}$
Input Offset Current, I_{IO}	I_{ABC}=500μA	–	0.3	0.7	–	0.3	0.7	μA
Input Bias Current, I_{IB}	I_{ABC}=500μA	–	1.8	5	–	1.8	5	μA
	I_{ABC}=500μA T_A=full temp. range	–	3	8	–	3	8	
Peak Output Current: Source IOM^+	I_{ABC}=500μA	350	410	650	350	410	650	μA
Sink IOM^-		−350	−410	−650	−350	−410	−650	
Source IOM^+	I_{ABC}=5μA	3	4.1	7	3	4.1	7	
Sink IOM^-		−3	−4.1	−7	−3	−4.1	−7	
Sink and Source, IOM^-, IOM^+	I_{ABC}=500μA T_A=full temp. range	350	450	550	350	450	550	
Linearization Diodes: Dynamic Impedance	I_D = 100μA	–	700	–	–	700	–	Ω
Offset Current	I_D =100μA	–	10	–	–	10	–	μA
	I_D=10μA	–	0.5	1	–	0.5	1	

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA3280			CA3280A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Diode Network Supply Current	I_{ABC}=100μA	250	400	800	250	400	800	μA
Amplifier Supply Current (Per amplifier)	I_{ABC}=500μA	–	2	2.4	–	2	2.4	mA
Amplifier Output Leakage Current, I_{OL}	I_{ABC}=0, V_O=0V	–	0.015	0.1	–	0.015	0.1	nA
	I_{ABC}=0, V_O=30V	–	0.15	1	–	0.15	1	
Common-Mode Rejection Ratio, CMRR	I_{ABC}=100μA	80	100	–	94	100	–	dB
Power-Supply Rejection Ratio, PSRR	I_{ABC}=100μA	86	105	–	94	105	–	dB
Open-Loop Voltage Gain, A_{OL}	I_{ABC}=100μA, R_L=∞,	94	100	–	94	100	–	dB
	V_O=20 Vp-p	50K	100K	–	50K	100K	–	V/V
Forward Transconductance: Large Signal, Gm	I_{ABC}=50μA	–	0.8	1.2	–	0.8	1.2	mmho
Small Signal, gm	I_{ABC}=1mA	–	16	22	–	16	22	
Input Resistance, R_I	I_{ABC}=10μA	0.5	–	–	0.5	–	–	MΩ
Channel Separation	f=1 kHz	–	94	–	–	94	–	dB
Open-Loop Total Harmonic Distortion	f=1 kHz, I_{ABC}= 1.5 mA, R_L=15kΩ, V_O= 20 Vp-p	–	0.4	–	–	0.4	–	%
Bandwidth	I_{ABC}=1mA, R_L=100Ω	–	9	–	–	9	–	MHz
Slew Rate, SR: Open Loop	I_{ABC}=1mA	–	125	–	–	125	–	V/μs
Capacitance: Input, C_I	I_{ABC}=100μA	–	4.5	–	–	4.5	–	pF
Output, C_O		–	7.5	–	–	7.5	–	
Output Resistance, R_O	I_{ABC}=100μA	–	63	–	–	63	–	MΩ

Figs. 2 and 3 show the equivalent circuits for the current source and linearization diodes in the CA3280. The current through the linearization network is approximately equal to the programming current. There are several advantages to driving these diodes with a current source. First, only the offset current from the biasing network flows through the input resistor. Second, another input is provided to extend the gain control dynamic range. And third, the input is truly differential and can accept signals within the common-mode range of the CA3280.

The structure of the variable operational amplifier eliminates the need for matched resistor networks in differential to single-ended converters, as shown in Fig. 4. A matched resistor network requires ratio matching of 0.01% or trimming for 80 dB of common-mode rejection. The CA3280, with its excellent common-mode rejection ratio, is capable of converting a small (±25 mV) differential input signal to a single-ended output without the need for a matched resistor network.

Fig. 5 shows the CA3280 in a typical gain-control application. The input-signal range as a function of distortion at various levels of linearization diode current is shown in Fig. 6 This curve shows only the AGC capability of the diode network, but gain control can also be performed with the amplifier bias current (I_{ABC}). With no diode bias current, the gain is merely gmR_L. For example, with an I_{ABC} of 1 mA, the gm is approximately 16 mmhos. With the CA3280 operating into a 5 kΩ resistor, the gain is 80.

The need for external buffers can be eliminated by the use of low-value load resistors, but the resulting increase in the required amplifier bias current reduces the input impedance of the CA3280. The linearization diode impedance also decreases as the diode bias current increases, which further loads the input. The diodes, in addition to acting as a linearization network, also operate as an additional attenuation system to accommodate input signals in the volt range when they are applied through appropriate input resistors.

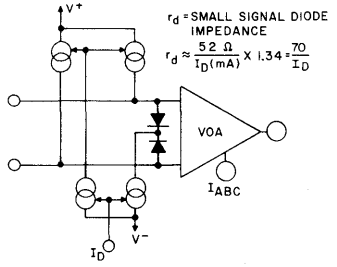


Fig. 2 – VOA showing linearization diodes and current drive.

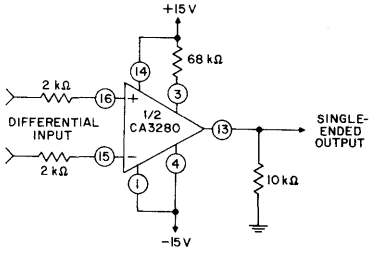


Fig. 4 – Differential to single-ended converter.

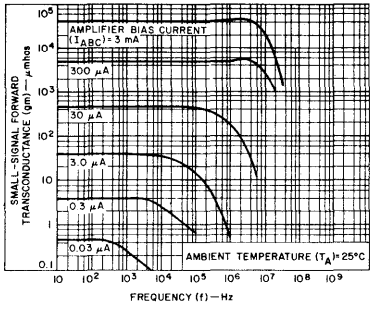


Fig. 6 – Amplifier gain as a function of frequency.

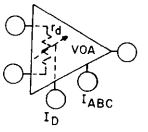


Fig. 3 – Block diagram of linearized VOA.

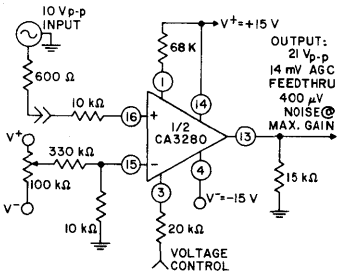
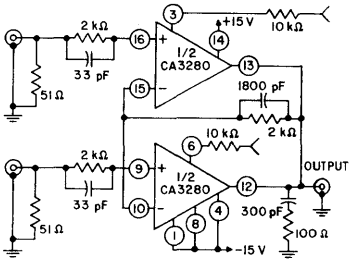


Fig. 5 – Typical gain control circuit.



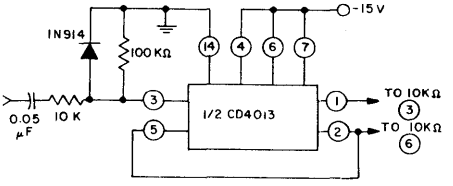


Fig. 7 – Two-channel linear multiplexer.

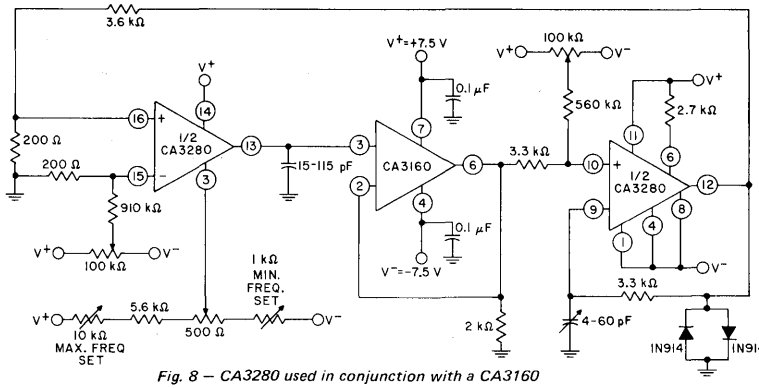


Fig. 8 — CA3280 used in conjunction with a CA3160 to provide a function generator with a tunable range of from 2 Hz to 1 MHz.

Fig. 9 shows a triangle wave-to-sine wave converter using the CA3280. Two 100KΩ resistors are connected between the differential amplifier emitters and V+ to reduce the current flow through the differential amplifier. This allows the amplifier to fully cut off during peak input signal excursions. THD is approximately 0.37% for this circuit.

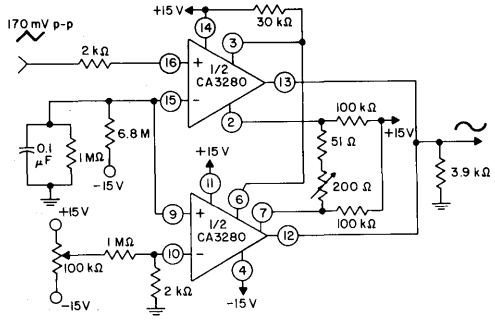


Fig. 9 — Triangle wave-to-sine wave converter.

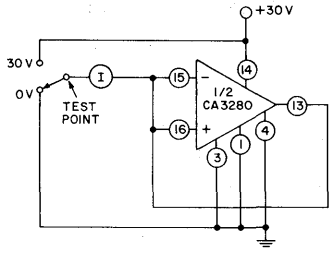


Fig. 10 — Leakage current test circuit.

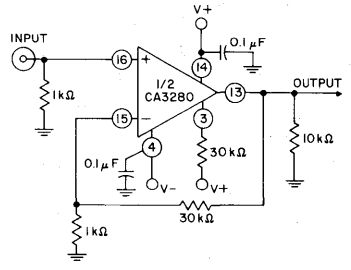
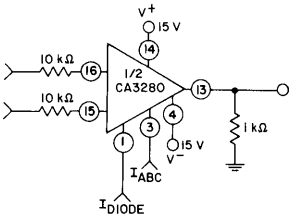
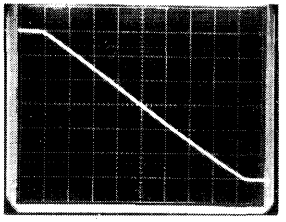


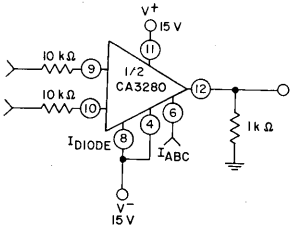
Fig. 11 — Channel separation test circuit.

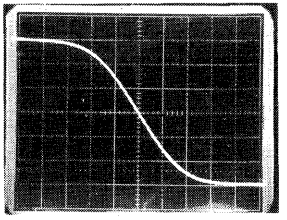




I_{abc} = 650 μA
I_D = 200 μA
VERT = 200 μA/DIV
HOR = 1 V/DIV

a) With diode programming terminal active





I_{abc} = 650 μA
I_D = 0
VERT = 200 μA/DIV
HOR = 25 mV/DIV

b) With diode programming terminal cut-off

Fig. 12 – CA3280 transfer characteristics.

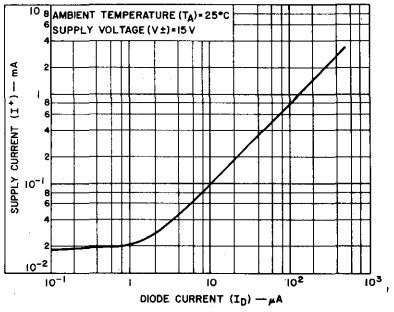


Fig. 13 – Supply current as a function of diode current.

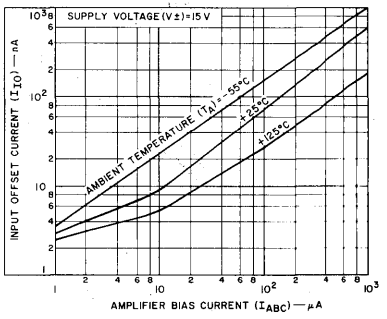


Fig. 14 – Input offset current as a function of amplifier bias current.

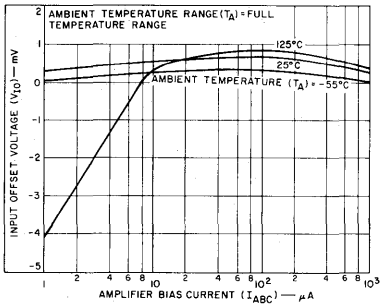


Fig. 15 – Input offset voltage as a function of amplifier bias current.

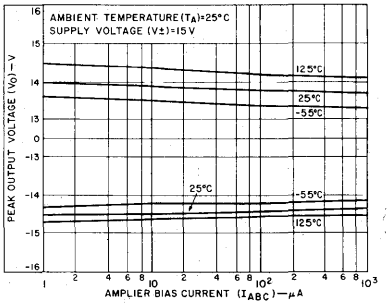


Fig. 16 – Peak output voltage as a function of amplifier bias current.

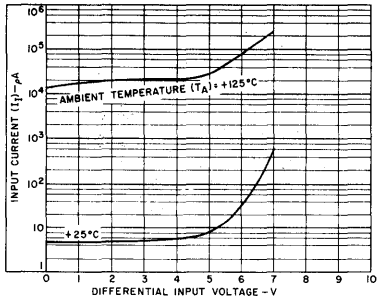


Fig. 17 – Input current as a function of input differential voltage.

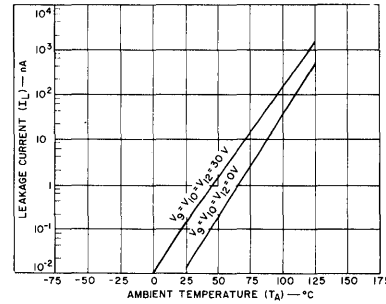


Fig. 18 – Leakage current as a function of temperature.

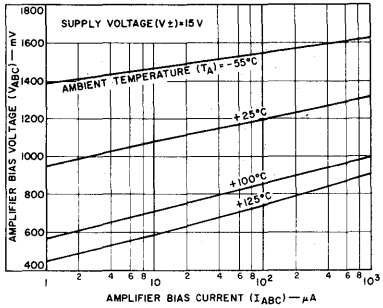


Fig. 19 – Amplifier bias voltage as a function of amplifier bias current.

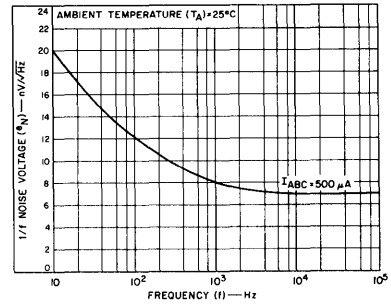


Fig. 20 – 1/F noise as a function of frequency.

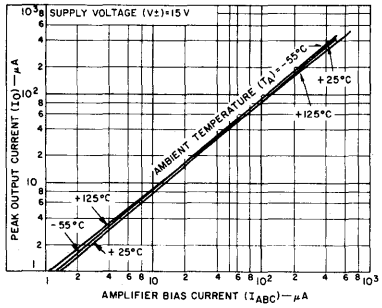


Fig. 21 – Peak output current as a function of amplifier bias current.

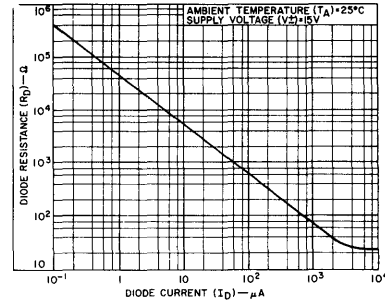


Fig. 22 – Diode resistance as a function of diode current.

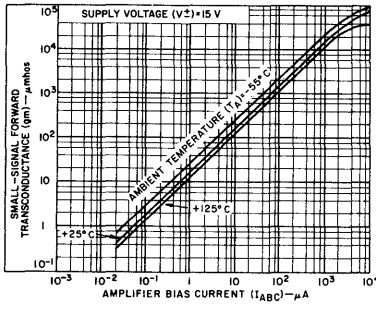


Fig. 23 – Amplifier gain as a function of amplifier bias current.

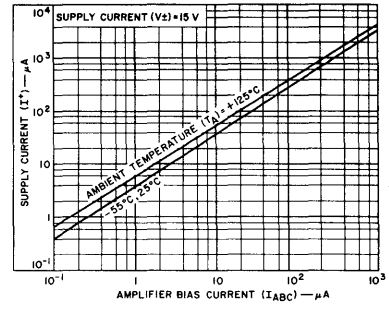


Fig. 24 – Supply current as a function of amplifier bias current.

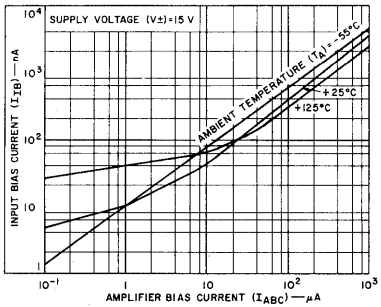
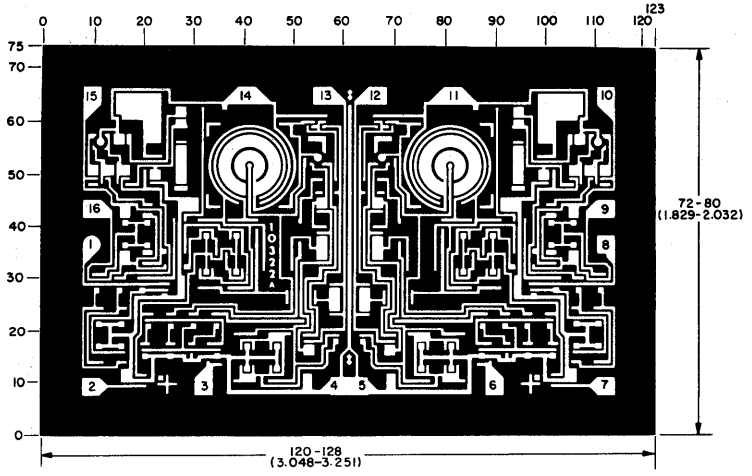


Fig. 25 – Input bias current as a function of amplifier bias current.



Dimensions and pad layout for CA3280H.

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

May 1990

Quad BiMOS Operational Amplifiers

With MOSFET Input, Biploar Output

Features:

- *Internally compensated*
- *MOSFET Input Stage*
  - *(a) Very high input impedance (Z_{IN}): 1.5 TΩ typ.*
  - *(b) Very low input current (I_I): 10 pA typ. at ±15 V*
  - *(c) Wide common-mode input voltage range (V_{ICR}): can be swung to the negative supply voltage rail*
  - *(d) Rugged input stage: bipolar diode protected*
- *Directly replaces industry type 324 in most applications*
- *Operation from 6-to-36 volts single or dual supplies*
- *Characterized for ±15-volt operation and for TTL supply systems with operation down to 6 volts*
- *Wide bandwidth: 5 MHz unity gain at ±15 V or a single 30 V supply*
- *High voltage follower slew rate: 10 V/μs*

Applications:

- *Ground referenced single supply amplifiers in automobile and portable instrumentation*
- *Sample and hold amplifiers*
- *Long duration timers/multivibrators (microseconds-minutes-hours)*
- *Photocurrent instrumentation*
- *Active filters*
- *Intrusion alarm systems*
- *Comparators*
- *Instrumentation amplifiers*
- *Function generators*
- *Power supplies*

The CA3410A and CA3410 are BiMOS integrated circuit operational amplifiers. They combine the advantage of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOSFET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range (typically to the negative supply rail). The bipolar output transistors allow a wide output voltage swing and provide a high output current capability

The CA3410A and CA3410 are supplied in the 14-lead dual-in-line plastic package (E suffix). They are pin-compatible with the industry standard 324 and 084 operational amplifiers in similar packages. The CA3410A and CA3410 have an operating temperature range of -40 to +85°C.

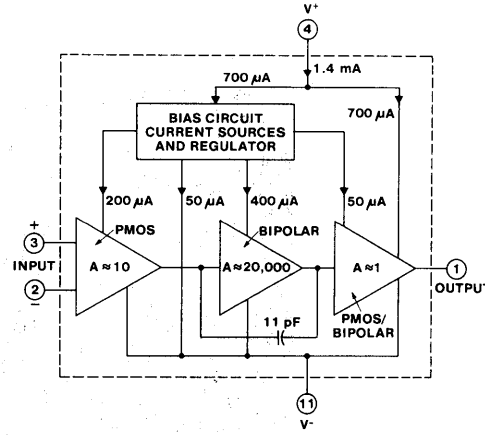


Figure 1 - Block diagram of ¼ of the CA3410E.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS) ..... 36 V
OPERATING VOLTAGE RANGE ..... 6 to 36 V
or ±2 to ±18 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±16 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8 V) to (V^- -0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
UP TO 55°C ..... 625 mW
ABOVE 55°C ..... Derate linearly 6.67 mW/°C
TEMPERATURE RANGE:
OPERATING ..... -40 to +85°C
STORAGE ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION• ..... UNLIMITED
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM)
FROM CASE FOR 10 SECONDS MAX. ..... +265°C

•Short circuit may be applied to ground or to either supply. Temperatures and/or supply voltages must be limited to keep dissipation within maximum rating.

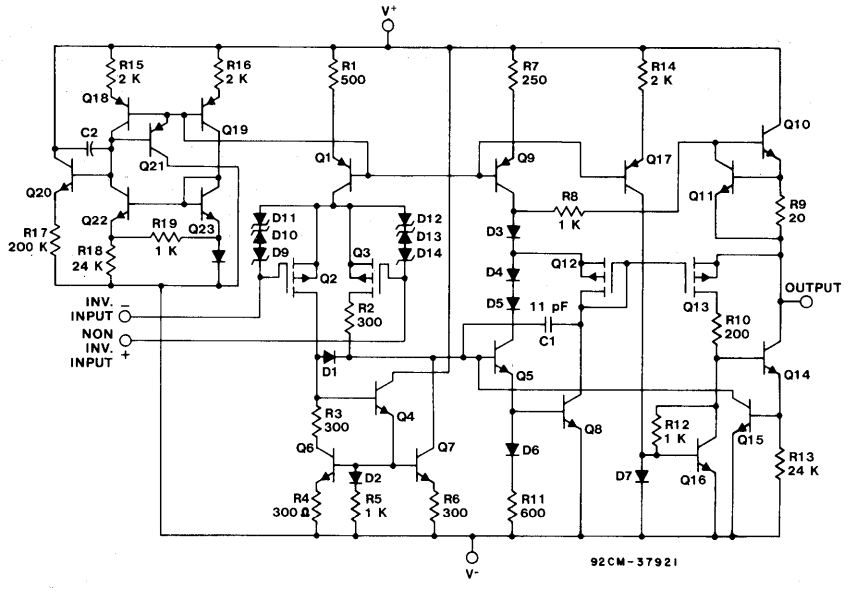


Fig. 2 - Schematic diagram for 1/4 of the CA3410.

Circuit Description

The schematic diagram of one amplifier section of the CA3410 is shown in Fig. 2. It consists of a differential amplifier stage using PMOS transistors Q2 and Q3 with gate-to-source protection against static discharge damage provided by zener diodes D9, D10, D11, and D12, D13, D14. Constant current bias is applied to the differential amplifier from transistors Q1 connected as a constant-current source. This assures a high common-mode rejection ratio. The output of the differential amplifier is coupled to the base of gain stage transistors Q5 and Q8 by means of an n-p-n current mirror that supplies the required differential-to-single-ended conversion.

ELECTRICAL CHARACTERISTICS for Equipment Design at V^+ = 15 V, V^- = 15 V, T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC		LIMITS						UNITS
		CA3410A			CA3410			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	—	3	8	—	8	15	mV
Input Offset Current	I_{IO}	—	0.5	10	—	0.5	30	pA
Input Current	I_I	—	10	30	—	10	40	pA
Large-Signal Voltage Gain	A_{OL}	20 k	100 k	—	20 k	100 k	—	V/V
R_L = 2 kΩ	V_O = ± 10 V	86	100	—	86	100	—	dB
Common-Mode Rejection Ratio	CMRR	—	32	100	—	32	320	μV/V
		80	90	—	70	90	—	dB
Common-Mode Input-Voltage Range	V_{ICR}	-15	-15.5 to 13	12.5	-15	-15.5 to 13	12.5	V
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V$	—	50	100	—	50	316	μV/V
	PSRR	80	86	—	70	86	—	dB
Maximum Output Voltage Swing	V_{OM}^+	13	13.9	—	13	13.9	—	V
R_L = 2 kΩ	V_{OM}^-	-10.5	-11.2	—	-10.5	-11.2	—	
Maximum Output Voltage Swing	V_{OM}^+	13.5	14.2	—	13.5	14.2	—	V
R_L = 10 kΩ	V_{OM}^-	-11	-12.2	—	-11	-12.2	—	
Total Supply Current	I^+	—	8	10	—	8	12	mA
Total Device Dissipation	P_D	—	240	300	—	240	360	mW

Circuit Description (Cont'd)

Output Stage

The output stage is a physo-complementary amplifier with n-p-n output transistors. Diode D3 complements Q10, while diode connected PMOS transistor Q12 complements PMOS transistor Q13. N-P-N transistor Q14 provides the sinking current while n-p-n transistor Q10 provides the sourcing current.

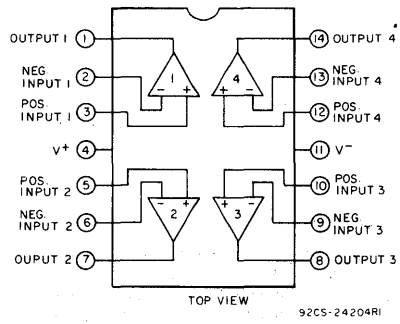


Fig. 3 - Functional diagram.

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS V^+ = 15 V, V^- = -15 V, T_A = 25°C		TYPICAL VALUES CA3410A	TYPICAL VALUES CA3410	UNITS
Input Resistance	R_I			1.5	1.5	TΩ
Input Capacitance	C_I			4	4	pF
Output Resistance	R_O			60	60	Ω
Equivalent Wideband Input Noise Voltage	e_n	BW = 140 kHz, R_S = 1 MΩ		48	48	μV
Equivalent Input Noise Voltage	e_n	f = 1 kHz	R_S =	40	40	nV/√Hz
		f = 10 kHz	100 Ω	30	30	
Short-Circuit Current to Opposite Supply						
Source	I_{OM}^+			35	35	mA
Sink	I_{OM}^-			17	17	
Gain-Bandwidth Product	f_T			5.4	5.4	MHz
Slew Rate	SR			10	10	V/μs
Transient Response:						
Rise Time:	t_r	R_L = 2 kΩ		0.08	0.08	μs
Overshoot		C_L = 100 pF		10	10	%
Crosstalk		f = 1 kHz		120	120	dB

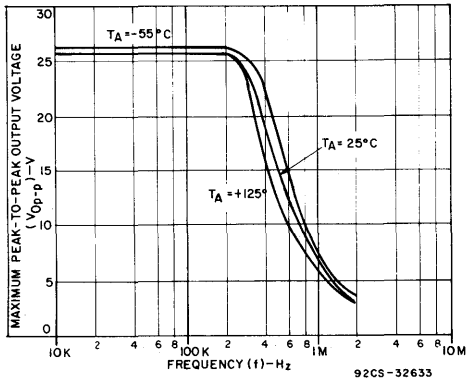


Fig. 4 - Output voltage as a function of frequency and temperature.

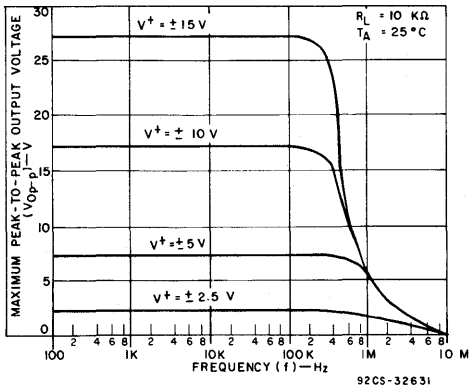


Fig. 5 - Output voltage as a function of frequency and supply voltage.

ELECTRICAL CHARACTERISTICS for Equipment Design at V^+ = 15 V, V^- = 15 V, T_A = -40 to 100°C Unless Otherwise Specified

CHARACTERISTIC		TYPICAL VALUES		UNITS
		CA3410A	CA3410	
Input Offset Voltage	V_{IO}	4	10	mV
Input Offset Current	I_{IO}	8	10	mA
Input Current	I_I	10	20	mA
Large-Signal Voltage Gain	A_{OL}	50 k	50 k	V/V
R_L = 2 kΩ	V_O = ± 10 V	94	94	dB
Common-Mode Rejection Ratio	CMRR	32	32	μV/V
		90	90	dB
Common-Mode Input-Voltage Range	V_{ICR}	-15 to +12.50	-15 to +12.50	V
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V$	150	150	μV/V
	PSRR	76	76	dB
Maximum Output Voltage	V_{OM}^+	13.50	13.50	V
R_L = 2 kΩ	V_{OM}^-	-10.50	-10.50	
Supply Current	I^+	9	10	mA
Total Device Dissipation	P_D	270	300	mW
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	10	12	μV/°C

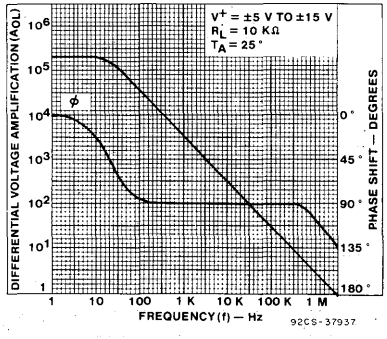


Fig. 6 - Differential voltage amplification as a function of frequency.

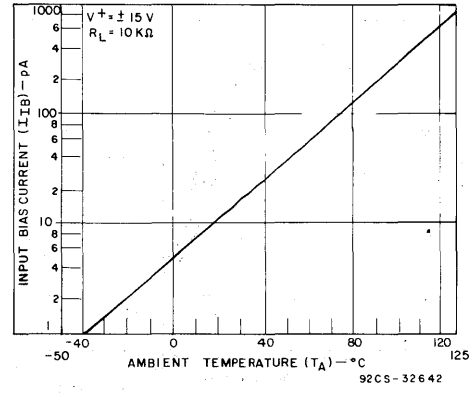


Fig. 7 - Input bias current as a function of ambient temperature.

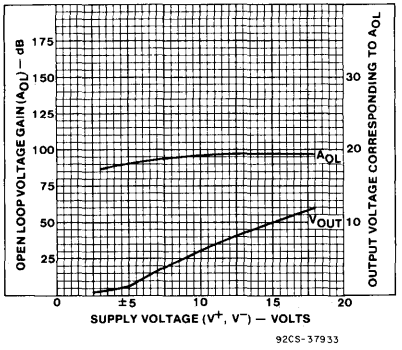


Fig. 8 - Open-loop voltage gain as a function of supply voltage and output voltage.

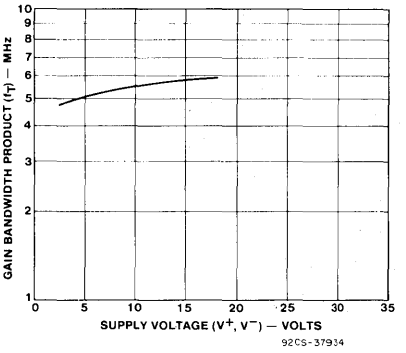


Fig. 9 - Gain-bandwidth product as a function of supply voltage.

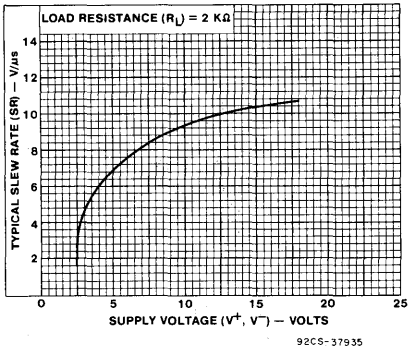


Fig. 10 - Slew rate as a function of supply voltage.

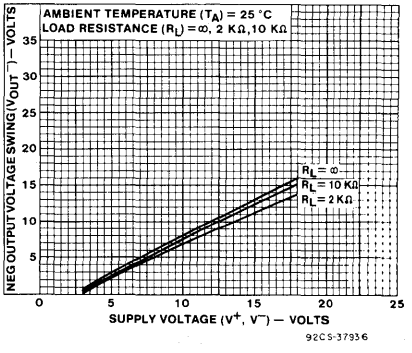


Fig. 11 - Negative output voltage swing as a function of supply voltage.

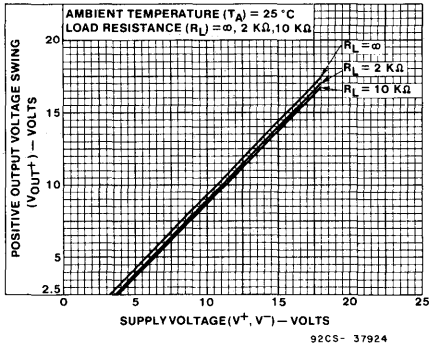


Fig. 12 - Positive output voltage swing as a function of supply voltage.

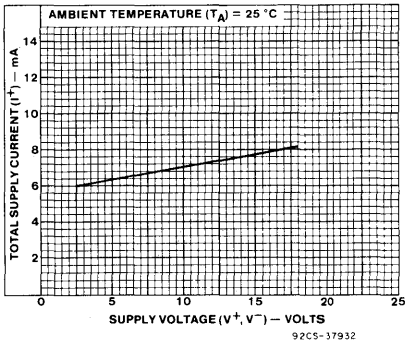


Fig. 13 - Total supply current as a function of supply voltage.

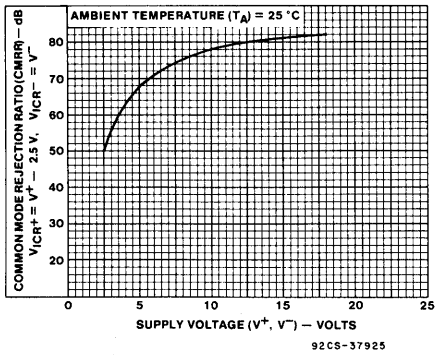


Fig. 14 - Typical common-mode rejection ratio as a function of supply voltage.

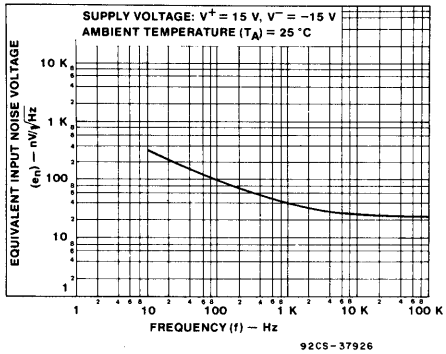


Fig. 15 - Equivalent input noise voltage as a function of frequency.

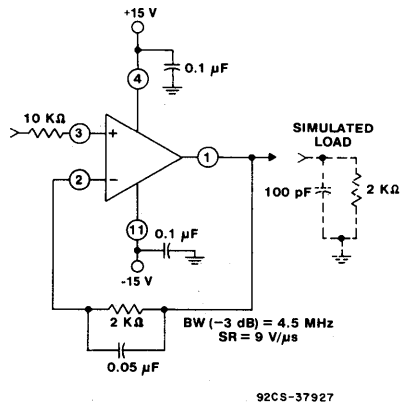


Fig. 16 - Split-supply voltage-follower test circuit.

APPLICATIONS CONSIDERATIONS

Input Circuit Considerations

As indicated by the typical VICR, this device will accept inputs as low as V^-. However, a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3410 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current.

It is well known that MOSFET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage.

TYPICAL APPLICATIONS

On/Off Touch Switch

The on/off touch switch shown in Fig. 18 uses the CA3410E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the "on" plate is touched, current flows between the two halves of the grid causing a positive shift in the output voltage (Term. 7) of the CA3410E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero-crossing triac driver. When a positive pulse occurs at Terminal 7 of the CA3410E, triac is turned on and held on by the CA3059 and its associated positive feedback circuitry (51-kΩ resistor and 36-kΩ/42-kΩ voltage divider). When the positive pulse occurs at Terminal 1 (CA3410E), the triac is turned off and held off in a similar manner. Note that power for the CA3410E is supplied by the CA3059 internal power supply.

The advantage of using the CA3410E in this circuit is that it can sense the small currents associated with skin conduction while allowing sufficiently high circuit impedance to provide protection against electrical shock.

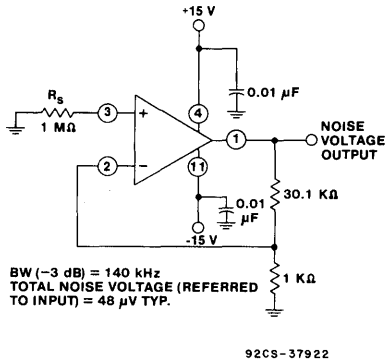


Fig. 17 - Test-circuit amplifier (30-dB gain) used for wideband noise measurement.

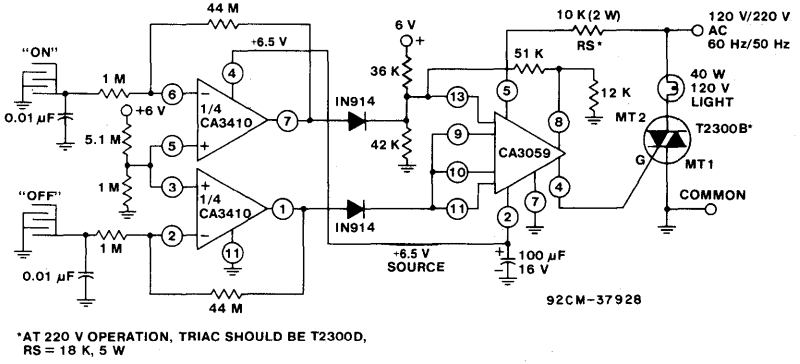


Fig. 18 - On/off touch switch.

Dual Level Detector (window comparator)

Fig. 19 illustrates a simple dual liquid level detector using the CA3410E as the sensing amplifier. This circuit operates on the principle that most liquids contain enough ions in solution to sustain a small amount of current flow between two electrodes submersed in the liquid. The current, induced by an 0.5-V potential applied between two halves of a PC board grid, is converted to a voltage level by the CA3410E in a circuit similar to that of the on/off touch switch shown in Fig. 18. The changes in voltage for both the upper and lower level sensors are processed by the amp 3 of their CA3410 to activate an LED whenever the liquid level is above the upper sensor or below the lower sensor.

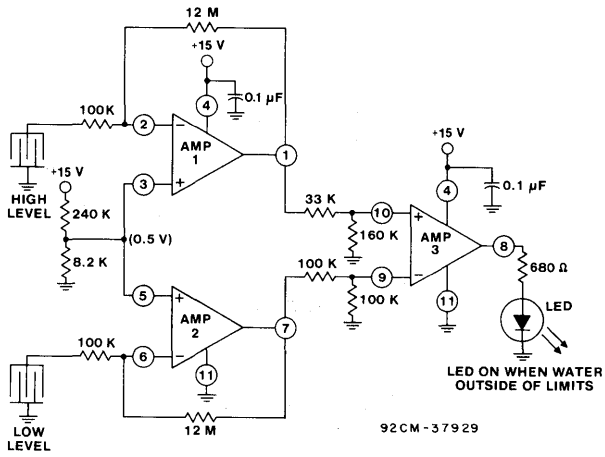


Fig. 19 - Dual level detector.

Precision Differential Amplifier

Fig. 20 shows the CA3410 in the classical precision differential amplifier circuit. The CA3410 is ideally suited for biomedical applications because of its extremely high input impedance. To insure patient safety, an extremely high electrode series resistance is required to limit any current that might result in patient discomfort in the event of a fault condition. In this case, 10-MΩ resistors have been used to limit the current to less than 2 μA without affecting the performance of the circuit. Fig. 21 shows a typical electrocardiogram waveform obtained with this circuit.

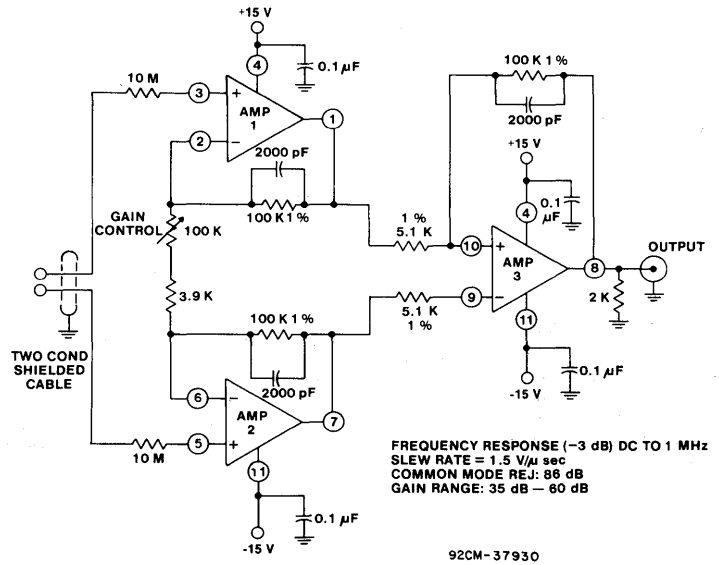
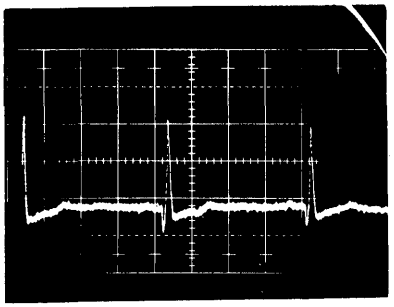


Fig. 20 - Precision differential amplifier.



VERTICAL : 1.0 mV/ DIV.
(AMPLIFIER GAIN = 100 X)
(SCOPE SENSITIVITY = 0.1V/DIV.

HORIZONTAL : > 0.2 SEC/DIV (UNCAL)

92CS-30033

TYPICAL ELECTROCARDIOGRAM WAVEFORM

Fig. 21 - Typical electrocardiogram waveform.

Differential Light Detector

In the circuit shown in Fig. 22, the CA3410E converts the current from two photo diodes to voltage, and applies 1 V of reverse bias to the diodes. The voltages from the CA3410 outputs are subtracted in the second stage (Amp 3) so that only the difference is amplified. In this manner, the circuit can be used over a wide range of ambient light conditions without circuit component adjustment. Also, when used with a light source, the circuit will not be sensitive to changes in light level as the source ages.

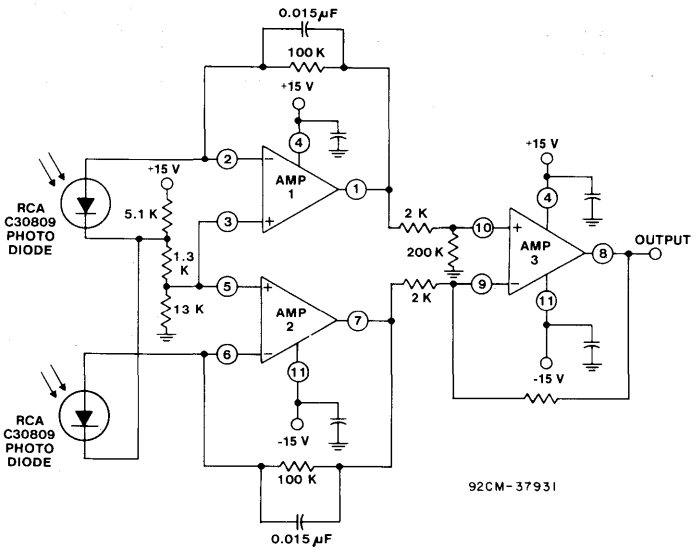


Fig. 22 - Differential light detector.

May 1990

Low-Supply Voltage, Low-Input Current BiMOS Operational Amplifiers

Features:

- *2 V supply at 300 μA supply current*
- *1 pA (typ.) input current (essentially constant to 85°C)*
- *Rail-to-rail output swing (Drive ±2 mA into 1 kΩ load)*
- *Pin compatible with 741 op amp*

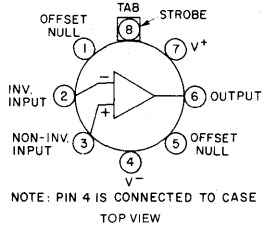
Applications:

- *pH probe amplifiers*
- *Picoammeters*
- *Electrometer (High Z) instruments*
- *Portable equipment*
- *Inaccessible field equipment*
- *Battery-dependent equipment (medical and military)*

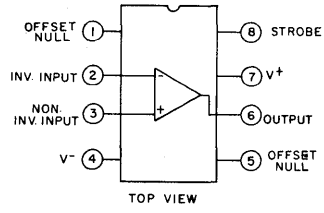
The CA3420A and CA3420* are integrated-circuit operational amplifiers that combine PMOS transistors and bipolar transistors on a single monolithic chip. The CA3420A and CA3420 BiMOS operational amplifiers feature gate-protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1 pA). The internal bootstrapping network features a unique guardbanding technique for reducing the doubling of leakage current for every 10°C increase in temperature. The CA3420 series operates at total supply voltages from 2 to 20 volts either single or dual supply. These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Additionally, they have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminal are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.45 volt below the negative supply terminal, an important attribute for single-supply application. The output stage uses a feedback OTA type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.5 mA (min) is provided by using non-linear current mirrors.

The CA3420 series has the same 8-lead pin-out used for the industry standard 741. They are supplied in the standard 8-lead TO-5 style package (S suffix, and T suffix); in the standard 8-lead dual-in-line plastic package (Minidip - E suffix), and are also available in chip form (H suffix).

*Formerly Dev. Type No. TA10841



S AND T SUFFIXES



E SUFFIX

Functional diagrams for CA3420A, CA3420.

MAXIMUM RATINGS, *Absolute-Maximum Values (T_C=25° C):*

DC Supply Voltage
(Between V^+ and V^- Terminals) ..... 22 V
Differntial-Mode
Input Voltage ..... ±15 V
Common-Mode DC
Input Voltage ..... (V^+ + 8 V) to (V^- -0.5 V)
Input-Terminal Current .....1 mA
Device Dissipation:
Without Heat Sink —
Up to 55° C..... 630 mW
Above 55° C.....Derate linearly 6.67 mW/° C
With Heat Sink -
Up to 110° C ..... 630 mW
Above 110° C..... Derate linearly 16.7 mW° C

Temperature Range:
Operating (All Types)..... -55 to +125° C
Storage (All Types)..... -65 to +150° C
Output Short-Circuit
Duration*.....Indefinite
Lead Temperature
(During Soldering):
At Distance 1/16 ± 1/32 Inch
(1.59 ± 0.79 mm) from case
For 10 seconds max..... +265° C

*Short circuit may be applied to ground or to either supply.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

Characteristic		Test Conditions V+ = +10V; V- = -10V TA = 25° C		CA3420A (T,S,E)	CA3420 (T,S,E)	Units
Input Resistance	R_I			150	150	TΩ
Input Capacitance	C_I			4.9	4.9	pF
Output Resistance	R_O			300	300	Ω
Equivalent Input		f = 1 KHz	R_S 100 Ω	62	62	
	e_n					nV/ Hz
Noise Voltage		f = 10 KHz		38	38	
Short-Circuit Current Source						
Source IOM+				2.6	2.6	mA
To Opposite Supply						
Sink IOM-				2.4	2.4	mA
Gain-Bandwidth Product	f_T			0.5	0.5	MHz
Slew Rate	SR			0.5	0.5	V/μs
Transient Response						
Rise Time tr		R_L = 2 K Ω		0.7	0.7	μs
Overshoot		C_L = 100 pF		15	15	%
Current from Terminal 8						
To V-	I_8+			20	20	μA
Current from Terminal 8						
To V+	I_8-			2	2	mA

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V+ = 1V, V- = -1V, TA = 25°C unless otherwise specified

Characteristic	Limits						Units
	CA3420A			CA3420			
	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $\|V_{IO}\|$	—	2	5	—	5	10	mV
Input Offset Current $\|I_{IO}\|$ *	—	0.01	4	—	0.01	4	pA
Input Current $\|I_I\|$ *	—	0.02	5	—	1	5	pA
Large-Signal Voltage Gain	20K	100K	—	10K	100K	—	V/V
AOL (R_L = 10 KΩ)	86	100	—	80	100	—	dB
Common-Mode	—	560	1000		560	1800	μV/V
Rejection Ratio CMRR	60	65	—	55	65	—	dB
Common-Mode Input VICR +	+0.2	+0.5	—	+0.2	+0.5	—	V
Voltage Range VICR -	-1	-1.3	—		-1.3	—	V
Power Supply Rejection	—	32	320	—	100	1000	μV/V
Ratio PSRR ΔVIO/ΔV	70	90	—	60	80	—	dB
Max Output Voltage VOM +	+0.90	+0.95	—	+0.90	+0.95	—	V
RL = 00 VOM -	-0.85	-0.91	—	-0.85	-0.91	—	V
Supply Current I+	—	350	650	—	350	650	μA
Device Dissipation P_D	—	0.7	1.1	—	0.7	1.1	mW
Input Offset Voltage Temp. Drift ΔVIO/ΔT	—	4	—	—	4	—	μV/°C

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V+ = 10V, V- = -10V, TA = 25°C unless otherwise specified

Characteristic	Limits						Units
	CA3420A			CA3420			
	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage $\|V_{IO}\|$	—	2	5	—	5	10	mV
Input Offset Current $\|I_{IO}\|$ *	—	0.03	4	—	0.03	4	pA
Input Current $\|I_I\|$ *	—	0.05	5	—	0.05	5	pA
Large-Signal Voltage Gain	20K	100K	—	10K	100K	—	V/V
AQL (R_L = 10K Ω)	86	100	—	80	100	—	dB
Common-Mode	—	100	320	—	100	320	μV/V
Rejection Ratio CMRR	70	80	—	70	80	—	dB
Common-Mode Input VICR +	+9.0	+9.3	—	+8.5	+9.3	—	V
Voltage Range VICR -	-10	-10.3	—	-10	-10.3	—	V
Power Supply Rejection	—	32	320	—	32	320	μV/V
Ratio PSRR ΔVIO/ΔV	70	90	—	70	90	—	dB
Max Output Voltage VOM +	+9.7	+9.9	—	+9.7	+9.9	—	V
RL = 00 VOM -	-9.7	-9.85	—	-9.7	-9.85	—	V
Supply Current I+	—	450	1000	—	450	1000	μA
Device Dissipation P_D	—	9	14	—	9	14	mW
Input Offset Voltage Temp. Drift ΔVIO/ΔT	—	4	—	—	4	—	μV/°C

* The maximum limit represents the levels obtainable on high speed automatic test equipment. Typical values are obtained under laboratory conditions.

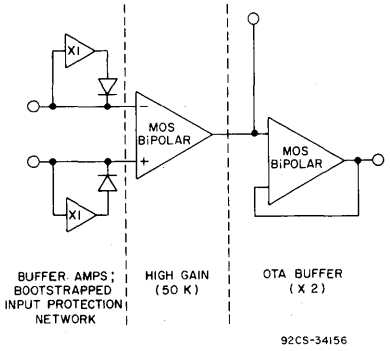


Fig. 1 - Functional diagram for CA3420.

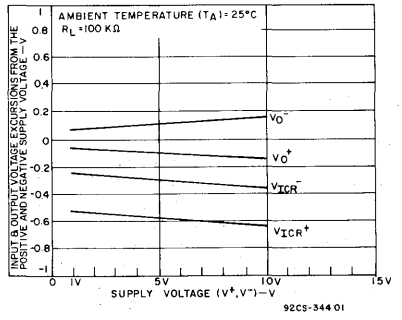


Fig. 2 - Output-voltage-swing and common-mode input-voltage range versus supply voltage.

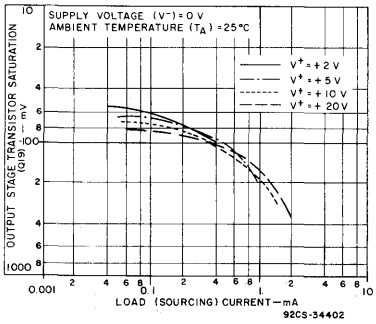


Fig. 3 - Output voltage versus load sourcing current.

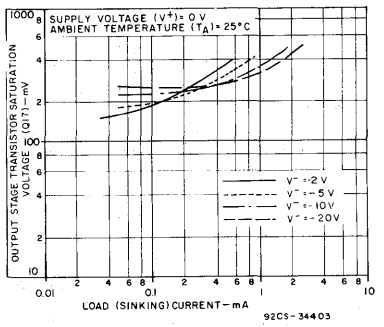


Fig. 4 - Output voltage versus load sinking current.

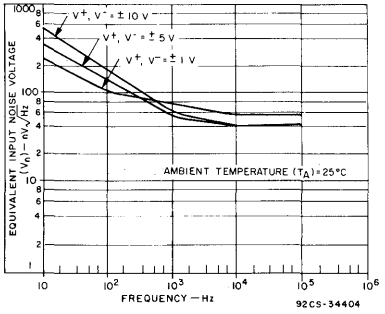


Fig. 5 - Input noise voltage versus frequency.

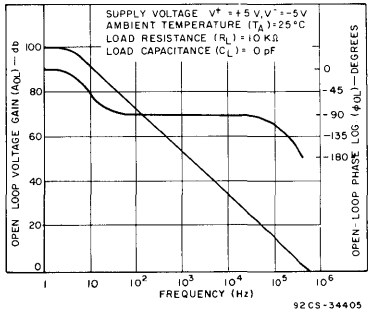


Fig. 6 - Open-loop gain and phase-shift response.

Application Circuits

Picoameter Circuit

The exceptionally low input current (typically 0.2 pA) makes the CA3420 highly suited for use in a picoameter circuit. With only a single 10K megohm resistor, this circuit covers the range from ±1.5 pA. Higher current ranges are possible with suitable switching techniques and current scaling resistors. Input transient protection is provided by the 1-megohm resistor in series with the input. Higher current ranges require that this resistor be reduced. The 10-megohm resistor connected to pin 2 of the CA3420 decouples the potentially high input capacitance often associated with lower current circuits and reduces the tendency for the circuit to oscillate under these conditions.

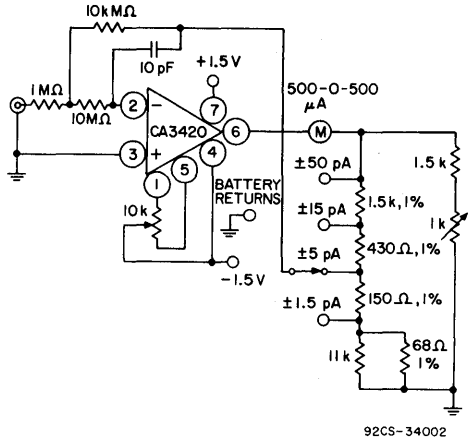


Fig. 7 - Picoameter circuit.

High-Input-Resistance Voltmeter

Advantage is taken of the high input impedance of the CA3420 in a high-input-resistance dc voltmeter. Only two 1.5 V "AA" type penlite batteries power this exceedingly high-input resistance (>1,000,000-megohms) dc voltmeter. Full-scale deflection is ±500 mV, ±150 mV, and ±15 mV. Higher voltage ranges are easily added with external input voltage attenuator networks.

The meter is placed in series with the gain network, thus eliminating the meter temperature coefficient error term.

Supply current in the standby position with the meter undeflected is 300 μA. At full-scale deflection this current rises to 800 μA. Carbon-zinc battery life should be in excess of 1,000 hours.

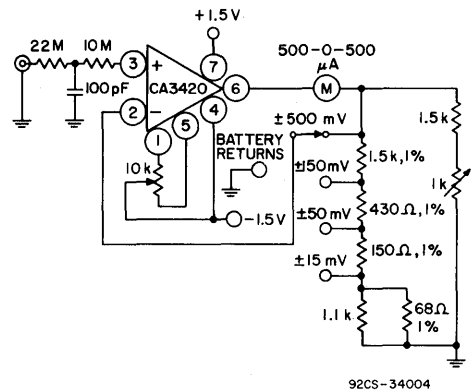


Fig. 8 - High input resistance voltmeter.

May 1990

Nanopower BiMOS Operational Amp

Features:

- *300 nW (typ.) standby power at V+ = 5 V*
- *Supply current, BW, slew rate programmable using external resistor*
- *10 pA (typ.) input current*
- *5 to 15 V supply*
- *Output drives typical bipolar-type loads*
- *Low cost 8-lead Mini-DIP, TO-5*

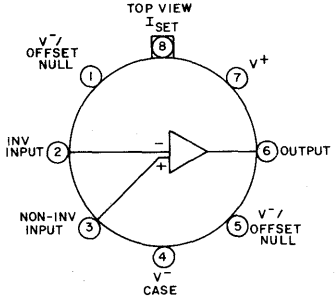
The CA3440A and CA3440* are integrated circuit operational amplifiers that combine the advantages of MOS and bipolar transistors on a single monolithic chip.

The CA3440A and CA3440 BiMOS op amps feature gate-protected PMOS transistors in the input circuit to provide very high input impedance and very low input current (10 pA). These devices operate at total supply voltage from 5 to 15 volts and can be operated over the temperature range from -55°C to +125°C. Their virtues are programmability and very low standby power consumption (300 nW). These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.5 volt below the negative supply terminals, an important attribute for single supply applications. The output stage uses MOS complementary source follower form which permits moderate load driving capability (10 KΩ) at very low total standby currents (50 nA).

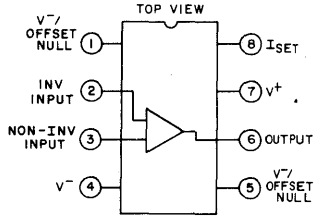
The CA3440A and CA3440 have the same 8-lead terminal pin-out used for "741" and other industry standard op amps with two exceptions: terminals one and five must be connected to the negative supply or to a potentiometer if nulling is required. Terminal 8 must be programmed through an external resistor returned to the negative supply.

These devices are supplied in either the standard 8-lead TO-5 style package (T suffix), 8-lead dual-in-line formed-lead TO-5 style "DIL-CAN" package (S suffix), or in the 8-lead dual-in-line plastic package "Mini-DIP" (E suffix). They are also available in chip form (H suffix).

*Formerly Dev. Type No. TA10590.



S AND T SUFFIXES



E SUFFIX

Functional diagrams for CA3440A and CA3440.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE
(BETWEEN V^+ AND V^- TERMINALS) ..... 25 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±9 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK —
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate linearly 6.67 mW/°C
WITH HEAT SINK —
AT 125°C ..... 418 mW
BELOW 125°C ..... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
OPERATING ..... −55 to +125°C
STORAGE ..... −65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 IN. (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX. ..... +265°C

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC	TEST CONDITIONS V^+=+5 V; V^-=-5 V R_{SET}=10 MΩ; T_A=25°C		CA3440A	CA3440	UNITS
Input Resistance, R_I			2	2	TΩ
Input Capacitance, C_T			3.5	3.5	pF
Ouput Resistance, R_O			450	450	Ω
Equivalent Input Noise Voltage, e_n	f= 1 kHz	R_S=100 Ω	110	110	nV/√Hz
	f=10 kHz		110	110	
Short-Circuit Current Source IOM+			15	15	mA
To Opposite Supply Sink IOM−			4.5	4.5	
Gain-Bandwidth Product, f_T			63	63	kHz
Slew Rate, SR			0.03	0.03	V/μs
Transient Response Rise Time, t_r	R_L= 10 kΩ		5.6	5.6	μs
Overshoot	C_L=100 pF		10	10	%

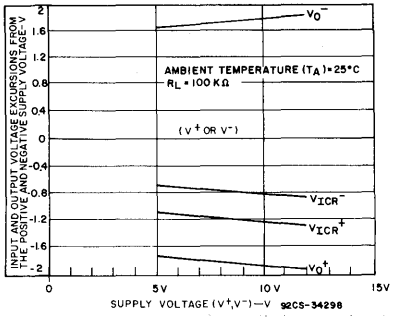


Fig. 1 - Output-voltage-swing and common-mode input-voltage range versus supply voltage.

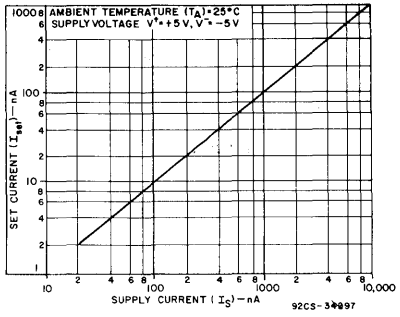


Fig. 2 - Set current versus supply current.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At V^+ = +5 V, V^- = -5 V, T_A = 25°C Unless Otherwise Specified, R_{SET}=10 MΩ

CHARACTERISTIC	LIMITS						UNITS
	CA3440A			CA3440			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	2	5	—	5	10	mV
Input Offset Current, $\|I_{IO}\|$	—	2.5	20	—	2.5	30	pA
Input Current, $\|I_I\|$	—	10	40	—	10	50	pA
Large-Signal Voltage Gain, AOL	10K	100K	—	10K	100K	—	V/V
(R_L=10 KΩ)	80	100	—	80	100	—	dB
Common-Mode	—	100	320	—	100	320	μV/V
Rejection Ratio, CMRR	70	80	—	70	80	—	dB
Common-Mode Input $VICR^+$	+3.5	+3.7	—	+3.5	+3.7	—	V
Voltage Range, $VICR^-$	−5.0	−5.3	—	−5.0	−5.3	—	V
Power Supply Rejection Ratio, $\Delta VIO/\Delta V$	—	32	320	—	32	320	μV/V
PSRR	70	90	—	70	90	—	dB
Maximum Output Voltage, VOM^+	+3	+3.2	—	+3	+3.2	—	V
VOM^-	−3	−3.2	—	−3	−3.2	—	V
Supply Current, I^+	—	10	17	—	10	17	μA
Device Dissipation, P_D	—	100	170	—	100	170	μW
Input Offset Voltage Temperature Drift, $\Delta VIO/\Delta T$	—	4	—	—	4	—	μV/°C

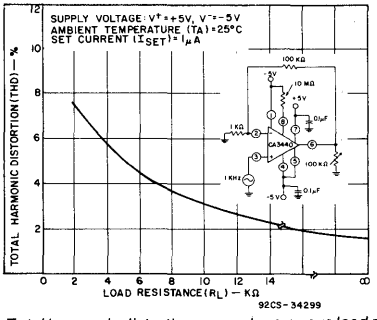


Fig. 3 - Total harmonic distortion percentage versus load resistance.

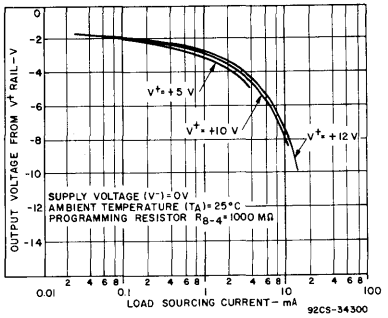


Fig. 4 - Output voltage versus sourcing load current.

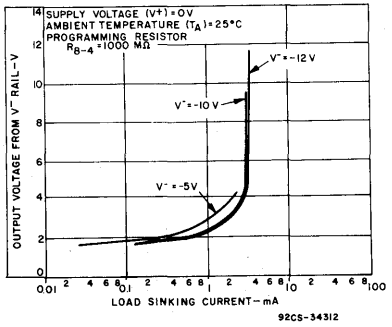


Fig. 5 - Output voltage versus sinking load current.

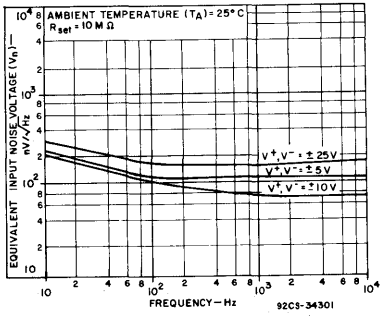


Fig. 6 - Input noise voltage versus frequency.

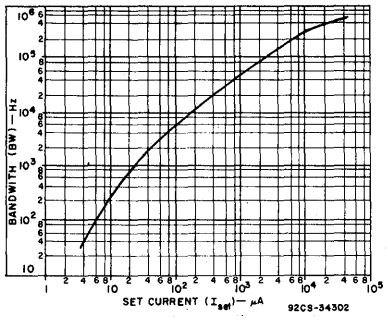


Fig. 7 - Bandwidth versus set current.

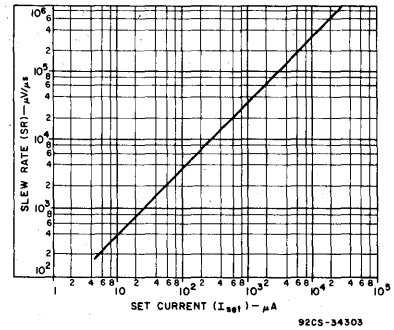


Fig. 8 - Slew rate versus set current.

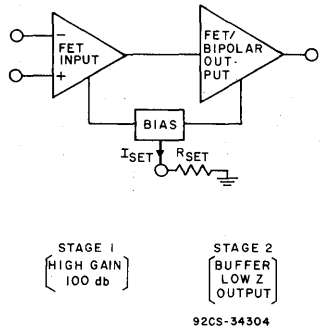


Fig. 9 - Nanopower op amp (supply current programmable using R_{SET}) 1-pA typical input bias current, 4.0 to 15-volt supply.

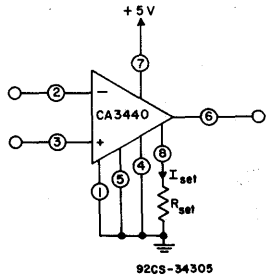


Fig. 10 - Nanopower op amp (usable standby power versus programming resistor R_{SET}).

As R_{SET} is increased, I_{SET} and the standby power decrease while the BW/SR also decreases.

Operating at a +5 V single supply, the CA3440 exhibits the following characteristics:

R_{SET}	Standby Power	BW	SR
1 MΩ	250 μW	164 kHz	0.17 V/μs
10 MΩ	25 μW	27 kHz	0.017 V/μs
100 MΩ	2.5 μW	2.6 kHz	.0017 V/μs
1000 MΩ	250 nW	78 Hz	0.00017 V/μs

The CA3440 is pin-compatible with the 741 except that pins 1 and 5 (typical negative nulling pins) must be connected either directly to pin 4 or to a negative nulling potentiometer. In addition, pin 8, the I_{SET} terminal, must be returned to either ground or −V via R_{SET}.

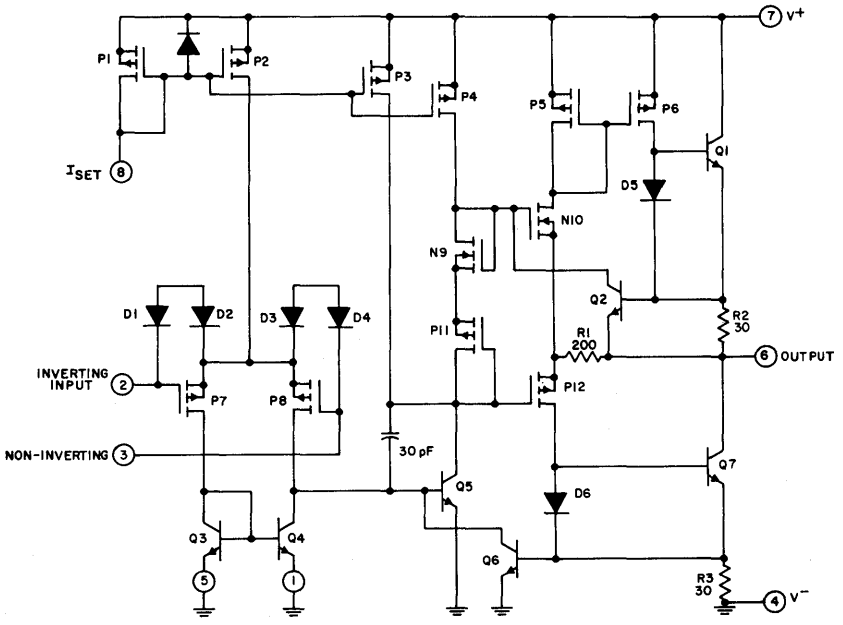


Fig. 11 - Schematic diagram for CA3440.

APPLICATIONS CIRCUITS

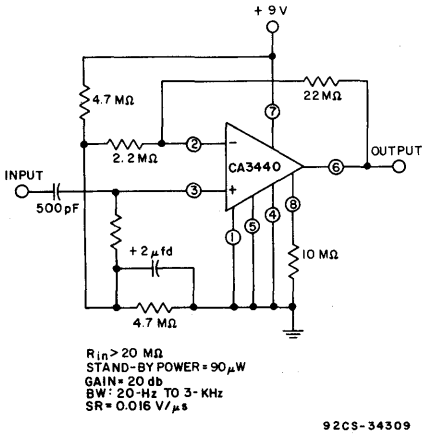


Fig. 12 - High-input impedance amplifier.

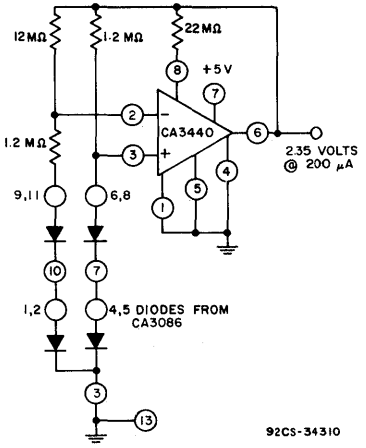


Fig. 13 - Micropower bandgap reference.

May 1990

Video Line Driver, High-Speed Operational Amplifiers

Features:

- *High open loop gain at video frequencies: A_{OL} = > 40 dB at f = 5 MHz*
- *Power bandwidth of 10 MHz; $A_{Closed\ Loop}$ = 5; V_O = ±3.5 V*
- *Slew rate of 330 V/μsec ($A_V \geq 10$) at full load*
- *f_T = 220 MHz; C_C = 5pF with a load of 50 ohm || 20 pF || 1 MΩ (scope input)*
- *V_{OUT} = ±4.1 V into 75 Ω*
- *Offset null terminals*

Applications:

- *Video line driver*
- *High-frequency unity gain buffer*
- *Pulse amplifier*
- *High-speed comparator*
- *High-frequency oscillator and video amplifiers*
- *Driver for A/Ds in video applications: 10 MHz BW*

The CA3450* is a large signal video line driver and high speed operational amplifier capable of driving 50 ohm transmission lines and flash A/Ds. The uncompensated unity gain crossing occurs at 230 MHz without load. It can operate dual or single supplies of ±7.25 V or 14.5 V, respectively. The CA3450 can be compensated with a single capacitor network. It has output drive capability of 75 mA SINK or SOURCE. The CA3450 is capable of driving Flash A/D's in video or high-speed instrumentation (accurate) applications with bandwidth up to 10 MHz. Offset voltage nulling terminals are also available.

The CA3450 is available in a 16-lead dual-in-line plastic package (E suffix).

*Formerly RCA Development Type No. TA11371A.

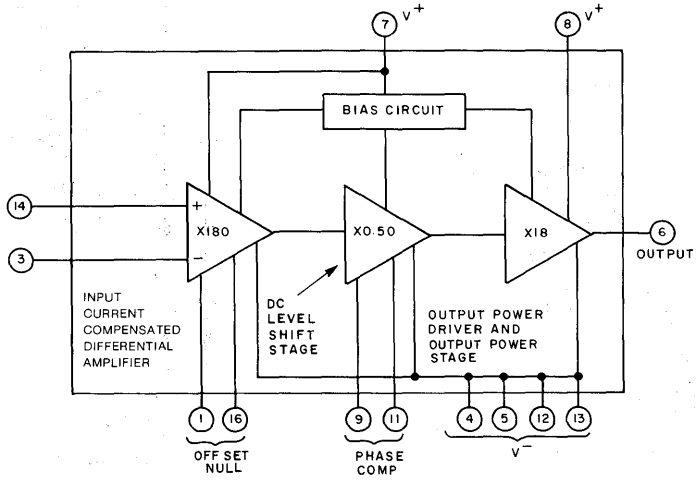
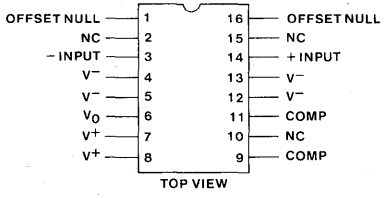


Figure 1 - Block diagram of the CA3450.

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE (BETWEEN V+ AND V- TERMINAL) ..... 14.5 V
DIFFERENTIAL INPUT VOLTAGE ..... ±5 V
DEVICE DISSIPATION:
  Up to 55°C ..... 1.5 W
  Above 55°C ..... Derate linearly at 16.6 mW/°C
OUTPUT CURRENT (SINK OR SOURCE) ..... 100 mA
TEMPERATURE RANGE
  Operating ..... -40°C to 85°C
  Storage ..... -55°C to 150°C
MAXIMUM JUNCTION TEMPERATURE ..... 150°C
MAXIMUM THERMAL RESISTANCE
  Junction to Air (θJ-A) ..... 60°C/W
  Junction to Case (θJ-C) ..... 12°C/W
  To pins 4, 5, 12, 13 at seat



TERMINAL ASSIGNMENT

ELECTRICAL CHARACTERISTICS, *At T_A = 25°C, C_C = 5 pF, V+, V- = 6 V**

CHARACTERISTICS	CONDITIONS		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
STATIC						
Input Offset Voltage, $\|V_{IO}\|$	T_A = 25°C		—	8	20	mV
	T_A = -40°C to 85°C		—	10	35	
Input Bias Current, $\|I_{IB}\|$	T_A = 25°C		—	100	400	nA
Input Offset Current, $\|I_{IO}\|$	T_A = 25°C		—	50	200	
Open Loop DC Gain, A_{OL}	V_{OUT} = ±2.5 V; R_L = 50 Ω	-40°C to 85°C	55	—	—	dB
		25°C	60	70	—	
Power Supply Rejection Ratio, P_{SRR}	ΔV = ±1 V		55	65	—	
Common-Mode Rejection Ratio, C_{MRR}	V_{ICR}± = ±3.5 V		50	60	—	
Common-Mode Input Range, V_{ICR}	T_A = -40°C to 85°C		±3.0	—	—	V
	T_A = 25°C		±3.5	±3.7	—	
Supply current, I	T_A = -40°C to 85°C		—	—	50	mA
	T_A = 25°C		—	30	40	

*All test are performed with ± 6 volts at the terminals of the device.

A 10 ohm, ¼ watt supply decoupling resistor is shown in all application circuits of this device. The resistor serves two purpose, first provides a means of decoupling the IC directly at its terminal without introducing additional supply resonance due to parallel connected capacitors. Secondly, it also provides protection for the device in event of a substained short circuit applied directly to the output terminals.

ELECTRICAL CHARACTERISTICS, *At T_A = 25°C, C_C = 5 pF, V+, V- = 6 V**

CHARACTERISTICS	CONDITIONS		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
DYNAMIC						
-3 dB Bandwidth	No Load		—	200	—	MHz
A_V = 1 (See Figure 3)	R_L = 1 MΩ‖20 pF		—	190	—	
C_C = 5 pF	R_L = 50 Ohms‖20 pF		—	185	—	
Bandwidth (Unity Gain Crossing)	No Load		210	230	—	
A_V = Open Loop	R_L = 20 pF‖1 MΩ		180	200	—	
C_C = 0 (See Figure 2)	R_L = 50 Ohms‖20 pF		180	220	—	
Bandwidth (Unity Gain Crossing)	No Load		200	210	—	
$A_V \geq 10$, C_C = 0 pF	50 Ω		175	190	—	
$R_{Feedback}$ = 450 Ω	1 M‖20 pF		180	195	—	
$R_{Pin\ 3-G}$ = 50 Ω (See Figure 3)	50 Ω‖1 M‖20 pF		170	188	—	
Transient Response, Overshoot	A_V = 1, C_C = 5 pF	R_L = 50 Ω‖20 pF	—	30	—	%
		No Load	—	20	—	
	$A_V \geq 10$, C_C = 0 pF, R_L = 50 Ω‖20 pF		—	10	—	
Settling Time	2 Volt Step	A_V = -1, C_C = 5 pF, 0.1%, 10 Bits	—	35	—	ns
(See Figure 6)	R_L = 50 Ω‖20 pF	A_V = 1, C_C = 5 pF, 0.1%, 10 Bits	—	50	—	
		A_V = 10, C_C = 0 pF, 0.1%, 10 Bits	—	35	—	
		A_V = 10, C_C = 0 pF, 1.0%, 7 Bits	—	25	—	
Slew Rate, SR	A_V = 1, C_C = 5 pF	No Load	—	220	—	V/μs
(See Figure 3)		R_L = 50 Ω‖20 pF	—	160	—	
	$A_V \geq 10$, C_C = 0 pF	No Load	370	440	—	
		R_L = 50 Ω‖20 pF	300	330	—	
Power Bandwidth PBW (MHz)	A_V = 5, C_C = 5 pF	No Load	—	10	—	MHz
PBW = SR/Ω Vpp	V_{OUT} = ±3.5 V	R_L = 50 Ω‖20 pF	—	7.2	—	
	A_V > 10, C_C = 0 pF	No Load	29	35	—	
	V_{OUT} = ±2.0 V	R_L = 50 Ω‖20 pF	24	26	—	
Input Noise Voltage e_n	f = 1 KHz		—	12	—	$nV/\sqrt{Hz}$
Differential Gain	See Figure 15		—	0.6	—	%
Differential Phase			—	0.3	—	Degrees
I_{OUT}	Into +4 V or -4 V		60	75	60	mA
Output Voltage Swing into 75 Ohms	V_{OM}+		3.9	+4.1	—	V
	V_{OM}-		-3.9	-4.1	—	
Input Capacitance, C_I	f = 1 MHz		—	2.2	—	pF
Input Resistance, R_I			—	1	—	MΩ
Output Resistance, R_{OUT}	See Figure 13, A = 1, 30 MHz		—	4	—	Ω

*All test are performed with ±6 volts at the terminals of the device.

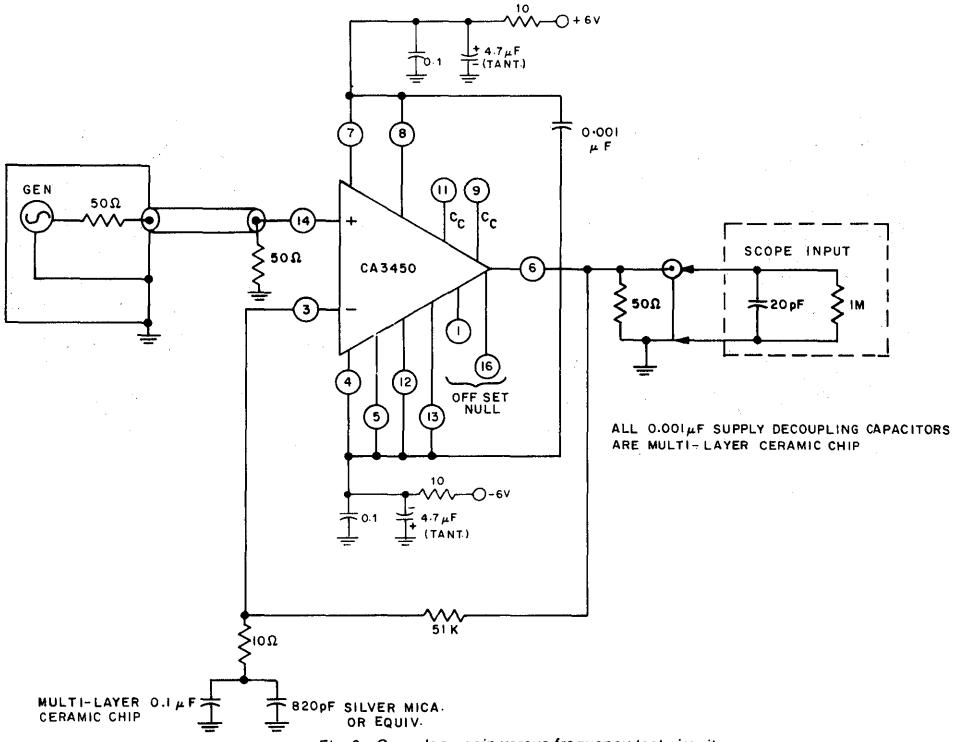


Fig. 2 - Open-loop gain versus frequency test circuit.

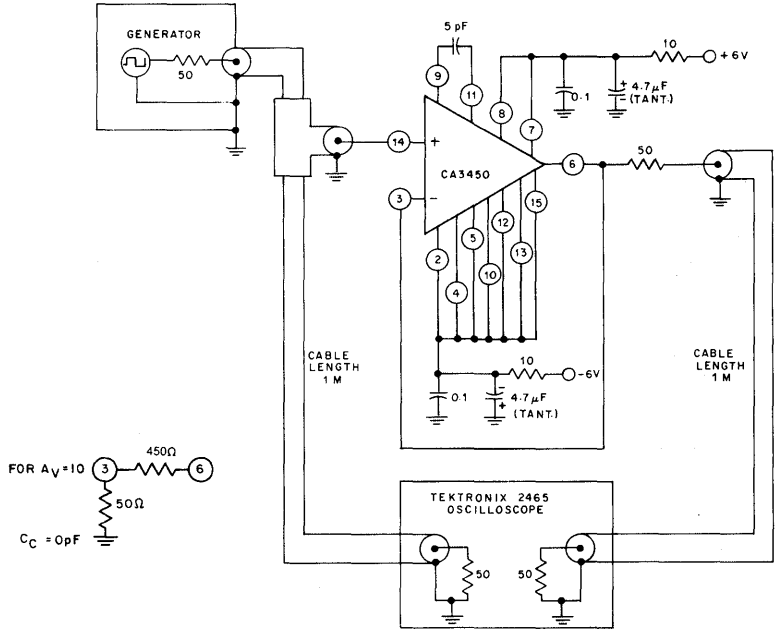


Fig. 3 - Unity-gain and X10 non-inverting amplifier/and slew rate test circuit.

Transient Response Waveforms

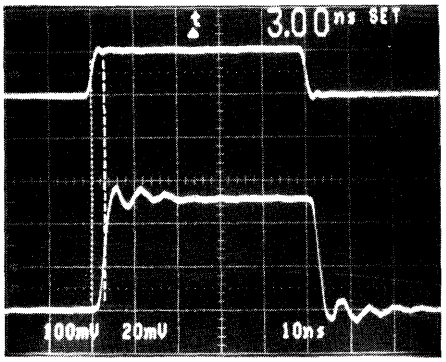


Figure 4 - Transient-response waveform.

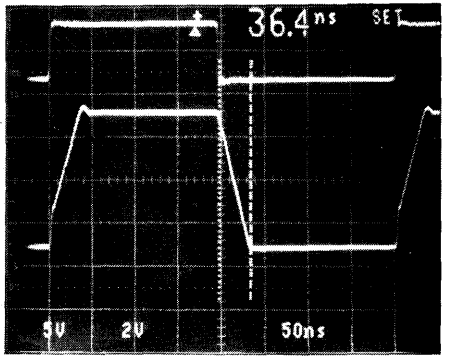


Figure 5 - Slew-rate waveform.

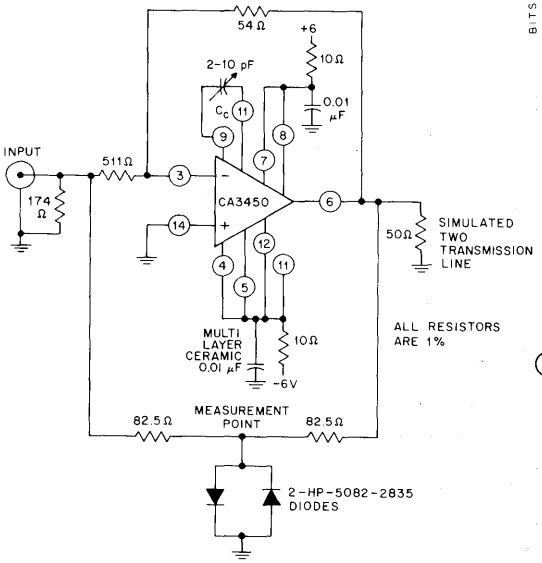


Figure 6 - Circuit used to measure settling time.

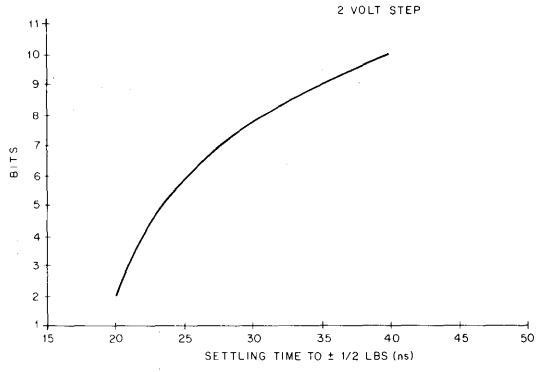


Figure 7 - Accuracy in bits as a function of settling time.

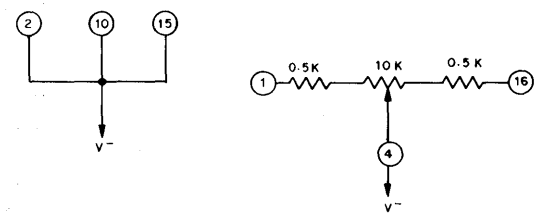


Figure 8 - Nulling circuit for the CA3450.

Typical Performance Curves

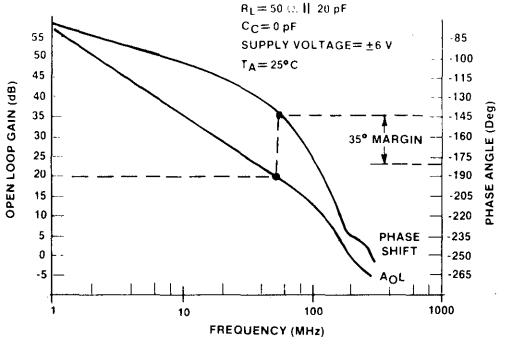


Figure 9 -Bode plot for the CA3450.

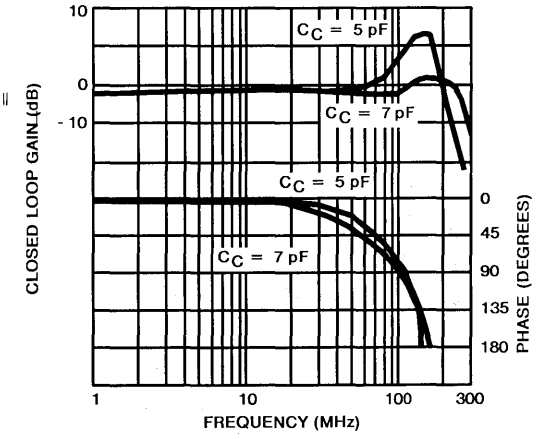


Figure 10 - Closed loop gain and phase vs frequency. (A_V = 1)

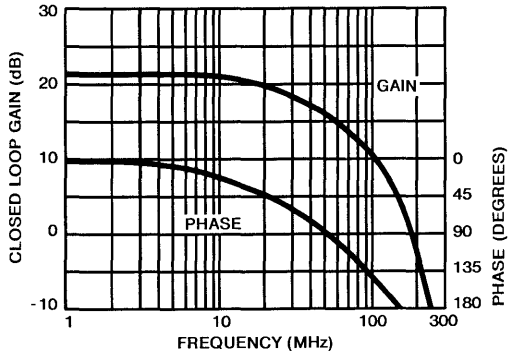


Figure 11 - Closed loop gain and phase vs frequency. (A_V = 10)

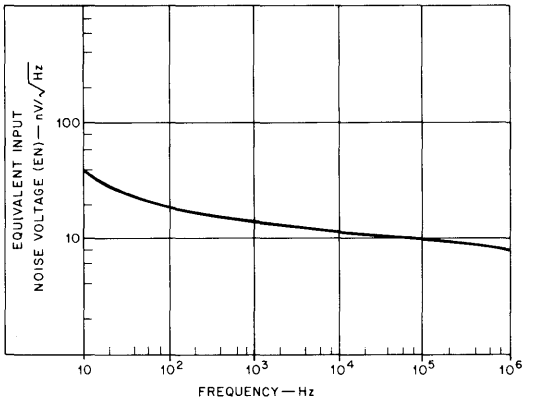


Figure 12 - Curve showing the equivalent input noise "e_n" of the op amp.

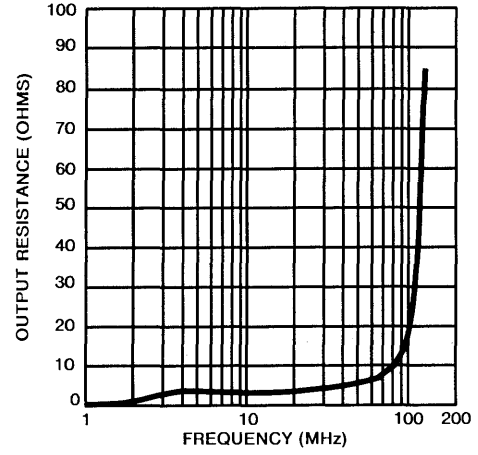


Figure 13 - Output resistance vs frequency.

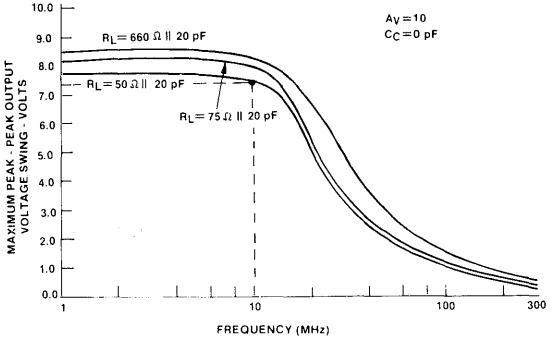


Figure 14 - Output voltage as a function of frequency for the CA3450 under various loads.

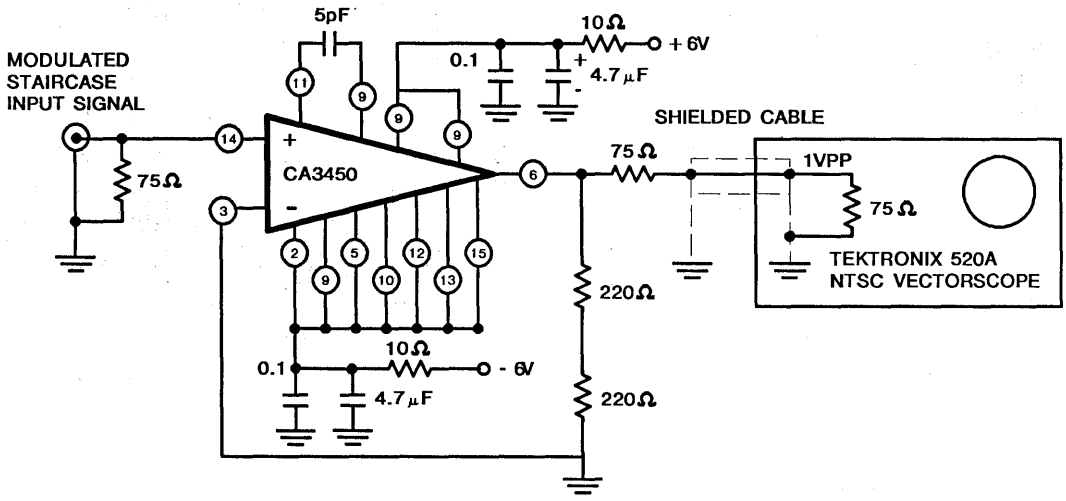


Figure 15 - Configuration used to measure differential gain and phase.

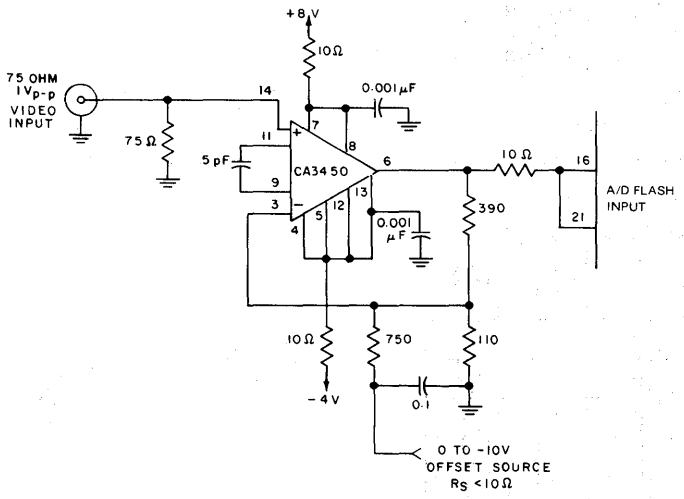


Figure 16 - Typical high-bandwidth X5 amplifier for driving the CA3318 Flash A/D.

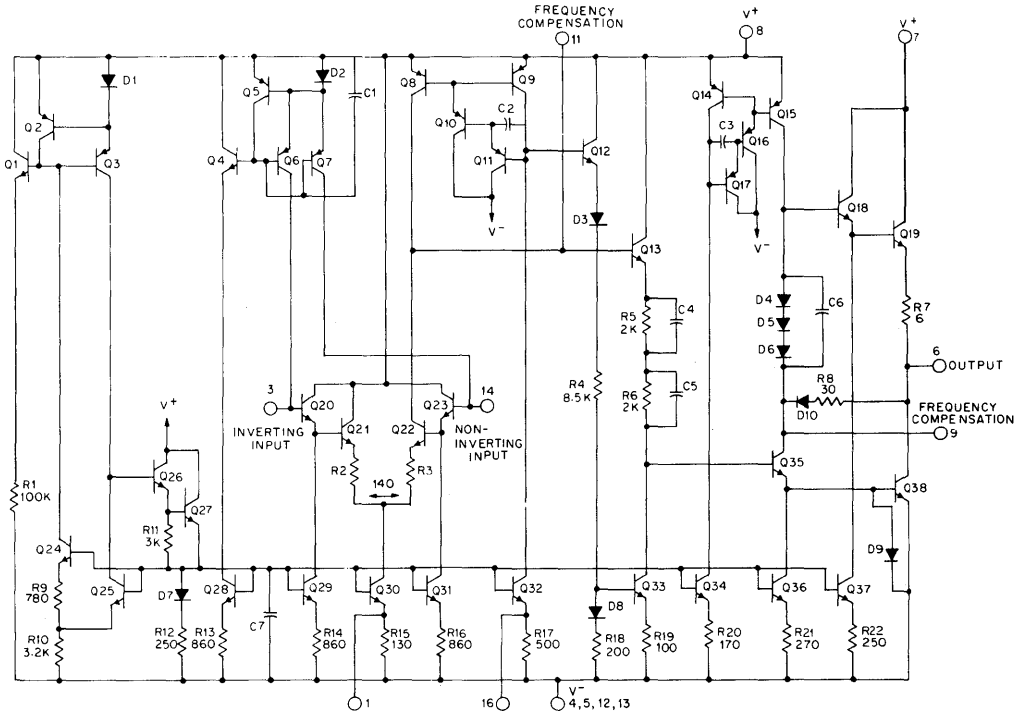
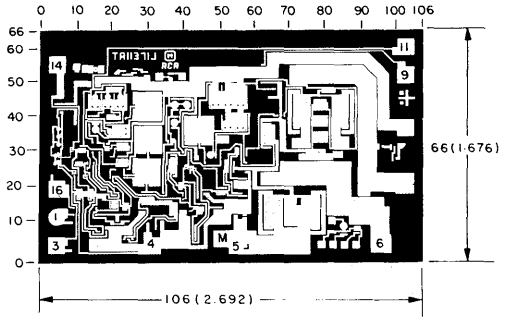


Figure 17 - Full schematic diagram of the CA3450.



M-Bonding wire to Chip Mounting Pad.
Pins 12 and 13 Connected to Chip Mounting Pad.
No Chip Pads for 2, 10, 12, 13, 15.

Figure 18 - Dimensions and pad layout for CA3450H.

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Scale graduations are in mils (10^{-3} inch).

Operational Amplifiers

CA3493A, CA3493

May 1990

BiMOS Precision Operational Amplifiers

Features:

- *Low V_{IO}: 200 µV max. (CA3493A)*
  500 µV max. (CA3493A)
- *Low $\Delta V_{IO}/\Delta T$: 3 µV/°C max. (CA3493A)*
  5 µV/°C max. (CA3493)
- *Low I_{IO} and I_I*
- *Low $\Delta/I_{IO}/\Delta T$: 150 pA/°C max. (CA3493)*
- *Low $\Delta/I_I/\Delta T$: 3.7 nA/°C max. (CA3493)*

Applications:

- *Thermocouple preamplifiers*
- *Strain-gauge bridge amplifiers*
- *Summing amplifiers*
- *Differential amplifiers*
- *Bilateral current sources*
- *Log amplifiers*
- *Differential voltmeters*
- *Precision voltage references*
- *Active filters*
- *Buffers*
- *Integrators*
- *Sample-and-hold circuits*
- *Low frequency filters*

The CA3493A and CA3493 are ultra-stable, precision instrumentation, operational amplifiers that employ both PMOS and bipolar transistors on a single monolithic chip. The CA3493A and CA3493 amplifiers are internally phase compensated and provide a gain-bandwidth product of 1.2 MHz. They are pin compatible with the industrial types such as 725, 108A, OP-7, LM11 and LM714 where positive nulling is employed.

Because of their low offset voltage and low offset voltage-versus-temperature coefficient the CA3493A and CA3493 amplifiers have a wider range of applications than most op amps and are particularly well suited for use as thermocouple amplifiers, high gain filters, buffer, strain gauge bridge amplifiers and precision voltage references.

The op amps are functionally identical. The CA3493 and CA3493A operate from supply voltage of ±3.5 V to ±18 V and have operating temperature ranges of 0°C to +70°C and -25°C to +85°C, respectively.

These types are supplied in standard 8-lead TO-5-style (T suffix), 8-lead dual-in-line formed lead TO-5-style (DIL-CAN S suffix) and 8-lead dual-in-line plastic (Mini-DIP E suffix) packages.

Circuit Description

The block diagram of the CA3493 amplifier, Fig. 2, shows the voltage gain and supply current for each of its four amplifier stages. Simplified and complete schematic diagrams of the CA3493 amplifier are shown in Figs. 3 and 4, respectively.

File Number **1290**

Absolute-Maximum Ratings, *Absolute-Maximum Values at $T_A = 25°C$*

	CA3493A	CA3493	
DC Supply Voltage	±18	±18	V
Differential-Mode Input Voltage	±5	±5	V
Common-Mode DC Input Voltage	(V+ −4), V−	(V+ −4), V−	V
Input Terminal Current	1	1	mA
Device Dissipation			
Without Heat Sink			
Up to 55°C	630	630	mW
Above 55°C	Derate Linearly 6.67		mW/°C
Temperature Range	−25 to 85	0 to 70	°C
Output Short-Circuit Duration*	Indefinite	Indefinite	
Lead Temperature (During Soldering) at distance of 1/16 in. ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max.	±265	±265	°C

*Short circuit may be applied to ground or to either supply.

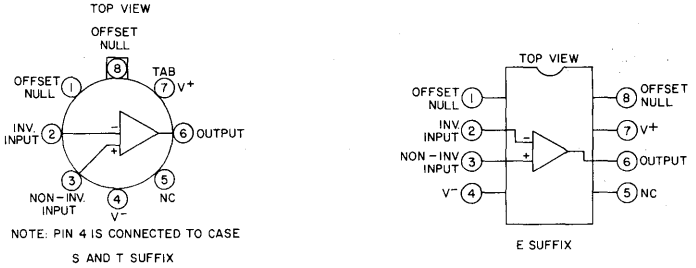


Fig. 1 - Functional diagram of CA3493A and CA3493.

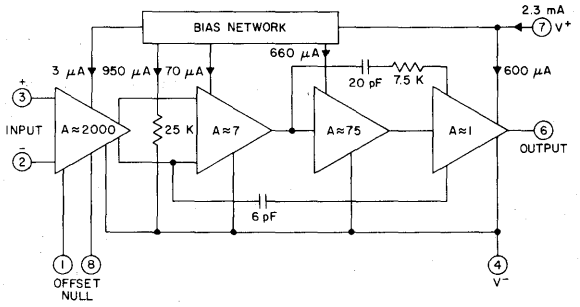


Fig. 2 - Block diagram of CA3493A and CA3493.

Circuit Description (cont'd)

A quad of physically cross-connected n-p-n transistors comprise the input-stage differential pair (Q1,Q2 in Figs. 3 and 4); this arrangement contributes to the low input offset-voltage characteristics of the amplifier. The ultra-high gain provided in the first stage ensures that subsequent stages cannot significantly influence the overall offset-voltage characteristics of the amplifier. High load impedances for the input-stage differential pair (Q1,Q2) are provided by the cascode-connected p-n-p transistors Q3,Q5 and Q4,Q6, thereby contributing to the high gain developed in the stage.

The second stage of the amplifier consists of a differential amplifier employing PMOS/FETs (Q7,Q8 in Figs. 3 and 4) with

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V+ = 15$ V and $V- = 15$ V unless otherwise specified.

CHARACTERISTIC	LIMITS						UNITS
	CA3493A			CA3493			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	—	140	200	—	300	500	μV
V_{IO} @ Max.Temp.	—	—	380	—	—	725	μV
Input Offset Voltage Temp.Coefficient, $\Delta V_{IO}/\Delta T$ (Over specified temperature range for each device)	—	1	3	—	1	5	μV/°C
Input Offset Current, I_{IO}	—	3	5	—	5	10	nA
$\|I_{IO}\|$ @ Max.Temp.	—	—	11	—	—	17	nA
Input Offset Current Temp. Coefficient, $\Delta I_{IO}/\Delta T$ (Over specified temperature range for each device)	—	0.03	0.10	—	0.04	0.15	nA/°C
Input Bias Current, I_I	—	10	20	—	20	40	nA
$\|I_B\|$ @ Max.Temp.	—	—	83	—	—	207	nA
Input Bias Current Temp. Coefficient, $\Delta I_I/\Delta T$	—	0.10	1.18	—	0.15	3.70	nA/°C
Input Noise Voltage, e_n p-p (0.1 to 10 Hz)	—	0.36	—	—	0.36	—	μV p-p
Input Noise Voltage Density, e_n							
$f_O = 10$ Hz	—	25	—	—	25	—	
$f_O = 100$ Hz	—	25	—	—	25	—	
$f_O = 1000$ Hz	—	24	—	—	24	—	nV/$\sqrt{Hz}$
$f_O = 10$ kHz	—	24	—	—	24	—	
$f_O = 100$ kHz	—	22	—	—	22	—	
Input Noise Current, i_n p-p (0.1 to 10 Hz)	—	12	20	—	12	20	pA p-p
Input Noise Current Density, i_n							
$f_O = 10$ Hz	—	0.83	—	—	0.83	—	
$f_O = 100$ Hz	—	0.80	—	—	0.80	—	
$f_O = 1000$ Hz	—	0.75	—	—	0.75	—	pA/$\sqrt{Hz}$
$f_O = 10$ kHz	—	0.72	—	—	0.72	—	
$f_O = 100$ kHz	—	0.60	—	—	0.60	—	

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V^+ = 15$ V and $V^- = 15$ V (Cont'd) unless otherwise specified.

CHARACTERISTIC	LIMITS						UNITS
	CA3493A			CA3493			
	Min.	Typ.	Max.	Min.	Typ.	Max.	
Common-Mode Input Voltage Range, V_{ICR}	−12	−13.5 to 11.5	10	−12	−13.5 to 11.5	10	V
Common-Mode Rejection Ratio, ($V_{CM} = V_{ICR}$)	110	115	—	100	110	—	dB
		1.78	3.16		3.16	10	μV/V
Power Supply Rejection Ratio, PSRR, $\Delta V_{IO}/\Delta V\pm$	100	130	—	100	130	—	dB
		0.316	10		0.316	10	μV/V
Maximum Output Voltage Swing ($R_L \geq 2$ KΩ)	±13.0	±13.5	—	±13.0	±13.5	—	V
Large-Signal Voltage Gain ($V_O = \pm 10$)							
$R_L \geq 1$ KΩ	—	—	—	—	—	—	
$R_L \geq 2$ KΩ	110	115	—	100	110	—	dB
$R_L \geq 10$ KΩ	—	125	—	—	115	—	
Short-Circuit Output Current to the Opposite Rail, I_{OM}^+, I_{OM}^-	−25	±7	25	−25	±7	25	mA
Slew Rate, SR ($R_L \geq 2$ KΩ; Unity Gain Voltage Follower)	—	0.25	—	—	0.25	—	V/μs
Gain-Bandwidth Product, f_t $A_{OL} = 0$ dB $R_L = 2$ kΩ $C_L = 100$ pF $V_{IN} = 20$ $f = 1$ kHz	—	1.20	—	—	1.20	—	MHz
Small-Signal Transient Response, t_r ($V_{IN} = 20$ mV p-p, $f = 1$ kHz	—	0.29	—	—	0.29	—	μs
Supply Current, $R_L = \infty$ $V^+ = 15$, $V^- = -15$	—	2.3	3.5	—	2.3	3.5	mA
Temperature Range	−25	—	85	0	—	70	°C

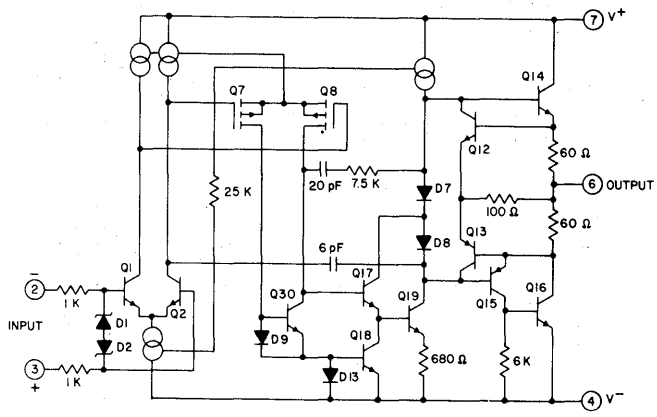


Fig. 3 - CA3493 simplified schematic diagram.

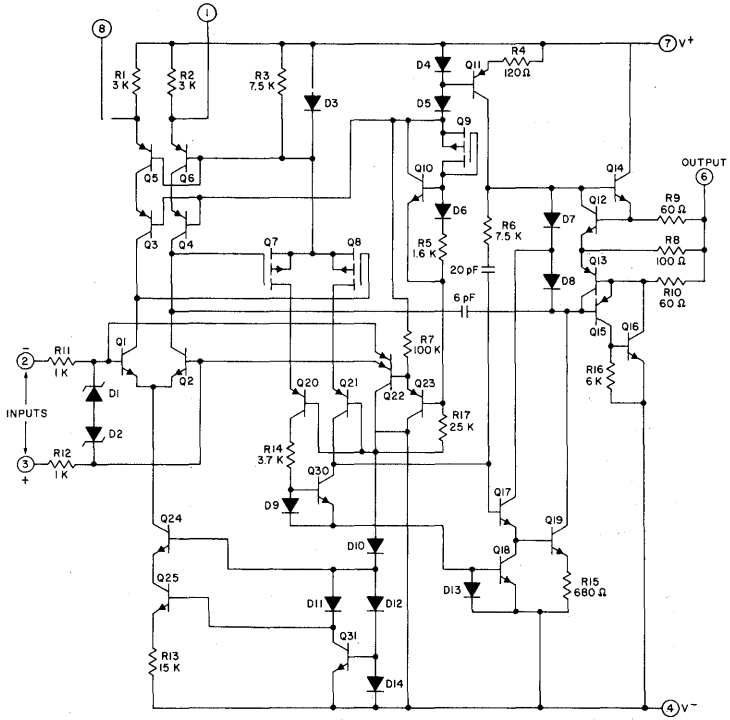


Fig. 4 - Schematic diagram of CA3493A and CA3493.

Circuit Description (cont'd)

appropriate drain loading. Since Q7 and Q8 are MOS/FETs, their loading on the first stage is quite low, thereby making an additional contribution to the high gain developed in the first stage. The second stage is also configured to convert its differential signal to a single-ended output signal by means of current mirror D9,Q30 (Figs. 3 and 4) to drive subsequent gain stage.

The third stage of the amplifier consists of Darlington-connected n-p-n transistors (Q17,Q19 in Figs. 3 and 4), driving the quasi-complementary Class AB output stage (Q14 and Q15,Q16 in Figs. 3 and 4). Output-stage short-circuit protection is activated by voltage drops developed across the 60-ohm resistors adjacent to the output terminal (R9 and R10, Fig. 4). When the voltage drop developed across either of these resistors reaches a potential equal to 1 V_{be}, the respective protective transistor (Q12 or Q13) is activated and shunts the base drive from the bases of the output stage transistors (Q14 and Q15,Q16).

Internal frequency compensation for the CA3493 amplifier is provided by two internal networks, a 6-pF capacitor connected between the input-stage transistor collectors and the node between the third and output stages and a second network, consisting of a 20-pF capacitor in series with a 7.5-KΩ resistor connected between the input and output nodes of the third stage.

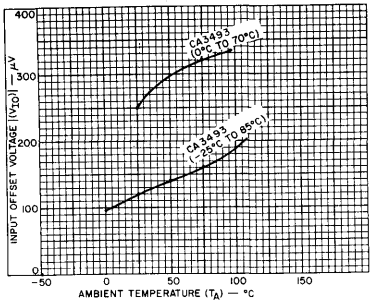


Fig. 5 - Typical input offset-voltage temperature characteristic for CA3493A and CA3493.

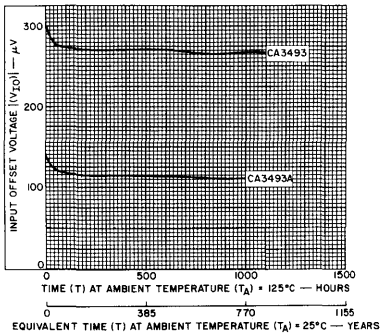


Fig. 6 — Input offset voltage vs. time.

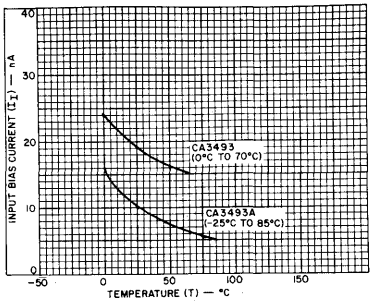


Fig. 7 — Typical input bias current vs. temperature

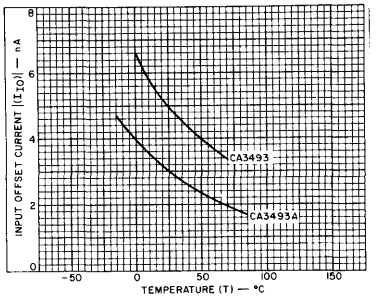


Fig. 8 — Typical input offset current vs. temperature.

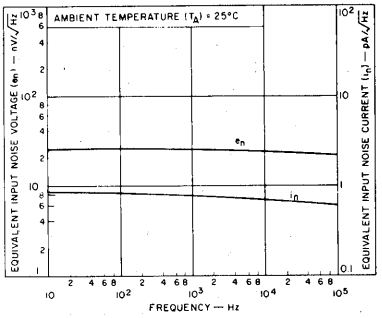


Fig. 9 — Input noise voltage and current density vs. frequency.

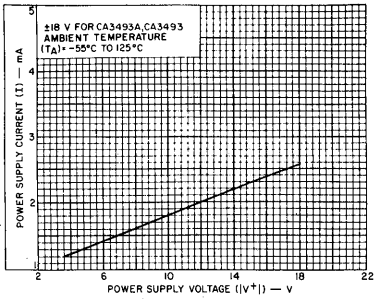


Fig. 10 — Power supply voltage (V+, V−) vs. supply current.

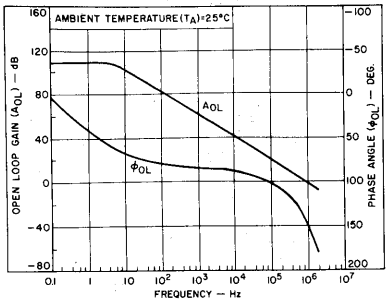


Fig. 11 - Open-loop gain and phase-shift response for CA3493.

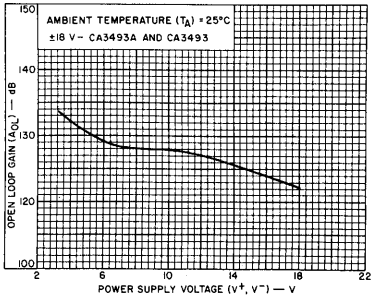


Fig. 12 — Open-loop gain vs. power-supply voltage.

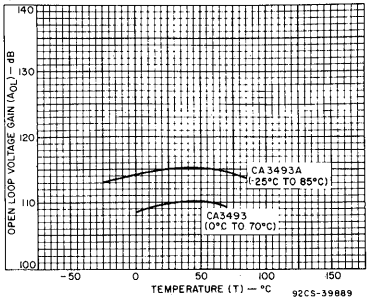


Fig. 13 - Open-loop gain vs. temperature for CA3493A and CA3493.

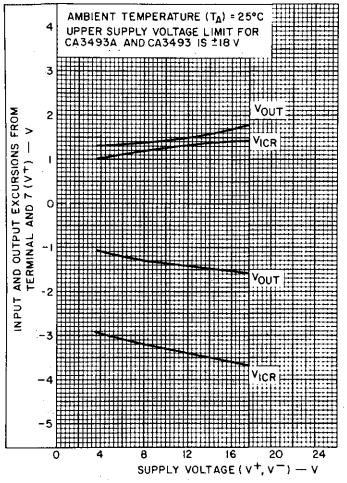


Fig. 15 — Output-voltage-swing capability and common-mode input-voltage vs. supply voltage.

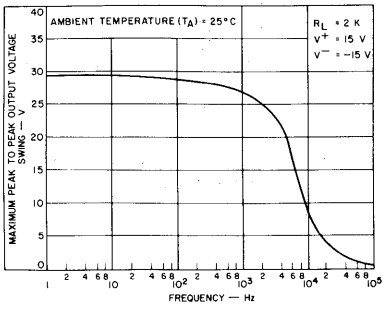


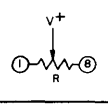
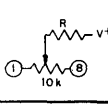
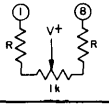
Fig. 14 — Maximum undistorted output voltage vs. frequency.

Offset Voltage Nulling

The input offset voltage can be nulled to zero by any of the three methods shown in the table below. A 10K potentiometer between terminals 1 and 8, with its wiper returned to V^+, will provide a gross nulling for all types. For finer nulling, either of the other two circuits shown below may be used, thus providing simpler improved resolution for all types.

CAUTION: The CA3493 amplifiers will be damaged if they are plugged into op-amp circuits employing nulling with respect to the V^- supply bus.

Offset Voltage Nulling

Offset Nulling Circuits			
Type	**Resistor R Value**	**Resistor R Value**	**Resistor R Value**
CA3493A CA3493	10K 10K	50K 20K	10K 5K
	Gross Offset Adjustment	Finer Offset Adjustments	

Test Circuits

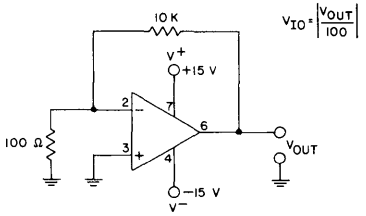
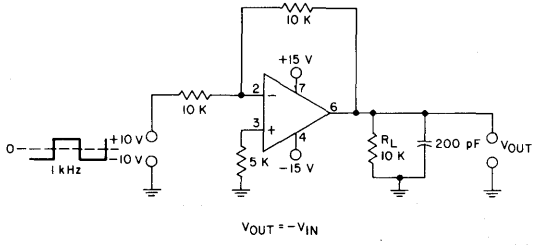
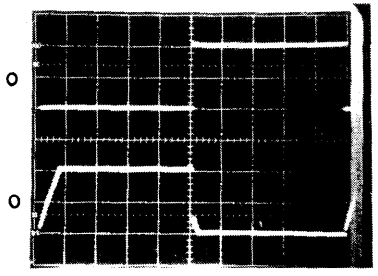


Fig. 16 - Input offset voltage test circuit.



a



b

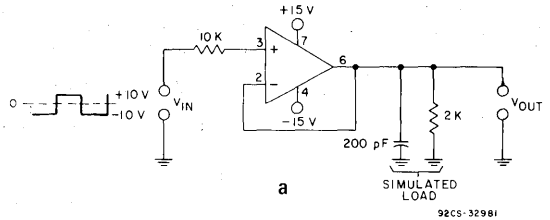
TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT. : $\frac{10\,V}{DIV}$

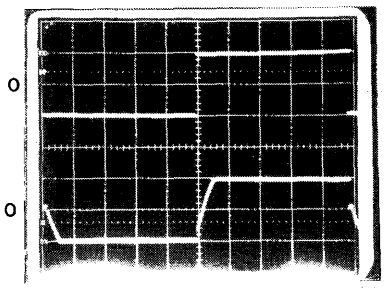
HOR. : $\frac{.1\,ms}{DIV}$

$V^+ = 15\,V$
$V^- = -15\,V$
$R_L = 10\,K$

Fig. 17 - Inverting amplifier (a) test circuit (b) response to 1-kHz, 20-V p-p square wave.



a



b

TOP TRACE : INPUT VOLTAGE
BOTTOM TRACE : OUTPUT VOLTAGE

VERT: $\frac{10\,V}{DIV}$

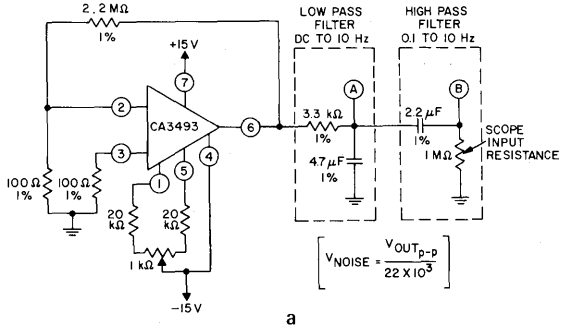
HOR : $\frac{.1\,ms}{DIV}$

$V+ = 15\,V$

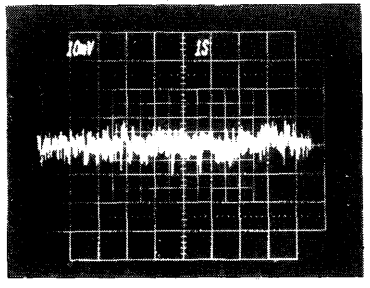
$V^- = 15\,V$

$R_L = 2K$

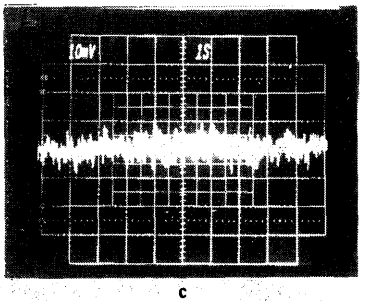
Fig. 18 - Voltage follower (a) test circuit (b) response to 20-V p-p, 1-kHz square-wave input.



a



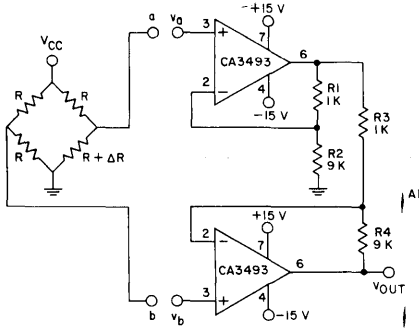
b



c

Fig. 19 - Low frequency noise (a) test circuit—0.1 to 10 Hz (b) output A waveform—0 to 10 Hz noise (c) output B waveform—0 to 10 Hz noise.

Application Circuits



$$V_{OUT} = -v_a\left(\frac{R2}{R1}+1\right)\frac{R4}{R3} + v_b\left(\frac{R4}{R3}+1\right)$$

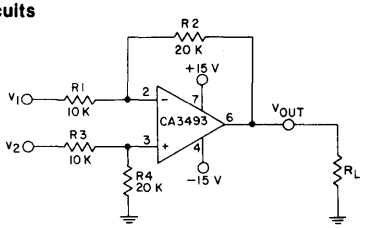
FOR IDEAL RESISTORS WITH $\frac{R1}{R2} = \frac{R3}{R4}$

$$V_{OUT} = v_b - v_a\left(\frac{R4}{R3}+1\right)$$

$$A = \frac{V_{OUT}}{v_b - v_a} = \left(\frac{R4}{R3}+1\right)$$

FOR VALUES ABOVE $V_{OUT} = (v_b - v_a)(10)$

Fig. 20 - Typical two-op amp bridge-type differential amplifier.



ALL RESISTANCE VALUES ARE IN OHMS

$$V_{OUT} = v_2\left(\frac{R4}{R3+R4}\right)\left(\frac{R1+R2}{R1}\right) - v_1\left(\frac{R2}{R1}\right)$$

IF R4 = R2, R3 = R1 AND $\frac{R2}{R1} = \frac{R4}{R3}$

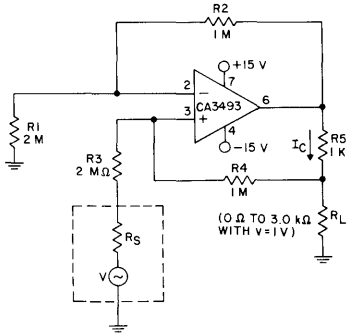
THEN $V_{OUT} = (V_2 - V_1)\left(\frac{R2}{R1}\right)$

FOR VALUES ABOVE $V_{OUT} = 2(V_2 - V_1)$

IF A_V IS TO BE MADE 1 AND IF R1 = R3 = R4 = R WITH R2 = 0.999 R (0.1% MISMATCH IN R2)

THEN $V_{OCM} = 0.0005\ V_{IN}$ OR CMRR = 66 dB
THUS, THE CMRR OF THIS CIRCUIT IS LIMITED BY THE MATCHING OR MISMATCHING OF THIS NETWORK RATHER THAN THE AMPLIFIER.

Fig. 21 - Differential amplifier (simple subtractor) using CA3493.



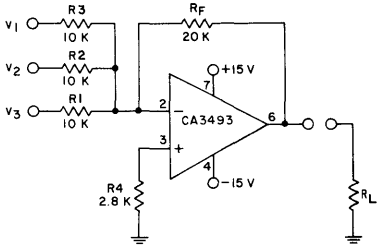
ALL RESISTORS ARE 1%

IF R1 = R3 AND R2 ≈ R4 + R5 THEN

I_L IS INDEPENDENT OF VARIATIONS IN R_L FOR R_L VALUES OF 0 Ω TO 3 kΩ WITH V = 1 V

$$I_L = \frac{V}{R3}\frac{R4}{R5} = \frac{V}{(2\,M)(1K)}\frac{1\,M}{2\,K} = \frac{V}{2\,K} = 500\ \mu A$$

Fig. 22 - Using CA3493 as a bilateral current source.



$$V_{OUT} = -\left(\frac{R_F}{R1}v_1 + \frac{R_F}{R2}v_2 + \frac{R_F}{R3}v_3\right)$$

$$V_{OUT} = -(2v_1 + 2v_2 + 2v_3)$$

ALL RESISTANCE VALUES ARE IN OHMS

Fig. 23 - Typical summing amplifier application.

The CA3493 is an excellent choice for use with themocouples. In Fig. 24, the CA3493 amplifies the signal generated 500 times. The three 22-megohm resistors will provide full-scale output if the thermocouple opens.

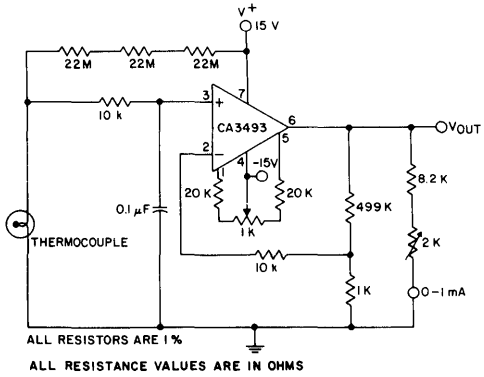


Fig. 24 - The CA3493 used in a thermocouple circuit.

May 1990

BiMOS Microprocessor Operational Amplifiers

With MOSFET Input/CMOS Output

Features:

- *MOSFET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 x 10^{12}Ω) typ.
  very low I_I = 5 pA typ. at 15 V operation
  = 2 pA typ. at 5 V operation
- *Ideal for single-supply applications*
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *CMOS output stage permits signal swing to either (or both) supply rails*
- *CA5130A, CA5130 5V have full military temperature range guaranteed specifications*
- *CA5130A, CA5130 are guaranteed to operate down to V_T = 4.5 V for AOL*
- *CA5130A, CA5130 are guaranteed to operate at ±7.5 CA3130A, CA3130 specifications*

Applications:

- *Ground-referenced single supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *High-input-impedance comparators (Ideal interface with digital CMOS)*
- *High-input-impedance wideband amplifiers*
- *Voltage followers (e.g. follower for single-supply D/A converter)*
- *Voltage regulators (permits control of output voltage down to zero volts)*
- *Peak detectors*
- *Single-supply full-wave precision rectifiers*
- *Photo-diode sensor amplifiers*
- *5 V logic systems*
- *Microprocessors interface*

CA5130A and CA5130 are integrated-circuit operation amplifiers that combine the advantage of both CMOS and biploar transistors on a monolithic chip. They are designed and guaranted to operate in microprocessors or logic systems that use +5 V supplies.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5130 Series circuits operate at supply voltages ranging from 4 to 16 volts, or ±2 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provision are also made to permit strobing of the output stage.

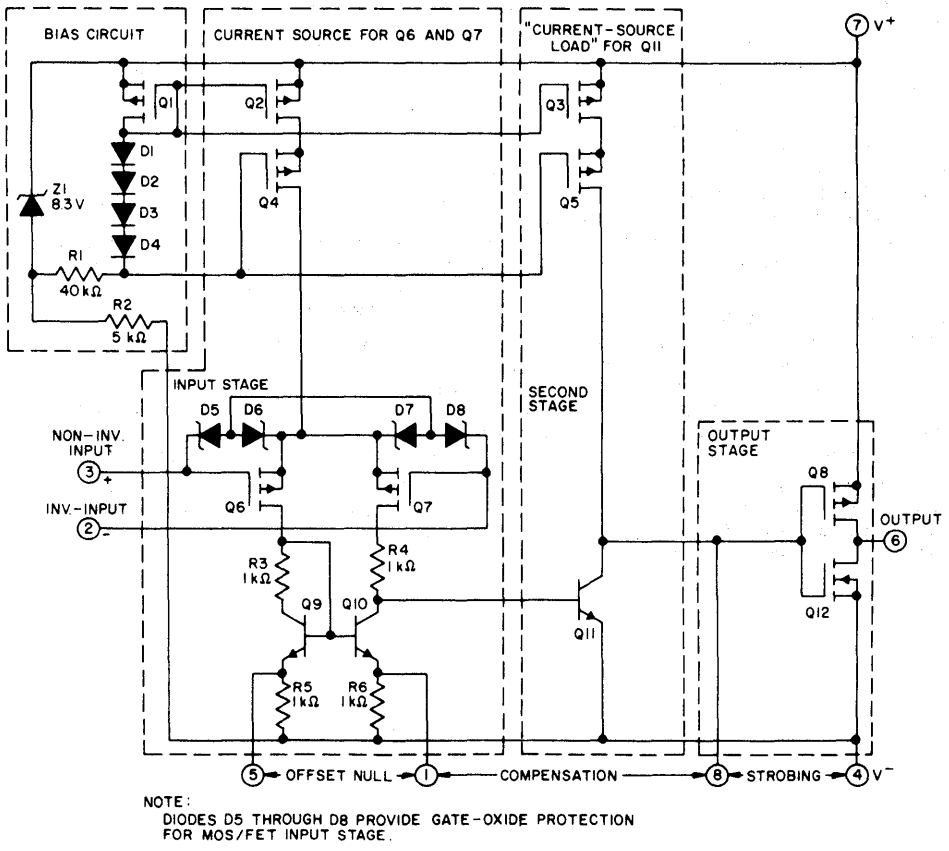
The CA5130 Series is supplied in standard 8-lead TO-5 style packages (T suffix) and 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA5130 is available in chip form (H suffix). The CA5130 and CA5130A are also available in the 8-lead Small Outline package (M suffix) and in the 8-lead dual-in-line plastic package (Mini-DIP E suffix).

The CA5130A, CA5130 have guaranteed specifications for 5 V operation over the full military-temperature range of -55°C to +125°C.

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8V) to (V^- -0.5V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK -
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate Linearly 6.67 mW/°C
WITH HEAT SINK -
UP TO 90°C ..... 1 W
ABOVE 90°C ..... Derate Linearly 16.7 mW/°C
SMALL OUTLINE PACKAGE ..... 250°/W
TEMPERATURE RANGE:
OPERATING (all types) ..... -55 to +125°C
STORAGE (all types) ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION * ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

* Short circuit may be applied to ground or to either supply.



NOTE:
DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION FOR MOS/FET INPUT STAGE.

Fig. 2 - Schematic diagram of the CA5130 series.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V^+ = 5 V, V^- = 0 V

CHARACTERISTIC		LIMITS						UNITS
		CA5130A			CA5130			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage V_O = 2.5 V	V_{IO}	—	1.5	4	—	2	10	mV
Input Offset Current V_O = 2.5 V	I_{IO}	—	0.1	5	—	0.1	10	pA
Input Current, V_O = 2.5 V	I_I	—	2	10	—	2	15	pA
Common-Mode Rejection Ratio	C_{MRR}							dB
V_{CM} = 0 to 1 V		75	87	—	70	85	—	
V_{CM} = 0 to 2.5 V	C_{MRR}	60	69	—	60	69	—	
Input Common-Mode Voltage Range								V
	V_{ICR}^+	2.5	2.8	—	2.5	2.8	—	
	V_{ICR}^-	—	-0.5	0	—	-0.5	0	
Power-Supply Rejection Ratio Δ^+ = 1 V; Δ^- = 1 V	P_{SRR}	60	75	—	55	73	—	dB
Large-Signal Voltage Gain*	A_{OL}							dB
V_O = 0.1 to 4.1 V	R_L = ∞	100	105	—	95	105	—	
V_O = 0.1 to 3.6 V	R_L = 10 k	90	97	—	85	95	—	
Source Current V_O = 0 V	I_{SOURCE}	1.0	3.1	4.0	1.0	2.6	4.0	mA
Sink Current V_O = 5 V	I_{SINK}	1.0	1.6	4.0	1.0	1.7	4.0	mA
Output Voltage	V_{OUT}							V
R_L = ∞	V_{OM}^+	4.99	5	—	4.99	5	—	
	V_{OM}^-	—	0	0.01	—	0	0.01	
R_L = 10 k	V_{OM}^+	4.4	4.7	—	4.4	4.7	—	
	V_{OM}^-	—	0	0.01	—	0	0.01	
R_L = 2 k	V_{OM}^+	2.5	3.5	—	2.5	3.5	—	
	V_{OM}^-	—	0	0.01	—	0	0.01	
Supply Current	I_{SUPPLY}							μA
V_O = 0 V		—	50	100	—	50	100	
V_O = 2.5 V	I_{SUPPLY}	—	260	400	—	260	400	

*For V^+ = 4.5 V and V^- = Gnd; V_{OUT} = 0.5 V to 3.2 V at R_L = 10 k.

ELECTRICAL CHARACTERISTICS AT T_A = -55°C to +125°C, V^+ = 5 V, V^- = 0 V

CHARACTERISTIC		LIMITS						UNITS
		CA5130A			CA5130			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage V_O = 2.5 V	V_{IO}	—	2	10	—	3	15	mV
Input Offset Current V_O = 2.5 V	I_{IO}	—	0.1	5	—	0.1	10	nA
Input Current V_O = 2.5 V	I_I	—	2	10	—	2	15	nA
Common-Mode Rejection Ratio	C_{MRR}							
V_{CM} = 0 to 1 V		60	80	—	60	80	—	dB
V_{CM} = 0 to 2.5 V	C_{MRR}	55	80	—	50	80	—	dB
Input Common-Mode Voltage Range								
	V_{ICR}^+	2.5	2.8	—	2.5	2.8	—	V
	V_{ICR}^-	—	-0.5	0	—	-0.5	0	V
Power-Supply Rejection Ratio	P_{SRR}							
Δ^+ = 1 V; Δ^- = 1 V		45	70	—	40	66	—	dB
Large-Signal Voltage Gain*	A_{OL}							
V_O = 0.1 to 4.1 V	R_L = ∞	94	98	—	90	98	—	dB
V_O = 0.1 to 3.6 V	R_L = 10 k	80	88	—	75	85	—	dB
Source Current V_O = 0 V	I_{SOURCE}	0.6	2.2	5.0	0.6	—	5.0	mA
Sink Current V_O = 5 V	I_{SINK}	0.6	1.15	5.0	0.6	—	5.0	mA
Output Voltage	V_{OUT}							
R_L = ∞	V_{OM}^+	4.99	5	—	4.99	5	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
R_L = 10 k	V_{OM}^+	4.0	4.6	—	4.0	4.6	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
R_L = 2 k	V_{OM}^+	2.0	3.0	—	2.0	3.0	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
Supply Current	I_{SUPPLY}							
V_O = 0 V		—	80	220	—	80	220	μA
V_O = 2.5 V	I_{SUPPLY}	—	300	500	—	300	500	μA

*For V^+ = 4.5 V and V^- = Gnd; V_{OUT} = 0.5 V to 3.2 V at R_L = 10 k.

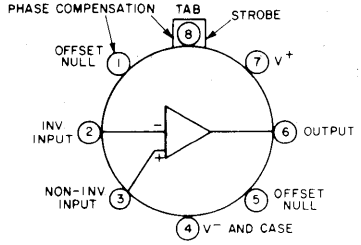
ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V^+ = 15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC		LIMITS						UNITS
		CA5130A (T, S, E)			CA5130 (T, S, E)			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage $V^{\pm}$ = ±7.5 V	V_{IO}	—	2	5	—	8	15	mV
Input Offset Current $V^{\pm}$ = ±7.5 V	I_{IO}	—	0.5	20	—	0.5	30	pA
Input Current $V^{\pm}$ = ±7.5 V	I_I	—	5	30	—	5	50	pA
Large-Signal Voltage Gain	A_{OL}	50 k	320 k	—	50 k	320 k	—	V/V
V_O = 10 V_{p-p}, R_L = 2 kΩ		94	110	—	94	110	—	dB
Common-Mode Rejection Ratio	C_{MRR}	80	90	—	70	90	—	dB
Common-Mode Input-Voltage Range	V_{ICR}	10	-0.5 to 12	0	10	-0.5 to 12	0	V
Power-Supply Rejection Ratio $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$ = ±7.5 V	P_{SRR}	—	32	150	—	32	320	μV/V
Maximum Output Voltage								
At R_L = 2 k	V_{OM}^+	12	13.3	—	12	13.3	—	V
	V_{OM}^-	—	0.002	0.01	—	0.002	0.01	
At R_L = ∞	V_{OM}^+	14.99	15	—	14.99	15	—	
	V_{OM}^-	—	0	0.01	—	0	0.01	
Maximum Output Current								
I_{OM}^+ (Source) @ V_O = 0 V		12	22	45	12	22	45	mA
I_{OM}^- (Sink) @ V_O = 15 V		12	20	45	12	20	45	
Supply Current	I^+							
V_O = 7.5 V, R_L = ∞		—	10	15	—	10	15	mA
V_O = 0 V, R_L = ∞		—	2	3	—	2	3	
Input Offset Voltage Temp. Drift $\Delta V_{IO}/\Delta T$*		—	10	—	—	10	—	μV/°C

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

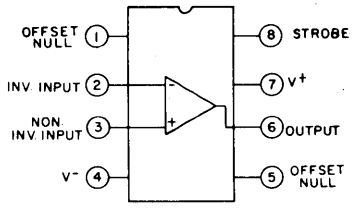
CHARACTERISTIC		TEST CONDITIONS V^+ = +7.5 V, V^- = -7.5 V, T_A = 25°C (Unless otherwise specified)	TYPICAL VALUES CA5130A (T, S, E)	TYPICAL VALUES CA5130 (T, S, E)	UNITS
Input Offset Voltage Adjustment Range		10 kΩ across Terms. 4 and 5 or 4 and 1	±22	±22	mV
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I	f = 1 MHz	4.3	4.3	pF
Equivalent Input Noise Voltage	e_n	BW = 0.2 MHz, R_S = 1 MΩ*	23	23	μV
Unity Gain Crossover Frequency	f_T	C_C = 0	15	15	MHz
		C_C = 47 pF	4	4	
Slew Rate, SR: Open Loop		C_C = 0	30	30	V/μs
Slew Rate, SR: Closed Loop		C_C = 56 pF	10	10	V/μs
Transient Response: Rise Time	t_r	C_C = 56 pF, C_L = 25 pF, R_L = 2 kΩ (Voltage Follower)	0.09	0.09	μs
Transient Response: Overshoot			10	10	%
Settling Time (4 Vp-p Input to < 0.1%)			1.2	1.2	μs

* Although a 1-MΩ source is used for this test, the equivalent input noise remains constant for values of R_S up to 10 MΩ.



TOP VIEW

S and T Suffixes



TOP VIEW

E and M Suffixes

Fig. 1 - Functional diagrams for the CA5130 series.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA5130 Series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA5130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA5130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

Input Stages

The circuit of the CA5130 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

Second-Stage

Most of the voltage gain in the CA5130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

Bias-Source Circuit

At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage

The output stage consists of a drain-loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance load, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feed-back for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 percent accuracy levels, including the negative supply rail.

†For general information on the characteristics of CMOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "CMOS Transistor Array".

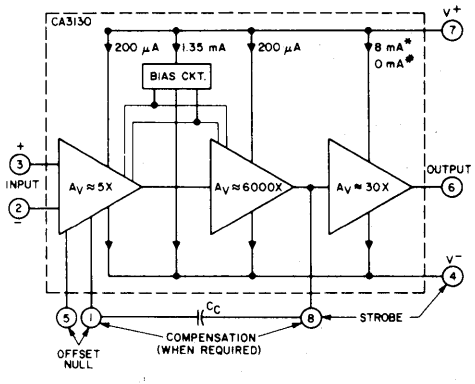


Fig. 3 - Block diagram of the CA5130 series.

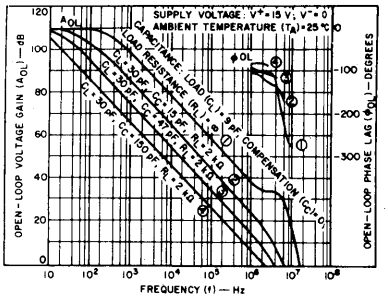


Fig. 4 - Open-loop voltage gain and phase shift vs. frequency for various values of C_L, C_C, and R_L.

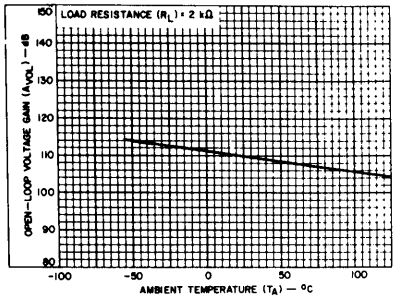


Fig. 5 - Open-loop gain vs. temperature.

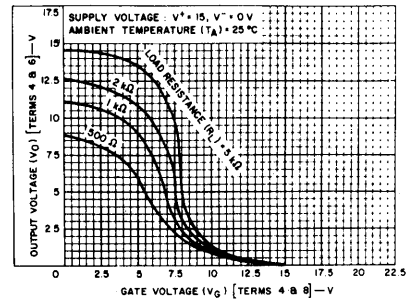


Fig. 6 - Voltage transfer characteristics of CMOS output stage.

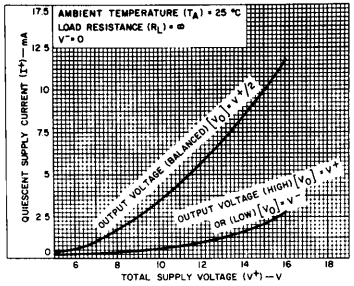


Fig. 7 - Quiescent supply current vs. supply voltage.

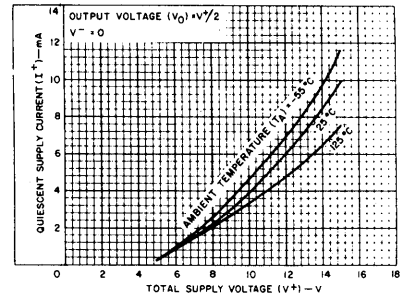


Fig. 8 - Quiescent supply current vs. supply voltage at several temperatures.

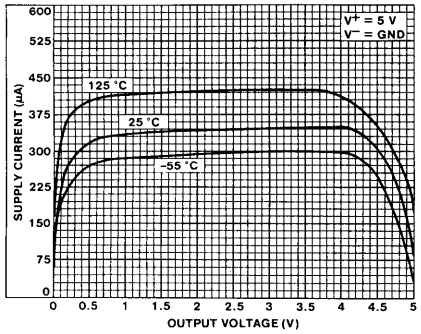


Fig. 9 - Supply current vs. output voltage.

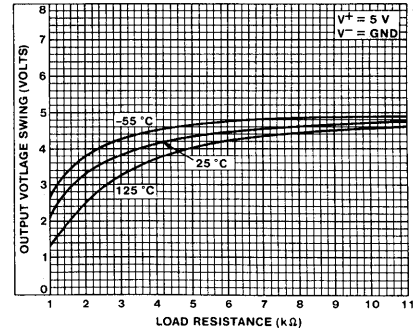


Fig. 10 - Output voltage swing vs. load resistance.

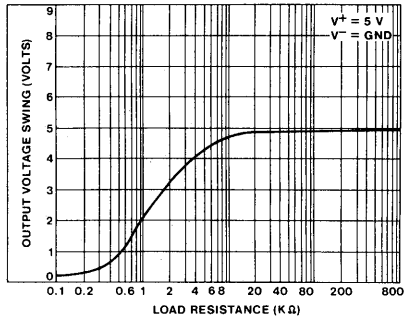


Fig. 11 - Output swing vs. load resistance.

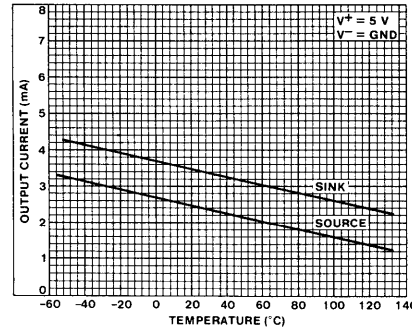


Fig. 12 - Output current vs. temperature.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA5130 Series Op-Amps is typically 5 pA at T_A = 25°C when terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig. 15 contains data showing the variation of input current as a function of common-mode input voltage at T_A = 25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA5130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA5130 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig. 16 provides data on the typical variation of input bias current as a function of temperature in the CA5130.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA5130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA5130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across

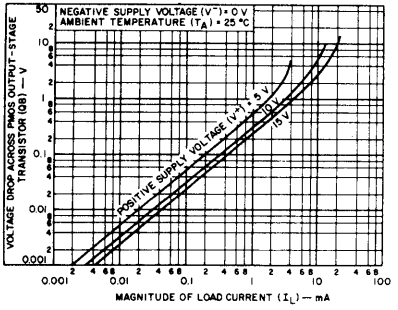


Fig. 13 - Voltage across PMOS output transistor (Q8) vs. load current.

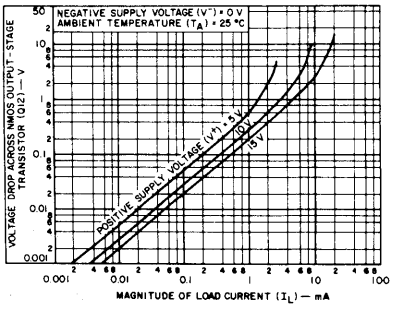


Fig. 14 - Voltage across NMOS output transistor (Q12) vs. load current.

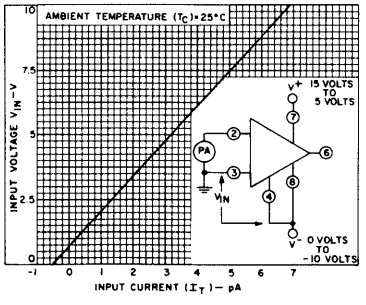


Fig. 15 - CA5130 input current vs. common-mode voltage.

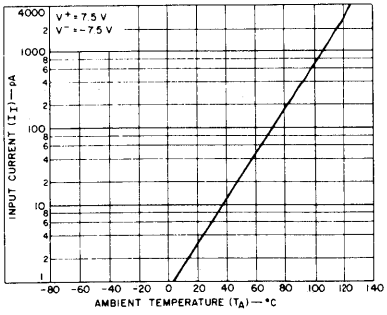


Fig. 16 - Input current vs. ambient temperature.

Terms. 2 and 3. Fig. 17 shows typical data pertinent to shifts in offset voltage encountered with CA5130 devices (TO-5 package) during life testing. At lower temperatures (TO-5 and plastic), for example at 85° C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

Power-Supply Considerations

Because the CA5130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 18a and 18b show the CA5130 connected for both dual- and single-supply operation.

Dual-supply operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA5130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceeding stages in the CA5130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 14a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig. 18b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is a $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to

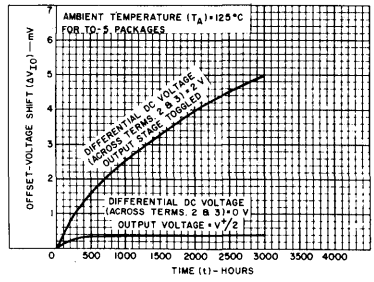


Fig. 17 - Typical incremental offset-voltage shift vs. operating life.

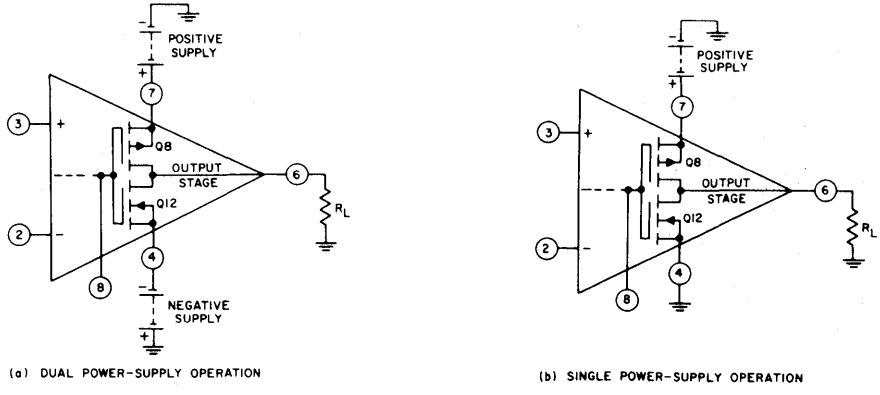


Fig. 18 - CA5130 output stage in dual and single power-supply operation.

both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA5130 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23 μV when the test-circuit amplifier of Fig. 19 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

TYPICAL APPLICATIONS

Voltage Followers

Operational amplifiers with very high input resistances, like the CA5130, are particularly suited to service as voltage followers. Fig. 20 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA5130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 21, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 21a with input-signal ramping. The waveforms in Fig. 21b show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 21b also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA5130 in a single-supply voltage-follower application.

9-Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig. 22. This system combines the concepts of multiple-switch CMOS IC's a low-cost ladder network of discrete metal-oxide-film resistors, a CA5130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 22.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one percent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA5130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the CMOS building blocks simplifies the design of DAC systems tailored to particular needs.

*"Digital-to-Analog Conversion Using the RCA-CD4007A CMOS IC", Application Note ICAN-6080.

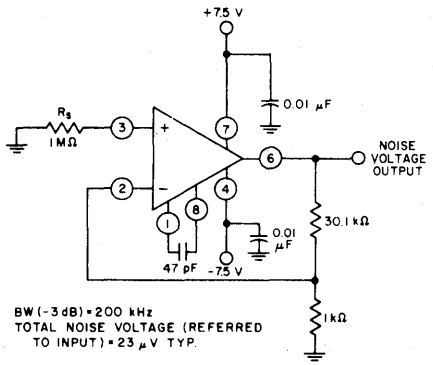
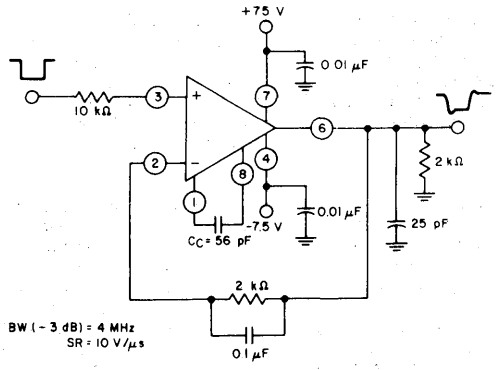
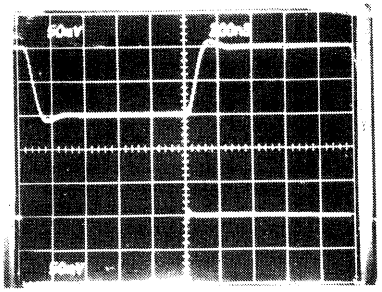


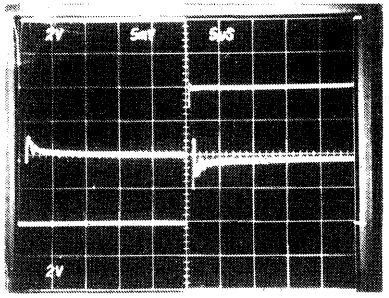
Fig. 19 - CA5130 test-circuit amplifier (30 -dB gain) used for wideband noise measurements.





Top Trace: Output
Bottom Trace: Input

(a) *Small-signal response (50 mV/div. and 200 ns/div.)*



Top Trace: Output signal (2 V/div. and 5 μs/div.)
Center Trace: Difference signal (5 mV/div. and 5 μs/div.)
Bottom Trace: Input signal (2 V/div. and 5 μs/div.)

(b) *Input-output difference signal showing settling time (Measurement made with Tektronix 7A13 differential amplifier)*

Fig. 20 - CA5130 split-supply voltage follower with associated waveforms.

Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

The absolute-value circuit using the CA5130 is shown in Fig. 23. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA5130 functions as a normal inverting amplifier with a gain equal to -R2/R1. When the equality of the two equations shown in Fig. 23 is satisfied, the full-wave output is symmetrical.

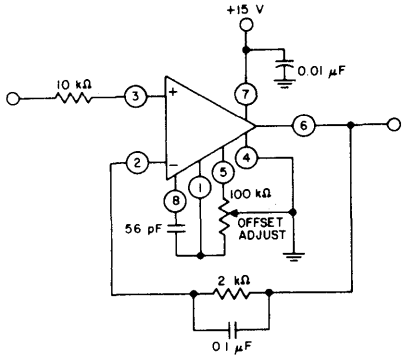
Peak Detectors

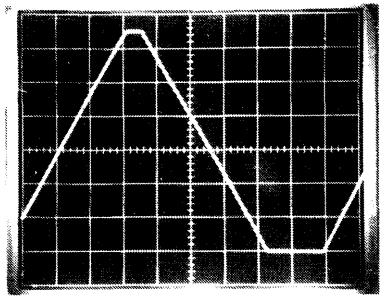
Peak-detector circuits are easily implemented with the CA5130, as illustrated in Fig. 24 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA5130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in active "pull-down" mode so that the intrinsic capacitance can be discharge more expeditiously.

Error-Amplifier in Regulated-Power Supplies

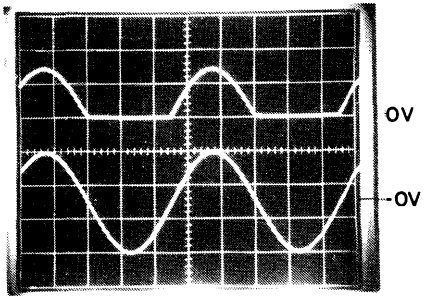
The CA5130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Fig. 25 shows the schematic diagram of a 40-mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zerners to provide supply-voltage for the CA5130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier.

Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.





(a) *Output-waveform with input-signal ramping (2 V/div. and 500 μs/div.)*



Top Trace: Output (5 V/div. and 200 μs/div.)
Bottom Trace: Input (5 V/div. and 200 μs/div.)

(b) *Output-waveform with ground-reference sine-wave input*

Fig. 21 - Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080).

Fig. 26 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA5130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on"and "off" periods, is shown in Fig. 27, Resistors R1 and R2 are used to bias the CA5130 to the mid-point of the supply-voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

Function Generator

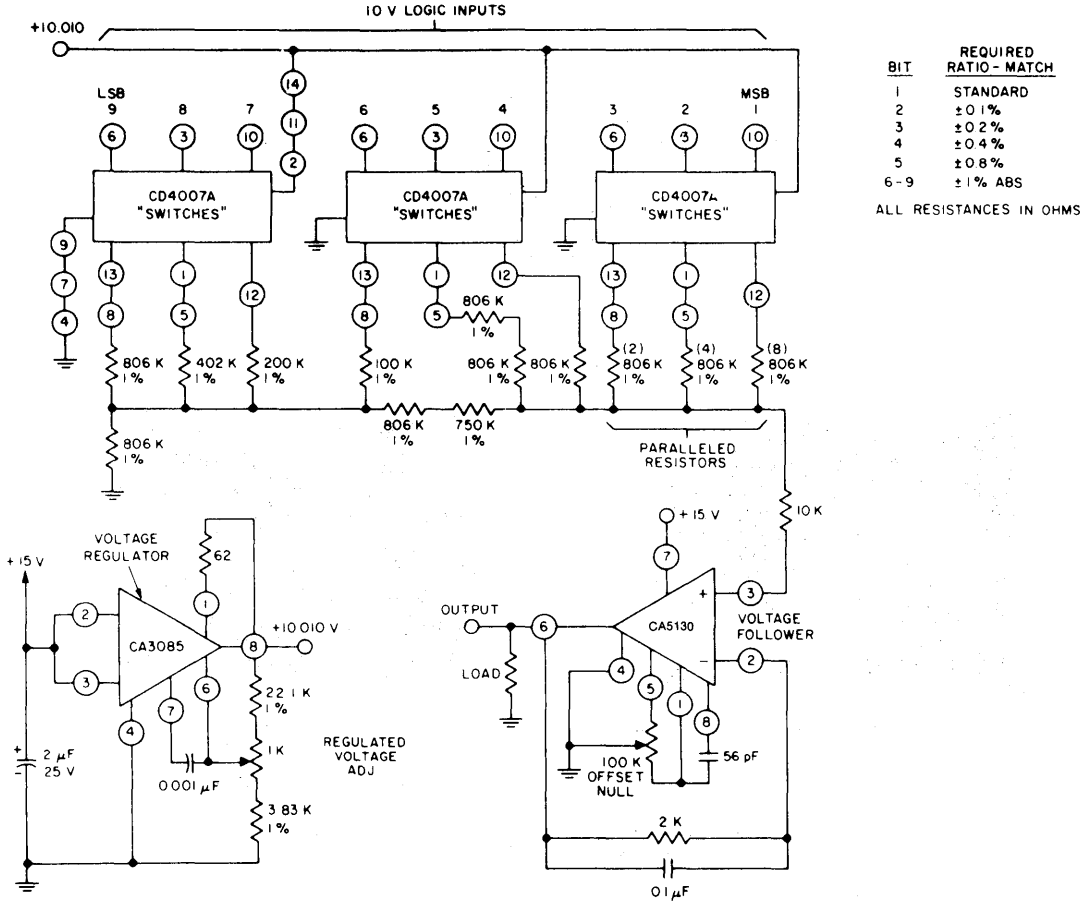
Fig. 24 contains a schematic diagram of a function generator using the CA5130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_o, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA5130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA5130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

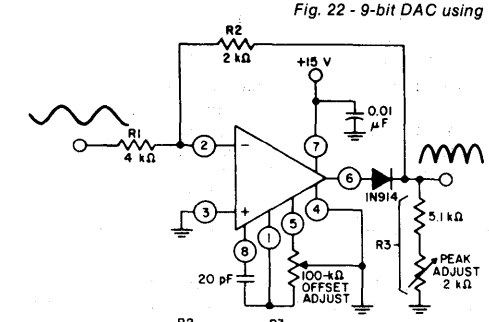
*See File No. 475 and ICAN-6668.



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS

ALL RESISTANCES IN OHMS

Fig. 22 - 9-bit DAC using CMOS digital switches and CA5130.



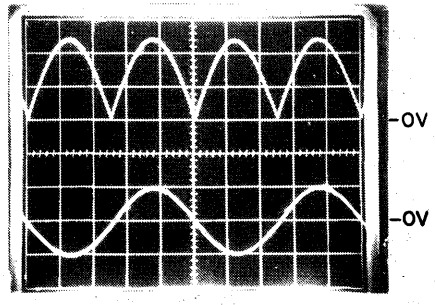
$$\text{GAIN} = \frac{R2}{RI} = X = \frac{R3}{RI + R2 + R3}$$

$$R3 = RI\left(\frac{X + X^2}{1 - X}\right)$$

$$\text{FOR } X = 0.5: \frac{2\text{ k}\Omega}{4\text{ k}\Omega} = \frac{R2}{RI}$$

$$R3 = 4\text{ k}\Omega\left(\frac{0.75}{0.5}\right) = 6\text{ k}\Omega$$

20 V p-p INPUT: BW(-3dB) = 230 kHz, DC OUTPUT (AVG.) = 3.2 V
1 VOLT p-p INPUT: BW(-3dB) = 130 kHz, DC OUTPUT (AVG.) = 160 mV



Top Trace: Output signal (2 V/div.)
Bottom Trace: Input signal (10 V/div.)
Time base on both traces: 0.2 ms/div.

Fig. 23 - CA5130 single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

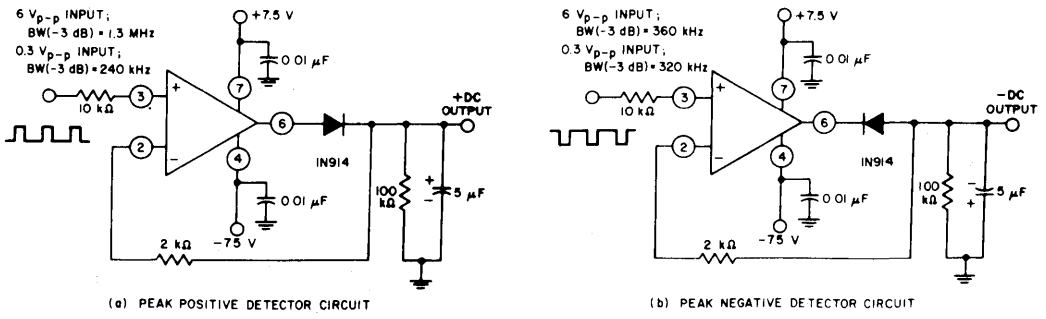


Fig. 24 - CA5130 peak-detector circuits.

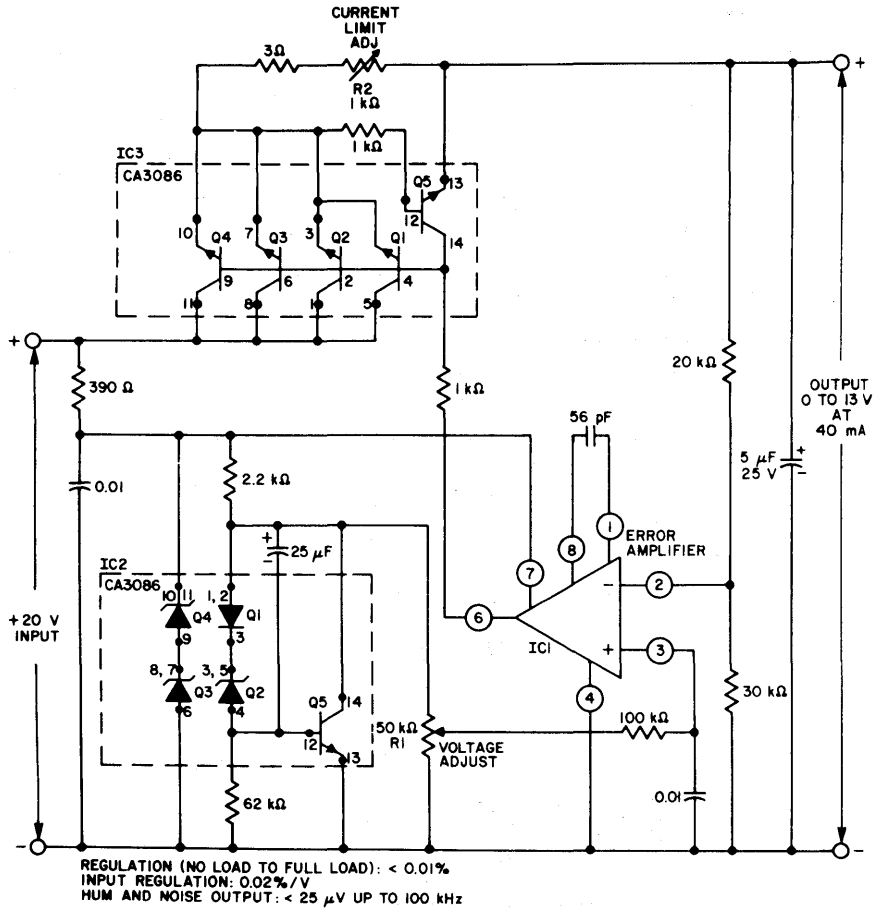


Fig. 25 - CA5130 voltage regulator circuit (0 to 13 V at 40 mA).

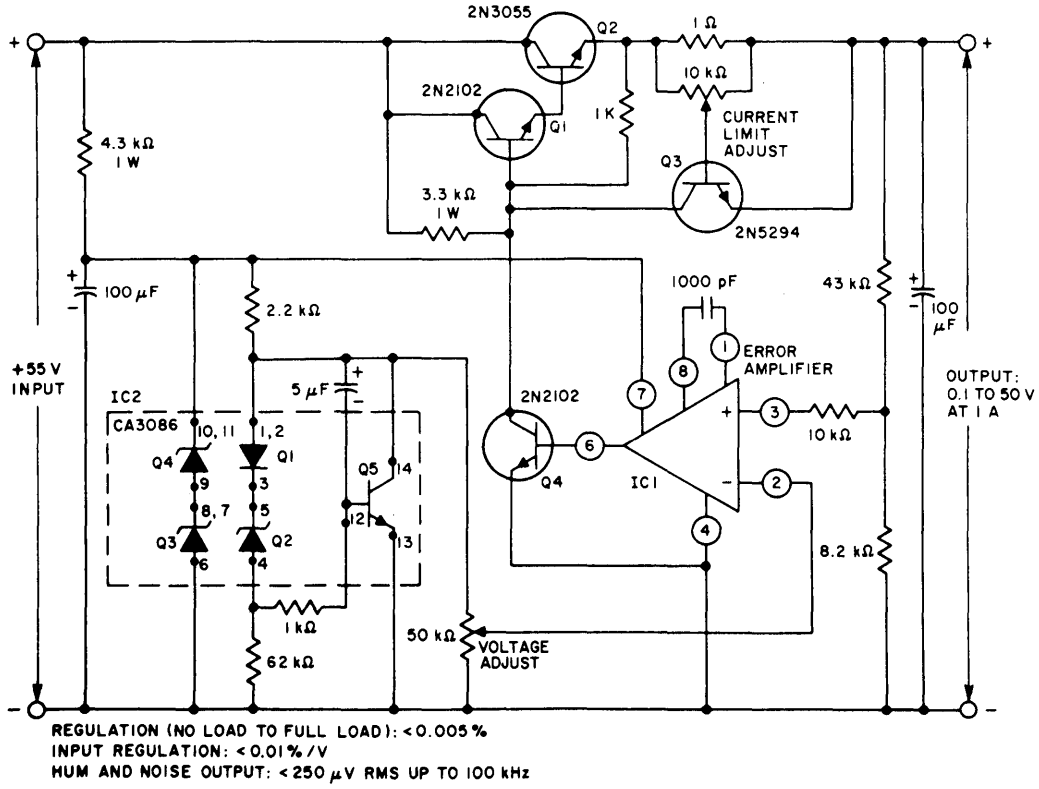
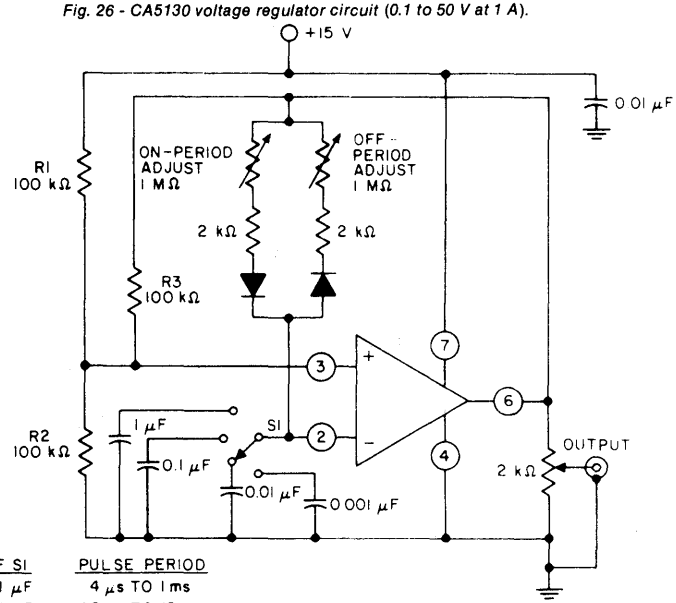


Fig. 26 - CA5130 voltage regulator circuit (0.1 to 50 V at 1 A).



FREQUENCY RANGE

POSITION OF S1	PULSE PERIOD
0.001 μF	4 μs TO 1 ms
0.01 μF	40 μs TO 10 ms
0.1 μF	0.4 ms TO 100 ms
1 μF	4 ms TO 1 s

Fig. 27 - CA5130 pulse generator (astable multivibrator) with provisions for independent control of "ON" and "OFF" periods.

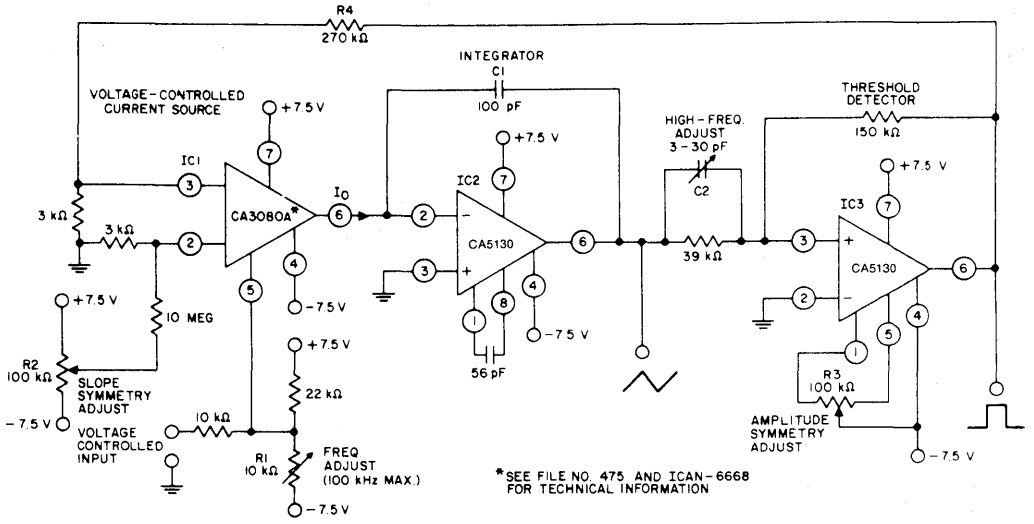


Fig. 28 - Function generator (frequency can be varied 1,000,000/1 with a single control).

Operation with Output-Stage Power-Booster

The current-sourcing and -sinking capability of the CA5130 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 29, three CMOS transistor-pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA5130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA5130 output stage by about 2.5X.

The amplifier circuit in Fig. 29 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (-3 dB) is 50 kHz.

*See File No. 619 for technical information.

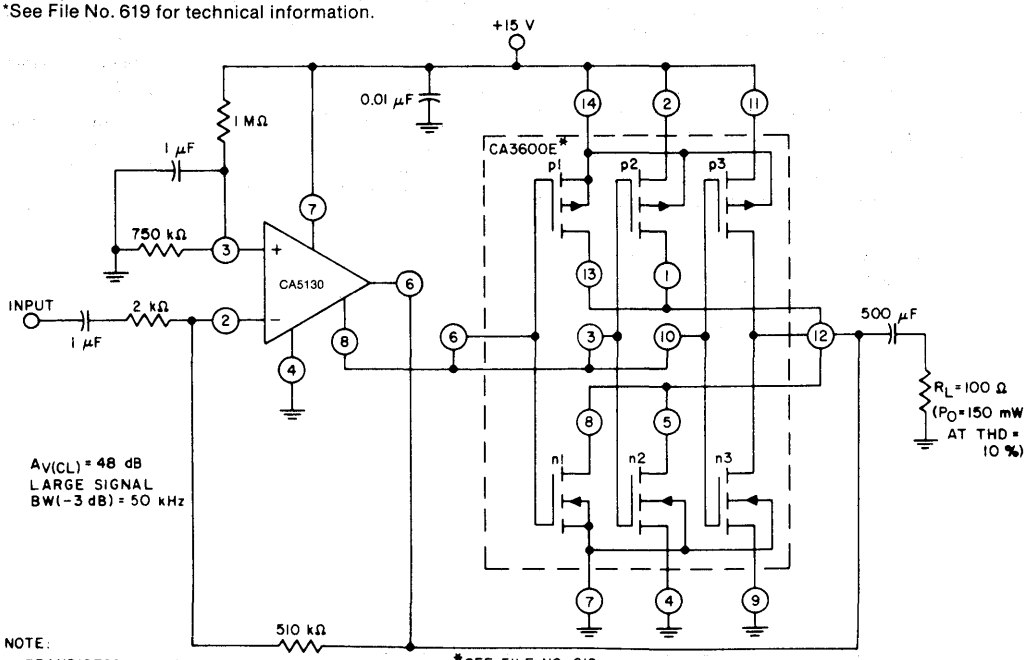


Fig. 29 - CMOS transistor array (CA3600E) connected as power-booster in the output stage of the CA5130.

May 1990

BiMOS Microprocessor Operational Amplifiers

With MOSFET Input/CMOS Output

Features:

- *MOSFET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 x 10^{12}Ω) typ.
  very low I_I = 5 pA typ. at 15 V operation
  = 2 pA typ. at 5 V operation
- *Common-mode input voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *CMOS output stage permits signal swing to either (or both) supply rails*
- *CA5160A, CA5160 5V have full military temperature range guaranteed specifications*
- *CA5160A, CA5160 are guaranteed to operate down to 4.5 V for AOL*
- *CA5160A, CA5160 are guaranteed up to +7.5*

Applications:

- *Ground referenced single supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long duration timers/monostables*
- *Ideal interface with digital CMOS*
- *High input impedance wideband amplifiers*
- *Voltage followers (e.g. follower for single supply D/A converter)*
- *Wien-Bridge oscillators*
- *Voltage controlled oscillators*
- *Photo diode sensor amplifiers*
- *5 V logic systems*
- *Microprocessors interface*

CA5160A and CA5160 are integrated circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA5160 series circuits are frequency compensated versions of the popular CA5130 series. They are designed and guaranteed to operate in microprocessors or logic systems that use +5 V supplies.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very high input impedance, very low input current, and exceptional speed performance. The use of PMOS field effect transistors in the input stage results in common-mode input voltage capability down to 0.5 volt below the negative supply terminal, an important attribute in single supply applications.

A complementary symmetry MOS (CMOS) transistor pair, capable of swinging the output voltage to within 10 millivolts of either supply voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5160 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA5160 Series is supplied in standard 8-lead TO-5 style packages (T suffix) and 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA5160 is available in chip form (H suffix). They have guaranteed specifications for 5 V operation over the full military temperature range of -55°C to +125°C.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE
INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC
INPUT VOLTAGE ..... (V^+ +8 V) to (V^- -0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK -
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate linearly 6.67 mW/°C
WITH HEAT SINK -
UP TO 90°C ..... 1 W
ABOVE 90°C ..... Derate linearly 16.7 mW/°C

TEMPERATURE RANGE:
OPERATING (All Types) ..... -55 to +125°C
STORAGE (All Types) ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT
DURATION* ..... INDEFINITE
LEAD TEMPERATURE
(DURING SOLDERING):
AT DISTANCE 1/16 ± 1/32 INCH
(1.59 ± 0.79 MM) FROM CASE
FOR 10 SECONDS MAX ..... +265°C

*Short circuit may be applied to ground or to either supply.

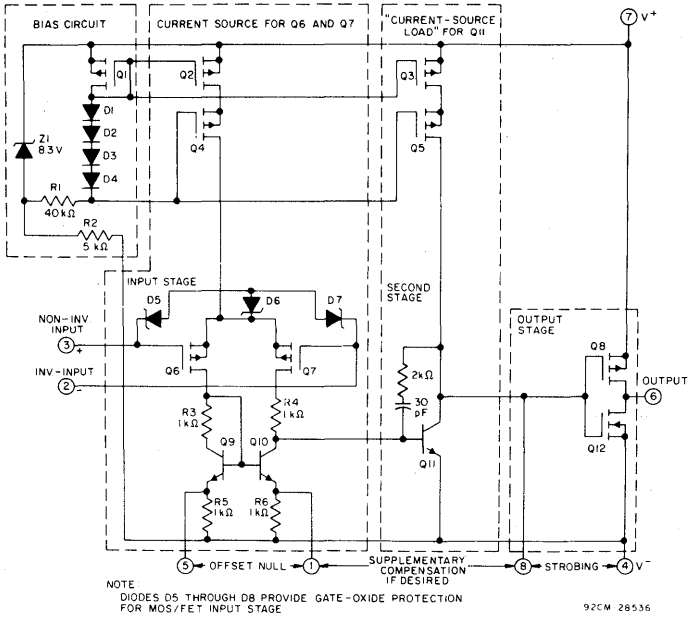
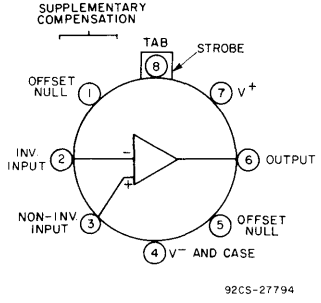
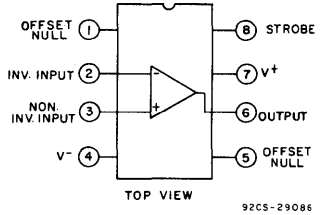


Fig. 1 — Schematic diagram of the CA5160 Series.



S and T Suffixes



CA5160 Series devices have an on-chip frequency-compensation network. Supplementary phase-compensation or frequency roll-off (if desired) can be connected externally between terminals 1 and 8.

E Suffix

Fig. 2 — Functional diagrams of the CA5160 Series.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 5 V, V^- = 0 V

CHARACTERISTIC		LIMITS						UNITS
		CA5160A			CA5160			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage V_O = 2.5 V	V_{IO}	—	1.5	4	—	2	10	mV
Input Offset Current V_O = 2.5 V	I_{IO}	—	0.1	5	—	0.1	10	pA
Input Current V_O = 2.5 V	I_I	—	2	10	—	2	15	pA
Common-Mode Rejection Ratio								
V_{CM} = 0 to 1 V	C_{MRR}	75	87	—	70	80	—	dB
V_{CM} = 0 to 2.5 V	C_{MRR}	60	69	—	60	69	—	dB
Input Common-Mode Voltage Range								
	V_{ICR}^+	2.5	2.8	—	2.5	2.8	—	V
	V_{ICR}^-	—	-0.5	0	—	-0.5	0	V
Power-Supply Rejection Ratio ΔV^+ = 1 V; ΔV^- = 1 V	P_{SRR}	60	75	—	55	67	—	dB
Large-Signal Voltage Gain*	A_{OL}							
V_O = 0.1 to 4.1 V	$R_L = \infty$	100	117	—	95	117	—	dB
V_O = 0.1 to 3.6 V	R_L = 10k	90	102	—	85	102	—	dB
Source Current V_O = 0 V	I_{SOURCE}	1.0	3.1	4.0	1.0	2.2	4.0	mA
Sink Current V_O = 5 V	I_{SINK}	1.0	1.6	4.0	1.0	3.4	4.0	mA
Output Voltage	V_{OUT}							
$R_L = \infty$	V_{OM}^+	4.99	5	—	4.99	5	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
R_L = 10k	V_{OM}^+	4.4	4.7	—	4.4	4.7	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
R_L = 2k	V_{OM}^+	2.5	3.3	—	2.5	3.3	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
Supply Current	I_{SUPPLY}							
V_O = 0 V		—	50	100	—	50	100	μA
V_O = 2.5 V	I_{SUPPLY}	—	320	400	—	320	400	μA

*For V^+ = 4.5 V and V^- = GND; V_{OUT} = 0.5 V to 3.2 V at R_L = 10k

ELECTRICAL CHARACTERISTICS at T_A = -55°C to +125°C, V^+ = 5 V, V^- = 0 V

CHARACTERISTIC		LIMITS						UNITS
		CA5160A			CA5160			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage V_O = 2.5 V	V_{IO}	—	2	10	—	3	15	mV
Input Offset Current V_O = 2.5 V	I_{IO}	—	0.1	5	—	0.1	10	nA
Input Current V_O = 2.5 V	I_I	—	2	10	—	2	15	nA
Common-Mode Rejection Ratio								
V_{CM} = 0 to 1 V	C_{MRR}	60	80	—	60	80	—	dB
V_{CM} = 0 to 2.5 V	C_{MRR}	55	80	—	50	75	—	dB
Input Common-Mode Voltage Range	V_{ICR}^+	2.5	2.8	—	2.5	2.8	—	V
	V_{ICR}^-	—	-0.5	0	—	-0.5	0	V
Power-Supply Rejection Ratio $\Delta^+ = V^+ = 2$ V	P_{SRR}	45	65	—	40	60	—	dB
Large-Signal Voltage Gain*	A_{OL}							
V_O = 0.1 to 4.1 V	$R_L = \infty$	94	110	—	90	110	—	dB
V_O = 0.1 to 3.6 V	R_L = 10k	80	100	—	75	100	—	dB
Source Current V_O = 0 V	I_{SOURCE}	0.6	2.2	5.0	0.6	—	5.0	mA
Sink Current V_O = 5 V	I_{SINK}	0.6	1.15	5.0	0.6	—	5.0	mA
Output Voltage	V_{OUT}							
$R_L = \infty$	V_{OM}^+	4.99	5	—	4.99	5	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
R_L = 10k	V_{OM}^+	4.0	4.3	—	4.0	4.3	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
R_L = 2k	V_{OM}^+	2.0	2.5	—	2.0	2.5	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
Supply Current	I_{SUPPLY}							
V_O = 0 V		—	170	220	—	170	220	μA
V_O = 2.5 V	I_{SUPPLY}	—	410	500	—	410	500	μA

*For V^+ = 4.5 V and V^- = GND; V_{OUT} = 0.5 V to 3.2 V at R_L = 10k

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 15V, V^- = 0 V (Unless Otherwise Specified)

CHARACTERISTIC		LIMITS						UNITS
		CA5160A (T, S, E)			CA5160 (T, S, E)			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage $V^{\pm}$ = ±7.5 V	$\lvert V_{IO} \rvert$	—	2	5	—	6	15	mV
Input Offset Current $V^{\pm}$ = ±7.5 V	$\lvert I_{IO} \rvert$	—	0.5	20	—	0.5	30	pA
Input Current $V^{\pm}$= ±7.5 V	I_I	—	5	30	—	5	50	pA
Large-Signal Voltage Gain	A_{OL}	50k	320k	—	50k	320k	—	V/V
V_O = 10 V_{p-p}, R_L = 2 kΩ		94	110	—	94	110	—	dB
Common-Mode Rejection Ratio	C_{MRR}	80	95	—	70	90	—	dB
Common-Mode Input Voltage Range	V_{ICR}	10	-0.5 to 12	0	10	-0.5 to 12	0	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$ = ±7.5 V	P_{SRR}	—	32	150	—	32	320	μV/V
Maximum Output Voltage								V
R_L = 2 kΩ	V_{OM}^+	12	13.3	—	12	13.3	—	
	V_{OM}^-	—	0.002	0.01	—	0.002	0.01	
R_L = ∞	V_{OM}^+	14.99	15	—	14.99	15	—	
	V_{OM}^-	—	0	0.01	—	0	0.1	
Maximum Output Current								mA
I_{OM}^+ (Source) @ V_O = 0 V	I_{OM}^+	12	22	45	12	22	45	
I_{OM}^- (Sink) @ V_O = 15 V	I_{OM}^-	12	20	45	12	20	45	
Supply Current	I^+							mA
V_O = 7.5 V	R_L = ∞	—	10	15	—	10	15	
V_O = 0 V	I^+ R_L = ∞	—	2	3	—	2	3	
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$*		—	6	—	—	8	—	μV/°C

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC		TEST CONDITIONS		CA5160/ CA5160A (T, S, E)	UNITS
		V^+ = +7.5 V, V^- = -7.5 V, T_A = 25°C (Unless Otherwise Specified)			
Input Offset Voltage Adjustment Range		10 kΩ across Terms 4 and 5 or 4 and 1		±22	mV
Input Resistance	R_I			1.5	TΩ
Input Capacitance	C_I	f = 1 MHz		4.3	pF
Equivalent Input Noise Voltage	e_n	BW = 0.2 MHz	R_S = 1 MΩ R_S = 10 MΩ	40 50	μV
Equivalent Input Noise Voltage	e_n	R_S = 100 Ω	1 kHz 10 kHz	72 30	$nV\sqrt{Hz}$
Unity Gain Crossover Frequency	f_T			4	MHz
Slew Rate	SR:			10	V/μs
Transient Response: Rise Time	t_r	C_L = 25 pF, R_L = 2 kΩ (Voltage Follower)		0.09	μs
Overshoot				10	%
Setting Time (4 V_{p-p} Input to <0.1%)				1.8	μs

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA5160 series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA5160 series circuits are ideal for single-supply operation. Three class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA5160. A biasing circuit provides two potentials for common use in the first and second stages. Terminals 8 and 1 can be used to supplement the internal phase compensation network if additional phase compensation or frequency roll-off is desired. Terminals 8 and 4 can also be used to strobe the output stage into a low quiescent current state. When Terminal 8 is tied to the negative supply rail (Terminal 4) by mechanical or electrical means, the output potential at Terminal 6 essentially rises to the positive supply-rail potential at Terminal 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

Input Stages — The circuit of the CA5160 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terminals 1 and 5 and the potentiometer slider arm to Terminal 4.

Cascode-connected PMOS transistors Q2, Q4, are the constant-current source for the input stage. The biasing curcuit for the constant-current source is subsequently described. The small diodes D5 through D7 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

Second-State — Most of the voltage gain in the CA5160 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS tranistors is described later. Miller Effect compensation (roll off) is accomplished by means of the 30-pf capacitor and 2-kΩ resistor connected between the base and collector of transistor Q11. These internal components provide sufficient compensation for unity gain operation in most applications. However, additional compensation, if desired, may be used between Terminals 1 and 8.

Bias-Source Circuit — At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Terminal 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Terminal 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage. Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ration (PSRR) at total supply voltages below 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage — The output stage consists of a drain-loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance loads, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feedback for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 per cent accuracy levels, including the negative supply rail.

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† For general information on the characteristics CMOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "CMOS Transistor Array".

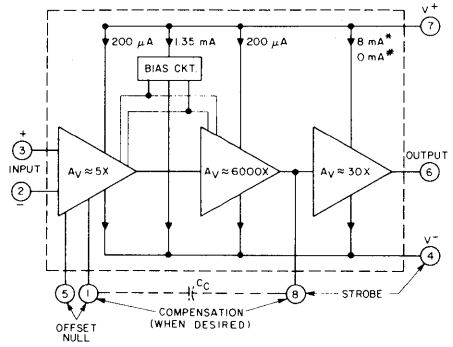


Fig. 3 — Block diagram of the CA5160 Series.

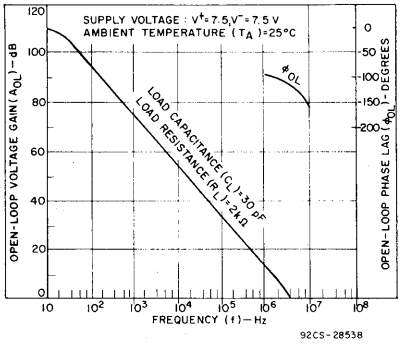


Fig. 4 — Open-loop voltage gain and phase shift vs. frequency.

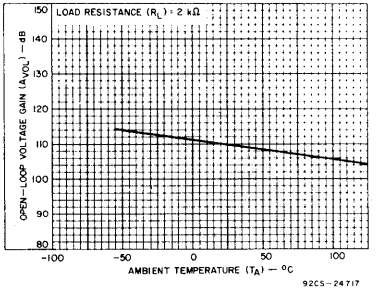


Fig. 5 — Open-loop gain vs. temperature.

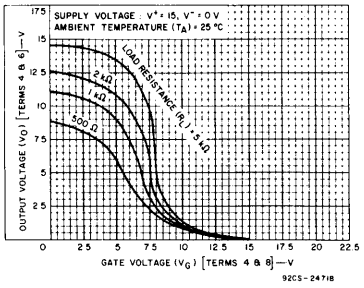


Fig. 6 — Voltage transfer characteristics of CMOS output stage.

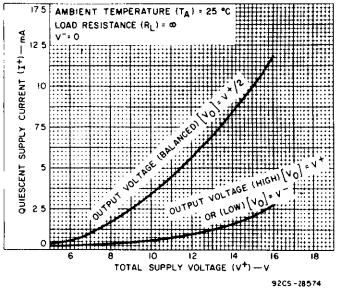


Fig. 7 — Quiescent supply current vs. supply voltage.

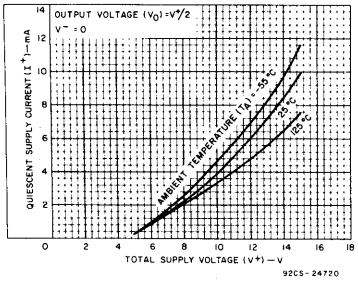


Fig. 8 — Quiescent supply current vs. supply voltage at several temperatures.

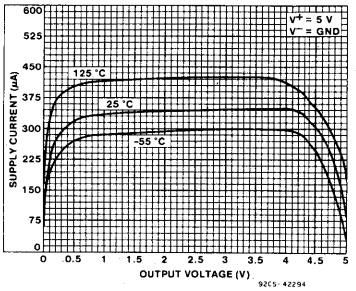


Fig. 9 — Supply current vs. output voltage.

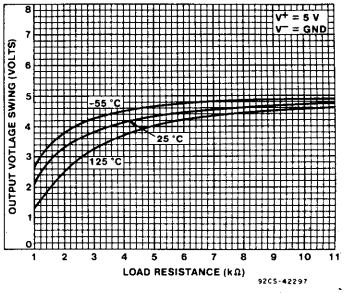


Fig. 10 — Output voltage swing vs. load resistance.

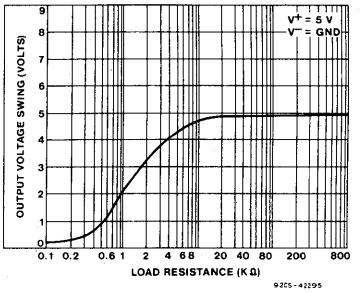


Fig. 11 — Output swing vs. load resistance.

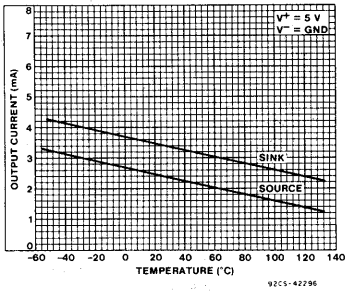


Fig. 12 — Output current vs. temperature.

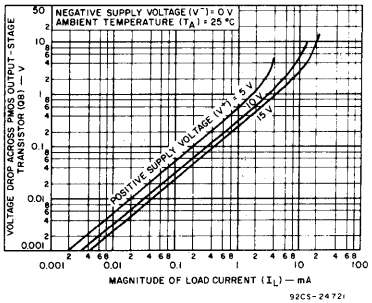


Fig. 13 — Voltage across PMOS output transistor (Q8) vs. load current.

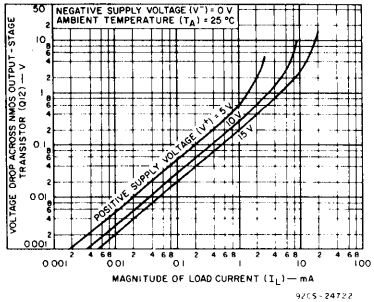


Fig. 14 — Voltage across NMOS output transistor (Q12) vs. load current.

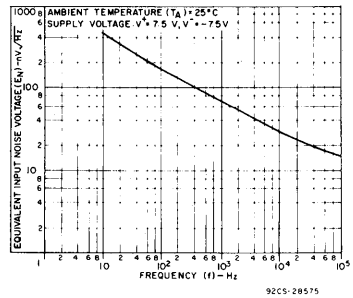


Fig. 15 — Equivalent noise voltage vs. frequency.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terminals 1 and 5 and with the potentiometer slider arm connected to Terminal 4. A fine offset-null adjustment usually can be affected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA5160 Series Op-Amps is typically 5 pA at T_A = 25°C when Terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig. 16 contains data showing the variation of input

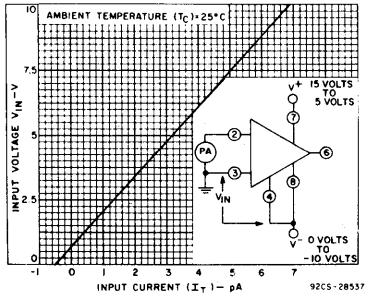


Fig. 16 — CA5160 input current vs. common-mode voltage.

current as a function of common-mode input voltage at T_A = 25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input curcuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA5160 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Input-Current Variation with Temperature

The input current of the CA5160 Series circuits is typically 5 pA at 25°C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig. 17 provides data on the typical variation of input bias current as a function of temperature in the CA5160.

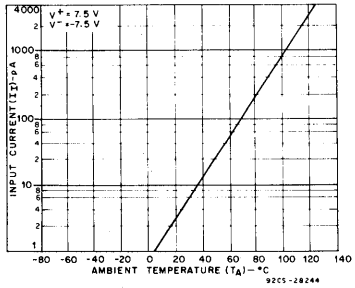


Fig. 17 — Input current vs. ambient temperature.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA5160. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA5160 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across Terminals 2 and 3. Fig. 18 shows typical data pertinent to shifts in offset voltage encountered with CA5160 devices in TO-5 packages during life testing. At lower temperatures (TO-5 and plastic) for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an oper-

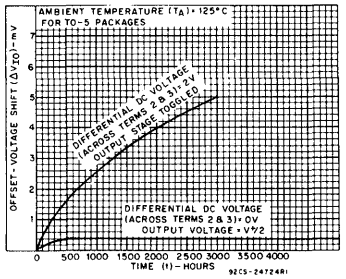


Fig. 18 — Typical incremental offset-voltage shift vs. operating life.

ational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output state is "toggled", e.g., as in comparator applications.

Power-Supply Considerations

Because the CA5160, is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single-and dual-supply service. Figs. 19 (a) and 19 (b) show the CA5160 connected for both dual-and-single-supply operation.

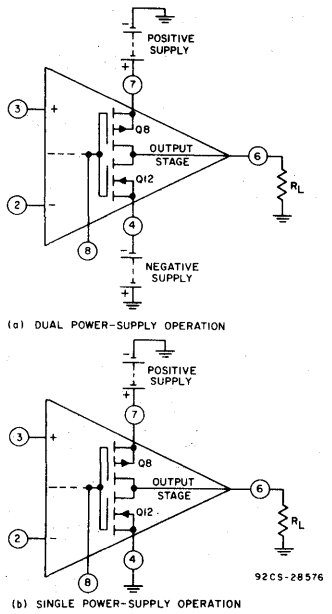


Fig. 19 — CA5160 output stage in dual and single power-supply operation

Dual-supply operation: When the output voltage at Terminal 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is at $V^+/2$, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA5160 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cutoff (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Terminal 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceding stages in the CA5160, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 15(a) shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Terminal 8 down to that of Terminal 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Terminal 6 and ground in the circuit of Fig. 19(b). Let it further be assumed again that the input-terminal bias (Terminals 2 and 3) is such that the output terminal (No. 6) voltage is $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply voltages. Fig. 6 shows the voltage-transfer characteristics of the output state for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA5160 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 40 μV when the test-circuit amplifier of Fig. 20 is operated at a total supply

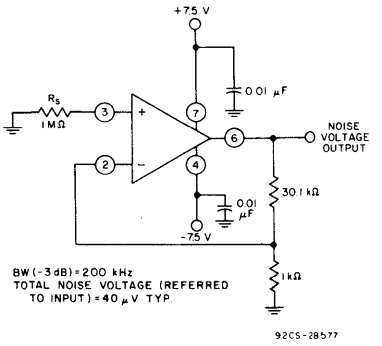


Fig. 20 — CA5160 Test-circuit amplifier (30-dB gain) used for wideband noise measurements.

voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

TYPICAL APPLICATIONS

Voltage Followers

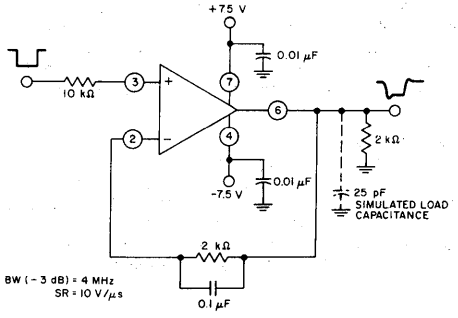
Operational amplifiers with very high input resistances, like the CA5160, are particularly suited to service as voltage followers. Fig. 21 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA5160 in a split-supply configuration.

A voltage follower, operated from a single-supply, is shown in Fig. 22 together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 22b with input-signal ramping. The waveforms in Fig. 22c show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 22c also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA5160 in a single-supply voltage-follower application.

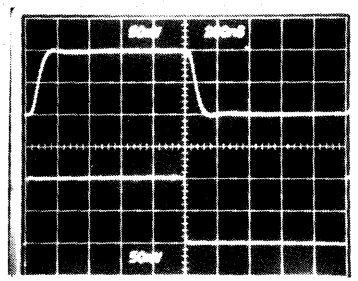
9-Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig. 23. This system combines the concepts of multiple-switch CMOS IC's, a low-cost ladder network of discrete metal-oxide-film resistors, a CA5160 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 23.

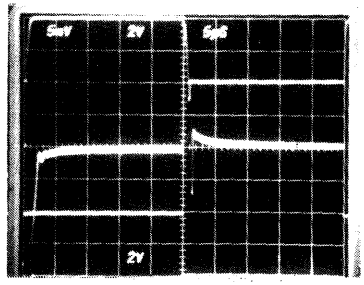
*"Digital-to-Analog Conversion Using the RCA-CD4007A CMOS IC", Application Note ICAN-6080.



(a)

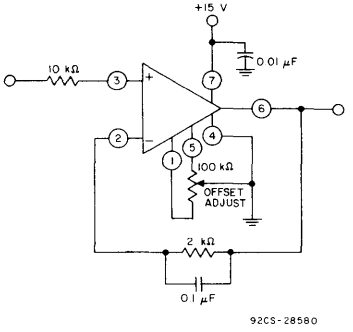


(b) Small Signal Response
Top Trace: Output
Bottom Trace: Input

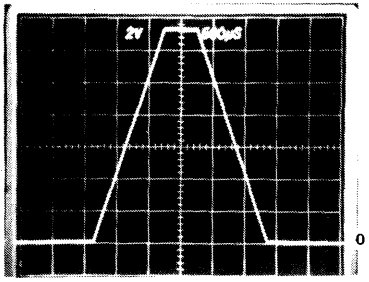


(c) Input-Output Difference Signal Showing Setting Time
Top Trace: Output Signal
Center Trace: Difference Signal 5 mV/div
Bottom Trace: Input Signal

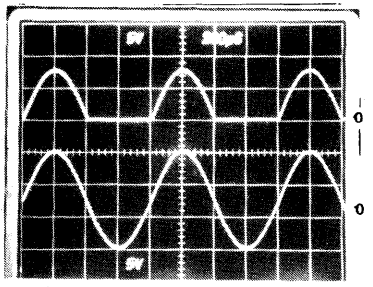
Fig. 21 — Split-supply voltage follower with associated waveforms for CA5160.



(a)



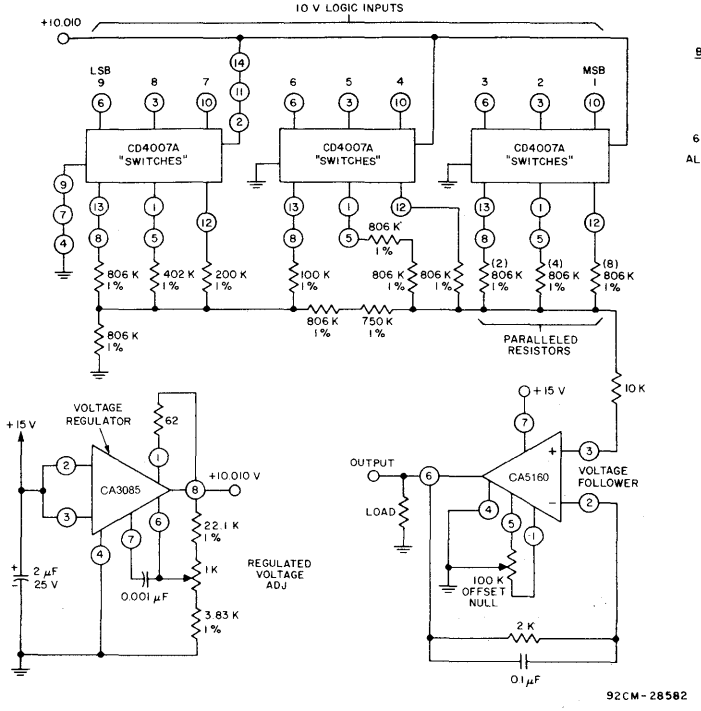
(b) Output signal with input-signal ramping.



92CS-28581R1

(c) Output-Waveform with Ground-Reference
Sine-Wave Input
Top Trace: Output
Bottom Trace: Input

Fig. 22 — CA5160 Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080.)



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS.

ALL RESISTANCES IN OHMS

Fig. 23 — 9-bit DAC using CMOS digital switches and CA5160.

The circuit uses an R/2R voltage-ladder network, with the output-potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R newtork at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one per cent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA5160 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the CMOS building blocks simplifies the design of DAC systems tailored to particular needs.

Error-Amplifier in Regulated Power Supplies

The CA5160 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero.

The circuit shown in Fig. 24 uses a CA5160 as an error amplifier in a continuously adjustable 1-ampere power supply. One of the key features of this circuit is its ability to regulate down to the vicinity of zero volts with only one dc power supply input.

An RC network, connected between the base of the output drive transistor and the input voltage, prevents "turn-on overshoot", a condition typical of many operational-amplifier regulator circuits. As the amplifier becomes operational, this RC network ceases to have any influence on the regulator performance.

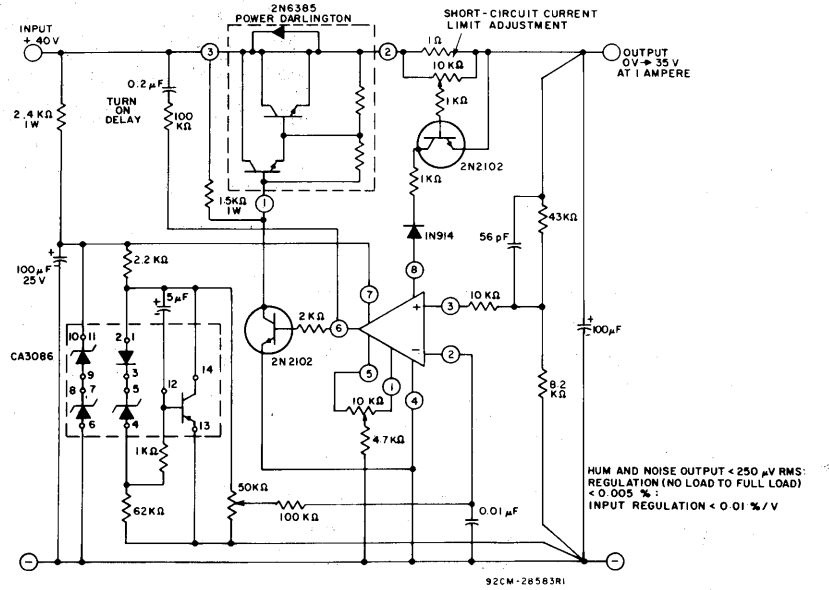


Fig. 24 — CA5160 Voltage regulator circuit (0.1 to 35 V at 1 A).

Precision Voltage-Controlled Oscillator

The circuit diagram of a precision voltage-controlled oscillator is shown in Fig. 25. The oscillator operates with a tracking error in the order of 0.02 percent and a temperature coefficient of 0.01%/°C. A multivibrator (A_1) generates pulses of constant amplitude (V) and width (T_2). Since the output (terminal 6) of A_1 (a CA5130) can swing within about 10 millivolts of either supply-rail, the output pulse amplitude (V) is essentially equal to V+. The average output voltage ($E_{avg} = V T_2/T_1$) is applied to the non-inverting input terminal of comparator A_2 (a CA5160) via an integrating network R_3, C_2. Comparator A_2 operates to establish circuit conditions such that $E_{avg} = V1$. This circuit condition is accomplished by feeding an output signal from terminal 6 of A_2 through R_4, D_4 to the inverting terminal (terminal 2) of A_1, thereby adjusting the multivibrator interval, T_3.

Voltmeter With High Input Resistance

The voltmeter circuit shown in Fig. 26 illustrates an application in which a number of the CA5160 characteristics are exploited. Range-switch SW1 is ganged between input and output circuitry to permit selection of the proper output voltage for feedback to Terminal 2 via 10 KΩ current-limiting resistor. The circuit is powered by a single 8.4-volt mercury battery. With zero input signal, the circuit consumes somewhat less than 500 microamperes plus the meter current required to indicate a given voltage. Thus, at full-scale input, the total supply current rises to slightly more than 1500 microamperes.

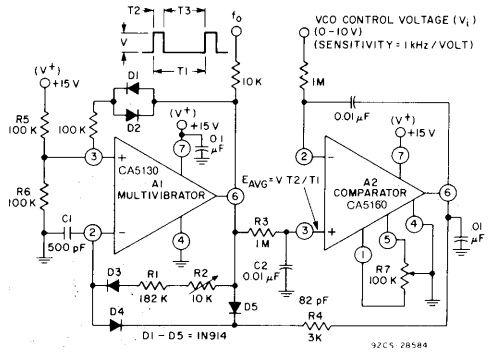


Fig. 25 — Voltage-controlled oscillator.

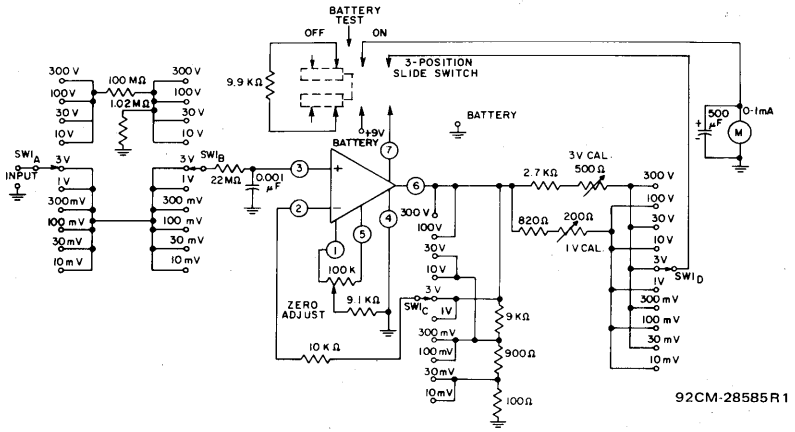


Fig. 26 — CA5160A high-input-resistance DC voltmeter

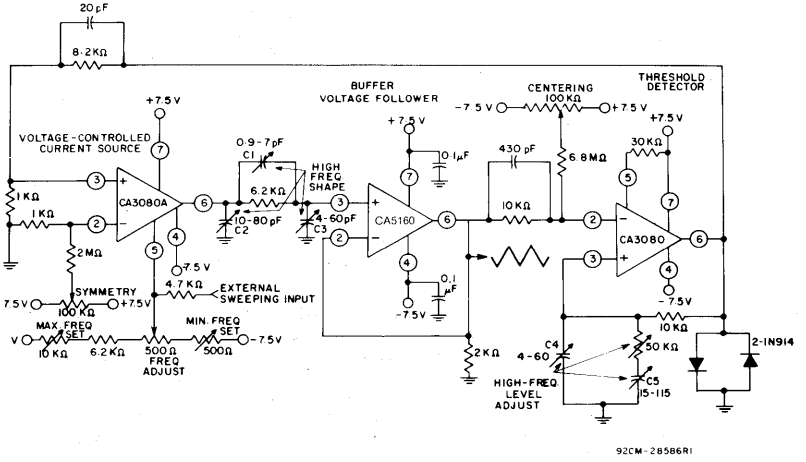


Fig. 27(a) — CA5160 1,000,000/1 single-control function generator — 1 MHz to 1 Hz.

Function Generator

A function generator having a wide tuning range is shown in Fig. 27. The adjustment range, in excess of 1,000,000/1, is accomplished by a single potentiometer. Three operational amplifiers are utilized: a CA5160 as a voltage follower, a CA3080 as a high-speed comparator, and a second CA3080A as a programmable current source. Three variable capacitors C1, C2, and C3 shape the triangular signal between 500 kHz and 1 MHz. Capacitors C4, C5 and the trimmer potentiometer in series with C5 maintain essentially constant (±10%) amplitude up to 1 MHz.

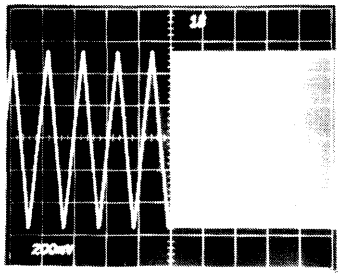
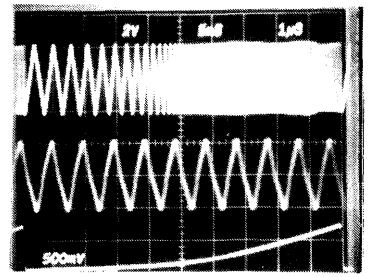


Fig. 27(b) — Two-tone output signal from the function generator. A square-wave signal modulates the external sweeping input to produce 1 Hz and 1 MHz, showing the 1,000,000/1 frequency range of the function generator.

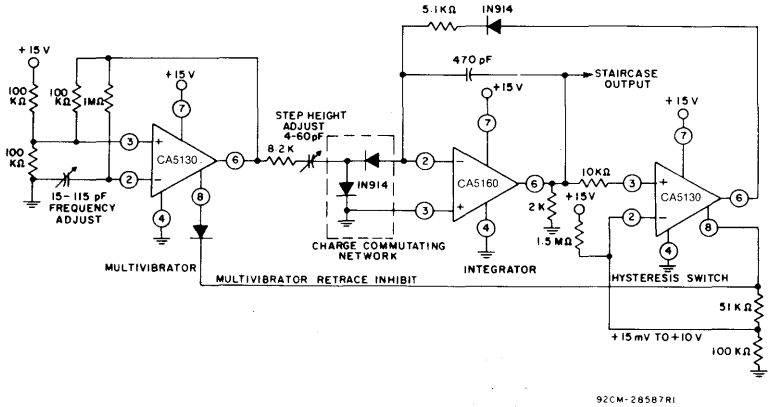


92CS-28588

Fig. 27(c) — Triple-trace of the function generator sweeping to 1 MHz. The bottom trace is the sweeping signal and the top trace is the actual generator output. The center trace displays the 1 MHz signal via delayed oscilloscope triggering of the upper swept output signal.

Staircase Generator

Fig. 28 shows a staircase generator circuit utilizing three CMOS operational amplifiers. Two CA5130's are used; one as a multivibrator, the other as a hysteresis switch. The third amplifier, a CA5160, is used as a linear staircase generator.



92CM-28587R1

Fig. 28(a) — Staircase generator circuit utilizing three CMOS operational amplifiers.

Picoammeter Circuit

Fig. 29 is a current-to-voltage converter configuration utilizing a CA5160 and CA3140 to provide a picoampere meter for ±3 pA full-scale meter deflection. By placing Terminals 2 and 4 of the CA5160 at ground potential, the CA5160 input is operated in the "guarded mode". Under this operating condition, even slight leakage reistance present between Terminals 3 and 2 or between Terminals 3 and 4 would result in zero voltage across this leakage resistance, thus substantially reducing the leakage current.

If the CA5160 is operated with the same voltage on input Terminals 3 and 2 as on Terminal 4, a further reduction in the input current to the less than one picoampere level can be achieved as shown in Fig. 16.

To further enhance the stability of this circuit, the CA5160 can be operated with its output (Terminal 6) near ground, thus markedly reducing the dissipation by reducing the supply current to the device.

The CA3140 stage serves as a X100 gain stage to provide the required plus and minus output swing for the meter and

feedback network. A 100-to-1 voltage divider network consisting of a 9.9-KΩ resistor in series with a 100-ohm resistor sets the voltage at the 10-KMΩ resistor (in series with Terminal 3) to ±30 mV full-scale deflection. This 30-mV signal results from ±3 volts appearing at the top of the voltage divider network which also drives the meter circuitry.

By utilizing a switching technique in the meter circuit and in the 9.9 KΩ and 100-ohm network similar to that used in voltmeter circuit shown in Fig. 26, a current range of 3 pA to 1 nA full scale can be handled with the single 10-KMΩ resistor.

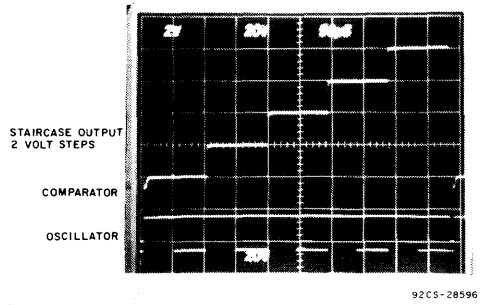


Fig. 28 (b) — Staircase Generator Waveform
Top Trace: Staircase Output
2 Volt Steps
Center Trace: Comparator
Bottom Trace: Oscillator

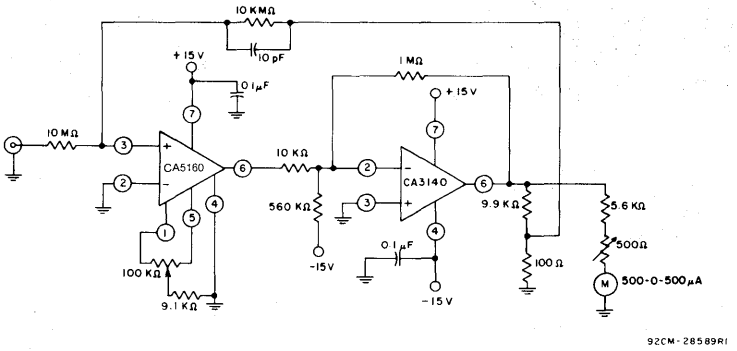


Fig. 29 — Current-to-voltage converter to provide a picoammeter with ± 3 pA full-scale deflection.

Single-Supply Sample-and-Hold System

Fig. 30 shows a single-supply sample-and-hold system using a CA5160 to provide a high input impedance and an input-voltage range of 0 to 10 volts. The output from the input buffer integrator network is coupled to a CA3080A. The CA3080A functions as a strobeable current source for the CA3140 output integrator and storage capacitor. The CA3140 was chosen because of its low output impedance and constant gain-bandwidth product. Pulse "droop" during the hold interval can be reduced to zero by adjusting the 100-KΩ bias-voltage potentiometer on the positive input of the CA3140. This zero adjustment sets the CA3080A output voltage at its zero current position. In this sample-and-hold circuit it is essential that the amplifier bias current be reduced to zero to minimize output signal current during the hold mode. Even with 320 mV at the amplifier bias circuit terminal (5) at least ± 100 pA of output current will be available.

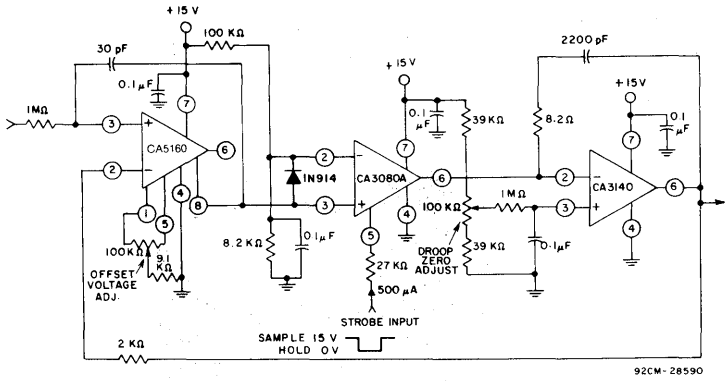
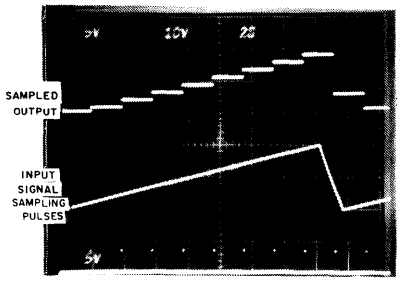
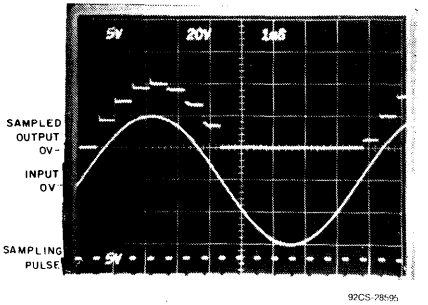


Fig. 30(a) — Single-supply sample-and-hold system— input 0-to-10 volts.



(b) — Sample-and-hold waveform.
Top Trace: Sampled Output
Center Trace: Input Signal
Bottom Trace: Sampling Pulses



(c) — Sample-and-hold waveform.
Top Trace: Sampled Output
Center Trace: Input
Bottom Trace: Sampling Pulse

Wien Bridge Oscillator

A simple, single-supply Wien Bridge oscillator using a CA5160 is shown in Fig. 31. A pair of parallel-connected 1N914 diodes comprise the gain-setting network which standardizes the output voltage at approximately 1.1 volts. The 500-ohm potentiometer is adjusted so that the oscillator will always start and the oscillation will be maintained. Increasing the amplitude of the voltage may lower the threshold level for starting and for sustaining the oscillation, but will introduce more distortion.

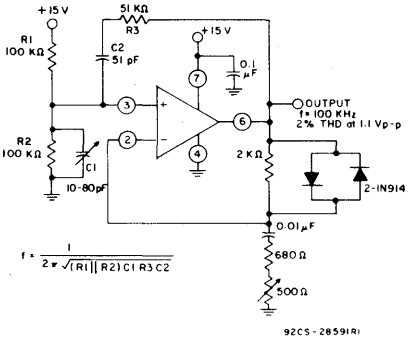


Fig. 31 — CA5160 Single-supply Wien Bridge oscillator.

Operation with Output-Stage Power-Booster

The current sourcing and sinking capability of the CA5160 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 32, three CMOS transistor-pairs in a single CA3600 IC array are shown parallel-connected with the output stage in the CA5160. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA5160 output stage by about 2.5X.

The amplifier circuit in Fig. 32 employs feedback to establish a closed-loop gain of 20 dB. The typical large-signal-bandwidth (-3 dB) is 190 kHz.

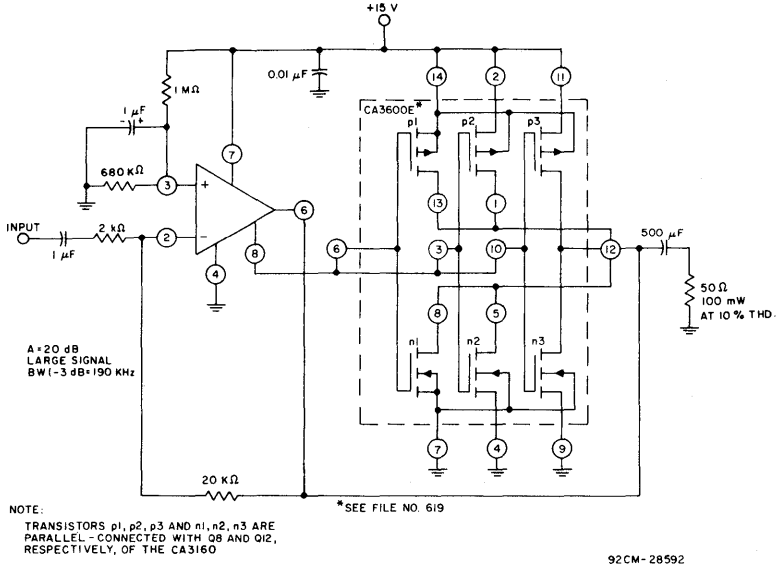


Fig. 32 — CMOS transistor array (CA3600E) connected as power booster in the output stage of the CA5160.

May 1990

BiMOS Microprocessor Operational Amplifiers

With MOSFET Input/CMOS Output

Features:

- *MOSFET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 x 10^{12}Ω) typ.
  very low I_I = 5 pA typ. at 15 V operation
  = 2 pA typ. at 5 V operation
- *Ideal for single-supply applications*
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *CMOS output stage permits signal swing to either (or both) supply rails*
- *CA5260A, CA5260 5V have full military temperature range guaranteed specifications*
- *CA5260A, CA5260 are guaranteed to operate down to V_T = 4.5 V for AOL*
- *Fully guaranteed to operate at -55°C to +125°C at V+ = 5 V, V- = Gnd*

Applications:

- *Ground-referenced single supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *Ideal interface with digital CMOS*
- *High-input-impedance wideband amplifiers*
- *Voltage followers (e.g. follower for single-supply D/A converter)*
- *Voltage regulators (permits control of output voltage down to zero volts)*
- *Wien-Bridge oscillators*
- *Voltage-controlled oscillators*
- *Photo-diode sensor amplifiers*
- *5 V logic systems*
- *Microprocessors interface*

The CA5260A and CA5260 are integrated-circuit operational amplifiers that combine the advantage of both CMOS and bipolar transistors on a monolithic chip. The CA5260 series circuits are dual versions of the popular CA5160 series. They are designed and guaranteed to operate in microprocessors or logic systems that use +5 V supplies.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5260 Series circuits operate at supply voltages ranging from 4.5 to 16 volts, or ±2.25 to ±8 volts when using split supplies.

The CA5260 Series is supplied in standard 8-lead TO-5 style packages (T suffix) and 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA5260 is available in chip form (H suffix). The CA5260A and CA5260 are also available in the Mini-Dip 8-lead dual-in-line surface-mount plastic packages (M suffix).

The CA5260A, CA5260 have guaranteed specifications for 5 V operation over the full military-temperature range of -55°C to +125°C.

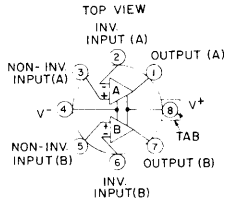
MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8V) to (V^- -0.5V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK -
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate Linearly 6.67 mW/°C
WITH HEAT SINK -
UP TO 90°C ..... 1 W
ABOVE 90°C ..... Derate Linearly 16.7 mW/°C
SMALL OUTLINE PACKAGE ..... 250°/W
TEMPERATURE RANGE:
OPERATING (all types) ..... -55 to +125°C
STORAGE (all types) ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION * ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max ..... +265°C

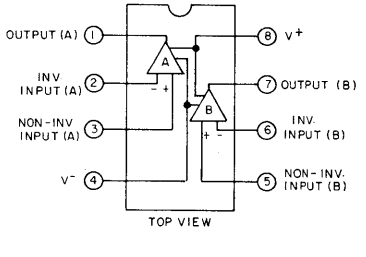
* Short circuit may be applied to ground or to either supply.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE
V^+ = 5 V, V^- = 0 V, T_A = 25°C (Unless Otherwise Specified)

CHARACTERISTIC		TEST CONDITIONS	TYPICAL VALUES		UNITS
			CA5260A	CA5260	
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I	f = 1 MHz	4.3	4.3	pF
Unity Gain Crossover Frequency	f_T		3	3	MHz
Slew Rate	SR	V_{OUT} = 2.5V_{P-P}	5	5	V/μs
Transient Response:	t_r	C_L = 25 pF			
Rise Time		R_L = 2 kΩ	0.09	0.09	μs
Overshoot		(Voltage Follower)	10	10	%
Settling Time (4 V_{p-p} Input to < 0.1%)			1.8	1.8	μs



S and T Suffixes
Pin compatible with the industry-standard 1458



E and M Suffixes
Pin compatible with the industry-standard 1458

Fig. 1 - Functional diagrams for the CA5260 series.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V^+ = 5 V, V^- = 0 V

CHARACTERISTIC		LIMITS						UNITS
		CA5260A			CA5260			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage V_O = 2.5 V	V_{IO}	—	1.5	4	—	2	15	mV
Input Offset Current V_O = 2.5 V	I_{IO}	—	1	10	—	1	10	pA
Input Current V_O = 2.5 V	I_I	—	2	15	—	2	15	pA
Common-Mode Rejection Ratio								
V_{CM} = 0 to 1 V	C_{MRR}	80	85	—	70	85	—	dB
V_{CM} = 0 to 2.5 V	C_{MRR}	50	55	—	50	55	—	dB
Input Common-Mode Voltage Range								
	V_{ICR}^+	2.5	3	—	2.5	3	—	V
	V_{ICR}^-	—	-0.5	0	—	-0.5	0	V
Power-Supply Rejection Ratio Δ^+ = 1 V; Δ^- = 1 V	P_{SRR}	75	84	—	70	84	—	dB
Large-Signal Voltage Gain*	A_{OL}							
V_O = 0.5 to 4 V	R_L = ∞	107	113	—	105	111	—	dB
V_O = 0.5 to 3.6 V	R_L = 10 k	83	86	—	80	86	—	dB
Source Current V_O = 0 V	I_{SOURCE}	1.75	2.2	—	1.75	2.2	—	mA
Sink Current V_O = 5 V	I_{SINK}	1.70	2	—	1.70	2	—	mA
Output Voltage	V_{OUT}							
R_L = ∞	V_{OM}^+	4.99	5	—	4.99	5	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
R_L = 10 k	V_{OM}^+	4.4	4.7	—	4.4	4.7	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
R_L = 2 k	V_{OM}^+	3	3.4	—	3	3.4	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
Supply Current	I_{SUPPLY}							
V_O = 0 V		—	1.60	2.0	—	1.60	2.0	mA
V_O = 2.5 V	I_{SUPPLY}	—	1.80	2.25	—	1.80	2.25	mA

*For V^+ = 4.5 V and V^- = Gnd; V_{OUT} = 0.5 V to 3.2 V at R_L = 10 k.

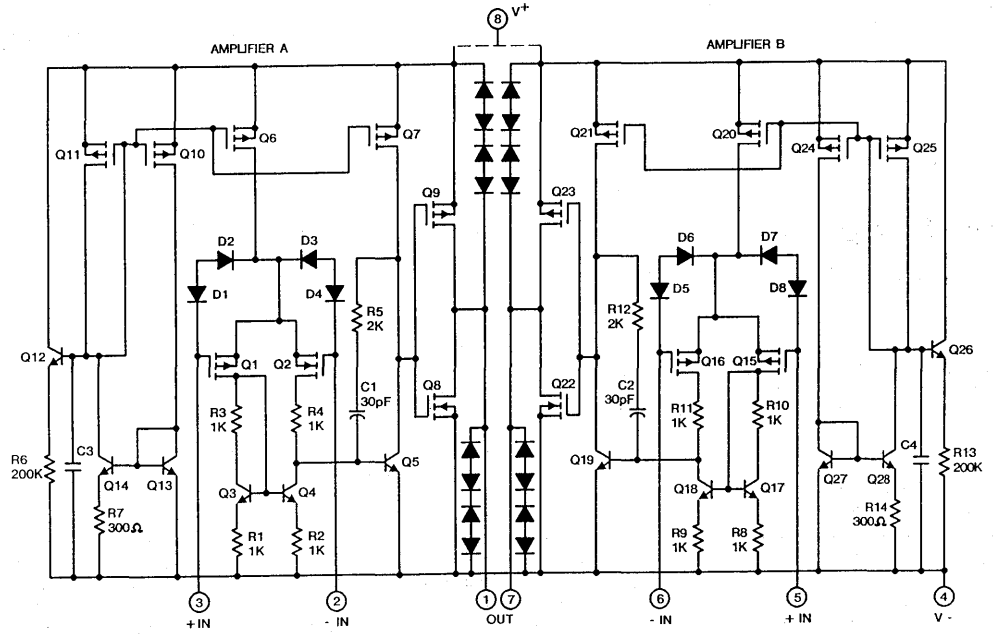
ELECTRICAL CHARACTERISTICS AT T_A = -55°C to +125°C, V^+ = 5 V, V^- = 0 V

CHARACTERISTIC		LIMITS						UNITS
		CA5260A			CA5260			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage V_O = 2.5 V	V_{IO}	—	2	15	—	3	20	mV
Input Offset Current V_O = 2.5 V	I_{IO}	—	1	10	—	1	10	nA
Input Current V_O = 2.5 V	I_I	—	2	15	—	2	15	nA
Common-Mode Rejection Ratio								
V_{CM} = 0 to 1 V	C_{MRR}	65	78	—	60	78	—	dB
V_{CM} = 0 to 2.5 V	C_{MRR}	50	60	—	50	60	—	dB
Input Common-Mode Voltage Range								
	V_{ICR}^+	2.5	3	—	2.5	3	—	V
	V_{ICR}^-	—	-0.5	0	—	-0.5	0	V
Power-Supply Rejection Ratio Δ^+ = 1 V; Δ^- = 1 V	P_{SRR}	62	65	—	60	65	—	dB
Large-Signal Voltage Gain *	A_{OL}							
V_O = 0.5 to 4 V	R_L = ∞	70	78	—	70	78	—	dB
V_O = 0.5 to 3.6 V	R_L = 10 k	60	65	—	60	65	—	dB
Source Current V_O = 0 V	I_{SOURCE}	1.3	1.6	—	1.3	1.6	—	mA
Sink Current V_O = 5 V	I_{SINK}	1.2	1.4	—	1.2	1.4	—	mA
Output Voltage	V_{OUT}							
R_L = ∞	V_{OM}^+	4.99	5	—	4.99	5	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
R_L = 10 k	V_{OM}^+	4.2	4.4	—	4.2	4.4	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
R_L = 2 k	V_{OM}^+	2.5	2.7	—	2.5	2.7	—	V
	V_{OM}^-	—	0	0.01	—	0	0.01	V
Supply Current	I_{SUPPLY}							
V_O = 0 V		—	1.65	2.2	—	1.65	2.2	mA
V_O = 2.5 V	I_{SUPPLY}	—	1.95	2.35	—	1.95	2.35	mA

*For V^+ = 4.5 V and V^- = Gnd; V_{OUT} = 0.5 V to 3.2 V at R_L = 10 k.

ELECTRICAL CHARACTERISTICS for Each Amplifier at T_A = 25°C, V^+ = 15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC		LIMITS						UNITS
		CA5260A (T, S, E)			CA5260 (T, S, E)			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage $V^{\pm}$ = ±7.5 V	V_{IO}	—	2	5	—	6	15	mV
Input Offset Current $V^{\pm}$ = ±7.5 V	I_{IO}	—	0.5	20	—	0.5	30	pA
Input Current $V^{\pm}$ = ±7.5 V	I_I	—	5	30	—	5	50	pA
Large-Signal Voltage Gain	A_{OL}	50 k	320 k	—	50 k	320 k	—	V/V
V_O = 10 V_{p-p}, R_L = 10 kΩ		94	110	—	94	110	—	dB
Common-Mode Rejection Ratio	C_{MRR}	80	95	—	70	90	—	dB
Common-Mode Input Voltage Range	V_{ICR}	10	-0.5 to 12	0	10	-0.5 to 12	0	V
Power-Supply Rejection Ratio, $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$ = ±7.5 V	P_{SRR}	—	32	150	—	32	320	μV/V
Maximum Output Voltage:								V
At R_L = 10 kΩ	V_{OM}^+	11	13.3	—	11	13.3	—	
	V_{OM}^-	—	0.002	0.01	—	0.002	0.01	
At R_L = ∞	V_{OM}^+	14.99	15	—	14.99	15	—	
	V_{OM}^-	—	0	0.01	—	0	0.01	
Maximum Output Current								mA
I_{OM}^+ (Source) @ V_O = 7.5 V		12	22	45	12	22	45	
I_{OM}^- (Sink) @ V_O = 7.5 V		12	20	45	12	20	45	
Total Supply Current R_L = ∞	I^+							mA
V_O (Ampli. A) = V_O (Ampli. B) = 7.5 V		—	9	16.5	—	9	16.5	
V_O (Ampli. A) = V_O (Ampli. B) = 0 V		—	1.2	4	—	1.2	4	
V_O (Ampli. A) = 0 V, V_O (Ampli. B) = 7.5 V		—	5	9.5	—	5	9.5	
Input Offset Voltage Temp. Drift	$\Delta V_{IO}/\Delta T$	—	6	—	—	8	—	μV/°C
Crosstalk f = 1 kHz		—	120	—	—	120	—	dB


8
V+
AMPLIFIER A
AMPLIFIER B
Q11
Q10
Q6
Q7
Q21
Q20
Q24
Q25
Q9
Q23
D2
D3
D6
D7
D1
D4
D5
D8
R5
2K
R12
2K
Q12
Q1
Q2
Q16
Q15
Q26
R3
1K
R4
1K
C1
30pF
Q8
Q22
C2
30pF
R11
1K
R10
1K
R6
200K
C3
Q19
C4
R13
200K
Q14
Q13
Q5
Q27
Q28
Q3
Q4
Q18
Q17
R7
300Ω
R14
300Ω
R1
1K
R2
1K
R9
1K
R8
1K
3
+IN
2
- IN
1
7
OUT
6
- IN
5
+ IN
4
V -

May 1990

Low-Supply Voltage, Low-Input Current BiMOS Operational Amplifiers

Features:

- *CA5420A, CA5420 at 5V supply voltage with full military temperature range guaranteed specifications*
- *CA5420A, CA5420 guaranteed to operate from ±1V to ±10V supplies*
- *2 V supply at 300 μA supply current*
- *1 pA (typ.) input current (essentially constant to 85°C)*
- *Rail-to-rail output swing (Drive ±2 mA into 1 kΩ load)*
- *Pin compatible with 741 op amp*

Applications:

- *pH probe amplifiers*
- *Picoammeters*
- *Electrometer (High Z) instruments*
- *Portable equipment*
- *Inaccessible field equipment*
- *Battery dependent equipment (medical and military)*
- *5V logic systems*
- *Microprocessor interface*

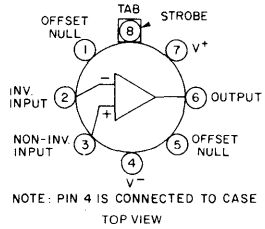
The CA5420A and CA5420* are integrated circuit operational amplifiers that combine PMOS transistors and bipolar transistors on a single monolithic chip. They are designed and guaranteed to operate in microprocessor logic systems that use V+ = 5V, V- = Gnd, since they can operate down to ±1V supplies. They will also be suitable for 3.3V logic systems.

The CA5420A and CA5420 BiMOS operational amplifiers feature gate-protected PMOS transistors in the input circuit to provide very high input impedance, very low input currents (less than 1 pA). The internal bootstrapping network features a unique guardbanding technique for reducing the doubling of leakage current for every 10°C increase in temperature. The CA5420 series operates at total supply voltages from 2 to 20 volts either single or dual supply. These operational amplifiers are internally phase compensated to achieve stable operation in the unity gain follower configuration. Additionally, they have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset voltage nulling. The use of PMOS in the input stage results in common-mode input voltage capability down to 0.45 volt below the negative supply terminal, an important attribute for single supply application. The output stage uses a feedback OTA-type amplifier that can swing essentially from rail-to-rail. The output driving current of 1.0 mA (min) is provided by using non-linear current mirrors.

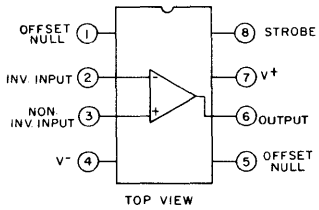
These devices have guaranteed specifications for 5 volt operation over the full military temperature range of -55°C to +125°C.

The CA5420 series has the same 8-lead pin-out used for the industry standard 741. They are supplied in the standard 8-lead TO-5 style package (S suffix, and T suffix); in the standard 8-lead dual-in-line plastic package (Minidip - E suffix), and are also available in chip form (H suffix).

*Formerly Dev. Type No. TA10841



S AND T SUFFIXES



E SUFFIX

Functional diagrams for CA5420A, CA5420.

MAXIMUM RATINGS, *Absolute-Maximum Values* ($T_C = 25°C$):

DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS) ..... 22 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±15 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8 V) to (V^- −0.5 V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
  WITHOUT HEAT SINK
    Up to 55°C ..... 630 mW
    Above 55°C ..... Derate linearly 6.67 mW/°C
  WITH HEAT SINK
    Up to 110°C ..... 630 mW
    Above 110°C ..... Derate linearly 16.7 mW/°C
TEMPERATURE RANGE:
  OPERATING (ALL TYPES) ..... −55 to +125°C
  STORAGE (ALL TYPES) ..... −65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION* ..... Indefinite
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

*Short circuit may be applied to ground or to either supply.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

CHARACTERISTIC		TEST CONDITIONS $V^+ = +5V; V^- = Gnd$ $T_A = 25°C$		CA5420A (T,S,E)	CA5420 (T,S,E)	UNITS
Input Resistance	R_I			150	150	TΩ
Input Capacitance	C_I			4.9	4.9	pF
Output Resistance	R_O			300	300	Ω
Equivalent Input	e_n	f = 1 kHz	$R_S = 100Ω$	62	62	nV/Hz
Noise Voltage		f = 10 kHz		38	38	
Short-Circuit Current Source						mA
Source I_{OM}^+				2.6	2.6	
To Opposite Supply						
Sink I_{OM}^-				2.4	2.4	
Gain-Bandwidth Product	f_T			0.5	0.5	MHz
Slew Rate	SR			0.5	0.5	V/μs
Transient Response						
Rise Time, t_r		$R_L = 2kΩ$		0.7	0.7	μs
Overshoot		$C_L = 100pF$		15	15	%
Current from Terminal 8						
To V^-	I_8^+			20	20	μA
Current from Terminal 8						
To V^+	I_8^-			2	2	mA
Settling Time	.01%	$A_V = 1$	$2V_{p-p}$ Input	8	8	μSec
	.10%	$A_V = 1$	$2V_{p-p}$ Input	4.5	4.5	μSec

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V^+ = 5 V, V^- = 0 V

CHARACTERISTIC		LIMITS						UNITS
		CA5420A			CA5420			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage V_O = 2.5 V	V_{IO}	—	1	5	—	1.5	10	mV
Input Offset Current V_O = 2.5 V	I_{IO}	—	0.02	0.5	—	0.02	1	pA
Input Current V_O = 2.5 V	I_I	—	0.02	1	—	0.02	2	pA
Common-Mode Rejection Ratio V_{CM} = 0 to 3.7 V; V_O = 2.5 V	C_{MRR}	75	83	—	70	80	—	dB
Input Common-Mode Voltage Range V_O = 2.5 V	V_{ICR}^+	3.7	4	—	3.7	4	—	V
	V_{ICR}^-	—	-0.3	0	—	-0.3	0	V
Power-Supply Rejection Ratio Δ^+ = 1 V; Δ^- = 1 V	P_{SRR}	75	83	—	70	80	—	dB
Large-Signal Voltage Gain	A_{OL}							dB
V_O = 0.5 to 4 V	R_L = ∞	85	87	—	85	87	—	dB
V_O = 0.5 to 4 V	R_L = 10k	85	87	—	85	87	—	dB
V_O = 0.7 to 3 V	R_L = 2k	80	85	—	80	85	—	dB
Source Current V_O = 0 V	I_{SOURCE}	1.2	2.7	—	1.2	2.7	—	mA
Sink Current V_O = 5 V	I_{SINK}	1.2	2.1	—	1.2	2.1	—	mA
Output Voltage	V_{OUT}							V
R_L = ∞	V_{OM}^+	4.9	4.94	—	4.9	4.94	—	V
	V_{OM}^-	—	0.13	0.15	—	0.13	0.15	V
R_L = 10k	V_{OM}^+	4.7	4.9	—	4.7	4.9	—	V
	V_{OM}^-	—	0.12	0.15	—	0.12	0.15	V
R_L = 2k	V_{OM}^+	3.5	4.6	—	3.5	4.6	—	V
	V_{OM}^-	—	0.1	0.15	—	0.1	0.15	V
Supply Current V_O = 0 V	I_{SUPPLY}	—	400	500	—	400	500	μA
V_O = 2.5 V	I_{SUPPLY}	—	430	550	—	430	550	μA

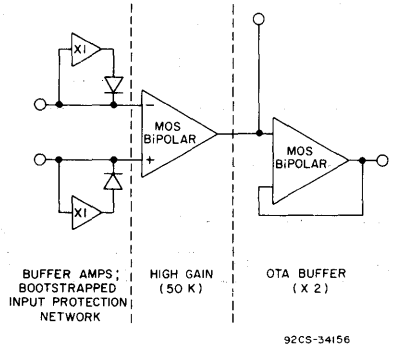


Fig. 1 - Functional diagram for CA5420.

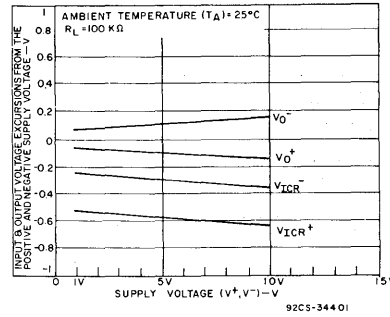


Fig. 2 - Output-voltage-swing and common-mode input-voltage range vs supply voltage.

ELECTRICAL CHARACTERISTICS at T_A = -55°C to +125°C, V^+ = 5 V, V^- = 0 V

CHARACTERISTIC		LIMITS						UNITS
		CA5420A			CA5420			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage V_O = 2.5 V	V_{IO}	—	2	10	—	3	15	mV
Input Offset Current	I_{IO}	—	1.5	3	—	1.5	3	nA
V_O = 2.5 V (Up to T_A = 85°C)	I_{IO}	—	2	10	—	2	10	pA
Input Current	$\|I_I\|$	—	2	5	—	2	5	nA
V_O = 2.5 V (Up to T_A = 85°C)	$\|I_I\|$	—	10	15	—	15	25	pA
Common-Mode Rejection Ratio V_{CM} = 0 to 3.7 V; V_O = 2.5 V	C_{MRR}	70	80	—	65	75	—	dB
Input Common-Mode Voltage Range V_O = 2.5 V	V_{ICR}^+	3.7	4	—	3.7	4	—	V
	V_{ICR}^-	—	-0.3	0	—	-0.3	0	
Power-Supply Rejection Ratio Δ^+ = 1 V; Δ^- = 1 V	P_{SRR}	70	83	—	65	80	—	dB
Large-Signal Voltage Gain	A_{OL}							
V_O = 0.5 to 4 V	R_L = ∞	85	87	—	80	85	—	
V_O = 0.7 to 4 V	R_L = 10k	80	87	—	80	85	—	
V_{OUT} = 0.7 to 2.5 V	R_L = 2k	75	80	—	75	80	—	
Source Current V_O = 0 V	I_{SOURCE}	1	2.7	—	1	2.7	—	mA
Sink Current V_O = 5 V	I_{SINK}	1	2.1	—	1	2.1	—	
Output Voltage	V_{OUT}							
R_L = ∞	V_{OM}^+	4.8	4.9	—	4.8	4.9	—	V
	V_{OM}^-	—	0.16	0.2	—	0.16	0.2	
R_L = 10k	V_{OM}^+	4.7	4.9	—	4.7	4.9	—	
	V_{OM}^-	—	0.15	0.2	—	0.15	0.20	
R_L = 2k	V_{OM}^+	3	4	—	3	4	—	
	V_{OM}^-	—	0.14	0.2	—	0.14	0.2	
Supply Current V_O = 0 V	I_{SUPPLY}	—	430	550	—	430	550	μA
V_O = 2.5 V	I_{SUPPLY}	—	480	600	—	480	600	

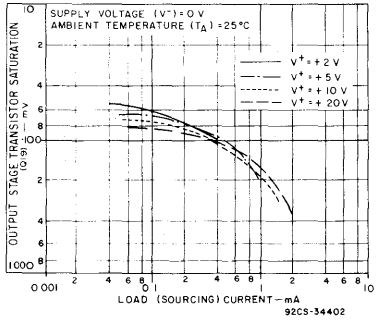


Fig. 3 - Output voltage vs load sourcing current.

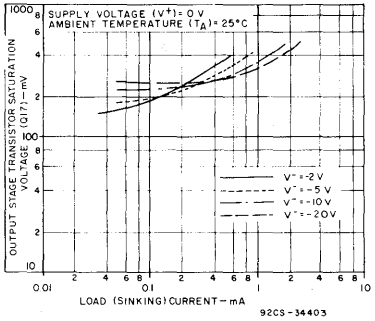


Fig. 4 - Output voltage vs load sinking current.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At V^+ = 1 V, V^- = -1 V, T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC		LIMITS						UNITS
		CA5420A			CA5420			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	—	2	5	—	5	10	mV
Input Offset Current	$\|I_{IO}\|$	—	0.01	4*	—	0.01	4*	pA
Input Current	$\|I_I\|$	—	0.02	5*	—	0.02	5*	pA
Large-Signal Voltage Gain	A_{OL}	20k	100k	—	10k	100k	—	V/V
R_L = 10 kΩ		86	100	—	80	100	—	dB
Common-Mode Rejection Ratio	C_{MRR}	—	560	1000	—	560	1800	μV/V
		60	65	—	55	65	—	dB
Input Common-Mode Voltage Range	V_{ICR}^+	0.2	0.5	—	0.2	0.5	—	V
	V_{ICR}^-	-1	-1.3	—	—	-1.3	—	
Power Supply Rejection Ratio	P_{SRR}	—	32	320	—	100	1000	μV/V
$\Delta V_{IO}/\Delta V$		70	90	—	60	80	—	dB
Maximum Output Voltage	V_{OUT}							
R_L = ∞	V_{OM}^+	0.9	0.95	—	0.9	0.95	—	V
	V_{OM}^-	-0.85	-0.91	—	-0.85	-0.91	—	
Supply Current	I_{SUPPLY}	—	350	650	—	350	650	μA
Device Dissipation	P_D	—	0.7	1.1	—	0.7	1.1	mW
Input Offset Voltage Temp. Drift	$\Delta V_{IO}/\Delta T$	—	4	—	—	4	—	μV/°C

*The maximum limit represents the levels obtainable on high-speed automatic test equipment.
Typical values are obtained under laboratory conditions.

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN
At V^+ = 10 V, V^- = -10 V, T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC		LIMITS						UNITS
		CA5420A			CA5420			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	—	2	5	—	5	10	mV
Input Offset Current	$\|I_{IO}\|$	—	0.03	4*	—	0.03	4*	pA
Input Current	$\|I_I\|$	—	0.05	5*	—	0.05	5*	pA
Large-Signal Voltage Gain	A_{OL}	20k	100k	—	10k	100k	—	V/V
R_L = 10 kΩ		86	100	—	80	100	—	dB
Common-Mode Rejection Ratio	C_{MRR}	—	100	320	—	100	320	μV/V
		70	80	—	70	80	—	dB
Input Common-Mode Voltage Range	V_{ICR}^+	9	9.3	—	8.5	9.3	—	V
	V_{ICR}^-	-10	-10.3	—	-10	-10.3	—	
Power Supply Rejection Ratio	P_{SRR}	—	32	320	—	32	320	μV/V
$\Delta V_{IO}/\Delta V$		70	90	—	70	90	—	dB
Maximum Output Voltage	V_{OUT}							
R_L = ∞	V_{OM}^+	9.7	9.9	—	9.7	9.9	—	V
	V_{OM}^-	-9.7	-9.85	—	-9.7	-9.85	—	
Supply Current	I_{SUPPLY}	—	450	1000	—	450	1000	μA
Device Dissipation	P_D	—	9	14	—	9	14	mW
Input Offset Voltage Temp. Drift	$\Delta V_{IO}/\Delta T$	—	4	—	—	4	—	μV/°C

*The maximum limit represents the levels obtainable on high-speed automatic test equipment.
Typical values are obtained under laboratory conditions.

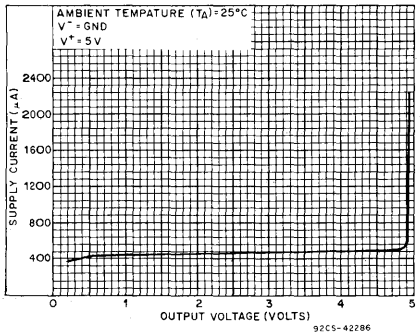


Fig. 5 - Supply current vs output voltage.

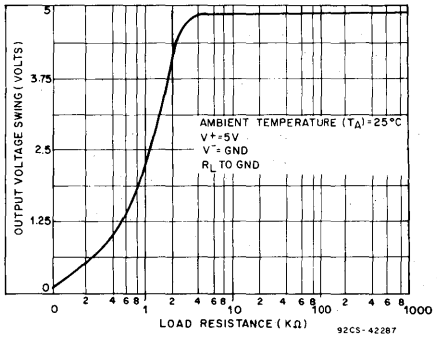


Fig. 6 - Output voltage swing vs load resistance.

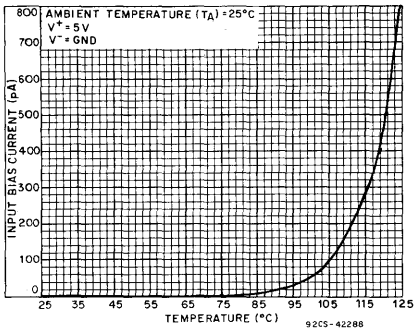


Fig. 7 - Input bias current drift ($\Delta I_B/\Delta T$).

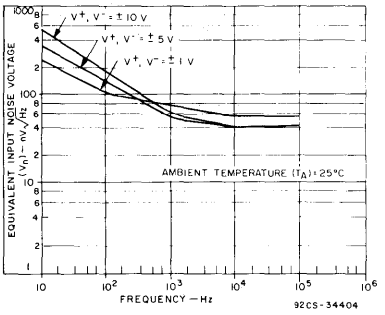


Fig. 8 - Input noise voltage vs frequency.

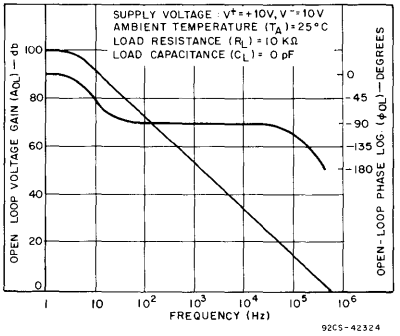


Fig. 9 - Open-loop gain and phase-shift response.

APPLICATION CIRCUITS

Picoammeter Circuit

The exceptionally low input current (typically 0.2 pA) makes the CA5420 highly suited for use in a picoammeter circuit. With only a single 10K-megohm resistor, this circuit covers the range from ±1.5 pA. Higher current ranges are possible with suitable switching techniques and current scaling resistors. Input transient protection is provided by the 1-megohm resistor in series with the input. Higher current ranges require that this resistor be reduced. The 10-megohm resistor connected to pin 2 of the CA5420 decouples the potentially high input capacitance often associated with lower current circuits and reduces the tendency for the circuit to oscillate under these conditions.

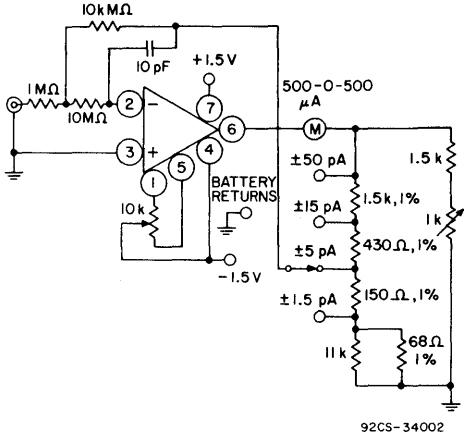


Fig. 10 - CA5420 picoammeter circuit.

High-Input-Resistance Voltmeter

Advantage is taken of the high input impedance of the CA5420 in a high-input-resistance dc voltmeter. Only two 1.5-V "AA"-type penlite batteries power this exceedingly high-input-resistance (>1,000,000 megohms) dc voltmeter. Full-scale deflection is ±500 mV, ±150 mV, and ±15 mV. Higher voltage ranges are easily added with external input voltage attenuator networks.

The meter is placed in series with the gain network, thus eliminating the meter temperature coefficient error term.

Supply current in the standby position with the meter undeflected is 300 μA. At full-scale deflection this current rises to 800 μA. Carbon-zinc battery life should be in excess of 1,000 hours.

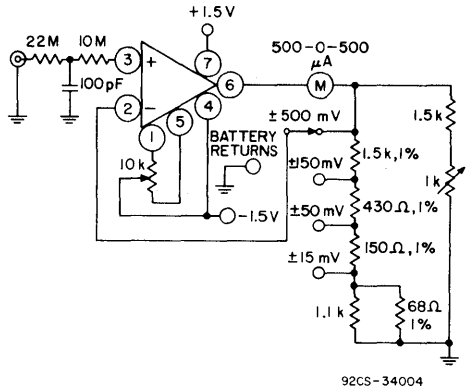


Fig. 11 - CA5420 high-input-resistance voltmeter.

May 1990

Quad Microprocessor BiMOS-E Operational Amplifiers

With MOSFET Input/Bipolar Output

Features:

- *High-speed CMOS input stage provides:*
  very high Zi = 3 T (3x10+12Ω) typ.
  very low I_I = 0.5 pA typ. at 5 V operation
  very low I_{IO} = 0.5 pA typ. at 5 V operation
- *ESD protection to 2000 V*
- *3 V to 16 V power supply operation*
- *Fully guaranteed specifications over full military range*
- *Wide BW; high SR 14MHz and 5 V/μsec at 5 V supply*
- *Wide V_{ICR} range form -0.5 V to 3.7 V typ. at 5 V supply*
- *Ideally suited for CMOS and HCMOS applications*
- *+5V characteristics for microprocessor applications*

Applications:

- *Bar Code readers*
- *Photodiode amplifiers (IR)*
- *Microprocessor buffering*
- *Ground reference single supply amplifiers*
- *Fast sample and hold*
- *Timers*
- *Voltage controlled oscillators*
- *Voltage followers*
- *V to I converters*
- *Peak detectors*
- *Precision rectifiers*
- *5 V logic systems*
- *3 V logic systems*

The CA5470 series are integrated circuit operational amplifiers that combine the advantages of both high-speed CMOS and bipolar transistors on a single monolithic chip. They are constructed in the BiMOS-E process which adds drain-extension implants to 3 μm polygate CMOS, enhancing both the voltage capability and providing vertical bipolar transistors for broadband analog/digital functions. This process lends itself easily to high-speed operational amplifiers, comparators, analog switches and interface peripherals, resulting in twice the speed of the conventional CMOS transistors having similar feature size.

BiMOS-E are broadbased bipolar transistors that have high transconductance, gains more constant with current level, stable "precision" base-emitter offset voltages and superior drive capability. Excellent interface with environmental potentials enable use in 5 V logic systems and future 3.3 V logic systems.

ESD capability exceeds the standard 2000 volt level. The CA5470 series can operate with single supply voltages from 3 V to 16 V or ±1.5 V to ±8 V. They have guaranteed specifications at both 5 V and ±7.5 V at room temperature as well as over the full -55°C to +125°C military range.

The CA5470 series is supplied in the standard 14-lead dual-in-line plastic package (E suffix) and the 14-lead dual-in-line surface-mount package (M suffix). The CA5470 is also available in chip form (H suffix).

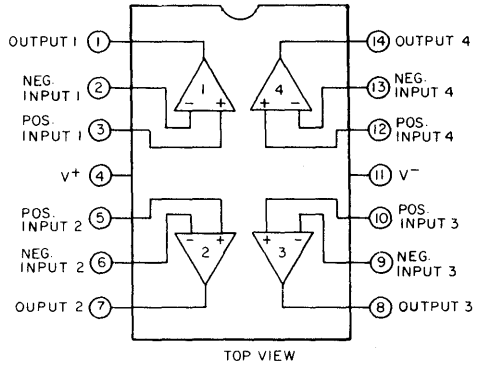
MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY-VOLTAGE
(Between V+ and V- Terminals) ..... 16 V
DIFFERENTIAL MODE INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC INPUT VOLTAGE ..... (V+ +8 V) to (V- -0.5V)
INPUT TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK -
up to 55°C ..... 630 mW
above 55°C ..... Derate Linearly 6.67 mW/°C
WITH HEAT SINK -
up to 90°C ..... 1 W
above 90°C ..... Derate Linearly 16.7 mW/°C
SMALL OUTLINE PACKAGE -
up to 65°C ..... 500 mW
above 65°C ..... Derate Linearly at 5.9 mW/°C
TEMPERATURE RANGE:
OPERATING (all types) ..... -55 to +125°C
STORAGE (all types) ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION* ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 (1.59 ± 0.79 mm) from case for 10 seconds max ..... +265°C

*Short circuit may be applied to ground or to either supply.

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE *V+ = 5 V, V- = 0, T_A = 25°C (Unless Otherwise Specified)*

CHARACTERISTIC		TEST CONDITIONS	TYPICAL VALUES	UNITS
Input Resistance	R_I		5	TΩ
Input Capacitance	C_I	f = 1 MHz	3.1	pF
Unity Gain Crossover Frequency	f_T		14	MHz
Slew Rate	SR	V_{OUT} = 3.65 V_{p-p}	4	v/μs
Transient Response:	t_r	C_L = 25 pF		
Rise Time/Fall Time		R_L = 2 kΩ	27/25	ns
Overshoot		(Voltage Follower)	20	%
Settling Time (4 V_{p-p} Input to < 0.1%)			1	μs
Full Power BW (V_{OUT} = 3.65 V) SR = 4 V/μs		A_V = 1	350	kHz



E and M Suffixes

Figure 1 - Functional diagrams for the CA5470 series.

ELECTRICAL CHARACTERISTICS *At T_A = 25°C, V+ = 5 V, V- = Gnd*

CHARACTERISTICS		LIMITS MIN.	LIMITS TYP	LIMITS MAX.	UNITS
Input Offset Voltage	$\|V_{IO}\|$	—	6	22	mV
Input Offset Current	$\|I_{IO}\|$	—	0.5	5	pA
Input Current	I_I	—	0.5	10	pA
Common-Mode Input Range	V_{ICR}	3.5	-0.5 to 3.7	0	V
Common-Mode Rejection Ratio V_{ICR} = 0 to 3.5 V	C_{MRR}	55	70	—	dB
Power-Supply Rejection Ratio ΔV = 2 V	P_{SRR}	60	75	—	dB
Positive Output Voltage Swing R_L = 2 k to GND	$V_{OM}+$	4	4.4	—	V
Negative Output Voltage Swing R_L = 2 k to GND	$V_{OM}-$	—	0.06	0.10	V
Total Supply Current V_{OUT} = 2.5 V	I_{SUPPLY}	—	8	10	mA
Unity Gain Bandwidth Product	f_T	10	14	—	MHz
Slew Rate	SR	4	5	—	V/μSec
Output Current					
Source to opposite supply	I_{SOURCE}	4	5.5	—	mA
Sink to opposite supply	I_{SINK}	0.8	1.2	—	mA
Open Loop Gain 0.5 V to 3.5 V	R_L = 10k	80	90	—	dB

ELECTRICAL CHARACTERISTICS *At T_A = -55°C to +125°C, V+ = 5 V, V- = Gnd*

CHARACTERISTICS		LIMITS MIN.	LIMITS TYP	LIMITS MAX.	UNITS
Input Offset Voltage	$\|V_{IO}\|$	—	6	25	mV
Input Offset Current	$\|I_{IO}\|$	—	550	5500	pA
Input Current	I_I	—	550	11000	pA
Common-Mode Input Range	V_{ICR}	3.5	-0.5 to 3.7	0	V
Common-Mode Rejection Ratio V_{ICR} = 0 to 3.5 V	C_{MRR}	50	65	—	dB
Power-Supply Rejection Ratio ΔV = 2 V	P_{SRR}	58	75	—	dB
Positive Output Voltage Swing R_L = 2 k to V-	$V_{OM}+$	3.8	4.2	—	V
Negative Output Voltage Swing R_L = 2 k to V-	$V_{OM}-$	—	0.08	0.11	V
Total Supply Current VOUT = 2.5 V	I_{SUPPLY}	—	9	11	mA
Unity Gain Bandwidth Product	f_T	8	12	—	MHz
Slew Rate	SR	3	5	—	V/μSec
Output Current					
Source to opposite supply	I_{SOURCE}	4	5.5	—	mA
Sink to opposite supply	I_{SINK}	0.8	1.2	—	mA
Open Loop Gain 0.5 V to 3.5 V	R_L = 10k	80	90	—	dB

ELECTRICAL CHARACTERISTICS *At T_A = 25°C, V+ = 7.5 V, V- = -7.5 V*

CHARACTERISTICS		LIMITS MIN.	LIMITS TYP	LIMITS MAX.	UNITS
Input Offset Voltage	$\|V_{IO}\|$	—	5	25	mV
Input Offset Current	$\|I_{IO}\|$	—	0.5	5	pA
Input Current	I_I	—	1	10	pA
Common-Mode Input Range	V_{ICR}	5.8	-7.8 to 6.0	-7.5	V
Common-Mode Rejection Ratio V_{ICR} = 0 to 3.5 V	C_{MRR}	60	70	—	dB
Power-Supply Rejection Ratio ΔV = 2 V	P_{SRR}	65	76	—	dB
Positive Output Voltage Swing R_L = 2 k to GND	$V_{OM}+$	6.3	6.5	—	V
R_L = 10k to GND		6.4	6.6	—	
Negative Output Voltage Swing R_L = 2 k to GND	$V_{OM}-$	—	-7.47	-7.45	V
R_L = 10k to GND		—	-7.3	-7.1	
Total Supply Current V_{OUT} = GND	I_{SUPPLY}	—	10	11	mA
Unity Gain Bandwidth Product	f_T	12	16	—	MHz
Slew Rate	SR	4	7	—	V/μSec
Output Current Source to opposite supply	I_{SOURCE}	6.2	6.8	—	mA
Sink to opposite supply	I_{SINK}	1	1.4	—	mA
Open Loop Gain -5 V to +5 V	R_L = 10k	80	90	—	dB

ELECTRICAL CHARACTERISTICS *At T_A = 55°C to +125°C, V+ = 7.5 V, V- = -7.5 V*

CHARACTERISTICS		LIMITS MIN.	LIMITS TYP	LIMITS MAX.	UNITS
Input Offset Voltage	$\|V_{IO}\|$	—	5	30	mV
Input Offset Current	$\|I_{IO}\|$	—	550	5500	pA
Input Current	I_I	—	1100	11000	pA
Common-Mode Input Range	V_{ICR}	5.8	-7.8 to 6.0	-7.5	V
Common-Mode Rejection Ratio V_{ICR} = 0 to 3.5 V	C_{MRR}	58	70	—	dB
Power-Supply Rejection Ratio ΔV = 2 V	P_{SRR}	60	76	—	dB
Positive Output Voltage Swing R_L = 2 k to V-	$V_{OM}+$	6	6.2	—	V
R_L = 10k to GND		6.1	6.4	—	
Negative Output Voltage Swing R_L = 2 k to V-	$V_{OM}-$	—	-7.47	-7.45	V
R_L = 10k to GND		—	-7.3	-7.1	
Total Supply Current V_{OUT} = GND	I_{SUPPLY}	—	11	12	mA
Unity Gain Bandwidth Product	f_T	10	15	—	MHz
Slew Rate	SR	3	7	—	V/μSec
Output Current Source to opposite supply	I_{SOURCE}	6.2	6.8	—	mA
Sink to opposite supply	I_{SINK}	1	1.4	—	mA
Open Loop Gain -5 V to +5 V	R_L = 10k	80	90	—	dB

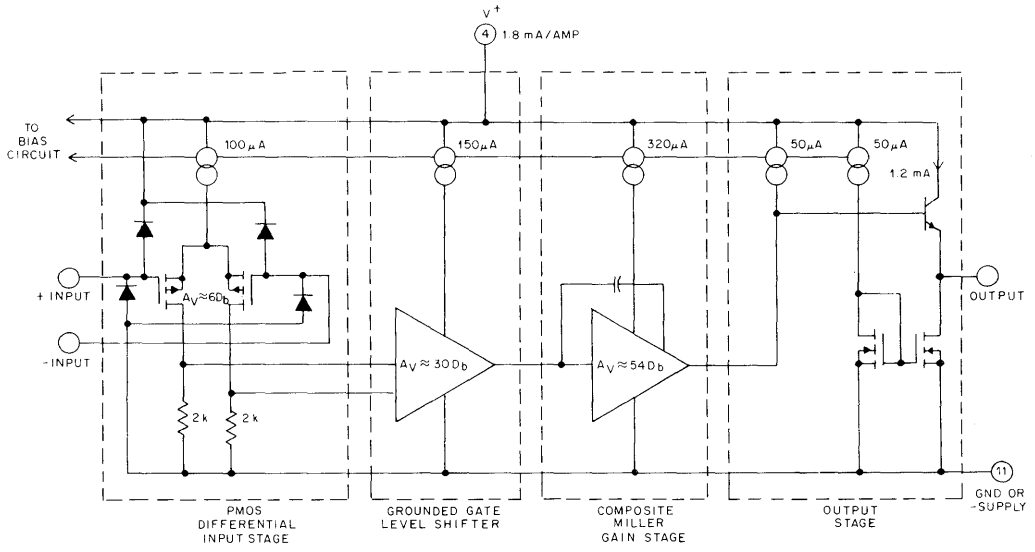
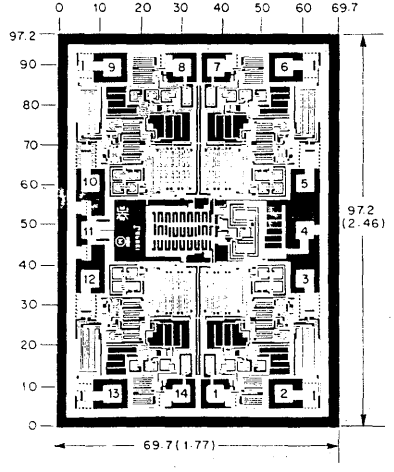


Figure 2 - Block diagram of the CA5470.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch). The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Figure 3 - Dimensions and pad layout for CA5470H.

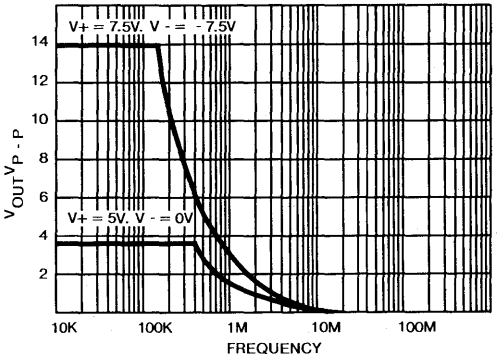


Figure 4 - Maximum output voltage swing vs frequency.

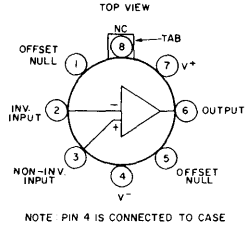
May 1990

Operational Amplifiers

CA6078AT - Micropower Type
CA6741T - General-Purpose Type

For Applications where Low Noise (Burst + 1/f) is a Prime Requirement

Virtually free from "popcorn" (burst) noise: device rejected if any noise burst exceeds 20 mV (peak), referred to input over a 30-second time period.



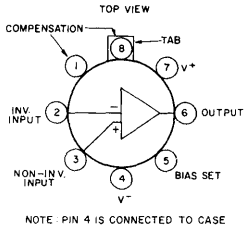
CA6741T

Features:

- *Internal phase compensation*
- *input bias current: 500 nA max.*
- *Input offset current: 200 nA max.*
- *Open loop voltage gain: 50,000 (94 dB) min.*
- *Input offset voltage: 5 mV max.*

Applications:

- *Low noise AC amplifier*
- *Narrow band or bandpass filter*
- *Integrator or differentiator*
- *DC amplifier*
- *Summing amplifier*



CA6078AT

Features:

- *Open loop voltage gain: 40,000 (92 dB) min.*
- *Input offset voltage: 3.5 mV max.*
- *Operates with low total supply voltage: 1.5 V min. (±0.75 V)*
- *Low quiescent operating current: adjustable for application optimization*
- *Input bias current: adjustable to below 1 nA*

Applications:

- *Portable electronics*
- *Medical electronics*
- *DC amplifier*
- *Narrow band or bandpass filter*
- *Integrator or differentiator*
- *Instrumentation*
- *Telemetry*
- *Summing amplifier*

CA6078AT and CA6741T* are low-noise linear IC operational amplifiers that are virtually free of "popcorn" (burst) noise.

These low noise versions of the CA3078AT and CA3471T are a result of improved processing developments and rigid burst noise inspection criteria. A highly selective test circuit (See Figure 2) assures that each type meets the rigid low noise standards in the data section. This low burst noise property also assures excellent performance throughout the 1/f noise spectrum.

In addition the CA6078AT and CA6741T offer the same features incorporated in the CA3078AT and CA3741T respectively, including output short circuit protection, latch free operation, wide common-mode and differential-mode signal ranges, and low offset nulling capability.

For detailed data, characteristics curves, schematic diagram, dimensional outline, and test circuits, refer to the Operational Amplifier Data Bulletins File No. 531 and 535. In addition, for details of considerations in burst-noise measurements, refer to Application Note, ICAN-6732, "Measurement of Burst ("Popcorn") Noise in Linear IC's".

The CA6078AT and CA6741T utilize the hermetically sealed 8-lead TO-5 type package. The CA6078AT and the CA6741T can also be supplied on request with dual-in-line formed leads. These types are identified as the CA6078AS and CA6741S. This formed-lead configuration conforms to that of the 8-lead dual-in-line (Mini-Dip) package. For terminal arrangements, see page 4.

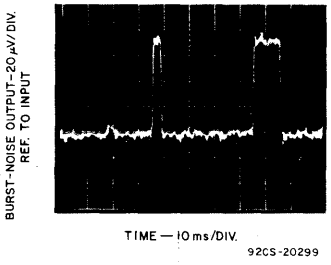
*Formerly Dev. No. TA5807X and TA6029 respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

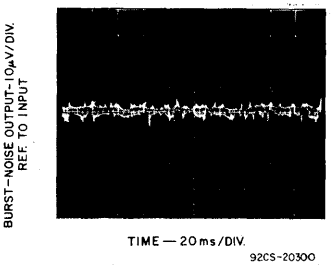
	CA6741T	CA6078AT
DC Supply Voltage (between V^+ and V^- terminals)	44 V	36 V
Differential-Mode Input Voltage	±30 V	±6 V
Common-Mode DC Input Voltage▲	±15 V	V^+ to V^-
Device Dissipation:		
Up to 75°C (CA6741T), Up to 125° (CA6078AT)	500 mW	250 mW
Above 75°C	Derate linearly 5 mW/°C	–
Temperature Range:		
Operating	−55 to +125 °C	−55 to +125 °C
Storage	−65 to +150 °C	−65 to +150 °C
Output Short-Circuit Duration●	No limitation	No limitation
Lead Temperature (During soldering):		
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max.	300 °C	300 °C

▲If Supply Voltage is less than ±15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

●Short circuit may be applied to ground or to either supply.



a. Typ. device with high-burst-noise characteristic.



b. Typ. device controlled for burst noise.

Fig.1—Typ. waveforms of type with high burst noise and type controlled for burst noise.

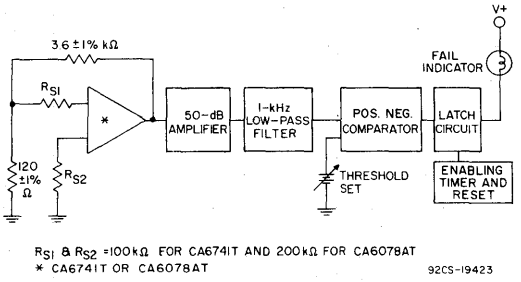


Fig.2—Block diagram of burst-noise "popcorn" test equipment.

ELECTRICAL CHARACTERISTICS – CA6078AT, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Supply Volts: $V^+ = 6$, $V^- = -6$ $T_A = 25^oC$, $I_Q = 20\ \mu A$	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz $R_{SI} = R_{S2} = 200\ k\Omega$	Device is rejected if the total noise voltage (burst + $1/f$), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3078AT Data Bulletin, File No. 535.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	0.7	3.5	mV
Input Offset Current	I_{IO}		–	0.5	2.5	nA
Input Bias Current	I_{IB}		–	7	12	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 10\ k\Omega$	40,000	100,000	–	
		$V_O = \pm 4V$	92	100	–	dB
Common-Mode Input Voltage Range	V_{ICR}	$V^+ = V^- = 15$ V	±14	–	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\Omega$	80	115	–	dB
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10\ \Omega$	±13.7	±14.1	–	V
		$R_L \geq 2\ k\Omega$	–	±14	–	
Supply Current	I_Q		–	20	25	μA

ELECTRICAL CHARACTERISTICS – CA6741T, *For Equipment Design.*

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS Supply Volts; $V^+ = 15$, $V^- = -15$ $T_A = 25^oC$	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Noise Characteristic						
"Popcorn" (Burst) Noise		Bandwidth = 1 kHz $R_{S1} = R_{S2} = 100\ k\Omega$	Device is rejected if the total noise voltage (burst + $1/f$), referred to input, exceeds 20 μV peak, during a 30-sec. test period.			
Principal Characteristics (For detailed Electrical Characteristics refer to CA3741T Data Bulletin, File No. 531.)						
Input Offset Voltage	V_{IO}	$R_S \leq 10\ k\Omega$	–	1	5	mV
Input Offset Current	I_{IO}		–	20	200	nA
Input Bias Current	I_{IB}		–	80	500	nA
Open-Loop Differential Voltage Gain	A_{OL}	$R_L \geq 2\ k\Omega$	50,000	200,000	–	
		$V_O = \pm 10$ V	94	106	–	dB
Common-Mode Input Voltage Range	V_{ICR}		±12	±13	–	V
Common-Mode Rejection Ratio	CMRR	$R_S \leq 10\ k\ \Omega$	70	90	–	dB
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10\ k\ \Omega$	±12	±14	–	V
		$R_L \geq 2\ k\ \Omega$	±10	±13		
Supply Current	I_Q		–	1.7	2.8	mA

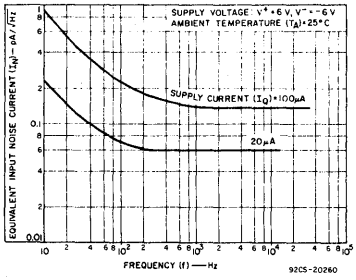


Fig.3—I_N vs. Frequency for CA6078AT.

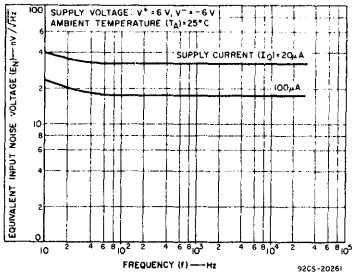


Fig.4—E_N vs. Frequency for CA6078AT.

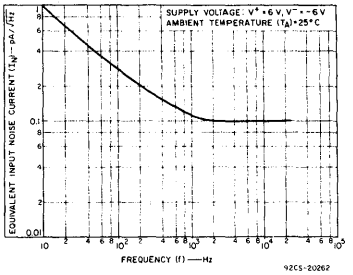


Fig.5—I_N vs. Frequency for CA6741T.

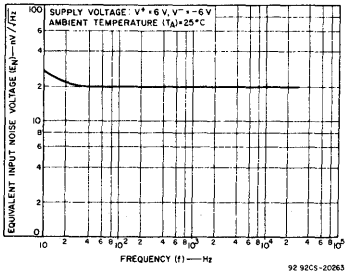


Fig.6—E_N vs. Frequency for CA6741T.

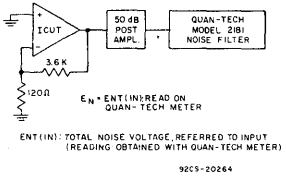


Fig.7—Test block diagram for E_N.

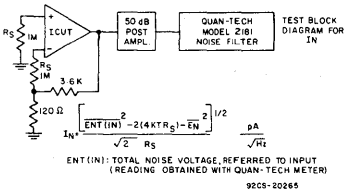


Fig.8—Test block diagram for I_N.

HARRIS

HA-2400/04/05

PRAM Four Channel Programmable Amplifier

May 1990

Features

- Programmability
- High Rate Slew 30V/μs
- Wide Gain Bandwidth 40MHz
- High Gain 150kV/V
- Low Offset Current 5nA
- High Input Impedance 30MΩ
- Single Capacitor Compensation
- DTL/TTL Compatible Inputs

Applications

- Thousands of Applications; Program:
  - Signal Selection/Multiplexing
  - Operational Amplifier Gain
  - Oscillator Frequency
  - Filter Characteristics
  - Add-Subtract Functions
  - Integrator Characteristics
  - Comparator Levels
- For Further Design Ideas, See App. Note 514.

Description

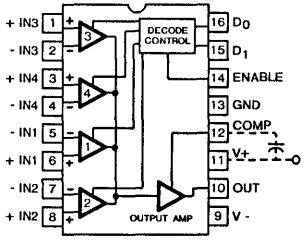
HA-2400/04/05 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

Each channel of the HA-2400/04/05 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing signal selection and mathematical function designs. With 30V/μs slew rate, 40MHz gain bandwidth and 30M ohms input impedance these devices are ideal building blocks for signal generators, active filters and data acquisition designs. Programmability, coupled with 2mV typical offset voltage and 5nA offset current, makes these amplifiers outstanding components for signal conditioning circuits.

HA-2400/04/05 are available in a 16 pin Dual-In-Line package. HA-2400 is specified from -55°C to +125°C. HA-2404 is specified over the -25°C to +85°C range, while HA-2405 operates from 0°C to +75°C.

Pinout

HA1-2400/04/05 (CERAMIC DIP)
TOP VIEW



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

Schematic

HA-2400

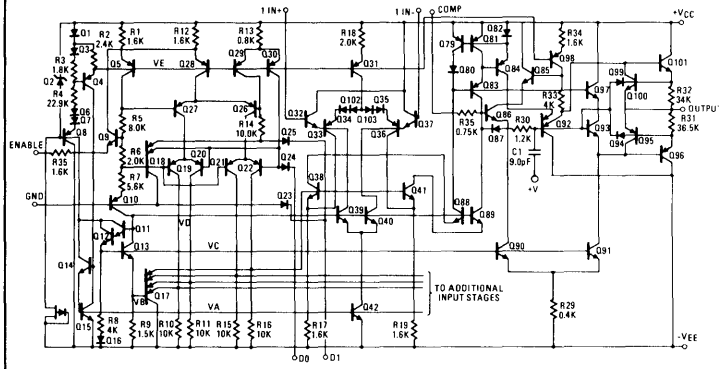


Diagram Includes: One Input Stage, Decode Control, Bias Network, and Output Stage.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Voltage between V+ and V- Terminals 45.0V
Differential Input Voltage ..... $\pm V_{SUPPLY}$
Digital Input Voltage ..... -0.76V to +10.0V
Output Current ..... Short Circuit Protected ($I_{SC} < \pm 33mA$)
Internal Power Dissipation (Note 13) 300mW

Operating Temperature Ranges

HA-2400 ..... $-55^oC \leq T_A \leq +125^oC$
HA-2404 ..... $-25^oC \leq T_A \leq +85^oC$
HA-2405 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$

Electrical Specifications

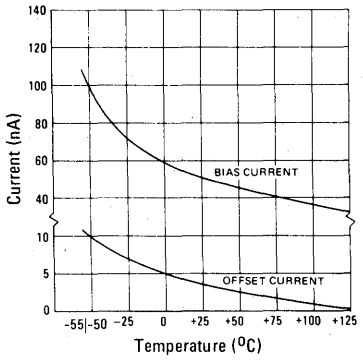
Test Conditions: $V_{SUPPLY} = \pm 15.0V$, Unless Otherwise Specified.
Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4$. Limits apply to each of the four channels, when addressed.

PARAMETER	TEMP	HA-2400/04 LIMITS MIN	HA-2400/04 LIMITS TYP	HA-2400/04 LIMITS MAX	HA-2405 LIMITS MIN	HA-2405 LIMITS TYP	HA-2405 LIMITS MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	4	9	-	4	9	mV
	Full	-	-	11	-	-	11	mV
Bias Current (Note 12)	+25°C	-	50	200	-	50	250	nA
	Full	-	-	400	-	-	500	nA
Offset Current (Note 12)	+25°C	-	5	50	-	5	50	nA
	Full	-	-	100	-	-	100	nA
Input Resistance (Note 12)	+25°C	-	30	-	-	30	-	MΩ
Common Mode Range	Full	±9.0	-	-	±9.0	-	-	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 1, 5)	+25°C	50k	150k	-	50k	150k	-	V/V
	Full	25K	-	-	25K	-	-	V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100	-	74	100	-	dB
Gain Bandwidth (Notes 3, 14)	+25°C	20	40	-	20	40	-	MHz
(Notes 4, 14)	+25°C	4	8	-	4	8	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0	-	±10.0	±12.0	-	V
Output Current	+25°C	10	20	-	10	20	-	mA
Full Power Bandwidth (Notes 3, 5, 15)	+25°C	200	500	-	200	500	-	kHz
(Notes 4, 5, 15)	+25°C	100	200	-	100	200	-	kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4, 6)	+25°C	-	20	45	-	20	50	ns
Overshoot (Notes 4, 6)	+25°C	-	25	40	-	25	40	%
Slew Rate (Notes 3, 7)	+25°C	20	30	-	20	30	-	V/µs
(Notes 4, 7, 14)	+25°C	6	8	-	6	8	-	V/µs
Settling Time (Notes 4, 7, 8, 14)	+25°C	-	1.5	2.5	-	1.5	2.5	µs
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full	-	1	1.5	-	1	1.5	mA
Digital Input Current ($V_{IN} = +5.0V$)	Full	-	5	-	-	5	-	nA
Output Delay (Notes 9, 14)	+25°C	-	100	250	-	100	250	ns
Crosstalk (Note 10)	+25°C	-80	-110	-	-74	-110	-	dB
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	4.8	6.0	-	4.8	6.0	mA
Power Supply Rejection Ratio (Note 11)	Full	74	90	-	74	90	-	dB

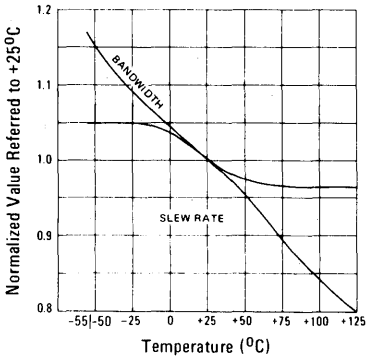
NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 5VDC$
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2k\Omega$, $C_L = 50pF$.
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2k\Omega$, $C_L = 50pF$.
5. $V_{OUT} = 20V$ peak to peak.
6. $V_{OUT} = 200mV$ peak.
7. $V_{OUT} = 10.0V$ peak to peak.
8. To 0.1% of final value.
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10VDC$
11. $V_{SUPPLY} = \pm 10VDC$ to $\pm 20VDC$
12. Unselected channels have approximately the same input parameters.
13. Derate by 4.3mW/°C above 105°C.
14. Guaranteed by design.
15. Full Power Bandwidth based on slew rate measurement using:
$$FPBW = \frac{S.R.}{2\pi\, Vpeak}$$

Typical Performance Curves V+ = +15VDC, V- = -15VDC, T_A = +25°C, Unless Otherwise Specified.

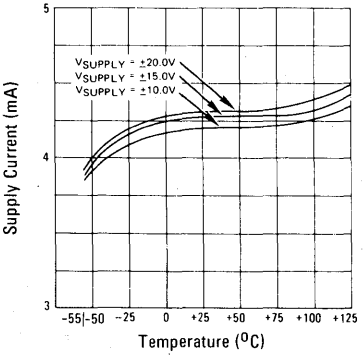
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



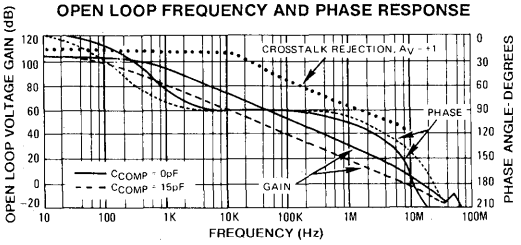
NORMALIZED A.C. PARAMETERS vs. TEMPERATURE



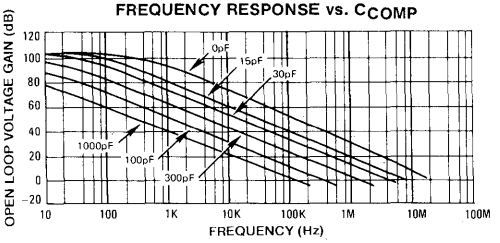
POWER SUPPIY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



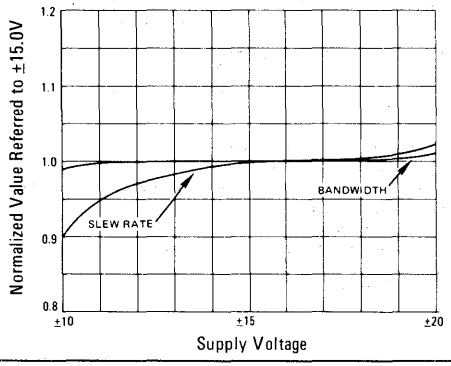
OPEN LOOP FREQUENCY AND PHASE RESPONSE



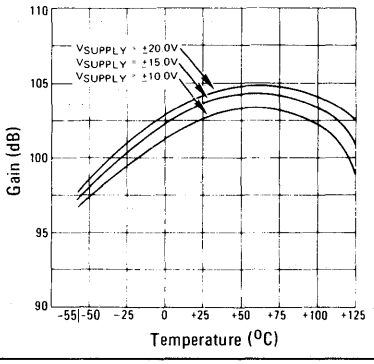
FREQUENCY RESPONSE vs. C_{COMP}



NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE

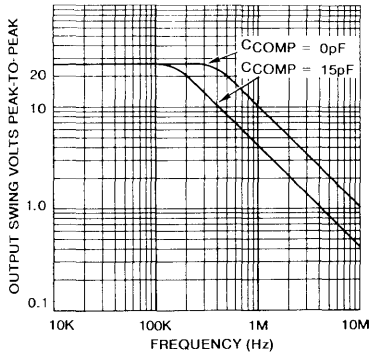


OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE

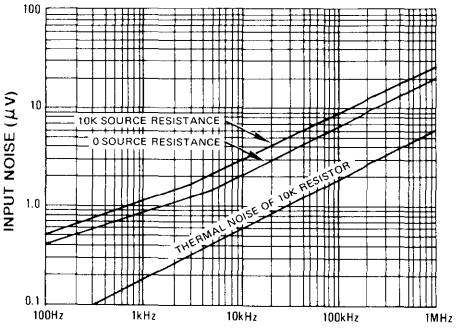


Typical Performance Curves (Continued)

OUTPUT VOLTAGE SWING vs. FREQUENCY

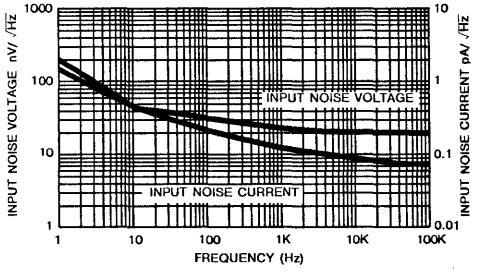


EQUIVALENT INPUT NOISE vs. BANDWIDTH

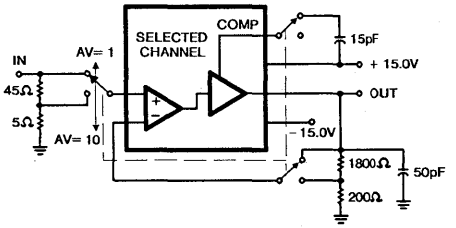


UPPER 3dB FREQUENCY
LOWER 3dB FREQUENCY-10Hz
BROADBAND NOISE CHARACTERISTICS

INPUT NOISE vs. FREQUENCY

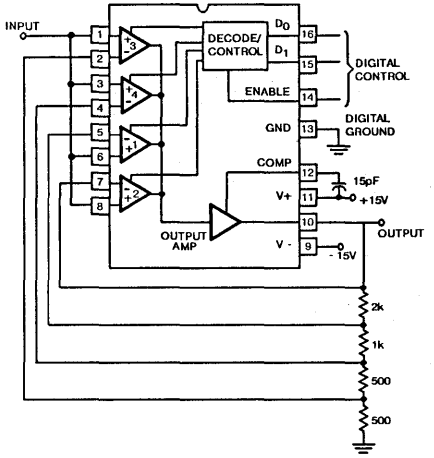


SLEW RATE AND TRANSIENT RESPONSE

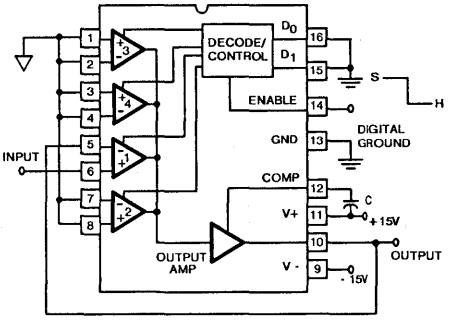


Typical Applications

HA-2400
AMPLIFIER, NONINVERTING PROGRAMMABLE GAIN



HA-2400
SAMPLE AND HOLD



Sample Charging Rate = $\frac{I_1}{C}$ V/Sec.

Hold Drift Rate = $\frac{I_2}{C}$ V/Sec.

Switch Pedestal Error = $\frac{Q}{C}$ Volts

$I_1 \approx 150 \times 10^{-6}$A
$I_2 \approx 200 \times 10^{-9}$A @ +25°C
$\approx 600 \times 10^{-9}$A @ -55°C
100×10^{-9}A @ +125°C
$Q \approx 2 \times 10^{-12}$ Coulomb

For More Examples, See Harris Application Note 514

3 OPERATIONAL AMPLIFIERS

HARRIS

HA-2406

Digitally Selectable Four Channel Operational Amplifier

January 1990

Features

- TTL Compatible Inputs
- Single Capacitor Compensation
- Low Crosstalk ..... -110dB
- High Slew Rate 20V/μs
- Low Offset Current 5nA
- Offset Voltage 7mV
- High Gain-Bandwidth 30MHz
- High Input Impedance 30MΩ

Applications

- Digital Control Of:
  - Analog Signal Multiplexing
  - Op Amp Gains
  - Oscillator Frequencies
  - Filter Characteristics
  - Comparator Levels
- For Further Design Ideas See Application Note 514

Description

The HA-2406 is a monolithic device consisting of four op amp input stages that can be individually connected to one output stage by decoding two TTL lines into four channel select signals. In addition to allowing each channel to be addressed, an enable control disconnects all input stages from the output stage when asserted low.

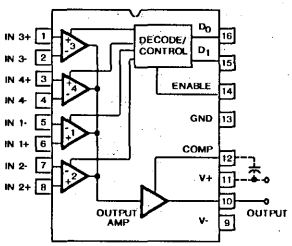
Each input-output combination of the HA-2406 is designed to be a 20V/μs, 30MHz gain-bandwidth amplifier that is stable at a gain of ten but by connecting one external 15pF capacitor all amplifiers are compensated for unity gain operation. The compensation pin may also be used to limit the output swing to TTL levels through suitable clamping diodes and divider networks (see Application Note 514).

Dielectric isolation and short-circuit protected output stages contribute to the quality and durability of the HA-2406. When used as a simple amplifier, its dynamic performance is very good and when its added versatility is considered, the HA-2406 is unmatched in the analog world. It can replace a number of individual components in analog signal conditioning circuits for digital signal processing systems. Its advantages include saving board space and reducing power supply requirements.

The HA-2406 is available in a 16 pin dual-in-line package and is guaranteed for operation over the full commercial temperature range (0°C to +75°C). An SOIC package option is also available with -5 and -9 temperature grades.

Pinout

HA9P2406-5, -9
HA3-2406-5
HA1-2406-5
TOP VIEW



TRUTH TABLE

D1	D0	EN	SEL.ECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

Schematic

HA-2406

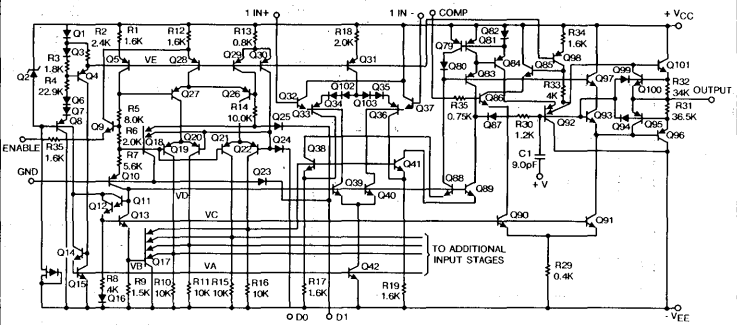


Diagram includes: One Input Stage, Decode Control, Bias Network and Output Stage.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 45.0V
Differential Input Voltage ..... $\pm V_{SUPPLY}$
Digital Input Voltage ..... -0.76V to +10.0V
Output Current ..... Short Circuit Protected ($I_{SC} < \pm 33mA$)
Internal Power Dissipation 300mW
Operating Temperature Range:
HA-2406-5 ..... $0^oC \leq T_A \leq +75^oC$
HA-2406-9 ..... $-40^oC \leq T_A \leq +85^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$

Electrical Specifications

Test Conditions: $V_{SUPPLY} = \pm 15.0V$ Unless Otherwise Specified.
Digital Inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$. Limits apply to each of the four channels, when addressed.

PARAMETER	TEMP	HA-2406-5, -9 LIMITS MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Offset Voltage	+25°C	-	7	10	mV
	Full	-	-	12	mV
Bias Current (Note 12)	+25°C	-	50	250	nA
	Full	-	-	500	nA
Offset Current (Note 12)	+25°C	-	5	50	nA
	Full	-	-	100	nA
Input Resistance (Note 12)	+25°C	-	30	-	MΩ
Common Mode Range	Full	±9.0	-	-	V
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (Notes 1, 5)	+25°C	40K	150K	-	V/V
	Full	20K	-	-	V/V
Common Mode Rejection Ratio (Note 2)	Full	74	80	-	dB
Gain Bandwidth (Note 3, 15)	+25°C	15	30	-	MHz
Gain Bandwidth (Note 4, 15)	+25°C	3	6	-	MHz
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 1)	Full	±10.0	±12.0	-	V
Output Current (Note 13)	+25°C	10	15	-	mA
Full Power Bandwidth (Notes 3, 5, 14, 15)	+25°C	240	320	-	kHz
Full Power Bandwidth (Notes 4, 5, 14)	+25°C	64	95	-	kHz
TRANSIENT RESPONSE					
Rise Time (Notes 4, 6)	+25°C	-	30	100	ns
Overshoot (Notes 4, 6)	+25°C	-	25	40	%
Slew Rate (Notes 3, 7, 15)	+25°C	15	20	-	V/µs
Slew Rate (Notes 4, 7)	+25°C	4	6	-	V/µs
Settling Time (Notes 4, 7, 8, 15)	+25°C	-	2.0	3.5	µs
CHANNEL SELECT CHARACTERISTICS					
Digital Input Current ($V_{IN} = 0V$)	Full	-	1	1.5	mA
Digital Input Current ($V_{IN} = +5.0V$)	Full	-	15	-	nA
Output Delay (Note 9, 15)	+25°C	-	150	300	ns
Crosstalk (Note 10)	+25°C	-74	-110	-	dB
POWER SUPPLY CHARACTERISTICS					
Supply Current	+25°C	-	4.8	7.0	mA
Power Supply Rejection Ratio (Note 11)	Full	74	90	-	dB

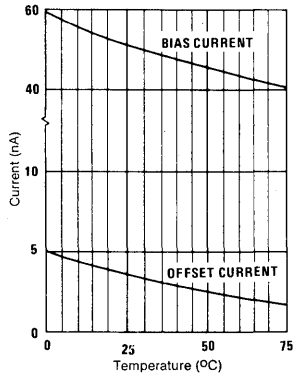
NOTES:
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 5VDC$
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2k\Omega$, $C_L = 50pF$.
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2k\Omega$, $C_L = 50pF$.
5. $V_{OUT} = 20V$ peak to peak.
6. $V_{OUT} = 200mV$ peak to peak.
7. $V_{OUT} = 10.0V$ peak to peak.
8. To 0.1% of final value.
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10VDC$
11. $V_{SUPPLY} = \pm 10VDC$ to $\pm 20VDC$
12. Unselected channels have approximately the same input parameters.
13. $V_{OUT} = \pm 10V$
14. Full power Bandwidth based on slew rate measurement using:

$$FPBW = \frac{S.R.}{2\pi\ Vpeak}$$

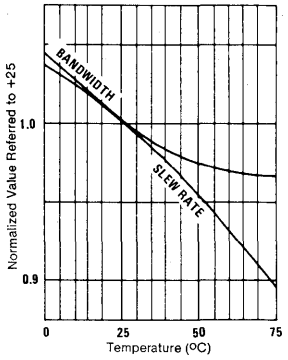
15. Sample tested.

Typical Performance Curves V+ = 15V D.C., V- = 15V D.C., T_A = +25°C Unless Otherwise Stated.

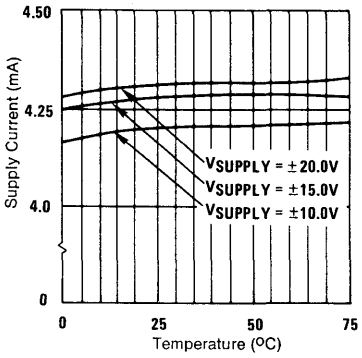
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



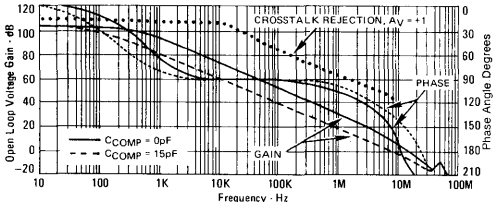
NORMALIZED A. C. PARAMETERS vs TEMPERATURE



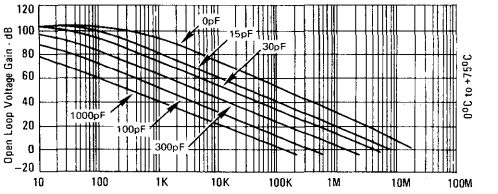
POWER SUPPLY CURRENT DRAIN AS A FUNCTION OF TEMPERATURE



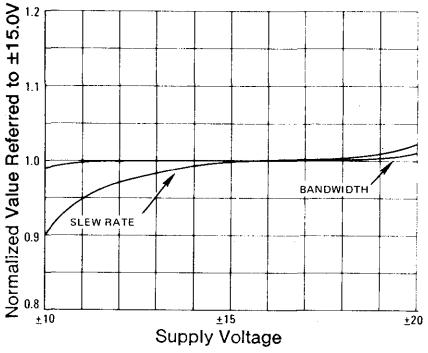
OPEN LOOP FREQUENCY AND PHASE RESPONSE



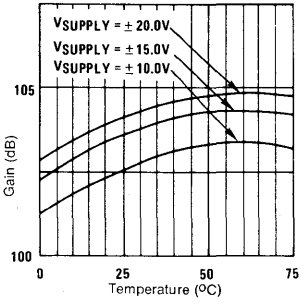
FREQUENCY RESPONSE vs CCOMP



NORMALIZED A. C. PARAMETERS vs SUPPLY VOLTAGE

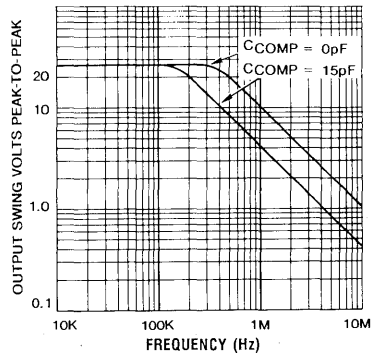


OPEN LOOP VOLTAGE GAIN vs TEMPERATURE

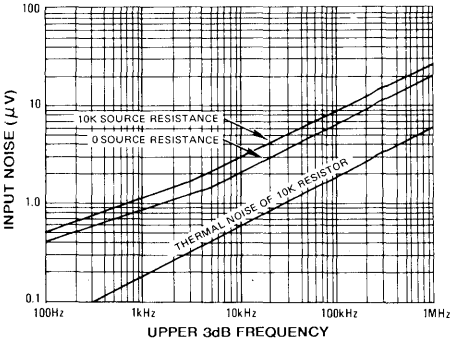


Typical Performance Curves (Continued)

OUTPUT VOLTAGE SWING vs FREQUENCY

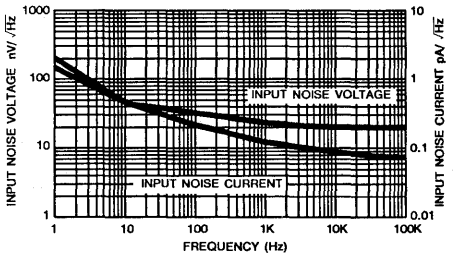


EQUIVALENT INPUT NOISE vs BANDWIDTH

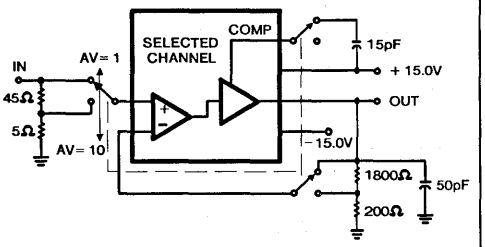


UPPER 3dB FREQUENCY
LOWER 3dB FREQUENCY-10Hz
BROADBAND NOISE CHARACTERISTICS

INPUT NOISE vs FREQUENCY

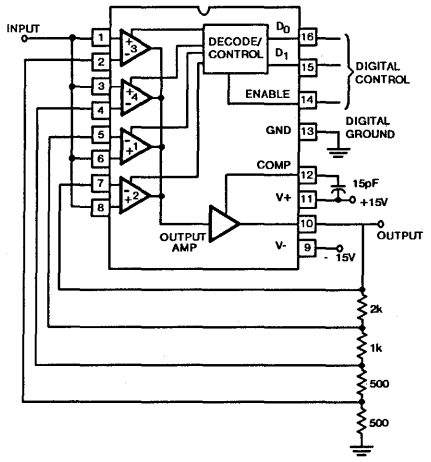


SLEW RATE AND TRANSIENT RESPONSE

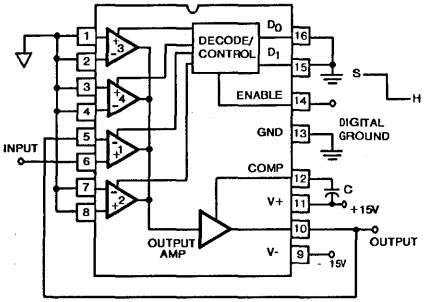


Typical Applications

HA-2406
AMPLIFIER, NON-INVERTING
PROGRAMMABLE GAIN



HA-2406
SAMPLE AND HOLD



Sample charging rate = $\frac{I1}{C}$ V/sec. $\quad I1 \approx 150 \times 10^{-6}$A

Hold drift rate = $\frac{I2}{C}$ V/sec. $\quad I2 \approx 200 \times 10^{-9}$A at +25°C; $\approx 600 \times 10^{-9}$A at -55°C; $\approx 100 \times 10^{-9}$A at +125°C

Switch pedestal error = $\frac{Q}{C}$ Volts $\quad Q \approx 2 \times 10^{-12}$ Coul.

For more examples, see Harris Application Note 514.

3 OPERATIONAL AMPLIFIERS

HARRIS HA-2500/02/05

May 1990

Precision High Slew Rate Operational Amplifiers

Features

- High Slew Rate 30V/μs
- Fast Settling 330ns
- Wide Power Bandwidth 500KHz
- High Gain Bandwidth 12MHz
- High Input Impedance 50MΩ
- Low Offset Current 10nA
- Internally Compensated For Unity Gain Stability

Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

HA-2500/2502/2505 comprises a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

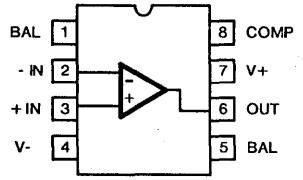
These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Slew rates of ±25V/μs and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12MHz small signal bandwidth and 500kHz power bandwidth make these devices well suited to R.F. and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2500/2502/2505 are particularly useful components in signal conditioning designs.

The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

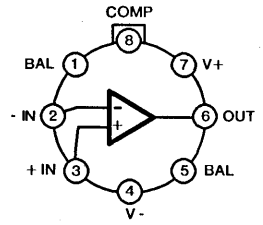
The HA-2500 and HA-2502 have guaranteed operation from -55°C to +125°C and are available in Hermetic Metal Can and Ceramic Mini-DIP packages. Both are offered as a /883 military grade part with the HA-2502 also available in LCC package. The HA-2505 has guaranteed operation from 0°C to +75°C and is available in Plastic and Ceramic Mini-DIP and Metal Can packages. Mil-Std-883 product and data sheets are available upon request. The HA-2505 is also offered in SOIC packaging in -5 and -9 temperature grades.

Pinouts

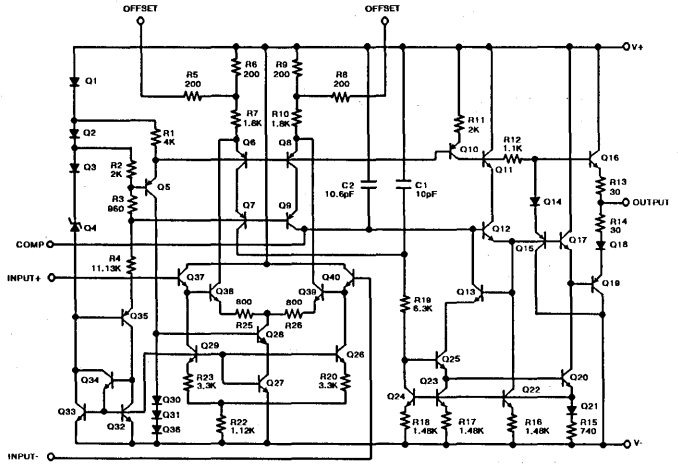
HA9P2505 (SOIC)
HA7-2500/02/05 (CERAMIC MINI-DIP)
HA3-2505 (PLASTIC MINI-DIP)
TOP VIEW



HA2-2500/02/05 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 6)

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage ..... ±15.0V
Peak Output Current 50mA
Internal Power Dissipation 300mW
Lead Solder Temperature (10 Seconds) ..... +275°C

Operating Temperature Range

HA-2500/2502-2 ..... $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-2505-5 ..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
HA-2505-9 ..... $-40^{\circ}C \leq T_A \leq +85^{\circ}C$
Storage Temperature Range ..... $-65^{\circ}C \leq T_A \leq +150^{\circ}C$
Maximum Junction Temperature ..... +175°C

Electrical Specifications V+ = +15V DC, V- = -15V DC

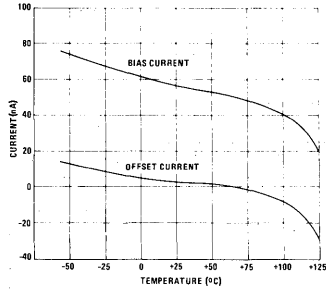
PARAMETER	TEMP.	HA-2500-2			HA-2502-2			HA-2505-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	2	5	-	4	8	-	4	8	mV
	Full	-	-	8	-	-	10	-	-	10	mV
Offset Voltage Average Drift	Full	-	20	-	-	20	-	-	20	-	µV/°C
Bias Current	+25°C	-	100	200	-	125	250	-	125	250	nA
	Full	-	-	400	-	-	500	-	-	500	nA
Offset Current	+25°C	-	10	25	-	20	50	-	20	50	nA
	Full	-	-	50	-	-	100	-	-	100	nA
Input Resistance (Note 10)	+25°C	25	50	-	20	50	-	20	50	-	MΩ
Common Mode Range	Full	±10.0	-	-	±10.0	-	-	±10.0	-	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	+25°C	20K	30K	-	15K	25K	-	15K	25K	-	V/V
(Note 1, 4)	Full	15K	-	-	10K	-	-	10K	-	-	V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90	-	74	90	-	74	90	-	dB
Gain Bandwidth Product (Note 3)	+25°C	-	12	-	-	12	-	-	12	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0	-	±10.0	±12.0	-	±10.0	±12.0	-	V
Output Current (Note 4)	+25°C	±10	±20	-	±10	±20	-	±10	±20	-	mA
Full Power Bandwidth (Notes 4, 11)	+25°C	350	500	-	300	500	-	300	500	-	KHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 7 & 8)	+25°C	-	25	50	-	25	50	-	25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C	-	25	40	-	25	50	-	25	50	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±25	±30	-	±20	±30	-	±20	±30	-	V/µs
Settling Time to 0.1% (Notes 1, 5, 8 & 12)	+25°C	-	0.33	-	-	0.33	-	-	0.33	-	µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C	-	4	6	-	4	6	-	4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:

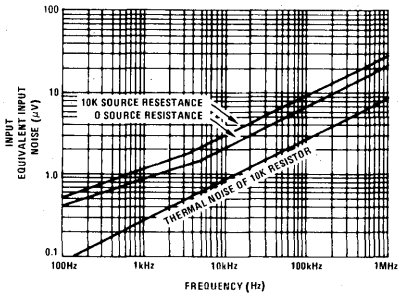
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. Absolute Maximum Ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired.
7. $V_O = \pm 200mV$
8. See Transient Response Test Circuits and Waveforms.
9. $\Delta V = \pm 5.0V$
10. This parameter value is based on design calculations.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = S.R./2πVpeak.
12. $V_{OUT} = \pm 5V$.

Performance Curves V+ = +15VDC, V- = -15VDC, T_A = +25°C, Unless Otherwise Stated

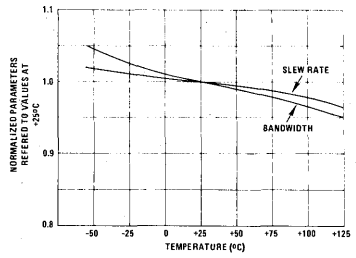
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



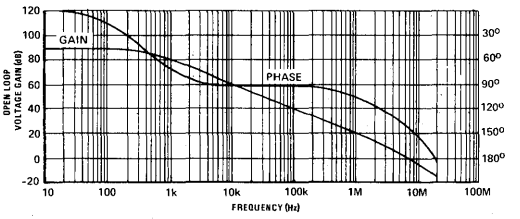
EQUIVALENT INPUT NOISE vs. BANDWIDTH
(With 10Hz High Pass Filter)



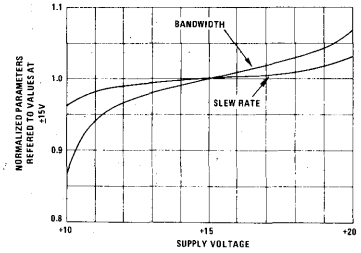
NORMALIZED AC PARAMETERS vs. TEMPERATURE



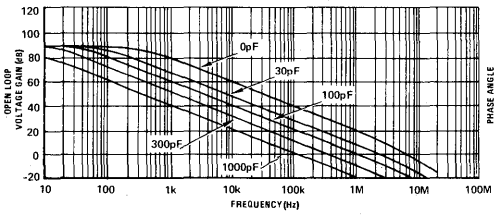
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE AT +25°C

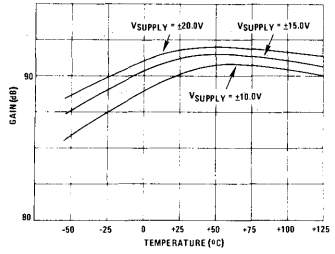


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

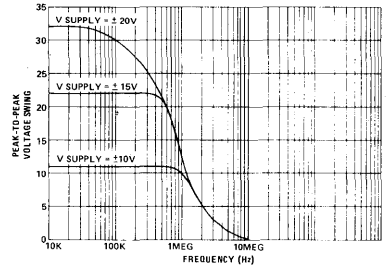


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE

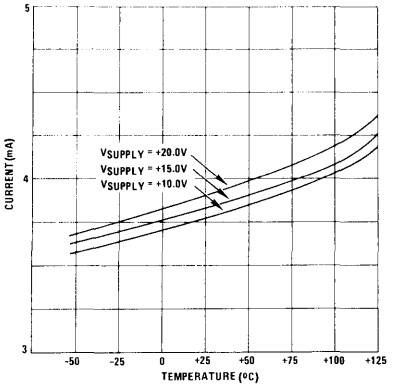


OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C

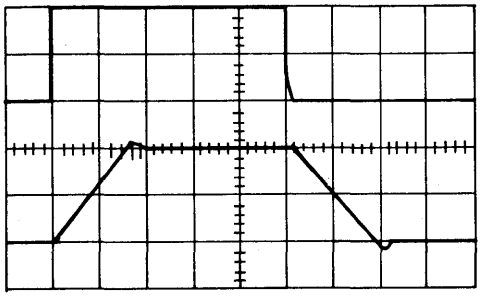


Typical Performance Curves (Continued)

POWER SUPPLY CURRENT vs TEMPERATURE



VOLTAGE FOLLOWER PULSE RESPONSE

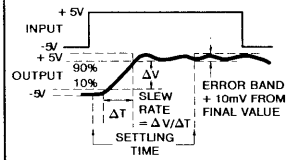


R_L = 2KΩ, C_L = 50pF
Upper Trace: Input
Lower Trace: Output

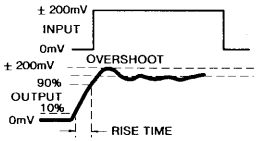
Vertical = 5V/Div.
Horizontal = 200ns/Div.
T_A = +25°C, V_S = ±15.0V

Test Circuits

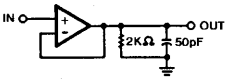
SLEW RATE AND SETTLING TIME



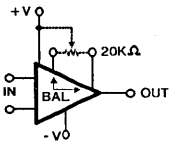
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE



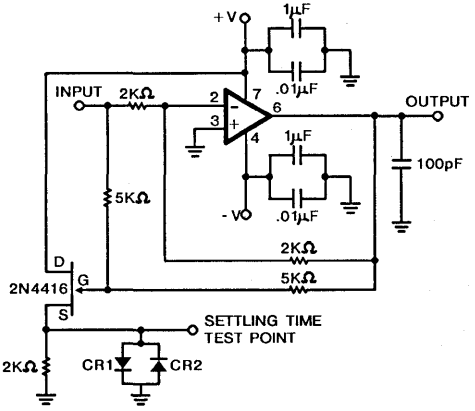
SUGGESTED V_{OS} ADJUSTMENT



NOTE: Measured on Both Positive and Negative Transitions from 0V to +200mV and 0V to -200mV at the output.

Tested Offset Adjustment Range is | V_{OS} +1mV | minimum referred to output. Typical ranges are ±6mV with R_T = 20kΩ.

Settling Time Circuit



- A_V = -1
- Feedback and Summing Resistor Ratios Should be 0.1% matched.
- Clipping Diodes CR1 and CR2 are Optional. HP5082-2810 Recommended.

Die Characteristics

Transistor Count 40
Die Dimensions ..... 57 x 65 x 19 mils
Substrate Potential ..... Unbiased
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-Metal Can (-2, -5, -7)	202	56
HA2-Metal Can (-8, /883)	168	52
HA3-Plastic Mini-DIP (-5)	84	34
HA4-Ceramic LCC (/883)	97	35
HA7-Ceramic Mini-DIP (-8, /883)	138	63
HA7-Ceramic Mini-DIP (-2, -5, -7)	204	112
HA9P-SOIC (-5, -9)	160	42

HARRIS HA-2510/12/15

May 1990

High Slew Rate Operational Amplifiers

Features

- High Slew Rate 60V/μs
- Fast Settling 250ns
- Wide Power Bandwidth 1,000kHz
- High Gain Bandwidth 12MHz
- High Input Impedance 100MΩ
- Low Offset Current 10nA
- Internally Compensated For Unity Gain Stability

Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

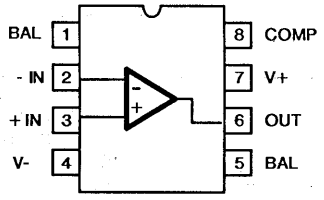
HA-2510/2512/2515 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidths for internally compensated monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

The ±60V/μs slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/2512/2515's superior 12MHz gain bandwidth and 1000kHz power-bandwidth is extremely useful in R.F. and video applications. For accurate signal conditioning these amplifiers also provide 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

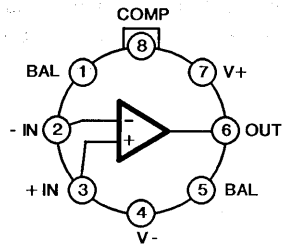
The HA-2510 and HA-2512 have guaranteed operation from -55°C to +125°C and are available in Metal Can and Ceramic Mini-DIP packages. Both are offered as a /883 military grade part with the HA-2512 also available in LCC package. The HA-2515 has guaranteed operation from 0°C to +75°C and is available in Plastic and Ceramic Mini-DIP and Metal Can packages. Mil-Std-883 product and data sheets are available upon request. Additionally, SOIC packaging is available for the HA-2515 in -5 and -9 temperature grades.

Pinouts

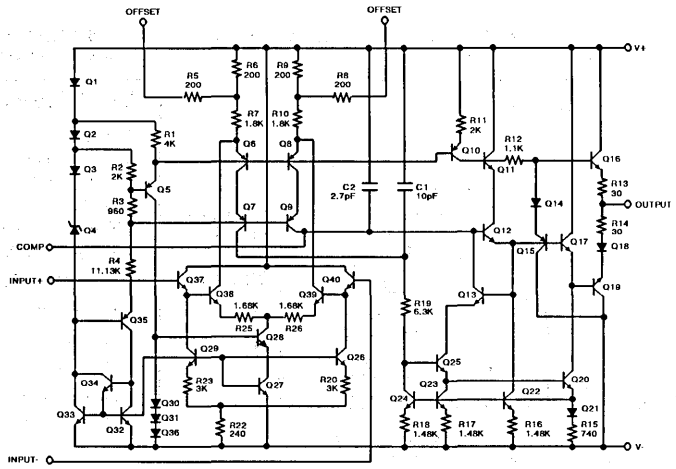
HA9P2515 (SOIC)
HA7-2510/12/15 (CERAMIC MINI-DIP)
HA3-2515 (PLASTIC MINI-DIP)
TOP VIEW



HA2-2510/12/15 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION:These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 6)

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage ..... ±15.0V
Peak Output Current 50mA
Internal Power Dissipation 300mW
Lead Solder Temperature (10 Seconds) ..... +275°C

Operating Temperature Range

HA-2510/2512-2 ..... $-55°C \leq T_A \leq +125°C$
HA-2515-5 ..... $0°C \leq T_A \leq +75°C$
HA-2515-9 ..... $-40°C \leq T_A \leq +85°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$
Maximum Junction Temperature ..... +175°C

Electrical Specifications V+ = +15V DC, V- = -15V DC

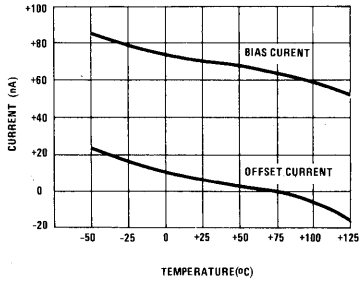
PARAMETER	TEMP.	HA-2510-2			HA-2512-2			HA-2515-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	4	8	-	5	10	-	5	10	mV
	Full	-	-	11	-	-	14	-	-	14	mV
Offset Voltage Average Drift	Full	-	20	-	-	25	-	-	30	-	µV/°C
Bias Current	+25°C	-	100	200	-	125	250	-	125	250	nA
	Full	-	-	400	-	-	500	-	-	500	nA
Offset Current	+25°C	-	10	25	-	20	50	-	20	50	nA
	Full	-	-	50	-	-	100	-	-	100	nA
Input Resistance (Note 10)	+25°C	50	100	-	40	100	-	40	100	-	MΩ
Common Mode Range	Full	±10.0	-	-	±10.0	-	-	±10.0	-	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	10K	15K	-	7.5K	15K	-	7.5K	15K	-	V/V
	Full	7.5K	-	-	5K	-	-	5K	-	-	V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90	-	74	90	-	74	90	-	dB
Gain Bandwidth Product (Note 3)	+25°C	-	12	-	-	12	-	-	12	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0	-	±10.0	±12.0	-	±10.0	±12.0	-	V
Output Current (Note 4)	+25°C	±10	±20	-	±10	±20	-	±10	±20	-	mA
Full Power Bandwidth (Notes 4, 11)	+25°C	750	1000	-	600	1000	-	600	1000	-	kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 7 & 8)	+25°C	-	25	50	-	25	50	-	25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C	-	25	40	-	25	50	-	25	50	%
Slew Rate (Notes 1, 5, 8 & 12)	+25°C	±50	±65	-	±40	±60	-	±40	±60	-	V/µs
Settling Time to 0.1% (Notes 1, 5, 8 & 12)	+25°C	-	0.25	-	-	0.25	-	-	0.25	-	µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C	-	4	6	-	4	6	-	4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:

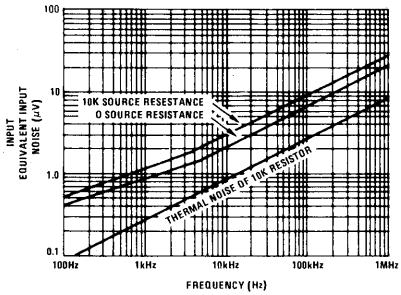
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. Absolute Maximum Ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired.
7. $V_O = \pm 200mV$
8. See Transient Response Test Circuits and Waveforms.
9. $\Delta V = \pm 5.0V$
10. This parameter value is based on design calculations.
11. Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = S.R./2πVpeak.
12. $V_{OUT} = \pm 5V$.

Performance Curves V+ = +15VDC, V- = -15VDC, T_A = +25°C, Unless Otherwise Stated

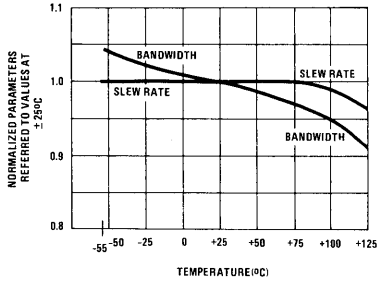
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



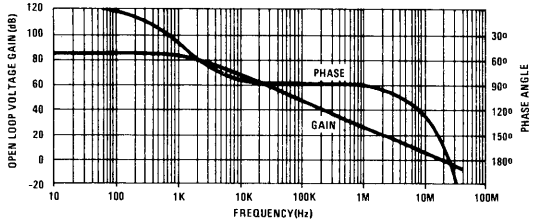
EQUIVALENT INPUT NOISE vs. BANDWIDTH (With 10Hz High Pass Filter)



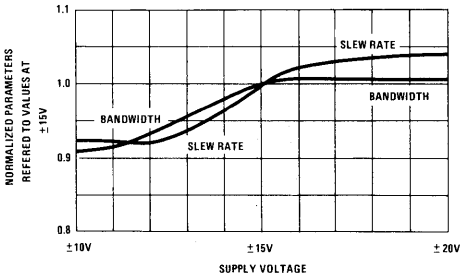
NORMALIZED AC PARAMETERS vs. TEMPERATURE



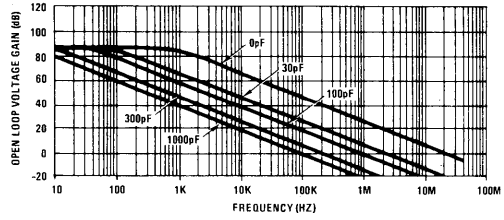
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE AT +25°C

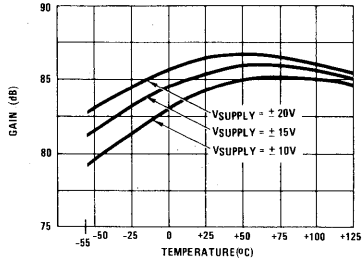


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

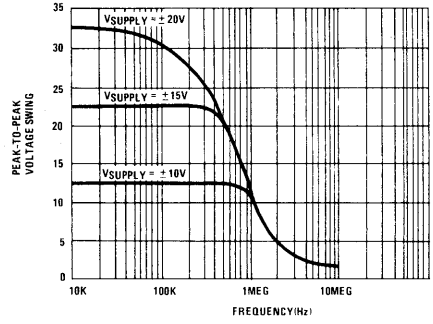


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE

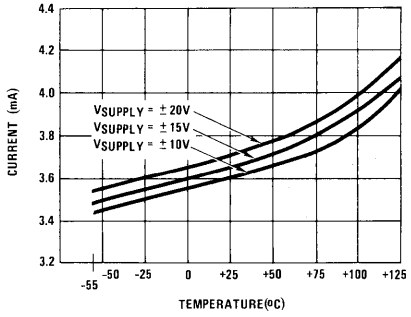


OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C

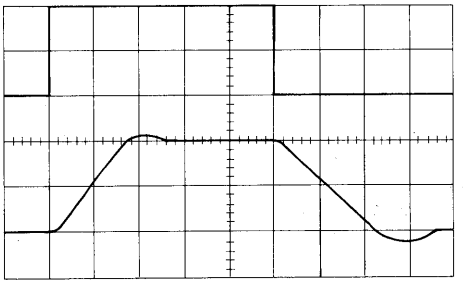


Typical Performance Curves (Continued)

POWER SUPPLY CURRENT vs TEMPERATURE



VOLTAGE FOLLOWER PULSE RESPONSE

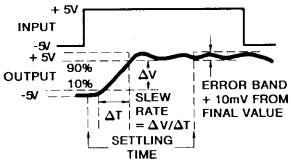


R_L = 2KΩ, C_L = 50pF
Upper Trace: Input
Lower Trace: Output

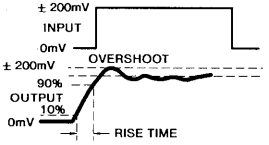
Vertical = 5V/Div.
Horizontal = 200ns/Div.
T_A = +25°C, V_S = ±15.0V

Test Circuits

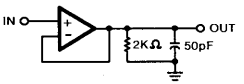
SLEW RATE AND SETTLING TIME



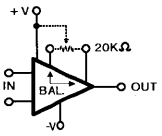
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE



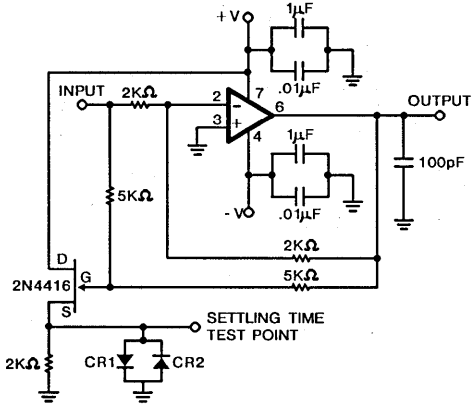
SUGGESTED V_{OS} ADJUSTMENT



NOTE: Measured on Both Positive and Negative Transitions from 0V to +200mV and 0V to -200mV at the output.

Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ minimum referred to output. Typical ranges are ±6mV with R_T = 20kΩ.

Settling Time Circuit



- A_V = -1
- Feedback and Summing Resistor Ratios Should be 0.1% matched.
- Clipping Diodes CR1 and CR2 are Optional. HP5082-2810 Recommended.

Die Characteristics

Transistor Count 40
Die Dimensions ..... 57 x 65 x 19 mils
Substrate Potential ..... Unbiased
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-Metal Can (-2, -5, -7)	202	56
HA2-Metal Can (-8, /883)	168	52
HA3-Plastic Mini-DIP (-5)	84	34
HA4-Ceramic LCC (/883)	97	35
HA7-Ceramic Mini-DIP (-8, /883)	138	63
HA7-Ceramic Mini-DIP (-2, -5, -7)	204	112
HA9P-SOIC (-5, -9)	160	42

HARRIS HA-2520/22/25

Uncompensated High Slew Rate Operational Amplifiers

May 1990

Features

- High Slew Rate 120V/μs
- Fast Settling 200ns
- Wide Power Bandwidth 2,000kHz
- High Gain Bandwidth ($A_V \geq 3$) 20MHz
- High Input Impedance 100MΩ
- Low Offset Current 10nA

Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

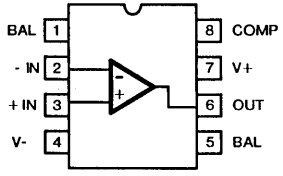
HA-2520/2522/2525 comprise a series of monolithic operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at close loop gains greater than 3 without external compensation. In addition, these high performance components also provide low offset current and high input impedance.

120V/μs slew rate and 200ns (0.2%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for R.F. and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complimented by 10nA offset current, 200MΩ input impedance and offset trim capability.

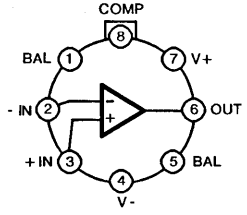
The HA-2520 and HA-2522 have guaranteed operation from -55°C to +125°C and are available in metal can and Ceramic Mini-DIP packages. Both are offered in /883 grade with the HA-2522 also available in LCC package. The HA-2525 has guaranteed operation from 0°C to +75°C and is available in plastic and Ceramic Mini-DIP and metal can packages. Mil-Std-883 product and data sheets are available upon request. Additionally, the HA2525 is available in SOIC packaging with -5 and -9 temperature ranges.

Pinouts

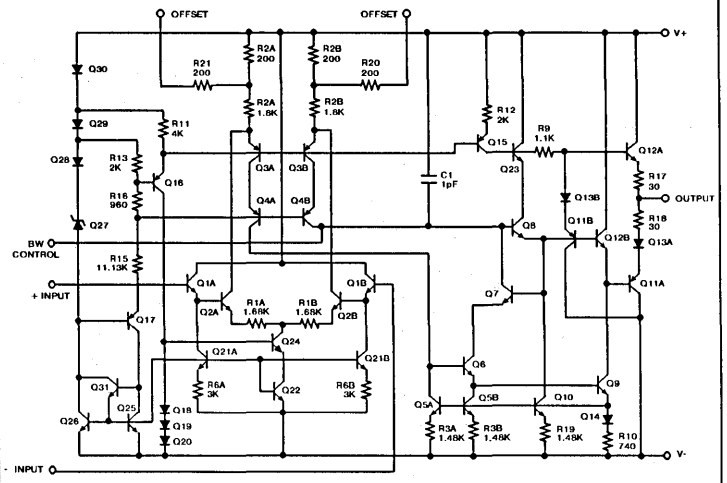
HA7-2520/22/25 (CERAMIC MINI-DIP)
HA3-2525 (PLASTIC MINI-DIP)
HA9P2525 (SOIC)
TOP VIEW



HA2-2520/22/25 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION:These devices are sensitive to electronic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 13)

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage..... ±15.0V
Peak Output Current 50mA
Internal Power Dissipation 300mW
Lead Solder Temperature (10 Seconds) ..... +275°C

Operating Temperature Range

HA-2520/2522-2 ..... $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-2525-5..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
HA-2525-9..... $-40^{\circ}C \leq T_A \leq +85^{\circ}C$
Storage Temperature Range ..... $-65^{\circ}C \leq T_A \leq +150^{\circ}C$
Maximum Junction Temperature..... +175°C

Electrical Specifications V+ = +15V DC, V- = -15V DC

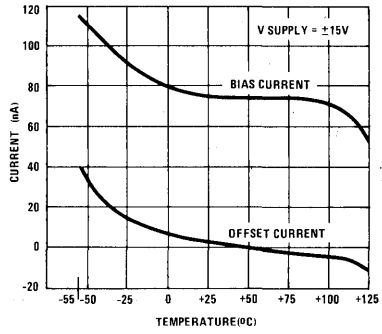
PARAMETER	TEMP	HA-2520-2			HA-2522-2			HA-2525-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	4	8	-	5	10	-	5	10	mV
	Full	-	-	11	-	-	14	-	-	14	mV
Offset Voltage Drift	Full	-	20	-	-	25	-	-	30	-	µV/°C
Bias Current	+25°C	-	100	200	-	125	250	-	125	250	nA
	Full	-	-	400	-	-	500	-	-	500	nA
Offset Current	+25°C	-	10	25	-	20	50	-	20	50	nA
	Full	-	-	50	-	-	100	-	-	100	nA
Input Resistance (Note 9)	+25°C	50	100	-	40	100	-	40	100	-	MΩ
Common Mode Range	Full	±10.0	-	-	±10.0	-	-	±10.0	-	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 1, 4)	+25°C	10K	15K	-	7.5K	15K	-	7.5K	15K	-	V/V
	Full	7.5K	-	-	5K	-	-	5K	-	-	V/V
Common Mode Rejection Ratio (Note 2)	Full	80	90	-	74	90	-	74	90	-	dB
Gain Bandwidth Product (Notes 3, 12)	+25°C	10	20	-	10	20	-	10	20	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0	-	±10.0	±12.0	-	±10.0	±12.0	-	V
Output Current (Note 4)	+25°C	±10	±20	-	±10	±20	-	±10	±20	-	mA
Full Power Bandwidth (Notes 4, 10)	+25°C	1500	2000	-	1200	1600	-	1200	1600	-	kHz
TRANSIENT RESPONSE (A_V = +3V)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C	-	25	50	-	25	50	-	25	50	ns
Overshoot (Notes 1, 5, 6, & 8)	+25°C	-	25	40	-	25	50	-	25	50	%
Slew Rate (Notes 1, 5, 8 & 11)	+25°C	±100	±120	-	±80	±120	-	±80	±120	-	V/µs
Settling Time (Notes 1, 5, 8 & 11)	+25°C	-	0.20	-	-	0.20	-	-	0.20	-	µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C	-	4	6	-	4	6	-	4	6	mA
Power Supply Rejection Ratio (Note 7)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:

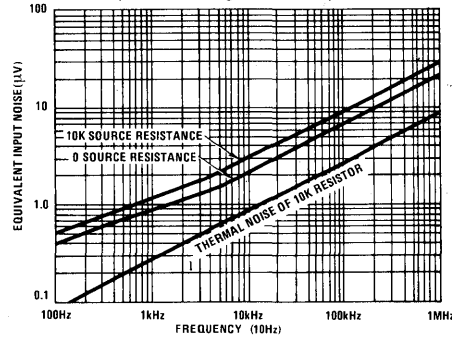
1. $R_L = 2k\Omega$
2. $V_{CM} = \pm 10V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. See Transient Response Test Circuits and Waveforms.
9. This parameter value is based on design calculations.
10. Full Power Bandwidth guaranteed based on slew rate measurement using: FPBW = S.R./2πVpeak.
11. $V_{OUT} = \pm 5V$
12. Guaranteed by design.
13. Absolute Maximum Ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

Performance Curves V+ = +15VDC, V- = -15VDC, T_A = +25°C, Unless Otherwise Stated

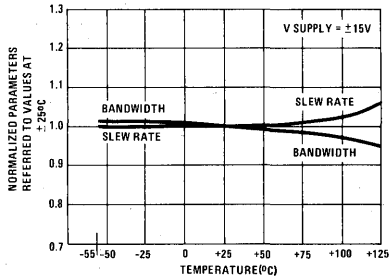
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



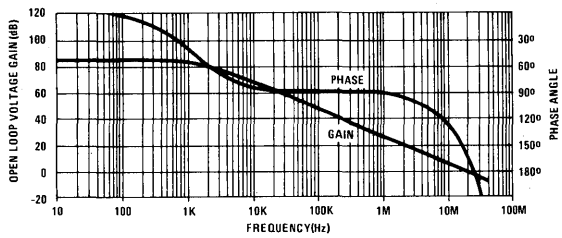
EQUIVALENT INPUT NOISE vs. BANDWIDTH
(with 10 Hz High Pass Filter)



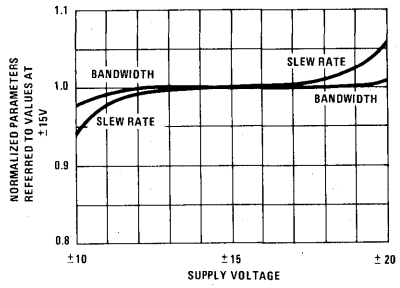
NORMALIZED AC PARAMETERS vs. TEMPERATURE



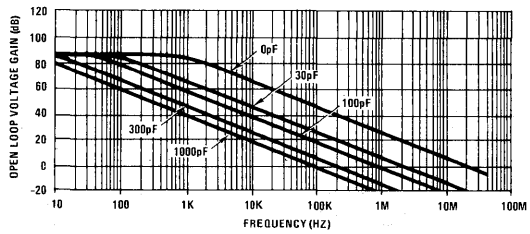
OPEN-LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE AT +25°C

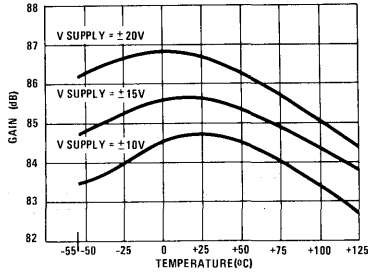


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND

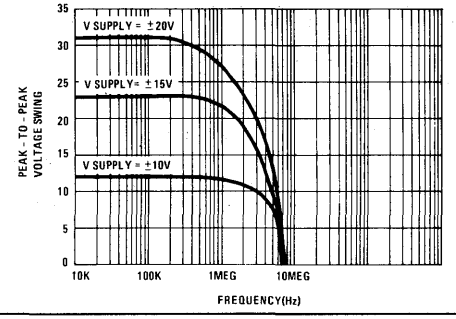


NOTE: External compensation components are not required for stability, but may be added to reduce bandwidth if desired.

OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE

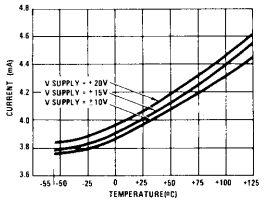


OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C

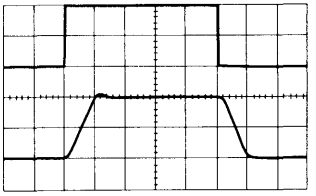


Performance Curves (Continued)

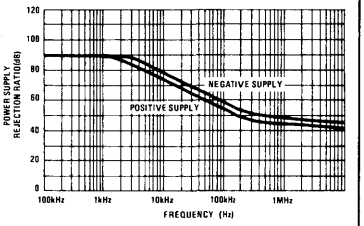
POWER SUPPLY CURRENT vs. TEMPERATURE



VOLTAGE FOLLOWER PULSE RESPONSE



POWER SUPPLY REJECTION RATIO vs. FREQUENCY

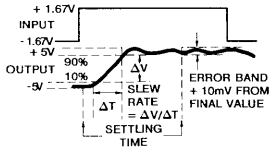


R_L = 2KΩ, C_L = 50pF
Upper Trace: Input; 1.67V/Div.
Lower Trace: Output; 5V/Div.

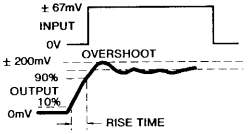
Horizontal = 100ns/Div.
T_A = +25°C, V_S = ±15V

Test Circuits

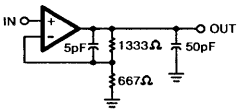
SLEW RATE AND SETTLING TIME



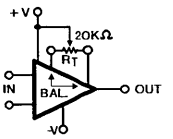
TRANSIENT RESPONSE



SLEW RATE AND TRANSIENT RESPONSE



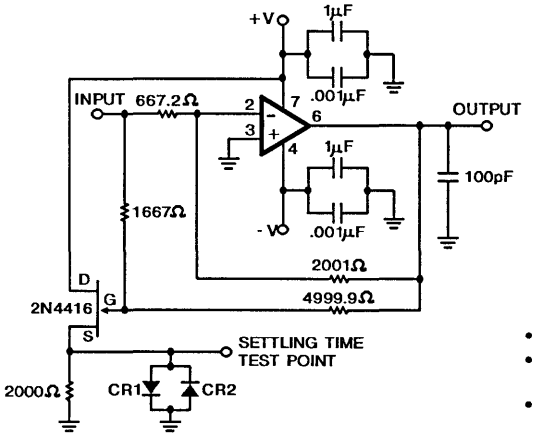
SUGGESTED V_{OS} ADJUSTMENT



NOTE: Measurement on both positive and negative transitions from 0V to +200mV and 0V to -200mV at the output.

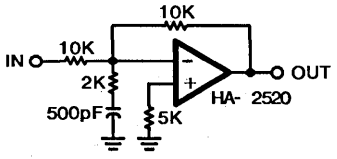
Tested Offset Adjustment Range is | VOS +1mV | minimum referred to ouput. Typical range is +20mV to -18mV with R_T = 20kΩ.

Settling Time Circuit



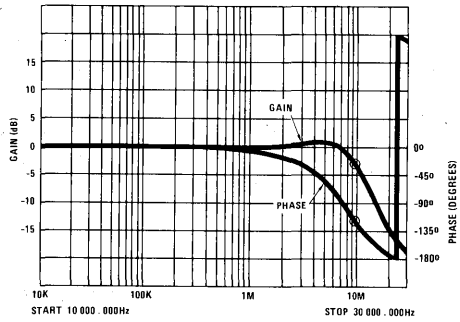
- A_V = -3
- Feedback and Summing Resistor Ratios Should be 0.1% matched.
- Clipping Diodes CR1 and CR2 are Optional. HP5082-2810 Recommended.

Typical Application



NOTE: Compensation Circuit for $A_V = -1$
Slew Rate ≈ 120V/μs
Bandwidth ≈ 10MHz
Settling Time (0.1%) ≈ 500ns
Capacitance at pin 8 must be minimized for maximum bandwidth.
Tested and functional with supply voltages from ±4V to ±15V.

FREQUENCY RESPONSE FOR
INVERTING UNITY GAIN CIRCUIT



Die Characteristics

Transistor Count 40
Die Dimensions ..... 57 x 65 x 19 mils
Substrate Potential ..... Unbiased
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-Metal Can (-2, -5, -7)	206	56
HA2-Metal Can (-8, /883)	168	52
HA3-Plastic Mini-DIP (-5)	90	39
HA4-Ceramic LCC (/883)	99	37
HA7-Ceramic Mini-DIP (-8, /883)	140	65
HA7-Ceramic Mini-DIP (-2, -5, -7)	204	112
HA9P-SOIC (-5, -9)	160	42

HARRIS

HA-2529

May 1990

Uncompensated, High Slew Rate High Output Current, Operational Amplifier

Features

- High Slew Rate 150V/μs
- Fast Settling 200ns
- Wide Power Bandwidth 2MHz
- Wide Gain Bandwidth ($A_V \geq 3$) 20MHz
- High Input Impedance 130MΩ
- Low Offset Current 200nA
- High Output Current ..... ±30mA

Applications

- Data Acquisition Systems
- R.F. Amplifiers
- Video Amplifiers
- Signal Generators
- Pulse Amplification

Description

The HA-2529 is a monolithic operational amplifier which typifies excellence of design. With a design based on years of experience coupled with the reliable dielectric isolation process, these amplifiers provide an outstanding combination of DC and AC parameters at closed loop gains greater than 3.

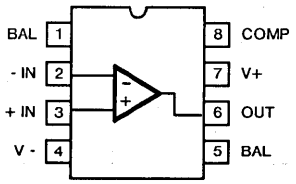
The HA-2529 offers 150V/μs slew rate and fast settling time (200ns), while consuming a mere 6mA of quiesent current, making these amplifiers ideal components for video circuitry and data acquisition designs. With 20MHz gain-bandwidth combined with 7.5kV/V open loop gain, the HA-2529 is an ideal component for demanding signal conditioning designs.These devices provide ±30mA output current drive with an output voltage swing of ±10V making then suited for pulse amplifier and R.F. amplifier components.

The HA-2529 will upgrade output current, slew rate, offset voltage drift and offset current drift in systems presently using the HA-2520/22/25 or EHA-2520/22/25.

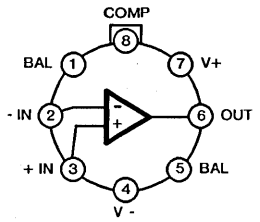
The HA-2529-2 has guaranteed operation over the military temperature range (-55°C to +125°C) and the HA-2529-5 has guaranteed operation over the commercial temperature range (0°C to +75°C). MIL-STD-883 product and data sheets are available upon request.

Pinouts

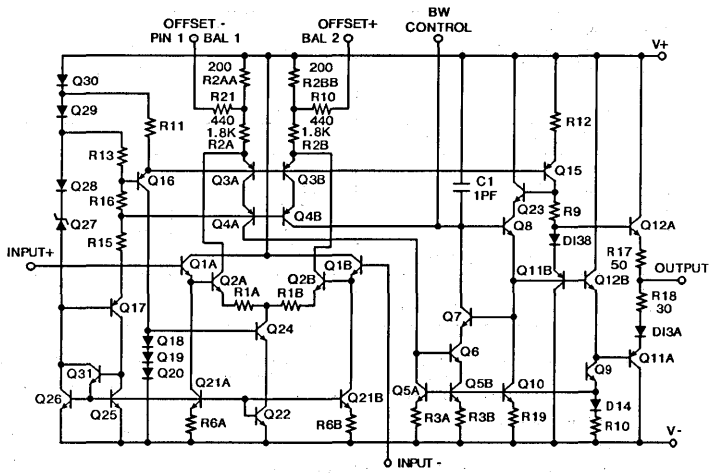
HA9P2529 (SOIC)
HA7-2529 (CERAMIC MINI-DIP)
HA3-2529 (PLASTIC MINI-DIP)
TOP VIEW



HA2-2529 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage..... ±15V
Output Current ..... 90mA (Peak)
Internal Power Dissipation (Note 10) 300mW
Maximum Junction Temperature..... +175°C

Operating Temperature Ranges

HA-2529-2.....$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-2529-5..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range .....$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

Electrical Specifications $V_S = \pm 15V$, $C_L = 50pF$, $R_L = 2k\Omega$, Unless Otherwise Specified

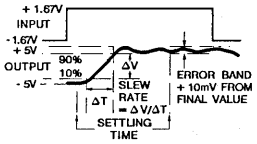
PARAMETER	TEMP	HA-2529-2 -55°C to +125°C MIN	TYP	MAX	HA-2529-5 0°C to +75°C MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage (Note 8)	+25°C	-	2	5	-	2	10	mV
	Full	-	-	8	-	-	14	mV
Average Offset Voltage Drift (Note 8)	Full	-	10	-	-	10	-	µV/°C
Bias Current (Note 8)	+25°C	-	50	200	-	50	250	nA
	Full	-	80	400	-	80	400	nA
Average Bias Current Drift (Note 8)	Full	-	0.2	-	-	0.2	-	nA/°C
Offset Current (Note 8)	+25°C	-	5	25	-	5	50	nA
	Full	-	10	50	-	10	100	nA
Average Offset Current Drift	Full	-	0.02	-	-	0.02	-	nA/°C
Common Mode Range	Full	±10	±13	-	±10	±13	-	V
Differential Input Resistance (Note 11)	+25°C	50	130	-	50	130	-	MΩ
Differential Input Capacitance	+25°C	-	3	-	-	3	-	pF
Input Noise Voltage (f = 1kHz)	+25°C	-	20	-	-	20	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C	-	1.8	-	-	1.8	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	10	18	-	7.5	18	-	kV/V
	Full	7.5	15	-	5	15	-	kV/V
Common Mode Rejection Ratio (Note 5)	Full	80	100	-	74	100	-	dB
Gain-Bandwidth Product (Note 2, 11)	+25°C	15	20	-	15	20	-	MHz
Minimum Stable Gain	+25°C	3	-	-	3	-	-	V/V
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10	±12	-	±10	±12	-	V
Full Power Bandwidth (Notes 3 & 6)	+25°C	2.1	2.6	-	2.1	2.6	-	MHz
Output Current (Note 8)	+25°C	30	35	-	30	35	-	mA
	Full	25	30	-	25	30	-	mA
Output Resistance (Open Loop)	+25°C	-	30	-	-	30	-	Ω
TRANSIENT RESPONSE ($A_V = +3$)								
Rise Time (Note 2, 7)	+25°C	-	20	45	-	20	50	ns
Overshoot (Note 2, 7)	+25°C	-	10	30	-	10	30	%
Slew Rate (Note 3, 7)	+25°C	135	150	-	135	150	-	V/µs
Settling Time (Note 4, 7)	+25°C	-	200	-	-	200	-	ns
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	4.5	6	-	4.5	6	mA
Power Supply Rejection Ratio (Note 12)	Full	80	90	-	74	90	-	dB

NOTE:

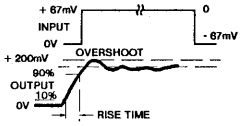
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $V_{OUT} = \pm 200mV$, $A_V \geq 3$.
3. $V_{OUT} = \pm 10V$.
4. Settling Time is specified to 0.1% of final value for a 10V output step and $A_V = -1$.
5. $\Delta V_{CM} = \pm 10V$.
6. Full Power Bandwidth is guaranteed by equation: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
7. See Transient Response and Settling Time Test Circuits.
8. Refer to typical performance curve in data sheet.
9. $V_{OUT} = \pm 5V$.
10. Refer to package thermal constants in Die Information section.
11. Parameter is guaranteed by design and characterization data.
12. $\Delta V_S = \pm 10V$ to $\pm 20V$.

Test Circuits

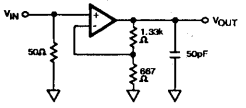
SLEW RATE AND SETTLING TIME WAVEFORM



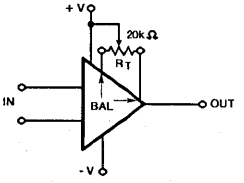
TRANSIENT RESPONSE WAVEFORM



SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



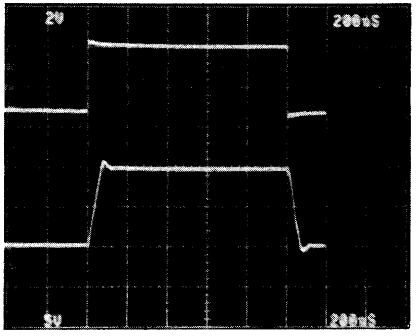
SUGGESTED V_{OS} ADJUSTMENT



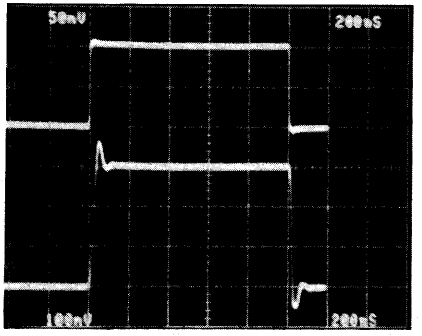
NOTE: Measured on both positive and negative transitions from 0 to +200mV and 0 to -200mV.

Tested Offset Adjustment is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is +28mV to -18mV with R_T = 20kΩ.

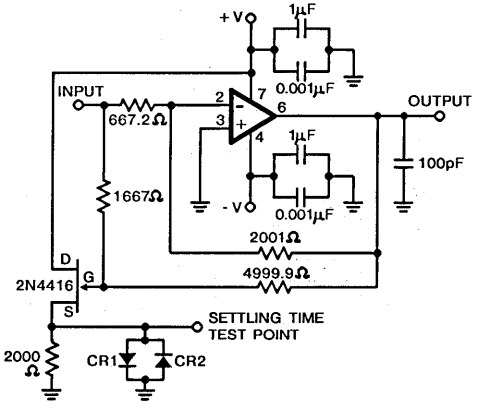
LARGE SIGNAL RESPONSE
Vertical Scale: (200ns/Div.)
Horizontal Scale: (2V/Div. Input)
(5V/Div. Output)



SMALL SIGNAL RESPONSE
Vertical Scale: (200ns/Div.)
Horizontal Scale : (50mV/Div. Input)
(100mV/Div. Output)



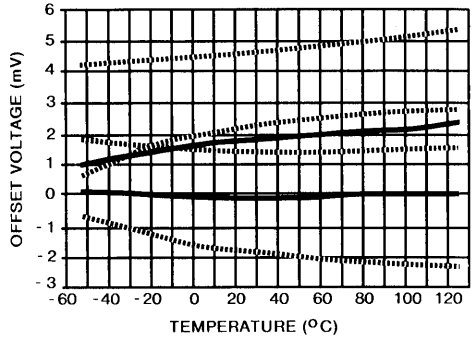
Settling Time Circuit



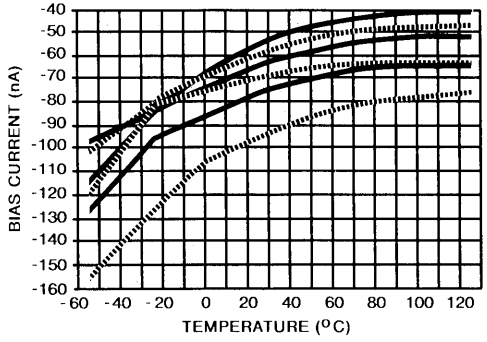
- A_V = -3
- Feedback and summing resistor ratios should be 0.1% matched.
- Clipping diodes CR1 and CR2 are optional. HP5082-2810 recommended.

Typical Performance Curves

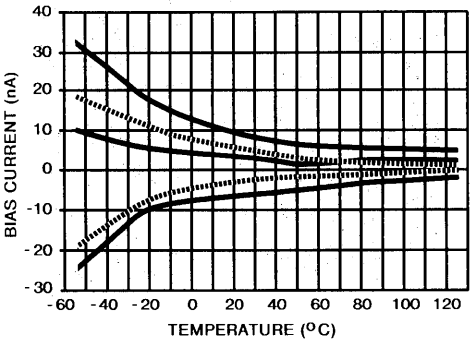
OFFSET VOLTAGE vs. TEMPERATURE
6 Typical Units From 3 Lots @ V_S = ±15V



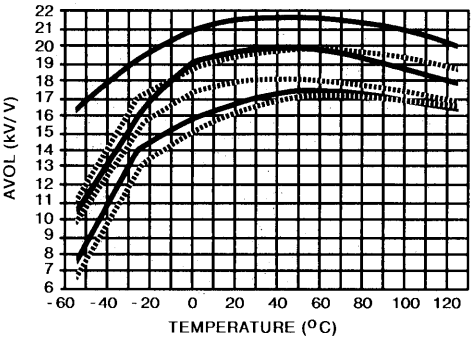
BIAS CURRENT vs. TEMPERATURE
6 Typical Units From 3 Lots @ V_S = ±15V



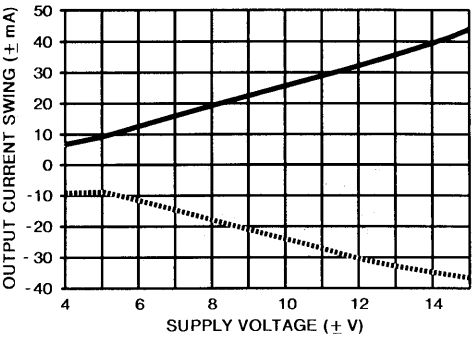
OFFSET CURRENT vs. TEMPERATURE
5 Typical Units From 3 Lots @ V_S = ±15V



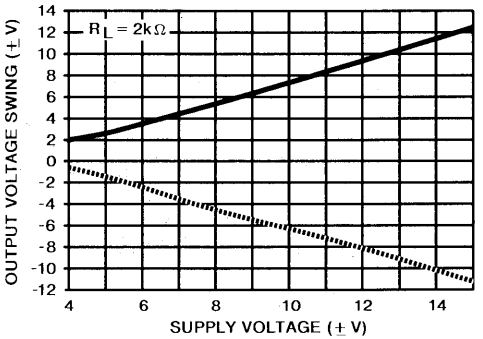
OPEN LOOP GAIN vs. TEMPERATURE
6 Typical Units From 3 Lots @ V_S = ±15V



OUTPUT CURRENT vs. SUPPLY VOLTAGE

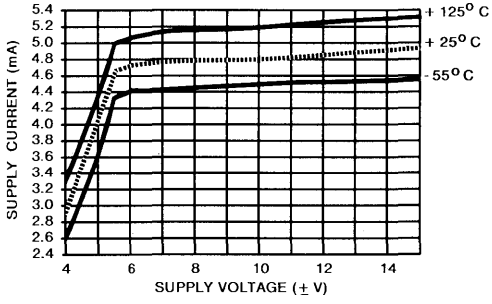


OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE

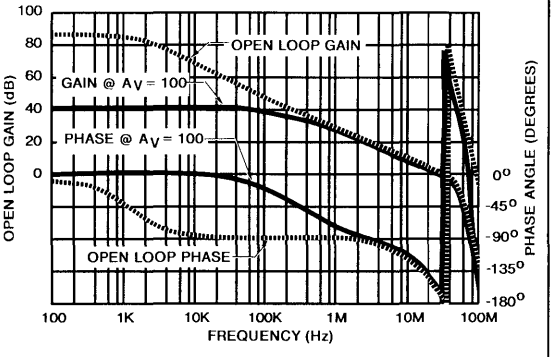


Typical Performance Curves (Continued)

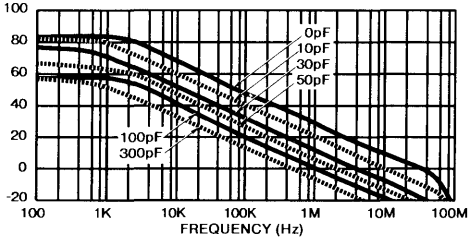
SUPPLY CURRENT vs. SUPPLY VOLTAGE
Over Full Temperature



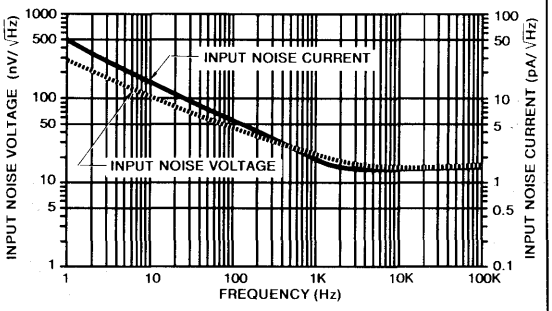
FREQUENCY RESPONSE AT VARIOUS GAINS



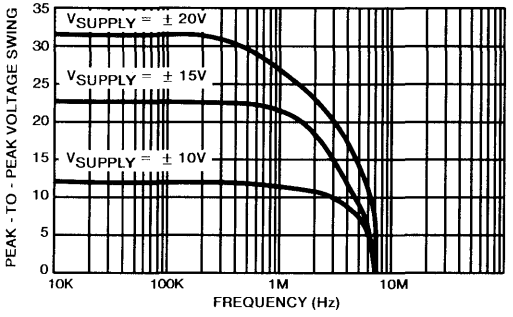
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM BANDWIDTH CONTROL PIN TO GROUND



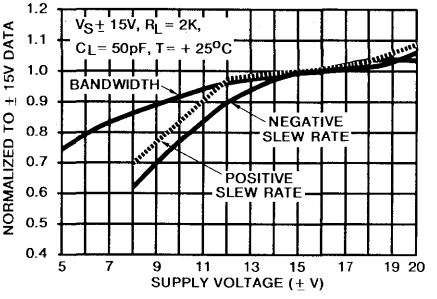
INPUT NOISE CHARACTERISTICS



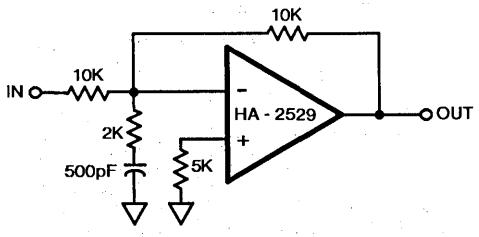
OUTPUT VOLTAGE SWING vs. FREQUENCY



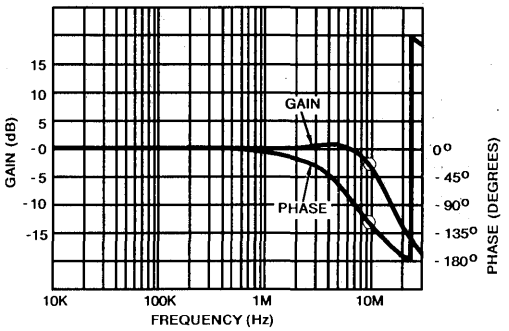
NORMALIZED A.C. PARAMETERS vs. SUPPLY VOLTAGE



Typical Applications



FREQUENCY RESPONSE FOR INVERTING UNITY GAIN CIRCUIT



NOTE:
- Compensation Circuit for $A_V = -1$
- Slew Rate ≈ 120V/µs
- Bandwidth ≈ 10MHz
- Settling Time (0.1%) ≈ 500ns
- Capacitance at pin 8 must be minimized for maximum bandwidth.
- Tested and functional with supply voltages from ±4V to ±15V.

Die Characteristics

Transistor Count 40

Die Dimensions ..... 1660µm x 1300µm x 485µm (65 mils x 51 mils x 19 mils)

Substrate Potential ..... V-

Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-Metal Can (-2, -5, -7)	206	56
HA2-Metal Can (-8, /883)	168	52
HA3-Plastic Mini-DIP (-5)	90	39
HA4-Ceramic LCC (/883)	99	37
HA7-Ceramic Mini-DIP (-8, /883)	140	65
HA7-Ceramic Mini-DIP (-2, -5, -7)	204	112

HARRIS

HA-2539

Very High Slew Rate Wideband Operational Amplifier

May 1990

Features

- Very High Slew Rate 600V/ms
- Open Loop Gain 30kV/V
- Wide Gain-Bandwidth ($A_V \leq 10$) 600MHz
- Power Bandwidth 9.5MHz
- Low Offset Voltage 8mV
- Input Voltage Noise ..... 6nV/$\sqrt{Hz}$
- Output Voltage Swing ..... ±10V
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- RF Oscillators

Description

The Harris HA-2539 represents the ultimate in high slew rate, wideband, monolithic operational amplifiers. It has been designed and constructed with the Harris High Frequency Bipolar Dielectric Isolation process and features dynamic parameters never before available from a truly differential device.

With a 600V/µs slew rate and a 600MHz gain bandwidth product, the HA-2539 is ideally suited for use in video and RF amplifier designs, in closed loop gains of 10 or greater. Full ±10V swing coupled with outstanding A.C. parameters and complemented by high open loop gain makes the devices useful in high speed data acquisition systems.

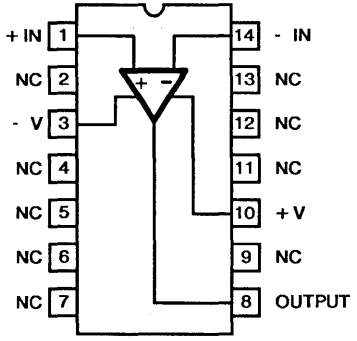
The HA-2539 is available in 14 pin ceramic and plastic DIP. The HA-2539-2 operates over -55°C to +125°C temperature range while the HA-2539-5 operates over the 0°C to +75°C range. Additionally, SOIC packaging is available in -5 and -9 temperature grades.

For further design assistance please refer to Application Note 541 (Using The HA-2539 Very High Slew Rate Wideband Operational Amplifiers) and Application Note 556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers).

For military grade product information, the HA-2539/883 data sheet is available upon request.

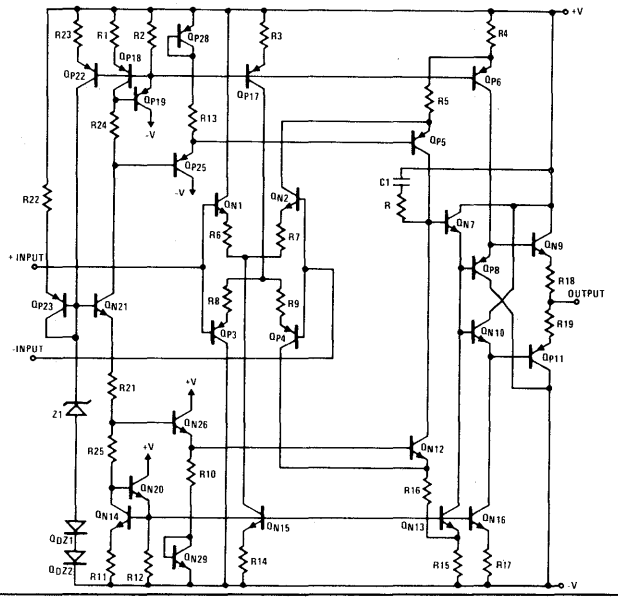
Pinout

HA1-2539/2539C (CERAMIC DIP)
HA3-2539/2539C (PLASTIC DIP)
HA9P2539/2539C (SOIC)
TOP VIEW



(N.C.) No Connection pins may be tied to a ground plane for better isolation and heat dissipation.

Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Voltage ..... ±6V
Peak Output Current 50mA
Continuous Output Current ..... $33mA_{rms}$
Internal Quiescent Power Dissipation (Note 2) ..... 870mW (Ceramic DIP)

Operating Temperature Range

HA-2539-2 ..... $-55^oC \leq TA \leq +125^oC$
HA-2539/2539C-5 ..... $0^oC \leq TA \leq +75^oC$
HA-2539-9 ..... $-40^oC \leq TA \leq +150^oC$
Storage Temperature Range ..... $-65^oC \leq TA \leq +150^oC$
Maximum Junction Temperature ..... $+175^oC$

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified.

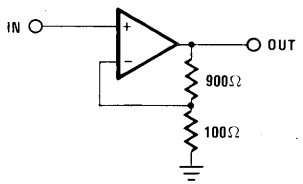
PARAMETER	TEMP	HA-2539-2			HA-2539-5, -9			HA-2539C-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	8	10	-	8	15	-	8	15	mV
	Full	-	13	15	-	13	20	-	13	20	mV
Average Offset Voltage Drift	Full	-	20	-	-	20	-	-	20	-	µV/°C
Bias Current	+25°C	-	5	20	-	5	20	-	5	20	µA
	Full	-	-	25	-	-	25	-	-	25	µA
Offset Current	+25°C	-	1	6	-	1	6	-	1	6	µA
	Full	-	-	8	-	-	8	-	-	8	µA
Input Resistance	+25°C	-	10	-	-	10	-	-	10	-	kΩ
Input Capacitance	+25°C	-	1	-	-	1	-	-	1	-	pF
Common Mode Range	Full	±10	-	-	±10	-	-	±10	-	-	V
Input Current Noise ($f = 1KHz, R_{SOURCE} = 0\Omega$)	+25°C	-	6	-	-	6	-	-	6	-	$pA/\sqrt{Hz}$
Input Voltage Noise ($f = 1KHz, R_{SOURCES} = 0\Omega$)	+25°C	-	6	-	-	6	-	-	6	-	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	10K	15K	-	10K	15K	-	7K	10K	-	V/V
	Full	5K	-	-	5K	-	-	5K	-	-	V/V
Common-Mode Rejection Ratio (Note 4)	Full	60	72	-	60	72	-	60	72	-	dB
Minimum Stable Gain	+25°C	10	-	-	10	-	-	10	-	-	V/V
Gain Bandwidth Product (Notes 5 & 6)	+25°C	-	600	-	-	600	-	-	600	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 3, 10)	Full	±10	-	-	±10	-	-	±10	-	-	V
Output Current (Note 3)	+25°C	±10	±20	-	±10	±20	-	±10	±20	-	mA
Output Resistance	+25°C	-	30	-	-	30	-	-	30	-	Ω
Full Power Bandwidth (Notes 3 & 7)	+25°C	8.7	9.5	-	8.7	9.5	-	8.7	9.5	-	MHz
TRANSIENT RESPONSE (Note 8)											
Rise Time	+25°C	-	7	-	-	7	-	-	7	-	ns
Overshoot	+25°C	-	15	-	-	15	-	-	15	-	%
Slew Rate	+25°C	550	600	-	550	600	-	550	600	-	V/µs
Settling Time: 10V Step to 0.1%	+25°C	-	180	-	-	180	-	-	200	-	ns
POWER REQUIREMENTS											
Supply Current	Full	-	20	25	-	20	25	-	20	25	mA
Power Supply Rejection Ratio (Note 9)	Full	60	70	-	60	70	-	60	70	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. This value assumes a no load condition: Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C. By using Application Note 556 on Safe Operating Area equations, along with the packaging thermal resistances listed in the die information section, proper load conditions can be determined. Heat sinking is recommended above +75°C with suggested models:
   Thermalloy #6007 (θ_{SA}=40°C/W) or AAVID #5602B (θ_{SA}=16°C/W).
3. $R_L = 1k\Omega$, $V_O = \pm 10V$
4. VCM = ±10V
5. V_O = 90mV
6. A_V = 10.
7. Full Power Bandwidth guaranteed based on slew rate measurement using FPBW = $\frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of data sheet.
9. V_{SUPPLY} = ±5VDC to ±15VDC
10. Guaranteed range for output voltage is ±10V. Functional operation outside of this range is not guaranteed.

Test Circuits

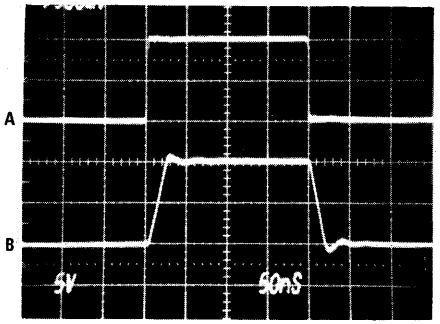
TEST CIRCUIT



V_S = ±15V
A_V = ±10
$C_L \leq$ 10pF

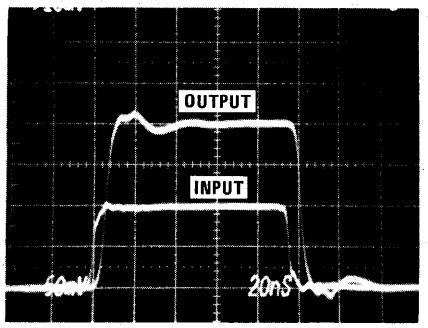
LARGE SIGNAL RESPONSE

Vertical Scale: A = 0.5V/Div., B = 5.0V/Div.
Horizontal Scale: Time: 50ns/Div.

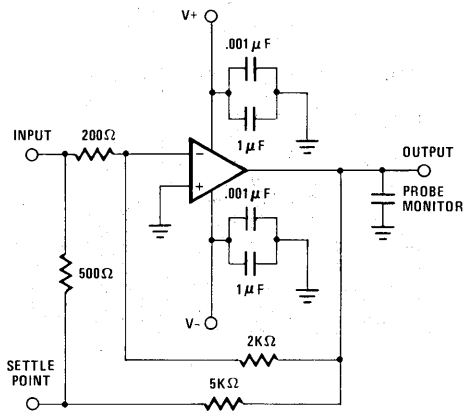


SMALL SIGNAL RESPONSE

Vertical Scale: Input = 10mV/Div., Output = 50mV/Div.
Horizontal Scale: 20ns/Div.



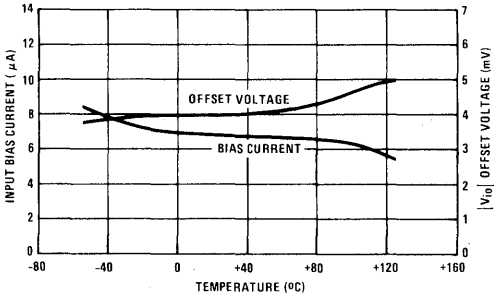
SETTLING TIME TEST CIRCUIT



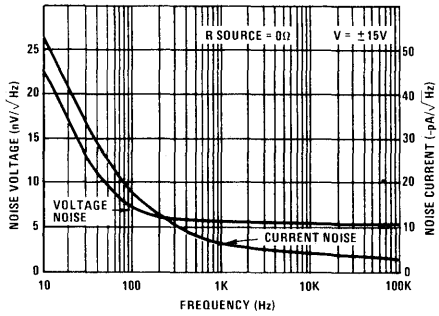
- A_V = -10
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

Typical Performance Curves

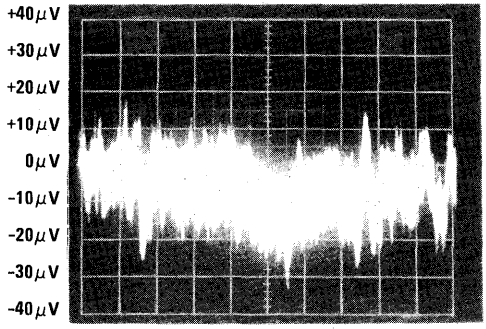
INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE



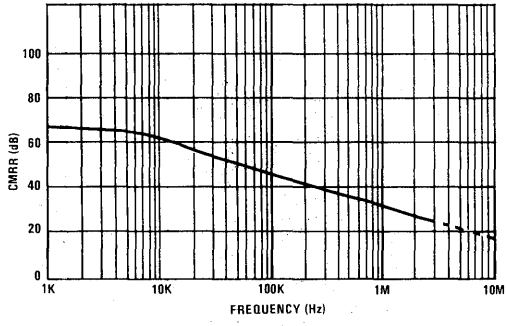
INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



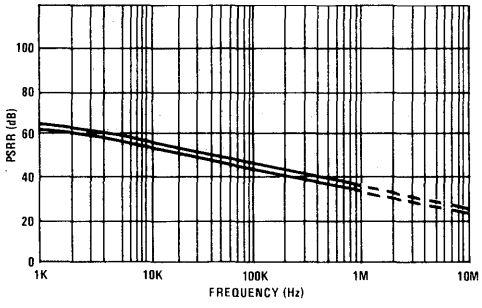
BROADBAND NOISE (0.1Hz to 1MHz)
Vertical Scale: 10μV/Div.
Horizontal Scale: 50ms/Div.



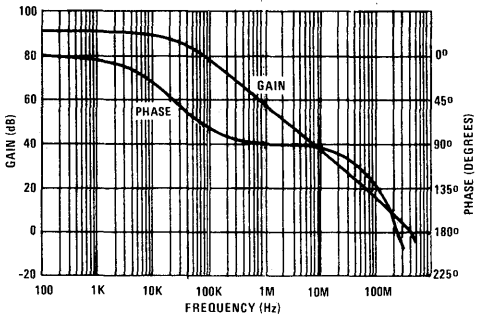
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY

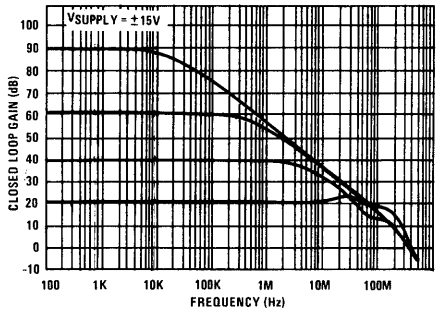


OPEN LOOP GAIN/PHASE vs. FREQUENCY HA-2539

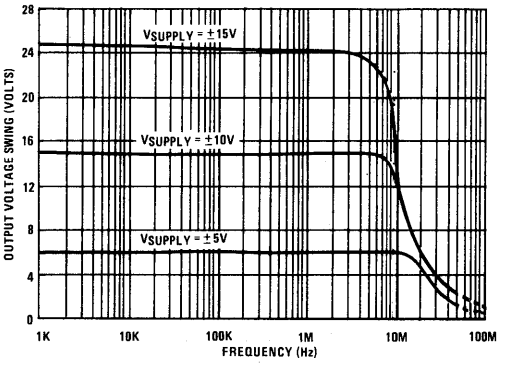


Typical Performance Curves (Continued)

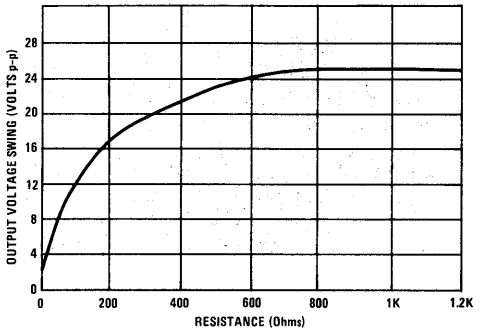
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



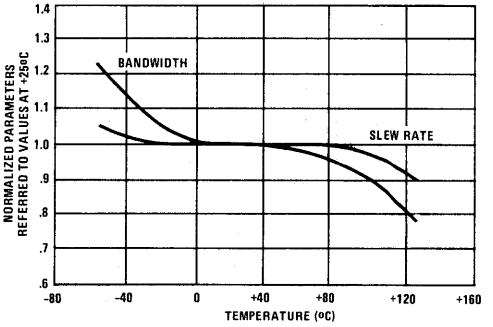
OUTPUT VOLTAGE SWING vs. FREQUENCY



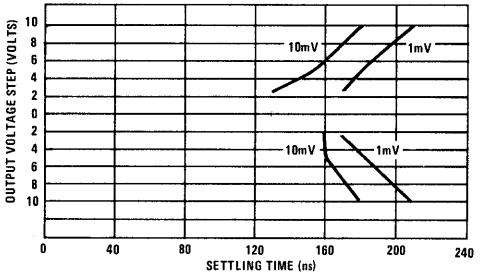
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



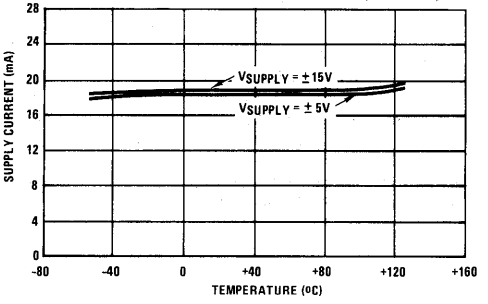
NORMALIZED AC PARAMETERS vs. TEMPERATURE



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



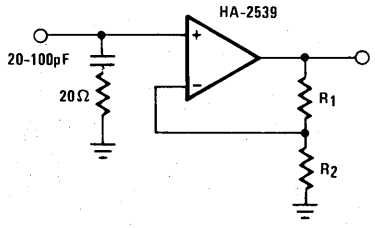
POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE



Applications

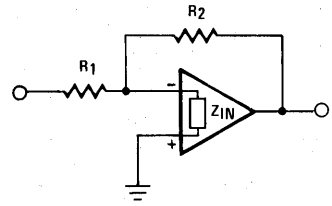
FREQUENCY COMPENSATION
BY OVERDAMPING

Set $A_V = 1 + \frac{R_1}{R_2} = 5$



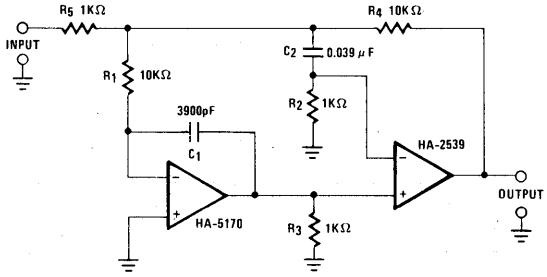
STABILIZATION USING Z_{IN}

Set $A_V = \frac{-R_2}{R_1} = -3$

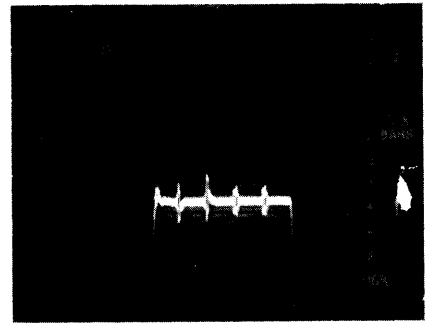


REDUCING DC ERRORS

COMPOSITE AMPLIFIER



DIFFERENTIAL GAIN ERROR (3%)
HA-2539 20dB VIDEO GAIN BLOCK



NOTE: No connect pins (NC) on the HA-2539 should be tied to a ground plane.
Refer to Figure 4 in Application Note 541 for detailed Application suggestions.

Die Characteristics

Transistor Count 30
Die Dimensions ..... 75 x 61 x 19 mils
(1910μm x 1550μm x 483μm)
Substrate Potential (Power Up)* ..... V-
Process ..... High Frequency Bipolar-DI
Passivation ..... Nitride

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA1-2539/2539C Ceramic DIP	104	48
HA3-2539/2539C Plastic DIP	95	46
HA9P2539/2539C SOIC	119	36

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on conductor at V- potential.

HARRIS

HA-2540

Wideband, Fast Settling Operational Amplifier

May 1990

Features

- Very High Slew Rate 400V/µs
- Fast Settling Time 200ns
- Wide Gain-Bandwidth (AV ≤ 10) 400MHz
- Power Bandwidth 6MHz
- Low Offset Voltage 8mV
- Input Voltage Noise ..... 6nV/$\sqrt{Hz}$
- Output Voltage Swing ..... ±10V
- Monolithic Bipolar Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters

Description

The Harris HA-2540 is a wideband, very high slew rate, monolithic operational amplifier featuring superior speed and bandwidth characteristics. Bipolar construction coupled with dielectric isolation allows this truly differential device to deliver outstanding performance in circuits where closed loop gain is 10 or greater. Additionally, the HA-2540 has a drive capability of ±10V into a 1KΩ load. Other desirable characteristics include low input voltage noise, low offset voltage, and fast settling time.

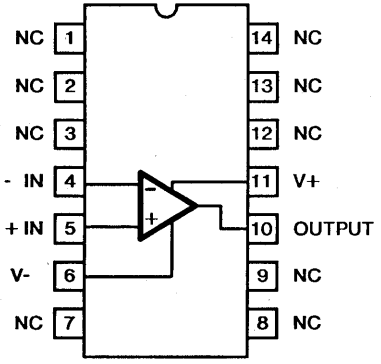
A 400/µs slew rate ensures high performance in video and pulse amplification circuits, while the 400MHz gain-bandwidth-product is ideally suited for wideband signal amplification. A settling time of 200ns also makes the HA-2540 an excellent selection for high speed Data Acquisition Systems.

The HA-2540-2 is specified over the -55°C to +125°C range while the HA-2540-5 is specified from 0°C to +75°C. The HA-2540 is available in the 14 pin Ceramic and Plastic DIP packages. A SOIC packaging option is also available in -5 and -9 temperature grades.

Refer to Application Note 541 and Application Note 556 for more information on High Speed Op-Amp applications. MIL-STD-883 data sheet is available on request.

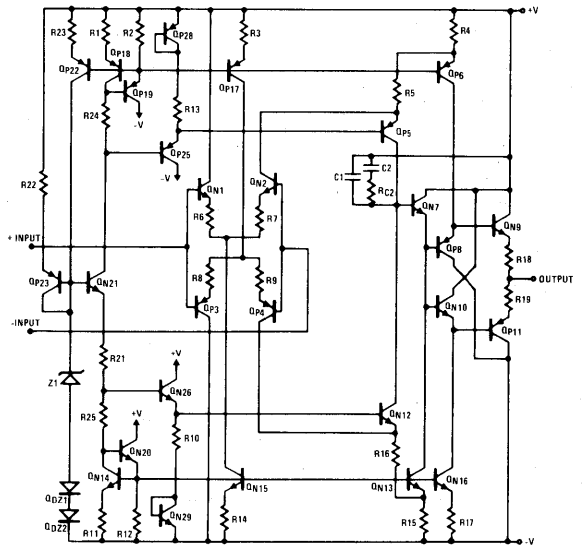
Pinout

HA1-2540/2540C (CERAMIC DIP)
HA3-2540/2540C (PLASTIC DIP)
HA92540/2540C (SOIC)
TOP VIEW



NC No Connection. These pins may be tied to a ground plane for added isolation and heat dissipation

Schematic



Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Voltage ..... ±6V
Output Current ..... 33mArms (Continuous), 50mA (Peak)
Internal Power Dissipation (Note 2) ..... 870mW (Cerdip)

Operating Temperature Ranges

HA-2540-2 ..... $-55^{o}C \leq T_A \leq +125^{o}C$
HA-2540/2540C-5 ..... $0^{o}C \leq T_A \leq +75^{o}C$
HA-2540/2540C-9 ..... $-40^{o}C \leq T_A \leq +85^{o}C$
Storage Temperature Range ..... $-65^{o}C \leq T_A \leq +150^{o}C$
Junction Temperature ..... $+175^{o}C$

Electrical Specifications $V_{SUPPLY} = \pm15V$, $R_L = 1k\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified.

PARAMETER	TEMP	HA-2540-2			HA-2540-5, -9			HA-2540C-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	8	10	-	8	15	-	8	15	mV
	Full	-	13	15	-	13	20	-	13	20	mV
Average Offset Voltage Drift	Full	-	20	-	-	20	-	-	20	-	µV/°C
Bias Current	+25°C	-	5	20	-	5	20	-	5	20	µA
	Full	-	-	25	-	-	25	-	-	25	µA
Offset Current	+25°C	-	1	6	-	1	6	-	1	6	µA
	Full	-	-	8	-	-	8	-	-	8	µA
Input Resistance	+25°C	-	10	-	-	10	-	-	10	-	kΩ
Input Capacitance	+25°C	-	1	-	-	1	-	-	1	-	pF
Common Mode Range	Full	±10	-	-	±10	-	-	±10	-	-	V
Input Noise Current ($f = 1kHz$, $R_{SOURCE} = 0\Omega$)	+25°C	-	6	-	-	6	-	-	6	-	$pA/\sqrt{Hz}$
Input Noise Voltage ($f = 1kHz$, $R_{SOURCES} = 0\Omega$)	+25°C	-	6	-	-	6	-	-	6	-	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	+25°C	10K	15K	-	10K	15K	-	7K	10K	-	V/V
(Note 3)	Full	5K	-	-	5K	-	-	5K	-	-	V/V
Common-Mode Rejection Ratio (Note 4)	Full	60	72	-	60	72	-	60	72	-	dB
Minimum Stable Gain	+25°C	10	-	-	10	-	-	10	-	-	V/V
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C	-	400	-	-	400	-	-	400	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 3, 10)	Full	±10	-	-	±10	-	-	±10	-	-	V
Output Current (Note 3)	+25°C	±10	±20	-	±10	±20	-	±10	±20	-	mA
Output Resistance	+25°C	-	30	-	-	30	-	-	30	-	Ω
Full Power Bandwidth (Notes 3 & 7)	+25°C	5.5	6	-	5.5	6	-	5.5	6	-	MHz
TRANSIENT RESPONSE (Note 8)											
Rise Time	+25°C	-	14	-	-	14	-	-	14	-	ns
Overshoot	+25°C	-	5	-	-	5	-	-	5	-	%
Slew Rate	+25°C	350	400	-	350	400	-	350	400	-	V/µs
Settling Time: 10V Step to 0.1%	+25°C	-	140	-	-	140	-	-	140	-	ns
POWER REQUIREMENTS											
Supply Current	Full	-	20	25	-	20	25	-	20	25	mA
Power Supply Rejection Ratio (Note 9)	Full	60	70	-	60	70	-	60	70	-	dB

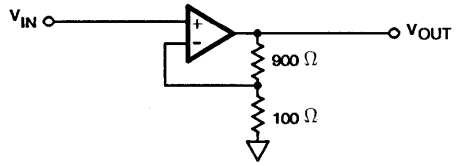
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. This value assumes a no load condition: Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below +175°C. By using Application Note 556 on Safe Operating Area Equations, along with the packaging thermal resistances listed in the Die Information section, proper load conditions can be determined. Heat sinking is recommended above +75°C with suggested models:

   Thermalloy #6007 ($\theta_{SA} \simeq 40^{o}C/W$) or AAVID #5602B ($\theta_{SA} \simeq 16^{o}C/W$).
3. $R_L = 1k\Omega$, $V_O = \pm 10V$.
4. $V_{CM} = \pm 10V$.
5. $V_O = 90mV$.
6. $A_V = 10V$.
7. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of the data sheet.
9. $V_{SUPPLY} = \pm 5VDC$ to $\pm 15VDC$.
10. Guaranteed range for output voltage is ±10V. Functional operation outside of this range is not guaranteed.

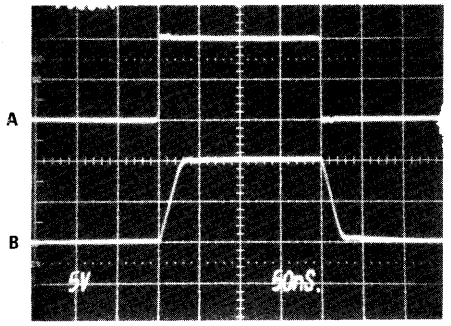
Test Circuits

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

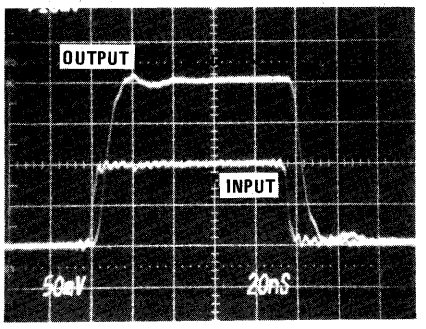


AV = +10
CL ≤ 10pF

LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: A = 0.5V/Div., B = 5.0V/Div.)
Horizontal Scale: (Time: 50ns/Div.)

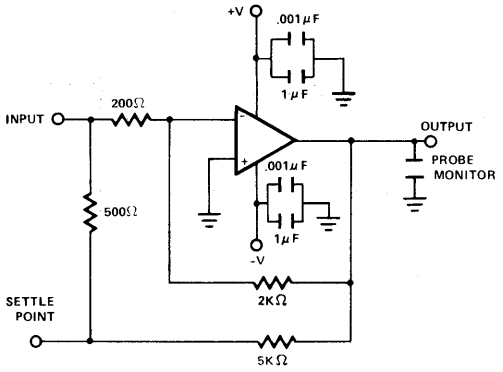


SMALL SIGNAL RESPONSE
Vertical Scale: Input = 10mV/Div.; Output = 50mV/Div.
Horizontal Scale: 20ns/Div.



TURN-ON TIME DELAY TYPICALLY 4ns.

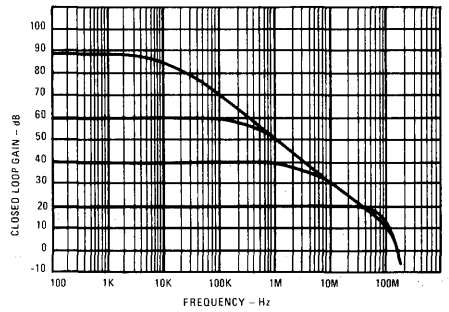
SETTLING TIME TEST CIRCUIT



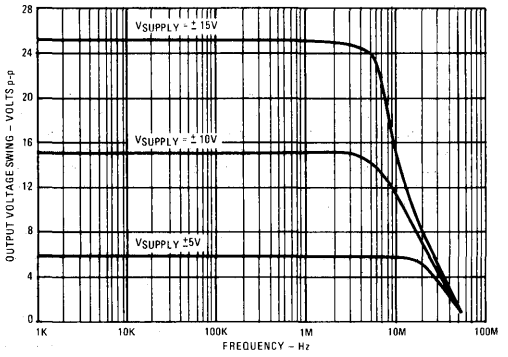
- $A_V = -10$.
- Load Capacitance should be less than 10pF. Turn on time delay typically 4ns.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- SETTLE POINT (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommened that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

Performance Curves

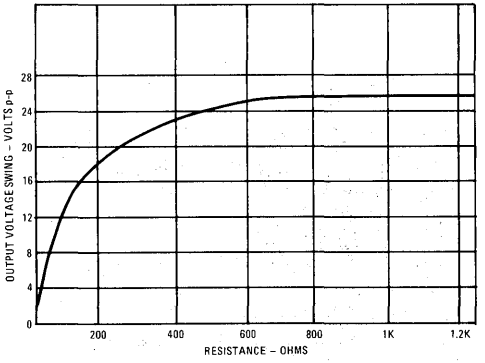
CLOSED LOOP FREQUENCY RESPONSE



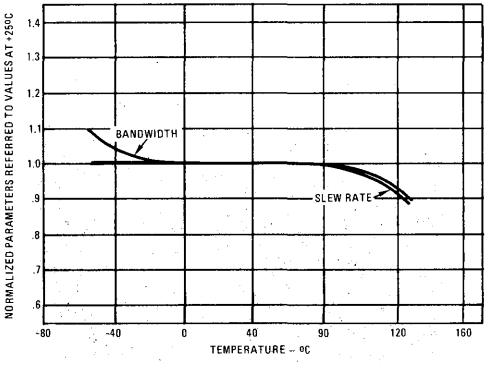
OUTPUT VOLTAGE SWING vs. FREQUENCY



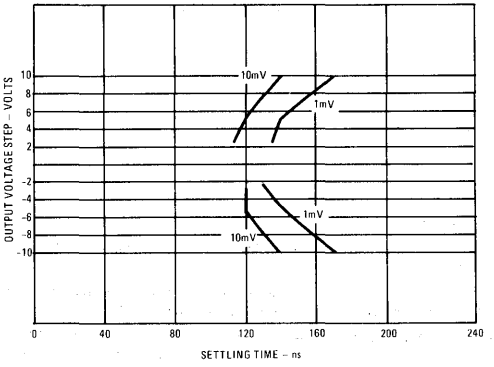
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



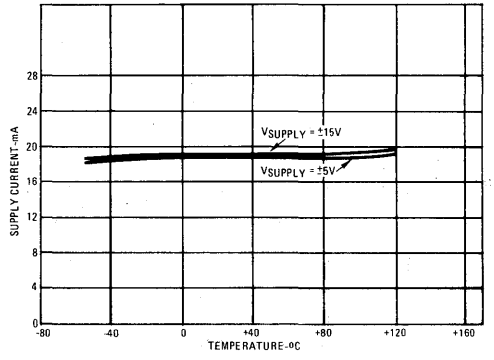
NORMALIZED AC PARAMETERS vs. TEMPERATURE



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

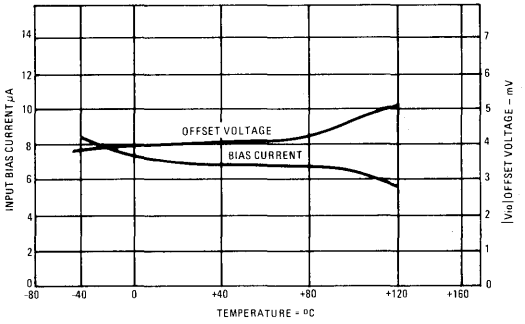


POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE

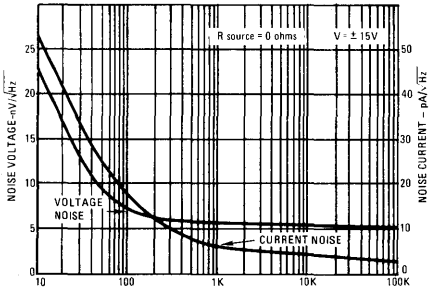


Performance Curves

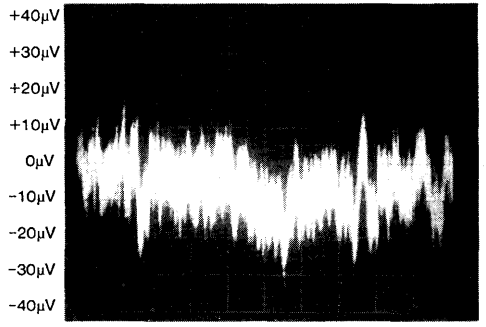
INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE



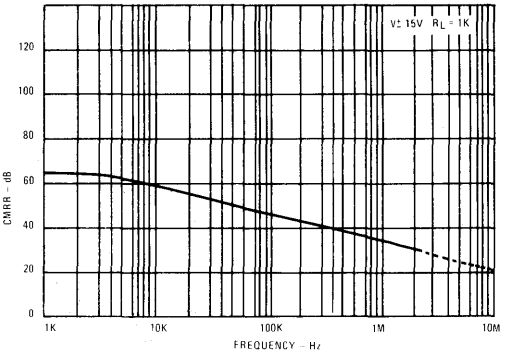
INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



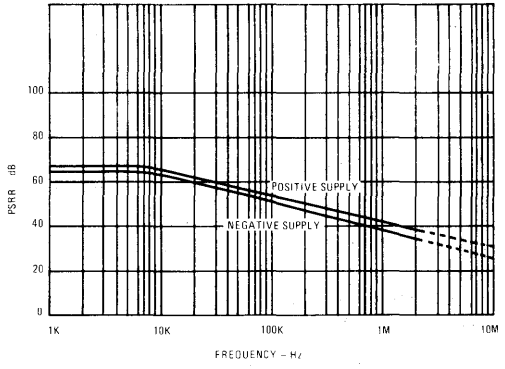
BROADBAND NOISE (0.1HZ to 1MHz)
Vertical Scale: 10mV/Div.
Horizontal Scale: 50ms/Div.



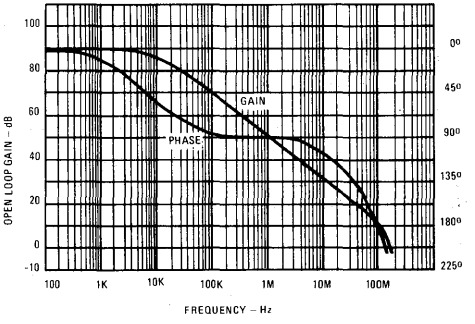
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



OPEN LOOP GAIN/PHASE vs. FREQUENCY HA-2540

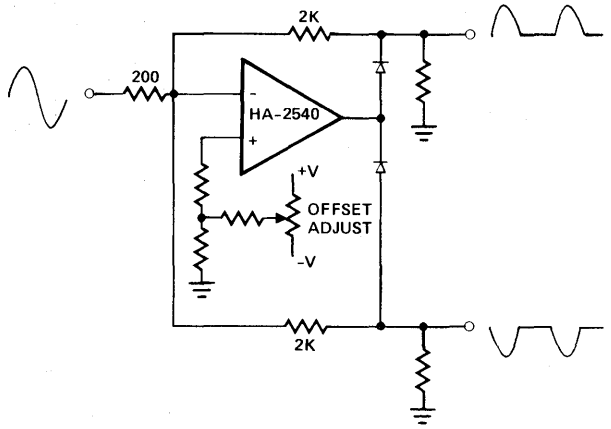


3 OPERATIONAL AMPLIFIERS

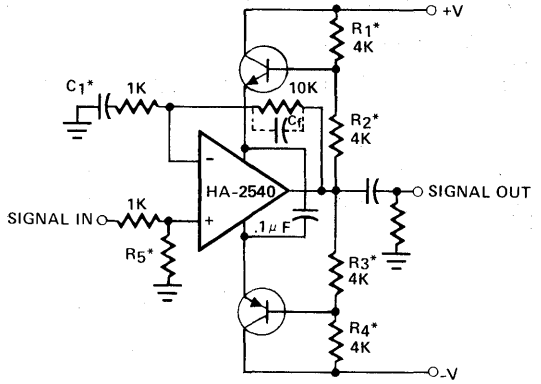
Applications

WIDEBAND SIGNAL SPLITTER

With one HA-2540 and two low capacitance switching diodes, signals exceeding 10MHz can be seperated. This circuit is most useful for full wave rectification, AM detectors or sync generation.



BOOTSTRAPPING FOR MORE OUTPUT CURRENT AND VOLTAGE SWING



NOTES:

1. Used for experimental purposes. Cf ≈ 3pF.
2. C_1 is optional (0.001μF → 0.01μF ceramic)
3. R_5 is optional and can be utilized to reduce input signal amplitude and/or balance input conditions. R_5 = 500Ω to 1kΩ.

Refer to Application Note 541 For Further Applications Information.

Die Characteristics

Transistor Count	30
Die Dimensions	75 x 61 x 19 mils
	(1910μm x 1550μm x 483μm)
Substrate Potential (Power Up)*	V-
Process	High Frequency Bipolar-DI
Passivaton	Nitride

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA-2540/2540C Ceramic DIP	104	48
HA-2540/2540C Plastic DIP	95	46
HA-2540/2540C SOIC	119	36

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential. V- potential.

HARRIS HA-2541

Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier

May 1990

Features

- Unity Gain Bandwidth 40MHz
- High Slew Rate 250V/μs
- Low Offset Voltage 0.8mV
- Fast Settling Time (0.1%) 90ns
- Power Bandwidth 4MHz
- Output Voltage Swing (Min) ..... ±10V
- Unity Gain Stability
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- High Speed Sample-Hold Circuits
- Fast, Precise D/A Converters
- High Speed A/D Input Buffer

Description

The HA-2541 is the first unity gain stable monolithic operational amplifier to achieve 40MHz unity gain bandwidth. A major addition to the Harris series of high speed, wideband op amps, the HA-2541 is designed for video and pulse applications requiring stable amplifier response at low closed loop gains.

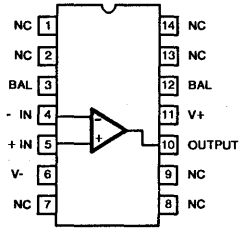
The uniqueness of the HA-2541 is that its slew rate and bandwidth characteristics are specified at unity gain. Historically, high slew rate, wide bandwidth and unity gain stability have been incompatible features for a monolithic operational amplifier. But features such as 250V/μs slew rate and 40MHz unity gain bandwidth clearly show that this is not the case for the HA-2541. These features, along with 90ns settling time to 0.1%, make this product an excellent choice for high speed data acquisition systems.

Packaged in a metal can (TO-8) or 14 pin ceramic DIP, the HA-2541 is pin compatible with the HA-2540 and HA-5190 op amps. The HA-2541-2 is specified over the temperature range of -55°C to +125°C. The HA-2541-5 is specified over the temperature range of 0°C to +75°C. For the military grade product, refer to the HA-2541 military data sheet.

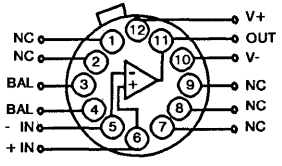
For further application suggestions on the HA-2541, please refer to Applicaton Note 550 (Using the HA-2541), and Application Note 556 (Thermal Safe-Operating-Areas For High Current Operational Amplifiers). Also see 'Applications' in this data sheet.

Pinouts

HA1-2541 CERAMIC DIP
TOP VIEW

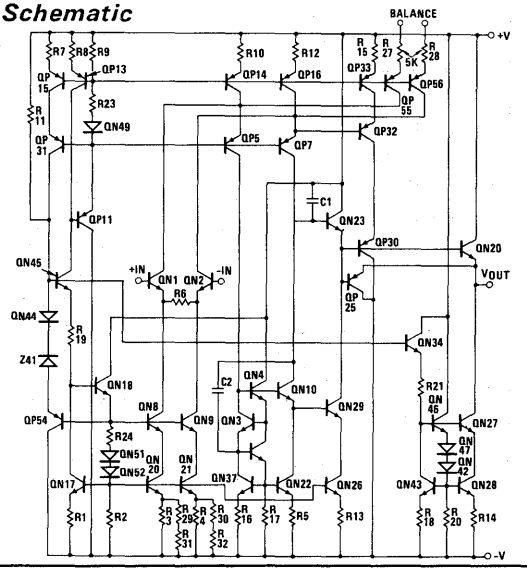


HA2-2541 METAL CAN (TO-8)
TOP VIEW



VCASE = V-

Schematic



CAUTION: These devices are sensitive to electrostic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between Vz and V- 35V
Differential Input Voltage ..... ±6V
Peak Output Current 50mA
Continuous Output Current 28mArms

Operating Temperature Range:

HA-2541-2 ..... $-55^{o}C \leq T_A \leq +125^{o}C$
HA-2541-5 ..... $0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range ..... $-65^{o}C \leq T_A \leq +150^{o}C$
Maximum Junction Temperature (Note 11) ..... $+175^{o}C$

Electrical Specifications V_{SUPPLY} = ±15 Volts; R_L = 1kΩ, $C_L \leq$ 10pF, Unless Otherwise Specified

PARAMETER	TEMP	HA-2541-2 -55°C to +125°C MIN	TYP	MAX	HA-2541-5 0°C to +75°C MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	0.8	2	-	1	2	mV
	Full	-	-	6	-	-	6	mV
Average Offset Voltage Drift	Full	-	9	-	-	9	-	µV/°C
Bias Current	+25°C	-	11	35	-	11	35	µA
	Full	-	-	50	-	-	50	µA
Average Bias Current Drift	Full	-	85	-	-	85	-	nA/°C
Offset Current	+25°C	-	1	7	-	1	7	µA
	Full	-	-	9	-	-	9	µA
Input Resistance	+25°C	-	100	-	-	100	-	kΩ
Input Capacitance	+25°C	-	1	-	-	1	-	pF
Common Mode Range	Full	±10	±11	-	±10	±11	-	V
Input Noise Voltage (f = 1kHz, $R_g = 0\Omega$)	+25°C	-	10	-	-	10	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz, $R_g = 0\Omega$)	+25°C	-	4	-	-	4	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	10k	16k	-	10k	16k	-	V/V
	Full	5k	-	-	5k	-	-	V/V
Common-Mode Rejection Ratio (Note 5)	Full	70	90	-	70	90	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	V/V
Unity Gain-Bandwidth (Note 6)	+25°C	-	40	-	-	40	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 4)	Full	±10	±11	-	±10	±11	-	V
Output Current (Note 4)	+25°C	±10	±15	-	±10	±15	-	mA
Output Resistance	+25°C	-	2	-	-	2	-	Ω
Full Power Bandwidth (Note 3 & 7)	+25°C	3	4	-	3	4	-	MHz
Differential Gain (Note 2)	+25°C	-	0.1	-	-	0.1	-	%
Differential Phase (Note 2)	+25°C	-	0.2	-	-	0.2	-	Degree
Harmonic Distortion (Note 10)	+25°C	-	<0.01	-	-	<0.01	-	%
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C	-	4	-	-	4	-	ns
Overshoot	+25°C	-	40	-	-	40	-	%
Slew Rate	+25°C	200	250	-	200	250	-	V/µs
Settling Time: 10V Step to 0.1%	+25°C	-	90	-	-	90	-	ns
10V Step to 0.01%	+25°C	-	175	-	-	175	-	ns
POWER REQUIREMENTS								
Supply Current	+25°C	-	29	-	-	29	-	mA
	Full	-	-	40	-	-	40	mA
Power Supply Rejection Ratio (Note 9)	Full	70	80	-	70	78	-	dB

NOTES:

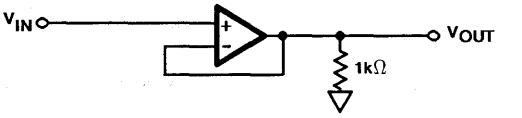
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Differential Gain and Phase are measured with a 1 Volt differential voltage at 5MHz.
3. $V_O = \pm 10V$
4. $R_L = 1k\Omega$
5. $V_{CM} = \pm 10V$
6. $V_O = 90mV$.
7. Full Power Bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of this data sheet.
9. $V_{SUPPLY} = \pm 5VDC$ to $\pm 15VDC$
10. $V_{IN} = 1V_{RMS}$; f = 10kHz; $A_V = 10$
11. This value assumes a no load condition:Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below $+175^oC$. By using Application Note 556 on Safe operating Area equations, along with the packaging thermal resistances listed in the Die Characteristics section, proper load conditions can be determined. Heat sinking is recommended above $+75^oC$ with suggested models:

    14 Lead Ceramic DIP:
    Thermalloy #6007 or AAVID #5602B ($\theta_{sa} = 16^oC/W$).

    12 Lead Metal Can (TO-8):
    Thermalloy #2240A ($\theta_{sa} = 27^oC/W$) or #2268B ($\theta_{sa} = 24^oC/W$)

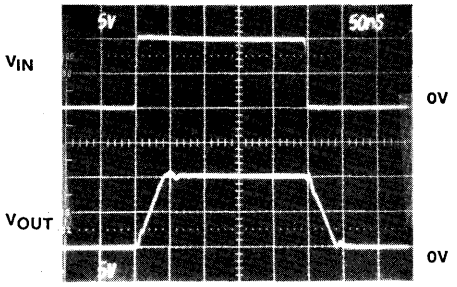
Test Circuits

TEST CIRCUIT

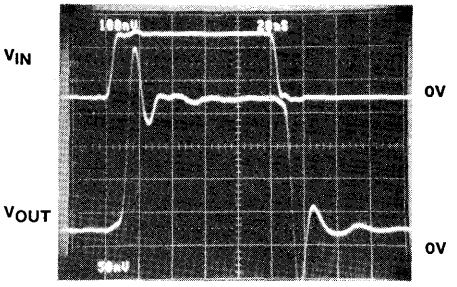


$V_S = \pm 15V$
$A_V = +1$
$C_L \leq 10pF$

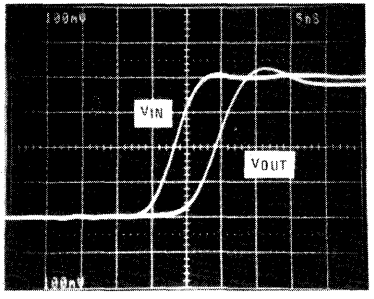
LARGE SIGNAL RESPONSE
Vertical Scale (Volts: 5V/Div.)
Horizontal Scale (Time: 50ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale (Volts: 100mV/Div.)
Horizontal Scale (Time: 50ns/Div.)



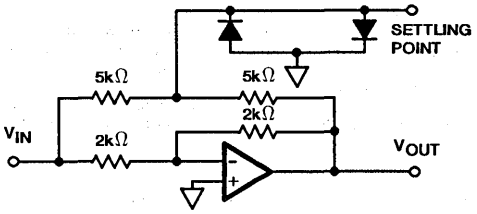
PROPAGATION DELAY
Vertical Scale (Volts: 100mV/Div.)
Horizontal Scale (Time: 5ns/Div.)



$V_S = \pm 15V$, $R_L = 1k\Omega$
$T = +25^oC$
Propagation delay variance is negligible over full temperature range.

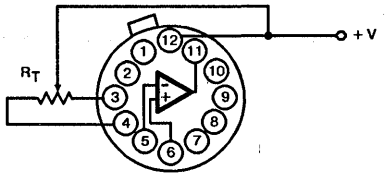
Test Circuits (Continued)

SETTLING TIME TEST CIRCUIT



- $A_V = -1$
- Feedback and Summing Resistors Must Be Matched (0.1%)
- HP5082-2810 Clipping Diodes Recommended
- Tektronix P6201 FET Probe Used At Settling Point.

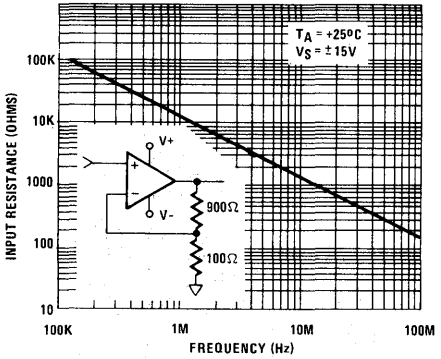
Suggested Offset Voltage Adjustment



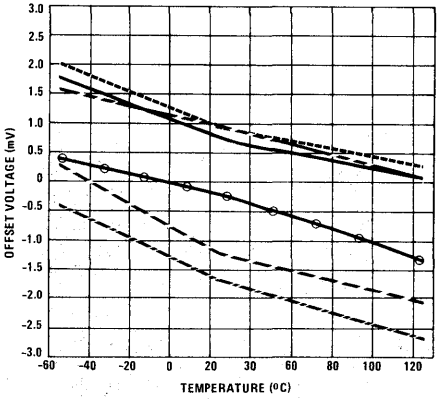
Tested Offset Adjustment Range is $|V_{OS}| = 1mV|$ minimum referred to output. Typical range is ±15mV for $R_T = 5k\Omega$

Typical Performance Curves

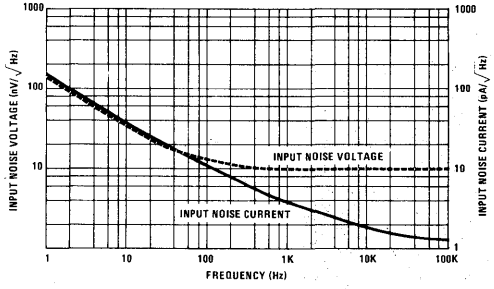
INPUT RESISTANCE vs. FREQUENCY



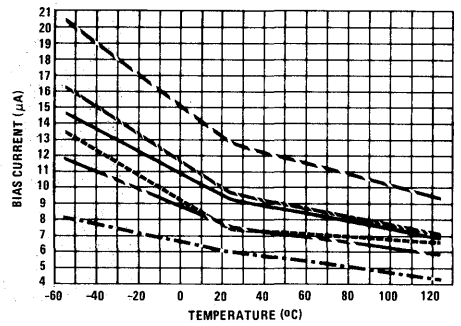
OFFSET VOLTAGE DRIFT WITH TEMPERATURE
Of 6 Representative Units



NOISE DENSITY vs. FREQUENCY
$T_A = +25°C$

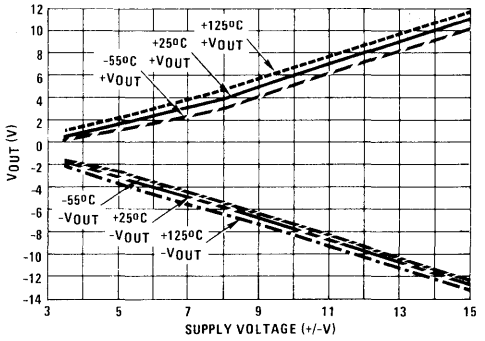


BIAS CURRENT DRIFT WITH TEMPERATURE
Of 6 Representative Units

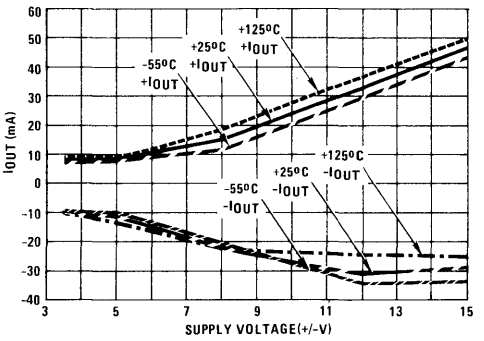


Typical Performance Curves (Continued)

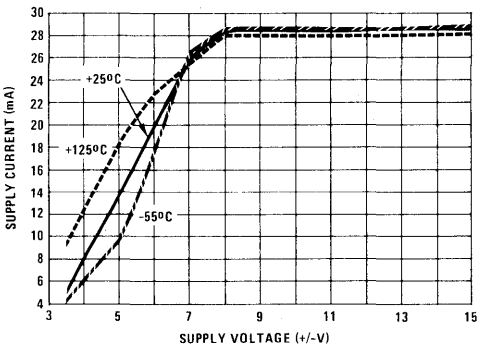
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
At Various Temperatures



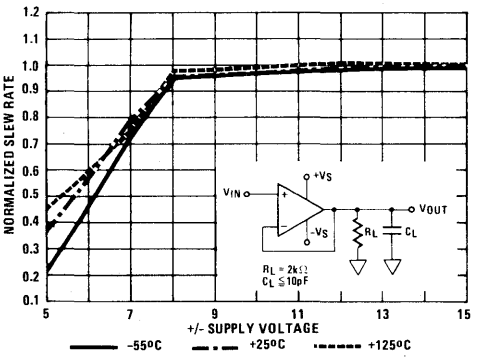
OUTPUT CURRENT vs. SUPPLY VOLTAGE
At Various Temperatures



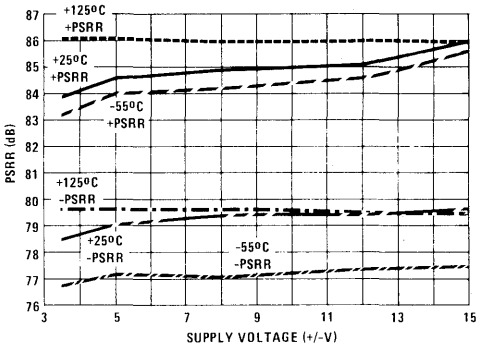
SUPPLY CURRENT vs. SUPPLY VOLTAGE
At Various Temperatures



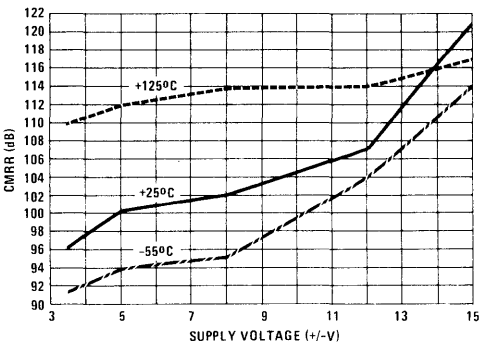
SLEW RATE vs. SUPPLY VOLTAGE
Normalized With V_S = ±15V at +25°C



PSRR vs. SUPPLY VOLTAGE
Average of 3 Lots At Various Temperatures

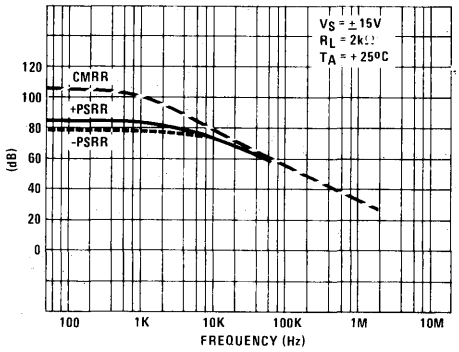


CMRR vs. SUPPLY VOLTAGE
Average of 3 Lots At Various Temperatures

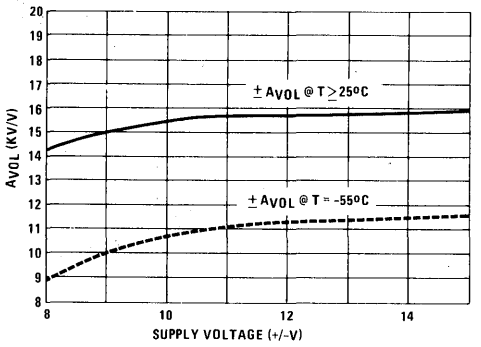


Typical Performance Curves (Continued)

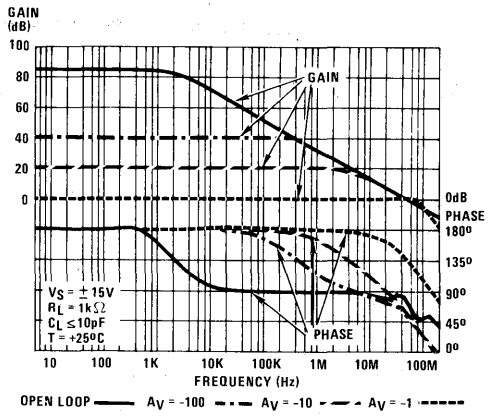
REJECTION RATIOS vs. FREQUENCY



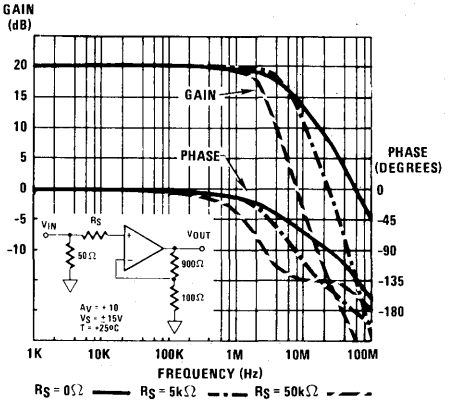
+/- OPEN LOOP GAIN vs. SUPPLY VOLTAGE
Average of 3 Lots Over Temperature



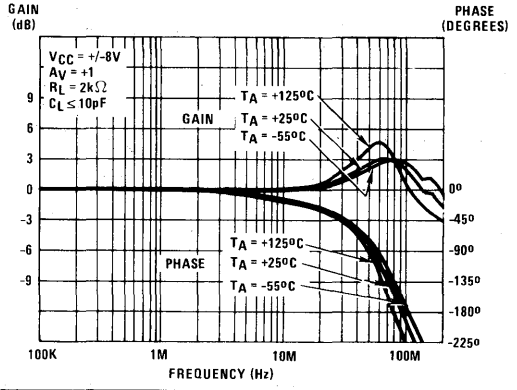
GAIN AND PHASE FREQUENCY RESPONSE
$V_S = \pm 15V$, $R_L = 1k$, $C_L \leq 10pF$, $T_A = +25^oC$



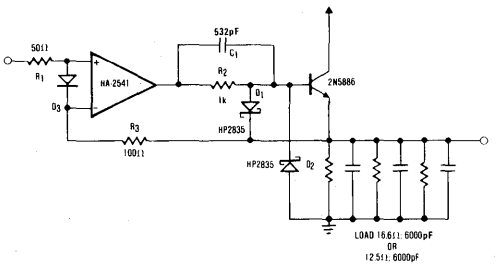
SMALL SIGNAL BANDWIDTH vs. SOURCE RESISTANCE
$V_S = \pm 15V$, $R_L = 1k\Omega$



CLOSE LOOP FREQUENCY RESPONSE vs. TEMPERATURE



Applications (Also See Application Note 550)



APPLICATION 1. DRIVING POWER TRANSISTORS TO GAIN ADDITIONAL CURRENT BOOSTING

APPLICATION 1

High power amplifiers and buffers are in use in a wide variety of applications. Many times the "high power" capability is needed to drive large capacitive loads as well as low value resistive loads. In both cases the final driver stage is usually a power transistor of some type, but because of their inherently low gain, several stages of pre-drivers are often required. The HA-2541, with its 10mA output rating, is powerful enough to drive a power transistor without additional stages of current amplification. This capability is well demonstrated with the high power buffer circuit in Application 1.

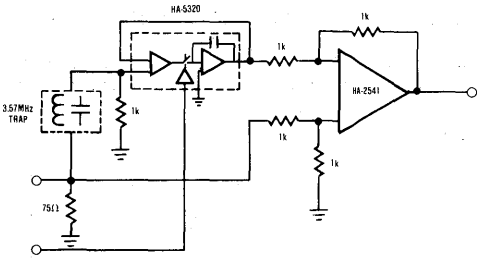
The HA-2541 acts as the pre-driver to the output power transistor. Together, they form a unity gain buffer with the ability to drive three 50 ohm coaxial cables in parallel, each with a capacitance of 2000pF. The total combined load is 16.6 ohms and 6000pF capacitance.

APPLICATION 2

Video

One of the primary uses of the HA-2541 is in the area of video applications. These applications include signal construction, synchronization addition and removal, as well as signal modification. A wide bandwidth device such as the HA-2541 is well suited for use in this class of amplifier. This, however, is a more involved group of applications than ordinary amplifier applications since video signals contain precise DC levels which must be retained.

The addition of a clamping circuit restores D.C. levels at the output of an amplifier stage. The circuit shown in Application 2 utilizes the HA-5320 sample and hold amplifier as the D.C. clamp. Also shown is a 3.57MHz trap in series, which will block the color burst portion of the video signal and allow the D.C. level to be amplified and restored.



APPLICATION 2. VIDEO D.C. RESTORER

Die Characteristics

Transistor Count 41
Die Dimensions ..... 89 x 79 x 19 mils
(2250µm x 1990µm x 485µm)
Substrate Potential (Power Up)* ..... V-
Process ..... High Frequency Bipolar
Dielectric Isolation
Passivation ..... Silox

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	91	35
Metal Can	66	30

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS

HA-2542

Wideband, High Slew Rate, High Output Current Operational Amplifier

May 1990

Features

- Stable at Gains of 2 or Greater
- Gain Bandwidth 70MHz
- High Slew Rate (Min.) 300V/μs
- High Output Current (Min.) 100mA
- Power Bandwidth (Typ.) 5.5MHz
- Output Voltage Swing (Min.) ..... ±10V
- Monolithic Bipolar Dielectric Isolation Construction

Applications

- Pulse and Video Amplifiers
- Wideband Amplifiers
- Coaxial Cable Drivers
- Fast Sample-Hold Circuits
- High Frequency Signal Conditioning Circuits

Description

The HA-2542 is a wideband, high slew rate, monolithic operational amplifier featuring an outstanding combination of speed, bandwidth, and output drive capability.

Utilizing the advantages of the Harris D. I. technology this amplifier offers 350V/μs slew rate, 70MHz gain bandwidth, and ±100mA output current. Application of this device is further enhanced through stable operation down to closed loop gains of 2.

For additional flexibility, offset null and frequency compensation controls are included in the HA-2542 pinout.

The capabilities of the HA-2542 are ideally suited for high speed coaxial cable driver circuits where low gain and high output drive requirements are necessary. With 5.5MHz full power bandwidth, this amplifier is most suitable for high frequency signal conditioning circuits and pulse video amplifiers. Other applications utilizing the HA-2542 advantages include wideband amplifiers and fast sample-hold circuits.

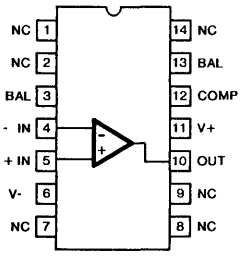
The HA-2542 is available in ceramic or plastic 14 lead DIP packages, or a 12 lead metal can (TO-8) which is pin compatible with the HA-2541, HA-5190, LH0032 and HOS-050C. The HA-2542-2 is specified over the -55°C to +125°C temperature range and is also offered as a military part. The HA-2542-5 is specified over the commercial temperature range of 0°C to +75°C.

For more information on the HA-2542, please refer to Application Note 552 (Using The HA-2542), or Application Note 556 (Thermal Safe-Operating-Areas For High Current Op Amps).

Pinouts

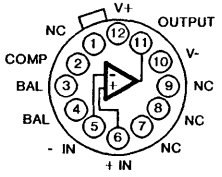
HA1-2542 (CERAMIC DIP), HA3-2542 (PLASTIC DIP)

TOP VIEW

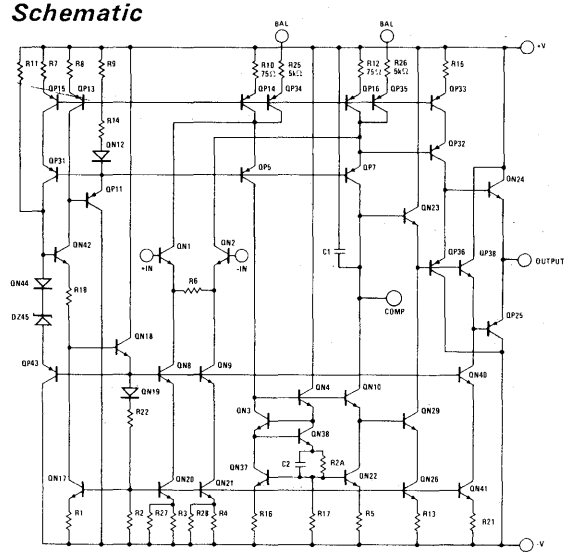


HA2-2542 (TO-8 METAL CAN)

TOP VIEW



Schematic



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage between V+ and V- Terminals 35V
Differential Input Voltage ..... ±6V
Output Current ..... 125mA (Peak)
107mA rms (Continuous)

Operating Temperature Range

HA-2542-2 ..... $-55^{o}C \leq T_A \leq +125^{o}C$
HA-2542-5 ..... $0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range ..... $-65^{o}C \leq T_A \leq +150^{o}C$
Maximum Junction Temperature (Note 11) ..... $+175^{o}C$

Electrical Specifications V_{SUPPLY} = ±15 Volts; R_L = 1kΩ, $C_L \leq$ 10pF, Unless Otherwise Specified.

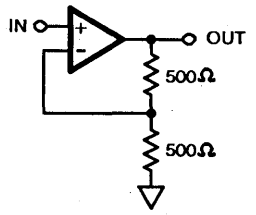
PARAMETER	TEMP	HA-2542-2 -55°C to +125°C MIN	TYP	MAX	HA-2542-5 0°C to +75°C MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	5	10	-	5	10	mV
	Full	-	8	20	-	8	20	mV
Average Offset Voltage Drift	Full	-	14	-	-	14	-	µV/°C
Bias Current	+25°C	-	15	35	-	15	35	µA
	Full	-	26	50	-	26	50	µA
Average Bias Current Drift	Full	-	66	-	-	45	-	nA/°C
Offset Current	+25°C	-	1	7	-	1	7	µA
	Full	-	-	9	-	-	9	µA
Input Resistance	+25°C	-	100	-	-	100	-	kΩ
Input Capacitance	+25°C	-	1	-	-	1	-	pF
Common Mode Range	Full	±10	-	-	±10	-	-	V
Input Noise Voltage (0.1Hz to 100Hz)	+25°C	-	2.2	-	-	2.2	-	µVp-p
Input Noise Voltage Density (fo = 1kHz, R_g = 0Ω)	+25°C	-	10	-	-	10	-	$nV/\sqrt{Hz}$
Input Noise Current Density (fo = 1kHz, R_g = 0Ω)	+25°C	-	3	-	-	3	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3)	+25°C	10k	30k	-	10k	30k	-	V/V
	Full	5k	15k	-	5k	20k	-	V/V
Common-Mode Rejection Ratio (Note 4)	Full	70	100	-	70	100	-	dB
Minimum Stable Gain	+25°C	2	-	-	2	-	-	V/V
Gain-Bandwidth-Product (Note 5)	+25°C	-	70	-	-	70	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	Full	±10	±11	-	±10	±11	-	V
Output Current (Note 6)	+25°C	100	-	-	100	-	-	mA
Output Resistance	+25°C	-	5	-	-	5	-	Ω
Full Power Bandwidth (Note 3 & 7)	+25°C	4.7	5.5	-	4.7	5.5	-	MHz
Differential Gain (Note 2)	+25°C	-	0.1	-	-	0.1	-	%
Differential Phase (Note 2)	+25°C	-	0.2	-	-	0.2	-	Degrees
Harmonic Distortion (Note 10)	+25°C	-	<0.04	-	-	<0.04	-	%
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C	-	4	-	-	4	-	ns
Overshoot	+25°C	-	25	-	-	25	-	%
Slew Rate	+25°C	300	350	-	300	350	-	V/µs
Settling Time: 1V Step to 0.1%	+25°C	-	100	-	-	100	-	ns
10V Step to 0.01%	+25°C	-	200	-	-	200	-	ns
POWER REQUIREMENTS								
Supply Current	+25°C	-	30	-	-	30	-	mA
	Full	-	31	34.5	-	31	40	mA
Power Supply Rejection Ratio (Note 9)	Full	70	79	-	70	79	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Differential gain and phase are measured at 5MHz with a 1 Volt differential input voltage.
3. $R_L = 1k\Omega$, $V_O = \pm 10V$
4. $V_{CM} = \pm 10V$
5. $A_{VCL} = 100$
6. $R_L = 50\Omega$, $V_O = \pm 5V$
7. Full Power Bandwidth guaranteed based on slew rate measurement using FPBW = $\frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of this data sheet.
9. $V_{SUPPLY} = \pm 5VDC$ to $\pm 15VDC$
10. $V_{IN} = 1V_{RMS}$; f = 10kHz; $A_V = 10$.
11. This value assumes a no load condition: Maximum power dissipation with load conditions must be designed to maintain the maximum junction temperature below $+175^oC$. By using Application Note 556 on Safe Operating Area equations, along with the packaging thermal resistances listed in the Die Characteristics section, proper load conditions can be determined. Heat sinking is recommended above $+75^oC$ with suggested models:
    14 Lead Ceramic DIP:
    Thermalloy #6007 or AAVID #5602B ($\theta_{sa} = 16^oC/W$).
    12 Lead Metal Can (TO-8):
    Thermalloy #2240A ($\theta_{sa} = 27^oC/W$) or #2268B ($\theta_{sa} = 24^oC/W$)

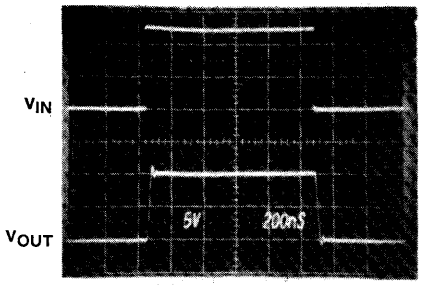
Test Circuits

TEST CIRCUIT

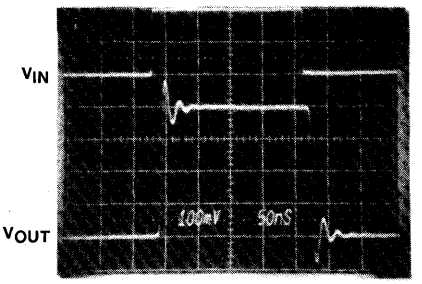


$V_S = \pm 15V$
$A_V = +2$
$C_L \leq 10pF$

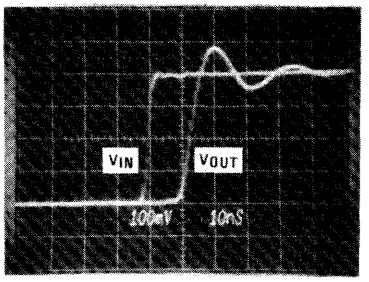
LARGE SIGNAL RESPONSE
Vertical Scale (Volts: V_{IN} = 2.0V/Div., V_{OUT} = 5.0V/Div.)
Horizontal Scale (Time: 200ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale (Volts: 100mV/Div.)
Horizontal Scale (Time: 50ns/Div.)



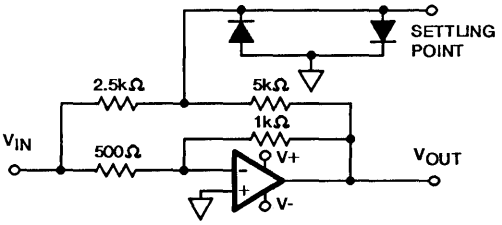
TIME DELAY
Vertical Scale (Volts: 100mV/Div.)
Horizontal Scale (Time: 10ns/Div.)



$V_S = \pm 15V$, $R_L = 1k\Omega$
$T = +25^oC$
Propagation delay variance is negligible over full temperature range.

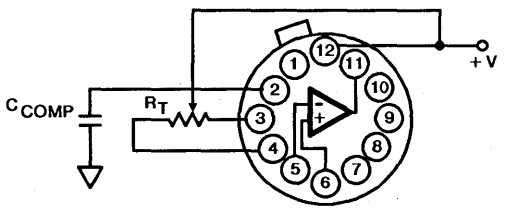
Test Circuits (Continued)

SETTLING TIME TEST CIRCUIT



- $A_V = -2$
- Feedback and summing resistors must be matched (0.1%)
- HP5082-2810 clipping diodes recommended
- Tektronix P6201 FET probe used at settling point
- For 0.01% settliing time, heat sinking is suggested to reduce thermal effects and an analog ground plane with supply decoupling is suggested to minimize ground loop errors.

SUGGESTED OFFSET VOLTAGE ADJUSTMENT

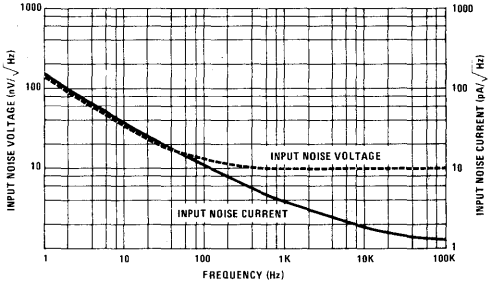


Suggested compensation scheme 5-20pF

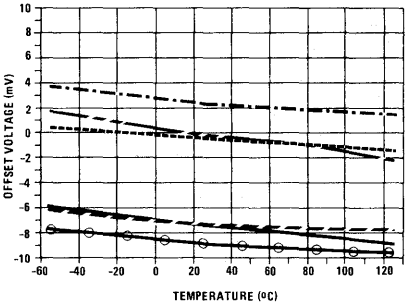
Tested Offset Adjustment Range is $|V_{OS}| + 1mV|$ minimum referred to output. Typical range is +20mV with $R_T = 5k\Omega$.

Typical Performance Curves

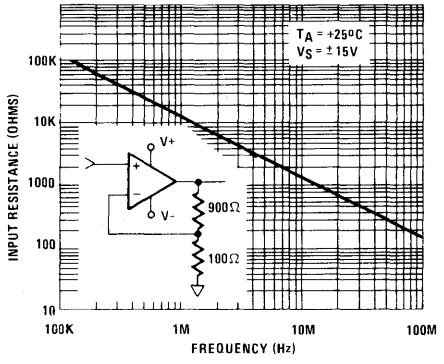
INPUT NOISE VOLTAGE AND INPUT NOISE CURRENT vs. FREQUENCY



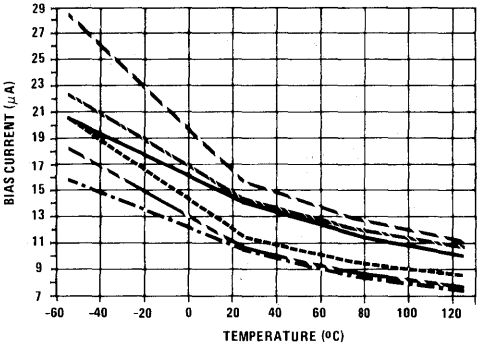
OFFSET VOLTAGE DRIFT WITH TEMPERATURE
Of Six Representative Units, $V_S = \pm 12V$



INPUT RESISTANCE vs. FREQUENCY

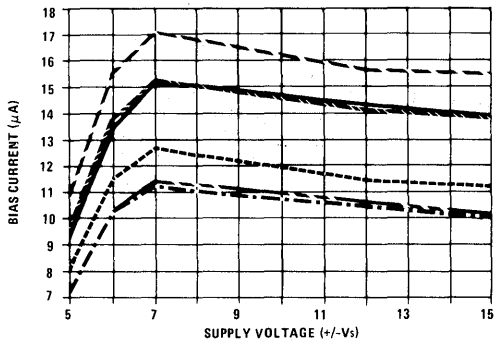


BIAS CURRENT DRIFT WITH TEMPERATURE
Of Six Representative Units, $V_S = \pm 12V$

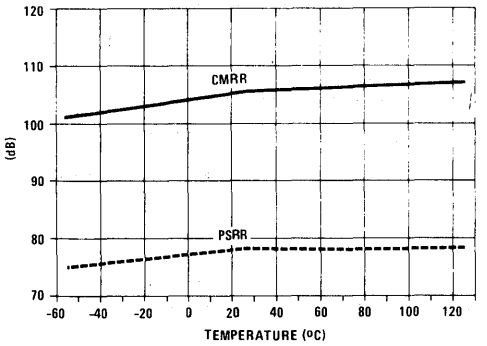


Typical Performance Curves (Continued)

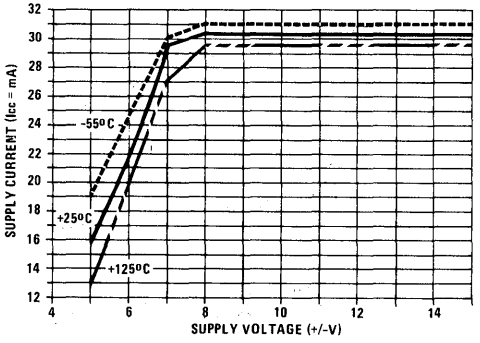
BIAS CURRENT vs. POWER SUPPLY
Six Units At Various Supplies At +25°C



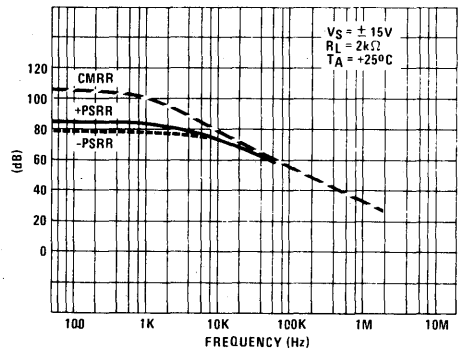
PSRR AND CMRR vs. TEMPERATURE
$V_S = \pm 15V$



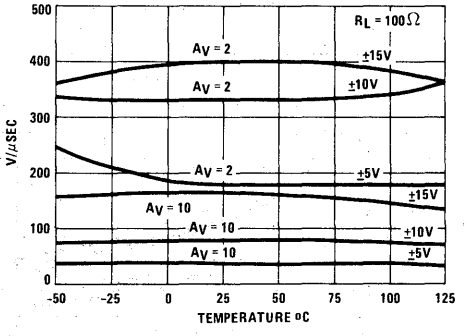
SUPPLY CURRENT vs. SUPPLY VOLTAGE
At Various Temperatures



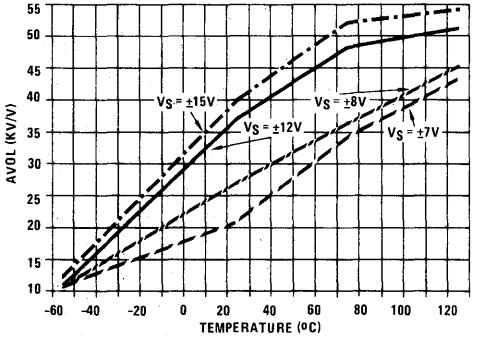
PSRR AND CMRR vs. FREQUENCY



SLEW RATE vs. TEMPERATURE
At Various Supply Voltages With $R_{Load} = 100\Omega$

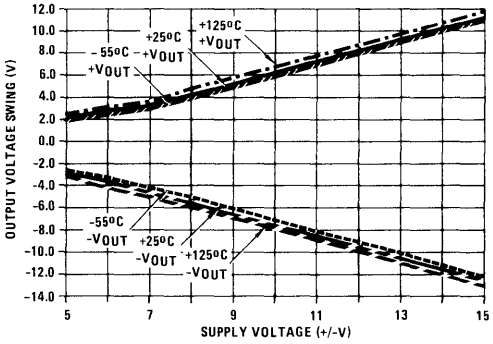


OPEN LOOP GAIN vs. TEMPERATURE
At Various Supply Voltages

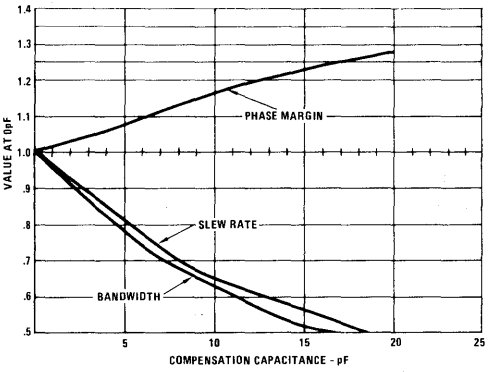


Typical Performance Curves (Continued)

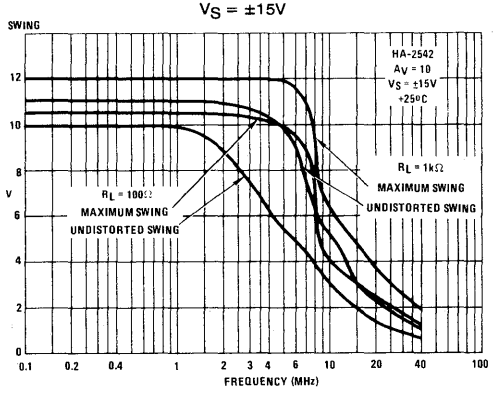
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
At Various Temperatures



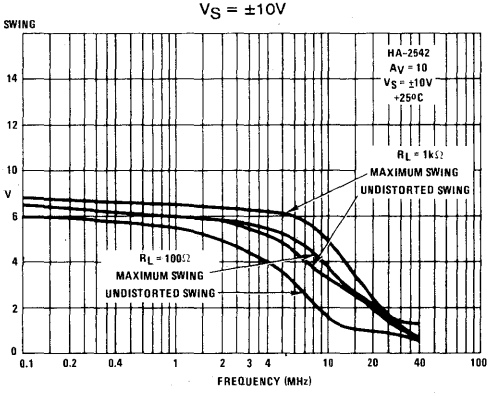
NORMALIZED AC PARAMETERS vs. COMPENSATION CAPACITANCE



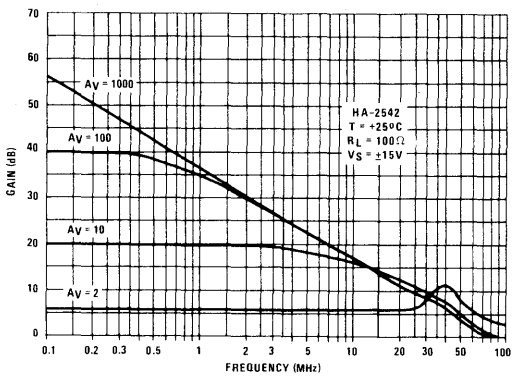
OUTPUT VOLTAGE SWING vs. FREQUENCY
$V_S = \pm 15V$



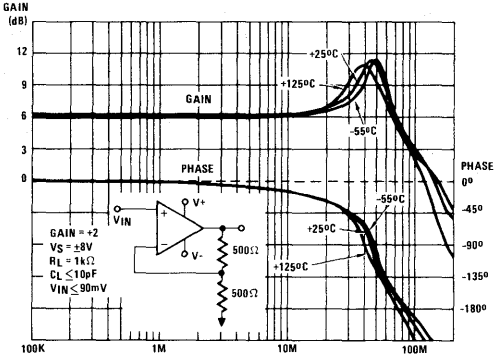
OUTPUT VOLTAGE SWING vs. FREQUENCY
$V_S = \pm 10V$



FREQUENCY RESPONSE CURVES



HA-2542 CLOSED LOOP GAIN vs. TEMPERATURE



Die Characteristics

Transistor Count 43
Die Dimensions ..... 72 x 105 x 19 mils
(1820µm x 2670µm x 485µm)
Substrate Potential* ..... V-
Process ..... High Frequency Bipolar-DI
Passivation ..... Nitride

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA1-2542 Ceramic DIP	86.6	32.5
HA3-2542 Plastic DIP	78.8	30.6
HA2-2542 Metal Can	58	29

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Typical Applications

(Refer to Application Note 552 for Further Information)

The Harris HA-2542 is a state of the art monolithic device which also approaches the "ALL-IN-ONE" amplifier concept. This device features an outstanding set of AC parameters augmented by excellent output drive capability providing for suitable application in both high speed and high output drive circuits.

Primarily intended to be used in balanced 50Ω and 75Ω coaxial cable systems as a driver, the HA-2542 could also be used as a power booster in audio systems as well as a power amp in power supply circuits. This device would also be suitable as a small DC motor driver.

The applications shown on the following page demonstrate the HA-2542 at gains of +100 and +2 and as a video cable driver for small signals.

Prototyping Guidelines

For best overall performance in any application, it is recommended that high frequency layout techniques be used. This should include: 1) mounting the device through a ground plane: 2) connecting unused pins (N.C.) to the ground plane: 3) mounting feedback components on Teflon standoffs and or locating these components as close to the device as possible; 4) placing power supply decoupling capacitors from device supply pins to ground.

As a result of speed and bandwidth optimization, the HA-2542 can's case potential, when powered-up, is equal to the V- potential. Therefore, contact with other circuitry or ground should be avoided.

Frequency Compensation

The HA-2542 may be externally compensated with a single capacitor to ground. This provides the user the additional flexibility in tailoring the frequency response of the amplifier. A guideline to the response is demonstrated on the typical performance curve showing the normalized A.C. parameters versus compensation capacitance. It is suggested that the user check and tailor the accurate compensation value for each application. As shown additional phase margin is achieved at the loss of slew rate and bandwidth.

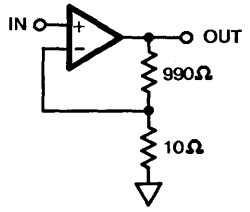
For example, for a voltage gain of +2 (or -1) and a load of 500pF/2kΩ, 20pF is needed for compensation to give a small signal bandwidth of 30MHz with 40° of phase margin. If a full power output voltage of ±10V is needed, this same configuration will provide a bandwidth of 5MHz and a slew rate of 200V/µs.

If maximum bandwidth is desired and no compensation is needed, care must be given to minimize parasitic capacitance at the compensation pin. In some cases where minimum gain applications are desired, bending up or totally removing this pin may be the solution. In this case, care must also be given to minimize load capacitance.

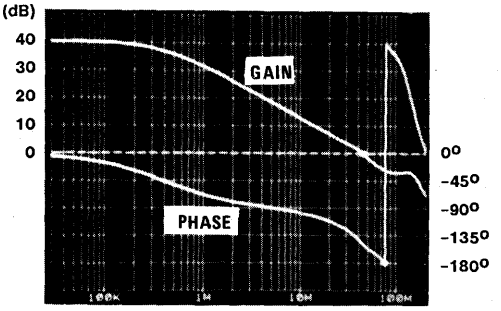
For wideband positive unity gain applications, the HA-2542 can also be over-compensated with capacitance greater than 30pF to achieve bandwidths of around 25MHz. This over-compensation will also improve capacitive load handling or lower the noise bandwidth. This versatility along with the ±100mA output current makes the HA-2542 an excellent high speed driver for many power applications.

Typical Applications

NONINVERTING CIRCUIT (A_{VCL} = 100)

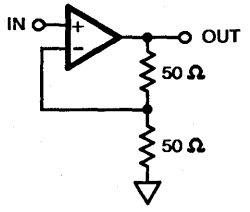


FREQUENCY (0dB) = 44.9MHz
PHASE MARGIN (0dB) = 40°

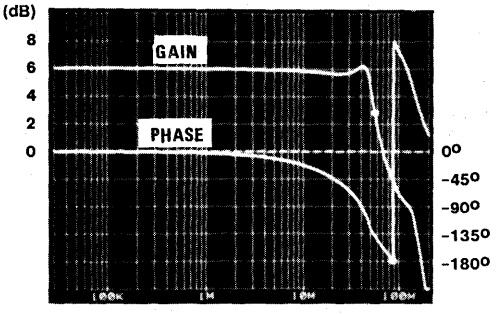


A_{VCL} = 100 PHASE AND GAIN

NONINVERTING CIRCUIT (A_{VCL} = 2)

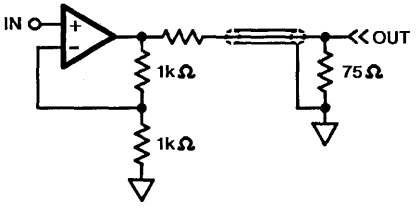


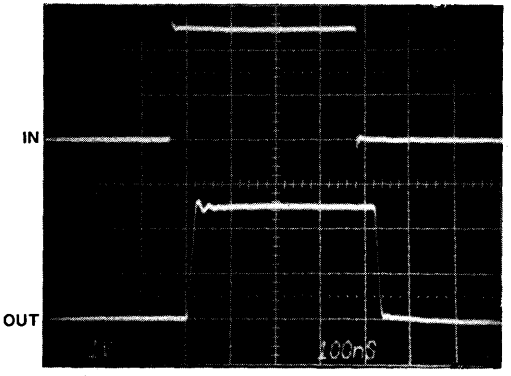
FREQUENCY (3dB) = 56MHz
PHASE (3dB) = 40°



A_{VCL} = 2 PHASE AND GAIN

VIDEO CABLE DRIVER (A_{VCL} = 2)





VIDEO CABLE DRIVER PULSE RESPONSE
(1V/Div.; 100ns/Div.)

HARRIS

HA-2544

May 1990

Video Operational Amplifier

Features

- Gain Bandwidth 50MHz
- High Slew Rate 150V/μs
- Low Supply Current 10mA
- Differential Gain Error ..... <0.05dB
- Differential Phase Error ..... <0.1 degree
- Gain Tolerance at 5MHz ..... <0.15dB

Applications

- Video Systems
- Video Test Equipment
- Radar Displays
- Imaging Systems
- Pulse Amplifiers
- Signal Conditioning Circuits
- Data Acquisition Systems

Description

The HA-2544 is a fast, unity gain stable, monolithic op amp designed to meet the needs required for accurate reproduction of video or high speed signals. It offers high voltage gain (6kV/V) and high phase margin (65 degrees) while maintaining tight gain tolerance over the video bandwidth. Built from high quality Dielectric Isolation, the HA-2544 is another addition to the Harris series of high speed, wideband Op-Amps, and offers true video performance combined with the versatility of an op-amp.

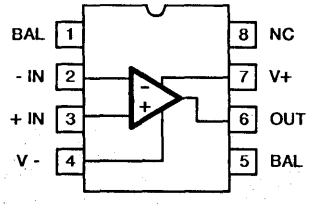
The primary features of the HA-2544 include 50MHz Gain Bandwidth, 150V/μs slew rate, < 0.05dB differential gain error and gain tolerance of just 0.15dB at 5MHz. High performance and low power requirements are met with a supply current of only 10mA.

Uses of the HA-2544 range from video test equipment, guidance systems, radar displays and other precise imaging systems where stringent gain and phase requirements have previously been met with costly hybrids and discrete circuitry. The HA-2544 will also be used in non-video systems requiring high speed signal conditioning such as data acquisition systems, medical electronics, specialized instrumentation and communication systems.

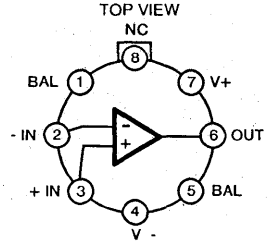
The HA-2544-2 is guaranteed over the military temperature range (-55°C to +125°C); the HA-2544/2544C-5 over the commercial range (0°C to +75°C) and the HA-2544/2544C-9 over the industrial range (-40°C to +85°C). The HA-2544 is available in TO-99 Metal Can, SOIC, and both Plastic and Ceramic Mini-DIP packages. Military (/883) product and data sheets are available upon request.

Pinouts

HA9P2544/2544C (SOIC)
HA7-2544 (CERAMIC MINI-DIP)
HA3-2544/2544C (PLASTIC MINI-DIP)
TOP VIEW

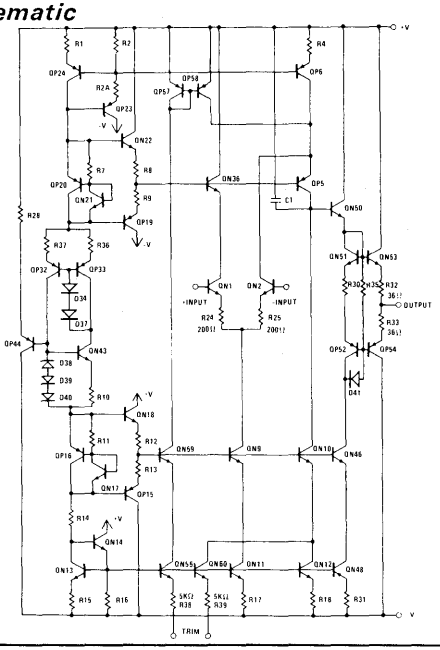


HA2-2544 (TO-99 METAL CAN)
TOP VIEW



NOTE: V_{CASE} = V-

Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 33V
Differential Input Voltage (Note 11) ..... ±6V
Output Current (Peak) ..... ±40mA
Internal Power Dissipation 700mW

Operating Temperature Range

HA-2544/2544C-5 ..... $0^oC \leq T_A \leq +75^oC$
HA-2544-9 ..... $40^oC \leq T_A \leq +85^oC$
HA-2544-2 ..... $-55^oC \leq T_A \leq +125^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature ..... $+175^oC$

Electrical Specifications $V_S = \pm15V$, $C_L \leq 10pF$, $R_L = 1k\Omega$, Unless Otherwise Specified

PARAMETER	TEMP	HA-2544-2/-5			HA-2544C-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	6	15	-	15	25	mV
	-2, -5	-	-	20	-	-	40	mV
	-9	-	-	25	-	-	40	mV
Average Offset Voltage Drift (Note 9)	Full	-	10	-	-	10	-	µV/°C
Bias Current	+25°C	-	7	15	-	9	18	µA
	Full	-	-	20	-	-	30	µA
Average Bias Current Drift (Note 9)	Full	-	0.04	-	-	0.04	-	µA/°C
Offset Current	+25°C	-	0.2	2	-	0.8	2	µA
	Full	-	-	3	-	-	3	µA
Offset Current Drift	Full	-	10	-	-	10	-	nA/°C
Common Mode Range	Full	±10	±11.5	-	±10	±11.5	-	V
Differential Input Resistance	+25°C	50	90	-	50	90	-	kΩ
Differential Input Capacitance	+25°C	-	3	-	-	3	-	pF
Input Noise Voltage (f = 1kHz)	+25°C	-	20	-	-	20	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C	-	2.4	-	-	2.4	-	$pA/\sqrt{Hz}$
Input Noise Voltage								
0.1Hz to 10Hz (Note 9)	+25°C	-	1.5	-	-	1.5	-	µV p-p
0.1Hz to 1MHz	+25°C	-	4.6	-	-	4.6	-	µV r.m.s.
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 4, 9)	+25°C	3.5	6	-	3	6	-	kV/V
	Full	2.5	-	-	2	-	-	kV/V
Common Mode Rejection Ratio (Notes 6, 9)	-2, -5	75	89	-	70	89	-	dB
	-9	75	89	-	65	89	-	dB
Minimum Stable Gain	+25°C	+1	-	-	+1	-	-	V/V
Unity Gain Bandwidth (Notes 3, 9)	+25°C	-	45	-	-	45	-	MHz
Gain Bandwidth Product (Notes 3, 9)	+25°C	-	50	-	-	50	-	MHz
Phase Margin	+25°C	-	65	-	-	65	-	Degrees

Electrical Specifications (Continued)

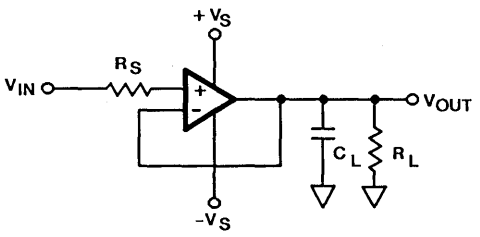
PARAMETER	TEMP	HA-2544-2/-5			HA-2544C-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±10	±11	-	±10	±11	-	V
Full Power Bandwidth (Note 7)	+25°C	3.2	4.2	-	3.2	4.2	-	MHz
Peak Output Current (Note 9)	+25°C	±25	±35	-	±25	±35	-	mA
Continuous Output Current (Note 9)	+25°C	±10	-	-	±10	-	-	mA
Output Resistance (Open Loop)	+25°C	-	20	-	-	20	-	Ω
TRANSIENT RESPONSE								
Rise Time (Note 3)	+25°C	-	7	-	-	7	-	ns
Overshoot (Note 3)	+25°C	-	10	-	-	10	-	%
Slew Rate	+25°C	100	150	-	100	150	-	V/μs
Settling Time (Note 5)	+25°C	-	120	-	-	120	-	ns
VIDEO PARAMETERS $R_S = 50\Omega$, $R_L = 1k\Omega$ (Notes 2, 10)								
Differential Phase (Notes 2, 12)								
$R_S = 50\Omega$	+25°C	-	0.05	0.11	-	0.05	0.11	Degree
$R_S = 1k\Omega$	+25°C	-	0.4	-	-	0.4	-	Degree
Differential Gain (Note 2, 12, 14)							-	
$R_S = 50\Omega$	+25°C	-	0.02	0.04	-	0.02	0.04	dB
$R_S = 50\Omega$	+25°C	-	0.23	0.46	-	0.23	0.46	%
$R_S = 1k\Omega$	+25°C	-	0.15	-	-	0.15	-	dB
$R_S = 1k\Omega$	+25°C	-	1.7	-	-	1.7	-	%
Gain Tolerance (Note 2)								
5MHz	+25°C	-	-0.10	±0.15	-	-0.10	±0.15	dB
10MHz	+25°C	-	-0.12	±0.35	-	-0.12	±0.35	dB
Chrominance to Luminance Gain (Note 13)	+25°C	-	0.1	-	-	0.1	-	dB
Chrominance to Luminance Delay (Note 13)	+25°C	-	7	-	-	7	-	ns
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	10	12	-	10	15	mA
Power Supply Rejection Ratio (Notes 8, 9)	-2, -5	70	80	-	70	80	-	dB
	-9	65	80	-	65	80	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Guaranteed by sample test and not 100% tested.
3. $V_{OUT} = \pm 100mV$. For Rise Time and Overshoot testing, V_{OUT} is measured from 0 to +200mV and 0 to -200mV.
4. $V_{OUT} = \pm 5V$
5. Settling Time is specified to 0.1% of final value for a 10V step and $A_V = -1$
6. $\Delta V_{CM} = \pm 10V$
7. Full Power Bandwidth is guaranteed by equation:
   $$\text{Full Power Bandwidth} = \frac{\text{Slew Rate}}{2\pi\ V_{peak}} \quad (V_{peak} \text{ used} = 5V)$$
8. $\Delta V_S = \pm 10$ to $\pm 20V$
9. Refer to typical performance curve in Data Sheet.
10. The video parameter specifications will degrade as the output load resistance decreases.
11. To achieve optimum AC performance, the input stage was designed without protective diode clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of the input transistors and probable degradation of the input parameters especially V_{OS}, I_{OS} and Noise.
12. Test signal used is ±200mV at 3.58MHz and 4.43MHz on a 0 and 1 Volt offset. For adaquate test repeatability, a minimum warm-up of 2 minutes is suggested.
13. C-L Gain and C-L Delay was less than the resolution of the test equipment used which is 0.1dB and 7ns, respectively.
14. $A_D(\%) = \left[10^{\frac{A_D(dB)}{20}} - 1 \right] \times 100$

Test Circuits

TRANSIENT RESPONSE

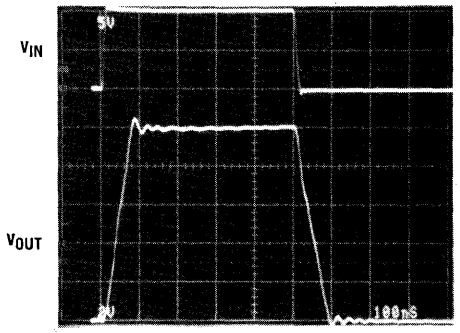


$V_S = \pm 15V$
$A_V = +1$
$R_S = 50$ or 75Ω (Optional)
$R_L = 1k\Omega$
$C_L < 10pF$

V_{IN} for Large Signal = $\pm 5V$
V_{IN} for Small Signal = 0 to +200mV and 0 to -200mV

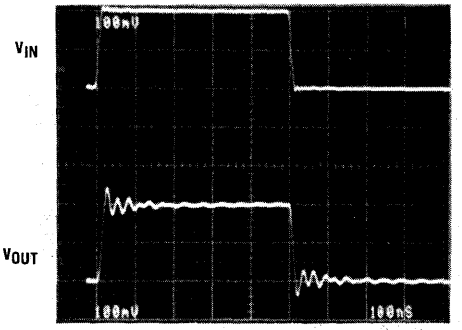
LARGE SIGNAL RESPONSE

V_{OUT} = 0 to +10V
Vertical Scale: (V_{IN} = 5V/Div.; V_{OUT} = 2V/Div.)
Horizontal Scale: (100ns/Div.)

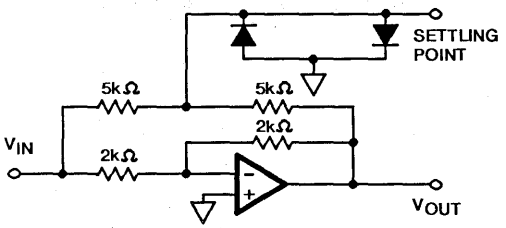


SMALL SIGNAL RESPONSE

V_{OUT} = 0 to +200mV
Vertical Scale: (V_{IN} = 100mV/Div.; V_{OUT} = 100mV/Div.)
Horizontal Scale: (100ns/Div.)

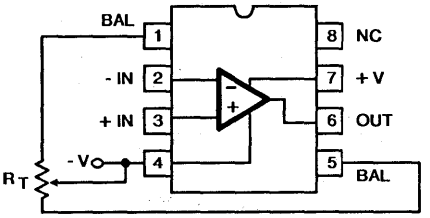


SETTLING TIME TEST CIRCUIT



- $A_V = -1$
- Feedback and Summing Resistors Must Be Matched (0.1%)
- HP5082-2810 Clipping Diodes Recommended.
- Tektronix P6201 FET Probe Used At Settling Point.

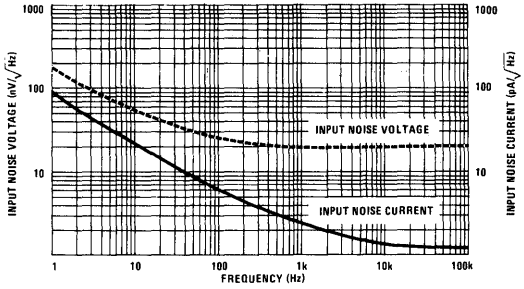
OFFSET VOLTAGE ADJUSTMENT



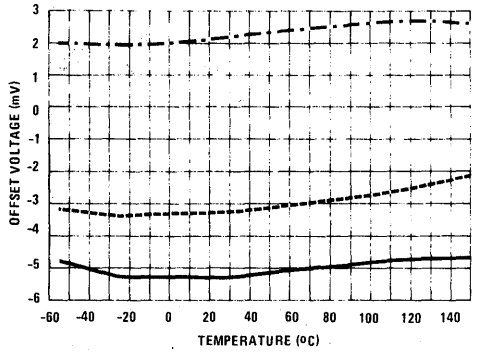
Tested Offset Adjustment Range Is | V_{OS} +1mV | Minimum Referred To Output. Typical Range For $R_T = 20k\Omega$ Is Approximately $\pm 30mV$

Typical Performance Curves

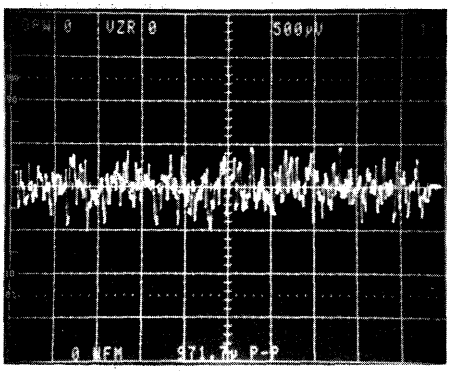
INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



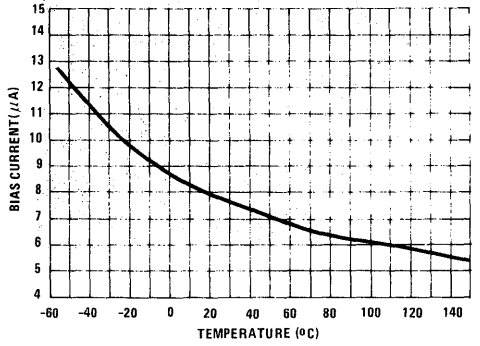
INPUT OFFSET VOLTAGE vs.TEMPERATURE
3 Typical Units



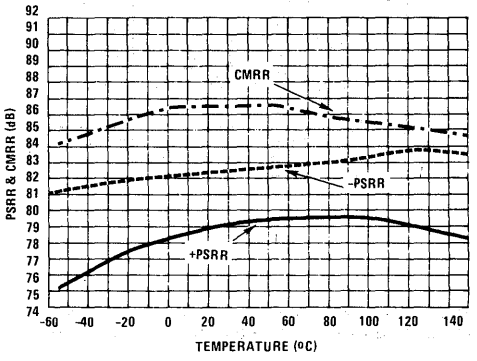
NOISE VOLTAGE
(A_V = 1000)
0.1Hz to 10Hz, Noise Voltage = 0.97μVp-p



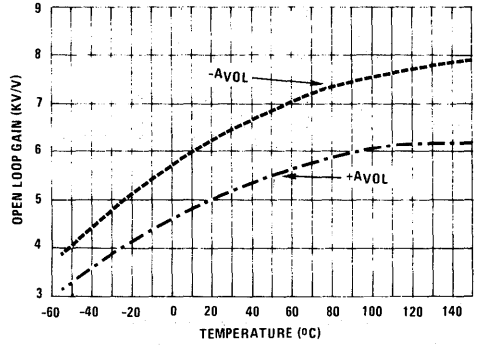
INPUT BIAS CURRENT vs. TEMPERATURE
V_S = ±15V, R_L = 1kΩ



PSRR and CMRR vs. TEMPERATURE
V_S = ±15V, R_L = 1kΩ

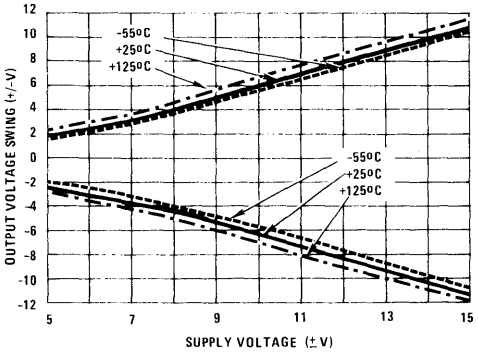


OPEN LOOP GAIN vs. TEMPERATURE
V_S = ±15V, R_L = 1kΩ

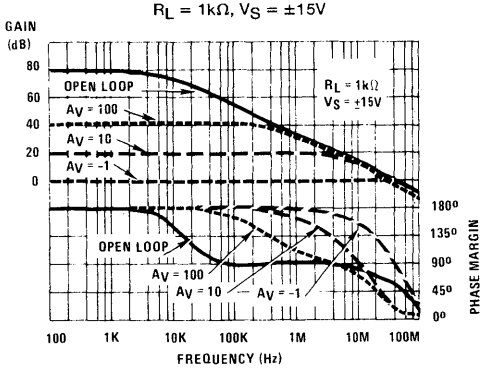


Typical Performance Curves (Continued)

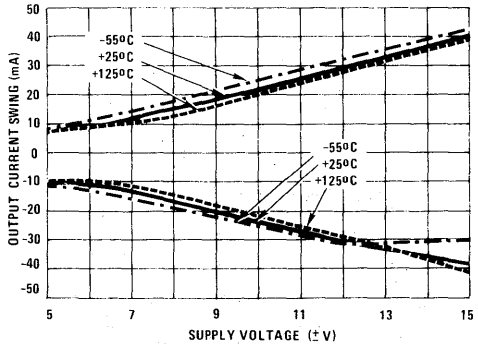
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
(Over Full Temperature)



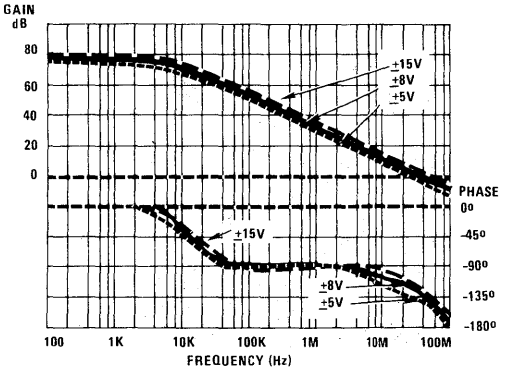
FREQUENCY RESPONSE AT VARIOUS GAINS
R_L = 1kΩ, V_S = ±15V



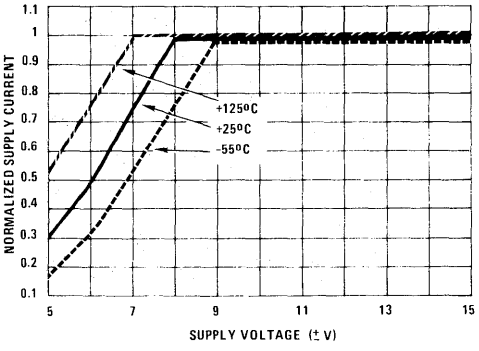
OUTPUT CURRENT vs. SUPPLY VOLTAGE
(Over Full Temperature)



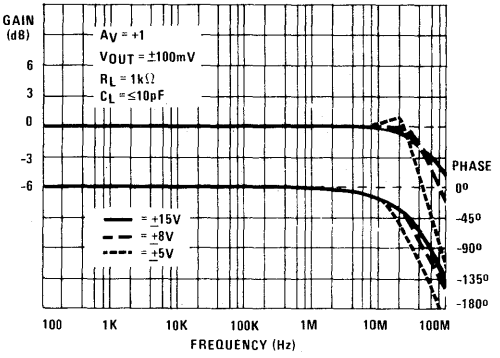
OPEN LOOP RESPONSE vs. SUPPLY VOLTAGE
V_{OUT} = ±100mV



SUPPLY CURRENT vs. SUPPLY VOLTAGE
Normalized at V_S = ±15V at +25°C

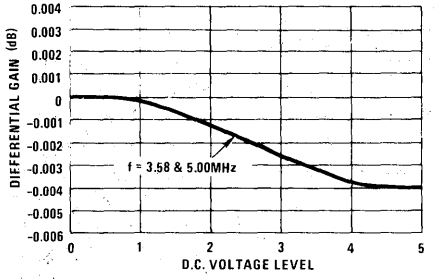


VOLTAGE FOLLOWER RESPONSE vs. SUPPLY VOLTAGE
A_V = +1, R_L = 1K, C_L < 10pF

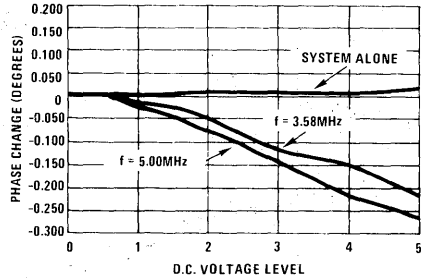


Typical Video Performance

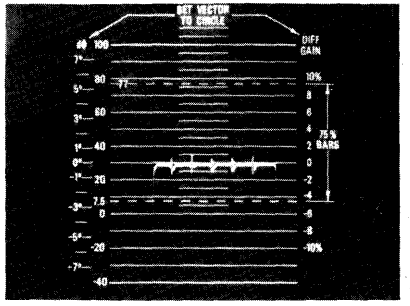
A.C. GAIN VARIATION vs. D.C. OFFSET LEVELS
(Differential Gain)



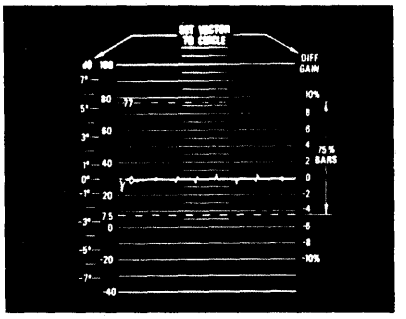
A.C. PHASE VARIATION vs. D.C. OFFSET LEVELS
(Differential Phase)



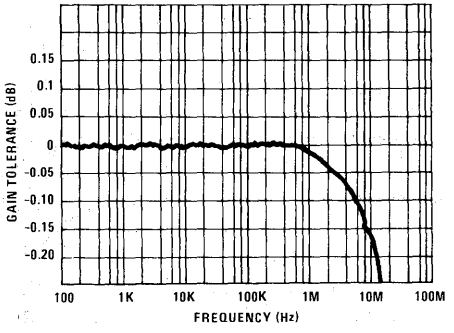
DIFFERENTIAL GAIN
NTSC Method, R_L = 1kΩ
Differential Gain < 0.05% at T_A = +75°C
No Visual Difference at T_A = -55°C or +125°C



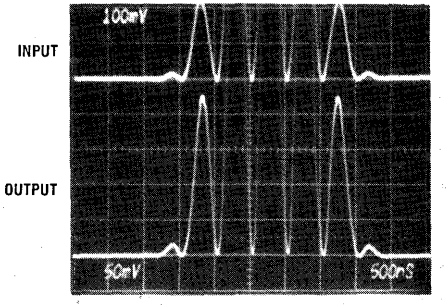
DIFFERENTIAL PHASE
NTSC Method, R_L = 1kΩ
Differential Phase < 0.05 Degree at T_A = +75°C
No Visual Difference at T_A = -55°C or +125°C



GAIN TOLERANCE
A_V = +1, V_{IN} = ±100mV
R_L = 1K, C_L < 10pF



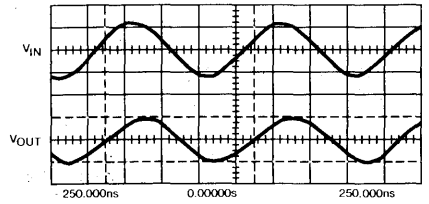
CHROMINANCE TO LUMINANCE DELAY
NTSC Method, R_L = 1kΩ
C-L Delay < 7ns at T_A = +75°C
No Visual Difference at T_A = -55°C or +125°C



Vertical Scale: Input = 100mV/Div.
Output = 50mV/Div.
Horizontal Scale: 500ns/Div.

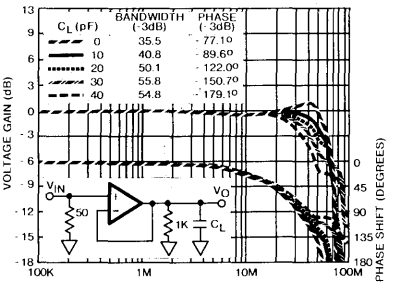
Typical Video Performance Curves (Continued)

±2 VOLT OUTPUT SWING
With R_{LOAD} = 75Ω (Frequency = 5.00MHz)



V_{IN} = 2.0V/Div., V_{OUT} = 2.0V/Div.
Timebase = 50ns/Div.

BANDWIDTH vs. LOAD CAPACITANCE
A_V = +1, V_S = ±15V, R_L = 1kΩ



Applications And Product Guidelines

The HA-2544 is a true differential op amp that is as versatile as any op amp but offers the advantages of high unity gain bandwidth, high speed and low supply current. More important than its' general purpose applications is that the HA-2544 was especially designed to meet the requirements found in a video amplifier system. These requirements include fine picture resolution and accurate color rendition, and must meet broadcast quality standards.

In a video signal, the video information is carried in the amplitude and phase as well as in the D.C. level. The amplifier must pass the 30Hz line rate luminance level and the 3.58MHz (NTSC) or 4.43MHz (PAL) color band without altering phase or gain. The HA-2544's key specifications aimed at meeting this include high bandwidth (50MHz), very low gain tolerance (<±0.15dB at 5MHz), near unmeasurable differential gain and differential phase (<0.04dB and 0.11 degrees), and low noise (20nV/$\sqrt{Hz}$). The HA-2544 meets these quidelines and are sample tested for standard grade product (/883, -2, -7, -5) at 5 and/or 10MHz. If a customer wishes to 100% test these specifications, arrangement can be made.

The HA-2544 also offers the advantage of a full output voltage swing of ±10V into a 1K ohm load. This equates to a full power bandwidth of 2.4MHz for this ±10V signal. If video signal levels of ±2V maximum is used (with R_L = 1K ohm), the full power bandwidth would be 11.9MHz without clipping distortion. Another usage might be required for a direct 50 ohm or 75 ohm load where the HA-2544 will still swing this ±2V signal as shown in the above display. One important note that must be realized is that as load resistance decreases the video parameters are also degraded. For optimal video performance a 1kΩ load is recommended.

If lower supply voltage are required, such as ±5V, many of the characterization curves indicate where the parameters vary. As shown the bandwidth, slew rate and supply current are still very well maintained.

Prototyping and PC Board Layout

When designing with the HA-2544 video op amp as with any high performance device, care should be taken to use high frequency layout techniques to avoid unwanted parasitic effects. Short lead lengths, low source impedance and lower value feedback resistors help reduce unwanted poles or zeros. This layout would also include ground plane construction and power supply decoupling as close to the supply pins with suggested parallel capacitors of 0.1μF and 0.001μF ceramic to ground.

In the noninverting configuration, the amplifier is sensitive to stray capacitance (<40pF) to ground at the inverting input. Therefore, the inverting node connections should be kept to a minimum. Phase shift will also be introduced as load parasitic capacitance is increased. A small series resistor (20 ohm to 100 ohm) before the capacitance effectively decouples this effect.

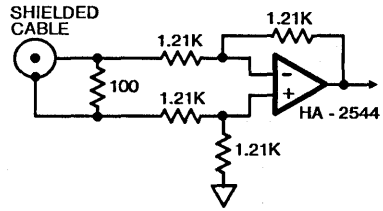
Stability/Phase Margin/Compensation

The HA-2544 has not sacrificed unity gain stability in achieving its superb AC performance. For this device, the phase margin exceeds 60 degrees at the unity crossing point of the open loop frequency response. Large phase margin is critical in order to reduce the differential phase and differential gain errors caused by most other op amps. Because this part is unity gain stable, no compensation pin is brought out. If compensation is desired to reduce the noise bandwidth, most standard methods may be used. One method suggested for an inverting scheme would be a series R-C from the inverting node to ground which will reduce bandwidth, but not effect slew rate. If the user wishes to achieve even higher bandwidth (>50MHz), and can tolerate some slight gain peaking and lower phase margin, experimenting with various load capacitance can be done.

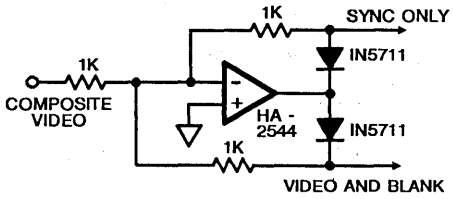
Shown in Application 1 is an excellent Differential Input, Unity Gain Buffer which also will terminate a cable to 75 ohm and reject common-mode voltages. Application 2 is a method of separating a video signal up into the Sync. only signal and the Video and Blanking signal. Application 3 shows the HA-2544 being used as a 100kHz High Pass 2-Pole Butterworth Filter. Also shown is the measured frequency response curves.

Typical Application

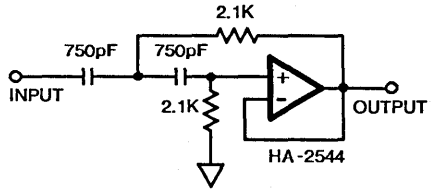
APPLICATION 1
75Ω Differential Input Buffer



APPLICATION 2
Composite Video Sync. Separator

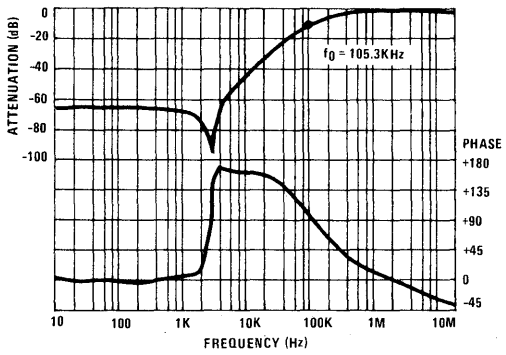


APPLICATION 3
100kHz High Pass 2-Pole Butterworth Filter



$$f_0 = \frac{1}{2\pi(2.1K \cdot 750pF)}$$

Measured Frequency Response of Application 3



Die Characteristics

Transistor Count 44
Die Dimensions ..... 80 x 65 x 19 mils (2030 x 1630 x 485µm)
Substrate Potential* ..... V-
Process ..... High Frequency Bipolar D.I.
Passivation ..... Nitride

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Metal Can TO-99, HA2-2544	186	50
Plastic Mini-DIP, HA3-2544/2544C	80	20
Ceramic Mini-DIP, HA7-2544	185	98
SOIC, HA9P2544	160	42

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS

HA-2548

Precision, High Slew Rate, Wideband Operational Amplifier

May 1990

Features

- High Slew Rate 120V/μs
- Low Offset Voltage 300μV
- High Open Loop Gain 130dB
- Gain Bandwidth Product 150MHz
- Low Voltage Noise @ 1kHz ..... 8.3nV/$\sqrt{Hz}$
- Minimum Gain Stability ..... ≥5

Applications

- High Speed Instrumentation
- Data Acquisition Systems
- Analog Signal Conditioning
- Precision, Wideband Amplifiers
- Pulse/RF Amplifiers

Description

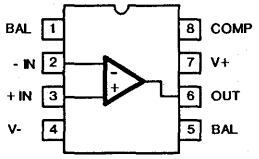
The HA-2548 is a monolithic op amp that offers a unique combination of bandwidth, slew rate, and precision specifications. These features can eliminate the need for composite op amp designs and external calibration circuitry.

Optimized for gains ≥5, the HA-2548 has a gain-bandwidth product of 150MHz and a slew rate of 120V/μs while maintaining extremely high open loop gain (130dB typ) and low offset voltage (300μV typ). These specifications are achieved through uniquely designed input circuitry and a single ultra-high gain stage that minimizes the AC signal path. Capable of delivering over 30mA of output current, the HA-2548 is ideal for precision, high speed applications such as signal conditioning, instrumentation, video/pulse amplifiers and buffers.

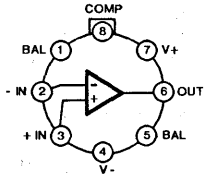
The HA-2548 is offered with a -5 temperature grade guaranteed between 0°C and +75°C and a -9 temperature grade guaranteed between -40°C and +85°C. Both grades are available in either a Ceramic Sidebrazed DIP or a TO-99 Metal Can. The HA-2548A is offered with the -5 temperature grade and is only available in the TO-99 Metal Can package. For information on the military version of this device please refer to the HA-2548/883 datasheet.

Pinouts

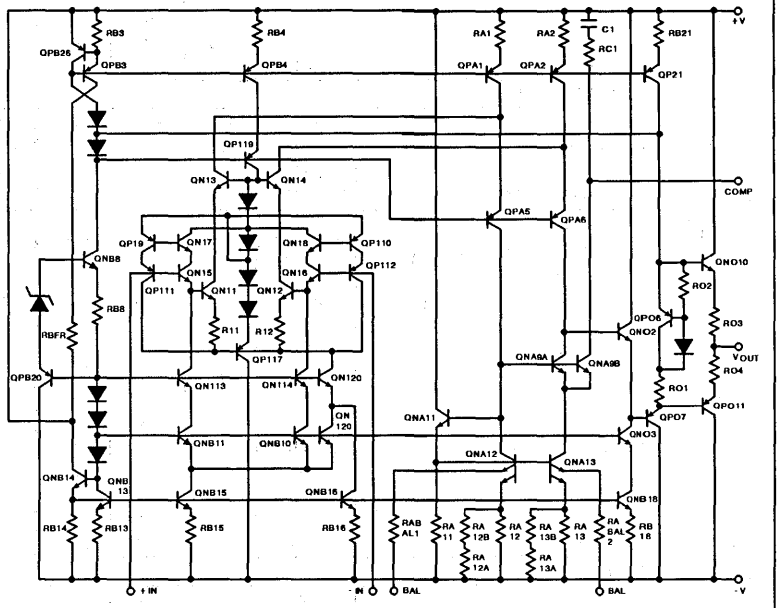
HA7-2548
(CERAMIC SIDEBRAZED DIP)
TOP VIEW



HA2-2548
(TO-99 METAL CAN)
TOP VIEW



Schematic (Simplified)



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage 5V
Output Current 40mA

Operating Temperature Range:

HA-2548-5 ..... $0^oC \leq T_A \leq +75^oC$
HA-2548-9 ..... $-40^oC \leq T_A \leq +85^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature ..... $+175^oC$

Electrical Specifications V+ = +15V, V- = -15V, R_L = 1K, C_L = 10pF. (Unless Otherwise Specified)

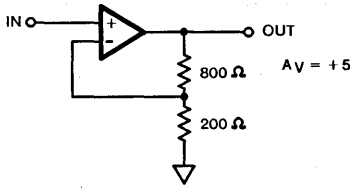
PARAMETER		TEMP	HA-2548-5, -9 MIN	HA-2548-5, -9 TYP	HA-2548-5, -9 MAX	HA-2548A-5 MIN	HA-2548A-5 TYP	HA-2548A-5 MAX	UNITS
INPUT CHARACTERISTICS									
Input Offset Voltage		+25°C	-	300	900	-	100	300	µV
		Full	-	400	1200	-	200	600	µV
Average Offset Voltage Drift (Note 12)		Full	-	4	9	-	3	7	µV/°C
Input Bias Current		+25°C	-	5	50	-	5	50	nA
		Full	-	20	100	-	20	100	nA
Input Offset Current		+25°C	-	5	50	-	5	50	nA
		Full	-	20	100	-	20	100	nA
Common Mode Range		+25°C	±7	±10	-	±7	±10	-	V
Differential Input Resistance		+25°C	-	1	-	-	1	-	MΩ
Input Noise Voltage	f_O = 0.1Hz to 10Hz	+25°C	-	0.2	-	-	0.2	-	µVrms
	f_O = 0.1Hz to 1MHz	+25°C	-	0.8	-	-	0.8	-	µVrms
Input Noise Voltage Density	f_O =10Hz	+25°C	-	30	-	-	30	-	$nV/\sqrt{Hz}$
(Note 2)	f_O =100Hz	+25°C	-	12	-	-	12	-	$nV/\sqrt{Hz}$
	f_O =1000Hz	+25°C	-	8.3	-	-	8.3	-	$nV/\sqrt{Hz}$
Input Noise Current Density	f_O =10Hz	+25°C	-	1.9	-	-	1.9	-	$pA/\sqrt{Hz}$
(Note 2)	f_O =100Hz	+25°C	-	0.7	-	-	0.7	-	$pA/\sqrt{Hz}$
	f_O =1000Hz	+25°C	-	0.4	-	-	0.4	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain (Note 3)		+25°C	114	130	-	120	130	-	dB
		Full	108	125	-	118	125	-	dB
Common Mode Rejection Ratio (Note 4)		Full	80	90	-	80	90	-	dB
Gain Bandwidth Product (Note 5,12)		+25°C	130	150	-	130	150	-	MHz
		Full	110	125	-	110	125	-	MHz
Minimum Stable Gain		Full	5	-	-	5	-	-	V/V
OUTPUT CHARACTERISTICS									
Output Voltage Swing		Full	±11	±12	-	±11	±12	-	Volts
Output Current (Note 6)		Full	±30	±33	-	±30	±33	-	mA
Output Resistance		+25°C	-	5	-	-	5	-	Ω
Full Power Bandwidth (Note 7,12)		+25°C	-	1.91	-	-	1.91	-	MHz
TRANSIENT RESPONSE									
Slew Rate (Note 8,12)	Positive	+25°C	80	120	-	80	120	-	V/µs
		Full	70	105	-	70	105	-	V/µs
	Negative	+25°C	70	110	-	70	110	-	V/µs
		Full	60	105	-	60	105	-	V/µs
Rise Time (Note 9,12)		+25°C	-	16.5	20	-	16.5	20	ns
		Full	-	19	23	-	19	23	ns
Fall Time (Notes 9,12)		+25°C	-	16	20	-	16	20	ns
		Full	-	18	23	-	18	23	ns
Overshoot (Note 9,12)	Positive	+25°C	-	15	25	-	15	25	%
		Full	-	25	35	-	25	35	%
	Negative	+25°C	-	8	15	-	8	15	%
		Full	-	20	30	-	20	30	%
Settling Time (Note 10,12)		+25°C	-	200	260	-	200	260	ns
POWER SUPPLY									
PSRR (Note 11)		Full	86	95	-	86	95	-	dB
I_{CC}		Full	-	12	18	-	12	18	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the servicability of the circuit may be impaired. Functional operation under any of these conditions is not nessarily implied.
2. Refer to typical performance curve in data sheet.
3. $V_{OUT} = \pm 10V$.
4. $V_{CM} = \pm 2V$.
5. Characterized in an $A_V = -100$ configuration from 100kHz to 10MHz.
6. $R_L = 1k\Omega$, $V_{OUT} > 10V$.
7. Full Power Bandwidth is calculated by:
$$FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}, V_{peak} = 10V$$
8. $V_{OUT} = \pm 5V$, $A_V = +5$.
9. $V_{OUT} = \pm 100mV$, $A_V = +5$.
10. Settling time is specified to 0.01% with a 10V step and $A_V = -5$.
11. Delta $V_S = \pm 10V$ to $\pm 20V$.
12. These parameters are not tested. The limits are guaranteed based on lab characterization and reflect lot to lot variation.

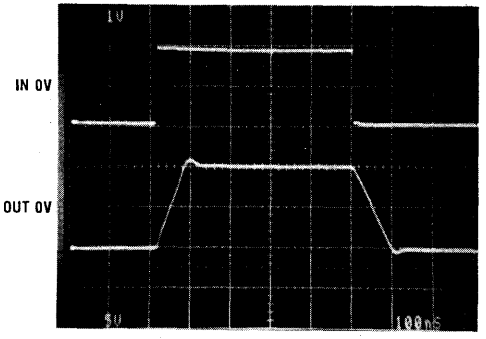
Test Circuits and Waveforms

LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



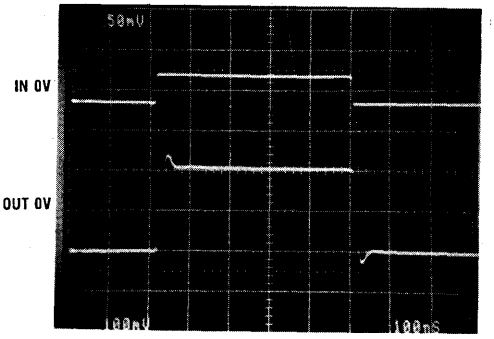
LARGE SIGNAL RESPONSE

$V_{OUT} = \pm 5V$, $A_V = \pm 5$, $R_L = 1K$, $C_L \leq 10pF$

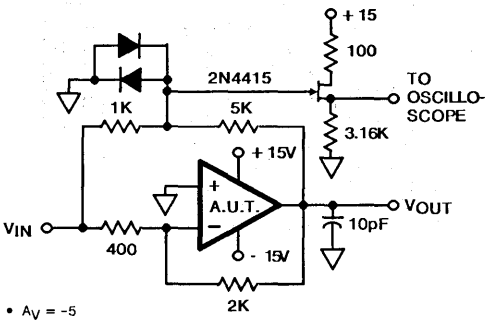


SMALL SIGNAL RESPONSE

$V_{OUT} = \pm 100mV$, $A_V = \pm 5$, $R_L = 1K$, $C_L \leq 10pF$



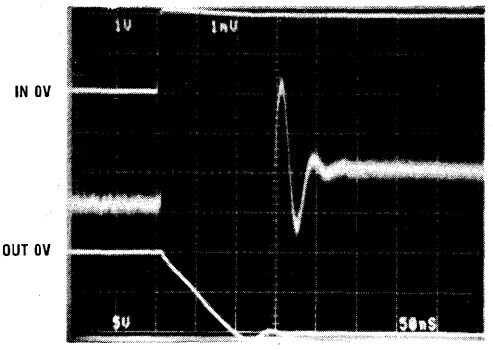
SETTLING TIME TEST CIRCUIT



- $A_V = -5$
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

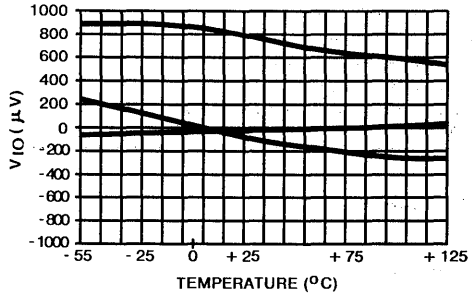
HA-2548 SETTLING TIME

$A_V = -5$, Output = -10V Output Scale Vertical: 1mV/Div
Horizontal: 50ns/Div

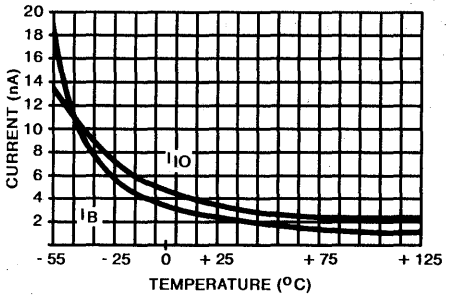


Typical Performance Curves $V_S = \pm15V$, $T_A = +25^oC$

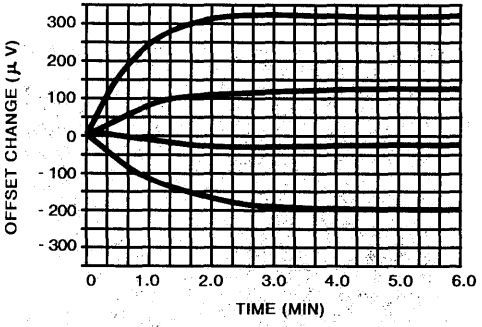
V_{IO} vs TEMPERATURE
(3 Representative Units)



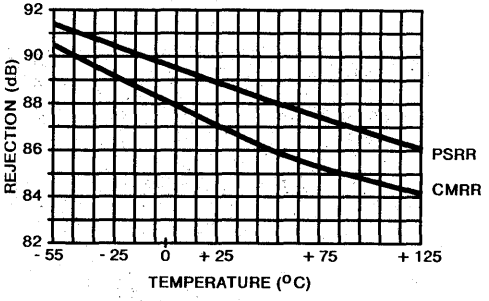
OFFSET CURRENT/BIAS CURRENT vs TEMPERATURE



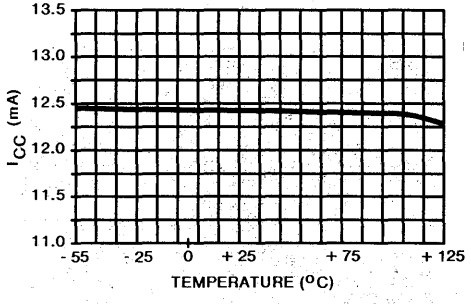
V_{IO} WARM-UP DRIFT (NORMALIZED FROM ZERO)
(4 Representative Units)



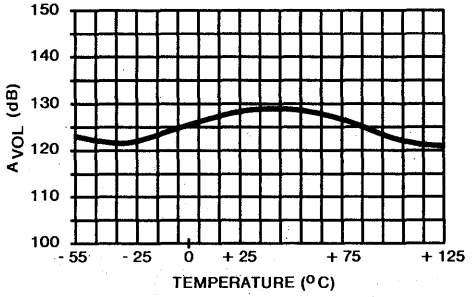
PSRR/CMRR vs TEMPERATURE
$V_{CC} = \pm15V$, $V_{CM} = \pm2V$, $V_S = \pm10V$ to $\pm20V$



I_{CC} vs TEMPERATURE

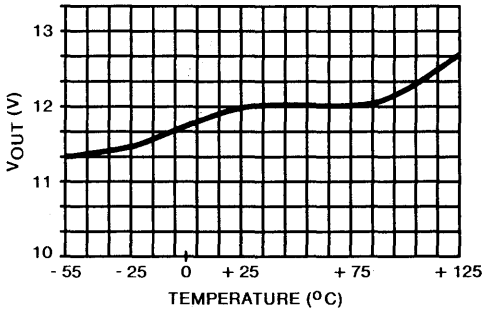


A_{VOL} vs TEMPERATURE
$V_{CC} = \pm15V$, $R_L = 1K\Omega$
$C_L = \leq10pF$, $V_{OUT} = \pm10V$

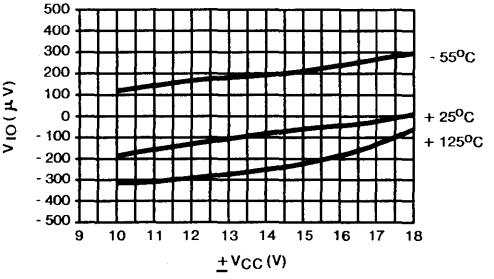


Typical Performance Curves (Continued) $V_S = \pm 15V$, $T_A = +25^oC$

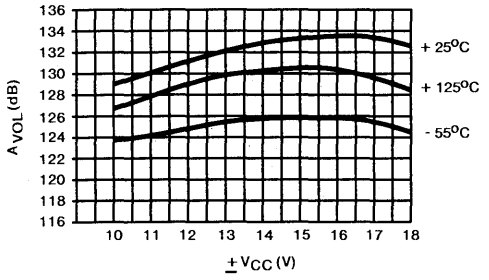
V_{OUT} vs TEMPERATURE
$V_{CC} = \pm 15V$, $R_L = 1k\Omega$, $C_L = \leq 10pF$



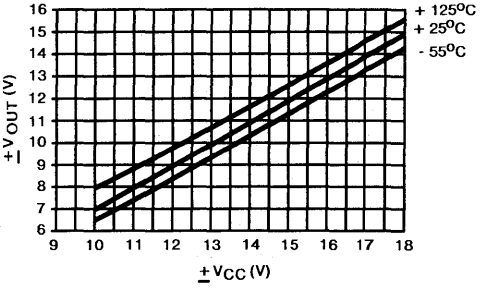
V_{IO} vs $\pm V_{CC}$ vs TEMPERATURE



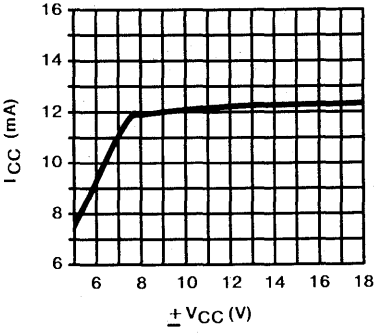
A_{VOL} vs $\pm V_{CC}$ vs TEMPERATURE
$V_{OUT} = \pm 5V$ @ $V_{CC} = \pm 10V$, $V_{OUT} = \pm 10V$ @ $V_{CC} = \pm 15V$
$V_{OUT} = \pm 12V$ @ $V_{CC} = 18V$



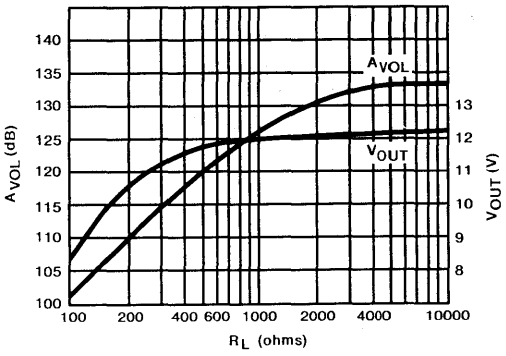
$\pm V_{OUT}$ vs $\pm V_{CC}$ vs TEMPERATURE
$R_L = 1K$



SUPPLY CURRENT vs ±SUPPLY VOLTAGE

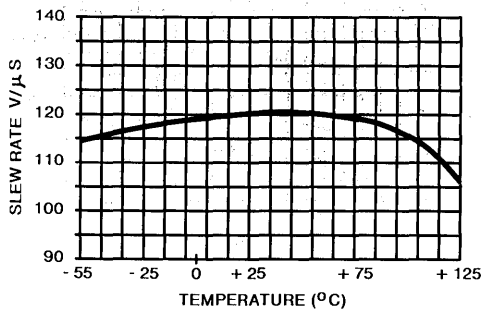


A_{VOL}/V_{OUT} vs R_L
$V_{IN} = \pm 3V$ For 100Ω, $V_{IN} = \pm 5V$ For 200Ω
$V_{IN} = \pm 10V$ For 600Ω to $10k\Omega$

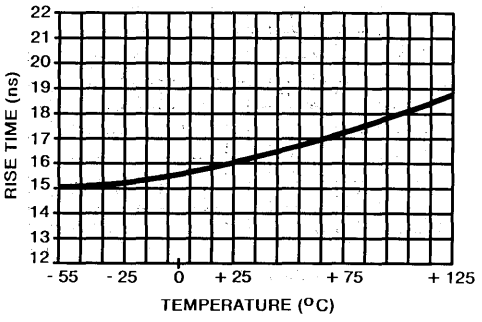


Typical Performance Curves (Continued) $V_S = \pm15V$, $T_A = +25^oC$

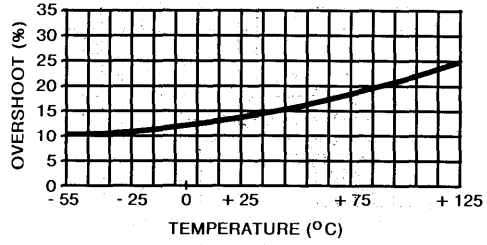
SLEW RATE vs TEMPERATURE
$V_{CC} = \pm15V$, $R_L = 1k\Omega$, $C_L = \leq 10pF$
$A_V = \pm5$, $V_{OUT} = \pm5V(10Vp\text{-}p)$



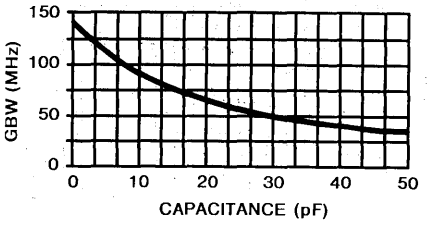
RISE TIME vs TEMPERATURE
$V_{CC} = \pm15V$, $R_L = 1k\Omega$, $C_L = \leq 10pF$
$A_V = +5$, $V_{OUT} = \pm100mV(200mVp\text{-}p)$



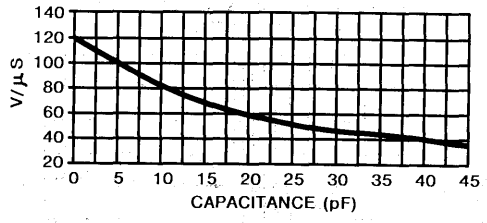
% OVERSHOOT vs TEMPERATURE
$A_V = +5$, $V_{OUT} = \pm100mV(200mVp\text{-}p)$
$R_L = 1k\Omega$, $C_L \leq 10pF$



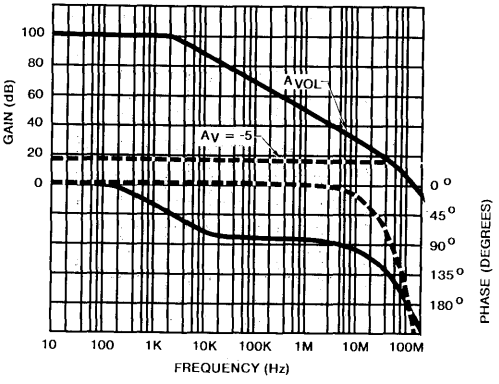
GAIN BANDWIDTH PRODUCT vs COMPENSATION CAPACITANCE



SLEW RATE vs COMPENSATION CAPACITANCE

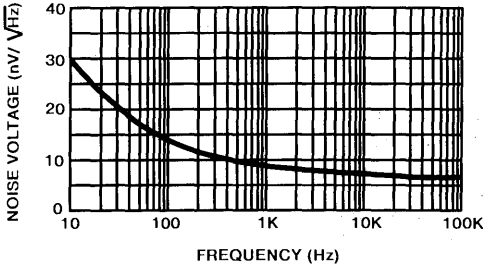


GAIN AND PHASE vs FREQUENCY
$R_L = 1k\Omega$, $C_L \leq 10pF$

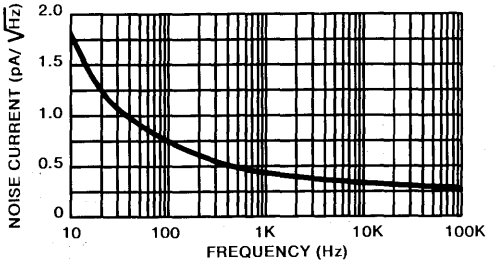


Typical Performance Curves (Continued) $V_S = \pm 15V$, $T_A = +25^oC$

INPUT NOISE VOLTAGE DENSITY

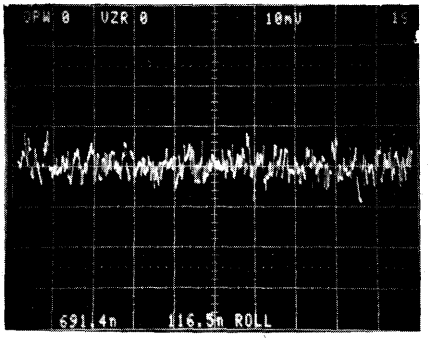


INPUT NOISE CURRENT DENSITY



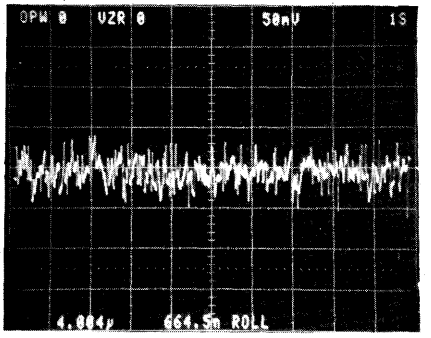
PEAK TO PEAK NOISE 0.1HZ TO 10HZ

p-p(RTI) = 691.4nV, rms(RTI) = 116.5nV, A_V = 25000



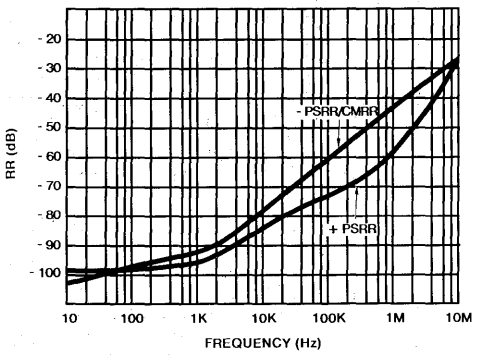
PEAK TO PEAK NOISE 0.1HZ TO 1MHZ

p-p(RTI) = 4.004µV, rms(RTI) = 664.5nV, A_V = 25000



REJECTION RATIOS vs FREQUENCY

$A_V = \pm 10$, V_{IN} = 300mVrms



HARRIS HA-2600/02/05

May 1990

Wideband, High Impedance Operational Amplifiers

Features

- Wide Bandwidth 12MHz
- High Input Impedance 500MΩ
- Low Input Bias Current 1nA
- Low Input Offset Current 1nA
- Low Input Offset Voltage 0.5mV
- High Gain 150kV/V
- High Slew Rate 7V/μs
- Output Short Circuit Protection
- Unity Gain Stable

Applications

- Video Amplifier
- Pulse Amplifier
- Audio Amplifiers and Filters
- High-Q Active Filters
- High-Speed Comparators
- Low Distortion Oscillators

Description

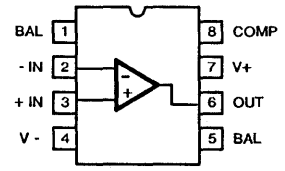
HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth, 7V/μs slew rate and 150kV/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characteristics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators. For more information, please refer to Application Note 515.

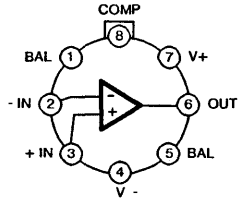
The HA-2600 and HA-2602 have guaranteed operation from -55°C to +125°C and are available in Metal Can and Ceramic Mini-DIP packages. Both are offered as /883 Military Grade; product and data sheets are available upon request. The HA-2605 has guaranteed operation from 0°C to +75°C and is available in Plastic and Ceramic Mini-DIP and Metal Can packages. SOIC packaging is also available for the HA-2605 with guaranteed operation from 0°C to +70°C (-5) and -40°C to +85°C (-9).

Pinouts

HA9P2605 (SOIC)
HA7-2600/02/05 (CERAMIC MINI-DIP)
HA3-2605 (PLASTIC MINI-DIP)
TOP VIEW

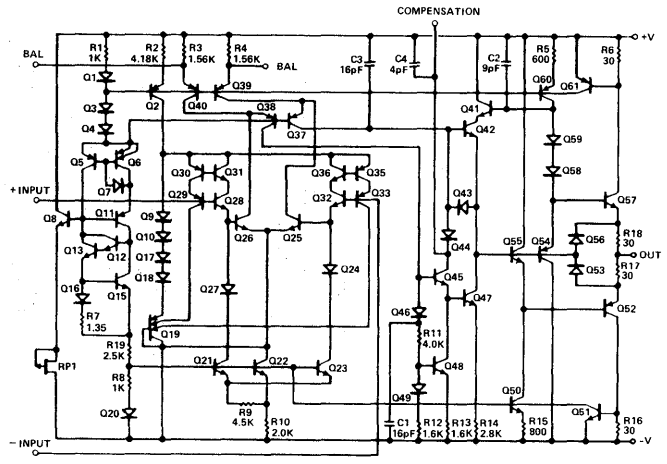


HA2-2600/02/05 (TO-99 METAL CAN)
TOP VIEW



NOTE: VCASE = V-

Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 13)

Voltage Between V+ and V- Terminals 45.0V
Differential Input Voltage..... ±12.0V
Peak Output Current ..... Full Short Circuit Protection
Internal Power Dissipation 300mW
Maximum Junction Temperature..... +175°C

Operating Temperature Ranges

HA-2600/HA-2602.....$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-2605-5..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
HA-2605-9..... $-40^{\circ}C \leq T_A \leq +85^{\circ}C$
Storage Temperature Range .....$-65^{\circ}C \leq T_A \leq +150^{\circ}C$
Lead Solder Temperature (10 Seconds) ..... +275°C

Electrical Specifications V_S = ±15V D.C., Unless Otherwise Specified.

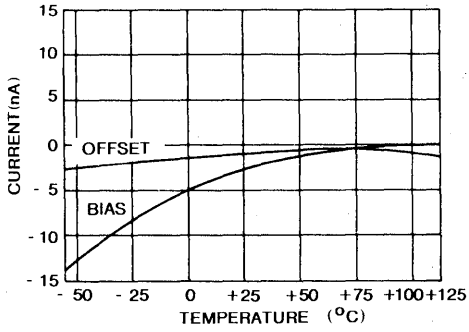
PARAMETER	TEMP	HA-2600-2 MIN	HA-2600-2 TYP	HA-2600-2 MAX	HA-2602-2 MIN	HA-2602-2 TYP	HA-2602-2 MAX	HA-2605-5 MIN	HA-2605-5 TYP	HA-2605-5 MAX	(NOTE 15) HA-2605-9 MAX	UNITS
INPUT CHARACTERISTICS												
Offset Voltage	+25°C	-	0.5	4	-	3	5	-	3	5	5	mV
	Full	-	2	6	-	-	7	-	-	7	7	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	-	5	-	-	µV/°C
Bias Current	+25°C	-	1	10	-	15	25	-	5	25	25	nA
	Full	-	10	30	-	-	60	-	-	40	70	nA
Offset Current	+25°C	-	1	10	-	5	25	-	5	25	25	nA
	Full	-	5	30	-	-	60	-	-	40	70	nA
Differential Input Resistance (Note 10)	+25°C	100	500	-	40	300	-	40	300	-	-	MΩ
Input Noise Voltage Density f_O = 1kHz	+25°C	-	11	-	-	11	-	-	11	-	-	$nV/\sqrt{Hz}$
Input Noise Current Density f_O = 1kHz	+25°C	-	0.16	-	-	0.16	-	-	0.16	-	-	$pA/\sqrt{Hz}$
Common Mode Range	Full	±11	±12	-	±11	±12	-	±11	±12	-	-	V
TRANSFER CHARACTERISTICS												
Large Signal Voltage Gain (Notes 1, 4)	+25°C	100K	150K	-	80K	150K	-	80K	150K	-	-	V/V
	Full	70K	-	-	60K	-	-	70K	-	-	-	V/V
Common Mode Rejection Ratio (Note 2)	Full	80	100	-	74	100	-	74	100	-	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	1	-	-	-	V/V
Gain Bandwidth Product (Note 3)	+25°C	-	12	-	-	12	-	-	12	-	-	MHz
OUTPUT CHARACTERISTICS												
Output Voltage Swing (Note 1)	Full	±10	±12	-	±10	±12	-	±10	±12	-	-	V
Output Current (Note 4)	+25°C	±15	±22	-	±10	±18	-	±10	±18	-	-	mA
Full Power Bandwidth (Notes 4, 11)	+25°C	50	75	-	50	75	-	50	75	-	-	kHz
TRANSIENT RESPONSE (Note 8)												
Rise Time (Notes 1, 5, 6 & 7)	+25°C	-	30	60	-	30	60	-	30	60	60	ns
Overshoot (Notes1, 5, 6 & 7)	+25°C	-	25	40	-	25	40	-	25	40	40	%
Slew Rate (Notes 1, 5, 7 & 12)	+25°C	±4	±7	-	±4	±7	-	±4	±7	-	-	V/µs
Settling Time (Notes 1, 5 & 14)	+25°C	-	1.5	-	-	1.5	-	-	1.5	-	-	µs
POWER SUPPLY CHARACTERISTICS												
Supply Current	+25°C	-	3	3.7	-	3	4	-	3	4	4	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90	-	74	90	-	74	90	-	-	dB

NOTES:

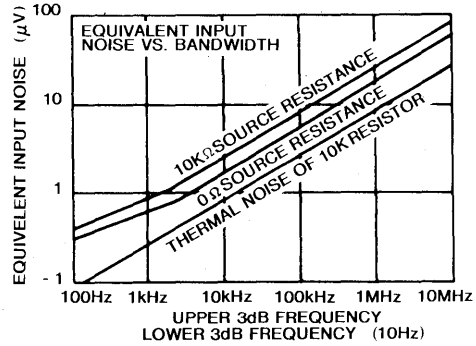
1. R_L = 2kΩ
2. V_{CM} = ±10V
3. V_{OUT} < 90mV
4. V_{OUT} = ±10V
5. C_L = 100pF
6. V_{OUT} = ±200mV
7. A_V = +1
8. See Transient Response Test Circuits & Waveforms.
9. ΔV_S = ±5V
10. This parameter value guaranteed by design calculations.
11. Full Power Bandwidth guaranteed by slew rate measurement: FPBW = S.R./$2\pi V_{PEAK}$.
12. V_{OUT} = ±5V
13. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
14. Settling time is characterized at A_V = -1 to 0.1% of a 10 Volt step.
15. Typical and minimum specifications for -9 are identical to those of -5.

Typical Performance Curves $V_S = \pm 15V$ D.C., $T_A = +25^oC$, Unless Otherwise Specified.

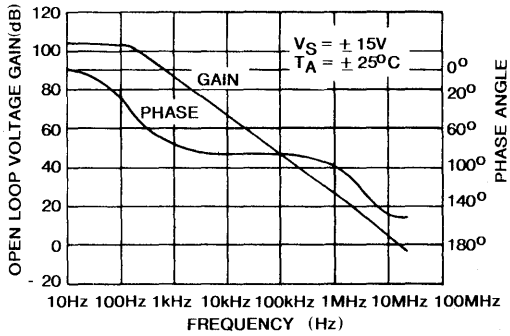
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



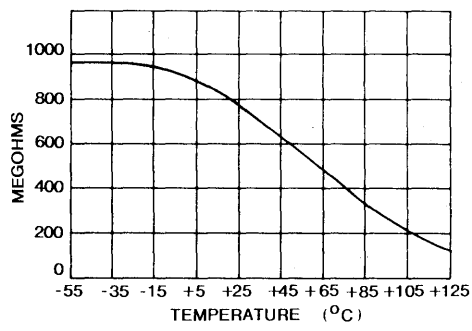
BROADBAND NOISE CHARACTERISTICS



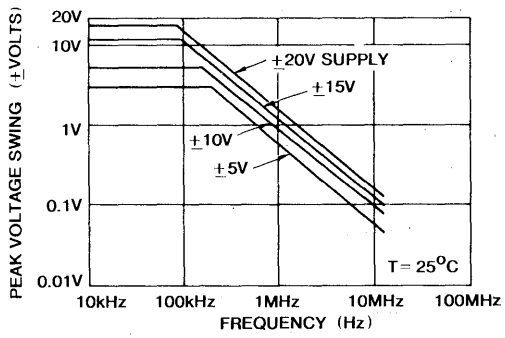
OPEN LOOP FREQUENCY AND PHASE RESPONSE



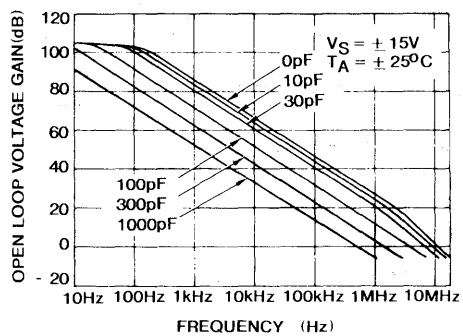
INPUT IMPEDANCE vs. TEMPERATURE, 100Hz



OUTPUT VOLTAGE SWING vs. FREQUENCY



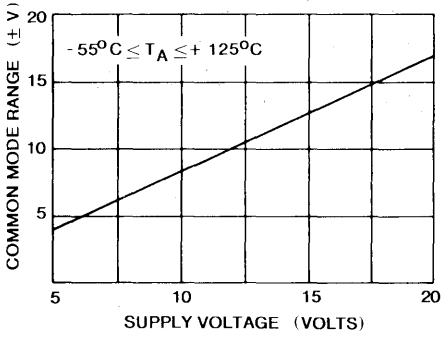
OPEN-LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND



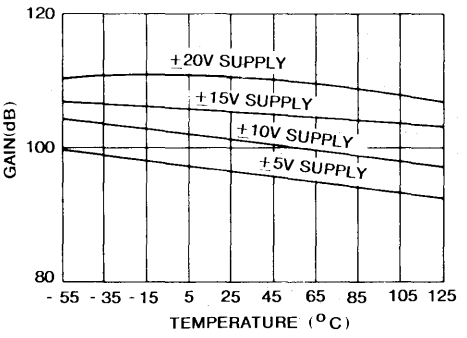
NOTE: External Compensation Components are not required for stability, but may be added to reduce bandwidth if desired. If External Compensation is used, also connect 100pF capacitor from output to ground.

Typical Performance Curves (Continued)

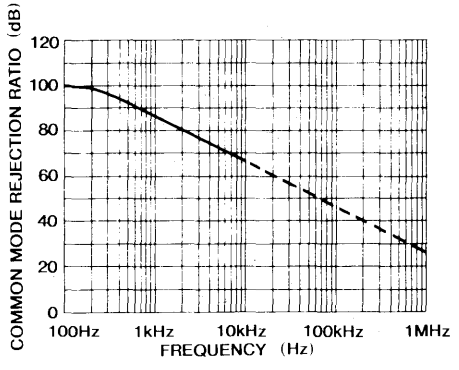
COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



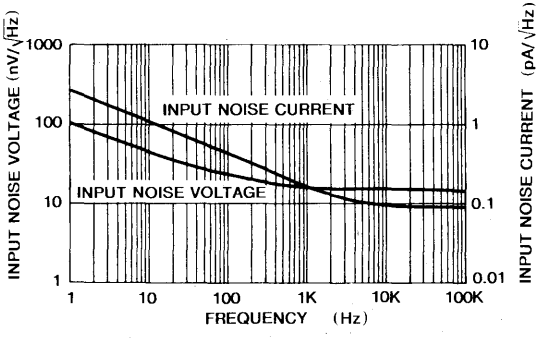
OPEN - LOOP VOLTAGE GAIN vs. TEMPERATURE



COMMON MODE REJECTION RATIO vs. FREQUENCY

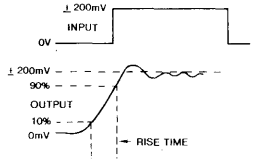


NOISE DENSITY vs. FREQUENCY

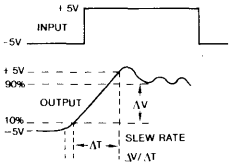


Test Circuits

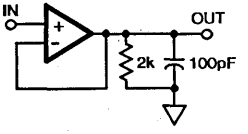
TRANSIENT RESPONSE



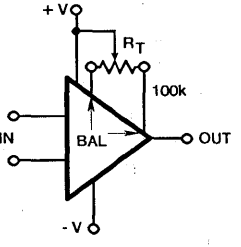
SLEW RATE



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK-UP

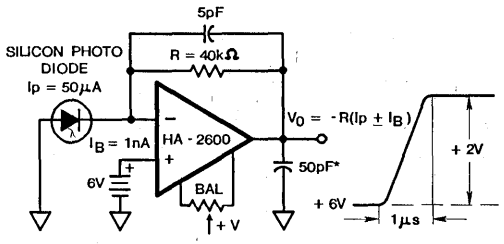


NOTE: Measured on both positive and negative transistions from 0 to +200mV and 0 to -200mV at output.

Tested Offset Adjustment is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is ±10mV with $R_T = 100k\Omega$.

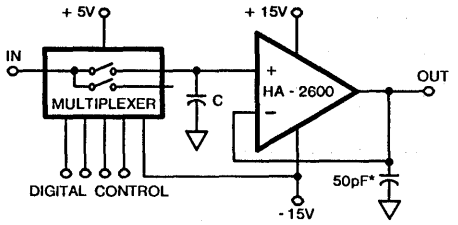
Typical Applications

PHOTO-CURRENT TO VOLTAGE CONVERTER



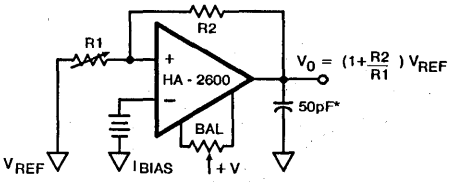
FEATURES:
1. Constant cell voltage
2. Minimum bias current error

SAMPLE-AND-HOLD



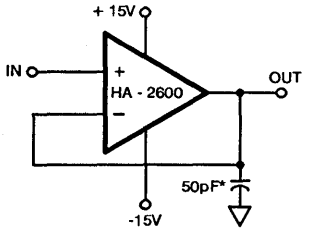
Drift rate $\frac{I_{bias}}{C}$ If C = 1000pF
Drift = 0.01V/ms Max.

REFERENCE VOLTAGE AMPLIFIER



FEATURES:
1. Minimum bias current in reference cell
2. Short circuit protection

VOLTAGE FOLLOWER



Z_{IN} = 10^{12} Min.
Z_{OUT} = 0.01 Max. B.W. = 12MHz Typ.
Slew Rate = 4V/μs Min. Output Swing = ±10V Min. to 50kHz

* A small load capacitance is recommended in all applications where practical to prevent possible high frequency oscillations resulting from external wiring parasitics. Capacitance up to 100pF has negligible effect on the bandwidth or slew rate.

Die Characteristics

Transistor Count 140
Die Dimensions ..... 73 x 52 x 19 mils
Substrate Potential ..... Unbiased

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-Metal Can (-2, -5, -7)	202	55
HA2-Metal Can (-8, /883)	161	48
HA3-Plastic DIP (-5)	83	33
HA4-Ceramic LCC (/883)	96	35
HA7-Ceramic DIP (-2, -5, -7)	204	112
HA7-Ceramic DIP (-8, /883)	81	32
HA9P-SOIC-(-5, -9)	160	42

HARRIS HA-2620/22/25

May 1990

Very Wideband, Uncompensated Operational Amplifiers

Features

- Gain Bandwidth Product ($A_V \geq 5$) 100MHz
- High Input Impedance 500MΩ
- Low Input Bias Current 1nA
- Low Input Offset Current 1nA
- Low Input Offset Voltage 0.5mV
- High Gain 150kV/V
- High Slew Rate 35V/μs
- Output Short Circuit Protection

Applications

- Video and R.F. Amplifier
- Pulse Amplifier
- Audio Amplifiers and Filters
- High-Q Active Filters
- High-Speed Comparators
- Low Distortion Oscillators

Description

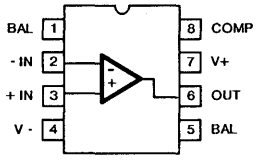
HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500MΩ, HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 100MHz gain-bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/μs slew rate and 150kV/V open-loop gain enables HA-2620/2622/2625 to perform high-gain amplification of very fast, wideband signals. These dynamic characteristics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs, HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators. For more information, please refer to Application Notes 509, 519 and 546.

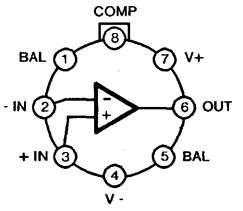
The HA-2620 and HA-2622 have guaranteed operation from -55°C to +125°C and are available in Metal Can and Ceramic Mini-DIP packages. Both are offered as /883 Military Grade with the HA-2622 also available in LCC packages. MIL-STD-883 data sheets are available upon request. The HA-2625 has guaranteed operation from 0°C to +75°C and is available in Plastic and Ceramic Mini-DIP and Metal Can packages. Additionally the HA-2625 is available in SOIC packaging with -5 and -9 temperature grades.

Pinouts

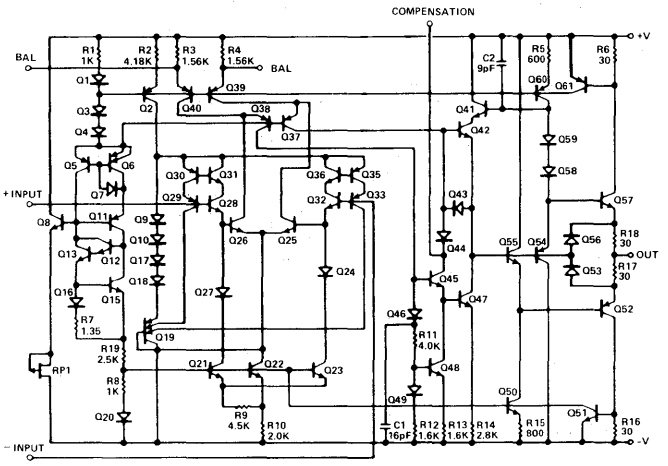
HA9P2625 (SOIC)
HA7-2620/22/25 (CERAMIC MINI-DIP)
HA3-2625 (PLASTIC MINI-DIP)
TOP VIEW



HA2-2620/22/25 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 13)

Voltage Between V+ and V- Terminals 45.0V
Differential Input Voltage..... ±12.0V
Peak Output Current ..... Full Short Circuit Protection
Internal Power Dissipation 300mW
Maximum Junction Temperature..... +175°C

Operating Temperature Ranges

HA-2620/HA-2622.....$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-2625-5..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
HA-2625-9..... $-40^{\circ}C \leq T_A \leq +80^{\circ}C$
Storage Temperature Range:.....$-65^{\circ}C \leq T_A \leq +150^{\circ}C$
Lead Solder Temperature (10 Seconds) ..... 275°C

Electrical Specifications V_S = ±15V D.C., Unless Otherwise Specified.

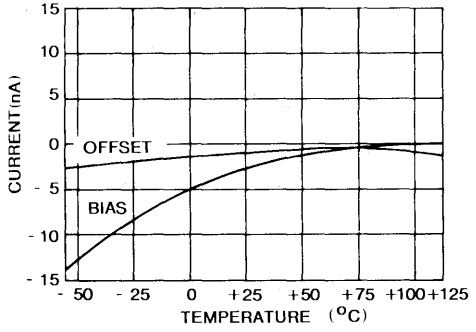
PARAMETER	TEMP	HA-2620			HA-2622			HA-2625-5, -9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage (Note 1)	+25°C	-	0.5	4	-	3	5	-	3	5	mV
	Full	-	2	6	-	-	7	-	-	7	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	-	5	-	µV/°C
Bias Current	+25°C	-	1	15	-	5	25	-	5	25	nA
	Full	-	10	35	-	-	60	-	-	40	nA
Offset Current	+25°C	-	1	15	-	5	25	-	5	25	nA
	Full	-	5	35	-	-	60	-	-	40	nA
Differential Input Resistance (Note 11)	+25°C	65	500	-	40	300	-	40	300	-	MΩ
Input Noise Voltage Density f_O = 1kHz	+25°C	-	11	-	-	11	-	-	11	-	$nV/\sqrt{Hz}$
Input Noise Current Density f_O = 1kHz	+25°C	-	0.16	-	-	0.16	-	-	0.16	-	$pA/\sqrt{Hz}$
Common Mode Range	Full	±11	±12	-	±11	±12	-	±11	±12	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Notes 2 & 3)	+25°C	100K	150K	-	80K	150K	-	80K	150K	-	V/V
	Full	70K	-	-	60K	-	-	70K	-	-	V/V
Common Mode Rejection Ratio (Note 4)	Full	80	100	-	74	100	-	74	100	-	dB
Minimum Stable Gain	+25°C	5	-	-	5	-	-	5	-	-	V/V
Gain Bandwidth Product (Notes 2, 5 & 6)	+25°C	-	100	-	-	100	-	-	100	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current (Note 3)	+25°C	±15	±22	-	±10	±18	-	±10	±18	-	mA
Full Power Bandwidth (Notes 2, 3, 7 & 12)	+25°C	400	600	-	320	600	-	320	600	-	kHz
TRANSIENT RESPONSE (Note 8)											
Rise Time (Notes 2, 7 & 8)	+25°C	-	17	45	-	17	45	-	17	45	ns
Slew Rate (Notes 2, 7, 8 & 10)	+25°C	±25	±35	-	±20	±35	-	±20	±35	-	V/µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C	-	3	3.7	-	3	4	-	3	4	mA
Power Supply Rejection Ratio (Note 9)	Full	80	90	-	74	90	-	74	90	-	dB

NOTES:

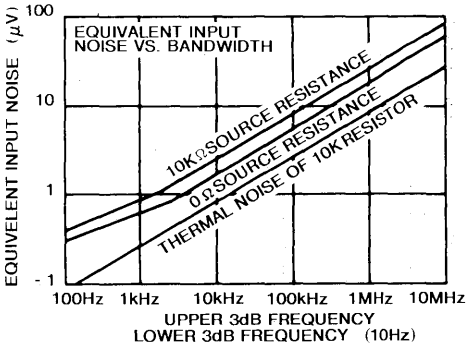
1. Offset may be externally adjusted to zero.
2. $R_L = 2k\Omega$
3. $V_{OUT} = \pm 10.0V$
4. $V_{CM} = \pm 10V$
5. $V_{OUT} < 90mV$
6. 40dB Gain
7. See Transient Response Test Circuits & Waveforms.
8. $A_V = 5$ (The HA-2620 family is not stable at unity gain without external compensation.)
9. $\Delta V_S = \pm 5V$
10. $V_{OUT} = \pm 5V$
11. This parameter value guaranteed by design calculations.
12. Full Power Bandwidth guaranteed by slew rate measurement: $FPBW = S.R./2\pi V_{PEAK}$.
13. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

Typical Performance Curves $V_S = \pm 15V$ D.C., $T_A = +25^oC$, Unless Otherwise Specified.

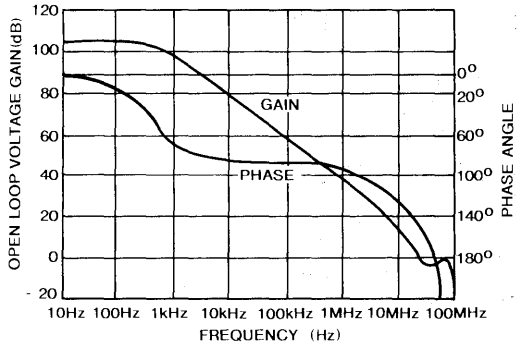
INPUT BIAS CURRENT AND OFFSET CURRENT AS A FUNCTION OF TEMPERATURE



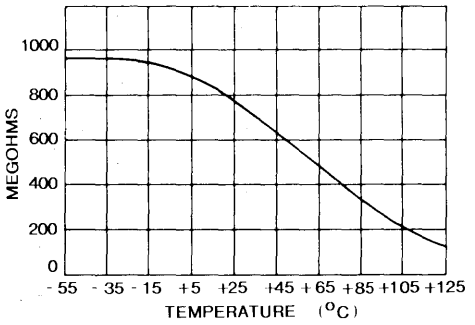
BROADBAND NOISE CHARACTERISTICS



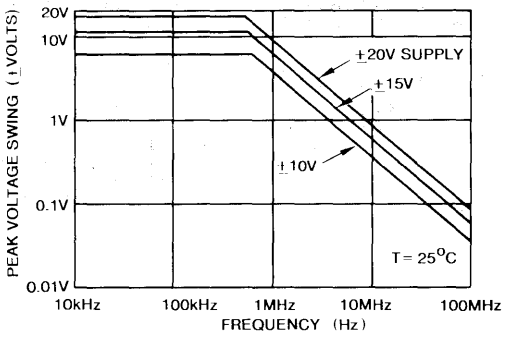
OPEN LOOP FREQUENCY AND PHASE RESPONSE



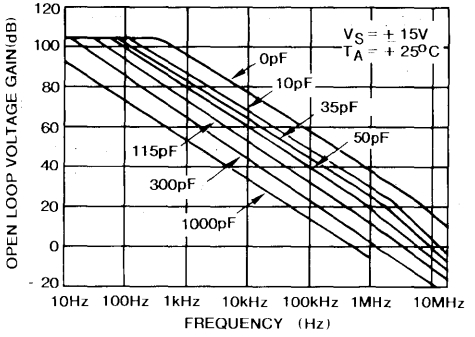
INPUT IMPEDANCE vs. TEMPERATURE, 100Hz



OUTPUT VOLTAGE SWING vs. FREQUENCY



OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND

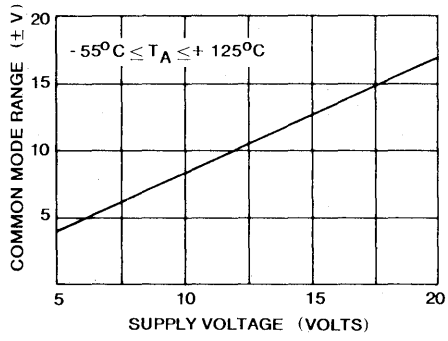


NOTE: External Compensation is required for closed loop gain < 5. If external compensation is used, also connect 100pF capacitor from output to ground.

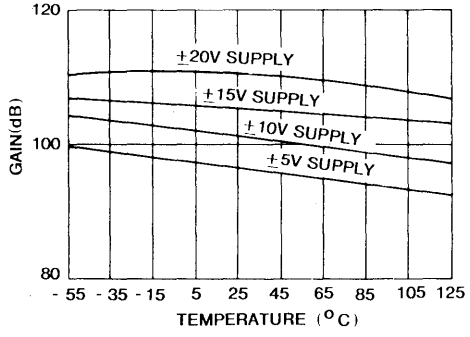
3 OPERATIONAL AMPLIFIERS

Typical Performance Curves (Continued)

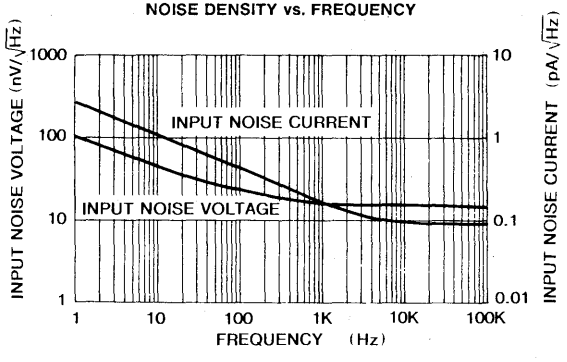
COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



OPEN LOOP VOLTAGE GAIN vs. TEMPERATURE

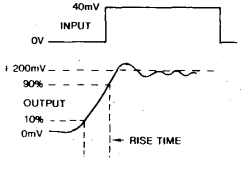


NOISE DENSITY vs. FREQUENCY

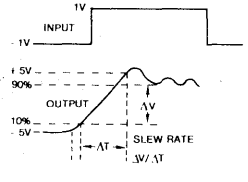


Test Circuits

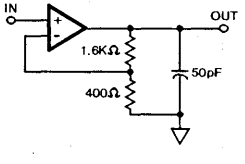
TRANSIENT RESPONSE



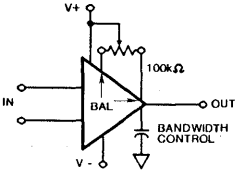
SLEW RATE



SLEW RATE AND TRANSIENT RESPONSE



SUGGESTED V_{OS} ADJUSTMENT AND COMPENSATION HOOK-UP

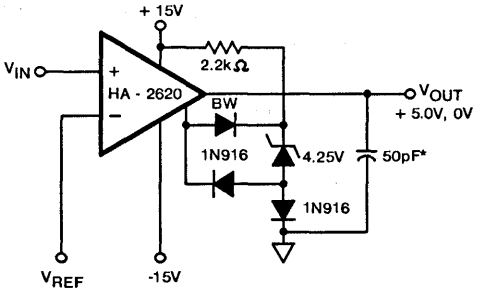


NOTE: Measured on both positive and negative transistions from 0 to +200mV and 0 to -200mV at output.

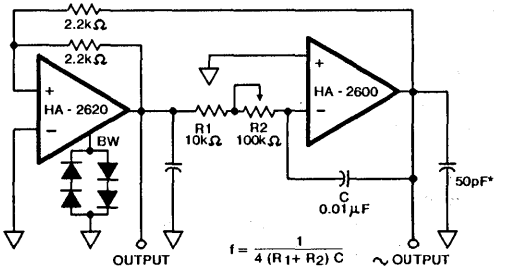
Tested Offset Adjustment is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is ±10mV with $R_T = 100k\Omega$.

Typical Applications

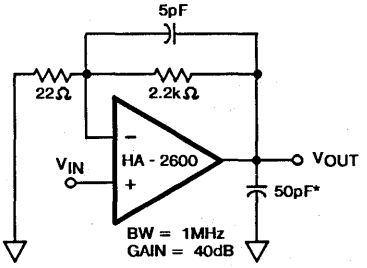
HIGH IMPEDANCE COMPARATOR



FUNCTION GENERATOR



VIDEO AMPLIFIER



* A small load capacitance of at least 30pF (including stray capacitance) is recommended to prevent possible high frequency oscillations.

Die Characteristics

Transistor Count 140
Die Dimensions ..... 73 x 52 x 19 mils
Substrate Potential ..... Unbiased

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-Metal Can (-2, -5, -7)	202	55
HA2-Metal Can (-8, /883)	161	48
HA3-Plastic DIP (-5)	83	33
HA4-Ceramic LCC (/883)	96	35
HA7-Ceramic DIP (-2, -5, -7)	204	112
HA7-Ceramic DIP (-8, /883)	81	32

HARRIS

HA-2640/45

High Voltage Operational Amplifiers

July 1990

Features

- Output Voltage Swing ..... ±35V
- Supply Voltage ..... ±10V to ±40V
- Offset Current 5nA
- Bandwidth 4MHz
- Slew Rate 5V/µs
- Common Mode Input Voltage Swing ..... ±35V
- Output Overload Protection

Applications

- Industrial Control Systems
- Power Supplies
- High Voltage Regulators
- Resolver Excitation
- Signal Conditioning

Description

HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

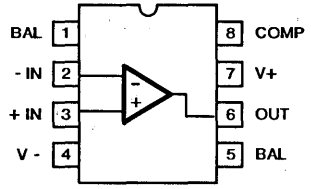
For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

These amplifiers deliver ±35V common mode input voltage swing, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and 5V/µs slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excellent components for resolver excitation designs.

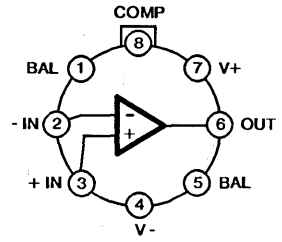
The HA-2640/2645 are available in Metal Can (TO-99) or Ceramic Mini-DIP and can be used as high performance pin-for-pin replacements for many general performance amplifiers. HA-2640 is specified from -55°C to +125°C and HA-2645 is specified over the 0°C to +75°C range.

Pinouts

HA7-2640/2645 (CERAMIC MINI-DIP)
TOP VIEW

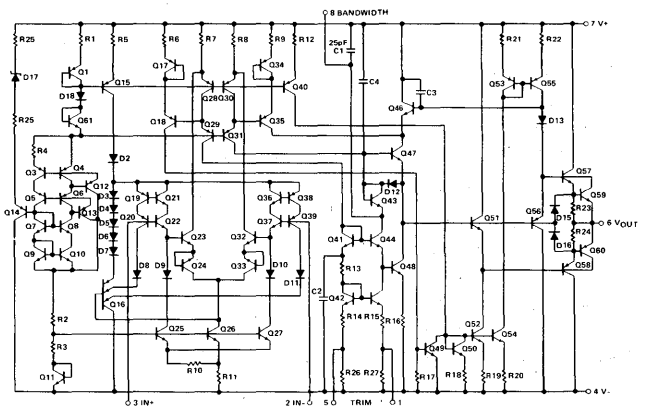


HA2-2640/2645 (TO-99 METAL CAN)
TOP VIEW



(TO-99 Case Voltage = -V)

Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 12)

Voltage Between V+ and V- Terminals 100V
Input Voltage Range ..... ±10V to ±37V
Output Current ..... Full Short Circuit Protection
Internal Power Dissipation ..... 680mW *
Maximum Junction Temperature ..... +175°C
* Derate by 4.6mW/°C above +25°C

Operating Temperature Ranges

HA-2640 ..... $-55°C \leq T_A \leq +125°C$
HA-2645 ..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$

Electrical Specifications $V_{SUPPLY} = \pm 40V$, $R_L = 5k\Omega$, Unless Otherwise Specified.

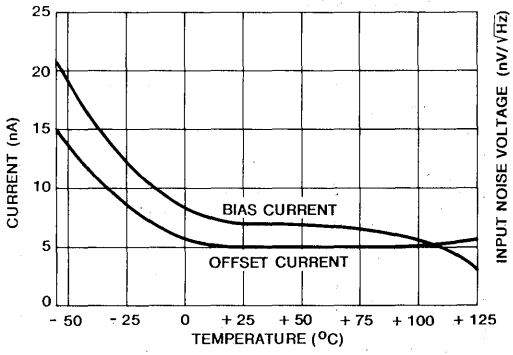
PARAMETER	TEMP	HA-2640 -55°C to +125°C			HA-2645 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	2	4	-	2	6	mV
	Full	-	-	6	-	-	7	mV
Average Offset Voltage Drift	Full	-	15	-	-	15	-	µV/°C
Bias Current	+25°C	-	10	25	-	12	30	nA
	Full	-	-	50	-	-	50	nA
Offset Current	+25°C	-	5	12	-	15	30	nA
	Full	-	-	35	-	-	50	nA
Input Resistance (Note 10)	+25°C	50	250	-	40	200	-	MΩ
Common Mode Range	Full	±35	-	-	±35	-	-	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 8)	+25°C	100K	200K	-	100K	200K	-	V/V
	Full	75K	-	-	75K	-	-	V/V
Common Mode Rejection Ratio (Note 1)	Full	80	100	-	74	100	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	V/V
Unity Gain Bandwidth (Note 2)	+25°C	-	4	-	-	4	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	±35	-	-	±35	-	-	V
Output Current (Note 9)	+25°C	±12	±15	-	±10	±12	-	mA
Output Resistance	+25°C	-	500	-	-	500	-	Ω
Full Power Bandwidth (Notes 3 & 11)	+25°C	-	23	-	-	23	-	kHz
TRANSIENT RESPONSE (Note 7)								
Rise Time (Notes 4 & 6)	+25°C	-	60	100	-	60	100	ns
Overshoot (Notes 4 & 6)	+25°C	-	15	30	-	15	40	%
Slew Rate (Note 6)	+25°C	±3	±5	-	±2.5	±5	-	V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	3.2	3.8	-	3.2	4.5	mA
Supply Voltage Range	Full	±10	-	±40	±10	-	±40	V
Power Supply Rejection Ratio (Note 5)	Full	80	90	-	74	90	-	dB

NOTES:

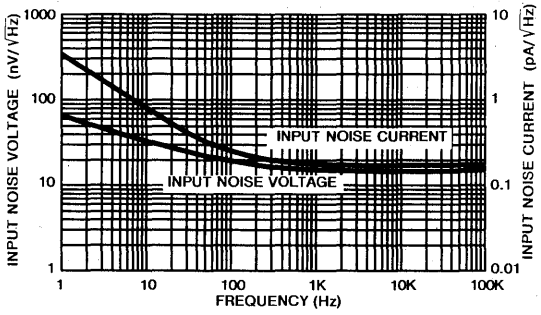
1. $V_{CM} = \pm 20V$
2. $V_{OUT} = 90mV$
3. $V_{OUT} = \pm 35V$
4. $V_{OUT} = \pm 200mV$
5. $V_S = \pm 10V$ to $\pm 40V$
6. $A_V = +1$
7. $C_L = 50pF$, $R_L = 5k\Omega$
8. $V_{OUT} = \pm 30V$
9. $R_L = 1k\Omega$
10. This parameter based upon design calculations.
11. Full Power Bandwidth guaranteed based upon slew rate measurement: $FPBW = S.R./2\pi V_{PEAK}$.
12. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

Typical Performance Curves V+ = V- = 40V D.C., T_A = +25°C, Unless Otherwise Specified.

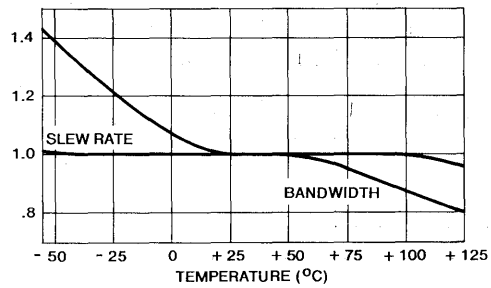
INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



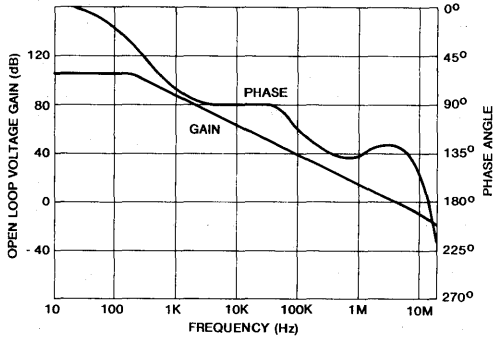
INPUT NOISE CHARACTERISTICS



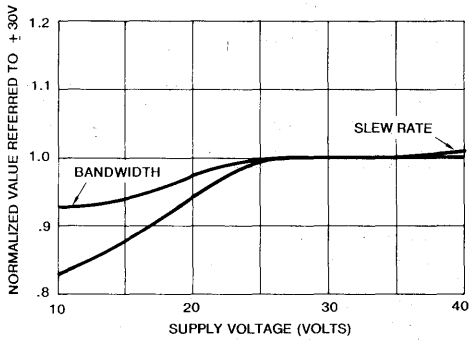
NORMALIZED AC PARAMETERS vs. TEMPERATURE



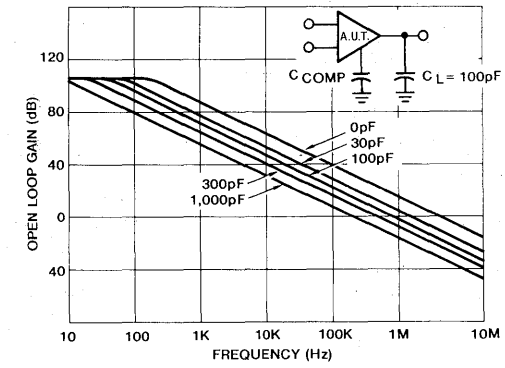
OPEN LOOP FREQUENCY AND PHASE RESPONSE



NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE AT +25°C



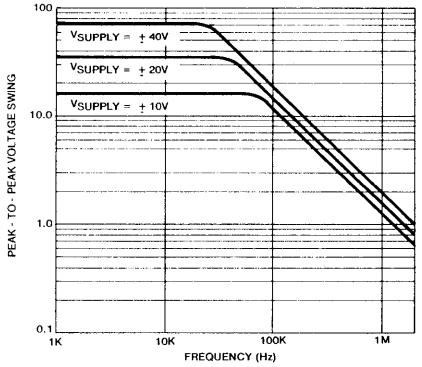
OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS VALUES OF CAPACITORS FROM COMPENSATION PIN TO GROUND



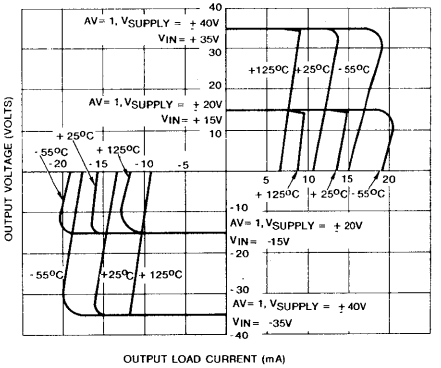
NOTE: External Compensation Components are not required for stability, but may be added to reduce bandwidth if desired. If External Compensation is used, also connect 100pF capacitor from output to ground.

Typical Performance Curves (Continued)

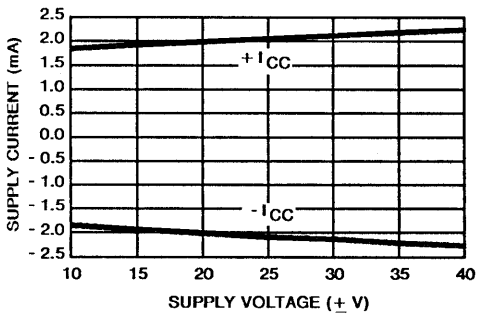
OUTPUT VOLTAGE SWING vs. FREQUENCY AT +25°C



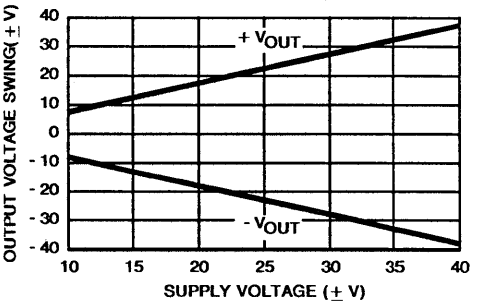
OUTPUT CURRENT CHARACTERISTIC



SUPPLY CURRENT vs. SUPPLY VOLTAGE



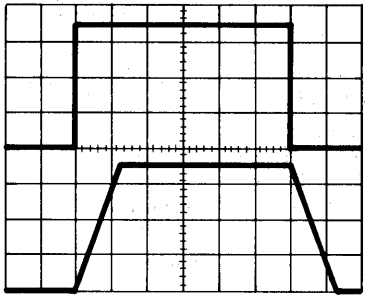
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE



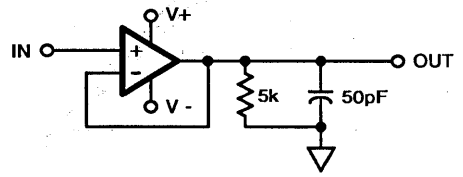
Switching Waveform and Test Circuits

VOLTAGE FOLLOWER PULSE RESPONSE

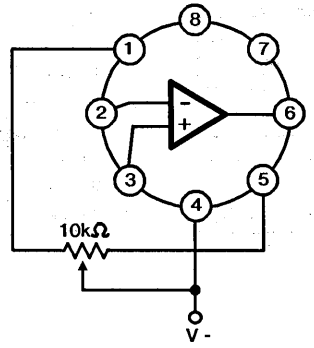
R_L = 5K, C_L = 50pF T_A = +25°C
Vertical = 10V/Div. V_S = ±40V
Horizontal = 5µs/Div.



SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



SUGGESTED V_{OS} ADJUSTMENT



Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ minimum referred to output. Typical range is ±20mV with R_T = 10kΩ.

HARRIS

HA-2650/55

Dual High Performance Operational Amplifier

February 1990

Features

- Slew Rate 5V/μs
- Bandwidth 8MHz
- Bias Current 35nA
- Avg. Offset Voltage Drift ..... 8μV/°C
- Power Consumption 75mW
- Supply Voltage Range ..... ±2V TO ±20V

Applications

- Video Amplifiers
- High Impedance, Wideband Buffers
- Integrators
- Audio Amplifiers
- Active Filters

Description

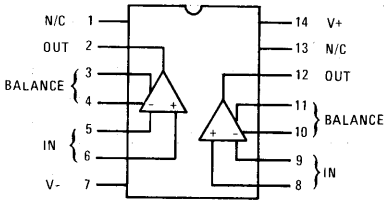
HA-2650/2655 contains two internally compensated operational amplifiers offering high slew rate and high frequency performance combined with exceptional DC characteristics. 5V/μsec slew rate and 8MHz bandwidth make these amplifiers suitable for processing fast, wideband signals extending into the video frequency spectrum. Signal processing accuracy is enhanced by front-end performance that includes 1.5mV offset voltage, 8μV/°C offset voltage drift and low offset and bias current (1nA and 35nA respectively). Offset voltage can be trimmed to zero on the devices offered in dual-in-line packages. Signal conditioning is further enhance by 500MΩ input impedance.

Applications for HA-2650/2655 include video circuit designs such as high impedance buffers, integrators, tone generators and filters. These amplifiers are also ideal components for active filtering of audio and voice signals.

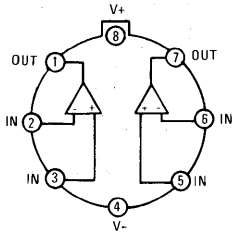
HA-2650/2655 are offered in 14 pin DIP and metal TO-99 packages and are also available in dice form. HA-2650 is specified from -55°C to +125°C. HA-2655 operates from 0°C to +75°C.

Pinouts

HA1-2650/2655 (CERAMIC DIP)
TOP VIEW

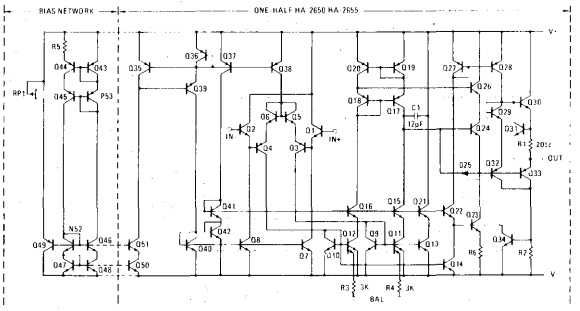


HA2-2650/2655 (TO-99 METAL CAN)
TOP VIEW



NOTE: Case Connected to V-

Schematic



3

OPERATIONAL AMPLIFIERS

Absolute Maximum Ratings (Note 1)

T_A = +25°C, Unless Otherwise Specified
Voltage Between V+ and V- Terminals 40V
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±15V
Output Short Circuit Duration ..... Indefinite
Power Dissipation (Note 2) TO-99 ..... 300mW

Operating Temperature Ranges

HA-2650 ..... -55°C ≤ TA ≤ +125°C
HA-2655 ..... 0°C ≤ TA ≤ +75°C
Storage Temperature Range ..... -65°C ≤ TA ≤ +150°C

Electrical Specifications

V+ = +15V D.C., V- + -15V D.C.

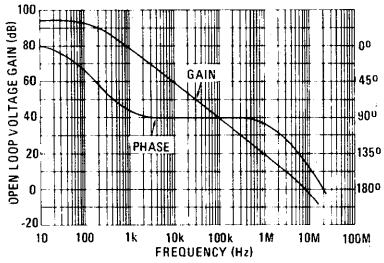
PARAMETER	TEMP.	HA-2650 -55°C to +125°C MIN.	TYP.	MAX.	HA-2655 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C Full		1.5	3 5		2	5 7	mV mV
Avg. Offset voltage Drift	Full		8			8		µV/°C
Bias Current	+25°C Full		35	100 200		50	200 300	nA nA
Offset Current	+25°C Full		1	30 60		2	60 100	nA nA
Common Mode Range	Full	±13			±13			V
Differential Input Resistance (Note 9)	+25°C	5	20		5	20		MΩ
Common Mode Input Resistance	+25°C		500			500		MΩ
Input Capacitance	+25°C		5			5		pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 3ab)	+25°C Full	20K 15K	40K		15K 10K	40K		V/V V/V
Common Mode Rejection Ratio (Note 4)	+25°C Full	80 80	100		74 74	100		dB dB
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3c)	+25°C Full	±13 ±13	±14		±13 ±13	±14		V V
Full Power Bandwidth (Notes 5 & 10)	+25°C	30	80		30	80		KHz
Output Current (Note 3a)	+25°C		±20			±18		mA
Output Resistance	+25°C		100			100		Ω
TRANSIENT RESPONSE (Note 6)								
Rise Time (Note 7)	+25°C		40	80		40	90	ns
Overshoot (Note 7)	+25°C		15	40		15	40	%
Slew Rate	+25°C	±2	±5		±2	±5		V/µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		2.5	4		3	5	mA
Power Supply Rejection Ratio (Note 8)	+25°C Full	80 80	100		74 74	100		dB dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above +110°C.
3. (a) V_O = ±10V (b) R_L = 2K (c) R_L = 10K
4. V_{CM} = ±5.0V
5. A_V = 1, R_L = 2K, V_O = $20V_{pp}$
6. See transient response/slew rate circuit.
7. V_{IN} = 200mV
8. Δ V = ±5.0V
9. This parameter value based upon design calculations
10. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./$2\pi V_{peak}$.

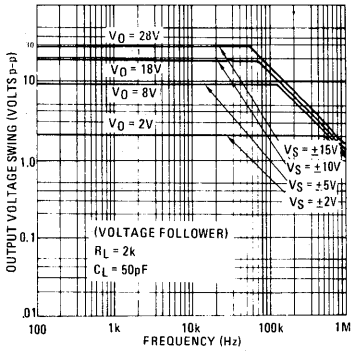
Typical Performance Curves

V+ = +15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified

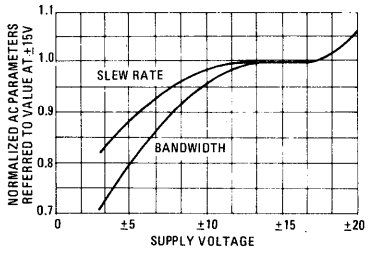
OPEN LOOP FREQUENCY RESPONSE



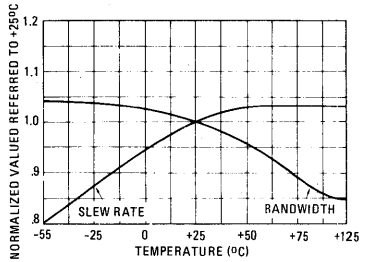
OUTPUT VOLTAGE SWING vs FREQUENCY



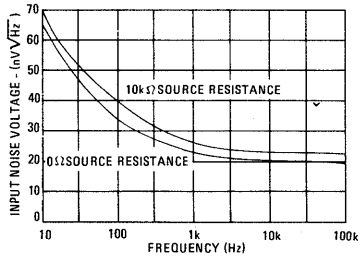
NORMALIZED AC PARAMETERS vs SUPPLY VOLTAGE



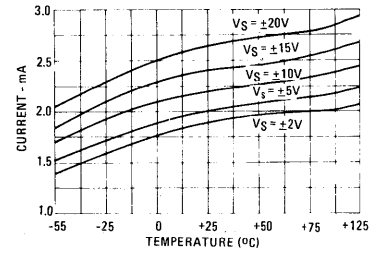
NORMALIZED AC PARAMETERS vs TEMPERATURE



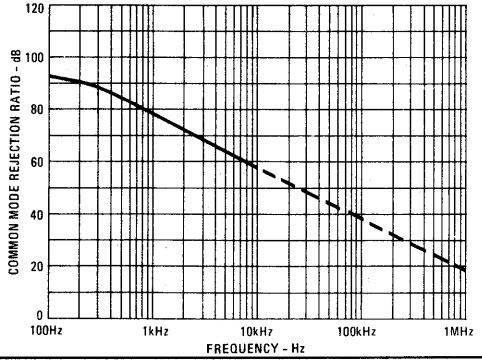
INPUT NOISE VOLTAGE vs FREQUENCY



POWER SUPPLY CURRENT vs TEMPERATURE

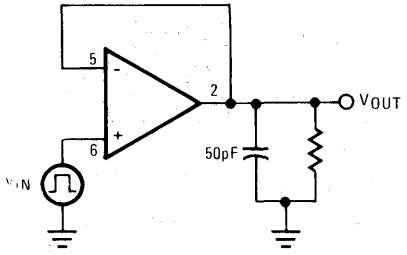


COMMON MODE REJECTION RATIO vs FREQUENCY

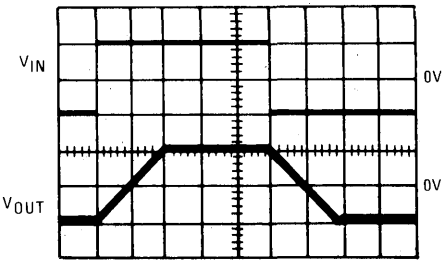


Test Circuits

TRANSIENT RESPONSE/SLEW RATE CIRCUIT



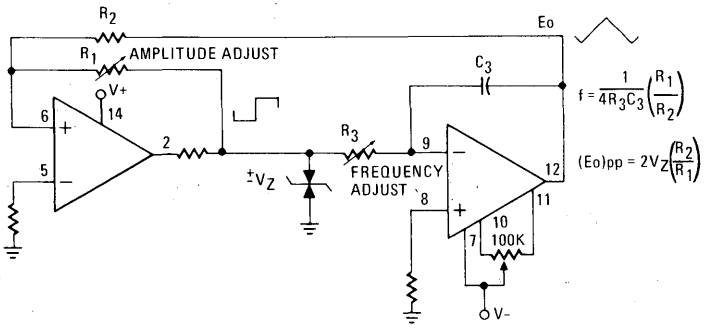
SLEWING WAVEFORM



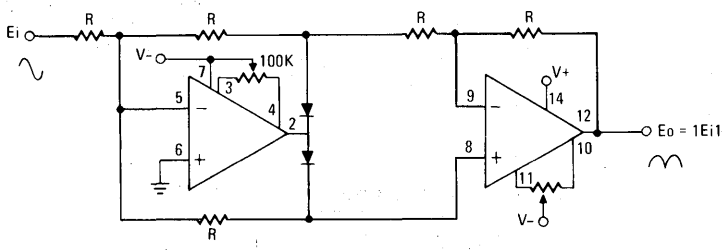
VERTICAL 5V/DIV. HORIZONTAL 1μs/DIV.

Typical Applications

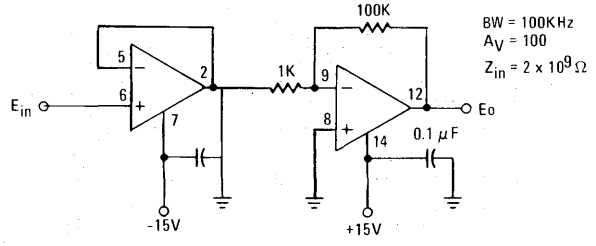
LOW COST HIGH FREQUENCY GENERATOR



ABSOLUTE - VALUE CIRCUIT



HIGH IMPEDANCE, HIGH GAIN, HIGH FREQUENCY INVERTING AMP



HARRIS

HA-2720/25

Wide Range Programmable Operational Amplifier

February 1990

Features

- Wide Programming Range
  - Slew Rate ..... 0.06 to 6V/μs
  - Bandwidth ..... 5KHz to 10MHz
  - Bias Current ..... 0.4 to 50nA
  - Supply Current ..... 1μA to 1.5mA
  - Power Consumption 75mW
  - Supply Voltage Range ..... ±2V to ±20V
- Wide Power Supply Range ..... ±1.2 to ±18V
- Constant AC Performance Over Supply Range

Applications

- Active Filters
- Current Controlled Oscillators
- Variable Active Filters
- Modulators
- Battery-Powered Equipment

Description

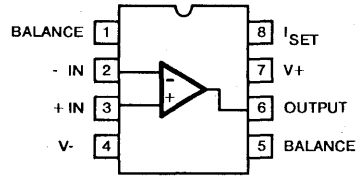
HA-2720/2725 programmable amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' 'set' current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables HA-2720/2725 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2720 and HA-2725 can, therefore, be utilized as the standard amplifier for a variety of designs simply of adjusting their programming current.

A major advantage of HA-2720/2725 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipment. A primary application for HA-2720/2725 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the 'set' current, HA-2720/2725 can be used for designs such as current controlled oscillators modulators, sample and hold circuits and variable active filters.

HA-2720 is guaranteed over -55°C to +125°C. HA-2725 is specified from 0°C to +75°C. Both parts are available in TO-99 cans or dice form.

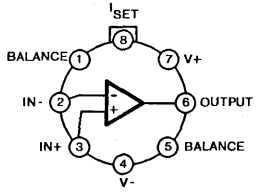
Pinouts

HA1-2720/2725 (CERAMIC MINI-DIP)
TOP VIEW

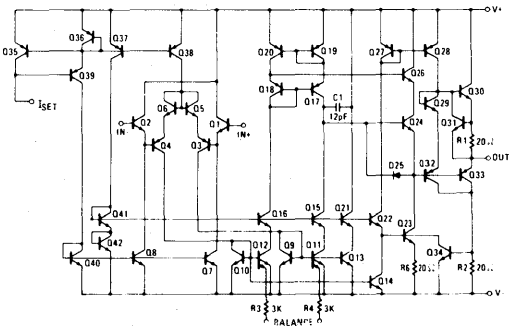


Note: Case tied to V-

HA2-2720/2655 (TO-99 METAL CAN)
TOP VIEW



Schematic



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 45V
Differential Input Voltage..... ±30V
Input Voltage (Note 1) ..... ±15V
I_{SET} (Current at I_{SET}) 500µA
V_{SET} (Voltage to GND at I_{SET}) ..... $V+ -2V \leq V_{SET} \leq V+$
Power Dissipation (Note 2) TO-99 ..... 300mW

Operating Temperature Ranges

HA-2720 .....$-55^oC \leq TA \leq +125^oC$
HA-2725 ..... $0^oC \leq TA \leq +75^oC$
Storage Temperature Range .....$-65^oC \leq TA \leq +150^oC$

Electrical Specifications

V+ = +3V D.C., V- + -3V.

		HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						
		I_{SET} = 1.5µA			I_{SET} = 15µA			I_{SET} = 1.5µA			I_{SET} = 15µA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
Offset Voltage	+25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
OffsetCurrent	+25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	+25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	+25°C		50			5			50			5		MΩ
Input Capacitance	+25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 9)	+25°C	15K	40K		15K	40K		15K	40K		15K	40K		V/V
	Full	15K			10K			10K			10K			V/V
Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	+25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±2.0			±2.0			±2.0			V
Output Current (Note 5)	+25°C		±0.2			±0.2			±0.2			±2.0		mA
Output Resistance	+25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	+25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	+25°C		2.5			0.25			2.5			0.25		µs
Overshoot (Note 6)	+25°C		5			10			5			10		%
Slew Rate (Note 7)	+25°C		0.07			0.70			0.07			0.70		V/µs
POWER SUPPLY CHARACTERISTICS														
Supply Current	+25°C		15			170			15			170		µA
	Full			25			250			25			250	µA
Power Supply Rejection Ratio (Note 8)	Full	80			80			76			76			dB

NOTES:

1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 6.8mW/°C for operation ambient temperatures above 75°C.

	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5µA	I_{SET} = 15µA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	←	A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF		→
7.	V_O = ±2.0v	V_O = ±10.0V	R_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

10. This parameter based upon design calculations.

Electrical Specifications (Continued) V+ = +15V, V- + -15V.

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		I_{SET} = 1.5µA			I_{SET} = 15µA			I_{SET} = 1.5µA			I_{SET} = 15µA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
Offset Voltage	+25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
OffsetCurrent	+25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	+25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance (Note 10)	+25°C		50			5			50			5		MΩ
Input Capacitance	+25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain (Note 3 & 9)	+25°C	30K	100K		30K	120K		25K	40K		25K	120K		V/V
	Full	20K			20K			20K			20K			V/V
Common Mode Rejection Ratio	+25°C		90			90			90			90		dB
(Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (Note 3)	+25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	+25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	+25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	+25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	+25°C		2.0			0.2			2.0			0.2		µs
Overshoot (Note 6)	+25°C		5			15			5			15		%
Slew Rate (Note 7)	+25°C		0.1			0.8			0.1			0.8		V/µs
POWER SUPPLY CHARACTERISTICS														
Supply Current	+25°C		20			210			20			210		µA
	Full			50			450			50			450	µA
Power Supply Rejection Ratio (Note 8)	Full	80			80			76			76			dB

NOTES:

1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 6.8mW/°C for operation ambient temperatures above 75°C.

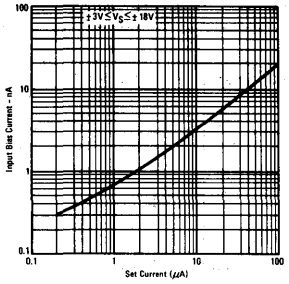
	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5µA	I_{SET} = 15µA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	←	A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF		→
7.	V_O = ±2.0v	V_O = ±10.0V	R_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

10. This parameter based upon design calculations.

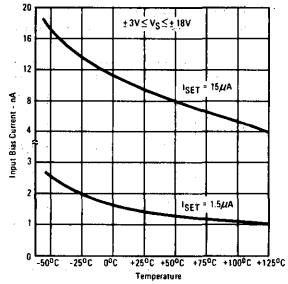
Typical Performance Curves

T_A = +25°C, V_S = ±15V D.C. Unless Otherwise Specified.

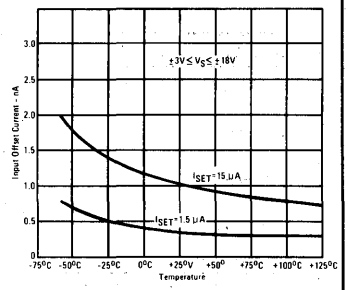
INPUT BIAS CURRENT vs SET CURRENT



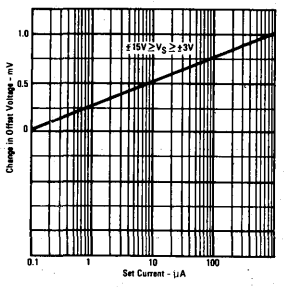
INPUT BIAS CURRENT vs TEMPERTURE



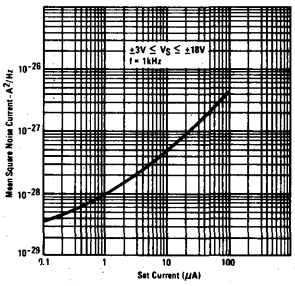
INPUT OFFSET CURRENT vs TEMPERATURE



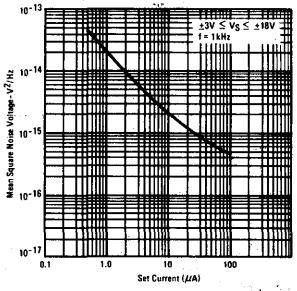
CHANGE IN OFFSET VOLTAGE vs I_{SET} (UNNULLED)



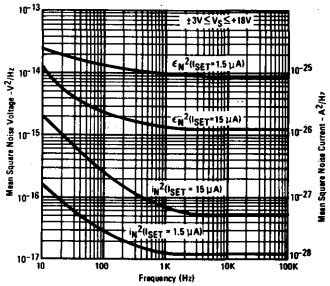
INPUT NOISE CURRENT vs I_{SET}



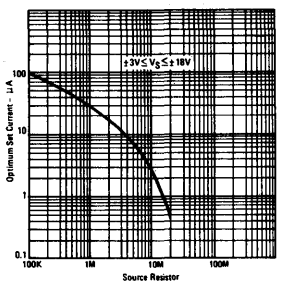
INPUT NOISE VOLTAGE vs I_{SET}



INPUT NOISE VOLTAGE AND CURRENT vs FREQUENCY

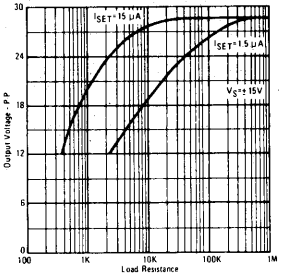


OPTIMUM SET CURRENT FOR MINIMUM NOISE vs SOURCE RESISTOR

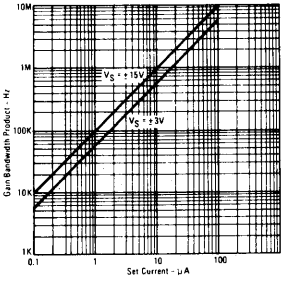


Typical Performance Curves (Continued) $T_A = +25^oC$, $V_S = \pm15V$ D.C. Unless Otherwise Specified.

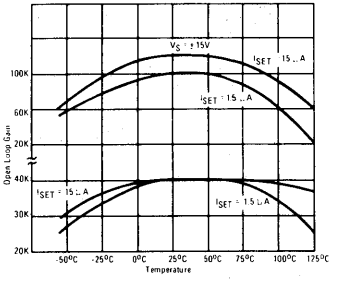
MAXIMUM OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



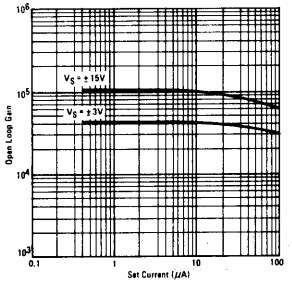
GAIN BANDWIDTH PRODUCT vs I_{SET}



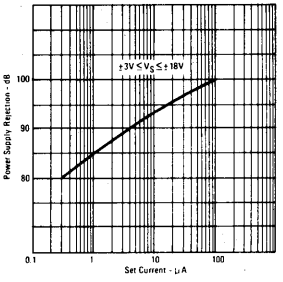
OPEN LOOP VOLTAGE GAIN vs TEMPERATURE



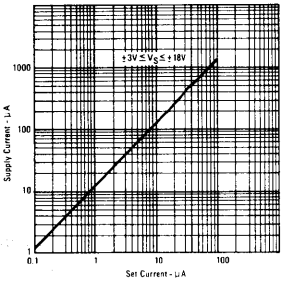
OPEN LOOP VOLTAGE GAIN vs I_{SET}



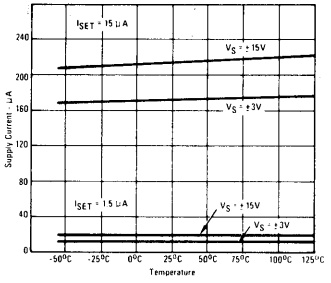
POWER SUPPLY REJECTION vs I_{SET}



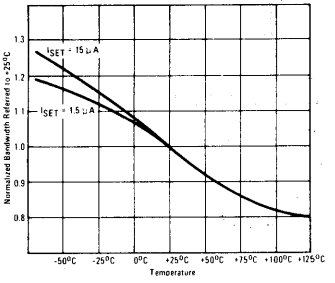
STANDBY SUPPLY CURRENT vs I_{SET}



SUPPLY CURRENT vs TEMPERATURE

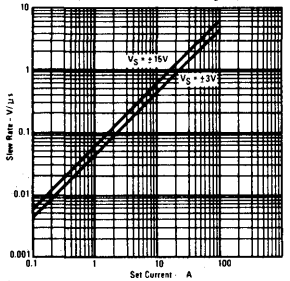


NORMALIZED BANDWIDTH vs TEMPERATURE

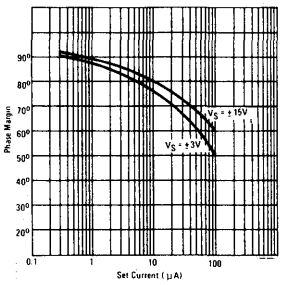


Typical Performance Curves (Continued) TA = +25°C, VS = ±15V D.C. Unless Otherwise Specified.

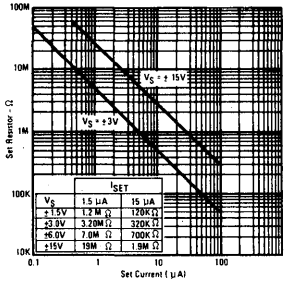
SLEW RATE vs I_{SET}



PHASE MARGIN vs SET CURRENT



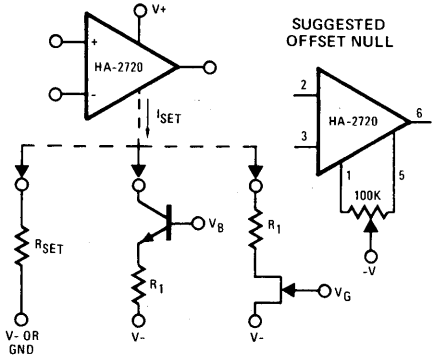
SET CURRENT vs SET RESISTOR



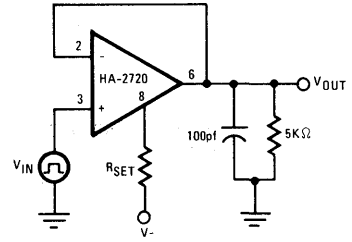
V_S	I_{SET} 1.5 µA	I_{SET} 15 µA
±15V	12M Ω	120K Ω
±3V	3.20M Ω	320K Ω
±6.0V	7.0M Ω	700K Ω
±15V	19M Ω	1.9M Ω

Test Circuits

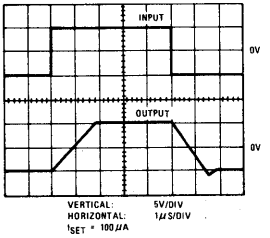
TYPICAL BIASING CIRCUITS



TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEWING WAVEFORM



Die Characteristics

Transistor Count 44

Die Dimensions ..... 60 x 44 x 19mils

Substrate Potential ..... Unbiased

Thermal Constants (°C/W)	θja	θjc
HA2-Metal Can (-2, -5)	212	58
HA2-Metal Can (-8)	173	52
HA7-Ceramic DIP (-2, -5)	218	123
HA7-Ceramic DIP (-8)	143	69
HA3-Plastic Mini-DIP (-5)	98	46

HA-4741

May 1990

Quad Operational Amplifier

Features

- Slew Rate 1.6V/μs
- Bandwidth 3.5MHz
- Input Voltage Noise ..... 9nV/√Hz
- Input Offset Voltage 0.5mV
- Input Bias Current 60nA
- Supply Range ..... ±2V to ±20V
- No Crossover Distortion
- Standard Quad Pinout

Applications

- Universal Active Filters
- D3 Communications Filters
- Audio Amplifiers
- Battery-Powered Equipment

Description

HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/√Hz at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion.

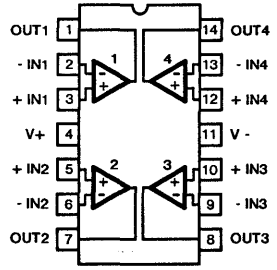
These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (108dB at 1kHz).

A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

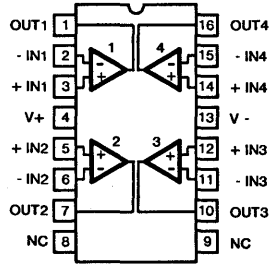
The HA-4741 is available in plastic or ceramic 14 lead DIP packages. The HA-4741-2 operates from -55°C to +125°C and the HA-4741-5 operates over the 0°C to +75°C temperature range. HA-4741/883 product and data sheets available upon request. This device is also offered in a 16 pin SOIC package with -5 or -9 temperature options.

Pinouts

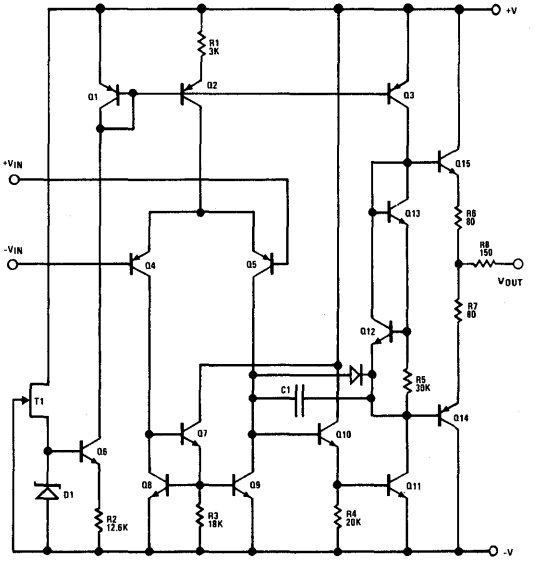
HA1-4741 (CERAMIC)
HA3-4741 (EPOXY)
TOP VIEW



HA9P4741 (SOIC)
TOP VIEW



Schematic



¼ HA-4741

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 13)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage ..... ±30.0V
Input Voltage (Note 1) ..... ±15.0V
Output Short Circuit Duration (Note 2) ..... Indefinite
Power Dissipation For Epoxy Package (Note 3) 880mW

Operating Temperature Ranges

HA-4741-2 ..... -55°C ≤ T_A ≤ +125°C
HA-4741-5 ..... 0°C ≤ T_A ≤ +75°C
HA-4741-9 ..... -40°C ≤ T_A ≤ +85°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

Electrical Specifications

V+ = +15V, V- = -15V, Unless Otherwise Specified.

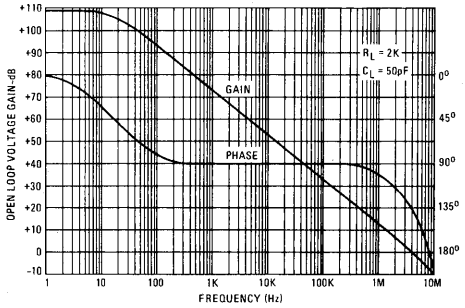
PARAMETER	TEMP	HA-4741-2			HA-4741-5			(NOTE 14) HA-4741-9	UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MAX	
INPUT CHARACTERISTICS									
Offset Voltage	+25°C	-	0.5	3	-	1	5	5	mV
	Full	-	4	5	-	4	6.5	8.5	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	-	µV/°C
Bias Current	+25°C	-	60	200	-	60	300	300	nA
	Full	-	-	325	-	-	400	400	nA
Offset Current	+25°C	-	15	30	-	30	50	50	nA
	Full	-	-	75	-	-	100	100	nA
Common Mode Range	Full	±12	-	-	±12	-	-	-	V
Differential Input Resistance	+25°C	-	0.5	-	-	0.5	-	-	MΩ
Input Voltage Noise (f = 1kHz)	+25°C	-	9	-	-	9	-	-	nV/√Hz
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain (Notes 4)	+25°C	50K	100K	-	25K	50K	-	-	V/V
	Full	25K	-	-	15K	-	-	-	V/V
Common Mode Rejection Ratio	+25°C	80	95	-	80	95	-	-	dB
	Full	74	-	-	74	-	-	-	dB
Channel Separation (Note 5)	+25°C	90	108	-	90	108	-	-	dB
Small Signal Bandwidth	+25°C	2.5	3.5	-	2.5	3.5	-	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing (R_L = 10K)	Full	±12	±13.7	-	±12	±13.7	-	-	V
(R_L = 2K)	Full	±10	±12.5	-	±10	±12.5	-	-	V
Full Power Bandwidth (Notes 4 & 9)	+25°C	14	25	-	14	25	-	-	kHz
Output Current (Note 6)	Full	±5	±15	-	±5	±15	-	-	mA
Output Resistance	+25°C	-	300	-	-	300	-	-	Ω
TRANSIENT RESPONSE (Note 7 & 10)									
Rise Time (Note 11)	+25°C	-	75	140	-	75	140	140	ns
Overshoot (Note 11)	+25°C	-	25	40	-	25	40	40	%
Slew Rate (Note 12)	+25°C	-	±1.6	-	-	±1.6	-	-	V/µs
POWER SUPPLY CHARACTERISTICS									
Supply Current	+25°C	-	4.5	5	-	5	7	7	mA
Power Supply Rejection Ratio (Note 8)	Full	80	95	-	80	95	-	-	dB

NOTES:

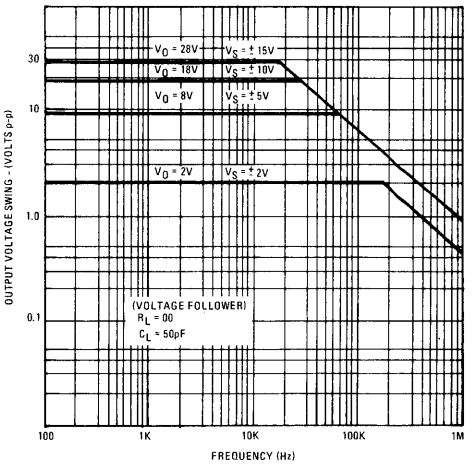
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely
3. Derate 5.8mW/°C above T_A = +25°C
4. V_{OUT} = ±10, R_L = 2K
5. Referred to input; f = 10kHz, R_S = 1K
6. V_{OUT} = ±10
7. See Pulse Response Characteristics
8. ΔV = ±5V
9. Full power bandwidth guaranteed based upon slew rate measurement FPBW = S.R./2π V_{PEAK}
10. R_L = 2K, C_L = 50pF
11. V_{OUT} = ±200mV
12. V_{OUT} = ±5V
13. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
14. Typical and Minimum specifications for the -9 version are the same as those for the -5 version.

Typical Performance Curves V+ =+15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified.

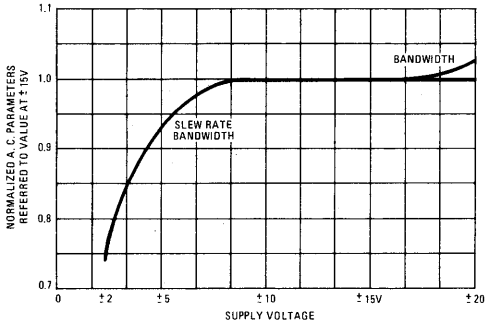
OPEN LOOP FREQUENCY RESPONSE



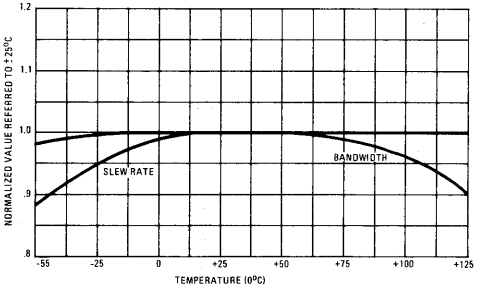
OUTPUT VOLTAGE SWING vs. FREQUENCY



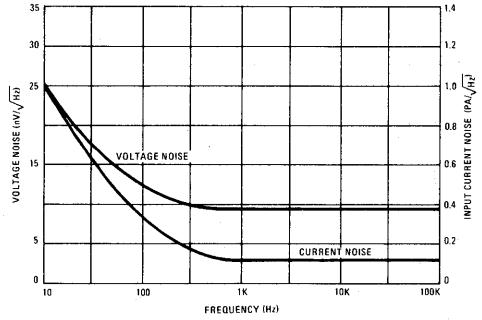
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



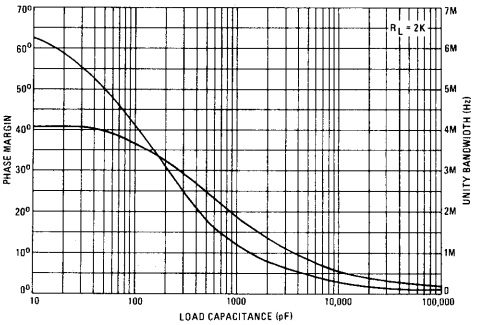
NORMALIZED AC PARAMETERS vs. TEMPERATURE



INPUT NOISE vs. FREQUENCY

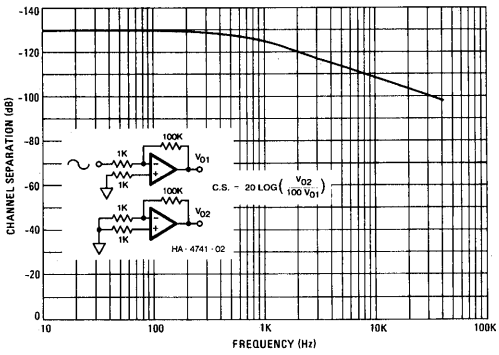


SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE

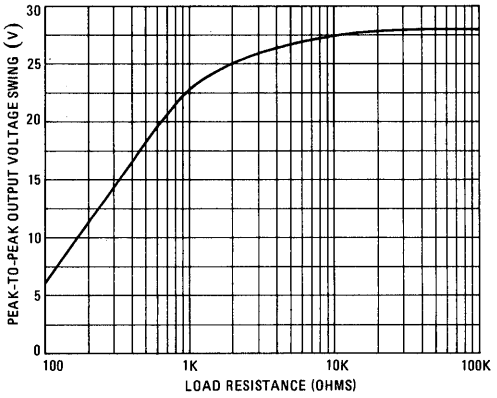


Typical Performance Curves (Continued)

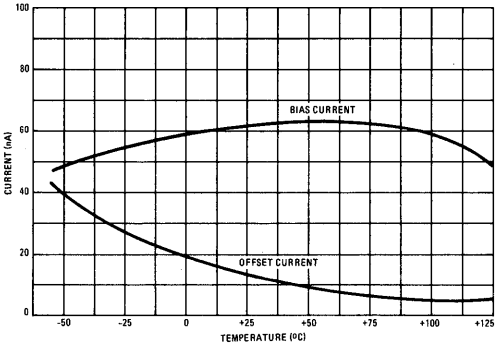
CHANNEL SEPARATION vs. FREQUENCY



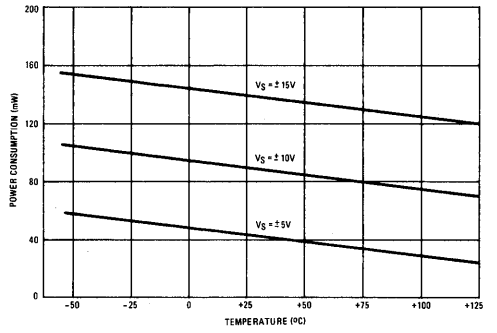
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE

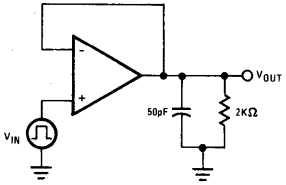


POWER CONSUMPTION vs. TEMPERATURE

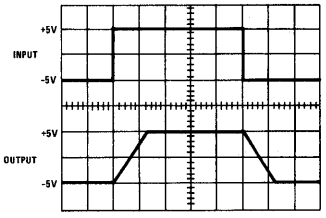


Pulse Response

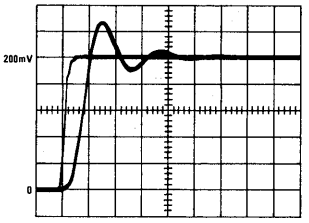
TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEW RESPONSE
(Volts: 5V/Div., Time: 5μs/Div.)



TRANSIENT RESPONSE
(Volts: 40mV/Div., Time: 100ns/Div.)



HARRIS

HA-5004

January 1989

100MHz Current Feedback Amplifier

Features

- Slew Rate 1200V/µs
- Output Current ..... ±100mA
- Drives ..... ±9V into 100Ω
- V_{SUPPLY} ..... ±5V to ±18V
- Thermal Overload Protection and Output Flag
- Bandwidth Nearly Independent of Gain
- Output Enable/Disable

Applications

- Unity Gain Video/Wideband Buffer
- Video Gain Block
- High Speed Peak Detector
- Fiber Optic Transmitters
- Zero Insertion Loss Transmission Line Drivers
- Current to Voltage Converter
- Radar Systems

Description

The HA-5004 current feedback amplifier is a video/wideband amplifier optimized for low gain applications. The design is based on current-mode feedback which allows the amplifier to achieve higher closed loop bandwidth than voltage-mode feedback operational amplifiers. Since feedback is employed, the HA-5004 can offer better gain accuracy and lower distortion than open loop buffers. Unlike conventional op amps, the bandwidth and rise time of the HA-5004 are nearly independent of closed loop gain. The 100MHz bandwidth at unity gain reduces to only 65MHz at a gain of 10. The HA-5004 may be used in place of a conventional op amp with a significant improvement in speed power product.

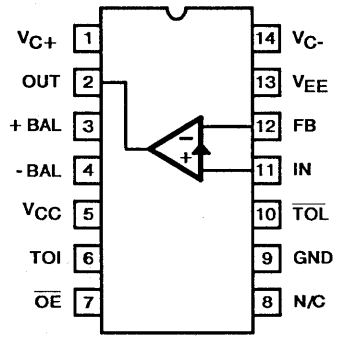
Several features have been designed in for added value. A thermal overload feature protects the part against excessive junction temperature by shutting down the output. If this feature is not needed, it can be inhibited via a TTL input (TOI). A TTL chip enable/disable ($\overline{OE}$) input is also provided; when the chip is disabled its output is high impedance. Finally, an open collector output flag ($\overline{TOL}$) is provided to indicate the status of the chip. The status flag goes low to indicate when the chip is disabled due to either the internal Thermal Overload shutdown or the external disable.

In order to maximize bandwidth and output drive capacity, internal current limiting is not provided. However, current limiting may be applied via the V_C+ and V_C- pins which provide power separately to the output stage.

The HA-5004 is available in a 14-pin Ceramic DIP and is specified for operation from 0°C to +75°C (HA1-5004-5) and -40°C to +85°C (HA1-5004-9). For Military grade product refer to the HA-5004/883 data sheet.

Pinouts

HA1-5004 (CERAMIC DIP)
TOP VIEW



INPUTS		TEMP	$\overline{TOL}$ OUTPUT (OPEN COLLECTOR)	OPERATION
$\overline{OE}$	TOI	T_J		
0	0	Normal	1	Normal
0	0	High*	0	Auto Shutdown, Hi-Z OUT
0	1	X	1	Normal
1	X	X	0	Manual Shutdown, Hi-Z OUT

*>180°C Typical

3 OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Supply Voltage ..... ±20V
Differential Input Voltage 5V
Common Mode Input Voltage ..... $\pm V_{SUPPLY}$
Output Current ..... ±120mA

Operating Temperature Range

HA-5004-9 ..... $-40^oC \leq T_A \leq +85^oC$
HA-5004-5 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature ..... $-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature ..... $+175^oC$

Electrical Specifications $V_{CC} = V_{C+} = +15V$, $V_{EE} = V_{C-} = -15V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $A_V = +1$, $R_F = 250\Omega$, $\overline{OE} = 0.8V$, TOI = 0.8V or 2.0V Unless Otherwise Specified.

PARAMETER		TEMP	HA-5004-5, -9 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage		+25°C	-	1	5	mV
		Full	-	-	20	mV
Average Offset Voltage Drift		Full	-	10	-	µV/°C
Bias Current (+Input Only) (Note 2)		+25°C	-	2	5	µA
		Full	-	-	20	µA
Input Resistance (+Input Only) (Note 2)		+25°C	-	3	-	MΩ
Input Capacitance		+25°C	-	3	-	pF
Common Mode Range		Full	±10	-	-	V
DISTORTION AND NOISE						
Total Harmonic Distortion $2V_{p-p}$, 200kHz	$A_{VCL} = +1$		-	-72	-	dBc
	$A_{VCL} = +2$		-	-70	-	dBc
	$A_{VCL} = +5$		-	-68	-	dBc
Input Noise Voltage 10Hz to 1MHz		+25°C	-	15	-	μV_{p-p}
Input Noise Voltage Density (Note 3)	$f_O = 10kHz$	+25°C	-	2.2	-	$nV/\sqrt{Hz}$
	$f_O = 100kHz$	+25°C	-	2.2	-	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 3)	$f_O = 10kHz$	+25°C	-	6	-	$pA/\sqrt{Hz}$
	$f_O = 100kHz$	+25°C	-	4	-	$pA/\sqrt{Hz}$
DIGITAL I/O CHARACTERISTICS						
Logic Inputs (OE and TOI)	V_{IH}	Full	2.0	-	-	V
	V_{IL}	Full	-	-	0.8	V
	I_{IH} @ $V_I = 2.4V$	Full	-	-	1	µA
	I_{IL} @ $V_I = 0.4V$	Full	-	-	10	µA
Logic Output (TOL) (Open Collector)	V_{OL} @ 800µA	Full	-	0.05	0.4	V
TRANSFER CHARACTERISTICS						
DC Gain Error	Small Signal (±100mV)	+25°C	-	0.25	0.43	%
		Full	-	0.25	0.75	%
	Large Signal (±10V) (R_L = 1K)	+25°C	-	0.25	0.43	%
		Full	-	0.25	0.75	%
DC Voltage Gain (Note 4)		+25°C	233	400	-	V/V
		Full	133	400	-	V/V
DC Transimpedance (Note 5)		+25°C	58	100	-	V/mA
		Full	33	100	-	V/mA
-3dB Bandwidth $A_V = +1$ (Note 6)		+25°C	-	100	-	MHz
Gain Flatness	DC to 5MHz	+25°C	-	0.03	-	dB
	DC to 10MHz	+25°C	-	0.05	-	dB
Differential Gain (Notes 6, 7, 8) 3.58MHz	$A_{VCL} = +1$	+25°C	-	0.035	-	%
	$A_{VCL} = +2$	+25°C	-	0.058	-	%
Differential Gain (Notes 6, 7, 8) 4.43MHz	$A_{VCL} = +1$	+25°C	-	0.035	-	%
	$A_{VCL} = +2$	+25°C	-	0.058	-	%
Differential Phase (Note 6, 7) 3.58MHz	$A_{VCL} = +1$	+25°C	-	0.15	-	Degree
	$A_{VCL} = +2$	+25°C	-	0.23	-	Degree
Differential Phase (Note 6, 7) 4.43MHz	$A_{VCL} = +1$	+25°C	-	0.17	-	Degree
	$A_{VCL} = +2$	+25°C	-	0.24	-	Degree
Common Mode Rejection Ratio (Note 9)		Full	-	58	-	dB
Minimum Stable Gain		Full	1	-	-	V/V

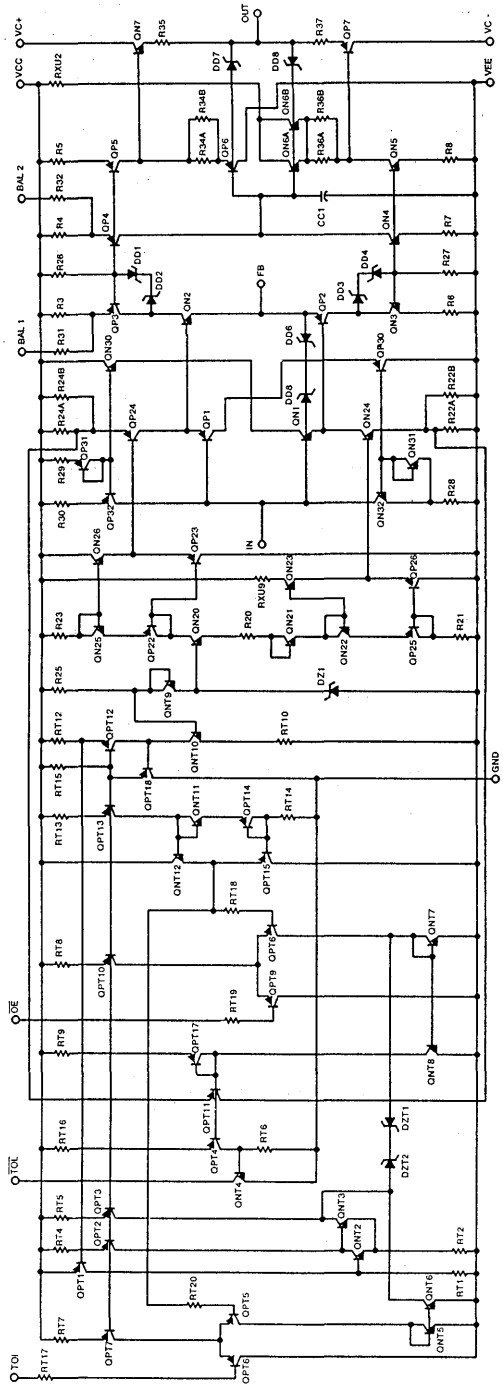
Electrical Specifications (Continued) $V_{CC} = V_{C+} = +15V$, $V_{EE} = V_{C-} = -15V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $A_V = +1$, $R_F = 250\Omega$, $\overline{OE} = 0.8V$, TOI = 0.8V or 2.0V Unless Otherwise Specified.

PARAMETER		TEMP	HA-5004-5, -9 MIN	HA-5004-5, -9 TYP	HA-5004-5, -9 MAX	UNITS
OUTPUT CHARACTERISTICS						
Output Voltage Swing	($R_L = 100\Omega$)	+25°C	±9.0	±9.5	–	V
	($R_L = 1k\Omega$)	+25°C	±11.5	±11.8	–	V
	($R_L = 100\Omega$)	Full	±8.0	±9.5	–	V
	($R_L = 1k\Omega$)	Full	±10.5	±11.8	–	V
Full Power Bandwidth ($A_V = +1$) (Note 10)		+25°C	–	100	–	MHz
Output Resistance, Open Loop		+25°C	–	5	–	Ω
Output Current		+25°C	±90	±100	–	mA
		Full	±80	±100	–	mA
Output Enable time (Hi Z to ±2V)		Full	–	100	–	ns
Output Disable time (±2V to Hi Z)		Full	–	3	–	µs
Output Leakage (Disabled)		Full	–	–	1	µA
TRANSIENT RESPONSE						
Rise Time/Fall Time		+25°C	–	6.3	–	ns
Propagation Delay (10V Step)		+25°C	–	7	–	ns
Slew Rate		+25°C	–	1200	–	V/µs
Settling Time (0.1%, 10V Step)		+25°C	–	50	–	ns
Overshoot		+25°C	–	10	–	%
POWER SUPPLY CHARACTERISTICS						
Supply Current	(Enabled)	+25°C	–	12	16	mA
		Full	–	–	22	mA
	(Disabled)	+25°C	–	7	–	mA
Power Supply Rejecton Ratio		Full	50	60	–	dB

NOTES:

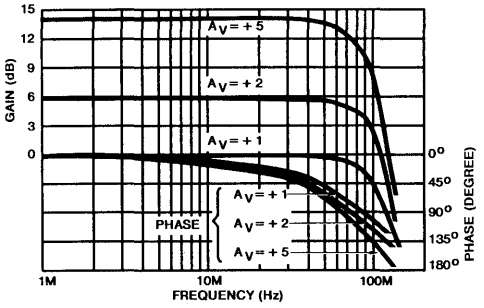
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Inverting (FB) input is a low impedance point; Bias Current, Offset Current, and Input Resistance are not specified for this terminal.
3. See typical performance curves.
4. DC Voltage Gain $= \dfrac{1}{\text{Gain Error}}$
5. DC Transimpedance $= \dfrac{R_F}{\text{Gain Error}}$, $R_F = 250\Omega$
6. $V_{IN} = 300mVp\text{-}p$
7. $V_{OFFSET} = 1.0V$
8. Differential Gain (dB) = 0.0869 Differential Gain (%)
9. $V_{CM} = \pm 10V$
10. Full power bandwidth guaranteed by equation: Full Power Bandwidth $= \dfrac{\text{Slew Rate}}{2\pi V_{peak}}$, $V_{peak} = 2V$

Schematic

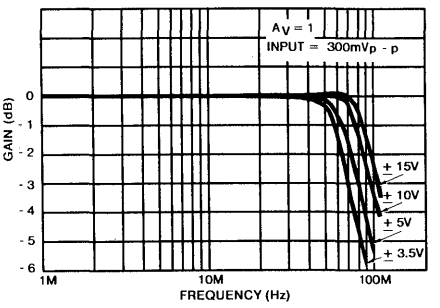


Typical Performance Curves $V_{SUPPLY} = \pm 15V$, $T_A = 25^oC$, Unless Otherwise Specified.

GAIN AND PHASE vs. FREQUENCY

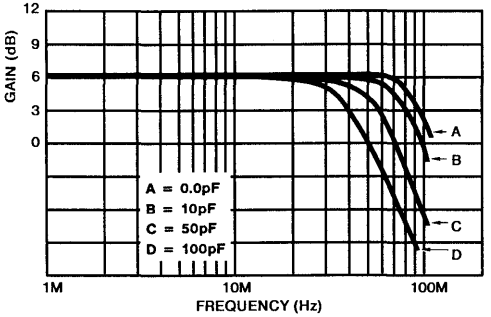


FREQUENCY RESPONSE vs. SUPPLY VOLTAGE



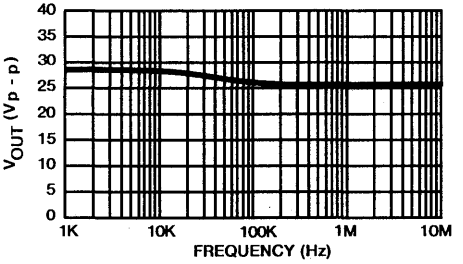
FREQUENCY RESPONSE vs. C_L

$V_{CC} = \pm 15V$, $A_V = +2$, $R_L = 1k\Omega$, Input = 10mV

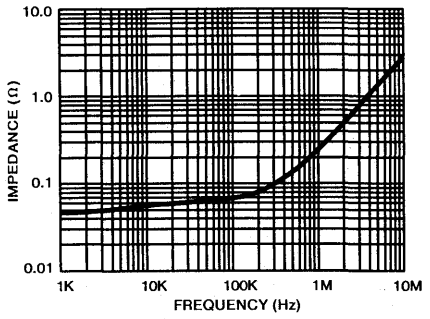


MAX. UNDISTORTED SINEWAVE OUTPUT vs. FREQUENCY

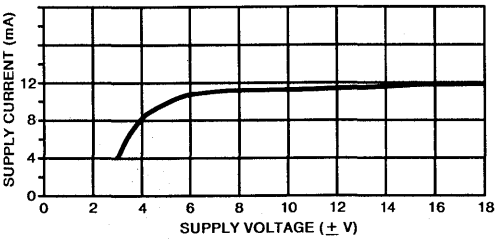
$V_{CC} = \pm 15V$, $A_V = +1$, Sinewave Input



CLOSED LOOP OUTPUT IMPEDANCE vs. FREQUENCY



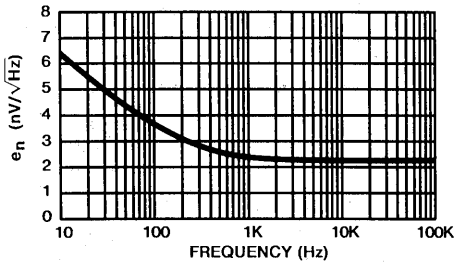
SUPPLY CURRENT vs. SUPPLY VOLTAGE



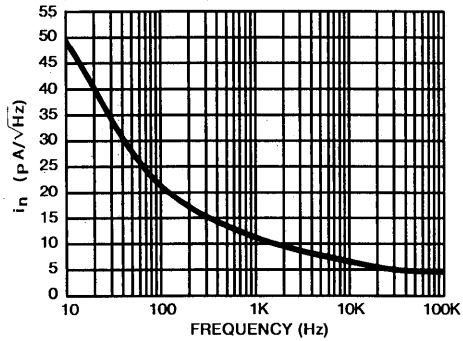
3 OPERATIONAL AMPLIFIERS

Typical Performance Curves (Continued) V_{SUPPLY} = ±15V, T_A = 25°C, Unless Otherwise Specified.

VOLTAGE NOISE vs. FREQUENCY
V_{CC} = ±15V

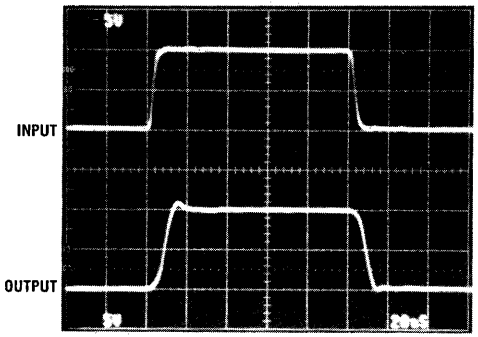


CURRENT NOISE vs. FREQUENCY
V_{CC} = ±15V



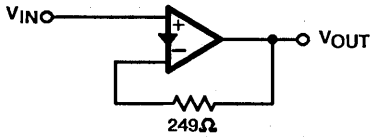
Switching Waveforms

LARGE SIGNAL RESPONSE, A_V = +1
Vertical Scale: 5V/Div.
Horizontal Scale: 20ns/Div.

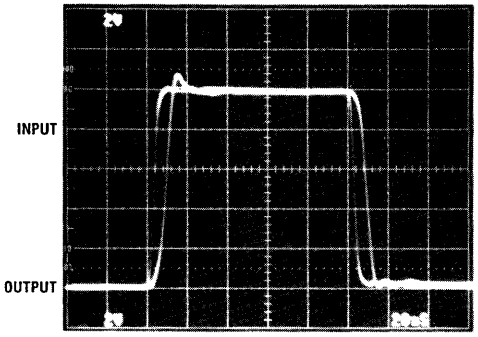


A_V = +1, V_{SUPPLY} = ±15V

TEST CIRCUIT

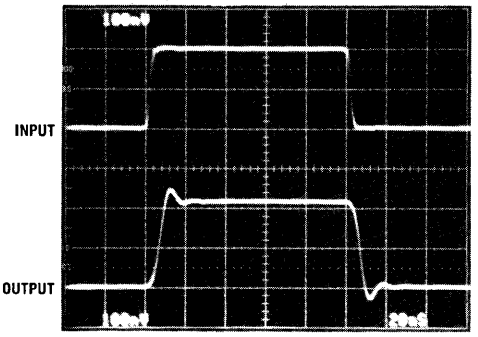


PROPAGATION DELAY
Vertical Scale: 2V/Div.
Horizontal Scale: 20ns/Div.



A_V = +1, V_{SUPPLY} = ±15V

SMALL SIGNAL RESPONSE
Vertical Scale: 100mV/Div.
Horizontal Scale: 20ns/Div.



A_V = +1, V_{SUPPLY} = ±15V

Applications Information

Theory of Operation

The HA-5004 is a high performance amplifier that uses current feedback to achieve its outstanding performance. Although it is externally configured like an ordinary op amp in most applications, its internal operation is significantly different.

Inside the HA-5004, there is a unity gain buffer from the non-inverting (+) input to the inverting (FB) input (as suggested by the circuit symbol), and the inverting terminal is a low impedance point. Error currents are sensed at the inverting input and amplified; a small change in input current produces a large change in output voltage. The ratio of output voltage delta due to input current delta is the transimpedance of the device.

Steady state current at the inverting input is very small because the transimpedance is large. The voltage across the input terminals is nearly zero due to the buffer amplifier. These two properties are similar to standard op amps and likewise simplify circuit analysis.

Resistor Selection

The HA-5004 is optimized for a feedback resistor of 250Ω, regardless of gain configuration. It is important to note that this resistor is required even for unity gain applications; higher gain settings use a second resistor like regular op amp circuits as shown in Figure 1 below.

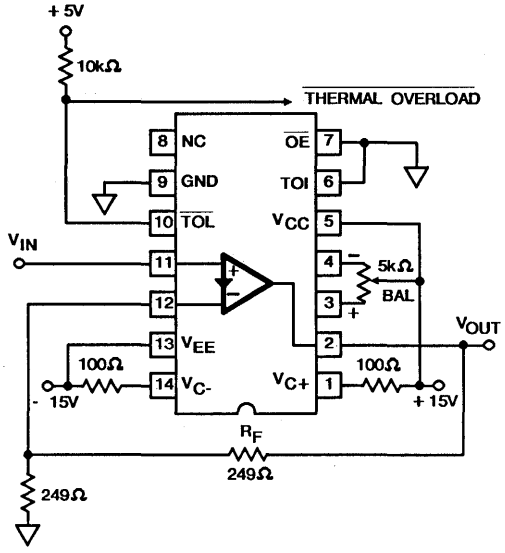


FIGURE 1: TYPICAL APPLICATION CIRCUIT, A_V = +2

Power Supplies

The HA-5004 will operate over a wide range of supply voltages with excellent performance. Supplies may be either single-ended or split, ranging from 6V (±3V) to 36V (±18V). Appropriate reduction in input and output signal excursion is necessary for operation at lower supply voltages. Bypass capacitors from each supply to ground are recommended, typically a 0.01μF ceramic in parallel with a 4.7μF electrolytic.

Current Limit

No internal current limiting is provided for the HA-5004 in order to maximize bandwidth and slew rate. However, power is supplied separately to the output stage via pins 1 (V_{C+}) and 14 (V_{C-}) so that external current limiting resistors may be used. If required, 100Ω resistors to each supply rail are recommended.

Enable/Disable and Thermal Overload Operation

The HA-5004 operates normally with a TTL low state on pin 7 ($\overline{OE}$) but it may be disabled manually by a TTL high state at this input. When disabled, the output and inverting (FB) input go to a high impedance state and the circuit is electrically debiased, reducing supply current by about 5mA. It is important to keep the differential input voltage below the absolute maximum rating of 5V when the device is disabled.

If the power dissipation becomes excessive and chip temperature exceeds approximately 180°C, the HA-5004 will automatically disable itself. The thermal overload condition will be indicated by a low state at the $\overline{TOL}$ output on pin 10. ($\overline{TOL}$ is also low for manual shutdown via pin 7). Automatic thermal shutdown can be bypassed by a TTL high state on Thermal Overload Inhibit (TOI) pin 6. See the truth table for a summary of operation.

Offset Adjustment

Offset voltage may be nulled with a 5KΩ potentiometer between pins 3 and 4, center tapped to the positive supply. Setting the slider towards pin 3 (+BAL) increases output voltage; towards pin 4 (-BAL) decreases output voltage. Offset can be adjusted by about ± 10mV with a 5K pot; this range is extended with a lower resistance potentiometer.

Die Characteristics

Transistor Count 64

Die Dimensions ..... 93 x 63 x 19mils (2370 x 1600 x 480μm)

Substrate Potential ..... V_{EE}

Process ..... Bipolar DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA1-Ceramic DIP	107	25

HARRIS HA-5101/5111

Low Noise, High Performance Operational Amplifiers

June 1990

Features

- Low Noise ..... 3.3nV/$\sqrt{Hz}$ at 1kHz
- Wide Bandwidth ..... 10MHz (Compensated)
  100MHz (Uncompensated)
- High Slew Rate ..... 10V/µs (Compensated)
  50V/µs (Uncompensated)
- Low Offset Voltage Drift ..... 3µV/°C
- High Gain ..... 1 x 10^6V/V
- High CMRR/PSRR 100dB
- High Output Drive Capability 30mA

Applications

- High Quality Audio Preamplifiers
- High Q Active Filters
- Low Noise Function Generators
- Low Distortion Oscillators
- Low Noise Comparators
- For Further Design Ideas, See App. Note 554

Description

The HA-5101/5111 are dielectrically isolated operational amplifiers featuring low noise and high performance. Both amplifiers have an excellent noise voltage density of 3.5nV/$\sqrt{Hz}$ at 1kHz. The uncompensated HA-5111 is stable at a minimum gain of 10 and has the same DC specifications as the unity gain stable HA-5101. The difference in compensation yields a 100MHz gain-bandwidth product and a 50V/µs slew rate for the HA-5111 versus a 10MHz unity gain bandwidth and a 6V/µs slew rate for the HA-5101.

DC characteristics of the HA-5101/5111 assure accurate performance. The 1mV offset voltage is externally adjustable and offset voltage drift is just 3µV/°C. An offset current of only 30nA reduces input current errors and an open loop voltage gain of 1 x 10^6V/V increases loop gain for low distortion amplification.

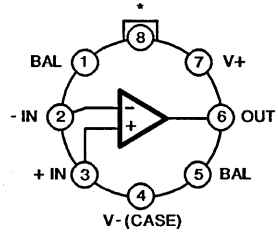
The HA-5101/5111 are ideal for audio applications, especially low-level signal amplifiers such as microphone, tape head and phono cartridge preamplifiers. Additionally, it is well suited for low distortion oscillators, low noise function generators and high Q filters.

The HA-5101/5111-2 has guaranteed operation from -55°C to +125°C and can be ordered as a military grade part. The HA-5101/5111-5 has guaranteed operation from 0°C to +75°C. All devices are available in Ceramic Mini-DIP and TO-99 Can packages. Additionally, the HA-5101/5111-5 is available in a Plastic Mini-DIP package.

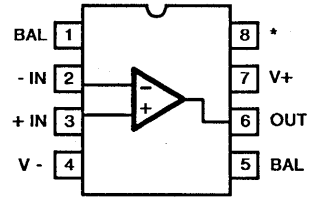
These devices are also available in SOIC packages in both -5 and -9 temperature grades.

Pinouts

HA2-5101/5111 (TO-99 METAL CAN)
TOP VIEW



HA3-5101/5111 (PLASTIC MINI-DIP)
HA7-5101/5111 (CERAMIC MINI-DIP)
HA9P5101/5111 (SOIC)
TOP VIEW



*HA-5101 No Connect
HA-5111 Compensation

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage..... ±7V
Voltage (at any pin) ..... $\pm V_{SUPPLY}$
Output Current ..... Full Short Circuit Protection
Junction Temperature ..... +175°C

Operating Temperature

HA-5101/5111-2 ..... -55°C to +125°C
HA-5101/5111-5 ..... 0°C to +75°C
HA-5101/5111-9 ..... -40°C to +85°C
Storage Temperature..... -65°C to +150°C
Internal Power Dissipation 560mW
(Derate at 5.3mW/°C Above 70°C Ambient)

Electrical Specifications

V+ = +15V, V- = -15V, R_S = 100Ω, R_L = 2kΩ, C_L = 50pF, Unless Otherwise Specified.

PARAMETER	TEMP	HA-5101-2, -5 HA-5111-2, -5			HA-5101-9 HA-5111-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	0.5	3	-	0.5	3	mV
	Full	-	-	4	-	-	4	mV
Offset Voltage Drift	Full	-	3	-	-	3	-	µV/°C
Bias Current	+25°C	-	100	200	-	100	200	nA
	Full	-	-	325	-	-	325	nA
Offset Current	+25°C	-	30	75	-	30	75	nA
	Full	-	-	125	-	-	125	nA
Input Resistance	+25°C	-	500	-	-	500	-	kΩ
Common Mode Range	Full	±12	-	-	±12	-	-	V/V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 2)	+25°C	-	1000K	-	-	1000K	-	V/V
	Full	100K	250K	-	100K	250K	-	V/V
Common Mode Rejection Ratio (Note 3)	Full	80	100	-	80	100	-	dB
Small Signal Bandwidth								
HA-5101 (A_V = 1)	+25°C	-	10	-	-	10	-	MHz
Minimum Stable Gain								
HA-5101	Full	1	-	-	1	-	-	V/V
HA-5111	Full	10	-	-	10	-	-	V/V
Gain Bandwidth Product HA-5111 (A_V = 10)	+25°C	-	100	-	-	100	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
R_L = 10K	Full	±12	±13	-	±12	±13	-	V
R_L = 2K	Full	±12	±13	-	±12	±13	-	V
(V_{PS} = ±18, R_L = 600)	+25°C	±15	-	-	±15	-	-	V
Output Current (Note 4)	+25°C	25	30	-	25	30	-	mA
Full Power Bandwidth (Note 5)								
HA-5101	+25°C	95	160	-	95	160	-	kHz
HA-5111	+25°C	630	790	-	630	790	-	kHz
Output Resistance	+25°C	-	110	-	-	110	-	Ω
Maximum Load Capacitance	+25°C	-	800	-	-	800	-	pF

Electrical Specifications (Continued) V+ =15V, V- = -15V, R_S = 100, R_L = 2K, C_L = 50pF Unless Otherwise Specified.

PARAMETER	TEMP	HA-5101-2, -5 HA-5111-2, -5 MIN	TYP	MAX	HA-5101-9 HA-5111-9 MIN	TYP	MAX	UNITS
TRANSIENT RESPONSE (Note 6)								
Rise Time								
HA-5101	+25°C	-	50	100	-	50	100	ns
HA-5111	+25°C	-	30	60	-	30	60	ns
Overshoot								
HA-5101	+25°C	-	20	35	-	20	35	%
HA-5111	+25°C	-	20	40	-	20	40	%
Slew Rate								
HA-5101	+25°C	6	10	-	6	10	-	V/µs
HA-5111	+25°C	40	50	-	40	50	-	V/µs
Settling Time (Note 7)								
HA-5101 0.01%	-	-	2.6	-	-	2.6	-	µs
HA-5111 0.01%	-	-	0.5	-	-	0.5	-	µs
NOISE CHARACTERISTICS (Note 8)								
Input Noise Voltage								
f = 10Hz	+25°C	-	7	17	-	7	17	$nV/\sqrt{Hz}$
f = 1kHz	+25°C	-	3.3	4.5	-	3.3	4.5	$nV/\sqrt{Hz}$
Input Noise Current								
f = 10Hz	+25°C	-	5.1	28	-	5.1	28	$pA/\sqrt{Hz}$
f = 1kHz	+25°C	-	1.1	3	-	1.1	3	$pA/\sqrt{Hz}$
Broadband Noise Voltage f = DC to 30kHz	+25°C	-	0.870	-	-	0.870	-	µVrms
POWER SUPPLY CHARACTERISTICS								
Supply Current HA-5101/5111	Full	-	4	6	-	4	7	mA
Power Supply Rejection Ratio (Note 9)	Full	80	100	-	80	100	-	dB

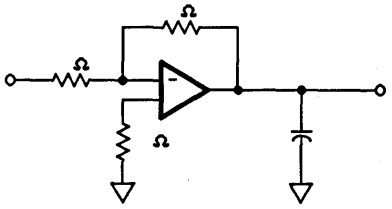
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, R_L = 2K.
3. V_{CM} = ±10V.
4. Output current is measured with V_{OUT} = ±15V with V_{SUPPLY} = ±18V.
5. Full power bandwidth is guaranteed by equation:

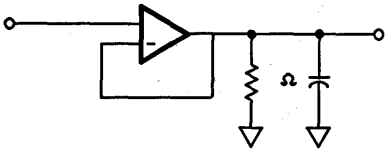
   Full power bandwidth = $\frac{\text{Slew Rate}}{2\pi V \text{ Peak}}$, V_{peak} = 10V.
6. Refer to Test Circuits section of the data sheet.
7. Settling time is measured to 0.01% of final value for a 10V output step, and A_V = -10 for HA-5111 and 0.01% of final value for a 10V output step, A_V = -1 for HA-5101.
8. Sample Tested.
9. Delta V_{SUPPLY} = ±5V.

Test Circuits

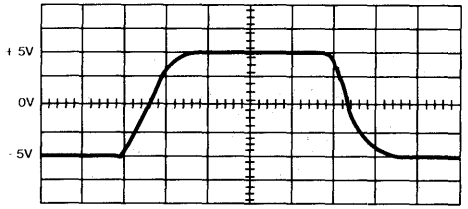
HA-5101 LARGE SIGNAL RESPONSE CIRCUIT



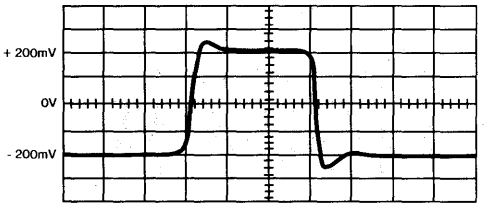
HA-5101 SMALL SIGNAL RESPONSE CIRCUIT



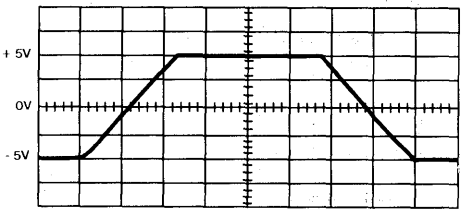
HA-5111 LARGE SIGNAL TRANSIENT RESPONSE
Ch. 1 = 2.5V/Div.
Timebase = 200ns/Div.



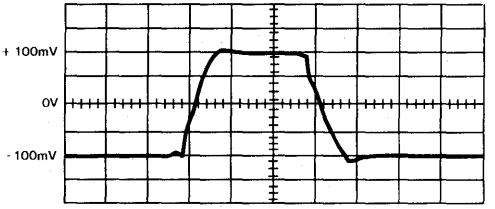
HA-5111 SMALL SIGNAL TRANSIENT RESPONSE
Ch. 1 = 100mV/Div.
Timebase = 100ns/Div.



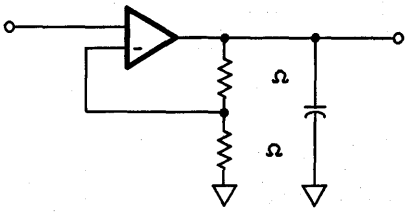
HA-5101 LARGE SIGNAL TRANSIENT RESPONSE
Ch. 1 = 2.5V/Div.
Timebase = 1.00µs/Div.



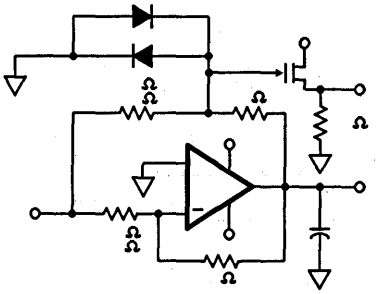
HA-5101 SMALL SIGNAL TRANSIENT RESPONSE
Ch. 1 = 50mV/Div.
Timebase = 100ns/Div.



HA-5111 LARGE AND SMALL RESPONSE CIRCUIT



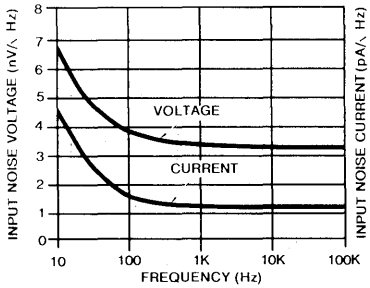
SETTLING TIME CIRCUIT



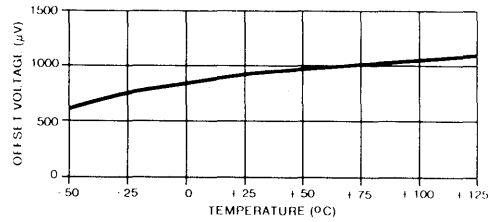
- A_V = -1 (HA-5101), *A_V = -10 (HA-5111)
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional, HP5082-2810 recommended.

Typical Performance Curves

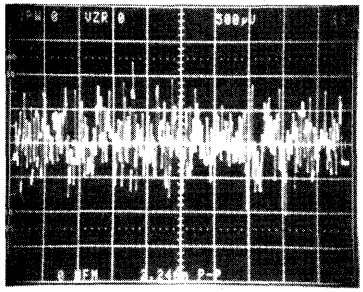
HA-5101/11 NOISE SPECTRUM



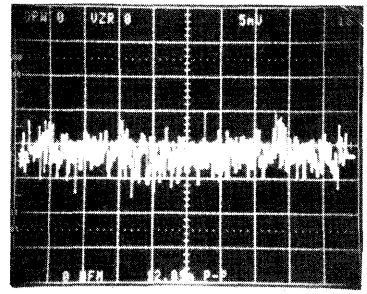
OFFSET VOLTAGE vs. TEMPERATURE



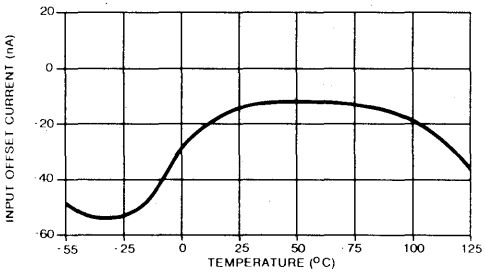
PEAK-TO-PEAK NOISE 0.1Hz to 10Hz
A_V = 25000 V_{CC} = ±15V
(2.25μVp-p RTO)



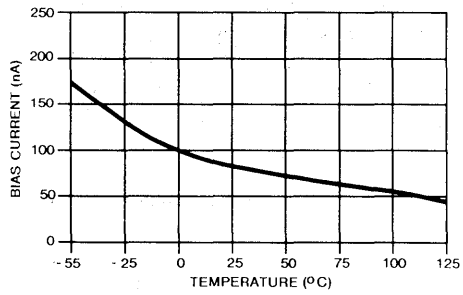
PEAK-TO-PEAK TOTAL NOISE 0.1Hz to 1MHz
A_V = 25000, V_{CC} = ±15V
(12.89mVp-p RTO)



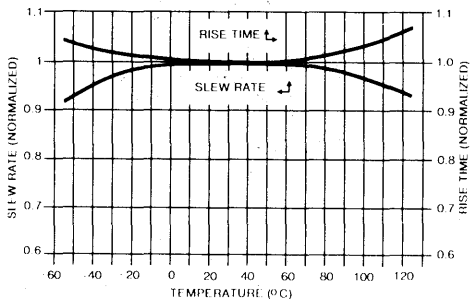
INPUT OFFSET CURRENT vs. TEMPERATURE



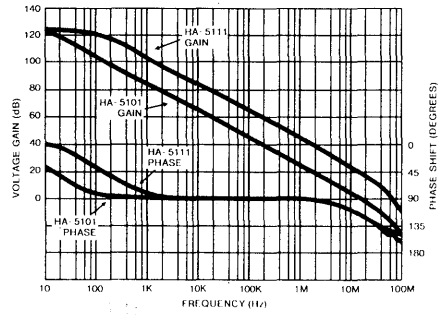
INPUT BIAS CURRENT vs. TEMPERATURE



SLEW RATE/RISE TIME vs. TEMPERATURE
R_L = 2K, C_L = 50pF, V_{CC} = ±15V

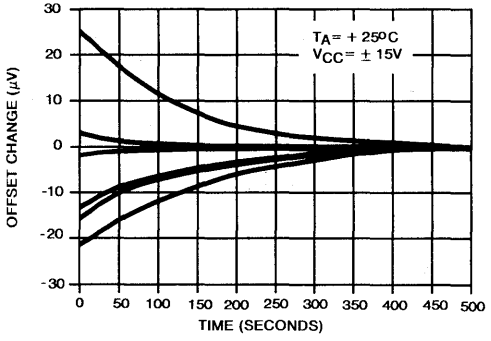


OPEN-LOOP GAIN/PHASE VS. FREQUENCY

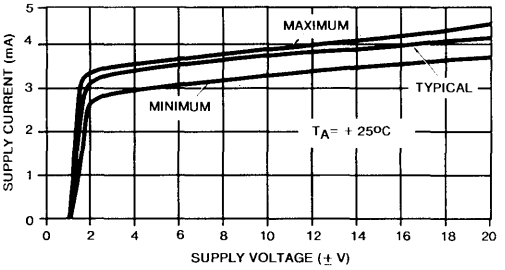


Typical Performance Curves (Continued)

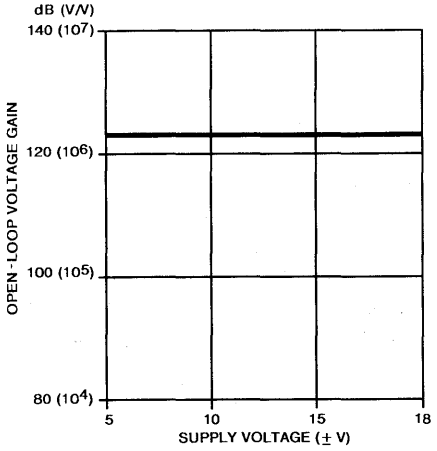
INPUT OFFSET WARMUP DRIFT vs. TIME
(Normalizd To Zero Final Value)
(Six Representative Units)



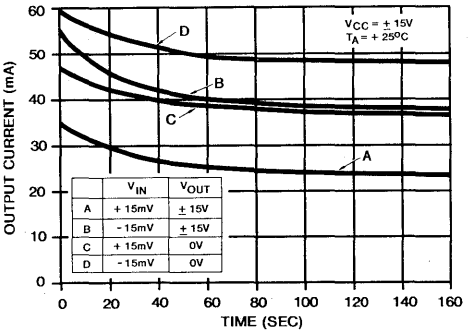
SUPPLY CURRENT vs. SUPPLY VOLTAGE



DC OPEN-LOOP VOLTAGE GAIN vs. SUPPLY VOLTAGE

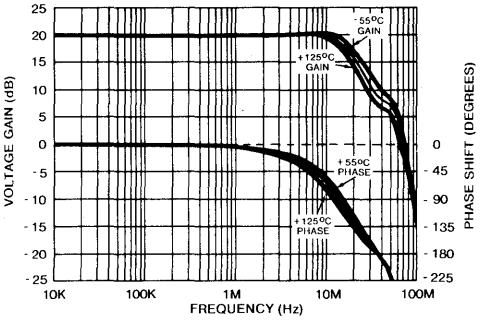


SHORT CIRCUIT CURRENT vs. TIME

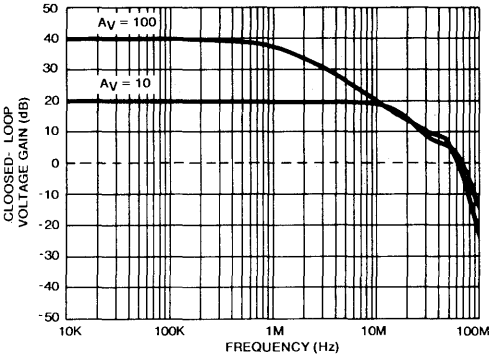


	V_{IN}	V_{OUT}
A	+ 15mV	± 15V
B	- 15mV	± 15V
C	+ 15mV	0V
D	- 15mV	0V

HA-5111 CLOSED-LOOP GAIN AND PHASE AT HIGH AND LOW TEMPERATURE
(Typical Rresponse Of One Amplifier)
V_{CC} = ±15V, A_V = 10V/V, R_L = 2K, C_L = 50pF

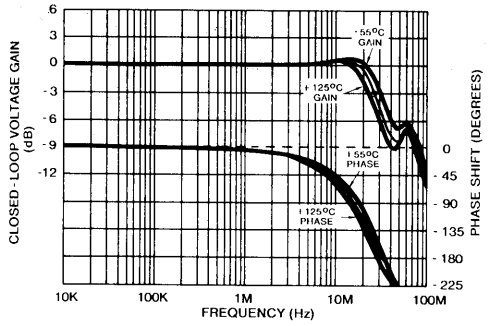


HA-5111 CLOSED-LOOP VOLTAGE GAIN FREQUENCY AT DIFFERENT CLOSED-LOOP GAINS
T_A = +25°C, V_{CC} = ±15V, A_V = 100,
10V/V, R_L = 2K, C_L = 50pF

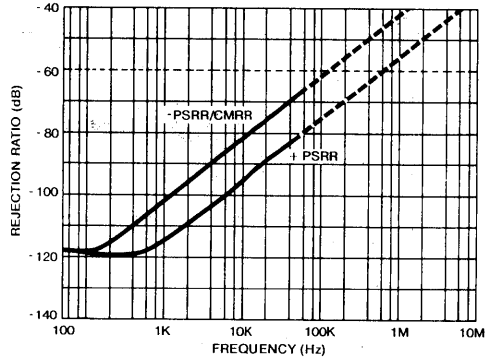


Typical Performance Curves (Continued)

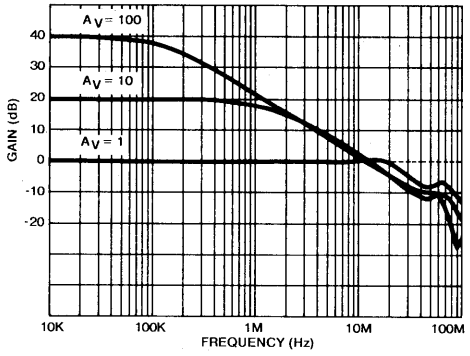
HA-5101 CLOSED-LOOP GAIN AND PHASE AT HIGH AND LOW TEMPERATURE
(Typical Response Of One Amplifier)
V_{CC} = ±15V, AV = 1V/V, R_L = 2K, C_L = 50pF



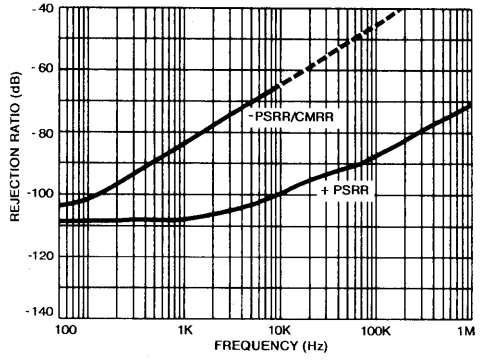
HA-5111 REJECTION RATIOS vs. FREQUENCY
T_A = +25°C, V_{CC} = ± 15V



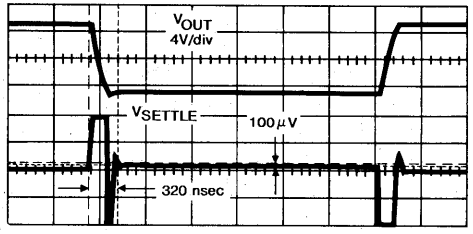
HA-5101 CLOSED-LOOP VOLTAGE GAIN vs. FREQUENCY AT DIFFERENT CLOSED-LOOP GAINS
T_A = +25°C, V_{CC} = ±15V, R_L = 2K, C_L = 50pF



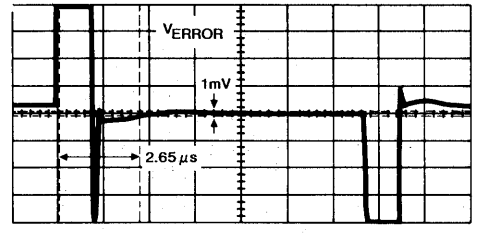
HA-5101 REJECTION RATIOS vs. FREQUENCY
T_A = +25°C, V_{CC} = ±15V



HA-5111 SETTLING WAVEFORM 500ns/DIV.



HA-5101 SETTLING WAVEFORM 1.5μs/DIV.



Applications Information

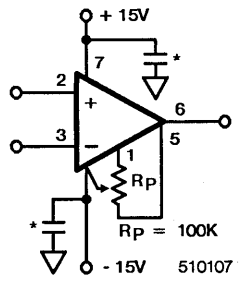
Operation At ±5V Supply

The HA-5101/11 performs well at V_{CC} = ±5V exhibiting typical characteristics as listed below:

I_{CC}	3.7	mA
V_{IO}	0.5	mA
I_{BIAS}	56	nA
A_{VOL} (V_O = ±3V)	106	KV/V
V_{OUT}	3.7	V
I_{OUT}	13	mA
CMRR (ΔV_{CM} = ±2.5V)	90	dB
PSRR (ΔV_{CC} = 0.5V)	90	dB
Unity Bandwidth (5101)	10	MHz
GBW (5111)	100	MHz
Slew Rate (5101)	7	V/µs
Slew Rate (5111)	40	V/µs

Offset Adjustment

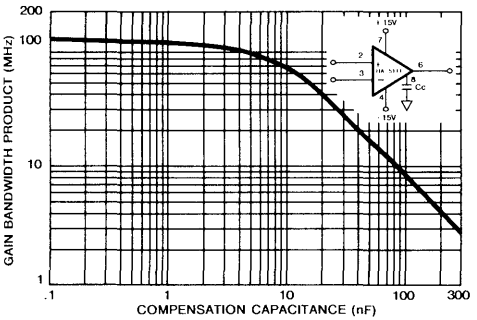
The following is the recommended V_{IO} adjust configuration:



* Proper decoupling is always recommended, 0.1µF high quality capacitor should be at or very near the devices's supply pins.

Compensation

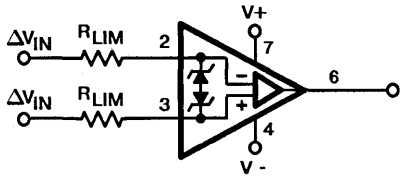
An external compensation capacitor can be used with the HA-5111 connected between pin 8 and ground (or V-, V+ not Recommended). A plot of gain bandwidth product vs. compensation capacitor has been included as a design aid. The capacitor should be a high frequency type mounted near the device leads to minimize parasitics.



Input Protection

The HA-5101/11 has built-in back-to-back protection diodes which will limit the differential input voltage to approximately 7V. If the 5101/11 will be used in conditions where that voltage may be exceeded, then current limiting resistors must be used. No more than 25mA should be allowed to flow in the HA-5101/11's input.

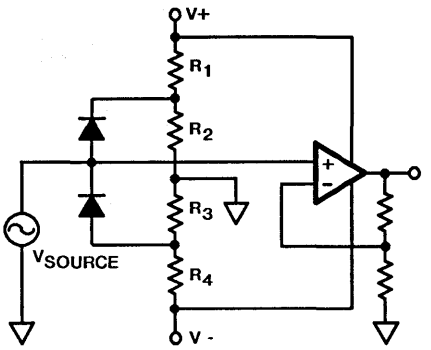
Comparator Circuit



Choose RLIM Such That: $\frac{(\Delta V_{IN}MAX - 7V)}{25mA} \leq 2RLIM$

Output Saturation

When an op amp is overdriven, output devices can saturate and sometimes take a long time to recover. Saturation can be avoided (sometimes) by using circuits such as:



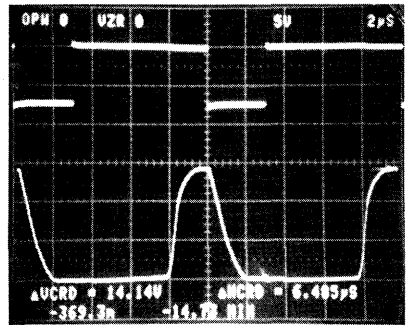
If saturation cannot be avoided the HA-5101/11 recovers from a 25% overdrive in about 6.5µs (see photos).

Applications Information (Continued)

TOP: Input
BOTTOM: Output, 5V/Div., 2μs/Div.

INPUT

OUTPUT



Output is overdriven negative and recovers in 6μs.

Die Characteristics

Transistor Count 54

Die Dimensions ..... 69 x 69 x 19 mils
(1800 x 1800 x 480μm)

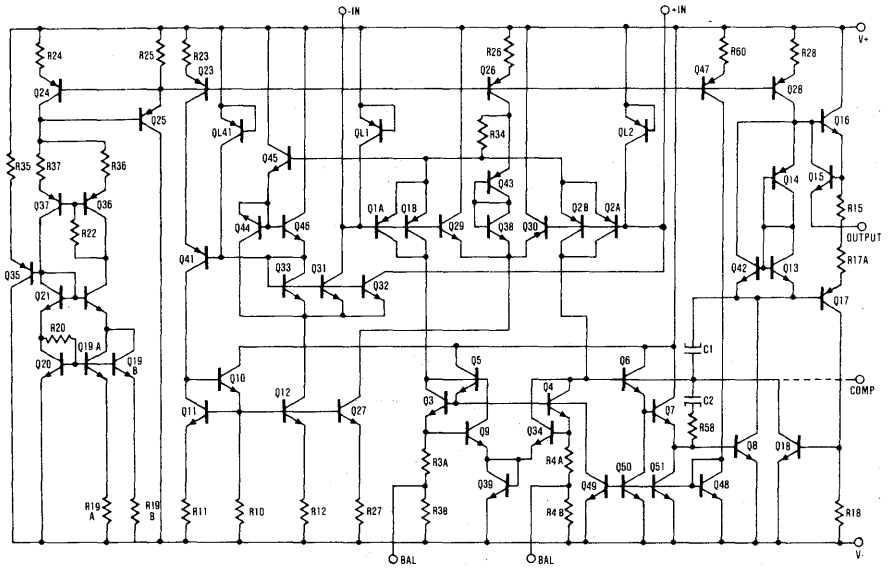
Substrate Potential* ..... V- or Float

Process ..... Bipolar DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-5101/5111 (-2/-5/-7)	192	52
HA2-5101/5111 (/883)	158	48
HA3-5101/5111 (-5)	80	29
HA7-5101/5111 (-2/-5/-7)	190	102
HA7-5101/5111 (/883)	136	61
HA9P5101/5111 (-5/-9)	160	42

* The Substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Schematic


-IN
+IN
V+
V-
OUTPUT
COMP
BAL
BAL
R24
R25
R23
Q23
Q24
Q25
R26
Q26
R60
Q47
R28
Q28
Q16
QL4T
QL1
QL2
R34
Q45
Q43
R35
R37
R36
Q37
Q36
R22
Q44
Q46
Q1A
Q1B
Q29
Q38
Q30
Q2B
Q2A
Q14
Q15
R15
Q41
Q33
Q31
Q32
Q42
Q13
R17A
Q35
Q21
Q17
R20
Q19A
Q20
Q19B
C1
Q10
Q5
Q6
Q11
Q12
Q27
Q3
Q4
Q7
C2
R58
Q9
Q34
Q8
Q18
R3A
R4A
Q39
Q49
Q50
Q51
Q48
R19A
R19B
R11
R10
R12
R27
R38
R4B
R18

HARRIS HA-5102/04/12/14

Low Noise High Performance Operational Amplifiers

June 1990

Features

- Low Noise ..... 4.3nV/√Hz
- Wide Bandwidth ..... 8MHz (Compensated)
  60MHz (Uncompensated)
- High Slew Rate ..... 3V/μs (Compensated)
  20V/μs (Uncompensated)
- Low Offset Voltage 0.5mV
- Available in Duals or Quads

Applications

- High Q, Active Filters
- Audio Amplifiers
- Instrumentation Amplifiers
- Integrators
- Signal Generators
- For Further Design Ideas, See App. Note 554.

Description

Low noise and high performance are key words describing HA-5102/04/12/14. These general purpose amplifiers offer an array of dynamic specifications ranging from a 3V/μs slew rate and 8MHz bandwidth (5102/04) to 20V/μs slew rate and 60MHz gain-bandwidth-product (HA-5112/14). Complementing these outstanding parameters is a very low noise specification of 4.3nV/√Hz at 1kHz.

Fabricated using the Harris high frequency DI process, these operational amplifiers also offer excellent input specifications such as a 0.5mV offset voltage and 30nA offset current. Complementing these specifications are 108dB open loop gain and 108dB channel separation. Consuming a very modest amount of power (90mW/package for duals and 150mW/package for quads), HA-5102/04/12/14 also provide 15mA of output current.

This impressive combination of features make this series of amplifiers ideally suited for designs ranging from audio amplifiers and active filters to the most demanding signal conditioning and instrumentation circuits.

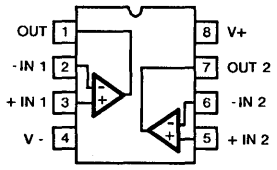
These operational amplifiers are available in dual or quad form with industry standard pinouts allowing for immediate inter-changeability with most other dual and quad operational amplifiers.

HA-5102	Dual, Comp.	HA-5104	Quad, Comp.
HA-5112	Dual, Uncomp.	HA-5114	Quad, Uncomp.

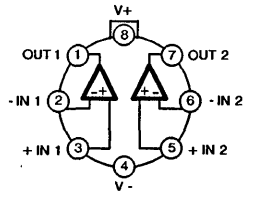
Each of these products are available in -2 (-55°C to +125°C), -5 and -7 (0°C to +75°C), -9 (-40°C to +85°C) or /883 grades. Refer to the /883 data sheet for military product.

Pinouts

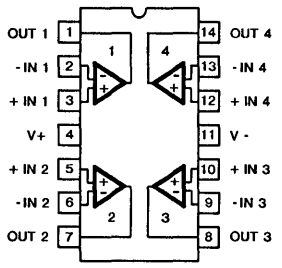
HA3-5102/5112 (PLASTIC MINI-DIP)
HA7-5102/5112 (CERAMIC MINI-DIP)
TOP VIEW



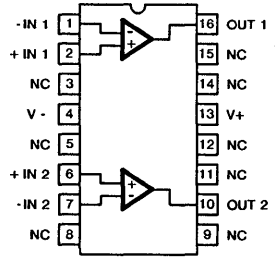
HA2-5102/5112 (TO-99 METAL CAN)
TOP VIEW



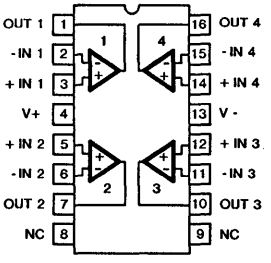
HA1-5104/5114 (CERAMIC DIP)
HA3-5104/5114 (PLASTIC DIP)
TOP VIEW



HA9P5102/5112 (SOIC)
TOP VIEW



HA9P5104/5114 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage ..... ±7V
Input Voltage (Note 2) ..... ±15.0V
Output Short Circuit Duration (Note 3) ..... Indefinite
Power Dissipation (Note 4) 880mW

Operating Temperature Ranges

HA-5102/5104/5112/5114-2 ..... -55°C ≤ T_A ≤ +125°C
HA-5102/5104/5112/5114-5 ..... -0°C ≤ T_A ≤ +75°C
HA-5102/5104/5112/5114-9 ..... -40°C ≤ T_A ≤ +85°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C

Electrical Specifications V+ = 15V D.C., V- = -15V D.C., Unless Otherwise Specified

PARAMETER	TEMP	HA-5102-2,-5 HA-5112-2,-5			HA-5104-2,-5 HA-5114-2,-5			HA-5102-9 HA-5112-9			HA-5104-9 HA-5114-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS														
Offset Voltage	+25°C	-	0.5	2.0	-	0.5	2.5	-	0.5	2.0	-	0.5	2.5	mV
	Full	-	-	2.5	-	-	3.0	-	-	2.5	-	-	3.0	mV
Offset Voltage Average Drift	Full	-	3	-	-	3	-	-	3	-	-	3	-	µV/°C
Bias Current	+25°C	-	130	200	-	130	200	-	130	200	-	130	200	nA
	Full	-	-	325	-	-	325	-	-	500	-	-	500	nA
Offset Current	+25°C	-	30	75	-	30	75	-	30	75	-	30	75	nA
	Full	-	-	125	-	-	125	-	-	125	-	-	125	nA
Input Resistance	+25°C	-	500	-	-	500	-	-	500	-	-	500	-	kΩ
Common Mode Range	Full	±12	-	-	±12	-	-	±12	-	-	±12	-	-	V
TRANSFER CHARACTERISTICS														
Large Signal Voltage Gain	+25°C	100	250	-	100	250	-	80	250	-	80	250	-	kV/V
(Note 5)	Full	100	-	-	100	-	-	80	-	-	80	-	-	kV/V
Common Mode Rejection Ratio (Note 6)	Full	86	95	-	86	95	-	80	95	-	80	95	-	dB
Small Signal Bandwidth HA-5102/5104 (A_V = 1)	+25°C	-	8	-	-	8	-	-	8	-	-	8	-	MHz
Gain Bandwidth Product HA-5112/5114 (A_V = 10)	+25°C	-	60	-	-	60	-	-	60	-	-	60	-	MHz
Channel Separation (Note 7)	+25°C	-	108	-	-	108	-	-	108	-	-	108	-	dB
OUTPUT CHARACTERISTICS														
Output Voltage Swing (R_L = 10K)	Full	±12	±13	-	±12	±13	-	±12	±13	-	±12	±13	-	V
(R_L = 2K)	Full	±10	±12	-	±10	±12	-	±10	±12	-	±10	±12	-	V
Output Current (Note 8)	Full	±10	±15	-	±10	±15	-	±7	±15	-	±7	±15	-	mA
Full Power Bandwidth (Note 9)														
HA-5102/5104	+25°C	16	47	-	16	47	-	16	47	-	16	47	-	kHz
HA-5112/5114	+25°C	191	318	-	191	318	-	191	318	-	191	318	-	kHz
Output Resistance	+25°C	-	110	-	-	110	-	-	110	-	-	110	-	Ω
STABILITY														
Minimum Stable Closed Loop Gain														
HA-5102/5104	Full	1	-	-	1	-	-	1	-	-	1	-	-	V/V
HA-5112/5114	Full	10	-	-	10	-	-	10	-	-	10	-	-	V/V

Electrical Specifications (Continued) V+ = 15V D.C., V- = -15V D.C., Unless Otherwise Specified

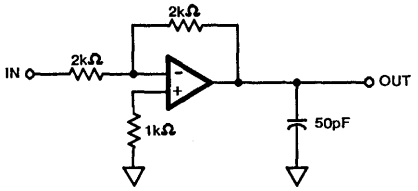
PARAMETER	TEMP	HA-5102-2, -5 HA-5112-2, -5			HA-5104-2, -5 HA-5114-2, -5			HA-5102-9 HA-5112-9			HA-5104-9 HA-5114-9			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE (Note 10)														
Rise Time														
HA-5102/5104	+25°C	-	108	200	-	108	200	-	108	200	-	108	200	ns
HA-5112/5114	+25°C	-	48	100	-	48	100	-	48	100	-	48	100	ns
Overshoot														
HA-5102/5104	+25°C	-	20	35	-	20	35	-	20	35	-	20	35	%
HA-5112/5114	+25°C	-	30	40	-	30	40	-	30	40	-	30	40	%
Slew Rate														
HA-5102/5104	+25°C	±1	±3	-	±1	±3	-	±1	±3	-	±1	±3	-	V/μs
HA-5112/5114	+25°C	±12	±20	-	±12	±20	-	±12	±20	-	±12	±20	-	V/μs
Settling Time (Note 11)														
HA-5102/5104	+25°C	-	4.5	-	-	4.5	-	-	4.5	-	-	4.5	-	μs
HA-5112/5114	+25°C	-	0.6	-	-	0.6	-	-	0.6	-	-	0.6	-	μs
NOISE CHARACTERISTICS														
Input Noise Voltage (Note 12)														
f = 10Hz	+25°C	-	9	17	-	9	17	-	9	17	-	9	17	$nV/\sqrt{Hz}$
f = 1kHz	+25°C	-	4.3	6.0	-	4.3	6.0	-	4.3	6.0	-	4.3	6.0	$nV/\sqrt{Hz}$
Input Noise Current (Note 12)														
f = 10Hz	+25°C	-	5.1	12	-	5.1	12	-	5.1	12	-	5.1	12	$pA/\sqrt{Hz}$
f = 1kHz	+25°C	-	0.57	3	-	0.57	3	-	0.57	3	-	0.57	3	$pA/\sqrt{Hz}$
Broadband Noise Voltage														
f = DC to 30kHz	+25°C	-	870	-	-	870	-	-	870	-	-	870	-	nVrms
POWER SUPPLY CHARACTERISTICS														
Supply Current														
HA-5102/5112	+25°C	-	3.0	5.0	-	3.0	5.0	-	3.0	5.0	-	3.0	5.0	mA
HA-5104/5114	+25°C	-	5.0	6.5	-	5.0	6.5	-	5.0	6.5	-	5.0	6.5	mA
Power Supply Rejection Ratio (Note 6)	Full	86	100	-	86	100	-	80	100	-	80	100	-	dB

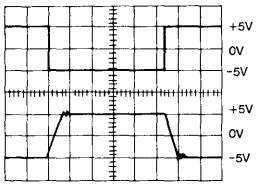
NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages < ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 9.6mW/°C above T_A = +25°C.
5. V_{OUT} = ±10V, R_L = 2K
6. V_{CM} = ±5.0V
7. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak to peak; R_S = 1kΩ. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
8. Output current is measured with V_{OUT} = ±5V.
9. Full power bandwidth is guaranteed by equation:
   $$\text{Full power bandwidth} = \frac{\text{Slew Rate}}{2\pi\ V\text{peak}}$$
10. Refer to Test Circuits section of the data sheet.
11. Settling time is measured to 0.1% of final value for a 1 volt input step, and A_V = -10 for HA-5112/5114, and a 10 volt input step, A_V = -1 for HA-5102/5104.
12. Sample tested.

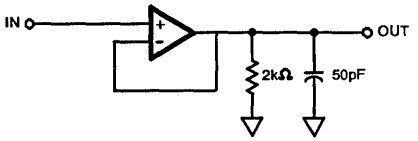
Test Circuits

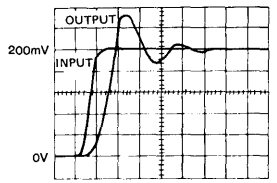
LARGE SIGNAL RESPONSE CIRCUIT
Volts: 5V/Div., Time: 5µs/Div. (A_V = -1)
HA-5102/5104



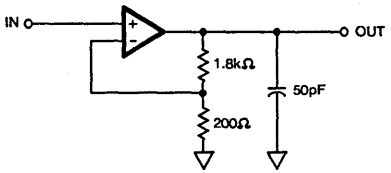


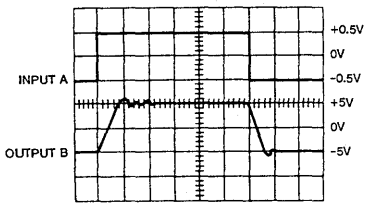
SMALL SIGNAL RESPONSE CIRCUIT
Volts: 40mV/Div., Time: 50ns/Div. (A_V = +1)
HA-5102/5104



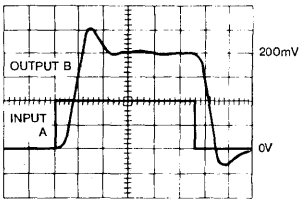


LARGE AND SMALL SIGNAL RESPONSE CIRCUIT
HA-5112/5114 (A_V = +10)



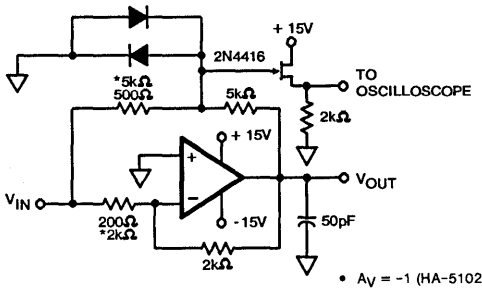


Volts: Input A: 0.5V/Div., Output B: 5V/Div.
Time: 50ns/Div.



Volts: Input A: 0.01V/Div., Output B: 50mV/Div.
Time: 50ns/Div.

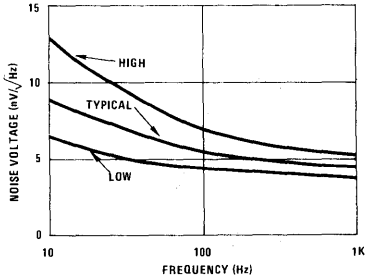
SETTLING TIME CIRCUIT



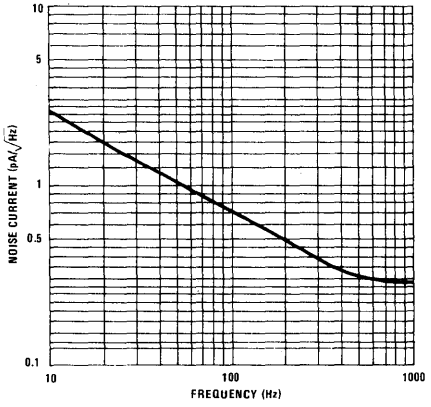
- A_V = -1 (HA-5102/5104), *A_V = -10 (HA-5112/5114)
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional, HP5082-2810 recommended.

Typical Performance Curves

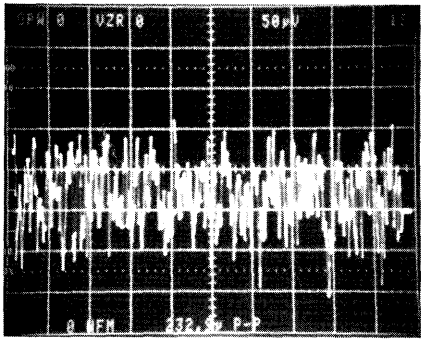
INPUT NOISE VOLTAGE DENSITY
V_{CC} = ±15V, T_A = +25°C



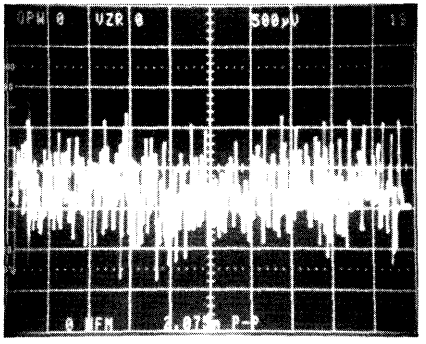
INPUT NOISE CURRENT DENSITY
V_{CC} = ±15V, T_A = +25°C



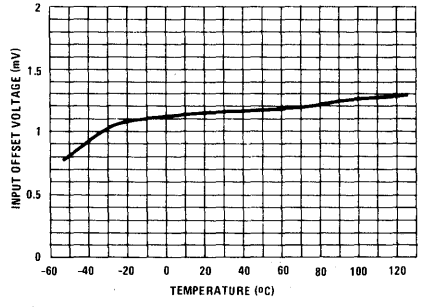
0.1Hz TO 10Hz NOISE
V_{CC} = ±15V, T_A = +25°C
50µV/Div., 1s/Div., A_V = 1000 V/V
Input Noise = 0.232µVp-p



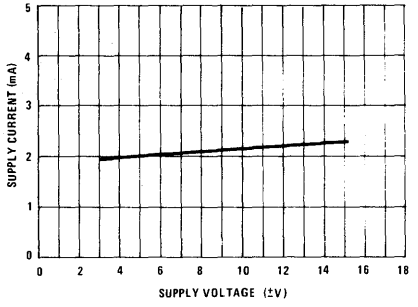
0.1Hz TO 1MHz NOISE
V_{CC} = ±15V, T_A = +25°C
500µV/Div., 1s/Div., A_V = 1000 V/V
Total Output Noise = 2.075µVp-p



V_{IO} vs. TEMPERATURE
V_{CC} = ±15V

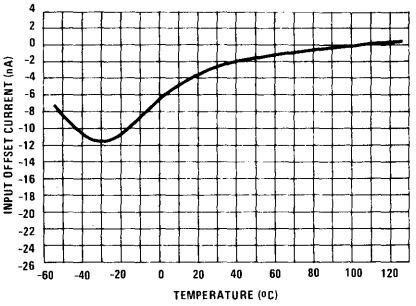


V_{IO} vs. V_{CC}
T_A = +25°C

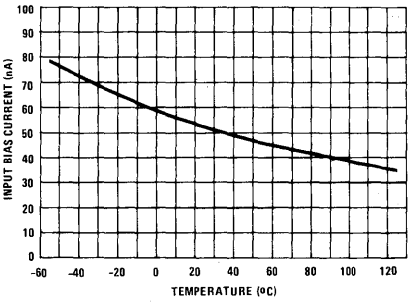


Typical Performance Curves (Continued)

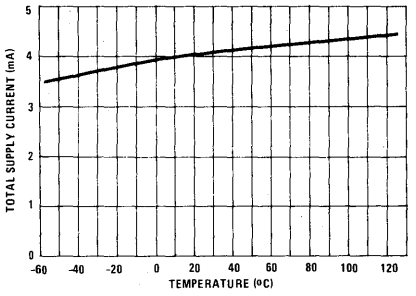
I_{IO} vs. TEMPERATURE
V_{CC} = ±15V



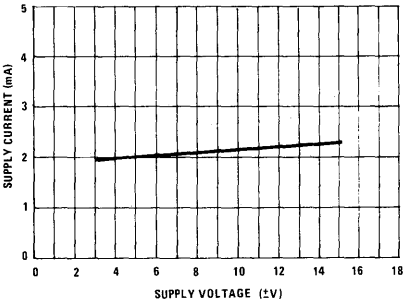
IBIAS vs. TEMPERATURE
V_{CC} = ±15V



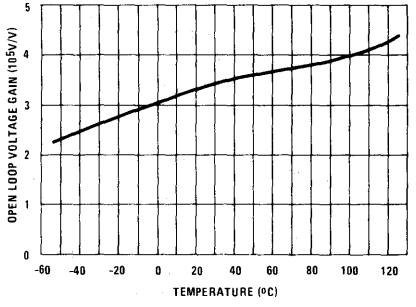
I_{CC} vs. TEMPERATURE
V_{CC} = ±15V, I_{OUT} = 0



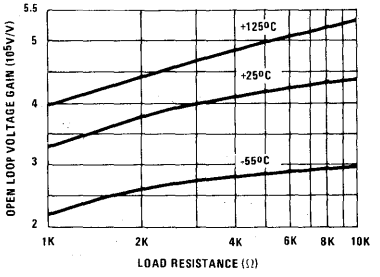
I_{CC} vs. V_{CC}
T_A = +25°C, I_{OUT} = 0



A_{VOL} vs. TEMPERATURE
V_{CC} = ±15V, ΔV_O = ±10V, R_L = 2K

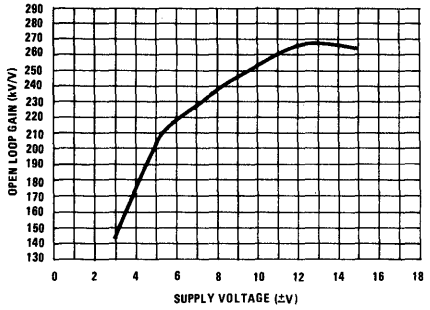


A_{VOL} vs. LOAD RESISTANCE
V_O = ±10V, V_{CC} = ±15V, T_A = +25°C

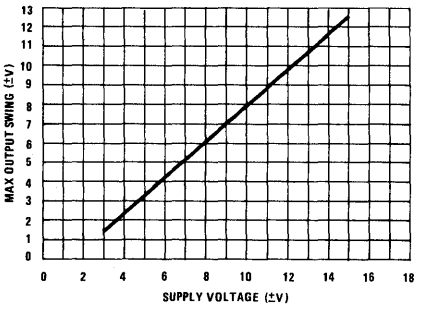


Typical Performance Curves (Continued)

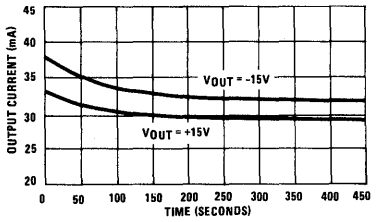
A_{VOL} vs. V_{CC}
$T_A = +25^oC$, $R_L = 2K$



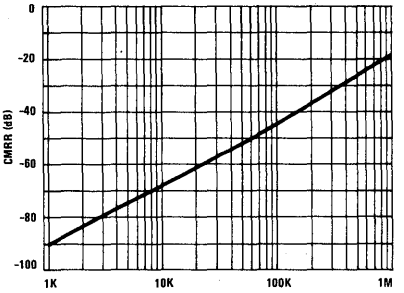
V_{OUT} vs. V_{CC}
$T_A = +25^oC$, $R_L = 2K$



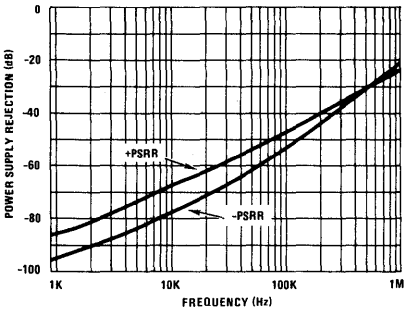
OUTPUT SHORT-CIRCUIT CURRENT vs. TIME
$V_{CC} = \pm 15V$, $T_A = +25^oC$



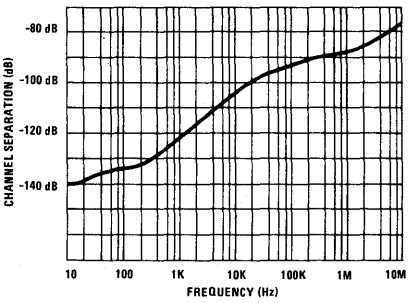
CMRR vs. FREQUENCY



PSRR vs. FREQUENCY

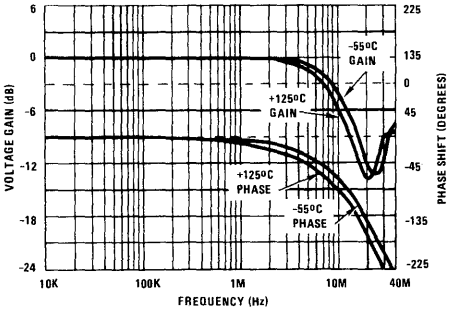


HA-5104 CHANNEL SEPARATION vs. FREQUENCY
$10Hz \leq f \leq 10MHz$

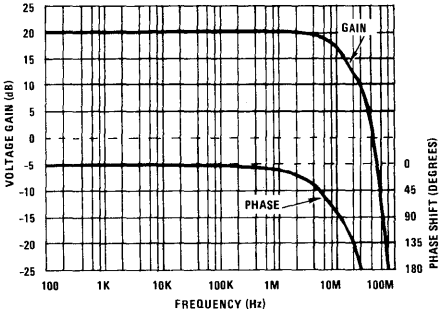


Typical Performance Curves (Continued)

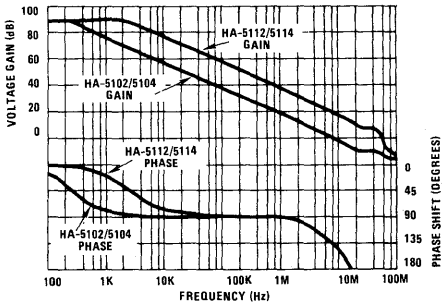
HA-5104/02 UNITY GAIN FREQUENCY RESPONSE
V_{CC} = ±15V, R_L = 2K, C_L = 50pF



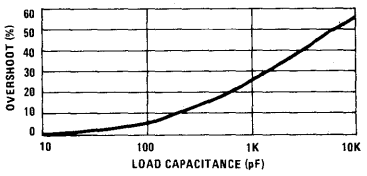
HA-5112/14 FREQUENCY RESPONSE
A_{VCL} = 10, T_A = +25°C, R_L = 2K, C_L = 50pF



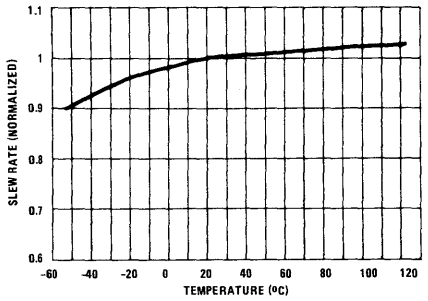
OPEN LOOP GAIN vs. FREQUENCY
V_{CC} = ±15V, R_L = 2K, C_L = 50pF, T_A = +25°C



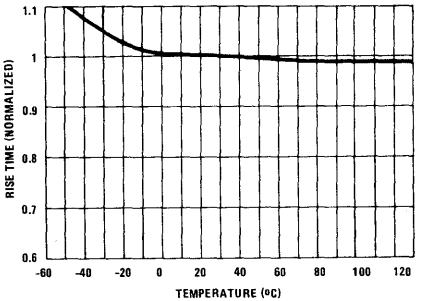
SMALL SIGNAL OVERSHOOT vs. CLOAD
V_{CC} = ±15V, T_A = +25°C, R_L = 2K



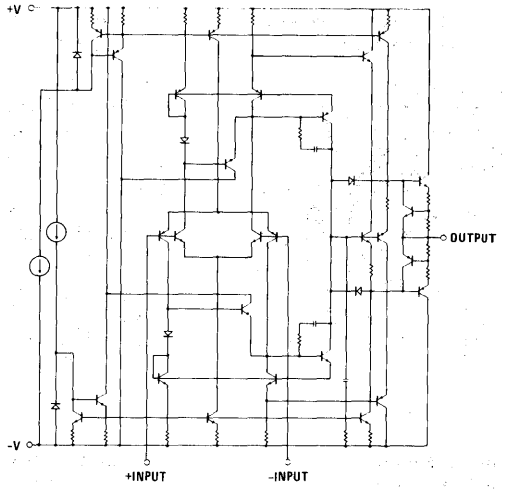
SLEW RATE vs. TEMPERATURE
R_L = 2K, C_L = 50pF, V_{CC} = ±15V



RISE TIME vs. TEMPERATURE
R_L = 2K, C_L = 50pF, V_{CC} = ±15V



Simplified Schematic



Die Characteristics

Transistor Count
- HA-5102/5112 93
- HA-5104/5114 175

Die Dimensions

HA-5102/5112 ..... 98.4 x 67.3 x 19 mils (2500 x 1710 x 480µm)

HA-5104/5114 ..... 99.6 x 95.3 x 19 mils (2530 x 2420 x 480µm)

Substrate Potential* ..... V-

Process ..... Bipolar-DI

Passivation ..... Nitride

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA1-5104 (-2, -5, -7)	103	35
HA1-5104 (/883)	78	25
HA2-5102/5112 (-2, -5, -7)	174	48
HA2-5102/5112 (/883)	134	40
HA3-5102/5112 (-5)	80	20
HA3-5104/5114 (-5)	75	23
HA7-5102/5112 (-2, -5, -7)	163	82
HA7-5102/5112 (/883)	124	47
HA9P5102/5112	160	42
HA9P5104/5114	94	26

HARRIS

HA-5127

Ultra-Low Noise Presision Operational Amplifier

May 1990

Features

- High Speed 10V/μs
- Wide Unity Gain Bandwidth 8.5MHz
- Low Noise ..... 3nV/$\sqrt{Hz}$ at 1KHz
- Low VOS 10μV
- High CMRR 126dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Description

The HA-5127 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/$\sqrt{Hz}$) precision instrumentation performance with high speed (10V/μs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (10μV), wide unity gain-bandwidth (8.5MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140mW of power.

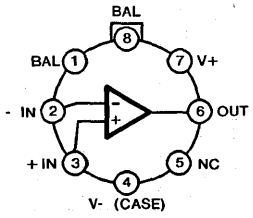
Using the HA-5127 allows designers to minimize errors while maximizing speed and bandwidth.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5127's qualities include instrumentation amplifiers, pulse amplifiers, audio preamplifiers, and signal conditioning circuits.

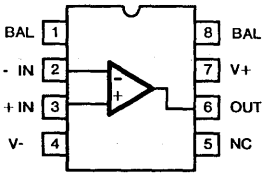
This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37. The HA-5127 is available in TO-99 Metal Can and Ceramic 8 pin Mini-DIPs. For the military grade product, refer to the HA-5127/883 data sheet.

Pinouts

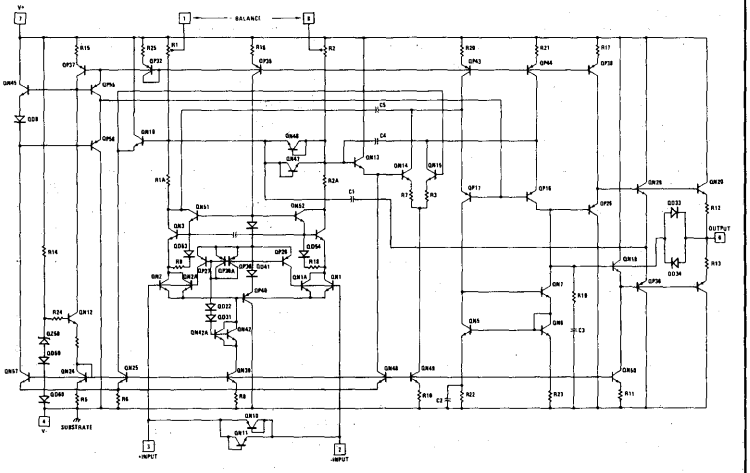
HA2-5127 (TO-99 METAL CAN)
TOP VIEW



HA7-5127 (CERAMIC MINI-DIP)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V- Terminals ..... ±22V
Differential Input Voltage (Note 2) ..... ±0.7V
Internal Power Dissipation 500mW
Output Current ..... Full Short Circuit Protection

Operating Temperature Ranges

HA-5127/27A-2 ..... -55°C ≤ T_A ≤ +125°C
HA-5127/27A-5 ..... 0°C ≤ T_A ≤ +75°C
Storage Temperature Range ..... -65°C ≤ T_A ≤ +150°C
Maximum Junction Temperature ..... +175°C

Electrical Specifications V+ = 15V, V- = -15V, C_L < 50pF, R_S < 100Ω

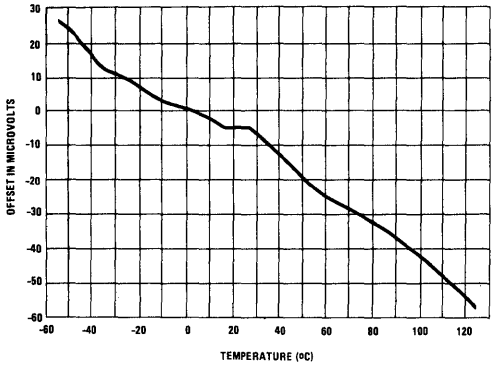
PARAMETER	TEMP	HA-5127A MIN	HA-5127A TYP	HA-5127A MAX	HA-5127 MIN	HA-5127 TYP	HA-5127 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	10	25	-	30	100	µV
	Full	-	30	60	-	70	300	µV
Average Offset Voltage Drift	Full	-	0.2	0.6	-	0.4	1.8	µV/°C
Bias Current	+25°C	-	±10	±40	-	±15	±80	nA
	Full	-	±20	±60	-	±35	±150	nA
Offset Current	+25°C	-	7	35	-	12	75	nA
	Full	-	15	50	-	30	135	nA
Common Mode Range	Full	±10.3	±11.5	-	±10.3	±11.5	-	V
Differential Input Resistance (Note 3)	+25°C	1.5	6	-	0.8	4	-	MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 4)	+25°C	-	0.08	0.18	-	0.09	0.25	µVp-p
Input Noise Voltage Density (Note 5) f_O = 10Hz	+25°C	-	3.5	5.5	-	3.8	8.0	$nV/\sqrt{Hz}$
f_O = 30Hz		-	3.1	4.5	-	3.3	5.6	$nV/\sqrt{Hz}$
f_O = 1000Hz		-	3.0	3.8	-	3.2	4.5	$nV/\sqrt{Hz}$
Input Noise Current Denisty (Note 5) f_O = 10Hz	+25°C	-	1.7	4.0	-	1.7	-	$pA/\sqrt{Hz}$
f_O = 30Hz		-	1.0	2.3	-	1.0	-	$pA/\sqrt{Hz}$
f_O = 1000Hz		-	0.4	0.6	-	0.4	0.6	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 7)	+25°C	1000	1800	-	700	1500	-	V/mV
	Full	600	1200	-	300	800	-	V/mV
Common Mode Rejection Ratio (Note 7)	Full	114	126	-	100	120	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	V/V
Unity-Gain-Bandwidth	+25°C	5	8.5	-	5	8.5	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing R_L = 600Ω	+25°C	±10.0	±11.5	-	±10.0	±11.5	-	V
R_L = 2KΩ	Full	±11.7	±13.8	-	±11.4	±13.5	-	V
Full Power Bandwidth (Note 8)	+25°C	111	160	-	111	160	-	kHz
Output Resistance, Open Loop	+25°C	-	70	-	-	70	-	V
Output Current	+25°C	16.5	25	-	16.5	25	-	mA
TRANSIENT RESPONSE (Note 9)								
Rise Time	+25°C	-	-	150	-	-	150	ns
Slew Rate (Note 11)	+25°C	7	10	-	7	10	-	V/µs
Settling Time (Note 10)	+25°C	-	1.5	-	-	1.5	-	µs
Overshoot	+25°C	-	20	40	-	20	40	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	3.5	-	-	3.5	-	mA
	Full	-	-	4.0	-	-	4.0	mA
Power Supply Rejection Ratio (Note 12)	Full	-	2	4	-	16	51	µV/V

NOTES:

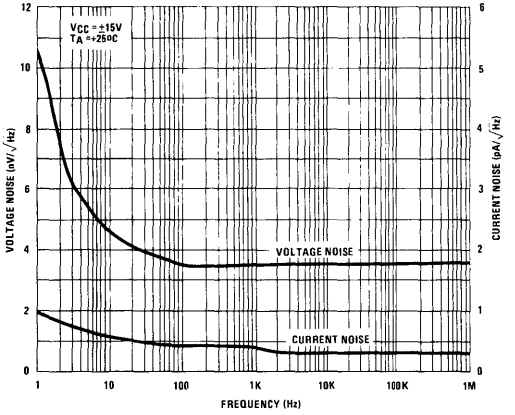
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. Sample tested.
6. V_{OUT} = ±10V, R_L = 2KΩ
7. V_{CM} = ±10V
8. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
9. Refer to Test Circuits section of the data sheet.
10. Settling time is specified to 0.1% of final value for a 10V output step and A_V = -1.
11. V_{OUT} = 10V Step
12. V_S = ±4V to ±18V

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

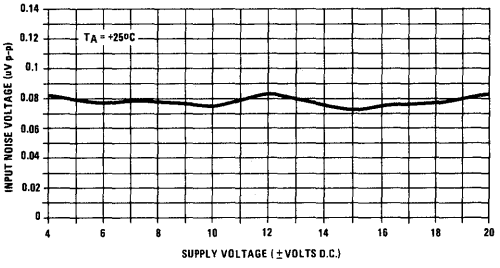
OFFSET VOLTAGE TYPICAL DRIFT vs. TEMPERATURE



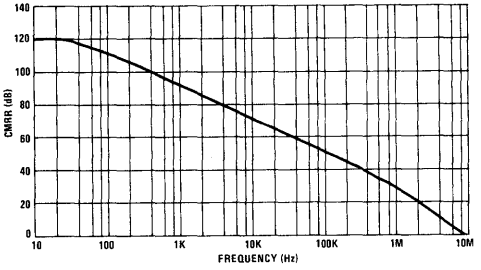
NOISE CHARACTERISTICS



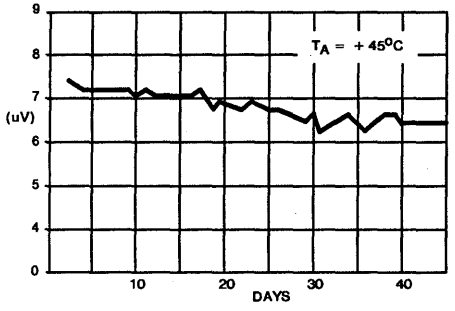
NOISE vs. SUPPLY VOLTAGE



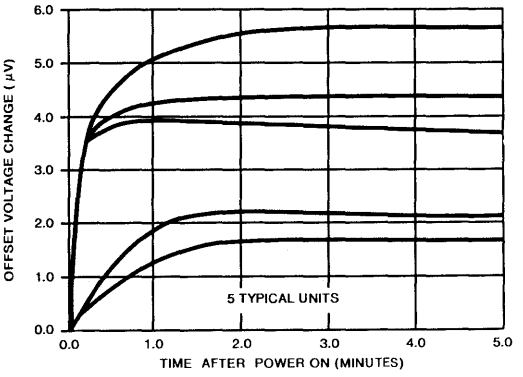
CMRR vs. FREQUENCY



OFFSET VOLTAGE DRIFT vs. TIME

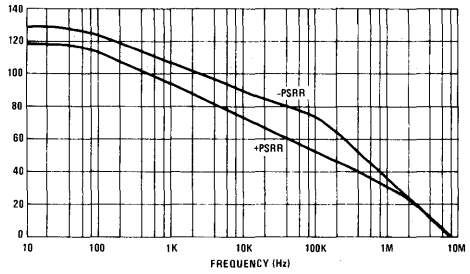


OFFSET VOLTAGE WARM UP DRIFT

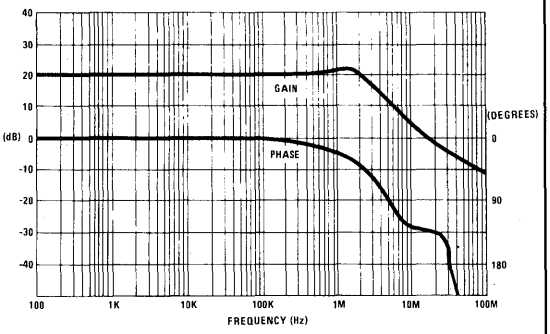


Typical Performance Curves Unless Otherwise Specified: TA = +25°C, V_{SUPPLY} = ±15V

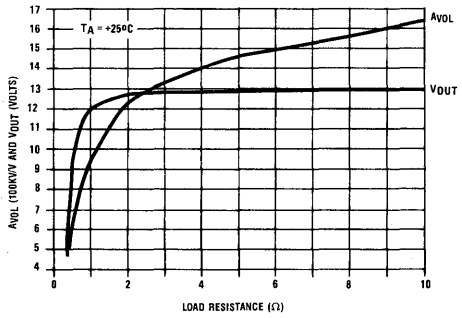
PSRR vs. FREQUENCY



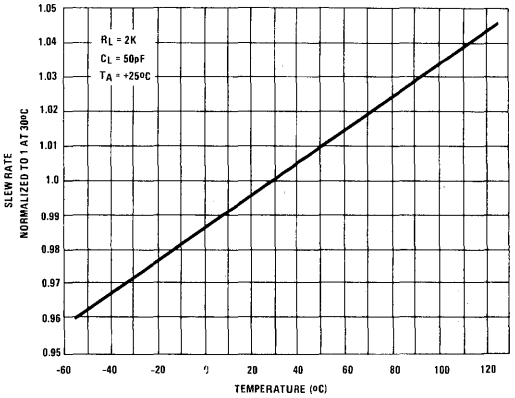
CLOSED LOOP GAIN AND PHASE vs. FREQUENCY



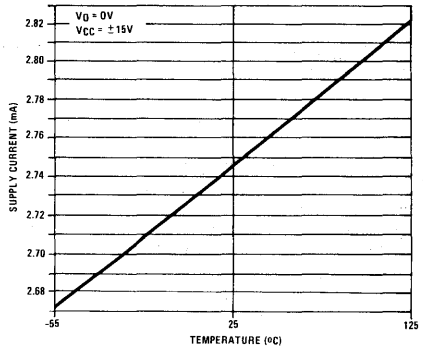
A_{VOL} AND V_{OUT} vs. LOAD RESISTANCE



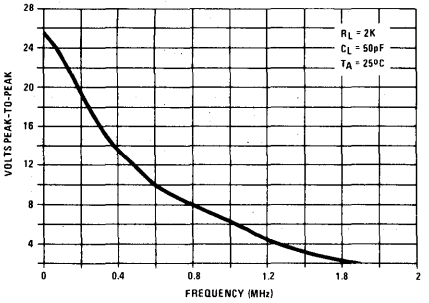
NORMALIZED SLEW RATE vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



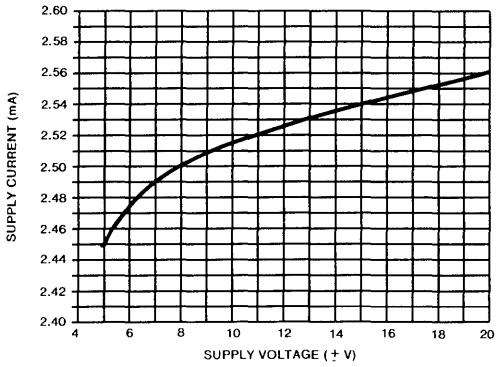
V_{OUT} MAX vs. FREQUENCY UNDISTORTED SINEWAVE OUTPUT



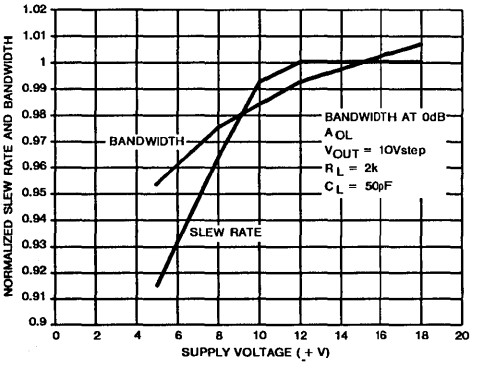
Typical Performance Curves

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

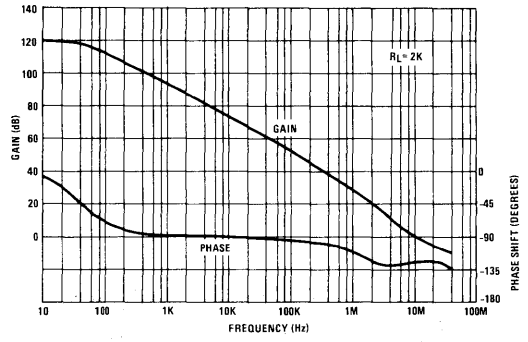
SUPPLY CURRENT vs. SUPPLY VOLTAGE



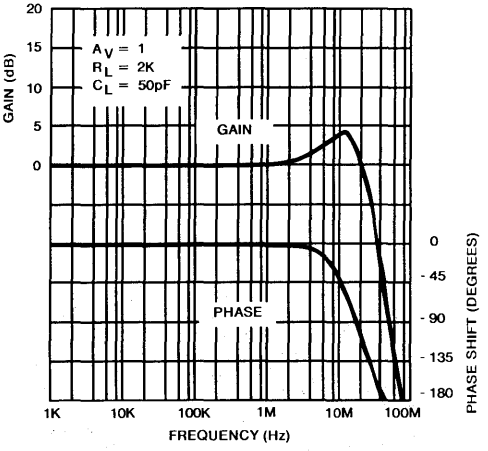
BANDWIDTH AND SLEW RATE vs. SUPPLY VOLTAGE



OPEN LOOP GAIN AND PHASE vs. FREQUENCY

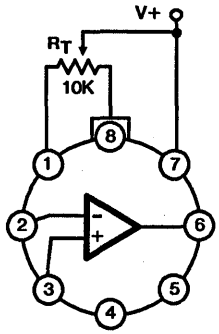


CLOSED LOOP GAIN AND PHASE vs. FREQUENCY



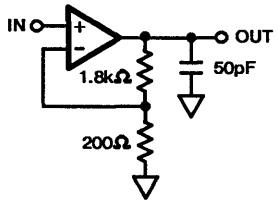
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$

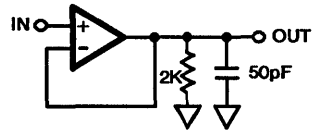
SUGGESTED OFFSET VOLTAGE ADJUSTMENT



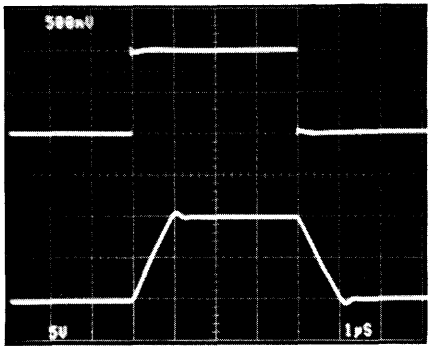
Tested Offset Adjustment Range is $|V_{OS} +1mV|$ minimum referred to output. Typical range is ±4mV with $R_T = 10k\Omega$.

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUITS



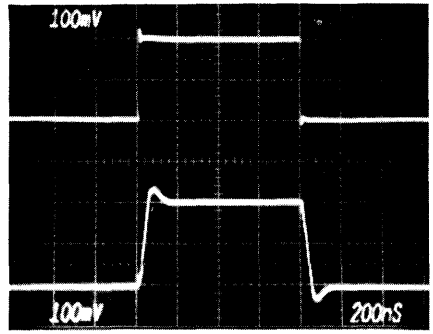


LARGE SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 0.5V/Div.)
(Output = 5V/Div.)
Horizontal Scale: (Time = 1μs/Div.)

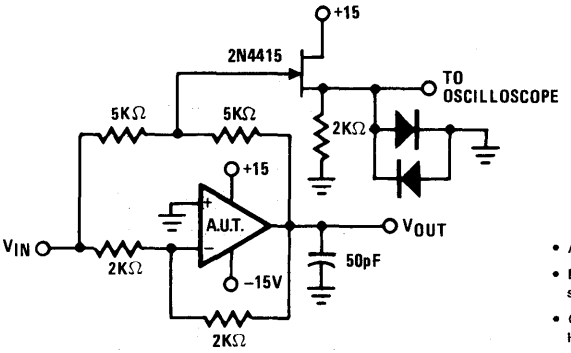
SMALL SIGNAL RESPONSE



Vertical Scale: (Volts: 100mV/Div.)
Horizontal Scale: (200ns/Div.)

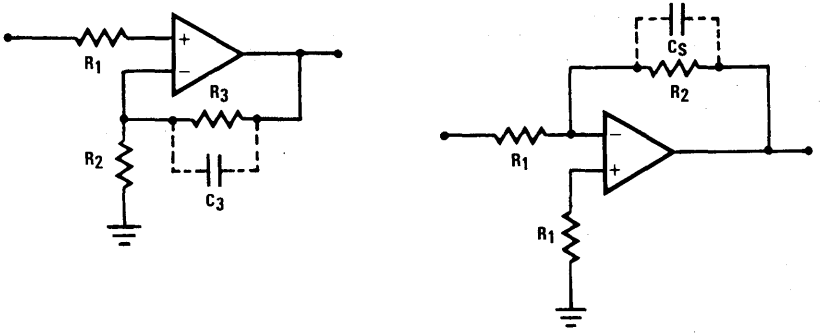
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

SETTLING TIME TEST CIRCUIT



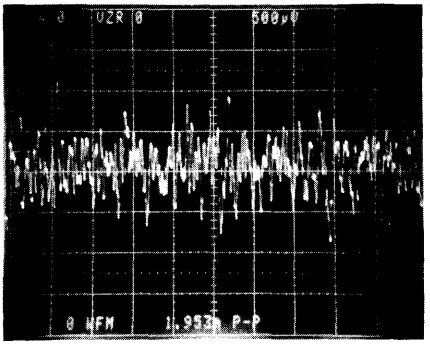
- $A_V = -1$
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended

SUGGESTED STABILITY CIRCUITS



Low resistances are preferred for low noise applications as a 1KΩ resistor has $4nV/\sqrt{Hz}$ of thermal noise. Total resistances of greater than 10KΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

0.1Hz TO 10Hz NOISE WITH A_{CL} = 25,000V/V



Horizontal Scale = 1sec/Div.
Vertical Scale = 0.002μV/Div.
0.08μVp-p

Die Characteristics

Transistor Count 63
Die Dimensions ..... 65 x 104.3 x 19 mils (1700μm x 2600μm x 480μm)
Substrate Potential* ..... V-
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA7-5127 Ceramic Mini-DIP	160	79
HA2-5127 TO-99 Metal Can	172	48

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS

HA-5130/35

NOT RECOMMENDED FOR NEW DESIGNS SEE HA-5177

Precision Operational Amplifier

Features

- Low Offset Voltage 10μV
- Low Offset Voltage Drift ..... 0.4μV/°C
- Low Noise ..... 9nV/$\sqrt{Hz}$
- Open Loop Gain 140dB
- Unity Gain Bandwidth 2.5MHz
- All Bipolar Construction

Applications

- High Gain Instrumentation
- Precision Data Acquisition
- Precision Integrators
- Biomedical Amplifiers
- Precision Threshold Detectors

Description

The Harris HA-5130/5135 are precision operational amplifiers manufactured using a combination of key technological advancements to provide outstanding input characteristics.

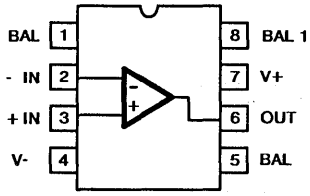
A Super Beta input stage is combined with laser trimming, dielectric isolation and matching techniques to produce 25μV (Maximum) input offset voltage and 0.4μV/°C input offset voltage average drift. Other features enhanced by this process include 9nV/$\sqrt{Hz}$ (Typ.) Input Noise Voltage, 1nA Input Bias Current and 140dB Open Loop Gain.

These features coupled with 120dB CMRR and PSRR make HA-5130/5135 an ideal device for precision DC instrumentation amplifiers. Excellent input characteristics in conjunction with 2.5MHz bandwidth and 0.8V/μs slew rate, makes this amplifier extremely useful for precision integrator and biomedical amplifier designs. These amplifiers are also well suited for precision data acquisition and for accurate threshold detector applications.

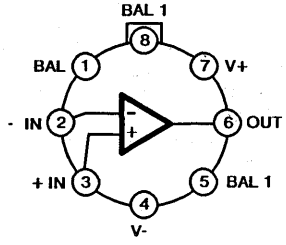
HA-5130/5135 is packaged in an 8 pin (TO-99) Metal Can and an 8 lead Cerdip and is pin compatible with many existing op amp configurations. It offers added features over the industry standard OP-07 in regards to bandwidth and slew rate specifications. For the military grade product, refer to the HA-5135/883 data sheet.

Pinouts

HA7-5130/5135 (CERAMIC MINI-DIP)
TOP VIEW

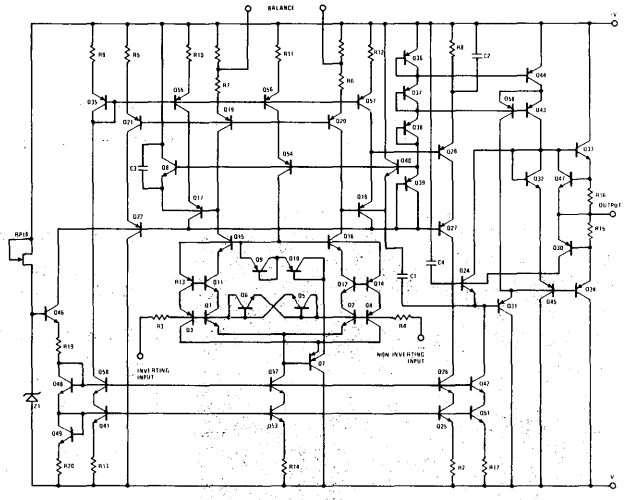


HA2-5130/5135 (TO-99 METAL CAN)
TOP VIEW



(Both BAL 1 Pins are Internally Connected)

Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage..... ±15.0V
Output Short Circuit Duration ..... Indefinite
Power Dissipation (Note 2)..... 300mW

Operating Temperature Ranges

HA-5130/5135-2 ..... $-55°C \leq T_A \leq +125°C$
HA-5130/5135-5 ..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$

Electrical Specifications V+ = +15V, V- = -15V

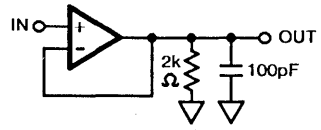
PARAMETER	TEMP	HA-5130-2/-5 MIN	HA-5130-2/-5 TYP	HA-5130-2/-5 MAX	HA-5135-2/-5 MIN	HA-5135-2/-5 TYP	HA-5135-2/-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	10	25	-	10	75	µV
	Full	-	50	60	-	50	130	µV
Average Offset Voltage Drift	Full	-	0.4	0.6	-	0.4	1.3	µV/°C
Bias Current	+25°C	-	±1	±2	-	±1	±4	nA
	Full	-	-	±4	-	-	±6	nA
Bias Current Average Drift	Full	-	0.02	0.04	-	0.02	0.04	nA/°C
Offset Current	+25°C	-	-	2	-	-	4	nA
	Full	-	-	4	-	-	5.5	nA
Offset Current Average Drift	Full	-	0.02	0.04	-	0.02	0.04	nA/°C
Common Mode Range	Full	±12	-	-	±12	-	-	V
Differential Input Resistance	+25°C	20	30	-	20	30	-	MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 3)	+25°C	-	-	0.6	-	-	0.6	μV_{p-p}
Input Noise Voltage Density (Note 3)	+25°C							
f_O = 10Hz		-	13.0	18.0	-	13.0	18.0	$nV/\sqrt{Hz}$
f_O = 100Hz		-	10.0	13.0	-	10.0	13.0	$nV/\sqrt{Hz}$
f_O = 1000Hz		-	9.0	11.0	-	9.0	11.0	$nV/\sqrt{Hz}$
Input Noise Current 0.1Hz to 10Hz (Note 3)	+25°C	-	15	30	-	15	30	pA_{p-p}
Input Noise Current Density (Note 3)	+25°C							
f_O = 10Hz		-	0.4	0.8	-	0.4	0.8	$pA/\sqrt{Hz}$
f_O = 100Hz		-	0.17	0.23	-	0.17	0.23	$pA/\sqrt{Hz}$
f_O = 1000Hz		-	0.14	0.17	-	0.14	0.17	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	120	140	-	120	140	-	dB
	Full	120	-	-	120	-	-	dB
Common Mode Rejection Ratio (Note 5)	Full	110	120	-	106	120	-	dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	0.6	2.5	-	0.6	2.5	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12	-	±10	±12	-	V
	Full	±10	-	-	±10	-	-	V
Full Power Bandwidth (Note 7)	+25°C	8	10	-	8	10	-	kHz
Output Current (Note 8)	+25°C	±15	±20	-	±15	±20	-	mA
Output Resistance (Note 8)	+25°C	-	45	-	-	45	-	Ω
TRANSIENT RESPONSE (Note 10)								
Rise Time	+25°C	-	340	-	-	340	-	ns
Slew Rate	+25°C	0.5	0.8	-	0.5	0.8	-	V/µs
Settling Time (Note 11)	+25°C	-	11	-	-	11	-	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	1.0	1.3	-	1.0	1.7	mA
Power Supply Rejection Ratio (Note 12)	Full	100	130	-	94	130	-	dB

NOTES:

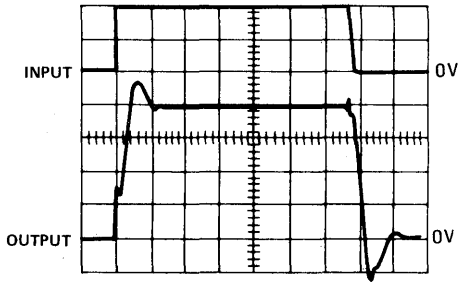
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Funtional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. Not tested. 90% of units meet or exceed these specifications.
4. V_{OUT} = ±10V; R_L = 2K. Gain dB = $20 \log_{10}$ Av ∴ 120dB = 1MV/V 140dB = 10MV/V
5. V_{CM} = ±10V DC
6. R_L = 600Ω.
7. R_L = 2K; Full power bandwidth guaranteed based on slew rate measurement using FPBW = $\frac{\text{SLEW RATE}}{2\pi V_{PEAK}}$
8. V_{OUT} = 10V
9. Output resistance measured under open loop conditions (f = 100Hz).
10. Refer to test circuits section of the data sheet.
11. Settling time is measured to 0.1p of final value for a 10V output step and A_V = -1.
12. V_{SUPPLY} = ±5V DC to ±20V DC.

Test Circuits

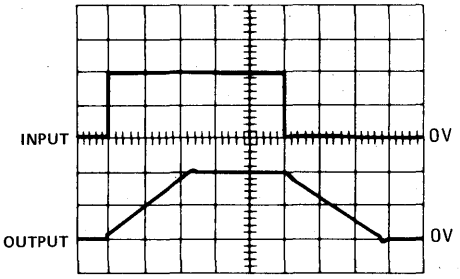
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



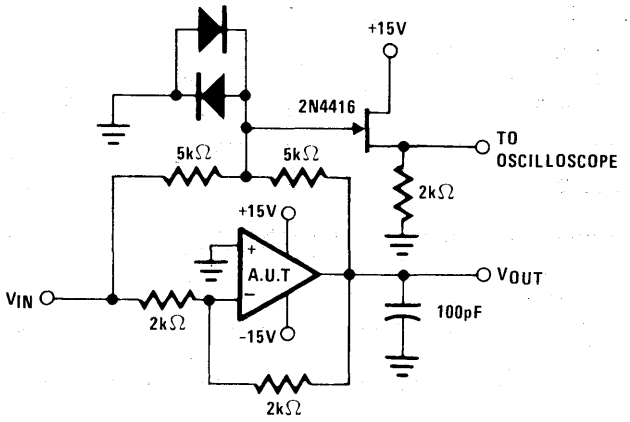
SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: 50mV/Div. Output)
(Volts: 100mV/Div. Input)
Horizontal Scale: (Time: 1μ/sDiv.)



LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: 5V/sDiv.)
Horizontal Scale: (Time: 5μs/Div.)



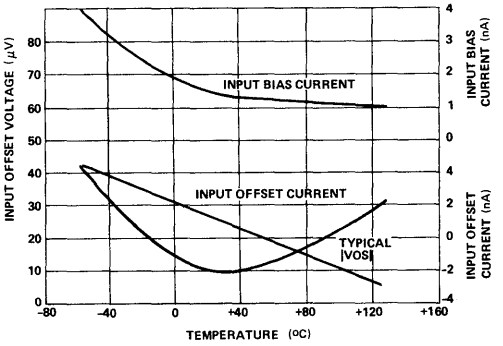
SETTLING TIME CIRCUIT



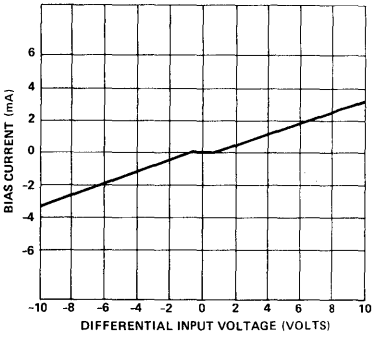
- $A_V = -1$.
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

Typical Performance Curves

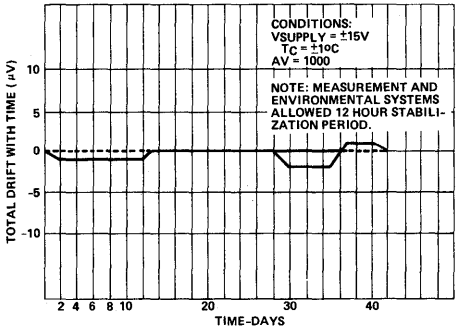
INPUT OFFSET VOLTAGE, INPUT BIAS AND OFFSET CURRENT vs. TEMPERATURE



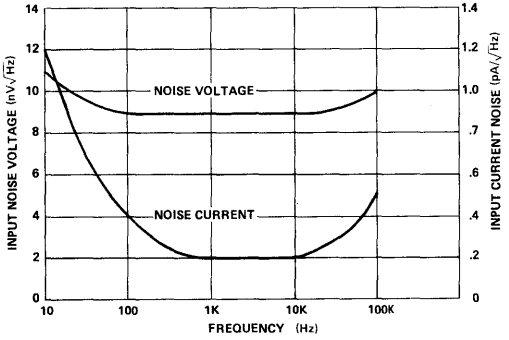
INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



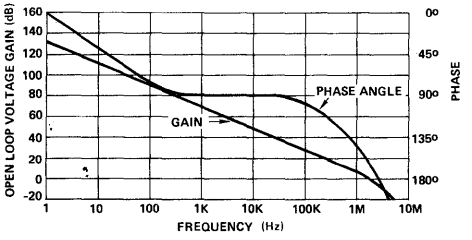
HA-5130 OFFSET VOLTAGE STABILITY vs. TIME



INPUT NOISE vs. FREQUENCY

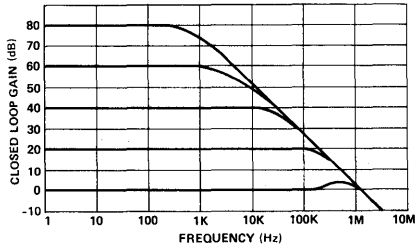


OPEN LOOP FREQUENCY RESPONSE

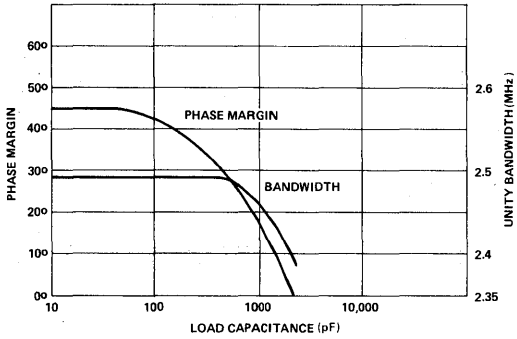


Typical Performance Curves (Continued)

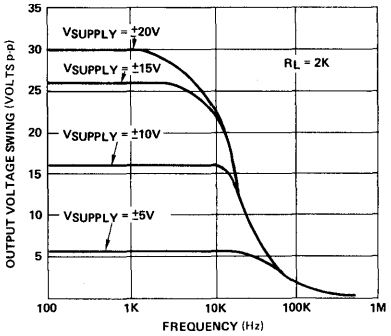
CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



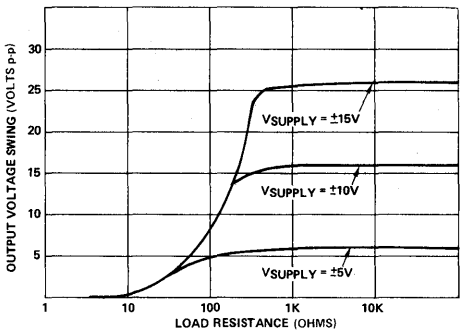
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



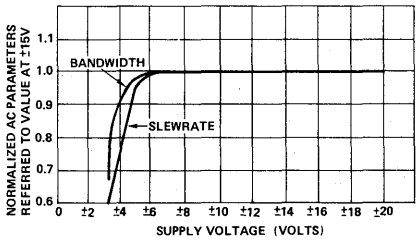
OUTPUT VOLTAGE SWING vs. FREQUENCY AND SUPPLY VOLTAGE



MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE AND SUPPLY VOLTAGE

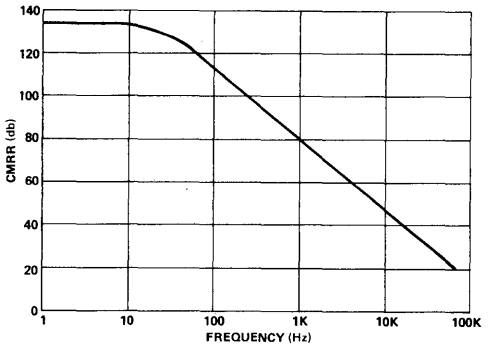


NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE

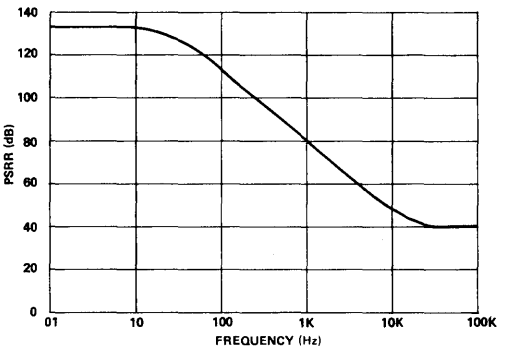


Typical Performance Curves (Continued)

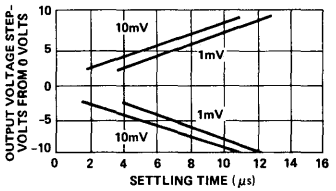
CMRR vs. FREQUENCY



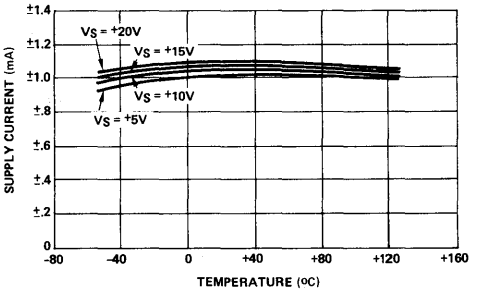
PSRR vs. FREQUENCY



SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



POWER SUPPLY CURRENT vs. TEMPERATURE AND SUPPLY VOLTAGE

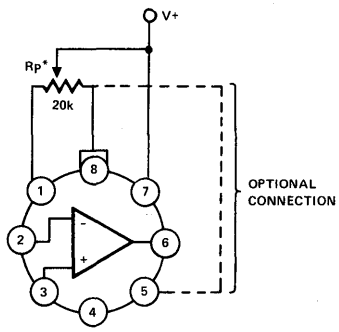


Applying the HA-5130/5135 Operational Amplifiers

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. CONSIDERATIONS FOR PROTOTYPING: The following list of recommendations are suggested for prototyping.
   - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces and implementation of moisture barriers when required is suggested.
   - Error voltages generated by theromocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuity from heat generating components is recommended.
   - Shielded cable input leads, guard rings and shield drivers are recommended for the most critical applications.
3. When driving large capacitive loads (> 500pF), as small value resistor (≈ 50Ω) should be connected in series with the output and inside the feedback loop.
4. OFFSET VOLTAGE ADJUSTMENT: A 20kΩ balance potentiometer is recommended if offset nulling is required. However, other potentiometer values such as 10kΩ, 50kΩ and 100kΩ may be used. The minimum adjustment range for given values is ±2mV.
5. SATURATION RECOVER: Input and output saturation recovery time is negligible in most applications. However, care should be exercised to avoid exceeding the absolute maximum ratings of the device.
6. DIFFERENTIAL INPUT VOLTAGES: Inputs are shunted with back-to-back diodes for overvoltage protection. In applications where differential input voltages in excess of 1V are applied between the inputs, the use of limiting resistors at the inputs is recommended.

Applications

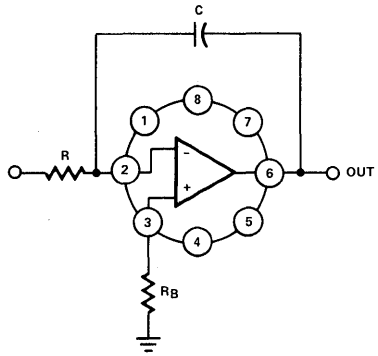
OFFSET NULLING CONNECTIONS



* Although R_P is shown equal to 20K, other values such as 50K, 100K and 1M may be used. Range of adjustment is approximately ±2.5mV. V_{OS} TC of the amplifier is optimized at minimal V_{OS}.

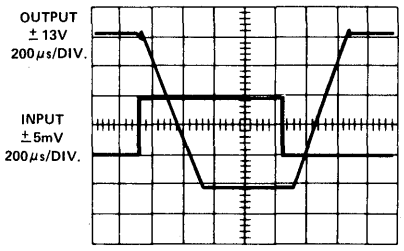
Tested Offset Adjustment is $|V_{OS} + 1mV|$ minimum referred to output.

PRECISION INTEGRATOR

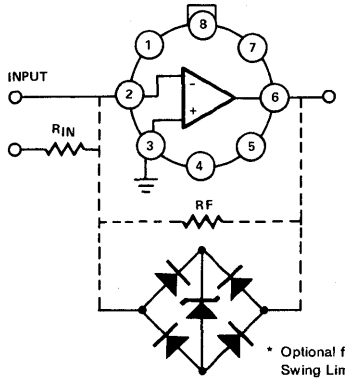


The excellent inputs and gain characteristics of HA-5130 are well suited for precision integrator applications. Accurate integration over seven decades of frequency using HA-5130, virtually nullifies the need for more expensive chopper-type amplifiers.

ZERO CROSSING DETECTOR

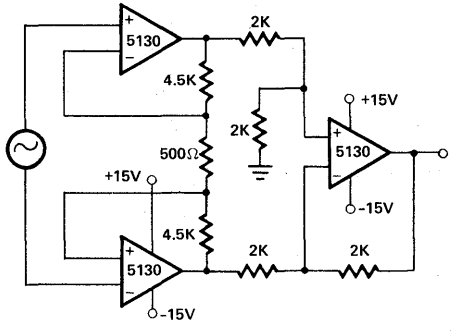


Low V_{OS} coupled with high open loop Gain, high CMRR and high PSRR make HA-5130 ideally suited for precision detector applications.



* Optional for Output Swing Limiting

PRECISION INSTRUMENTATION AMPLIFIER (A_V = 100)



HARRIS

HA-5134

May 1990

Precision Quad Operational Amplifier

Features

- Low Offset Voltage ..... Max 200μV
- Low Offset Voltage Drift ..... Max 2μV/°C
- Offset Voltage Match (5134A).. Full Temp. Max 250μV
- High Channel Separation 120dB
- Low Noise ..... 7nV/$\sqrt{Hz}$
- Wide Unity Gain Bandwidth 4MHz
- High CMRR/PSRR (Typ)..... 120dB
- Dielectric Isolation

Applications

- Instrumentation Amplifiers
- State-Variable Filters
- Precision Integrators
- Threshold Detectors
- Precision Data Acquisition Systems
- Low-Level Transducer Amplifiers

Description

The HA-5134 is a precision quad operational amplifier that is pin compatible with the OP-400, LT1014, OP11, RM4156, and LM148 as well as the HA-4741. Each amplifier features guaranteed maximum values for offset voltage of 200μV, offset voltage drift of 2μV/°C, and offset current of 75nA over the full military temperature range while CMRR/PSRR is guaranteed greater than 94dB and A_{VOL} is guaranteed above 750kV/V from -55°C to +125°C.

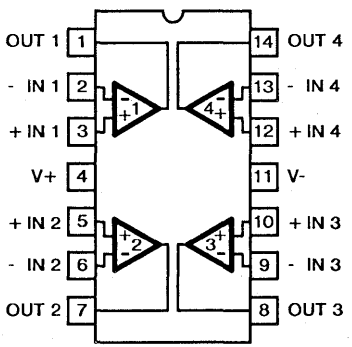
Precision performance of the HA-5134 is enhanced by a noise voltage density of 7nV/$\sqrt{Hz}$ at 1kHz, noise current density of 2pA/$\sqrt{Hz}$ at 1kHz and channel separation of 120dB. Each unity-gain stable quad amplifier is fabricated using the dielectric isolation process to assure performance in the most demanding applications.

The HA-5134 is ideal for compact circuits such as instrumentation amplifiers, state-variable filters, and low-level transducer amplifiers. Other applications include precision data acquisition, precision integrators, and accurate threshold detectors in designs where board space is a limitation.

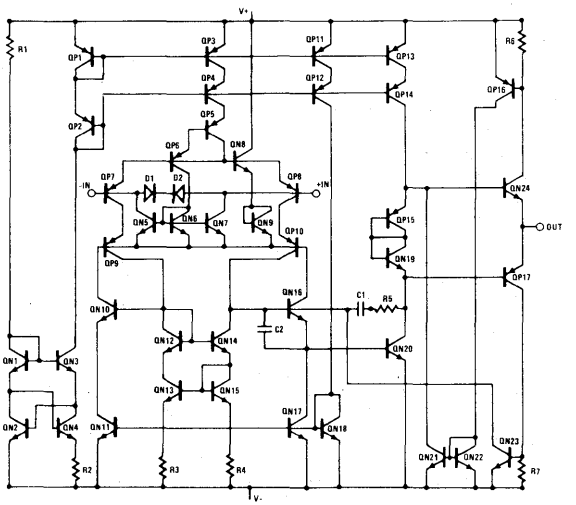
The HA-5134-2 has guaranteed operation from -55°C to +125°C and can be ordered as a military grade part. The HA-5134-5 is guaranteed from 0°C to +75°C and all devices are available in ceramic dual-in-line packages. For military grade product, refer to the HA-5134/883 Data Sheet.

Pinout

HA1-5134 (CERAMIC DIP)
TOP VIEW



Schematic (Each Amplifier)



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

TA = +25°C Unless Otherwise Stated
Voltage Between V+ and V- Terminals 40.0V
Differential Input Voltage (Note 2) ..... ±6.0V
Internal Power Dissipation (Note 3) 800mW
Output Current ..... Full Short Circuit Protection
Voltage at any Op Amp Terminal ..... V+, V-
Maximum Junction Temperature ..... +175°C

Operating Temperature Ranges

HA-5134A/5134-2 ..... $-55^{o}C \leq T_A \leq +125^{o}C$
HA-5134A/5134-5 ..... $0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range ..... $-65^{o}C \leq T_A \leq +150^{o}C$

Electrical Specifications $V_{CC} = \pm15V$, $R_{LOAD} = 2K$, $C_{LOAD} = 50pF$, $R_S \leq 100\Omega$ Unless Otherwise Specified

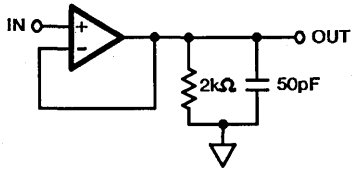
PARAMETER	TEMP	HA-5134A-2/-5 MIN	HA-5134A-2/-5 TYP	HA-5134A-2/-5 MAX	HA-5134-2/-5 MIN	HA-5134-2/-5 TYP	HA-5134-2/-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	50	100	-	50	200	µV
	Full	-	75	250	-	75	350	µV
Average Offset Voltage Drift	Full	-	0.3	1.2	-	0.3	2	µV/°C
Offset Voltage Match	Full	-	-	250	-	-	-	µV
Bias Current	+25°C	-	±10	±25	-	±10	±50	nA
	Full	-	±20	±50	-	±20	±75	nA
Offset Current	+25°C	-	10	25	-	10	50	nA
	Full	-	15	50	-	15	75	nA
Average Offset Current Drift	Full	-	0.05	-	-	0.05	-	nA/°C
Common Mode Range	Full	±10	-	-	±10	-	-	V
Differential Input Resistance	+25°C	-	30	-	-	30	-	MΩ
Input Noise Voltage (0.1Hz to 10Hz)	+25°C	-	0.2	-	-	0.2	-	µVp-p
Input Noise Voltage Density $f_O = 10Hz$	+25°C	-	10	-	-	10	-	$nV/\sqrt{Hz}$
$f_O = 100Hz$		-	7.5	-	-	7.5	-	$nV/\sqrt{Hz}$
$f_O = 1kHz$		-	7	-	-	7	-	$nV/\sqrt{Hz}$
Input Noise Current Density $f_O = 10Hz$	+25°C	-	3	-	-	3	-	$pA/\sqrt{Hz}$
$f_O = 100Hz$		-	1.5	-	-	1.5	-	$pA/\sqrt{Hz}$
$f_O = 1kHz$		-	1	-	-	1	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain	+25°C	1500	3000	-	1200	3000	-	V/mV
($V_{OUT} = \pm10V$)	Full	1000	2000	-	750	2000	-	V/mV
Common Mode Rejection Ratio	+25°C	115	120	-	100	120	-	dB
($V_{CM} = \pm10V$)	Full	110	115	-	94	115	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	V/V
Unity-Gain Bandwidth	+25°C	-	4	-	-	4	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing	Full	12	13.5	-	12	13.5	-	V
Output Current	+25°C	-	20	-	-	20	-	mA
Full Power Bandwidth (Note 4)	+25°C	12	16	-	12	16	-	kHz
Channel Separation ($V_{OUT} = \pm10V$)	+25°C	120	136	-	120	136	-	dB
TRANSIENT RESPONSE (Note 5)								
Rise Time (Note 6)	+25°C	-	200	400	-	200	400	ns
Slew Rate	+25°C	0.75	1.0	-	0.75	1.0	-	V/µs
Overshoot	+25°C	-	20	40	-	20	40	%
Settling Time (Note 7)	+25°C	-	13	-	-	13	-	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current (All Amps)	Full	-	6.5	8	-	6.5	8	mA
Power Supply Rejection Ratio (Note 8)	+25°C	110	120	-	100	120	-	dB
	Full	100	115	-	94	115	-	dB

NOTES:

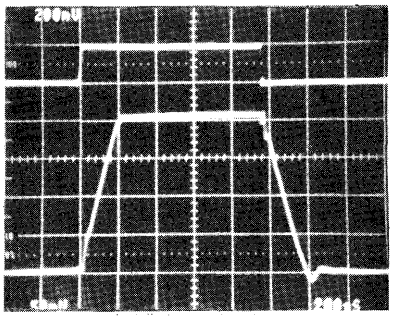
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 6V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. Derate at 10mW/°C for ambient temperatures greater than +95°C.
4. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$; $V_{peak} = 10V$
5. Refer to Test Circuits section of the data sheet.
6. Time from 10% to 90% of 200mV output step, $A_V = 1$.
7. Specified to 0.01% of a 10V step, $A_V = -1$.
8. $V_S = \pm5V$ to $\pm18V$.

Test Circuits

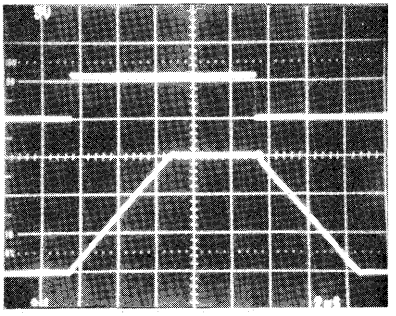
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



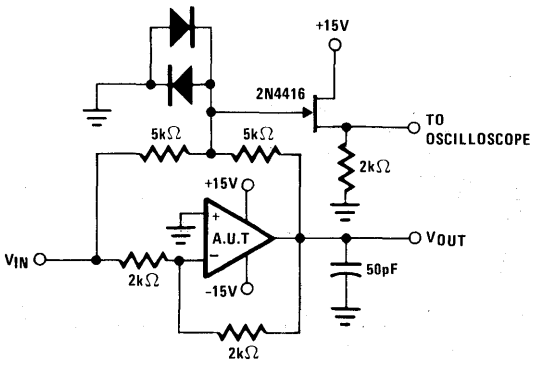
SMALL SIGNAL RESPONSE
Vertical: 50mV/Div. Horizontal: 200ns/Div.
$T_A = +25^oC$, $V_{CC} = \pm15V$
$A_V = +1$, $R_L = 2K$, $C_L = 50pF$



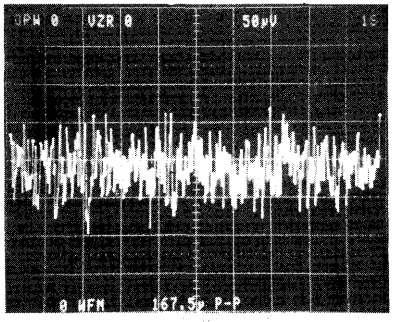
LARGE SIGNAL RESPONSE
Vertical: 2V/Div. Horizontal: 2µs/Div.
$T_A = +25^oC$, $V_{CC} = \pm15V$
$A_V = +1$, $R_L = 2K$, $C_L = 50pF$



SETTLING TIME CIRCUIT



PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz
$T_A = +25^oC$, $V_{CC} = \pm15V$, $A_V = 1000$

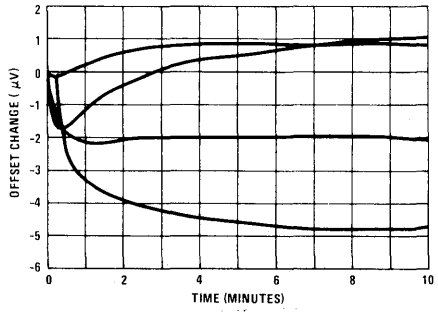


$en_{p-p} = 0.167\mu V_{p-p}$
0.05µV/Div., 1s/Div.

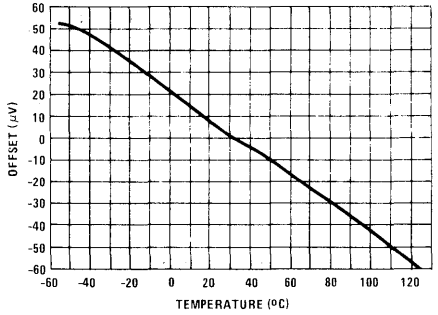
- $A_V = -1$.
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

Performance Curves

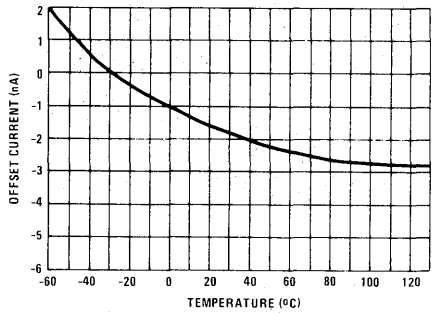
V_{IO} WARMUP DRIFT
T_A = +25°C, V_{CC} = ±15V



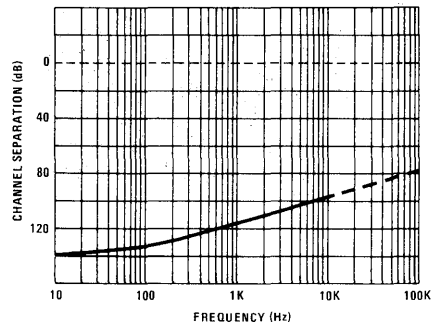
INPUT OFFSET VOLTAGE vs. TEMPERATURE



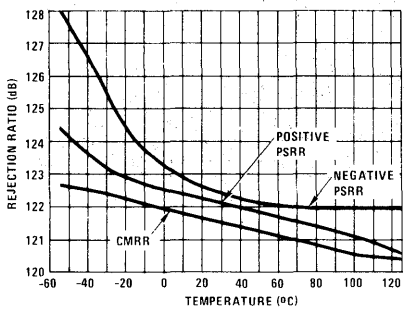
OFFSET CURRENT vs. TEMPERATURE
A_{CL} = +1, V_{CC} = ±15V



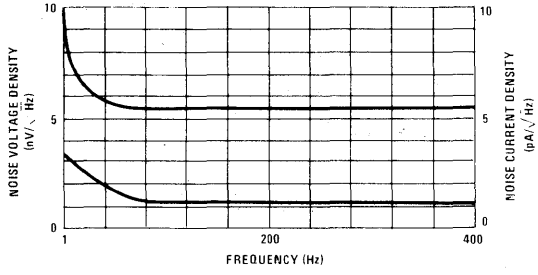
CHANNEL SEPARATION vs. FREQUENCY



REJECTION RATIOS vs. TEMPERATURE
V_{CC} = ±5V to ±20V, V_{CM} = ±10V

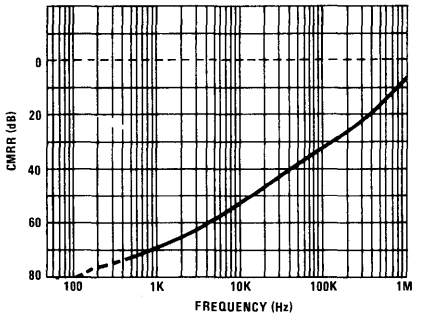


NOISE VOLTAGE DENSITY vs. FREQUENCY

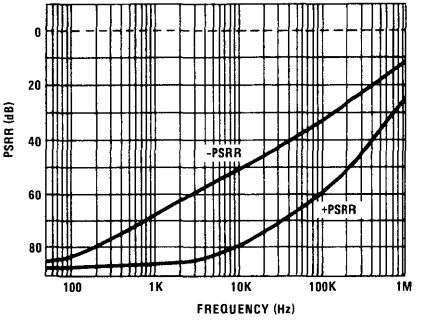


Performance Curves (Continued)

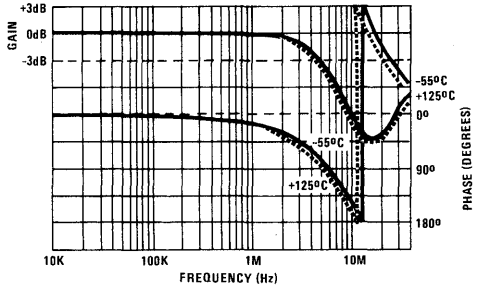
CMRR vs. FREQUENCY



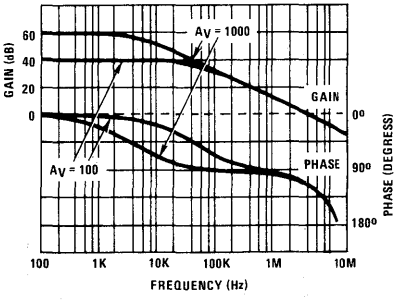
PSRR vs. FREQUENCY



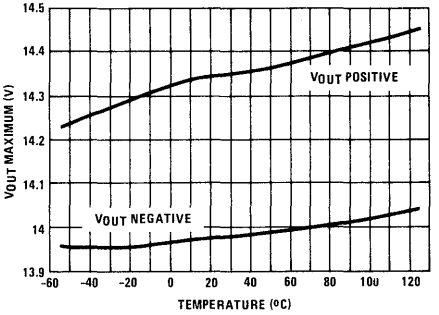
CLOSED-LOOP FREQUENCY RESPONSE vs. TEMPERATURE



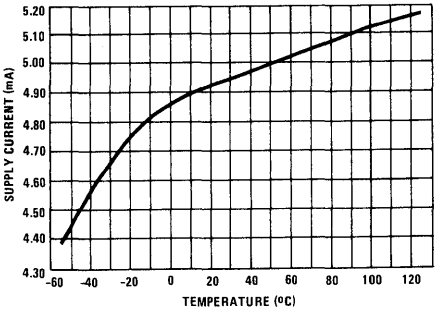
CLOSED-LOOP GAIN/PHASE vs. FREQUENCY
T_A = +25°C, V_{CC} = ±15V



MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE
R_{LOAD} = 2K, A_V = 1000, V_{IN} = ±2V



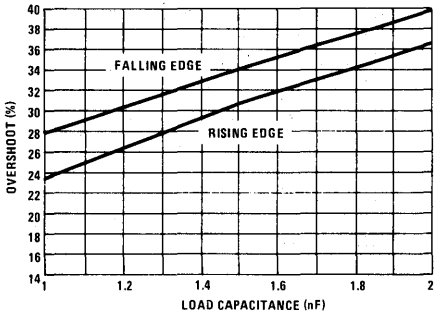
SUPPLY CURRENT vs. TEMPERATURE
V_{CC} = ±15V



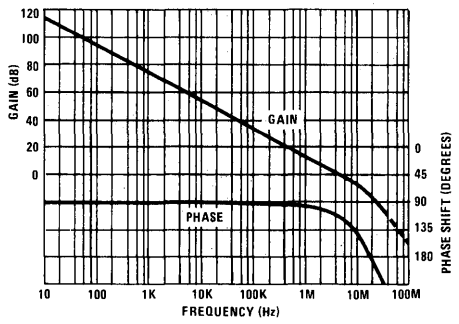
Performance Curves (Continued)

OVERSHOOT vs. C_{LOAD}

V_{CC} = ±15V, T_A = +25°C, A_V = 1, V_{OUT} = 200mV



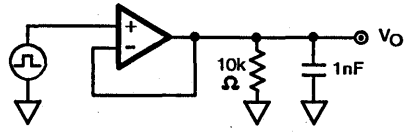
OPEN LOOP GAIN & PHASE vs. FREQUENCY

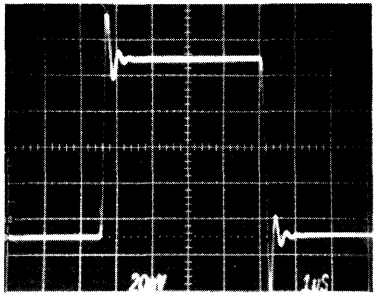


Applications Information

SMALL SIGNAL TRANSIENT RESPONSE

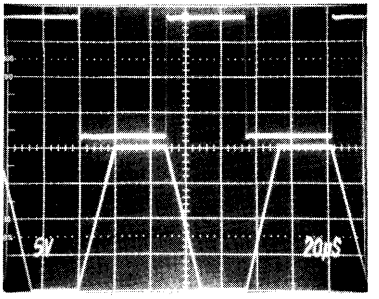
C_{LOAD} = 1nF





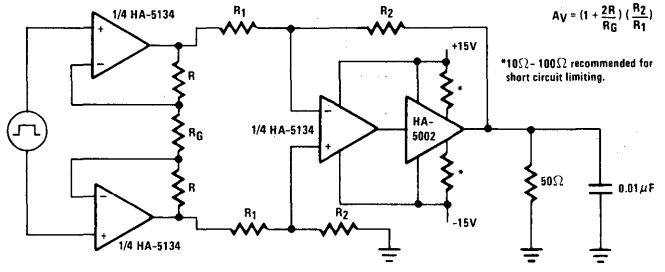
T_A = +25°C, V_{CC} = ±15V,
A_V = 1, R_L = 10K
20mV/Div, 1µs/Div.

TRANSIENT RESPONSE OF APPLICATION CIRCUIT #1



V_{OUT} = ±10V, R_{LOAD} = 50V
C_{LOAD} = 0.01mF, A_V = 3, V_{CC} = ±15V
Top: Input, 2V/Div., 20µs/Div. Bottom: Output, 5V/Div, 20µs/Div.

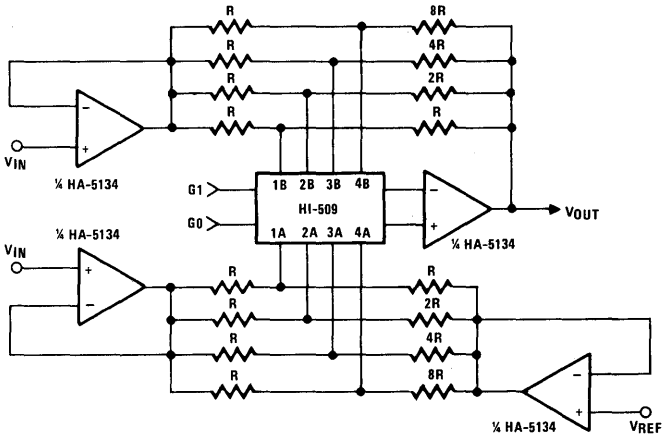
APPLICATION CIRCUIT #1:
INSTRUMENTATION AMPLIFIER WITH POWER OUTPUT



NOTE: When driving heavy loads the HA-5002 may contribute to thermal errors. Proper thermal shielding is recommended.

Applications Information (Continued)

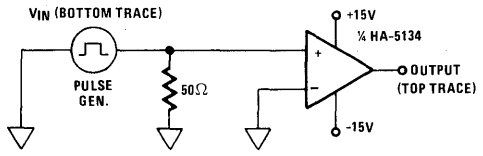
APPLICATION CIRCUIT #2: PROGRAMMABLE GAIN AMPLIFIER

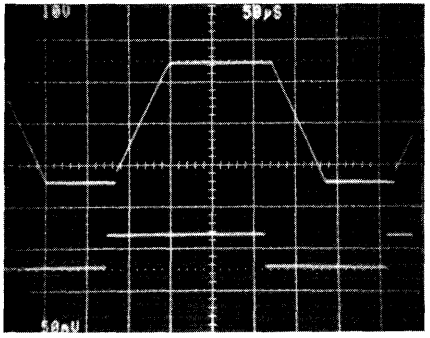


G_1	G_0	A_V
0	0	-1
0	1	-2
1	0	-4
1	1	-8

High A_{VOL} of HA-5134 reduces gain error.
Gain Error ≅ 0.004% @ A_V = 8

APPLICATION CIRCUIT #3: PRECISION COMPARATOR





Horizontal: 50µs/Div.
V_{IN} = ±25mV, V_{OUT} = ±14V

NOTE: If differential input voltages greater than 6V are present, input current must be limited to less than 25mA.

General Considerations

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01µF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. CONSIDERATIONS FOR PROTOTYPING: The following list of recommendations are suggested for prototyping.
   - Resolving low level signals requires minimizing leakage currents caused by external circuitry. Use of quality insulating materials, thorough cleaning of insulating surfaces and implementation of moisture barriers when required is suggested.
   - Error voltages generated by thermocouples formed between dissimilar metals in the presence of temperature gradients should be minimized. Isolation of low level circuitry from heat generating components is recommended.
   - Shielded cable input leads, guard rings and shield drivers are recommended for the most critical applications.

HARRIS

HA-5137

Ultra-Low Noise Precision Wideband Operational Amplifier

May 1990

Features

- High Speed 20V/μs
- Wide Gain Bandwidth ($A_V \geq 5$) 63MHz
- Low Noise ..... 3nV/$\sqrt{Hz}$ at 1KHz
- Low VOS 10μV
- High CMRR 126dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers
- For Further Design Ideas See Application Note 553

Description

The HA-5137 monolithic operational amplifier features an unparalleled combination of precision DC and wide-band high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/$\sqrt{Hz}$) precision instrumentation performance with high speed (20V/μs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (10μV), wide gain-bandwidth (63MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140mW of power.

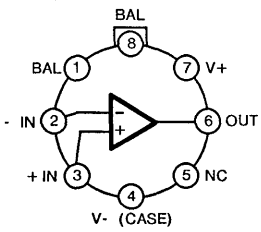
Using the HA-5137 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than five.

This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5137's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits.

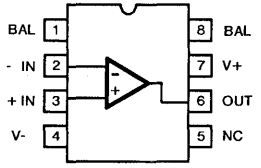
This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than five. The HA-5137 is available in TO-99 Metal Can and Ceramic 8 pin Mini- DIPs. For the military grade product, refer to the HA-5137/883 data sheet.

Pinouts

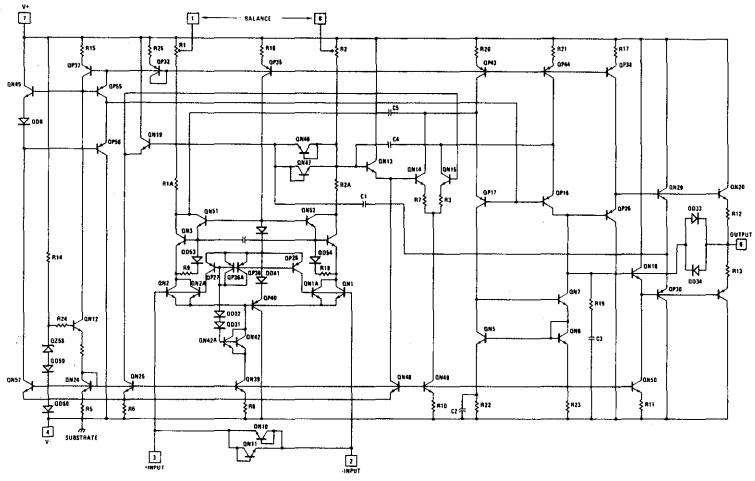
HA2-5137 (TO-99 METAL CAN)
TOP VIEW



HA7-5137 (CERAMIC MINI-DIP)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated
Voltage Between V+ and V- Terminals ..... ±22V
Differential Input Voltage (Note 2) ..... ±0.7V
Internal Power Dissipation 500mW
Output Current ..... Full Short Circuit Protection

Operating Temperature Ranges

HA-5137/37A-2 ..... $-55^oC \leq T_A \leq +125^oC$
HA-5137/37A-5 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature ..... +175°C

Electrical Specifications V+ = 15V, V- = -15V, $C_L \leq 50pF$, $R_S \leq 100\Omega$

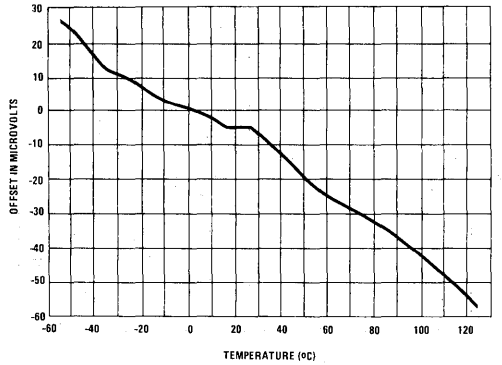
PARAMETER	TEMP	HA-5137A			HA-5137			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	10	25	-	30	100	µV
	Full	-	30	60	-	70	300	µV
Average Offset Voltage Drift	Full	-	0.2	0.6	-	0.4	1.8	µV/°C
Bias Current	+25°C	-	±10	±40	-	±15	±80	nA
	Full	-	±20	±60	-	±35	±150	nA
Offset Current	+25°C	-	7	35	-	12	75	nA
	Full	-	15	50	-	30	135	nA
Common Mode Range	Full	±10.3	±11.5	-	±10.3	±11.5	-	V
Differential Input Resistance (Note 3)	+25°C	1.5	6	-	0.8	4	-	MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 4)	+25°C	-	0.08	0.18	-	0.09	0.25	µVp-p
Input Noise Voltage Density (Note 5) f_O = 10Hz	+25°C	-	3.5	5.5	-	3.8	8.0	$nV/\sqrt{Hz}$
f_O = 30Hz		-	3.1	4.5	-	3.3	5.6	$nV/\sqrt{Hz}$
f_O = 1000Hz		-	3.0	3.8	-	3.2	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 5) f_O = 10Hz	+25°C	-	1.7	4.0	-	1.7	-	$pA/\sqrt{Hz}$
f_O = 30Hz		-	1.0	2.3	-	1.0	-	$nV/\sqrt{Hz}$
f_O = 1000Hz		-	0.4	0.6	-	0.4	0.6	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 6)	+25°C	1000	1800	-	700	1500	-	V/mV
	Full	600	1200	-	300	800	-	V/mV
Common Mode Rejection Ratio (Note 7)	Full	114	126	-	100	120	-	dB
Minimum Stable Gain	+25°C	5	-	-	5	-	-	V/V
Gain-Bandwidth-Product f_O = 10KHz	+25°C	60	80	-	60	80	-	MHz
f_O = 1MHz	+25°C	-	63	-	-	63	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing R_L = 600Ω	+25°C	±10.0	±11.5	-	±10.0	±11.5	-	V
R_L = 2KΩ	Full	±11.7	±13.8	-	±11.4	±13.5	-	V
Full Power Bandwidth (Note 8)	+25°C	220	320	-	220	320	-	KHz
Output Resistance, Open Loop	+25°C	-	70	-	-	70	-	Ω
Output Current	+25°C	16.5	25	-	16.5	25	-	mA
TRANSIENT RESPONSE (Note 9)								
Rise Time	+25°C	-	-	100	-	-	100	ns
Slew Rate (Note 11)	+25°C	14	20	-	14	20	-	V/µs
Settling Time (Note 10)	+25°C	-	1.0	-	-	1.0	-	µs
Overshoot	+25°C	-	20	40	-	20	40	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	3.5	-	-	3.5	-	mA
	Full	-	-	4.0	-	-	4.0	mA
Power Supply Rejection Ratio (Note 12)	Full	-	2	4	-	16	51	µV/V

NOTES:

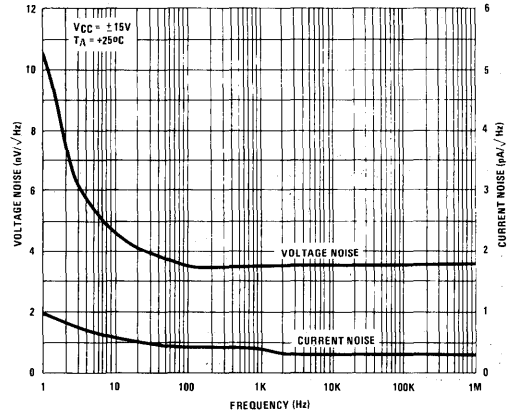
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. Sample tested.
6. $V_{OUT} = \pm 10V$, $R_L = 2k\Omega$
7. $V_{CM} = \pm 10V$
8. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{Peak}}$
9. Refer to Test Circuits section of the data sheet.
10. Settling time is specified to 0.1% of final value for a 10V output step and $A_V = -5$.
11. $V_{OUT} = 10V$ Step
12. $V_S = \pm 4V$ to $\pm 18V$

Typical Performance Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

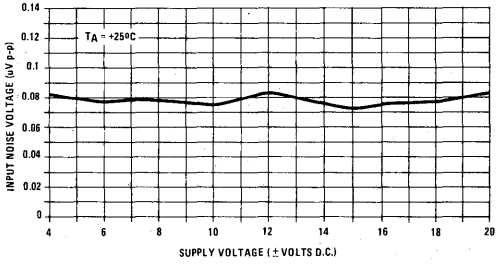
OFFSET VOLTAGE TYPICAL DRIFT vs. TEMPERATURE



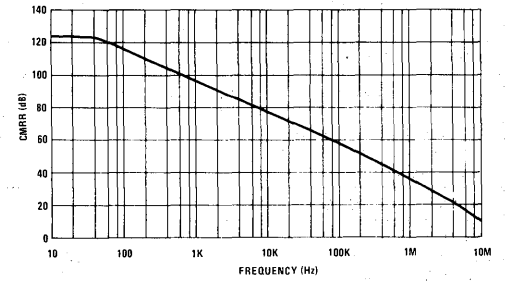
NOISE CHARACTERISTICS



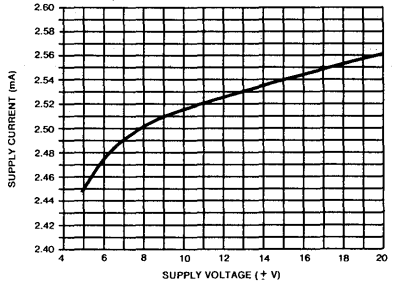
NOISE vs. SUPPLY VOLTAGE



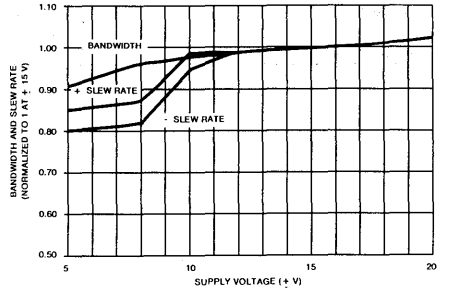
CMRR vs. FREQUENCY



SUPPLY CURRENT vs. SUPPLY VOLTAGE

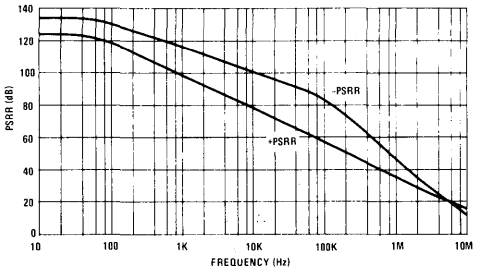


BANDWIDTH AND SLEW RATE vs. SUPPLY VOLTAGE

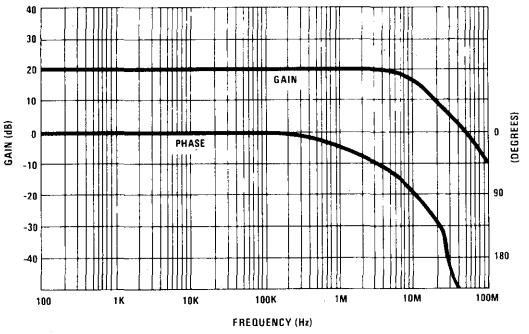


Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

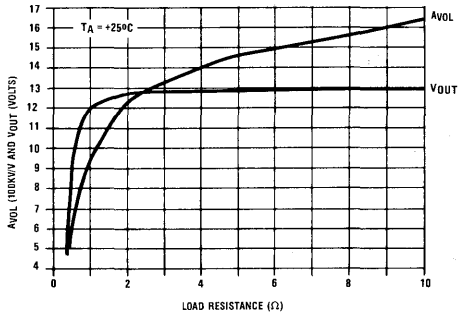
PSRR vs. FREQUENCY



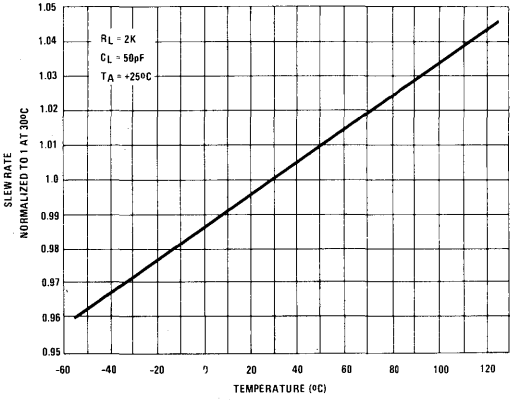
CLOSED LOOP GAIN AND PHASE vs. FREQUENCY



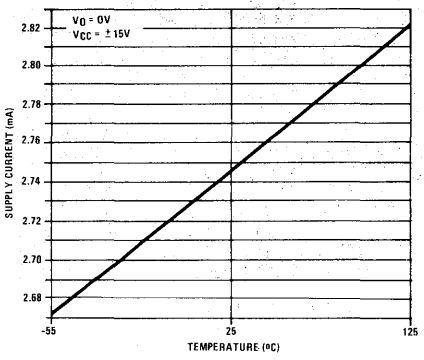
A_{VOL} AND V_{OUT} vs. LOAD RESISTANCE



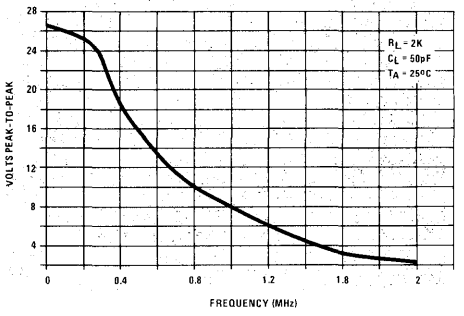
NORMALIZED SLEW RATE vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE

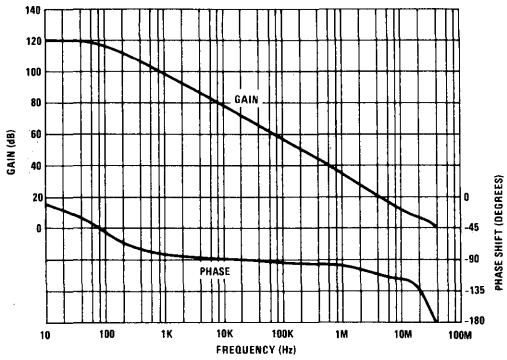


V_{OUT} MAX vs. FREQUENCY
UNDISTORTED SINEWAVE OUTPUT

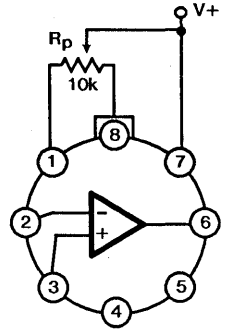


Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

OPEN LOOP GAIN AND PHASE vs. FREQUENCY

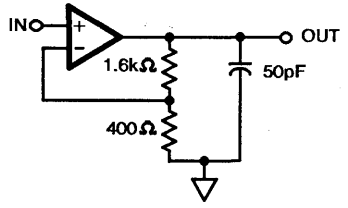


SUGGESTED OFFSET VOLTAGE ADJUSTMENT

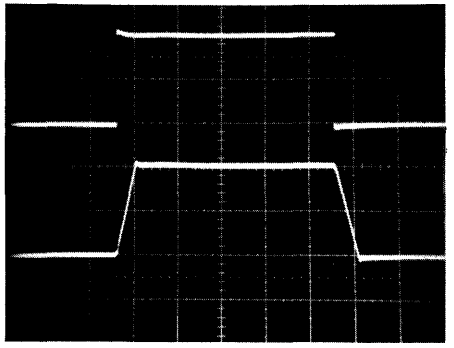


Test Offset Adjustment Range is $|V_{OS} \pm 1mV|$ minimum referred to output.
Typical range is ±4mV with $R_P = 10k\Omega$.

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

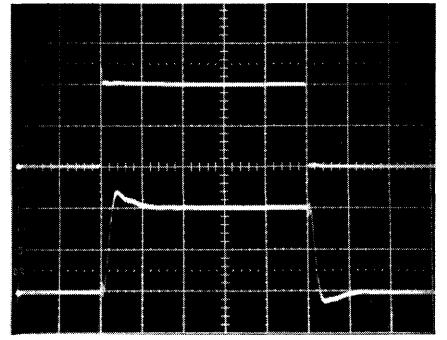


LARGE SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 1V/Div.)
(Volts: Output = 5V/Div.)
Horizontal Scale: (Time = 1µs/Div.)

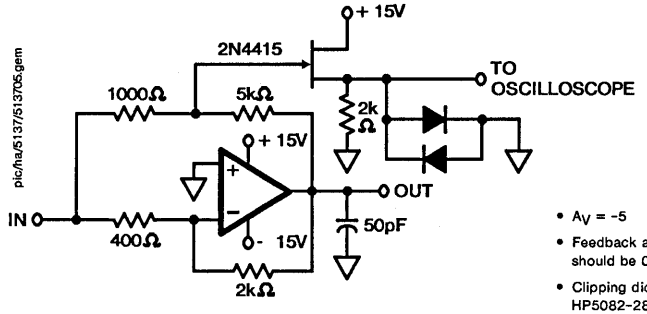
SMALL SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 20mV/Div.)
(Volts: Output = 100mV/Div.)
Horizontal Scale: (Time = 100ns/Div.)

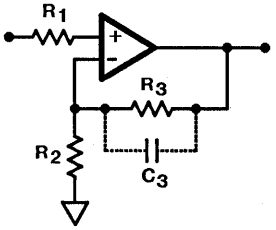
Typical Performance Curves (Continued) Unless Otherwise Specified: T_A = +25°C, V_{SUPPLY} = ±15V

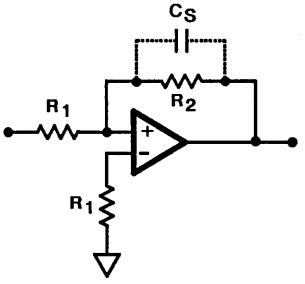
SETTLING TIME TEST CIRCUIT



- A_V = -5
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

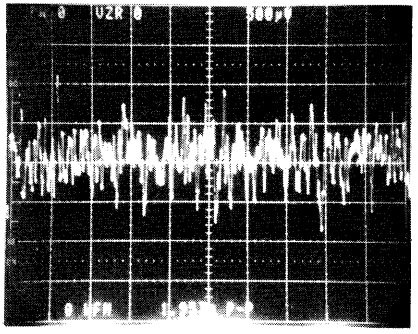
SUGGESTED STABILITY CIRCUITS





Low resistances are preferred for low noise applications as a 1KΩ resistor has 4nV/$\sqrt{Hz}$ of thermal noise. Total resistances of greater than 10KΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

0.1Hz TO 10Hz NOISE WITH A_{CL} = 25,000V/V



Horizontal Scale = 1sec/Div.
Vertical Scale = 0.002μV/Div.
0.08μVp-p

Die Characteristics

Transistor Count 63
Die Dimensions ..... 65 x 104.3 x 19 mils
(1700μm x 2600μm x 480μm)
Substrate Potential* ..... V-
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA7-5137 Ceramic Mini-DIP	160	79
HA2-5137 TO-99 Metal Can	172	48

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS HA-5141/42/44

Single/Dual/Quad Ultra-Low Power Operational Amplifiers

May 1990

Features

- Low Supply Current 45μA/Amp
- Wide Supply Voltage Range..... Single 3V to 30V or Dual ±1.5V to ±15V
- High Slew Rate 1.5V/μs
- High Gain 100kV/V
- Unity Gain Stable
- Available in Singles, Duals and Quads

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Instrumentation
- For Further Design Ideas See Application Note 544

Description

The HA-5141/42/44 ultra-low power operational amplifiers provide AC and DC performance characteristics similar to or better than most general purpose amplifiers while only drawing 1/30 of the supply current of most general purpose amplifiers. In applications which require low power dissipation and good A.C. electrical charactersistics, this family offers the industry's best speed/power ratio.

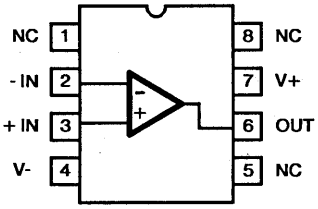
The HA-5141/42/44 provides accurate signal processing by virtue of their low input offset voltage (0.5mV), low input bias current (45nA), high open loop gain (100kV/V) and low noise, for low power operational amplifiers ($20nV/\sqrt{Hz}$). These characteristics coupled with a 1.5/μs slew rate and a 400kHz bandwidth make the HA-5141/42/44 ideal for use in low power instrumentation, audio amplifier and active filter designs. The wide range of supply voltages (3V to 30V) also allow these amplifiers to be very useful in low voltage battery powered equipment. These parts are also tested and guaranteed at both ±15V and single ended +5V supplies.

These amplifiers are available in singles (HA-5141, SOIC, Can or Mini-DIP), duals (HA-5142, SOIC, Can or Mini-DIP) or quads (HA-5144, SOIC or DIP) with industry standards pinouts which allow the HA-5141/5142/5144's to be interchangeable with most other operational amplifiers. For military grade product refer to the 5141, 5142, 5144/883 data sheet.

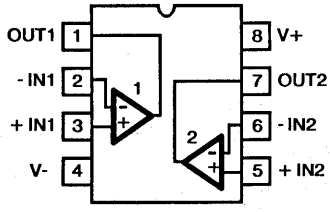
Pinouts

TOP VIEWS

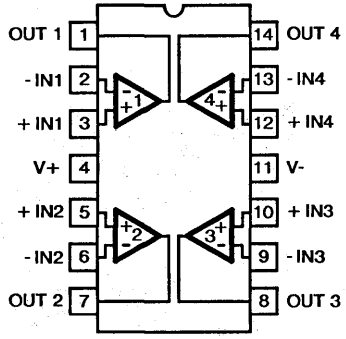
HA1-5141 (CERAMIC MINI-DIP)
HA3-5141 (PLASTIC MINI-DIP)



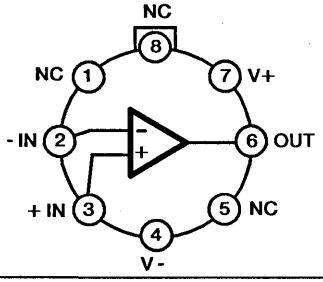
HA3-5142 (PLASTIC MINI-DIP)
HA7-5142 (CERAMIC DIP)



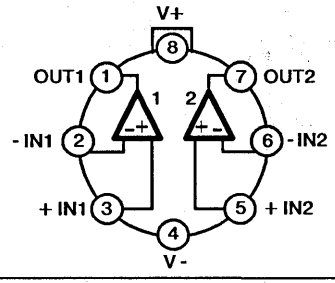
HA1-5144 (CERAMIC DIP)
HA3-5144 (PLASTIC DIP)



HA2-5141 (TO-99 METAL CAN)



HA2-5142 (TO-99 METAL CAN)



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage ..... ±7V
Output Current ..... S/C Protected
Internal Power Dissipation 500mW

Operating Temperature Range

HA-5141/42/44-5 ..... $0^oC \leq T_A \leq +75^oC$
HA-5141/42/44-2 ..... $-55^oC \leq T_A \leq +125^oC$
HA-5141/42/44-9 ..... $-40^oC \leq T_A \leq +85^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature ..... $+175^oC$

Electrical Specifications $R_S = 100\Omega$, $C_L \leq 10pF$ Unless Otherwise Specified.

PARAMETER	TEMP	-2, -5 V+ = +5V, V- = 0V			-2, -5 V+ = +15V, V- = -15V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage (Note 11)	+25°C	-	2	6	-	2	6	mV
	Full	-	-	8	-	-	8	mV
Average Offset Voltage Drift	Full	-	3	-	-	3	-	µV/°C
Bias Current (Note 11)	+25°C	-	45	100	-	45	100	nA
	Full	-	-	125	-	-	125	nA
Offset Current (Note 11)	+25°C	-	0.3	10	-	0.3	10	nA
	Full	-	-	20	-	-	20	nA
Common Mode Range	Full	0 to 3	-	-	±10	-	-	V
Differential Input Resistance	+25°C	-	0.6	-	-	0.6	-	MΩ
Input Noise Voltage (f = 1kHz)	+25°C	-	20	-	-	20	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C	-	0.25	-	-	0.25	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 2, 4)	+25°C	20k	100k	-	20k	100k	-	V/V
	Full	15k	-	-	15k	-	-	V/V
Common Mode Rejection Ratio (Note 7)	Full	77	105	-	77	105	-	dB
Bandwidth (Notes 2, 3)	+25°C	-	0.4	-	-	0.4	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Notes 2, 10)	+25°C	1.0 to 3.8	0.7 to 4.2	-	±10	±13	-	V
	Full	1.2 to 3.5	0.9 to 4.0	-	±10	±13	-	V
Full Power Bandwidth (Notes 2, 4, 8)	+25°C	-	240	-	-	24	-	kHz
TRANSIENT RESPONSE (Notes 2, 3)								
Rise Time	+25°C	-	600	-	-	600	-	ns
Slew Rate (Note 6)	+25°C	0.8	1.5	-	0.8	1.5	-	V/µs
Settling Time (Note 5)	+25°C	-	10	-	-	10	-	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	45	80	-	100	150	µA/Amp
	Full	-	-	100	-	-	200	µA/Amp
Power Supply Rejection Ratio (Note 9)	Full	77	105	-	77	105	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $R_L = 50k\Omega$
3. $C_L = 50pF$
4. $V_O = 1.4$ to 2.5V for $V_{CC} = +5, 0V$; $V_O = \pm 10V$ for $V_{CC} = \pm 15V$.
5. Settling Time is specified to 0.1% of final value for a 3V output step and $A_V = -1$ for $V_{CC} = +5V, 0V$. Output step = 10V for $V_{CC} = \pm 15V$.
6. Maximum input slew rate = 10V/µs.
7. $V_{CM} = 0$ to 3V for $V_{CC} = +5, 0V$; $V_{CM} = \pm 10V$ for $V_{CC} = \pm 15V$
8. Full Power Bandwidth is guaranteed by equation:
   Full Power Bandwidth = $\frac{\text{Slew Rate}}{2\pi V \text{ Peak}}$
9. $\Delta V_S = +10V$ for $V_{CC} = +5, 0V$; $\Delta V_S = \pm 5V$ for $V_{CC} = \pm 15V$.
10. For $V_{CC} = +5, 0V$ terminate R_L at +2.5V. Typical output current is ±3mA.
11. $V_O = 1.4V$ for $V_{CC} = +5V, 0V$.

Electrical Specifications R_S = 100Ω, C_L < 10pF Unless Otherwise Specified.

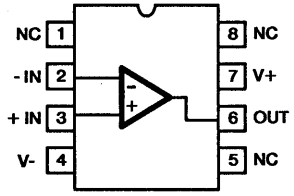
PARAMETER	TEMP	-9 V+ = +5V, V- = 0V			-9 V+ = +15V, V- = -15V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage (Note 11)	+25°C	-	2	6	-	2	6	mV
	Full	-	-	8	-	-	8	mV
Average Offset Voltage Drift	Full	-	3	-	-	3	-	µV/°C
Bias Current (Note 11)	+25°C	-	45	100	-	45	100	nA
	Full	-	-	125	-	-	125	nA
Offset Current (Note 11)	+25°C	-	0.3	10	-	0.3	10	nA
	Full	-	-	20	-	-	20	nA
Common Mode Range	Full	0 to 3	-	-	±10	-	-	V
Differential Input Resistance	+25°C	-	0.6	-	-	0.6	-	MΩ
Input Noise Voltage (f = 1kHz)	+25°C	-	20	-	-	20	-	nV/√Hz
Input Noise Current (f = 1kHz)	+25°C	-	0.25	-	-	0.25	-	pA/√Hz
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 2, 4)	+25°C	20k	100k	-	20k	100k	-	V/V
	Full	12k	-	-	12k	-	-	V/V
Common Mode Rejection Ratio (Note 7)	Full	70	105	-	70	105	-	dB
Bandwidth (Notes 2, 3)	+25°C	-	0.4	-	-	0.4	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Notes 2, 10)	+25°C	1.0 to 3.8	0.7 to 4.2	-	±10	±13	-	V
	Full	1.2 to 3.5	0.9 to 4.0	-	±10	±13	-	V
Output Current	+25°C	-	-	-	-	-	-	V
Full Power Bandwidth (Notes 2, 4, 8)	+25°C	-	240	-	-	24	-	kHz
TRANSIENT RESPONSE (Notes 2, 3)								
Rise Time	+25°C	-	600	-	-	600	-	ns
Slew Rate (Note 6)	+25°C	0.8	1.5	-	0.8	1.5	-	V/µs
Settling Time (Note 5)	+25°C	-	10	-	-	10	-	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	45	80	-	100	150	µA/Amp
	Full	-	-	100	-	-	200	µA/Amp
Power Supply Rejection Ratio (Note 9)	Full	70	105	-	70	105	-	dB

NOTE: The notes from the -2, -5 table apply to this -9 table. Absolute maximum ratings and the operating temperature ranges also apply.

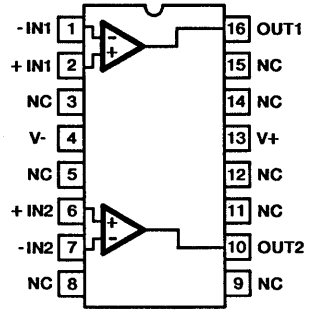
SOIC Pinouts

TOP VIEWS

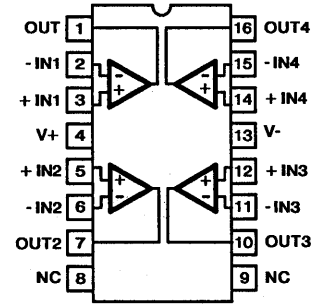
HA9P5141 (SOIC)



HA9P5142 (SOIC)

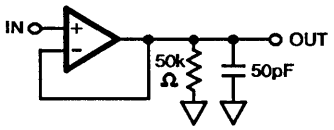


HA9P5144 (SOIC)

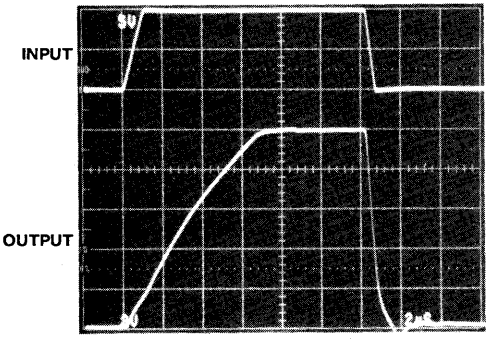


Test Circuits

SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT

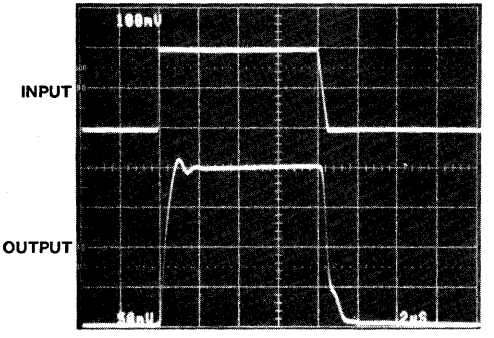


LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 5V/Div.; Output = 2V/Div.)
Horizontal Scale: (Time: 2µs/Div.)



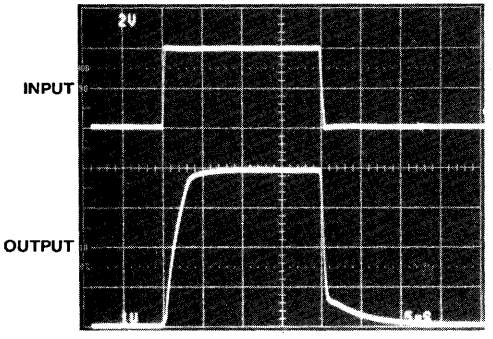
$+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V

SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 2µs/Div.)



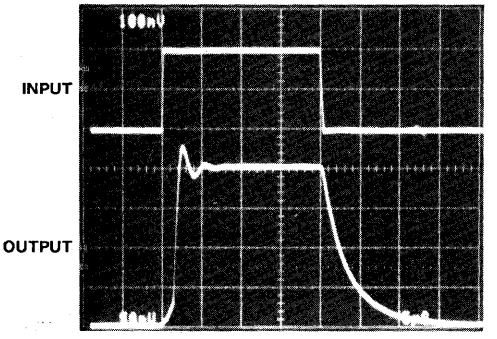
$+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V

LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 2V/Div.; Output = 1V/Div.)
Horizontal Scale: (Time: 5µs/Div.)



$+V_{SUPPLY}$ = +5V, $-V_{SUPPLY}$ = 0V

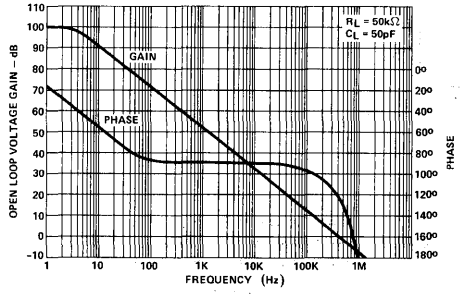
SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.; Output = 50mV/Div.)
Horizontal Scale: (Time: 5µs/Div.)



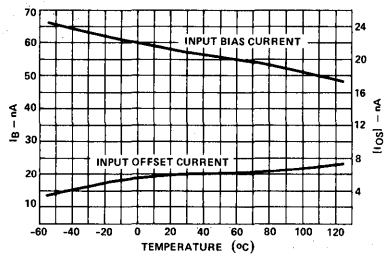
$+V_{SUPPLY}$ = +5V, $-V_{SUPPLY}$ = 0V

Performance Curves $V_S = \pm 2.5V$, $T_A = +25^oC$ Unless Otherwise Specified

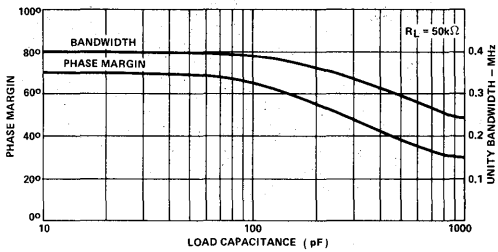
OPEN LOOP FREQUENCY RESPONSE



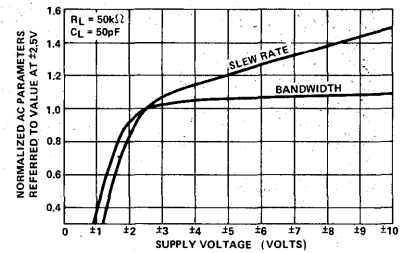
INPUT OFFSET CURRENT AND BIAS CURRENT vs. TEMPERATURE



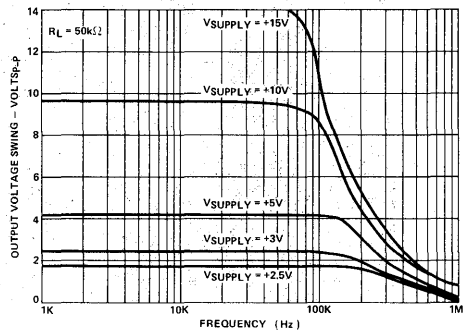
BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



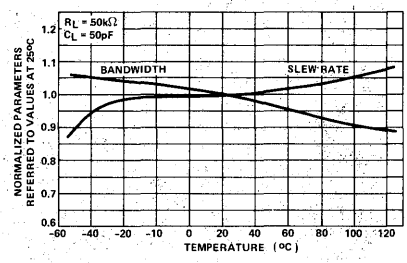
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING vs. FREQUENCY AND SINGLE SUPPLY VOLTAGE

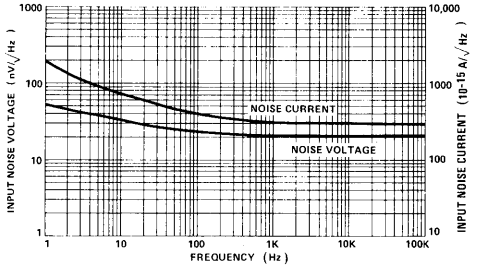


NORMALIZED AC PARAMETERS vs. TEMPERATURE

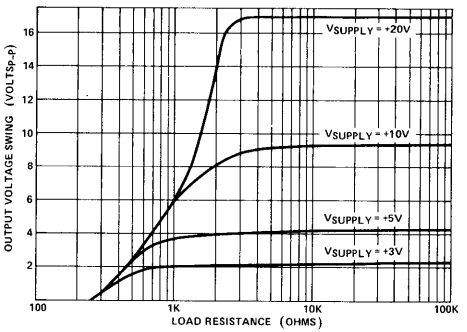


Performance Curves (Continued) $V_S = \pm 2.5V$, $T_A = +25^oC$ Unless Otherwise Specified

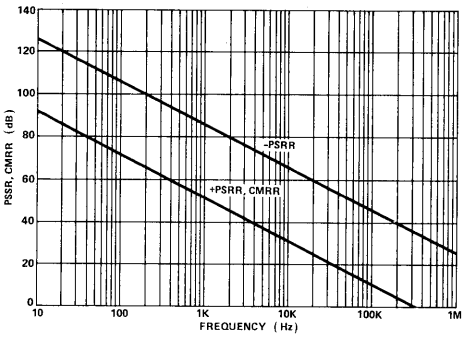
INPUT NOISE vs. FREQUENCY



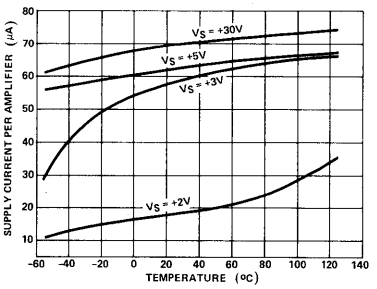
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE AND SINGLE SUPPLY VOLTAGE



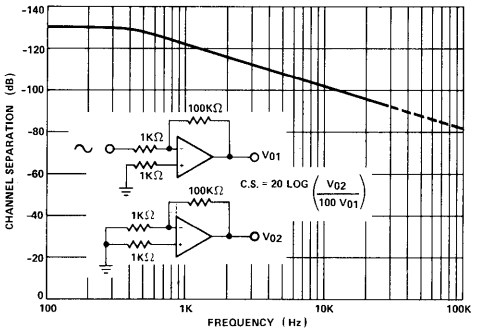
PSRR AND CMRR vs. FREQUENCY



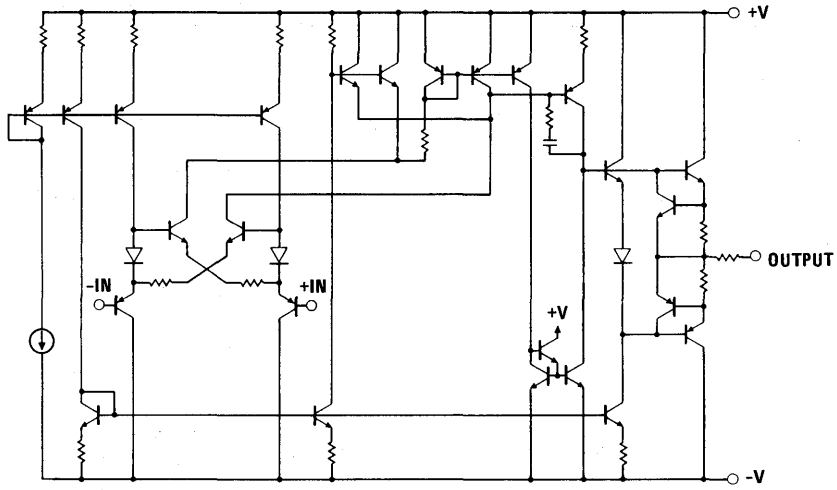
POWER SUPPLY CURRENT vs. TEMPERATURE AND SINGLE SUPPLY VOLTAGE



CHANNEL SEPARATION vs. FREQUENCY



Schematic



Die Characteristics

Transistor Count

HA-5141	33
HA-5142	66
HA-5144	132
Substrate Potential*	V-
Process	Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA1-5144 (-2, -5, -7)	101	33
HA1-5144 (/883)	75	22
HA2-5144 (-2, -5, -7)	206	56
HA2-5141 (/883)	168	50
HA2-5142 (-2, -5, -7)	184	50
HA2-5142 (/883)	143	43
HA3-5141 (-5)	90	40
HA3-5142 (-5)	80	20
HA3-5144 (-5)	75	20
HA7-5141 (-2, -5, -7)	210	117
HA7-5141 (/833)	90	40
HA7-5142 (-2, -5, -7)	177	92
HA7-5142 (/883)	80	20
HA9P5141 (-5, -9)	161	42
HA9P5142 (-5, -9)	94	26
HA9P5144 (-5, -9)	90	26

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

NOTE: Consult Harris for LCC/PLCC information.

HARRIS

HA-5147

Ultra-Low Noise Precision High Slew Rate Wideband Operational Amplifier

May 1990

Features

- High Speed 35V/μs
- Wide Gain Bandwidth (A_V > 10) 120MHz
- Low Noise ..... 3nV/√Hz at 1 KHz
- Low VOS 10μV
- High CMRR 126dB
- High Gain 1800V/mV

Applications

- High Speed Signal Conditioners
- Wide Bandwidth Instrumentation Amplifiers
- Low Level Transducer Amplifiers
- Fast, Low Level Voltage Comparators
- Highest Quality Audio Preamplifiers
- Pulse/RF Amplifiers

Description

The HA-5147 monolithic operational amplifier features an unparalleled combination of precision DC and wideband high speed characteristics. Utilizing the Harris D. I. technology and advanced processing techniques, this unique design unites low noise (3nV/√Hz) precision instrumentation performance with high speed (35V/μs) wideband capability.

This amplifier's impressive list of features include low V_{OS} (10μV), wide gain-bandwidth (120MHz), high open loop gain (1800V/mV), and high CMRR (126dB). Additionally, this flexible device operates over a wide supply range (±5V to ±20V) while consuming only 140mW of power.

Using the HA-5147 allows designers to minimize errors while maximizing speed and bandwidth in applications requiring gains greater than ten.

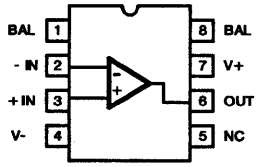
This device is ideally suited for low level transducer signal amplifier circuits. Other applications which can utilize the HA-5147's qualities include instrumentation amplifiers, pulse or RF amplifiers, audio preamplifiers, and signal conditioning circuits. Further application ideas are given in Application Note 553.

This device can easily be used as a design enhancement by directly replacing the 725, OP25, OP06, OP07, OP27 and OP37 where gains are greater than ten. The HA-5147 is available in TO-99 Metal Can and Ceramic 8 pin Mini-DIPs. For military grade product, refer to the HA-5147/883 data sheet.

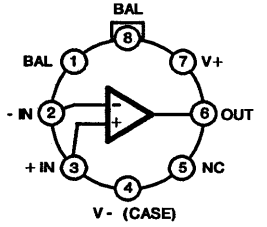
Pinouts

TOP VIEWS

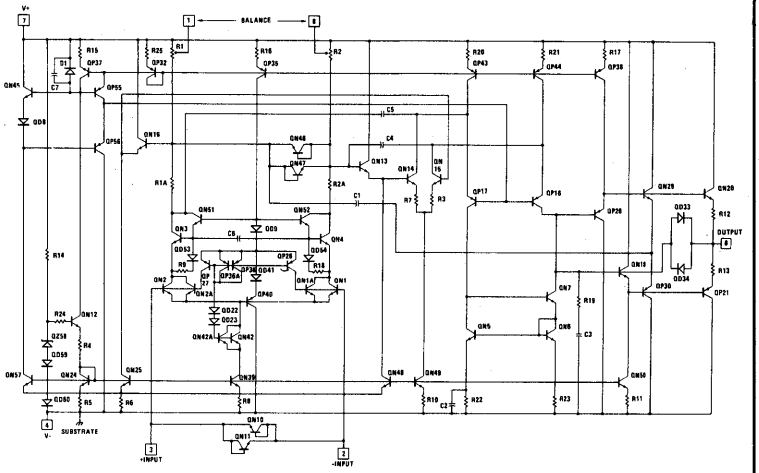
HA7-5147 (CERAMIC MINI-DIP)



HA2-5147 (TO-99 METAL CAN)



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals ..... ±22V
Differential Input Voltage (Note 2) ..... ±0.7V
Internal Power Dissipation 500mW
Output Current ..... Full Short Circuit Protection

Operating Temperature Ranges

HA-5147/47A-2 ..... $-55^oC \leq T_A \leq +125^oC$
HA-5147/47A-5 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature ..... +175°C

Electrical Specifications V+ = 15V, V- = -15V, $C_L \leq 50pF$, $R_S \leq 100\Omega$

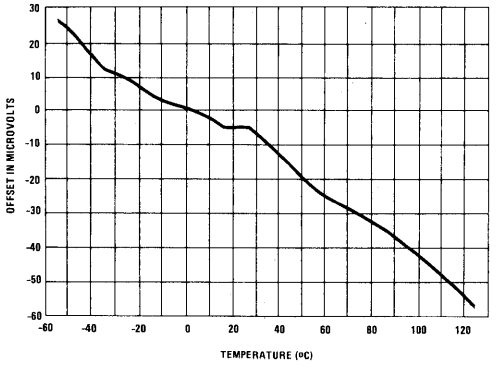
PARAMETER	TEMP	HA-5147A MIN	HA-5147A TYP	HA-5147A MAX	HA-5147 MIN	HA-5147 TYP	HA-5147 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	10	25	-	30	100	µV
	Full	-	30	60	-	70	300	µV
Average Offset Voltage Drift	Full	-	0.2	0.6	-	0.4	1.8	µV/°C
Bias Current	+25°C	-	±10	±40	-	±15	±80	nA
	Full	-	±20	±60	-	±35	±150	nA
Offset Current	+25°C	-	7	35	-	12	75	nA
	Full	-	15	50	-	30	135	nA
Common Mode Range	Full	±10.3	±11.5	-	±10.3	±11.5	-	V
Differential Input Resistance (Note 3)	+25°C	1.5	6	-	0.8	4	-	MΩ
Input Noise Voltage 0.1Hz to 10Hz (Note 4)	+25°C	-	0.08	0.18	-	0.09	0.25	µVp-p
Input Noise Voltage Density (Note 5) f_0 = 10Hz	+25°C	-	3.5	5.5	-	3.8	8.0	$nV/\sqrt{Hz}$
f_0 = 30Hz		-	3.1	4.5	-	3.3	5.6	$nV/\sqrt{Hz}$
f_0 = 1000Hz		-	3.0	3.8	-	3.2	4.5	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 5) f_0 = 10Hz	+25°C	-	1.7	4.0	-	1.7	-	$pA/\sqrt{Hz}$
f_0 = 30Hz		-	1.0	2.3	-	1.0	-	$pA/\sqrt{Hz}$
f_0 = 1000Hz		-	0.4	0.6	-	0.4	0.6	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Minimum Stable Gain	+25°C	10	-	-	10	-	-	V/V
Large Signal Voltage Gain (Note 6)	+25°C	1000	1800	-	700	1500	-	V/mV
	Full	600	1200	-	300	800	-	V/mV
Common Mode Rejection Ratio (Note 7)	Full	114	126	-	100	120	-	dB
Gain-Bandwidth-Product f_0 = 10KHz	+25°C	120	140	-	120	140	-	MHz
f_0 = 1MHz	+25°C	-	120	-	-	120	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing R_L = 600Ω	+25°C	±10.0	±11.5	-	±10.0	±11.5	-	V
R_L = 2KΩ	Full	±11.7	±13.8	-	±11.4	±13.5	-	V
Full Power Bandwidth (Note 8)	+25°C	445	500	-	445	500	-	KHz
Output Resistance, Open Loop	+25°C	-	70	-	-	70	-	Ω
Output Current	+25°C	16.5	25	-	16.5	25	-	mA
TRANSIENT RESPONSE (Note 9)								
Rise Time	+25°C	-	22	50	-	22	50	ns
Slew Rate (Note 11)	+25°C	28	35	-	28	35	-	V/µs
Settling Time (Note 10)	+25°C	-	400	-	-	400	-	ns
Overshoot	+25°C	-	20	40	-	20	40	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	3.5	-	-	3.5	-	mA
	Full	-	-	4.0	-	-	4.0	mA
Power Supply Rejection Ratio (Note 12)	Full	-	2	4	-	16	51	µV/V

NOTES:

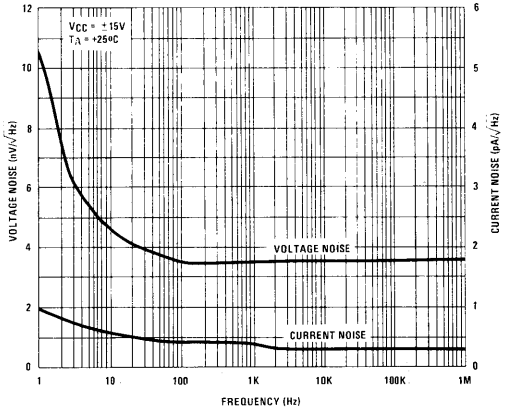
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For differential input voltages greater than 0.7V, the input current must be limited to 25mA to protect the back-to-back input diodes.
3. This parameter value is based upon design calculations.
4. Refer to Typical Performance section of the data sheet.
5. Sample tested.
6. $V_{OUT} = \pm 10V$, $R_L = 2K\Omega$
7. $V_{CM} = \pm 10V$
8. Full power bandwidth guaranteed based on slew rate measurement using: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
9. Refer to Test Circuits section of the data sheet.
10. Settling time is specified to 0.1% of final value for a 10V output step and $A_V = -10$.
11. $V_{OUT} = 10V$ Step
12. $V_S = \pm 4V$ to $\pm 18V$

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

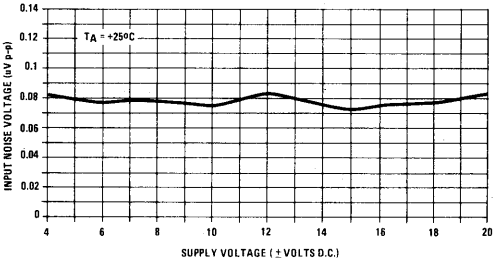
OFFSET VOLTAGE TYPICAL DRIFT vs. TEMPERATURE



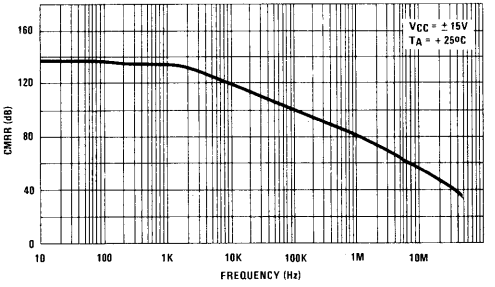
NOISE CHARACTERISTICS



NOISE vs. SUPPLY VOLTAGE

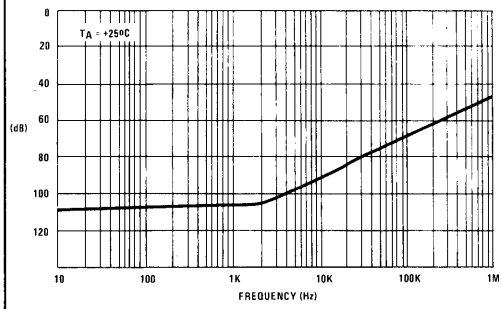


CMRR vs. FREQUENCY

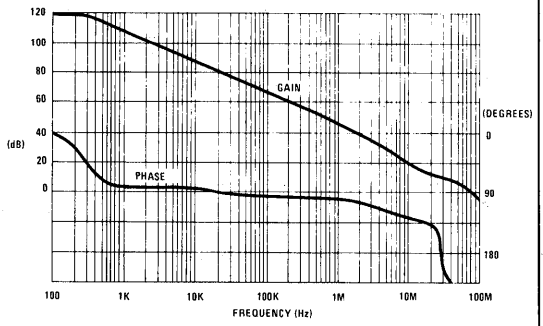


Typical Performance Curves (Continued) Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

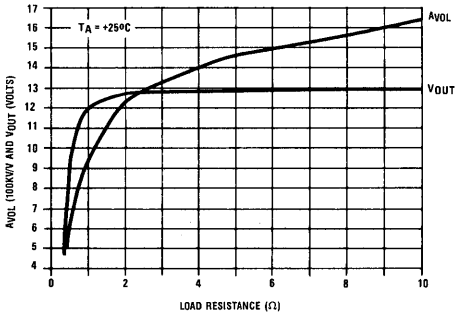
PSRR vs. FREQUENCY



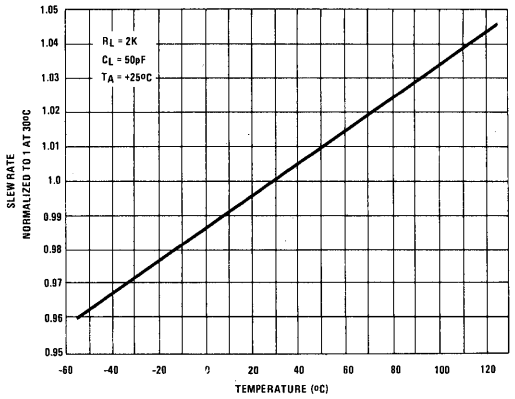
OPEN LOOP GAIN AND PHASE vs. FREQUENCY



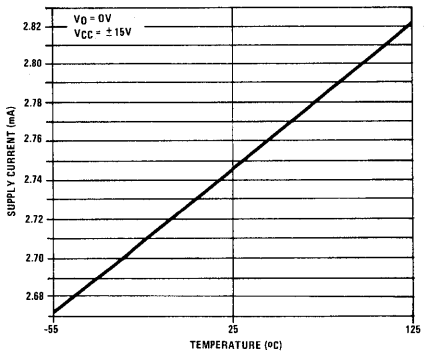
A_{VOL} AND V_{OUT} vs. LOAD RESISTANCE



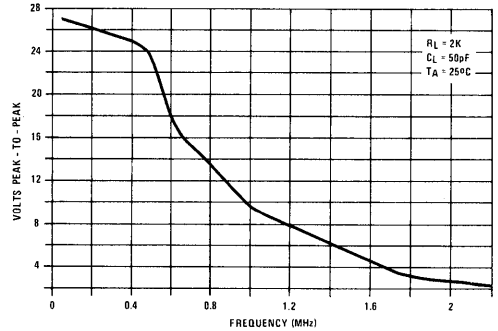
NORMALIZED SLEW RATE vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE

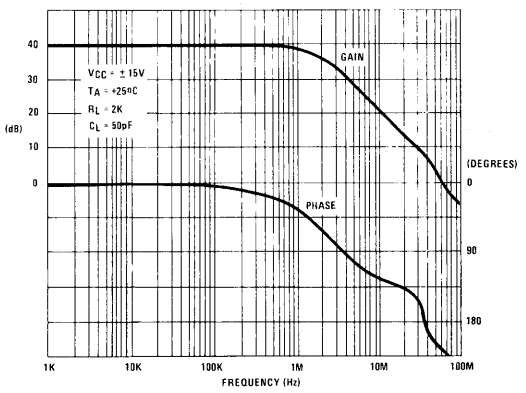


V_{OUT} MAX vs. FREQUENCY UNDISTORTED SINEWAVE OUTPUT

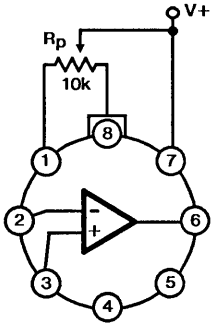


Typical Performance Curves (Continued) Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

CLOSED LOOP GAIN AND PHASE vs. FREQUENCY

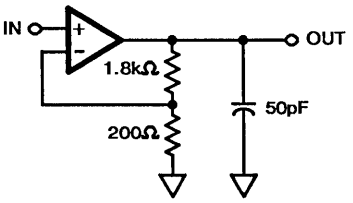


SUGGESTED OFFSET VOLTAGE ADJUSTMENT

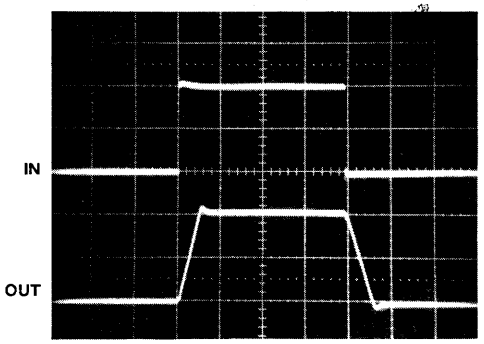


Tested Offset Adjustment Range is $|V_{OS} \pm 1mV|$ minimum referred to output.
Typical range is ±4mV with $R_T = 10k\Omega$.

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT

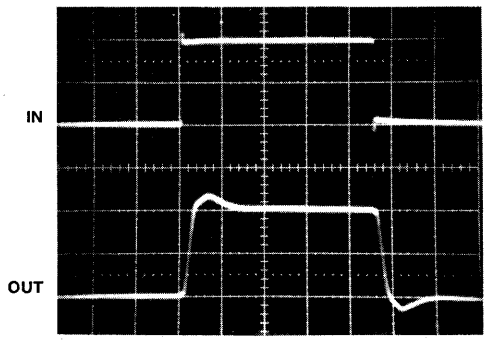


LARGE SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 0.5V/Div.)
(Volts: Output = 5V/Div.)
Horizontal Scale: (Time: 500ns/Div)

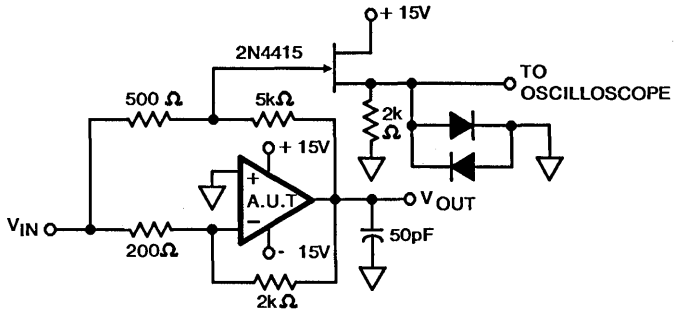
SMALL SIGNAL RESPONSE



Vertical Scale: (Volts: Input = 10mV/Div)
(Volts: Output = 100mV/Div)
Horizontal Scale: (Time: 100ns/Div)

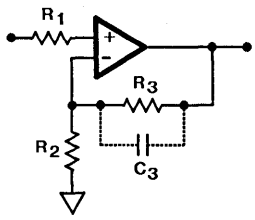
Typical Performance Curves (Continued) Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

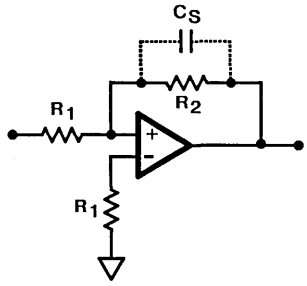
SETTLING TIME TEST CIRCUIT



- $A_V = -10$
- Feedback and summing resistors should be 0.1%
- Clipping diodes are optional. HP5082-2810 recommended

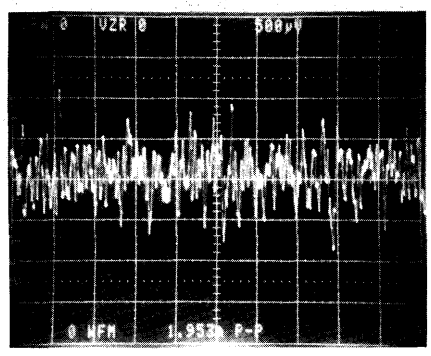
SUGGESTED STABILITY CIRCUITS





Low resistances are preferred for low noise applications as a 1kΩ resistor has $4nV/\sqrt{Hz}$ of thermal noise. Total resistances of greater than 10kΩ on either input can reduce stability. In most high resistance applications, a few picofarads of capacitance across the feedback resistor will improve stability.

0.1Hz TO 10Hz NOISE WITH A_{CL} = 25,000V/V



Horizontal Scale = 1sec/Div.
Vertical Scale = 0.002μV/Div.
0.08μVp-p

Die Characteristics

Transistor Count		63
Die Dimensions		65 x 104.3 x 19 mils
Substrate Potential*		V-
Process		Bipolar-DI
Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA7-5147 Ceramic Mini-DIP	160	79
HA2-5147 TO-99 Metal Can	172	48

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS HA-5151/52/54

Single/Dual/Quad Low Power Operational Amplifiers

July 1990

Features

- Low Supply Current ..... <200μA/Amplifier
- Dual Supply Voltage Range ..... ±1.5V to ±15V
- Single Supply Voltage Range..... 3V to 30V
- High Slew Rate 6V/μs
- Low V_{OS} Drift ..... 3μV/°C
- Low Noise ..... 15nV/$\sqrt{Hz}$
- Dielectric Isolation

Applications

- Portable Instruments
- Meter Amplifiers
- Telephone Headsets
- Microphone Amplifiers
- Remote SensorsTransmitter
- Battery Powered Equipment
- For Further Design Ideas See Application Note 544

Description

The HA-5151/52/54 series is a group of dielectrically isolated bipolar amplifiers designed to provide excellent AC performance while drawing less than 200μA of supply current per amplifier. These unity gain stable amplifiers are especially well suited for portable and lightweight equipment where available power is limited.

The HA-5151/52/54 series combines superior low power AC performance with DC precision not usually found in general purpose amplifiers. The DC performance is centered around low input offset voltage (0.5mV), low offset voltage drift (3μV/°C), and low input bias current (70nA). This is combined with a very low input noise voltage of 15nV/$\sqrt{Hz}$ at 1kHz.

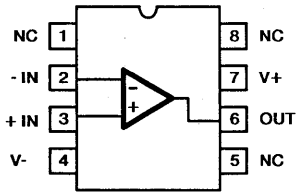
The AC performance of the HA-5151/52/54 series surpasses that of typical low power amplifiers with 6V/μs slew rate and a full power bandwidth of 95kHz. This makes the HA-5151/52/54 series an excellent choice for virtually all audio processing applications as well as remote sensor/transmitter designs requiring both low power and high speed. The suitability of the HA-5151/52/54 series for remote and low power operation is further enhanced by the wide range of supply voltages (±1.5V to ±15V) as well as single supply operation (3V to 30V). These parts are also tested and guaranteed at both ±15 and single ended +5V supplies.

These amplifiers are available in singles (HA-5151, Can or Mini-DIP), duals (HA-5152, Can or Mini-DIP) or quads (HA-5154, 14 pin DIP), as well as over both the commercial (0°C to +75°C) and military (-55°C to +125°C) temperature ranges. These amplifiers also carry industry standard pinouts which allow the HA-5151/52/54's to be interchangeable with most other operational amplifiers. For military grade product refer to the HA-5151, 5152, 5154/883 data sheets.

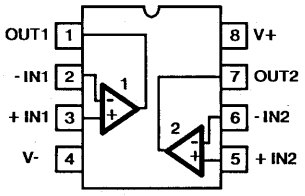
Pinouts

TOP VIEWS

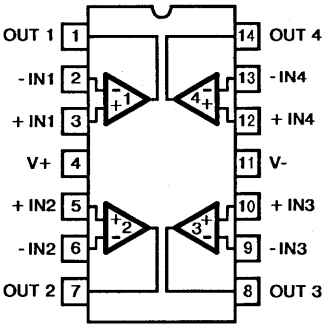
HA3-5151 (PLASTIC MINI-DIP)
HA7-5151 (CERAMIC DIP)



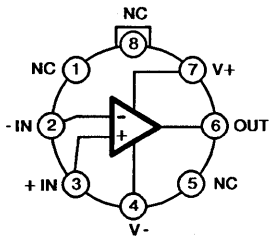
HA3-5152 (PLASTIC MINI-DIP)
HA7-5152 (CERAMIC DIP)



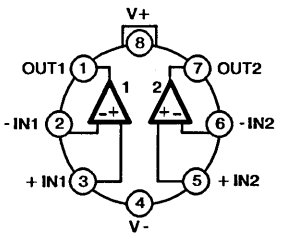
HA1-5154 (CERAMIC DIP)
HA3-5154 (PLASTIC DIP)



HA2-5151 (TO-99 METAL CAN)



HA2-5152 (TO-99 METAL CAN)



CAUTION:These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage ..... ±7V
Output Current ..... S/C Protected
Internal Power Dissipation 500mW

Operating Temperature Range

HA-5151/52/54-5 ..... $0^oC \leq T_A \leq +75^oC$
HA-5151/52/54-2 ..... $-55^oC \leq T_A \leq +125^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature ..... $+175^oC$

Electrical Specifications $R_S = 100\Omega$, $C_L \leq 10pF$ Unless Otherwise Specified.

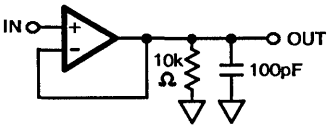
PARAMETER	TEMP	V+ = +5V, V- = 0V			V+ = +15V, V- = -15V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	0.5	3	-	0.5	3	mV
	Full	-	-	4	-	-	4	mV
Average Offset Voltage Drift	Full	-	3	-	-	3	-	µV/°C
Bias Current	+25°C	-	100	250	-	100	250	nA
	Full	-	-	400	-	-	400	nA
Offset Current	+25°C	-	5	50	-	5	50	nA
	Full	-	-	80	-	-	80	nA
Common Mode Range	Full	0 to 3	-	-	±10	-	-	V
Differential Input Resistance	+25°C	-	1.5	-	-	1.5	-	MΩ
Input Noise Voltage (f = 1kHz)	+25°C	-	14.8	-	-	14.8	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C	-	0.25	-	-	0.25	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 2, 4)	+25°C	50k	100k	-	50k	100k	-	V/V
	Full	25k	50k	-	25k	50k	-	V/V
Common Mode Rejection Ratio (Note 7)	Full	80	105	-	80	105	-	dB
Bandwidth (Notes 2, 3)	+25°C	-	1.3	-	-	1.3	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Notes 2, 10)	+25°C	1 to 3.2	0.7 to 3.5	-	±10	±13	-	V
	Full	1.2 to 2.9	0.9 to 3.2	-	±10	±13	-	V
Full Power Bandwidth (Notes 2, 4, 8)	+25°C	-	700	-	-	95	-	kHz
TRANSIENT RESPONSE (Notes 2, 3)								
Rise Time	+25°C	-	300	-	-	300	-	ns
Slew Rate (Note 6)	+25°C	2	4.5	-	4	6	-	V/µs
Settling Time (Note 5)	+25°C	-	5	-	-	5	-	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C	-	200	250	-	200	250	µA/Amp
	Full	-	-	275	-	-	275	µA/Amp
Power Supply Rejection Ratio (Note 9)	Full	80	105	-	80	105	-	dB

NOTES:

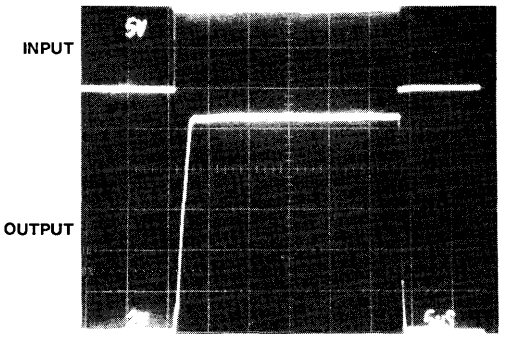
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $R_L = 10k\Omega$
3. $C_L = 100pF$
4. $V_O = 1.4$ to 2.5V for $V_{CC} = +5, 0V$; $V_O = \pm 10V$ for $V_{CC} = \pm 15V$.
5. Settling Time is specified to 0.1% of final value for a 3V output step and $A_V = -1$. For $V_{CC} = +5V, 0V$; output step = 10V for $V_{CC} = \pm 15V$.
6. Maximum input slew rate = 25V/µs.
7. $V_{CM} = 0$ to 3V for $V_{CC} = +5, 0V$; $V_{CM} = \pm 10V$ for $V_{CC} = \pm 15V$
8. Full Power Bandwidth is guaranteed by equation:
$$\text{Full Power Bandwidth} = \frac{\text{Slew Rate}}{2\pi V_{Peak}}$$
9. $\Delta VS = +10V$ for $V_{CC} = +5, 0V$; $\Delta VS = \pm 5V$ for $V_{CC} = \pm 15V$.
10. For $V_{CC} = +5, 0V$ terminate R_L at +2.5V.

Test Circuits

SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT

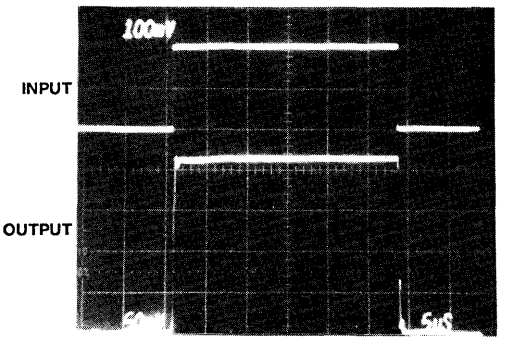


LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 5V/Div.)
(Volts: Output = 2/VDiv.)
Horizontal Scale: (Time: 5µs/Div.)



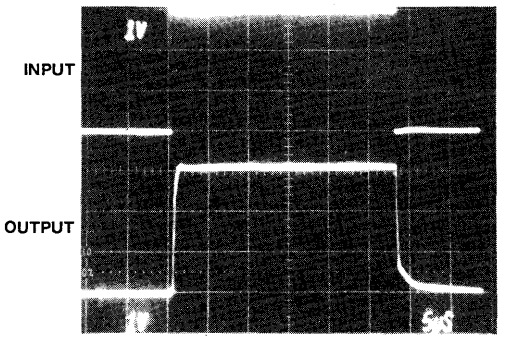
$+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V

SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: Input = 100mV/Div.)
(Volts: Output = 50mV/Div.)
Horizontal Scale: (Time: 5µs/Div.)



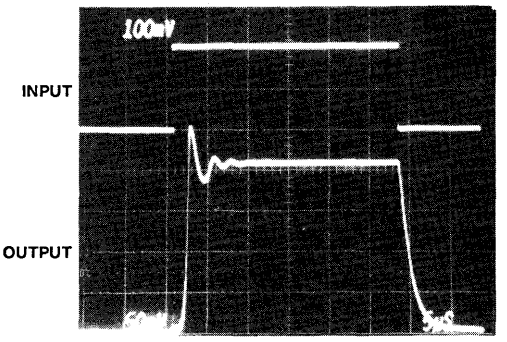
$+V_{SUPPLY}$ = +15V, $-V_{SUPPLY}$ = -15V

Vertical Scale: (Volts: Input = 1V/Div.)
(Volts: Output = 1V/Div.)
Horizontal Scale: (Time: 5µs/Div.)



$+V_{SUPPLY}$ = +5V, $-V_{SUPPLY}$ = 0V

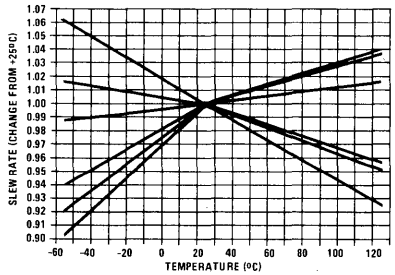
Vertical Scale: (Volts: Input = 100mV/Div.)
(Volts: Output = 50mV/Div.)
Horizontal Scale: (Time: 5µs/Div.)



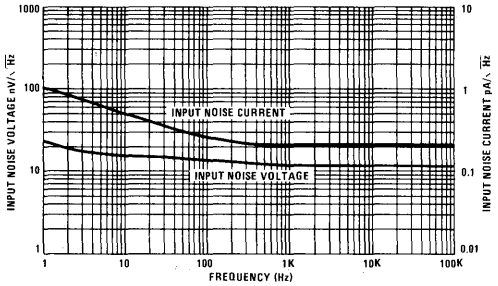
$+V_{SUPPLY}$ = +5V, $-V_{SUPPLY}$ = 0V

Typical Characteristics

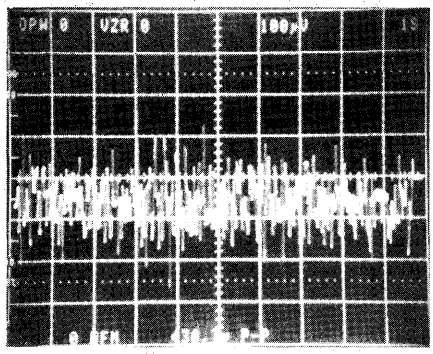
SLEW RATE vs. TEMPERATURE
Normalized to Unity at +25°C, 6 Representative Units



NOISE SPECTRAL DENSITY

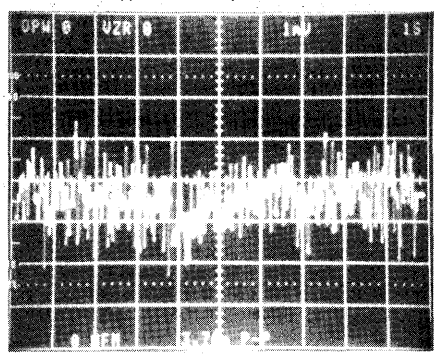


PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz
T_A = +25°C, A_V = 1000V/V



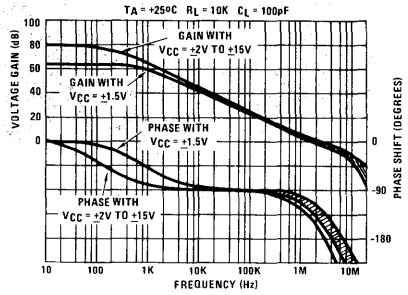
Horizontal Scale: (1sec/div)
Vertical Scale: (100µs/div)
430nV$_{p-p}$ RTI

PEAK-TO-PEAK 0.1Hz TO 1MHz
T_A = +25°C, A_V = 1000V/V

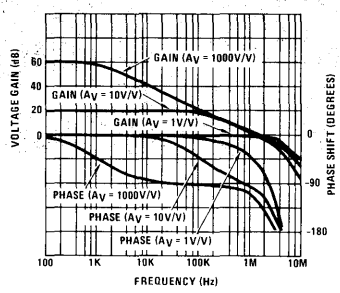


Horizontal Scale: (1sec/div)
Vertical Scale: (1mV/div)
3.70µV$_{p-p}$ RTI

FREQUENCY RESPONSE vs. SUPPLY VOLTAGE
T_A = +25°C, R_L = 10k, C_L = 100pF

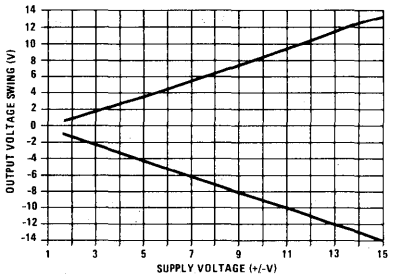


FREQUENCY RESPONSE AT VARIOUS GAINS
T_A = +25°C, V_{CC} = ±15V, R_L = 10k, C_L = 100pF

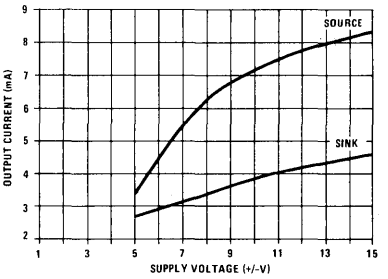


Typical Characteristics (Continued)

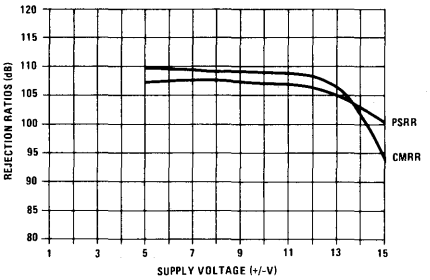
OUTPUT VOLTAGE SWING vs. SUPPLY VOLTAGE
(+25°C)



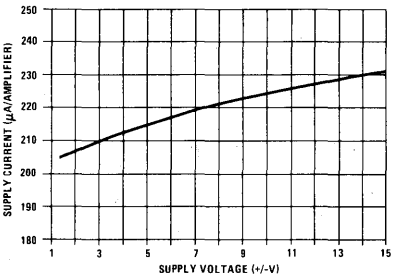
OUTPUT CURRENT vs. SUPPLY VOLTAGE
(+25°C)



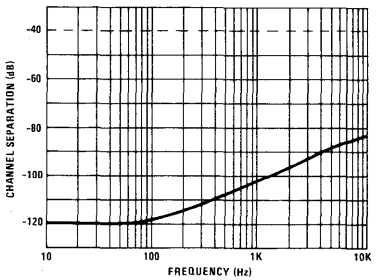
CMMR, PSRR vs. SUPPLY VOLTAGE
(+25°C)



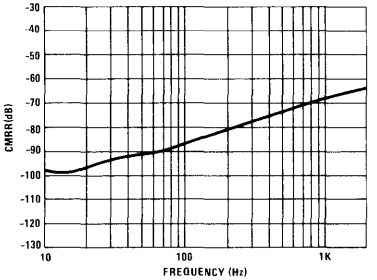
SUPPLY CURRENT vs. SUPPLY VOLTAGE
Per Amplifier (+25°C)



CHANNEL SEPARATION vs. FREQUENCY
V_{CC} = ±15V, T_A = +25°C



CMRR vs. FREQUENCY
T_A = +25°C, V_{CC} = ±15V



Applications Information

Independent Amplifiers

The HA-5152 dual op amp and the HA-5154 quad op amp consist of completely separate amplifier circuits. Unlike most duals and quads, these devices do not share a common bias network. Thus, one amplifier passing large, or noisy signals will have minimal effect on another channel carrying small, sensitive signals.

Loading

Although the standard load is 10kΩ, the HA-515X is capable of driving resistive loads down to 2kΩ and capacitive loads beyond 300pF.

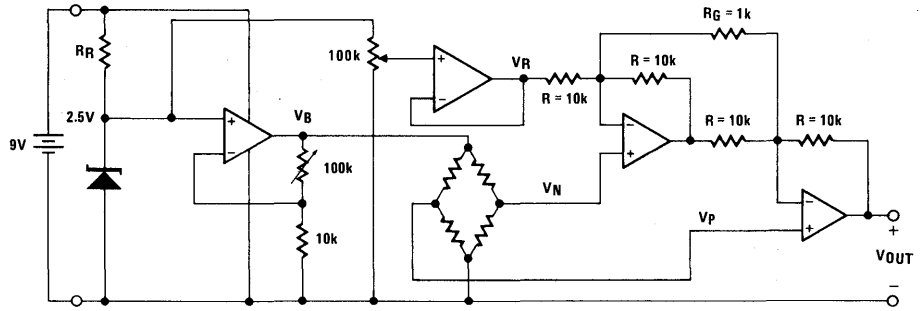
Input Stage

This amplifier uses a current amplifying input stage (see Application Note 544) and is not recommended for use in applications which involve large differential input voltages such as open-loop comparators. Most op amp applications use feedback and keep the input terminals at approximately the same voltage. The HA-515X will perform well in these circuits as long as the input terminals see less than 7 volts differential.

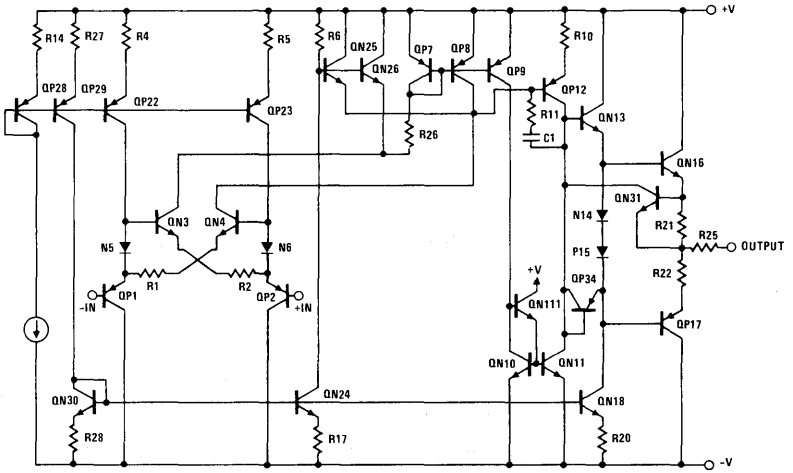
Typical Applications

The low power consumption of the HA-5154 makes it ideal for applications like battery-powered instrumentation where the bridge amplifier circuit below would be used. Choose a low-current zener voltage reference such as LM285Z-2.5 and select R_R accordingly. This circuit was evaluated using the resistor values shown and a laboratory voltage source for the 2.5V reference. With unmatched, off-the-shelf, 1% resistors, a gain accuracy of 1% to 2% can be expected. Temperature testing indicated a voltage offset tempco of less than 100µV/°C referred to output.

$$V_{OUT} = (V_P - V_N)\left[2\left(1 + \frac{R}{R_G}\right)\right] + V_R$$



Schematic



Die Characteristics

Transistor Count

HA-5151	34
HA-5142	68
HA-5144	136
Substrate Potential*	V-
Process	Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA1-5154 (-2, -5, -7)	101	33
HA1-5154 (/883)	75	22
HA2-5151 (-2, -5, -7)	206	56
HA2-5151 (/883)	168	50
HA2-5152 (-2, -5, -7)	184	50
HA2-5152 (/883)	143	43
HA3-5151 (-5)	90	40
HA3-5152 (-5)	80	20
HA3-5154 (-5)	75	20
HA7-5151 (-2, -5, -7)	210	117
HA7-5151 (/833)	90	40
HA7-5152 (-2, -5, -7)	177	92
HA7-5152 (/883)	80	20

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

NOTE: Consult Harris for LCC/PLCC information.

HARRIS

HA-5160/62

Wideband, JFET Input High Slew Rate, Uncompensated, Operational Amplifier

May 1990

Features

- Wide Gain Bandwidth ($A_V \geq 10$) 100MHz
- High Slew Rate 120V/μs
- Settling Time 280ns
- Power Bandwidth 1MHz
- Offset Voltage 1.0mV
- Bias Current 20pA

Applications

- Video and RF Amplifiers
- Data Acquisition
- Pulse Amplifiers
- Precision Signal Generation

Description

The HA-5160 is a wideband, uncompensated, operational amplifier with FET/Bipolar technologies and Dielectric Isolation. This monolithic amplifier features superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. This device has excellent phase margin at a closed loop gain of 10 without external compensation.

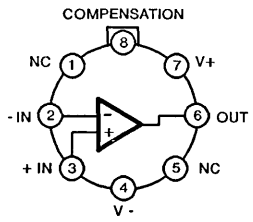
The HA-5160/5162 offers a number of important advantages over similiar FET input op amps from other manufacturers. In addition to superior bandwidth and settling characteristics, the Harris devices have nearly constant slew rate, bandwidth, and settling characteristics over the operating temperature range. This provides the user predictable performance in applications where settling time, full power bandwidth, closed loop bandwidth, or phase shift is critical. Note also that Harris specified all parameters at ambient (rather than junction) temperature to provide the designer meaningful data to predict actual operating performance.

Complementing the HA-5160/5162's predictable and excellent dynamic characteristics are very low input offset voltage, very low input bias current, and a very high input impedance. This ideal combination of features make these amplifiers most suitable for precision, high speed, data acquisition system designs and for a wide variety of signal conditioning applications. The HA-5160 provides excellent performance for applications which require both precision and high speed performance. The HA-5162 meets or exceeds the performance specifications of National's hybrid op amp, the LH0062.

The HA2-5160-2 denotes a temperature range of -55°C to +125°C and the HA2-5160/62-5 denotes a 0°C to +75°C range. Military version (/883) data sheets are available upon request.

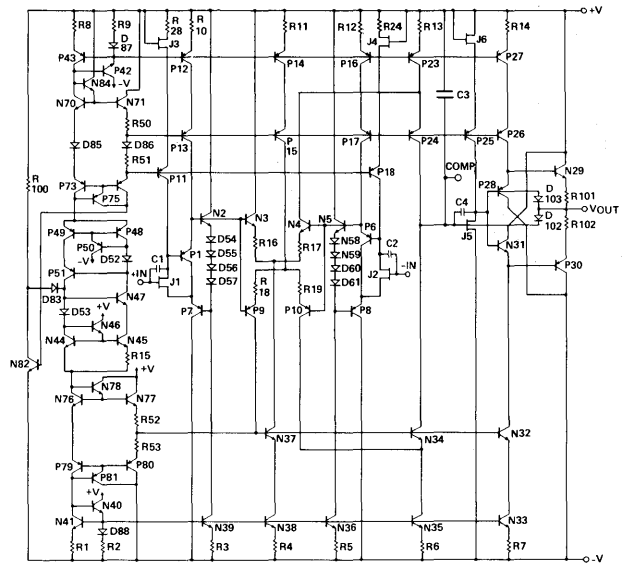
Pinout

HA2-5160/5162
(TO-99 METAL CAN)
TOP VIEW



Case Connected to V-

Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Voltage Between V+ and V- 40V
Differential Input Voltage ..... ±40V
Peak Output Current ..... Full Short Circuit Protection
Internal Power Dissipation (Note 2) 675mW

Operating Temperature Ranges:

HA-5160-2 ..... $-55^oC \leq T_A \leq +125^oC$
HA-5160-5 ..... $0^oC \leq T_A \leq +75^oC$
HA-5162-5 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature (Note 2) ..... $+175^oC$

Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified.

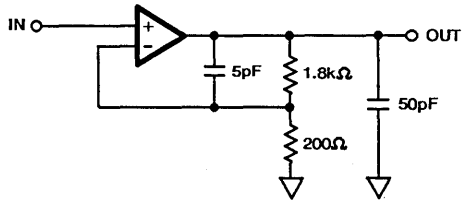
PARAMETER	TEMP	HA-5160-2 -55°C to 125°C			HA-5160-5 0°C to +75°C			HA-5162-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage	+25°C	-	1	3	-	1	3	-	3	15	mV
	Full	-	3	5	-	3	5	-	5	20	mV
Offset Voltage Average Drift	Full	-	10	-	-	20	-	-	20	35	µV/°C
Bias Current	+25°C	-	20	50	-	20	50	-	20	65	pA
	Full	-	5	10	-	5	10	-	5	10	nA
Offset Current	+25°C	-	2	10	-	2	10	-	2	10	pA
	Full	-	2	5	-	2	5	-	2	5	nA
Input Capacitance	+25°C	-	5	-	-	5	-	-	5	-	pF
Input Resistance	+25°C	-	10^{12}	-	-	10^{12}	-	-	10^{12}	-	Ω
Common Mode Range	Full	±10	±11	-	±10	±11	-	±10	±11	-	V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 3)	+25°C	75K	150K	-	75K	150K	-	25K	100K	-	V/V
	Full	60K	100K	-	60K	100K	-	25K	75K	-	V/V
Common Mode Rejection Ratio (Note 4)	Full	74	80	-	74	80	-	70	80	-	dB
Minimum Stable Gain	+25°C	10	-	-	10	-	-	10	-	-	V/V
Gain Bandwidth Product ($A_V \geq 10$)	Full	-	100	-	-	100	-	-	100	-	MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing	+25°C	±10	±11	-	±10	±11	-	±10	±11	-	V
(Note 5)	Full	±10	±11	-	±10	±11	-	±10	±11	-	V
Output Current (Note 6)	+25°C	±10	±20	-	±10	±20	-	±10	±20	-	mA
Output Short Circuit Current	+25°C	-	±35	-	-	±35	-	-	±35	-	mA
Full Power Bandwidth (Note 3, 7)	+25°C	1.6	1.9	-	1.6	1.9	-	0.8	1.1	-	MHz
Output Resistance (Note 8)	+25°C	-	50	-	-	50	-	-	50	-	Ω
TRANSIENT RESPONSE (Note 9)											
Rise Time	+25°C	-	20	-	-	20	-	-	20	-	ns
Slew Rate	+25°C	100	120	-	100	120	-	50	70	-	V/µs
Settling Time (Note 10)	+25°C	-	280	-	-	280	-	-	400	-	ns
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full	-	8	10	-	8	10	-	8	12	mA
Power Supply Rejection Ratio (Note 11)	+25°C	74	86	-	74	86	-	70	86	-	dB

NOTES:

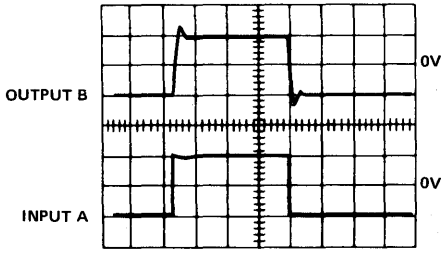
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8mW/°C for operation at ambient temperatures above +75°C.
3. V_{OUT} = ±10V, R_L = 2K
4. V_{CM} = ±10V DC
5. R_L = 2K
6. V_{OUT} = ±10V
7. Full Power Bandwidth guaranteed, based on slew rate measurement using FPWB = $\frac{\text{Slew Rate}}{2\pi V_{peak}}$
8. Output resistance measured under open loop conditions.
9. Refer to Test circuits section of the data sheet, where A_V = +10.
10. Settling Time is measured to 0.2% of final value for a 10 volt output step and A_V = 10.
11. V_{SUPPLY} = ±10V DC to ±20V DC

Test Circuits

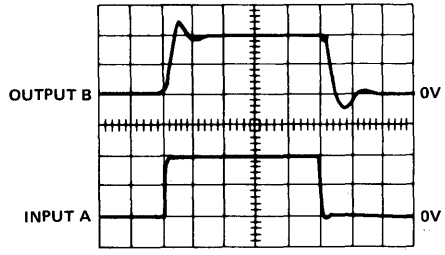
LARGE AND SMALL SIGNAL RESPONSE CIRCUIT



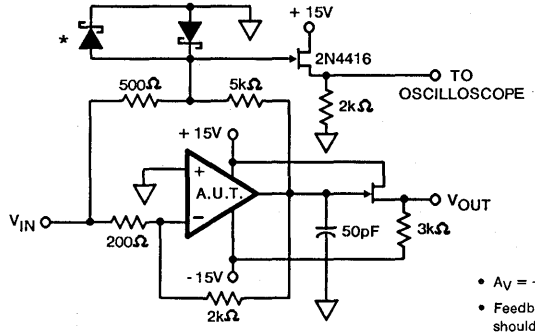
LARGE SIGNAL RESPONSE
Vertical Scale: A = 0.5V/Div., B = 5V/Div.
Horizontal Scale: Time = 500ns/Div.



SMALL SIGNAL RESPONSE
Vertical Scale: A = 10mV/Div., B = 100mV/Div.
Horizontal Scale: Time = 100ns/Div.



SETTLING TIME CIRCUIT

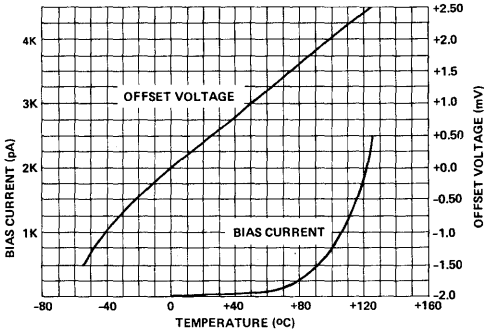


- A_V = -10
- Feedback and summing resistors should be 0.1% matched.

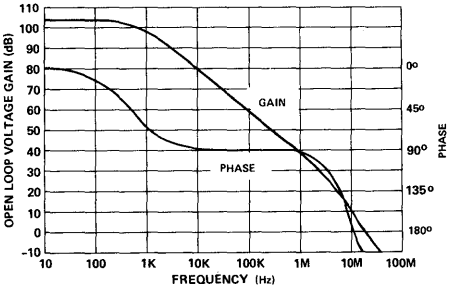
* Clipping Diodes are optional. HP5082-2810 recommended.

Typical Performance Curves

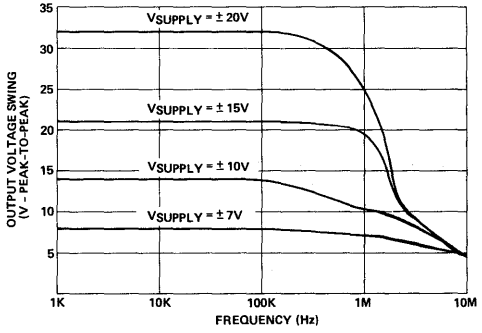
INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE



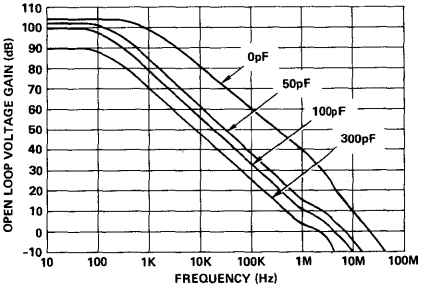
OPEN LOOP FREQUENCY RESPONSE



OUTPUT VOLTAGE SWING vs. FREQUENCY

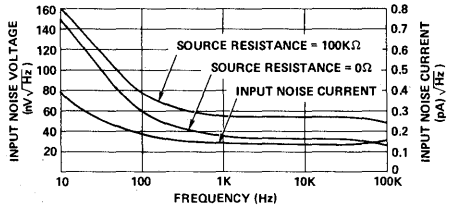


OPEN LOOP FREQUENCY RESPONSE FOR VARIOUS BANDWIDTH CONTROL CAPACITANCES

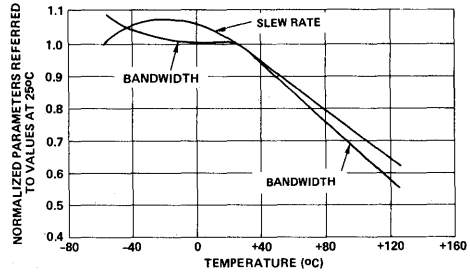


Typical Performance Curves (Continued)

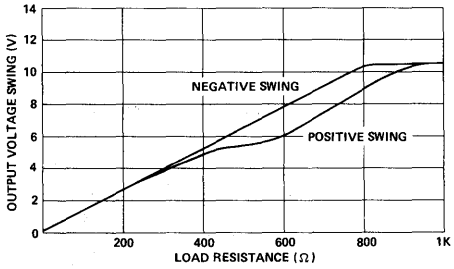
INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY



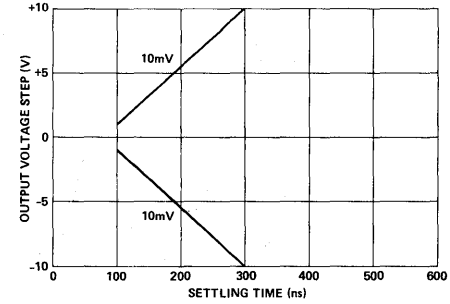
NORMALIZED AC PARAMETERS vs. TEMPERATURE



OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE

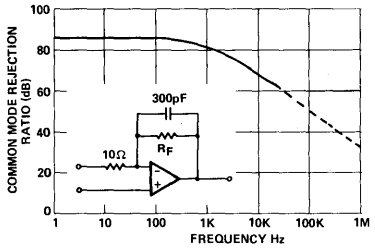


SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES

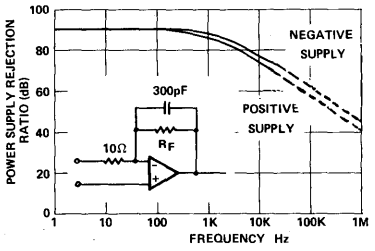


Typical Performance Curves (Continued)

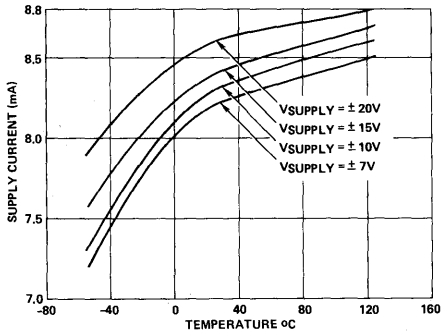
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



POWER SUPPLY CURRENT vs. TEMPERATURE



Die Characteristics

Transistor Count 82

Die Dimensions ..... 131 x 72 x 19 mils (3330 x 1830 x 483µm)

Substrate Potential (Powered Up) ..... None

Process ..... Bipolar/JFET DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-5160 (-8, /883) (Gold Eutectic Die Attach)	103	31
HA2-5160/5162 (-2, -5, -7) (Glass Die Attach)	146	38

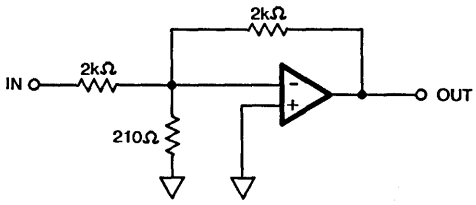
Applying the HA-5160/5162

1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01µF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. STABILITY: The phase margin of the HA-5160/5162 will be improved by connecting a small capacitor (>10pF) between the output and the inverting input of the device This small capacitor compensated for the input capacitance of the FET.
3. CAPACITIVE LOADS: When driving large capacitive loads (>100pF), it is suggested that a small resistor (≈100Ω) be connected in series with the output of the device and inside the feedback loop.
4. POWER SUPPLY MINIMUM: The absolute supply minimum is ±6V and the safe level is ±7V.

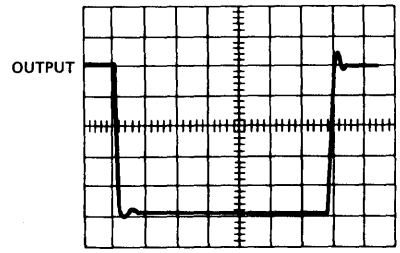
Applications

Suggested Compensation For Unity Gain Stability*

INVERTING UNITY GAIN CIRCUIT

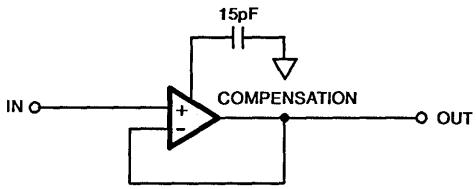


INVERTING UNITY GAIN PULSE RESPONSE

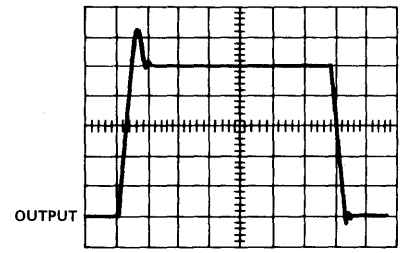


Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 500ns/Div.)

NONINVERTING UNITY GAIN CIRCUIT



NONINVERTING UNITY GAIN PULSE RESPONSE



Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 500ns/Div.)

* Values Were Determined Experimentally
For Optimum Speed and Settling Time.

HARRIS

HA-5170

Precision JFET Input Operational Amplifier

May 1990

Features

- Low Offset Voltage 100μV
- Low Offset Voltage Drift ..... 2μV/°C
- Low Noise ..... 10nV/√Hz
- High Open Loop Gain ..... 600K V/V
- Wide Bandwidth 8MHz
- Unity Gain Stable

Applications

- High Gain Instrumentation Amplifiers
- Precision Data Acquisition
- Precision Integrators
- Precision Threshold Detectors
- For Further Design Ideas, Refer to App. Note 540.

Description

The Harris HA-5170 is a precision, JFET input, operational amplifier which features low noise, low offset voltage and low offset voltage drift. Constructed using FET/Bipolar technology, the Harris Dielectric Isolation (DI) process, and laser trimming this amplifier offers low input bias and offset currents. This operational amplifier design also completely eliminates the troublesome errors due to warm-up drift.

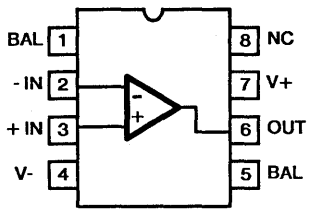
Complementing these excellent input characteristics are dynamic performance characteristics never before available from precision operational amplifiers. An 8V/μs slew rate and 8MHz bandwidth allow the designer to extend precision instrumentation applications in both speed and bandwidth. These characteristics make the HA-5170 well suited for precision integrator amplifier designs.

The superior input characteristics also make the HA-5170 ideally suited for transducer signal amplifiers, precision voltage followers and precision data acquisition systems. For application assistance, please refer to Application Note 540 addressing specifically this device.

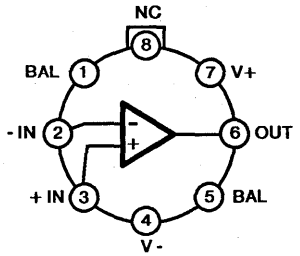
The HA-5170 is available in Metal Can (TO-99) and Ceramic Mini-DIP packages. HA-5170-2 denotes a -55°C to +125°C temperature range and HA-5170-5 denotes the 0°C to +75°C range. Military version (/883) product and data sheets available upon request.

Pinouts

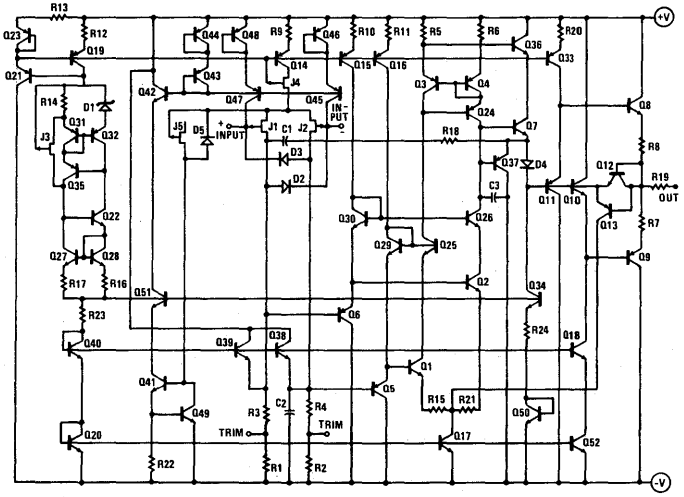
HA7-5170 (CERAMIC MINI-DIP)
TOP VIEW



HA2-5170 (TO-99 METAL CAN)
TOP VIEW



Schematic



3 OPERATIONAL AMPLIFIERS

Absolute Maximum Ratings (Note)

T_A = +25°C, Unless Otherwise Specified.

Voltage Between V+ and V- Terminals 44.0V
Differential Input Voltage..... ±30.0V
Output Short Circuit Duration ..... Indefinite
Power Dissipation (Note 2)..... 675mW
Maximum Junction Temperature..... +175°C

Operating Temperature Ranges

HA-5170-2 ..... $-55°C \leq T_A \leq +125°C$
HA-5170-5 ..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range ..... $-65°C \leq T_A \leq +150°C$

Electrical Specifications

V+ = +15V, V- = -15V, Unless Otherwise Specified.

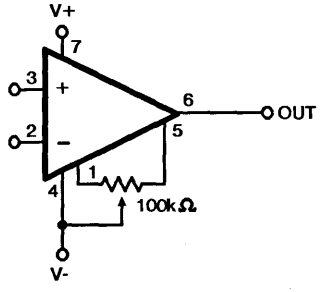
PARAMETER	TEMP	HA-5170-2 -55°C to +125°C			HA-5170-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	0.1	0.3	-	0.1	0.3	mV
	Full	-	-	0.5	-	-	0.5	mV
Average Offset Voltage Drift (Note 3)	Full	-	2	5	-	2	5	µV/°C
Bias Current	+25°C	-	20	100	-	20	100	pA
	Full	-	3	30	-	0.1	2	nA
Bias Current Average Drift	Full	-	3	-	-	3	-	pA/°C
Offset Current	+25°C	-	3	30	-	3	60	pA
	Full	-	-	5	-	-	0.1	nA
Offset Current Average Drift (Note 3)	Full	-	0.3	1	-	0.3	1	pA/°C
Common Mode Range	Full	±10	+15.1 -12	-	±10	+15.1 -12	-	V V
Differential Input Capacitance	+25°C	-	80	100	-	80	100	pF
Differential Input Resistance (Note 3)	+25°C	$1x10^{10}$	$6x10^{10}$	-	$1x10^{10}$	$6x10^{10}$	-	Ω
Input Capacitance (Single Ended)	+25°C	-	12	-	-	12	-	pF
Input Noise Voltage 0.1Hz to10Hz (Note 3)	+25°C	-	0.5	5	-	0.5	5	μV_{p-p}
Input Noise Voltage Density (Note 3)								
f_O = 10Hz	+25°C	-	20	150	-	20	150	$nV/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	12	50	-	12	50	$nV/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	10	25	-	10	25	$nV/\sqrt{Hz}$
Input Noise Current Density (Note 3)								
f_O = 10Hz	+25°C	-	0.05	-	-	0.05	-	$pA/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	0.01	-	-	0.01	-	$pA/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	0.01	0.1	-	0.01	0.1	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 4)	+25°C	300K	600K	-	300K	600K	-	V/V
	Full	200K	-	-	250K	-	-	V/V
Common Mode Rejection Ratio (Note 5)	Full	85	100	-	90	100	-	dB
Minimum Stable Gain	+25°C	1	-	-	1	-	-	V/V
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	4	8	-	4	8	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12	-	±10	±12	-	V
Full Power Bandwidth (Note 7)	+25°C	80	120	-	80	120	-	kHz
Output Current (Note 8)	+25°C	±10	±15	-	±10	±15	-	mA
Output Resistance (Note 3 & 9)	+25°C	-	45	100	-	45	100	Ω
TRANSIENT RESPONSE								
Rise Time	+25°C	-	45	100	-	45	100	ns
Slew Rate	+25°C	5	8	-	5	8	-	V/µs
Settling Time (Notes 3 & 10)	+25°C	-	1	5	-	1	5	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	1.9	2.5	-	1.9	2.5	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105	-	90	105	-	dB

NOTES:

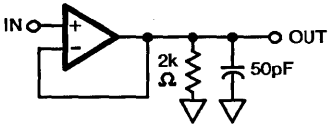
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate at 6.8 mW/°C for operation at ambient temperatures above +75°C.
3. Parameter is not 100% tested. 90% of all units meet or exceed these specifications.
4. V_{OUT} = ±10, R_L = 2kΩ.
5. ΔV_{CM} = ±10V D.C.
6. R_L = 2kΩ.
7. R_L = 2kΩ; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi V_{PEAK}}$
8. V_{OUT} = ±10V. I_{SC} turns on at ≅ 23mA.
9. Output resistance measured under open loop conditions (f = 100Hz).
10. Settling time is measured to 0.1% of final value for a 10V output step and A_V = -1.
11. ΔV_{SUPPLY} = ±10V D.C. to ±20V D.C.

Test Circuits

V_{OS} ADJUSTMENT

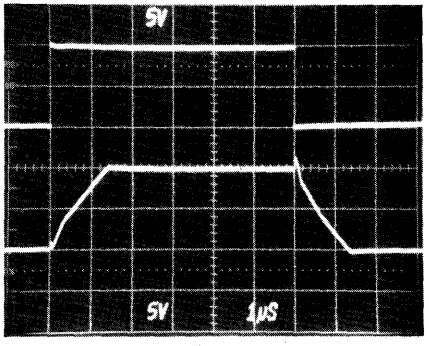


LARGE AND SMALL SIGNAL RESPONSE CIRCUIT

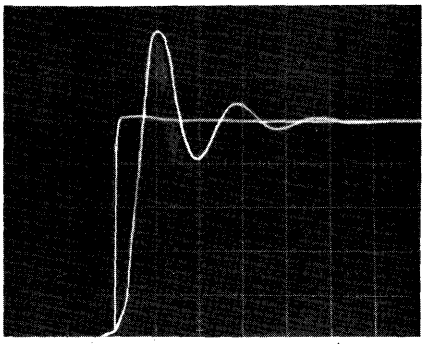


Tested Offset Adjustment Range is $|V_{OS} + 1mV|$ minimum referred to output.
Typical range is ±5mV with R_T = 1kΩ and ±15mV with R_T = 100kΩ.

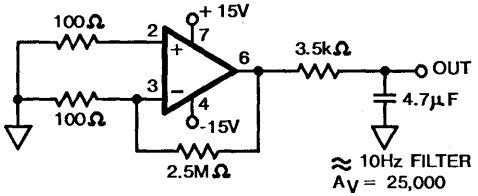
LARGE SIGNAL RESPONSE
Vertical Scale: 5V/Div.
Horizontal Scale: 500ns/Div.



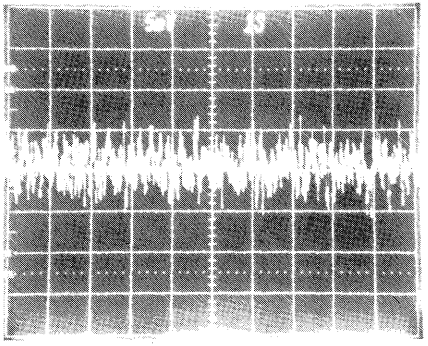
SMALL SIGNAL RESPONSE
Vertical Scale: 10mV/Div.
Horizontal Scale: 100ns/Div.



LOW FREQUENCY NOISE TEST CIRCUIT

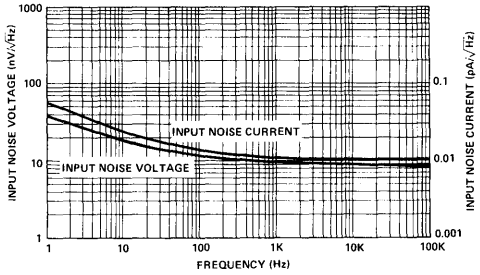


HA-5170 LOW FREQUENCY NOISE (0.1Hz TO 10Hz)
Vertical Scale: 200nV/Div. (Noise Referred to Input)
5mV/Div. at Output, A_{VCL} = 25,000.
Horizontal Scale: 1 Sec./Div.

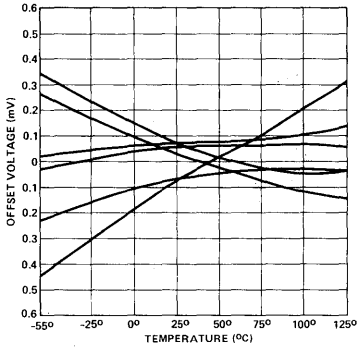


Typical Performance Curves

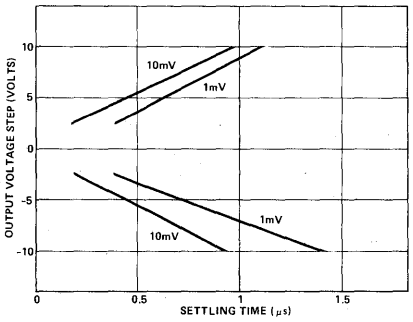
INPUT VOLTAGE NOISE vs. FREQUENCY



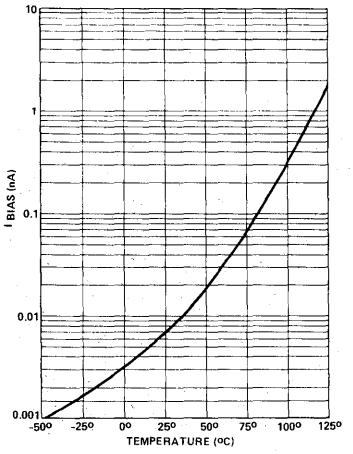
OFFSET VOLTAGE vs. TEMPERATURE DRIFT OF REPRESENTATIVE UNITS



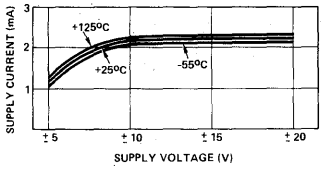
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



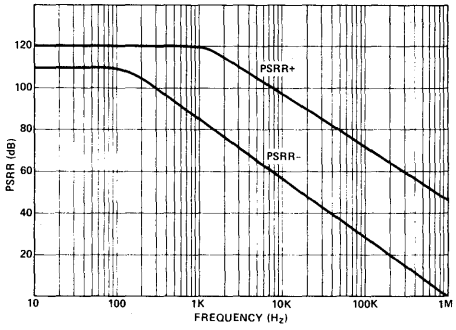
BIAS CURRENT vs. TEMPERATURE



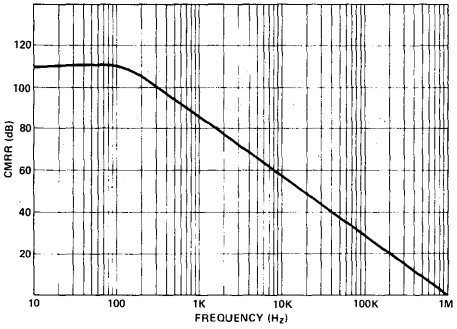
POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE AND TEMPERATURE



POWER SUPPLY REJECTION RATIO vs. FREQUENCY

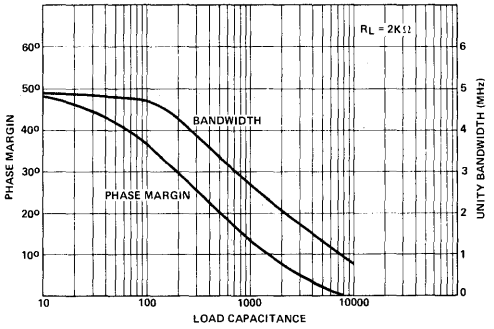


COMMON MODE REJECTION RATIO vs. FREQUENCY

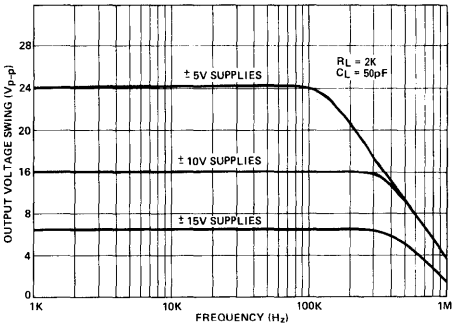


Typical Performance Curves (Continued)

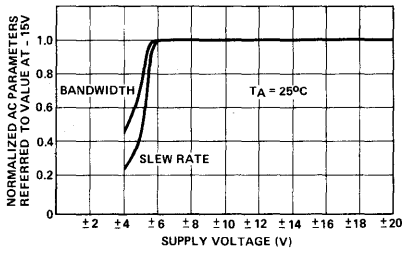
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



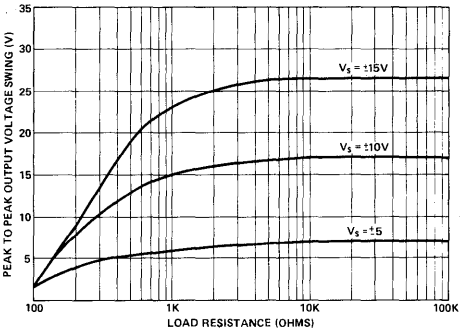
OUTPUT VOLTAGE SWING vs. FREQUENCY AND SUPPLY VOLTAGE



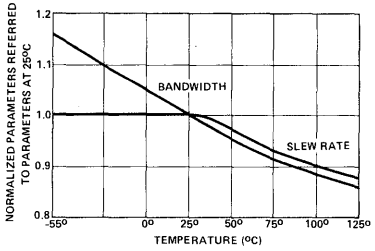
NORMALIZED AC PARAMETERS vs. SUPPLY VOLTAGE



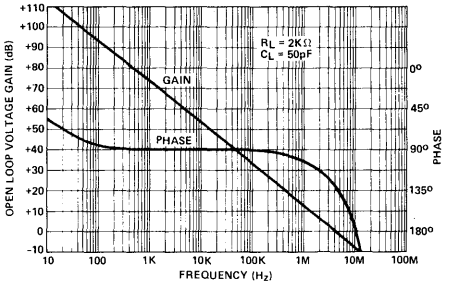
MAXIMUM OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



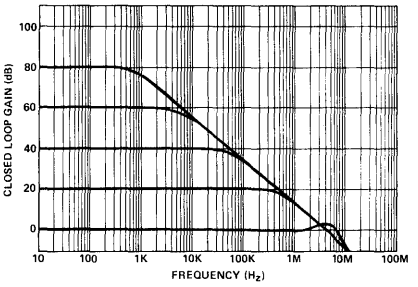
NORMALIZED AC PARAMETERS vs. TEMPERATURE



OPEN LOOP FREQUENCY RESPONSE



CLOSED LOOP FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS



HARRIS

HA-5177

Ultra-Low Offset Voltage Operational Amplifier

May 1990

Features

- Low Offset Voltage 10μV
- Low Offset Voltage Drift ..... 0.1μV/°C
- High Voltage Gain 150dB
- High CMRR 140dB
- High PSRR 135dB
- Low Noise ..... 3.8nV/$\sqrt{Hz}$
- Low Power Consumption ..... 51mW Max.

Applications

- High Gain Instrumentation Amplifiers
- Precision Control Systems
- Precision Integrators
- High Resolution Data Converters
- Precision Threshold Detectors
- Low Level Transducer Amplifiers

Description

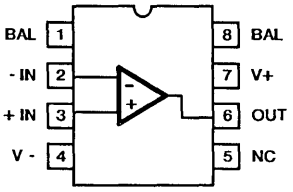
The HA-5177 is a monolithic, all bipolar, precision operational amplifier, utilizing Harris dielectric isolation and advance processing techniques. This design features a combination of precision input characteristics, wide bandwidth (2MHz) and high speed (0.8V/μs).

The HA-5177 uses advanced matching techniques and laser trimming to produce low offset voltage (10μV) and low offset voltage drift (0.1μV/°C). This design also features low voltage noise (3.8nV/$\sqrt{Hz}$), low current noise (0.32pA/$\sqrt{Hz}$), nanoamp input currents, and 120dB minimum gain. These outstanding features along with high CMRR (140dB) and high PSRR (135dB) make this unity gain stable amplifier ideal for high resolution data acquisition systems, precision integrators, and low level transducer amplifiers.

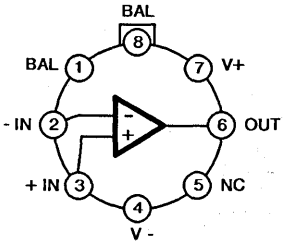
The HA-5177 can be used as a direct replacement for the OP05, OP07, and OP77 while offering higher bandwidth and slew rate. The HA-5177 is packaged in an 8 pin (TO-99) Metal Can and Ceramic 8 pin Mini-DIP and is pin compatible with many existing op amps. See the HA-5177/883 data sheet for military grade parts and LCC package.

Pinouts

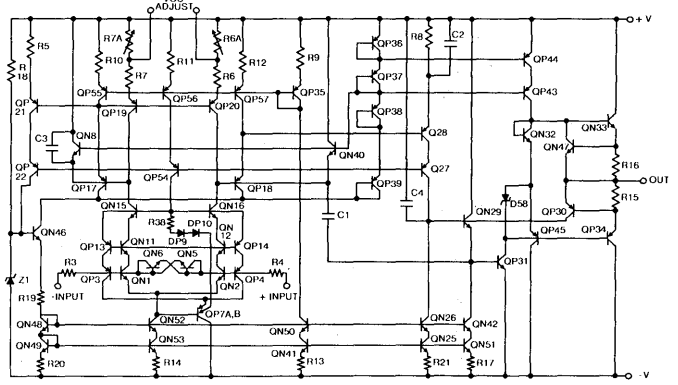
HA7-5177 (CERAMIC MINI-DIP)
TOP VIEW



HA2-5177 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 44V
Differential Input Voltage..... ±15V
Output Current ..... Short Circuit Protected

Operating Temperature Ranges

HA-5177A/5177-2 .....$-55^oC \leq T_A \leq +125^oC$
HA-5177A/5177-5 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range .....$-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature..... $+175^oC$

Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified

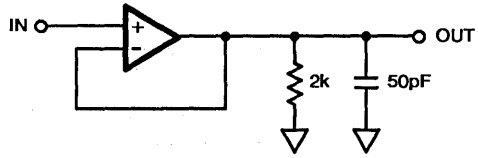
PARAMETER	TEMP	HA-5177A MIN	HA-5177A TYP	HA-5177A MAX	HA-5177 MIN	HA-5177 TYP	HA-5177 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	10	25	-	20	60	µV
	Full	-	25	60	-	40	100	µV
Average Offset Voltage Drift	Full	-	0.1	0.3	-	0.2	0.6	µV/°C
Bias Current	+25°C	-	1.2	2	-	1.2	6	nA
	Full	-	2.4	4	-	2.4	8	nA
Bias Current Average Drift	Full	-	8	25	-	15	35	pA/°C
Offset Current	+25°C	-	0.6	2	-	0.6	6	nA
	Full	-	1.0	4	-	1.0	8	nA
Offset Current Average Drift	Full	-	1.5	25	-	1.5	50	pA/°C
Common Mode Range	Full	±12	-	-	±12	-	-	V
Differential Input Resistance	+25°C	-	47	-	-	47	-	MΩ
Input Noise Voltage 0.1Hz to 10Hz	+25°C	-	0.35	0.6	-	0.35	0.6	μV_{p-p}
Input Noise Voltage Density								
f_o = 10Hz	+25°C	-	13	18	-	13	18	$nV/\sqrt{Hz}$
f_o = 100Hz	+25°C	-	10	13	-	10	13	$nV/\sqrt{Hz}$
f_o = 1000Hz	+25°C	-		11	-		11	$nV/\sqrt{Hz}$
Input Noise Current 0.1Hz to 10Hz	+25°C	-	14	45	-	14	45	pA_{p-p}
Input Noise Current Density								
f_o = 10Hz	+25°C	-	1.1	4	-	7.1	10	$pA/\sqrt{Hz}$
f_o = 100Hz	+25°C	-	0.55	2.3	-	3.3	5	$pA/\sqrt{Hz}$
f_o = 1000Hz	+25°C	-	0.32	1	-	1.2	2	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 2)	+25°C	134	150	-	126	150	-	dB
	Full	126	140	-	120	140	-	dB
Common Mode Rejection Ratio (Note 3)	Full	120	140	-	110	140	-	dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	0.6	2	-	0.6	2	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing R_L = 600Ω	+25°C	±10	±12.5	-	±10	±12.5	-	V
R_L = 2K	+25°C	±12	±13	-	±12	±13	-	V
R_L = 2K	Full	±12	±12.5	-	±12	±12.5	-	V
Full Power Bandwidth (Note 5)	+25°C	8	10	-	8	10	-	kHz
Output Current (Note 6)	+25°C	15	20	-	15	20	-	mA
Output Resistance	+25°C	-	60	-	-	60	-	Ω
TRANSIENT RESPONSE								
Rise Time (Note 10)	+25°C	-	310	420	-	310	420	ns
Slew Rate (Note 11)	+25°C	0.5	0.8	-	0.5	0.8	-	V/µs
Settling Time (Notes 7, 8)	+25°C	-	14	-	-	14	-	µs
Overshoot (Note 10)	+25°C	-	10	40	-	10	40	%
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	1.2	1.7	-	1.2	1.7	mA
Power Supply Rejection Ratio (Note)	Full	110	135	-	110	135	-	dB

NOTES:

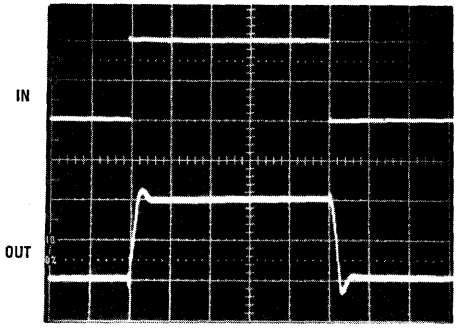
1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, R_L = 2kΩ
3. ΔV_{CM} = ±10V D.C.
4. R_L = 2K
5. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$, V_{PEAK} = 10V.
6. V_{OUT} = ±10.
7. Refer to test circuits section of the data sheet.
8. Settling time is measured to 0.1% of final value for a 10V output step and A_V = +1.
9. ΔV_{SUPPLY} = ±10V D.C. to ±20V D.C.
10. A_V = 1, R_L = 2K, V_{OUT} = ±200mV
11. A_V = 1, R_L = 2K, V_{OUT} = 0 to ±3V

Test Circuits

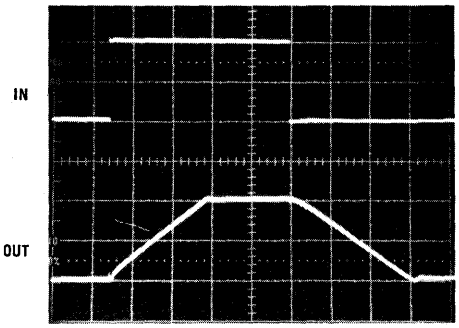
SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT



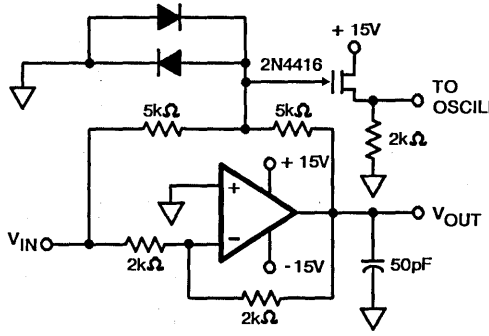
SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: 100mV/Div.)
Horizontal Scale: (Time: 2μs/Div.)



LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: 5V/Div.)
Horizontal Scale: (Time: 5μs/Div.)



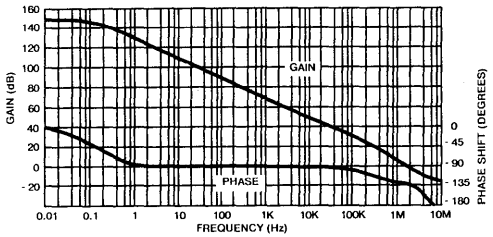
SETTLING TIME CIRCUIT



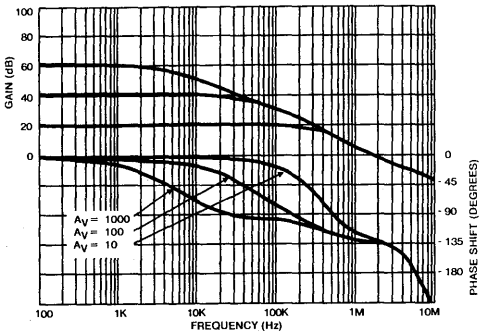
- $A_V = -1$
- Feedback and summing resistors should be 0.1% matched.
- Clipping diodes are optional. HP5082-2810 recommended.

Typical Performance Curves $V_S = \pm 15V$, $T_A = +25^oC$

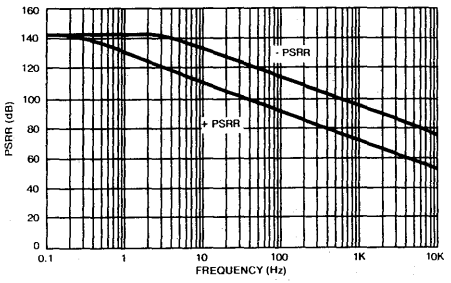
OPEN LOOP GAIN AND PHASE vs. FREQUENCY



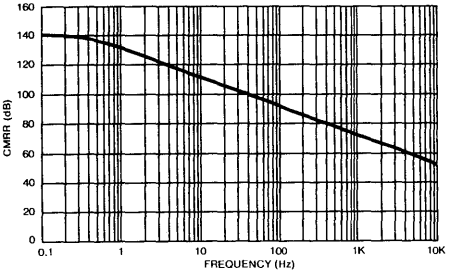
VARIOUS CLOSED LOOP GAINS vs. FREQUENCY
$R_L = 2K$, $C_L = 50pF$



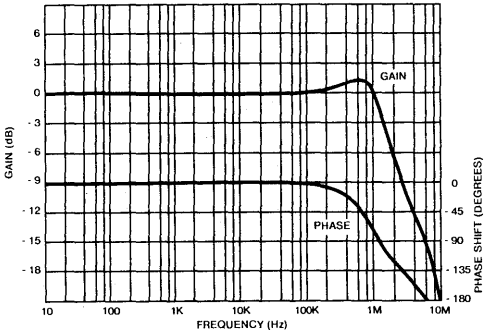
PSRR vs. FREQUENCY



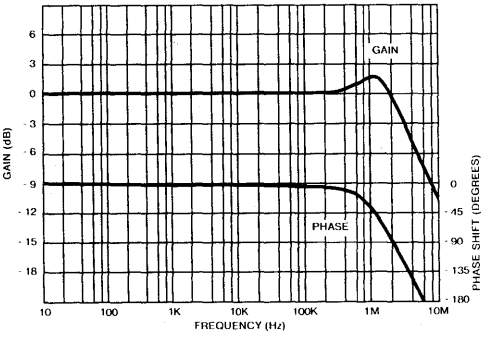
CMRR vs. FREQUENCY



CLOSED LOOP GAIN AND PHASE vs. FREQUENCY
$A_V = -1$, $R_L = 2K$, $C_L = 50pF$

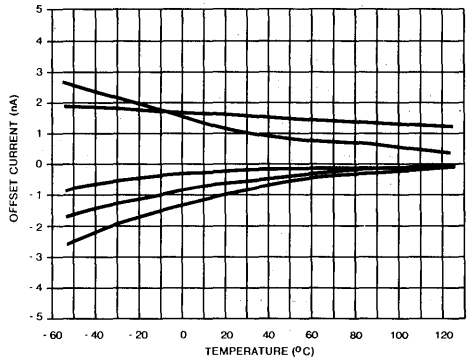


CLOSED LOOP GAIN AND PHASE vs. FREQUENCY
$A_V = +1$, $R_L = 2K$, $C_L = 50pF$

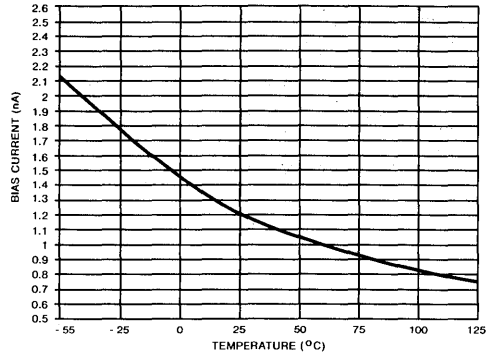


Typical Performance Curves $V_S = \pm 15V$, $T_A = +25^oC$

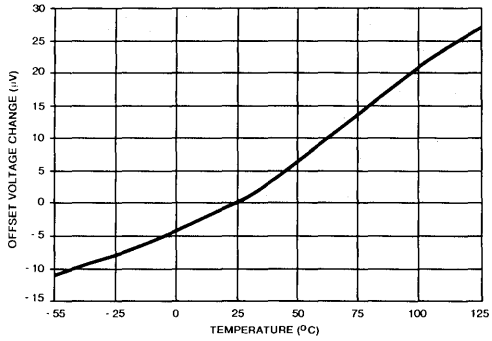
OFFSET CURRENT vs. TEMPERATURE
Five Representative Units



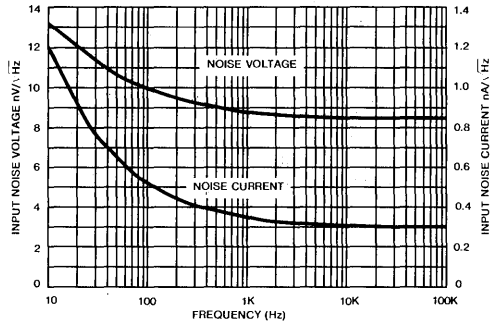
BIAS CURRENT vs. TEMPERATURE



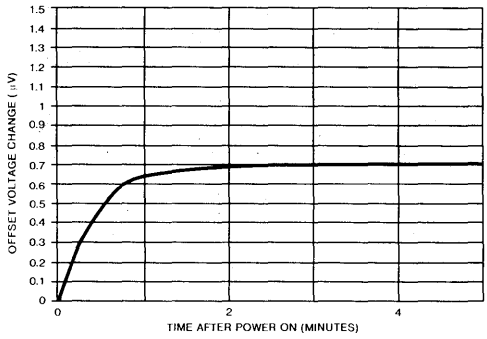
OFFSET VOLTAGE vs. TEMPERATURE



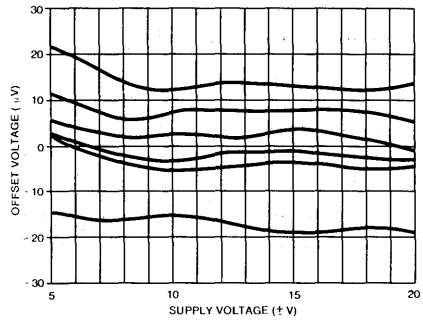
INPUT NOISE vs. FREQUENCY



OFFSET VOLTAGE WARM-UP DRIFT

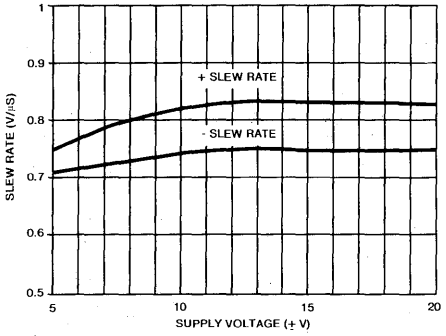


OFFSET VOLTAGE vs. SUPPLY VOLTAGE
Six Representative Units

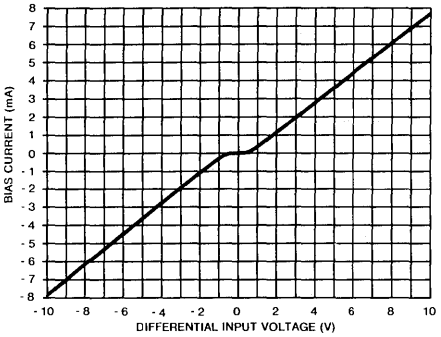


Typical Performance Curves $V_S = \pm15V, T_A = +25^oC$

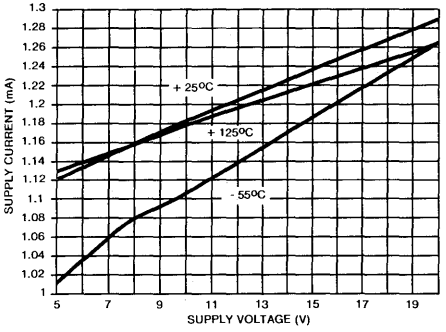
SLEW RATE vs. SUPPLY VOLTAGE
$A_V = -1, R_L = 2K, C_L = 50pF$



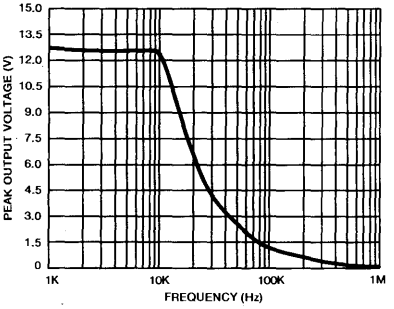
BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



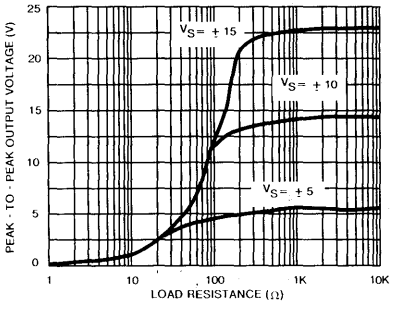
SUPPLY CURRENT vs. SUPPLY VOLTAGE



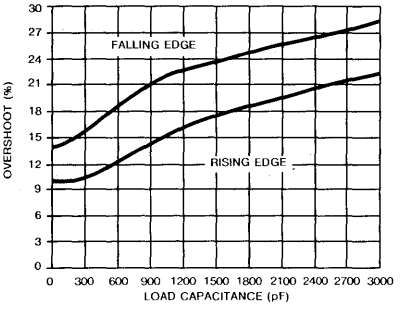
OUTPUT VOLTAGE vs. FREQUENCY
$A_V = -1, R_L = 2K, C_L = 50pF$



OUTPUT VOLTAGE vs. LOAD RESISTANCE
$A_V = -1, V_{IN} = 100Hz, C_L = 50pF$



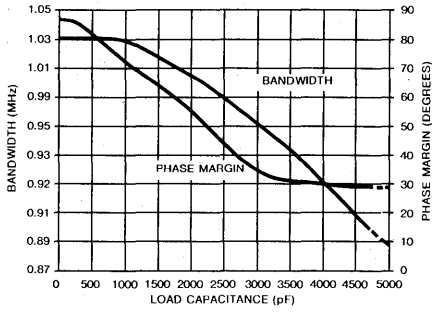
OVERSHOOT vs. LOAD CAPACITANCE
$V_S = \pm15V, A_V = +1, V_{OUT} = \pm200mV$



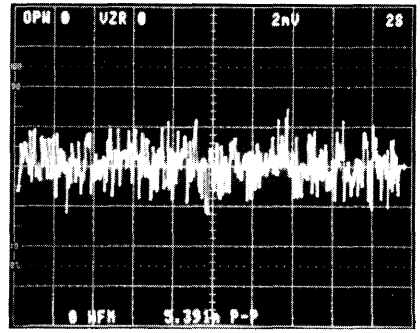
3 OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_S = \pm15V$, $T_A = +25^oC$

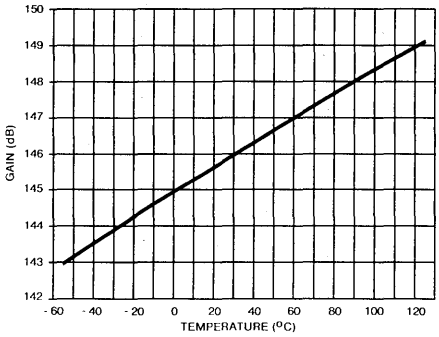
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE
$A_V = +1$



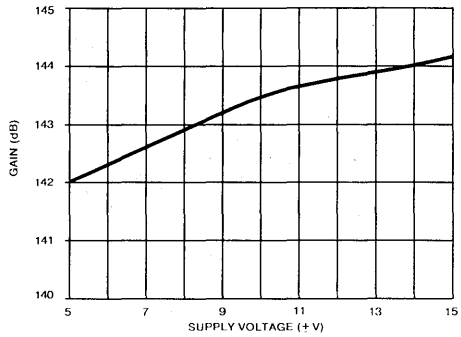
PEAK-TO-PEAK NOISE 0.1Hz TO 10Hz
$A_V = 25{,}000$, $0.22\mu V_{p-p}$ RTI



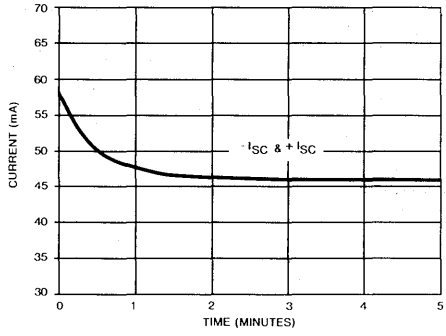
OPEN LOOP GAIN vs. TEMPERATURE



OPEN LOOP GAIN vs. SUPPLY VOLTAGE



OUTPUT SHORT CIRCUIT CURRENT vs. TIME
$V_{IN} = \pm10V$, $A_V = -1$



Applications Information

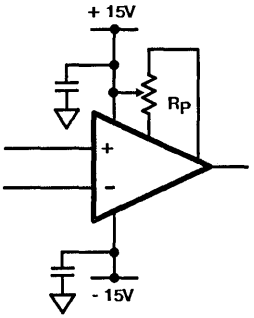
Operation Below ±5V Supply

The HA-5177 performs well down to ±5V supplies.

At ±5V supplies there is a slight degradation of slew rate and open loop gain. There is very little change in bias currents and offset voltage.

Offset Adjustment

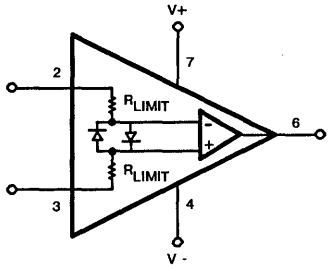
The following is the recommended V_{IO} adjust configuration:



Settling RP = 20K will give an adjustment range of ±2.6mV.

Input Protection

The HA-5177 input stage has built in back-to-back protection diodes with series current limiting resistors.



The Bias currents will increase when a differential voltage of 0.7 volts is exceeded.

The internal current limiting resistors sufficiently limit current therefore, no external resistors are required.

Refer to the "Bias Current vs. Differential Input Voltage" curve in the Typical Performance Curves section.

Die Characteristics

Transistor Count 71

Die Dimensions ..... 102 x 71.7 x 19 mils (2590 x 1820 x 485µm)

Substrate Potential* ..... V-

Process ..... High Frequency Bipolar DI

Passivation ..... Silox

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic Mini-DIP, HA7-5177	154	74
Metal Can TO-99, HA2-5177	124	38

* The substrate may be left floating (insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS

HA-5180

Low Bias Current, Low Power JFET Input Operational Amplifier

May 1990

Features

- Ultra Low Bias Current 250fA
- Low Power Supply Current 0.8mA
- Low Offset Voltage ..... 0.5mV Max.
- Unity Gain Bandwidth 2MHz
- Slew Rate 7V/μs

Applications

- Electrometer Amplifier Designs
- Photo Current Detectors
- Precision, Long-Term Integrators
- Low Drift Sample & Hold Circuits
- Very High Impedance Buffers
- High Impedance Biological Micro Probes
- Refer to Application Note 555

Description

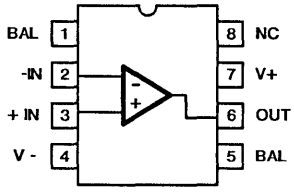
The Harris HA-5180 is an ultra low input bias current, JFET input, monolithic operational amplifier which also features low power, low offset voltage and excellent AC characteristics. Employing FET/Bipolar construction coupled with dielectric isolation this operational amplifier offers the lowest input bias currents (250fA typical) available in any monolithic operational amplifier. The HA-5180 has another unique feature in which the offset bias current may be nulled by externally adjusting the offset voltage.

The HA-5180 also offers excellent AC performance not previously available in similar hybrid or monolithic op amp designs. The 2MHz bandwidth and 7V/μs slew rate of the HA-5180 extends the bandwidth and speed for applications such as very low drift sample and hold amplifiers and photo-current detectors. Other applications include use in electrometer designs, pH/Ion sensitive electrodes, low current oxygen sensors, long term precision integrators and very high impedance buffer measurement designs.

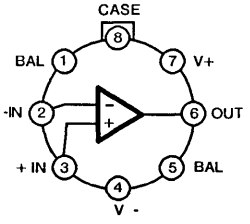
The HA-5180 is packaged in an 8 pin (TO-99) Metal Can and an 8 lead Mini-DIP and is pin compatible with most existing op amp configurations. The case of the TO-99 package is internally connected to pin 8 so that it may be connected to the same potential as the input. This feature helps minimize stray leakage to the case, helps shield the amplifier from external noise and reduces common mode input capacitance. For military grade product, refer to the HA-5180/883 data sheet.

Pinouts

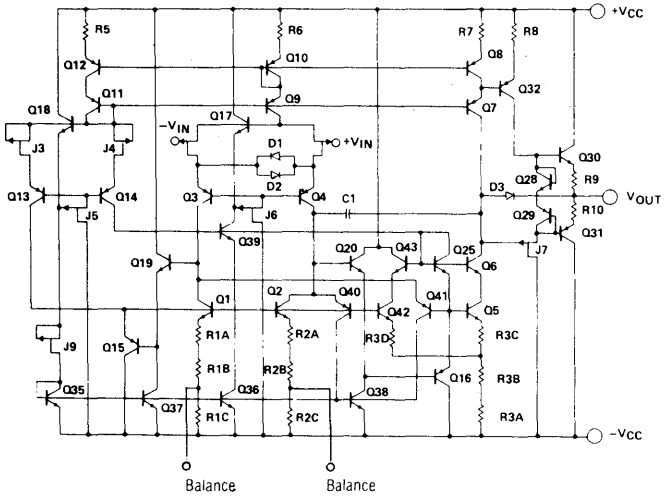
HA7-5180 (CERAMIC MINI-DIP)
TOP VIEW



HA2-5180 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Specified
Voltage Between V+ and V- Terminals 40V
Differential Input Voltage..... ±40V
Output Short Circuit Duration ..... Indefinite
Power Dissipation (Note 2)..... 300mW

Operating Temperature Ranges

HA-5180-2.....$-55°C \leq T_A \leq +125°C$
HA-5180-5..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range .....$-65°C \leq T_A \leq +150°C$

Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified.

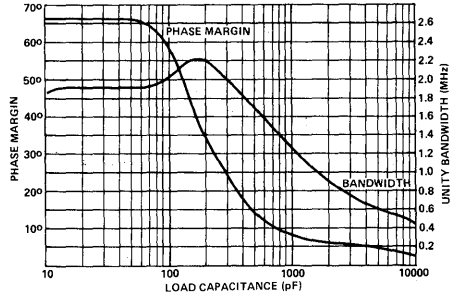
PARAMETER	TEMP	HA-5180-2 -55°C to +125°C			HA-5180-5 0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	1	3	-	1	3	mV
	Full	-	-	4	-	-	4	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	µV/°C
Bias Current (Note 3)	+25°C	-	250	1000	-	250	1000	fA
	Full	-	100	500	-	6	30	pA
Offset Current (Note 3)	+25°C	-	30	200	-	30	200	fA
	Full	-	6	30	-	1	5	pA
Common Mode Range	Full	±10	±12	-	±10	±12	-	V
Differential Input Resistance	+25°C	-	10^{12}	-	-	10^{12}	-	Ω
Input Capacitance	+25°C	-	5	-	-	5	-	pF
Input Noise Voltage, 0.1Hz to 10Hz	+25°C	-	5	-	-	5	-	μV_{p-p}
Input Noise Voltage Density								
f_O = 10Hz	+25°C	-	200	-	-	200	-	$nV/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	120	-	-	120	-	$nV/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	70	-	-	70	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C	-	0.01	-	-	0.01	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 4)	+25°C	200K	1M	-	200K	1M	-	V/V
	Full	150K	-	-	150K	-	-	V/V
Common Mode Rejection Ratio (Note 5)	Full	90	110	-	90	110	-	dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	-	2	-	-	2	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12	-	±10	±12	-	V
	Full	±10	-	-	±10	-	-	V
Full Power Bandwidth (Note 7)	+25°C	-	110	-	-	110	-	kHz
Output Current (Note 8)	+25°C	±10	±15	-	±10	±15	-	mA
Output Resistance (Note 9)	+25°C	-	25	-	-	25	-	Ω
TRANSIENT RESPONSE								
Overshoot	+25°C	-	30	50	-	30	50	%
Rise Time	+25°C	-	75	-	-	75	-	ns
Slew Rate	+25°C	4	7	-	4	7	-	V/µs
Settling Time (Note 10)	+25°C	-	2	-	-	2	-	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	0.7	1	-	0.8	1	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105	-	85	105	-	dB

NOTES:

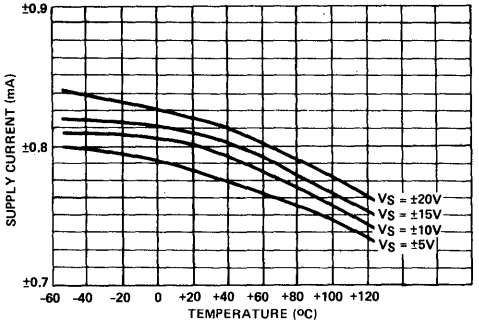
1. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Derate at 6.9 mW/°C for operation at ambient temperatures above +75°C.
3. This parameter is guaranteed by design and is not 100% tested.
4. V_{OUT} = ±10V; R_L = 2K. Gain dB = 20 $\log_{10} A_V$.
5. ΔV_{CM} = ±10V D.C.
6. R_L = 2K.
7. R_L = 2K, V_{PEAK} = 10V; Full power bandwidth guaranteed based on slew rate measurement using FPBW = $\frac{\text{Slew Rate}}{2\pi V_{Peak}}$
8. V_{OUT} = ±10V.
9. Output resistance specified under open loop conditions (f = 100Hz).
10. Settling time is speified to 0.1% of final value for a 10V output step and A_V = -1.
11. ΔV_{SUPPLY} = ±10V D.C. to ±20V D.C.

Typical Performance Curves

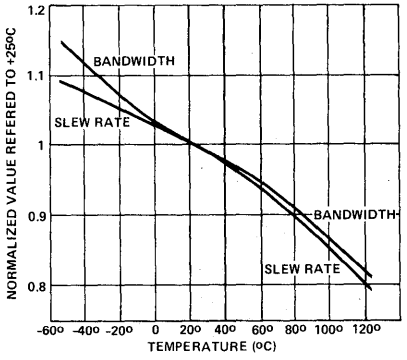
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



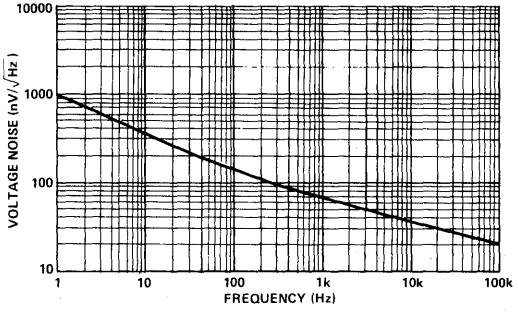
SUPPLY CURRENT vs. TEMPERATURE



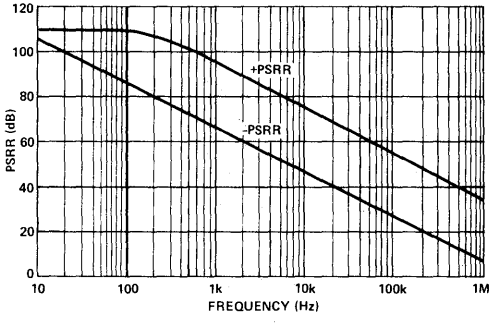
NORMALIZED AC PARAMETERS vs. TEMPERATURE



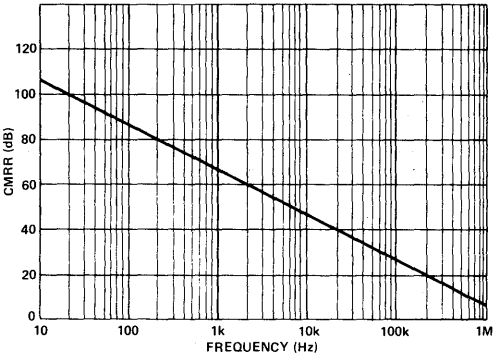
INPUT VOLTAGE NOISE vs. FREQUENCY



PSRR vs. FREQUENCY

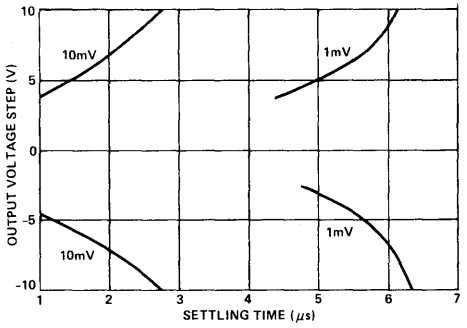


CMRR vs. FREQUENCY

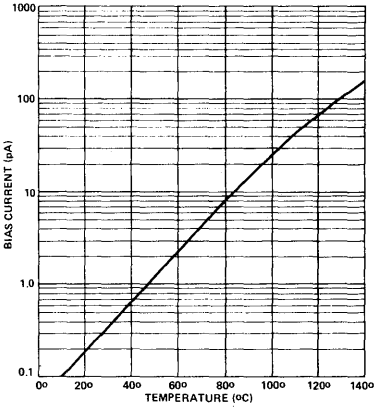


Typical Performance Curves (Continued)

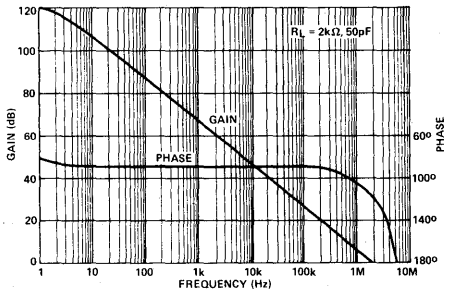
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



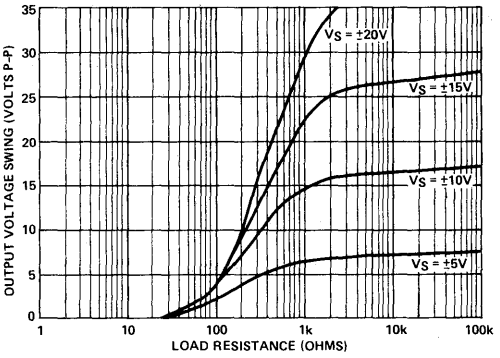
BIAS CURRENT vs. TEMPERATURE



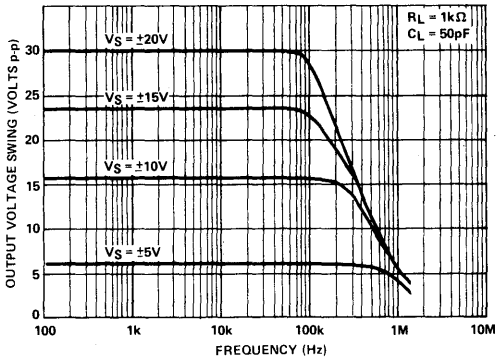
OPEN LOOP FREQUENCY RESPONSE



OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



OUTPUT VOLTAGE SWING vs. FREQUENCY



Typical Applications

The HA-5180 offers one of the lowest input bias currents of any monolithic operational amplifier and is ideal for use in applications for measuring signals from very high impedance or very low current sources. To fully utilize the capabilities of the HA-5180, care should be taken to minimize noise pickup and current leakage paths with the use of shielding and guarding techniques and by placing the device as close as possible to the signal source. The small size and low quiesent current (possible battery operation) of the HA-5180 allows easy installation at the signal source or inside a probe. The HA-5180 is internally compensated and is capable of driving long signal cables which have several hundred pF capacitive loading.

If it is not possible to place the HA-5180 very close to the signal source, then the use of shielded coaxial cable will offer the best isolation of the high impedance signal line from external noise sources. However, the effects of leakage, capacitance and vibrational noise should be taken into account when using coaxial cables. Leakage can be minimized by using cables with very high insulation resistance (such as polyethylene or Virgin Teflon). For example, the current to voltage converter circuit (as shown in Figure 1) will eliminate leakage across the insulation of the cable by forcing the signal line to the same potential as the shield. This circuit also provides fast response to input signals because the cable capacitance is never forced to be charged or discharged. However, the cable capacitance directly increases the input capacitance of the circuit and could cause the circuit to become unstable; if so, adding capacitance across Rf will stabilize the circuit again. Leakage can also be reduced in the high-impedance non-inverting configuration (see Figure 2) by bootstrapping the shield to the same potential as the signal source instead of ground. If low closed-loop gains are used, the non-inverting configuration could also become unstable due to the positive feedback to the input through the cable capacitance. One method of compensating this circuit is to place a small (low leakage) capacitor from the input to ground. This technique will also reduce the effective capacitance presented to the signal source. When large closed-loop gains and/or long cable lengths are used, a buffer should be added to the circuit to drive the shield.

When using coaxial cable with the HA-5180 the cable should be kept as rigid and vibration free as possible. Frictional movement of the shield over the insulation can generate electrical charge which is picked up by the high impedance signal line as noise. Movement and bending of the cable can also cause charge movement due to small changes in cable capacitance and capacitance to surrounding objects. Another source of noise currents is that which is generated by the movement of a conductor in a magnetic field.

For lowest leakage at the device inputs either use a teflon IC socket or connect the signal line to the HA-5180 inputs using teflon standoffs. A guard ring, as shown in Figure 3, applied to both sides of the pc board and bootstrapped to the same potential as the input signal will minimize leakage paths across the pc board. Pin 8 of the TO-99 can, which is internally tied to the case, should also be tied to the bootstrap potential to help minimize noise pickup and leakage currents across the package insulation. This technique will also reduce common mode input capacitance.

Cleanliness of circuit boards and components is also important for achieving low leakage currents. Printed circuit boards and components should be thoroughly cleaned by using a low residue solvent such as TMC Freon , rinsed by deionized water and dried with nitrogen. The circuit board should be protected from high contamination and high humidity environments. A good quality conformal coating with low dielectric absorption provides the best protection from humidity and contamination.

Input protection is generally not necessary when designing with the HA-5180. Many electrometer type devices, especially CMOS, require elaborate zener protection schemes which may compromise overall performance. The Harris dielectric isolation process and JFET input design enables the HA-5180 to withstand input signals several volts beyond either supply and large differential signals equal to the rail-to-rail supply voltage without damage or degradation of performance.

For more information see Application Note 555.

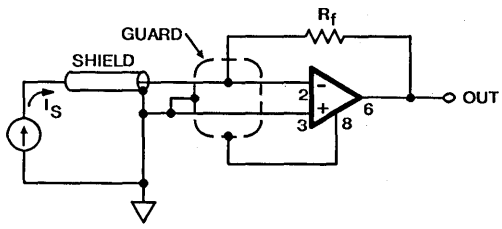


FIGURE 1. CURRENT TO VOLTAGE CONVERTER

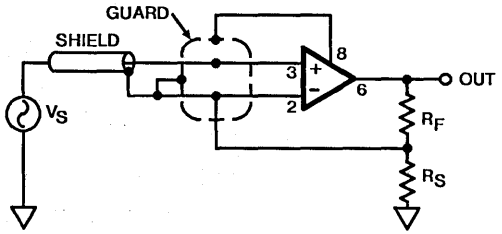


FIGURE 2. VERY HIGH IMPEDANCE NON-INVERTING AMPLIFIER

Typical Applications (Continued)

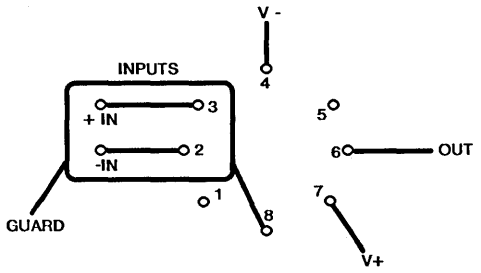


FIGURE 3. GUARD RING EXAMPLE

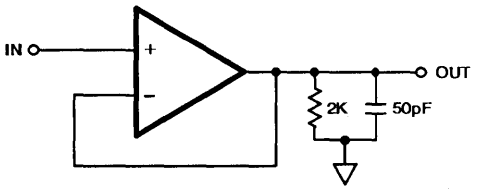


FIGURE 4. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT

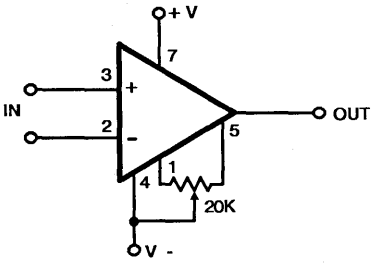
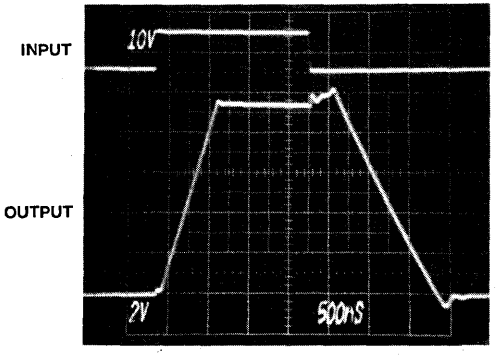
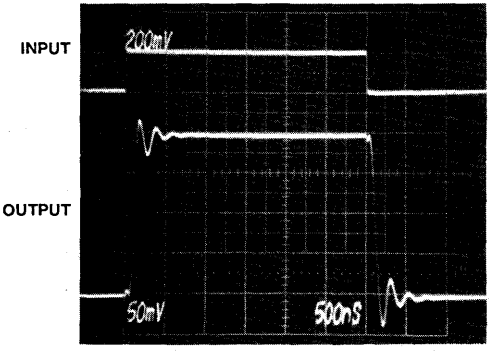


FIGURE 5. SUGGESTED OFFSET ADJUSTMENT CIRCUIT

LARGE SIGNAL RESPONSE
Vertical Scale (Volts: 5V/Div. Input)
(Volts: 2V/Div. Output)
Horizontal Scale (Time: 500ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale (Volts: 100mV/Div. Input)
(Volts: 50mV/Div. Output)
Horizontal Scale (Time: 500ns/Div.)



HARRIS HA-5190/95

May 1990

Wideband, Fast Settling Operational Amplifier

Features

- Fast Settling Time (0.1%) 70ns
- Very High Slew Rate 200V/μs
- Wide Gain-Bandwidth ($A_V \geq 5$) 150MHz
- Power Bandwidth 6.5MHz
- Low Offset Voltage 3mV
- Input Noise Voltage ..... 6nV/$\sqrt{Hz}$
- Monolithic Bipolar D.I. Construction

Applications

- Fast, Precise D/A Converters
- High Speed Sample-Hold Circuits
- Pulse and Video Amplifiers
- WideBand Amplifiers
- Replace Costly Hybrids

Description

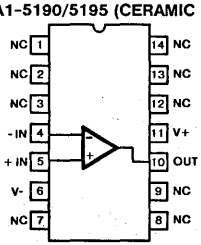
HA-5190/5195 are monolithic operational amplifiers featuring an ultimate combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with Dielectric Isolation, these devices are capable of delivering an unparalleled 200V/μs slew rate with a settling time of 70ns (0.1%, 5V output step). These truly differential amplifiers are designed to operate at gains ≥ 5 without the need for external compensation. Other oustanding HA-5190/5195 features are 150MHz gain-bandwidth-product and 6.5MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 3mV offset voltage and 6.0nV/$\sqrt{Hz}$ input voltage noise at 1kHz.

With 200V/μs slew rate and 70ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. The 5190/5195 are also ideally suited for a variety of pulse and wideband video amplifiers. Please refer to Application Notes 525 and 526 for some of these application designs.

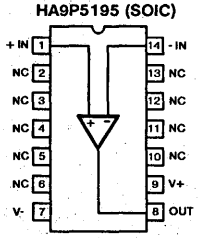
The HA-5190 is specified over the -55°C to +125°C range while the HA-5195 is specified from 0°C to +75°C. The HA-5190/5195 are available in 12 pin Metal Can (TO-8) and 14 pin Ceramic DIP packages. The HA-5195 is also available in SOIC packaging. At temperatures above +75°C a heat sink is required for the HA-5190 (see Note 2 and Application Note 556). For military versions, please request the HA-5190/883 data sheet.

Pinouts TOP VIEWS

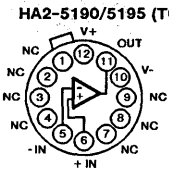
HA1-5190/5195 (CERAMIC DIP)



HA9P5195 (SOIC)

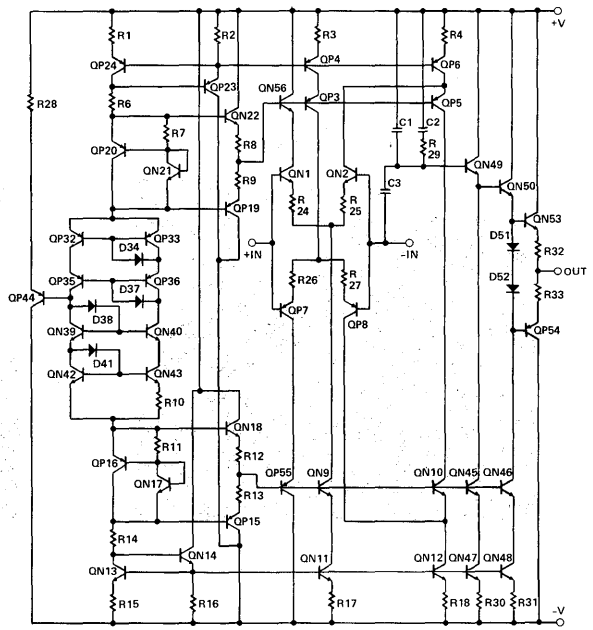


HA2-5190/5195 (TO-8 METAL CAN)



Case Tied To V-

Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage ..... ±6V
Output Current ..... 50mA (Peak)
Internal Power Dissipation (Note 2) ..... 870mW (Cerdip); 1W (TO-8) Free Air
Maximum Junction Temperature (Note 2) ..... +175°C

Operating Temperature Ranges

HA-5190-2 ..... $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-5195-5 ..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range ..... $-65^{\circ}C \leq T_A \leq +150^{\circ}C$

Electrical Specifications $V_{SUPPLY} = \pm 15V$; $R_L = 200\Omega$, Unless Otherwise Specified.

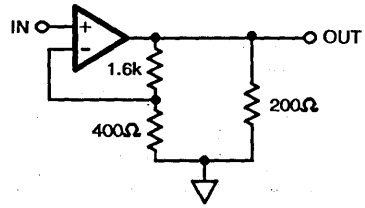
PARAMETER	TEMP	HA-5190-2 MIN	HA-5190-2 TYP	HA-5190-2 MAX	HA-5195-5 MIN	HA-5195-5 TYP	HA-5195-5 MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	3	5	-	3	6	mV
	Full	-	-	10	-	-	10	mV
Average Offset Voltage Drift	Full	-	20	-	-	20	-	µV/°C
Bias Current	+25°C	-	5	15	-	5	15	µA
	Full	-	-	20	-	-	20	µA
Offset Current	+25°C	-	1	4	-	1	4	µA
	Full	-	-	6	-	-	6	µA
Input Resistance	+25°C	-	10	-	-	10	-	kΩ
Input Capacitance	+25°C	-	1	-	-	1	-	pF
Common Mode Range	Full	±5	-	-	±5	-	-	V
Input Noise Current (f = 1kHz, Rg = 0Ω)	+25°C	-	5	-	-	5	-	$pA/\sqrt{Hz}$
Input Noise Voltage (f = 1kHz, Rg = 0Ω)	+25°C	-	6	-	-	6	-	$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 3)	+25°C	15K	30K	-	10K	30K	-	V/V
	Full	5K	-	-	5K	-	-	V/V
Common Mode Rejection Ratio (Note 4)	Full	74	95	-	74	95	-	dB
Minimum Stable Gain	+25°C	5	-	-	5	-	-	V/V
Gain-Bandwidth-Product (Notes 5 & 6)	+25°C	-	150	-	-	150	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 3)	Full	±5	±8	-	±5	±8	-	V
Output Current (Note 3)	+25°C	±25	±30	-	±25	±30	-	mA
Output Resistance	+25°C	-	30	-	-	30	-	Ω
Full Power Bandwidth (Note 3 & 7)	+25°C	5	6.5	-	5	6.5	-	MHz
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C	-	13	18	-	13	18	ns
Overshoot	+25°C	-	8	-	-	8	-	%
Slew Rate	+25°C	160	200	-	160	200	-	V/µs
Settling Time:								
5V Step to 0.1%	+25°C	-	70	-	-	70	-	ns
5V Step to 0.01%	+25°C	-	100	-	-	100	-	ns
2.5V Step to 0.1%	+25°C	-	50	-	-	50	-	ns
2.5V Step to 0.01%	+25°C	-	80	-	-	80	-	ns
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	19	28	-	19	28	mA
Power Supply Rejection Ratio (Note 9)	Full	70	90	-	70	90	-	dB

NOTES:

1. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Recommended heat sinks: For TO-8 Metal Can, Thermalloy #2240A ($\theta_{SA} = 27^{\circ}C/W$) or #2268B ($\theta_{SA} = 24^{\circ}C/W$). For 14 pin Ceramic DIP: AAVID #5602B ($\theta_{SA} = 16^{\circ}C/W$). See Die Characteristics Section for θ_{ja}/θ_{jc} values.
3. $R_L = 200\Omega$, $C_L < 10pF$, $V_{OUT} = \pm 5V$.
4. $\Delta V_{CM} = \pm 5V$.
5. $V_{OUT} = 90mV$.
6. $A_V = 10$.
7. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$
8. Refer to Test Circuits section of data sheet.
9. $\Delta V_{SUPPLY} = \pm 10V$ D.C. to $\pm 20V$ D.C.

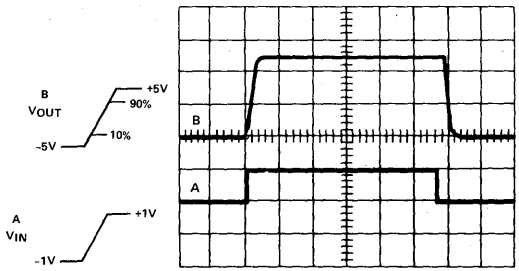
Test Circuits

LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT*

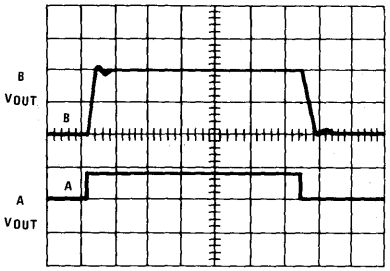


$A_V = 5$
* $C_L < 10pF$

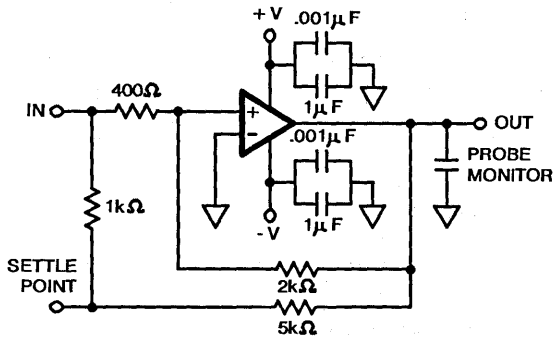
LARGE SIGNAL RESPONSE
Vertical Scale: (Volts: A = 2.0V/Div., B = 4.0/Div.)
Horizontal Scale: (Time: 100ns/Div.)



SMALL SIGNAL RESPONSE
Vertical Scale: (Volts: A = 50mV/Div., B = 100mV/Div.)
Horizontal Scale: (Time: 100ns/Div.)



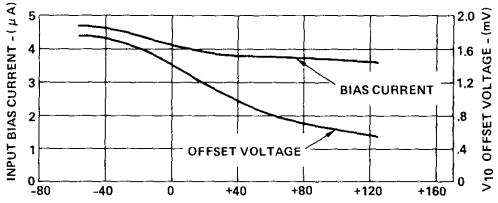
SETTLING TIME TEST CIRCUIT



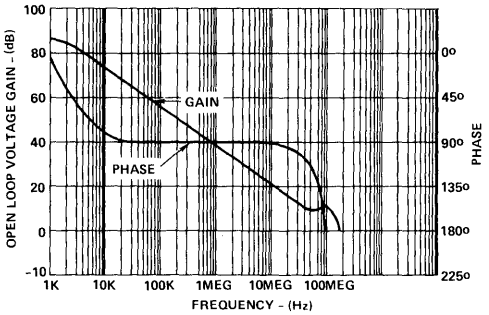
- $A_V = -5$
- Load Capacitance should be less than 10pF.
- It is recommended that resistors be carbon composition and that feedback and summing network ratios be matched to 0.1%.
- Settle Point (Summing Node) capacitance should be less than 10pF. For optimum settling time results, it is recommended that the test circuit be constructed directly onto the device pins. A Tektronix 568 Sampling Oscilloscope with S-3A sampling heads is recommended as a settle point monitor.

Typical Performance Curves V+ = +15V, V- = -15V, T_A = +25°C, Unless Otherwise Specified.

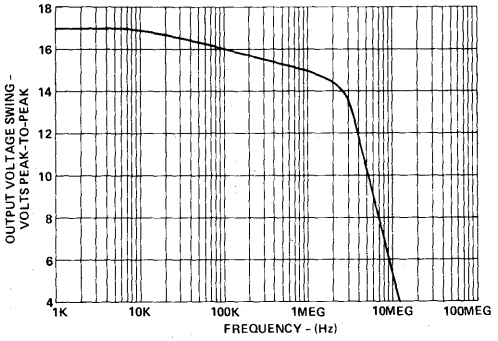
INPUT OFFSET VOLTAGE AND BIAS CURRENT vs. TEMPERATURE



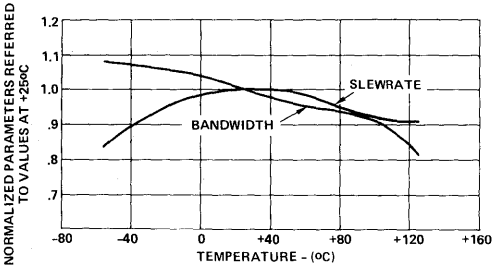
OPEN LOOP FREQUENCY RESPONSE



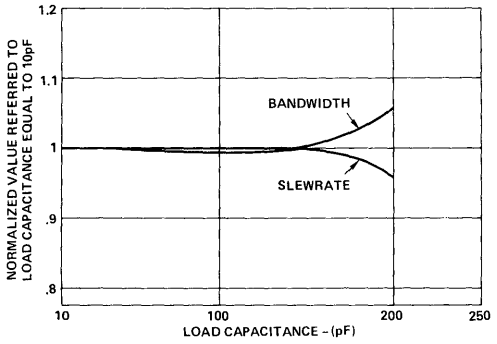
OUTPUT VOLTAGE SWING vs. FREQUENCY



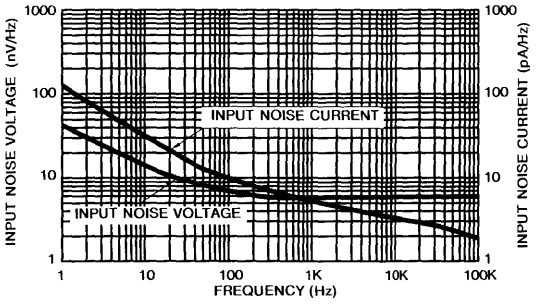
NORMALIZED AC PARAMETERS vs. TEMPERATURE



NORMALIZED AC PARAMETERS vs. LOAD CAPACITANCE

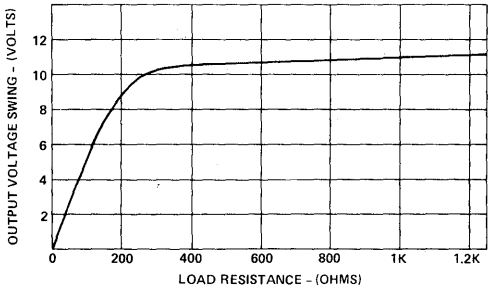


INPUT NOISE VOLTAGE AND NOISE CURRENT vs. FREQUENCY

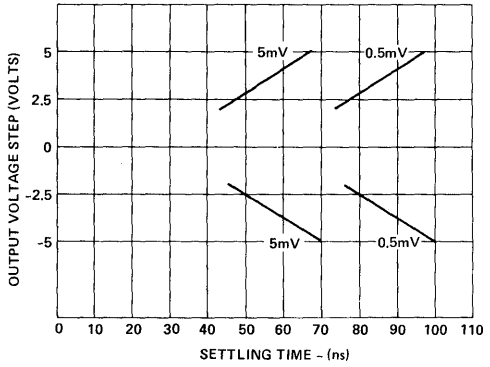


Typical Performance Curves (Continued)

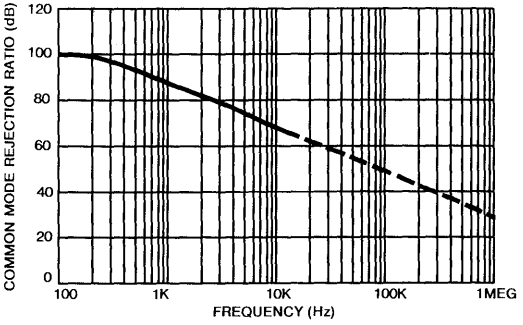
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



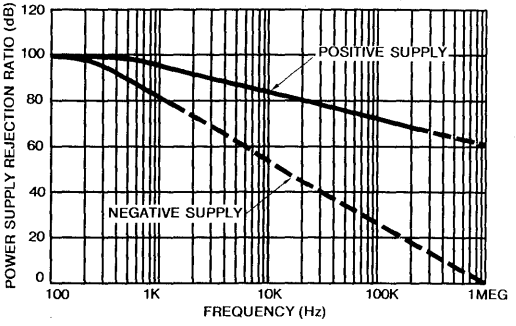
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



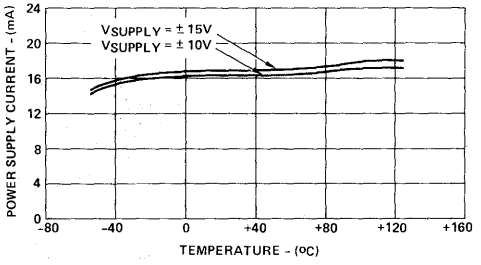
COMMON MODE REJECTION RATIO vs. FREQUENCY



POWER SUPPLY REJECTION RATIO vs. FREQUENCY



POWER SUPPLY CURRENT vs. TEMPERATURE

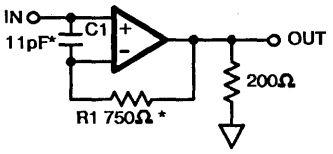


Applying the HA-5190/5195

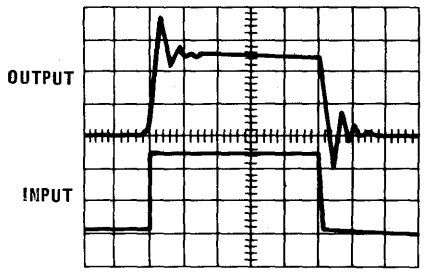
1. POWER SUPPLY DECOUPLING: Although not absolutely necessary, it is recommended that all power supply lines be decoupled with 0.01μF ceramic capacitors to ground. Decoupling capacitors should be located as near to the amplifier terminals as possible.
2. STABILITY CONSIDERATIONS: HA-5190/5195 is stable at gains > 5. Gains < 5 are covered elsewhere in this data sheet. Feedback resistors should be of carbon composition located as near to the input terminals as possible.
3. WIRING CONSIDERATIONS: Video pulse circuits should be built on a ground plane. Minimum point to point connections directly to the amplifier terminals should be used. When ground planes cannot be used, good single point grounding techniques should be applied.
4. OUTPUT SHORT CIRCUIT: HA-5190/5195 does not have output short circuit protection. Short circuits to ground can be tolerated for approximately 10 seconds. Short circuits to either supply will result in immediate destruction of the device.
5. HEAVY CAPACITIVE LOADS: When driving heavy capacitive loads (> 100pF) a small resistor (100Ω) should be connected in series with the output and inside the feedback loop.

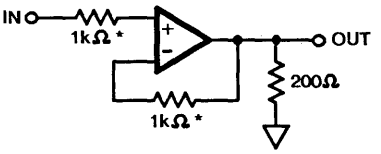
Typical Applications (Also see Application Notes 525 and 526)

SUGGESTED COMPENSATION FOR UNITY GAIN STABILITY: NONINVERTING

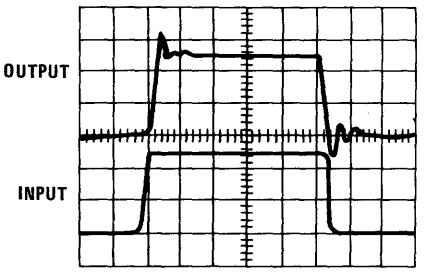


Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 100ns/Div.)



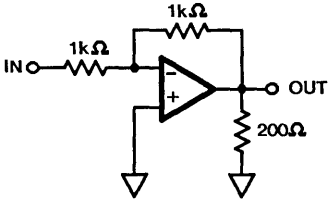


Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 100ns/Div.)

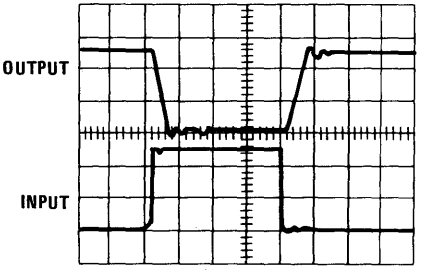


* Values were determined experimentally for optimum speed and settling time. R1 and C1 should be optimized for each particular application to ensure best overall frequency response.

INVERTING

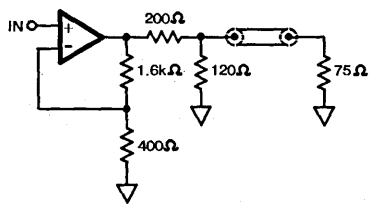


Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (50ns/Div.)

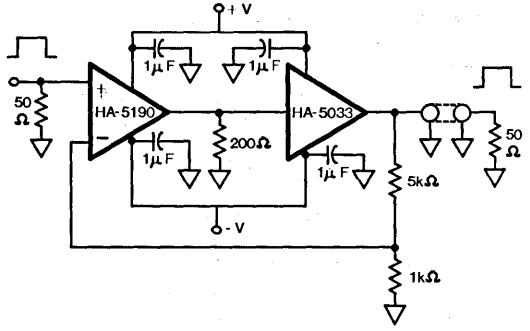


Typical Applications (Continued)

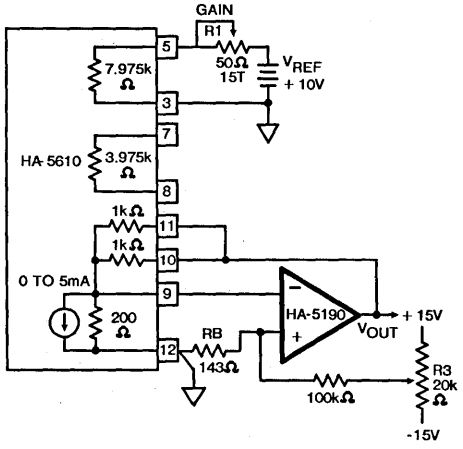
VIDEO PULSE AMPLIFIER/75Ω COAXIAL DRIVER



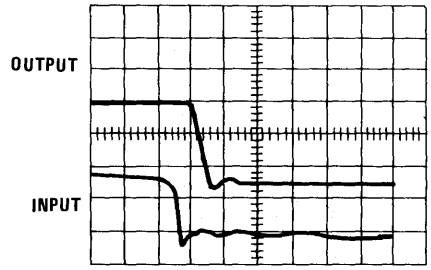
VIDEO PULSE AMPLIFIER COAXIAL LINE DRIVER



FAST DAC OUTPUT BUFFER



Vertical Scale: (Volts: 2V/Div.)
Horizontal Scale: (Time: 50ns/Div.)
B = V_{OUT} C = Digital Input



* Time delay between B and C represents total time delay for 0V to +5V full scale coded change.

Die Characteristics

Transistor Count 49
Die Dimensions ..... 0.087 x 0.052 x 0.019 inches (2210 x 1320 x 483 μm)
Substrate Potential (Powered Up)* ..... V-
Process ..... High Frequency Bipolar Dielectric Isolation
Passivation ..... Nitride

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	104	48
Metal Can	87	32

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS

HA-5221/22

Low Noise, Wideband Precision Operational Amplifier

July 1989

Features

- Gain Bandwidth Product 100MHz
- Unity Gain Bandwidth 35MHz
- High Slew Rate 25V/μs
- Low Offset Voltage 0.3mV
- High Open Loop Gain 128dB
- Channel Separation @ 10kHz 110dB
- Low Noise Voltage @ 1kHz ..... 3.4nV/$\sqrt{Hz}$
- High Output Current 56mA
- Low Supply Current per Amplifier 8mA

Applications

- Precision Test Systems
- Active Filtering
- Small Signal Video
- Accurate Signal Processing
- RF Signal Conditioning

Description

The HA-5221/5222 are single and dual high performance dielectrically isolated, monolithic op amps, featuring precision DC characteristics while providing excellent AC characteristics. Designed for audio, video, and other demanding applications, noise (3.4nV/$\sqrt{Hz}$ @ 1kHz), total harmonic distortion (<0.005%), and DC errors are kept to a minimum.

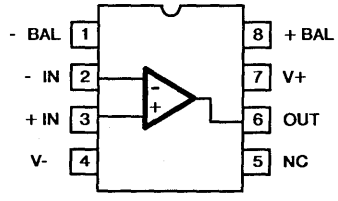
The precision performance is shown by low offset voltage (0.3mV), low bias currents (60nA), low offset currents (20nA), and high open loop gain (128dB). The combination of these excellent DC characteristics with the fast settling time (0.4μs) make the HA-5221/5222 ideally suited for precision signal conditioning.

The unique design of the HA-5221/5222 gives them outstanding AC characteristics not normally associated with precision op amps, high unity gain bandwidth (35MHz) and high slew rate (25V/μs). Other key specifications include high CMRR (95dB) and high PSRR (100dB). The combination of these specifications will allow the HA-5221/5222 to be used in RF signal conditioning as well as video amplifiers.

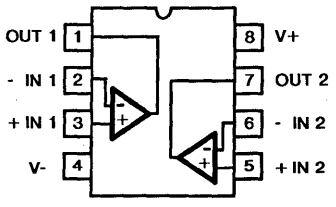
The performance of the HA-5221/5222-9 is guaranteed from -40°C to +85°C, while the HA-5221/5222-5 is guaranteed from 0°C to +75°C. The HA-5221 is available in 8 pin Ceramic Mini-DIP and 8 pin Metal Can (TO-99) and the HA-5222 is available in the 8 pin Ceramic Mini-DIP. For MIL-STD-883C compliant product and Ceramic LCC packaging, consult the HA-5221/5222/883C data sheet.

Pinouts

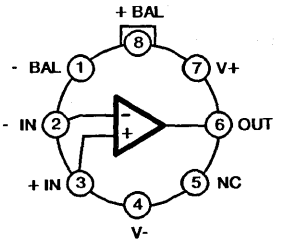
HA7-5221 (CERAMIC MINI-DIP)
TOP VIEW



HA7-5222 (CERAMIC MINI-DIP)
TOP VIEW



HA2-5221 (TO-99 METAL CAN)
TOP VIEW



3
OPERATIONAL AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage (Note 14) 5V
Output Current Short Circuit Duration ..... Indefinite

Operating Temperature Ranges

HA-5221/5222-9 ..... $-40^oC \leq T_A \leq +85^oC$
HA-5221/5222-5 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range ..... $-65^oC \leq T_A \leq +150^oC$
Maximum Junction Temperature ..... $+175^oC$

Electrical Specifications V+ = 15V, V- = -15V, Unless Otherwise Specified

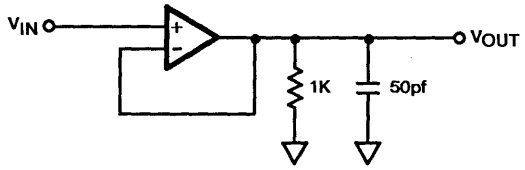
PARAMETER	TEMP	HA-5221-9 & HA-5222-9 MIN	HA-5221-9 & HA-5222-9 TYP	HA-5221-9 & HA-5222-9 MAX	HA-5221-5 & HA-5222-5 MIN	HA-5221-5 & HA-5222-5 TYP	HA-5221-5 & HA-5222-5 MAX	UNITS
INPUT CHARACTERISTICS								
Input Offset Voltage	+25°C	-	0.30	0.75	-	0.30	0.75	mV
	Full	-	0.35	1.5	-	0.35	1.5	mV
Average Offset Voltage Drift	Full	-	0.5	-	-	0.5	-	µV/°C
Input Bias Current	+25°C	-	40	80	-	40	100	nA
	Full	-	70	200	-	70	200	nA
Input Offset Current	+25°C	-	15	50	-	15	100	nA
	Full	-	30	150	-	30	150	nA
Input Offset Voltage Match	+25°C	-	400	750	-	400	750	µV
	Full	-	-	1500	-	-	1500	µV
Common Mode Range	+25°C	±12	-	-	±12	-	-	V
Differential Input Resistance	+25°C	-	70	-	-	70	-	kΩ
Input Noise Voltage f_o = 0.1Hz to 10Hz	+25°C	-	0.25	-	-	0.25	-	µVp-p
Input Noise Voltage f_o = 10Hz	+25°C	-	6.2	10	-	6.2	10	$nV/\sqrt{Hz}$
Density (Note 2, 15) f_o = 100Hz	+25°C	-	3.6	6	-	3.6	6	$nV/\sqrt{Hz}$
f_o = 1000Hz	+25°C	-	3.4	4.0	-	3.4	4.0	$nV/\sqrt{Hz}$
Input Noise Current f_o = 10Hz	+25°C	-	4.7	8.0	-	4.7	8.0	$pA/\sqrt{Hz}$
Density (Note 2, 15) f_o = 100Hz	+25°C	-	1.8	2.8	-	1.8	2.8	$pA/\sqrt{Hz}$
f_o = 1000Hz	+25°C	-	0.97	1.8	-	0.97	1.8	$pA/\sqrt{Hz}$
THD+N (Note 3)	+25°C	-	<0.005	-	-	<0.005	-	%
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 4)	+25°C	106	128	-	106	128	-	dB
	Full	100	120	-	100	120	-	dB
Common Mode Rejection Ratio (Note 5)	Full	86	95	-	86	95	-	dB
Unity Gain Bandwidth (-3dB)	+25°C	-	35	-	-	35	-	MHz
Gain Bandwidth Product (1kHz to 400kHz)	+25°C	-	100	-	-	100	-	MHz
Minimum Stable Gain	Full	1	-	-	1	-	-	V/V
OUTPUT CHARACTERISTICS								
Output Voltage Swing R_L = 333Ω	Full	±10	-	-	±10	-	-	V
R_L = 1K	+25°C	±12	±12.5	-	±12	±12.5	-	V
R_L = 1K	Full	±11.5	±12.1	-	±11.5	±12.1	-	V
Output Current (Note 6)	Full	±30	±56	-	±30	±56	-	mA
Output Resistance	+25°C	-	10	-	-	10	-	Ω
Full Power Bandwidth (Note 7)	+25°C	238	398	-	238	398	-	kHz
Channel Separation (Note 8)	+25°C	-	110	-	-	110	-	dB
TRANSIENT RESPONSE (Note 13)								
Slew Rate (Note 9, 15)	Full	15	25	-	15	25	-	V/µs
Rise Time (Note 10, 15)	Full	-	13	20	-	13	20	ns
Overshoot (Note 10, 15)	Full	-	28	50	-	28	50	%
Settling Time (Note 11) 0.1%	+25°C	-	0.4	-	-	0.4	-	µs
0.01%	+25°C	-	1.5	-	-	1.5	-	µs
POWER SUPPLY								
PSRR (Note 12)	Full	86	100	-	86	100	-	dB
Supply Current	Full	-	8	11	-	8	11	mA/Op Amp

NOTES:

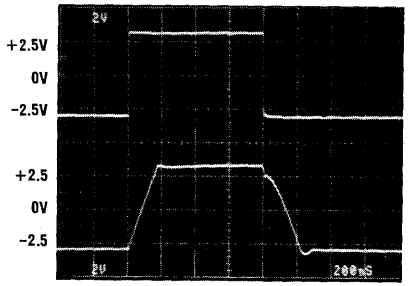
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Refer to typical performance curve in data sheet.
3. A_{VCL} = 10, f_o = 1kHz, V_O = 5Vrms, R_L = 600Ω, 10Hz to 100kHz, Minimum resolution of test equipment is 0.005%.
4. V_{OUT} = 0 to ±10V, R_L = 1K, C_L = 50pF.
5. V_{CM} = ±10V.
6. V_{OUT} = ±10V.
7. Full Power Bandwidth is calculated by: $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$, V_{PEAK} = 10V.
8. HA-5222 only, f_o = 10kHz, R_L = 1K, C_L = 50pF.
9. V_{OUT} = ±2.5V, R_L = 1K, C_L = 50pF.
10. V_{OUT} = ±100mV, R_L = 1K, C_L = 50pF.
11. Settling time is specified for a 10V step and A_V = -1.
12. V_S = ±10V to ±20V.
13. See Test Circuits.
14. Input is protected by back-to-back zener diodes. See applications section.
15. Guaranteed by characterization.

Test Circuits

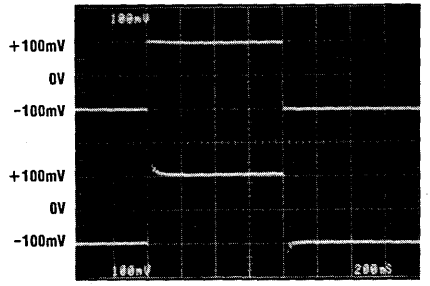
TRANSIENT RESPONSE TEST CIRCUIT



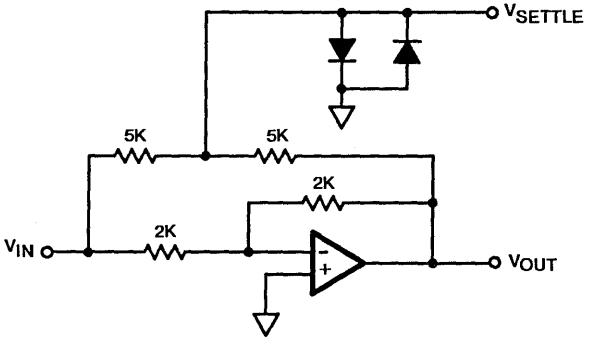
LARGE SIGNAL RESPONSE
V_{OUT} = ±2.5V
Vertical Scale: 2V/div Horizontal Scale: 200ns/div



SMALL SIGNAL RESPONSE
V_{OUT} = ±100mV
Vertical Scale: 100mV/div Horizontal Scale: 200ns/div



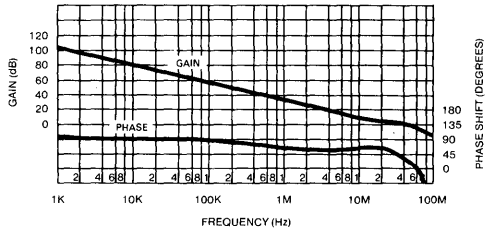
SETTLING TIME TEST CIRCUIT



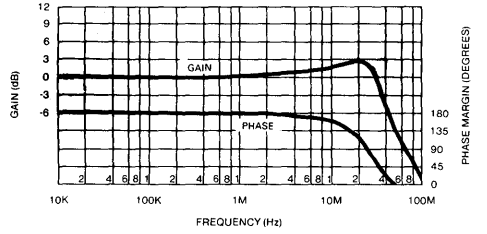
- A_V = -1
- Feedback and summing resistors must be matched (0.1%).
- HP5082-2810 clipping diodes recommended.
- Tektronix P6201 FET probe used at settling point.

Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$

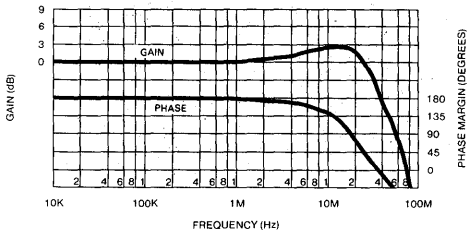
OPEN LOOP GAIN AND PHASE vs FREQUENCY
$R_L = 1K$, $C_L = 50pF$



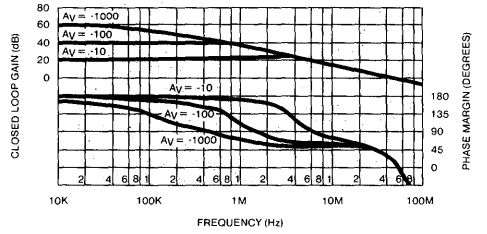
CLOSED LOOP GAIN vs FREQUENCY
$A_V = +1$, $R_L = 1K$, $C_L = 50pF$



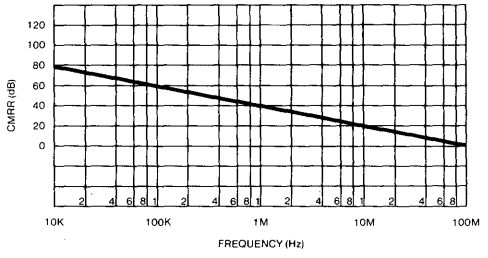
CLOSED LOOP GAIN vs FREQUENCY
$A_V = -1$, $R_L = 1K$, $C_L = 50pF$



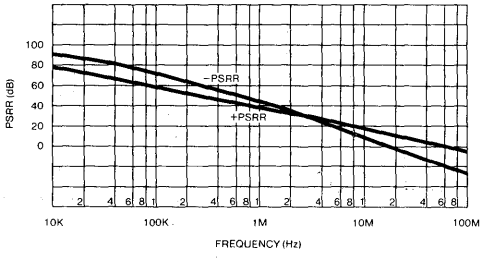
VARIOUS CLOSED LOOP GAINS vs FREQUENCY
$R_L = 1K$, $C_L = 50pF$



CMRR vs FREQUENCY
$A_V = +1$, $R_L = 1K$

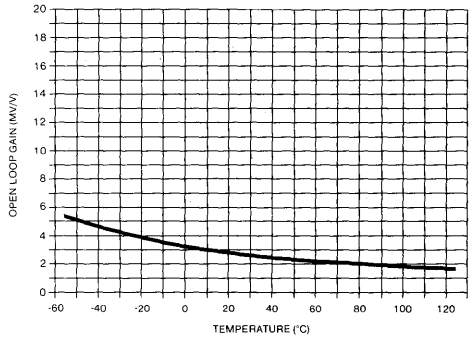


PSRR vs FREQUENCY
$A_V = +1$, $R_L = 1K$

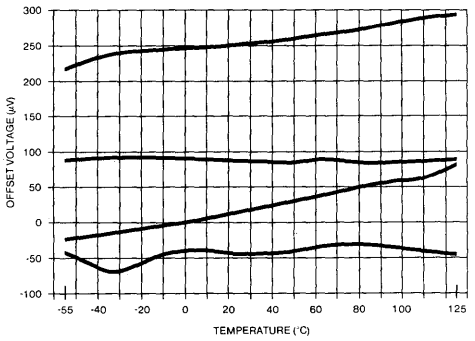


Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$

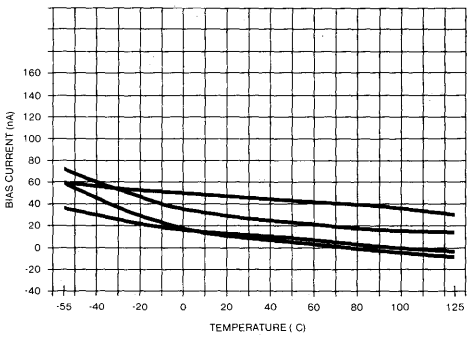
OPEN LOOP GAIN vs TEMPERATURE
$R_L = 1K$



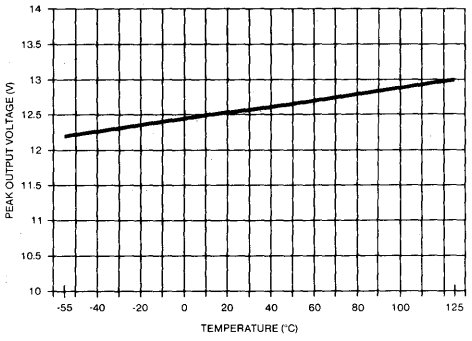
OFFSET VOLTAGE vs TEMPERATURE
4 Representative Units



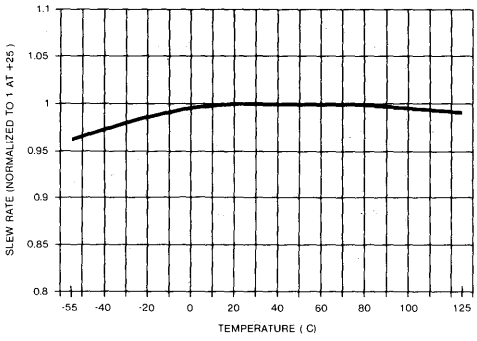
BIAS CURRENT TEMPERATURE
4 Representative Units



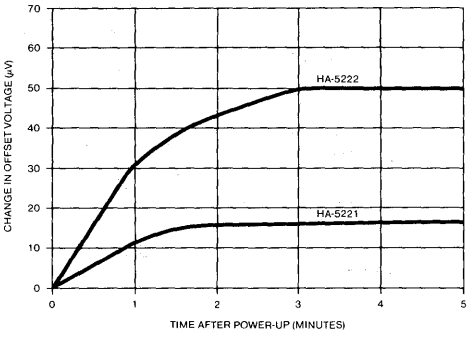
OUTPUT VOLTAGE SWING vs TEMPERATURE
$R_L = 600\Omega$



SLEW RATE vs TEMPERATURE
$A_V = +1$, $R_L = 1K$, $C_L = 50pF$

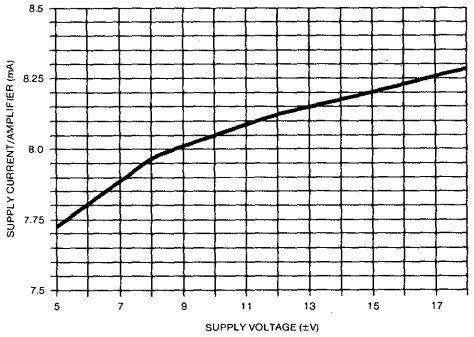


OFFSET VOLTAGE WARM-UP DRIFT
Ceramic DIP Packages

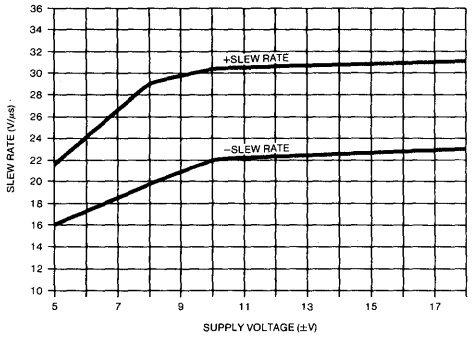


Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$

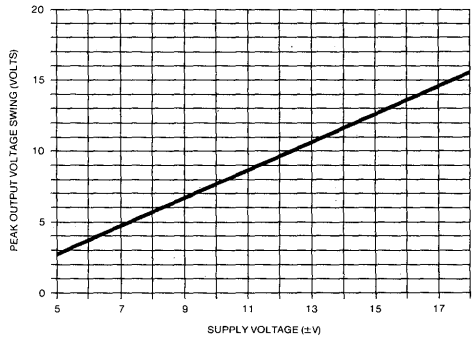
SUPPLY CURRENT vs SUPPLY VOLTAGE



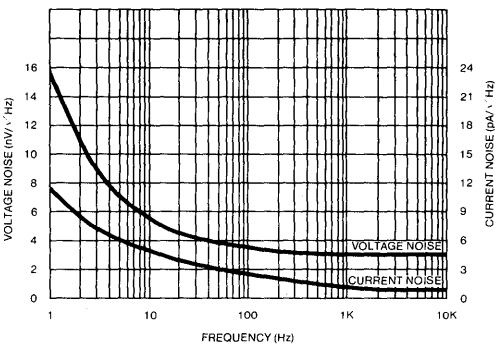
SLEW RATE vs SUPPLY VOLTAGE
$A_V = +1$, $R_L = 2K$, $C_L = 50pF$



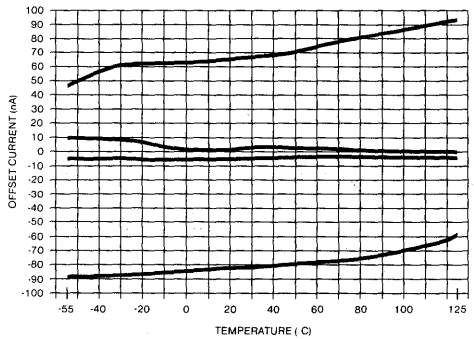
OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE
$R_L = 600\Omega$



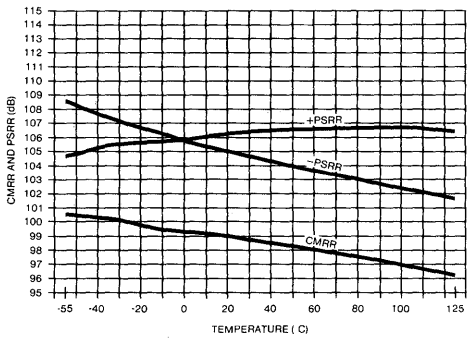
NOISE CHARACTERISTICS



OFFSET CURRENT vs TEMPERATURE
4 Representative Units

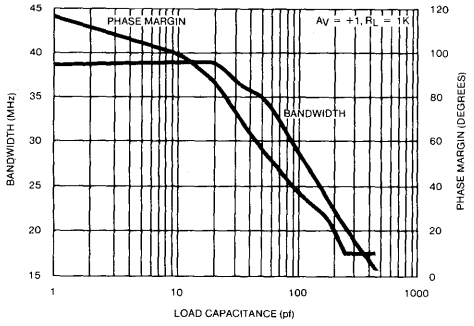


CMRR AND PSRR vs TEMPERATURE

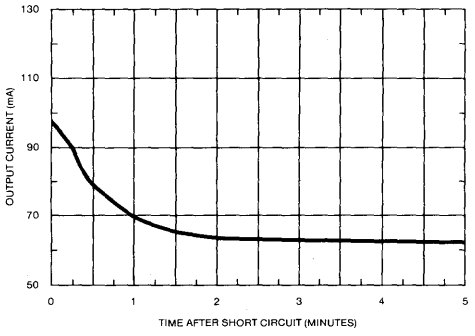


Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$

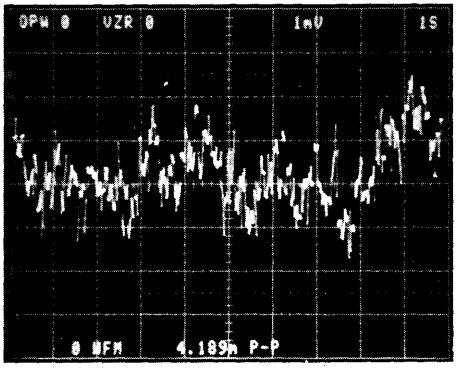
BANDWIDTH AND PHASE MARGIN vs LOAD CAPACITANCE



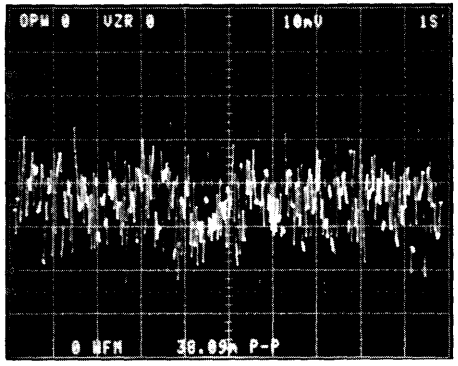
SHORT CIRCUIT OUTPUT CURRENT vs TIME



0.1Hz TO 10Hz NOISE
Vertical Scale: 1mV/div Horizontal Scale: 1 S/div
A_V = +25,000 (0.168μVp-p RTI)

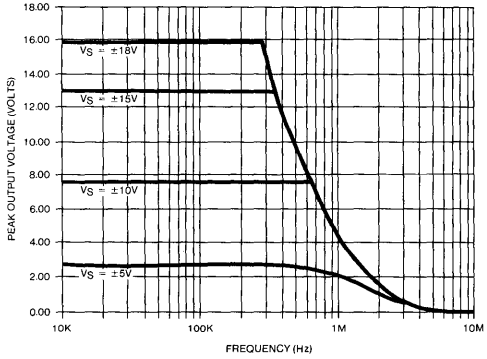


0.1Hz TO 1Hz 1MHz
Vertical Scale: 10mV/div Horizontal Scale: 1 S/div
A_V = +25,000 (1.5μVp-p RTI)

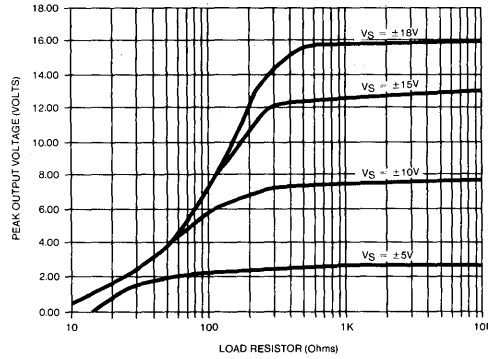


Typical Performance Curves $V_S = \pm 15V$, $T_A = 25^oC$

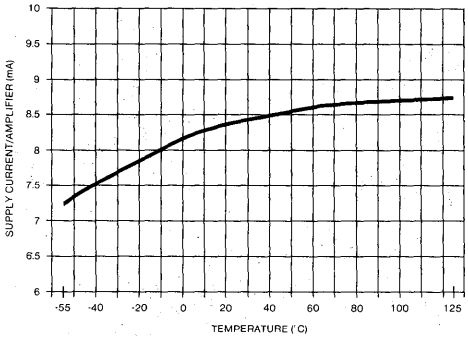
OUTPUT VOLTAGE SWING vs FREQUENCY
$A_V = +1$, $R_L = 1K$, $C_L = 15pF$, THD $\leq 0.01\%$



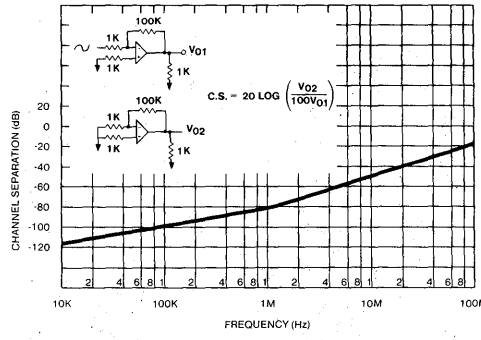
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE
$A_V = +1$, THD $\leq 0.01\%$, f = 1kHz



SUPPLY CURRENT/AMPLIFIER vs TEMPERATURE



CHANNEL SEPARATION vs FREQUENCY
(HA-5222 only)



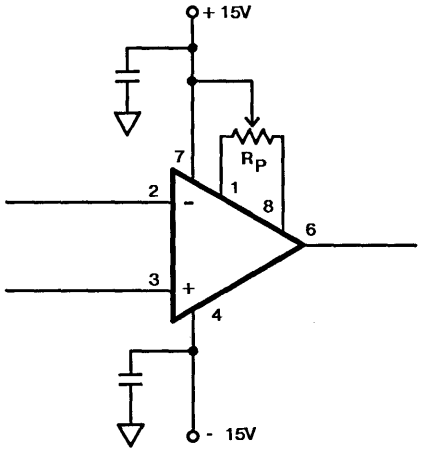
Applications Information

Operation at Various Supply Voltages

The HA-5221/5222 operates over a wide range of supply voltages with little variation in performance. The supplies may be varied from ±5 volts to ±15 volts. See typical performance curves for variations in supply current, slew rate and output voltage swing.

Offset Adjustment

The following diagram shows the offset voltage adjustment configuration for the HA-5221. By moving the potentiometer wiper towards pin 8 (+BAL), the op amps output voltage will increase; towards pin 1 (-BAL) decreases the output voltage.



A 20kΩ trim pot will allow an offset voltage adjustment of about 10mV.

Capacitive Loading Considerations

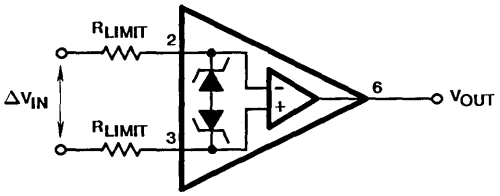
When driving capacitive loads >80pF, a small resistor, 50 to 100Ω, should be connected in series with the output and inside the feedback loop.

Saturation Recovery

When an op amp is over driven, output devices can saturate and sometimes take a long time to recover. By clamping the input, output saturation can be avoided. If output saturation can not be avoided, the maximum recovery time when overdriven into the positive rail is 10.6μs. When driven into the negative rail the maximum recovery time is 3.8μs.

Input Protection

The HA-5221/5222 has built in back-to-back protection diodes which limit the maximum allowable differential input voltage to approximately 5 volts. If the HA-5221/5222 will be used in circuits where the maximum differential voltage may be exceeded, then current limiting resistors must be used. The input current should be limited to a maximum of 10mA.



PC Board Layout Guidelines

When designing with the HA-5221 or the HA-5222, good high frequency (RF) techniques should be used when building a p.c. board. Use of ground plane is recommended. Power supply decoupling is very important. A 0.01μf to 0.1μf high quality ceramic capacitor at each power supply pin with a 2.2μf to 10μf tantalum close by will provide excellent decoupling. Chip capacitors produce the best results due to ease of placement next to the op amp and basically no lead inductance. If leaded capacitors are used, the leads should be kept as short as possible to minimize lead inductance.

Die Characteristics

Transistor Count
- HA-5221 64
- HA-5222 128

Die Dimensions
- HA-5221 ..... 94 x 72 x 19mils (2400 x 1840 x 480μm)
- HA-5222 ..... 185 x 78 x 19mils (4690 x 1980 x 480μm)

Substrate Potential* ..... V-

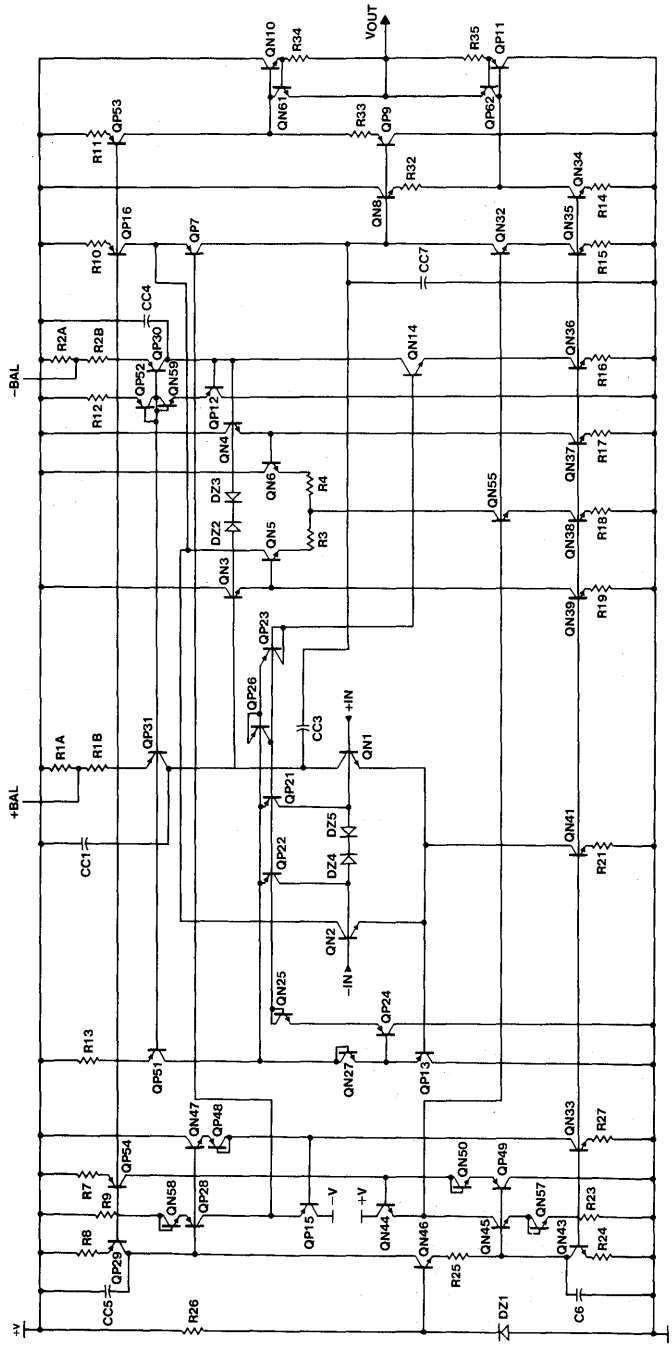
Process ..... High Frequency, Bipolar, DI

Passivation ..... Silox

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA2-5221	163	36
HA7-5221	152	76
HA7-5222	134	59

*The substrate may be left floating (Insulating Die Mount) or it may be on a conductor at V- potential.

Schematic (One Amplifier)



HARRIS

HFA-0001

Ultra High Slew Rate Operational Amplifier

May 1990

Features

- Unity Gain Bandwidth 350MHz
- Full Power Bandwidth 53MHz
- High Slew Rate 1000V/μs
- High Output Drive ..... ±50mA
- Monolithic Construction

Applications

- RF/IF Processors
- Video Amplifiers
- High Speed Cable Drivers
- Pulse Amplifiers
- High Speed Communications
- Fast Data Acquisition Systems

Description

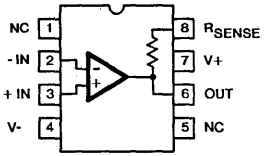
The HFA-0001 is an all bipolar op amp featuring high slew rate (1000V/μs), and high unity gain bandwidth (350MHz). These features combined with fast settling time (25ns) make this product very useful in high speed data acquisition systems as well as RF, video, and pulse amplifier designs.Other outstanding characteristics include low bias currents (15μA), low offset current (18μA), and low offset voltage (6mV).

The HFA-0001 offers high performance at low cost. It can replace hybrids and RF transistor amplifiers, simplifying designs while providing increased reliability due to monolithic construction. To enhance the ease of design, the HFA-0001 has a 50Ω ±20% resistor connected from the output of the op amp to a separate pin. This can be used when driving 50Ω strip line, microstrip, or coax cable.

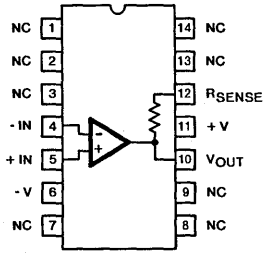
The performance of the HFA-0001-9 is guaranteed from -40°C to +85°C, while the HFA-0001-5 is guaranteed from 0°C to +75°C. The HFA-0001 is available in 8 pin SOIC, 8 pin Plastic Mini-Dip and 14 pin Sidebraze packages. For MIL-STD-883 compliant product and Ceramic LCC package consult the HFA-0001/883 datasheet.

Pinouts

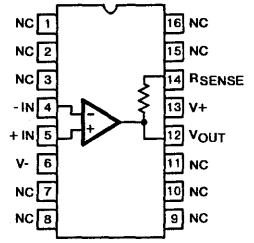
HFA3-0001-5 (PLASTIC MINI-DIP)
TOP VIEW



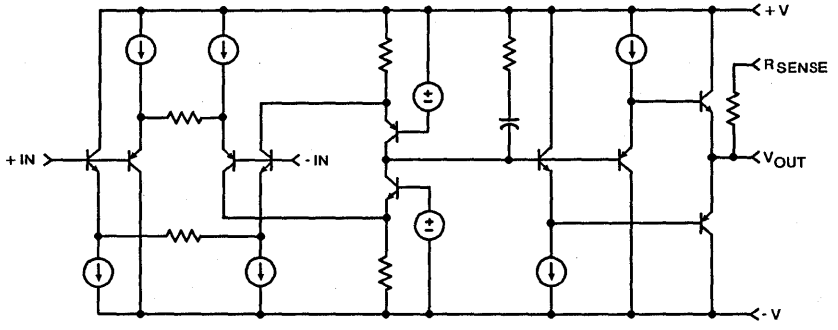
HFA1-0001-5/-9 (CERAMIC SIDEBRAZE DIP)
TOP VIEW



HFA9P0001-5/-9 (SOIC)
TOP VIEW



Simplified Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 12V
Differential Input Voltage 5V
Common Mode Input Voltage ..... ±4V
Output Current 60mA

Operating Temperature Range

HFA-0001-9 ..... $-40^{o}C \leq T_A \leq +85^{o}C$
HFA-0001-5 ..... $0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature ..... $-65^{o}C \leq T_A \leq +150^{o}C$
Maximum Junction Temperature ..... $+175^{o}C$

Electrical Specifications V+ = +5V, V- = -5V, Unless Otherwise Specified

PARAMETER		TEMP	HFA-0001-9 MIN	HFA-0001-9 TYP	HFA-0001-9 MAX	HFA-0001-5 MIN	HFA-0001-5 TYP	HFA-0001-5 MAX	UNITS
INPUT CHARACTERISTICS									
Offset Voltage		+25°C	-	6	15	-	6	30	mV
		High	-	4.5	20	-	4.5	30	mV
		Low	-	12.5	45	-	12.5	35	mV
Average Offset Voltage Drift		High	-	50	-	-	50	-	µV/°C
		Low	-	100	-	-	100	-	µV/°C
Bias Current		+25°C	-	15	50	-	15	100	µA
		Full	-	20	50	-	20	100	µA
Offset Current		+25°C	-	18	25	-	18	50	µA
		Full	-	22	50	-	22	50	µA
Common Mode Range		+25°C	±3	-	-	±3	-	-	V
Differential Input Resistance		+25°C	-	10	-	-	10	-	KΩ
Input Capacitance		+25°C	-	2	-	-	2	-	pF
Input Noise Voltage	0.1Hz to 10Hz	+25°C	-	3.5	-	-	3.5	-	µVrms
	10Hz to 1MHz	+25°C	-	6.7	-	-	6.7	-	µVrms
Input Noise Voltage	f_O = 10Hz	+25°C	-	640	-	-	640	-	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	-	170	-	-	170	-	$nV/\sqrt{Hz}$
	f_O = 1000Hz	+25°C	-	43	-	-	43	-	$nV/\sqrt{Hz}$
Input Noise Current	f_O = 10Hz	+25°C	-	2.35	-	-	2.35	-	$nA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	-	0.57	-	-	0.57	-	$nA/\sqrt{Hz}$
	f_O = 1000Hz	+25°C	-	0.16	-	-	0.16	-	$nA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain (Note 2)		+25°C	150	200	-	150	200	-	V/V
		High	150	170	-	100	170	-	V/V
		Low	150	220	-	150	220	-	V/V
Common Mode Rejection Ratio (Note 3)		+25°C	45	47	-	42	47	-	dB
		High	40	45	-	40	45	-	dB
		Low	45	48	-	42	48	-	dB
Unity Gain Bandwidth		+25°C	-	350	-	-	350	-	MHz
Minimum Stable Gain		Full	1	-	-	1	-	-	V/V
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 100Ω	+25°C	-	±3.5	-	-	±3.5	-	V
	R_L = 1k	+25°C	±3.5	±3.7	-	±3.5	±3.7	-	V
		High	±3.0	±3.6	-	±3.0	±3.6	-	V
		Low	±3.5	±3.7	-	±3.5	±3.7	-	V
Full Power Bandwidth (Note 5)		+25°C	-	53	-	-	53	-	MHz
Output Resistance, Open Loop		+25°C	-	3	-	-	3	-	Ω
Output Current		Full	±30	±50	-	±30	±50	-	mA

Electrical Specifications (Continued) V+ = +5V, V- = -5V, Unless Otherwise Specified

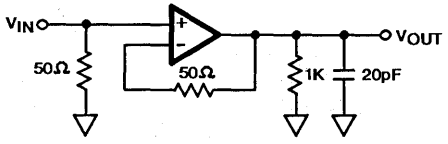
PARAMETER		TEMP	HFA-0001-9 MIN	HFA-0001-9 TYP	HFA-0001-9 MAX	HFA-0001-5 MIN	HFA-0001-5 TYP	HFA-0001-5 MAX	UNITS
TRANSIENT RESPONSE									
Rise Time (Note 4, 6)		+25°C	-	480	-	-	480	-	ps
Slew Rate (Note 4, 7)	R_L = 1K	+25°C	-	1000	-	-	1000	-	V/µs
	R_L = 100Ω	+25°C	-	875	-	-	875	-	V/µs
Settling Time (3V Step)	0.1%	+25°C	-	25	-	-	25	-	ns
Overshoot (Note 4, 6)		+25°C	-	36	-	-	36	-	%
POWER SUPPLY CHARACTERISTICS									
Supply Current		Full	-	65	75	-	65	75	mA
Power Supply Rejection Ratio (Note 8)		+25°C	40	42	-	37	42	-	dB
		High	35	41	-	35	41	-	dB
		Low	40	42	-	37	42	-	dB

NOTES:

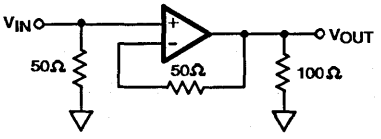
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = 0 to ±2V, R_L = 1K
3. ΔV_{CM} = ±2V
4. R_L = 100Ω
5. Full Power Bandwidth is calculated by equation:
$$FPB = \frac{\text{Slew Rate}}{2\pi\ V\text{peak}}, V\text{peak} = 3.0V$$
6. V_{OUT} = ±200mV, A_V = +1
7. V_{OUT} = ±3V, A_V = +1
8. ΔV_S = ±4V to ±6V

Test Circuits

LARGE SIGNAL RESPONSE TEST CIRCUIT



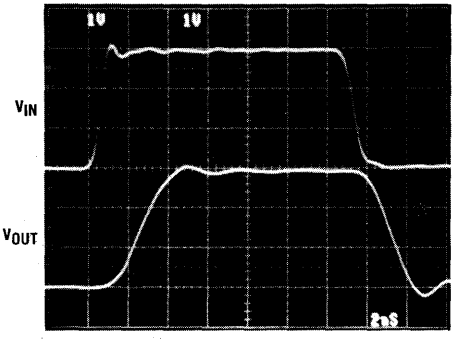
SMALL SIGNAL RESPONSE TEST CIRCUIT



LARGE SIGNAL RESPONSE

V_{OUT} = 0 to 3V

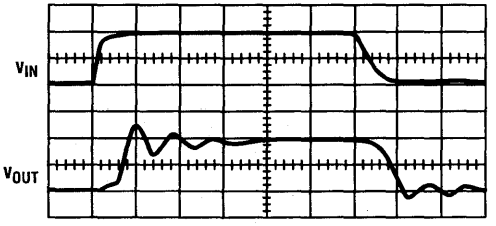
Vertical Scale: 1V/Div. Horizontal Scale: 2ns/Div.



SMALL SIGNAL RESPONSE

V_{OUT} = 0 to 200mV

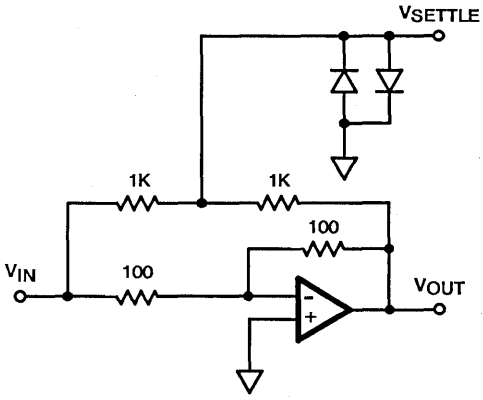
Vertical Scale: 100mV/Div. Horizontal Scale: 2ns/Div.



NOTE: Initial step in output is due to fixture feedthrough

Test Circuits (Continued)

SETTLING TIME SCHEMATIC

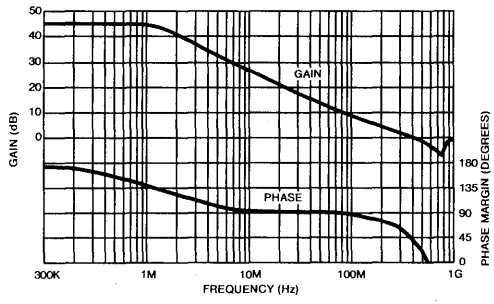


PROPAGATION DELAY
Vertical Scale: 500mV/Div. Horizontal Scale: 2ns/Div.
A_V = +1, R_L = 100Ω, V_{OUT} = 0 to 3V

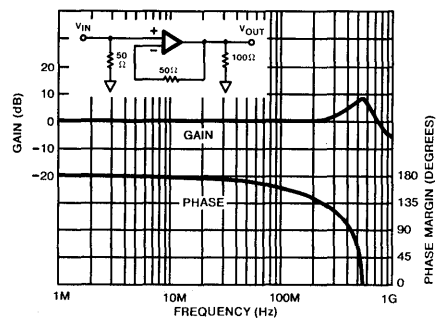
NOTE: Test Fixture delay of 450ps is included

Typical Performance Curves V_S = ±5V, T_A = +25°C, Unless Otherwise Specified

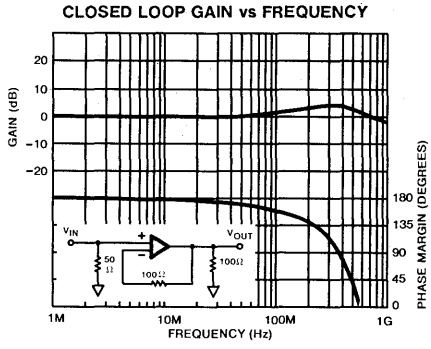
OPEN LOOP GAIN AND PHASE vs FREQUENCY
R_L = 100Ω



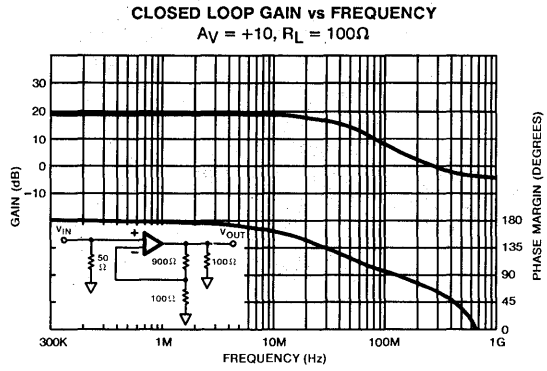
CLOSED LOOP GAIN vs FREQUENCY
A_V = +1, R_L = 100Ω, R_F = 50Ω



CLOSED LOOP GAIN vs FREQUENCY



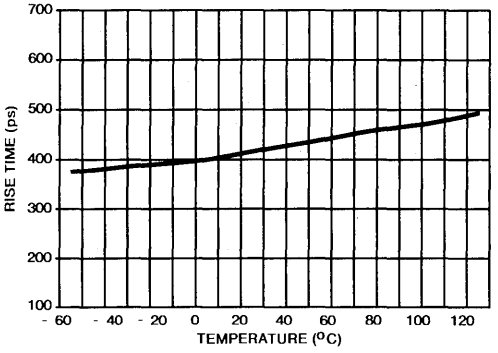
CLOSED LOOP GAIN vs FREQUENCY
A_V = +10, R_L = 100Ω



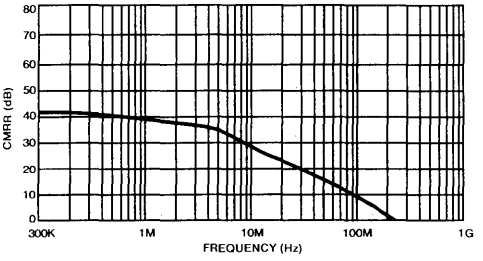
Typical Performance Curves (Continued) $V_S = \pm 5V$, $T_A = +25^oC$, Unless Otherwise Specified

RISE TIME vs TEMPERATURE

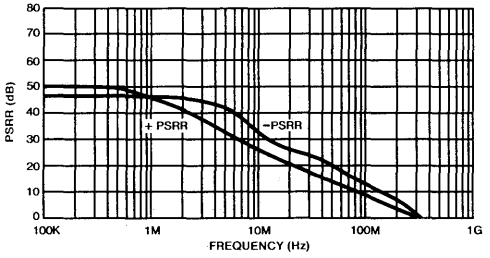
$A_V = +1$, $R_L = 100\Omega$, $V_{OUT} = 0$ to 200mV



CMRR vs FREQUENCY

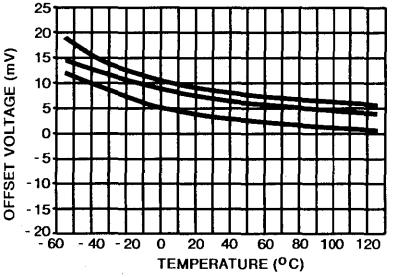


PSRR vs FREQUENCY



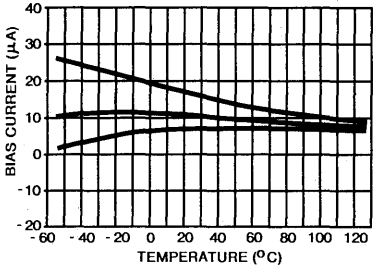
OFFSET VOLTAGE vs TEMPERATURE

3 Representative Units



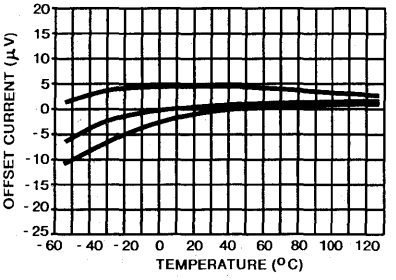
BIAS CURRENT vs TEMPERATURE

3 Representative Units



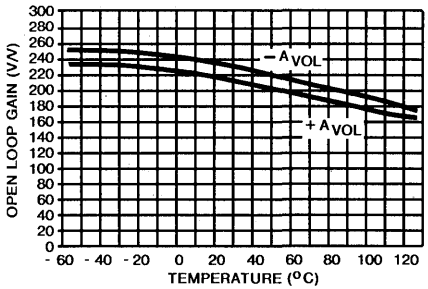
OFFSET CURRENT vs TEMPERATURE

3 Representative Units

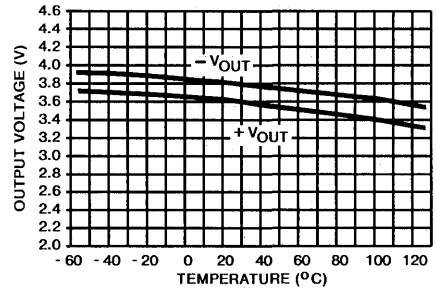


Typical Performance Curves (Continued) $V_S = \pm 5V$, $T_A = +25^oC$, Unless Otherwise Specified

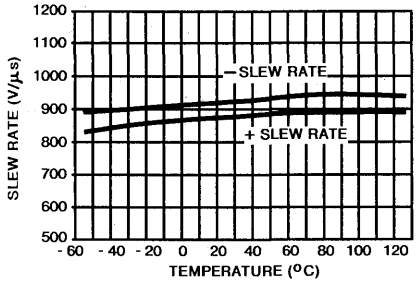
OPEN LOOP GAIN vs TEMPERATURE
R_L = 1K, V_{OUT} = 0 to ± 2V



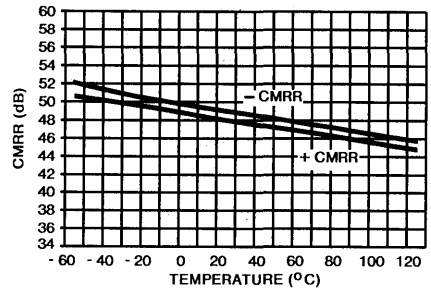
OUTPUT VOLTAGE SWING vs TEMPERATURE
R_L = 1K



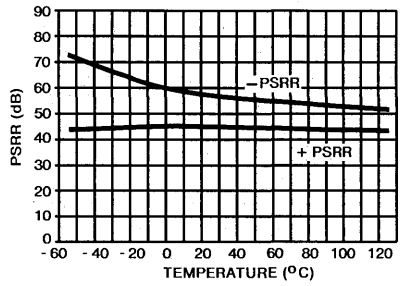
SLEW RATE vs TEMPERATURE
A_V = +1, R_L = 100, V_{OUT} = ± 3V



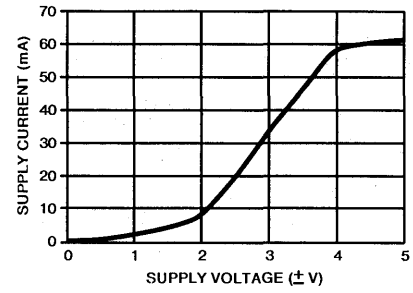
CMRR vs TEMPERATURE



PSRR vs TEMPERATURE
ΔV_S = ±4V to ±6V

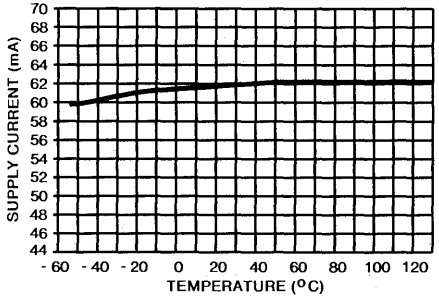


SUPPLY CURRENT vs SUPPLY VOLTAGE



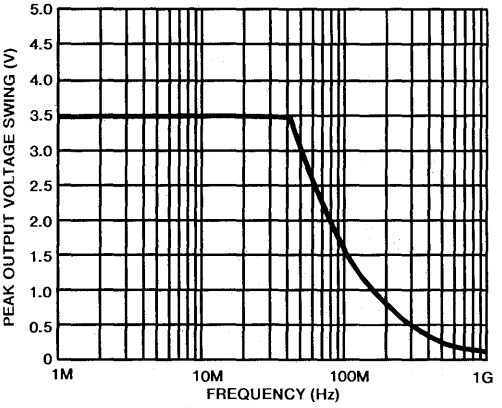
Typical Performance Curves (Continued) $V_S = \pm5V$, $T_A = +25^oC$, Unless Otherwise Specified

SUPPLY CURRENT vs TEMPERATURE



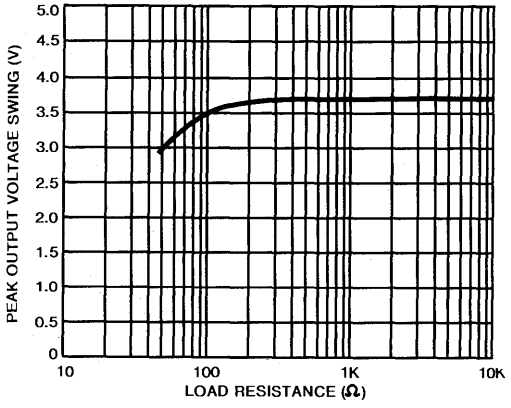
MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY

$A_V = +1$, $R_L = 100\Omega$, THD < 1%



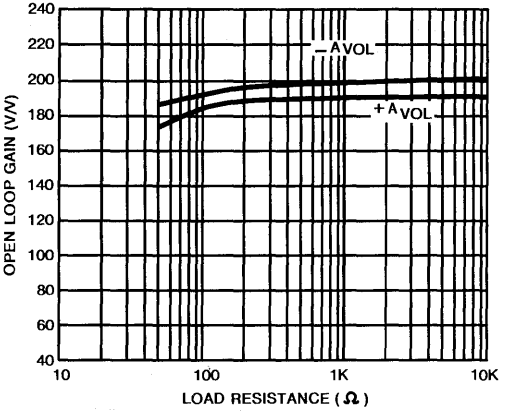
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

$A_V = +1$, $f_o = 50kHz$, THD < 1%

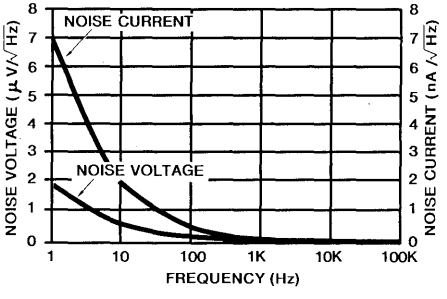


OPEN LOOP GAIN vs LOAD RESISTANCE

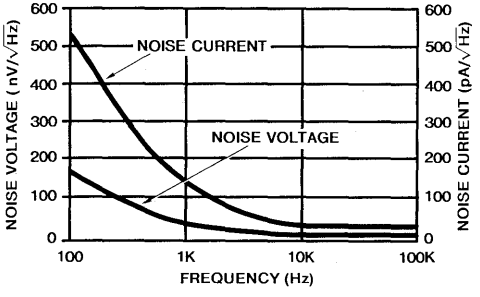
$V_{OUT} = \pm2V$



INPUT NOISE vs FREQUENCY



INPUT NOISE vs FREQUENCY

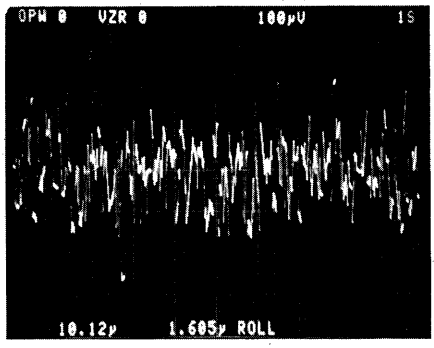


3

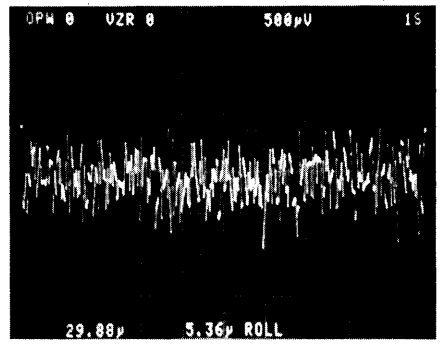
OPERATIONAL AMPLIFIERS

Typical Performance Curves (Continued) $V_S = \pm5V$, $T_A = +25^oC$, Unless Otherwise Specified

INPUT VOLTAGE NOISE
0.1Hz to 10Hz
$A_V = 50$, Noise Voltage = $1.605V_{rms}$ (RTI)
Noise Voltage = 10.12Vp-p



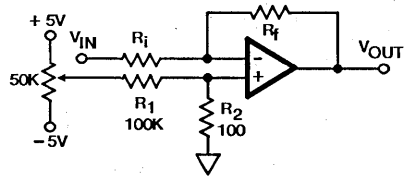
INPUT NOISE VOLTAGE
10Hz to 1MHz
$A_V = 50$, Noise Voltage = $5.36\mu V_{rms}$ (RTI)
Noise Voltage = 29.88µVp-p



Applications Information

Offset Adjustment

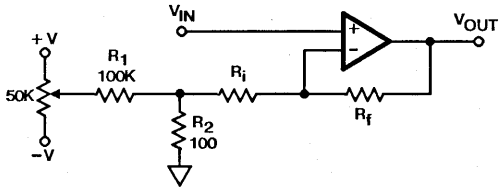
When applications require the offset voltage to be as low as possible, the figure below shows two possible schemes for adjusting offset voltage.



Adjustment Range $\simeq \pm V \left(\frac{R_2}{R_1}\right)$

FIGURE 1. INVERTING GAIN

For a voltage follower application, use the circuit in Figure 2 without R2 and with Ri shorted. R1 should be 1MΩ to 10MΩ. the adjustment resistors will cause only a very small gain error.



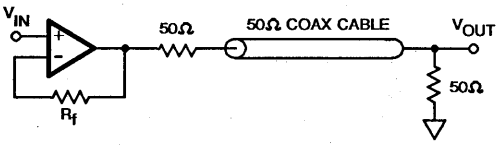
Adjustment Range $\simeq \pm V \left(\frac{R_2}{R_1}\right)$ Gain $\simeq 1 + \left(\frac{R_f}{R_i + R_2}\right)$

FIGURE 2. NON-INVERTING GAIN

PC Board Layout Guidelines

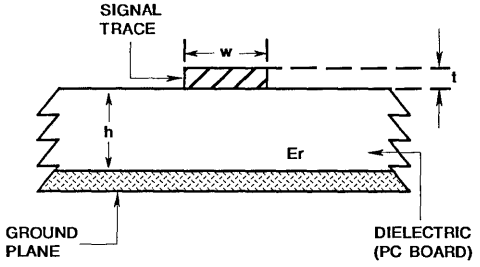
When designing with the HFA-0001, good high frequency (RF) techniques should be used when making a PC board. A massive ground plane should be used to maintain a low impedance ground. Proper shielding and use of short interconnection leads are also very important.

To achieve maximum high frequency performance, the use of low impedance transmission lines with impedance matching is recommended: 50Ω lines are common in communications and 75Ω lines in video systems. Impedance matching is important to minimize reflected energy therefore minimizing transmitted signal distortion. This is accomplished by using a series matching resistor (50Ω or 75Ω), matched transmission line (50Ω or 75Ω), and a matched terminating resistor, as shown in the figure below. Note that there will be a 6dB loss from input to output. The HFA-0001 has an integral 50Ω ±20% resistor connected to the op amps output with the other end of the resistor pinned out. This 50Ω resistor can be used as the series resistor instead of an external resistor.



Applications Information (Continued)

PC board traces can be made to look like a 50Ω or 75Ω transmission line, called microstrip. Microstrip is a PC board trace with a ground plane directly beneath, on the opposite side of the board, as shown below.



When manufacturing pc boards, the trace width can be calculated based on a number of variables. The following equation is reasonably accurate for calculating the proper trace width for a 50Ω transmission line.

$$Z_0 = \frac{87}{\sqrt{E_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \Omega$$

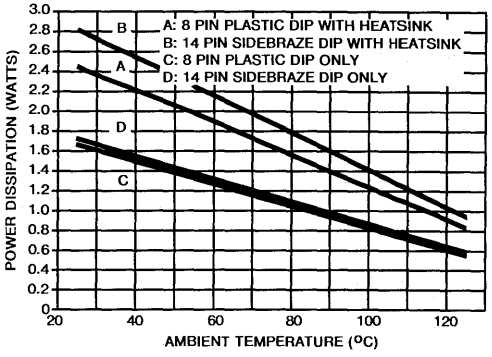
Power supply decoupling is essential for high frequency op amps. A 0.01µf high quality ceramic capacitor at each supply pin in parallel with a 1µf tantalum capacitor will provide excellent decoupling as shown in Figure 3. Chip capacitors produce the best results due to ease of placement next to the op amp and they have negligible lead inductance. If leaded capacitors are used, the leads should be kept as short as possible to minimize lead inductance. The figures below illustrate two different decoupling schemes. Figure 4 improves the PSRR because the resistor and capacitors create low pass filters. Note that the supply current will create a voltage drop across the resistor.

Saturation Recovery

When an op amp is over driven output devices can saturate and sometimes take a long time to recover. By clamping the input to safe levels, output saturation can be avoided. If output saturation cannot be avoided, the recovery time from 25% over-drive is 20ns and 30ns from 50% over-drive.

Thermal Management

The HFA-0001 can sink and source a large amount of current making it very useful in many applications. Care must be taken not to exceed the power handling capability of the part to insure proper performance and maintain high reliability. The following graph shows the maximum power handling capability of the HFA-0001 without exceeding the maximum allowable junction temperature of 175°C. The curves also show the improved power handling capability when heatsinks are used based on AVVID heatsink #5801B for the 8 pin Plastic DIP and IERC heatsink #PEP50AB for the 14 pin Sidebraze DIP. These curves are based on natural convection. Forced air will greatly improve the power dissipation capabilities of a heatsink.



Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HFA1-0001-5/-9	87	27
HFA3-0001-5	90	30

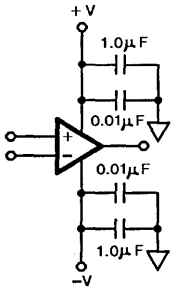


FIGURE 3. POWER SUPPLY DECOUPLING

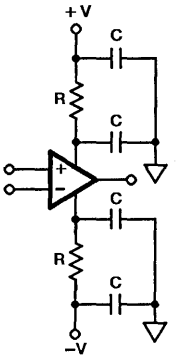


FIGURE 4. IMPROVED DECOUPLING/CURRENT LIMITING

HARRIS

HFA-0002

Low Noise Wideband Operational Amplifier

May 1990

Features

- Wide Gain Bandwidth Product 1GHz
- High Slew Rate 250V/μs
- High Open Loop Gain 105V/mV
- Low Offset Voltage 0.45mV
- Low Power Consumption 143mW
- Low Input Voltage Noise @ 1KHz ..... 2.7nV/$\sqrt{Hz}$
- Monolithic Construction

Applications

- RF/IF Processors
- Video Amplifiers
- Radar Systems
- Pulse Amplifiers
- High Speed Communications
- Fast Data Acquisition Systems

Description

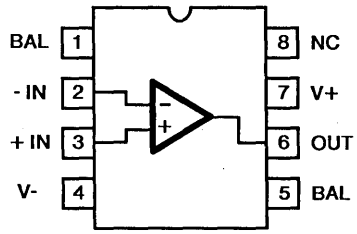
The HFA-0002 is a very wideband, high slew rate, op amp, featuring precision DC characteristics. Stable in gains of 10 or greater this all bipolar op amp offers a combination of AC and DC performance never seen before in monolithic form.

The high gain bandwidth product (1GHz) and high slew rate (250V/μs) make this op amp ideal for use in video and RF circuits. The low offset voltage (0.45mV), low bias current (0.23μA), and low voltage noise (2.7nV/$\sqrt{Hz}$) specifications combined with the excellent AC characteristics make this op amp ideal for high speed data acquisition systems with high accuracy.

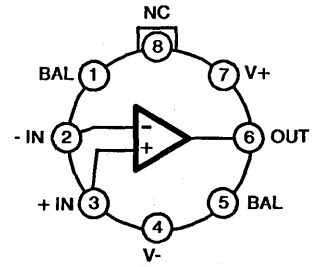
The HFA-0002-9 operates over the -40°C to +85°C temperature range, while the HFA-0002-5 operates over 0°C to +75°C. The HFA-0002 is available in 8 pin SOIC, 8 pin Ceramic Sidebraze DIP, 8 pin Plastic DIP, and 8 pin TO-99 Metal Can packages. For MIL-STD-883 compliant product and Ceramic LCC package consult the HFA-0002/883 datasheet.

Pinouts

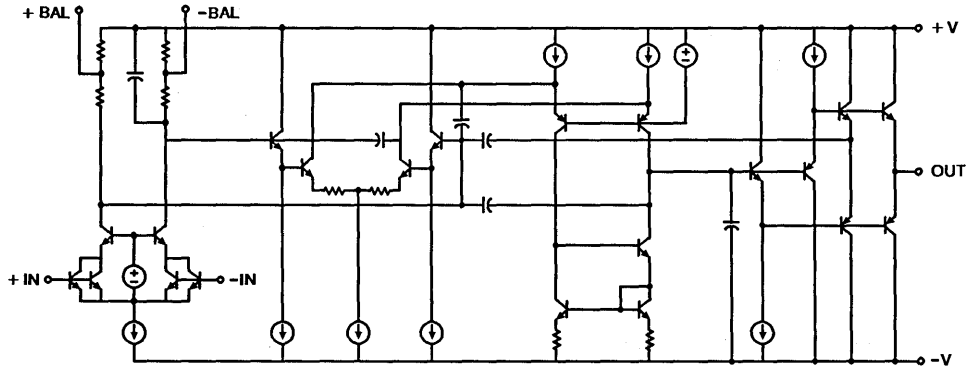
HFA9P0002-5/-9 (SOIC)
HFA7-0002-5/-9
(CERAMIC SIDEBRAZE DIP)
HFA3-0002-5/-9 (PLASTIC MINI-DIP)
TOP VIEW



HFA2-0002-5/-9 (TO-99 METAL CAN)
TOP VIEW



Simplified Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 12V
Differential Input Voltage..... 5V
Common Mode Input Voltage ..... ±5V
Output Current ..... ±20mA

Operating Temperature Range

HFA-0002-9..... $-40^{o}C \leq T_A \leq +85^{o}C$
HFA-0002-5..... $0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature..... $-65^{o}C \leq T_A \leq +150^{o}C$
Maximum Junction Temperature..... $+175^{o}C$

Electrical Specifications +V = +5V, -V = -5V, Unless Otherwise Specified

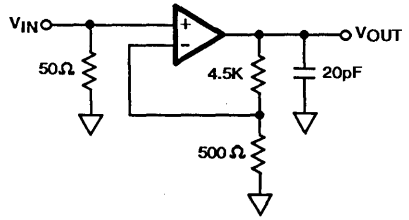
PARAMETER		TEMP	HFA-0002-5/-9 MIN	HFA-0002-5/-9 TYP	HFA-0002-5/-9 MAX	UNITS
INPUT CHARACTERISTICS						
Offset Voltage		+25°C	-	0.6	1	mV
		Full	-	1.2	2	mV
Average Offset Voltage Drift		Full	-	2.0	-	µV/°C
Bias Current		+25°C	-	0.23	1.0	µA
		High	-	0.1	1.0	µA
		Low	-	0.32	2.0	µA
Offset Current		+25°C	-	0.12	1.0	µA
		Full	-	0.16	1.0	µA
Common Mode Range		Full	±2.5	-	-	V
Differential Input Resistance		+25°C	-	1	-	MΩ
Input Capacitance		+25°C	-	2	-	pF
Input Noise Voltage	0.1Hz to 10Hz	+25°C	-	5.1	-	nVrms
	10Hz to 1MHz	+25°C	-	375	-	nVrms
Input Noise Voltage	f_O = 10Hz	+25°C	-	8.9	-	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	-	3.7	-	$nV/\sqrt{Hz}$
	f_O = 1000Hz	+25°C	-	2.7	-	$nV/\sqrt{Hz}$
Input Noise Current	f_O = 10Hz	+25°C	-	25	-	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	-	8.4	-	$pA/\sqrt{Hz}$
	f_O = 1000Hz	+25°C	-	4.5	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain (Note 2, 4)		Full	80	105	-	V/mV
Common Mode Rejection Ratio (Note 3)		+25°C	100	110	-	dB
		Full	90	108	-	dB
Gain Bandwidth Product	f_O = 1MHz	+25°C	-	1	-	GHz
Minimum Stable Gain		Full	10	-	-	V/V
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 4)		Full	±3.5	±3.9	-	V
Full Power Bandwidth (Note 5)		+25°C	10.6	13.3	-	MHz
Output Resistance, Open Loop		+25°C	-	5	-	Ω
Output Current		Full	±10	±12	-	mA
TRANSIENT RESPONSE						
Rise Time (Note 4, 6)		+25°C	-	3.2	-	ns
Slew Rate (Note 4, 7)		+25°C	200	250	-	V/µs
Settling Time (Note 4, 7)		+25°C	-	50	-	ns
Overshoot (Note 4, 6)		+25°C	-	30	-	%
POWER SUPPLY CHARACTERISTICS						
Supply Current		Full	-	14	20	mA
Power Supply Rejection Ratio (Note 8)		Full	90	99	-	dB

NOTES:

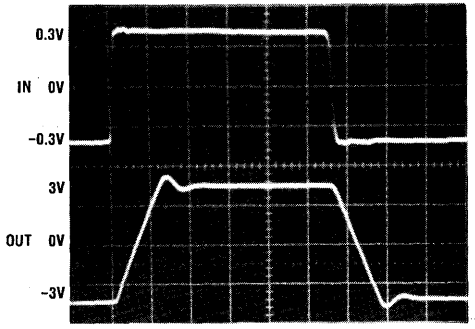
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±3V
3. ΔV_{CM} = ±2V
4. R_L = 5K, C_L = 20pF
5. Full Power Bandwidth is guaranteed by equation:
   $FPB = \frac{\text{Slew Rate}}{2\pi\ V\text{peak}}$, Vpeak = 3.0V
6. V_{OUT} = ±100mV, A_V = +10
7. V_{OUT} = ±3V, A_V = +10
8. ΔV_S = ±4V to ±6V
9. V_{OUT} = ±3.5V

Test Circuits

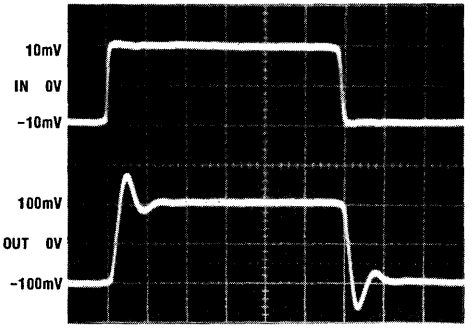
LARGE & SMALL SIGNAL RESPONSE TEST CIRCUIT



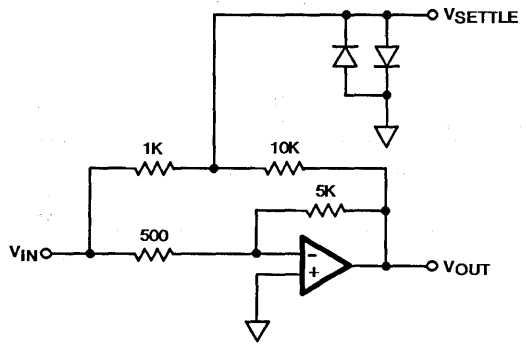
LARGE SIGNAL RESPONSE
Input: 0.2V/Div. Output: 2V/Div.
Horizontal Scale: 20ns/Div.



SMALL SIGNAL RESPONSE
Input: 10mV/Div. Output: 100mV/Div.



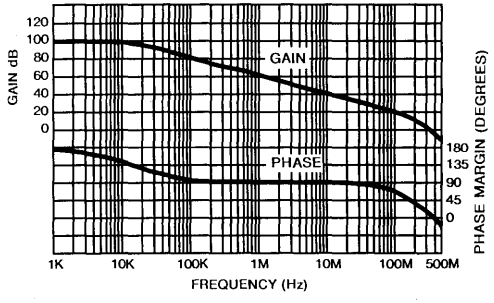
SETTLING TIME SCHEMATIC



- A_V = -1
- Feedback and summing resistors must be matched (0.1%)
- HP5082-2810 clipping diodes recommended
- Tektronix P6201 FET probe used at settling point

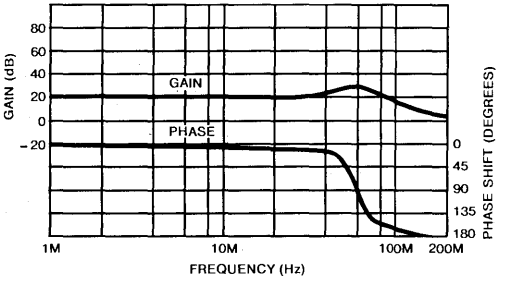
Typical Performance Curves $V_S = \pm5V$, $T_A = +25^oC$, Unless Otherwise Specified

OPEN LOOP GAIN AND PHASE vs FREQUENCY

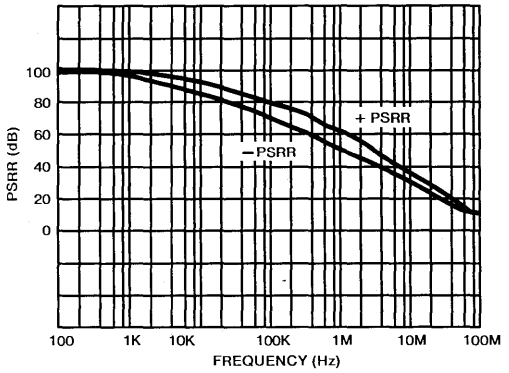


CLOSED LOOP GAIN vs FREQUENCY

$A_V = +10$, $R_L = 5K$, $C_L = 20pF$

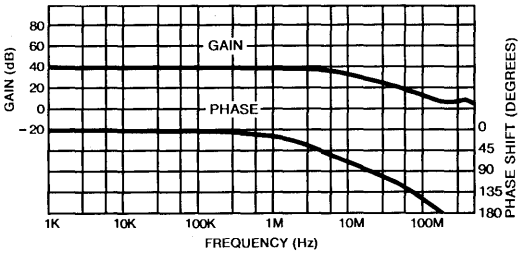


PSRR vs FREQUENCY

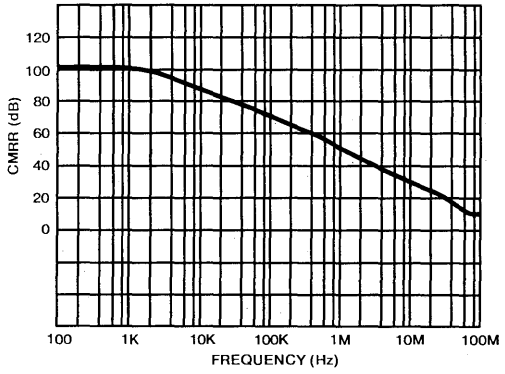


CLOSED LOOP GAIN vs FREQUENCY

$A_V = +100$, $R_L = 5K$, $C_L = 20pF$

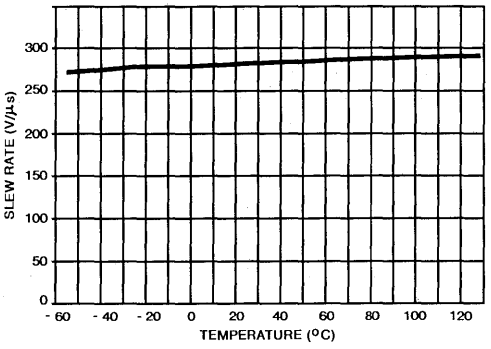


CMRR vs FREQUENCY



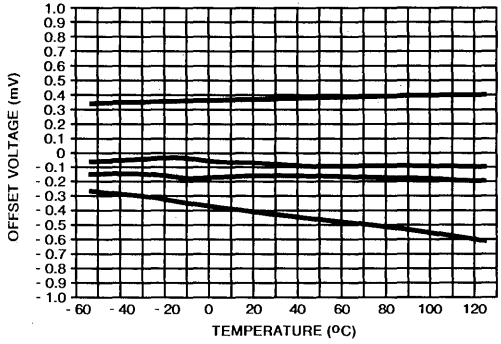
SLEW RATE vs TEMPERATURE

$V_{OUT} = 3V$, $R_L = 5K$, $C_L = 20pF$

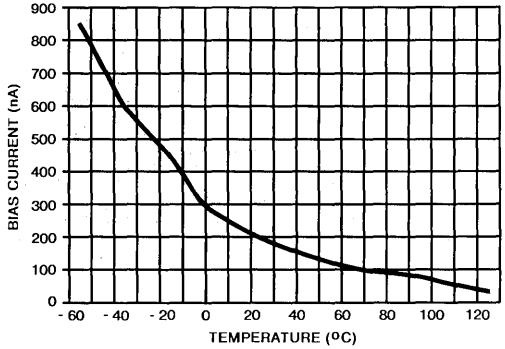


Typical Performance Curves (Continued) $V_S = \pm 5V$, $T_A = +25^oC$, Unless Otherwise Specified

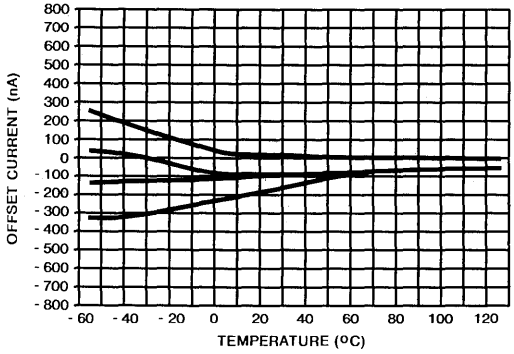
OFFSET VOLTAGE vs TEMPERATURE
4 Representative Units



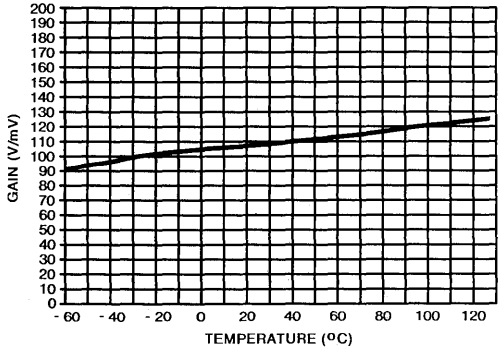
BIAS CURRENT vs TEMPERATURE



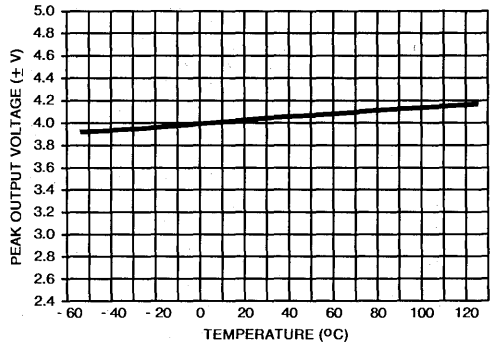
OFFSET CURRENT vs TEMPERATURE
4 Representative Units



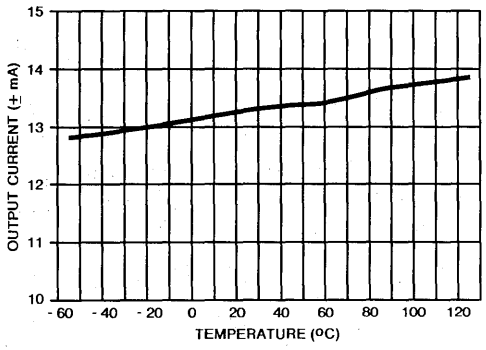
OPEN LOOP GAIN vs TEMPERATURE
$R_L = 5K$, $V_{OUT} = 0$ to $\pm 3\Omega$



OUTPUT VOLTAGE SWING vs TEMPERATURE
$R_L = 5K$

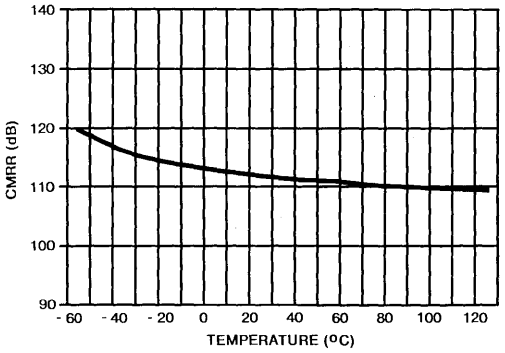


OUTPUT CURRENT vs TEMPERATURE
$V_{OUT} = \pm 3V$

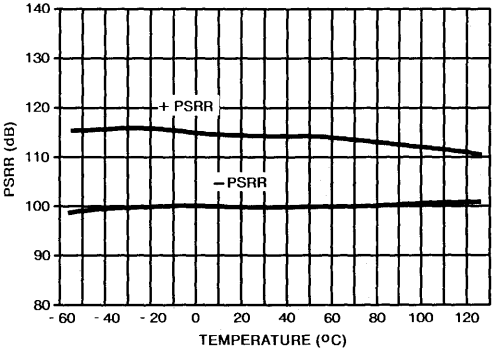


Typical Performance Curves (Continued) $V_S = \pm5V$, $T_A = +25^oC$, Unless Otherwise Specified

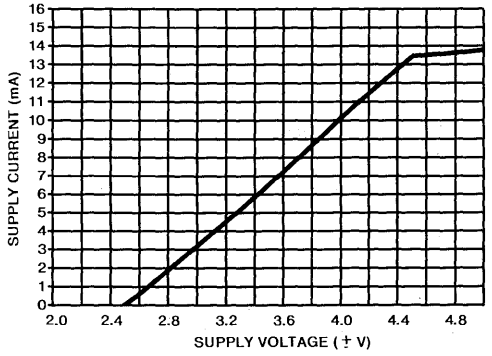
CMRR vs TEMPERATURE
V_{CM} = 0 to ±3V



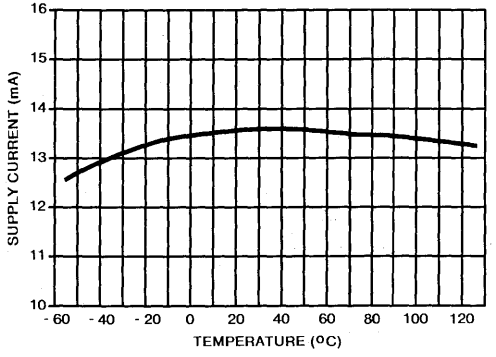
PSRR vs TEMPERATURE
ΔV_S = ±4V to ±6V



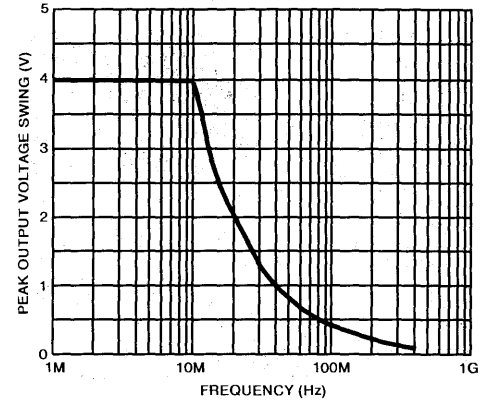
SUPPLY CURRENT vs SUPPLY VOLTAGE



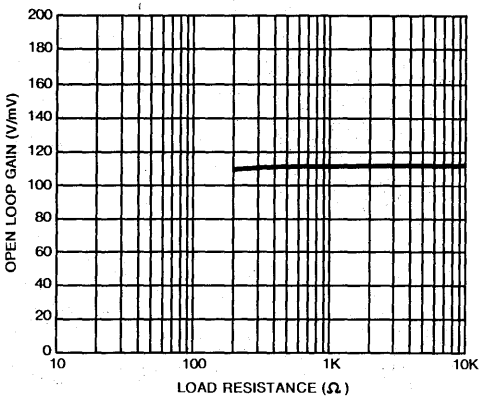
SUPPLY CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs FREQUENCY
A_V = +10, R_L = 5K,

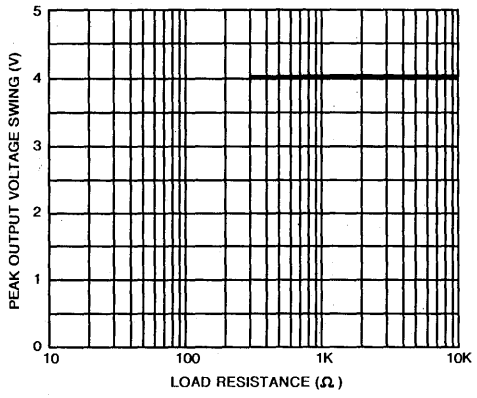


OPEN LOOP GAIN vs LOAD RESISTANCE
V_{OUT} = ±3V

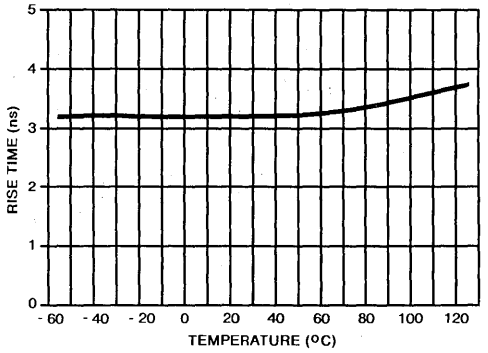


Typical Performance Curves (Continued) $V_S = \pm5V$, $T_A = +25^oC$, Unless Otherwise Specified

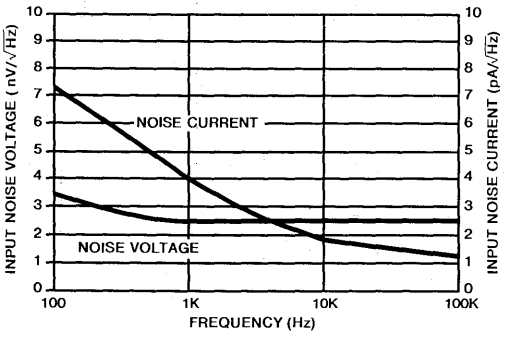
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



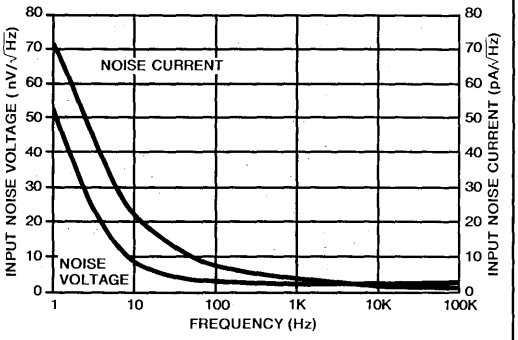
RISE TIME vs TEMPERATURE



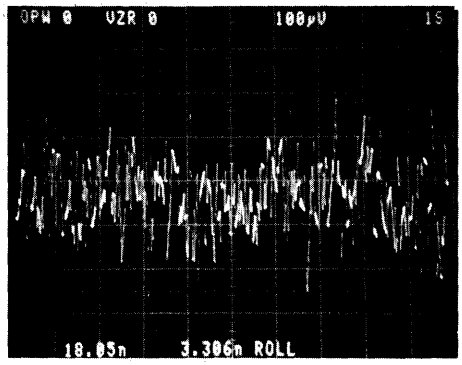
INPUT NOISE vs FREQUENCY



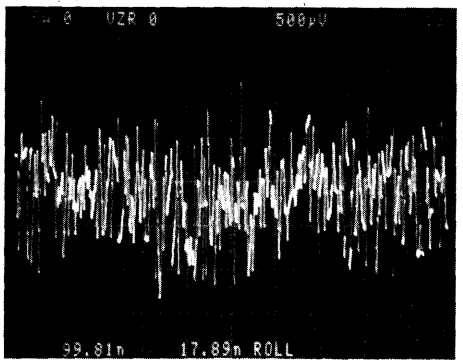
INPUT NOISE vs FREQUENCY



INPUT NOISE VOLTAGE
0.1Hz to 10Hz
A_V = 25,000, Noise Voltage = 3.31nV$_{rms}$ (RTI)



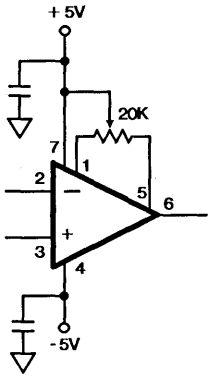
INPUT NOISE VOLTAGE
10Hz to 1MHz
A_V = 25,000, Noise Voltage = 17.89nV$_{rms}$ (RTI)



Applications Information

Offset Voltage Adjustment

The HFA-0002, due to its low offset voltage, will typically not require any external offset adjustment. If certain applications do require lower offset, the following diagram shows one possible configuration.



The power supply lines must be well decoupled to filter any power supply noise. A 20K trim pot will allow an offset adjustment of about 3mV, referred to input.

PC Board Layout Guidelines

When designing with the HFA-0002, good high frequency (RF) techniques should be used when doing pc board layouts. A massive ground plane should be used to maintain a low impedance ground. PC board traces should be kept as short as possible and kept wide to minimize trace inductance and impedance. Stray capacitance at the op amps output and at the high impedance inputs should be kept to a minimum, to prevent any unwanted phase shift and bandwidth limiting.

When breadboarding remember to keep feedback resistor values low ($\leq$5kΩ) for optimum performance. The use of metal film resistors for values over 200Ω and carbon film resistors under 200Ω typically gives the best performance. Remember to keep all lead lengths as short as possible to minimize lead inductance.

Sockets will add parasitic capacitance and inductance and therefore can limit AC performance as well as reduce stability. If sockets must be used, a low profile socket with minimum pin to pin capacitance will minimize any performance degradation.

Power supply decoupling is essential for high frequency op amps. A 0.01μF high quality ceramic capacitor at each supply pin in parallel with a 1μF tantalum capacitor will provide excellent decoupling. Chip capacitors produce the best results due to the ease of placement next to the op amp and they have negligible lead inductance. If leaded capacitors are used, again the lead lengths should be kept to a minimum.

Saturation Recovery

When an op amp is over driven output devices can saturate and sometime take a long time to recover. By clamping the input to safe levels, output saturation can be avoided. If output saturation cannot be avoided, the recovery time for an input sine wave at 25% overdrive is 100ns.

Thermal Constants (^{o}C/W)	θja	θjc
HFA2-0002-5/-9	153	46
HFA3-0002-5/-9	90	30
HFA7-0002-5/-9	87	27

HARRIS

HFA-0005

High Slew Rate Operational Amplifier

May 1990

Features

- Unity Gain Bandwidth 300MHz
- Full Power Bandwidth 22MHz
- High Slew Rate 420V/μs
- High Output Drive ..... ±50mA
- Monolithic Bipolar Construction

Applications

- RF/IF Processors
- Video Amplifiers
- Radar Systems
- Pulse Amplifiers
- High Speed Communications
- Fast Data Acquisition Systems

Description

The HFA-0005 is an all bipolar op amp featuring high slew rate (420V/μs), and high unity gain bandwidth (300MHz). These features combined with fast settling time (20ns) make this product very useful in high speed data acquisition systems as well as RF, video, and pulse amplifier designs.

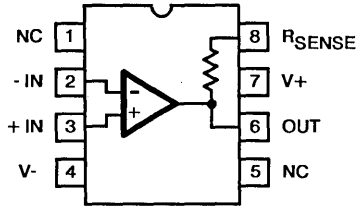
Other outstanding characteristics include low bias currents (15μA), low offset current (6μA), and low offset voltage (6mV). These high performance characteristics are achieved with only 40mA of supply current.

The HFA-0005 offers high performance at low cost. It can replace hybrids and RF transistor amplifiers, simplifying designs while providing increased reliability due to monolithic construction. To enhance the ease of design, the HFA-0005 has a 50Ω ±20% resistor connected from the output of the op amp to a separate pin. This can be used when driving 50Ω strip line, microstrip, or coax cable.

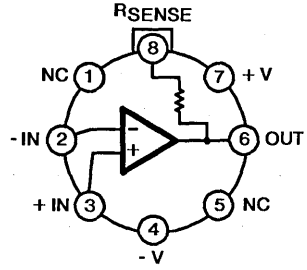
The performance of the HFA-0005-9 is guaranteed from -40°C to +85°C, while the HFA-0005-5 is guaranteed from 0°C to +75°C. The HFA-0005 is available in 8 pin SOIC, 8 pin Sidebraze, 8 pin Epoxy Mini-Dip, and 8 pin TO-99 Metal Can packages. For MIL-STD-883 compliant product and Ceramic LCC package consult the HFA-0005/883 datasheet.

Pinouts

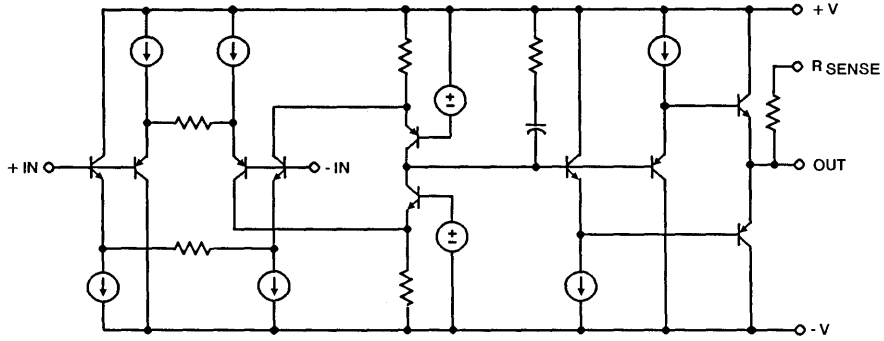
HFA9P0005-5/-9 (SOIC)
HFA7-0005-5/-9
(CERAMIC SIDEBRAZE DIP)
HFA3-0005-5/-9 (PLASTIC MINI-DIP)
TOP VIEW



HFA2-0005 (TO-99 METAL CAN)
TOP VIEW



Simplified Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals ..... ±12V
Differential Input Voltage..... 5V
Common Mode Input Voltage ..... ±4V
Output Current ..... ±60mA

Operating Temperature Range

HFA-0005-9..... $-40^{o}C \leq T_A \leq +85^{o}C$
HFA-0005-5..... $0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature..... $-65^{o}C \leq T_A \leq +150^{o}C$
Maximum Junction Temperature..... $+175^{o}C$

Electrical Specifications V+ = +5V, V- = -5V, Unless Otherwise Specified

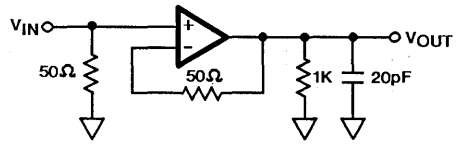
PARAMETER		TEMP	HFA-0005-9 MIN	HFA-0005-9 TYP	HFA-0005-9 MAX	HFA-0005-5 MIN	HFA-0005-5 TYP	HFA-0005-5 MAX	UNITS
INPUT CHARACTERISTICS									
Offset Voltage		+25°C	-	6	15	-	6	30	mV
		Full	-	11	45	-	11	35	mV
Average Offset Voltage Drift		Full	-	100	-	-	100	-	µV/°C
Bias Current		+25°C	-	15	50	-	15	100	µA
		Full	-	20	50	-	20	100	µA
Offset Current		+25°C	-	6	25	-	6	50	µA
		Full	-	12	50	-	12	50	µA
Common Mode Range		Full	±3	-	-	±3	-	-	V
Differential Input Resistance		+25°C	-	10	-	-	10	-	KΩ
Input Capacitance		+25°C	-	2	-	-	2	-	pF
Input Noise Voltage	0.1Hz to 10Hz	+25°C	-	2.5	-	-	2.5	-	µVrms
	10Hz to 1MHz	+25°C	-	5.8	-	-	5.8	-	µVrms
Input Noise Voltage	f_O = 10Hz	+25°C	-	450	-	-	450	-	$nV/\sqrt{Hz}$
	f_O = 100Hz	+25°C	-	160	-	-	160	-	$nV/\sqrt{Hz}$
	f_O = 1000Hz	+25°C	-	40	-	-	40	-	$nV/\sqrt{Hz}$
Input Noise Current	f_O = 10Hz	+25°C	-	2.0	-	-	2.0	-	$pA/\sqrt{Hz}$
	f_O = 100Hz	+25°C	-	0.57	-	-	0.57	-	$pA/\sqrt{Hz}$
	f_O = 1000Hz	+25°C	-	0.11	-	-	0.11	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS									
Large Signal Voltage Gain (Note 2)		+25°C	150	230	-	150	230	-	V/V
		High	150	180	-	150	180	-	V/V
		Low	150	250	-	150	250	-	V/V
Common Mode Rejection Ratio (Note 3)		Full	45	47	-	42	45	-	dB
Unity Gain Bandwidth		+25°C	-	300	-	-	300	-	MHz
Minimum Stable Gain		Full	1	-	-	1	-	-	V/V
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 100Ω	+25°C	-	±3.5	-	-	±3.5	-	V
	R_L = 1K	Full	±3.5	±4.0	-	±3.5	±4.0	-	V
Full Power Bandwidth (Note 5)		+25°C	-	22	-	-	22	-	MHz
Output Resistance, Open Loop		+25°C	-	3.0	-	-	3.0	-	Ω
Output Current		Full	±25	±50	-	±25	±50	-	mA
TRANSIENT RESPONSE									
Rise Time (Note 4, 6)		+25°C	-	480	-	-	480	-	ps
Slew Rate (Note 7)		+25°C	-	420	-	-	420	-	V/µs
Settling Time (3V Step) 0.1%		+25°C	-	20	-	-	20	-	ns
Overshoot (Note 4, 6)		+25°C	-	30	-	-	30	-	%
POWER SUPPLY CHARACTERISTICS									
Supply Current		+25°C	-	35	40	-	35	40	mA
		Full	-	37	40	-	37	45	mA
Power Supply Rejection Ratio (Note 8)		+25°C	40	42	-	37	40	-	dB

NOTES:

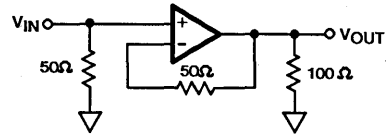
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = 0 to ±2V, R_L = 1K
3. ΔV_{CM} = ±2V
4. R_L = 100Ω
5. Full Power Bandwidth is calculated by equation:
$$FPB = \frac{\text{Slew Rate}}{2\pi\ Vpeak} \quad Vpeak = 3.0V$$
6. V_{OUT} = ±200mV, A_V = +1
7. V_{OUT} = ±3V, A_V = +1
8. ΔV_S = ±4V to ±6V

Test Circuits

LARGE SIGNAL RESPONSE TEST CIRCUIT



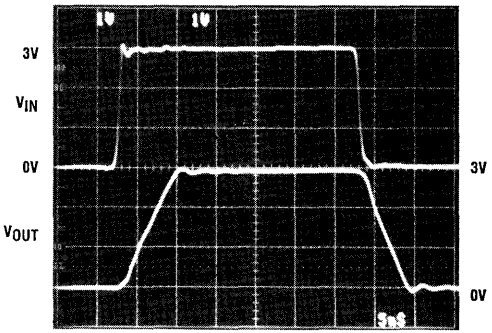
SMALL SIGNAL RESPONSE TEST CIRCUIT



LARGE SIGNAL RESPONSE

V_{OUT} = 0 to 3V

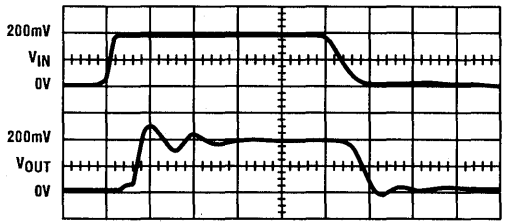
Vertical Scale: 1V/Div. Horizontal Scale: 5ns/Div.



SMALL SIGNAL RESPONSE

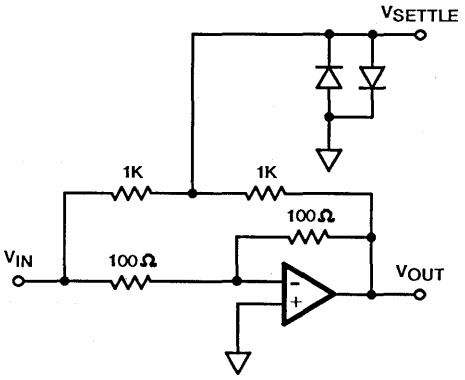
V_{OUT} = 0 to 200mV

Vertical Scale: 100mV/Div. Horizontal Scale: 2ns/Div.



NOTE: Initial step in output is due to fixture feedthrough

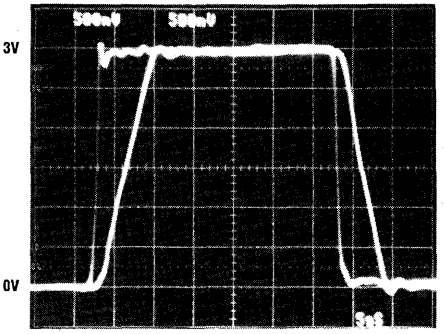
SETTLING TIME SCHEMATIC



PROPAGATION DELAY

Vertical Scale: 500mV/Div. Horizontal Scale: 5ns/Div.

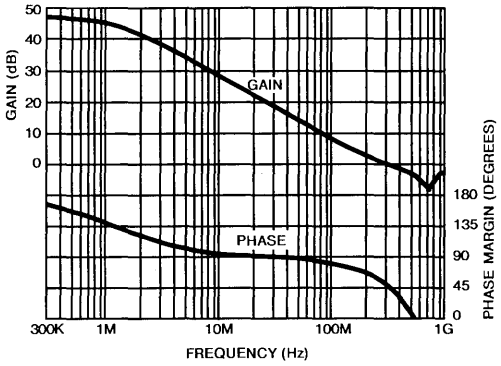
A_V = +1, R_L = 1K, V_{OUT} = 0 to 3V



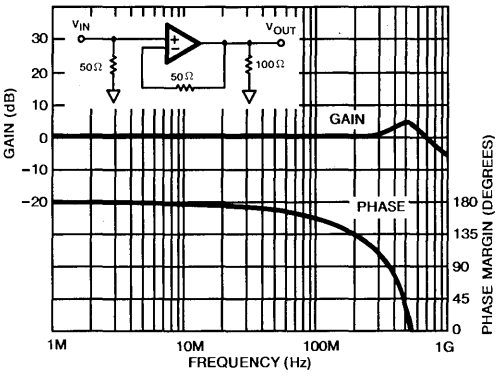
*NOTE: Test fixture delay of 450ps is included.

Typical Performance Curves $V_S = \pm5V$, $T_A = +25^oC$, Unless Otherwise Specified

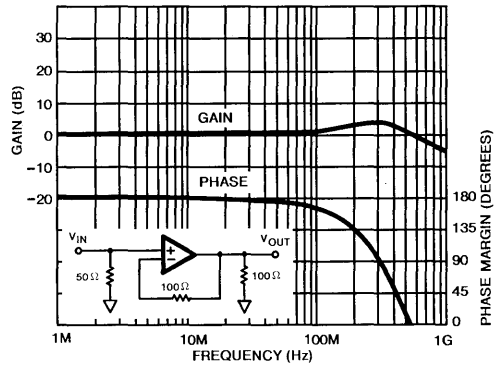
OPEN LOOP GAIN AND PHASE vs FREQUENCY
$R_L = 100\Omega$



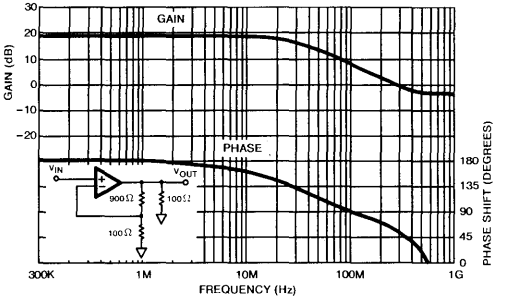
CLOSED LOOP GAIN vs FREQUENCY
$A_V = +1$, $R_L = 100$, $R_F = 50\Omega$, $V_{IN} = 70.7mV_{rms}$



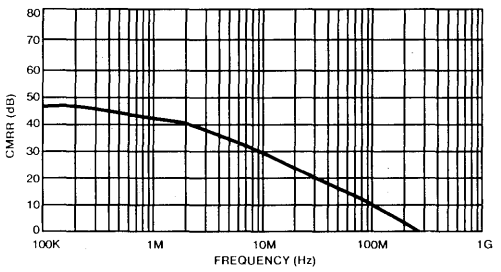
CLOSED LOOP GAIN vs FREQUENCY



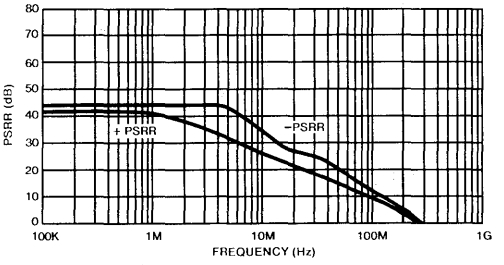
CLOSED LOOP GAIN vs FREQUENCY
$A_V = +10$, $R_L = 100\Omega$



CMRR vs FREQUENCY

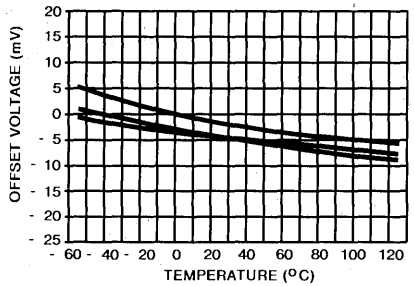


PSRR vs FREQUENCY

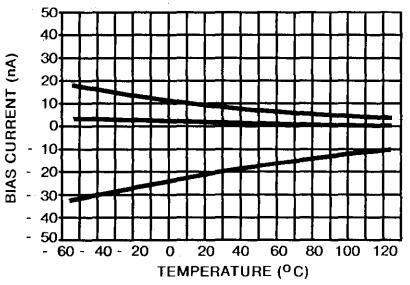


Typical Performance Curves (Continued) $V_S = \pm 5V$, $T_A = +25^oC$, Unless Otherwise Specified

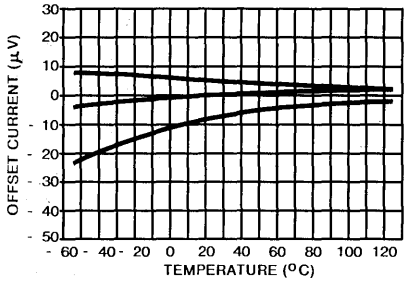
OFFSET VOLTAGE vs TEMPERATURE
3 Representative Units



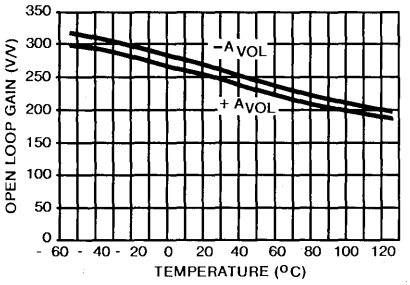
BIAS CURRENT vs TEMPERATURE
3 Representative Units



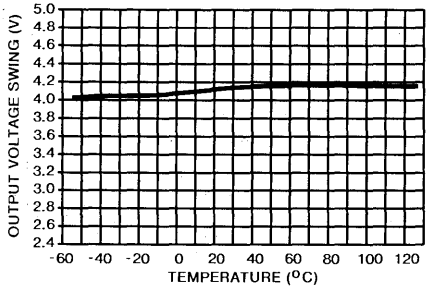
OFFSET CURRENT vs TEMPERATURE
3 Representative Units



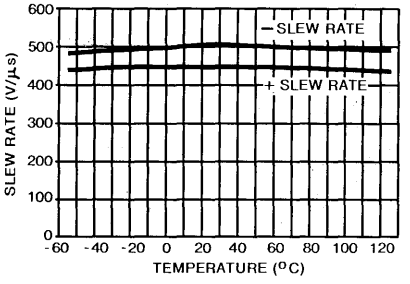
OPEN LOOP GAIN vs TEMPERATURE
R_L = 1K, V_{OUT} = 0 to ±2V



OUTPUT VOLTAGE SWING vs TEMPERATURE
R_L = 1K

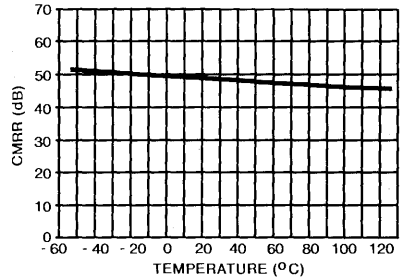


SLEW RATE vs TEMPERATURE
A_V = +1, R_L = 100Ω, V_{OUT} = 3V

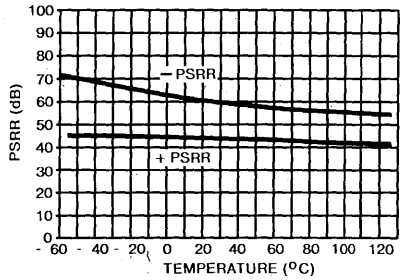


Typical Performance Curves (Continued) $V_S = \pm 5V$, $T_A = 25^oC$, Unless Otherwise Specified

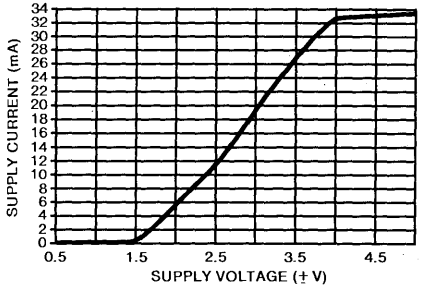
CMRR vs TEMPERATURE



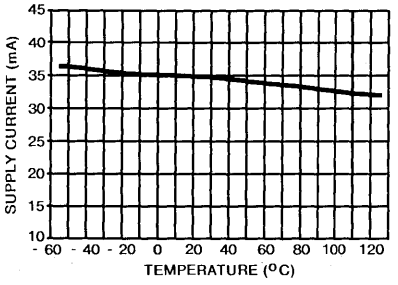
PSRR vs TEMPERATURE
$\Delta V_S = \pm 4V$ to $\pm 6V$



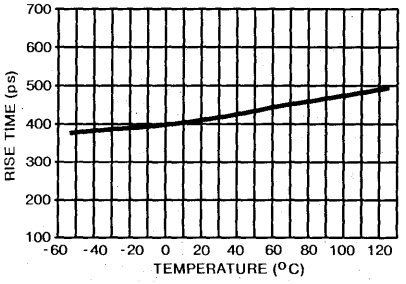
SUPPLY CURRENT vs SUPPLY VOLTAGE



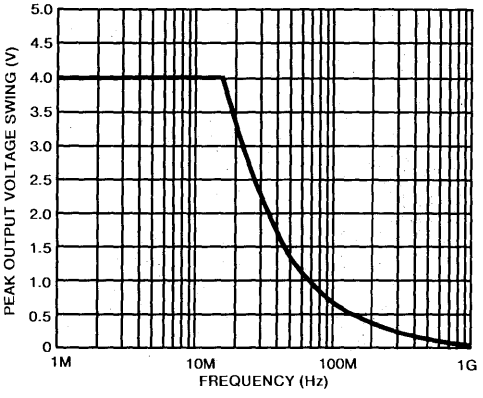
SUPPLY CURRENT vs TEMPERATURE



RISE TIME vs TEMPERATURE
$A_V = +1$, $R_L = 100\Omega$, $V_{OUT} = 0$ to 200mV

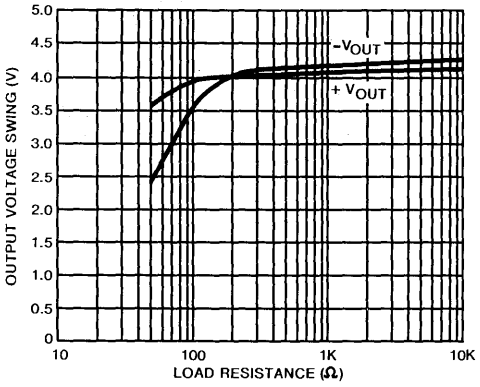


MAXIMUM OUTPUT VOLTAGE SWING vs FREQUENCY
$A_V = +1$, $R_L = 1K$, THD $\leq 1\%$

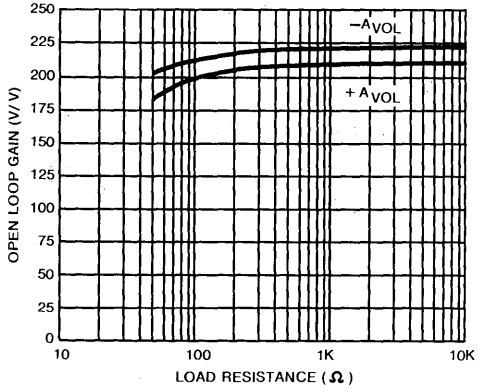


Typical Performance Curves (Continued) $V_S = \pm5V$, $T_A = +25^oC$, Unless Otherwise Specified

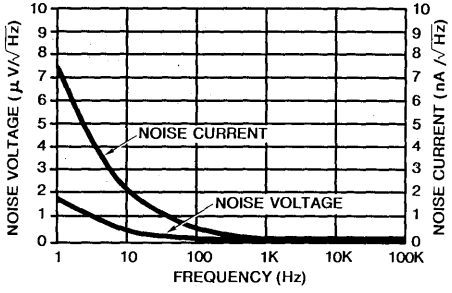
OUTPUT VOLTAGE SWING vs LOAD RESISTANCE



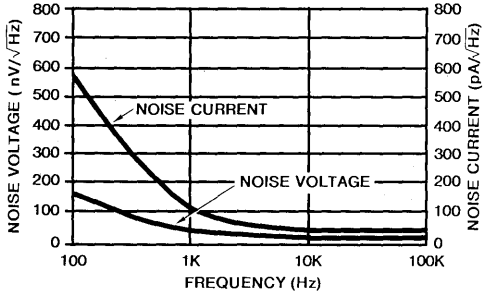
OPEN LOOP GAIN vs LOAD RESISTANCE
V_{OUT} = 0 to ±3V



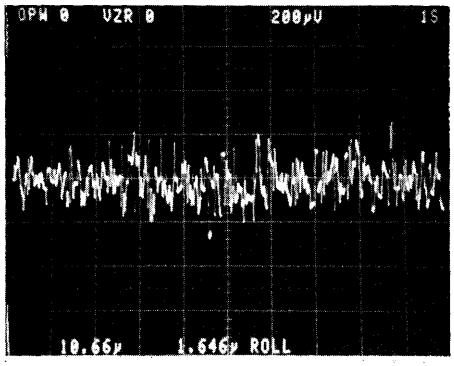
INPUT NOISE vs FREQUENCY



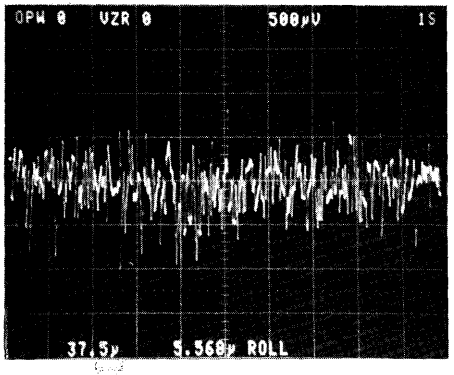
INPUT NOISE vs FREQUENCY



INPUT NOISE VOLTAGE
A_V = 50, Noise Voltage = 1.646μV_{rms} (RTI)



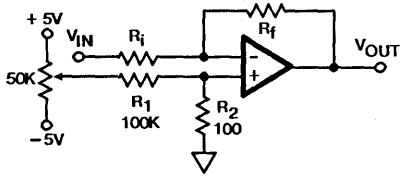
INPUT NOISE VOLTAGE
A_V = 50, Noise Voltage = 5.568μV_{rms} (RTI)



Applications Information

Offset Adjustment

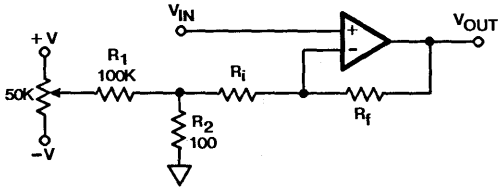
When applications require the offset voltage to be as low as possible, the figure below shows two possible schemes for adjusting offset voltage.



Adjustment Range $\simeq \pm V \left(\frac{R_2}{R_1}\right)$

FIGURE 1. INVERTING GAIN

For a voltage follower application, use the circuit in Figure 2 without R2 and with Ri shorted. R1 should be 1MV to 10MV. the adjustment resistors will cause only a very small gain error.



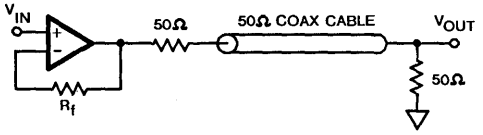
Adjustment Range $\simeq \pm V \left(\frac{R_2}{R_1}\right)$ Gain $\simeq 1 + \left(\frac{R_f}{R_i + R_2}\right)$

FIGURE 2. NON-INVERTING GAIN

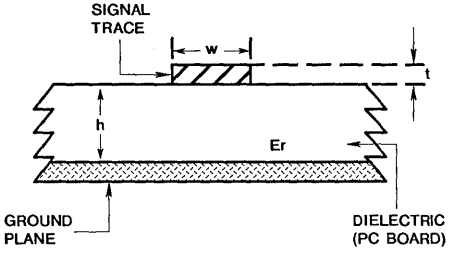
PC Board Layout Guidelines

When designing with the HFA-0005, good high frequency (RF) techniques should be used when making a PC board. A massive ground plane should be used to maintain a low impedance ground. Proper shielding and use of short interconnection leads are also very important.

To achieve maximum high frequency performance, the use of low impedance transmission lines with impedance matching is recommended: 50Ω lines are common in communications and 75Ω lines in video systems. Impedance matching is important to minimize reflected energy therefore minimizing transmitted signal distortion. This is accomplished by using a series matching resistor (50 or 75Ω), matched transmission line (50 or 75Ω), and a matched terminating resistor, as shown in the figure below. Note that there will be a 6dB loss from input to output. The HFA-0005 has an integral 50Ω ±20% resistor connected to the op amps output with the other end of the resistor pinned out. This 50Ω resistor can be used as the series resistor instead of an external resistor.



PC board traces can be made to look like a 50 or 75Ω transmission line, called microstrip. Microstrip is a PC board trace with a ground plane directly beneath, on the opposite side of the board, as shown below.



Applications Information (Continued)

When manufacturing pc boards the trace width can be calculated based on a number of variables.

The following equation is reasonably accurate for calculating the proper trace width for a 50Ω transmission line.

$$Z_0 = \frac{87}{\sqrt{E_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right) \Omega$$

Power supply decoupling is essential for high frequency op amps. A 0.01μf high quality ceramic capacitor at each supply pin in parallel with a 1μf tantalum capacitor will provide excellent decoupling. Chip capacitors produce the best results due to ease of placement next to the op amp and they have negligible lead inductance. If leaded capacitors are used, the leads should be kept as short as possible to minimize lead inductance. The figures below illustrate two different decoupling schemes. Figure 4 improves the PSRR because the resistor and capacitors create low pass filters. Note that the supply current will create a voltage drop across the resistor.

Saturation Recovery

When an op amp is over driven output devices can saturate and sometimes take a long time to recover. By clamping the input to safe levels, output saturation can be avoided. If output saturation cannot be avoided, the recovery time from 25% over-drive is 20ns and 30ns from 50% over-drive.

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HFA2-0005-5/-9	153	46
HFA3-0005-5	90	30
HFA7-0005-5/-9	87	27

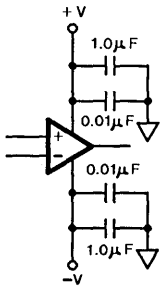


FIGURE 3.

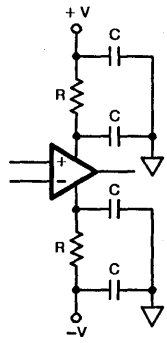


FIGURE 4.

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICL7605/ICL7606
Commutating Auto-Zero (CAZ) Instrumentation Amplifier

GENERAL DESCRIPTION

The ICL7605/ICL7606 CMOS commutating auto-zero (CAZ) instrumentation amplifiers are designed to replace most of today's hybrid or monolithic instrumentation amplifiers, for low frequency applications from DC to 10Hz. This is made possible by the unique construction of this Harris device, which takes an entirely new design approach to low frequency amplifiers.

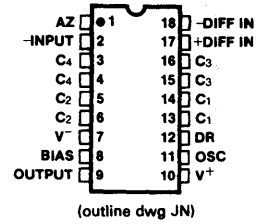
Unlike conventional amplifier designs, which employ three op-amps and require ultra-high accuracy in resistor tracking and matching, the CAZ instrumentation amplifier requires no trimming except for gain. The key features of the CAZ principle involve automatic compensation for long-term drift phenomena and temperature effects, and a flying capacitor input.

The ICL7605/ICL7606 consist of two analog sections — a unity gain differential to single-ended voltage converter and a CAZ op amp. The first section senses the differential input and applies it to the CAZ amp section. This section consists of an operational amplifier circuit which continuously corrects itself for input voltage errors, such as input offset voltage, temperature effects, and long term drift.

The ICL7605/ICL7606 is intended for low-frequency operation in applications such as strain gauge amplifiers which require voltage gains from 1 to 1000 and bandwidths from DC to 10Hz. Since the CAZ amp automatically corrects itself for internal errors, the only periodic adjustment required is that of gain, which is established by two external resistors. This, combined with extremely low offset and temperature coefficient figures, makes the CAZ instrumentation amplifier very desirable for operation in severe environments (temperature, humidity, toxicity, radiation, etc.) where equipment service is difficult.

FEATURES

- **Exceptionally Low Input Offset Voltage — 2μV**
- **Low Long Term Input Offset Voltage Drift — 0.2μV/Year**
- **Low Input Offset Voltage Temperature Coefficient — 0.05μV/°C**
- **Wide Common Mode Input Voltage Range — 0.3V Above Supply Rail**
- **High Common Mode Rejection Ratio — 100 dB**
- **Operates at Supply Voltages As Low As ±2V**
- **Short Circuit Protection On Outputs for ±5V Operation**
- **Static-Protected Inputs — No Special Handling Required**
- **Compensated (ICL7605) or Uncompensated (ICL7606) Versions**



(outline dwg JN)

0306-1

Figure 1: Pin Configuration

ORDERING INFORMATION

Order parts by the following part numbers:

Part Number	Compensation	Temperature Range	Package
ICL7605CJN	INTERNAL	0°C to +70°C	18-PIN CERDIP
ICL7605IJN	INTERNAL	−25°C to +85°C	18-PIN CERDIP
ICL7605MJN	INTERNAL	−55°C to +125°C	18-PIN CERDIP
ICL7606CJN	EXTERNAL	0°C to +70°C	18-PIN CERDIP
ICL7606IJN	EXTERNAL	−25°C to +85°C	18-PIN CERDIP
ICL7606MJN	EXTERNAL	−55°C to +125°C	18-PIN CERDIP

301681-004

NOTE: All typical values have been characterized but are not tested.

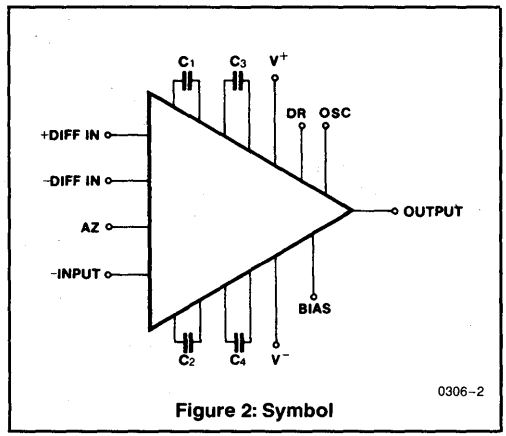


Figure 2: Symbol

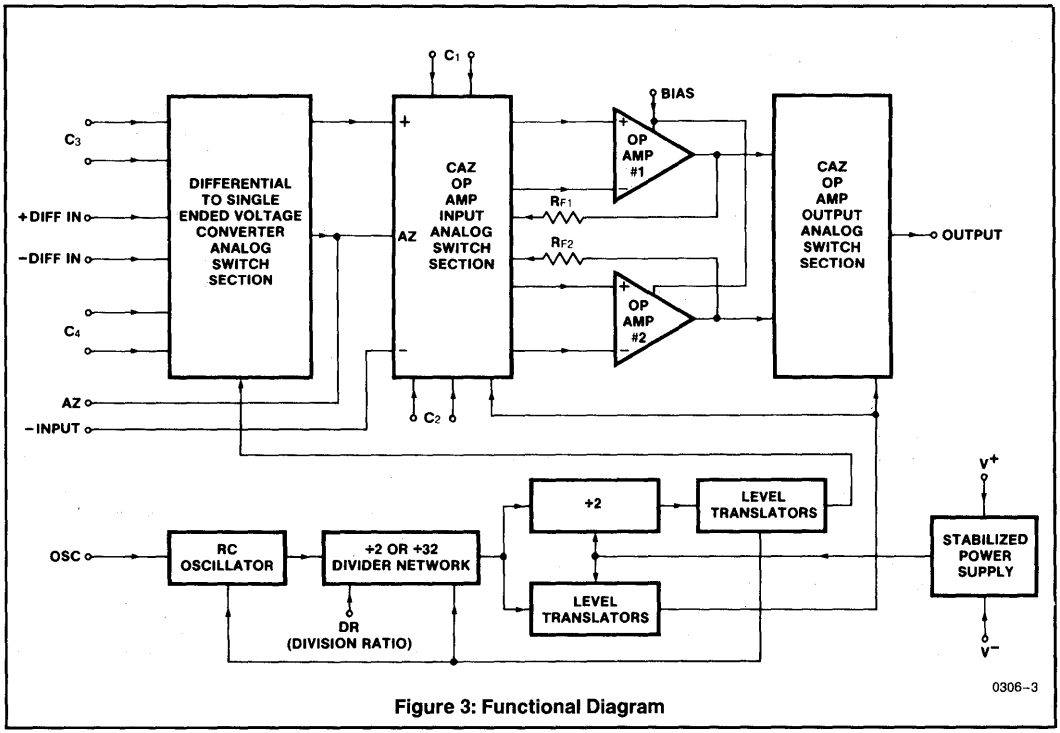


Figure 3: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
DR Input Voltage ..... ($V^+ - 8$) to ($V^+ + 0.3$)V
Input Voltage (C_1, C_2, C_3, C_4 + DIFF IN, − DIFF IN, − INPUT, BIAS, OSC), (Note 1) ..... ($V^- - 0.3$) to ($V^+ + 0.3$)V
Differential Input Voltage (+ DIFF IN to − DIFF IN) (Note 2) ..... ($V^- - 0.3$) to ($V^+ + 0.3$)V
Duration of Output Short Circuit (Note 3) ..... Unlimited
Continuous Total Power Dissipation (Note 4) 500mW
Operating Temperature Range:
ICL7605/ICL7606C ..... 0 to +70°C
ICL7605/ICL7606I ..... −25°C to +85°C
ICL7605/ICL7606M ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Note 1: Due to the SCR structure inherent in all CMOS devices, exceeding these limits may cause destructive latch up. For this reason, it is recommended that no inputs from sources operating on a separate power supply be applied to the 7605/6 before its own power supply is established, and that when using multiple supplies, the supply for the 7605/6 should be turned on first.

Note 2: No restrictions are placed on the differential input voltages on either the + DIFF IN or − DIFF IN inputs so long as these voltages do not exceed the power supply voltages by more than 0.3V.

Note 3: The outputs may be shorted to ground (GND) or to either supply (V^+ or V^-). Temperatures and/or supply voltages must be limited to insure that the dissipation ratings are not exceeded.

Note 4: For operation above 25°C ambient temperature, derate 4mW/°C from 500mW above 25°C.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$, $f_{COM1} \cong 80Hz$), $C_1 = C_2 = C_3 = C_4 = 1\mu F$, Test Circuit 1 unless otherwise specified.

Symbol	Parameter	Test Conditions		Value Min	Value Typ	Value Max	Units
V_{OS}	Input Offset Voltage	$R_S \leq 1k\Omega$	Low Bias Setting		±2		μV
			Med Bias Setting		±2	±5	μV
			High Bias Setting		±7		μV
		MIL version over temp.	Med Bias Setting			±30	μV
$\Delta V_{OS}/\Delta T$	Average Input Offset Voltage Temperature Coefficient (Note 5)	Low or Med Bias Settings	$-55°C > T_A > +25°C$		0.01	0.2	μV/°C
			$+25°C > T_A > +85°C$		0.01	0.2	μV/°C
			$+25°C > T_A > +125°C$		0.05	0.2	μV/°C
$\Delta V_{OS}/\Delta t$	Long Term Input Offset Voltage Stability	Low or Med Bias Settings			0.5		μV/Year
CMVR	Common Mode Input Range			−5.3		+5.3	V
CMRR	Common Mode Rejection Ratio	$C_{OSC} = 0$, DR connected to V^+, $C_3 = C_4 = 1\mu F$			94		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 1\mu F$			100		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 10\mu F$			104		dB
PSRR	Power Supply Rejection Ratio				110		dB
$-I_{BIAS}$	− INPUT Bias Current	Any bias setting, $f_c = 160Hz$ (Includes charge injection currents)			0.15	1.5	nA
$\bar{e}_n$(p-p)	Equivalent Input Noise Voltage peak-to-peak	Band Width 0.1 to 10Hz	Low Bias Mode		4.0		μV
			Med Bias Mode		4.0		μV
			High Bias Mode		5.0		μV

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$, $f_{COM1} \cong 80Hz$), $C_1 = C_2 = C_3 = C_4 = 1\mu F$, Test Circuit 1 unless otherwise specified. (Continued)

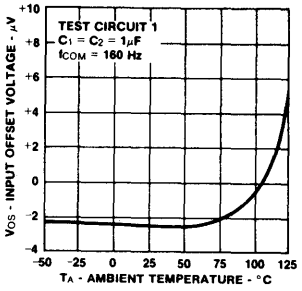
Symbol	Parameter	Test Conditions		Value			Units
				Min	Typ	Max	
$\bar{e}_n$	Equivalent Input Noise voltage	Band Width 0.1 to 1.0Hz	All Bias Modes		1.7		μV
A_{VOL}	Open Loop Voltage Gain	$R_L = 100k\Omega$	Low Bias Setting	90	105		dB
			Med Bias Setting	90	105		dB
			High Bias Setting	80	100		dB
$\pm V_O$	Maximum Output Voltage Swing	$R_L = 1M\Omega$			± 4.9		V
		$R_L = 100k\Omega$			± 4.8		V
		$R_L = 10k\Omega$	Positive Swing	+4.4			V
			Negative Swing			−4.5	V
GBW	Bandwidth of Input Voltage Translator	$C_3 = C_4 = 1\mu F$	All Bias Modes		10		Hz
f_{COM}	Nominal Commutation Frequency	$C_{OSC} = 0$	DR Connected to V^+		160		Hz
			DR Connected to GND		2560		Hz
f_{COM1}	Nominal Input Converter Commutation Frequency	$C_{OSC} = 0$	DR Connected to V^+		80		Hz
			DR Connected to GND		1280		Hz
V_{BH}	Bias Voltage required to set Quiescent Current	Low Bias Setting		$V^+ - 0.3$	V^+	$V^+ + 0.3$	V
V_{BM}		Med Bias Setting		$V^- + 1.4$	GND	$V^+ - 1.4$	V
V_{BL}		High Bias Setting		$V^- - 0.3$	V^-	$V^- + 0.3$	V
I_{BIAS}	Bias (Pin 8) Input Current				±30		pA
I_{DR}	Division Ratio Input Current	$V^+ - 8.0 \le V_{DR} \le V^+ + 0.3$ volt			±30		pA
V_{DRH}	DR Voltage required to set Oscillator division ratio	Internal oscillator division ratio 32		$V^+ - 0.3$		$V^+ + 0.3$	V
V_{DRL}		Internal oscillator division ratio 2		$V^+ - 8$		$V^+ - 1.4$	V
R_{AS}	Effective Impedance of Voltage Translator Analog Switches				30		kΩ
I_{SUPP}	Supply Current	High Bias Setting			7	15	mA
		Med Bias Setting			1.7	5	mA
		Low Bias Setting			0.6	1.5	mA
$V^+ - V^-$	Operating Supply Voltage Range	High Bias Setting		5		10	V
		Med or Low Bias Setting		4		10	V

Note 5: For Design only, not tested.

NOTE: All typical values have been characterized but are not tested.

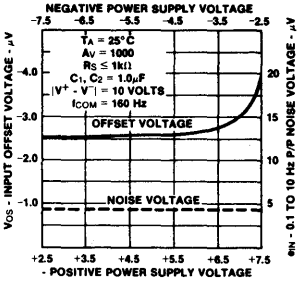
TYPICAL PERFORMANCE CHARACTERISTICS

INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE



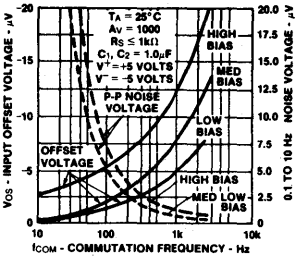
0306-4

INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES



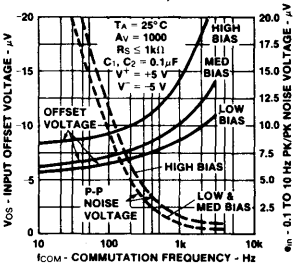
0306-5

INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 1μF)



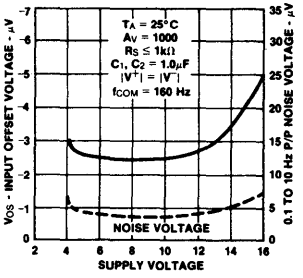
0306-6

INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 0.1 μF)



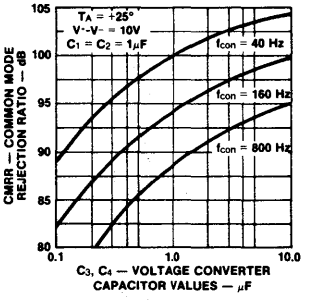
0306-7

INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE (V^+-V^-)



0306-8

COMMON MODE REJECTION RATIO AS A FUNCTION OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER CAPACITORS



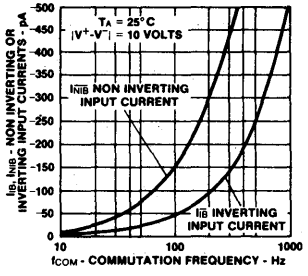
0306-9

3 OPERATIONAL AMPLIFIERS

NOTE: All typical values have been characterized but are not tested.

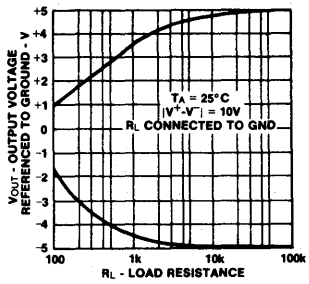
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY



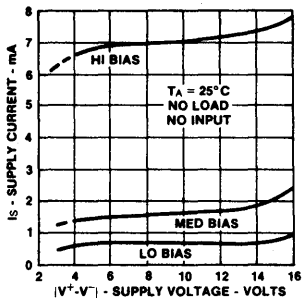
0306-10

MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE



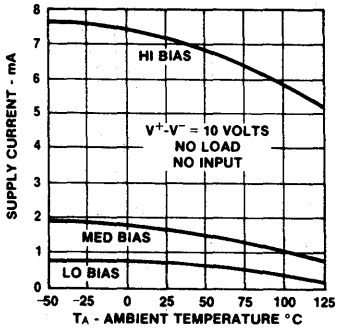
0306-11

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



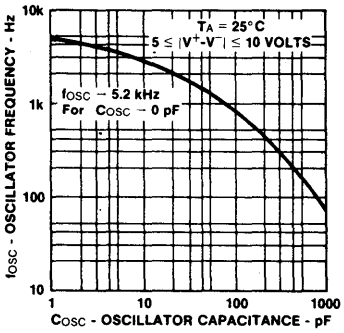
0306-12

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



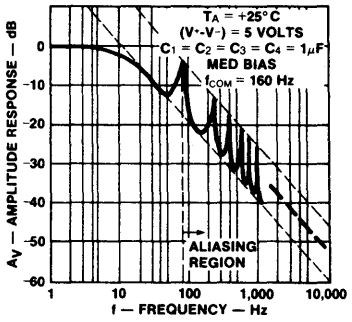
0306-13

OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING



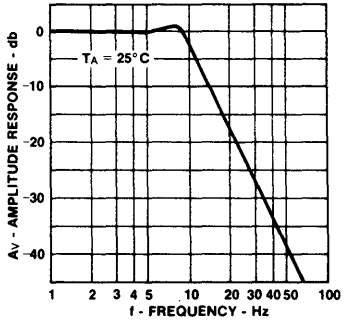
0306-14

AMPLITUDE RESPONSE OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER



0306-15

FREQUENCY RESPONSE OF THE 10Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 2).



0306-16

NOTE: All typical values have been characterized but are not tested.

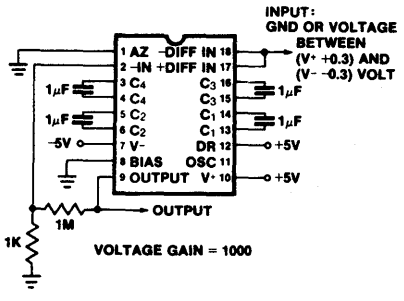


Figure 4: Test Circuit 1

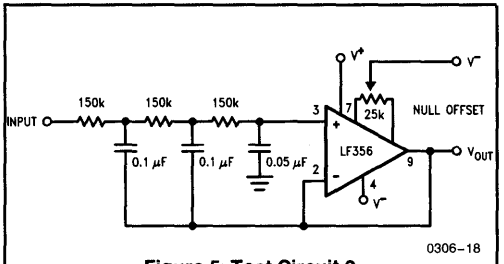


Figure 5: Test Circuit 2
DC to 10Hz Unity Gain Low Pass Filter

DETAILED DESCRIPTION

CAZ Instrumentation Amp Overview

The CAZ instrumentation amplifier operates on principles which are very different from those of the conventional three op-amp designs, which must use ultra-precise trimmed resistor networks in order to achieve acceptable accuracy. An important advantage of the ICL7605/ICL7606 CAZ instrumentation amp is the provision for self-compensation of internal error voltages, whether they are derived from steady-state conditions, such as temperature and supply voltage fluctuations, or are due to long term drift.

The CAZ instrumentation amplifier is constructed with monolithic CMOS technology, and consists of three distinct sections, two analog and one digital. The two analog sections — a differential to single-ended voltage converter, and a CAZ op amp — have on-chip analog switches to steer the input signal. The analog switches are driven from a self-contained digital section which consists of an RC oscillator, a programmable divider, and associated voltage translators. A functional layout of the ICL7605/ICL7606 is shown in Figure 6.

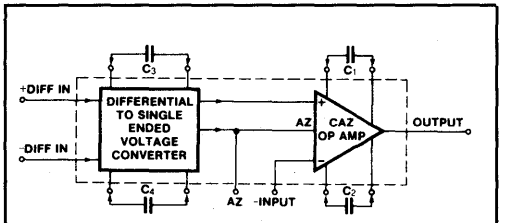


Figure 6: Simplified Block Diagram

The ICL7605/ICL7606 have approximately constant equivalent input noise voltage, CMRR, PSRR, input offset voltage and drift values independent of the gain configuration. By comparison, hybrid-type modules which use the traditional three op amp configuration have relatively poor performance at low gain (1 to 100) with improved performance above a gain of 100.

The only major limitation of the ICL7605/ICL7606 is its low-frequency operation (10 to 20Hz maximum). However in many applications bandwidth is not the most important parameter.

CAZ Op Amp Section

Operation of the CAZ op-amp section of the ICL7605/ICL7606 is best illustrated by referring to Figure 7. The basic amplifier configuration, represented by the large triangles, has one more input than does a regular op amp — the AZ, or auto-zero terminal. The voltage on the AZ input is that level at which each of the internal op amps will be auto-zeroed. In Mode A, op amp #2 is connected in a unity gain mode through on-chip analog switches. It charges external capacitor C_2 to a voltage equal to the DC input offset voltage of the amplifier plus the instantaneous low-frequency noise voltage. A short time later, the analog switches reconnect the on-chip op amps to the configuration shown in Mode B. In this mode, op amp #2 has capacitor C_2 (which is charged to a voltage equal to the offset and noise voltage of op amp #2) connected in series to its non-inverting (+) input in such a manner as to null out the input offset and noise voltages of the amplifier. While one of the on-chip op amps is processing the input signal, the second op amp is in an auto-zero mode, charging a capacitor to a voltage equal to its equivalent DC and low frequency error voltage. The on-chip amplifiers are connected and reconnected at a rate designated as the commutation frequency (f_{COM}), so that at all times one or the other of the on-chip op amps is processing the input signal, while the voltages on capacitors C_1 and C_2 are being updated to compensate for variables such as low frequency noise voltage and input offset voltage changes due to temperature, drift or supply voltages effects.

NOTE: All typical values have been characterized but are not tested.

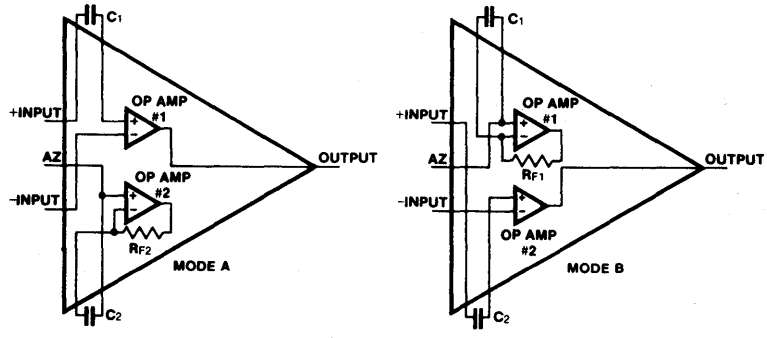


Figure 7: Diagrammatic representation of the 2 half cycles of operation of the CAZ OP AMP.

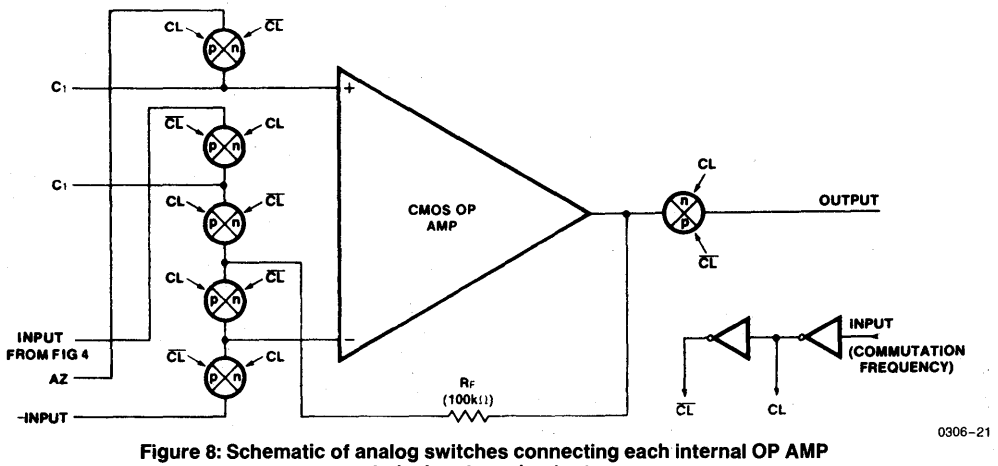


Figure 8: Schematic of analog switches connecting each internal OP AMP to its inputs and output.

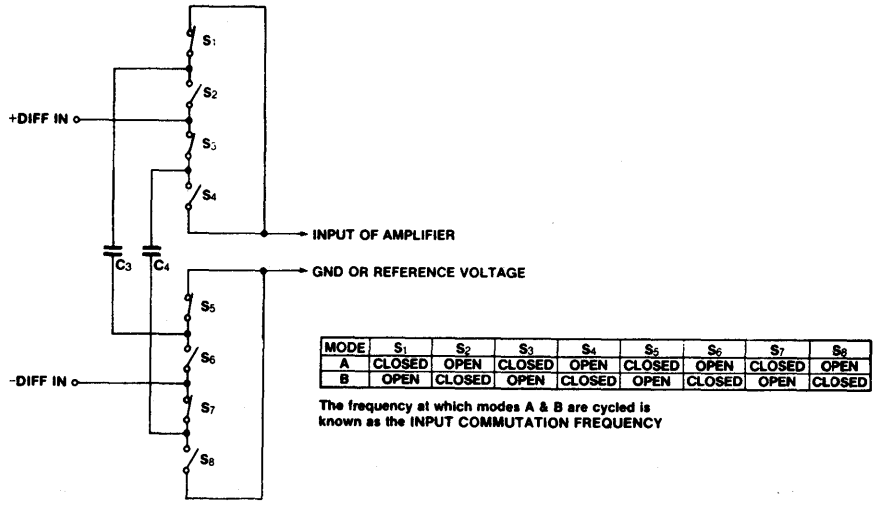
Compared to the standard bipolar or FET input op amps, the CAZ amp scheme demonstrates a number of important advantages:

* Effective input offset voltages can be reduced from 1000 to 10,000 times without trimming.
* Long-term offset voltage drift phenomena can be compensated and dramatically reduced.
* Thermal effects can be compensated for over a wide operating temperature range. Reductions can be as much as 100 times or better.
* Supply voltage sensitivity is reduced.

CMOS processing is ideally suited to implement the CAZ amp structure. The digital section is easily fabricated, and the transmission gates (analog switches) which connect the on-chip op amps can be constructed for minimum charge injection and the widest operating voltage range. The analog section, which includes the on-chip op amps, contributes performance figures which are similar to bipolar or FET input designs. The CMOS structure provides the CAZ op-amp with open-loop gains of greater than 100dB, typical input offset voltages of ±5mV, and ultra-low leakage currents, typically 1pA.

The CMOS transmission gates connect the on-chip op amps to external input and output terminals, as shown in Figure 8. Here, one op amp and its associated analog switches are required to connect each on-chip op amp, so that at any time three switches are open and three switches are closed. Each analog switch consists of a P-channel transistor in parallel with an N-channel transistor.

NOTE: All typical values have been characterized but are not tested.



MODE	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
A	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN
B	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED

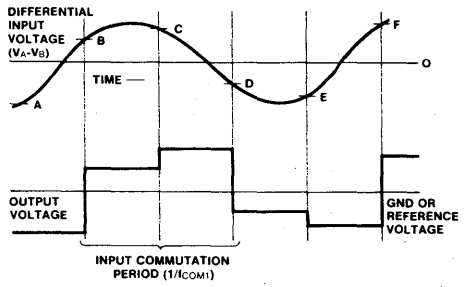
The frequency at which modes A & B are cycled is known as the INPUT COMMUTATION FREQUENCY

0306-22

Figure 9: Schematic of the differential to single ended voltage converter

DIFFERENTIAL-TO-SINGLE-ENDED UNITY GAIN VOLTAGE CONVERTER

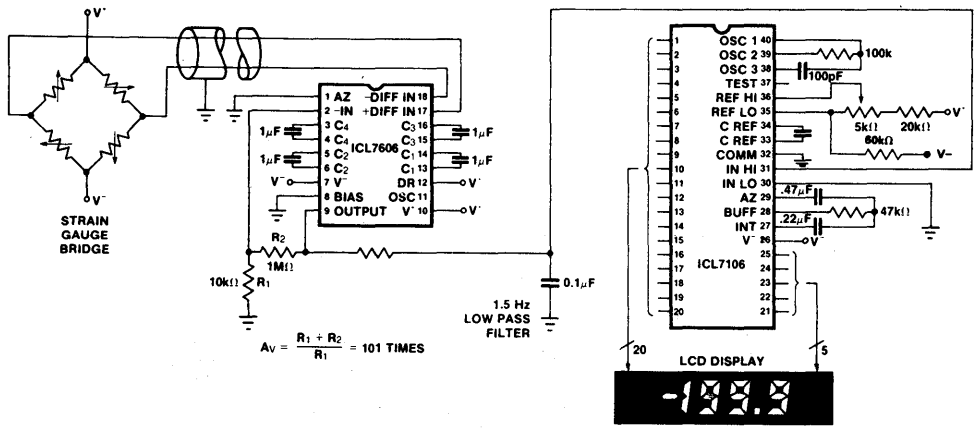
An idealized schematic of the voltage converter block is shown in Figure 9. The mode of operation is quite simple, involving two capacitors and eight switches. The switches are arranged so that four are open and four are closed. The four conducting switches connect one of the capacitors across the differential input, and the other from a ground or reference voltage to the input of the CAZ instrumentation amp. The output signal of this configuration is shown in Figure 10, where the voltage steps equal the differential voltage (V_A-V_B) at commutation times a, b, c, etc. The output waveform thus represents all information contained in the input signal from DC up to the commutation frequency, including commutation and noise voltages. Sampling theory states that to preserve the information to be processed, at least two samples must be taken within a period (1/f) of the highest frequency being sampled. Consequently this scheme preserves information up to the commutation frequency. Above the commutation frequency, the input signal is translated to a lower frequency. This phenomenon is known as aliasing. Although the output responds to inputs above the commutation frequency, the frequencies of the output responses will be below the commutation frequency.



0306-23

Figure 10: Input to Output Voltage waveforms from the differential to single ended voltage converter. For additional information, see frequency characteristics in Amplitude Response of the Input Differential to single ended voltage converter graph.

NOTE: All typical values have been characterized but are not tested.



0306-24

Figure 11: 3-½ Digit Digital Readout Torque Wrench

The voltage converter is fabricated with CMOS analog switches, which contain a parallel combination of P-channel and N-channel transistors. The switches have a finite ON impedances of 30kΩ, plus parasitic capacitances to the substrate. Because of the charge injection effects which appear at both the switches and the output of the voltage converter, the values of capacitors C_3 and C_4 must be about 1μF to preserve signal translation accuracies to 0.01%. The 1μF capacitors, coupled with the 30kΩ equivalent impedance of the switches, produce a low-pass filter response from the voltage converter which is down approximately 3dB at 10Hz.

APPLICATIONS

Using the ICL7605/ICL7606 to Build a Digital Readout Torque Wrench

A typical application for the ICL7605/ICL7606 is in a strain gauge system, such as the digital readout torque wrench circuit shown in Figure 6. In this application, the CAZ instrumentation amplifier is used as a preamplifier, taking the differential voltage of the bridge and converting it to a single-ended voltage referenced to ground. The signal is then amplified by the CAZ instrumentation amplifier and applied to the input of a 3-½ digit dual-slope A/D converter which drives the LCD panel meter display. The A/D converter device used in this instance is the Harris ICL7106.

In the digital readout torque wrench circuit, the reference voltage for the ICL7106 is derived from the stimulus applied to the strain gauge, to utilize the ratiometric capabilities of the A/D. In order to set the full-scale reading, a value of gain for the ICL7605/ICL7606 instrumentation CAZ amp must be selected along with an appropriate value for the reference voltage. The gain should be set so that at full scale, the output will swing about 0.5V. The reference voltage required is about one-half the maximum output swing, or approximately 0.25V.

In this type of system, only one adjustment is required. Either the amplifier gain or the reference voltage must be varied for full-scale adjustment. Total current consumption of all circuitry, less the current through the strain gauge bridge, is typically 2mA. The accuracy is limited only by resistor ratios and the transducer.

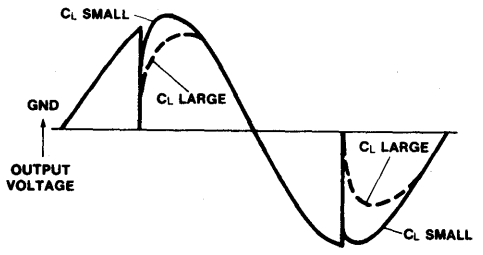
SOME HELPFUL HINTS

Testing the ICL7605/ICL7606 CAZ Instrumentation Amplifier

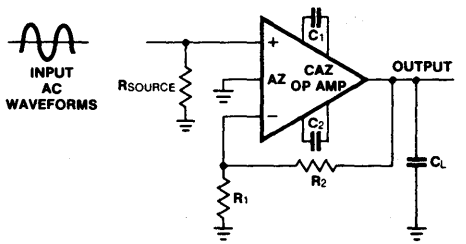
Figure 4 and 5 (Test Circuits) provide a convenient means of measuring most of the important electrical parameters of the CAZ instrumentation amp. The output signal can be viewed on an oscilloscope after being fed through a low-pass filter. It is recommended that for most applications, a low-pass filter of about 1.0 to 1.5Hz be used to reduce the peak-to-peak noise to about the same level as the input offset voltage.

The output low-pass filter must be a high-input impedance RC type — not simply a capacitor across the feedback resistor R_2. Resistor and capacitor values of about 100kΩ and 1.0μF are necessary so that the output load impedance on the CAZ op-amp is greater than 100kΩ.

NOTE: All typical values have been characterized but are not tested.



0306-25



0306-26

Figure 12: Effect of a load capacitor on output voltage waveforms.

Bias Control

The on-chip op amps consume over 90% of the power required by the ICL7605/ICL7606. For this reason, the internal op amps have externally programmable bias levels. These levels are set by connecting the BIAS terminal to either V^+, GND, or V^-, for LOW, MED or HIGH BIAS levels, respectively. The difference between each bias setting is about a factor of 3, allowing a 9:1 ratio of quiescent supply current versus bias setting. This current programmability provides the user with a choice of device power dissipation levels, slew rates (the higher the slew rate, the better the recovery from commutation spikes), and offset errors due to "IR" voltage drops and thermoelectric effects (the higher the power dissipation, the higher the input offset error). In most cases, the medium bias (MED BIAS) setting will be found to be the best choice.

Output Loading (Resistive)

With a 10kΩ load, the output voltage swing can vary across nearly the entire supply voltage range, and the device can be used with loads as low as 2kΩ.

However, with loads of less than 50kΩ, the on-chip op amps will begin to exhibit the characteristics of transconductance amplifiers, since their respective output impedances are nearly 50kΩ each. Thus the open-loop gain is 20dB less with a 2kΩ load than it would be with a 20kΩ load. Therefore, for high gain configurations requiring high accuracy, an output load of 100kΩ or more is suggested.

There is another consideration in applying the CAZ instrumentation op amps which must not be overlooked. This is the additional power dissipation of the chip which will result from a large output voltage swing into a low resistance load. This added power dissipation can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output of the CAZ instrumentation op amp to reduce high-frequency noise outside the desired signal passband. An obvious solution when using a conventional op amp would be to place a capacitor across the external feedback resistor and thus produce a low-pass filter.

However, with the CAZ op amp concept this is not possible because of the nature of the commutation spikes. These voltage spikes exhibit a low-impedance characteristic in the direction of the auto-zero voltage and a high-impedance characteristic on the recovery edge, as shown in Figure 12. It can be seen that the effect of a large load capacitor produces an area error in the output waveform, and hence an effective gain error. The output low-pass filter must be of a high-impedance type to avoid these area errors. For example, a 1.5Hz filter will require a 100kΩ resistor and a 1.0μF capacitor, or a 1MΩ resistor and a 0.1μF capacitor.

Oscillator and Digital Circuitry Considerations

The oscillator has been designed to run free at about 5.2kHz when the OSC terminal is open circuit. If the full divider network is used, this will result in a nominal commutation frequency of approximately 160Hz. The commutation frequency is that frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160Hz commutation frequency represents the best compromise between input offset voltage and low frequency noise. Other commutation frequencies may provide optimization of some parameters, but always at the expense of others.

The oscillator has a very high output impedance, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the natural oscillator frequency is desired (5.2kHz) the terminal remains open circuit. In other instances, it may be desirable to synchronize the oscillator with an external clock source, or to run it at another frequency. The ICL7605/ICL7606 CAZ amp provides two degrees of flexibility in this respect. First, the DR (division ratio) terminal allows a choice of either dividing the oscillator by 32 (DR terminal to V^+) or by 2 (DR terminal to GND) to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and the V^+ or system GND terminals. For situations which require that the commutation frequency be synchronized with a master clock, (Figure 13) the OSC terminal may be driven from TTL logic (with resistive pull-up) or by CMOS logic, provided that the V^+ supply is +5V (±10%) and the logic driver also operates from a similar voltage supply. The reason for this requirement is that the logic section (including the oscillator) operates from an internal −5V supply, referenced to V^+ supply, which is not accessible externally.

NOTE: All typical values have been characterized but are not tested.

Thermoelectric Effects

The ultimate limitations to ultra-high-sensitivity DC amplifiers are due to thermoelectric, Peltier, or thermocouple effects in electrical junctions consisting of various metals (alloys, silicon, etc.) Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about 0.1μV/°C. However, these voltages can be several tens of microvolts per °C for certain thermocouple materials.

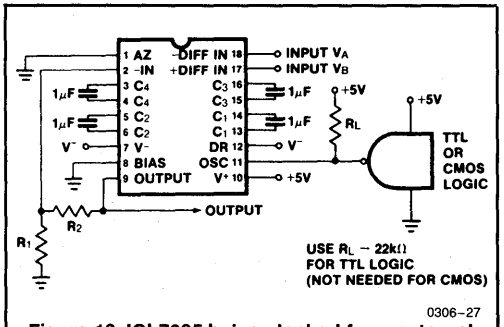


Figure 13: ICL7605 being clocked from external logic into the oscillator terminal.

In order to realize the extremely low offset voltages which the CAZ op amp can produce, it is necessary to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. In addition, the supply voltages and power dissipation should be kept to a minimum by use of the MED BIAS setting. Employ a high impedance load and keep the ICL7605/ICL7606 away from equipment which dissipates heat.

Component Selection

The four capacitors (C_1 thru C_4) should each be about 1.0μF. These are relatively large values for non-electrolytic capacitors, but since the voltages stored on them change significantly, problems of dielectric absorption, charge bleed-off and the like are as significant as they would be for integrating dual-slope A/D converter applications. Polypropylene types are the best for C_3 and C_4, although Mylar may be adequate for C_1 and C_2.

Excellent results have been obtained for commercial temperature ranges using several of the less-expensive, smaller-size capacitors, since the absolute values of the capacitors are not critical. Even polarized electrolytic capacitors rated at 1.0μF and 50V have been used successfully at room temperature, although no recommendations are made concerning the use of such capacitors.

Commutation Voltage Transient Effects

Although in most respects the CAZ instrumentation amplifier resembles a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 10Hz. The is due to the finite switching transients which occur at both the input and output terminals because of commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and including all of the higher harmonics of the commutation frequency. Assuming that the commutation frequency is higher than the highest in-band frequency, then the commutation transients can be filtered out with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage which is equal to the input offset voltages (about 5-10mV), usually occurring during the transition between the signal processing mode and the auto-zero mode. Since the input capacitances of the on-chip op-amps are typically in the 10pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must have values of at least 10,000×10pF, or 0.1μF each.

The charge that is injected into the input of each op amp when being switched into the signal processing mode produces a rapidly-decaying voltage spike at the input, plus an equivalent DC input bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically 1.0pA at an ambient temperature of 25°C.

The output waveform in Figure 4 (with no input signal) is shown in Figure 14. Note that the equivalent noise voltage is amplified 1000 times, and that due to the slew rate of the on-chip op amps, the input transients of approximately 7mV are amplified by a factor of less than 1000.

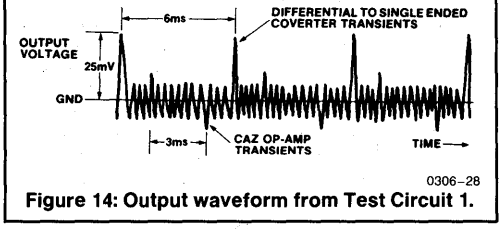


Figure 14: Output waveform from Test Circuit 1.

Layout Considerations

Care should be exercised in positioning components on the PC board particularly the capacitors C_1, C_2, C_3 and C_4, which must all be shielded from the OSC terminal. Also, parasitic PC board leakage capacitances associated with these four capacitors should be kept as low as possible to minimize charge injection effects.

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICL76XX

ICL76XX Series Low Power CMOS Operational Amplifiers

GENERAL DESCRIPTION

The ICL761X/762X/763X/764X series is a family of monolithic CMOS operational amplifiers. These devices provide the designer with high performance operation at low supply voltages and selectable quiescent currents, and are an ideal design tool when ultra low input current and low power dissipation are desired.

The basic amplifier will operate at supply voltages ranging from ±1V to ±8V, and may be operated from a single Lithium cell.

A unique quiescent current programming pin allows setting of standby current to 1mA, 100μA, or 10μA, with no external components. This results in power consumption as low as 20μW. Output swings range to within a few millivolts of the supply voltages.

Of particular significance is the extremely low (1pA) input current, input noise current of .01pA/$\sqrt{Hz}$, and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

The inputs are internally protected. Outputs are fully protected against short circuits to ground or to either supply.

AC performance is excellent, with a slew rate of 1.6V/μs, and unity gain bandwidth of 1MHz at I_Q = 1mA.

Because of the low power dissipation, operating temperatures and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

FEATURES

- **Wide Operating Voltage Range ±1V to ±8V**
- **High Input Impedance — $10^{12}\Omega$**
- **Programmable Power Consumption — Low As 20μW**
- **Input Current Lower Than BIFETs — Typ 1pA**
- **Available As Singles, Duals, Triples, and Quads**
- **Output Voltage Swings to Within Millivolts Of V^- and V^+**
- **Low Power Replacement for Many Standard Op Amps**
- **Compensated and Uncompensated Versions**
- **Input Common Mode Voltage Range Greater Than Supply Rails (ICL7612)**

APPLICATIONS

- **Portable Instruments**
- **Telephone Headsets**
- **Hearing Aid/Microphone Amplifiers**
- **Meter Amplifiers**
- **Medical Instruments**
- **High Impedance Buffers**

3 OPERATIONAL AMPLIFIERS

SELECTION GUIDE

DEVICE NOMENCLATURE

ICL76XX X X XX

- XX — Package Code
  - TV — TO-99, 8 pin
  - PA — Plastic 8 pin Minidip
  - PD — 14 pin Plastic Dip
  - PE — 16 pin Plastic Dip
  - BA — 8 pin SOIC
- X — Temperature Range
  - C = 0°C to 70°C
  - M = −55°C to +125°C
- X — V_{OS} Selection
  - A = 2mV
  - B = 5mV
  - C = 10mV
  - D = 15mV
  - E = 20mV

SPECIAL FEATURE CODES

C	=	INTERNALLY COMPENSATED
H	=	HIGH QUIESCENT CURRENT (1mA)
L	=	LOW QUIESCENT CURRENT (10μA)
M	=	MEDIUM QUIESCENT CURRENT (100μA)
O	=	OFFSET NULL CAPABILITY
P	=	PROGRAMMABLE QUIESCENT CURRENT
V	=	EXTENDED CMVR

302060-003

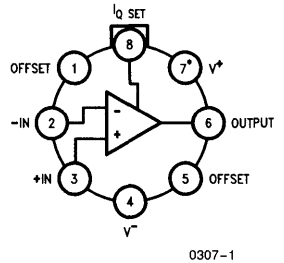
NOTE: All typical values have been characterized but are not tested.

ORDERING INFORMATION

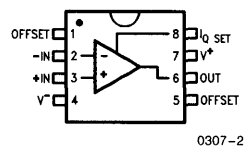
Basic Part Number	Number of OP-AMPS in Package, and Special Features (SEE CODES)	Package Type and Suffix				
		8-Lead TO-99		8-Pin MINIDIP	8-Pin SOIC	Plastic DIP (1)
		0°C to +70°C	−55°C to +125°C	0°C to +70°C	0°C to +70°C	0°C to +70°C
ICL7611 ICL7612	SINGLE OP-AMP: C, O, P C, O, P, V	ACTV BCTV DCTV	AMTV BMTV DMTV	ACPA BCPA DCPA	DCBA-T DCBA	
ICL7621	DUAL OP-AMP: C, M	ACTV BCTV DCTV	AMTV BMTV DMTV	ACPA BCPA DCPA	DCBA DCBA-T	
ICL7631	TRIPLE OP-AMP: C, P					CCPE ECPE
ICL7641 ICL7642	QUAD OP-AMP: C, H C, L					CCPD ECPD

NOTES: 1. Duals and quads are available in 14 pin DIP package, triples in 16 pin only.
2. Ordering code must consist of basic part number and package suffix, e.g., ICL7611BCPA.

Device	Description	Pin Assignments
ICL7611XCPA ICL7611XCTV ICL7611XMTV ICL7611XCBA ICL7612XCPA ICL7612XCTV ICL7612XMTV ICL7612XCBA	Internal compensation, plus offset null capability and external I_Q control	TO-99 (TOP VIEW) (outline dwg TV) 8 PIN DIP (TOP VIEW) (outline dwg PA) 8 PIN DIP (TOP VIEW) (outline dwg BA)



*Pin 7 connected to case.



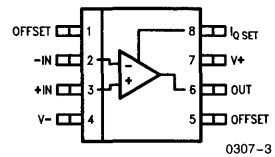


Figure 1: Pin Configurations

NOTE: All typical values have been characterized but are not tested.

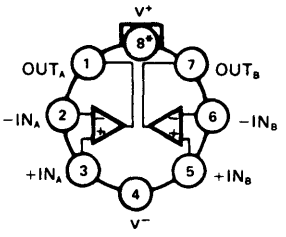
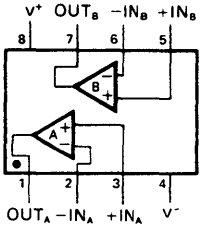
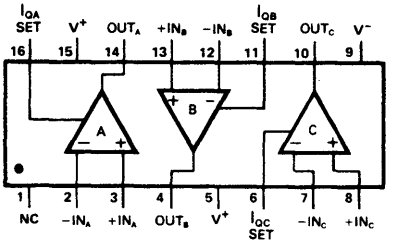
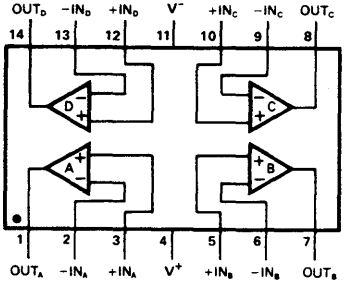
Device	Description	Pin Assignments
ICL7621XCPA ICL7621XCTV ICL7621XMTV ICL7621XCBA	Dual op amps with internal compensation; I_Q fixed at 100μA Pin compatible with Texas Inst. TL082 Motorola MC1458 Raytheon RC4558	TO-99 (TOP VIEW) (outline dwg TV)  0307-6 *Pin 8 connected to case. * PIN DIP (TOP VIEW) (outline dwg PA)  0307-7
ICL7631XCPE	Triple op amps with internal compensation. Adjustable I_Q Same pin configuration as ICL8023.	16 PIN DIP (TOP VIEW) (outline dwg PE)  0307-9 Note: pins 5 and 15 are internally connected.
ICL7641XCPD ICL7642XCPD	Quad op amps with internal compensation. I_Q fixed at 1mA (ICL7641) I_Q fixed at 10μA (ICL7642) Pin compatible with Texas Instr. TL084 National LM324 Harris HA4741	14 PIN DIP (TOP VIEW) (outline dwg PD)  0307-10

Figure 1: Pin Configurations (Cont.)

3 OPERATIONAL AMPLIFIERS

NOTE: All typical values have been characterized but are not tested.

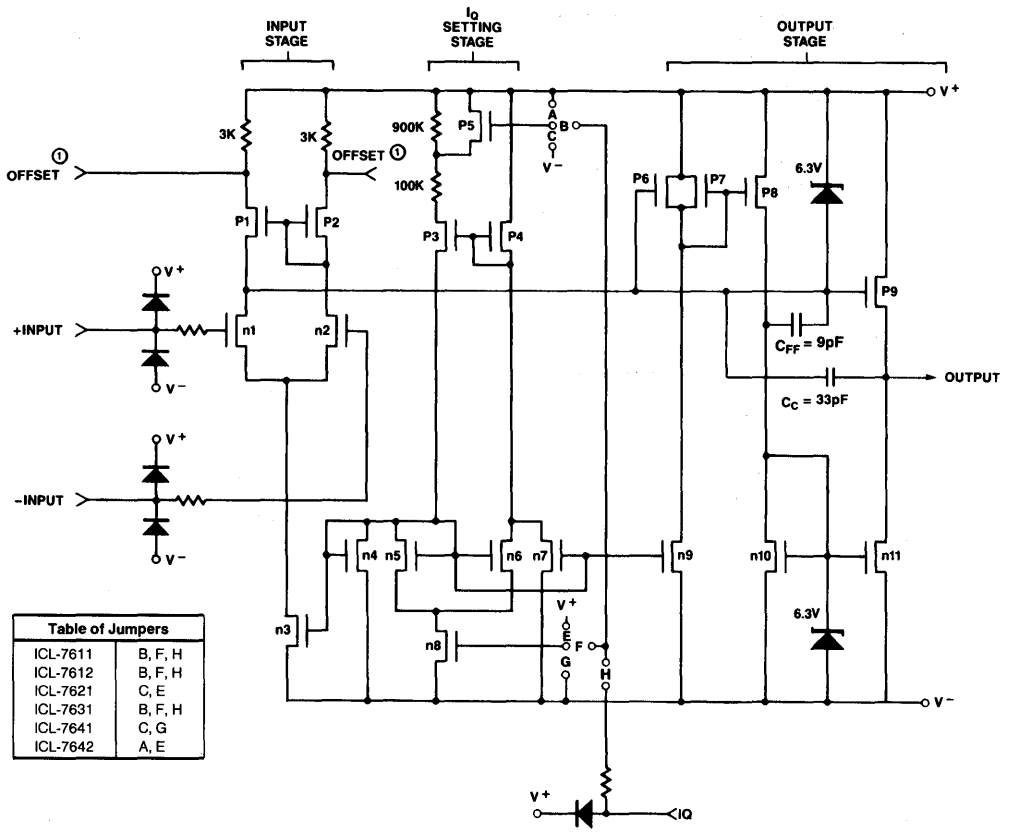


Table of Jumpers	
ICL-7611	B, F, H
ICL-7612	B, F, H
ICL-7621	C, E
ICL-7631	B, F, H
ICL-7641	C, G
ICL-7642	A, E

NOTE 1: Offset nulling pins are not available on the dual (ICL-7621), triple (ICL-7631), and quad (ICL-764X) versions.

Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage V^+ to V^- 18V
Input Voltage ..... V^- −0.3 to V^+ +0.3V
Differential Input Voltage[1] . ±[(V^+ +0.3)−(V^- −0.3)]V
Duration of Output Short Circuit[2] ..... Unlimited

Continuous Power Dissipation

	@25°C	Above 25°C derate as below:
TO-99	250mW	2mW/°C
8 Lead Minidip	250mW	2mW/°C
14 Lead Plastic	375mW	3mW/°C
14 Lead Cerdip	500mW	4mW/°C
16 Lead Plastic	375mW	3mW/°C
16 Lead Cerdip	500mW	4mW/°C

Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range
ICL76XXM ..... −55°C to +125°C
ICL76XXC ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE 1. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
2. The outputs may be shorted to ground or to either supply. for $V_{SUPP} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS (7611/12 and 7621 ONLY)

($V_{SUPPLY} = \pm 5.0V$, $T_A = 25°C$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	76XXA			76XXB			76XXD			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S \leq 100k\Omega$, $T_A = 25°C$ $T_{MIN} \leq T_A \leq T_{MAX}$			2 3			5 7			15 20	mV
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}	$R_S \leq 100k\Omega$		10			15			25		µV/°C
I_{OS}	Input Offset Current	$T_A = 25°C$ $\Delta T_A = C_{(2)}$ $\Delta T_A = M_{(2)}$		0.5	30 300 800		0.5	30 300 800		0.5	30 300 800	pA
I_{BIAS}	Input Bias Current	$T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$		1.0	50 400 4000		1.0	50 400 4000		1.0	50 400 4000	pA
V_{CMR}	Common Mode Voltage Range (Except ICL7612)	$I_Q = 10\mu A$(1) $I_Q = 100\mu A$ $I_Q = 1mA$(1)	±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			V
V_{CMR}	Extended Common Mode Voltage Range (ICL7612 Only)	$I_Q = 10\mu A$	±5.3			±5.3			±5.3			V
		$I_Q = 100\mu A$	+5.3 −5.1			+5.3 −5.1			+5.3 −5.1			
		$I_Q = 1mA$	+5.3 −4.5			+5.3 −4.5			+5.3 −4.5			
V_{OUT}	Output Voltage Swing	(1) $I_Q = 10\mu A$, $R_L = 1M\Omega$ $T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$	 ±4.9 ±4.8 ±4.7			 ±4.9 ±4.8 ±4.7			 ±4.9 ±4.8 ±4.7			V
		$I_Q = 100\mu A$, $R_L = 100k\Omega$ $T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$	 ±4.9 ±4.8 ±4.5			 ±4.9 ±4.8 ±4.5			 ±4.9 ±4.8 ±4.5			
		(1) $I_Q = 1mA$, $R_L = 10k\Omega$ $T_A = 25°C$ $\Delta T_A = C$ $\Delta T_A = M$	 ±4.5 ±4.3 ±4.0			 ±4.5 ±4.3 ±4.0			 ±4.5 ±4.3 ±4.0			

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (7611/12 and 7621 ONLY) (Continued)

(V_{SUPPLY} = ±5.0V, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	76XXA			76XXB			76XXD			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
A_{VOL}	Large Signal Voltage Gain	V_O = ±4.0V, R_L = 1MΩ										
		I_Q = 10μA(1), T_A = 25°C	86	104		80	104		80	104		
		ΔT_A = C	80			75			75			
		ΔT_A = M	74			68			68			
		V_O = ±4.0V, R_L = 100kΩ										
		I_Q = 100μA, T_A = 25°C	86	102		80	102		80	102		
		ΔT_A = C	80			75			75			dB
		ΔT_A = M	74			68			68			
		V_O = ±4.0V, R_L = 10kΩ										
		I_Q = 1mA(1), T_A = 25°C	80	83		76	83		76	83		
		ΔT_A = C	76			72			72			
		ΔT_A = M	72			68			68			
GBW	Unity Gain Bandwidth	I_Q = 10μA(1)		0.044			0.044			0.044		MHz
		I_Q = 100μA		0.48			0.48			0.48		
		I_Q = 1mA(1)		1.4			1.4			1.4		
R_{IN}	Input Resistance			10^{12}			10^{12}			10^{12}		Ω
CMRR	Common Mode Rejection Ratio	R_S ≤ 100kΩ, I_Q = 10μA(1)	76	96		70	96		70	96		
		R_S ≤ 100kΩ, I_Q = 100μA	76	91		70	91		70	91		dB
		R_S ≤ 100kΩ, I_Q = 1mA(1)	66	87		60	87		60	87		
PSRR	Power Supply Rejection Ratio	R_S ≤ 100kΩ, I_Q = 10μA(1)	80	94		80	94		80	94		
	V_{SUPPLY} = ±8V to ±2V	R_S ≤ 100kΩ, I_Q = 100μA	80	86		80	86		80	86		dB
		R_S ≤ 100kΩ, I_Q = 1mA(1)	70	77		70	77		70	77		
e_n	Input Referred Noise Voltage	R_S = 100Ω, f = 1kHz		100			100			100		nV/√Hz
i_n	Input Referred Noise Current	R_S = 100Ω, f = 1kHz		0.01			0.01			0.01		pA/√Hz
I_{SUPPLY}	Supply Current	No Signal, No Load										
	(Per Amplifier)	I_Q SET = +5V(1) Low Bias		0.01	0.02		0.01	0.02		0.01	0.02	
		I_Q SET = 0V Medium Bias		0.1	0.25		0.1	0.25		0.1	0.25	mA
		I_Q SET = −5V(1) High Bias		1.0	2.5		1.0	2.5		1.0	2.5	
V_{O1}/V_{O2}	Channel Separation	A_V = 100		120			120			120		dB
SR	Slew Rate(3)	A_V = 1, C_L = 100pF										
		V_{IN} = 8Vp-p										
		I_Q = 10μA(1), R_L = 1MΩ		0.016			0.016			0.016		V/μs
		I_Q = 100μA, R_L = 100kΩ		0.16			0.16			0.16		
		I_Q = 1mA(1), R_L = 10kΩ		1.6			1.6			1.6		
t_r	Rise Time(3)	V_{IN} = 50mV, C_L = 100pF										
		I_Q = 10μA(1), R_L = 1MΩ		20			20			20		μs
		I_Q = 100μA, R_L = 100kΩ		2			2			2		
		I_Q = 1mA(1), R_L = 10kΩ		0.9			0.9			0.9		
	Overshoot Factor(3)	V_{IN} = 50mV, C_L = 100pF										
		I_Q = 10μA1, R_L = 1MΩ		5			5			5		
		I_Q = 100μA, R_L = 100kΩ		10			10			10		%
		I_Q = 1mA1, R_L = 10kΩ		40			40			40		

NOTES: 1. ICL7611, 7612 only.

2. C = Commercial Temperature Range: 0°C to +70°C
M = Military Temperature Range: −55°C to +125°C

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (7611/12 A AND B GRADES ONLY)

($V_{SUPPLY} = \pm 1.0V$, $I_Q = 10\mu A$, $T_A = 25°C$, unless otherwise specified.)

Symbol	Parameter	Test Conditions	76XXA			76XXB			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S \leq 100k\Omega$, $T_A = 25°C$ $T_{MIN} \leq T_A \leq T_{MAX}$			2 3			5 7	mV
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}	$R_S \leq 100k\Omega$		10			15		$\mu V/°C$
I_{OS}	Input Offset Current	$T_A = 25°C$ $\Delta T_A = C$		0.5	30 300		0.5	30 300	pA
I_{BIAS}	Input Bias Current	$T_A = 25°C$ $\Delta T_A = C$		1.0	50 500		1.0	50 500	pA
V_{CMR}	Common Mode Voltage Range (Except ICL7612)		± 0.6			± 0.6			V
V_{CMR}	Extended Common Mode Voltage Range (ICL7612 Only)		$+0.6$ to -1.1			$+0.6$ to -1.1			V
V_{OUT}	Output Voltage Swing	$R_L = 1M\Omega$, $T_A = 25°C$ $\Delta T_A = C$		± 0.98 ± 0.96			± 0.98 ± 0.96		V
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 0.1V$, $R_L = 1M\Omega$ $T_A = 25°C$ $\Delta T_A = C$		90 80			90 80		dB
GBW	Unity Gain Bandwidth			0.044					MHz
R_{IN}	Input Resistance			10^{12}			10^{12}		
CMRR	Common Mode Rejection Ratio	$R_S \leq 100k\Omega$		80			80		
PSRR	Power Supply Rejection Ratio	$R_S \leq 100k\Omega$		80			80		dB
e_n	Input Referred Noise Voltage	$R_S = 100\Omega$, f = 1kHz		100			100		$nV/\sqrt{Hz}$
i_n	Input Referred Noise Current	$R_S = 100\Omega$, f = 1kHz		0.01			0.01		$pA/\sqrt{Hz}$
I_{SUPPLY}	Supply Current (Per Amplifier)	No Signal, No Load		6	15		6	15	μA
SR	Slew Rate	$A_V = 1$, $C_L = 100pF$ $V_{IN} = 0.2Vp\text{-}p$ $R_L = 1M\Omega$		0.016			0.016		$V/\mu s$
t_r	Rise Time	$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		20			20		μs
	Overshoot Factor	$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		5			5		%

NOTE: C = Commercial Temperature Range (0°C to +70°C) M = Military Temperature Range (−55°C to +125°C).

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (7631, 7641/42 ONLY)

(V_{SUPPLY} = ±5.0V, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	76XXC (6)			76XXE (6)			Units
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S \leq 100k\Omega$, T_A = 25°C $T_{MIN} \leq T_A \leq T_{MAX}$			10 15			20 25	mV
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}	$R_S \leq 100k\Omega$ (Note 5)		20			30		
I_{OS}	Input Offset Current	T_A = 25°C ΔT_A = C ΔT_A = M		0.5	30 300 800		0.5	30 300 800	pA
I_{BIAS}	Input Bias Current	T_A = 25°C ΔT_A = C ΔT_A = M		1.0	50 500 4000		1.0	50 500 4000	pA
V_{CMR}	Common Mode Voltage Range	I_Q = 10μA(1) I_Q = 100μA(3) I_Q = 1mA(2)	±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			V
V_{OUT}	Output Voltage Swing	I_Q = 10μA(1), R_L = 1MΩ T_A = 25°C ΔT_A = C ΔT_A = M	 ±4.9 ±4.8 ±4.7			 ±4.9 ±4.8 ±4.7			V
		I_Q = 100μA(3), R_L = 100kΩ T_A = 25°C ΔT_A = C ΔT_A = M	 ±4.9 ±4.8 ±4.5			 ±4.9 ±4.8 ±4.5			V
		I_Q = 1mA(2), R_L = 10kΩ T_A = 25°C ΔT_A = C ΔT_A = M	 ±4.5 ±4.3 ±4.0			 ±4.5 ±4.3 ±4.0			
A_{VOL}	Large Signal Voltage Gain	V_O = ±4.0V, R_L = 1MΩ(1) I_Q = 10μA(1), T_A = 25°C ΔT_A = C ΔT_A = M	 80 75 68	104		 80 75 68	104		dB
		V_O = ±4.0V, R_L = 100kΩ(3) I_Q = 100μA(3), T_A = 25°C ΔT_A = C ΔT_A = M	 80 75 68	102		 80 75 68	102		
		V_Q = ±4.0V, R_L = 10kΩ(2) I_Q = 1mA(2), T_A = 25°C ΔT_A = C ΔT_A = M	 76 72 68	98		 76 72 68	98		
GBW	Unity Gain Bandwidth	I_Q = 10μA(1) I_Q = 100μA(3) I_Q = 1mA(2)		0.044 0.48 1.4			0.044 0.48 1.4		MHz
R_{IN}	Input Resistance			10^{12}			10^{12}		Ω
CMRR	Common Mode Rejection Ratio	$R_S \leq 100k\Omega$, I_Q = 10μA(1) $R_S \leq 100k\Omega$, I_Q = 100μA $R_S \leq 100k\Omega$, I_Q = 1mA(2)	70 70 60	96 91 87		70 70 60	96 91 87		dB

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (7631, 7641/42 ONLY) (Continued)

(V_{SUPPLY} = ±5.0V, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	76XXC (6)			76XXE (6)			Units
			Min	Typ	Max	Min	Typ	Max	
PSRR	Power Supply Rejection Ratio V_{SUPPLY} = ±8V to ±2V	$R_S \leq 100k\Omega$, $I_Q = 10\mu A$(1) $R_S \leq 100k\Omega$, $I_Q = 100\mu A$ $R_S \leq 100k\Omega$, $I_Q = 1mA$(2)	80 80 70	94 86 77		80 80 70	94 86 77		dB
e_n	Input Referred Noise Voltage	$R_S = 100\Omega$, f = 1kHz		100			100		nV/$\sqrt{Hz}$
I_n	Input Referred Noise Current	$R_S = 100\Omega$, f = 1kHz		0.01			0.01		pA/$\sqrt{Hz}$
I_{SUPPLY}	Supply Current (Per Amplifier)	No Signal, No Load 7642 ONLY $I_Q = 10\mu A$(1) Low Bias $I_Q = 100\mu A$ Medium Bias $I_Q = 1mA$(2) High Bias		0.01 0.01 0.1 1.0	0.03 0.022 0.25 2.5		0.01 0.01 0.1 1.0	0.03 0.022 0.25 2.5	mA
V_{O1}/V_{O2}	Channel Separation	$A_V = 100$		120			120		dB
SR	Slew Rate	$A_V = 1$, $C_L = 100pF$ $V_{IN} = 8Vp\text{-}p$ $I_Q = 10\mu A$(1), $R_L = 1M\Omega$ $I_Q = 100\mu A$, $R_L = 100k\Omega$ $I_Q = 1mA$(2), $R_L = 10k\Omega$		 0.016 0.16 1.6			 0.016 0.16 1.6		V/μs
t_r	Rise Time	$V_{IN} = 50mV$, $C_L = 100pF$ $I_Q = 10\mu A$(1), $R_L = 1M\Omega$ $I_Q = 100\mu A$, $R_L = 100k\Omega$ $I_Q = 1mA$(2), $R_L = 10k\Omega$		 20 2 0.9			 20 2 0.9		μs
	Overshoot Factor	$V_{IN} = 50mV$, $C_L = 100pF$ $I_Q = 10\mu A$(1), $R_L = 1M\Omega$ $I_Q = 100\mu A$, $R_L = 100k\Omega$ $I_Q = 1mA$(2), $R_L = 10k\Omega$		 5 10 40			 5 10 40		%

NOTES: **1.** Does not apply to 7641.
2. Does not apply to 7642.
3. ICL7631 only.

For Test Conditions:
C = Commercial Temperature Range: 0°C to +70°C
M = Military Temperature Range: −55°C to +125°C

ELECTRICAL CHARACTERISTICS (7631 AND 7642 ONLY)

(V_{SUPPLY} = ±1.0V, I_Q = 10μA, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	76XXC			Units
			Min	Typ	Max	
V_{OS}	Input Offset Voltage	$R_S \leq 100k\Omega$, T_A = 25°C $T_{MIN} \leq T_A \leq T_{MAX}$			10 12	mV
$\Delta V_{OS}/\Delta T$	Temperature Coefficient of V_{OS}	$R_S \leq 100k\Omega$		20		μV/°C
I_{OS}	Input Offset Current	T_A = 25°C ΔT_A = C		0.5	30 300	pA
I_{BIAS}	Input Bias Current	T_A = 25°C ΔT_A = C		1.0	50 500	pA
V_{CMR}	Common Mode Voltage Range		±0.6			V

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (7631 AND 7642 ONLY) (Continued)

($V_{SUPPLY} = \pm 1.0V$, $I_Q = 10\mu A$, $T_A = 25°C$, unless otherwise specified.)

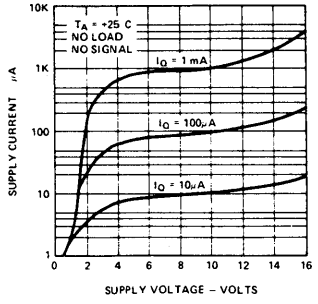
Symbol	Parameter	Test Conditions	76XXC			Units
			Min	Typ	Max	
V_{OUT}	Output Voltage Swing	$R_L = 1M\Omega$, $T_A = 25°C$ $\Delta T_A = C$		± 0.98 ± 0.96		V
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 0.1V$, $R_L = 1M\Omega$ $T_A = 25°C$ $\Delta T_A = C$		 90 80		dB
GBW	Unity Gain Bandwidth			0.044		MHz
R_{IN}	Input Resistance			10^{12}		Ω
CMRR	Common Mode Rejection Ratio	$R_S \leq 100k\Omega$		80		dB
PSRR	Power Supply Rejection Ratio			80		dB
e_n	Input Referred Noise Voltage	$R_S = 100\Omega$, f = 1kHz		100		$nV/\sqrt{Hz}$
i_n	Input Referred Noise Current	$R_S = 100\Omega$, f = 1kHz		0.01		$pA/\sqrt{Hz}$
I_{SUPPLY}	Supply Current (Per Amplifier)	No Signal, No Load		6	15	μA
$V_{O1/VO2}$	Channel Separation	$A_V = 100$		120		dB
SR	Slew Rate	$A_V = 1$, $C_L = 100pF$ $V_{IN} = 0.2Vp\text{-}p$ $R_L = 1M\Omega$		0.016		$V/\mu s$
t_r	Rise Time	$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		20		μs
	Overshoot Factor	$V_{IN} = 50mV$, $C_L = 100pF$ $R_L = 1M\Omega$		5		%

NOTE: C = Commercial Temperature Range (0°C to +70°C)

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF SUPPLY VOLTAGE



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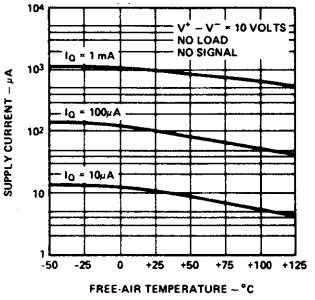
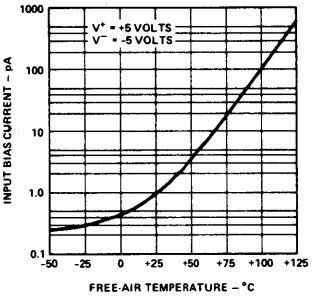
SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF FREE-AIR TEMPERATURE



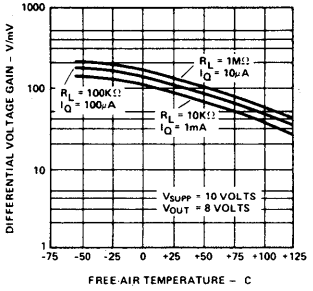
0307-13

INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE



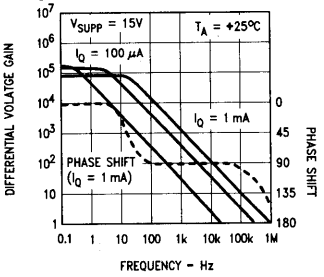
0307-14

LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF FREE-AIR TEMPERATURE



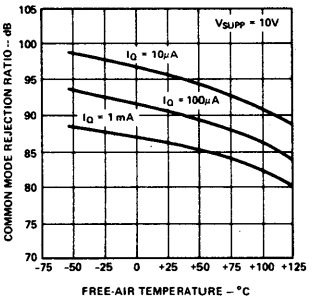
0307-15

LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AND PHASE SHIFT AS A FUNCTION OF FREQUENCY



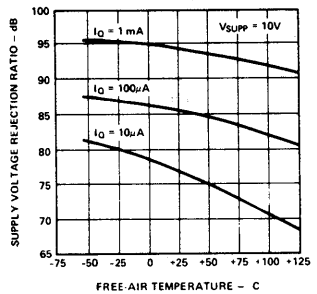
0307-16

COMMON MODE REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



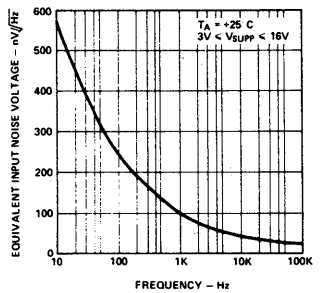
0307-17

POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE



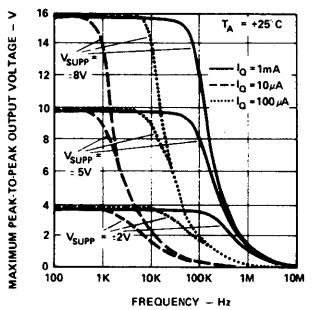
0307-18

EQUIVALENT INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



0307-19

PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY

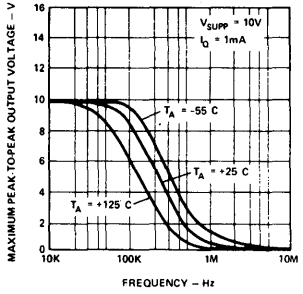


0307-20

NOTE: All typical values have been characterized but are not tested.

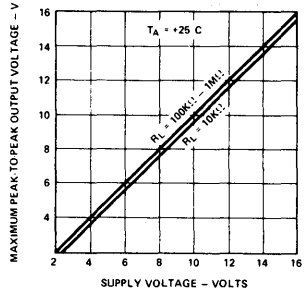
TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY



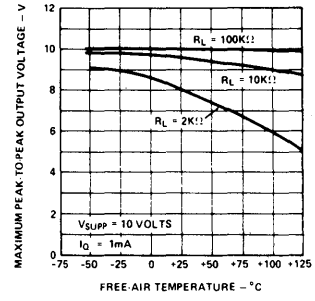
0307-21

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE



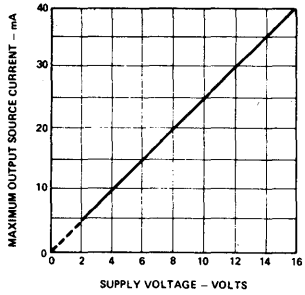
0307-22

MAXIMUM PEAK-TO-PEAK VOLTAGE AS A FUNCTION OF FREE-AIR TEMPERATURE



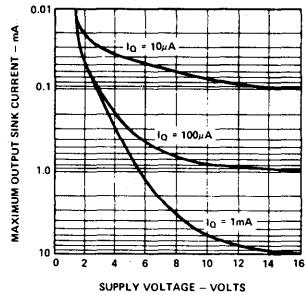
0307-23

MAXIMUM OUTPUT SOURCE CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



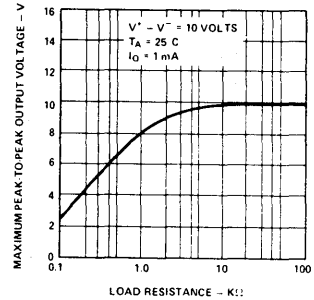
0307-24

MAXIMUM OUTPUT SINK CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



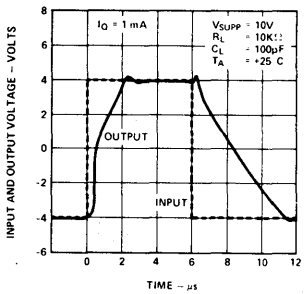
0307-25

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE



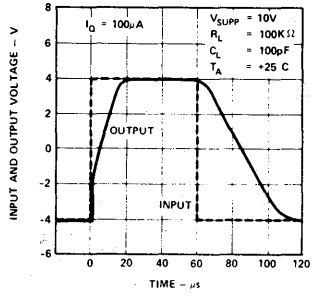
0307-26

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



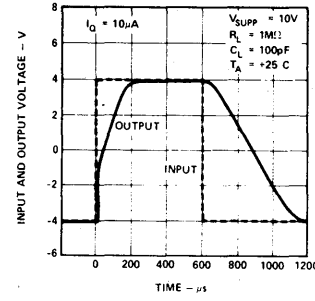
0307-27

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



0307-28

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



0307-29

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

Static Protection

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

Latchup Avoidance

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. In general, the op-amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2mA to prevent latchup.

Choosing the Proper I_Q

Each device in the ICL76XX family has a similar I_Q set-up scheme, which allows the amplifier to be set to nominal quiescent currents of 10μA, 100μA or 1mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12 and ICL7631 have an external I_Q control terminal, permitting user selection of each amplifiers' quiescent current. (The 7621 and 7641/42 have fixed I_Q settings — refer to selector guide for details.) To set the I_Q of programmable versions, connect the I_Q terminal as follows:

$I_Q = 10\mu A$ — I_Q pin to V^+

$I_Q = 100\mu A$ — I_Q pin to ground. If this is not possible, any voltage from $V^+ - 0.8$ to $V^- + 0.8$ can be used.

$I_Q = 1mA$ — I_Q pin to V^-

NOTE: The output current available is a function of the quiescent current setting. For maximum p-p output voltage swings into low impedance loads, I_Q of 1mA should be selected.

Output Stage and Load Driving Considerations

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the I_Q settings. This allows output swings to almost the supply rails for output loads of 1MΩ, 100kΩ, and 10kΩ, using the output stage in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB for higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

Input Offset Nulling

For those models provided with OFFSET NULLING pins, nulling may be achieved by connecting a 25K pot between the OFFSET terminals with the wiper connected to V^+. At quiescent currents of 1mA and 100μA, the nulling range provided is adequate for all V_{OS} selections; however with $I_Q = 10\mu A$, nulling may not be possible with higher values of V_{OS}.

Frequency Compensation

The ICL76XX are internally compensated, and are stable for closed loop gains as low as unity with capacitive loads up to 100pF

Extended Common Mode Input Range

The ICL7612 incorporates additional processing which allows the input CMVR to exceed each power supply rail by 0.1 volt for applications where $V_{SUPP} \geq \pm 1.5V$. For those applications where $V_{SUPP} \leq \pm 1.5V$, the input CMVR is limited in the positive direction, but may exceed the negative supply rail by 0.1 volt in the negative direction (eg. for $V_{SUPP} = \pm 1.0V$, the input CMVR would be +0.6 volts to −1.1 volts).

OPERATION AT $V_{SUPP} = \pm 1.0$ VOLTS

Operation at $V_{SUPP} = \pm 1.0V$ is guaranteed at $I_Q = 10\mu A$ for A and B grades only. This applies to those devices with selectable I_Q, and devices that are set internally to $I_Q = 10\mu A$ (i.e., ICL7611, 7612, 7631, 7642).

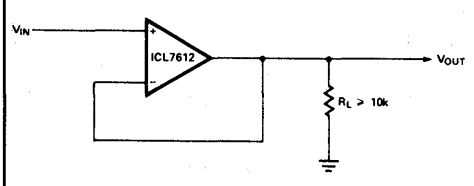
Output swings to within a few millivolts of the supply rails are achievable for $R_L \geq 1M\Omega$. Guaranteed input CMVR is ±0.6V minimum and typically +0.9V to −0.7V at $V_{SUPP} = \pm 1.0V$. For applications where greater common mode range is desirable, refer to the description of ICL7612 above.

NOTE: All typical values have been characterized but are not tested.

The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup.

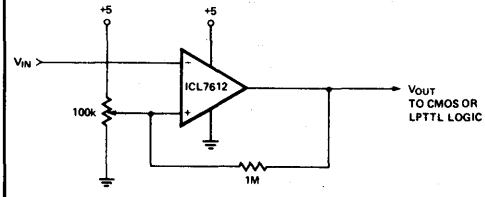
APPLICATIONS

Note that in no case is I_Q shown. The value of I_Q must be chosen by the designer with regard to frequency response and power dissipation.



0307-30

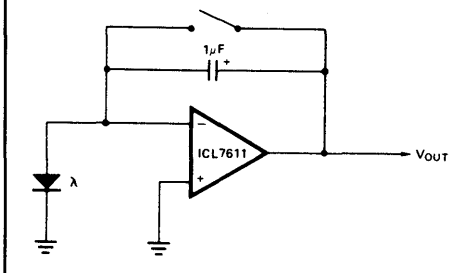
Figure 3: Simple Follower*



0307-31

*By using the ICL7612 in these applications, the circuits will follow rail to rail inputs.

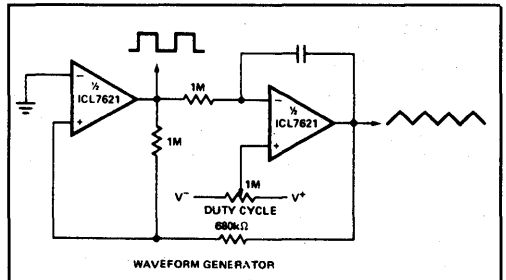
Figure 4: Level Detector*



0307-32

*Low leakage currents allow integration times up to several hours.

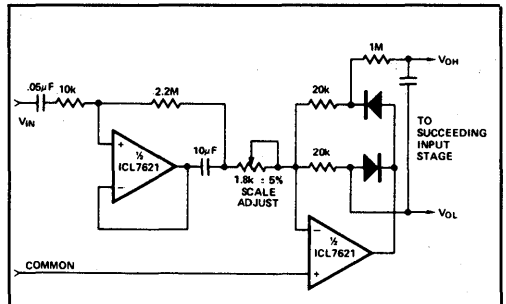
Figure 5: Photocurrent Integrator



0307-33

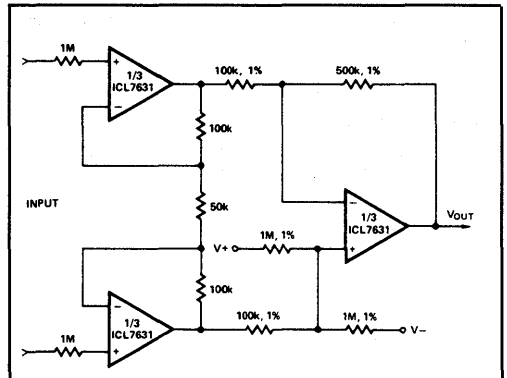
Since the output range swings exactly from rail to rail, frequency and duty cycle are virtually independent of power supply variations.

Figure 6: Precise Triangle/Square Wave Generator



0307-34

Figure 7: Averaging AC to DC Converter for A/D Converters Such as ICL7106, 7107, 7109, 7116, 7117

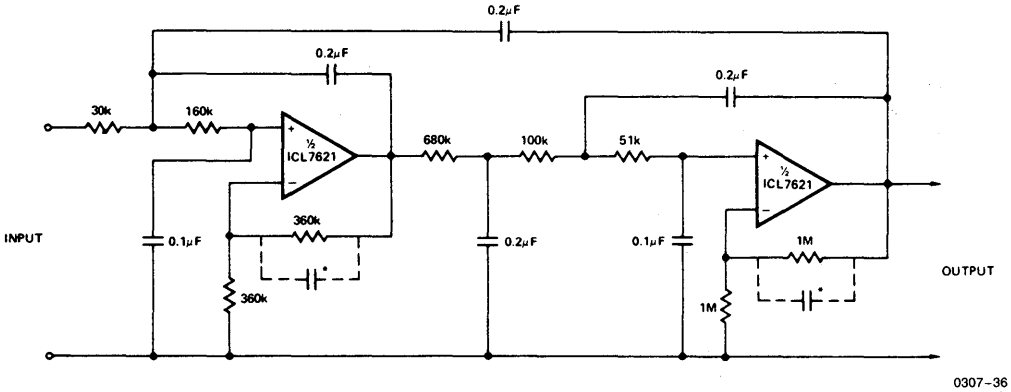


0307-35

Note that $A_{VOL} = 25$; single Ni-cad battery operation. Input current (from sensors connected to patient) limited to $< 5\mu A$ under fault conditions.

Figure 8: Medical Instrument Preamp

NOTE: All typical values have been characterized but are not tested.

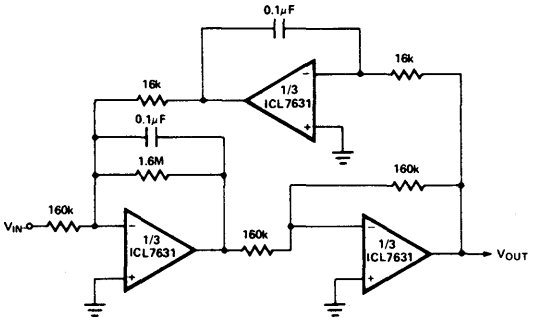


0307-36

The low bias currents permit high resistance and low capacitance values to be used to achieve low frequency cutoff. $f_c = 10Hz$, $A_{VCL} = 4$, Passband ripple = 0.1dB

*Note that small capacitors (25 – 50pF) may be needed for stability in some cases.

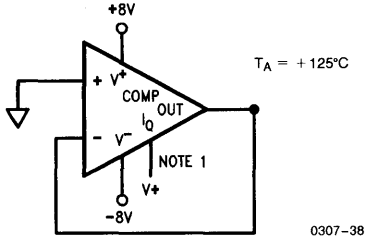
Figure 9: Fifth Order Chebyshev Multiple Feedback Low Pass Filter



0307-37

Note that I_Q on each amplifier may be different. $A_{VCL} = 10$, $Q = 100$, $f_o = 100Hz$.

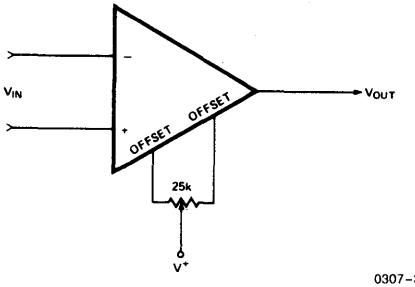
Figure 10: Second Order Biquad Bandpass Filter



0307-38

NOTE 1. For devices with programmable standby current, connect I_Q pin to V+ ($I_Q = 10\mu A$ mode).

Figure 11: Burn-In and Life Test Circuit



0307-39

Figure 12: V_{OS} Null Circuit

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR
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ICL7650S
Super Chopper-Stabilized Operational Amplifier

GENERAL DESCRIPTION

The ICL7650S Super Chopper-Stabilized Amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is a direct replacement for the industry-standard ICL7650 offering ***improved*** input offset voltage, ***lower*** input offset voltage temperature coefficient, ***reduced*** input bias current, and ***wider*** common mode voltage range. All improvements are highlighted in ***bold italics*** in the Electrical Characteristics section. ***Critical parameters are guaranteed over the entire commercial, industrial and military temperature ranges.***

Harris' unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lock-up.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained. However the 14-lead version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7650S is internally compensated for unity-gain operation.

FEATURES

- ***Guaranteed*** **Max Input Offset Voltage for *All* Temperature Ranges**
- **Low Long-Term and Temperature Drifts of Input Offset Voltage**
- ***Guaranteed*** **Max Input Bias Current—10 pA**
- ***Extremely Wide*** **Common Mode Voltage Range—+3.5 to −5V**
- ***Reduced*** **Supply Current—2 mA**
- ***Guaranteed*** **Minimum Output Source/Sink Current**
- **Extremely High Gain—150 dB**
- **Extremely High CMRR and PSRR—140 dB**
- **High Slew Rate—2.5V/μs**
- **Wide Bandwidth—2 MHz**
- **Unity-gain Compensated**
- **Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use**
- **Extremely Low Chopping Spikes at Input and Output**
- **Characterized Fully *Over All* Temperature Ranges**
- ***Improved, Direct*** **Replacement for Industry-Standard ICL7650 and other Second-Source Parts**

ORDERING INFORMATION

Part	Temperature Range	Package
ICL7650SCPA-1	0°C to +70°C	8-Pin Plastic
ICL7650SCPD		14-Pin Plastic
ICL7650SCTV-1		8-Pin TO-99
ICL7650SIPA-1	−25°C to +85°C	8-Pin Plastic
ICL7650SIPD		14-Pin Plastic
ICL7650SIJD		14-Pin CERDIP
ICL7650SITV-1		8-Pin TO-99
ICL7650SMJD	−55°C to +125°C	14-Pin CERDIP
ICL7650SMTV-1		8-Pin TO-99

302161-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage ..... (V^+ +0.3) to (V^- −0.3)
Voltage on Oscillator Control Pins ..... V^+ to V^-
Duration of Output Short Circuit ..... Indefinite
Current into Any Pin ..... 10 mA
—while operating (Note 1) ..... 100 μA
Continuous Total Power Dissipation (T_A = 25°C)
CERDIP Package ..... 500 mW
Plastic Package ..... 375 mW
TO-99 ..... 250 mW

Storage Temperature Range ..... −55°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Operating Temperature Range
ICL7650SC ..... 0°C to +70°C
ICL7650SI ..... −25°C to +85°C
ICL7650SM ..... −55°C to +125°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

Test Conditions: (V^+ = +5V, V^- = −5V, T_A = +25°C, Test Circuit as in Fig. 3 (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{OS}	***Input Offset Voltage*** (Note 2)	T_A = +25°C		***±0.7***	+5	μV
		0°C ≤ T_A ≤ +70°C		***±1***	***±8***	
		−25°C ≤ T_A ≤ +85°C		***±2***	***±10***	
		−55°C ≤ T_A ≤ +125°C		***±4***	***±20***	
$\Delta V_{OS}/\Delta T$	***Average Temperature Coefficient of Input Offset Voltage*** (Note 2)	0°C ≤ T_A ≤ +70°C		***0.02***		μV/°C
		−25°C ≤ T_A ≤ +85°C		***0.02***		
		−55°C ≤ T_A ≤ +125°C		***0.03***	0.1	
$\Delta V_{OS}/\Delta t$	Change in Input Offset with Time			100		$nV/\sqrt{month}$
I_{bias}	***Input Bias Current*** $\|I(+)\|, \|I(-)\|$	T_A = 25°C		4	10	pA
		0°C ≤ T_A ≤ +70°C		***5***	***20***	
		−25°C ≤ T_A ≤ +85°C		***20***	***50***	
		−55°C ≤ T_A ≤ +85°C		***20***	***50***	
		+85°C ≤ T_A ≤ +125°C		***100***	***500***	
I_{OS}	***Input Offset Current*** $\|I(-)-I(+)\|$	T_A = 25°C		***8***	***20***	pA
		0°C ≤ T_A ≤ +70°C		***10***	***40***	
		−25°C ≤ T_A ≤ +85°C		***20***	***40***	
		−55°C ≤ T_A ≤ +85°C		***20***	***40***	
		+85°C ≤ T_A ≤ +125°C		***20***	***50***	
R_{IN}	Input Resistance			10^{12}		Ω
A_{VOL}	***Large Signal Voltage Gain*** (Note 2)	R_L = 10 kΩ, V_O = ±4V, T_A = 25°C	***135***	***150***		dB
		0°C ≤ T_A ≤ +70°C	***130***			
		−25°C ≤ T_A ≤ +85°C	***130***			
		−55°C ≤ T_A ≤ +125°C	***120***			
V_{OUT}	Output Voltage Swing (Note 3)	R_L = 10 kΩ	±4.7	±4.85		V
		R_L = 100 kΩ		±4.95		

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

Test Conditions: ($V^+ = +5V$, $V^- = -5V$, $T_A = +25°C$, Test Circuit as in Fig. 3 (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
CMVR	***Common Mode Voltage Range*** (Note 2)	$T_A = 25°C$	-5	***−5.2 to +4***	***+3.5***	V
		$0°C \le T_A \le +70°C$	-5		***+3.5***	
		$-25°C \le T_A \le +85°C$	-5		***+3.5***	
		$-55°C \le T_A \le +125°C$	-5		***+3.5***	
CMRR	***Common Mode Rejection Ratio*** (Note 2)	CMVR = −5V to +3.5V, $T_A = 25°C$	***120***	***140***		dB
		$0°C \le T_A \le +70°C$	***120***			
		$25°C \le T_A \le +85°C$	***115***			
		$-55°C \le T_A \le +125°C$	***110***			
PSRR	***Power Supply Rejection Ratio***	V+, V− = ±3V to ±8V	120	***140***		dB
en	Input Noise Voltage	$R_S = 100\Omega$, f = DC to 10 Hz		2		μVp-p
in	Input Noise Current	f = 10 Hz		0.01		$pA/\sqrt{Hz}$
GBW	Gain Bandwidth Product			2		MHz
SR	Slew Rate	$C_L = 50$ pF, $R_L = 10$ kΩ		2.5		V/μs
t_r	Rise Time			0.2		μs
	Overshoot			20		%
V^+ to V^-	Operating Supply Range		4.5		16	V
I_{supp}	***Supply Current***	No Load, $T_A = 25°C$		2	***3***	mA
		$0°C \le T_A \le +70°C$			***3.2***	
		$-25°C \le T_A \le +85°C$			***3.5***	
		$-55°C \le T_A \le +125°C$			***4***	
$I_{O\ source}$	Output Source Current	$T_A = 25°C$	2.9	4.5		mA
		$0°C \le T_A \le +70°C$	2.3			
		$-25°C \le T_A \le +85°C$	2.2			
		$-55°C \le T_A \le +125°C$	2			
$I_{O\ sink}$	Output Sink Current	$T_A = 25°C$	25	30		mA
		$0°C \le T_A \le +70°C$	20			
		$-25°C \le T_A \le +85°C$	19			
		$-55°C \le T_A \le +125°C$	17			
f_{ch}	Internal Chopping Frequency	Pins 12 & 14 Open	120	250	375	Hz
	Clamp ON Current (Note 4)	$R_L = 100$ kΩ, $T_A = 25°C$	25	70		μA
	Clamp OFF Current (Note 4)	$-4V \le V_{out} \le +4V$, $T_A = 25°C$		***0.001***	***5***	nA
		$0°C \le T_A \le +70°C$			***10***	
		$-25°C \le T_A \le +85°C$			***10***	
		$-55°C \le T_A \le +125°C$			***15***	

NOTE 1: Limiting input current to 100 μA is recommended to avoid latchup problems. Typically 1 mA is safe, however this is not guaranteed.

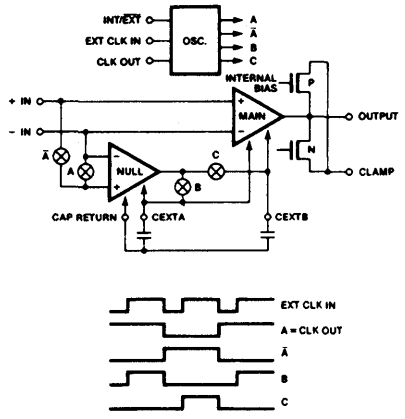
2: These parameters are guaranteed by design and characterization, but not tested at temperature extremes because thermocouple effects prevent precise measurement of these voltages in automatic test equipment.

3: OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs. clamp current characteristics.

4: See OUTPUT CLAMP under detailed description.

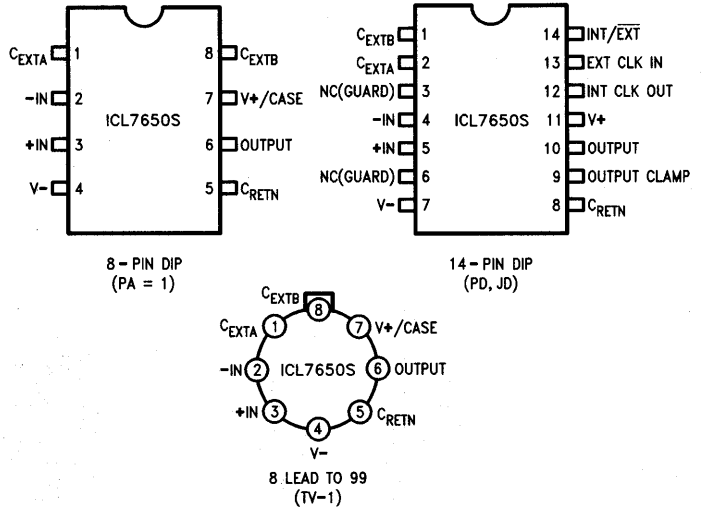
5: All significant improvements over the industry-standard ICL7650 are highlighted in ***bold italics.***

NOTE: All typical values have been characterized but are not tested.



0089-1

Figure 1: Functional Diagram



0089-2

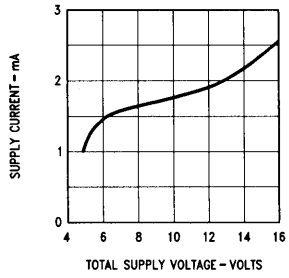
Figure 2: Pin Configurations

3 OPERATIONAL AMPLIFIERS

NOTE: All typical values have been characterized but are not tested.

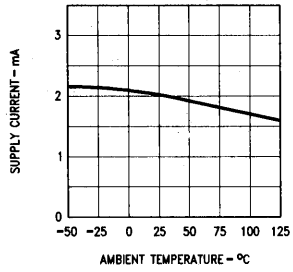
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs. Supply Voltage



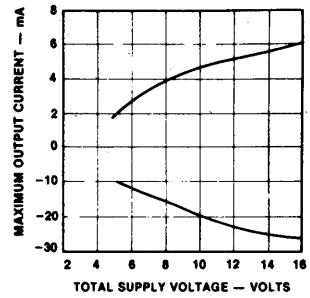
0089-3

Supply Current vs. Ambient Temperature



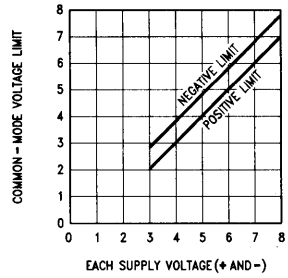
0089-4

Maximum Output Current vs. Supply Voltage



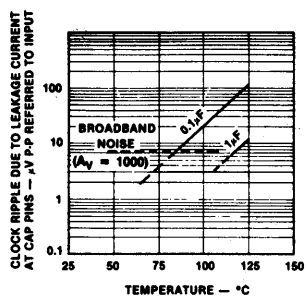
0089-5

Common-Mode Input Voltage Range vs. Supply Voltage



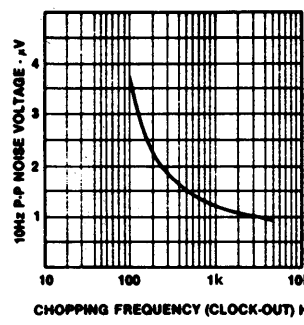
0089-6

Clock Ripple Referred to the Input vs. Temperature



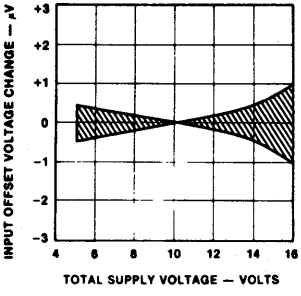
0089-7

10Hz P-P Noise Voltage vs. Chopping Frequency



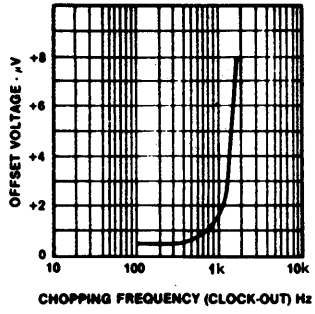
0089-8

Input Offset Voltage Change vs. Supply Voltage



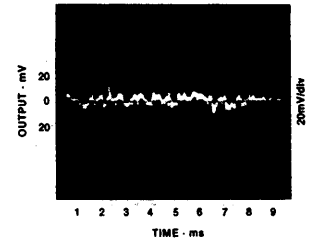
0089-9

Input Offset Voltage vs. Chopping Frequency



0089-10

Output with Zero Input; Gain = 1000; Balanced Source Impedance = 10 kΩ

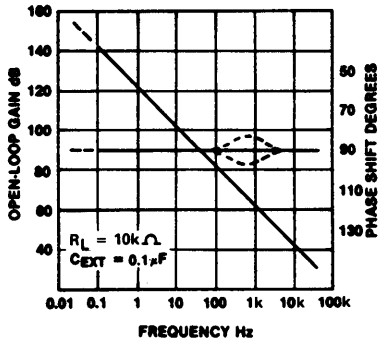


0089-11

NOTE: All typical values have been characterized but are not tested.

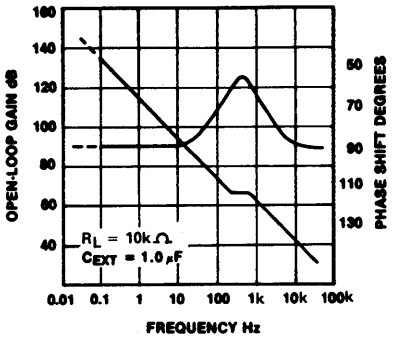
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Open Loop Gain and Phase Shift vs. Frequency



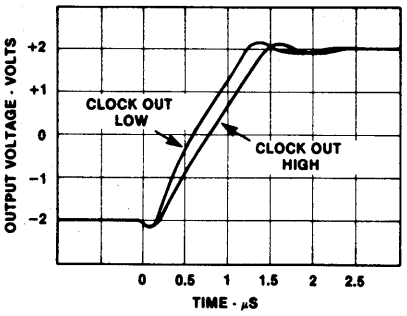
0089-12

Open Loop Gain and Phase Shift vs. Frequency



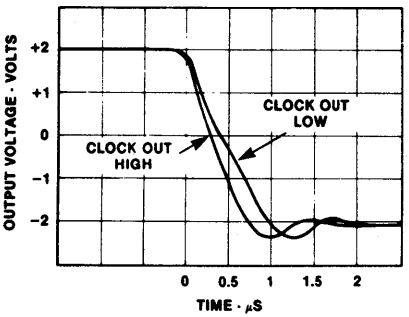
0089-13

Voltage Follower Large Signal Pulse Response*



0089-14

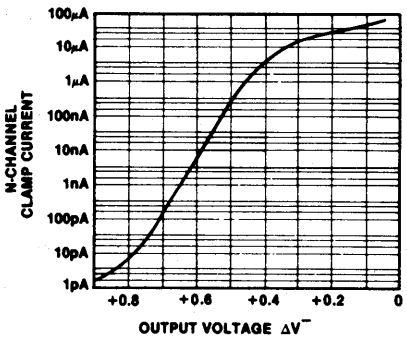
Voltage Follower Large Signal Pulse Response*



0089-15

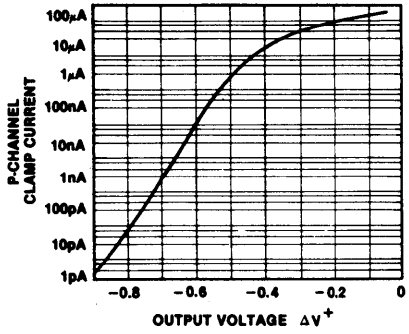
*THE TWO DIFFERENT RESPONSES CORRESPOND TO THE TWO PHASES OF THE CLOCK.

N-Channel Clamp Current vs. Output Voltage



0089-16

P-Channel Clamp Current vs. Output Voltage



0089-17

NOTE: All typical values have been characterized but are not tested.

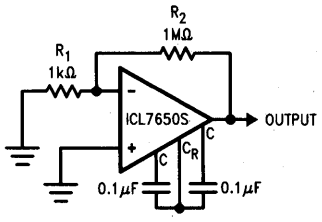


Figure 3: ICL7650S Test Circuit

DETAILED DESCRIPTION

Amplifier

The functional diagram shows the major elements of the ICL7650S. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output, while the nulling amplifier, under the control of the chopping oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power-supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, and the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals, and also the feedforward-type injection into the compensation capacitor, which is the main cause of output spikes in this type of circuit.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs. frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7650S by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7650S, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Capacitor Connection

The null/storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN}.

Output Clamp

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled input differential inputs are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

Clock

The ICL7650S has an internal oscillator, giving a chopping frequency of 200 Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/$\overline{\text{EXT}}$ pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V^- to disable the internal clock. The external clock signal may then be applied to the EXT CLOCK IN pin. An internal divide-by-two provides the desired 50% input switching duty cycle. Since the capacitors are charged only when EXT CLOCK IN is high, a 50%–80% positive duty cycle is recommended, especially for higher frequencies. The external clock can swing between V^+ and V^-. The logic threshold will be at about 2.5V below V^+. Note also that a signal of about 400 Hz, with a 70% duty cycle, will be present at the EXT CLOCK IN pin with INT/EXT high or open. This is the internal clock signal before being fed to the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10 μV/sec, and relatively long measurements can be made with little change in offset.

BRIEF APPLICATION NOTES

Component Selection

The two required capacitors, C_{EXTA} and C_{EXTB}, have optimum values depending on the clock or chopping frequency. For the preset internal clock, the correct value is 0.1 μF, and to maintain the same relationship between the chopping frequency and the nulling time constant this value should be scaled approximately in proportion if an external clock is used. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest setting on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 μV.

Static Protection

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics, which may result in increased input-leakage currents.

NOTE: All typical values have been characterized but are not tested.

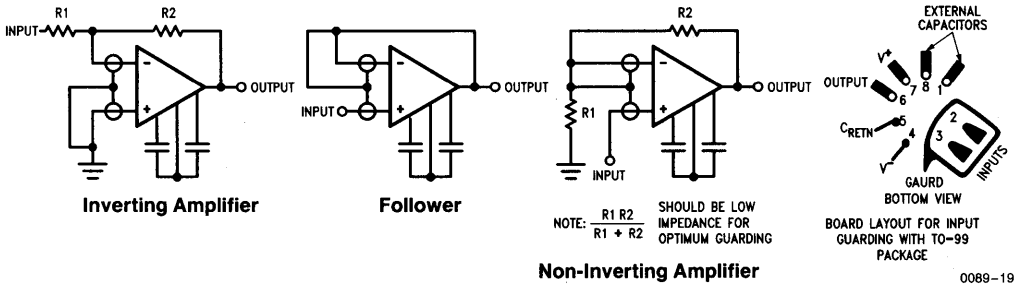


Figure 4: Connection of Input Guards

Latchup Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1 mA to avoid latchup, even under fault conditions.

Output Stage/Load Driving

The output circuit is a high-impedance type (approximately 18 kΩ), and therefore with loads less than this value, the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120 dB even with a 1 kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or higher. This will result in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 10° in the transition region where the main amplifier takes over from the null amplifier.

Thermo-Electric Effects

The ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon, etc. Unless all junctions are at the same temperature, thermoelectric voltages typically around 0.1 μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-efficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7650S. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the 14-pin dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

NOTE: All typical values have been characterized but are not tested.

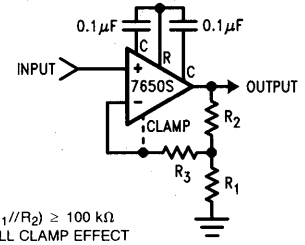
Pin Compatibility

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, usually used for offset null or compensation capacitors, or simply not connected. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V+, by two capacitors from those pins to pin 5, will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to pin 5 is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, μA748, and similar parts.

The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert it to the ICL7650S.

TYPICAL APPLICATIONS

Clearly the applications of the ICL7650S will mirror those of other op amps. Anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7650S is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 5 and 6. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op amps by the ICL7650S are the supply voltage (±8V max.) and the output drive capability (10 kΩ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 7, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7650S. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.

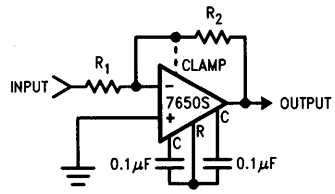


$R_3 + (R_1//R_2) \geq 100\ k\Omega$
FOR FULL CLAMP EFFECT

0089-20

Figure 5: Non Inverting Amplifier With Optional Clamp

NOTE: R_1/R_2 indicates the parallel combination of R_1 and R_2



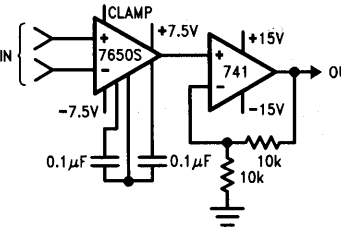
$(R_1//R_2) \geq 100\ k\Omega$
FOR FULL CLAMP EFFECT

0089-21

Figure 6: Inverting Amplifier With (Optional) Clamp

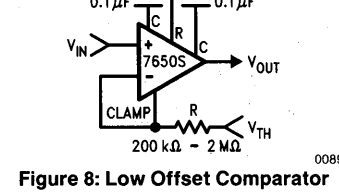
NOTE: R_1/R_2 indicates the parallel combination of R_1 and R_2

Figure 8 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current $\approx V_{IN}/R$ without disturbing other portions of the system.



0089-22

Figure 7: Using 741 to Boost Output Drive Capacity



0089-23

Figure 8: Low Offset Comparator

Normal logarithmic amplifiers are limited in dynamic range in the voltage-input mode by their input-offset voltage. The built-in temperature compensation and convenience features of the ICL8048 can be extended to a voltage-input dynamic range of close to 6 decades by using the ICL7650S to offset-null the ICL8048, as shown in Figure 9. The same concept can also be used with such devices as the HA2500 or HA2600 families of op amps to add very low offset voltage capability to their very high slew rates and bandwidths. Note that these circuits will also have their DC gains, CMRR, and PSRR enhanced.

NOTE: All typical values have been characterized but are not tested.

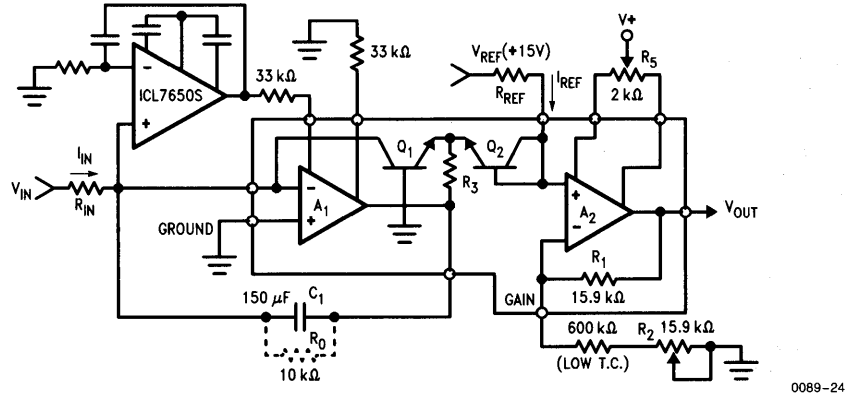


Figure 9: ICL8048 Offset Nulled by ICL7650S

FOR FURTHER APPLICATIONS ASSISTANCE, SEE A053 AND R017

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

ICL7652S

Super Chopper-Stabilized Low-Noise Operational Amplifier

GENERAL DESCRIPTION

The ICL7652S Super Chopper-Stabilized Low-Noise Amplifier offers exceptionally low input offset voltage and is extremely stable with respect to time and temperature. It is a direct replacement for the industry-standard ICL7652 offering ***improved*** input offset voltage, ***lower*** input offset voltage temperature coefficient, ***reduced*** input bias current, and ***wide*** common mode voltage range. All improvements are highlighted in ***bold italics*** in the Electrical Characteristics Section. ***Critical parameters are guaranteed over the entire commercial, industrial, and military temperature range.***

Harris' unique CMOS chopper-stabilized amplifier circuitry is user-transparent, virtually eliminating the traditional chopper amplifier problems of intermodulation effects, chopping spikes, and overrange lock-up.

The chopper amplifier achieves its low offset by comparing the inverting and non-inverting input voltages in a nulling amplifier, nulled by alternate clock phases. Two external capacitors are required to store the correcting potentials on the two amplifier nulling inputs; these are the only external components necessary.

The clock oscillator and all the other control circuitry is entirely self-contained, however the 14-lead version includes a provision for the use of an external clock, if required for a particular application. In addition, the ICL7652S is internally compensated for unity-gain operation.

FEATURES

- ***Guaranteed*** **Max Input Offset Voltage for *All* Temperature Ranges**
- **Low Long-Term and Temperature Drifts of Input Offset Voltage**
- ***Reduced*** **Input Bias Current—3 pA Typ; 30 pA *Max* over Temperature**
- ***Extremely Wide*** **Common Mode Voltage Range—+3.5 to −4.3 Volts**
- ***Reduced*** **Supply Current—1.7 mA; 3.5 mA *Max* over mil Temperature**
- ***Guaranteed*** **Minimum Output Source/Sink Current**
- **Extremely High Gain −150 dB**
- **Low Input Noise Voltage—0.2 μVp-p (DC−1 Hz)**
- **Unity-Gain Compensated**
- **Very Low Intermodulation Effects (Open-Loop Phase Shift < 2°μ @ Chopper Frequency)**
- **Clamp Circuit to Avoid Overload Recovery Problems and Allow Comparator Use (14-Lead only)**
- **Extremely Low Chopping Spikes at Input and Output**
- **Characterized Fully Over Military Temperature Range**
- ***Improved*** **Direct Replacement for Industry-Standard IC7652 and other Second-Source Parts**

ORDERING INFORMATION

Part	Temperature Range	Package
ICL7652SCPD	0°C to +70°C	14-Pin Plastic
ICL7652SIPD	−25°C to +85°C	14-Pin Plastic

302162-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage ..... (V^+ + 0.3) to (V^- − 0.3)
Voltage on Oscillator Control Pins ..... V^+ to V^-
Duration of Output Short Circuit ..... Indefinite
Current into Any Pin ..... 10 mA
—While Operating (Note 1) ..... 100 μA
Continuous Total Power Dissipation (T_A = 25°C)
Plastic Package ..... 375 mW
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... +300°C
Operating Temperature Range
ICL7652SC ..... 0°C to +70°C
ICL7652SI ..... −25°C to +85°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

Test Conditions: V^+ = +5V, V^- = −5V, T_A = +25°C, Test Circuit as in Figure 3 (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{OS}	***Input Offset Voltage***	T_A = +25°C		***±0.7***	±5	μV
		0°C ≤ T_A ≤ +70°C		***±2***	***±7***	
		−25°C ≤ T_A ≤ +85°C		***±3***	***±10***	
$\Delta V_{OS}/\Delta T$	***Average Temp. Coefficient of Input Offset Voltage*** (Note 2)	0°C ≤ T_A ≤ +70°C		***0.01***	***0.06***	μV/°C
		−25°C ≤ T_A ≤ +85°C		***0.02***	***0.07***	
		−55°C ≤ T_A ≤ +85°C		***0.02***	***0.07***	
$\Delta V_{OS}/\Delta t$	Change in Input Offset with Time			150		nV/$\sqrt{\text{month}}$
I_{bias}	***Input Bias Current*** $\lvert I(+)\rvert$, $\lvert I(-)\rvert$	T_A = 25°C		***3***	30	pA
		0°C ≤ T_A ≤ +70°C			***30***	
		−25°C ≤ T_A ≤ +85°C			***30***	
		−55°C ≤ T_A ≤ +85°C			***30***	
I_{OS}	***Input Offset Current*** $\lvert I(-) - I(+)\rvert$	T_A = 25°C		***15***	***40***	pA
		0°C ≤ T_A ≤ +70°C			***40***	
		−25°C ≤ T_A ≤ +85°C			***40***	
		−55°C ≤ T_A ≤ +85°C			***40***	
R_{IN}	Input Resistance			10^{12}		Ω
A_{VOL}	***Large Signal Voltage Gain*** (Note 2)	RL = 10 KΩ, V_O = ±4V, T_A = 25°C	***135***	150		dB
		0°C ≤ T_A ≤ +70°C	***130***			
		−25°C ≤ T_A ≤ +85°C	***130***			
V_{OUT}	Output Voltage Swing (Note 3)	RL = 10 KΩ	±4.7	±4.85		V
		RL = 100 KΩ		±4.95		

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $T_A = +25°C$, Test Circuit (unless otherwise specified) (Continued)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
CMRR	***Common Mode Rejection Ratio*** (Note 2)	CMVR = −4.3V to +3.5, T_A = 25°C	***120***	130		dB
		0°C ≤ T_A ≤ +70°C	***110***			
		−25°C ≤ T_A ≤ +85°C	***110***			
PSRR	***Power Supply Rejection Ratio*** (Note 2)	V^+, V^- = ±3V to ±8V	***120***	130		dB
		0°C ≤ T_A ≤ +70°C	***110***			
		−25°C ≤ T_A ≤ +85°C	***110***			
en	Input Noise Voltage	Rs = 100Ω, f = DC to 1 Hz		0.2		μVp-p
		f = DC to 10 Hz		0.7		
in	Input Noise Current	f = 10 Hz		0.01		pA/√Hz
GBW	***Gain Bandwidth***			500		kHz
SR	***Slew Rate***	CL = 50 pF, RL = 10 KΩ		1.0		V/μs
	Overshoot			15		%
V^+ to V^-	Operating Supply Range		5.0		16	V
I_{SUPP}	***Supply Current***	No Load T_A = 25°C		***1.7***	***2.5***	mA
		0°C < T_A < 70°C			***3.0***	
		−25°C < T_A < 85°C			***3.0***	
$I_{O\ source}$	Output Source Current	T_A = 25°C	2.4	4.4		mA
		0°C < T_A < 70°C	2.0			
		−25°C < T_A < 85°C	1.9			
$I_{o\ sink}$	Output Sink Current	T_A = 25°C	15.0	20.0		mA
		0°C < T_A < 70°C	12.0			
		−25°C < T_A < 85°C	12.0			
fch	***Internal Chopping Frequency***	Pins 12 & 14 Open (dip)	250	***450***	***650***	Hz
	Clamp ON Current (Note 4)	RL = 100 KΩ, T_A = 25°C	***30***	100		μA
	Clamp OFF Current (Note 4)	−4.0V < V_{OUT} < +4.0V, T_A = 25°C		***0.001***	***10***	nA
		0°C ≤ T_A ≤ +70°C			***10***	
		−25°C ≤ T_A ≤ +85°C			***10***	

NOTE 1: Limiting input current to 100 μA is recommended to avoid latchup problems. Typically 1 mA is safe, however this is not guaranteed.

2: These parameters are guaranteed by design and characterization, but not tested at temperature extremes because thermocouple effects prevent precise measurement of these voltages in automatic test equipment.

3: OUTPUT CLAMP not connected. See typical characteristic curves for output swing vs clamp current characteristics.

4: See OUTPUT CLAMP under detailed description.

5: All significant improvements over the industry-standard ICL7652 are highlighted in ***bold italics.***

NOTE: All typical values have been characterized but are not tested.

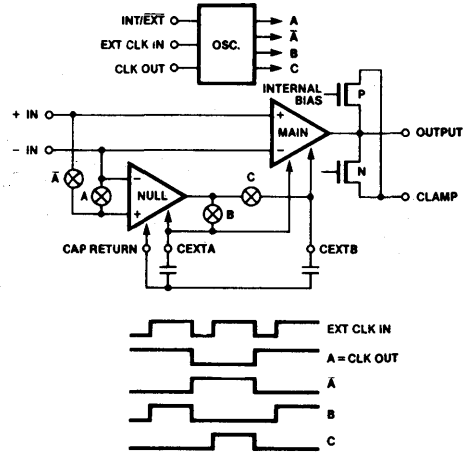


Figure 1: Functional Diagram

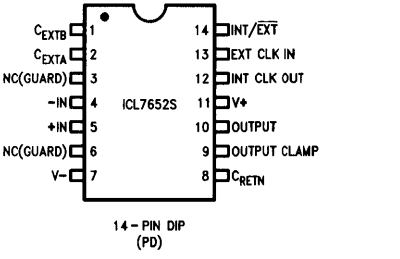
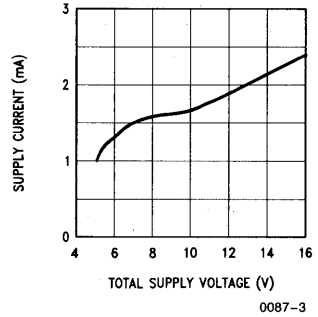


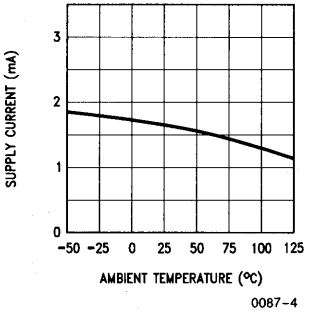
Figure 2: Pin Configuration

TYPICAL PERFORMANCE CHARACTERISTICS

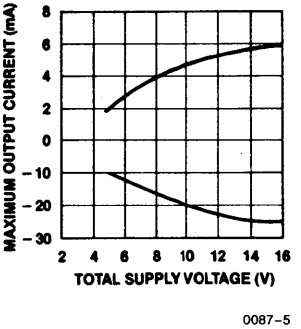
Supply Current vs Supply Voltage



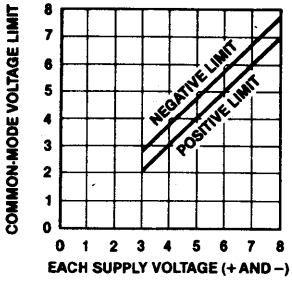
Supply Current vs Ambient Temperature



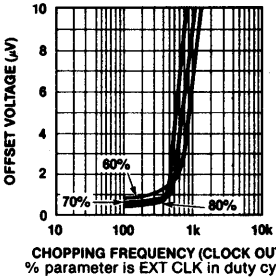
Maximum Output Current vs Supply Voltage



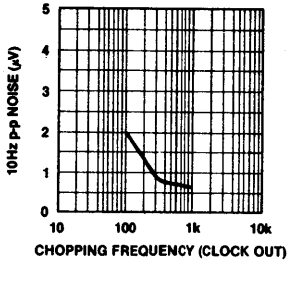
Common-Mode Input Voltage Range vs Supply Voltage



Input Offset Voltage vs Chopping Frequency



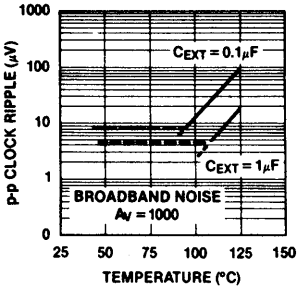
10 Hz P-P Noise Voltage vs Chopping Frequency



NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Clock Ripple Referred to the Input vs Temperature



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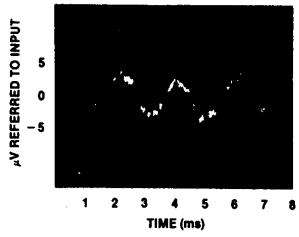
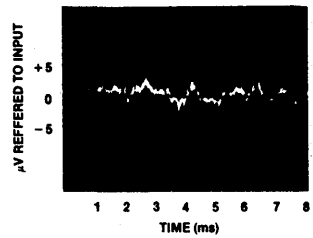
Broadband Noise Balanced Source Impedance = 1 kΩ Gain = 1000 C_{EXT} = 0.1 μF



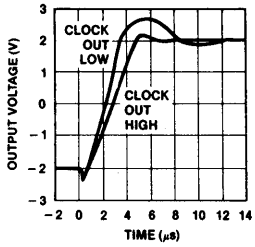
0087-10

Broadband Noise Balanced Source Impedance = 1 kΩ Gain = 1000 C_{EXT} = 1.0 μF



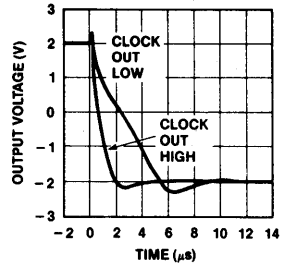
0087-11

Voltage Follower Large Signal Pulse Response*



0087-12

Voltage Follower Large Signal Pulse Response*



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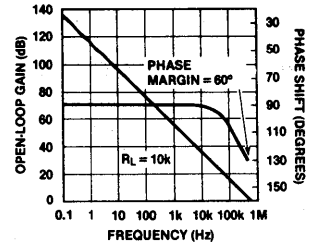
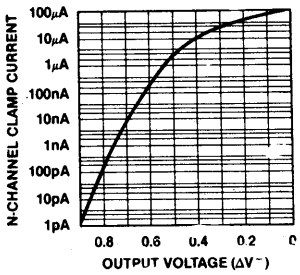
Open-Loop Gain and Phase Shift vs Frequency



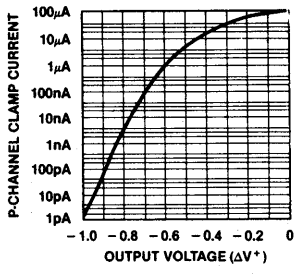
0087-14

*THE TWO DIFFERENT RESPONSES CORRESPOND TO THE TWO PHASES OF THE CLOCK.

N-Channel Clamp Current vs Output Voltage



P-Channel Clamp Current vs Output Voltage



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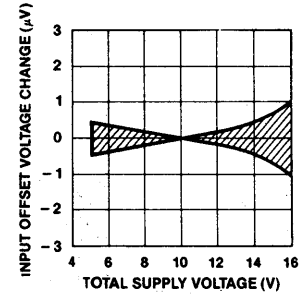
Input Offset Voltage Change vs Supply Voltage



0087-17

NOTE: All typical values have been characterized but are not tested.

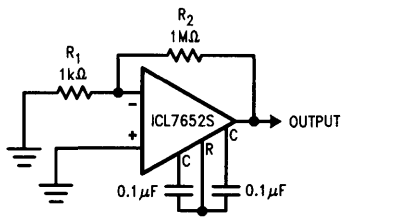


Figure 3: Test Circuit

DETAILED DESCRIPTION

The Functional Diagram (Figure 1) shows the major elements of the ICL7652S. There are two amplifiers, the main amplifier, and the nulling amplifier. Both have offset-null capability. The main amplifier is connected continuously from the input to the output. The nulling amplifier, under the control of the chopping frequency oscillator and clock circuit, alternately nulls itself and the main amplifier. The nulling connections, which are MOSFET gates, are inherently high-impedance, and two external capacitors provide the required storage of the nulling potentials and the necessary nulling-loop time constants. The nulling arrangement operates over the full common-mode and power supply ranges, and is also independent of the output level, thus giving exceptionally high CMRR, PSRR, and A_{VOL}.

Careful balancing of the input switches, together with the inherent balance of the input circuit, minimizes chopper frequency charge injection at the input terminals. Feedforward-type injection into the compensation capacitor is also minimized, which is the main cause of output spikes in this type of circuit.

Intermodulation

Previous chopper-stabilized amplifiers have suffered from intermodulation effects between the chopper frequency and input signals. These arise because the finite AC gain of the amplifier necessitates a small AC signal at the input. This is seen by the zeroing circuit as an error signal, which is chopped and fed back, thus injecting sum and difference frequencies and causing disturbances to the gain and phase vs frequency characteristics near the chopping frequency. These effects are substantially reduced in the ICL7652S by feeding the nulling circuit with a dynamic current, corresponding to the compensation capacitor current, in such a way as to cancel that portion of the input signal due to finite AC gain. Since that is the major error contribution to the ICL7652S, the intermodulation and gain/phase disturbances are held to very low values, and can generally be ignored.

Capacitor Connection

The null-storage capacitors should be connected to the C_{EXTA} and C_{EXTB} pins, with a common connection to the C_{RETN} pin. This connection should be made directly by either a separate wire or PC trace to avoid injecting load current IR drops into the capacitive circuitry. The outside foil, where available, should be connected to C_{RETN}.

Output Clamp

The OUTPUT CLAMP pin allows reduction of the overload recovery time inherent with chopper-stabilized amplifiers. When tied to the inverting input pin, or summing junction, a current path between this point and the OUTPUT pin occurs just before the device output saturates. Thus uncontrolled differential input voltages are avoided, together with the consequent charge build-up on the correction-storage capacitors. The output swing is slightly reduced.

Clock

The ICL7652S has an internal oscillator, giving a chopping frequency of 400 Hz, available at the CLOCK OUT pin on the 14-pin devices. Provision has also been made for the use of an external clock in these parts. The INT/$\overline{\text{EXT}}$ pin has an internal pull-up and may be left open for normal operation, but to utilize an external clock this pin must be tied to V^- to disable the internal clock. The external clock signal may then be applied to the EXT CLOCK IN pin. An internal divide-by-two provides the desired 50% input switching duty cycle. Since the capacitors are charged only when EXT CLOCK IN is high, a 50%-80% positive duty cycle is recommended, especially for higher frequencies. The external clock can swing between V^+ and V^-. The logic threshold will be at about 2.5V below V^+. Note also that a signal of about 800 Hz, with a 70% duty cycle, will be present at the EXT CLOCK IN pin with INT/EXT high or open. This is the internal clock signal before being fed to the divider.

In those applications where a strobe signal is available, an alternate approach to avoid capacitor misbalancing during overload can be used. If a strobe signal is connected to EXT CLK IN so that it is low during the time that the overload signal is applied to the amplifier, neither capacitor will be charged. Since the leakage at the capacitor pins is quite low at room temperature, the typical amplifier will drift less than 10 μV/sec , and relatively long measurements can be made with little change in offset.

BRIEF APPLICATION NOTES

Component Selection

The required capacitors, C_{EXTA} and C_{EXTB}, are normally in the range of 0.1 μF to 1.0 μF. A 1.0 μF capacitor should be used in broad bandwidth circuits if minimum clock ripple noise is desired. For limited bandwidth applications where clock ripple is filtered out, using a 0.1 μF capacitor results in slightly lower offset voltage. A high-quality film-type capacitor such as mylar is preferred, although a ceramic or other lower-grade capacitor may prove suitable in many applications. For quickest setting on initial turn-on, low dielectric absorption capacitors (such as polypropylene) should be used. With ceramic capacitors, several seconds may be required to settle to 1 μV.

Static Protection

All device pins are static-protected by the use of input diodes. However, strong static fields and discharges should be avoided, as they can cause degraded diode junction characteristics which may result in increased input-leakage currents.

NOTE: All typical values have been characterized but are not tested.

Latchup Avoidance

Junction-isolated CMOS circuits inherently include a parasitic 4-layer (p-n-p-n) structure which has characteristics similar to an SCR. Under certain circumstances this junction may be triggered into a low-impedance state, resulting in excessive supply current. To avoid this condition no voltage greater than 0.3V beyond the supply rails should be applied to any pin. In general, the amplifier supplies must be established either at the same time or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to under 1 mA to avoid latchup, even under fault conditions.

Output Stage/Load Driving

The output circuit is a high-impedance type (approximately 18 kΩ), and therefore, with loads less than this the chopper amplifier behaves in some ways like a transconductance amplifier whose open-loop gain is proportional to load resistance. For example, the open-loop gain will be 17 dB lower with a 1 kΩ load than with a 10 kΩ load. If the amplifier is used strictly for DC, this lower gain is of little consequence, since the DC gain is typically greater than 120 dB even with a 1 kΩ load. However, for wideband applications, the best frequency response will be achieved with a load resistor of 10 kΩ or higher. This will result in a smooth 6 dB/octave response from 0.1 Hz to 2 MHz, with phase shifts of less than 2° in the transition region where the main amplifier takes over from the null amplifier.

Thermo-Electric Effects

Tne ultimate limitations to ultra-high precision DC amplifiers are the thermo-electric or Peltier effects arising in thermocouple junctions of dissimilar metals, alloys, silicon etc. Unless all junctions are at the same temperature, thermo-electric voltages typically around 0.1 μV/°C, but up to tens of μV/°C for some materials, will be generated. In order to realize the extremely low offset voltages that the chopper amplifier can provide, it is essential to take special precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement, especially that caused by power-dissipating elements in the system. Low thermoelectric-coefficient connections should be used where possible and power supply voltages and power dissipation should be kept to a minimum. High-impedance loads are preferable, and good separation from surrounding heat-dissipating elements is advisable.

Guarding

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the ICL7652S. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8 lead TO-99 package is accomplished by using a 10 lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low-impedance point that is at approximately the same voltage as the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

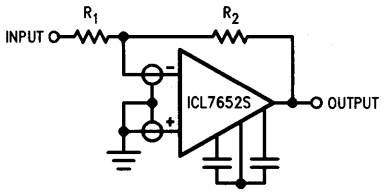
The pin configuration of the 14-pin dual-in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration, but corresponds to that of the LM108).

PIN COMPATIBILITY

The basic pinout of the 8-pin device corresponds, where possible, to that of the industry-standard 8-pin devices, the LM741, LM101, etc. The null-storing external capacitors are connected to pins 1 and 8, which are usually used for offset-null or compensation capacitors. In the case of the OP-05 and OP-07 devices, the replacement of the offset-null pot, connected between pins 1 and 8 and V^+, by two capacitors from those pins to pin 5, will provide easy compatibility. As for the LM108, replacement of the compensation capacitor between pins 1 and 8 by the two capacitors to pin 5 is all that is necessary. The same operation, with the removal of any connection to pin 5, will suffice for the LM101, μA 748, and similar parts.

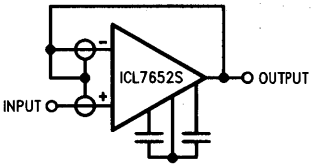
The 14-pin device pinout corresponds most closely to that of the LM108 device, owing to the provision of "NC" pins for guarding between the input and all other pins. Since this device does not use any of the extra pins, and has no provision for offset-nulling, but requires a compensation capacitor, some changes will be required in layout to convert to the ICL7652S.

NOTE: All typical values have been characterized but are not tested.



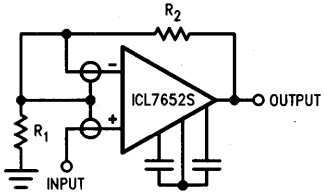
0087-19

Inverting Amplifier



0087-20

Follower

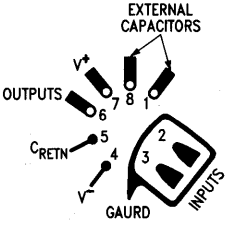


0087-21

Note: $\frac{R_1 R_2}{R_1 + r_2}$

Should be low impedance for optimum guarding

Non-Inverting Amplifier



0087-22

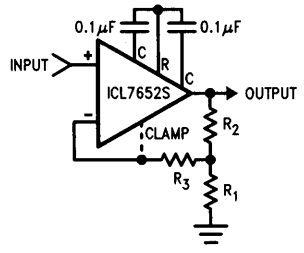
BOTTOM VIEW

Board Layout for Input Guarding with TO-99 Package

Figure 4: Connection of Input Guards

NOTE: All typical values have been characterized but are not tested.

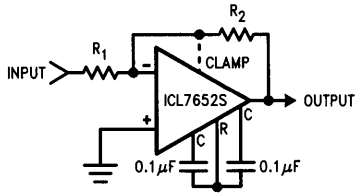
TYPICAL APPLICATIONS



0087-23

$R_3 + (R_1//R_2) \geq 100\ k\Omega$
For Full Clamp Effect

Figure 5: Non-Inverting Amplifier with Optional Clamp

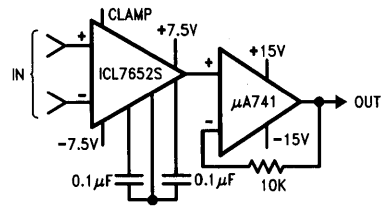


0087-24

$(R_1//R_2) \geq 100\ k\Omega$
For Full Clamp Effect

Figure 6: Inverting Amplifier with Optional Clamp

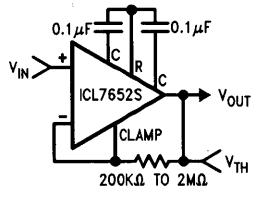
Clearly the applications of the ICL7652S will mirror those of other op-amps. Thus, anywhere that the performance of a circuit can be significantly improved by a reduction of input-offset voltage and bias current, the ICL7652S is the logical choice. Basic non-inverting and inverting amplifier circuits are shown in Figures 5 and 6. Both circuits can use the output clamping circuit to enhance the overload recovery performance. The only limitations on the replacement of other op-amps by the ICL7652S are the supply voltage (±8V max) and the output drive capability (10 kΩ load for full swing). Even these limitations can be overcome using a simple booster circuit, as shown in Figure 7, to enable the full output capabilities of the LM741 (or any other standard device) to be combined with the input capabilities of the ICL7652S. The pair form a composite device, so loop gain stability, when the feedback network is added, should be watched carefully.



0087-25

Figure 7: Using 741 to Boost Output Drive Capability

Figure 8 shows the use of the clamp circuit to advantage in a zero-offset comparator. The usual problems in using a chopper-stabilized amplifier in this application are avoided, since the clamp circuit forces the inverting input to follow the input signal. The threshold input must tolerate the output clamp current $\approx V_{IN}/R$ without disturbing other portions of the system.



0087-26

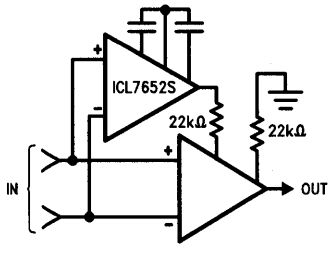
Figure 8: Low Offset Comparator

It is possible to use the ICL7652S to offset-null such high slew rate and bandwidth amplifiers as the HA2500 and HA2600 series, as shown in Figure 9. The same basic idea can be used with low-noise bipolar devices, such as the OP-05, and also with the ICL8048 logarithmic amplifier, to achieve a voltage-input dynamic range of close to 6 decades. Note that these circuits will also have their DC gains, CMRR and PSRR enhanced. More details on these and other ideas are explained in application note A053.

Mixing the ICL7652S with circuits operating at ±15V supplies requires the provision of a lower voltage. Although this can be done fairly easily, a highly efficient voltage divider can be built using the ICL7660S voltage converter circuit "backwards". A suitable connection is shown in Figure 10.

NOTE: All typical values have been characterized but are not tested.

TYPICAL APPLICATIONS (Continued)



HA2500/10/20
HA2600/20
or Similar Device

Figure 9: HA2500 or HA2600 Offset-Nulled by ICL7652S

FOR FURTHER APPLICATIONS ASSISTANCE, SEE A053 AND R017.

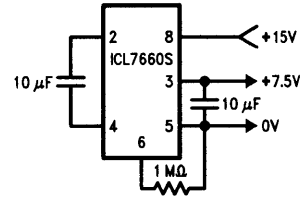


Figure 10: Splitting + 15V with ICL7660S at > 95% Efficiency. Same for − 15V

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

ICL 8023 NOT RECOMMENDED FOR NEW DESIGNS SEE ICL 7630

ICL8021/ICL8023

Low Power Bipolar Operational Amplifier

GENERAL DESCRIPTION

The Harris ICL8021 series are low power operational amplifiers specifically designed for applications requiring very low standby power consumption over a wide range of supply voltages. The electrical characteristics of the 8021 series can be tailored to a particular application by adjusting an external resistor, R_{SET}, which controls the quiescent current. This is advantageous because I_Q can be made independent of the supply voltages: it can be set to an extremely low value where power is critical, or to a larger value for high slew rate or wideband applications.

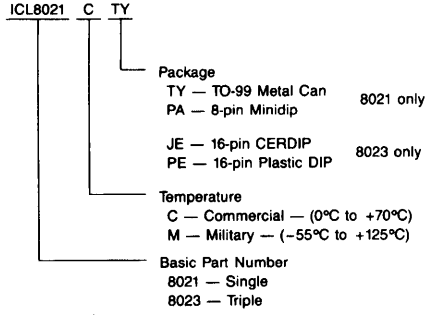
Other features of the 8021 series include low input current that remains constant with temperature, low noise, high input impedance, internal compensation and pin-for-pin compatibility with the 741.

The Harris 8023 consists of three low power operational amplifiers in a single 16-pin DIP. Each amplifier is identical to an 8021 low power op amp, and has separate connections for adjusting its electrical characteristics by means of an external resistor, R_{SET}, which controls the quiescent current of that amplifier.

FEATURES

- **V_{OS} = 3mV Max (Adjustable to Zero)**
- **±1.5V to ±18V Power Supply Operation**
- **Power Consumption — 20μW @ ±1V**
- **Input Bias Current — 30nA Max**
- **Internal Compensation**
- **Pin-For-Pin Compatible With 741**
- **Short Circuit Protected**

ORDERING INFORMATION



0311-20

Part Number	Temperature Range	Package
ICL8021CJA	0°C to 70°C	8 Lead CERDIP
ICL8021CBA	0°C to 70°C	8 Lead S.O.I.C
ICL8021CPA	0°C to 70°C	8 Lead MINIDIP
ICL8021CTY	0°C to 70°C	8 Lead Metal Can
ICL8021MJA	−55°C to +125°C	8 Lead CERDIP
ICL8021MTY*	−55°C to +125°C	8 Lead Metal Can
ICL8023CJE	0°C to 70°C	16 Lead CERDIP
ICL8023CPE	0°C to 70°C	16 Lead MINIDIP
ICL8023MJE*	−55°C to +125°C	16 Lead CERDIP

*Add /88313 to Part Number if 883B processing is required.

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Differential Input Voltage (Note 1) ..... ±15V
Common Mode Input Voltage (Note 1) ..... ±15V
Output Short Circuit Duration ..... Indefinite
Power Dissipation (Note 2) 300mW

Operating Temperature Range
8021M/8023M ..... −55°C to +125°C
8021C/8023C ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

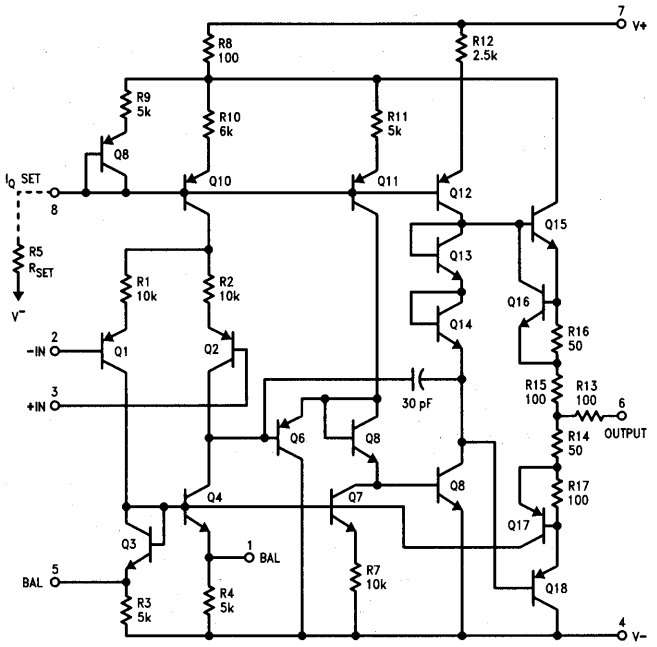


Figure 1: Functional Diagram

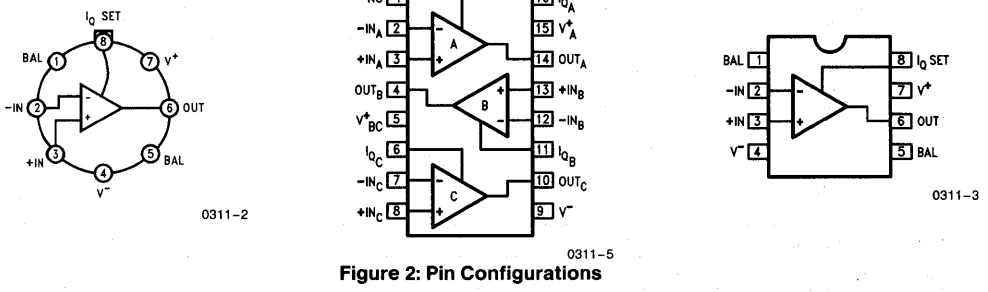
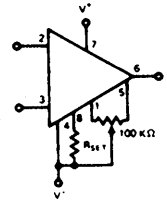


Figure 2: Pin Configurations

NOTE: All typical values have been characterized but are not tested.



0311-6

Figure 3: Voltage Offset Null Circuit

ELECTRICAL CHARACTERISTICS ($V_{SUPPLY} = \pm 6V$, $I_Q = 30\mu A$, unless otherwise specified.)

Characteristics	Test Conditions	8021M			8021C			Units
		Min	Typ	Max	Min	Typ	Max	
The following specifications apply for $T_A = 25°C$:								
Input Offset Voltage	$R_S \leq 100k\Omega$		2	3		2	6	mV
Input Offset Current			0.5	7.5		0.7	10	nA
Input Bias Current			5	20		7	30	nA
Input Resistance(1)		3	10		3	10		MΩ
Input Voltage Range	$V_{SUPPLY} = \pm 15V$	±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	80		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		30	150		30	150	μV/V
Output Resistance	Open Loop		2			2		kΩ
Output Voltage Swing	$R_L \geq 20k\Omega$, $V_{SUPPLY} = \pm 15V$	±12	±14		±12	±14		V
	$R_L \geq 10k\Omega$, $V_{SUPPLY} = \pm 15V$	±11	±13		±11	±13		V
Output Short-Circuit Current			±13			±13		mA
Power Consumption	$V_{OUT} = 0$		360	480		360	600	μW
Slew Rate (Unity Gain)			0.16			0.16		V/μs
Unity Gain Bandwidth	$R_L = 20k\Omega$, $V_{IN} = 20mV$		270			270		kHz
Transient Response (Unity Gain) Risetime Overshoot	$R_L = 20k\Omega$, $V_{IN} = 20mV$		 1.3 10			 1.3 10		 μs %
Specifications Applicable over Temperature		$-55°C \leq T_A \leq +125°C$			$0°C \leq T_A \leq +70°C$			
Input Offset Voltage	$R_S \leq 10k\Omega$		2.0	5.0		2.0	7.5	mV
Input Offset Current			1.0	11		1.5	15	nA
Input Bias Current			10	32		15	50	nA
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 10k\Omega$		5			5		μV/°C
Average Temperature Coefficient of Input Offset Current			1.7			0.8		pA/°C
Large Signal Voltage Gain	$R_L = 10k\Omega$	50	200		50	200		V/mV
Output Voltage Swing	$R_L \geq 10k\Omega$	±10	±13		±10	±13		V

NOTE 1: Not tested; guaranteed by design and process.

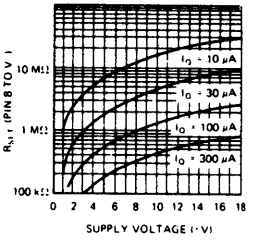
NOTE: All typical values have been characterized but are not tested.

QUIESCENT CURRENT ADJUSTMENT

QUIESCENT CURRENT SETTING RESISTOR (PIN 8 to V^-)

V_S	I_Q			
	10μA	30μA	100μA	300μA
±1.5	1.5MΩ	470kΩ	150kΩ	–
±3	3.3MΩ	1.1MΩ	330kΩ	100kΩ
±6	7.5MΩ	2.7MΩ	750kΩ	220kΩ
±9	13MΩ	4MΩ	1.3MΩ	350kΩ
±12	18MΩ	5.6MΩ	1.5MΩ	510kΩ
±15	22MΩ	7.5MΩ	2.2MΩ	620kΩ

QUIESCENT CURRENT SETTING RESISTOR (PIN 8 to V^-)

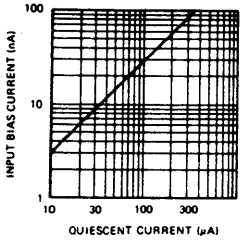


0311-7

TYPICAL PERFORMANCE CHARACTERISTICS*

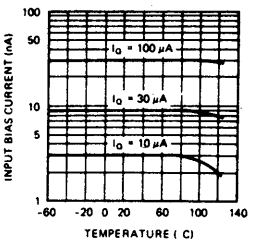
(T_A = +25°C, V_S = ±6V, I_Q = 30μA unless otherwise specified.)

INPUT BIAS CURRENT VS QUIESCENT CURRENT



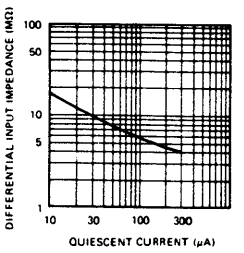
0311-8

INPUT BIAS CURRENT VS AMBIENT TEMPERATURE



0311-9

DIFFERENTIAL INPUT IMPEDANCE VS QUIESCENT CURRENT



0311-10

$$I_{SET} = \frac{V^+ + |V^-| - 0.6V}{R_{SET} + 5\,k\Omega}$$

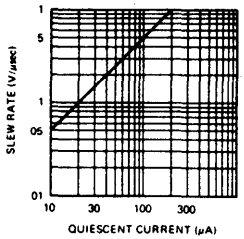
$$I_Q = \frac{I_{SET} + 3 \times 10^{-7}}{0.165}$$

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS*

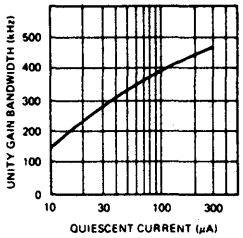
($T_A = +25°C$, $V_S = \pm 6V$, $I_Q = 30\mu A$ unless otherwise specified.) (Continued)

SLEW RATE VS QUIESCENT CURRENT



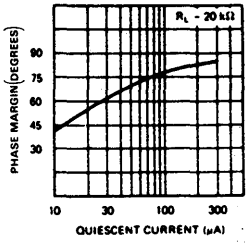
0311-11

FREQUENCY RESPONSE VS QUIESCENT CURRENT



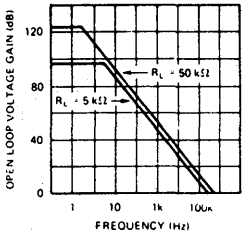
0311-12

PHASE MARGIN VS QUIESCENT CURRENT



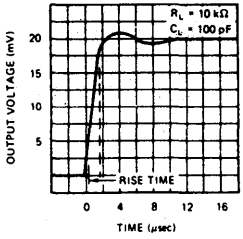
0311-13

OPEN-LOOP FREQUENCY RESPONSE



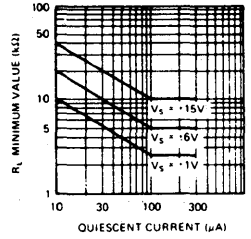
0311-14

TRANSIENT RESPONSE



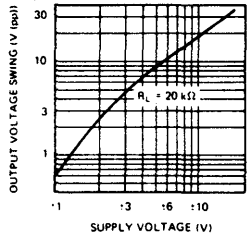
0311-15

MAXIMUM LOAD VS QUIESCENT CURRENT



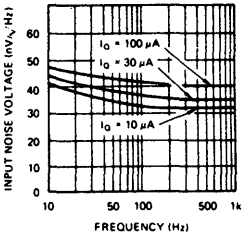
0311-16

OUTPUT VOLTAGE SWING VS SUPPLY VOLTAGE



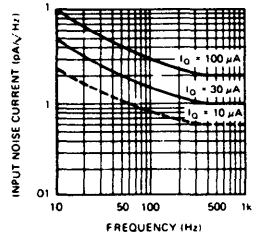
0311-17

EQUIVALENT INPUT NOISE VOLTAGE VS FREQUENCY



0311-18

EQUIVALENT INPUT NOISE CURRENT VS FREQUENCY



0311-19

*ICL8021C guaranteed only for $0°C \leq T_A \leq +70°C$

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

LM4250
Programmable Operational Amplifier

GENERAL DESCRIPTION

The 4250 is an extremely versatile programmable monolithic operational amplifier. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product.

The 4250C is guaranteed over a 0°C to 70°C temperature range.

RESISTOR BIASING

Set Current Setting Resistor to V⁻

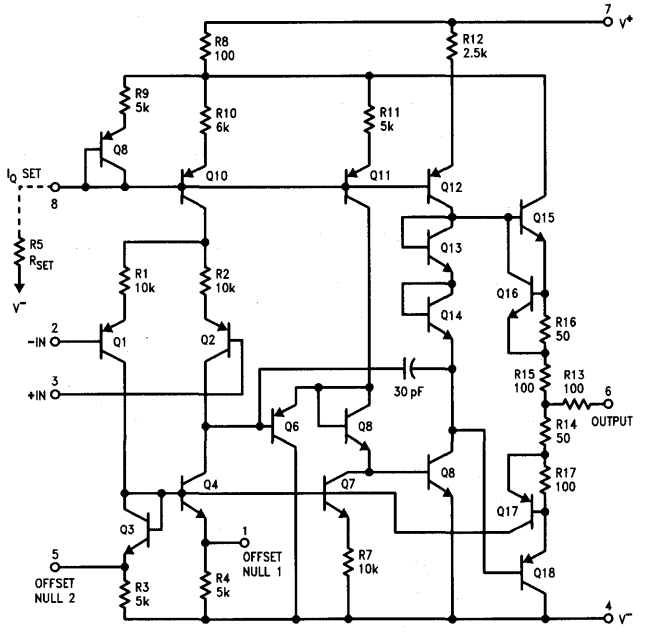
	I_{SET}				
V_S	0.1 μA	0.5 μA	1.0 μA	5 μA	10 μA
±1.5V	25.6 MΩ	5.04 MΩ	2.5 MΩ	492 kΩ	244 kΩ
±3.0V	55.6 MΩ	11.0 MΩ	5.5 MΩ	1.09 MΩ	544 kΩ
±6.0V	116 MΩ	23.0 MΩ	11.5 MΩ	2.29 MΩ	1.14 MΩ
±9.0V	176 MΩ	35.0 MΩ	17.5 MΩ	3.49 MΩ	1.74 MΩ
±12.0V	236 MΩ	47.0 MΩ	23.5 MΩ	4.69 MΩ	2.34 MΩ
±15.0V	296 MΩ	59.0 MΩ	29.5 MΩ	5.89 MΩ	2.94 MΩ

FEATURES

- **±1V to ±18V Power Supply Operation**
- **3 nA Input Offset Current**
- **Standby Power Consumption as Low as 500 nW**
- **No Frequency Compensation Required**
- **Programmable Electrical Characteristics**
- **Offset Voltage Nulling Capability**
- **Can be Powered by Two Flashlight Batteries**
- **Short Circuit Protection**

ORDERING INFORMATION

Part Number	Temperature Range	Package
LM4250 CN	0°C to +70°C	8 Lead MINIDIP
LM4250 CJ	0°C to +70°C	8 Lead CERDIP
LM4250 CH	0°C to +70°C	TO-99 CAN
LM4250 J	−55°C to +125°C	8 Lead CERDIP
LM4250 H	−55°C to +125°C	TO-99 CAN



$$I_{SET} = \frac{V^+ + |V^-| - 0.6V}{R_{SET} + 5k}$$

$$I_{SUPPLY} = \frac{I_{SET} + 3 \times 10^{-7}}{0.165}$$

Figure 1: Functional Diagram

HARRIS SEMICONDUCTOR, 2450 Walsh Avenue, Santa Clara, Ca. 95051

NOTE: All typical values have been characterized but are not tested.

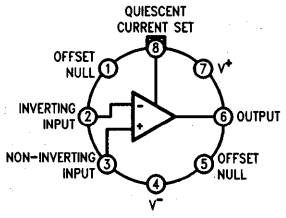
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Power Dissipation (Note 1) ..... 500 mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V
I_{SET} Current ..... 150 μA
Operating Temperature Range
LM4250C ..... 0°C to +70°C
LM4250 ..... −55°C to +125°C

Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Top View



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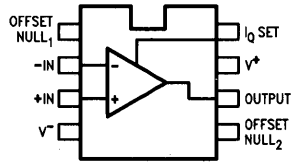

0108-2

Figure 2: Pin Configurations

ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ +70°C unless otherwise specified)

Parameters	Conditions	V_S = ±1.5V			
		I_{SET} = 1 μA		I_{SET} = 10 μA	
		Min	Max	Min	Max
V_{OS}	T_A = 25°C, R_S ≤ 100 kΩ		5 mV		6 mV
I_{OS}	T_A = 25°C		6 nA		20 nA
I_{bias}	T_A = 25°C		10 nA		75 nA
Large Signal Voltage Gain	T_A = 25°C, R_L = 100 kΩ V_O = ± 0.6V, R_L = 10 kΩ	25k		25k	
Supply Current	T_A = 25°C		8 μA		90 μA
Power Consumption	T_A = 25°C		24 μW		270 μW
V_{OS}	R_S ≤ 10 kΩ		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	V_O = ±0.6V, R_L = 100 kΩ R_L = 10 kΩ	25k		25k	
Output Voltage Swing	R_L = 100 kΩ R_L = 10 kΩ	±0.6V		±0.6V	
Common Mode Rejection Ratio	R_S ≤ 10 kΩ	70 dB		70 dB	
Supply Voltage Rejection Ratio	R_S ≤ 10 kΩ	65 dB		65 dB	
Supply Current			8 μA		90 μA
Power Consumption			24 μW		270 μW

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (0°C ≤ T_A ≤ +70°C unless otherwise specified) (Continued)

Parameters	Conditions	V_S = ±15V			
		I_{SET} = 1 μA		I_{SET} = 10 μA	
		Min	Max	Min	Max
V_{OS}	T_A = 25°C, R_S ≤ 100 kΩ		5 mV		6 mV
I_{OS}	T_A = 25°C		6 nA		20 nA
I_{bias}	T_A = 25°C		10 nA		75 nA
Large Signal Voltage Gain	T_A = 25°C, R_L = 100 kΩ V_O = ±10V, R_L = 10 kΩ	60k		60k	
Supply Current	T_A = 25°C		11 μA		100 μA
Power Consumption	T_A = 25°C		330 μW		3 mW
V_{OS}	R_S ≤ 10 kΩ		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	V_O = ±10V, R_L = 100 kΩ R_L = 10 kΩ	50k		50k	
Output Voltage Swing	R_L = 100 kΩ R_L = 10 kΩ	±12V		±12V	
Common Mode Rejection Ratio	R_S ≤ 10 kΩ	70 dB		70 dB	
Supply Voltage Rejection Ratio	R_S ≤ 10 kΩ	74 dB		74 dB	
Supply Current			11 μA		100 μA
Power Consumption			300 μW		3 mW

NOTE 1: Derate linearly at −6.7 mW/°C for ambient temperatures above +95°C for the military temperature range. Derate linearly at −6.3 mW/°C for ambient temperatures above +45°C for the commercial temperature range.

2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$ unless otherwise specified)

Parameters	Conditions	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$T_A = 25°C$, $R_S \leq 100\ k\Omega$		6 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$T_A = 25°C$, $R_L = 100\ k\Omega$ $V_O = \pm 0.6V$, $R_L = 10\ k\Omega$	25k		25k	
Supply Current	$T_A = 25°C$		8 μA		90 μA
Power Consumption	$T_A = 25°C$		24 μW		270 mW
V_{OS}	$R_S \leq 10\ k\Omega$		7.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		±0.6V		±0.6V	
Large Signal Voltage Gain	$V_O = \pm 0.5V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	25k		25k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	±0.6V		±0.6V	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	65 dB		65 dB	
Supply Current			8 μA		90 μA
Power Consumption			24 μW		270 μW

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq +125°C$ unless otherwise specified) (Continued)

Parameters	Conditions	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		Min	Max	Min	Max
V_{OS}	$T_A = 25°C$, $R_S \leq 100\ k\Omega$		6 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$T_A = 25°C$, $R_L = 100\ k\Omega$ $V_O = \pm 10V$, $R_L = 10\ k\Omega$	60k		60k	
Supply Current	$T_A = 25°C$		11 μA		100 μA
Power Consumption	$T_A = 25°C$		330 μW		3 mW
V_{OS}	$R_S \leq 10\ k\Omega$		7.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		$\pm 13.5V$		$\pm 13.5V$	
Large Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	50k		50k	
Output Voltage Swing	$R_L = 100\ k\Omega$ $R_L = 10\ k\Omega$	$\pm 12V$		$\pm 12V$	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	74 dB		74 dB	
Supply Current			11 μA		100 μA
Power Consumption			300 μW		3 mW

NOTE: All typical values have been characterized but are not tested.

Operational Amplifiers Glossary

AVERAGE INPUT OFFSET CURRENT DRIFT - The average change in offset current between room (+25°C) and high temperature (+125°C, +85°C or +75°C) or between room temperature and low temperature (0°C, -25°C or -55°C) divided by the temperature difference.

AVERAGE OFFSET VOLTAGE DRIFT - The average change in offset voltage between room (+25°C) and high temperature (+125°C, +85°C or +75°C) or between room temperature and low temperature (0°C, -25°C or -55°C) divided by the temperature difference.

CHANNEL SEPARATION - The ratio of the output of a driven amplifier to the output (referred to input) of an adjacent undriven amplifier.

COMMON MODE INPUT VOLTAGE (V_{IC}) - The average of the voltages present at the differential input terminals.

COMMON MODE INPUT VOLTAGE RANGE (V_{ICR}) - The range of voltage that if exceeded at either input terminal will cause the amplifier to cease operating properly.

COMMON MODE REJECTION RATIO (CMRR) - The ratio of change in input offset voltage to change in input common-mode voltage, expressed in dB.

$$CMRR = 20 \times \log_{10}\left(\frac{VIO}{VCM}\right)$$

COMMON MODE RESITANCE (r_{ic}) - The ratio of change in input common-mode voltage to the resulting change in input current.

DIFFERENTIAL INPUT RESISTANCE (r_{id}) - The ratio of change in input differential voltage (small-signal, assumes amplifier operating linearly) to the resulting change in differential input current.

FULL POWER BANDWIDTH (FPBW) - The maximum frequency at which a full scale undistorted (THD $\leq$ 1%) sine wave can be obtained at the output of the amplifier.

GAIN BANDWIDTH (GBW) - The open-loop gain of an op amp (in V/V) at a mid-band, linear-region frequency (usually between 1KHz and 10KHz) times that frequency (in Hz). GBW = $[A_{VOL}] \bullet f$

INPUT BIAS CURRENT (I_{BIAS}) - The average of the currents flowing into or out of the input terminals when the output is at zero volts.

INPUT CAPACITANCE (C_{IN}) - The equivalent capacitance seen looking into either input terminal.

INPUT NOISE CURRENT (i_n) - The input noise current that would reproduce the noise seen at the output if all amplifier noise sources were set to zero and the source impedances were large compared to the optimum source impedance.

INPUT OFFSET CURRENT (I_{OS}) - The difference in the currents flowing into the two input terminals when the output is at zero volts.

INPUT OFFSET VOLTAGE (V_{OS}) - The differential D.C. voltage required to zero the output voltage with no input signal or load. Input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT NOISE VOLTAGE (e_n) - The input noise voltage that would reproduce the noise seen at the output if all the amplifier noise sources and source resistances were set to zero.

LARGE SIGNAL VOLTAGE GAIN (A_V) - The ratio of the peak to peak output voltage swing (over a specified range) to the change in input voltage required to drive the output.

OUTPUT CURRENT (I_{OUT}) - The output current available from the amplifier at some specified output voltage.

OUTPUT RESISTANCE (RO) - The ratio of the change in output voltage to the change in output current.

OUTPUT SHORT CIRCUIT CURRENT (I_{SC}) - The output current available from the amplifier with the output shorted to ground (or other specified potential).

OUTPUT VOLTAGE SWING (V_{OUT}) - The maximum output voltage swing, referred to ground, that can be obtained under specified loading conditions.

OVERSHOOT - Peak excursion above final value of an output step response.

POWER SUPPLY REJECTION RATIO (PSRR) - The ratio of the change in input offset voltage to the change in power supply voltage producing it.

RISE TIME (t_r) - The time required for an output voltage step to change from 10% to 90% of its final value, when the input is subjected to a small-signal voltage pulse.

SETTLING TIME ($t_{set.}$) - The time required, after application of a step input signal, for the output voltage to settle and remain within a specified error band around the final value.

SLEW RATE (SR) - The rate of change of the output under large-signal conditions. Slew rate may be specified separately for both positive and negative going changes.

SUPPLY CURRENT (I_S) - The current required from the power supply to operate the amplifier with no load and the output at zero volts.

SUPPLY VOLTAGE RANGE - The range of power supply voltage over which the amplifier may be safely operated.

UNITY GAIN BANDWIDTH - The frequency range from D.C. to that frequency where the amplifiers open loop gain is unity.

LINEAR 4

COMPARATORS

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COMPARATORS DATA SHEETS		
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Selection Guide

COMPARATORS

General Purpose Electrical Characteristics, $T_A = 25^oC$

Type	V_{IO} Max. mV	I_I Max. nA	I^+ Max. Ma	Max. V^+, V^-	A_{OL} (Min.) dB	Unity Gain BW Typ. MHz	SR (Typ.) V/μs	Pkg. No. of Pins*
Single-Unit Types								
CA311	7.5	250	8	±8	106	Response Time (1)		8E, S, T
Dual-Unit Types								
CA3290	20	50pA	3	±18	88	Response Time (2)		8E, S, T 14E1
CA3290A	10	40pA	3	±18	88			
Quad-Unit Types								
CA139	5	100	8	±18	-	Response Time (3)		14E
CA139A	2	100	8	±18	94			14E
CA239	5	250	2	±18	-			14E
CA239A	2	250	2	±18	94			14E
CA339	5	250	2	±18	94			14E
CA339A	2	250	2	±18	94			14E

*See Packaging Section.

Response Time:

1 - 200 ns
2 - tr = 1.2 μs, tf = 200 ns
3 - tr = 1.3 μs, tf = 300 ns

Type	V_{IO} mV	I_{IO} nA	Comments	Response Time	Pkg. No. of Pins*
HA-4900	2	10	Single or dual supply. Analog and logic supplies separated for easier interface and noise immunity	130ns	16
HA-4902	2	10		130ns	16
HA-4905	4	25		130ns	16

High-Speed

Type	Comments	Propagation Delay ns	Tracking Bandwidth MHz
HFA-0003	New Product in Development	< 3	300

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

Voltage Comparators

CA139, CA139A, CA239, CA239A, CA339, CA339A, LM339*, LM339A*

May 1990

Quad Voltage Comparators

For Industrial, Commercial, and Military Applications

Features:

- *Operation from single or dual supplies*
- *Common mode input voltage range to ground*
- *Output voltage compatible with TTL, DTL, ECL, MOS and CMOS*
- *Differential input voltage range equal to the supply voltage*
- *Maximum input offset voltage (V_{IO}):*
  CA139A, CA239A, CA339A - 2 mV
  CA139, CA239, CA339 - 5 mV
- *Replacement for industry types 139, 239, 339, 139A, 239A, and 339A*

Applications:

- *Square wave generators*
- *Time delay generators*
- *Pulse generators*
- *Multivibrators*
- *High voltage digital logic gates*
- *A/D converters*
- *MOS clock timers*

The CA139, CA239, CA339, CA139A, CA239A, and CA339A types consist of four independent single or dual supply voltage comparators on a single monolithic substrate. The common mode input voltage range includes ground even when operated from a single supply, and the low power sypply current drain makes these comparators suitable for battery operation. These types were designed to directly interface with TTL and CMOS.

Types CA139A, CA239A, and CA339A have all the features and characteristics of their prototype counter parts CA139, CA239, and CA339 plus an even lower input offset voltage characteristic. These devices are supplied in a 14-lead Small Outline package (M suffix), in a 14-lead dual-in-line plastic package (E suffix) and in a 14-lead dual-in-line hermetic (frit-seal) ceramic package (F suffix). The CA339 is also available in chip form (H suffix).

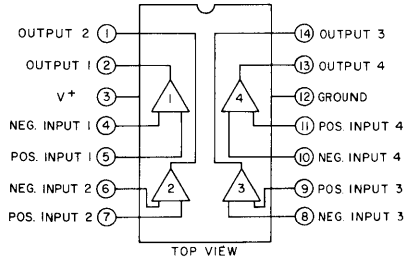


Figure 1 - Functional diagram.

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

File Number **795**

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$:*

DC SUPPLY VOLTAGE	36 V or ±18 V
DC DIFFERENTIAL INPUT VOLTAGE	±36 V
INPUT VOLTAGE	−0.3 V to +36 V
INPUT CURRENT ($V_I < -0.3$ V)*	50 mA
OUTPUT SHORT CIRCUIT TO GROUND▲	
(Single Supply)	Continuous
DEVICE DISSIPATION:	
Up to T_A = 55°C	750 mW
Above T_A = 55°C	derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:	
Operating	−55 to +125°C
Storage	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)	
from case for 10 seconds max.	+265°C

* Inputs must not go more negative than −0.3 V.

▲Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current independent of V^+ is approximately 20 mA.

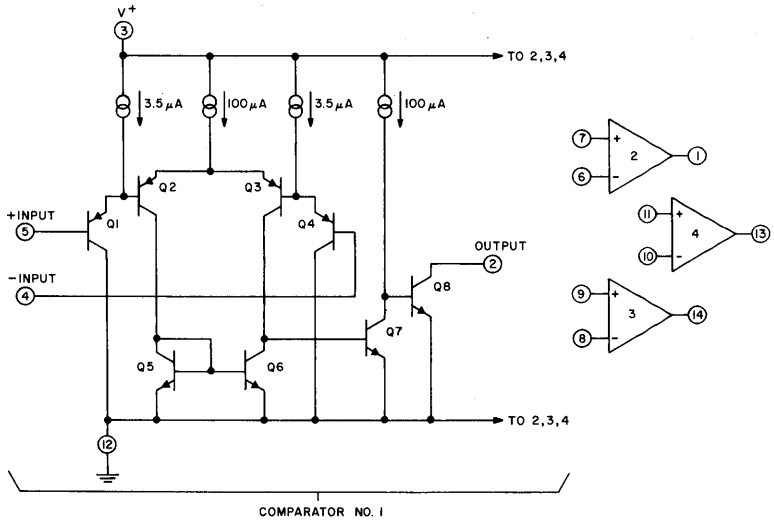


Fig. 2—Schematic diagram.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
	$V^+ = 5$ V, Unless otherwise indicated		CA139			CA139A			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage (V_{IO}) At Output Switch Point $V \cong 1.4$ V	V_{REF} = 1.4 V, $R_S = 0$	25°C	–	2	5	–	1	2	mV
		Note 1	–	–	9	–	–	4	
Differential Input Voltage (V_{ID})	Keep all inputs ⩾0 V for V^- (If used), Notes 1, 2		–	–	36	–	–	36	V
Saturation Voltage (V_{sat})	$V_I^- = 1$ V, $V_I^+ = 0$ V, $I_{SINK} \leqslant$ 4 mA	25°C	–	250	400	–	250	400	mV
		Note 1	–	–	700	–	–	700	
Common-Mode Input Voltage Range (V_{ICR})	Note 3	25°C	0	–	$V^+-1.5$	0	–	$V^+-1.5$	V
		Note 1	0	–	V^+-2	0	–	V^+-2	
Input Offset Current (I_{IO})	$I_I^+ - I_I^-$	25°C	–	3	25	–	3	25	nA
		Note 1	–	–	100	–	–	100	
Input Bias Current (I_{IB})	I_I^+ or I_I^- with Output in Linear Range	25°C	–	25	100	–	25	100	nA
		Note 1	–	–	300	–	–	300	
Total Supply Current (I^+)	$R_L = \infty$ on all comparators, T_A = 25°C		–	0.8	2	–	0.8	2	mA
Output Leakage Current	$V_I^+ \geqslant 1$ V, $V_I^- = 0$, $V_O = 5$ V	25°C	–	0.1	–	–	0.1	–	nA
	$V_I^+ \geqslant 1$ V, $V_I^- = 0$, $V_O = 30$ V	Note 1	–	–	1	–	–	1	μA
Output Sink Current	$V_I^- \geqslant 1$ V, $V_I^+ = 0$, $V_O \leqslant +1.5$ V, T_A = 25°C		6	16	–	6	16	–	mA
Voltage Gain (A_{OL})	$R_L \geqslant 15$ kΩ, $V^+ = 15$ V, T_A = 25°C		–	200	–	50	200	–	V/mV
Large Signal Response Time	V_I = TTL Logic Swing, V_{REF} = +1.4 V, $V_{RL} = 50$ V, $R_L = 5.1$ kΩ, T_A = 25°C		–	300	–	–	300	–	ns
Response Time See Figs. 5 & 6	$V_{RL} = 5$ V, $R_L = 5.1$ kΩ, T_A = 25°C		–	1.3	–	–	1.3	–	μs

Note 1: Ambient Temperature (T_A) applicable over operating temperature range as shown below.

CA139 / CA139A	CA239 / CA239A	CA339 / CA339A
(−55 to +125°C)	(−25 to +85°C)	(0 to +70°C)

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than −0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is $(V^+) - 1.5$ V, but either or both inputs can go to +30 V without damage.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS (V^+ = 5 V Unless otherwise indicated)		LIMITS						UNITS
			CA239, CA339			CA239A, CA339A			
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage (V_{IO}) At Output Switch Point V ≅ 1.4 V	V_{REF} = 1.4 V, R_S = 0	25°C	–	2	5	–	1	2	mV
		Note 1	–	–	9	–	–	4	
Differential Input Voltage (V_{ID})	Keep all inputs ⩾0 V for V^- (If used), Notes 1, 2		–	–	36	–	–	36	V
Saturation Voltage (V_{sat})	V_I^- = 1 V, V_I^+ = 0 V, I_{SINK} ⩽ 4 mA	25°C	–	250	400	–	250	400	mV
		Note 1	–	–	700	–	–	700	
Common-Mode Input Voltage Range (V_{ICR})	Note 3	25°C	0	–	V^+–1.5	0	–	V^+–1.5	V
		Note 1	0	–	V^+–2	0	–	V^+–2	
Input Offset Current (I_{IO})	$I_I^+ - I_I^-$	25°C	–	5	50	–	5	50	nA
		Note 1	–	–	150	–	–	150	
Input Bias Current (I_{IB})	I_I^+ or I_I^- with Output in Linear Range	25°C	–	25	250	–	25	250	nA
		Note 1	–	–	400	–	–	400	
Total Supply Current (I^+)	R_L = ∞ on all comparators, T_A = 25°C		–	0.8	2	–	0.8	2	mA
Output Leakage Current	V_I^+ ⩾1 V, V_I^- = 0, V_O = 5 V	25°C	–	0.1	–	–	0.1	–	nA
	V_I^+ ⩾1 V, V_I^- = 0, V_O = 30 V	Note 1	–	–	1	–	–	1	μA
Output Sink Current	V_I^- ⩾1 V, V_I^+ = 0, V_O ⩽+1.5 V, T_A = 25°C		6	16	–	6	16	–	mA
Voltage Gain (A_{OL})	R_L ⩾15 kΩ V^+=15 V, T_A = 25°C		–	200	–	50	200	–	V/mV
Large Signal Response Time	V_I = TTL Logic Swing, V_{REF} = +1.4 V, V_{RL} = 50 V, R_L = 5.1 kΩ, T_A = 25°C		–	300	–	–	300	–	ns
Response Time See Figs. 5 & 6	V_{RL} = 5 V, R_L = 5.1 kΩ, T_A = 25°C		–	1.3	–	–	1.3	–	μs

Note 1: Ambient Temperature (T_A) applicable over operating temperature range as shown below.
CA139, CA139A (–55 to +125°C) CA239, CA239A (–25 to +85°C) CA339, CA339A (0 to +70°C)

Note 2: The comparator will provide a proper output state even if the positive swing of the inputs exceeds the power supply voltage level, if the other input remains within the common-mode voltage range. The low input voltage state must not be less than –0.3 V (or 0.3 V below the magnitude of the negative power supply, if used).

Note 3: The upper end of the common-mode voltage range is (V^+) – 1.5 V, but either or both inputs can go to +30 V without damage.

TYPICAL CHARACTERISTICS

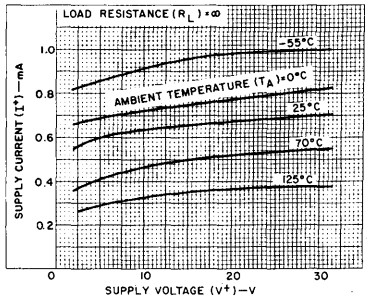


Fig. 3—Supply current vs. supply voltage.

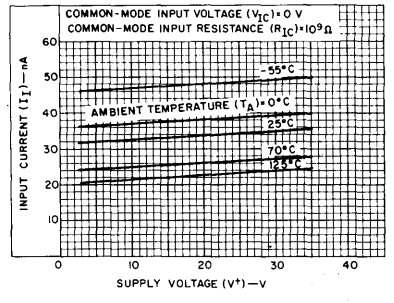


Fig. 4—Input current vs. supply voltage.

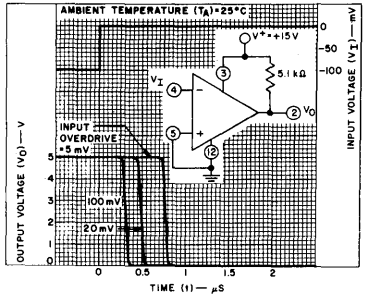


Fig. 5—Response time for various input overdrives—negative transition.

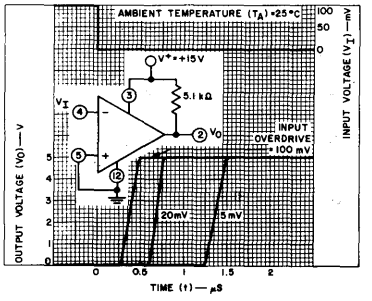


Fig. 6—Response time for various input overdrives—positive transition.

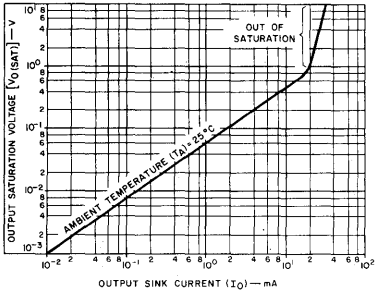
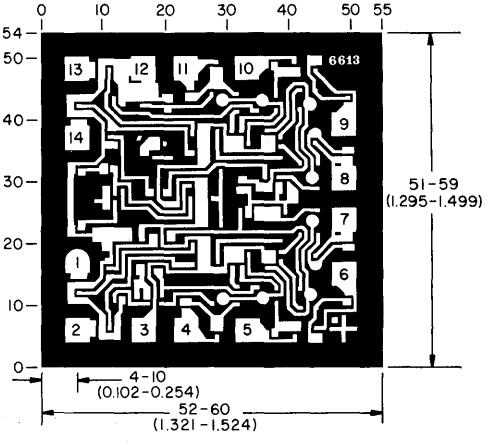


Fig. 7—Output saturation voltage vs. output sink current.

Chip Version (CA339H)



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Voltage Comparators

CA311, LM311*

May 1990

Voltage Comparator

For Commercial and Industrial Applications

Features:

- *Single- or dual-supply operation*
- *Power consumption - 135 mW at ±15 V*
- *Strobe capability*
- *Low input-offset current - 6 nA(typ.)*
- *Differential input-voltage range - ±30 V*
- *Directly interchangeable with National Semiconductor LM311 Series*

Applications:

- *Multivibrators*
- *Positive and negative peak detectors*
- *Crystal oscillators*
- *Zero-crossing detectors*
- *Solenoid, relay, and lamp drivers*

The CA311 is a monolithic voltage comparator that operates from dual supplies up to ±15 V, or from single supplies down to 5 V. This single supply capability makes the outputs of these devices compatible with RTL, DTL, TTL, and MOS circuits. In addition they can drive lamps or relays, and switch voltages up to 40 V at currents as high as 50 mA.

The inputs and outputs of the CA311 can be isolated from system ground, allowing the output to drive loads referred to ground V+, or V-.

The CA311 is available in 8-lead TO-5 style packages with standard leads (T suffix), dual-in-line formed leads ("DIL-CAN", S suffix), 8-lead dual-in-line plastic package ("MINI-DIP", E suffix), and in chip form (H suffix).

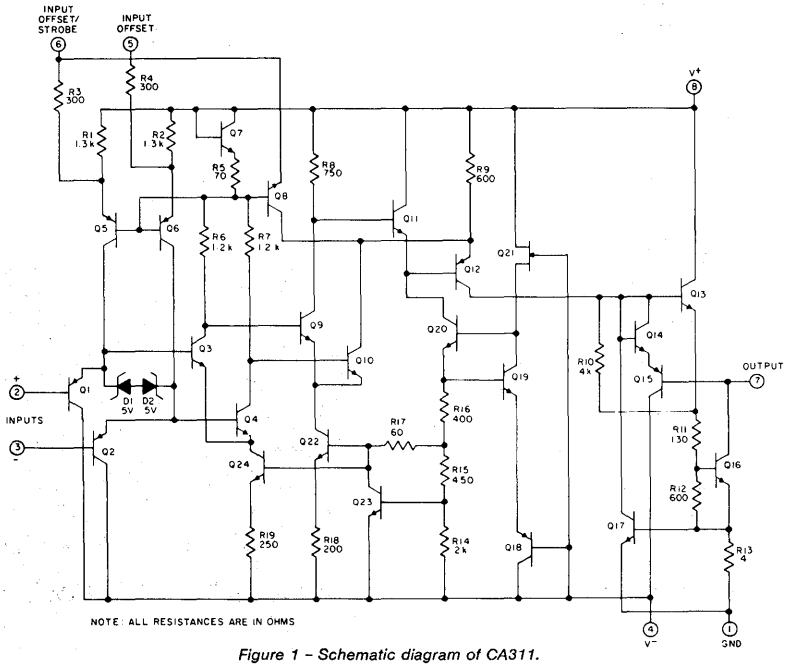


Figure 1 - Schematic diagram of CA311.

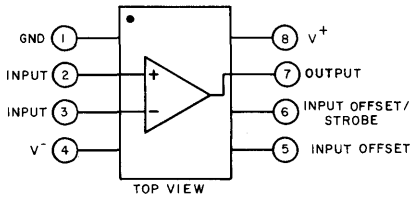
*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

Maximum Ratings, *Absolute Maximum Values at T_A = 25° C:*

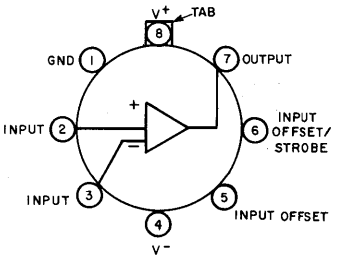
DC SUPPLY VOLTAGE (between V+ and V⁻ terminals) ..... 36 V
DC INPUT VOLTAGE* ..... ±15 V
DIFFERENTIAL INPUT VOLTAGE ..... ±30 V
OUTPUT TO NEGATIVE SUPPLY VOLTAGE (V_{7-4}) ..... 40 V
GROUND TO NEGATIVE SUPPLY VOLTAGE (V_{1-4}) ..... 30 V
OUTPUT SHORT-CIRCUIT DURATION ..... 10 s
DEVICE DISSIPATION:
UP TO T_A = 25°C ..... 500 mW
Above T_A = 25°C ..... derate linearly at 6.67 mW/° C
AMBIENT TEMPERATURE RANGE:
Operating ..... 0 to +70° C†
Storage ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265° C

*This rating applies for ±15 V supplies. The positive input-voltage limit is 30 V above the negative supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply. The negative input-voltage limit is equal to the negative supply voltage or 30 V below the positive supply, whichever is less.

†Types CA311 E, S, and T can be operated over the temperature range of -55 to +125° C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to 70° C.



FUNCTIONAL DIAGRAM FOR PLASTIC PACKAGE.



FUNCTIONAL DIAGRAM FOR TO-5 STYLE PACKAGE.

TYPICAL CHARACTERISTICS

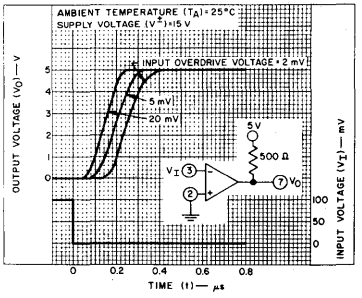


Fig. 2 - Response time for various input overdrive voltages - positive input.

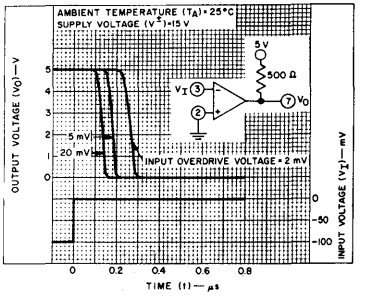


Fig. 3 - Response time for various input overdrive voltages - negative input.

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	TEST CONDITIONS		LIMITS			UNITS
	SUPPLY VOLTAGE (V±) = 15V UNLESS OTHERWISE SPECIFIED		CA311			
			MIN.	TYP.	MAX.	
Input Offset Voltage V_{IO}	$R_S \leq 5$ kΩ, Note 2	T_A = 25°C	—	2	7.5	mV
		Note 1	—	—	10	
Saturation Voltage	$V_I \leq$ -10 mV, I_O = 50 mA	T_A = 25°C	—	0.75	1.5	V
	$V^+ \geq$ 4.5 V, V^- -0, $V_I \leq$ -10 mV, $I_{SINK} \leq$ 8 mA	Note 1	—	0.23	0.4	
Input Voltage Range V_{IPP}		Note 1	—	±14	—	V
Input Offset Current I_{IO}	Note 2	T_A = 25°C	—	6	50	nA
		Note 1	—	—	70	
Input Bias Current I_{IB}	Note 2	T_A = 25°C	—	100	250	nA
		Note 1	—	—	300	
Postive Supply Current I^+		T_A = 25°C	—	5.1	7.5	mA
Negative Supply Current I^-		T_A = 25°C	—	4.1	5	mA
Output Leakage Current	$V_I \geq$ 10 mV, V_O = 35 V	T_A = 25°C	—	—	50	nA
Strobe on Current		T_A = 25°C	—	3	—	mA
Voltage Gain, A		T_A = 25°C	40	200	—	V/mV
Response Time	100 mV Input Step with 5 mV Overdrive Voltage	T_A = 25°C	—	200	—	ns
Input Voltage Range		T_A = 25°C	-14.5	13.8 -14.7	13	V

Note 1: Ambient temperature (T_A) over applicable operating temperature of 0 to + 70° C.

Note 2: The input offset characteristics given are the values required to drive the output to within 1 V of either supply with a 1 mA load. These characteristics define an error band which takes into account the worst-case effects of voltage gain and input impedance. The input offset voltage, input offset current, and input bias current specifications apply for any supply voltage from a 5 V single supply up to a ± 15 V dual supply.

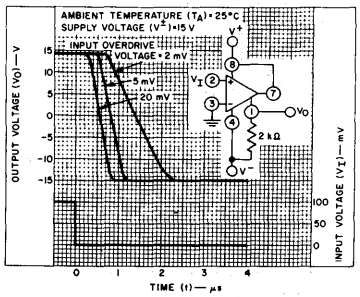


Fig. 4 - Response time for various input overdrive voltages - positive input.

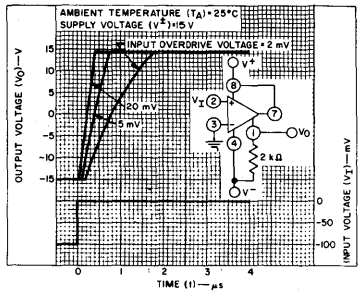


Fig. 5 - Response time for various input overdrive voltages - negative input.

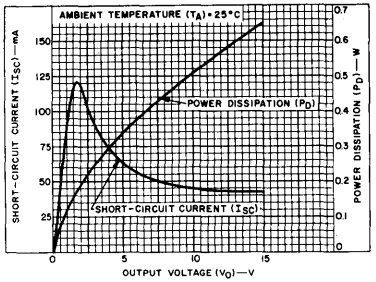


Fig. 6 - Output limiting characteristics.

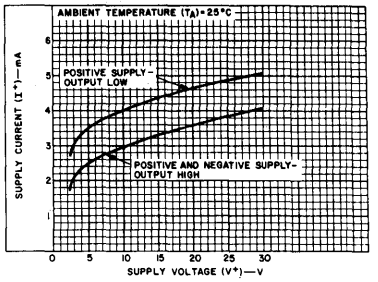


Fig. 7 - Supply current vs. supply voltage.

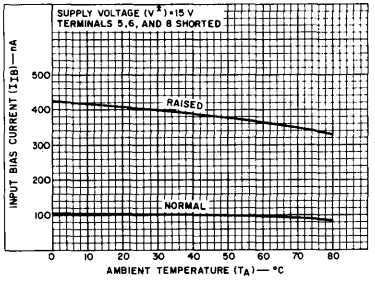


Fig. 8 - Input bias current vs. ambient temperature.

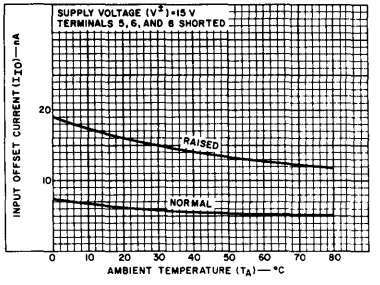


Fig. 9 - Input offset current vs. ambient temperature.

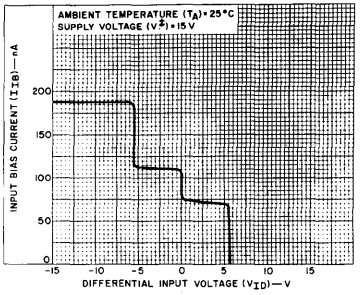


Fig. 10 - Input characteristics.

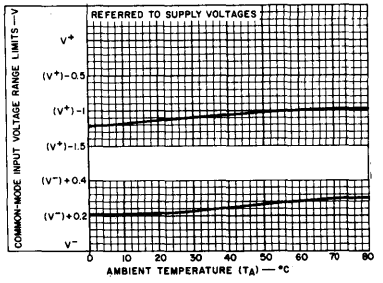


Fig. 11 - Common-mode voltage range limits vs. ambient temperature.

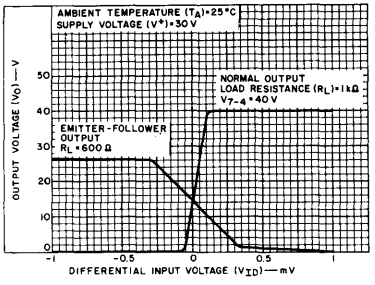


Fig. 12 - Transfer function.

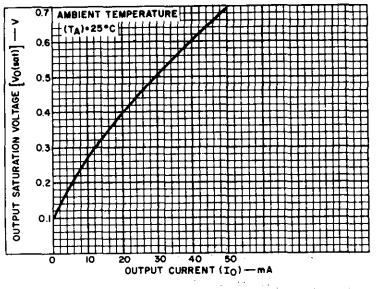


Fig. 13 - Output saturation voltage vs. output current.

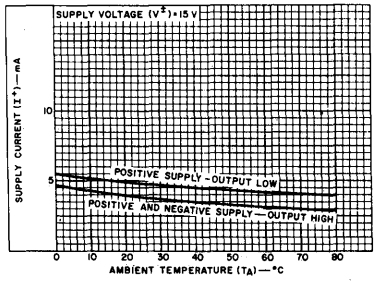


Fig. 14 - Supply current vs. ambient temperature.

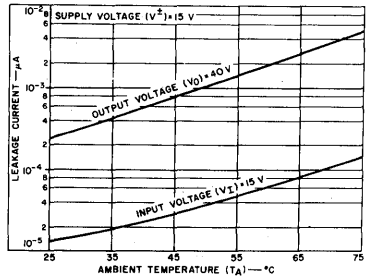


Fig. 15 - Input and output leakage current vs. ambient temperature.

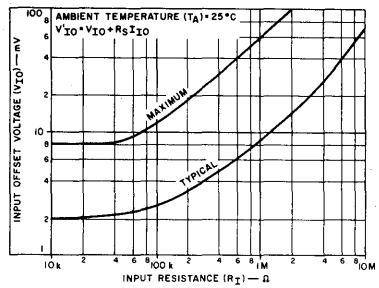


Fig. 16 - Offset error.

TYPICAL APPLICATIONS

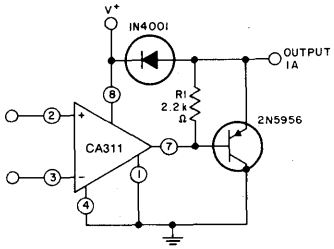


Fig. 17 - Comparator and solenoid driver.

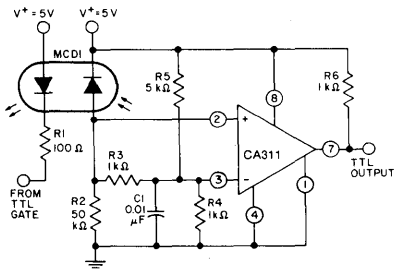


Fig. 18 - Digital transmission isolator.

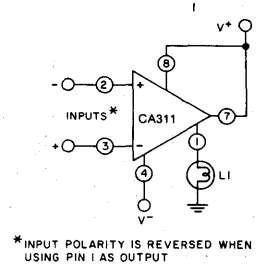


Fig. 19 - Driving a ground-referred load.

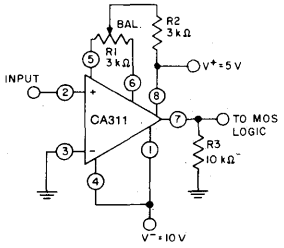


Fig. 20 - Zero-crossing detector driving MOS logic.

TYPICAL APPLICATIONS (cont'd)

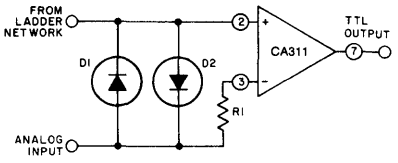


Fig. 21 - Using clamp diodes to improve response.

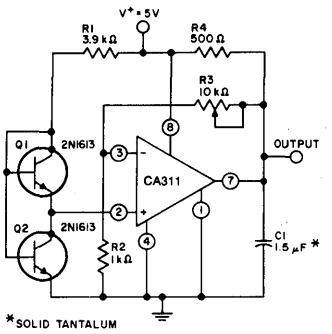


Fig. 22 - Low-voltage adjustable-reference supply.

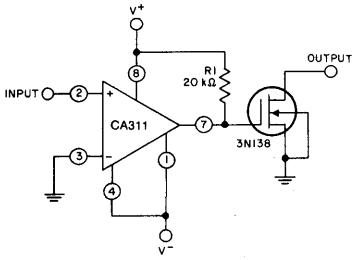


Fig. 23 - Zero-crossing detector driving and MOS switch.

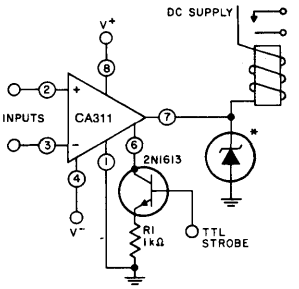


Fig. 24 - Relay driver with strobe.

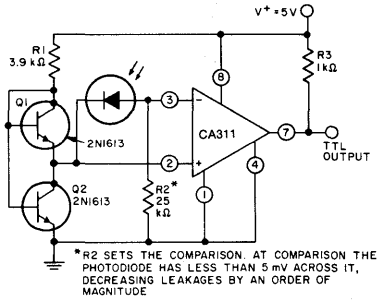


Fig. 25 - Precision photodiode comparator.

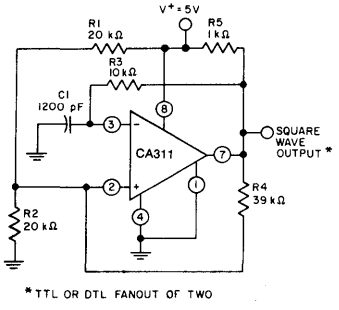


Fig. 26 - 100-kHz free-running multivibrator.

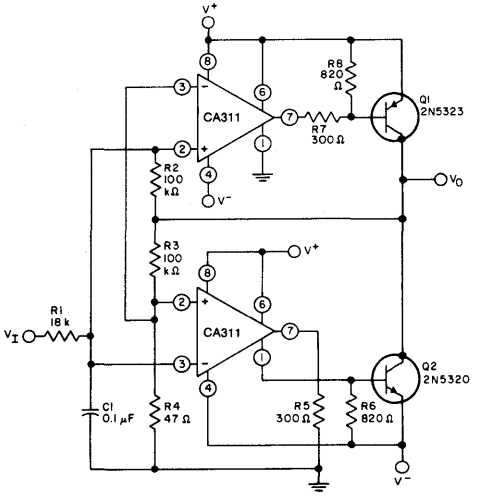


Fig. 27 - Switching power amplifier.

TYPICAL APPLICATIONS (cont'd)

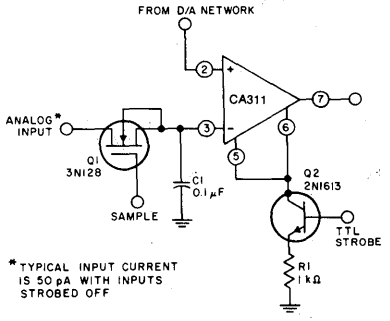


Fig. 28 - Strobing off both input and output stages.

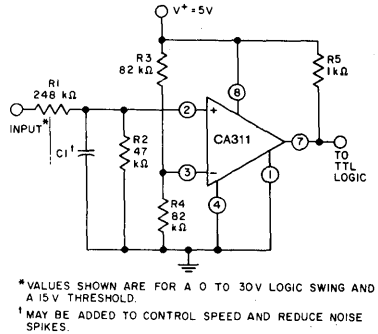


Fig. 29 - TTL interface with high-level logic.

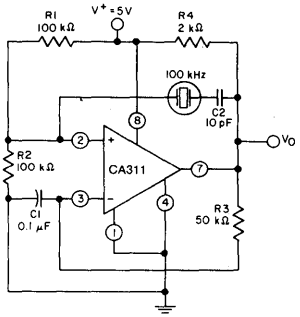


Fig. 30 - Crystal oscillator.

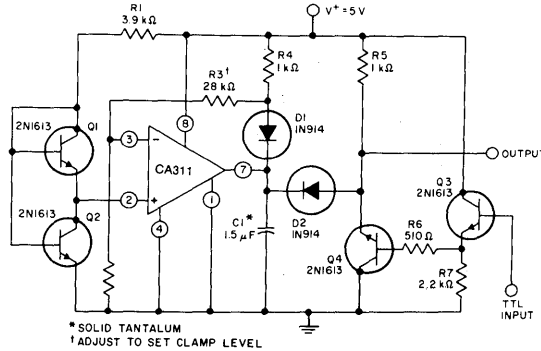


Fig. 31 - Precision squarer.

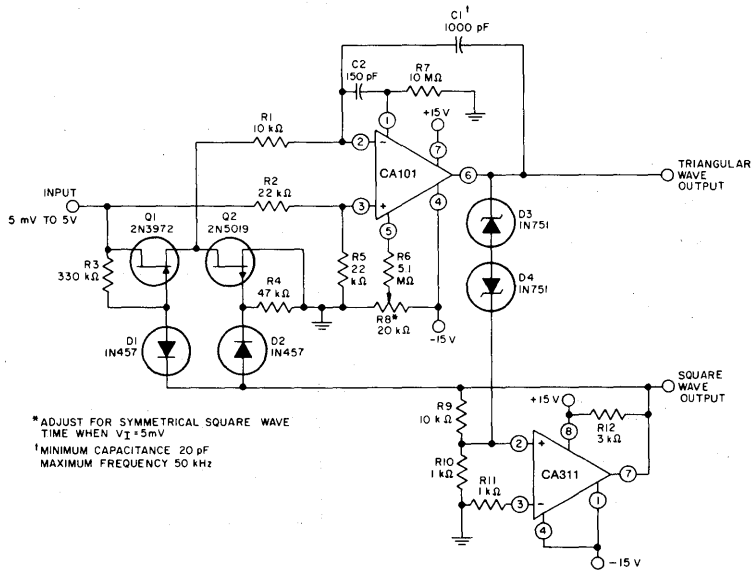


Fig. 32 - 10 Hz to 10 kHz voltage controlled oscillator.

TYPICAL APPLICATIONS (cont'd)

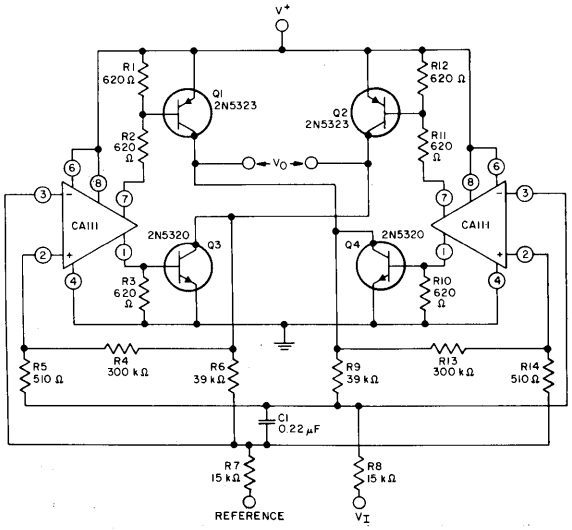
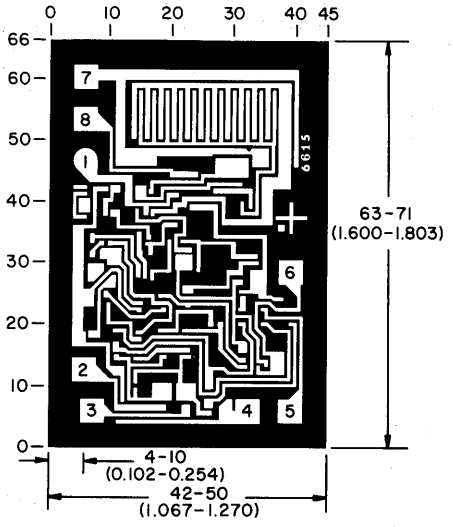


Fig. 33 - Switching power amplifier.



Dimensions and pad layout for CA311H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

NOT RECOMMENDED FOR NEW DESIGNS

May 1990

Programmable Schmitt Trigger - With Memory

Dual-Input Precision Level Detectors

Features:

- *Programmable operating current*
- *Micropower standby dissipation*
- *Direct control of currents up to 150 mA*
- *Low input on/off current of less than 1 nA for programmable bias current of 1 μA*
- *Built-in hysteresis: 20 mV max.*

Applications:

- *Control of relays, heaters, LEDS, lamps, photosensitive devices, thyristors, solenoids, etc.*
- *Signal reconditioning*
- *Phase and frequency modulators*
- *On/off motor switching*
- *Schmitt triggers, level detectors*
- *Time delays*
- *Overvoltage, overcurrent, overtemperature protection*
- *Battery-operated equipment*
- *Square and triangular-wave generators*

The CA3098 Programmable Schmitt Trigger is a monolithic silicon integrated circuit designed to control high-operating-current loads such as thyristors, lamps, relays, etc. The CA3098 can be operated with either a single power supply with maximum operating voltage of 16 volts, or a dual power supply with maximum operating voltage of ±8 volts. It can directly control currents up to 150 mA and operates with microwatt standby power dissipation when the current to be controlled is less than 30 mA. The CA3098 contains the following major circuit-function features (see Fig. 1):

1. Differential amplifiers and summer: the circuit uses two differential amplifiers, one to compare the input voltage with the "high" reference, and the other to compare the input with the "low" reference. The resultant output of the differential amplifiers actuates a summer circuit which delivers a trigger that initiates a change in state of a flip-flop.

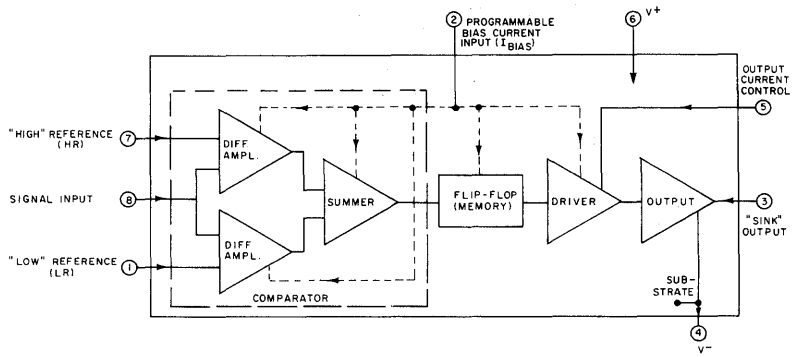


Figure 1 - Block diagram of CA3098 programmable Schmitt trigger.

2. Flip-flop: the flip-flop functions as a bistable "memory" element that changes state in response to each trigger command.
3. Driver and output stages: these stages permit the circuit to "sink" maximum peak load currents up to 150 mA at terminal 3.
4. Programmable operating current: the circuit incorporates access at terminal 2 to permit programming the desired quiescent operating current and performance parameters.

The CA3098 is supplied in the 8-lead dual-in-line plastic package ("Mini-Dip", E suffix), and in chip form (H suffix).

For information on another RCA Dual-Input Precision Level Detector, see the data bulletin for the RCA-CA3099E, File No. 620.

ELECTRICAL CHARACTERISTICS at T_A = 25°C Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	Fig. No.	LIMITS			UNITS
			Min.	Typ.	Max.	
Input Offset Voltage:						
"Low" Ref., $V_{IO(LR)}$	V_{LR} = Gnd, V_{HR} = 3 V I_{BIAS} = 100 μA	5	−15	−3	6	mV
"High" Ref., $V_{IO(HR)}$	V_{HR} = Gnd, V_{LR} = −3 V I_{BIAS} = 100 μA	6	−10	±10	10	
Temp. Coeff:						
"Low" Ref.	−55 °C to + 125 °C	7	–	4.5	–	μV/°C
"High" Ref.	−55 °C to + 125 °C	8	–	±8.2	–	
Min. Hysteresis Voltage $V_{IO(HR-LR)}$:	V_{REG} = 6 V, V^+ = 12 V I_{BIAS} = 100 μA	9	–	3	20	mV
Temp. Coeff.	−55°C to + 125 °C	10	–	6.7	–	μV/°C
Output Saturation Voltage, $V_{CE(SAT)}$	V_I = 4 V, V_{REG} = 6 V, V^+ = 12 V, I_{BIAS} = 100 μA	11,12	–	0.72	1.2	V
Total Supply Current, I_{TOTAL}:						
"ON"	V_I = 4 V, V_{REG} = 6 V; V^+ = 12 V, I_{BIAS} = 100 μA	13,14	500	710	800	μA
"OFF"	V_I = 8 V, V_{REG} = 6 V V^+ = 12 V, I_{BIAS} = 100 μA		400	560	750	μA
Input Bias Current, I_{IB}:						
$I_{B(p-n-p)}$	V_I = 4 V, V_{REG} = 6 V V^+ = 12 V, I_{BIAS} = 100 μA	15	–	42	100	nA
$I_{B(n-p-n)}$	V_I = 8 V, V_{REG} = 6 V V^+ = 12 V, I_{BIAS} = 100 μA		–	28	100	nA
Output Leakage Current, $I_{CE(OFF)}$	Current from Term. 3 when Q46 is "OFF"	–	–	–	10	μA
Switching Times:						
Delay, t_d	I_C = 100 μA	18	–	600	–	ns
Fall, t_f	I_{BIAS} = 100 μA		–	50	–	ns
Rise, t_r	V^+ = 5 V		–	500	–	ns
Storage, t_s	V_{REG} = 2.5 V		–	4.5	–	μs
Output Current, I_O	V^+ = 12 V, I_{BIAS} = 50 μA	–	100	–	–	mA

Maximum Ratings, *Absolute-Maximum Values at T_A = 25°C:*

Supply Voltage Between Terminals 6 and 4,	16	V
Output Voltage Between Terminals 7 and 4, and 3 and 4	16	V
Differential Input Voltage Between Terminals 8 and 1, and Terminals 7 and 8	10	V
Operating Voltage Range:		
Term. 8	V^- to V^+	
Term. 7	(V^- plus 2.0 V) to V^+	
Term. 1	(V^-) to (V^+ minus 2.0 V)	
Load Current (Term. 3)	150	mA
Input Current to Voltage Regulator (Term. 5)	25	mA
Programmable Bias Current (Term. 2)	1	mA
Output Current Control (Term. 5)	15	mA
Power Dissipation:		
Up to T_A = 55°C	630	mW
Above T_A = 55°C Derate linearly at	6.67	mW/°C
Ambient Temperature Range (All Packages):		
Operating	−55 to +125	°C
Storage	−65 to +150	°C
Lead Temperature (During Soldering):		
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	265	°C

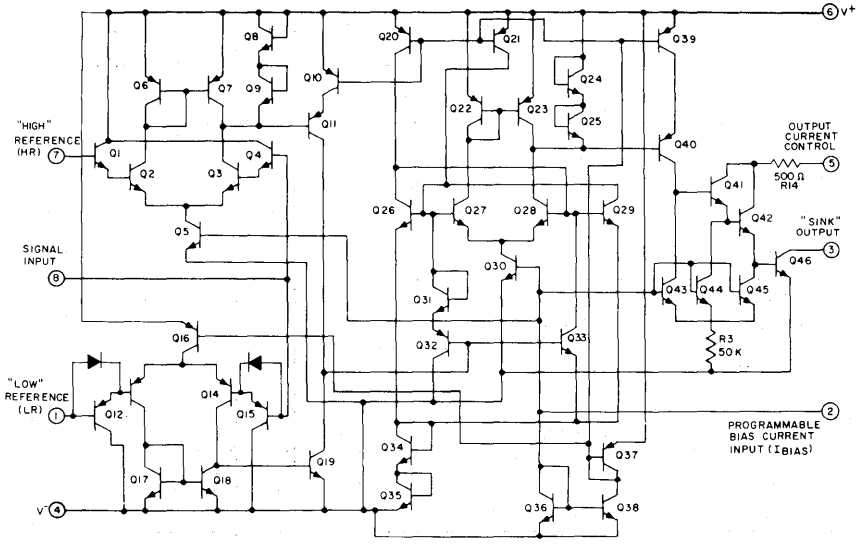


Fig. 2 - Schematic diagram of CA3098.

General Description of Circuit Operation (Refer to Figs. 2, 3, 4)

When the signal-input voltage of the CA3098 is equal to or less than the "low" reference voltage (LR), current flows from an external power supply through a load connected to terminal 3 ("sink" output). This condition is maintained until the signal-input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop (memory) such that the output stage interrupts current flow in the external load. This condition, in turn, is maintained until such time as the signal again becomes equal to or less than the "low" reference voltage (VR).

The CA3098 comparator is unique in that it contains circuit provisions to permit programmability. This feature provides flexibility to the designer to optimize quiescent power consumption, input-circuit characteristics, hysteresis, and additionally permits independent control of the comparator, namely, pulsing, strobing, keying, squelching, etc. Programmability is accomplished by means of the bias current (I_{bias}) supplied to terminal 2.

An auxiliary means of controlling the magnitude of load-current flow at terminal 3 is provided by "sinking" current into terminal 5. Figs 3 and 4 highlight the operation of the CA3098 when connected as a simple hysteresis switch (Schmitt trigger).

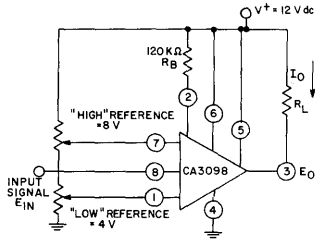


Fig. 3 - Basic hysteresis switch (Schmitt trigger).

Sequence	Input Signal Level	Output Voltage (V) (Term. 3)
1	$4 \geqslant E_{IN} > 0$	0
2	$8 \geqslant E_{IN} > 4$	0
3	$E_{IN} > 8$	12
2	$8 \geqslant E_{IN} > 4$	12
1	$4 \geqslant E_{IN} > 0$	0

Fig. 4 - Resultant output states of the CA3098, shown in Fig. 3 as a function of various input signal levels.

TYPICAL CHARACTERISTIC CURVES

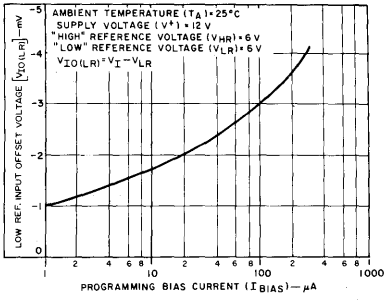


Fig. 5 - Input-offset voltage ("low" reference) vs. programming bias current.

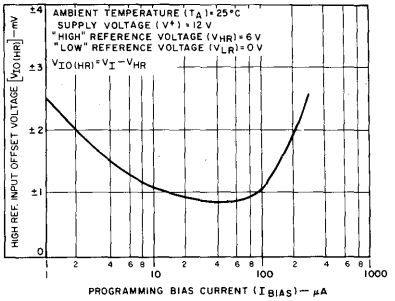


Fig. 6 - Input-offset voltage ("high" reference) vs. programming bias current.

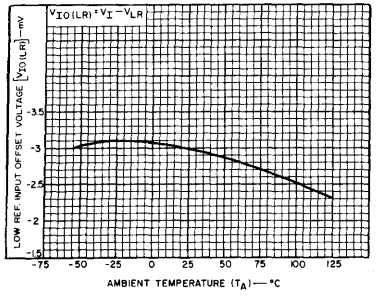


Fig. 7 - Input-offset voltage ("low" reference) vs. ambient temperature.

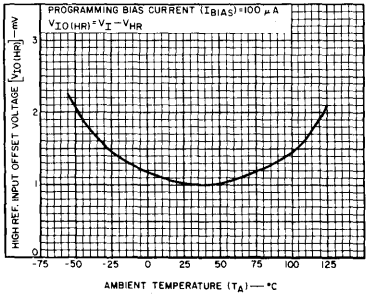


Fig. 8 - Input-offset voltage ("high" reference) vs. ambient temperature.

TYPICAL CHARACTERISTIC CURVES (Cont'd)

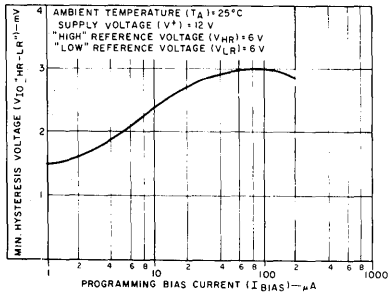


Fig. 9 - Min. hysteresis voltage vs. programming bias current.

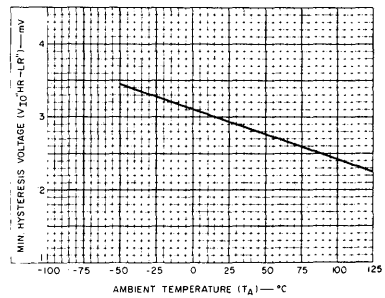


Fig. 10 - Min. hysteresis voltage vs. ambient temperature.

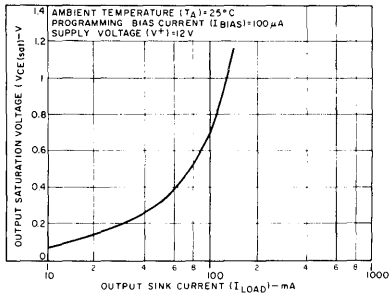


Fig. 11 - Output saturation voltage vs. output sink current.

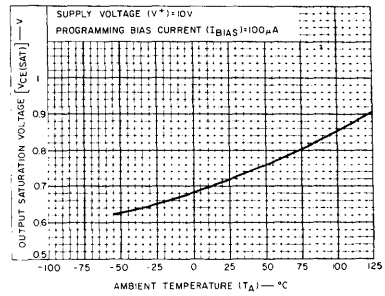


Fig. 12 - Output saturation voltage vs. ambient temperature.

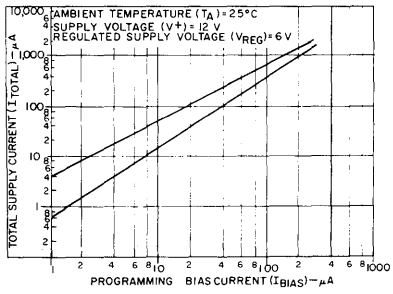


Fig. 13 - Total supply current vs. programming bias current.

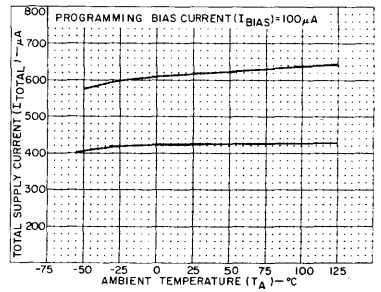


Fig. 14 - Total supply current vs. ambient temperature.

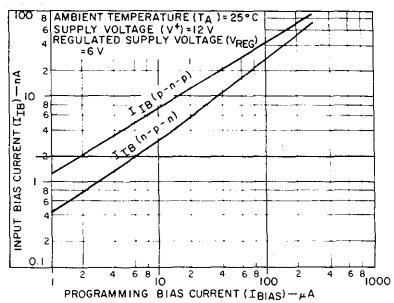


Fig. 15 - Input bias current vs. programming bias current.

TEST CIRCUITS

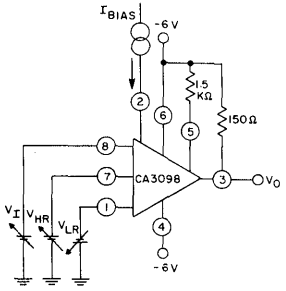


Fig. 16 - Input-offset voltage test circuit.

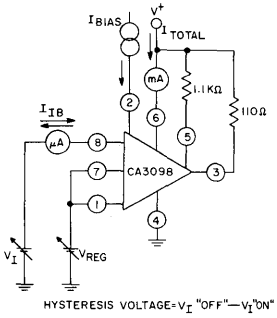


Fig. 17 - Min. hysteresis voltage, total supply current, and input-bias-current test circuit.

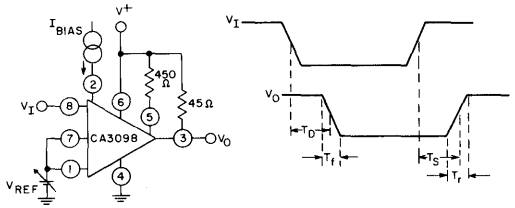


Fig. 18 - Switching time test circuit.

TYPICAL APPLICATIONS

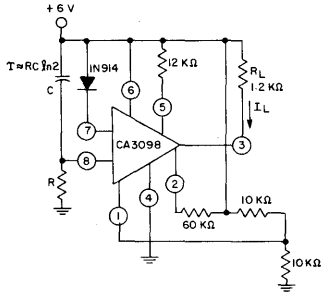


Fig. 19 - Time delay circuit: Terminal 3 "sinks" after τ seconds.

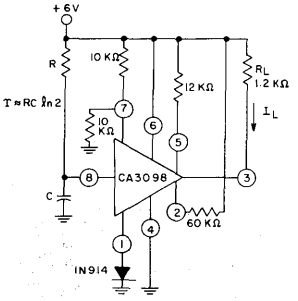


Fig. 20 - Time delay circuit: "sink" current interrupted after τ seconds.

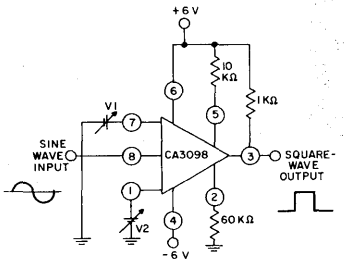
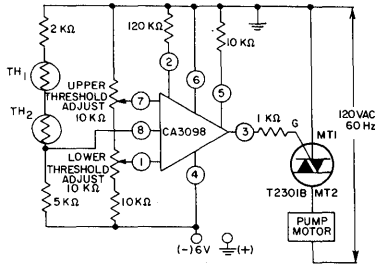


Fig. 21 - Sine-wave to square-wave converter with duty-cycle adjustment (V_1 and V_2).

TYPICAL APPLICATIONS (Cont'd)



Notes (a) Motor pump is "ON" when water level rises above thermistor TH_2.
(b) Motor pump remains "ON" until water level falls below thermistor TH_1.
(c) Thermistors, operate in self-heating mode.

Fig. 22(a) - Water-level control.

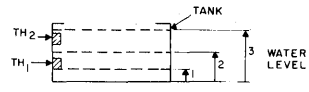


Fig. 22(b) - Water level diagram for circuit of Fig. 22(a).

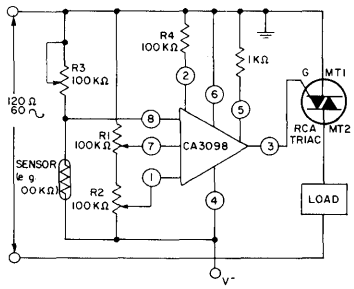


Fig. 23 - OFF/ON control of triac with programmable hysteresis.

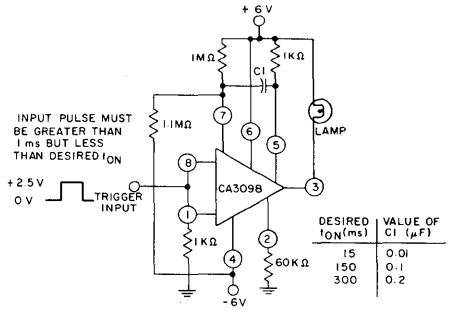
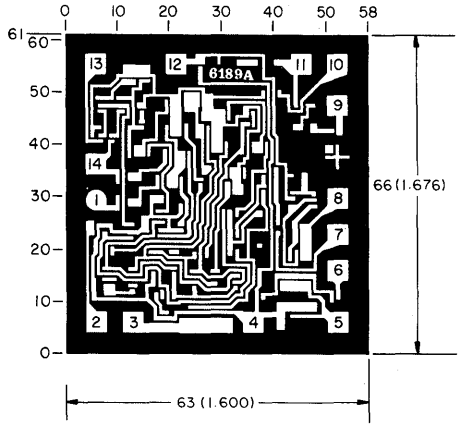


Fig. 24 - One-shot multivibrator.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions and pad layout for the CA3098H.

May 1990

BiMOS Dual Voltage Comparators

With MOSFET Input, Bipolar Output

Features:

- *MOSFET input stage:*
  - *(a) Very high input impedance (Z_{IN}) - 1.7 TV typ.*
  - *(b) Very low input current - 3.5 pA typ. at ±5 V supply voltage*
  - *(c) Wide common mode input voltage range (V_{ICR}) - can be swung 1.5 V (typ.) below negative supply- voltage rail*
  - *(d) Virtually eliminates errors due to flow of input currents*
- *Output voltage compatible with TTL, DTL, ECL, MOS, and CMOS logic systems in most applications*

Applications:

- *High source impedance voltage comparators*
- *Long time delay circuits*
- *Square wave generators*
- *A/D converters*
- *Window comparators*

The CA3290A and CA3290 types consist of a dual voltage comparator on a single monolithic chip. The common mode input voltage range includes ground when operated from a single supply. The low supply current drain makes these comparators suitable for battery operation; their extremely low input currents allow their use in applications that employ sensors with extremely high source impedances. Package options are shown in the table below.

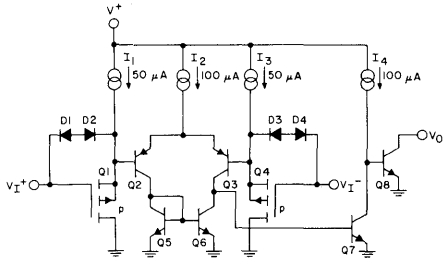


Fig. 1 - Basic CA3290 comparator.

SELECTION CHART

SELECTION	CHARACTERISTIC				PACKAGE AND SUFFIX			
					TO-5		PLASTIC	
	MAX. V_{IO} (mV)	MAX. I_I (pA)	MIN. A_{OL}	V+ (V)	STD.	DIL-CAN	8-LEAD	14-LEAD
CA3290A	10	40	25K	36	T	S	E	E1
CA3290	20	50	25K	36	T	S	E	E1

The CA3290 is also available in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE:
- Single Supply:
  - CA3290A, CA3290 . . . . . +36 V
- Dual Supply:
  - CA3290A, CA3290 . . . . . ±18 V

DIFFERENTIAL INPUT VOLTAGE . . . . . ±36 V or ± [(V^+–V^-)+5 V] (whichever is less)

COMMON-MODE INPUT VOLTAGE . . . . . V^++5 V to V^-–5 V

DEVICE DISSIPATION:
- Up to 55°C . . . . . 630 mW
- Above 55°C . . . . . Derate linearly at 6.67 mW/°C

OUTPUT-TO-V^- SHORT CIRCUIT DURATION* . . . . . CONTINUOUS

TEMPERATURE RANGE, ALL TYPES:
- Operating . . . . . –55 to +125°C
- Storage . . . . . –65 to +150°C

INPUT TERMINAL CURRENT . . . . . 1 mA

LEAD TEMPERATURE (DURING SOLDERING):
- AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX. . . . . 265°C

*Short circuits from the output to V^+ can cause excessive heating and eventual destruction of the device.

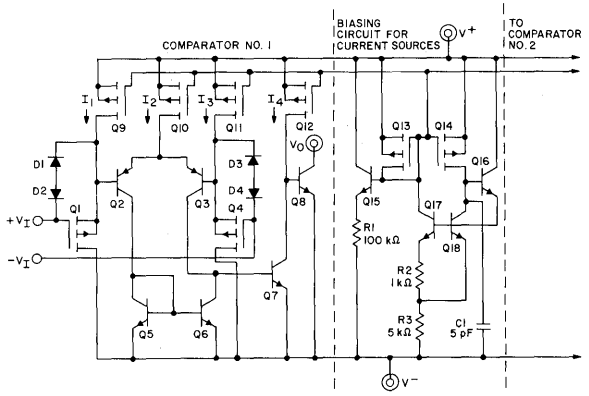


Fig. 2 – Schematic diagram of CA3290 (only one is shown).

CIRCUIT DESCRIPTION

The Basic Comparator

Fig. 1 shows the basic circuit diagram for one of the two comparators in the CA3290. It is generically similar to the industry-type "139" comparators, with PMOS transistors replacing p-n-p transistors as input stage elements. Transistors Q1 through Q4 comprise the differential input stage, with Q5 and Q6 serving as a mirror-connected active load and differential-to-single-ended converter. The differential input at Q1 and Q4 is amplified so as to toggle Q6 in accordance with the input-signal polarity. For example, if $+V_{IN}$ is greater than $-V_{IN}$, Q1, Q2, and current mirror transistors Q5 and Q6 will be turned off; transistors Q3, Q4, and Q7 will be turned on, causing Q8 to be turned off. The output is pulled positive when a load resistor is connected between the output and V^+.

In essence, Q1 and Q4 function as source-followers to drive Q2 and Q3, respectively, with zener diodes D1 through D4 providing gate-oxide protection against input voltage transients (e.g., static electricity). The current flow in Q1 and Q2 is established at approximately 50 microamperes by constant-current sources I_1 and I_3, respectively. Since Q1 and Q4 are operated with a constant current load, their gate-to-source voltage drops will be effectively constant as long as the input voltages are within the common-mode range.

As a result, the input offset voltage ($V_{GS(Q1)} + V_{BE(Q2)} - V_{BE(Q3)} - V_{GS(Q4)}$) will not be degraded when a large differential dc voltage is applied to the device for extended periods of time at high temperatures.

Additional voltage gain following the first stage is provided by transistors Q7 and Q8. The collector of Q8 is open, offering the user a wide variety of options in applications. An additional discrete transistor can be added if it becomes necessary to boost the output sink-current capability.

The detailed schematic diagram for one comparator and the common current-source biasing is shown in Fig. 2. PMOS transistors Q9 through Q12 are the current-source elements identified in Fig. 1 as I_1 through I_4, respectively. Their gate-source potentials (V_{GS}) are supplied by a common bus from the biasing circuit shown in the right-hand portion of the Fig. 2. The currents supplied by Q10 and Q12 are twice those supplied by Q9 and Q11. The transistor geometries are appropriately scaled to provide the requisite currents with common V_{GS} applied to Q9 through Q12.

ELECTRICAL CHARACTERISTICS at T_A = –55 to +125°C

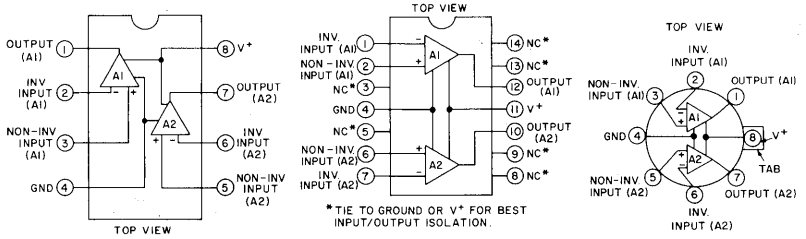
CHARACTERISTIC	TEST CONDITIONS		VALUES				UNITS
			CA3290A		CA3290		
		V^+	Typ.	Max.	Typ.	Max.	
Input Offset Voltage, V_{IO}	V_{CM}=1.4 V, V_O=1.4 V	5 V	4.5	–	8.5	–	mV
	V_{CM}=0 V, V_O=0 V	±15 V	8.5	–	8.5		
Temp. Coefficient of Input Offset Voltage, $\Delta V_{IO}/\Delta T$			8	–	8	–	μV/°C
Input Offset Current, I_{IO}	V_{CM}=1.4 V	5 V	2	28	2	32	nA
	V_{CM}=0 V	±15 V	7	28	7	32	
Input Current, I_I▲	V_{CM}=1.4 V	5 V	2.8	45	2.8	55	nA
	V_{CM}=0 V	±15 V	13	45	13	55	
Supply Current, I^+*	$R_L = \infty$	5 V	0.85	1	0.85	1.6	mA
		30 V	1.62	3	1.62	3.5	
Voltage Gain, A_{OL}	R_L=15 kΩ	±15 V	150	–	150	–	V/mV
			103	–	103	–	dB
Saturation Voltage I_{SINK} = 4 mA	V^+=5 V, $+V_I$=0 V, $-V_I$=1 V	+125°C	0.22	0.7	0.22	0.7	V
		–55°C	0.1	–	0.1	–	
Output Leakage Current, I_{OL}		15 V	65	–	65	–	nA
		36 V	130	1k	130	1k	

▲At T_A = +125°C
*At T_A = –55°C

ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$

CHARACTERISTIC	TEST COND. V^+	LIMITS CA3290A Min.	CA3290A Typ.	CA3290A Max.	CA3290 Min.	CA3290 Typ.	CA3290 Max.	UNITS
Input Offset Voltage, V_{IO} V_{CM}=1.4 V, V_O=1.4 V	5 V	–	4	10	–	7.5	20	mV
V_{CM}=0 V, V_O=0 V	±15 V	–	4	10	–	7.5	20	mV
Input Current, I_I V_{CM}=1.4 V	5 V	–	3.5	40	–	3.5	50	pA
V_{CM}=0 V	±15 V	–	12	40	–	12	50	pA
Input Offset Current, I_{IO} V_{CM}=1.4 V	5 V	–	2	25	–	2	30	pA
V_{CM}=0 V	±15 V	–	7	25	–	7	30	pA
Common-Mode Input-Voltage Range, V_{ICR} V_O=1.4 V	5 V	V^+–3.5 to V^-	V^+–3.1 to V^-–1.5	–	V^+–3.5 to V^-	V^+–3.1 to V^-–1.5	–	V
V_O=0 V	±15 V	V^+–3.8 to V^-	V^+–3.4 to V^-–1.6	–	V^+–3.8 to V^-	V^+–3.4 to V^-–1.6	–	V
Supply Current, I^+ $R_L = \infty$	30 V	–	1.35	3	–	1.35	3	mA
	5 V	–	0.8	1.4	–	0.8	1.4	mA
Voltage Gain, A_{OL} R_L=15 kΩ	±15 V	25	800	–	25	800	–	V/mV
		88	118	–	88	118	–	dB
Output Sink Current V_O=1.4 V	5 V	6	30	–	6	30	–	mA
Saturation Voltage $+V_I$=0 V, $-V_I$=1 V, I_{SINK} = 4 mA	5 V	–	0.12	0.4	–	0.12	0.4	V
Output Leakage Current, I_{OL}	15 V	–	100	–	–	100	–	pA
	36 V	–	500	–	–	500	–	pA
Response Time R_L=5.1 kΩ Rising Edge	15 V	–	1.2	–	–	1.2	–	μs
Falling Edge		–	200	–	–	200	–	ns
Common-Mode Rejection Ratio, CMRR	±15 V	–	44	562	–	44	562	μV/V
	5 V	–	100	562	–	100	562	μV/V
Power-Supply Rejection Ratio, PSRR	±15 V	–	15	316	–	15	316	μV/V
Large-Signal Response Time R_L=5.1 kΩ	15 V	–	500	–	–	500	–	ns
	5 V	–	400	–	–	400	–	ns

TERMINAL ASSIGNMENTS



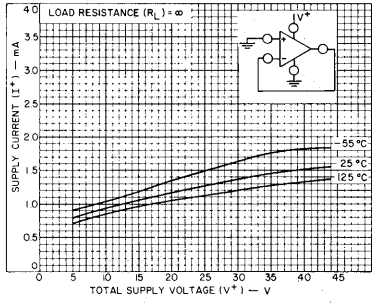


Fig. 3 — Supply current as a function of supply voltage (both amplifiers).

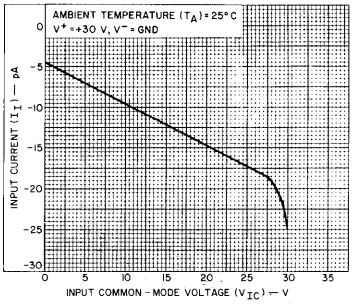


Fig. 4 — Input current as a function of input common-mode voltage.

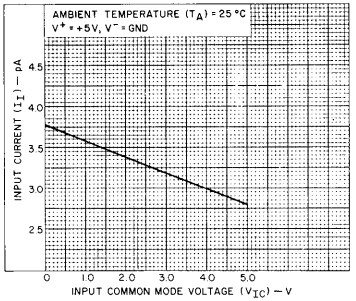


Fig. 5 — Input current as a function of input common-mode voltage.

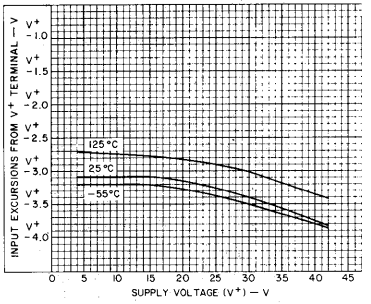


Fig. 6 — Positive common-mode input voltage range as a function of supply voltage.

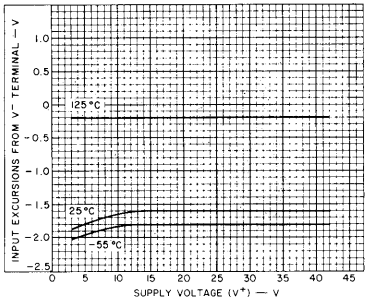


Fig. 7 — Negative common-mode input voltage range as a function of supply voltage.

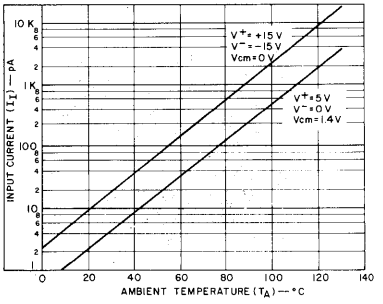


Fig. 8 — Input current as a function of ambient temperature.

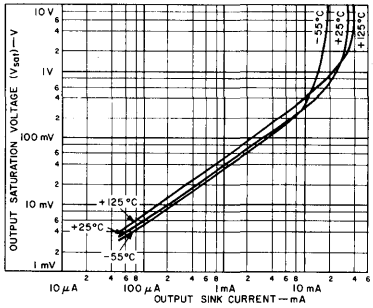
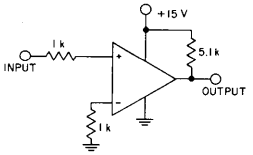
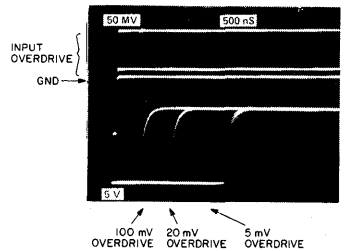


Fig. 9 — Output saturation voltage as a function of output sink current.





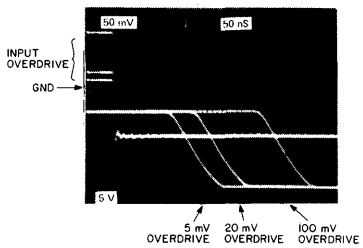
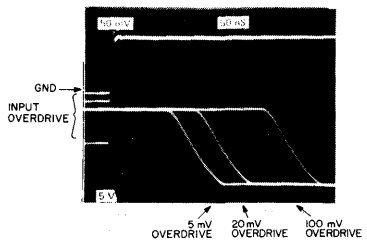
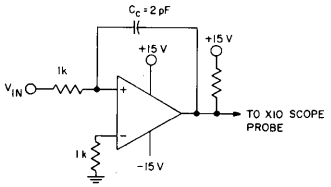
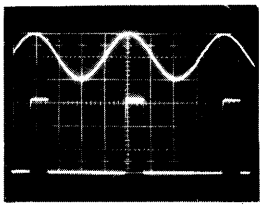


Fig. 11 — Non-inverting comparator response-time test circuit and waveforms.

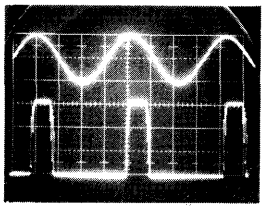






WITH C_C

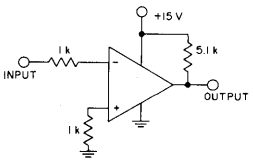
TOP TRACE ≈ 4.5 mV/DIV = V_{IN}
BOTTOM TRACE = 10V/DIV = V_{OUT}
H = 5 μs/DIV



WITHOUT C_C

TOP TRACE ≈ 4.5 mV/DIV
BOTTOM TRACE = 10V/DIV
H = 5 μs/DIV

Fig. 10 — Parasitic-oscillations test circuit and associated waveforms.



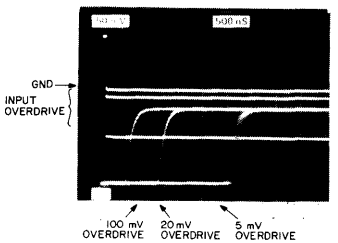


Fig. 12 — Inverting comparator response-time test circuit and waveforms.

OPERATING CONSIDERATIONS

Input Circuit

The use of MOS transistors in the input stage of the CA3290 series circuits provides the user with the following features for comparator applications:

1. Ultra-high input impedance ($\cong 1.7\ T\Omega$);
2. The availability of common-mode rejection for input signals at potentials below that of the negative power-supply rail;
3. Retention of the in-phase relationship of the input and output signals for input signals below the negative rail.

Although the CA3290 employs rugged bipolar (zener) diodes for protection of the input circuit, the input-terminal currents should not exceed 1 mA. Appropriate series-connected limiting resistors should be used in circuits where greater current flows might exist, allowing the signal input voltage to be greater than the supply voltage without damaging the circuit.

Output Circuit

The output of the CA3290 is the open collector of an n-p-n transistor, a feature providing flexibility in a broad range of comparator applications. An output ORing function can be implemented by parallel-connection of the open collectors. An output pull-up resistor can be connected to a power supply having a voltage range within the rating of the particular CA3290 in use; the magnitude of this voltage may be set at a value which is independent of that applied to the V^+ terminal of the CA3290.

Parasitic Oscillations

The ideal comparator has, among other features, ultra-high input impedance, high gain, and wide bandwidth. These desirable characteristics may, however, produce parasitic oscillations unless certain precautions are observed to minimize the stray capacitive coupling between the input and output terminals. Parasitic oscillations manifest themselves during the output voltage transition intervals as the comparator switches states. For high source impedances, stray capacitance can induce parasitic oscillations. The addition of a small amount (1 to 10 mV) of positive feedback (hysteresis) produces a faster transition, thereby reducing the likelihood of parasitic oscillations. Furthermore, if the input signal is a pulse waveform, with relatively rapid rise and fall times, parasitic tendencies are reduced.

When dual comparators, like the CA3290, are packaged in an 8-lead configuration, the output terminal of each comparator is adjacent to an input terminal. The lead-to-lead capacitance is approximately 1 pF, which may be sufficient to cause undesirable feedback effects in certain applications. Circuit factors such as impedance levels, supply voltage, toggling rate, etc., may increase the possibility of parasitic oscillations. To minimize this potential oscillatory condition, it is recommended that for source impedances greater than 1 kΩ a capacitor ($\geqslant$ 1-2 pF) be connected between the appropriate input terminal and the output terminal. (See Fig. 10.)

The CA3290A and CA3290 are also supplied in a 14-lead dual-in-line plastic package. To minimize the possibility of parasitic oscillations the input and output terminals are positioned on opposite sides of the package. In addition, there are two leads between the output terminal of each comparator and its corresponding inverting input terminal, reducing the input/output coupling significantly. These leads (8, 9, 13, 14) should be tied to either the V^+ or V^- supply rail. If either comparator is unused, its input terminals should also be tied to either the V^+ or V^- supply rail.

TYPICAL APPLICATIONS

Light-Controlled One-Shot Timer

In Fig. 13 one comparator (A1) of the CA3290 is used to sense a change in photo diode current. The other comparator (A2) is configured as a one-shot timer and is triggered by the output of A1. The output of the circuit will switch to a low state for approximately 60 seconds after the light source to the photo diode has been interrupted. The circuit operates at normal room lighting levels. The sensitivity of the circuit may be adjusted by changing the values of R1 and R2. The ratio of R1 to R2 should be constant to insure constant reverse voltage bias on the photo diode.

Low-Frequency Multivibrator

In this application, one-half of the CA3290 is used as a conventional multivibrator circuit. Because of the extremely high input impedance of this device, large values of timing resistor (R1) may be used for long time delays with relatively small leakage timing capacitors. The second half of the CA3290 is used as an output buffer to insure that the multivibrator frequency will not be affected by output loading.

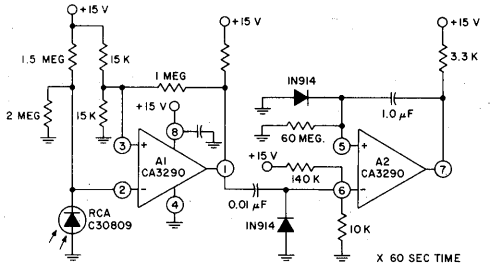


Fig. 13 – Light-controlled one-shot timer.

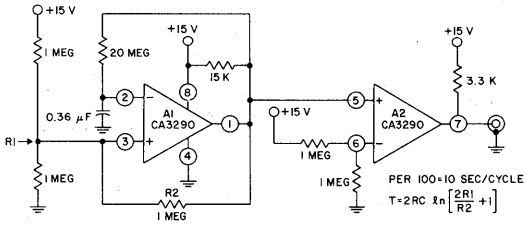


Fig. 14 – Low-frequency multivibrator.

Window Comparator

Both halves of the CA3290 can be used in a high input-impedance window comparator as shown in Fig. 15. The LED will be turned "on" whenever the input signal is above the lower limit (V_L) but below the upper limit (V_U), as determined by the R1/R2/R3 resistor divider.

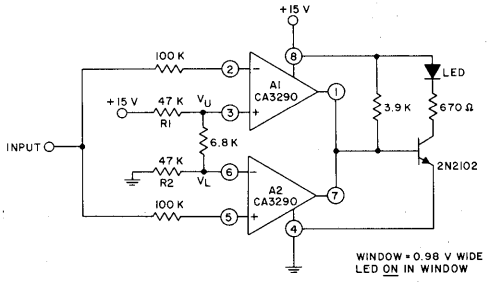


Fig. 15 – Window comparator.

LED Bar Graph Driver

The circuit in Fig. 16 demonstrates the use of the CA3290 in a bar graph display. The non-inverting inputs of both comparators are tied to the voltage divider reference and the input signal is applied to both of the inverting inputs. The LED for a particular comparator will be turned "on" when the input voltage reaches the voltage on the resistor divider reference. The CA3290 is ideal for this application where input-signal loading is critical even though many comparator inputs are driven in parallel.

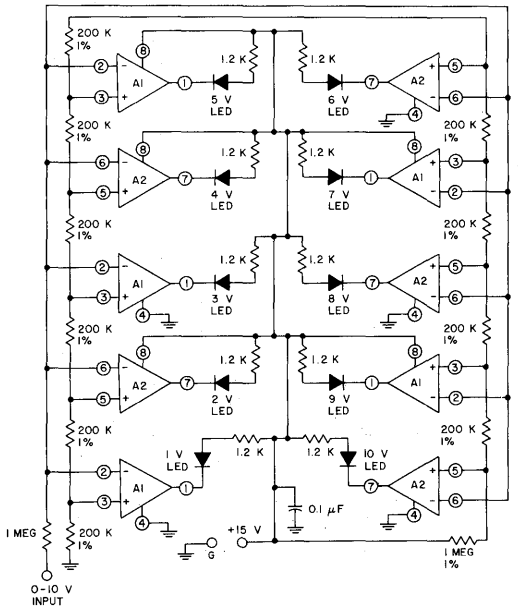
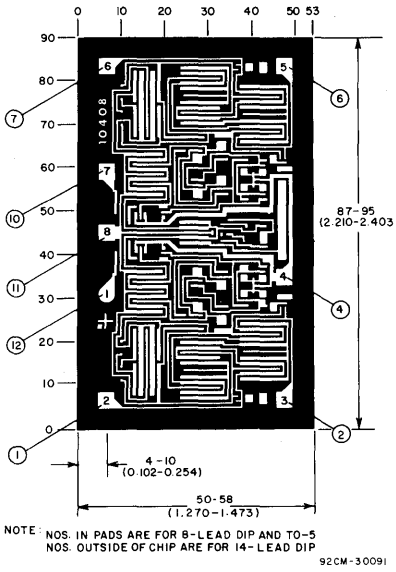


Fig. 16 – LED bar-graph driver.



Dimensions and pad layout for the CA3290H.

The photographs and dimensions of each chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

HARRIS HA-4900/02/05

May 1990

Precision Quad Comparator

Features

- Fast Response Time 130ns
- Low Offset Voltage 2.0mV
- Low Offset Current 10nA
- Single or Dual-Voltage Supply Operation
- Selectable Output Logic Levels
- Active Pull-Up/Pull-Down Output Circuit-No External Resistors Required

Applications

- Threshold Detector
- Zero-Crossing Detector
- Window Detector
- Analog Interfaces for Microprocessors
- High Stability Oscillators
- Logic System Interfaces

Description

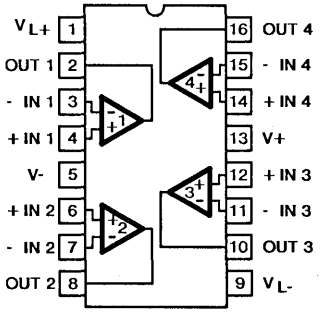
The HA-4900 series are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5 volt supply (digital systems) or from dual supplies (analog networks) up to ±15volts. The HA-4900 series contains a unique current driven output stage which can be connected to logic system supplies (V_{Logic} + and V_{Logic} -) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900 series input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

These comparators' combination of features makes them ideal components for signal detection and processing in data acquisition systems, test equipment and microprocessor/analog signal interface networks.

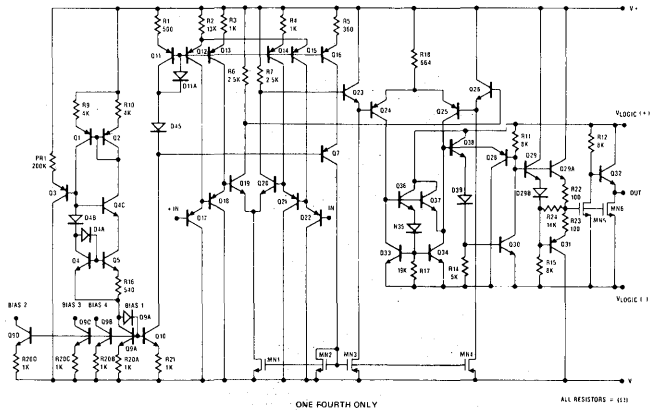
All devices are available in 16 pin dual-in-line ceramic packages. The HA-4900/4902-2 operates from -55°C to +125°C and the HA-4905-5 operates over a 0°C to +75°C temperature range. For military grade product, refer to the HA-4902/883 data sheet.

Pinouts

HA1-4900/02/05 (CERAMIC DIP)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 33V
Differential Input Voltage ..... ±15V
Voltage Between V_{Logic} (+) and V_{Logic} (-) 18V
Peak Output Current ..... ±50mA
Internal Power Dissipation (Note 7, 8) 2.0W

Operating Temperature Ranges

HA-4900-2 ..... $-55^oC \leq T_A \leq +125^oC$
HA-4902-2 ..... $-55^oC \leq T_A \leq +125^oC$
HA-4905-5 ..... $0^oC \leq T_A \leq +75^oC$
Storage Temperature Range: ..... $-65^oC \leq T_A \leq +150^oC$

Electrical Specifications

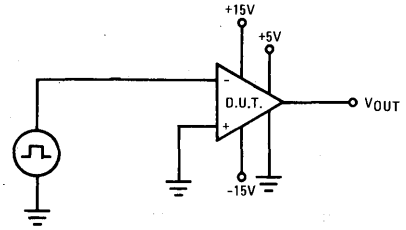
V+ = +15V, V- = -15V, V_{Logic} (+) = 5V, V_{Logic} (-) = GND.

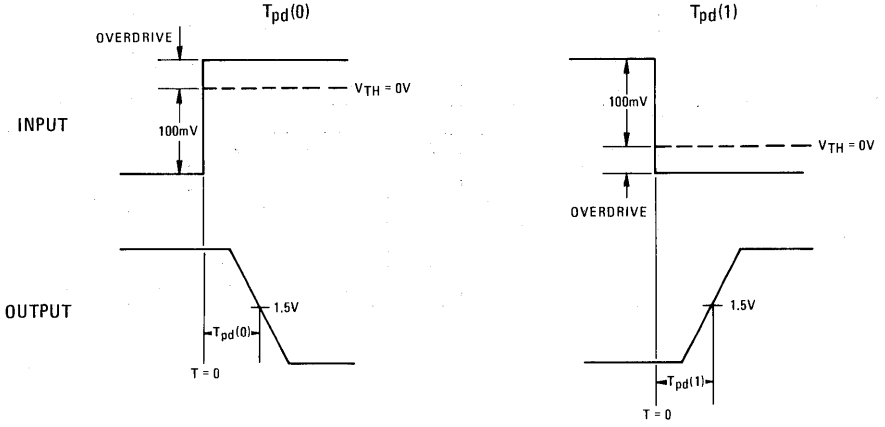
PARAMETER	TEMP	HA-4900-2 -55°C to +125°C			HA-4902-2 -55°C to +125°C			HA-4905-5 0°C to +125°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage (Note 2)	+25°C		2	3		2	5		4	7.5	mV
	Full			4			8			10	mV
Offset Current	+25°C		10	25		10	35		25	50	nA
	Full			35			45			70	nA
Bias Current (Note 3)	+25°C		50	75		50	150		100	150	nA
	Full			150			200			300	nA
Input Sensitivity (Note 4)	+25°C			V_{IO} +.3			V_{IO} +.5			V_{IO} +.5	mV
	Full			V_{IO} +.4			V_{IO} +.6			V_{IO} +.7	mV
Common Mode Range	Full	V-		(V+)-2.4	V-		(V+)-2.6	V-		(V+)-2.4	V
Differential Input Resistance	+25°C		250			250			250		MΩ
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	+25°C		400K			400K			400K		V/V
Response Time ($T_{pd}0$) (Note 5)	+25°C		130	200		130	200		130	200	ns
Response Time ($T_{pd}1$) (Note 5)	+25°C		180	215		180	215		180	215	ns
OUTPUT CHARACTERISTICS											
Output Voltage Level											
Logic "Low State" (V_{OL}) (Note 6)	Full		0.2	0.4		0.2	0.4		0.2	0.4	V
Logic "High State" (V_{OH}) (Note 6)	Full	3.5	4.2		3.5	4.2		3.5	4.2		V
Output Current											
I_{Sink}	Full	3.0			3.0			3.0			mA
I_{Source}	Full	3.0			3.0			3.0			mA
POWER SUPPLY CHARACTERISTICS											
Supply Current, I_{ps} (+)	+25°C		6.5	20		6.5	20		7	20	mA
Supply Current, I_{ps} (-)	+25°C		4	8		4	8		5	8	mA
Supply Current, I_{ps} (Logic)	+25°C		3.5	4		3.5	4		3.5	4	mA
Supply Voltage Range											
V_{Logic} (+) (Note 7)	Full	0		+15.0	0		+15.0	0		+15.0	V
V_{Logic} (-) (Note 7)	Full	-15.0		0	-15.0		0	-15.0		0	V

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Minimum differential input voltage required to ensure a defined output state.
3. Input bias currents are essentially constant with differential input voltages up to ± 9 volts. With differential input voltages from ±9 to ±15 volts, bias current on the more negative input can rise to approximately 500µA. This will also cause higher supply currents.
4. $R_S \leq 200\Omega$ $V_{IN} \leq$ Common Mode Range. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state. This parameter includes the effects of offset voltage, offset current, common mode rejection, and voltage gain.
5. For $T_{pd}(1)$; 100mV input step, -10mV overdrive. For $T_{pd}(0)$; -100mV input step, 10mV overdrive. Frequency $\approx$100Hz; Duty Cycle $\approx$ 50%; Inverting input driven. See Test Circuit below. All unused inverting inputs tie to +5V.
6. For V_{OH} and V_{OL}: $I_{Sink} = I_{Source}$ = 3.0mA. For other values of V_{Logic}: V_{OH} (min.) = V_{Logic} + -1.5V.
7. Total Power Dissipation (T.P.D.) is the sum of individual dissipation contributions of V+, V- and V_{Logic} shown in curves of Power Dissipation vs. Supply Voltages (see Performance Curves). The calculated T.P.D. is then located on the graph of Maximum Allowable Package Dissipation vs. Ambient Temperature to determine ambient temperature operating limits imposed by the calculated T.P.D. (See Performance Curves). For instance, the combination of +15V, -15V, +5V, 0V (V+, V-, V_{Logic}+, V_{Logic}-) gives a T.P.D. of 350mW, the combination +15V, -15V, 0V gives a T.P.D. of 450mW.
8. Derate By 5.8mW/°C above T_A = +75°C. θ_{ja} = 75°C/W, θ_{jc} = 20°C/W.

Test Circuits

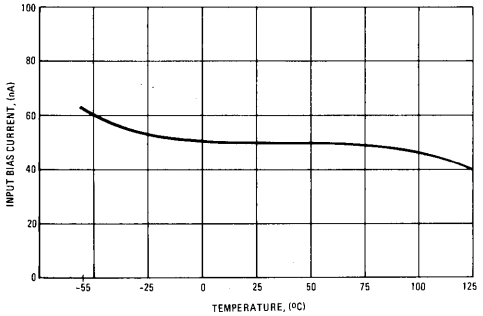




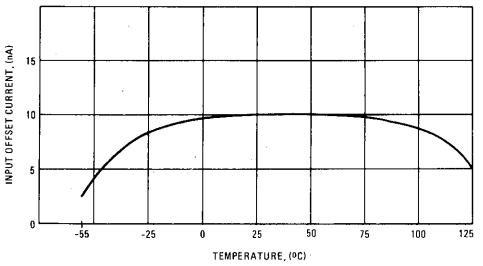
For input and output voltage waveforms for various input overdrives see Performance Curves.

Typical Performance Curves V+ = 15V, V_{Logic} (+) = 5V, V_{Logic} (-) = 0V, T_A = +25°C, Unless Otherwise Specified.

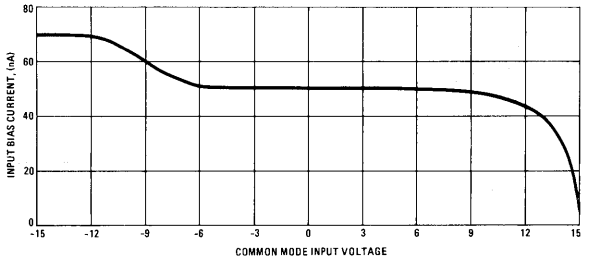
INPUT BIAS CURRENT vs. TEMPERATURE



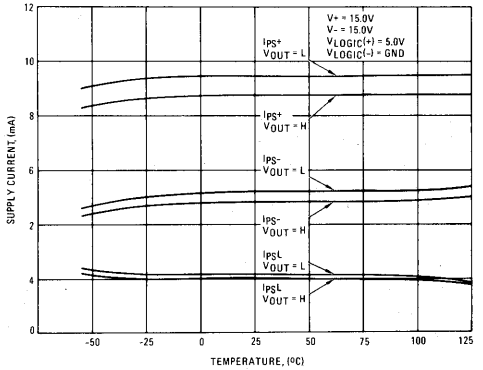
INPUT OFFSET CURRENT vs. TEMPERATURE



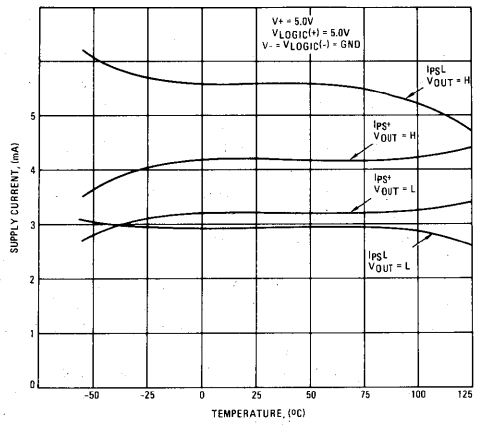
INPUT BIAS CURRENT vs. COMMON MODE INPUT VOLTAGE
($V_{DIFF.}$ = 0V)



SUPPLY CURRENT vs. TEMPERATURE
FOR ±15V SUPPLIES AND ± 5V LOGIC SUPPLY

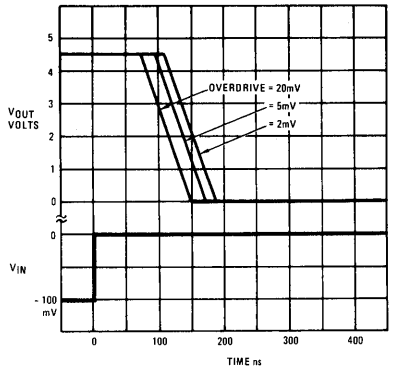


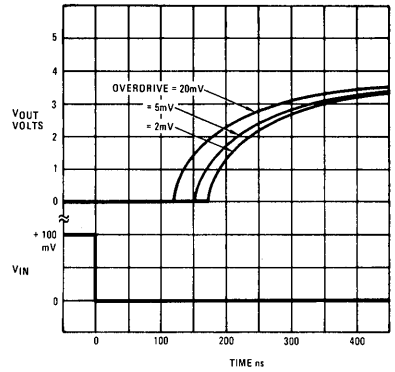
SUPPLY CURRENT vs. TEMPERATURE
FOR SINGLE +5V OPERATION



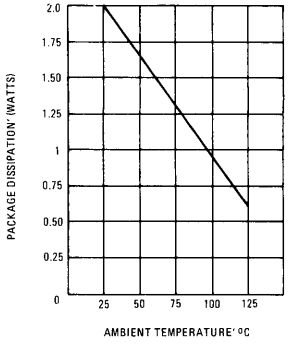
Typical Performance Curves (Continued) $V+ = 15V$, $V_{Logic}(+) = 5V$, $V_{Logic}(-) = 0V$, $T_A = +25^oC$, Unless Otherwise Specified.

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

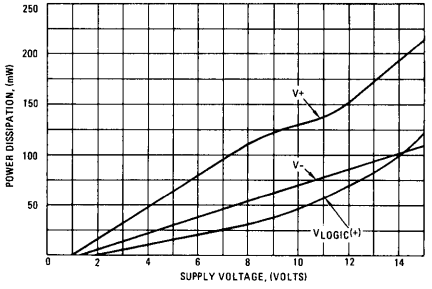




MAXIMUM PACKAGE DISSIPATION vs. $T_{AMBIENT}$



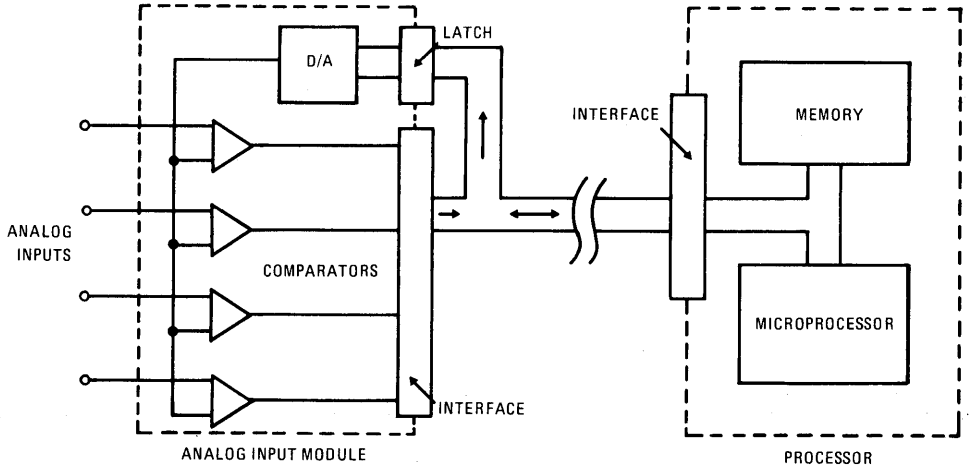
MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE
(NO LOAD CONDITION)



Applying the HA-4900 Series Comparators

1. SUPPLY CONNECTIONS: This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to $V_{Logic}+$ and $V_{Logic}-$. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings (15V P-P, max.) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to 15V), V+ and $V_{Logic}+$ may be connected together to the positive supply while V- and $V_{Logic}-$ are grounded. If an input signal could swing negative with respect the V- terminal, a resistor should be connected in series with the input to limit input current to < 5mA since the C-B junction of the input transistor would be forward biased.
2. UNUSED INPUTS: Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter".
3. CROSSTALK: Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{OS}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.
4. POWER SUPPLY DECOUPLING: Decouple all power supply lines with .01µF ceramic capacitors to ground line located near the package to reduce coupling between channels or from external sources.
5. RESPONSE TIME: Fast rise time (< 200ns) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.

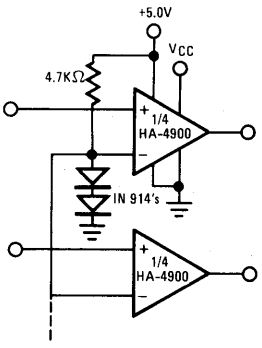
Typical Applications



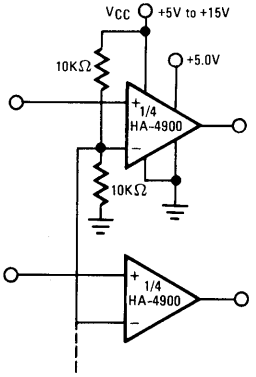
Data Acquisition System

In this circuit the HA-4900 series is used in conjunction with a D to A converter to form a simple, versatile, multi-channel analog input for a data acquisition system. In operation the processor first sends an address to the D to A, then the processor reads the digital word generated by the comparator outputs.

To perform a simple comparision, the processor sets the D to A to a given reference level, then examines one or more comparator outputs to determine if their inputs are above or below the reference. A window comparison consists of two such cycles with 2 reference levels set by the D to A. One way to digitize the inputs would be for the processor to increment the D to A in steps. The D to A address, as each comparator switches, is the digitized level of the input. While stairstepping the D to A is slower than successive approximation, all channels are digitized during one staircase ramp.



TTL TO CMOS



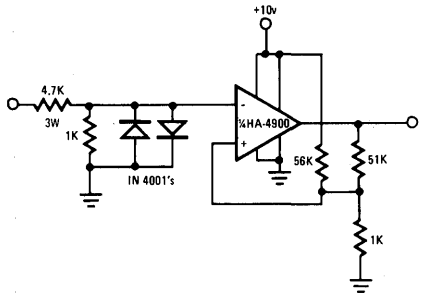
CMOS TO TTL

Logic Level Translators

The HA-4900 series comparators can be used as versatile logic interface devices as shown in the circuits above. Negative logic devices may also be interfaced with appropriate supply connections.

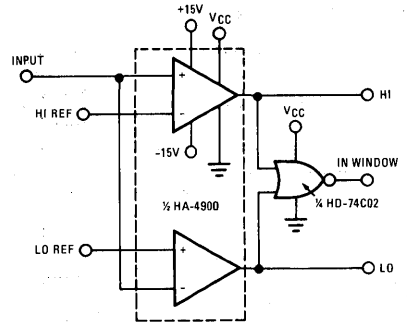
If separate supplies are used for V- and V_{Logic-}, these logic level translators will tolerate several volts of ground line differential noise.

Typical Applications (Continued)



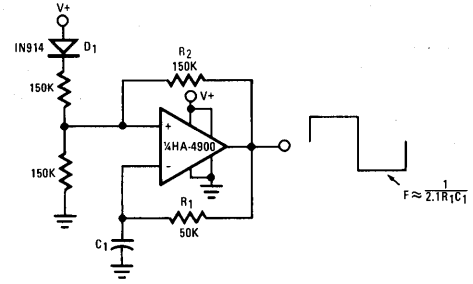
RS-232 To CMOS Line Receiver

This RS-232 type line receiver to drive CMOS logic uses a Schmitt trigger feedback network to give about 1 volt input hysteresis for added noise immunity. A possible problem in an interface which connects two equipments, each plugged into a different AC receptacle, is that the power line voltage may appear at the receiver input when the interface connection is made or broken. The two diodes and a 3 watt input resistor will protect the inputs under these conditions.



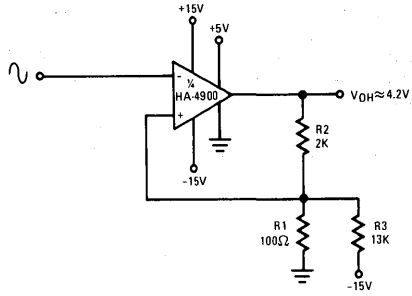
Window Detector

The high switching speed, low offset current and low offset voltage of the HA-4900 series makes this window detector circuit extremely well suited to applications requiring fast, accurate, decision-making. The circuit above is ideal for industrial process system feedback controllers or "out-of-limit" alarm indicators.



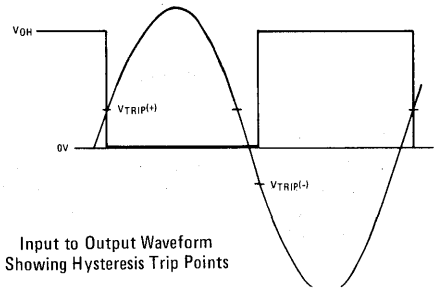
Oscillator/Clock Generator

This self-starting fixed frequency oscillator circuit gives excellent frequency stability. R_1 and C_1 comprise the frequency determining network while R_2 provides the regenerative feedback. Diode D_1 enhances the stability by compensating for the difference between V_{OH} and V_{Supply}. In applications where a precision clock generator up to 100kHz is required, such as in automatic test equipment, C_1 may be replaced by a crystal.



Schmitt Trigger (Zero Crossing Detector With Hysteresis)

This Circuit has a 100mV hysteresis which can be used in applications where very fast transition times are required at the output even though the signal input is very slow. The hysteresis loop also reduces false triggering due to noise on the input. The waveforms below show the trip points developed by the hysteresis loop.



Input to Output Waveform
Showing Hysteresis Trip Points

LINEAR 5

SAMPLE AND HOLD AMPLIFIERS

		PAGE
SELECTION GUIDE		5-2
SAMPLE AND HOLD DATA SHEETS		
HA 2420, 25	Fast Sample and Hold Amplifier	5-3
HA 5320	High Speed Precision Monolithic Amplifier	5-10
HA 5330	Very High Speed Monolithic Amplifier	5-17
HA 5340	High Speed, Low Distortion, Monolithic Amplifier	5-21

Selection Guide

SAMPLE-AND-HOLD AMPLIFIERS

Type	Sample/Hold Type	Temperature Range	Package*	Acquisition Time (to 0.01%) Typ, +25°C	Charge Transfer Typ, +25°C	Aperture Time Typ, +25°C	Gain Bandwidth Product Typ, +25°C
HA1-2420-2 HA1-2425-5 HA3-2425-5 HA4-2420-8 HA4P2425-5	Low Droop Rate	-55°C to +125°C 0°C to +75°C 0°C to +75°C -55°C to +125°C 0°C to +75°C	14-Pin Cerdip 14-Pin Cerdip 14-Pin Epoxy 20-Pin LCC Ceramic 20-Pin PLCC Epoxy	3.2µs (C_H =1,000pF)	10pC	30ns	2.5MHz
HA1-5320-2 HA1-5320-5 HA1-5320-8 HA4-5320-8	High Speed Low Charge Transfer Precision Complete-Includes Hold Capacitor	-55°C to +125°C 0°C to +75°C -55°C to +125°C -55°C to +125°C	14-Pin Cerdip 14-Pin Cerdip 14-Pin Cerdip 20-Pin LCC Ceramic	1µs (C_H = Internal)	0.1pC	25ns	2.0MHz C_H = 100pF
HA1-5330-5 HA1-5330-4 HA1-5330-2	Very High Speed Precision Monolithic Complete-Includes Hold Capacitor	0°C to +75°C -25°C to +85°C -55°C to +125°C	14-Pin Cerdip 14-Pin Cerdip 14-Pin Cerdip	500ns	0.05pC	20ns	4.5MHz
HA1-5340-5 HA1-5340-4 HA1-5340-2	High Speed Low Distortion- Includes Hold Capacitor	0°C to +75°C -25°C to +85°C -55°C to +125°C	14-Pin Cerdip 14-Pin Cerdip 14-Pin Cerdip	0.7µs	0.5pC	15ns	10MHz

* See Packaging Section

HARRIS HA-2420/25

May 1990

Fast Sample and Hold

Features

- Maximum Acquisition Time (10V Step to 0.1%) ... 4μs (10V Step to 0.01%) 6μs
- Low Droop Rate (C_H = 1000pF) ..... 5μV/ms (Typ.)
- Gain Bandwidth Product ..... 2.5MHz (Typ.)
- Low Effective Aperture Delay Time ..... 30ns (Typ.)
- TTL Compatible Control Input
- ±12V to ±15V Operation

Applications

- 12-Bit Data Acquisition
- Digital to Analog Deglitcher
- Auto Zero Systems
- Peak Detector
- Gated Operational Amplifier

Description

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and MOSFET input unity gain amplifier.

With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

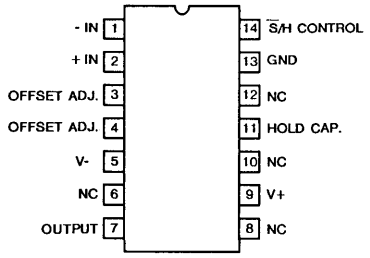
Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc. For more information, please see Application Note 517.

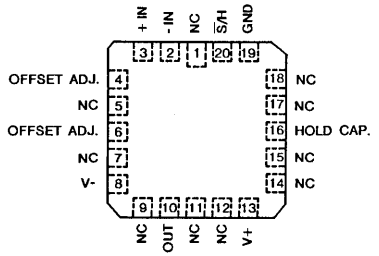
The HA-2420/25 is offered in a 14 pin Ceramic or Plastic DIP and a 20 pad Ceramic LCC or 20 pad PLCC. The MIL-STD-883 data sheet for this device is available on request.

Pinouts

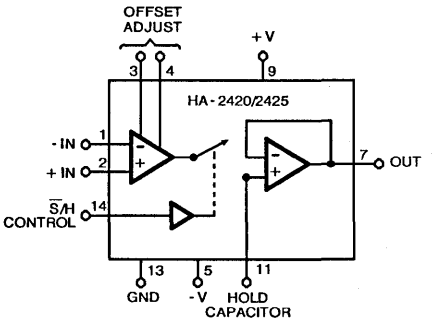
14 PIN CERAMIC/PLASTIC DIP
TOP VIEW



20 PAD LCC/PLCC
TOP VIEW



Functional Diagram



5 SAMPLE AND HOLD AMPLIFIERS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage..... ±24V
Digital Input Voltage (Sample and Hold Pin) ..... +8V, -15V
Output Current ..... Short Circuit Protected
Junction Temperature ..... +175°C

Operating Temperature Range

HA-2420-2.....$-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-2425-5/-7.....$0^{\circ}C \leq T_A \leq +75^{\circ}C$
Storage Temperature Range .....$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

Electrical Specifications

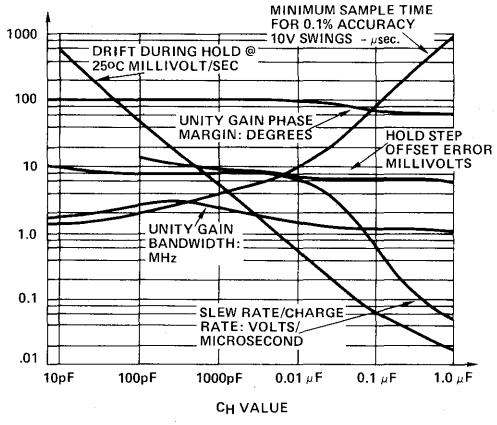
Test Conditions (Unless Otherwise Specified) $V_{SUPPLY} = \pm 15.0V$; $C_H = 1000pF$; Digital Input: $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold), Unity Gain Configuration (Output tied to -Input)

PARAMETER	TEMP	HA-2420-2			HA-2425-5/-7			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10	-	-	±10	-	-	V
Offset Voltage	+25°C	-	2	4	-	3	6	mV
	Full	-	3	6	-	4	8	mV
Bias Current	+25°C	-	40	200	-	40	200	nA
	Full	-	-	400	-	-	400	nA
Offset Current	+25°C	-	10	50	-	10	50	nA
	Full	-	-	100	-	-	100	nA
Input Resistance	+25°C	5	10	-	5	10	-	MΩ
Common Mode Range	Full	±10	-	-	±10	-	-	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 1, 4)	Full	25K	50K	-	25K	50K	-	V/V
Common Mode Rejection (Note 2)	Full	-80	-90	-	-74	-90	-	dB
Hold Mode Feedthrough Attenuation (Note 3)	Full	-	-76	-	-	-76	-	dB
Gain Bandwidth Product (Note 3)	+25°C	-	2.5	-	-	2.5	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10	-	-	±10	-	-	V
Output Current	+25°C	±15	-	-	±15	-	-	mA
Full Power Bandwidth (Notes 3, 4)	+25°C	-	100	-	-	100	-	kHz
Output Resistance (D.C.)	+25°C	-	0.15	-	-	0.15	-	Ω
TRANSIENT RESPONSE								
Rise Time (Notes 3, 5)	+25°C	-	75	100	-	75	100	ns
Overshoot (Notes 3, 5)	+25°C	-	25	40	-	25	40	%
Slew Rate (Notes 3, 6)	+25°C	3.5	5	-	3.5	5	-	V/μs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full	-	-	-0.8	-	-	-0.8	mA
Digital Input Current ($V_{IN} = +5.0V$)	Full	-	-	20	-	-	20	μA
Digital Input Voltage (Low)	Full	-	-	0.8	-	-	0.8	V
Digital Input Voltage (High)	Full	2.0	-	-	2.0	-	-	V
SAMPLE AND HOLD CHARACTERISTICS								
Acquisition Time to 0.1% 10V Step (Note 3)	+25°C	-	2.3	4	-	2.3	4	μs
Acquisition Time to 0.01% 10V Step (Note 3)	+25°C	-	3.2	6	-	3.2	6	μs
Aperture Time (Note 9)	+25°C	-	30	-	-	30	-	ns
Effective Aperture Delay Time	+25°C	-	30	-	-	30	-	ns
Aperture Uncertainty	+25°C	-	5	-	-	5	-	ns
Drift Current (Notes 3, 7)	+25°C	-	5	-	-	5	-	pA
HA1-2420, HA4-2420	Full	-	1.8	10	-	-	-	nA
HA1-2425	Full	-	-	-	-	0.1	1.0	nA
HA3-2425, HA4P2425	Full	-	-	-	-	7.5	10.0	nA
Hold Step Error (Note 7)	+25°C	-	10	20	-	10	20	mV
POWER SUPPLY CHARACTERISTICS								
Supply Current (+)	+25°C	-	3.5	5.5	-	3.5	5.5	mA
Supply Current (-)	+25°C	-	2.5	3.5	-	2.5	3.5	mA
Power Supply Rejection	Full	-80	-90	-	-74	-90	-	dB

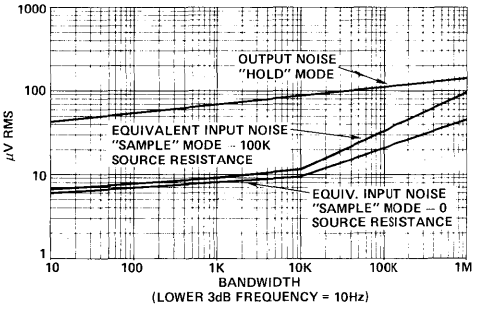
NOTES:
1. $R_L = 2k\Omega$.
2. $V_{CM} = \pm 10VDC$.
3. $A_V = \pm 1$, $R_L = 2k\Omega$, $C_L = 50pF$.
4. $V_{OUT} = 20V$ peak-to-peak.
5. $V_{OUT} = 200mV$ peak-to-peak.
6. $V_{OUT} = 10.0V$ peak-to-peak.
7. $V_{IN} = 0V$.
8. $f_{IN} \leq 100kHz$.
9. Derived from computer simulation only; not tested.

Performance Curves V_{SUPPLY} = ±15VDC, T_A = +25°C, C_H = 1000pF Unless Otherwise Specified

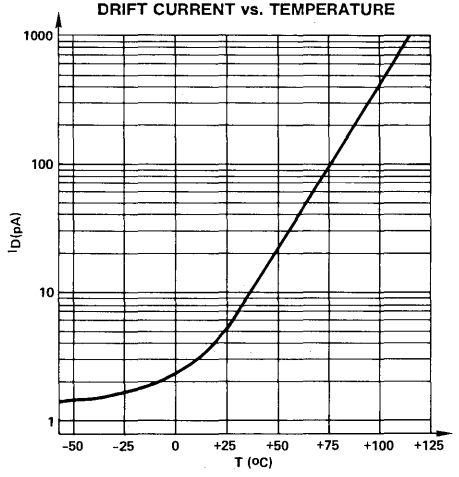
TYPICAL SAMPLE AND HOLD PERFORMANCE AS A FUNCTION OF HOLDING CAPACITOR



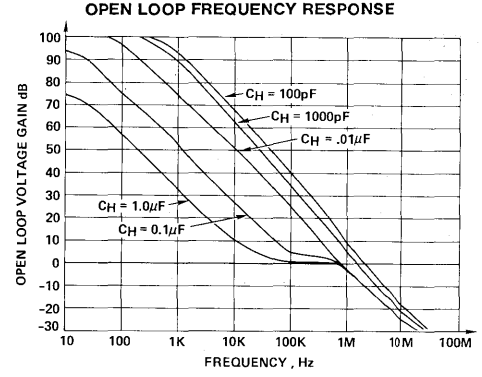
BROADBAND NOISE CHARACTERISTICS



DRIFT CURRENT vs. TEMPERATURE

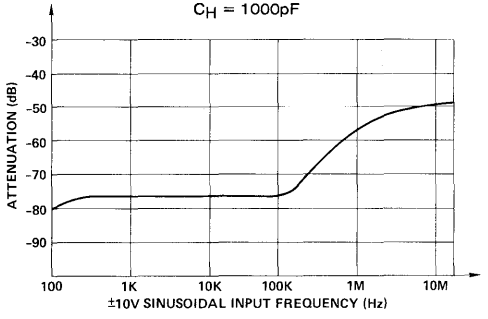


OPEN LOOP FREQUENCY RESPONSE

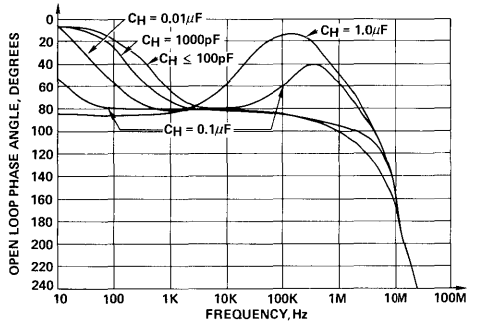


HOLD MODE FEED THROUGH ATTENUATION

C_H = 1000pF

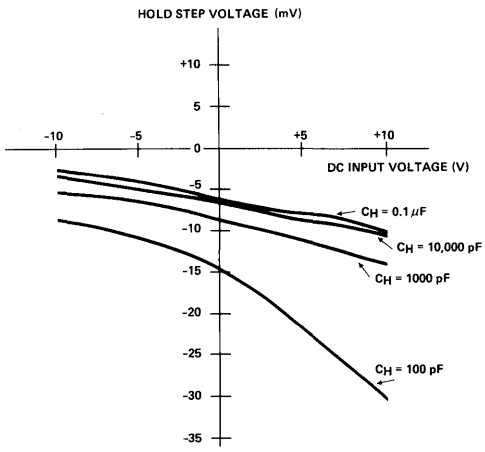


OPEN LOOP PHASE RESPONSE



Offset and Gain Adjustment

HOLD STEP vs. INPUT VOLTAGE



OFFSET ADJUSTMENT

The offset voltage of the HA-2420/2425 may be adjusted using a 100kΩ trim pot, as shown in Figure 6. The recommended adjustment procedure is:

1. Apply zero volts to the sample-and-hold input, and a square wave to the $\overline{S}$/H control.
2. Adjust the trim pot for zero volts output in the hold mode.

GAIN ADJUSTMENT

The linear variation in pedestal voltage with sample-and-hold input voltage causes a -0.06% gain error (C_H = 1000pF). In some applications (D/A deglitcher, A/D converter) the gain error can be adjusted elsewhere in the system, while in other applications it must be adjusted at the sample-and-hold. The two circuits shown below demonstrate how to adjust gain error at the sample-and-hold.

The recommended procedure for adjusting gain error is:

1. Perform offset adjustment.
2. Apply the nominal input voltage that should produce a +10V output.
3. Adjust the trim pot for +10V output in the hold mode.
4. Apply the nominal input voltage that should produce a -10V output.
5. Measure the output hold voltage ($V_{-10\ NOMINAL}$). Adjust the trim pot for an output hold voltage of

$$\frac{(V_{-10\ NOMINAL}) + (-10V)}{2}$$

INVERTING CONFIGURATION

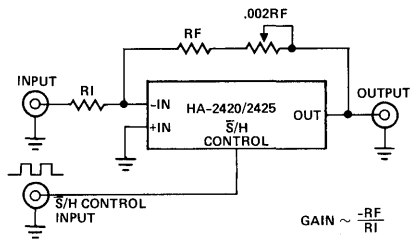


FIGURE 2.

NONINVERTING CONFIGURATION

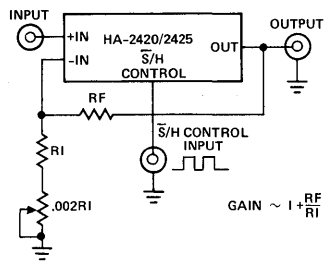


FIGURE 3.

Test Circuits

HOLD STEP ERROR AND DRIFT CURRENT

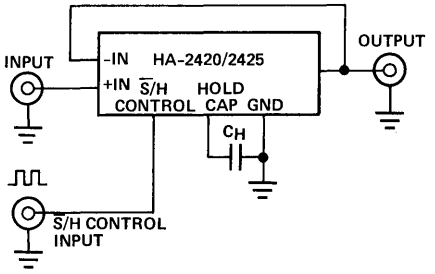
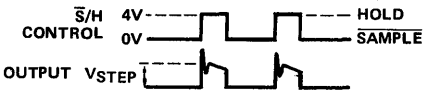


FIGURE 4.

HOLD STEP ERROR TEST

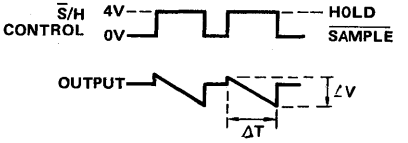
1. With a D.C. input voltage, observe the following waveforms:



2. Set rise/fall times of S/H Control to approximately 20ns.

DRIFT CURRENT TEST

1. With a D.C. input voltage, observe the following waveforms:



2. Measure the slope of the output during hold, $\Delta V/\Delta t$, and compute drift current from: $I_D = C_H \Delta V/\Delta t$.

HOLD MODE FEEDTHROUGH ATTENUATION

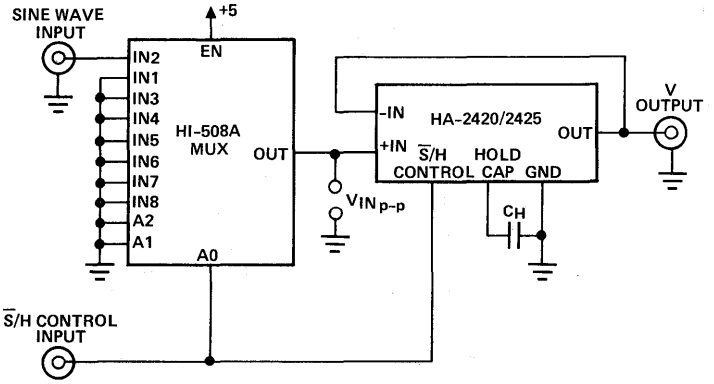


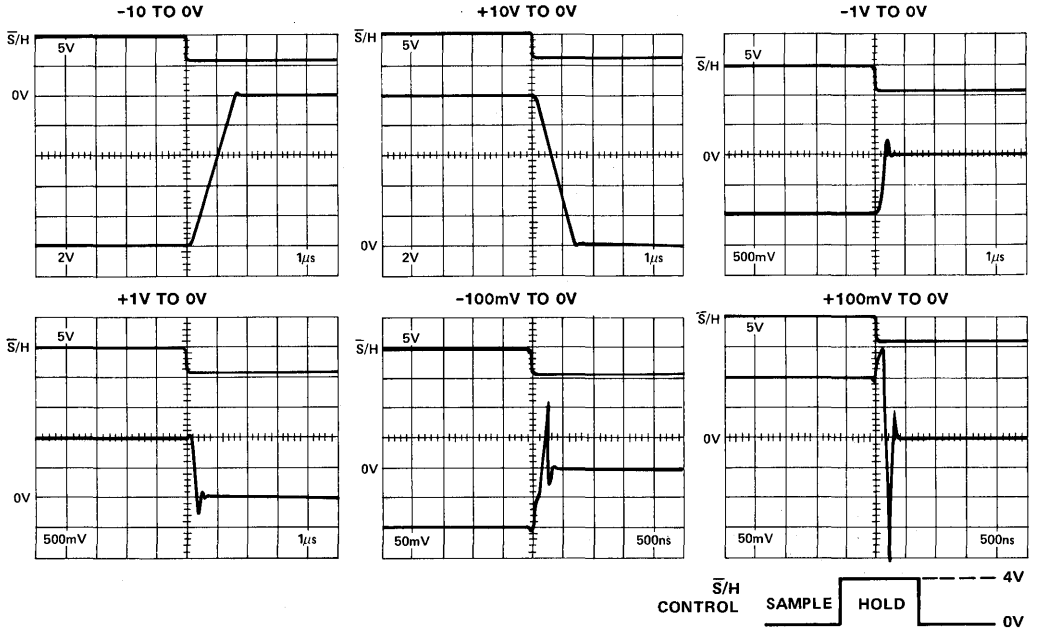
FIGURE 5.

NOTE: Compute hold mode feedthrough attenuation from the formula:

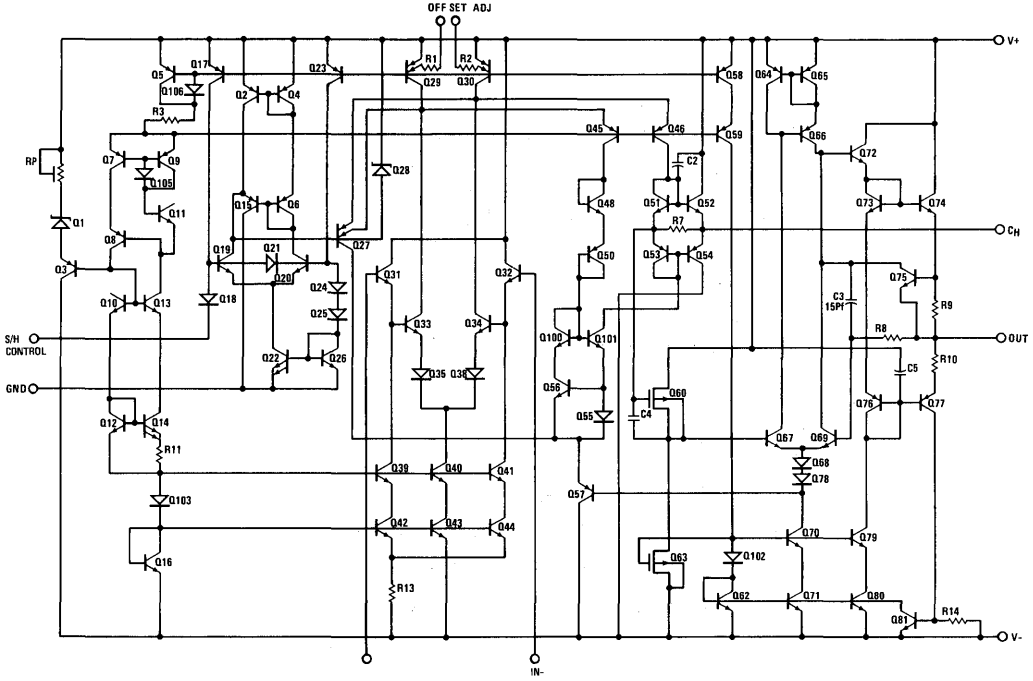
$$\text{Feedthrough Attenuation} = 20 \text{ Log } \frac{V_{OUT\ HOLD}}{V_{IN\ HOLD}}$$

Where V_{OUT} HOLD = Peak-to-Peak value of output sinewave during the hold mode.

Acquisition Times (C_H = 1000pF)



Schematic



Applications

BASIC SAMPLE-AND-HOLD
TOP VIEW

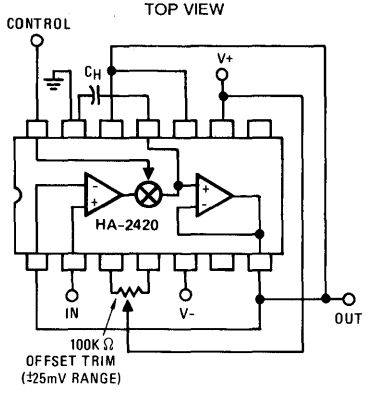


FIGURE 6.

GUARD RING LAYOUT
BOTTOM VIEW

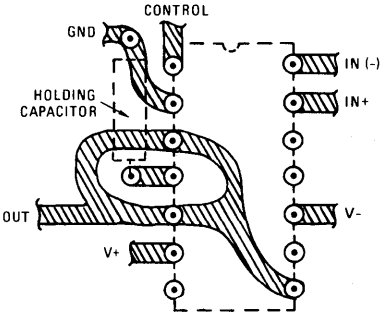


FIGURE 7.

NOTES:

1. Figure 6 shows a typical unity gain circuit, with Offset Zeroing. All of the other normal op amp feedback configurations may be used with the HA-2420/2425. The input amplifier may be used as a gated amplifier by utilizing Pin 11 as the output. This amplifier has excellent drive capabilities along with exceptionally low switch leakage.
2. The method used to reduce leakage paths on the P.C. board and the device package is shown in Figure 7. This guard ring is recommended to minimize the drift during hold mode.
3. The holding capacitor should have extremely high insulation resistance and low dielectric absorption. Polystyrene (below +85°C), Teflon, or Parlene types are recommended.

For more applications, consult Harris Application Note 517, or factory applications group.

Glossary of Terms:

ACQUISITION TIME:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

APERTURE TIME:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

EFFECTIVE APERTURE DELAY TIME (EADT):

The difference between propagation time from the analog input to the S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}/H$ amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

APERTURE UNCERTAINTY:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

DRIFT CURRENT:

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D\ (pA) = C_H\ (pF) \times \frac{\Delta V}{\Delta T}\ (Volts/sec)$$

Die Characteristics

Transistor Count 78
Die Dimensions ..... 97 x 61 x 19 mils
Substrate Potential ..... $-V_{SUPPLY}$
Process ..... Bipolar DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	94	39
Ceramic LCC	88	28

HARRIS

HA-5320

High Speed Precision Monolithic Sample and Hold Amplifier

May 1990

Features

- Gain, D.C. ..... 2 x 10^6 V/V
- Aquisition Time 1.0μs (0.01%)
- Droop Rate ..... 0.08μV/μs (+25°C)
  17μV/μs (Full Temperature)
- Aperture Time 25ns
- Hold Step Error (See Glossary) 1.0mV
- Internal Hold Capacitor
- Fully Differential Input
- TTL Compatible

Applications

- Precision Data Acquisition Systems
- Digital to Analog Converter Deglitcher
- Auto Zero Circuits
- Peak Detector

Description

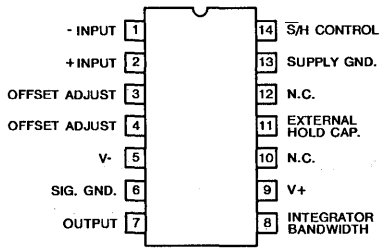
The HA-5320 was designed for use in precision, high speed data acquisition systems.

The circuit consists of an input transconductance amplifier capable of providing large amounts of charging current, a low leakage analog switch, and an output integrating amplifier. The analog switch sees virtual ground as its load; therefore, charge injection on the hold capacitor is constant over the entire input/output voltage range. The pedestal voltage resulting from this charge injection can be adjusted to zero by use of the offset adjust inputs. The device includes a hold capacitor. However, if improved droop rate is required at the expense of acquisition time, additional hold capacitance may be added externally.

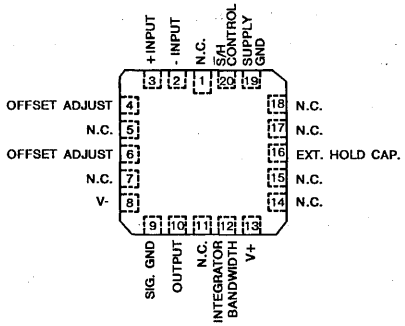
This monolithic device is manufactured using the Harris Dielectric Isolation Process, minimizing stray capacitance and eliminating SCR's. This allows higher speed and latch-free operation. The HA-5320 is available in a Ceramic 14-pin DIP, and a Ceramic 20-pin LCC package. For further information, please see Application Note 538.

Pinouts

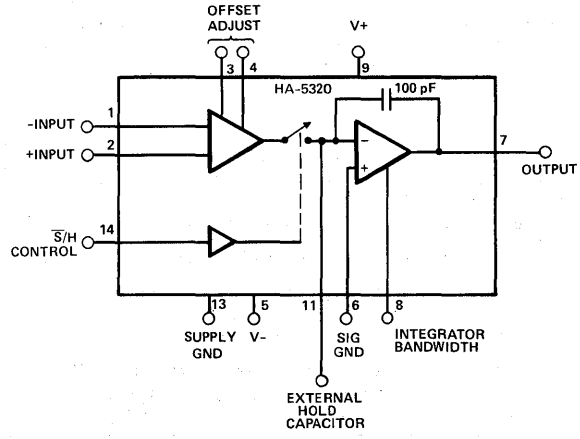
14 PIN CERAMIC DIP
TOP VIEW



20 PIN CERAMIC LCC
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 40V
Differential Input Voltage..... ±24V
Digital Input Voltage ..... +8V, -15V
Output Current, Continuous..... ±20mA (Note 2)
Junction Temperature ..... +175°C

Operating Temperature Range

HA-5320-2/-8 ..... $-55^{o}C \leq T_A \leq +125^{o}C$
HA-5320-5 ..... $0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range ..... $-65^{o}C \leq T_A \leq +150^{o}C$

Electrical Specifications

Test Conditions (Unless Otherwise Specified) $V_{SUPPLY} = \pm 15.0V$; C_H = Internal; Digital Input: $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold), Unity Gain Configuration (Output tied to -Input)

PARAMETER	TEMP	HA-5320-2/-8 MIN	HA-5320-2/-8 TYP	HA-5320-2/-8 MAX	HA-5320-5/-7 MIN	HA-5320-5/-7 TYP	HA-5320-5/-7 MAX	UNITS
INPUT CHARACTERISTICS								
Input Voltage Range	Full	±10	-	-	±10	-	-	V
Input Resistance	+25°C	1	5	-	1	5	-	MΩ
Input Capacitance	+25°C	-	-	3	-	-	3	pF
Offset Voltage	+25°C	-	0.2	-	-	0.5	-	mV
	Full	-	-	2.0	-	-	1.5	mV
Bias Current	+25°C	-	70	200	-	100	300	nA
	Full	-	-	200	-	-	300	nA
Offset Current	+25°C	-	30	100	-	30	300	nA
	Full	-	-	100	-	-	300	nA
Common Mode Range	Full	±10	-	-	±10	-	-	V
CMRR (Note 3)	+25°C	80	90	-	72	90	-	dB
Offset Voltage T.C.	Full	-	5	15	-	5	20	µV/°C
TRANSFER CHARACTERISTICS								
Gain, D.C. (Note 12)	+25°C	10^6	$2x10^6$	-	$3x10^5$	$2x10^6$	-	V/V
Gain Bandwidth Product ($A_V = +1$)	+25°C							
(Note 5) $C_H = 100pF$		-	-	2.0	-	-	2.0	-	MHz
$C_H = 1000pF$		-	-	0.18	-	-	0.18	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage	Full	±10	-	-	±10	-	-	V
Output Current	+25°C	±10	-	-	±10	-	-	mA
Full Power Bandwidth (Note 4)	+25°C	-	600	-	-	600	-	kHz
Output Resistance (Hold Mode)	+25°C	-	1.0	-	-	1.0	-	Ω
Total Output Noise, D.C. to 10MHz								
Sample	+25°C	-	125	200	-	125	200	μV_{RMS}
Hold	+25°C	-	125	200	-	125	200	μV_{RMS}
TRANSIENT RESPONSE								
Rise Time (Note 5)	+25°C	-	100	-	-	100	-	ns
Overshoot (Note 5)	+25°C	-	15	-	-	15	-	%
Slew Rate (Note 6)	+25°C	-	45	-	-	45	-	V/µs
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{IH}	Full	2.0	-	-	2.0	-	-	V
Input Voltage (Low), V_{IL}	Full	-	-	0.8	-	-	0.8	V
Input Current ($V_{IL} = 0V$)	Full	-	-	4	-	-	4	µA
Input Current ($V_{IH} = +5V$)	Full	-	-	0.1	-	-	0.1	µA

Electrical Specifications (Continued)

PARAMETER	TEMP	HA-5320-2/-8			HA-5320-5/-7			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SAMPLE AND HOLD CHARACTERISTICS								
Acquisition Time to 0.1% (Note 7)	+25°C	-	0.8	1.2	-	0.8	1.2	µs
Acquisition Time to 0.01% (Note 7)	+25°C	-	1.0	1.5	-	1.0	1.5	µs
Aperture Time (Note 8)	+25°C	-	25	-	-	25	-	ns
Effective Aperture Delay Time (See Glossary)	+25°C	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty	+25°C	-	0.3	-	-	0.3	-	ns
Droop Rate	+25°C	-	0.08	0.5	-	0.08	0.5	µV/µs
	Full	-	17	100	-	1.2	100	µV/µs
Drift Current (Note 9)	+25°C	-	8	50	-	8	50	pA
	Full	-	1.7	10	-	0.12	10	nA
Charge Transfer (Note 9)	+25°C	-	0.1	0.5	-	0.1	0.5	pC
Hold Mode Settling Time 0.01%	Full	-	165	350	-	165	350	ns
Hold Mode Feedthrough ($10V_{p-p}$, 100kHz)	Full	-	2	-	-	2	-	mV
POWER SUPPLY CHARACTERISTICS								
Positive Supply Current (Note 10)	+25°C	-	11	13	-	11	13	mA
Negative Supply Current (Note 10)	+25°C	-	-11	-13	-	-11	-13	mA
Power Supply Rejection V+	Full	80	-	-	80	-	-	dB
(Note 11) V-	Full	65	-	-	65	-	-	dB

NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below 20mA.
3. V_{CM} = ±5V D.C.
4. $V_O = 20V_{p-p}$; $R_L = 2k\Omega$; $C_L = 50pF$; unattenuated output.
5. $V_O = 200mV_{p-p}$; $R_L = 2k\Omega$; $C_L = 50pF$.
6. V_O = 20V Step; $R_L = 2k\Omega$; $C_L = 50pF$.
7. V_O = 10V Step; $R_L = 2k\Omega$; $C_L = 50pF$.
8. Derived from computer simulation only; not tested.
9. V_{IN} = 0V, V_{IH} = +3.5V, $t_r < 20ns$ (V_{IL} to V_{IH}).
10. Specified for a zero differential input voltage between +IN and -IN. Supply current will increase with differential input (as may occur in the Hold mode) to approximately ±28mA at 20V.
11. Based on a one volt delta in each supply, i.e. 15V ±0.5V D.C.
12. R_L = 1K, C_L = 30pF

Applying the HA-5320

The HA-5320 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Harris Application Note 517 for a collection of circuit ideas.

LAYOUT

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01 to 0.1μF, ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

HOLD CAPACITOR

The HA-5320 includes a 100pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor). Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

If an external hold capacitor C_H is used, then a noise bandwidth capacitor of value 0.1 C_H should be connected from pin 8 to ground. Exact value and type are not critical.

The hold capacitor C_H should have high insulation resistance and low dielectric absorption, to minimize droop errors. Polystyrene dielectric is a good choice for operating temperatures up to +85°C. Teflon® and glass dielectrics offer good performance to +125°C and above.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

®Teflon is a registered Trademark of Dupont Corporation.

Applications

Figure 1 shows the HA-5320 connected as a unity gain noninverting amplifier — its most widely used configuration. As an input device for a fast successive — approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5320's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12-bit accurate output from the converter.

The application may call for an external hold capacitor C_H as shown. As mentioned earlier, $0.1C_H$ is then recommended at pin 8 to reduce output noise in the Hold mode.

The HA-5320 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

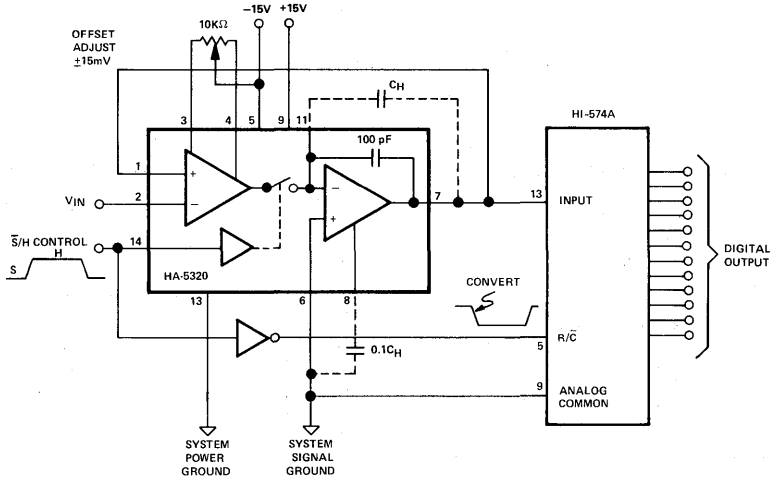
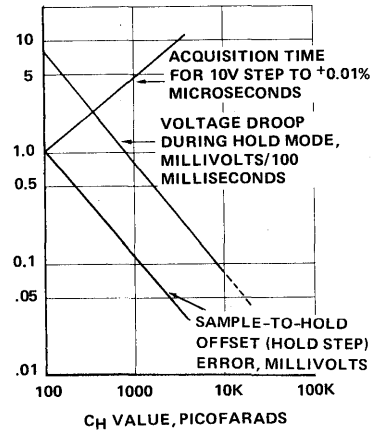


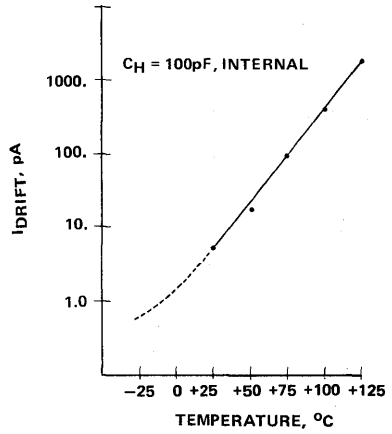
FIGURE 1.
TYPICAL HA-5320 CONNECTIONS; NONINVERTING UNITY GAIN MODE
NOTE: Pin Numbers Refer to DIP Package Only.

Performance Curves $V_{SUPPLY} = \pm 15VDC$

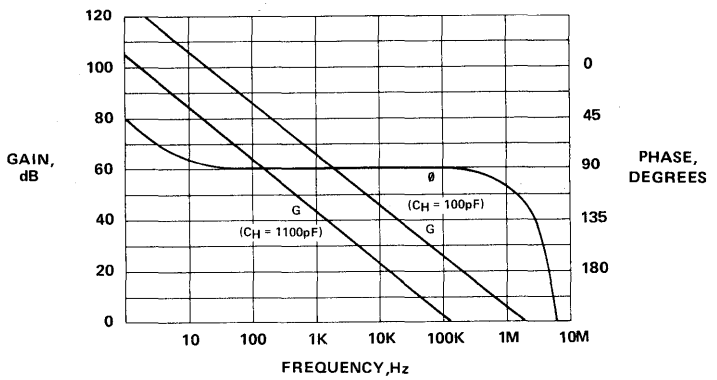
TYPICAL SAMPLE AND HOLD PERFORMANCE AS FUNCTION OF HOLDING CAPACITOR



DRIFT CURRENT vs. TEMPERATURE

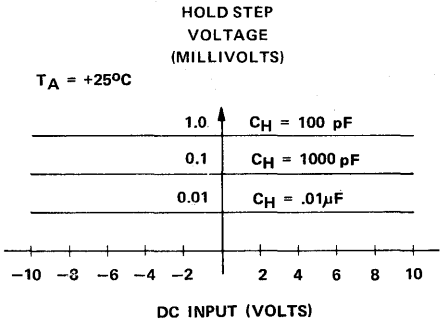


OPEN LOOP GAIN AND PHASE RESPONSE

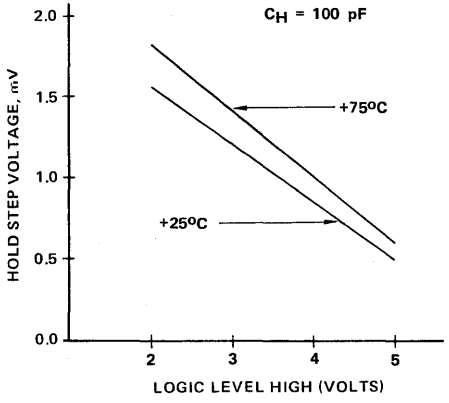


TYPICAL SAMPLE-TO-HOLD OFFSET (HOLD STEP) ERROR

HOLD STEP vs. INPUT VOLTAGE

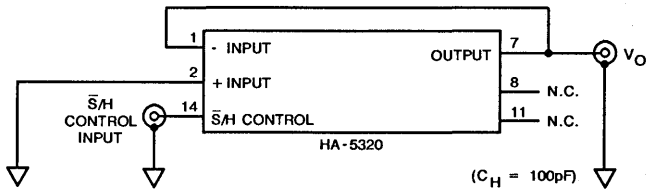


HOLD STEP vs. LOGIC (V_{IH}) VOLTAGE



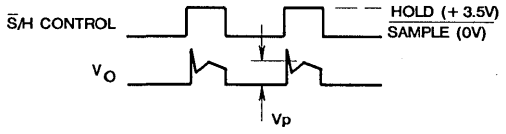
Test Circuits

CHARGE TRANSFER AND DRIFT CURRENT



CHARGE TRANSFER TEST

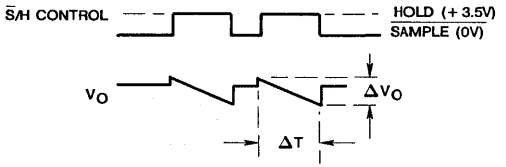
1. Observe the "hold step" voltage V_p:



2. Compute charge transfer: $Q = V_p C_H$

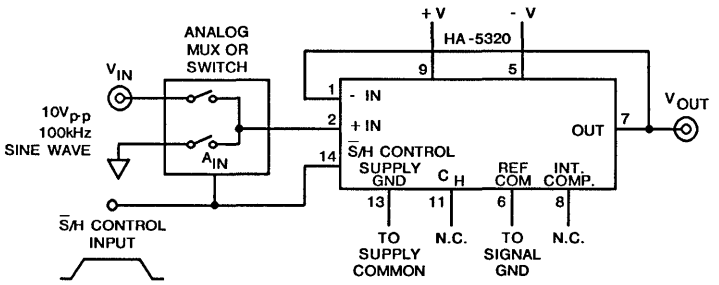
DRIFT CURRENT TEST

1. Observe the voltage "droop", $\Delta V_O/\Delta T$:



2. Measure the slope of the output during hold, $\Delta V_O/\Delta T$, and compute drift current: $I_D = C_H \ \Delta V_O/\Delta T$.

HOLD MODE FEED THROUGH ATTENUATION



Feedthrough in dB = 20 Log $\frac{V_{OUT}}{V_{IN}}$ where:

V_{OUT} = Volts$_{p-p}$, Hold Mode,

V_{IN} = Volts$_{p-p}$.

Glossary of Terms

ACQUISITION TIME:

The time required following a "sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

CHARGE TRANSFER:

The small charge transferred to the holding capacitor from the inter-electrode capacitance of the switch when the unit is switched to the HOLD mode. Charge transfer is directly proportional to sample-to-hold offset pedestal error, where:

$$\text{Charge Transfer (pC)} = C_H \text{ (pF)} \times \text{Offset Error (V)}$$

APERTURE TIME:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is the interval between the conditions of 10% open and 90% open.

HOLD STEP ERROR:

Hold Step Error is the output error due to Charge Transfer (see above). It may be calculated from the specified parameter, Charge Transfer, using the following relationship:

$$\text{HOLD STEP (V)} = \frac{\text{CHARGE TRANSFER (pC)}}{\text{HOLD CAPACITANCE (pF)}}$$

See Performance Curves.

EFFECTIVE APERTURE DELAY TIME (EADT):

The difference between propagation time from the analog input to S/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}$/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

APERTURE UNCERTAINTY:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

DRIFT CURRENT:

The net leakage current from the hold capacitor during the hold mode. Drift current can be calculated from the droop rate using the formula:

$$I_D \text{ (pA)} = C_H \text{ (pF)} \times \frac{\Delta V}{\Delta T} \text{ (Volts/sec)}$$

Die Characteristics

Transistor Count	175
Die Dimensions	90.2 x 143.7 x 19 mils
Substrate Potential	$-V_{SUPPLY}$
Process	Bipolar DI

Thermal Constants (C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	75	15
Ceramic LCC	76	19

HARRIS

HA-5330

Very High Speed Precision Monolithic Sample and Hold

May 1990

Features

- Very Fast Acquisition 350ns (0.1%) 500ns (0.01%)
- Low Droop Rate 0.01μV/μs
- Very Low Offset 0.2mV
- High Slew Rate 90V/μs
- Wide Supply Range ..... ±11V to ±18V
- Internal Hold Capacitor
- Fully Differential Input
- TTL/CMOS Compatible

Applications

- Precision Data Acquisition Systems
- D/A Converter Deglitching
- Auto-Zero Circuits
- Peak Detectors

Description

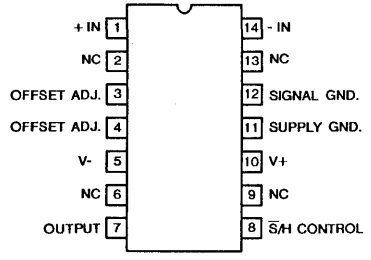
The HA-5330 is a very fast sample and hold amplifier designed primarily for use with high speed A/D converters. It utilizes the Harris Dielectric Isolation process to achieve a 500ns acquisition time to 12-bit accuracy and a droop rate of 0.01μV/μs. The circuit consists of an input transconductance amplifier capable of producting large amounts of charging current, a low leakage analog switch, and an integrating output stage which includes a 90pF hold capacitor.

The analog switch operates into a virtual ground, so charge injection on the hold capacitor is constant and independent of V_{IN}. Charge injection is held to a low value by compensation circuits and, if necessary, the resulting 0.5mV hold step error can be adjusted to zero via the Offset Adjust terminals. Compensation is also used to minimize leakage currents which cause voltage droop in the Hold mode.

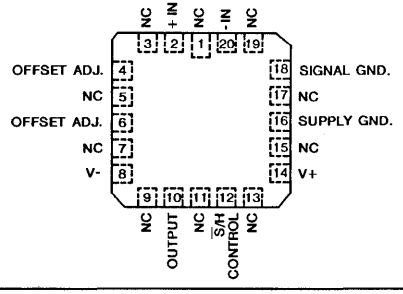
The HA-5330 will operate at reduced supply voltages (to ±11V) with a reduced signal range. This monolithic device is available in a 14 pin Ceramic DIP and a 20 pad LCC package. The MIL-STD-883 data sheet for this device is available on request.

Pinouts

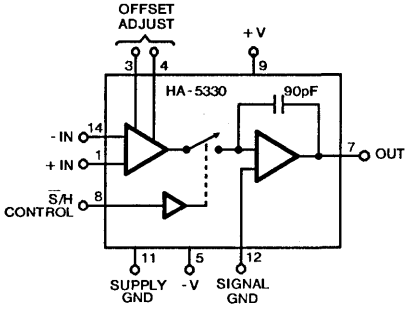
14 PIN CERAMIC DIP
TOP VIEW



20 PAD (LCC)
TOP VIEW



Functional Diagram



5
SAMPLE AND HOLD AMPLIFIERS

CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage between V+ and SUPPLY/SIG GND ..... +20V
Voltage between V- and SUPPLY/SIG GND ..... -20V
Voltage between SUPPLY GND and SIG GND ..... ±2.0V
Differential Input Voltage ..... ±24V
Voltage between $\overline{S}$/H Control and SUPPLY/SIG GND ... +8V, -6V
Output Current, Continuous ..... ±17mA (Note 2)
Junction Temperature ..... +175°C

Operating Temperature Range

HA-5330-2 ..... -55°C to +125°C
HA-5330-4 ..... -25°C to +85°C
HA-5330-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

Test Conditions Unless Otherwise Specified: V_{SUPPLY} = ±15V; S/H Control V_{IL} = +0.8V (Sample): V_{IH} = +2.0V (Hold); SIG GND = SUPPLY GND, Unity Gain Configuration (Output tied to -Input)

PARAMETER		TEMP	HA-5330-2, -4			HA-5330-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Input Voltage Range		Full	±10	-	-	±10	-	-	V
Input Resistance (Note 3)		+25°C	5	15	-	5	15	-	MΩ
Input Capacitance		+25°C	-	3	-	-	3	-	pF
Offset Voltage		+25°C	-	0.2	-	-	0.2	-	mV
		Full	-	-	2.0	-	-	1.5	mV
Offset Voltage Temperature Coefficient		Full	-	1	10	-	1	10	µV/°C
Bias Current		+25°C	-	±20	-	-	±20	-	nA
		Full	-	-	±500	-	-	±300	nA
Offset Current		+25°C	-	20	-	-	20	-	nA
		Full	-	-	500	-	-	300	nA
Common Mode Range		Full	±10	-	-	±10	-	-	V
CMRR (Note 4)		Full	86	100	-	86	100	-	dB
TRANSFER CHARACTERISTICS									
Gain, DC		Full	2×10^6	2×10^7	-	2×10^6	2×10^7	-	V/V
Gain Bandwidth Product (Note 12)		+25°C	-	4.5	-	-	4.5	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage		Full	±10	-	-	±10	-	-	V
Output Current		Full	±10	-	-	±10	-	-	mA
Full Power Bandwidth (Note 6)		+25°C	-	1.4	-	-	1.4	-	MHz
Output Resistance	Hold Mode	+25°C	-	0.2	-	-	0.2	-	Ω
	Sample Mode	+25°C	-	10^{-5}	0.001	-	10^{-5}	0.001	Ω
Total Output Noise, DC to 4.0MHz	Sample Mode	+25°C	-	230	-	-	230	-	µV RMS
	Hold Mode	+25°C	-	190	-	-	190	-	µV RMS

Die Characteristics

Transistor Count 205
Die Dimensions ..... 99 x 166 x 19 mils
Substrate Potential ..... SIG. GND
Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	75	15
Ceramic LCC	76	19

Electrical Specifications (Continued)

PARAMETER	TEMP	HA-5330-2, -4			HA-5330-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TRANSIENT RESPONSE								
Rise Time (Note 5)	+25°C	-	70	-	-	70	-	ns
Overshoot (Note 5)	+25°C	-	10	-	-	10	-	%
Slew Rate (Note 7)	+25°C	-	90	-	-	90	-	V/µs
DIGITAL INPUT CHARACTERISTICS								
Input Voltage (High), V_{IH}	Full	2.0	-	-	2.0	-	-	V
Input Voltage (Low), V_{IL}	Full	-	-	0.8	-	-	0.8	V
Input Current (V_{IL} = 0V)	Full	-	10	40	-	10	40	µA
Input Current (V_{IH} = +5V)	Full	-	10	40	-	10	40	µA
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time (Note 8) (0.1%)	+25°C	-	350	-	-	350	-	ns
	Full	-	-	500	-	-	500	ns
(0.01%)	+25°C	-	500	-	-	500	-	ns
	Full	-	-	900	-	-	900	ns
Aperture Time (Note 3)	+25°C	-	20	-	-	20	-	ns
Effective Aperture Delay Time (See Glossary)	+25°C	-50	-25	0	-50	-25	0	ns
Aperture Uncertainty	+25°C	-	0.1	-	-	0.1	-	ns
Droop Rate (Note 9)	+25°C	-	0.01	-	-	0.01	-	µV/µs
	Full	-	-	100	-	-	10	µV/µs
Hold Step Error (Note 10)	+25°C	-	0.5	-	-	0.5	-	mV
Hold Mode Settling Time (0.01%)	+25°C	-	100	200	-	100	200	ns
Hold Mode Feedthru 20V_{p-p}, 100kHz	Full	-	-88	-	-	-88	-	dB
POWER SUPPLY CHARACTERISTICS								
Positive Supply Current	Full	-	18	22	-	18	24	mA
Negative Supply Current	Full	-	19	23	-	19	25	mA
Power Supply Rejection, V+, V- (Note 11)	Full	86	100	-	86	100	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Internal Power Dissipation may limit Output Current below ±17mA.
3. Derived from computer simulation only; not tested.
4. $+V_{CM}$ = ±10V DC.
5. V_i = 200mV Step; R_L = 2K; C_L = 50pF
6. Full power bandwidth based on slew rate measurement using $FPBW = \frac{SLEW\ RATE}{2\pi\ Vpeak}$

   Distortion of wave shape occurs beyond 100KHz due to slew rate enhancement circuitry
7. V_O = 20V Step; R_L = 2K; C_L = 50pF.
8. V_O = 10V Step; R_L = 2K; C_L = 50pF.
9. This parameter is measured at ambient temperature extremes in a high speed test environment. Consequently, steady state heating effects from internal power dissipation are not included.
10. V_{IN} = 0V; V_{IH} = +3.5V; t_r = 22ns (V_{IL} to V_{IH}). See graph.
11. Based on a three volt delta in each supply, i.e. 15V = ±1.5V DC.
12. V_{OUT} = 200mV_{p-p}, R_L = 2K, C_L = 50pF.

Applying the HA-5330

The HA-5330 has the uncommitted differential inputs of an op amp, allowing the Sample/Hold function to be combined with many conventional op amp circuit ideas. See the Harris Application Note 517 for a collection of circuit ideas.

Layout

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01 to 0.1μF, ceramic) should be provided from each power supply terminal to the Supply GND Terminal on pin 11.

Applications

The HA-5330 is configured as a unity gain noninverting amplifier by simply connecting the output (pin 7) to the inverting input (pin 14). As an input device for a fast successive - approximation A/D converter, it offers an extremely high throughput rate. Also, the HA-5330's pedestal error is adjustable to zero by using an Offset Adjust potentiometer (10K to 50K) center tapped to V-.

The ideal ground connections are pin 11 (Supply Ground) directly to the system Supply Common, and pin 12 (Signal Ground) directly to the system Signal Ground (Analog Ground).

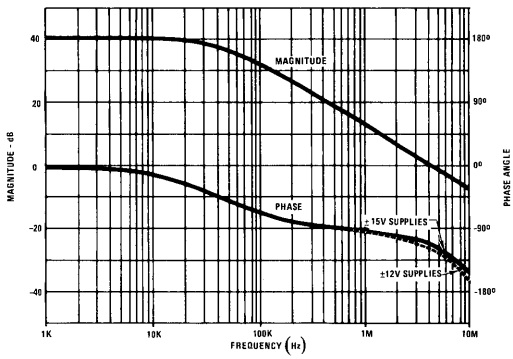
Hold Capacitor

The HA-5330 includes a 90pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on the internal capacitor).

Output Stage

The HA-5330 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the $\overline{S}$/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

MAGNITUDE AND PHASE RESPONSE
(Closed Loop Gain = 100)



Glossary of Terms

Acquisition Time:

The time required following a sample" command, for the output to reach its final value within ±0.1% or ±0.01%. This is the minimum sample time required to obtain a given accuracy, and includes switch delay time, slewing time and settling time.

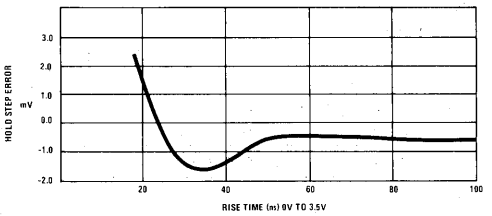
Aperture Time:

The time required for the sample-and-hold switch to open, independent of delays through the switch driver and input amplifier circuitry. The switch opening time is that interval between the conditions of 10% open and 90% open.

Hold Step Error:

Hold step error is the output shift due to charge transfer from the sample to the hold mode. It is also referred to as "offset step" or "pedestal error".

HOLD STEP ERROR vs. $\overline{S}$/H CONTROL RISE TIME



Effective Aperture Delay Time (EADT):

The difference between propagation time from the analog input to the $\overline{S}$/H switch, and digital delay time between the Hold command and opening of the switch.

EADT may be positive, negative or zero. If zero, the $\overline{S}$/H amplifier will output a voltage equal to V_{IN} at the instant the Hold command was received. For negative EADT, the output in Hold (exclusive of pedestal and droop errors) will correspond to a value of V_{IN} that occurred before the Hold command.

Aperture Uncertainty:

The range of variation in Effective Aperture Delay Time. Aperture Uncertainty (also called Aperture Delay Uncertainty, Aperture Time Jitter, etc.) sets a limit on the accuracy with which a waveform can be reconstructed from sample data.

HARRIS

HA-5340

May 1990

High Speed, Low Distortion, Precision Monolithic Sample and Hold Amplifier

Features

- Fast Acquisition Time (0.01%) 700ns
- Fast Hold Mode Settling Time (0.01%) 200ns
- Low Distortion (Hold Mode) ..... -72dBc (V_{IN} = 200kHz, Fs = 450kHz, 5Vp-p)
- Bandwidth Minimally Affected By External C_H
- Fully Differential Analog Inputs
- Built-in 135pF Hold Capacitor
- Pin Compatible with HA-5320

Applications

- High Bandwidth Precision Data Acquisition Systems
- Inertial Navigation and Guidance Systems
- Ultrasonics
- SONAR
- RADAR

Ordering Information

MODEL NUMBER	OPERATING TEMPERATURE RANGE	PRODUCT DESCRIPTION
HA1-5340-5	0°C to +75°C	14 Pin Ceramic DIP
HA1-5340-9	-40°C to +85°C	14 Pin Ceramic DIP

Description

The HA-5340 combines the advantages of two sample/hold architectures to create a new generation of monolithic sample/hold. High amplitude, high frequency signals can be sampled with very low distortion being introduced. The combination of exceptionally fast acquisition time and specified/characterized hold mode distortion is an industry first. Additionally, the AC performance is only minimally affected by additional hold capacitance.

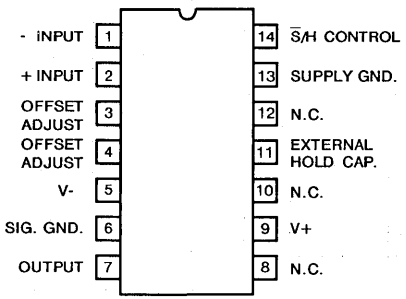
To achieve this level of performance, the benefits of an integrating output stage have been combined with the advantages of a buffered hold capacitor. To the user this translates to a front-end stage that has high bandwidth due to charging only a small capacitive load and an output stage with constant pedestal error which can be nulled out using the offset adjust pins. Since the performance penalty for additional hold capacitance is low, the designer can further minimize pedestal error and droop rate without sacrificing speed.

Low distortion, fast acquisition, and low droop rate are the result, making the HA-5340 the obvious choice for high speed, high accuracy sampling systems.

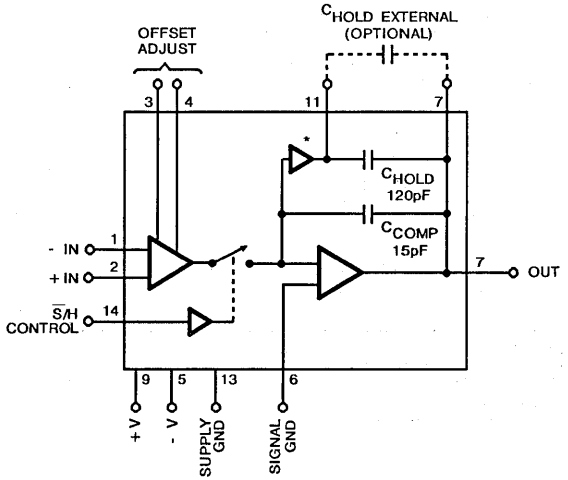
For a Military temperature range version request the HA-5340/883 data sheet.

Pinout

HA1-5340 (CERAMIC DIP)
TOP VIEW



Functional Diagram



* Buffer acts as a buffer in sample mode, acts as a closed switch in hold mode.

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 36V
Differential Input Voltage 24V
Digital Input Voltage ..... +8V, -6V
Output Current, Continuous ..... ±20mA
Junction Temperature ..... +175°C

Operating Temperature Range

HA-5340-9 ..... $-40^{o}C \leq T_A \leq +85^{o}C$
HA-5340-5 ..... $0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range ..... $-65^{o}C \leq T_A \leq +150^{o}C$

Electrical Specifications Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = ±15.0V; C_H = Internal = 135pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold). Non-Inverting Unity Gain Configuration (Output tied to -Input), R_L = 2K, C_L = 60pF

PARAMETER	TEMP	HA-5340-9 HA-5340-5 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Input Voltage Range	Full	-10	-	+10	V
Input Resistance (Note 2)	+25°C	-	1	-	MΩ
Input Capacitance	+25°C	-	-	3	pF
Input Offset Voltage	+25°C	-	-	1.5	mV
	Full	-	-	3.0	mV
Offset Voltage Temperature Coefficient	Full	-	-	30	µV/°C
Bias Current	+25°C	-	±70	-	nA
	Full	-	-	±350	nA
Offset Current	+25°C	-	±50	-	nA
	Full	-	-	±350	nA
Common Mode Range	Full	-10	-	+10	V
CMRR (±10 Vdc) (Note 3)	+25°C	-	83	-	dB
	Full	72	-	-	dB
TRANSFER CHARACTERISTICS					
Gain, DC	+25°C	110	140	-	dB
Gain Bandwidth Product C_H External = 0pF	Full	-	10	-	MHz
C_H External = 100pF	Full	-	9.6	-	MHz
C_H External = 1000pF	Full	-	6.7	-	MHz
TRANSIENT RESPONSE					
Rise Time (200mV step)	+25°C	-	20	30	ns
Overshoot (200mV step)	+25°C	-	35	50	%
Slew Rate (10V step)	+25°C	40	60	-	V/µs
DIGITAL INPUT CHARACTERISTICS					
Input Voltage (High), V_{IH}	Full	2.0	-	-	V
Input Voltage (Low), V_{IL}	Full	-	-	0.8	V
Input Current V_{IL} = 0V I_{IL}	Full	-	7	40	µA
Input Current V_{IH} = 5V I_{IH}	Full	-	4	40	µA
OUTPUT CHARACTERISTICS					
Output Voltage	Full	-10	-	+10	V
Output Current	Full	-10	-	+10	mA
Full Power Bandwidth (Slew Rate Limited) (Note 4)	Full	0.6	0.9	-	MHz
Output Resistance - Hold Mode	+25°C	-	0.05	0.1	Ω
	Full	-	0.07	0.15	Ω
TOTAL OUTPUT NOISE, D.C. TO 10MHz					
Sample Mode	+25°C	-	325	400	µVrms
Hold Mode	+25°C	-	325	400	µVrms

Electrical Specifications Test Conditions (Unless Otherwise Specified) V_{SUPPLY} = ±15.0V; C_H = Internal = 135pF; Digital Input: V_{IL} = +0.8V (Sample), V_{IH} = +2.0V (Hold). Non-Inverting Unity Gain Configuration (Output tied to -Input), R_L = 2K, C_L = 60pF

PARAMETER		TEMP	HA-5340-9 HA-5340-5 MIN	TYP	MAX	UNITS
DISTORTION CHARACTERISTICS						
SAMPLE MODE						
Signal to Noise Ratio (RMS Signal to RMS noise)	V_{IN} = 200kHz (20Vp-p)	Full	-	115	-	dB
Total Harmonic Distortion	V_{IN} = 200kHz, 5Vp-p	Full	-90	-100	-	dBc
	V_{IN} = 200kHz, 10Vp-p	Full	-76	-82	-	dBc
	V_{IN} = 200kHz, 20Vp-p	Full	-70	-74	-	dBc
	V_{IN} = 500kHz, 5Vp-p	Full	-66	-75	-	dBc
Intermodulation Distortion V_{IN} = 10Vp-p	(f1 = 20kHz, f2 = 21kHz)	Full	-78	-83	-	dBc
HOLD MODE (50% Duty Cycle $\overline{S}$/H)						
Signal to Noise Ratio (RMS Signal to RMS noise)						
Fs = 450kHz	V_{IN} = 200kHz, 5Vp-p	+25°C	-	76	-	dB
	V_{IN} = 200kHz, 10Vp-p	+25°C	-	76	-	dB
Total Harmonic Distortion						
Fs = 450kHz	V_{IN} = 200kHz, 5Vp-p	+25°C	-	-72	-	dBc
	V_{IN} = 200kHz, 10Vp-p	+25°C	-	-66	-	dBc
	V_{IN} = 200kHz, 20Vp-p	+25°C	-	-56	-	dBc
Fs = 450kHz	V_{IN} = 100kHz, 5Vp-p	+25°C	-	-84	-	dBc
	V_{IN} = 100kHz, 10Vp-p	+25°C	-	-71	-	dBc
	V_{IN} = 100kHz, 20Vp-p	+25°C	-	-61	-	dBc
Fs = $2f_{IN}$(Nyquist)	V_{IN} = 20kHz, 5Vp-p	+25°C	-	-95	-	dBc
	V_{IN} = 50kHz, 5Vp-p	+25°C	-	-91	-	dBc
	V_{IN} = 100kHz, 5Vp-p	+25°C	-	-82	-	dBc
Intermodulation Distortion Fs = 450kHz	V_{IN} = 10Vp-p (f1 = 20kHz, f2 = 21kHz)	+25°C	-	-79	-	dBc
SAMPLE/HOLD CHARACTERISTICS						
Acquisition Time	10V Step to 0.01%	+25°C	-	700	-	ns
		Full	-	-	900	ns
	10V Step to 0.1%	+25°C	-	430	600	ns
Droop Rate (C_H = Internal)		+25°C	-	0.1	-	µV/µs
		Full	-	-	95	µV/µs
Hold Step Error (V_{IL} = 0V, V_{IH} = 4.0V, t_r = 5ns)		+25°C	-15	-	+15	mV
Hold Mode Settling Time (to ±1mV)		Full		200	300	ns
Hold Mode Feedthrough (20Vp-p, 200kHz, sine)		Full	-	-76	-	dB
EADT (Effective Aperture Delay Time)		+25°C	-	-15	-	ns
Aperture Uncertainty		+25°C	-	0.2	-	ns
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current		Full	-	19	25	mA
Negative Supply Current		Full	-	19	25	mA
PSRR (V or -V, 10% delta)		Full	75	82	-	dB

NOTES: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

2. Derived from Computer Simulation only, not tested.

3. +CMRR is measured from 0V to +10V, -CMRR is measured from 0V to -10V

4. Based on the calculation FPBW = Slew Rate/2πVpeak (Vpeak = 10V).

Applying the HA-5340

The HA-5340 has the uncommitted differential inputs of an op amp, allowing the Sample and Hold function to be combined with many conventional op amp circuits. See the Harris Application Note 517 for a collection of circuit ideas.

LAYOUT

A printed circuit board with ground plane is recommended for best performance. Bypass capacitors (0.01 to 0.1μF, ceramic) should be provided from each power supply terminal to the Supply Ground terminal on pin 13.

The ideal ground connections are pin 6 (SIG. Ground) directly to the system Signal Ground, and pin 13 (Supply Ground) directly to the system Supply Common.

HOLD CAPACITOR

The HA-5340 includes a 135pF MOS hold capacitor, sufficient for most high speed applications (the Electrical Specifications section is based on this internal capacitor). Additional capacitance may be added between pins 7 and 11. This external hold capacitance will reduce droop rate at the expense of acquisition time, and provide other trade-offs as shown in the Performance Curves.

The hold capacitor C_H should have high insulation resistance and low dielectric absorption, to minimize droop errors. Teflon®, polystyrene and polypropylene dielectric capacitor types offer good performance over the specified operating temperature range.

The hold capacitor terminal (pin 11) remains at virtual ground potential. Any PC connection to this terminal should be kept short and "guarded" by the ground plane, since nearby signal lines or power supply voltages will introduce errors due to drift current.

®Teflon is a registered Trademark of Dupont Corporation.

Applications

Figure 1 shows the HA-5340 connected as a unity gain noninverting amplifier — its most widely used configuration. As an input device for a fast successive — approximation A/D converter, it offers very high throughput rate for a monolithic IC sample/hold amplifier. Also, the HA-5340's hold step error is adjustable to zero using the Offset Adjust potentiometer, to deliver a 12-bit accurate output from the converter.

The HA-5340 output circuit does not include short circuit protection, and consequently its output impedance remains low at high frequencies. Thus, the step changes in load current which occur during an A/D conversion are absorbed at the S/H output with minimum voltage error. A momentary short circuit to ground is permissible, but the output is not designed to tolerate a short of indefinite duration.

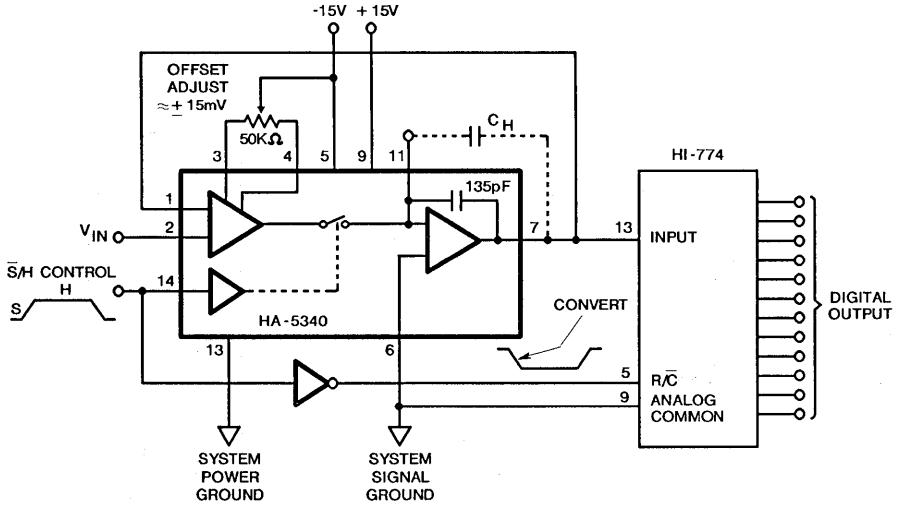
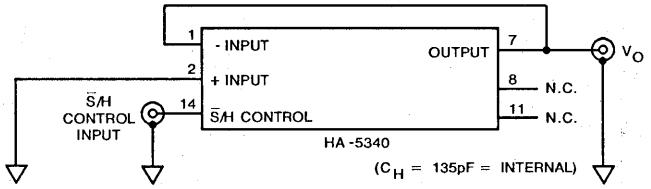


FIGURE 1.
TYPICAL HA-5340 CONNECTIONS; NONINVERTING UNITY GAIN MODE
NOTE: Pin Numbers Refer to DIP Package Only.

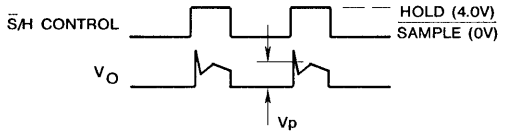
Test Circuits

HOLD STEP ERROR AND DROOP RATE



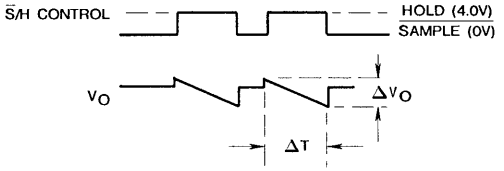
HOLD STEP ERROR

1. Observe the "hold step" voltage V_p:



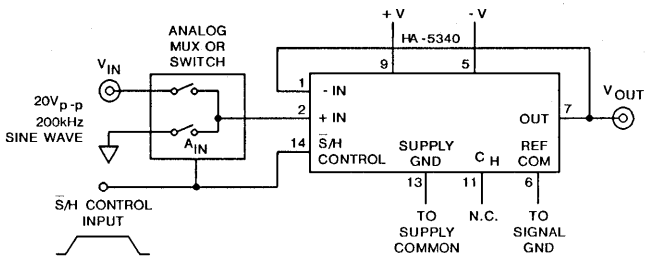
Ddroop RATE TEST

1. Observe the voltage "droop", $\Delta V_O/\Delta T$:



2. Measure the slope of the output during hold, $\Delta V_O/\Delta T$.
3. Droop can be positive or negative - usually to one rail or the other not to GND.

HOLD MODE FEED THROUGH ATTENUATION



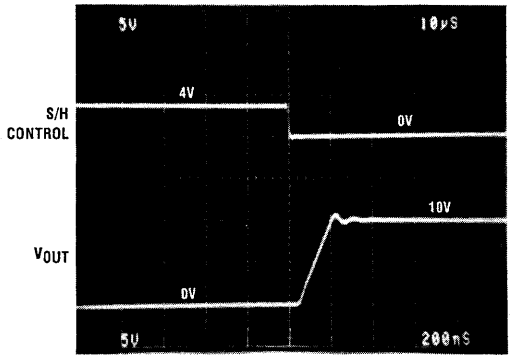
Feedthrough in dB = 20 Log $\frac{V_{OUT}}{V_{IN}}$ where:

V_{OUT} = Volts$_{p-p}$, Hold Mode,

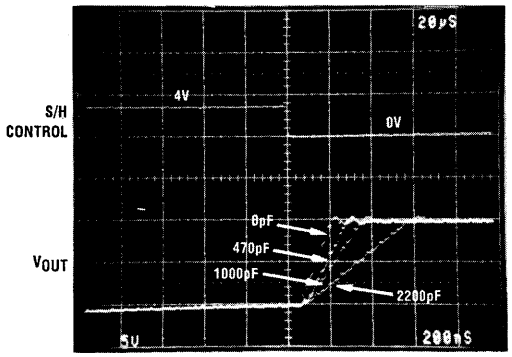
V_{IN} = Volts$_{p-p}$.

Performance Curves $V_S = \pm 15V$, $T_A = +25^oC$, unless otherwise specified.

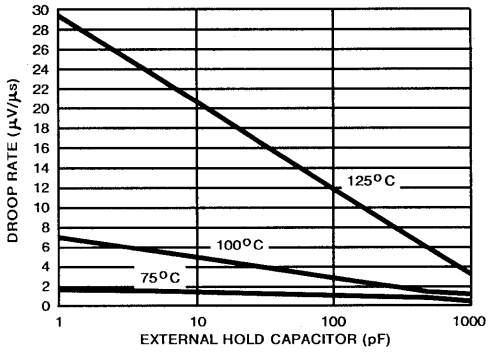
T_{ACQ} POS 0 TO +10 STEP



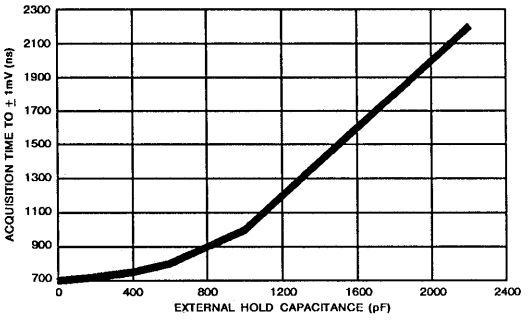
T_{ACQ} vs. ADDITIONAL C_H



DROOP RATE vs. HOLD CAPACITOR SIZE

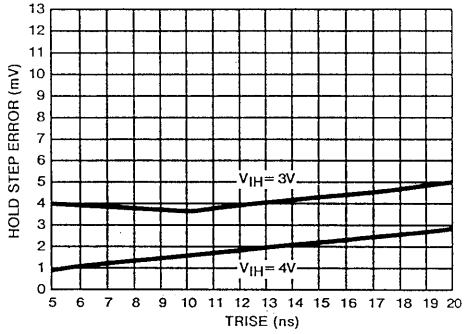


ACQUISITION TIME (0.01%) vs. HOLD CAPACITANCE

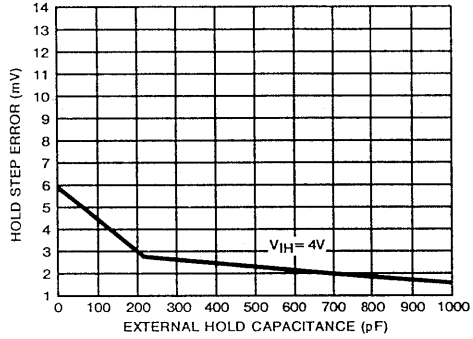


Performance Curves (Continued) $V_S = \pm 15V$, $T_A = +25^oC$, unless otherwise specified.

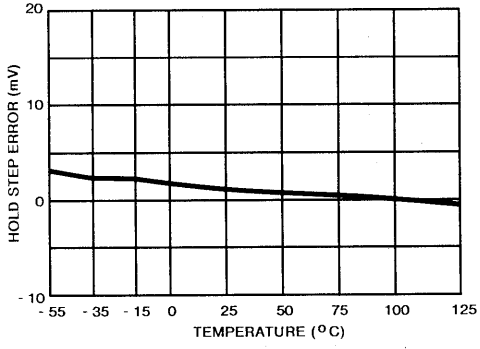
HOLD STEP ERROR vs. T_{RISE}
C_H = Internal; Temperature = $+25^oC$



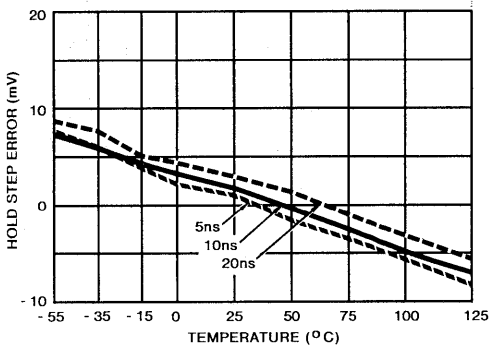
HOLD STEP ERROR vs. HOLD CAPACITANCE
T_{RISE} = 5ns; Temperature = $+25^oC$



HOLD STEP ERROR vs. TEMPERATURE
V_{IH} = 4V, C_H = 470pF

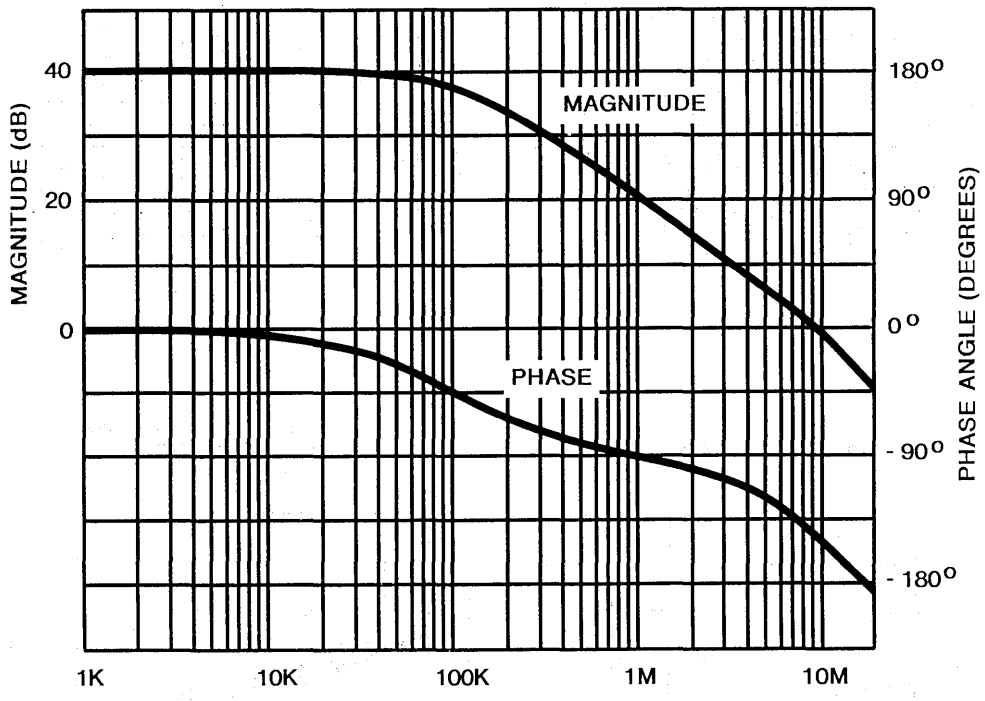


HOLD STEP ERROR vs. TEMPERATURE
V_{IH} = 4V, C_H = Internal
t_r=5ns, 10ns, 20ns



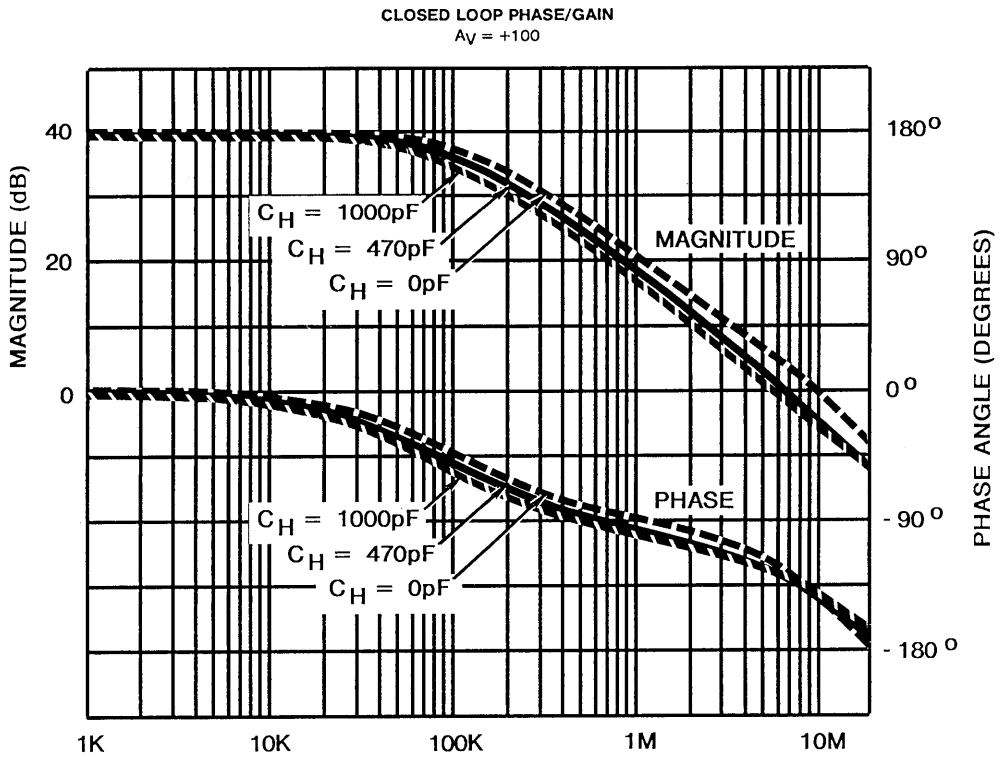
Performance Curves **(Continued)** $V_S = \pm 15V$, $T_A = +25^oC$, unless otherwise specified.

CLOSED LOOP PHASE/GAIN
$A_V = +100$, ±15V and ±12V Supplies*



* ±15V and ±12V supplies trace the same line within the width of the line, therefore only one line is shown.

Performance Curves (Continued) $V_S = \pm15V$, $T_A = +25^oC$, unless otherwise specified.



Die Characteristics

Transistor Count 196
Die Size ..... 139 x 84 x 19 mils
Thermal Impedance:
θ_{ja} ..... $75^oC/W$
θ_{jc} ..... $15^oC/W$
Tie Substrate to: ..... -V
Process ..... Bipolar-DI

LINEAR 6

DIFFERENTIAL AMPLIFIERS

		PAGE
SELECTION GUIDE		6-2
DIFFERENTIAL AMPLIFIERS DATA SHEETS		
CA 3002	IF Amplifier	6-3
CA 3028A, B	Differential/Cascode Amplifier	6-9
CA 3049	Dual High-Frequency Differential Amplifier	6-20
CA 3053	Differential/Cascode Amplifier	6-9
CA 3054	Transistor Array-Dual Differential Amplifier	6-25
CA 3102	Dual High-Frequency Differential Amplifier	6-20

Selection Guide

DIFFERENTIAL AMPLIFIERS

Type	Description	Features	Freq. Range DC to MHz	A (typ.) dB	BW (3dB Point) (typ.) MHz	I/F, NF (typ.) dB	AGC Range (typ.) dB	Pkg. No. of Pins*
CA3002	IF Amplifier	• Balanced differential-amplifier configuration with controlled constant-current source • RF, if, and video frequency capability • Balanced agc capability • Operation from dc to 500MHz • CA3028B is controlled for input offset voltage, current, and input bias current, and is intended for "balance" requirements • Push-pull inputs and outputs • CA3028 and CA3053 are identical except for 100MHz noise specification	20	24	11■	4	-	10T
CA3028A	Differential /Cascode Amplifiers		120	40□	-	7.2	62	8C, S, T
CA3028B			120	40	8	7.2	62	
CA3049	Dual High Frequency		500	22	1.35▲	53	75	12T
CA3053	Differential /Cascode Amplifier		120	40	Recommended for IF Amplifier Applications			8E, S, T
CA3054	Dual Independent		120	32	550†	3.25	75	14E
CA3102	Dual High-Frequency		500	22	1.35▲	1.5	7.5	14E

*See Packaging Section °Min ■RMS ▲GHz °Transistor Array †f_T (MHz) □G_P Min. at 100MHz Cascode. 16dB. Diff Ampl. 14dB

V_{OUT} (p-p V): CA3002, 5.5; CA3028B, 11.5; CA3040, 05. (RMS). T_A Range: -55 to +125°C except for types CA3051, CA3054 (-40 to +85°C)

May 1990

IF Amplifier

For Use in Communication Equipment

Features:

- *Input resistance - 100 kΩ typ.*
- *Output resistance - 70Ωtyp.*
- *Voltage gain - 24 dB typ. @ 1.75 MHz*
- *Push-pull input, single-ended output*
- *-3 dB bandwidth - 11 MHz typ.*
- *AGC range - 80 dB typ.*
- *Useful frequency range DC to 15 MHz*

Applications:

- *Product detector*
- *IF & video amplifier*
- *AM detector*
- *Schmitt trigger*

The CA3002 integrated-circuit IF amplifier is a balanced differential amplifier that can be used with either a single-ended or a push-pull input and can provide either a direct-coupled or a capacitance-coupled single-ended output. Its applications include RC-coupled IF amplifiers that use the internal silicon output-coupling capacitor, video amplifiers that use an external coupling capacitor, envelope detectors, product detectors, and various trigger circuits.

The CA3002 is supplied in the 10-lead hermetic TO-5 style package.

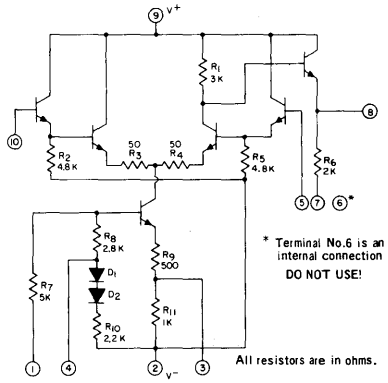


Figure 1 - Schematic diagram.

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, *at* $T_A = 25°C$

COMMON-MODE INPUT SIGNAL VOLTAGE . . . . . ±2 V
MAXIMUM POWER SUPPLY VOLTAGE . . . . . 16 V or ±8 V
OPERATING-TEMPERATURE RANGE . . . . . −55°C to +125°C
STORAGE-TEMPERATURE RANGE . . . . . −65°C to +150°C
LEAD TEMPERATURE (During Soldering):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . . +265°C
MAXIMUM INPUT-SIGNAL VOLTAGE . . . . . ±4 V
MAXIMUM DEVICE DISSIPATION:
−55 to 85°C . . . . . 450 mW
Above 85°C . . . . . Derate linearly 5 mW/°C

ELECTRICAL CHARACTERISTICS, at $T_A = 25°C$, $V_{CC} = +6$ V, $V_{EE} = -6$ V

CHARACTERISTICS	SPECIAL TEST CONDITIONS TERMINALS No. 3 & No.4 NOT CONNECTED UNLESS OTHERWISE NOTED	TEST CIRCUITS	LIMITS CA3002			UNITS
		Fig.	Min.	Typ.	Max.	
STATIC CHARACTERISTICS						
Input Unbalance Voltage V_{IU}		4	–	2.2	–	mV
Input Unbalance Current I_{IU}		5	–	2.2	10	μA
Input Bias Current I_I		5	–	20	36	μA
Quiescent Operating Voltage	MODE: A; TERMINAL 2: V_{EE}; TERMINAL 4: NC	7a	–	2.8	–	V
	MODE: B; TERMINAL 2: V_{EE}; TERMINAL 4: V_{EE}	8b	–	3.9	–	V
Device Dissipation P_T		4	–	55	–	mW
DYNAMIC CHARACTERISTICS						
Differential Voltage Gain A_{DIF} (Single-Ended Input and Output)	f = 1.75 MHz	10	19	24	–	dB
Bandwith at −3 dB Point BW	–	10	–	11	–	MHz
Maximum Output Voltage Swing $V_{OUT(P-P)}$	–	10	–	5.5	–	V_{P-P}
Noise Figure NF	f = 1.75 MHz R_S = 1 kΩ	12	–	4	8	dB
Input Impedance Components: Parallel Input Resistance R_{IN}	f = 1.75 MHz	None	–	100k	–	Ω
Parallel Input Capacitance C_{IN}	f = 1.75 MHz	None	–	4	–	pF
Output Resistance R_{OUT}	f = 1.75 MHz	14	–	70	–	Ω
3rd Harmonic Intermodulation Distortion IMD	–	16	−30	−40	–	dB
AGC Range (Maximum Voltage Gain to Complete Cutoff AGC	f = 1.75 MHz	18	60	80	–	dB

ABSOLUTE-MAXIMUM VOLTAGE AND CURRENT LIMITS, at $T_A = 25°C$

Indicated voltage or current limits for each terminal can be applied under the specified operating conditions for other terminals.

All voltages are with respect to ground ($-V_{CC}$, $+V_{EE}$,) or common terminal of Positive and Negative DC supplies).

TERMINAL	VOLTAGE OR CURRENT LIMITS		CONDITIONS	
	NEGATIVE	POSITIVE	TERMINAL	VOLTAGE
1	−8 V	0 V	2, 7 5, 10 9	−8 0 +6
2	−10 V	0 V	1, 5, 10 9	0 +6
3	−8.5 V	0 V	1, 5, 10 7 9	0 −6 +6
4	−8 V	0 V	1, 5, 10 2, 7 9	0 −8 +6
5	−3.5 V	+3.5 V	1, 10 2, 7 9	0 −6 +6
6	INTERNAL CONNECTION DO NOT USE			
7	−12 V	0 V	1, 5, 10 2 9	0 −6 +6
8	20 mA		1, 5, 10 2 9 200 Ω Resistor Between Terminals 7 & 8	0 −6 +6
9	0 V	+10 V	1, 5, 10 2, 3, 7	0 −6
10	−3.5 V	+3.5 V	1, 5 2, 7 9	0 −6 +6
CASE	INTERNALLY CONNECTED TO TERMINAL No.2 (SUBSTRATE) DO NOT GROUND			

STATIC CHARACTERISTICS

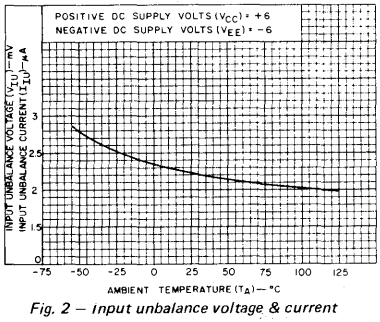


Fig. 2 – Input unbalance voltage & current vs temperature.

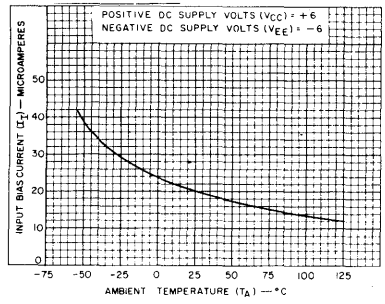


Fig. 3 – Input bias current vs temperature.

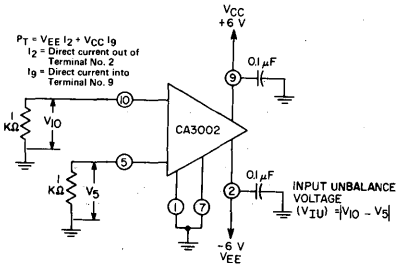


Fig. 4 – Input unbalance voltage and device dissipation test circuit.

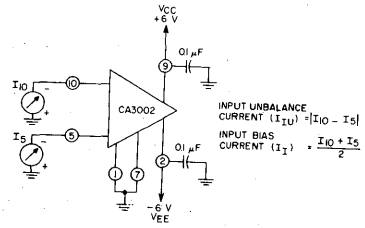


Fig. 5 – Input unbalance current & bias current test circuit.

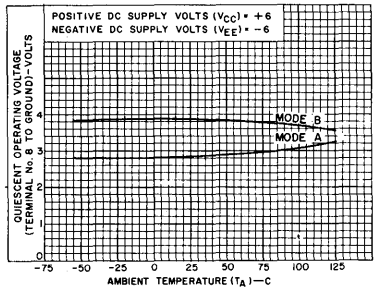


Fig. 6 – Quiescent operating voltage vs temperature.

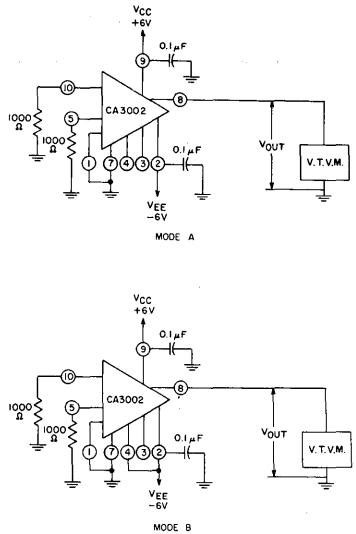


Fig. 7 – Quiescent operating voltage.

DYNAMIC CHARACTERISTICS

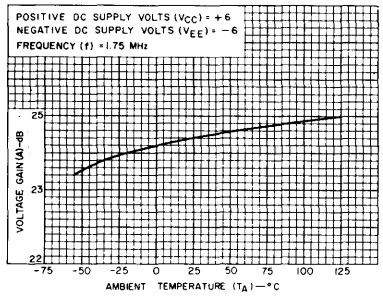


Fig. 8a – Differential voltage gain vs temperature.

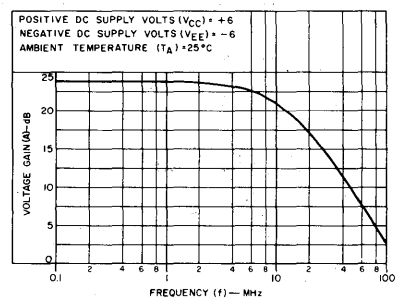


Fig. 8b – Differential voltage gain vs frequency.

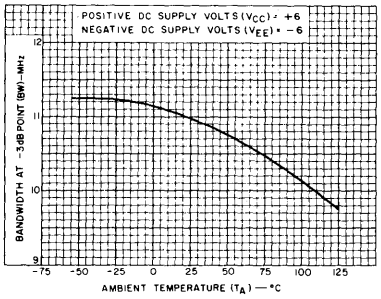


Fig. 9 – Bandwidth of −3 dB point vs temperature.

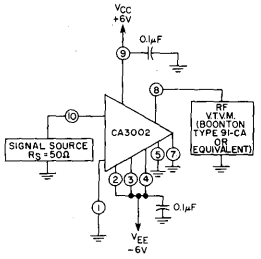


Fig. 10 – Differential voltage gain, −3 dB bandwidth, and maximum output voltage swing.

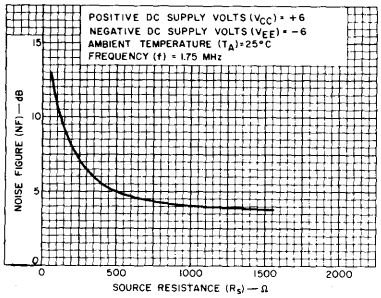
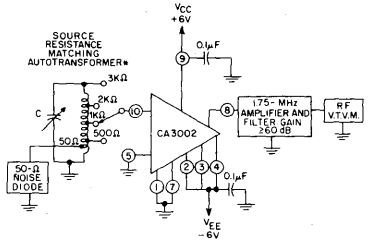


Fig. 11 – Noise figure vs source resistance.



*Taps are adjusted to provide indicated equivalent values of R_S with tank tuned to resonance at 1.75 MHz, and a 50-Ω resistor connected to simulate the noise diode.

Fig. 12 – Noise figure.

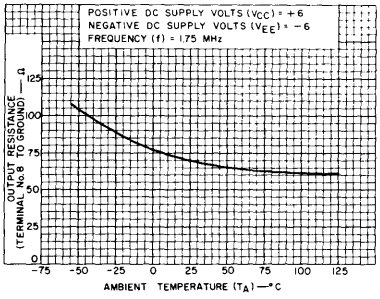


Fig. 13a – Output resistance vs temperature.

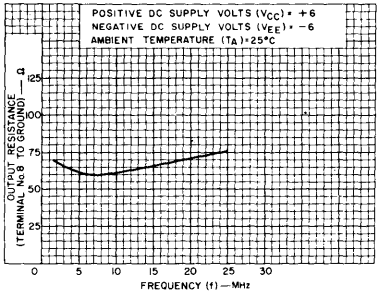


Fig. 13b – Output resistance vs frequency.

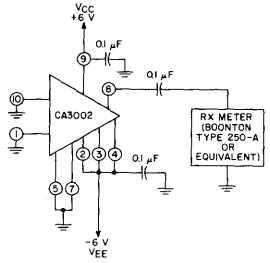


Fig. 14 – Output resistance.

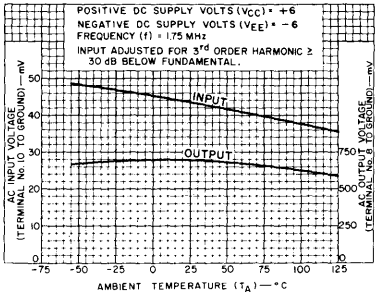
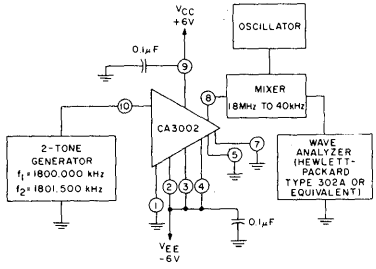


Fig. 15 – Input level for −30 dB intermodulation vs temperature.



1) Increase both input-signal tones until the $2f_2$-f1 and $2f_1$-f2 output-signal voltages are 30 dB below the f_1 and f_2 output-signal voltages.
2) Measure rms values of the input and output signal voltages.
3) The measured input signal voltage is that value when the 3rd-harmonic intermodulation products are 30 dB below the fundamental outputs.

Fig. 16 – Intermodulation circuit.

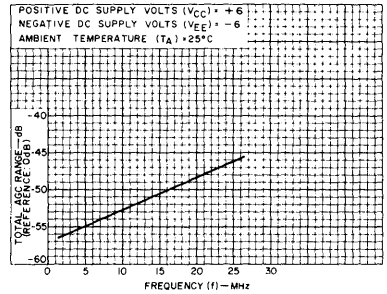
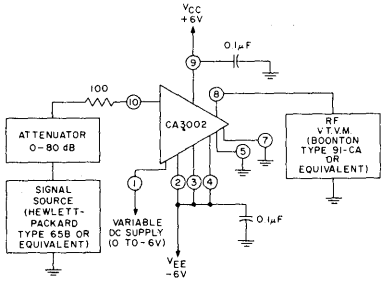


Fig. 17 – AGC range vs frequency.



1) Set attenuator at 80 dB attenuation.
2) Set variable dc supply voltage at 0 V.
3) Increase signal input voltage until RF V.T.V.M. indicates 5 mV output.
4) Set variable dc supply voltage at -6 V.
5) Adjust attenuator until RF V.T.V.M. again indicates 5 mV output.
6) Change in attenuator setting in dB is total AGC Range.

Fig. 18 – AGC range.

May 1990

Differential/Cascode Amplifiers

For Communications and Industrial Equipment at Frequencies from DC to 120 MHz

Features:

- *Controlled for input offset voltage, input offset current, and input bias current (CA3028 series only)*
- *Balanced differential amplifier configuration with controlled constant-current source*
- *Single- and dual-ended operation*

Applications:

- *RF and IF amplifiers (differential or cascode)*
- *DC, audio, and sense amplifiers*
- *Converter in the commercial FM band*
- *Oscillator*
- *Mixer*
- *Limiter*
- *Companion Application Note, ICAN 5337 "Application of the CA3028 Integrated Circuit Amplifier in the HF and VHF Ranges." This note covers characteristics of different operating modes, noise performance, mixer, limiter, and amplifier design considerations.*

The CA3028A and CA3028B are differential/cascode amplifiers designed for use in communications and industrial equipment operating at frequencies from dc to 120 MHz.

The CA3028B is like the CA3028A but is capable of premium performance particularly in critical dc and differential amplifier applications requiring tight controls for input offset voltage, input offset current, and input bias current.

The CA3053 is similar to the CA3028A and CA3028B but is recommended for IF amplifier applications.

The CA3028A, CA3028B, and CA3053 are available in 8-lead packages as shown below. When ordering these devices, it is important to add the appropriate suffix letter to the device.

Package/Lead Options

SMALL OUTLINE (150 mil)	STRAIGHT LEAD TO-5	DUAL-IN-LINE FORMED-LEAD TO-5	DUAL-IN-LINE PLASTIC (MINI-DIP)
CA3028AM	CA3028A*	CA3028AS	CA3028AE
CA3028BM	CA3028B*	CA3028BS	CA3028BE
CA3053M	CA3053*	CA3053S	CA3053E

*Most types in a straight-lead TO-5 package carry a "T" suffix. This one does not. Order type number as shown.

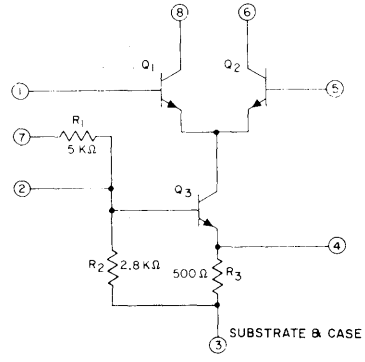


Figure 1 - Schematic diagram for CA3028A, CA3028B and CA3053.

6 DIFFERENTIAL AMPLIFIERS

ABSOLUTE MAXIMUM RATINGS at T_A = 25°C

DISSIPATION:
- At T_A Up to 85°C (CA3028A, CA3028B, CA3053) ..... 450 mW
- At T_A 85°C (CA3028A, CA3028B, CA3053) ..... Derate linearly 5 mW/°C

AMBIENT-TEMPERATURE RANGE:
- Operating ..... -55°C to +125°C
- Storage ..... -65°C to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

MAXIMUM VOLTAGE RATINGS at T_A = 25°C

TERMINAL No.	1	2	3	4	5	6	7	8
1		0 to -15▲	0 to -15▲	0 to -15▲	+5 to -5	*	*	+20⊕ to 0
2			+5 to -11	+5 to -1	+15ϕ to 0	*	+15ϕ to 0	*
3‡				+10 to 0	+15ϕ to 0	+30● to 0	+15ϕ to 0	+30● to 0
4					+15ϕ to 0	*	*	*
5						+20⊕ to 0	*	*
6							*	*
7								*
8								

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of the horizontal terminal 4 with respect to terminal 2 is −1 to +5 volts.

‡ Terminal #3 is connected to the substrate and case.

* Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe, if the specified voltage limits between all other terminals are not exceeded.

▲ Limit is −12V for CA3053.

⊕ Limit is +15V for CA3053.

ϕ Limit is +12V for CA3053.

● Limit is +24V for CA3028A and +18V for CA3053.

MAXIMUM CURRENT RATINGS

TERMINAL No.	I_{IN} mA	I_{OUT} mA
1	0.6	0.1
2	4	0.1
3	0.1	23
4	20	0.1
5	0.6	0.1
6	20	0.1
7	4	0.1
8	20	0.1

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	SYMBOL	TEST CIRCUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A			LIMITS TYPE CA3028B			LIMITS TYPE CA3053			UNITS	TYPICAL CHARACTERISTICS CURVES Fig.
					Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
STATIC CHARACTERISTICS															
			$+V_{CC}$	$-V_{EE}$											
Input Offset Voltage	V_{IO}	2	6V 12V	6V 12V	- -	- -	- -	- -	0.98 0.89	5 5	- -	- -	- -	mV	4
Input Offset Current	I_{IO}	3a	6V 12V	6V 12V	- -	- -	- -	- -	0.56 1.06	5 6	- -	- -	- -	μA	4
Input Bias Current	I_I	3a	6V 12V	6V 12V	- -	16.6 36	70 106	- -	16.6 36	40 80	- -	- -	- -	μA	5a
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	29 36	85 125		5b
Quiescent Operating Current	I_6 or I_8	3a	6V 12V	6V 12V	0.8 2	1.25 3.3	2 5	1 2.5	1.25 3.3	1.5 4	- -	- -	- -	mA	6a 7
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	1.2 2.0	2.2 3.3	3.5 5.0		6b
AGC Bias Current (Into Constant-Current Source Terminal No.7)	I_7	8a	12V 12V	V_{AGC} =+9 V_{AGC} = +12	- -	1.28 1.65	- -	- -	1.28 1.65	- -	- -	- -	- -	mA	8b
		-	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	1.15 1.55	- -		-
Input Current (Terminal No.7)	I_7	-	6V 12V	6V 12V	0.5 1	0.85 1.65	1 2.1	0.5 1	0.85 1.65	1 2.1	- -	- -	- -	mA	-
Device Dissipation	P_T	3a	6V 12V	6V 12V	24 120	36 175	54 260	24 120	36 175	42 220	- -	- -	- -	mW	9
		3b	9V 12V	- -	- -	- -	- -	- -	- -	- -	- -	50 100	80 150		-

ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT Fig.	SPECIAL TEST CONDITIONS		LIMITS TYPE CA3028A Min.	Typ.	Max.	LIMITS TYPE CA3028B Min.	Typ.	Max.	LIMITS TYPE CA3053 Min.	Typ.	Max.	UNITS	TYPICAL CHARACTERISTICS CURVE Fig.
DYNAMIC CHARACTERISTICS															
Power Gain	G_P	10a	f = 100 MHz	Cascode	16	20	-	16	20	-	-	-	-	dB	10b
		11a,d	V_{CC} = +9V	Diff.-Ampl.	14	17	-	14	17	-	-	-	-		11b,e
		10a	f = 10.7 MHz	Cascode	35	39	-	35	39	-	35	39	-	dB	10b *
		11a	V_{CC} = +9V	Diff.-Ampl.	28	32	-	28	32	-	28	32	-		11b *
Noise Figure	NF	10a	f = 100 MHz	Cascode	-	7.2	9	-	7.2	9	-	-	-	dB	10c
		11a,d	V_{CC} = +9V	Diff.-Ampl.	-	6.7	9	-	6.7	9	-	-	-		11c,e
Input Admittance	Y_{11}	-	f = 10.7 MHz V_{CC} = +9V	Cascode				-	0.6 + j 1.6	-				mmho	12
		-		Diff.-Ampl.				-	0.5 + j 0.5	-					13
Reverse Transfer Admittance	Y_{12}	-		Cascode				-	0.0003 - j0	-				mmho	14
		-		Diff.-Ampl.				-	0.01 - j0.0002	-					15
Forward Transfer Admittance	Y_{21}	-		Cascode				-	99 - j18	-				mmho	16
		-		Diff.-Ampl.				-	-37 + j0.5	-					17
Output Admittance	Y_{22}	-		Cascode				-	0. + j0.08	-				mmho	18
		-		Diff.-Ampl.				-	0.04 + j0.23	-					19
Power Output (Untuned)	P_o	20a	f = 10.7 MHz	Diff.-Ampl. 50 Ω Input-Output	-	5.7	-	-	5.7	-	-	-	-	μW	20b
AGC Range (Max. Power Gain to Full Cutoff)	AGC	21a	V_{CC} = +9V	Diff.-Ampl.	-	62	-	-	62	-	-	-	-	dB	21b
Voltage Gain at f = 10.7 MHz	A	22a	f = 10.7 MHz	Cascode	-	40	-	-	40	-	-	40	-	dB	22b
		22c	V_{CC} = +0V R_L = 1 kΩ	Diff.-Ampl.	-	30	-	-	30	-	-	30	-		22d
Voltage Gain Differential at f = 1 kHz		23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	35	38	42	-	-	-	dB	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	40	42.5	45	-	-	-		
Max. Peak-to-Peak Output Voltage at f = 1 kHz	$V_{o(P-P)}$	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	7	11.5	-	-	-	-	V_{P-P}	-
			V_{CC} = +12V, V_{EE} = -12V R_L = 1.6 kΩ		-	-	-	15	23	-	-	-	-		
Bandwidth at -3 dB point	BW	23	V_{CC} = +6V, V_{EE} = -6V, R_L = 2 kΩ		-	-	-	-	7.3	-	-	-	-	MHz	-
			V_{CC} = +12V, V_{EE} = -12V, R_L = 1.6 kΩ		-	-	-	-	8	-	-	-	-		
Common-Mode Input-Voltage Range	V_{CMR}	24	V_{CC} = +6V, V_{EE} = -6V V_{CC} = +12V, V_{EE} = -12V		-	-	-	-2.5 -5	(-3.2 - 4.5) (-7 - 9)	4 7	-	-	-	V	-
Common-Mode Rejection Ratio	CMR	24	V_{CC} = +6V, V_{EE} = -6V V_{CC} = +12V, V_{EE} = -12V		-	-	-	60 60	110 90	-	-	-	-	dB	-
Input Impedance at f = 1 kHz	Z_{IN}		V_{CC} = +6V, V_{EE} = -6V V_{CC} = +12V, V_{EE} = -12V		-	-	-	-	5.5 3	-	-	-	-	kΩ	-
Peak-to-Peak Output Current	I_{P-P}		V_{CC} = +9V V_{CC} = +12V	f = 10.7 MHz e_{in} = 400 mV Diff.-Ampl.	2 3.5	4 6	7 10	2.5 4.5	4 6	6 8	2 3.5	4 6	7 10	mA	-

* Does not apply to CA3053

DEFINITION OF TERMS

AGC Bias Current

The current drawn by the device from the AGC-voltage source, at maximum AGC voltage.

AGC Range

The total change in voltage gain (from maximum gain to complete cutoff) which may be achieved by application of the specified range of dc voltage to the AGC input terminal of the device.

Common-Mode Rejection Ratio

The ratio of the full differential voltage gain to the common-mode voltage gain.

Device Dissipation

The total power drain of the device with no signal applied and no external load current.

Input Bias Current

The average value (one-half the sum) of the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Current

The difference in the currents at the two input terminals when the quiescent operating voltages at the two output terminals are equal.

Input Offset Voltage

The difference in the dc voltages which must be applied to the input terminals to obtain equal quiescent operating voltages (zero output offset voltage) at the output terminals.

Noise Figure

The ratio of the total noise power of the device and a resistive signal source to the noise power of the signal source alone, the signal source representing a generator of zero impedance in series with the source resistance.

Power Gain

The ratio of the signal power developed at the output of the device to the signal power applied to the input, expressed in dB.

Quiescent Operating Current

The average (dc) value of the current in either output terminal.

Voltage Gain

The ratio of the change in output voltage at either output terminal with respect to ground, to a change in input voltage at either input terminal with respect to ground, with the other input terminal at ac ground.

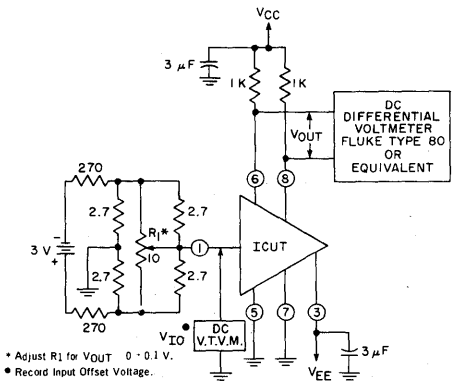


Fig. 2 - Input offset voltage test circuit for CA3028B.

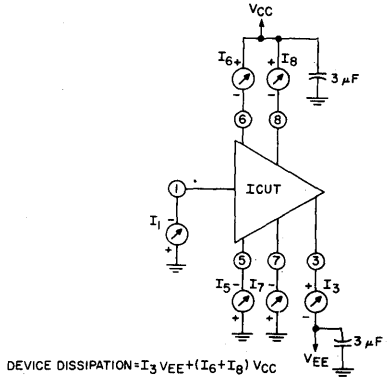


Fig. 3a - Input offset current, input bias current, device dissipation, and quiescent operating current test circuit for CA3028A and CA3028B.

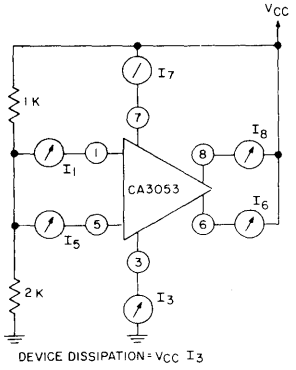


Fig. 3b - Input bias current, device dissipation and quiescent operating current test circuit for CA3053.

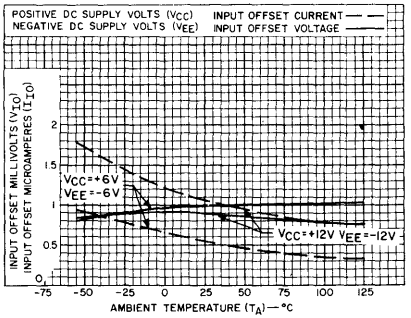


Fig. 4 - Input offset voltage and input offset current for CA3028B.

TYPICAL CHARACTERISTICS

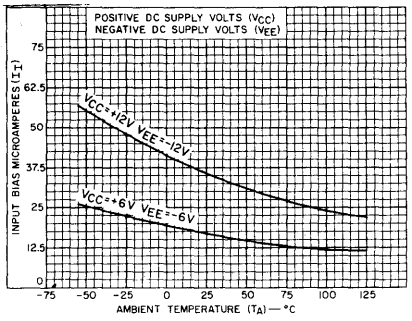


Fig. 5a - Input bias current vs. ambient temperature for CA3028A and CA3028B.

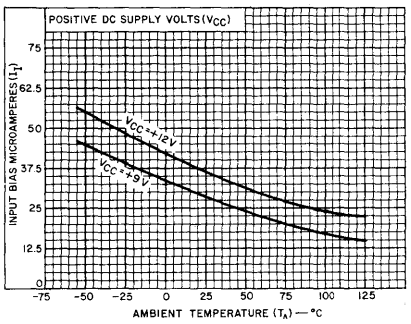


Fig. 5b - Input bias current vs. ambient temperature for CA3053.

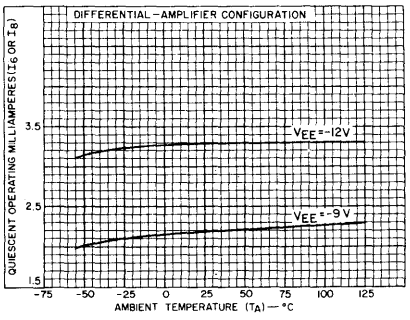


Fig. 6a - Quiescent operating current vs. ambient temperature for CA3028A and CA3028B.

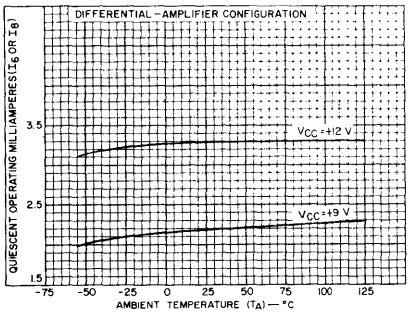


Fig. 6b - Quiescent operating current vs. ambient temperature for CA3053.

TYPICAL CHARACTERISTICS (Continued)

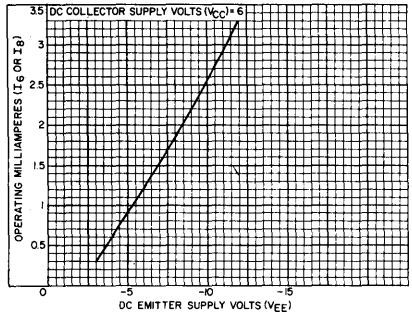


Fig. 7 - Operating current vs. V_{EE} voltage for CA3028A and CA3028B.

TYPICAL CHARACTERISTICS AND TEST CIRCUITS

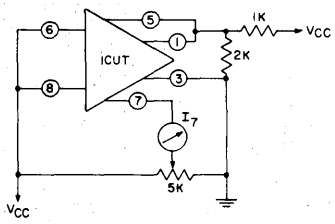


Fig. 8a - AGC bias current test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

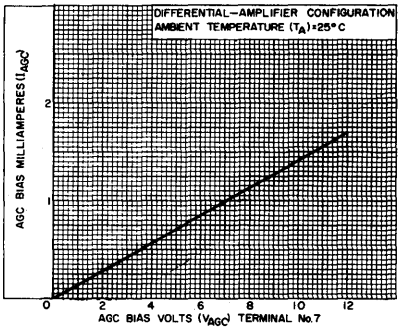


Fig. 8b - AGC bias current vs. bias volts (terminal No. 7) for CA3028A and CA3028B.

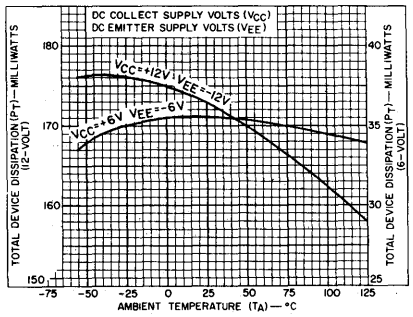
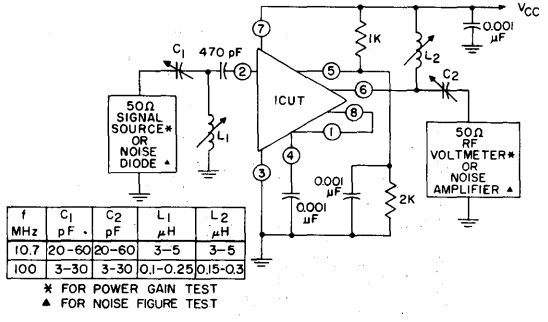


Fig. 9 - Device dissipation vs. temperature for CA3028A and CA3028B.



f MHz	C_1 pF	C_2 pF	L_1 µH	L_2 µH
10.7	20-60	20-60	3-5	3-5
100	3-30	3-30	0.1-0.25	0.15-0.3

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig. 10a - Power gain and noise figure test circuit (cascode configuration) for CA3028A, CA3028B and CA3053.*

** 10.7 MHz Power Gain Test Only.*

TYPICAL CHARACTERISTICS AND TEST CIRCUITS (Continued)

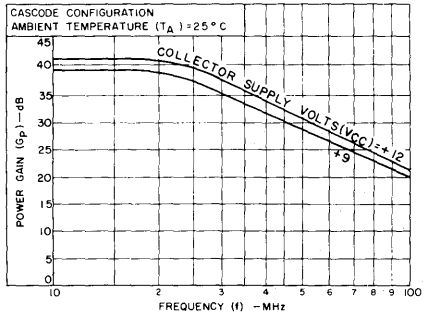


Fig 10b - Power gain vs. frequency (cascode configuration) for CA3028A and CA3028B.

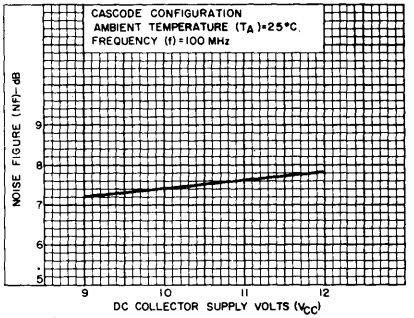
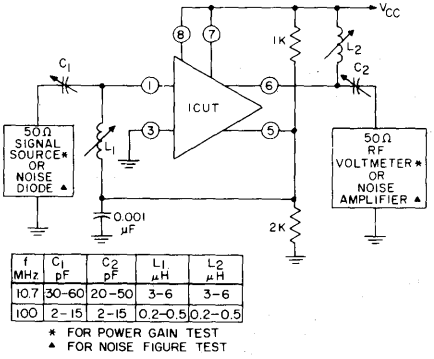


Fig. 10c - 100 MHz noise figure vs. collector supply volts (cascode configuration) for CA3028A and CA3028B.

TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS



f MHz	C_1 pF	C_2 pF	L_1 μH	L_2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig 11a - Power gain and noise figure test circuit (differential-amplifier configuration and terminal No. 7 connected to V_{CC}) for CA3028A, CA3028B and CA3053*

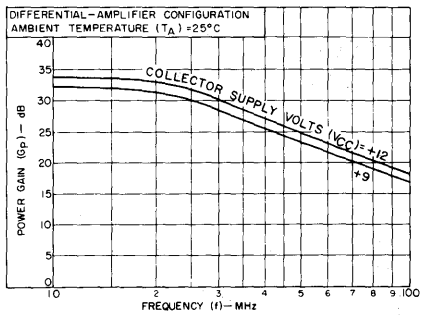


Fig. 11b - Power gain vs. frequency (differential-amplifier configuration) for CA3028A and CA3028B.

* 10.7 MHz Power Gain Test Only.

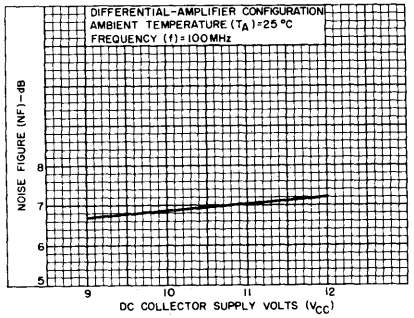
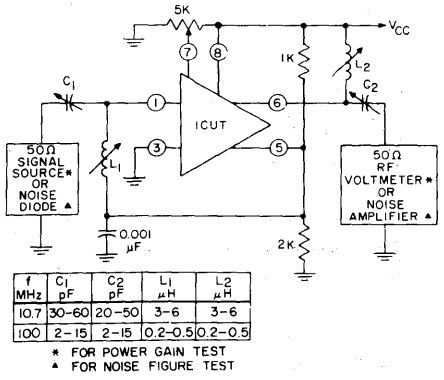


Fig. 11c - 100 MHz noise figure vs. collector supply voltage (differential-amplifier configuration) for CA3028A and CA3028B.



f MHz	C_1 pF	C_2 pF	L_1 μH	L_2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

* FOR POWER GAIN TEST
▲ FOR NOISE FIGURE TEST

Fig. 11d - Power gain and noise figure test circuit (differential-amplifier configuration) for CA3028A and CA3028B.

TYPICAL NOISE FIGURE AND POWER GAIN TEST CIRCUITS AND CHARACTERISTICS (Continued)

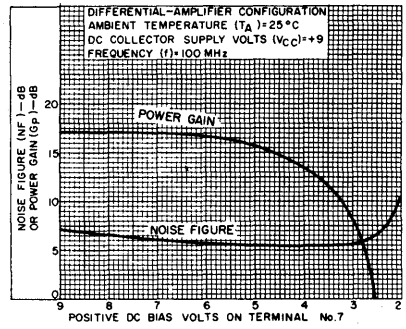


Fig. 11e - 100 MHz noise figure and power gain vs. base-to-emitter bias (terminal No. 7) for CA3028A and CA3028B.

TYPICAL ADMITTANCE PARAMETERS

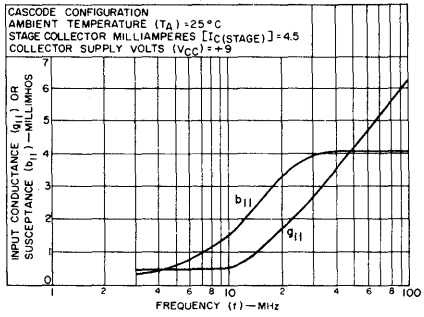


Fig. 12 - Input admittance (Y_{11}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

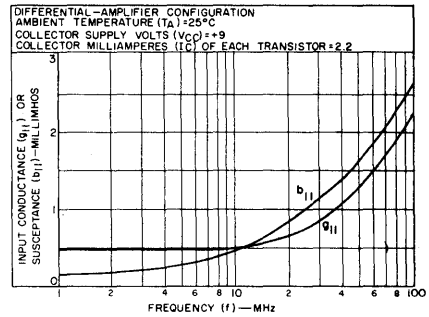


Fig. 13 - Input admittance (Y_{11}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

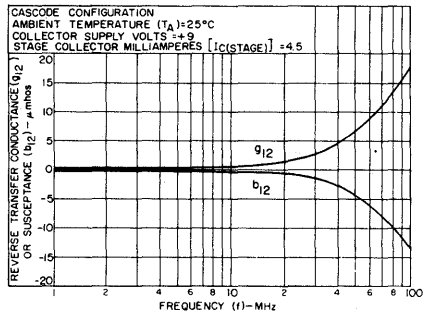


Fig. 14 - Reverse transadmittance (Y_{12}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

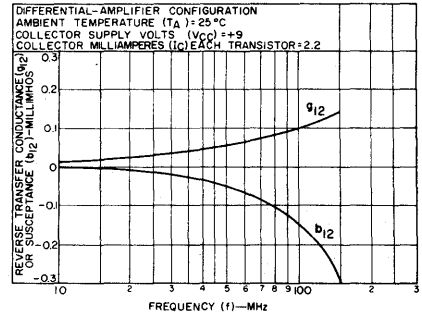


Fig 15 - Reverse transadmittance (Y_{12}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

TYPICAL ADMITTANCE PARAMETERS (Continued)

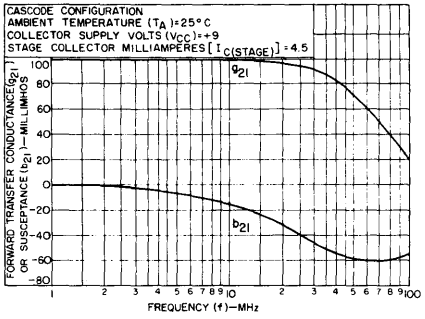


Fig. 16 - Forward transadmittance (Y_{21}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

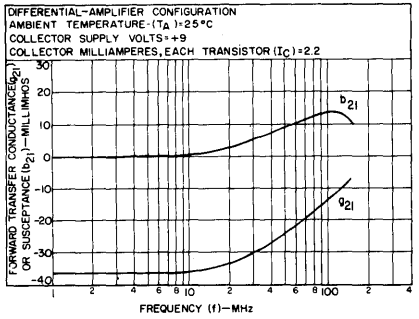


Fig. 17 - Forward transadmittance (Y_{21}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

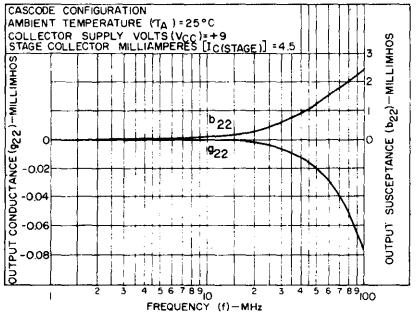


Fig. 18 - Output admittance (Y_{22}) vs. frequency (cascode configuration) for CA3028A, CA3028B and CA3053.

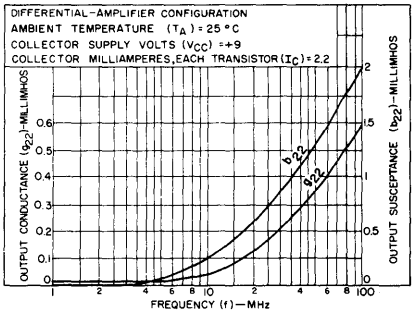


Fig. 19 - Output admittance (Y_{22}) vs. frequency (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

TYPICAL TEST CIRCUITS AND CHARACTERISTICS

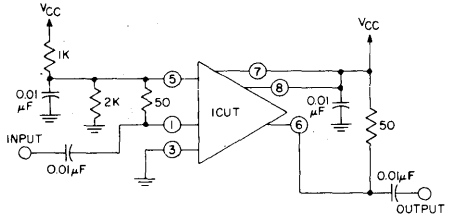


Fig. 20a - Output power test circuit for CA3028A and CA3028B.

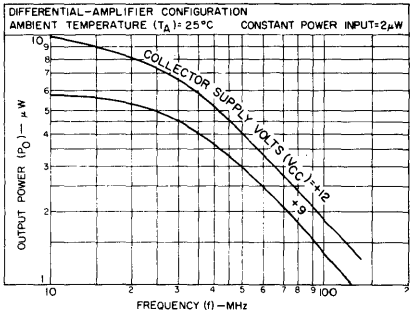
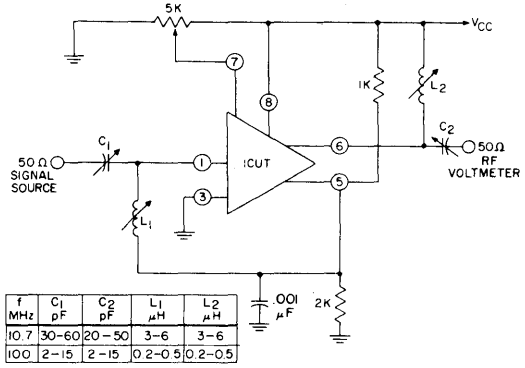


Fig. 20b - Output power vs. frequency - 50 Ω input and 50 Ω output (differential-amplifier configuration) for CA3028A and CA3028B.

TYPICAL TEST CIRCUITS AND CHARACTERISTICS (Continued)



f MHz	C_1 pF	C_2 pF	L_1 μH	L_2 μH
10.7	30-60	20-50	3-6	3-6
100	2-15	2-15	0.2-0.5	0.2-0.5

Fig. 21a - AGC range test circuit (differential amplifier) for CA3028A and CA3028B.

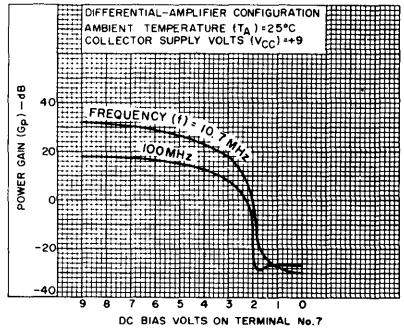


Fig. 21b - AGC characteristics for CA3028A and CA3028B.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS

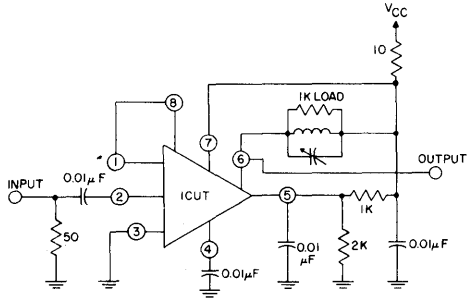


Fig. 22a - Transfer characteristic (voltage gain) test circuit (10.7 MHz) cascode configuration for CA3028A, CA3028B and CA3053.

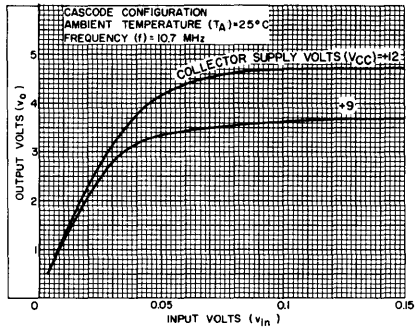


Fig. 22b - Transfer characteristics (cascode configuration) for CA3028A, CA3028B and CA3053.

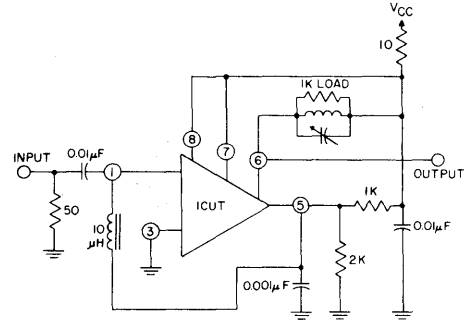


Fig. 22c - Transfer characteristic (voltage gain) test circuit (10.7 MHz) differential-amplifier configuration for CA3028A, CA3028B and CA3053.

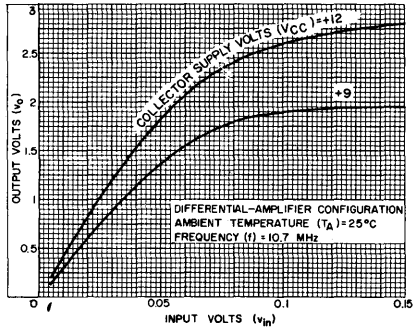
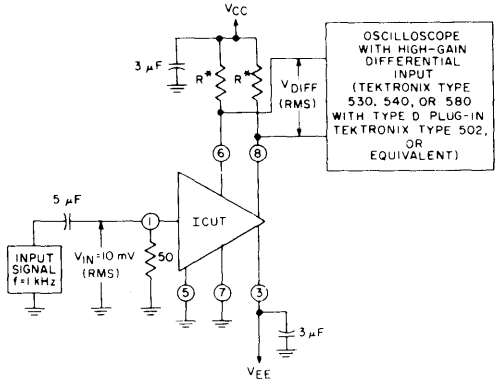


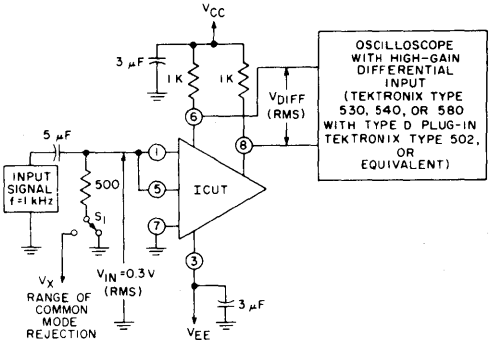
Fig 22d - Transfer characteristics (differential-amplifier configuration) for CA3028A, CA3028B and CA3053.

TEST CIRCUITS AND TYPICAL CHARACTERISTICS (Continued)



* For R = 1.6 kΩ – (V_{CC} = 12V, V_{EE} = -12V)
For R = 2 kΩ – (V_{CC} = 6 V, V_{EE} = -6V)

Fig. 23 - Differential voltage gain, maximum peak-to-peak output voltage, and bandwidth test circuit for CA3028B.



For CMR test: S_1 to ground
For input common-mode voltage range test: S_1 to V_X

Common mode rejection ratio = $20 \log_{10} \frac{(A^*)(2)(0.3)}{V_{DIFF}(RMS)}$

* A = Single-ended voltage gain.

Fig. 24 - Common-mode rejection ratio and common-mode input-voltage range test circuit for CA3028B.

May 1990

Dual High-Frequency Differential Amplifiers

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- *Power Gain 23 dB (typ.) at 200 MHz*
- *Noise Figure 4.6 dB (typ.) at 200 MHz*
- *Two differential amplifiers on a common substrate*
- *Independently accessible inputs and outputs*
- *Full military-temperature-range capability- (-55°C to +125°C) for the CA3102E and for the CA3049T*

Applications:

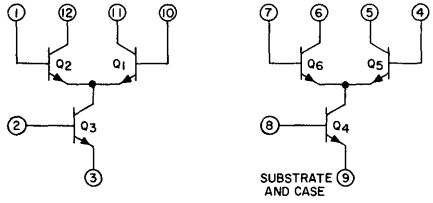
- *VHF amplifiers*
- *VHF mixers*
- *Multifunction combinations - RF/Mixer/Oscillator; Converter/IF*
- *IF amplifiers (differential and/or cascode)*
- *Product detectors*
- *Doubly balanced modulators and demodulators*
- *Balanced quadrature detectors*
- *Cascade limiters*
- *Synchronous detectors*
- *Balanced mixers*
- *Synthesizers*
- *Balanced (push-pull) cascode amplifiers*
- *Sense amplifiers*

The CA3049T and CA3102E* consist of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six transistors which comprise the amplifiers are general-purpose devices which exhibit low I/f noise and a value of f_T in excess of 1 GHz. These features make the CA3049T and CA3102E useful from dc to 500 MHz. Bias and load registers have been omitted to provide maximum application flexibility.

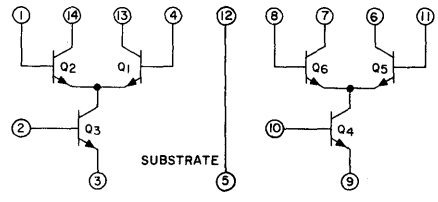
The monolithic construction of the CA3049T and CA3102E provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3102E is like the CA3049T except that it has a separate substrate connection for greater design flexibility. The CA3049T is supplied in the 12-lead TO-5 package; the CA3102E, in the 14-lead plastic dual-in-line package (E suffix) and in the 14-lead Small Outline package (M suffix).

*Formerly Developmental No. TA6228.



Schematic Diagram for CA3049T.



Schematic Diagram for CA3102E.

MAXIMUM RATINGS, *ABSOLUTE-MAXIMUM VALUES, AT T_A = 25°C*

	CA3049T	CA3102E	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	600	750	mW
For $T_A > 55°C$ Derate at:	5	6.67	mW/°C
Temperature Range:			
Operating	−55 to + 125	−55 to + 125	°C
Storage	−65 to + 150	−65 to + 150	°C

The following ratings apply for each transistor in the devices

Collector-to-Emitter Voltage, V_{CEO}	15	V
Collector-to-Base Voltage, V_{CBO}	20	V
Collector-to-Substrate Voltage, V_{CIO}*	20	V
Emitter-to-Base Voltage, V_{EBO}	5	V
Collector Current, I_C	50	mA

*The collector of each transistor of the CA3049T and CA3102E is isolated from the substrate by an integral diode. The substrate (terminal 9) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		TEST CIR-CUIT	CA3102E LIMITS			CA3049T LIMITS				TYPICAL CHARAC-TERISTICS CURVES
				FIG.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS	FIG.
STATIC CHARACTERISTICS												
For Each Differential Amplifier												
Input Offset Voltage	V_{IO}			1	---	0.25	5	---	0.25	---	mV	4
Input Offset Current	I_{IO}	$I_3 = I_9$ = 2 mA		1	---	0.3	3	---	0.3	---	μA	---
Input Bias Current	I_{IB}			1	---	13.5	33		13.5	33	μA	5
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$			1	---	1.1	---	---	1.1	---	μV/°C	4
For Each Transistor												
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CE} = 6 V, I_C = 1 mA		---	674	774	874	---	774	---	mV	6
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 6 V, I_C = 1 mA		---	---	-0.9	---	---	-0.9	---	mV/°C	6
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0		---	---	0.0013	100	---	0.0013	100	nA	7
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0		---	15	24	---	15	24	---	V	---
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		---	20	60	---	20	60	---	V	---
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_B = 0, I_E = 0		---	20	60	---	20	60	---	V	---
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0		---	5	7	---	5	7	---	V	---
DYNAMIC CHARACTERISTICS												
1/f Noise Figure (For Single Transistor)	NF	f = 100 KHz, R_S = 500 Ω, I_C = 1 mA		---	---	1.5	---	---	1.5	---	dB	12
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 6 V, I_C = 5 mA		---	---	1.35	---	---	1.35	---	GH_z	11
Collector-Base Capacitance	C_{CB}	I_C = 0	V_{CB} = 5V	*	---	0.28	---	---	0.28	---	pF	8
				**	---	0.15	---	---	0.28	---	pF	
Collector-Substrate Capacitance	C_{CI}	I_C = 0	V_{CI} = 5V		---	1.65	---	---	1.65	---	pF	8
For Each Differential Amplifier												
Common-Mode Rejection Ratio	CMR	$I_3 = I_9$ = 2 mA		---	---	100	---	---	100	---	dB	---
AGC Range, One Stage	AGC	Bias Voltage = -6V		2	---	75	---	---	75	---	dB	---
Voltage Gain, Single-Ended Output	A	Bias Voltage = -4.2V, f = 10 MHz		2	18	22	---	---	22	---	dB	9, 10
Insertion Power Gain	G_p	f = 200 MHz	Cascode	3	---	23	---	---	23	---	dB	---
Noise Figure	NF	V_{CC} = 12V	Cascode	3	---	4.6	---	---	4.6	---	dB	---
Input Admittance	Y_{11}	For Cascode Configuration, $I_3 = I_9$ = 2 mA	Cascode	---	---	1.5 + j 2.45	---	---	1.5 + j 2.45	---	mmho	14, 16, 18
			Diff.Amp.	---	---	0.878 + j 1.3	---	---	0.878 + j 1.3	---		15, 17, 19
Reverse Transfer Admittance	Y_{12}	For Diff. Amplifier Configuration, $I_3 = I_9$ = 4mA (each collector $I_C \simeq$ 2mA)	Cascode	---	---	0 - j 0.008	---	---	0 - j 0.008	---	mmho	---
			Diff.Amp.	---	---	0 - j 0.013	---	---	0 - j 0.013	---		---
Forward Transfer Admittance	Y_{21}		Cascode	---	---	17.9 - j 30.7	---	---	17.9 - j 30.7	---	mmho	26, 28, 30
			Diff. Amp.	---	---	- 10.5 + j 13	---	---	- 10.5 + j 13	---		27, 29, 31
Output Admittance	Y_{22}		Cascode	---	---	- 0.503 - j 15	---	---	- 0.503 - j 15	---	mmho	20, 22, 24
			Diff.Amp.	---	---	0.071 + j 0.62	---	---	0.071 + j 0.62	---		21, 23, 25

*Terminals 1 & 14, or 7 & 8. (CA3102E) 1 & 12 or 6 & 7 (CA3049T)
**Terminals 13 & 4, or 6 & 11. (CA3102E) 10 & 11 or 4 & 5 (CA3049T)

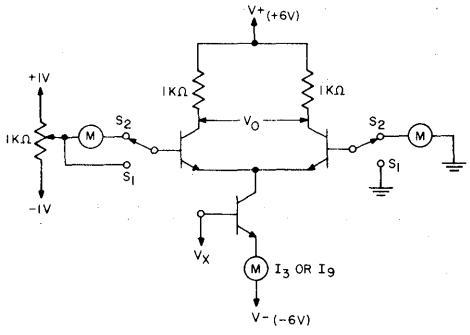


Fig.1—Static characteristics test circuit for CA3102E.

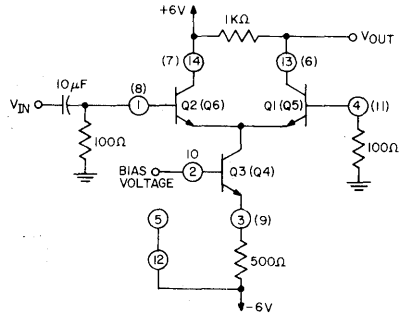
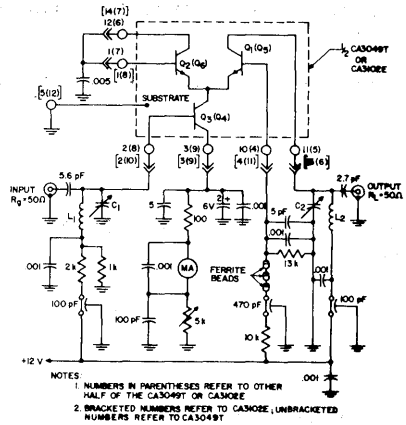


Fig.2—AGC range and voltage gain test circuit for CA3102E.



L_1, L_2 – Approx. 1/2 Turn #18 Tinned Copper Wire, 5/8" Dia.

C_1, C_2 – 15 pF Variable Capacitors (Hammarlund, MAC-15; or Equivalent)

All Capacitors in μF Unless Otherwise Indicated

All Resistors in Ohms Unless Otherwise Indicated

Fig.3—200 MHz cascode power gain and noise figure test circuit.

Typical Characteristics for CA3049T and CA3102E

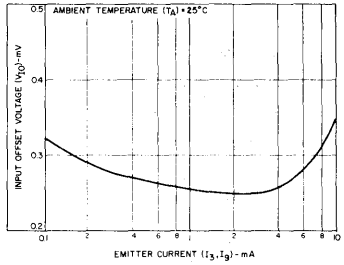


Fig. 4—Input offset voltage vs. emitter current.

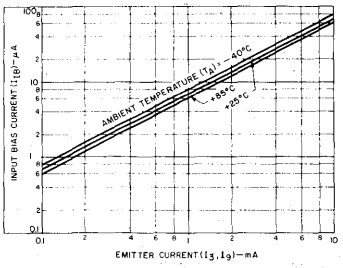


Fig. 5—Input bias current vs. emitter current.

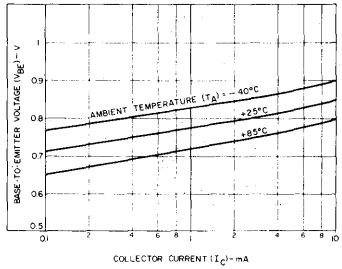


Fig. 6—Base-to-emitter voltage vs. collector current.

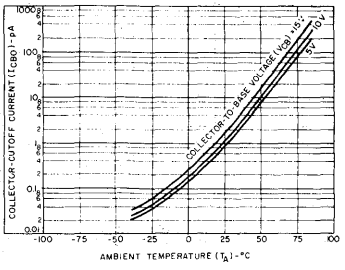


Fig. 7—Collector-cutoff current vs. temperature.

Typical Characteristics for CA3049T and CA3102E (cont'd)

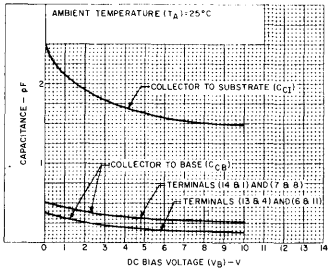


Fig. 8—Capacitance vs. dc bias voltage.

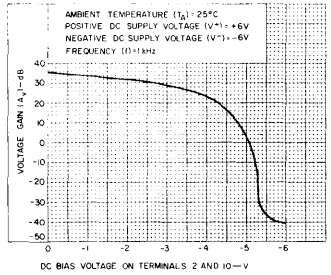


Fig. 9—Voltage gain vs. dc bias voltage.

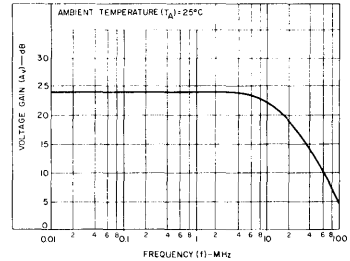


Fig. 10—Voltage gain vs. frequency.

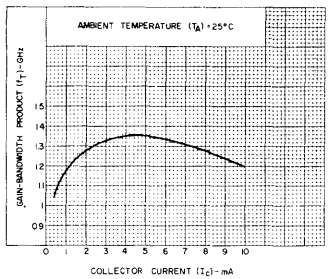


Fig. 11—Gain-bandwidth product vs. collector current.

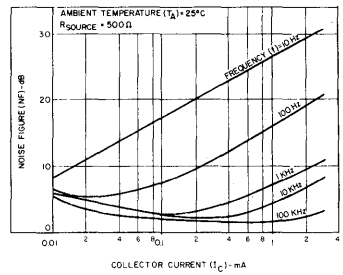


Fig. 12—1/f noise figure vs. collector current.

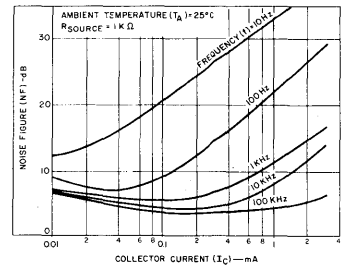


Fig. 13—1/f noise figure vs. collector current.

Typical Input Admittance Characteristics for CA3049T and CA3102

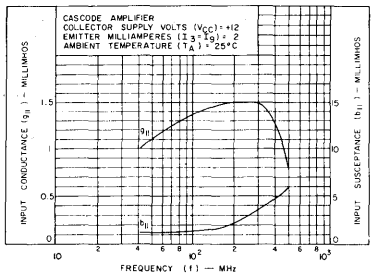


Fig. 14—Input admittance (Y_{11}) vs. frequency.

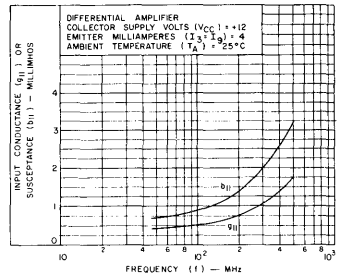


Fig. 15—Input admittance (Y_{11}) vs. frequency.

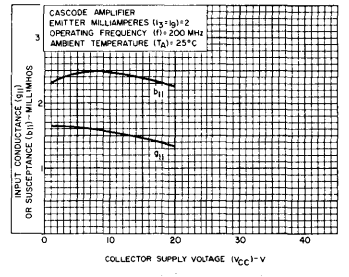


Fig. 16—Input admittance (Y_{11}) vs. collector supply voltage.

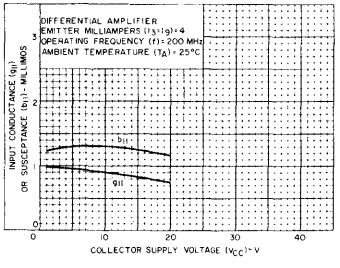


Fig. 17—Input admittance (Y_{11}) vs. collector supply voltage.

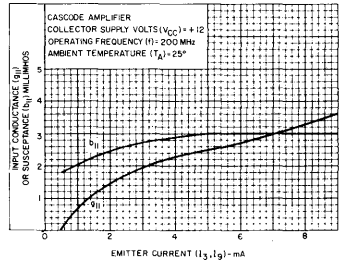


Fig. 18—Input admittance (Y_{11}) vs. emitter current.

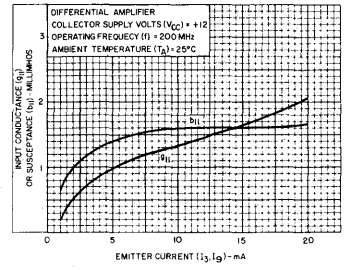


Fig. 19—Input admittance (Y_{11}) vs. emitter current.

Typical Output Admittance Characteristics for CA3049T and CA3102E

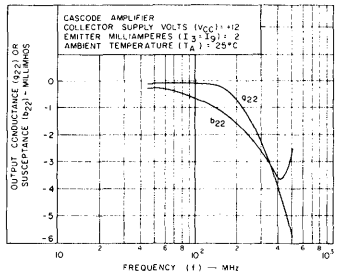


Fig. 20—Output admittance (Y_{22}) vs. frequency.

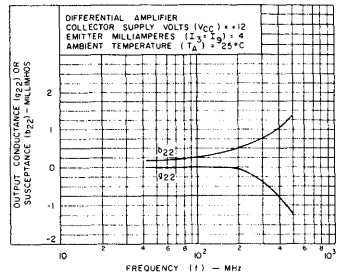


Fig. 21—Output admittance (Y_{22}) vs. frequency.

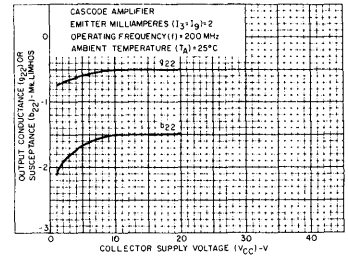


Fig. 22—Output admittance (Y_{22}) vs. collector supply voltage.

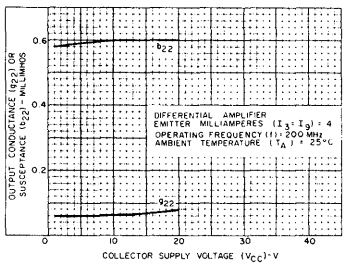


Fig. 23—Output admittance (Y_{22}) vs. collector supply voltage.

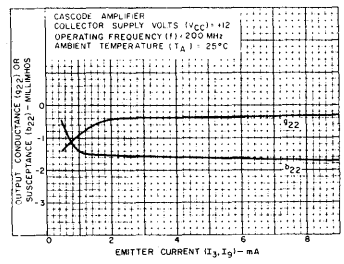


Fig. 24—Output admittance (Y_{22}) vs. emitter current.

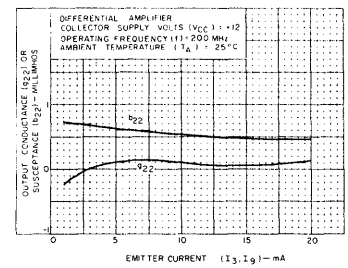


Fig. 25—Output admittance (Y_{22}) vs. emitter current.

Typical Forward Transfer Characteristics for CA3049T and CA3102E

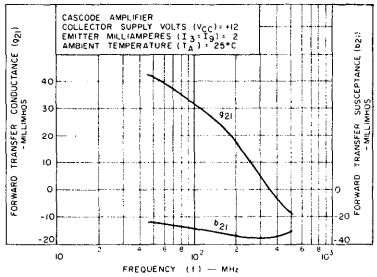


Fig. 26—Forward transfer admittance (Y_{21}) vs. frequency.

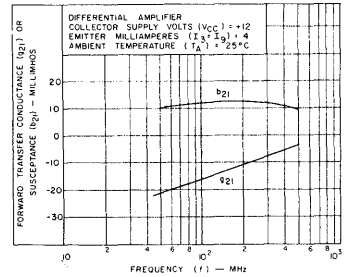


Fig. 27—Forward transfer admittance (Y_{21}) vs. frequency.

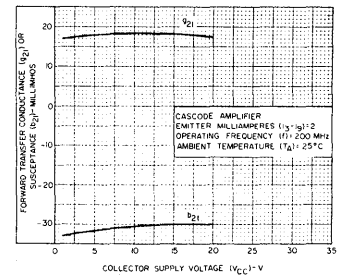


Fig. 28—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

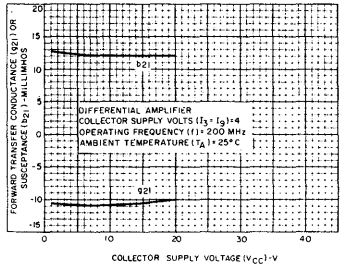


Fig. 29—Forward transfer admittance (Y_{21}) vs. collector supply voltage.

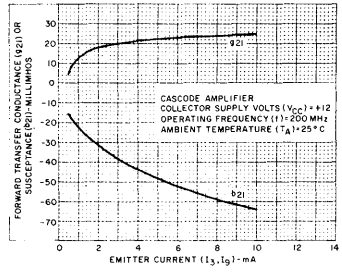


Fig. 30—Forward transfer admittance (Y_{21}) vs. emitter current.

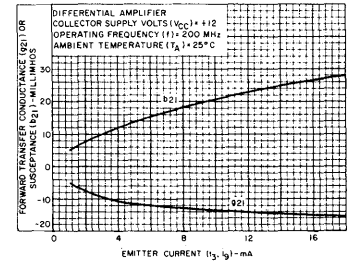


Fig. 31—Forward transfer admittance (Y_{21}) vs. emitter current.

Differential Amplifiers

CA3054

May 1990

Transistor Array - Dual Independent Differential Amplifiers

For Low Power Applications
at Frequencies from DC to 120 MHz

Features:

- *Two differential amplifiers on a common substrate*
- *Independently accessible inputs and outputs*
- *Maximum input offset voltage: ±5 mV*
- *Temperature range: 0°C to +85°C*

Applications:

- *Dual sense amplifiers*
- *Dual Schmitt triggers*
- *Multifunction combinations - RF/Mixer/Oscillator; Converter/IF*
- *IF amplifiers (differential and/or cascode)*
- *Product detectors*
- *Doubly balanced modulators and demodulators*
- *Balanced quadrature detectors*
- *Cascade limiters*
- *Synchronous detectors*
- *Pairs of balanced mixers*
- *Synthesizer mixers*
- *Balanced (push-pull) cascode amplifiers*

The CA3054 consists of two independent differential amplifiers with associated constant-current transistors on a common monolithic substrate. The six n-p-n transistors which comprise the amplifiers are general-purpose devices which exhibit low 1/f noise and a value of f_T in excess of 300 MHz. These features make the CA3054 useful from dc to 120 MHz. Bias and load resistors have been omitted to provide maximum application flexibility.

The monolithic construction of the CA3054 provides close electrical and thermal matching of the amplifiers. This feature makes these devices particularly useful in dual-channel applications where matched performance of the two channels is required.

The CA3054 is supplied in a 14-lead plastic dual-in-line package with a limited temperature range. The availability of extra terminals allows the introduction of an independent substrate connection for maximum flexibility.

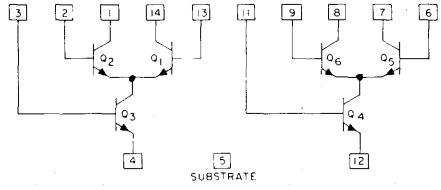


Figure 1 - Schematic Diagram for CA3054.

CAUTION: Substrate MUST be maintained negative with respect to all collector terminals of this device. See Maximum Voltage Ratings chart.

MAXIMUM RATINGS, ABSOLUTE-MAXIMUM VALUES, AT $T_A = 25^oC$

POWER DISSIPATION, P:	CA3054	
Any one transistor	300	mW
Total package	750	mW
For $T_A > 55^oC$	6.67	mW/°C
TEMPERATURE RANGE:		
Operating	-40 to +85	°C
Storage	-65 to +150	°C

The following ratings apply for each transistor in the device:

COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}	15	V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}	20	V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}*	20	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}	5	V
COLLECTOR CURRENT, I_C	50	mA

LEAD TEMPERATURE (During Soldering)

At distance 1/16 ± 1/32 inch (1.59 ±0.79 mm) from case for 10 seconds max. ..... +265°C

*The collector of each transistor of the CA3054 is isolated from the substrate by an integral diode. *The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide for normal transistor action. The substrate should be maintained at signal (AC) ground by means of a suitable grounding capacitor, to avoid undesired coupling between transistors.*

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminals listed vertically with respect to the terminals listed horizontally. For example, the voltage range between vertical terminal 2 and horizontal terminal 4 is +15 to -5 volts.

CA3054 → Terminal No. ↓	13	14	1	2	3	4	6	7	8	9	11	12	5
13		0 -20	*	+5 -5	*	+15 -5	*	*	*	*	*	*	*
14			*	*	*	+20 0	*	*	*	*	*	*	+20 0
1				+20 0	*	+20 0	*	*	*	*	*	*	+20 0
2					*	+15 -5	*	*	*	*	*	*	*
3						+1 -5	*	*	*	*	*	*	*
4							*	*	*	*	*	*	*
6								0 -20	*	+5 -5	*	+15 -5	*
7									*	*	*	*	+20 0
8										+20 0	*	*	+20 0
9											*	+15 -5	*
11												-1 -5	*
12													*
5													Ref Sub- strate

*Voltages are not normally applied between these terminals. Voltages appearing between these terminals will be safe if the specified limits between all other terminals are not exceeded.

Maximum Current Ratings

CA3054 Terminal No.•	I_{IN} mA	I_{OUT} mA
13	5	0.1
14	50	0.1
1	50	0.1
2	5	0.1
3	5	0.1
4	0.1	-50
6	5	0.1
7	50	0.1
8	50	0.1
9	5	0.1
11	5	0.1
12	0.1	50

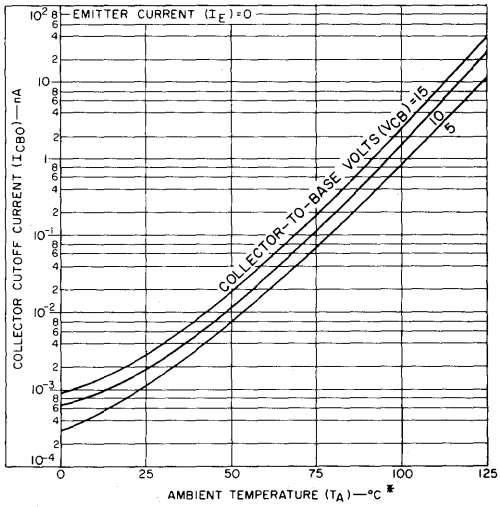
• Terminal No. 10 of CA3054 is not used.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS	TEST CIR-CUIT	CA3054 LIMITS			UNITS	TYPICAL CHARAC-TERISTICS CURVES
			FIG.	MIN.	TYP.	MAX.		FIG.
STATIC CHARACTERISTICS								
For Each Differential Amplifier								
Input Offset Voltage	V_{IO}	V_{CB} = 3 V $I_{E(Q3)} = I_{E(Q4)}$ = 2 mA	-	-	0.45	5	mV	6
Input Offset Current	I_{IO}		-	-	0.3	2	μA	7
Input Bias Current	I_I		-	-	10	24	μA	3
Quiescent Operating Current Ratio	$\frac{I_{C(Q1)}}{I_{C(Q2)}}$ or $\frac{I_{C(Q5)}}{I_{C(Q6)}}$		-	-	0.98 to 1.02	-	-	3
Temperature Coefficient Magnitude of Input-Offset Voltage	$\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		-	-	1.1	-	μV/°C	5
For Each Transistor								
DC Forward Base-to-Emitter Voltage	V_{BE}	V_{CB} = 3 V, I_C = 50 μA	-	-	0.630	0.700	V	6
		I_C = 1 mA	-	-	0.715	0.800		
		I_C = 3 mA	-	-	0.750	0.850		
		I_C = 10 mA	-	-	0.800	0.900		
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CB} = 3 V, I_C = 1 mA	-	-	-1.9	-	μV/°C	4
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	-	0.002	100	nA	2
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	-	15	24	-	V	-
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	-	20	60	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	-	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	-	5	7	-	V	-
DYNAMIC CHARACTERISTICS								
Common-Mode Rejection Ratio For Each Amplifier	CMR	V_{CC} = 12 V V_{EE} = -6 V V_X = -3.3 V f = 1 kHz	8a	-	100	-	dB	8b
AGC Range, One Stage	AGC		9a	-	75	-	dB	9b
Voltage Gain, Single Stage Double-Ended Output	A		9a	-	32	-	dB	9b
AGC Range, Two Stage	AGC		10a	-	105	-	dB	10b
Voltage Gain, Two Stage Double-Ended Output	A		10a	-	60	-	dB	10b
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics: (For Single Transistor)								
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	-	110	-	-	11
Short-Circuit Input Impedance	h_{ie}		-	-	3.5	-	kΩ	11
Open-Circuit Output Impedance	h_{oe}		-	-	15.6	-	μmho	11
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	-	1.8×10^{-4}	-	-	11

DYNAMIC CHARACTERISTICS CONT'D.								
1/f Noise Figure (For Single Transistor)	NF	f = 1 kHz, V_{CE} = 3 V	-	-	3.25	-	dB	-
Gain-Bandwidth Product (For Single Transistor)	f_T	V_{CE} = 3 V, I_C = 3 mA	-	-	550	-	MHz	12
Admittance Characteristics; Differential Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Each Collector $I_C \approx$ 1.25 mA f = 1 MHz	-	-	-20+j0	-	mmho	13a
Input Admittance	y_{11}		-	-	0.22+j0.1	-	mmho	13b
Output Admittance	y_{22}		-	-	0.01+j0	-	mmho	13c
Reverse Transfer Admittance	y_{12}		-	-	-0.003 +j0	-	mmho	13d
Admittance Characteristics; Cascode Circuit Configuration: (For Each Amplifier)								
Forward Transfer Admittance	y_{21}	V_{CB} = 3 V Total Stage $I_C \approx$ 2.5 mA f = 1 MHz	-	-	68-j0	-	mmho	14a
Input Admittance	y_{11}		-	-	0.55+j0	-	mmho	14b
Output Admittance	y_{22}		-	-	0+j0.02	-	mmho	14c
Reverse Transfer Admittance	y_{12}		-	-	0.004-j0.005	-	μmho	14d
Noise Figure	NF	f = 100 MHz	-	-	8	-	dB	-

TYPICAL STATIC CHARACTERISTICS



* For CA3054: use data from 0°C to 85°C only

Fig.2 - Collector-to-base cutoff current vs ambient temperature for each transistor.

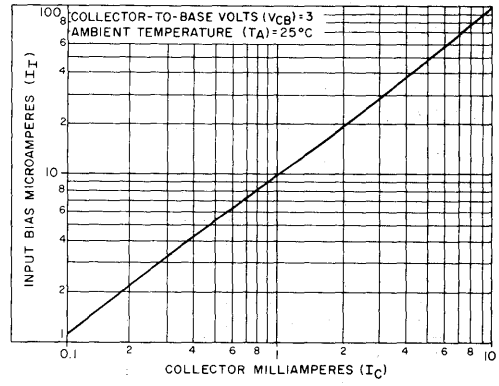


Fig.3 - Input bias current characteristic vs collector current for each transistor.

TYPICAL STATIC CHARACTERISTICS

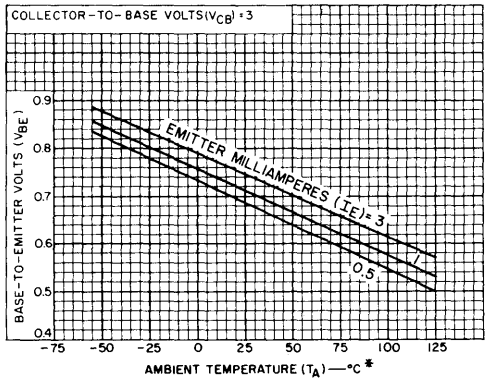


Fig.4 - Base-to-emitter voltage characteristic for each transistor vs ambient temperature.

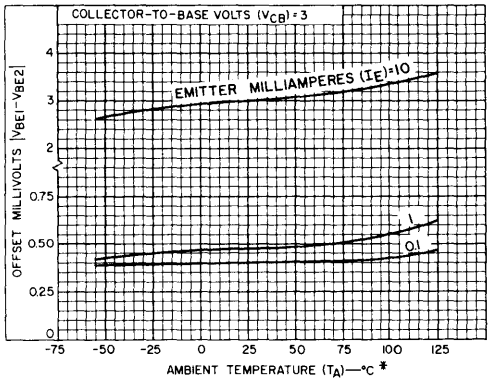


Fig.5 - Offset voltage characteristic vs ambient temperature for differential pairs.

* For CA3054: use data from 0°C to 85°C only

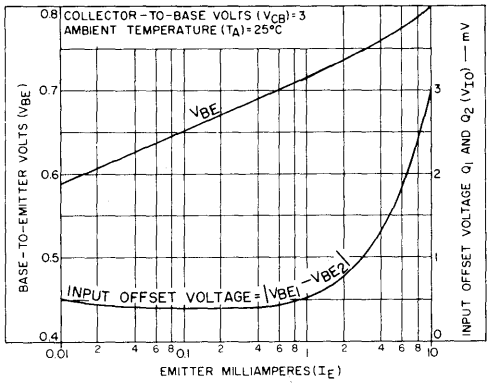


Fig.6 - Static base-to-emitter voltage characteristic and input offset voltage for differential pairs vs emitter current.

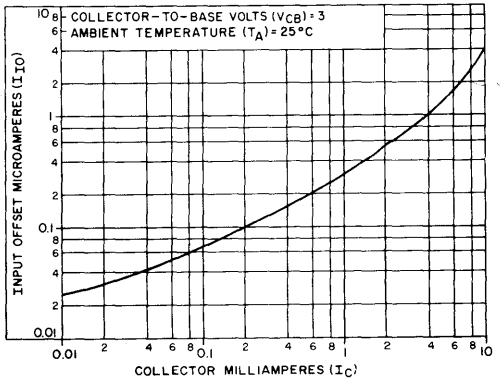


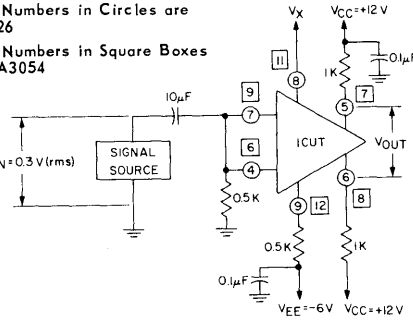
Fig.7 - Input offset current for matched differential pairs vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS

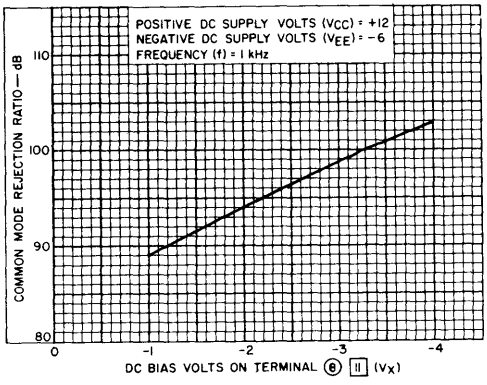
COMMON MODE REJECTION RATIO

Terminal Numbers in Circles are for CA3026

Terminal Numbers in Square Boxes are for CA3054



(a) Test setup

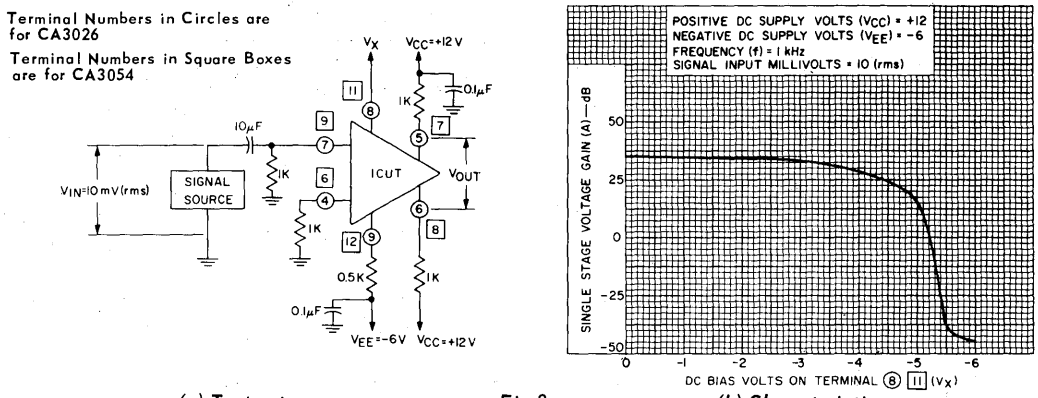


(b) Characteristic

Fig.8

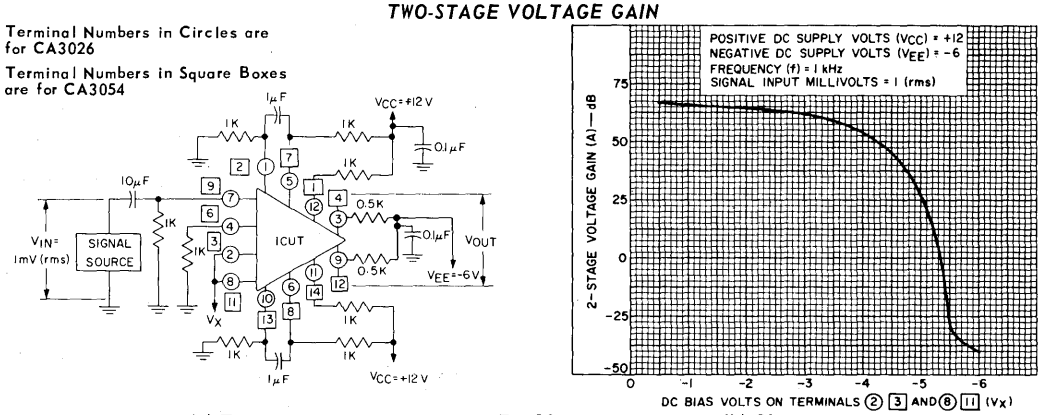
TYPICAL DYNAMIC CHARACTERISTICS (cont'd)

SINGLE-STAGE VOLTAGE GAIN



(a) Test setup — Fig.9 — (b) Characteristic

TWO-STAGE VOLTAGE GAIN



(a) Test setup — Fig.10 — (b) Characteristic

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

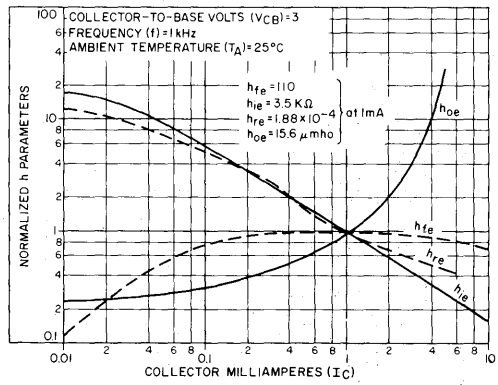


Fig.11 - Forward current-transfer ratio (h_{fe}), short-circuit input impedance (h_{ie}), open-circuit output impedance (h_{oe}), and open-circuit reverse voltage-transfer ratio (h_{re}) vs collector current for each transistor.

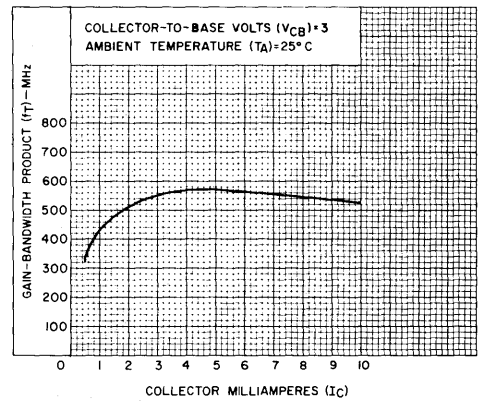


Fig.12 - Gain-bandwidth product (f_T) vs collector current.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH DIFFERENTIAL AMPLIFIER

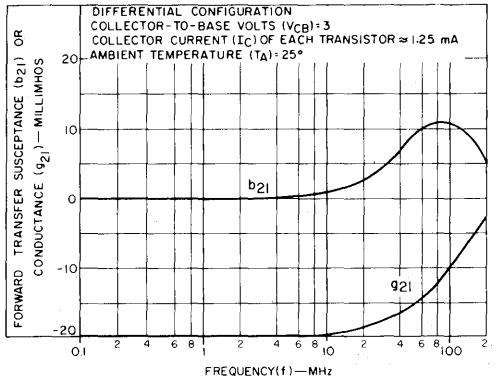


Fig.13(a) - Forward transfer admittance (Y_{21}) vs frequency.

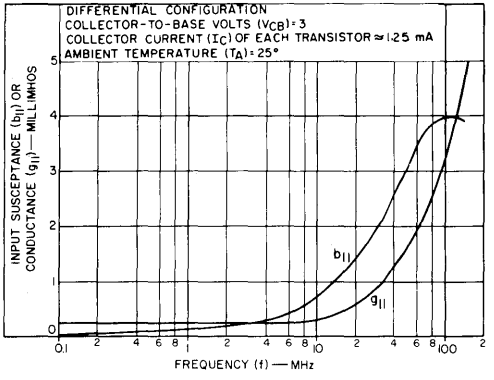


Fig.13(b) - Input admittance (Y_{11}).

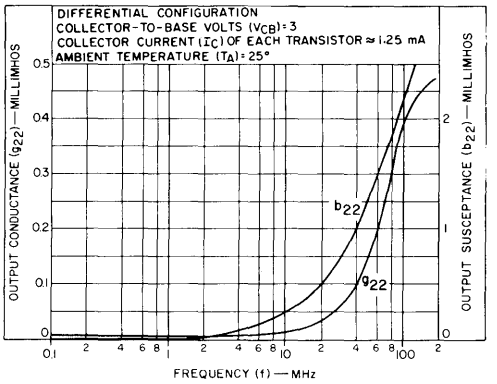


Fig.13(c) - Output admittance (Y_{22}) vs frequency.

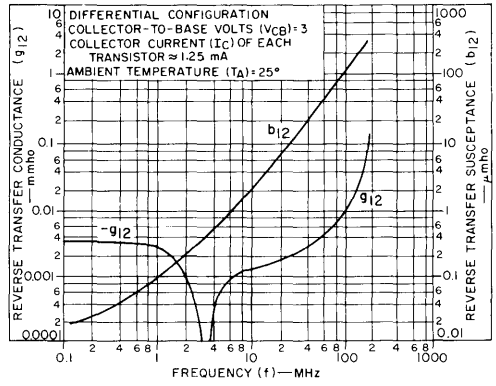


Fig.13(d) - Reverse transfer admittance (Y_{12}) vs frequency.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH CASCODE AMPLIFIER

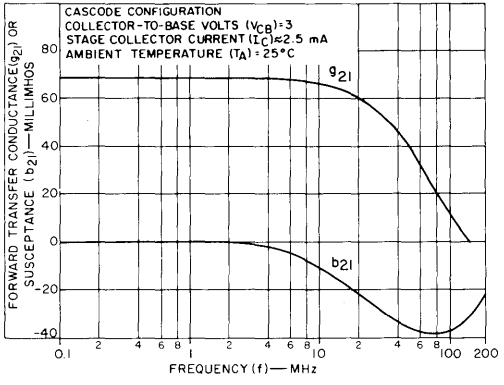


Fig.14(a) - Forward transfer admittance (Y_{21}) vs frequency.

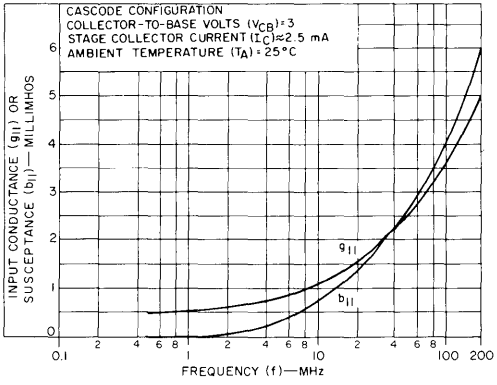


Fig.14(b) - Input admittance (Y_{11}) vs frequency.

TYPICAL CHARACTERISTICS FOR EACH CASCODE AMPLIFIER (cont'd)

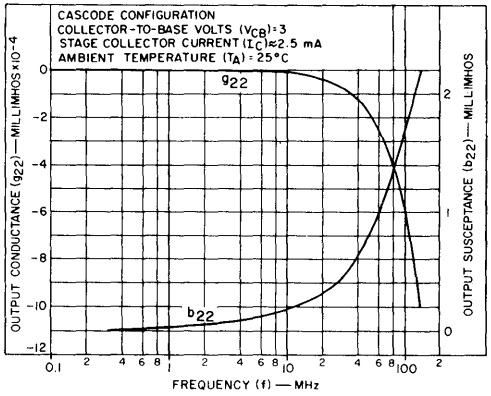


Fig.14(c) - Output admittance (Y_{22}) vs frequency.

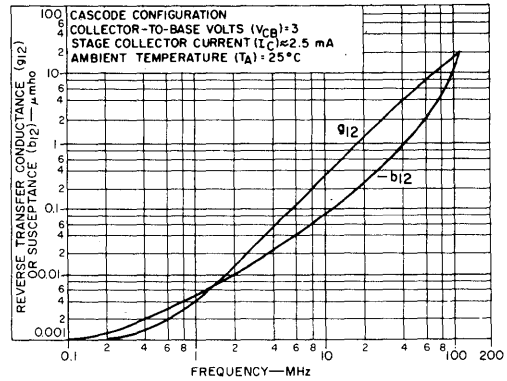


Fig.14(d) - Reverse transfer admittance (Y_{12}) vs frequency.

LINEAR 7

ARRAYS

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Selection Guide

TRANSISTOR ARRAYS

Electrical Characteristics at $T_A = 25^oC$

Type	Description	$V_{(BR)CEO}$ (Min.) V	$V_{(BR)CBO}$ (Min.) V	hFE (Min.)	I_C (Max.) mA	Package Number of Pins
CA3018	Two Isolated Transistors plus a Darlington Pair	15	20	30	50	12T
CA3018A		15	30	60	50	
		h_{FE} matched ± 10%. V_{BE} matched ±2mV and ±5mV max. Operation from DC to 120MHz.				
CA3045	Three Transistors plus a Differential Pair	15	20	40	50	14D, 14F
CA3046		15	20	40	50	14E
		f_t > 300MHz 2 matched pairs ±5mV				
CA3081	General-Purpose n-p-n High-Current Transistors	16	20	40	100	16E, 16F
		Seven Common-Emitter				
CA3082		16	20	40	100	16E, 16F
		Seven Common-Collector				
CA3083		15	20	40	100	16E, 16F
		Five independent transistors Q_1 and Q_2 matched: (I_{IO} at 1mA.) 2.5μA maximum.				
CA3086	Three Isolated Transistors plus a Differential Pair	15	20	40	50	14E, 14F
		f_T > 550MHz typ. Operation from DC to 120MHz				
CA3127	Five Independent Transistors	15	20	40	20/trans.	16E, 16F
		f_T > 1 GHz. Operation from DC to 500MHz.				
CA3146	Three Transistors plus a Differential Pair	30	40	30	50	16E
CA3146A		40	50	30	50	
		f_T > 500MHz typ. Operation from DC to 120MHz.				
CA3183	Five High-Current Transistors	30	40	40	75	16E
CA3183A		40	50	40	75	
		High-voltage versions of CA3083 Transistors Q_1 and Q_2 matched at 1mA.				
CA3227	Five Independent Transistors	8	12	40	20/trans.	16E
		ft = 3GHz typ. Operation from DC to 1.5GHz.				
CA3246	Three Independent Transistors plus a Differential Pair	8	12	40	20	14E
		f_t = 3GHz typ. Operation from DC to 1.5GHZ.				

Selection Guide

TRANSISTOR ARRAYS (Continued)

Electrical Characteristics at T_A = 25°C

Type	Description	$V_{(BR)CEO}$ (Min.) V n-p-n/p-n-p	$V_{(BR)CBO}$ (Min.) V n-p-n/p-n-p	h_{FE} (Min..) n-p-n/p-n-p	I_C (Max.) n-p-n/p-n-p	Package Number of Pins*
CA3096	Five Independent Transistors, 3 n-p-n, 2 p-n-p	35/-40	45/-40	150/20	50/-10	16E
CA3096A		35/-40	45/-40	150/20	50/-40	
CA3096C		24/-24	30/-24	100/15	50/-10	
		n-p-n		p-n-p		
		$\lvert V_{IO} \rvert$ = 5mV max.		5mV max.		
		$\lvert I_{IO} \rvert$ 0.6 μA max.		0.25 μA max.		
CA3097	Thyristor/Transistor Array 1 n-p-n, 1 n-p-n/p-n-p transistor pair, 1 zener, 1 PUT, 1 SCR	30/-40	50/-50	n-p-n/p-n-p pr. 8000 typ.	100/-10	16E
		PUT: I_P = 15nA, V_{AK} = ±30V Zener V_Z = 8V ± 10% Z_Z = 15Ω typ. at 10mA				

DIODE ARRAYS

Electrical Characteristics at T_A = 25°C. Apply for each Diode

Type	Description	$V_{(BR)R}$ (Min.) V	I_R (Max.) μA	C_D (Typ.) pF	$V_{F1} - V_{F2}$ (Max.) mV	Package Number of Pins*
CA3039	6 Individual	5	0.1	0.65	5 (I_F = 1 mA)	12T
		• Ultra-fast low-capacitance matched diodes				
CA3141	10 High Reverse Breakdown Voltage Diodes□□	30	0.1	0.3	0.55 (typ. ea. diode pr.)	16E
		• Low-noise performance • Low-leakage current				

□□ Six connected to form 3 common-cathode diode pairs.
Four connected to form 2 common-anode diode pairs.

* See Packaging Section.

May 1990

General-Purpose Transistor Arrays

Two Isolated Transistors and a Darlington-Connected Transistor Pair
For Low-Power Applications at Frequencies from DC Through the VHF Range

Features:

- *Matched monolithic general purpose transistors*
- *H_{FE} matched ± 10%*
- *V_{BE} matched ± 2 mV CA3018A (± 5m V CA3018)*
- *Operation from DC to 120 MHz*
- *Wide operating current range*
- *CA3018A performance characteristics controlled from 10 μA to 10 mA*
- *Low noise figure - 3.2 dB typical at 1 KHz*
- *Full military temperature range capability (-55°C to +125°C)*

Applications:

- *General use in signal processing systems in DC through VHF range*
- *Custom designed differential amplifiers*
- *Temperature compensated amplifiers*
- *See Application Note, ICAN-5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for suggested applications.*

The CA3018 and CA3018A consist of four general purpose silicon n-p-n transistors on a common monolithic substrate.

Two of the four transistors are connected in the Darlington configuration. The substrate is connected to a separate terminal for maximum flexibility.

The transistors of the CA3018 and the CA3018A are well suited to a wide variety of applications in low-power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits but in addition they provide the advantages of close electrical and thermal matching inherent in integrated circuit construction.

The CA3018A is similar to the CA3018 but features tighter control of current gain, leakage, and offset parameters making it suitable for more critical applications requiring premium performance.

Both devices are supplied in a 12-lead TO-5 style can package (T suffix).

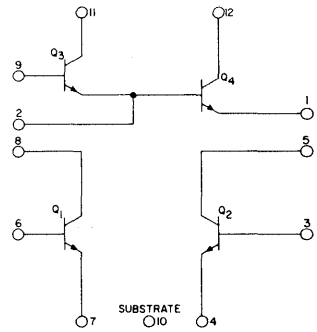


Fig. 1 - Schematic Diagram for CA3018 and CA3018A.

Maximum Ratings, Absolute-Maximum Values, at TA=25°C

	CA3018	CA3018A	
Power Dissipation, P:			
Any one transistor	300	300	mW
Total package	450	450	mW
Derate at 5 mW/°C for $T_A > 85°C$			
Temperature Range:			
Operating	-55 to + 125	-55 to + 125	°C
Storage	-65 to + 150	-65 to + 150	°C

The following ratings apply for each transistor in the device:

	CA3018	CA3018A	
Collector-to-Emitter Voltage, V_{CEO}	15	15	V
Collector-to-Base Voltage, V_{CBO}	20	30	V
Collector-to-Substrate Voltage, V_{CIO}*	20	40	V
Emitter-to-Base Voltage, V_{EBO}	5	5	V
Collector Current, I_C	50	50	mA

*The collector of each transistor of the CA3018 and CA3018A is isolated from the substrate by an integral diode. *The substrate (terminal 10) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

LEAD TEMPERATURE (During Soldering)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max. . . . . +265°C

Characteristics apply for each transistor in the CA3018 and CA3018A as specified.

ELECTRICAL CHARACTERISTICS at T_A = 25°C	SYMBOLS	SPECIAL TEST CONDITIONS	CA3018 LIMITS			CA3018A LIMITS			Units	CHARACTERISTICS CURVES
			Min.	Typ.	Max.	Min.	Typ.	Max.		Fig.
STATIC CHARACTERISTICS										
Collector-Cutoff Current	I_{CBO}	V_{CB}=10V, I_E=0	–	0.002	100	–	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE}=10V, I_B=0	–	See Curve	5	–	See Curve	0.5	μA	3
Collector-Cutoff Current Darlington Pair	I_{CEOD}	V_{CE}=10V, I_B=0	–	–	–	–	–	5	μA	–
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	15	24	–	15	24	–	V	–
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10μA, I_E=0	20	60	–	30	60	–	V	–
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E=10μA, I_C=0	5	7	–	5	7	–	V	–
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C=10μA, I_{CI}=0	20	60	–	40	60	–	V	–
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B=1mA, I_C=10mA	–	0.23	–	–	0.23	0.5	V	–
Static Forward Current Transfer Ratio	h_{FE}	V_{CE}=3V, I_C=10mA	–	100	–	50	100	–	–	4
		V_{CE}=3V, I_C=1mA	30	100	200	60	100	200	–	
		V_{CE}=3V, I_C=10μA	–	54	–	30	54	–	–	
Magnitude of Static-Beta Ratio (Isolated Transistors Q_1 and Q_2)		V_{CE}=3V, I_{C1}=I_{C2}=1mA	0.9	0.97	–	0.9	0.97	–	–	4
Static Forward Current Transfer Ratio Darlington Pair (Q_3 & Q_4)	h_{FED}	V_{CE}=3V, I_C=1mA	1500	5400	–	2000	5400	–	–	5
		V_{CE}=3V, I_C=100μA	–	–	–	1000	2800	–		
Base-to-Emitter Voltage	V_{BE}	V_{CE}=3V, I_E=1mA	–	0.715	–	0.600	0.715	0.800	V	6
		V_{CE}=3V, I_E=10mA	–	0.800	–	–	0.800	0.900		
Input Offset Voltage	$\lvert V_{BE_1} - V_{BE_2} \rvert$	V_{CE}=3V, I_E=1mA	–	0.48	5	–	0.48	2	mV	6,8
Temperature Coefficient: Base-to-Emitter Voltage Q_1,Q_2	$\lvert \frac{\Delta V_{BE}}{\Delta T} \rvert$	V_{CE}=3V, I_E=1mA	–	-1.9	–	–	-1.9	–	mV/°C	7
Base (Q_3)-to-Emitter (Q_4) Voltage-Darlington Pair	V_{BED} (V_{9-1})	V_{CE}=3V, I_E=10mA	–	1.46	–	–	1.46	1.60	V	9
		V_{CE}=3V, I_E=1mA	–	1.32	–	1.10	1.32	1.50		
Temperature Coefficient: Base-to-Emitter Voltage Darlington Pair-Q_3,Q_4	$\lvert \frac{\Delta V_{BED}}{\Delta T} \rvert$	V_{CE}=3V, I_E=1mA	–	4.4	–	–	4.4	–	mV/°C	10
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\lvert \frac{V_{BE_1} - V_{BE_2}}{\Delta T} \rvert$	V_{CC}=+6V, V_{EE}=-6V, I_{C1}=I_{C2}=1mA	–	10	–	–	10	–	μV/°C	–

ELECTRICAL CHARACTERISTICS, (CONT'D)

DYNAMIC CHARACTERISTICS											
Low Frequency Noise Figure	NF	f=1 KHz, V_{CE}=3V, I_C=100μA Source resistance=1KΩ	–	3.25	–	–	3.25	–	dB	11(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Forward Current-Transfer Ratio	h_{fe}	f=1kHz, V_{CE}=3V, I_C=1mA	–	110	–	–	110	–	–	12
Short-Circuit Input Impedance	h_{ie}		–	3.5	–	–	3.5	–	KΩ	12
Open-Circuit Output Impedance	h_{oe}		–	15.6	–	–	15.6	–	μmho	12
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		–	$1.8x10^{-4}$	–	–	$1.8x10^{-4}$	–	–	12
Admittance Characteristics:										
Forward Transfer Admittance	Y_{fe}	f=1MHz, V_{CE}=3V, I_C=1mA	–	31-j1.5	–	–	31-j1.5	–	mmho	13
Input Admittance	Y_{ie}		–	0.3+j0.04	–	–	0.3+j0.04	–	mmho	14
Output Admittance	Y_{oe}		–	0.001+j0.03	–	–	0.001+j0.03	–	mmho	15
Reverse Transfer Admittance	Y_{re}		See Curve			See Curve			mmho	16
Gain-Bandwidth Product	f_T	V_{CE}=3V, I_C=3mA	300	500	–	300	500	–	MHz	17
Emitter-to-Base Capacitance	C_{EB}	V_{EB}=3V, I_E=0	–	0.6	–	–	0.6	–	pF	–
Collector-to-Base Capacitance	C_{CB}	V_{CB}=3V, I_C=0	–	0.58	–	–	0.58	–	pF	–
Collector-to-Substrate Capacitance	C_{CI}	V_{CI}=3V, I_C=0	–	2.8	–	–	2.8	–	pF	–

STATIC CHARACTERISTICS

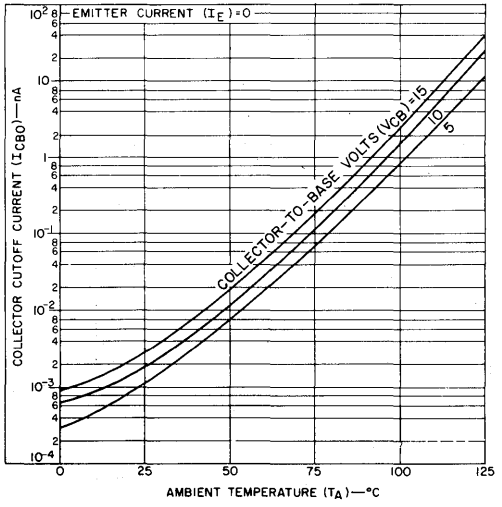


Fig.2 - Typical Collector-To-Base Cutoff Current vs Ambient Temperature for Each Transistor.

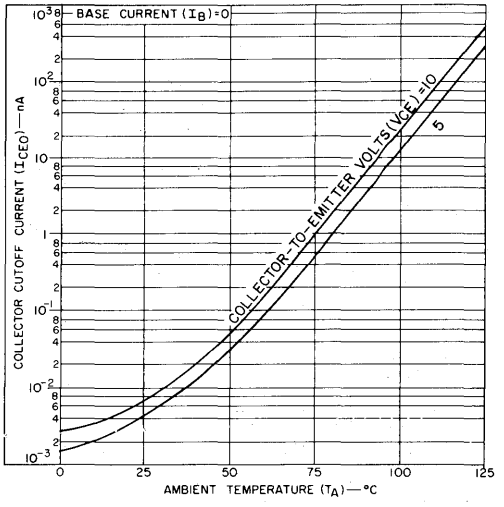


Fig.3 - Typical Collector-To-Emmiter Cutoff Current vs Ambient Temperature for Each Transistor.

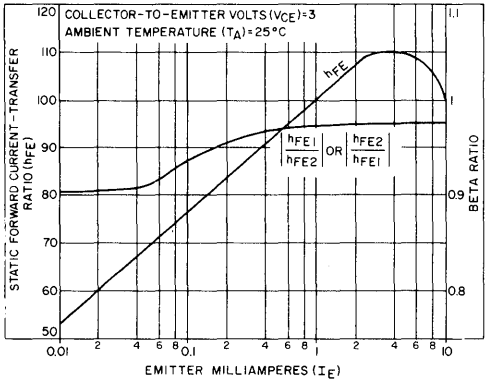


Fig.4 - Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q_1 and Q_2 vs Emitter Current.

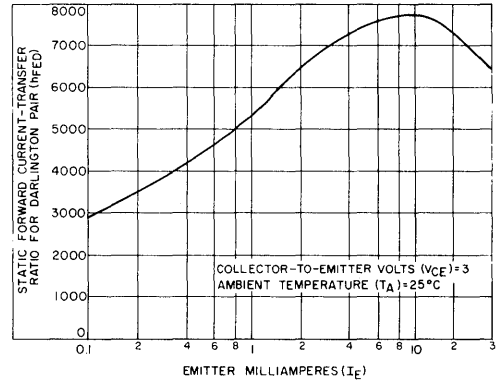


Fig.5 - Typical Static Forward Current - Transfer Ratio for Darlington-connected Transisters Q_3 and Q_4 vs Emitter Current.

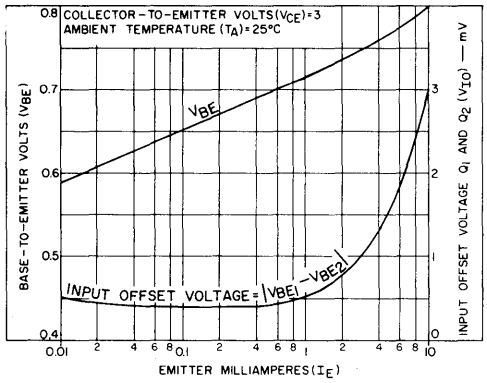


Fig.6 - Typical Static Base-to-Emitter Voltage Characteristic and Input Offset Voltage for Q_1 and Q_2 vs Emitter Current.

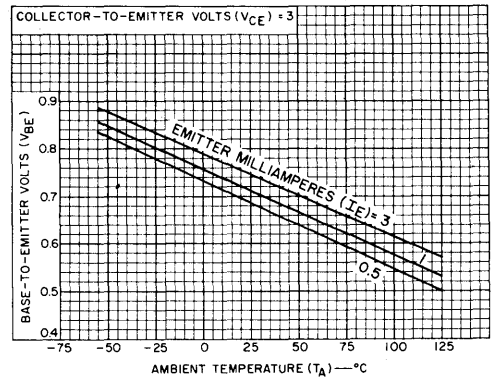


Fig.7 - Typical Base-To-Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature

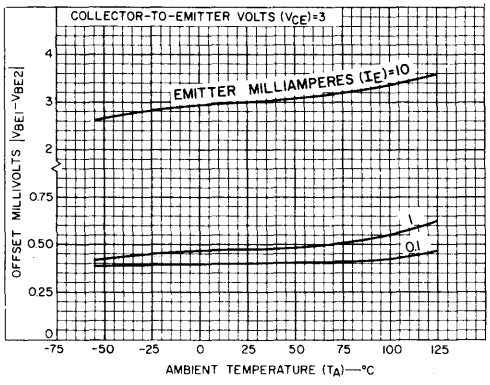


Fig.8 - Typical Offset Voltage Characteristic vs Ambient Temperature

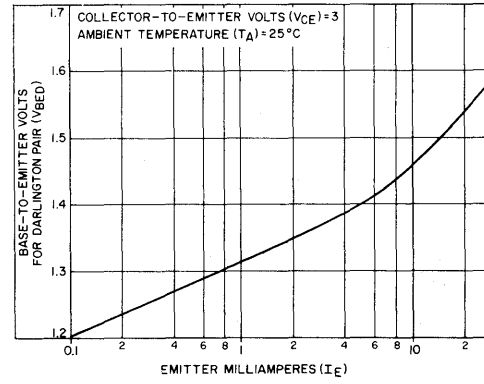


Fig.9 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Emitter Current

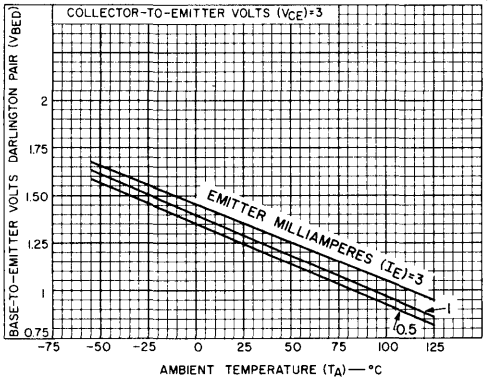


Fig.10 - Typical Static Input Voltage Characteristic for Darlington Pair (Q_3 and Q_4) vs Ambient Temperature.

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

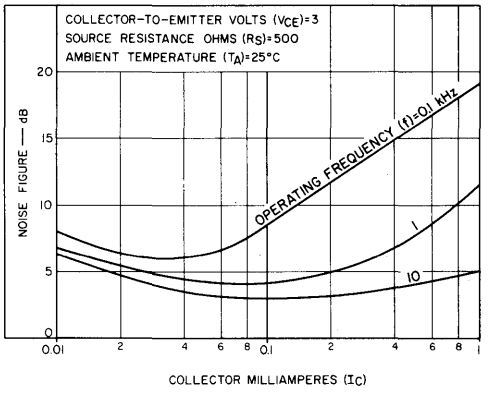


Fig.11(a) - Noise Figure vs Collector Current, R_S = 500 Ω.

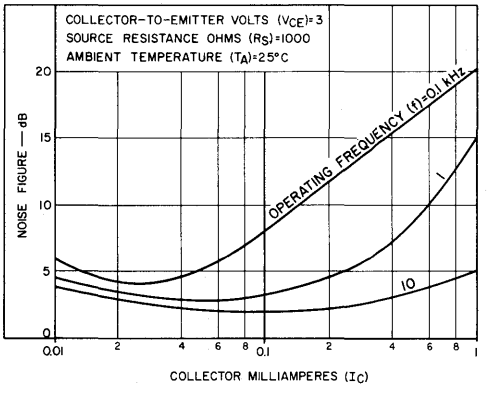


Fig.11(b) - Noise Figure vs Collector Current, R_S = 1 KΩ.

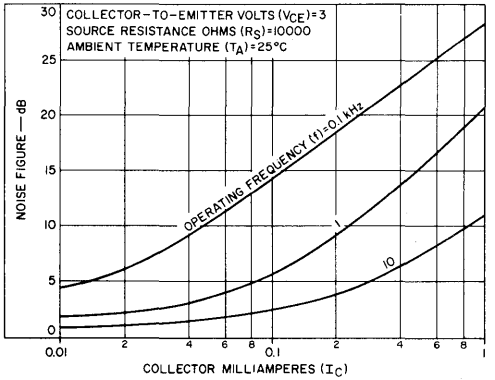


Fig.11(c) - Noise Figure vs Collector Current, R_S = 10 KΩ.

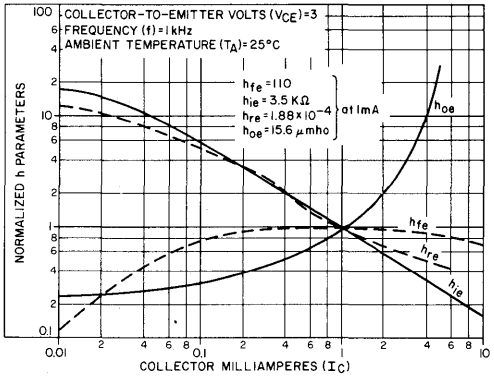


Fig.12 - Forward Current-Transfer Ratio (h_{fe}), Short-Circuit Input Impedance (h_{ie}), Open-Circuit Output Impedance (h_{oe}), and Open-Circuit Reverse Voltage-Transfer Ratio (h_{re}) vs Collector Current

TYPICAL DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

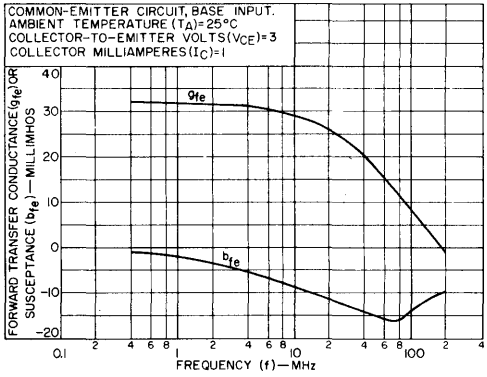


Fig. 13 - Forward Transfer Admittance (Y_{fe})

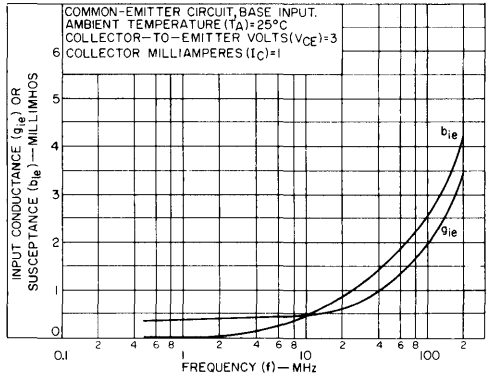


Fig. 14 - Input Admittance (Y_{ie})

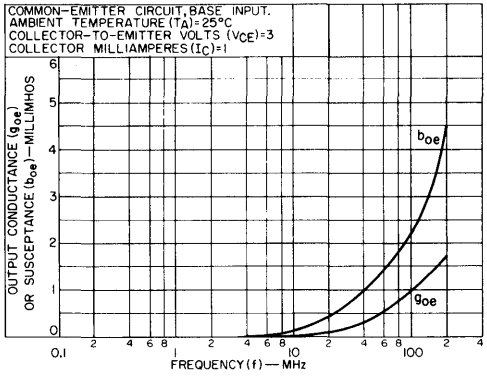


Fig. 15 - Output Admittance (Y_{oe})

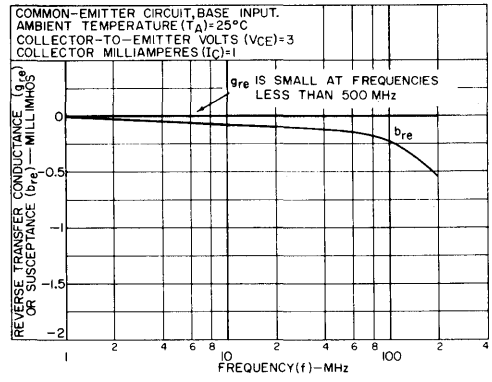


Fig. 16 - Reverse Transfer Admittance (Y_{re})

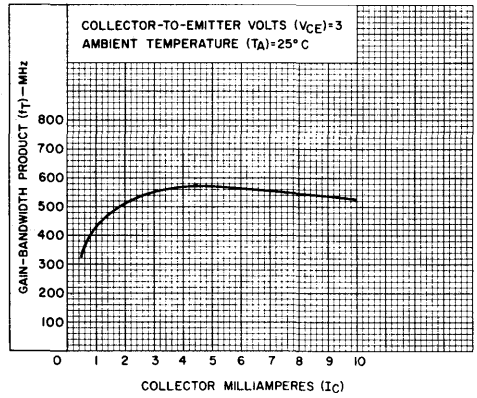


Fig. 17 - Typical Gain-Bandwidth Product (f_T) vs Collector Current

May 1990

Diode Array

Six Matched Diodes on a Common Substrate
Ultra-Fast Low-Capacitance Matched Diodes
For Applications in Communications and Switching Systems

Features:

- *Excellent reverse recovery time - 1 ns typ.*
- *Matched monolithic construction - V_F matched within 5 mV*
- *Low diode capacitance - C_D = 0.65 pF typical at V_R = -2 V*

Applications:

- *Balanced modulators or demodulators*
- *Ring modulators*
- *High speed diode gates*
- *Analog switches*

The CA3039 consists of six ultra-fast, low capacitance diodes on a common monolithic substrate. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the array extremely useful for a wide variety of applications in communication and switching systems.

Five of the diodes are independently accessible, the sixth shares a common terminal with the substrate.

For applications such as balanced modulators or ring modulators where capacitive balance is important, the substrate should be returned to a DC potential which is significantly more negative (with respect to the active diodes) than the peak signal applied.

The CA3039 is available in a 12-lead TO-5 style can package (T suffix) and in a 14-lead Small Outline package (M suffix).

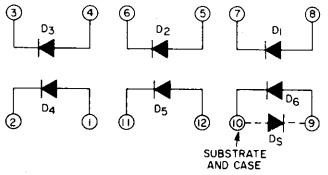


Figure 1 - Schematic Diagram for CA3039.

ABSOLUTE MAXIMUM RATINGS at T_A = 25 °C

Dissipation:

Any one diode unit . . . . . 100 mW

Total for device . . . . . 600 mW

For T_A > 55 °C . . . . . derate linearly 5.7 mW/°C

Temperature Range:

Operating . . . . . -55 to +125 °C

Storage . . . . . -65 to +150°C

Peak Inverse Voltage, PIV for: D_1-D_5 . . . 5 V

D_6 . . . . . 0.5 V

Peak Diode-to-Substrate Voltage, V_{DI}

for D_1-D_5 (term. 1,4,5,8 or 12 to term. 10) +20, -1 V

DC Forward Current, I_F . . . . . 25 mA

Peak Recurrent Forward Current, I_f . . . . . 100 mA

Peak Forward Surge Current, I_f (surge) . . . 100 mA

LEAD TEMPERATURE (During Soldering)

At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm)

from case for 10 seconds max. . . . . + 265 °C

ELECTRICAL CHARACTERISTICS, at T_A = 25° C

Characteristics apply for each diode unit, unless otherwise specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS			UNITS	CHARACTERISTIC CURVES
			MIN.	TYP.	MAX.		FIG.
DC Forward Voltage Drop	V_F	I_F = 50 μA	–	0.65	0.69	V	2
		1 mA	–	0.73	0.78	V	
		3 mA	–	0.76	0.80	V	
		10 mA	–	0.81	0.90	V	
DC Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = -10 μA	5	7	–	V	–
DC Reverse Breakdown Voltage Between any Diode Unit and Substrate	$V_{(BR)R}$	I_R = -10 μA	20	–	–	V	–
DC Reverse (Leakage) Current	I_R	V_R = -4 V	–	0.016	100	nA	3
DC Reverse (Leakage) Current Between any Diode Unit and Substrate	I_R	V_R = -10 V	–	0.022	100	nA	4
Magnitude of Diode Offset Voltage (Difference in DC Forward Voltage Drops of any Two Diode Units)	$\lvert V_{F_1} - V_{F_2} \rvert$	I_F = 1 mA	–	0.5	5	mV	2
Temperature Coefficient of $\lvert V_{F_1} - V_{F_2} \rvert$	$\frac{\Delta \lvert V_{F_1} - V_{F_2} \rvert}{\Delta T}$	I_F = 1 mA	–	1	–	μV/°C	5
Temperature Coefficient of Forward Drop	$\frac{\Delta V_F}{\Delta T}$	I_F = 1 mA	–	-1.9	–	mV/°C	6
DC Forward Voltage Drop for Anode-to-Substrate Diode (D_S)	V_F	I_F = 1 mA	–	0.65	–	V	–
Reverse Recovery Time	t_{rr}	I_F = 10 mA, I_R = 10 mA	–	1	–	ns	–
Diode Resistance	R_D	f = 1 kHz, I_F = 1 mA	25	30	45	Ω	7
Diode Capacitance	C_D	V_R = -2 V, I_F = 0	–	0.65	–	pF	8
Diode-to-Substrate Capacitance	C_{DI}	V_{DI} = +4 V, I_F = 0	–	3.2	–	pF	9

TYPICAL CHARACTERISTICS

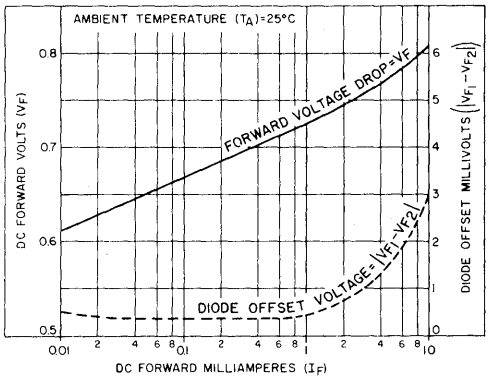


Fig. 2 - DC forward voltage drop (any diode) and diode offset voltage vs DC forward current

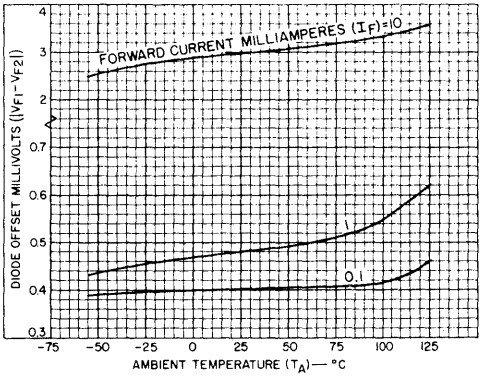


Fig. 5 - Diode offset voltage (any diode) vs temperature

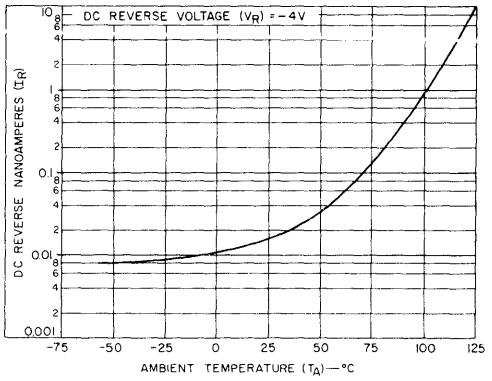


Fig. 3 - DC reverse (leakage) current (diodes 1,2,3,4,5) vs temperature

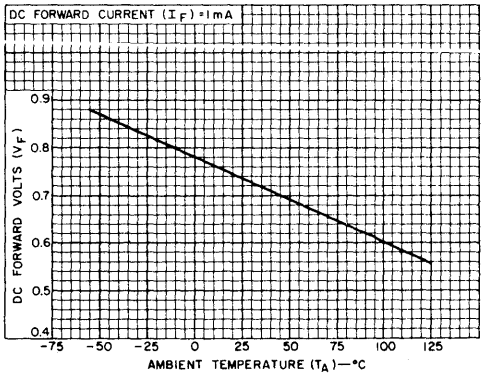


Fig. 6 - DC forward voltage drop (any diode) vs temperature

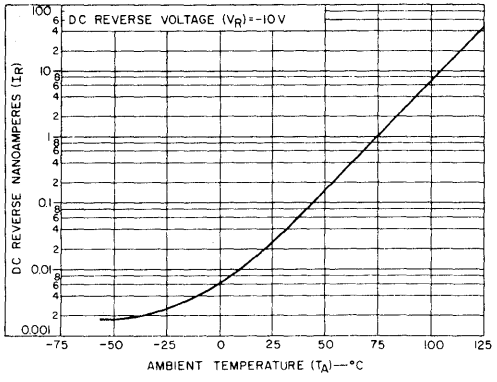


Fig. 4 - DC reverse (leakage) current between diodes (1,2,3,4,5) and substrate vs temperature

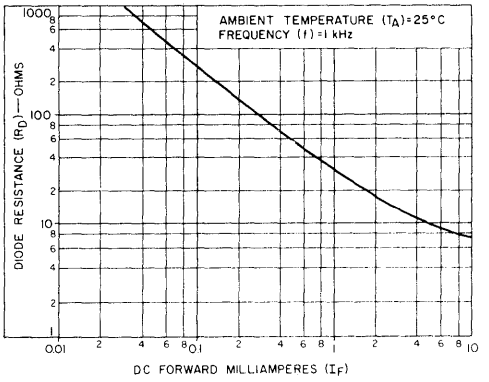


Fig. 7 - Diode resistance (any diode) vs DC forward current

7 ARRAYS

TYPICAL CHARACTERISTICS

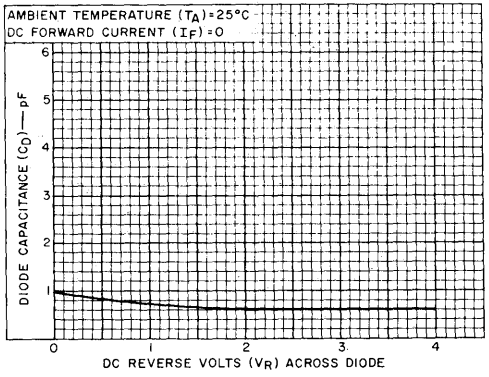


Fig. 8 - Diode capacitance (diodes 1,2,3,4,5) vs reverse voltage

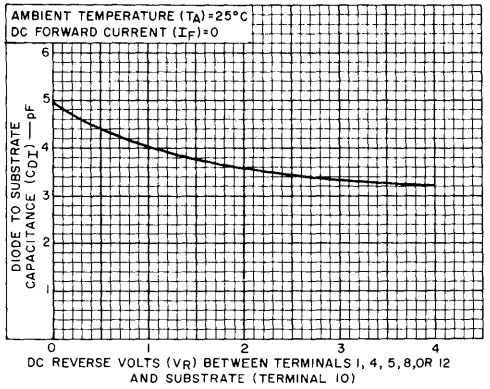


Fig. 9 - Diode-to-substrate capacitance vs reverse voltage

May 1990

General-Purpose N-P-N Transistor Arrays

Three Isolated Transistors and One Differentially-Connected Transistor Pair
For Low-Power Applications at Frequencies from DC through the VHF Range

Features:

- *Two matched pairs of transistors*
  V_{BE} matched ± 5 mV
  Input offset current 2 μA max. at I_C = 1 mA
- *5 general purpose monolithic transistors*
- *Operation from DC to 120 MHz*
- *Wide operating current range*
- *Low noise figure - 3.2 dB typ. at 1 KHz*
- *Full military temperature range for CA3045 -55°C to +125°C*

Applications:

- *General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF*
- *Custom designed differential amplifiers*
- *Temperature compensated amplifiers*
- *See Application Note, ICAN-5296 "Application of the CA3018 Integrated-Circuit Transistor Array" for suggested applications.*

The CA3045 and CA3046 each consist of five general purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3045 and CA3046 are well suited to a wide variety of applications in low power systems in the DC through VHF range. They may be used as discrete transistors in conventional circuits. However, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching.

The CA3045 is supplied in a 14-lead dual-in-line hermetic (welded-seal) ceramic package and the CA3045F in a 14-lead dual-in-line hermetic (frit-seal) ceramic package.

The CA3046 is electrically identical to the CA3045 but is supplied in a 14-lead dual-in-line plastic package (E suffix) and in 14-lead Small Outline package (M suffix) for applications requiring only a limited temperature range.

The CA3045 and CA3046 are available in the packages shown below

PACKAGE	SUFFIX LETTER	CA3045	CA3046
14-Lead Dual-In-Line Plastic	E		√
14-Lead Dual-In-Line Ceramic	D	√	
14-Line Dual-In-Line Frit-Seal Ceramic	F	√	
Chip	H	√	
14-Lead Small Outline	M		√

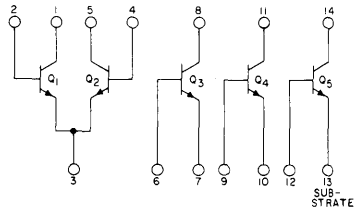


Figure 1 - Schematic diagram.

7 ARRAYS

ABSOLUTE MAXIMUM RATINGS AT T_A = 25°C

	CA3045		CA3046, CA3045F		
	Each Transistor	Total Package	Each Transistor	Total Package	
Power Dissipation:					
T_A up to 55°C	–	–	300	750	mW
T_A > 55°C	–	–	Derate at 6.67		mW/°C
T_A up to 75°C	300	750	–	–	mW
T_A > 75°C	Derate at 8		–	–	mW/°C
Collector-to-Emitter Voltage, V_{CEO}	15	–	15	–	V
Collector-to-Base Voltage, V_{CBO}	20	–	20	–	V
Collector-to-Substrate Voltage, V_{CIO}*	20	–	20	–	V
Emitter-to-Base Voltage, V_{EBO}	5	–	5	–	V
Collector Current	50	–	50	–	mA
Temperature Range:					
Operating	–55 to +125		–55 to +125		°C
Storage	–65 to +150		–65 to +150		°C
Lead Temperature (During Soldering):					
At distance 1/16 ±1/32" (1.59 ±0.79 mm) from case for 10 seconds max.	+265		+265		°C

* The collector of each transistor of the CA3045 and CA3046 is isolated from the substrate by an integral diode. *The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.*

ELECTRICAL CHARACTERISTICS, at T_A = 25°C

Characteristics apply for each transistor in the CA3045 and CA3046 as specified.

CHARACTERISTICS	SYMBOLS	SPECIAL TEST CONDITIONS	LIMITS Type CA3045 Type CA3046 MIN.	TYP.	MAX.	UNITS	CHARACTERISTIC CURVES FIG.
STATIC CHARACTERISTICS							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	20	60	-	V	-
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	15	24	-	V	-
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	20	60	-	V	-
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	5	7	-	V	-
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	-	0.002	40	nA	2
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	-	See curve	0.5	μA	3
Static Forward Current-Transfer Ratio (Static Beta)	h_{FE}	V_{CE} = 3 V, I_C = 10 mA	-	100	-	-	4
		V_{CE} = 3 V, I_C = 1 mA	40	100	-	-	
		V_{CE} = 3 V, I_C = 10 μA	-	54	-	-	
Input Offset Current for Matched Pair Q_1 and Q_2. $\lvert I_{IO_1} - I_{IO_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.3	2	μA	5
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V, I_E = 1 mA	-	0.715	-	V	6
		V_{CE} = 3 V, I_E = 10 mA	-	0.800	-		
Magnitude of Input Offset Voltage for Differential Pair $\lvert V_{BE_1} - V_{BE_2} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV	6,8
Magnitude of Input Offset Voltage for Isolated Transistors $\lvert V_{BE_3} - V_{BE_4} \rvert$, $\lvert V_{BE_4} - V_{BE_5} \rvert$, $\lvert V_{BE_5} - V_{BE_3} \rvert$		V_{CE} = 3 V, I_C = 1 mA	-	0.45	5	mV	6,8
Temperature Coefficient of Base-to-Emitter Voltage	$\frac{\Delta V_{BE}}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	-1.9	-	mV °C	7
Collector-to-Emitter Saturation Voltage	V_{CES}	I_B = 1 mA, I_C = 10 mA	-	0.23	-	V	-
Temperature Coefficient: Magnitude of Input-Offset Voltage	$\frac{\lvert \Delta V_{IO} \rvert}{\Delta T}$	V_{CE} = 3 V, I_C = 1 mA	-	1.1	-	μV °C	8

ELECTRICAL CHARACTERISTICS (Cont'd.)

DYNAMIC CHARACTERISTICS							
Low-Frequency Noise Figure	NF	f = 1 kHz, V_{CE} = 3 V, I_C = 100 μA Source Resistance = 1 kΩ	-	3.25	-	dB	9(b)
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:							
Forward Current-Transfer Ratio	h_{fe}	f = 1 kHz, V_{CE} = 3 V, I_C = 1 mA	-	110	-	-	10
Short-Circuit Input Impedance	h_{ie}		-	3.5	-	kΩ	
Open-Circuit Output Impedance	h_{oe}		-	15.6	-	μmho	
Open-Circuit Reverse Voltage-Transfer Ratio	h_{re}		-	1.8×10^{-4}	-	-	
Admittance Characteristics:							
Forward Transfer Admittance	Y_{fe}	f = 1 MHz, V_{CE} = 3 V, I_C = 1 mA	-	31-j1.5	-	-	11
Input Admittance	Y_{ie}		-	0.3+j0.04	-	-	12
Output Admittance	Y_{oe}		-	0.001+j0.03	-	-	13
Reverse Transfer Admittance	Y_{re}		-	See curve	-	-	14
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 3 mA	300	550	-	-	15
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 3 V, I_E = 0	-	0.6	-	pF	-
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 3 V, I_C = 0	-	0.58	-	pF	-
Collector-to-Substrate Capacitance	C_{CI}	V_{CS} = 3 V, I_C = 0	-	2.8	-	pF	-

STATIC CHARACTERISTICS

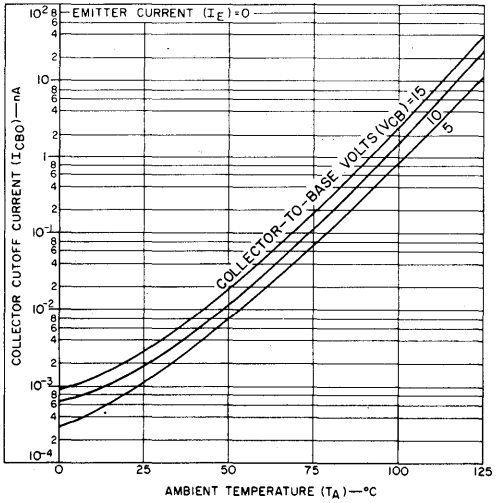


Fig.2 - Typical collector-to-base cutoff current vs ambient temperature for each transistor.

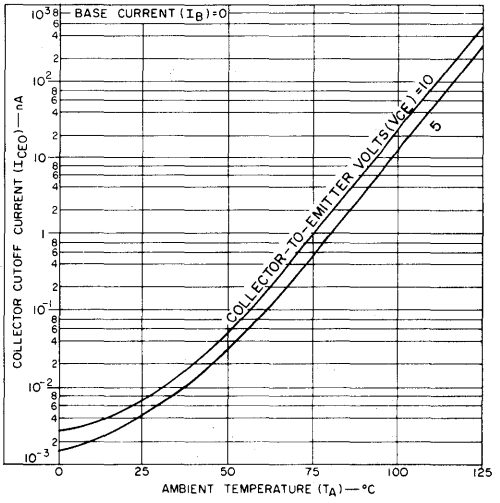


Fig.3 - Typical collector-to-emitter cutoff current vs ambient temperature for each transistor.

STATIC CHARACTERISTICS

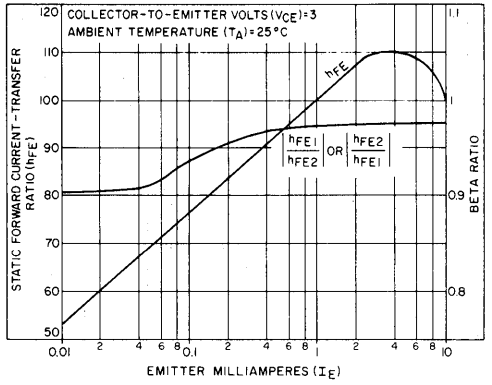


Fig.4 - Typical static forward current-transfer ratio and beta ratio for transistors Q_1 and Q_2 vs emitter current.

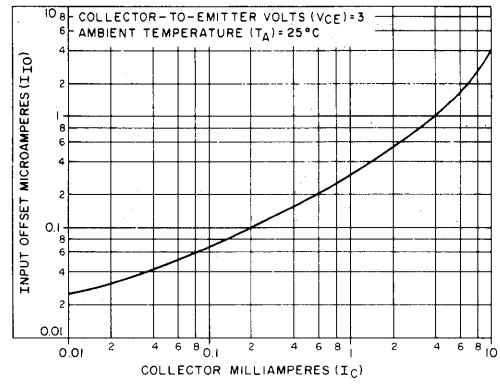


Fig.5 - Typical input offset current for matched transistor pair Q_1Q_2 vs collector current.

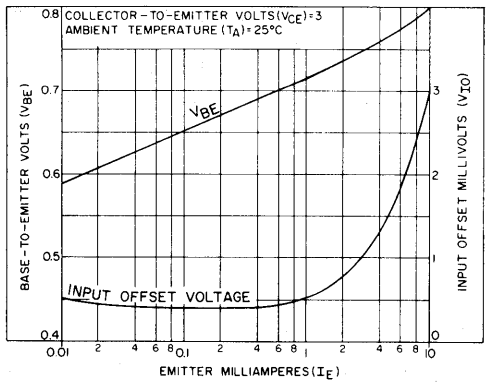


Fig.6 - Typical static base-to-emitter voltage characteristic and input offset voltage for differential pair and paired isolated transistors vs emitter current.

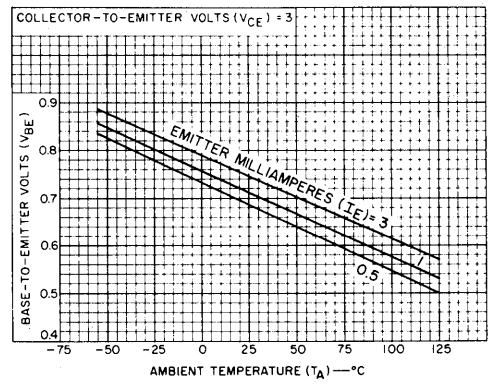


Fig.7 - Typical base-to-emitter voltage characteristic vs ambient temperature for each transistor.

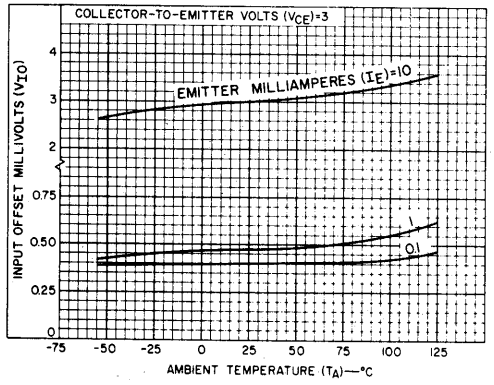


Fig.8 - Typical input offset voltage characteristics for differential pair and paired isolated transistors vs ambient temperature.

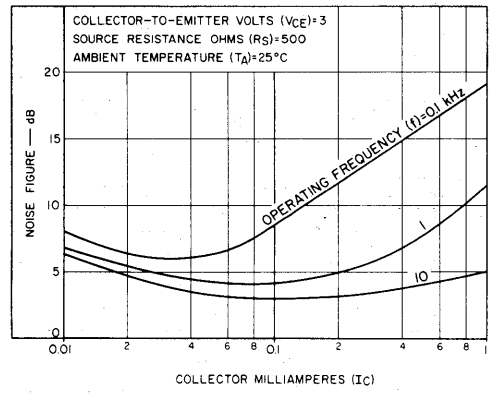


Fig.9(a) - Typical noise figure vs collector current.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

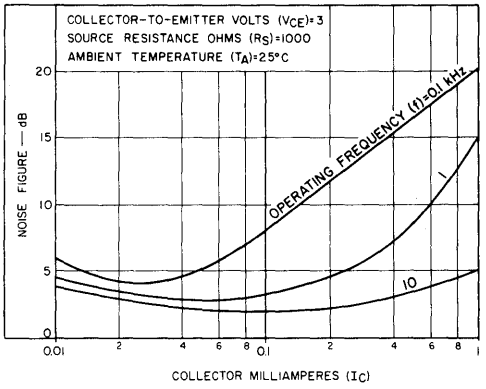


Fig.9(b) - Typical noise figure vs collector current.

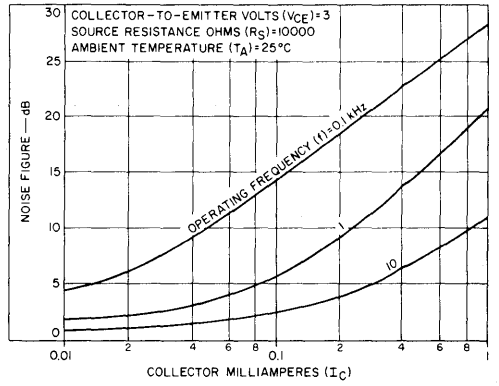


Fig.9(c) - Typical noise figure vs collector current.

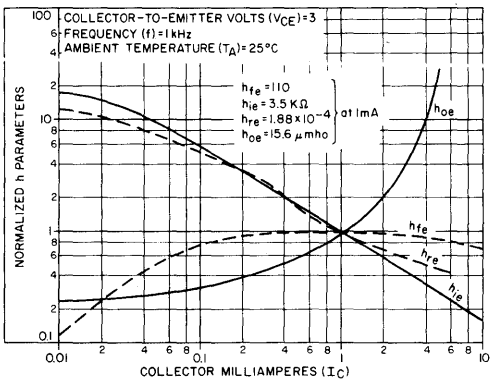


Fig.10 - Typical normalized forward current-transfer ratio, short-circuit input impedance, open-circuit output impedance, and open-circuit reverse voltage-transfer ratio vs collector current.

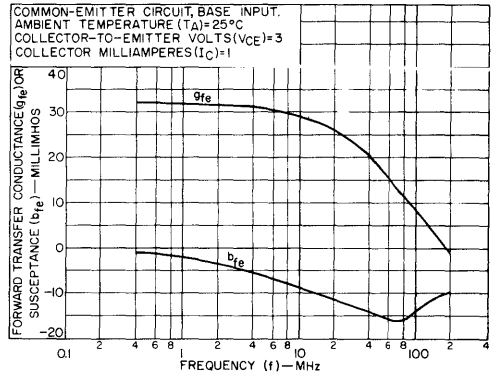


Fig.11 - Typical forward transfer admittance vs frequency.

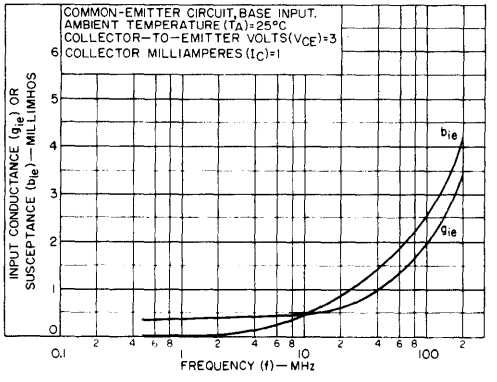


Fig.12 - Typical input admittance vs frequency.

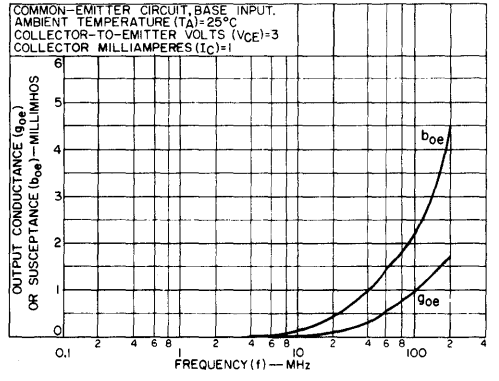


Fig.13 - Typical output admittance vs frequency.

DYNAMIC CHARACTERISTICS FOR EACH TRANSISTOR

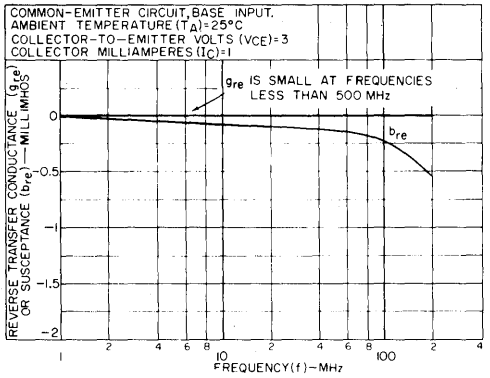


Fig.14 - Typical reverse transfer admittance vs frequency.

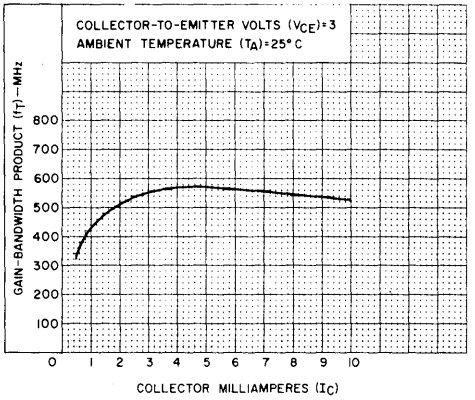


Fig.15 - Typical gain-bandwidth product vs collector current.

May 1990

General-Purpose High-Current N-P-N Transistor Arrays

CA3081 - Common-Emitter Array
CA3082 - Common-Collector Array

Directly Drive 7-Segment Incandescent Displays and Light-Emitting-Diode (LED) Displays

Features:

- *7 transistors permit a wide range of applications in either a common-emitter (CA3081) or common-collector (CA3082) configuration*
- *High I_C: 100 mA max.*
- *Low V_{CE} sat (at 50 mA): 0.4 V typ.*

Applications:

- *Drivers for:*
  -Incandescent display devices
  -LED displays
  -Relay control
  -Thyristor firing

CA3081 and CA3082 consist of seven high-current (to 100 mA) silicon n-p-n transistors on a common monolithic substrate. The CA3081 is connected in a common-emitter configuration and the CA3082 is connected in a common-collector configuration.

The CA3081 and CA3082 are capable of directly driving seven-segment displays, and light-emitting diode (LED) displays. These types are also well-suited for a variety of other drive applications, including relay control and thyristor firing.

The CA3081 and CA3082 are supplied in a 16-lead Small Outline package (M suffix), in a 16-lead dual-in-line plastic package (E suffix), and in a 16-lead dual-in-line frit-seal ceramic package (F suffix), which include a separate substrate connection for maximum flexibility in circuit design. Both types are also available in chip form.

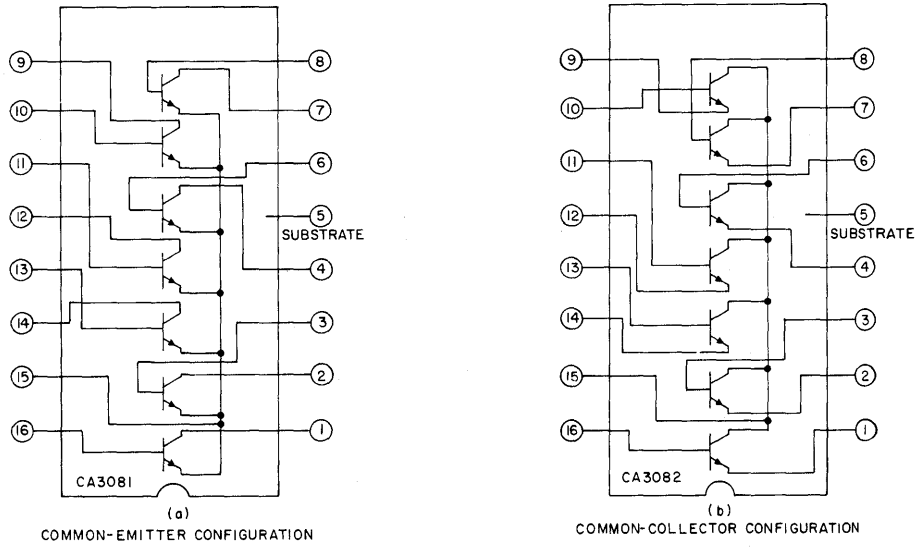


Figure 1 - Functional diagrams of types CA3081 and CA3082.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:

Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C

Ambient Temperature Range:

Operating	−55 to +125	°C
Storage	−65 to + 150	°C

Lead Temperature (During Soldering):

At distance 1/16" ±1/32" (1.59 mm ±0.79 mm)

from case for 10 seconds max.	265	°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage (V_{CEO})	16	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})*	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

* The collector of each transistor of the CA3081 and CA3082 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

For Equipment Design

CHARACTERISTIC	SYMBOL	TEST CONDITIONS		LIMITS			UNITS
			Typ. Char. Curve Fig. No.	Min.	Typ.	Max.	
Collector-to-Base Breakdown Voltage	$V_{(BR)CES}$	I_C = 500 μA, I_E = 0	–	20	60	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 500 μA, I_E = 0, I_B = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	–	16	24	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_C = 500 μA	–	5	6.9	–	V
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 0.5 V, I_C = 30 mA	–	30	68	–	
		V_{CE} = 0.8 V, I_C = 50 mA	–	40	70	–	
Base-to-Emitter Saturation Voltage	$V_{BE\ sat}$	I_C = 30 mA, I_B = 1 mA	3	–	0.87	1.0	V
Collector-to-Emitter Saturation Voltage:	$V_{CE\ sat}$						V
CA3081, CA3082		I_C = 30 mA, I_B = 1 mA	–	–	0.27	0.5	
CA3081		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.7	
CA3082		I_C = 50 mA, I_B = 5 mA	4	–	0.4	0.8	
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10 V, I_B = 0	–	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10 V, I_E = 0	–	–	–	1	μA

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR OF TYPES CA3081 AND CA3082

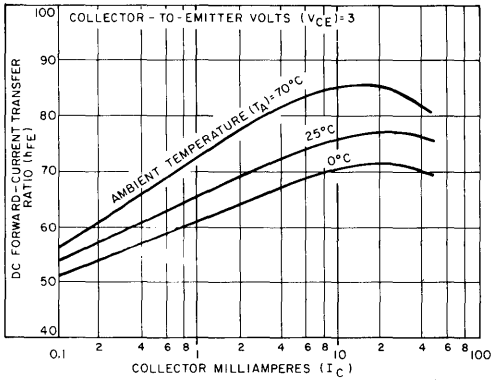


Fig. 2-h_{FE} vs. I_C

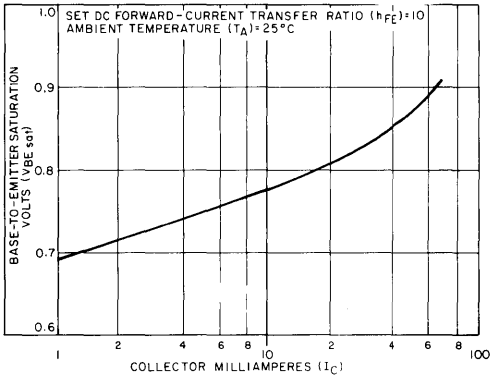


Fig. 3-V_{BEsat} vs. I_C

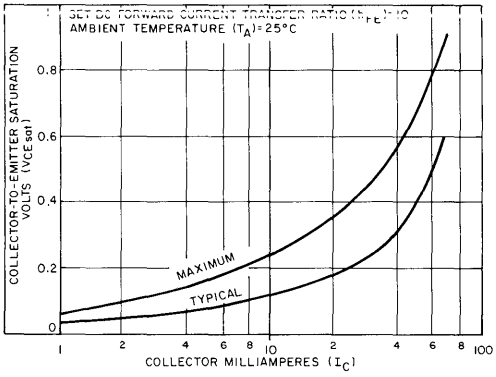


Fig. 4-V_{CEsat} vs. I_C at T_A = 25°C

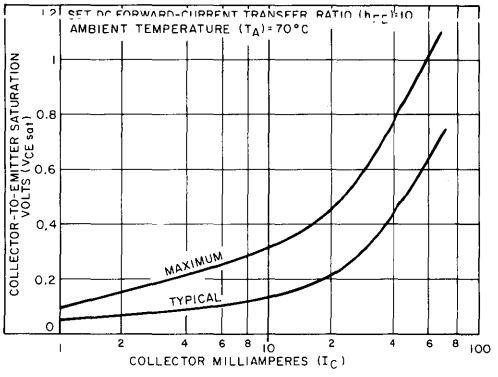


Fig. 5-V_{CEsat} vs. I_C at T_A = 70°C

TYPICAL READ-OUT DRIVER APPLICATIONS

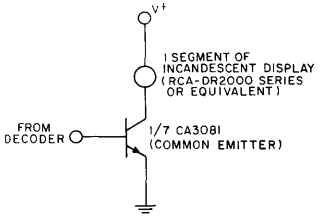
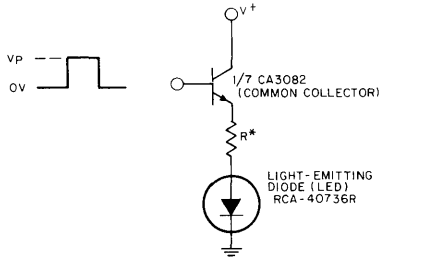


Fig.6—Schematic diagram showing one transistor of the CA3081 driving one segment of an incandescent display.



*THE RESISTANCE FOR R IS DETERMINED BY THE RELATIONSHIP

$$R = \frac{V_P - V_{BE} - V_F(LED)}{I\,(LED)}$$

WHERE: V_P = INPUT PULSE VOLTAGE

V_F = FORWARD VOLTAGE DROP ACROSS THE DIODE

R = 0 FOR $V_P = V_{BE} + V_F(LED)$

Fig.7—Schematic diagram showing one transistor of the CA3082 driving a light-emitting diode (LED).

May 1990

General-Purpose High-Current N-P-N Transistor Array

Features:

- *High I_C: 100 mA max.*
- *Low V_{CEsat} (at 50 mA): 0.7V max.*
- *Matched pair (Q1 and Q2) -*
  V_{IO} (V_{BE} matched): ± 5 μV max.
  I_{IO} (at 1 mA): 2.5 mA max.
- *5 independent transistors plus separate substrate connection*

Applications:

- *Signal processing and switching systems operating from DC to VHF*
- *Lamp and relay driver*
- *Differential amplifier*
- *Temperature-compensated amplifier*
- *Thyristor firing*
- *See Application Note, ICAN-5296 "Application of the CA3018 Circuit Transistor Array" for suggested applications*

The CA3083 is a versatile array of five high-current (to 100 mA) n-p-n transistors on a common monolithic substrate. In addition, two of these transistors (Q1 and Q2) are matched at low currents (i.e. 1 mA) for applications in which offset parameters are of special importance.

Independent connections for each transistor plus a separate terminal for the substrate permit maximum flexibility in circuit design. The CA3083 is supplied in a 16-lead dual-in-line frit-seal ceramic package (F suffix) and in a 16-lead Small Outline package (M suffix). The CA3083 is also available in chip form.

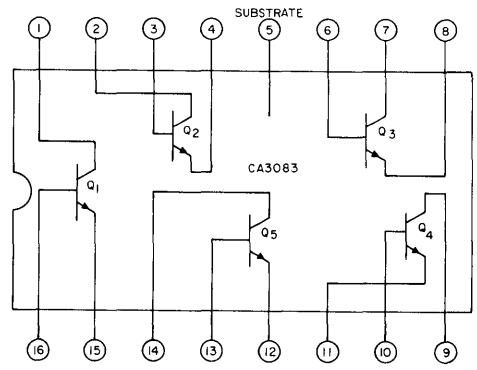


Figure 1 - Functional diagram of the CA3083.

MAXIMUM RATINGS, Absolute-Maximum Values at T_A = 25°C

Power Dissipation:

Any one transistor	500	mW
Total package	750	mW
Above 55°C	Derate linearly 6.67	mW/°C

Ambient Temperature Range:

Operating	−55 to +125	°C
Storage	−65 to +150	°C

Lead Temperature (During Soldering):

At distance 1/16" ±1/32" (1.59 mm ±0.79 mm) from case for 10 seconds max.	265	°C

The following ratings apply for each transistor in the device:

Collector-to-Emitter Voltage (V_{CEO})	15	V
Collector-to-Base Voltage (V_{CBO})	20	V
Collector-to-Substrate Voltage (V_{CIO})■	20	V
Emitter-to-Base Voltage (V_{EBO})	5	V
Collector Current (I_C)	100	mA
Base Current (I_B)	20	mA

■ The collector of each transistor of the CA3083 is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal (5) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	Typ. Char. Curve Fig. No.	LIMITS Min.	Typ.	Max.	UNITS
For Each Transistor:							
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	–	5	6.9	–	V
Collector-Cutoff-Current	I_{CEO}	V_{CE} = 10V, I_B = 0	–	–	–	10	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB} = 10V, I_E = 0	–	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 10mA I_C = 50mA	2	40 40	76 75	– –	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.74	0.85	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 50mA, I_B = 5mA	4	–	0.40	0.70	V
Gain-Bandwidth Product	f_T	V_{CE} = 3 V, I_C = 10 mA		–	450	–	MHz
For Transistors Q1 and Q2 (As a Differential Amplifier):							
Absolute Input Offset Voltage	$\lvert V_{IO} \rvert$	V_{CE} = 3V, I_C = 1mA	7	–	1.2	5	mV
Absolute Input Offset Current	$\lvert I_{IO} \rvert$		8	–	0.7	2.5	μA

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

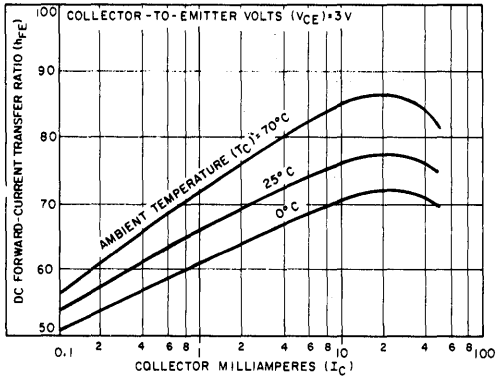


Fig.2 – h_{FE} vs I_C

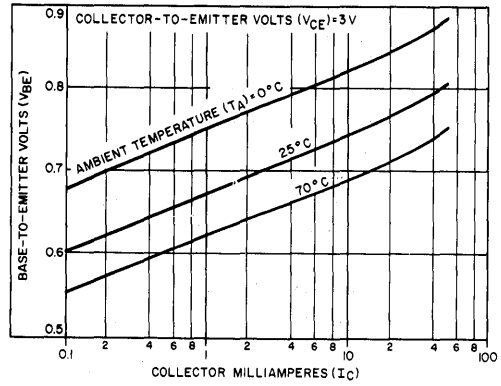


Fig.3 – V_{BE} vs I_C

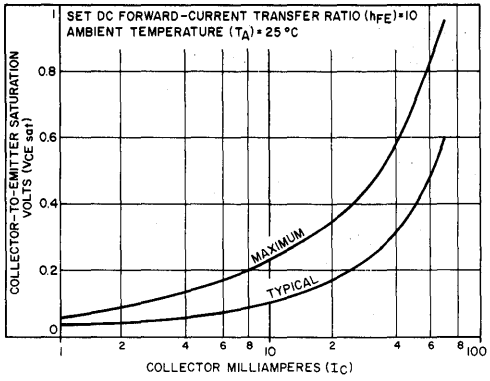


Fig.4 – V_{CEsat} vs I_C at 25°C

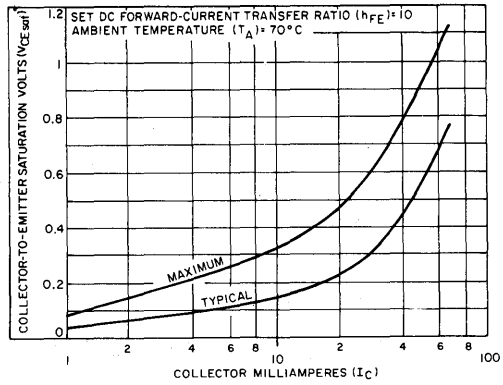


Fig.5 – V_{CEsat} vs I_C at 70°C

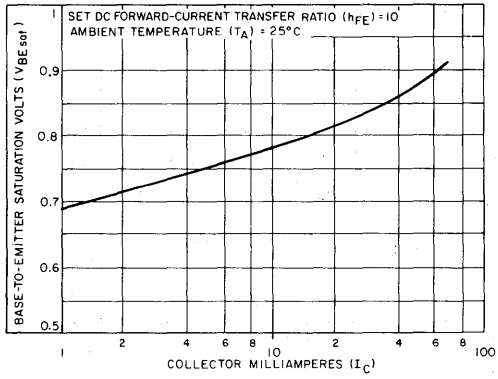


Fig.6 – V_{BEsat} vs I_C

TYPICAL STATIC CHARACTERISTICS FOR DIFFERENTIAL AMPLIFIER

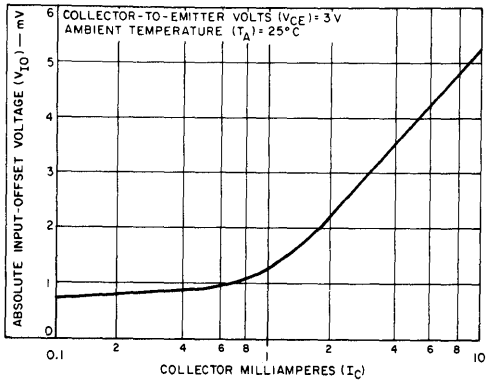


Fig.7 – V_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

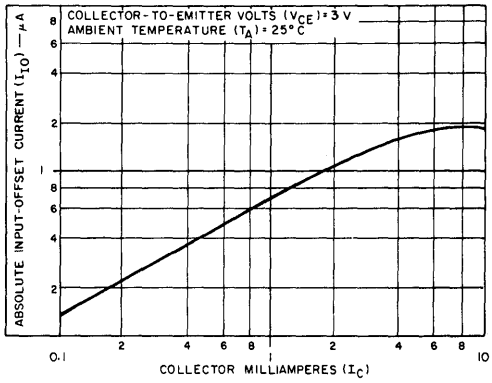


Fig.8 – I_{IO} vs I_C (transistors Q1 and Q2 as a differential amplifier).

May 1990

General-Purpose N-P-N Transistor Array

Three Isolated Transistors and One Differentially - Connected Transistor Pair
For Low-Power Applications from DC to 120 MHz

Applications:

- *General-purpose use in signal processing systems operating in the DC to 190-MHz range*
- *Temperature compensated amplifiers*
- *See Application Note, ICAN-5296 "Application of the CA3018 Integrated-Circuit Transistor Array"' for suggested applications.*

The CA3086 consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair.

The transistors of the CA3086 are well suited to a wide variety of applications in low-power systems at frequencies from DC to 120 MHz. They may be used as discrete transistors in conventional circuits. However, they also provide the very significant inherent advantages unique to integrated circuits, such as compactness, ease of physical handling and thermal matching.

The CA3086 is supplied in a 14-lead dual-in-line plastic package. The CA3086F is supplied in a 14-lead dual-in-line hermetic (frit-seal) ceramic package. The CA3086M is supplied in a 14-lead Small Outline package.

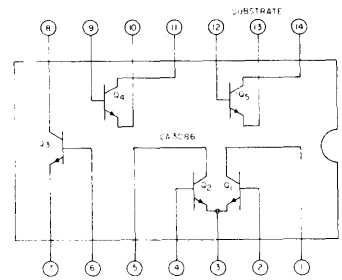


Figure 1 - Functional diagram of the CA3086.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

DISSIPATION:
- Any one transistor ..... 300 mW
- Total package up to T_A = 55°C ..... 750 mW
- Above T_A = 55°C ..... Derate linearly 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating ..... -55 to +125 °C
- Storage ..... -65 to +150 °C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ±1/32 inch (1.59 ± 0.79 mm)
- From case for 10 seconds max ..... +265°C

The following ratings apply for each transistor in the device:

COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO} ..... 15 V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO} ..... 20 V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}* 20V
EMITTER-TO-BASE VOLTAGE, V_{EBO} ..... 5 V
COLLECTOR CURRENT, I_C ..... 50 mA

*The collector of each transistor in the CA3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action. To avoid undesirable coupling between transistors, the substrate (terminal 13) should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTICS	SYMBOLS	TEST CONDITIONS		LIMITS			UNITS
			Typ. Characteristic Curves Fig. No.	Min.	Typ.	Max.	
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	–	20	60	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	–	15	24	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_C = 10 μA, I_{CI} = 0	–	20	60	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	–	5	7	–	V
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	2	–	0.002	100	nA
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	3	—	See Curve	5	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3V, I_C = 1mA	4	40	100	–	

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

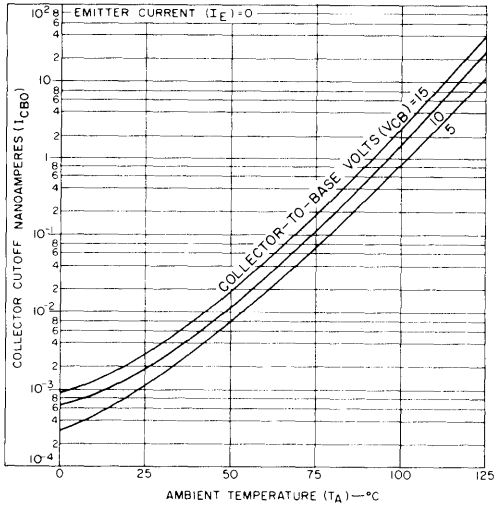


Fig.2 – I_{CBO} vs T_A.

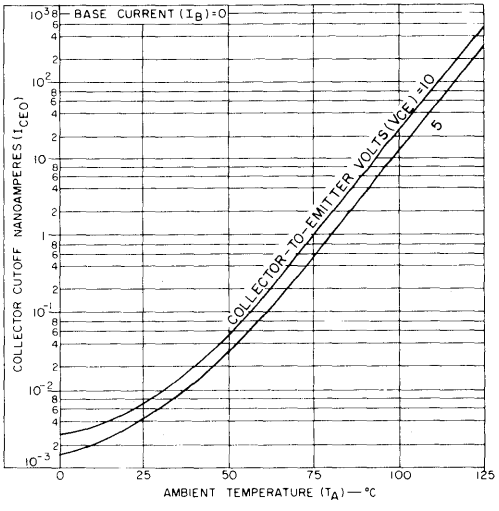


Fig.3 – I_{CEO} vs T_A.

ELECTRICAL CHARACTERISTICS at T_A = 25°C
Typical Values Intended Only for Design Guidance

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		Typ. Characteristics Curves Fig. No.	TYPICAL VALUES	UNITS
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE} = 3 V	I_C = 10 mA	4	100	
			I_C = 10 μA	4	54	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3 V	I_E = 1 mA	5	0.715	V
			I_E = 10 mA	5	0.800	V
V_{BE} Temperature Coefficient	$\Delta V_{BE}/\Delta T$	V_{CE} = 3V, I_C = 1mA		6	−1.9	mV/°C
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_B = 1mA, I_C = 10mA		–	0.23	V
Noise Figure (low frequency)	NF	f = 1kHz, V_{CE} = 3V, I_C = 100μA, R_S = 1k Ω		–	3.25	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:						
Forward Current-Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 3V, I_C = 1mA		7	100	–
Short-Circuit Input Impedance	h_{ie}			7	3.5	kΩ
Open-Circuit Output Impedance	h_{oe}			7	15.6	μmho
Open-Circuit Reverse-Voltage Transfer Ratio	h_{re}			7	1.8×10^{-4}	–
Admittance Characteristics:						
Forward Transfer Admittance	y_{fe}	f = 1MHz, V_{CE} = 3V, I_C = 1mA		8	31 − j1.5	mmho
Input Admittance	y_{ie}			9	0.3 + j0.04	mmho
Output Admittance	y_{oe}			10	0.001 + j0.03	mmho
Reverse Transfer Admittance	y_{re}			11	See Curve	–
Gain-Bandwidth Product	f_T	V_{CE} = 3V, I_C = 3mA		12	550	MHz
Emitter-to-Base Capacitance	C_{EBO}	V_{EB} = 3V, I_E = 0		–	0.6	pF
Collector-to-Base Capacitance	C_{CBO}	V_{CB} = 3V, I_C = 0		–	0.58	pF
Collector-to-Substrate Capacitance	C_{CIO}	V_{CI} = 3V, I_C = 0		—	2.8	pF

TYPICAL STATIC CHARACTERISTICS FOR EACH TRANSISTOR

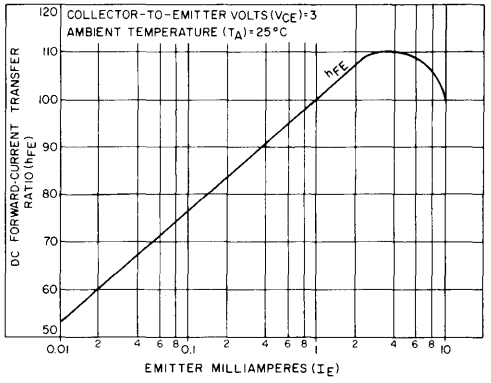


Fig.4 – h_{FE} vs I_E.

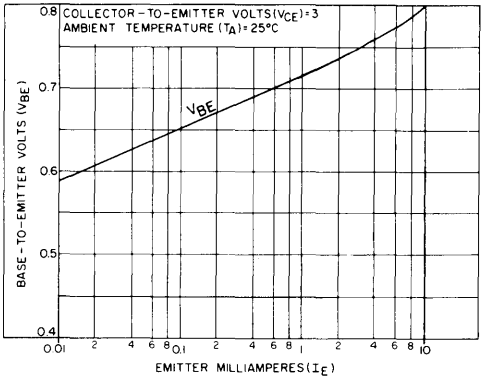


Fig.5 – V_{BE} vs I_E.

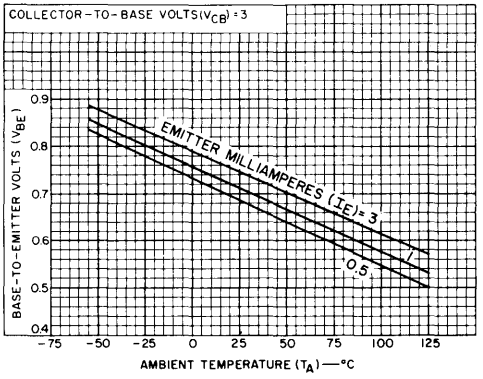


Fig.6 – V_{BE} vs T_A.

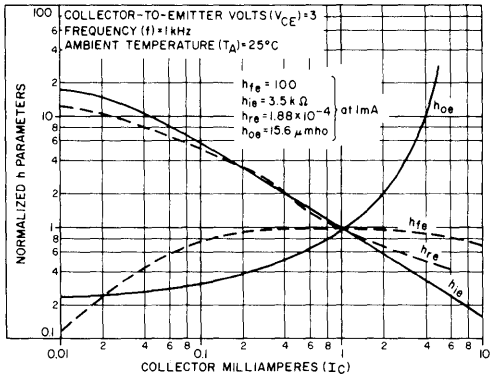


Fig.7 – Normalized h_{fe}, h_{ie}, h_{oe}, h_{re} vs I_C.

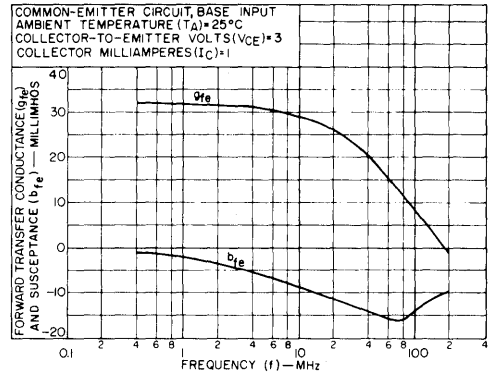


Fig.8 – y_{fe} vs f.

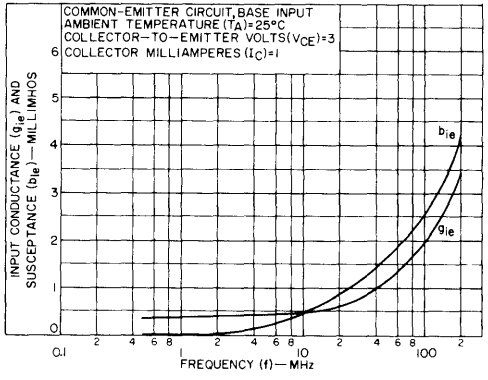


Fig.9 – y_{ie} vs f.

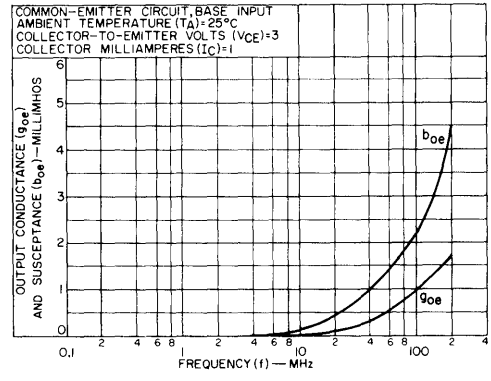


Fig.10 – y_{oe} vs f.

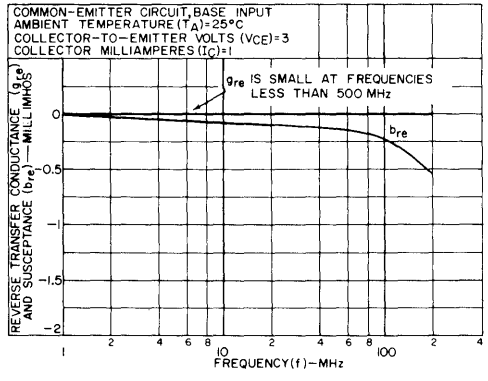


Fig.11 – y_{re} vs f.

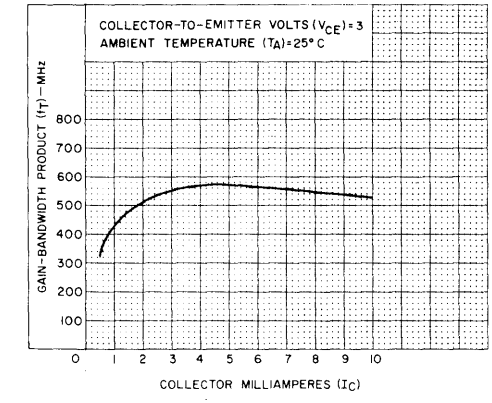


Fig.12 – f_T vs I_C.

May 1990

N-P-N/P-N-P Transistor Array

Five-Independent Transistors: Three n-p-n and Two p-n-p

Applications:

- *Differential Amplifiers*
- *DC Amplifiers*
- *Sense Amplifiers*
- *Level Shifters*
- *Timers*
- *Lamp and Relay Drivers*
- *Thyristor Firing Circuits*
- *Temperature-Compensated Amplifiers*
- *Operational Amplifiers*

The CA3096CE, CA3096E, and CA3096AE are general purpose high-voltage silicon transistor arrays. Each array consists of five independent transistors (two p-n-p and three n-p-n types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096AE, CA3096E, and CA3096CE are identical, except that the CA3096AE specifications include parameter matching and greater stringency in I_{CBO}, I_{CEO}, and $V_{CE(SAT)}$. The CA3096CE is a relaxed version of the CA3096E.

The CA3096CE, CA3096E, and CA3096AE are supplied in 16-lead dual-in-line plastic packages (E-suffix), and in 16-lead Small Outline packages (M suffix). The CA3096 is also available in chip form (H suffix).

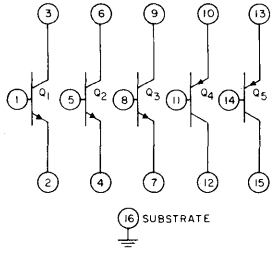


Figure 1 - Schematic Diagram.

CA3096AE, CA3096E, CA3096CE ESSENTIAL DIFFERENCES

CHARACTERISTIC		CA3096AE	CA3096E	CA3096CE
$V_{(BR)CEO}$ (V) Min.	n-p-n	35	35	24
	p-n-p	-40	-40	-24
$V_{(BR)CBO}$ (V) Min.	n-p-n	45	45	30
	p-n-p	-40	-40	-24
h_{FE} @ 1 mA	n-p-n	150-500	150-500	100-670
	p-n-p	20-150	20-150	15-200
h_{FE} @ 100 μA	p-n-p	40-200	40-200	30-300
I_{CBO} (nA) Max.	n-p-n	40	100	100
	p-n-p	-40	-100	-100
I_{CEO} (nA) Max.	n-p-n	100	1000	1000
	p-n-p	-100	-1000	-1000
$V_{CE(SAT)}$ (V) Max.	p-n-p	0.5	0.7	0.7
$\lvert V_{IO} \rvert$ (mV) Max.	n-p-n	5	-	-
	p-n-p	5	-	-
$\lvert I_{IO} \rvert$ (μA) Max.	n-p-n	0.6	-	-
	p-n-p	0.25	-	-

7 ARRAYS

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	EACH N-P-N	EACH P-N-P	
COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO}:			
CA3096AE, CA3096E	35	−40	V
CA3096CE	24	−24	V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO}:			
CA3096AE, CA3096E	45	−40	V
CA3096CE	30	−24	V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}:			
CA3096AE, CA3096E	45	–	V
CA3096CE	30	–	V
EMITTER-TO-SUBSTRATE VOLTAGE, V_{EIO}:			
CA3096AE, CA3096E	–	−40	V
CA3096CE	–	−24	V
EMITTER-TO-BASE VOLTAGE, V_{EBO}:			
CA3096E, CA3096E	6	−40	V
CA3096CE	6	−24	V
COLLECTOR CURRENT, I_C (All Types)	50	−10	mA
POWER DISSIPATION, P_D:			
Up to T_A = 55°C:			
Device (Total)	750		mW
Each Transistor	200		mW
Above T_A = 55°C derate linearly at	6.67		mW/°C
AMBIENT-TEMPERATURE RANGE, T_A:			
Operating	−55 to +125°C		
Storage	−65 to +150°C		
LEAD TEMPERATURE (DURING SOLDERING):			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	265°C		

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096AE			CA3096E			CA3096CE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each n-p-n Transistor											
I_{CBO}	V_{CB} = 10 V, I_E = 0	–	0.001	40	–	0.001	100	–	0.001	100	nA
I_{CEO}	V_{CE} = 10 V, I_B = 0	–	0.006	100	–	0.006	1000	–	0.006	1000	nA
$V_{(BR)CEO}$	I_C = 1 mA, I_B = 0	35	50	–	35	50	–	24	35	–	V
$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0	45	100	–	45	100	–	30	80	–	V
$V_{(BR)CIO}$	I_{CI} = 10 μA, $I_B = I_E$ = 0	45	100	–	45	100	–	30	80	–	V
$V_{(BR)EBO}$	I_E = 10 μA, I_C = 0	6	8	–	6	8	–	6	8	–	V
V_Z	I_Z = 10 μA	6	7.9	9.8	6	7.9	9.8	6	7.9	9.8	V
$V_{CE(SAT)}$	I_C = 10 mA, I_B = 1 mA	–	0.24	0.5	–	0.24	0.7	–	0.24	0.7	V
V_{BE}	I_C = 1 mA, V_{CE} = 5 V	0.6	0.69	0.78	0.6	0.69	0.78	0.6	0.69	0.78	V
h_{FE}		150	390	500	150	390	500	100	390	670	
$\lvert\Delta V_{BE}/\Delta T\rvert$	I_C = 1 mA, V_{CE} = 5 V	–	1.9	–	–	1.9	–	–	1.9	–	mV/°C

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ (Cont'd)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS									UNITS
		CA3096AE			CA3096E			CA3096CE			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each p-n-p Transistor											
I_{CBO}	$V_{CB} = -10$ V, $I_E = 0$	–	−0.006	−40	–	−0.06	−100	–	−0.06	−100	nA
I_{CEO}	$V_{CE} = -10$V, $I_B = 0$	–	−0.12	−100	–	−0.12	−1000	–	−0.12	−1000	nA
$V_{(BR)CEO}$	$I_C = -100\,\mu$A, $I_B = 0$	−40	−75	–	−40	−75	–	−24	−30	–	V
$V_{(BR)CBO}$	$I_C = -10\,\mu$A, $I_E = 0$	−40	−80	–	−40	−80	–	−24	−60	–	V
$V_{(BR)EBO}$	$I_E = -10\,\mu$A, $I_C = 0$	−40	−100	–	−40	−100	–	−24	−80	–	V
$V_{(BR)EIO}$	$I_{EI} = 10\,\mu$A, $I_B = I_C = 0$	−40	−100	–	−40	−100	–	−24	−80	–	V
$V_{CE(SAT)}$	$I_C = -1$ mA, $I_B = -100\,\mu$A	–	−0.16	−0.4	–	−0.16	−0.4	–	−0.16	−0.4	V
V_{BE}	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	−0.5	−0.6	−0.7	−0.5	−0.6	−0.7	−0.5	−0.6	−0.7	V
h_{FE}	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	40	85	250	40	85	250	30	85	300	
	$I_C = -1$ mA, $V_{CE} = -5$ V	20	47	200	20	47	200	15	47	200	
$\lvert\Delta V_{BE}/\Delta T\rvert$	$I_C = -100\,\mu$A, $V_{CE} = -5$ V	–	2.2	–	–	2.2	–	–	2.2	–	mV/°C

I_{CBO} Collector-Cutoff Current

I_{CEO} Collector-Cutoff Current

$V_{(BR)CEO}$ Collector-to-Emitter Breakdown Voltage

$V_{(BR)CBO}$ Collector-to-Base Breakdown Voltage

$V_{(BR)CIO}$ Collector-to-Substrate Breakdown Voltage

$V_{(BR)EBO}$ Emitter-to-Base Breakdown Voltage

V_Z Emitter-to-Base Zener Voltage

$V_{CE(SAT)}$ Collector-to-Emitter Saturation Voltage

V_{BE} Base-to-Emitter Voltage

h_{FE} DC Forward-Current Transfer Ratio

$\lvert\Delta V_{BE}/\Delta T\rvert$ Magnitude of Temperature Coefficient: (for each transistor)

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (CA3096AE Only)
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS	LIMITS CA3096AE			UNITS
		Min.	Typ.	Max.	
For Transistors Q1 and Q2 (as a Differential Amplifier)					
Absolute Input Offset Voltage, $\lvert V_{IO}\rvert$	V_{CE} = 5 V, I_C = 1 mA	–	0.3	5	mV
Absolute Input Offset Current, $\lvert I_{IO}\rvert$		–	0.07	0.6	μA
Absolute Input Offset Voltage Temperature Coefficient, $\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		–	1.1	–	μV/°C
For Transistors Q4 and Q5 (As a Differential Amplifier)					
Absolute Input Offset Voltage, $\lvert V_{IO}\rvert$	V_{CE} = −5 V, I_C = −100 μA, R_S = 0	–	0.15	5	mV
Absolute Input Offset Current, $\lvert I_{IO}\rvert$		–	2	250	nA
Absolute Input Offset Voltage Temperature Coefficient, $\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$		–	0.54	–	μV/°C

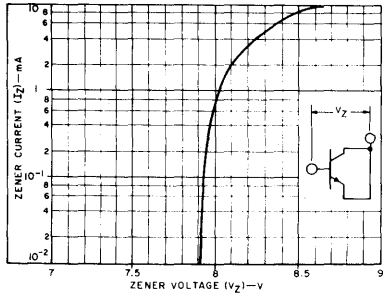


Fig. 1 – Base-to-emitter zener characteristic (n-p-n).

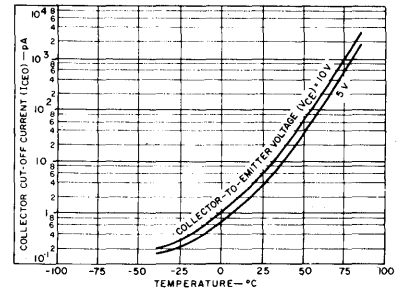


Fig. 2 – Collector cut-off current (I_{CEO}) as a function of temperature (n-p-n).

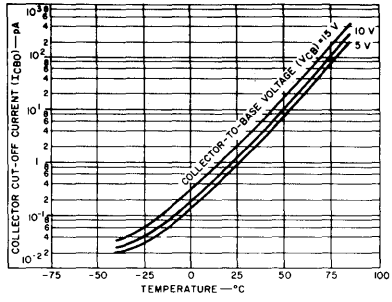


Fig. 3 – Collector cut-off current (I_{CBO}) as a function of temperature (n-p-n).

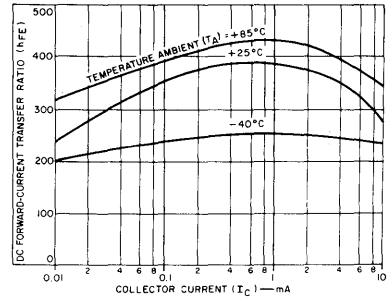


Fig. 4 – Transistor (n-p-n) h_{FE} as a function of collector current.

DYNAMIC

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

Typical Values Intended Only for Design Guidance

CHARACTERISTICS	TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each n-p-n Transistor			
Noise Figure (low frequency), NF	f = 1 kHz, V_{CE} = 5 V, I_C = 1 mA, R_S = 1 kΩ	2.2	dB
Low-Frequency, Input Resistance, R_i	f = 1.0 kHz, V_{CE} = 5 V, I_C = 1 mA	10	kΩ
Low-Frequency Output Resistance, R_o		80	kΩ
Admittance Characteristics:			
Forward Transfer Admittance, $\frac{g_{fe}}{Y_{fe}\ b_{fe}}$	f = 1 MHz, V_{CE} = 5 V, I_C = 1 mA	7.5 −j13	mmho
Input Admittance, $\frac{g_{ie}}{Y_{ie}\ b_{ie}}$		2.2 j3.1	mmho
Output Admittance, $\frac{g_{oe}}{Y_{oe}\ b_{oe}}$		0.76 j2.4	mmho
Gain-Bandwidth Product, f_T	V_{CE} = 5 V, I_C = 1.0 mA	280	MHz
	V_{CE} = 5 V, I_C = 5 mA	335	
Emitter-to-Base Capacitance, C_{EB}	V_{EB} = 3 V	0.75	pF
Collector-to-Base Capacitance, C_{CB}	V_{CB} = 3 V	0.46	pF
Collector-to-Substrate Capacitance, C_{CI}	V_{CI} = 3 V	3.2	pF
For Each p-n-p Transistor			
Noise Figure (low frequency), NF	f = 1 kHz, I_C = 100 μA, R_S = 1 kΩ	3	dB
Low-Frequency Input Resistance, R_i	f = 1 kHz, V_{CE} = 5 V, I_C = 100 μA	27	kΩ
Low-Frequency Output Resistance, R_o		680	kΩ
Gain-Bandwidth Product, f_T	V_{CE} = 5 V, I_C = 100 μA	6.8	MHz
Emitter-to-Base Capacitance, C_{EB}	V_{EB} = −3 V	0.85	pF
Collector-to-Base Capacitance, C_{CB}	V_{CB} = −3 V	2.25	pF
Base-to-Substrate Capacitance, C_{BI}	V_{BI} = 3 V	3.05	pF

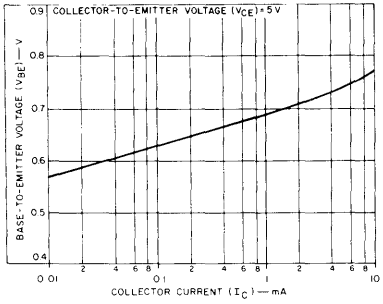


Fig. 5 – V_{BE} (n-p-n) as a function of collector current.

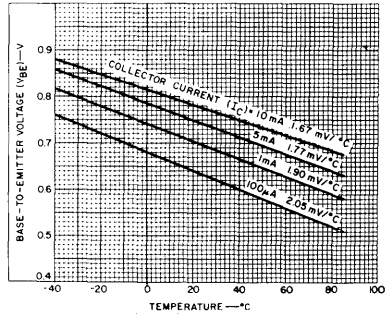


Fig. 6 – V_{BE} (n-p-n) as a function of temperature.

7 ARRAYS

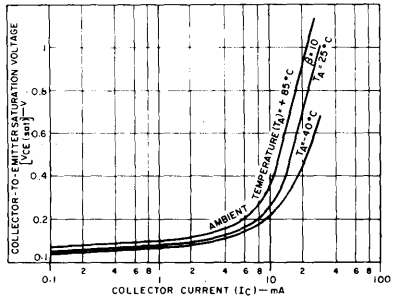


Fig. 7 – $V_{CE}(SAT)$ (n-p-n) as a function of collector current.

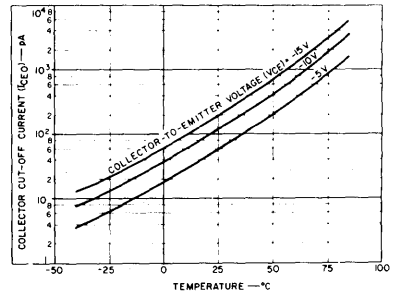


Fig. 8 – Collector cut-off current (I_{CEO}) as a function of temperature (p-n-p).

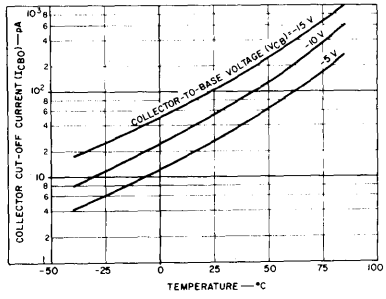


Fig. 9 – Collector cut-off current (I_{CBO}) as a function of temperature (p-n-p).

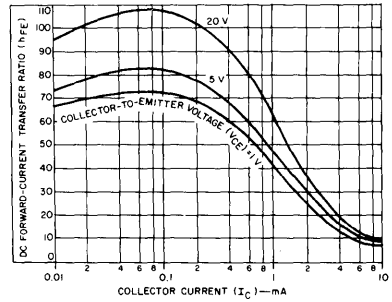


Fig. 10 – Transistor (p-n-p) h_{FE} as a function of collector current.

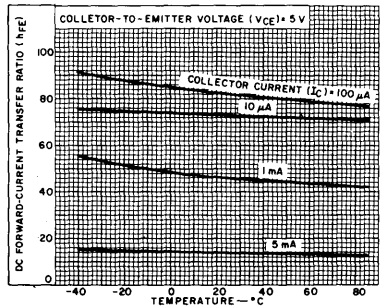


Fig. 11 – Transistor (p-n-p) h_{FE} as a function of temperature.

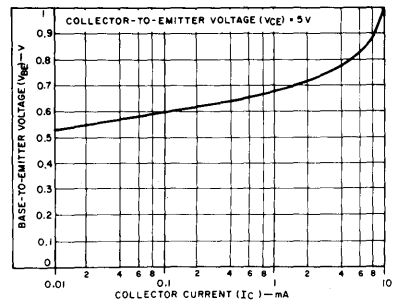


Fig. 12 – V_{BE} (p-n-p) as a function of collector current.

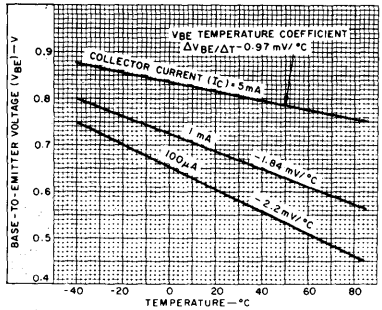


Fig. 13 – V_{BE} (p-n-p) as a function of temperature.

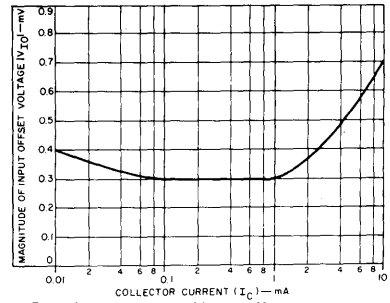


Fig. 14 – Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for n-p-n transistor Q_1–Q_2.

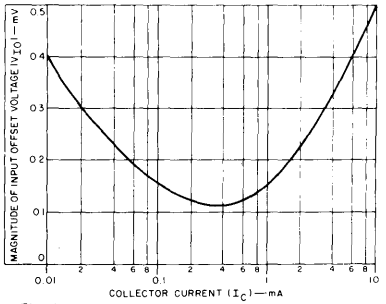


Fig. 15 – Magnitude of input offset voltage $|V_{IO}|$ as a function of collector current for p-n-p transistor Q_4–Q_5

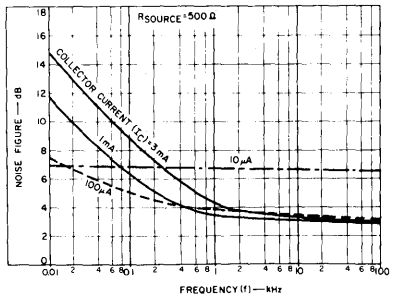


Fig. 16 – Noise figure as a function of frequency for n-p-n transistors.

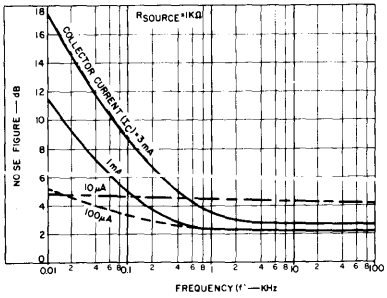


Fig. 17 – Noise figure as a function of frequency for n-p-n transistors.

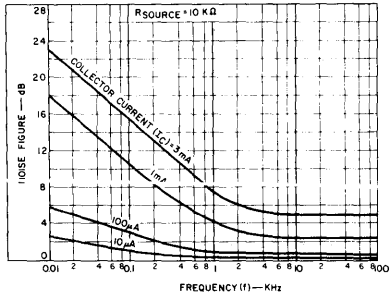


Fig. 18 – Noise as a function of frequency for n-p-n transistors.

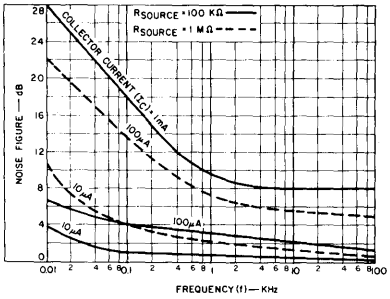


Fig. 19 – Noise figure as a function of frequency for n-p-n transistors.

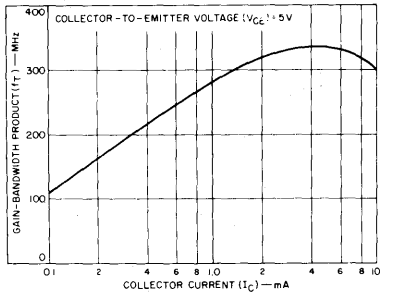


Fig. 20 – Gain-bandwidth product as a function of collector current (n-p-n).

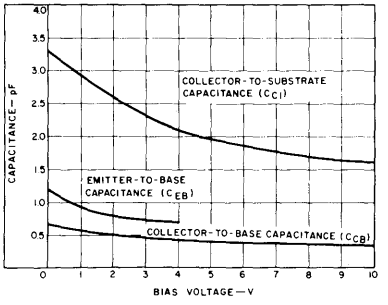


Fig. 21 – Capacitance as a function of bias voltage (n-p-n).

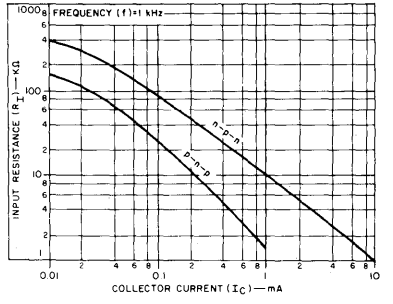


Fig. 22 – Input resistance as a function of collector current.

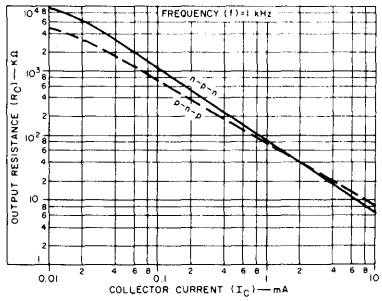


Fig. 23 – Output resistance as a function of collector current.

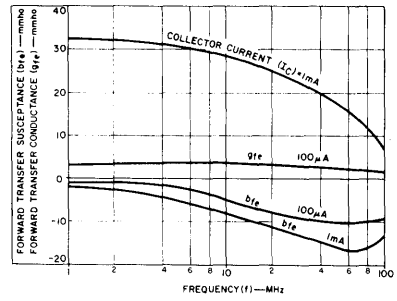


Fig. 24 – Forward transconductance as a function of frequency.

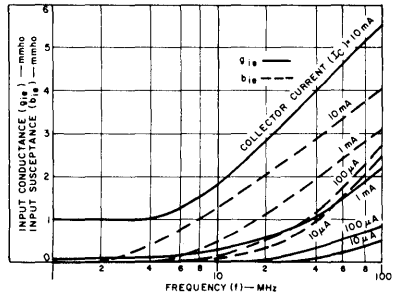


Fig. 25 – Input admittance as a function of frequency.

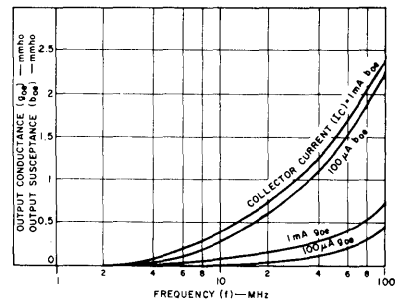


Fig. 26 – Output admittance as a function of frequency.

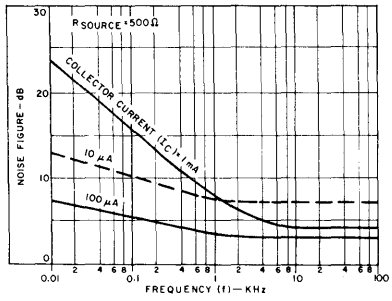


Fig. 27 – Noise figure as a function of frequency (p-n-p).

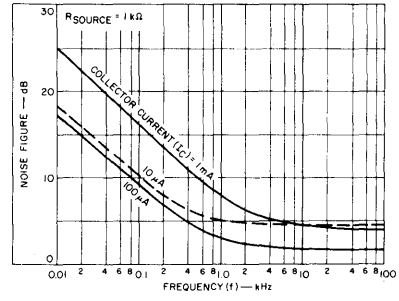


Fig. 28 – Noise figure as a function of frequency (p-n-p).

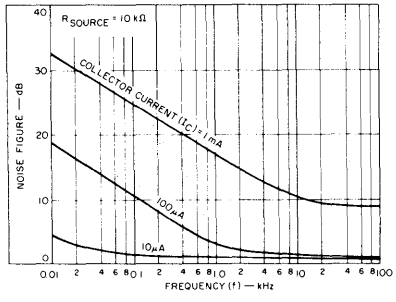


Fig. 29 – Noise figure as a function of frequency (p-n-p).

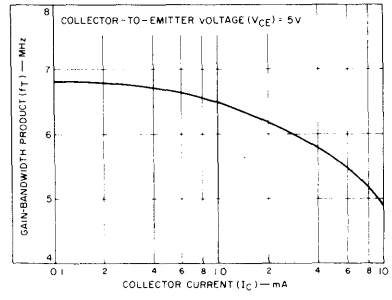


Fig. 30 – Gain-bandwidth product as a function of collector current (p-n-p).

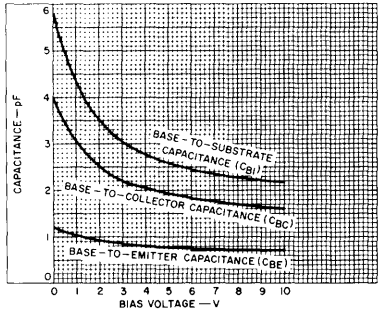


Fig. 31 – Capacitance as a function of bias voltage (p-n-p).

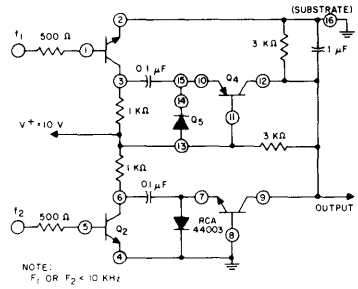


Fig. 32 – Frequency comparator using CA3096E.

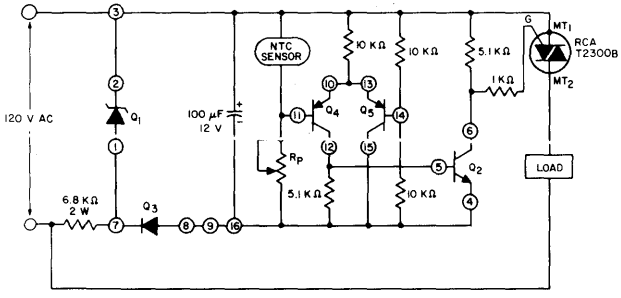


Fig. 33 – Line-operated level switch using CA3096AE or CA3096E.

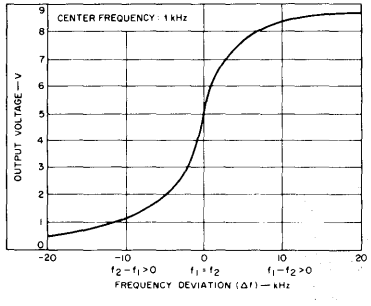


Fig. 34 – Frequency comparator characteristics.

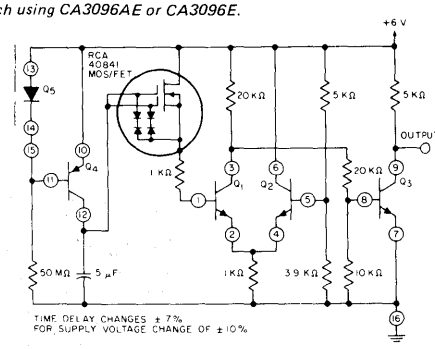


Fig. 35 – One-minute timer using CA3096AE and a MOS/FET.

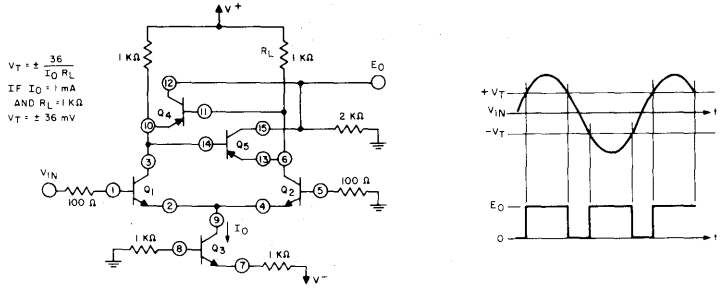


Fig. 36 – CA3096AE small-signal zero-voltage detector having noise immunity.

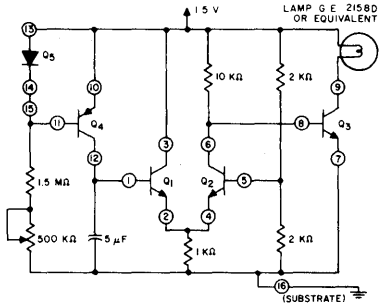


Fig. 37 — Ten-second timer operated form 1.5-volt supply using CA3096E.

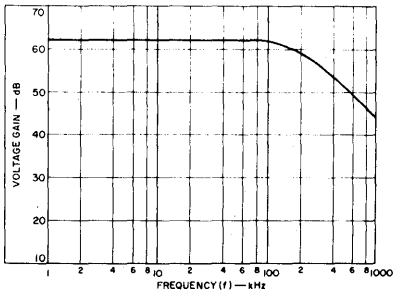


Fig. 38 — Gain-frequency characteristics.

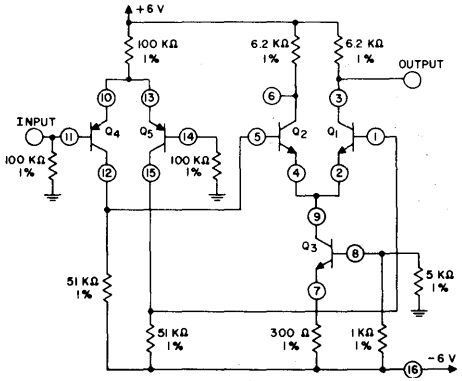
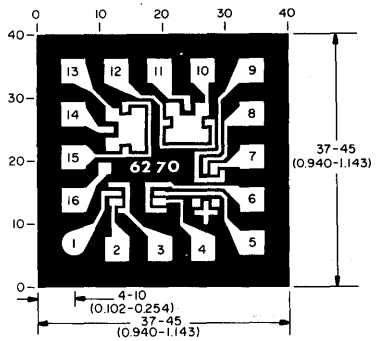


Fig. 39 — Cascade of differential amplifiers using CA3096AE.

Features:

1. Can be operated with either dual supply or single supply.
2. Wide-input common-mode range +5 V to −5 V.
3. Low bias current: $<1\ \mu A$.



CA3096H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

May 1990

Thyristor/Transistor Array

For Military, Commercial, and Industrial Applications

Features:

- *Complete isolation between elements*
- *n-p-n transistor - V_{CEO} = 30 V (min), I_C = 100 mA (max.)*
- *p-n-p/n-p-n transistor pair - beta ≥ 8000 (typ.) @ I_C = 10 mA individual p-n-p, n-p-n, or transistor pair operation*
- *Programmable unijunction transistor (PUT) - peak-point current = 15 nA (typ.) at R_G = 1 MΩ; V_{AK} = ±30 V*
- *(PUT) Extremely long RC time constants with low value of external capacitor*
- *Sensitive-gate silicon controlled rectifier (SCR) - 150 mA forward current (max.)*
- *Zener-diode impedance (Z_Z) = 15 Ω (typ.) at 10 mA*

Applications:

- *Timers*
- *Light dimmers/motor controls*
- *Oscillators*
- *"One-shot" multivibrators*
- *Voltage regulators*
- *Comparators, Schmitt triggers*
- *Constant-current sources*
- *Amplifiers*
- *Logic circuits*
- *SCR triggering*
- *Pulse circuits*

The CA3097E* Thyristor/Transistor Array is a monolithic integrated circuit that enables circuit designers to further integrate control systems. The CA3097E consists of five independent and completely isolated elements on one chip: an n-p-n transistor, a p-n-p/n-p-n transistor pair, a zener diode, a programmable unijunction transistor (PUT), and a sensitive-gate silicon controlled rectifier (SCR).

The CA3097 is supplied in either the 16-lead dual-in-line plastic package ("E" suffix) or the chip version ("H" suffix), and operates over the full military-temperature range of -55°C to +125°C.

*Formerly Dev. No. TA6281.

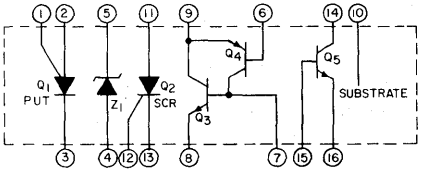


Figure 1 - Schematic diagram of CA3097E.

7 ARRAYS

File Number **633**

MAXIMUM RATINGS, *Absolute-Maximum Values at $T_A = 25^oC$*

Isolation Voltage, any terminal to substrate*	+50 V
Dissipation, Total Package:	
Up to $T_A = 55^oC$	750 mW
Above $T_A = 55^oC$	derate linearly at 6.67 mW/°C
Ambient Temperature Range:	
Operating	−55 to +125°C
Storage	−65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max.	+265 °C
Each n-p-n Transistor (Q3,Q5)	
The following ratings apply with terminals 6 & 9 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	30 V
Collector-to-Base Voltage (V_{CBO})	50 V
Emitter-to-Base Voltage (V_{EBO})	5 V
Collector Current (I_C)	100 mA
Base Current (I_B)	20 mA
Dissipation (P_D)	500 mW
p-n-p Transistor (Q4)	
The following ratings apply with terminals 7 & 8 connected together.	
Collector-to-Emitter Voltage (V_{CEO})	−40 V
Collector-to-Base Voltage (V_{CBO})	−50 V
Emitter-to-Base Voltage (V_{EBO})	−40 V
Collector Current (I_C)	−10 mA
Base Current (I_B)	−3 mA
Dissipation (P_D)	200 mW
p-n-p/n-p-n Transistor Pair (Q3,Q4)	
Dissipation (P_D)	500 mW
Programmable Unijunction Transistor, PUT (Q1)	
Gate-to-Cathode Positive Voltage (V_{GK})	30 V
Gate-to-Cathode Negative Voltage (V_{GKR})	5 V
Gate-to-Anode Negative Voltage (V_{GA})	30 V
Anode-to-Cathode Voltage (V_{AK})	±30 V
DC Anode Current	150 mA
Peak Anode Non-Recurrent Forward (On-State) Current (10 μs pulse)	2 A
Total Average Dissipation	300 mW
Silicon Controlled Rectifier, SCR (Q2)	
Repetitive Peak Reverse Voltage (V_{RRXM}), R_{GK} = 1 KΩ	30 V
Repetitive Peak Off-State Voltage (V_{DRXM}), R_{GK} = 1 kΩ	30 V
DC On-State Current (I_{TDC})	150 mA
Peak Surge (Non-Repetitive) On-State Current (10 μs pulse)	2 A
Forward Peak Gate Current (I_{GFM})	20 mA
Peak Gate-to-Cathode Reverse Voltage (V_{GRM})	5 V
Total Average Dissipation	300 mW
Zener Diode, (Z1)	
DC Current (I_Z)	25 mA
Dissipation (P_D)	250 mW

* One or more of the terminals of each element of the CA3097E is isolated from the substrate by a junction diode. In order to maintain electrical isolation between elements, the substrate terminal must be connected to a voltage which is no more positive than that of any other terminal. To avoid undesirable coupling between elements, the substrate terminal (terminal 10) should be maintained at either dc or signal (ac) ground.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
n-p-n TRANSISTORS Q3, Q5 (TERMINALS 6 and 9 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = 10 V, I_E = 0		–	–	1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = 10 V, I_B = 0		–	–	10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = 100μA, I_B = 0		30	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = 100μA, I_E = 0		50	–	–	V
COLLECTOR-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)CIO}$	I_{CI} = 100μA, I_B = 0, I_E = 0		50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = 100μA, I_C = 0		5	7.5	10	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE}(SAT)$	I_C = 50mA, I_B = 5mA	5	–	–	0.65	V
		I_C = 10mA, I_B = 1 mA		–	0.10	–	
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE}(SAT)$	I_C = 10mA, I_B = 1mA	2	–	0.76	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = 3V, I_C = 10mA	3	0.65	0.73	0.85	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = 3V, I_C = 10mA	4	100	130	–	
		V_{CE} = 3V, I_C = 50mA		80	120	–	
p-n-p TRANSISTOR Q4 (TERMINALS 7 and 8 CONNECTED)							
COLLECTOR CUTOFF CURRENT	I_{CBO}	V_{CB} = -10 V, I_E = 0		–	–	–1	μA
COLLECTOR CUTOFF CURRENT	I_{CEO}	V_{CE} = -10 V, I_B = 0		–	–	–10	μA
COLLECTOR-TO-EMITTER BREAKDOWN VOLTAGE	$V_{(BR)CEO}$	I_C = -100μA, I_B = 0		–40	–	–	V
COLLECTOR-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)CBO}$	I_C = -10μA, I_E = 0		–50	–	–	V
EMITTER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)EIO}$	I_{EI} = 10μA, I_B = 0, I_E = 0		–50	–	–	V
EMITTER-TO-BASE BREAKDOWN VOLTAGE	$V_{(BR)EBO}$	I_E = –10μA, I_C = 0		–40	–	–	V
COLLECTOR-TO-EMITTER SATURATION VOLTAGE	$V_{CE}(SAT)$	I_C = -1mA, I_B = -100μA	6	–	–	–0.33	V
BASE-TO-EMITTER SATURATION VOLTAGE	$V_{BE}(SAT)$	I_C = -1mA, I_B = –100μA	7	–	–0.7	–	V
BASE-TO-EMITTER VOLTAGE	V_{BE}	V_{CE} = -3 V, I_C = –100μA	8	–0.5	–0.6	–0.7	V
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} = – 3 V, I_C = –100μA	9	30	60	–	
		V_{CE} = –3 V, I_C = –1 mA		40	–	–	
n-p-n/p-n-p TRANSISTOR PAIR Q3, Q4							
DC FORWARD-CURRENT TRANSFER RATIO	h_{FE}	V_{CE} (n-p-n) = 3V, I_C = 10mA	10	–	8000	–	
		V_{CE} (n-p-n) = 3V, I_C = 50mA	10	–	6500	–	

ELECTRICAL CHARACTERISTICS (Cont'd.)

CHARACTERISTIC	SYMBOL	TEST CONDITIONS Ambient Temperature (T_A) = 25°C Unless Otherwise Specified	FIG. NO.	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
PROGRAMMABLE UNIJUNCTION TRANSISTOR (PUT), Q1							
OFFSET VOLTAGE	V_T*	V_S = 10V, R_G = 10kΩ	11,22[a]	0.2	–	0.7	V
		V_S = 10V, R_G = 1MΩ		0.2	–	0.7	
ANODE-TO-CATHODE ON-STATE VOLTAGE	V_F	I_F = 50mA	12	–	0.90	1.5	V
		I_F = 100mA		–	1	–	
PEAK OUTPUT VOLTAGE	V_{OM}	C = 0.22μF Anode Supply Voltage = 20V	13,23	–	10	–	V
PEAK-POINT CURRENT	I_P	V_S = 10V, R_G = 10kΩ	14,22[a]	–	0.55	1	μA
		V_S = 10V, R_G = 1MΩ	–	–	0.015	0.15	
VALLEY-POINT CURRENT	I_V	V_S = 10V, R_G = 10kΩ	17,15	4	40	–	μA
		V_S = 10V, R_G = 1MΩ	16	–	–	25	
GATE REVERSE CURRENT	I_{GAO}	V_S = 30V	22[c]	–	0.02	–	nA
GATE REVERSE CURRENT	I_{GKS}	Anode-To-Cathode Short, V_S, = 30V	22[d]	–	0.2	–	nA
OUTPUT PULSE RISETIME	t_r	Anode-Supply Voltage = 20V C = 0.22 μF	23	–	60	–	ns
SILICON CONTROLLED RECTIFIER (SCR), Q2							
PEAK OFF-STATE CURRENT: FORWARD	I_{DXM}	V_{DRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	μA
REVERSE	I_{RXM}	V_{RRXM} = 30V, R_{GK} = 1kΩ	24	–	–	2	
FORWARD DC VOLTAGE DROP	V_T	I_T = 50 mA	18	–	0.90	1.5	V
GATE-TO-SOURCE TRIGGER CURRENT	I_{GS}	T_A = 25°C	26	–	33	100	μA
		T_A = −55°C	26	–	50	–	
DC GATE-TRIGGER VOLTAGE	V_{GT}	V_L = 10V, R_L = 100Ω	19	–	0.55	0.75	V
HOLDING CURRENT	I_{HO}	R_{GK} = 1kΩ	20,24	–	1.2	–	mA
CRITICAL RATE-OF-RISE OF OFF-STATE VOLTAGE	dv/dt	EXPONENTIAL RISE, R_{GK} = 1kΩ, V_{DRXM} = 30V	25	–	150	–	V/μs
GATE-CONTROLLED TURN-ON TIME	t_{gt}	See Fig. 33	33	–	50	–	ns
CIRCUIT-COMMUTATED TURN-OFF TIME	t_q	See Fig. 33	33	–	10	–	μs
ZENER DIODE, Z1							
ZENER VOLTAGE	V_Z	I_Z = 10mA	21	7.2	8	8.8	V
ZENER IMPEDANCE	Z_Z	I_Z = 10mA, f = 1kHz		–	15	25	Ω
ZENER VOLTAGE TEMPERATURE COEFFICIENT	$(\Delta V_Z/V_Z)/\Delta T$	I_Z = 10mA		–	+0.05	–	%/°C
	$\Delta V_Z/\Delta T$			–	+4	–	mV/°C
ZENER-TO-SUBSTRATE BREAKDOWN VOLTAGE	$V_{(BR)ZIO}$	I_Z = 100μA TERM. 5 TO SUBSTRATE		50	80	–	V

* $V_T = V_P - V_S$ (Fig. 22)

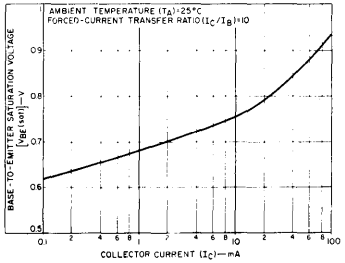


Fig. 2 – Base-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.

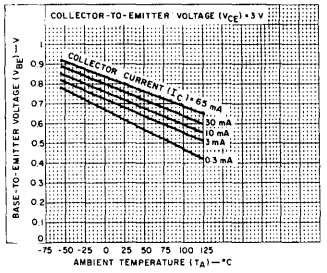


Fig. 3 – Base-to-emitter voltage vs. ambient temperature for n-p-n transistors Q3 & Q5.

TYPICAL CHARACTERISTICS

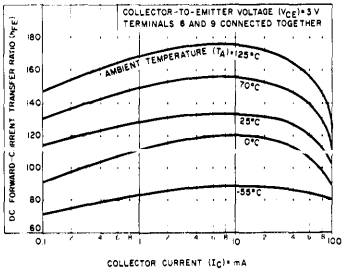


Fig. 4 – DC forward-current transfer ratio vs. collector current for n-p-n transistors Q3 & Q5.

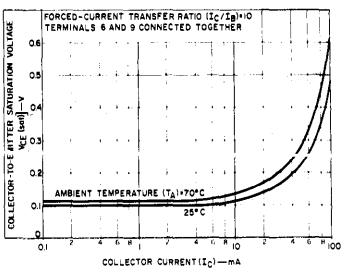


Fig. 5 – Collector-to-emitter saturation voltage vs. collector current for n-p-n transistors Q3 & Q5.

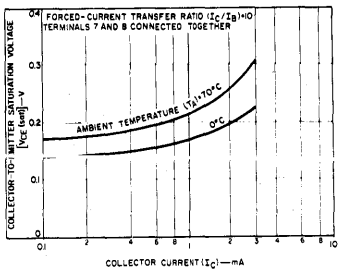


Fig. 6 – Collector-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

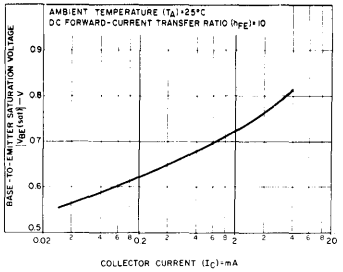


Fig. 7 – Base-to-emitter saturation voltage vs. collector current for p-n-p transistor Q4.

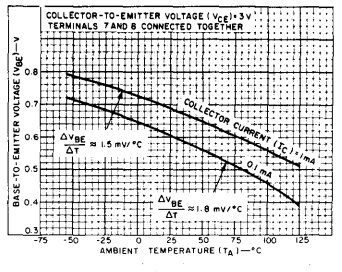


Fig. 8 – Base-to-emitter voltage vs. ambient temperature for p-n-p transistor Q4.

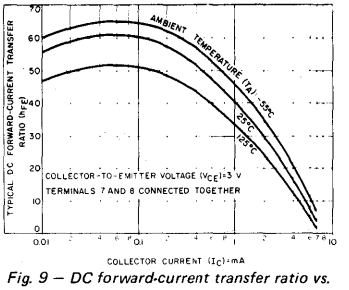


Fig. 9 – DC forward-current transfer ratio vs. collector current for p-n-p transistor Q4.

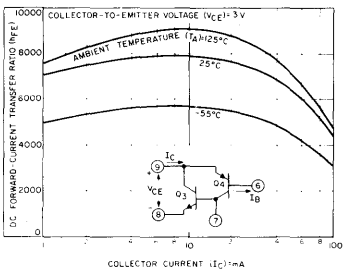


Fig. 10 – DC forward-current transfer ratio vs. collector current for transistor pair Q3, Q4.

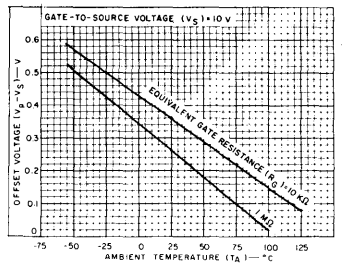


Fig. 11 – Offset voltage vs. ambient temperature for Q1 (PUT).

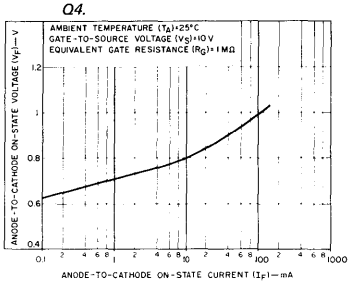


Fig. 12 – Anode-to-cathode on-state voltage vs. anode-to-cathode on-state current for Q1 (PUT).

TYPICAL CHARACTERISTICS (CONT'D)

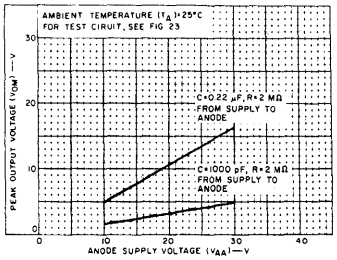


Fig. 13 – Peak output voltage vs. anode supply voltage for Q1 (PUT).

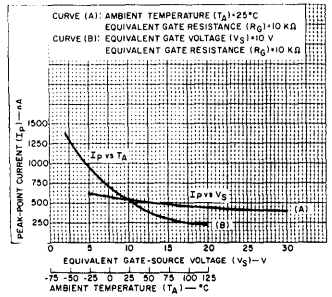


Fig.14 – Peak-point current vs. gate-source voltage and ambient temperature for Q1 (PUT).

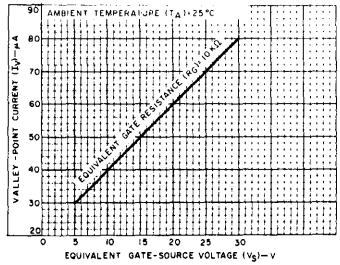


Fig.15 – Valley-point current vs. gate-source voltage for Q1 (PUT).

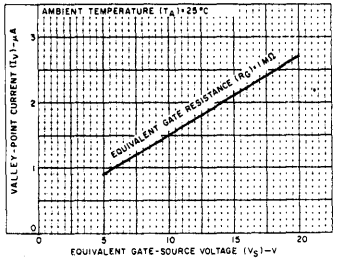


Fig.16 – Valley-point current vs. gate-source voltage for Q1 (PUT).

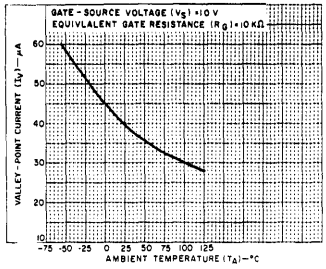


Fig. 17 – Valley-point current vs. ambient temperature for Q1 (PUT).

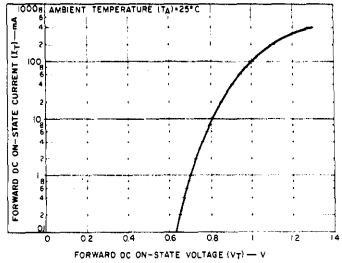


Fig. 18 – Forward DC on-state current vs. on-state voltage for Q2 (SCR).

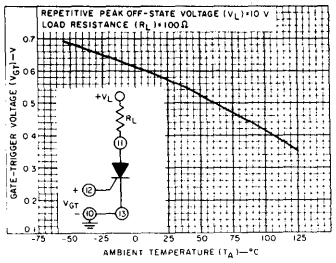


Fig. 19 – Gate-trigger voltage vs. ambient temperature for Q2 (SCR).

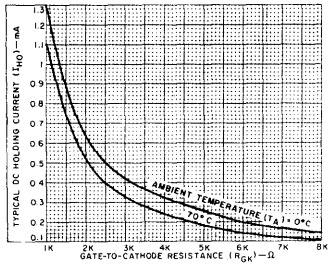


Fig. 20 – Typical DC holding current vs. gate-to-cathode resistance for Q2 (SCR).

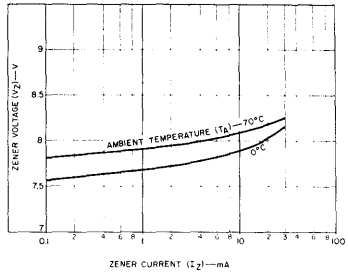


Fig. 21 – Zener voltage vs. zener current for Z1.

OPERATING CONSIDERATIONS FOR CA3097

1. Composite p-n-p/n-p-n Transistors Q3, Q4 (See Fig. 3)

To use Q3 as an individual n-p-n transistor, join terminals no. 6 and no. 9 to disable p-n-p transistor Q4.

The appropriate terminal connections are then:

Collector..... terminal 9
Base ..... terminal 7
Emitter..... terminal 8

To use Q4 as an individual p-n-p transistor, join terminals no. 7 and no. 8 to disable n-p-n transistor Q3.

The appropriate terminal connections are then:

Collector..... terminal 7
Base ..... terminal 6
Emitter..... terminal 9

To use Q3 and Q4 as a composite use terminals 6, 7, 8, and 9 as required.

2. Programmable Unijunction Transistor Q1 (PUT)

The programmable unijunction transistor is essentially an anode-gate SCR. The volt-ampere characteristic of the device is shown in Fig. 22. When an equivalent Thevenin source (V_S, R_G), as shown in Fig. 22, is applied to the gate terminal the device will be "off" if the anode-voltage is negative with respect to the gate voltage. Under this condition, any current flow is exclusively leakage current. When the anode voltage becomes more positive than the gate voltage by an increment equal to the threshold voltage (V_T = 0.4 V typ.), the device can turn "on" only if the current available at the anode terminal **is greater** than the specified peak-point current. The PUT will then switch through its negative-resistance region to the "on" state (low anode-to-gate voltage). It should be noted that I_P is not the maximum current allowed through the device, but is the current required at the peak of the V-I curve. I_P is typically a very low value of current.

After the PUT has switched to its low-impedance state, the device will remain "on" if the anode-current (I_A) exceeds the valley-point current (I_V). If $I_A < I_V$, the PUT will switch back to its high-impedance "off" state. Thus, the PUT can be made to "latch" or recover, depending on I_V. Since I_V is a function of the "on"-state gate current (which depends on R_G and V_S) a choice of R_G and/or V_S will determine the operating mode, i.e., "off" state→"on" state or "off" state → "on" state → "off" state. The value of I_V increases directly as a function of V_G and inversely with R_G. The PUT in the CA3097E has a low i_P.....i_P – 15 nA at V_S – 10 V, R_G = 1 MΩ. This low value of I_P indicates that an extremely large value of anode-supply resistor, e.g. 60 MΩ (typ.), can be used in timing circuits requiring long RC time constants. This becomes important when considering the size of the external

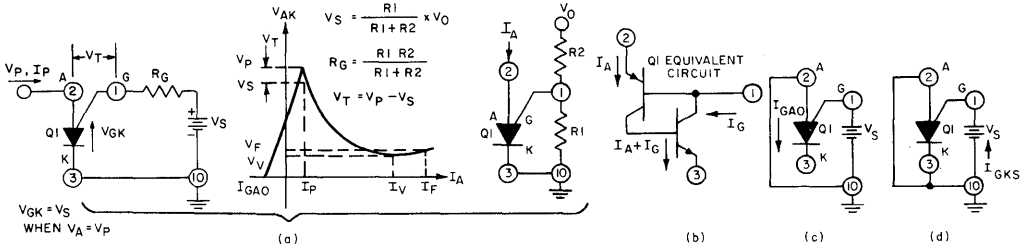


Fig. 22 – General anode characteristics for Q1 (PUT).

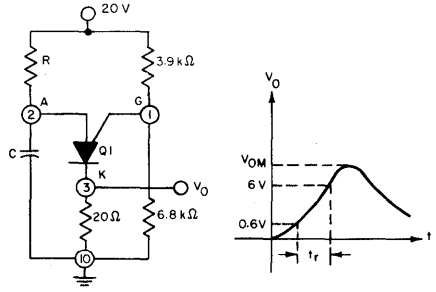


Fig. 23 – Output pulse characteristics for Q1 (PUT).

OPERATING CONSIDERATIONS (CONT'D)

timing capacitor to be used. Consequently, the use of the PUT in the CA3097E is advantageous since it has a lower I_P than most discrete PUT's.

Temperature Compensation of Switching Point

As described previously, the PUT will switch to its low-impedance state when its anode voltage is approximately a diode-drop above the gate voltage. Since the anode-to-gate threshold voltage vs. temperature characteristic is similar to that of a typical silicon-diode junction, a compensating series diode such as used in the circuit of Fig. 29 (Z1 connected as forward-biased diode) considerably reduces the effect of temperature on the switching point.

Bypassing Anode Current

If the PUT gate equivalent source is such that $I_A > I_V$, the PUT will remain "on". A method for turning the PUT off is by shunting current away from the anode until $I_A < I_V$. An example of this technique is the oscillator circuit of Fig. 29. Q3 transistor is turned "on" after the PUT fires and shunts current away from the anode, thereby forcing $I_A < I_V$. The PUT then turns "off" allowing C_T to recharge through R_T, to repeat the cycle.

Protecting The PUT Against Discharge Current Of The Capacitor

A current-limiting resistor in series with the PUT is normally required to dissipate capacitive discharge energy (see Figs. 23 and 29).

Silicon Controlled Rectifier, Q2 (SCR)

The SCR should be used with a 1 kΩ (or less) resistor connected between the cathode and gate terminals if the SCR is to be subjected to its maximum forward and reverse voltage ratings (V_{DXM} and V_{RXM}). Selecting a value for R_{GK} of 1 kΩ (or lower) increases the capability of the device to withstand greater dv/dt and increases the noise immunity of the SCR against false triggering at the gate. Practical considerations such as available current drive from the triggering devices (e.g., a PUT) will determine the lowest value of R_{GK} at which the SCR will fire with a $V_{GK} \approx 0.55$ V. With a value of 500Ω for R_{GK}, the trigger source must be capable of supplying 1.1 mA. R_{GK} should be non-inductive within the frequency band of the noise transients normally encountered in a particular application.

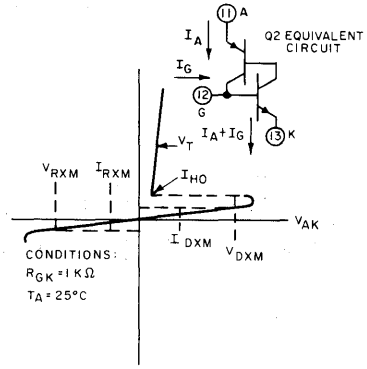


Fig. 24 – Principle voltage-current characteristics for Q2 (SCR).

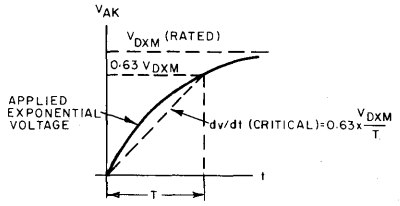
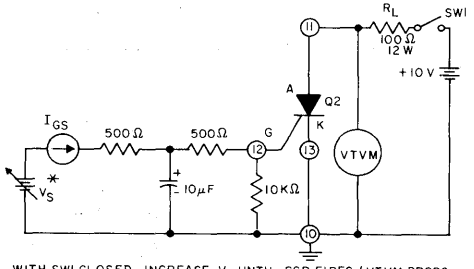


Fig. 25 – Definition of critical rate of rise of off-state voltage for Q2 (SCR).

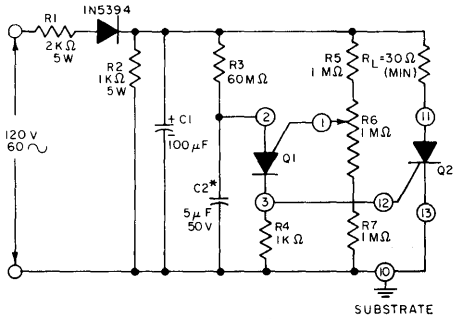


WITH SW1 CLOSED, INCREASE V_S UNTIL SCR FIRES (VTVM DROPS FROM 10V TO APPROXIMATELY 1V). I_{GS} (TRIGGER) IS MEASURED JUST PRIOR TO THIS TRIGGERING POINT. NOTE THAT I_{GS} MAY DECREASE AS V_S IS INCREASED DUE TO CURRENT DRAWN OUT OF THE GATE TERMINAL OF THE SCR AS IT TURNS ON. TO UNLATCH THE SCR OPEN SW1.

* V_S SHOULD BE CAPABLE OF SUPPLYING MILLIVOLT INCREMENTS NEAR THE TRIGGER POINT

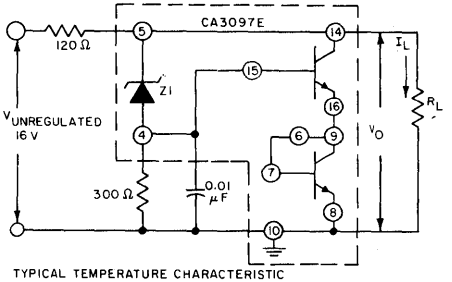
Fig. 26 – Test circuit for determining I_{GS} in Q2 (SCR).

APPLICATIONS CIRCUITS



TIMING PERIOD ≈ 200 SEC. WITH 1 MΩ POT CENTERED
TIMING CYCLE BEGINS WHEN AC IS APPLIED
* SPRAGUE TYPE 4308, 5μF AT 50 V
SPRAGUE TYPE 6308, 5μF AT 50 V
OR EQUIVALENT

Fig. 27 – AC line-operated one-shot timer.



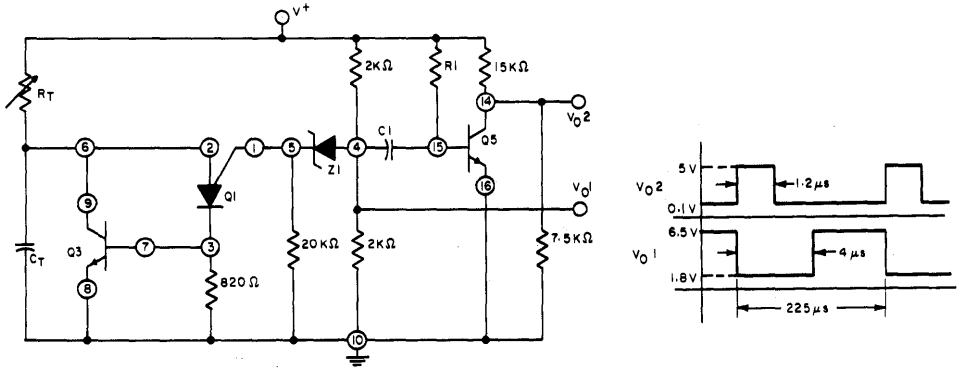
TYPICAL TEMPERATURE CHARACTERISTIC

$@\ R_L = 330\,\Omega\ \frac{\Delta V_O / V_O}{\Delta T} \times 100 = \pm 0.01\ \%/°C$

TYP. LOAD REGULATION @ I_L = 0 TO 40 mA, $(\Delta V_O / V_O) \times 100 =$ −3% (NO LOAD TO FULL LOAD)

TYP. LINE REGULATION $@\ R_L = 330\,\Omega, \frac{\Delta V_O / V_O}{\Delta V_{UNREG.}} \times 100 = \pm 0.55\ \%/V$

Fig. 28 – Temperature-compensated shunt regulator.

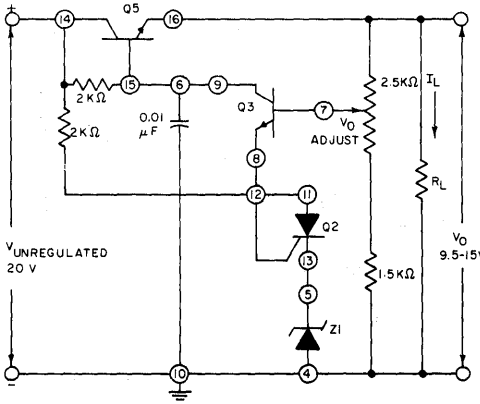


PULSE RATE ADJUSTED BY VARYING R_T OR C_T.
OUTPUT PULSE WIDTH ADJUSTED BY $R_1 C_1$
DIFFERENTIATING TIME CONSTANT

TYPICAL OPERATION FOR:
$V^+ = 15$ V, $C_T = 0.1\ \mu F$, $R_T = 4.3\ K\Omega$
$C_1 = 82$ pF, $R_1 = 60\ K\Omega$

Fig. 29 – Pulse generator.

APPLICATIONS CIRCUITS



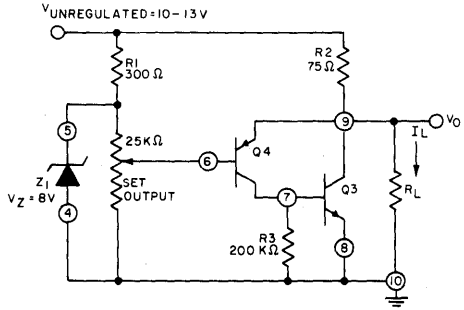
TYPICAL LOAD REGULATION @ V_O=12 V, I_L=0 TO 40 mA

$\frac{\Delta V_O}{V_O} \times 100 = \pm 0.4\%$ (NO LOAD TO FULL LOAD)

TYPICAL LINE REGULATION @ V_O=12 V

$\frac{\Delta V_O / V_O}{\Delta V_{UNREG.}} \times 100 = \pm 0.45\%/V$

Fig. 30 – Series voltage regulator.



TYPICAL LOAD REGULATION @ V_O=7 V, I_L=0 TO 40 mA

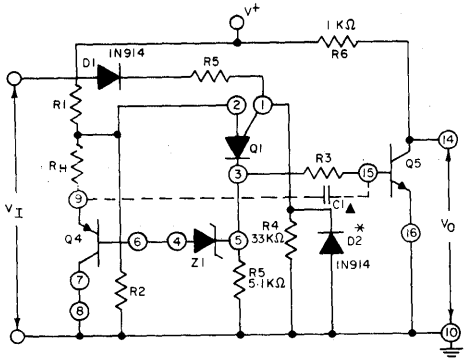
$\frac{\Delta V_O}{V_O} \times 100 = -1.1\%$

TYPICAL LINE REGULATION @ V_O=7 V, I_L=20 mA

$\frac{\Delta V_O}{V_O} = \pm 0.85\%/VOLT$

$\Delta V_{UNREGULATED}$

Fig. 31 – 5 to 7.5 V shunt regulator.



▲ OPTIONAL SPEED-UP CAPACITOR

* REQUIRED IF V_I SWINGS BELOW GROUND

TYPICAL OPERATING CONDITIONS:

FREQUENCY IN = 0-10 KHz

SUPPLY VOLTAGE (V^+) = 15 V

R1, R2, R_H = 5.1 KΩ

R3 = 6.2 KΩ, R_S = 300Ω

C_1 = 820 pF

$V_{TH}U$ = 7.5 V, $V_{TH}L$ = 5 V

HYSTERESIS VOLTAGE = 2.5 V

UPPER THRESHOLD VOLTAGE ($V_{TH}U$) $\approx V^+ \frac{R2}{R1+R2}$

LOWER THRESHOLD VOLTAGE ($V_{TH}L$) $\approx \frac{(V^+)\left(\frac{R2\,R_H}{R2+R_H}\right)}{\frac{R2\,R_H}{R2+R_H} + R1}$

HYSTERESIS VOLTAGE = $V_{TH}U - V_{TH}L$

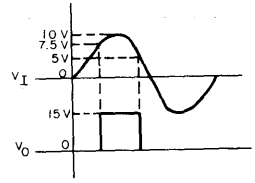
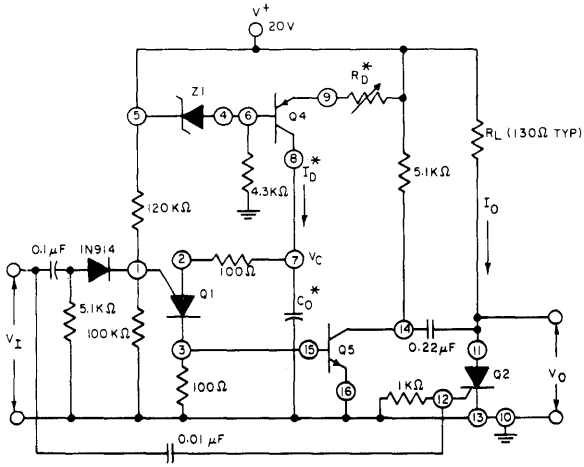
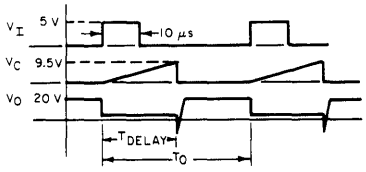


Fig. 32 – Schmitt trigger.

APPLICATIONS CIRCUITS (CONT'D)

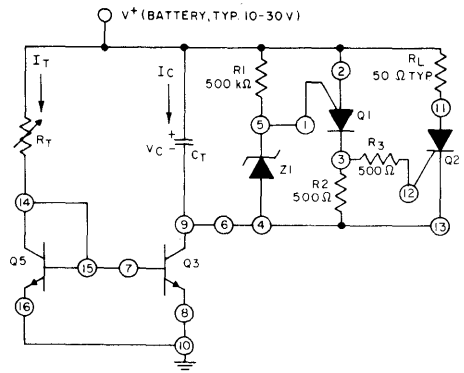




*MONOSTABLE DELAY TIME SET BY ADJUSTMENT OF I_D (VARY R_D) OR BY $C_D I_D$ MUST BE GREATER THAN I_V OF Q1 (PUT) FOR MONOSTABLE OPERATION.

Q2 (SCR) SWITCHING TIMES:
GATE-CONTROLLED TURN-ON TIME (t_{gt}) = 50 ns (TYP.)
CIRCUIT-COMMUTATED TURN-OFF TIME (t_q) = 10 μs (TYP.)

Fig. 33 – Monostable multivibrator with variable delay.



T_{OFF} = TIMING PERIOD (NO LOAD CURRENT)
PUT FIRES WHEN $V_C \approx 8$ V

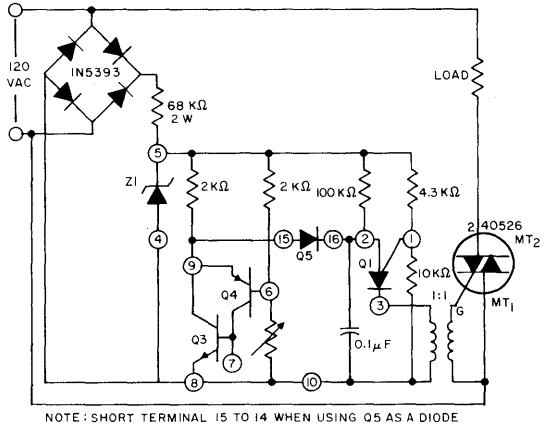
$V_C = \frac{I_C (T_{OFF})}{C_T}$, $I_C \approx I_T$ (Q3, Q5 MATCHED)

I_T SET BY ADJUSTING R_T, $I_T \approx \frac{V^+ - 0.7}{R_T}$

T_{ON} = CAPACITOR DISCHARGE TIME THROUGH LOAD. LOAD TURNS OFF WHEN SCR ANODE CURRENT FALLS BELOW HOLDING CURRENT (I_{HO}). TYPICAL I_{HO} = 1.2 mA

EXAMPLE: FOR TIMING PERIOD OF 8.3 MIN
C_T = 1000 μF, I_T = 16 μA
$R_T = \frac{V^+ - 0.7}{I_T}$ (FOR V^+ = 16 V, $R_T \approx$ 1 MΩ)

Fig.34 – Low-current-drain battery-operated long interval astable timer.



NOTE: SHORT TERMINAL 15 TO 14 WHEN USING Q5 AS A DIODE

Fig.35 – Phase control circuit.

May 1990

High-Frequency N-P-N Transistor Array

For Low-Power Applications at Frequencies up to 500 MHz

Features:

- *Gain-bandwidth product (f_T) > 1 GHz*
- *Power gain = 30 dB (typ.) at 100 MHz*
- *Noise figure = 3.5 dB (typ.) at 100 MHz*
- *Five independent transistors on a common substrate*

Applications:

- *VHF amplifiers*
- *Multifunction combinations - RF/mixer/oscillator*
- *Sense amplifiers*
- *Synchronous detectors*
- *VHF mixers*
- *IF converter*
- *IF amplifiers*
- *Synthesizers*
- *Cascade amplifiers*

The CA3127* consists of five general-purpose silicon n-p-n transistors on a common monolithic substrate. Each of the completely isolated transistors exhibits low 1/f noise and a value of f_T in excess of 1 GHz, making the CA3127 useful from dc to 500 MHz. Access is provided to each of the terminals for the individual transistors and a separate substrate connection has been provided for maximum application flexibility. The monolithic construction of the CA3127 provides close electrical and thermal matching of the five transistors.

The CA3127 is supplied in the 16-lead Small Outline package (M suffix), 16-lead dual-in-line plastic package (E suffix), 16-lead dual-in-line frit-seal ceramic package (F suffix), and is also available in clip form (H suffix). It operates over the full military temperature range of -55°C to +125°C.

*Formerly RCA Dev. No. TA6206.

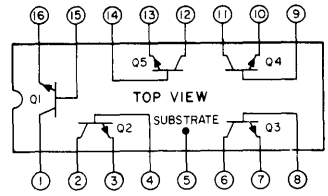


Figure 1 - Schematic diagram of CA3127.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

POWER DISSIPATION, P_D:
- Any one transistor ..... 85 mW

Total Package:
- For T_A up to 75°C ..... 425 mW
- For T_A > 75°C ..... Derate Linearly at 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating ..... -55°C to +125°C
- Storage ..... -65°C to +125°C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

The following ratings apply for each transistor in the device:

COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO} ..... 15 V

COLLECTOR-TO-BASE VOLTAGE, V_{CBO} ..... 20 V

COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}* ..... 20 V

COLLECTOR CURRENT, I_C ..... 20 mA

*The collector of each transistor of the CA3127 is isolated from the substrate by an integral diode. The substrate (terminal 5) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	TEST CONDITIONS		LIMITS			UNITS
			Min.	Typ.	Max.	
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$I_C = 10\ \mu A$, $I_E = 0$		20	32	–	V
Collector-to-Emitter Breakdown Voltage	$I_C = 1$ mA, $I_B = 0$		15	24	–	V
Collector-to-Substrate Breakdown Voltage	$I_{C1} = 10\ \mu A$, $I_B = 0$, $I_E = 0$		20	60	–	V
Emitter-to-Base Breakdown Voltage*	$I_E = 10\ \mu A$, $I_C = 0$		4	5.7	–	V
Collector-Cutoff-Current	$V_{CE} = 10$ V, $I_B = 0$		–	–	0.5	μA
Collector-Cutoff-Current	$V_{CB} = 10$ V, $I_E = 0$		–	–	40	nA
DC Forward-Current Transfer Ratio	$V_{CE} = 6$ V	$I_C = 5$ mA	35	88	–	
		$I_C = 1$ mA	40	90	–	
		$I_C = 0.1$ mA	35	85	–	
Base-to-Emitter Voltage	$V_{CE} = 6$ V	$I_C = 5$ mA	0.71	0.81	0.91	V
		$I_C = 1$ mA	0.66	0.76	0.86	
		$I_C = 0.1$ mA	0.60	0.70	0.80	
Collector-to-Emitter Saturation Voltage	$I_C = 10$ mA, $I_B = 1$ mA		–	0.26	0.50	V
Magnitude of Difference in V_{BE}	Q_1 & Q_2 Matched		–	0.5	5	mV
Magnitude of Difference in I_B	$V_{CE} = 6$ V, $I_C = 1$ mA		–	0.2	3	μA

*When used as a zener for reference voltage, the device must not be subjected to more than 0.1 millijoule of energy from any possible capacitance or electrostatic discharge in order to prevent degradation of the junction. Maximum operating zener current should be less than 10 mA.

DYNAMIC CHARACTERISTICS at $T_A = 25^oC$

CHARACTERISTICS	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
I/F Noise Figure	f = 100 kHz, $R_S = 500\ \Omega$, $I_C = 1$ mA	–	1.8	–	dB
Gain-Bandwidth Product	$V_{CE} = 6$ V, $I_C = 5$ mA	–	1.15	–	GHz
Collector-to-Base Capacitance	$V_{CB} = 6$ V, f = 1 MHz	–	See	–	pF
Collector-to-Substrate Capacitance	$V_{CI} = 6$ V, f = 1 MHz	–	Fig.	–	pF
Emitter-to-Base Capacitance	$V_{BE} = 4$ V, f = 1 MHz	–	5	–	pF
Voltage Gain	$V_{CE} = 6$ V, f = 10 MHz, $R_L = 1\ k\Omega$, $I_C = 1$ mA	–	28	–	dB
Power Gain	Cascode Configuration, f = 100 MHz, $V^+ = 12$ V	27	30	–	dB
Noise Figure	$I_C = 1$ mA	–	3.5	–	dB
Input Resistance	Common-Emitter	–	400	–	Ω
Output Resistance	Configuration	–	4.6	–	$k\Omega$
Input Capacitance	$V_{CE} = 6$ V	–	3.7	–	pF
Output Capacitance	$I_C = 1$ mA	–	2	–	pF
Magnitude of Forward Transadmittance	f = 200 MHz	–	24	–	mmho

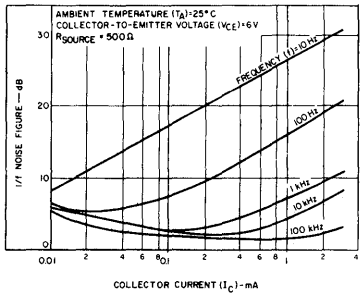


Fig. 2 – 1/f noise figure as a function of collector current at R_{SOURCE} = 500 Ω.

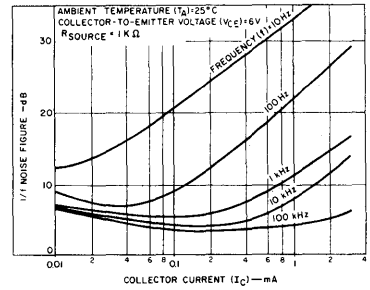


Fig. 3 – 1/f noise figure as a function of collector current at R_{SOURCE} = 1 kΩ.

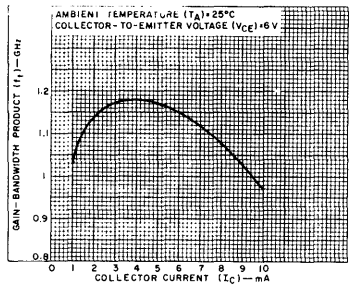


Fig. 4 – Gain-bandwidth product as a function of collector current.

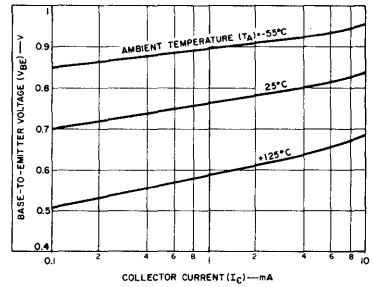


Fig. 5 – Base-to-emitter voltage as a function of collector current.

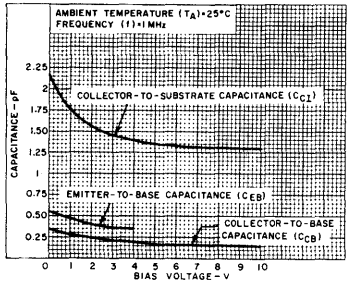


Fig. 6(a) – Capacitance as a function of bias voltage for Q_2.

Transistor	Capacitance (pF)							
	C_{CB}		C_{CE}		C_{EB}		C_{CI}	
	Pkg.	Total	Pkg.	Total	Pkg.	Total	Pkg.	Total
Bias Voltage	–	6 V	–	6 V	–	4 V	–	6 V
Q1	0.025	0.190	0.090	0.125	0.365	0.610	0.475	1.65
Q2	0.015	0.170	0.225	0.265	0.130	0.360	0.085	1.35
Q3	0.040	0.200	0.215	0.240	0.360	0.625	0.210	1.40
Q4	0.040	0.190	0.225	0.270	0.365	0.610	0.085	1.25
Q5	0.010	0.165	0.095	0.115	0.140	0.365	0.090	1.35

Fig. 6(b) – Typical capacitance values at f = 1 MHz. Three terminal measurement. Guard all terminals except those under test.

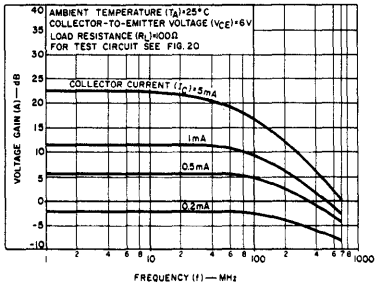


Fig. 7 – Voltage gain as a function of frequency at R_L = 100 Ω.

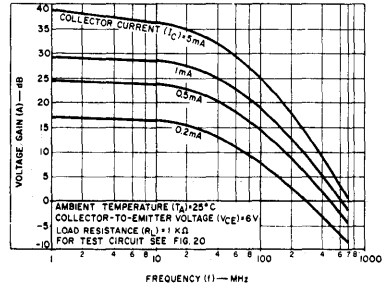


Fig. 8 – Voltage gain as a function of frequency at R_L = 1 kΩ.

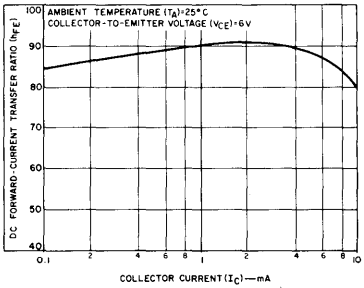


Fig. 9 – DC forward-current transfer ratio as a function of collector current.

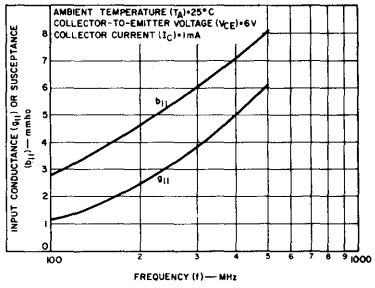


Fig. 10 – Input admittance (Y_{11}) as a function of frequency.

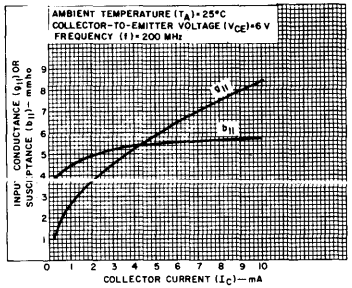


Fig. 11 – Input admittance (Y_{11}) as a function of collector current.

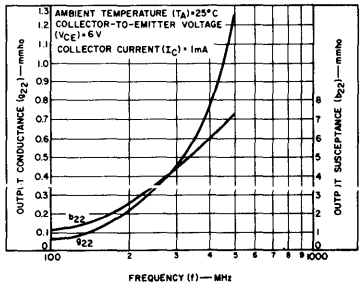


Fig. 12 – Output admittance (Y_{22}) as a function of frequency.

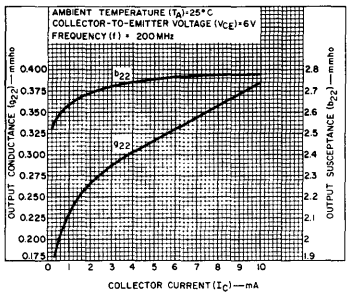


Fig. 13 – Output admittance (Y_{22}) as a function of collector current.

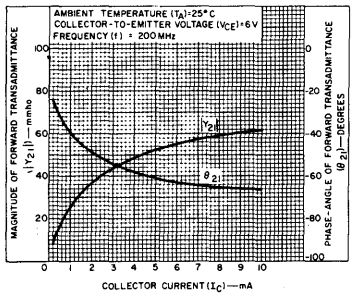


Fig. 14 – Forward transadmittance (Y_{21}) as a function of collector current.

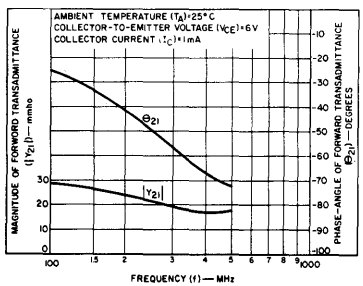


Fig. 15 – Forward transadmittance (Y_{21}) as a function of frequency.

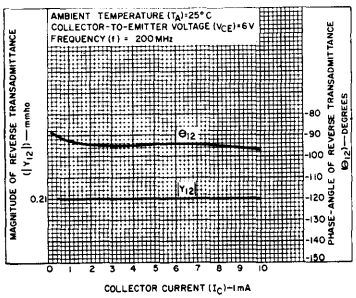


Fig. 16 – Reverse transadmittance (Y_{12}) as a function of collector current.

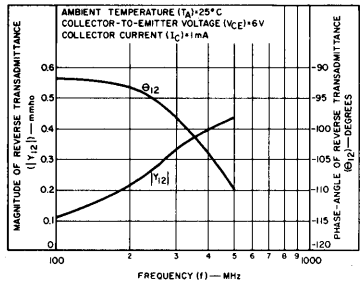


Fig. 17 – Reverse transadmittance (Y_{12}) as a function of frequency.

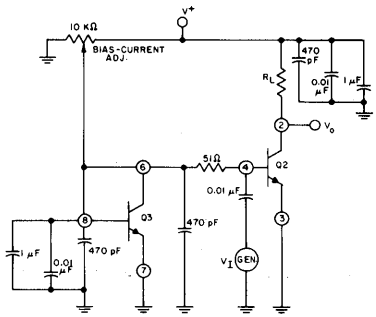
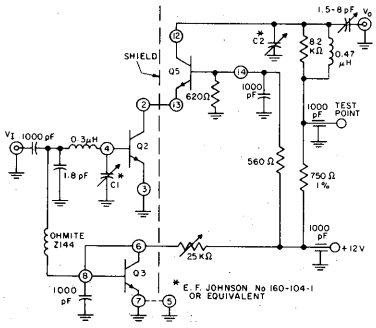


Fig. 18 – Voltage-gain test circuit using current-mirror biasing for Q_2.



This circuit was chosen because it conveniently represents a close approximation in performance to a properly unilateralized single transistor of this type. The use of Q3 in a current-mirror configuration facilitates simplified biasing. The use of the cascode circuit in no way implies that the transistors cannot be used individually.

Fig. 19 – 100-MHz power-gain and noise-figure test circuit.

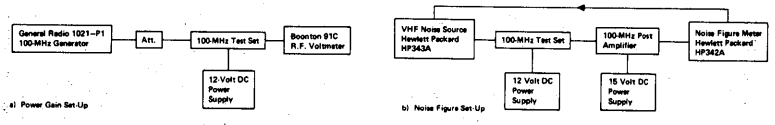


Fig. 20 – Block diagrams of power-gain and noise-figure test set-ups.

May 1990

High-Voltage Diode Array

For Commercial, Industrial, and Military Applications

Features:

- *Matched monolithic construction – V_F for each diode pair matched to within 0.55 mV (typ.) at I_F = 1 mA*
- *Low diode capacitance – 0.3 pF (typ.) at V_R = 2 V*
- *High diode-to-substrate breakdown voltage – 30 V (min.)*
- *Low reverse (leakage) current – 100 nA (max.)*

Applications:

- *Balanced modulators of demodulators*
- *Analog switches*
- *High-voltage diode gates*
- *Current ratio detectors*

The CA3141E High Voltage Diode Array Consists of ten general purpose high reverse breakdown diodes. Six diodes are internally connected to form three common cathode diode pairs, and the remaining four diodes are internally connected to form two common anode diode pairs. Integrated circuit construction assures excellent static and dynamic matching of the diodes, making the CA3141 extremely useful for a wide variety of applications in communications and switching systems.

The CA3141 is supplied in the 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

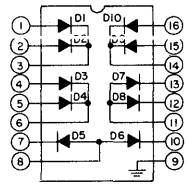


Figure 1 – Terminal assignment.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

PEAK INVERSE VOLTAGE (PIV) ..... 30 V
PEAK DIODE-TO-SUBSTRATE VOLTAGE ..... 30 V
PEAK FORWARD SURGE CURRENT [I_F (SURGE)] ..... 100 mA
DC FORWARD CURRENT (I_F) ..... 25 mA
DISSIPATION:
  Any one diode unit ..... 50 mW
  Total Package:
    Up to 55°C ..... 650 mW
    For T_A > 55°C ..... Derate linearly at 6.67 mW/°C
AMBIENT TEMPERATURE RANGE:
  Operating ..... -55 to +125°C
  Storage ..... -65 to +150°C
LEAD TEMPERATURE (During Soldering):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max ..... +265°C

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARACTERISTIC	TEST CONDITIONS		LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNIT
DC Forward Voltage Drop, V_F	I_F (Anode)	100 μA	–	0.7	0.9	V
		1 mA	–	0.78	1	
		10 mA	–	0.93	1.2	
DC Reverse Breakdown Voltage, $V_{(BR)R}$	$I_F = -10$ μA		30	50	–	V
DC Breakdown Voltage Between Any Diode and Substrate, $V_{(BR)DI}$	$I_{DI} = 10$ μA		30	50	–	V
DC Reverse (Leakage) Current, I_R	$V_F = -20$ V		–	–	100	nA
DC Reverse (Leakage) Current Between Any Diode and Substrate, I_{DI}	$V_{DI} = 20$ V		–	–	100	nA
Magnitude of Diode Offset Voltage Between Diode Pairs	$V_{DI} = 20$ V $I_{FA} = 1$ mA		–	0.55	–	mV
Temperature Coefficient of Forward Voltage Drop, $\Delta V_F/\Delta T$	$I_F = 1$ mA		–	–1.5	–	mV/°C
Reverse Recovery Time, t_{rr}	$I_F = 2$ mA, $I_R = 2$ mA		–	50	–	ns
Diode Capacitance, C_D			See Fig. 5			pF
Diode Anode-to-Substrate Capacitance, C_{DAI}			See Fig. 6			pF
Diode Cathode-to-Substrate Capacitance, C_{DCI}			See Fig. 7			pF
Magnitude of Cathode-to-Anode Current Ratio, $\lvert I_{FC}/I_{FA} \rvert$	$I_{FA} = 1$ mA, $V_{DS} = 10$ V		0.9	0.96	–	

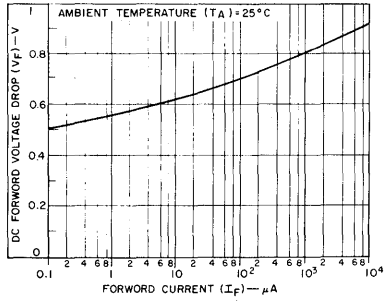


Fig. 2 – DC forward voltage drop vs. forward current.

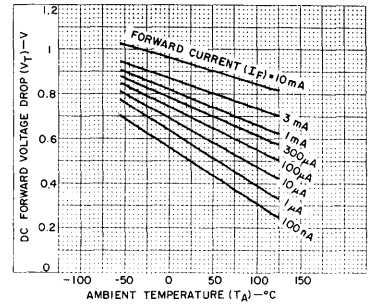


Fig. 3 – DC forward voltage drop vs. ambient temperature.

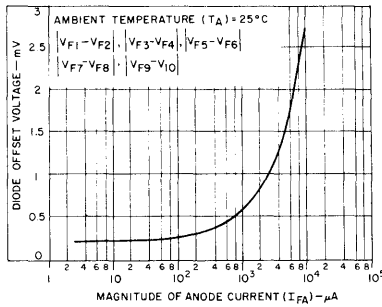


Fig. 4 — Diode offset voltage vs. magnitude of anode current.

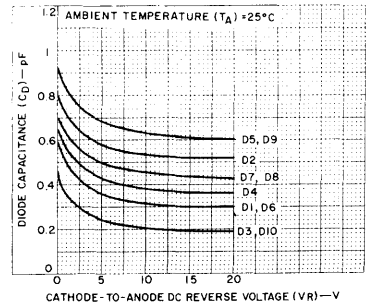


Fig. 5 — Diode capacitance vs. cathode-to-anode reverse voltage.

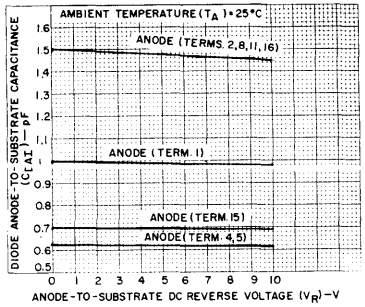


Fig. 6 — Diode anode-to-substrate capacitance vs. reverse voltage.

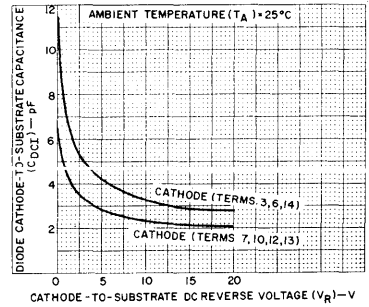


Fig. 7 — Diode cathode-to-substrate capacitance vs. cathode-to-substrate DC reverse voltage.

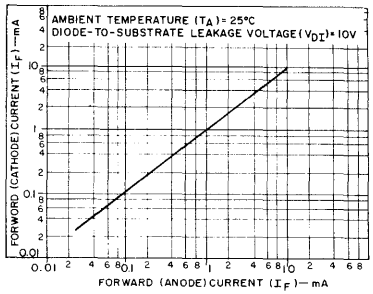


Fig. 8 — Forward (cathode) current vs. forward (anode) current.

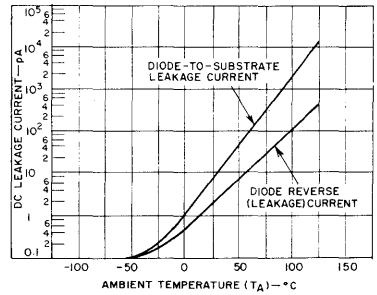


Fig. 9 — DC leakage current vs. ambient temperature.

7 ARRAYS

May 1990

High-Voltage Transistor Arrays

Features:

- *Matched general-purpose transistors*
- *V_{BE} matched ± 5 mV max.*
- *Operation from DC to 120 MHz (CA3146AE, E)*
- *Low-noise figure: 3.2 dB typ. at 1 kHz (CA3146AE, E)*
- *High I_C: 75 mA max. (CA3183AE, E)*

Applications:

- *General use in signal processing systems in DC through VHF range*
- *Custom designed differential amplifiers*
- *Temperature compensated amplifiers*
- *Lamp and relay drivers (CA3183AE, E)*
- *Thyristor firing (CA3183AE, E)*

The CA3146AE, CA3146E, CA3183AE, and CA3183E* are general-purpose high-voltage silicon n-p-n transistor arrays on a common monolithic substrate.

Types CA3146AE and CA3146E consist of five transistors with two of the transistors connected to form a differentially-connected pair. These types are recommended for low-power applications in the DC through VHF range. Both types are supplied in a 14-lead dual-in-line plastic package and operate over the ambient temperature range of -40°C to +85°C. Additionally, the CA3146 is supplied in a 14-lead Small Outline package (M suffix). (CA3146AE and CA3146E are high-voltage versions of the popular predecessor type CA3046.)

Types CA3183AE and CA3183E consist of five high-current transistors with independent connections for each transistor. In addition two of these transistors (Q1 and Q2) are matched at low-current (i.e. 1 mA) for applications where offset parameters are of special importance. A special substrate terminal is also included for greater flexibility in circuit design. Both types are supplied in a 16-lead dual-in-line plastic package and operate over the ambient temperature range of -40°C to +85°C. Additionally, the CA3183 is supplied in a 14-lead Small Outline package (M suffix). (CA3183AE and CA3183E are high-voltage versions of the popular predecessor type CA3083.)

The types with an "A" suffix are premium versions of their non-"A" counterparts and feature tighter control of breakdown voltages making them more suitable for higher voltage applications.

For detailed application information, see companion Application Note, ICAN-5296 "Application of the CA3018 Integrated Circuit Transistor Array."

*Formerly Developmental Types Nos.
CA3146AE - TA6084 CA3183AE - TA6094
CA3146E - TA6181 CA3183E - TA6183

TYPE	P_T• MAX. mW	I_C MAX. mA	V_{CEO} MAX. V	V_{CBO} MAX. V	V_{CE} sat. at 10 mA TYP. V	h_{FE} at 1 mA, & V_{CE} = 5 V TYP.	DIFF. PAIR AT 1 mA V_{IO} MAX. mV	DIFF. PAIR AT 1 mA I_{IO} MAX. µA	T_A Range (OPERATING) °C
VALUES APPLY FOR EACH TRANSISTOR									
CA3146AE	300	50	40	50	0.33	95	±5	2	-40 - +85
CA3146E	300	50	30	40	0.33	95	±5	2	-40 - +85
CA3183AE	500	75	40	50	0.16	75	±5	2.5	-40 - +85
CA3183E	500	75	30	40	0.16	75	±5	2.5	-40 - +85

• Caution on Total Package Power Dissipation: The maximum total package dissipation rating for the CA3146 and CA3183 Series circuits is 750 mW at temperatures up to +55°C, then derate linearly at 6.67 mW/°C.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

POWER DISSIPATION:
- Any one transistor -
  - CA3146AE, CA3146E ..... 300 mW
  - CA3183AE, CA3183E ..... 500 mW
- Total package -
  - Up to 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E) ..... 750 mW
  - Above to 55°C (CA3146AE, CA3146E, CA3183AE, CA3183E) ..... Derate linearly 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating -
  - CA3146AE, CA3146E, CA3183AE, CA3183E ..... -40 to +85°C
- Storage (all types) ..... -65 to +150°C

The following ratings apply for each transistor in the device:

COLLECTOR-TO-EMITTER VOLTAGE (V_{CEO}):
- CA3146AE, CA3183AE ..... 40 V
- CA3146E, CA3183E ..... 30 V

COLLECTOR-TO-BASE VOLTAGE (VCBO):
- CA3146AE, CA3183AE ..... 50 V
- CA3146E, CA3183E ..... 40 V

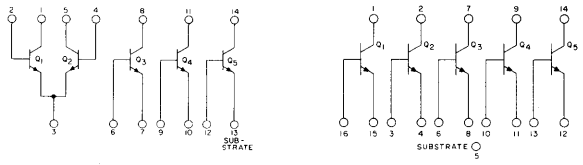
COLLECTOR-TO-SUBSTRATE VOLTAGE (V_{CIO}):■
- CA3146AE, CA3183AE ..... 50 V
- CA3146E, CA3183E ..... 40 V

EMITTER-TO-BASE VOLTAGE (V_{EBO}) all types ..... 5 V

COLLECTOR CURRENT -
- CA3146AE, CA3146E ..... 50 mA
- CA3183E ..... 75 mA

BASE CURRENT (I_B) - CA3183AE, CA3183E ..... 20 mA

■ The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either DC or signal (AC) ground. A suitable bypass capacitor can be used to establish a signal ground.



CA3146AE, CA314E CA3183AE, CA3183E

Figure 1 - Schematic diagrams of high-voltage arrays.

7 ARRAYS

COMPARISON OF RELATED PREDECESSOR TYPE WITH TYPES IN THIS DATA BULLETIN

	DATA FILE NO.	V_{CEO} MIN.	V_{CBO} MIN.	V_{CE} sat. TYP. V	V_{BE} TYP. V	I_C MAX. mA	C_{CB} TYP. pF	C_{CI} TYP. pF	C_{EB} TYP. pF
				I_C = 10 mA	I_C = 1 mA				
CA3046	341	15	20	0.23	0.715	50	0.58	2.8	0.6
CA3146AE		40	50	0.33	0.730	50	0.37	2.2	0.7
CA3146E		30	40	0.33	0.730	50	0.37	2.2	0.7
				I_C = 50 mA	I_C = 10 mA				
CA3083	481	15	20	0.4	0.74	100	—	—	—
CA3183AE		40	50	1.7	0.75	75	—	—	—
CA3183E		30	40	1.7	0.75	75	—	—	—

STATIC ELECTRICAL CHARACTERISTICS – CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		Typ. Char. Curve Fig. No.	LIMITS						UNITS
		T_A = 25°C			CA3146AE			CA3146E			
					Min.	Typ.	Max.	Min.	Typ.	Max.	
For Each Transistor:											
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 10 μA, I_E = 0		–	50	72	–	40	72	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0		–	40	56	–	30	56	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI} = 10μA, I_B = 0, I_E = 0		–	50	72	–	40	72	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 10μA, I_C = 0		–	5	7	–	5	7	–	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0		2	–	see curve	5	–	see curve	5	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0		3	–	0.002	100	–	0.002	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=5V	I_C=10 mA	4	–	85	–	–	85	–	–
			I_C=1 mA	4	30	100	–	30	100	–	
			I_C=10μA	4	–	90	–	–	90	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 1 mA		5	0.63	0.73	0.83	0.63	0.73	0.83	V
Collector-to-Emitter Saturation Voltage	V_{CEsat}	I_C = 10mA, I_B = 1 mA		6	–	0.33	–	–	0.33	–	V
For transistors Q3 and Q4 (Darlington Configeration):											
Base-to-Emitter (Q3 to Q4)	V_{BE}	V_{CE}=5V	I_E = 10mA	8	–	1.46	–	–	1.46	–	V
			I_E = 1mA	8,9	–	1.32	–	–	1.32	–	
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\lvert\frac{\triangle V_{BE}}{\triangle T}\right\rvert$	V_{CE} = 5V, I_E = 1 mA		–	–	4.4	–	–	4.4	–	mV/°C
For transistors Q1 and Q2 (AS a Differential Amplifier):											
Magnitude of Input Offset Voltage $\lvert V_{BE1} = V_{BE2}\rvert$	$\lvert V_{IO}\rvert$	V_{CE} = 5V, I_E = 1 mA		10, 11	–	0.48	5	–	0.48	5	mV
Magnitude of Base-to-Emitter Temperature Coefficient	$\left\lvert\frac{\triangle V_{BE}}{\triangle T}\right\rvert$	V_{CE} = 5V, I_E = 1 mA		–	–	1.9	–	–	1.9	–	mV/°C
Magnitude of V_{IO} (V_{BE1} - V_{BE2}) Temperature Coefficient	$\left\lvert\frac{\triangle V_{IO}}{\triangle T}\right\rvert$	V_{CE} = 5V, I_{C1} = I_{C2} = 1 mA		–	–	1.1	–	–	1.1	–	μV/°C
Magnitude of Input Offset Current $\lvert I_{IO_1} - I_{IO_2}\rvert$	CA3146AE and CA3146E only I_{IO}	V_{CE} = 5V, I_{C_1} = I_{C_2} = 1 mA		12	–	0.3	2	–	0.3	2	μA

DYNAMIC ELECTRICAL CHARACTERISTICS – CA3146 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	Typ. Char. Curve Fig.No.	CA3146AE Min.	CA3146AE Typ.	CA3146AE Max.	CA3146E Min.	CA3146E Typ.	CA3146E Max.	UNITS
Low Frequency Noise Figure	NF	f = 1kHz, V_{CE} = 5V, I_C = 100μA, Source resistance = 1 kΩ	14	–	3.25	–	–	3.25	–	dB
Low-Frequency, Small-Signal Equivalent-Circuit Characteristics:										
Foward-Current Transfer Ratio	h_{fe}	f = 1kHz, V_{CE} = 5V, I_C = 1mA	16	–	100	–	–	100	–	–
Short-Circuit Input Impedance	h_{ie}		16	–	2.7	–	–	3.5	–	kΩ
Open-Circuit Output Impedance	h_{oe}		16	–	15.6	–	–	15.6	–	μmho
Open-Circuit Reverse-Voltage Transfer Ratio	h_{re}		16	–	$1.8x10^{-4}$	–	–	$1.8x10^{-4}$	–	–
Admittance Characteristics:										
Foward Transfer Admittance	Y_{fe}	f = 1MHz, V_{CE} = 5V, I_C = 1mA	17	–	31-j1.5	–	–	31-j1.5	–	mmho
Input Admittance	Y_{ie}		18	–	0.35+j0.04	–	–	0.3+j0.04	–	mmho
Output Admittance	Y_{oe}		19	–	0.001+j0.03	–	–	0.001+j0.03	–	mmho
Reverse Transfer Admittance	Y_{re}		20		See curve			See curve		mmho
Gain-Bandwidth Product	f_T	V_{CE} = 5V, I_C = 3mA	21	300	500	–	300	500	–	MHz
Emitter-to-Base Capacitance	C_{EB}	V_{EB} = 5V, I_E = 0	22	–	0.70	–	–	0.70	–	pF
Collector-to-Base Capacitance	C_{CB}	V_{CB} = 5V, I_C = 0	22	–	0.37	–	–	0.37	–	pF
Collector-to-Substrate Capacitance	C_{CI}	V_{CI} = 5V, I_C = 0	22	–	2.2	–	–	2.2	–	pF

STATIC ELECTRICAL CHARACTERISTICS – CA3183 Series

CHARACTERISTICS	SYMBOL	TEST CONDITIONS T_A = 25°C	Typ. Char Curve Fig. No.	LIMITS CA3183AE Min.	CA3183AE Typ.	CA3183AE Max.	CA3183E Min.	CA3183E Typ.	CA3183E Max.	UNITS
For Each Transistor:										
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=100μA, I_E=0	–	50	–	–	40	–	–	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1mA, I_B=0	–	40	–	–	30	–	–	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{CI}=100μA, I_B=0, I_E = 0	–	50	–	–	40	–	–	V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 500μA, I_C = 0	–	5	–	–	5	–	–	V
Collector-Cutoff Current	I_{CEO}	V_{CE} = 10V, I_B = 0	23	–	–	10	–	–	10	μA
Collector-Cutoff Current	I_{CBO}	V_{CB} = 10V, I_E = 0	24	–	–	1	–	–	1	μA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}= 3 V, I_C = 10mA	25,26	40	–	–	40	–	–	–
		V_{CE} = 5V, I_C = 50mA	–	40	–	–	40	–	–	
Base-to-Emitter Voltage	V_{BE}	V_{CE} = 3V, I_C = 10mA	27	0.65	0.75	0.85	0.65	0.75	0.85	V
Collector-to-Emitter Saturation Voltage	*V_{CEsat}	I_C = 50mA, I_B = 5mA	28	–	1.7	3.0	–	1.7	3.0	V
For Transistors Q1 and Q2 (As a Differential Amplifier):										
Absolute Input Offset Voltage	$\lvert V_{IO}\rvert$	V_{CE} = 3V, I_C = 1mA	29	–	0.47	5	–	0.47	5	mV
Absolute Input Offset Current	$\lvert I_{IO}\rvert$		30	–	0.78	2.5	–	0.78	2.5	μA

* A maximum dissipation of 5 transistors x 150mW = 750mW is possible for a particular application.

TYPICAL STATIC CHARACTERISTICS CURVES – CA3146 SERIES

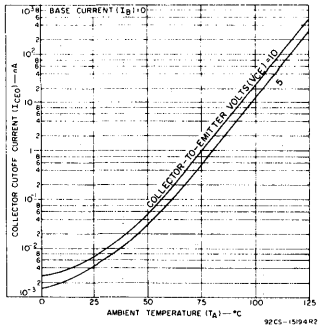


Fig. 2 – I_{CEO} vs. T_A for any transistor.

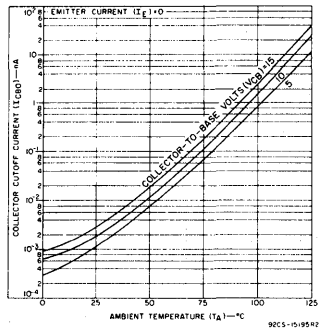


Fig. 3 – I_{CBO} vs. T_A for any transistor.

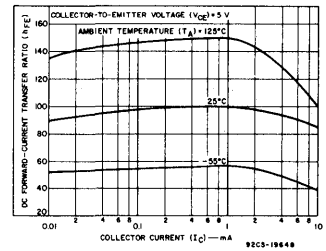


Fig. 4 – h_{FE} vs. I_C for any transistor.

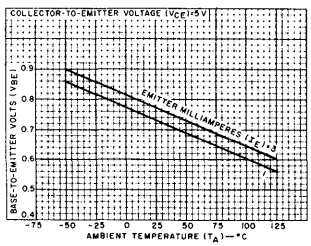


Fig. 5 – V_{BE} vs. T_A for any transistor.

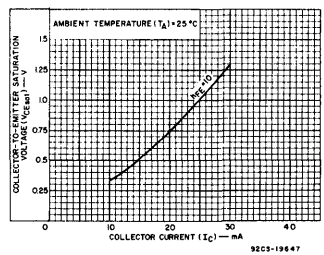


Fig. 6 – $V_{CE\ sat}$ vs. I_C for any transistor.

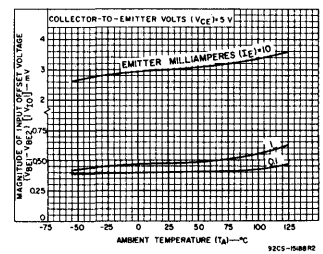


Fig. 10 – V_{IO} vs. T_A for Q1 and Q2.

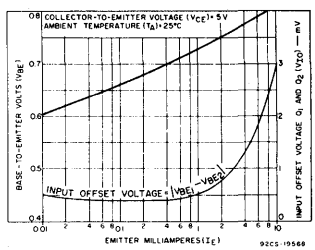


Fig. 11 – V_{BE} and V_{IO} vs. I_E for Q1 and Q2.

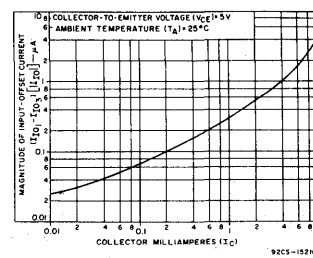


Fig. 12 – I_{IO} vs. I_C (Q1 and Q2) for types CA3146AE and CA3146E.

TYPICAL DYNAMIC CHARACTERISTICS CURVES (FOR ANY TRANSISTOR) – CA3146 SERIES

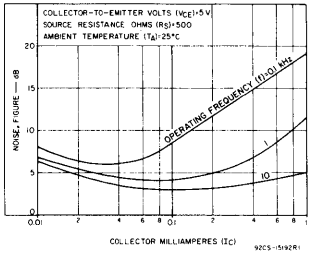


Fig. 13 – NF vs. I_C @ R_S = 500Ω.

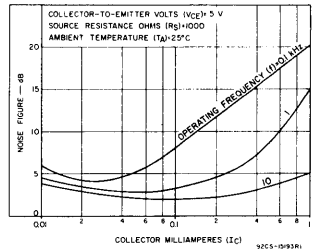


Fig. 14 – NF vs. I_C @ R_S = 1kΩ.

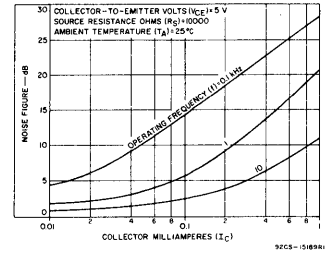


Fig. 15 – NF vs. I_C @ R_S = 10kΩ.

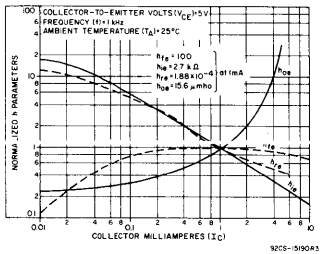


Fig. 16 – h_{fe}, h_{ie}, h_{oe}, h_{re} vs. I_C.

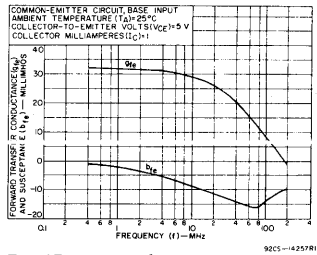


Fig. 17 – y_{fe} vs. f.

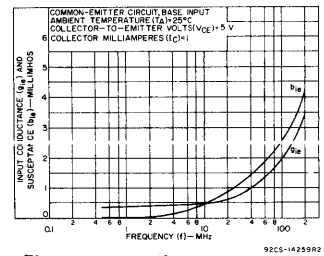


Fig. 18 – y_{ie} vs. f.

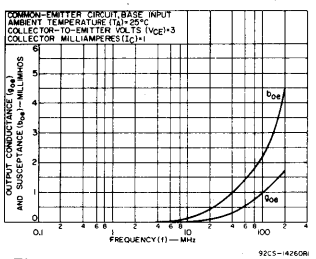


Fig. 19 – y_{oe} vs. f.

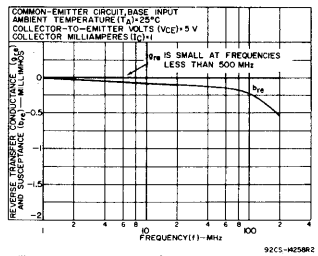


Fig. 20 – y_{re} vs. f.

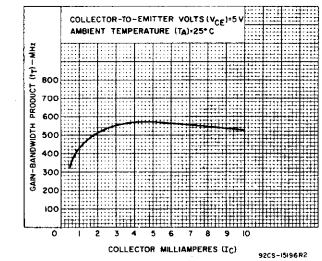


Fig. 21 – f_T vs. I_C.

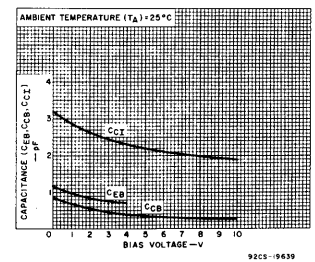


Fig. 22 – C_{EB}, C_{CB}, C_{CI} vs. bias voltage

7 ARRAYS

TYPICAL STATIC CHARACTERISTICS CURVES – CA3183 SERIES

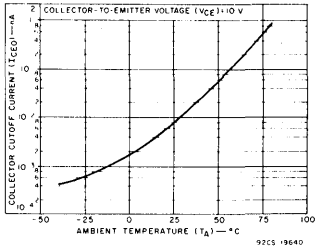


Fig. 23 – I_{CEO} vs. T_A for any transistor.

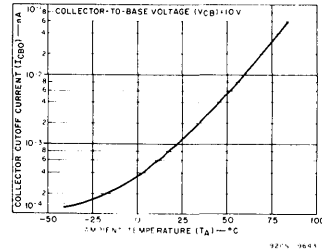


Fig. 24 – I_{CBO} vs. T_A for any transistor.

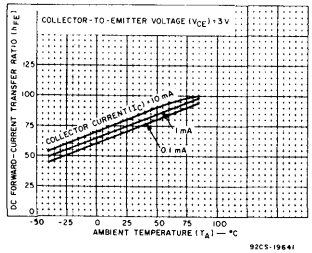


Fig. 25 – h_{FE} vs. T_A for any transistor.

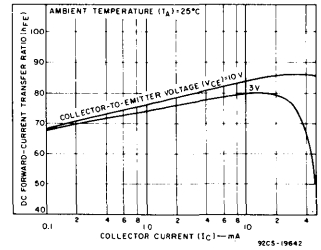


Fig. 26 – h_{FE} vs. I_C for any transistor.

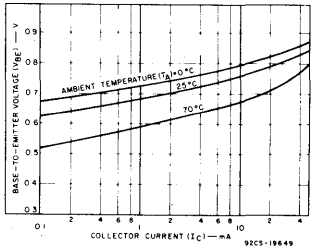


Fig. 27 V_{BE} vs. I_C for any transistor.

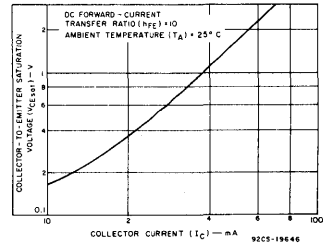


Fig. 28 – $V_{CE\,sat}$ vs. I_C for any transistor.

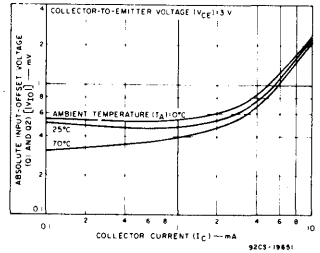


Fig. 29 – $|V_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2).

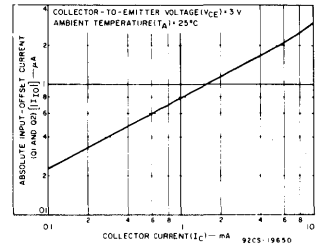


Fig. 30 – $|I_{IO}|$ vs. I_C for differential amplifier (Q1 and Q2).

May 1990

High-Frequency N-P-N Transistor Arrays

For Low-Power Applications at Frequencies up to 1.5 GHz

Features:

- *Gain-bandwidth product (f_T) > 3 GHz*
- *Five transistors on a common substrate*

Applications:

- *VHF amplifiers*
- *VHF mixers*
- *Multifunction combinations-RF/mixer/oscillator*
- *IF converter*
- *IF amplifiers*
- *Sense amplifiers*
- *Synthesizers*
- *Synchronous detectors*
- *Cascade amplifiers*

The CA3227E and CA3246E* consist of five general purpose silicon n-p-n transistors on a common monolithic substrate. Each of the transistors exhibits a value of f_T in excess of 3 GHz, making them useful from dc to 1.5 GHz. The monolithic construction of these devices provides close electrical and thermal matching of the five transistors.

The CA3227 is supplied in a 16-lead Small Outline package (M suffix) and in 16-lead dual-in-line plastic package (E suffix). The CA3246 is supplied in a 14-lead Small Outline package (M suffix) and in a 14-lead dual-in-line plastic package (E suffix).

*Formerly RCA Development Nos. TA10854 and TA10855, respectively.

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C*

POWER DISSIPATION, P_D:
- Any one transistor ..... 85 mW

Total Package:
- For T_A up to 75°C ..... 425 mW
- For T_A > 75°C ..... Derate Linearly at 6.67 mW/°C

AMBIENT TEMPERATURE RANGE:
- Operating ..... -55 to +125°C
- Storage ..... -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

The following ratings apply for each transistor in the device:

COLLECTOR-TO-EMITTER VOLTAGE, V_{CEO} ..... 8 V
COLLECTOR-TO-BASE VOLTAGE, V_{CBO} ..... 12 V
COLLECTOR-TO-SUBSTRATE VOLTAGE, V_{CIO}§ ..... 20 V
COLLECTOR CURRENT, I_C ..... 20 mA

§The collector of each transistor of these devices is isolated from the substrate by an integral diode. The substrate (terminal 5/CA3227E and terminal 13/CA3246E) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

STATIC ELECTRICAL CHARACTERISTICS at T_A=25°C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
For Each Transistor:						
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C=10 μA, I_E=0	12	20	—	V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C=1 mA, I_B=0	8	10	—	V
Collector-to-Substrate Breakdown Voltage	$V_{(BR)CIO}$	I_{C1}=10 μA, I_B=0, I_E=0	20	—	—	V
Emitter-Cutoff-Current*	I_{EBO}	V_{EB}=4.5 V, I_C=0	—	—	10	μA
Collector-Cutoff-Current	I_{CEO}	V_{CE}=5 V, I_B=0	—	—	1	μA
Collector-Cutoff-Current	I_{CBO}	V_{CB}=8 V, I_E=0	—	—	100	nA
DC Forward-Current Transfer Ratio	h_{FE}	V_{CE}=6 V, I_C=10 mA	—	110	—	
		V_{CE}=6 V, I_C=1 mA	40	150	—	
		V_{CE}=6 V, I_C=0.1 mA	—	150	—	
Base-to-Emitter Voltage	V_{BE}	V_{CE}=6 V, I_C=1 mA	0.62	0.71	0.82	V
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	I_C=10 mA, I_B=1 mA	—	0.13	0.50	V
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	I_C=10 mA, I_B=1 mA	0.74	—	0.94	V

*On small-geometry, high-frequency transistors, it is very good practice never to take the Emitter Base Junction into reverse breakdown. To do so may permanently degrade the h_{FE}. Hence, the use of I_{EBO} rather than $V_{(BR)EBO}$. These devices are also susceptible to damage by electrostatic discharge and transients in the circuits in which they are used. Moreover, CMOS handling procedures should be employed.

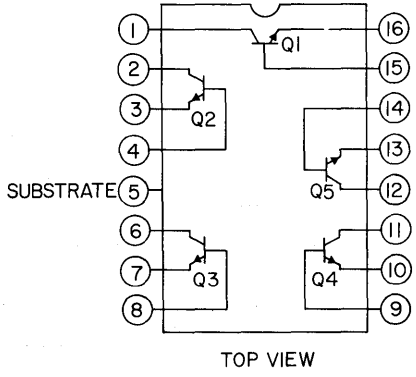


Fig. 1 - Schematic diagram of CA3227

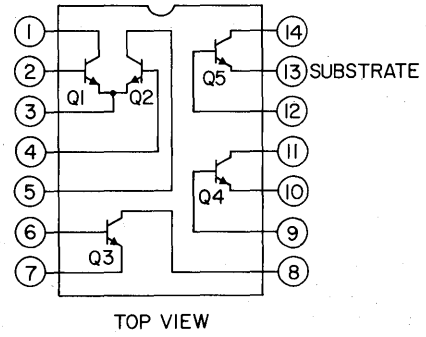


Fig. 2 - Schematic diagram of CA3246

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C, 200 MHz, Common Emitter
Typical Values Intended Only for Design Guidance

CHARACTERISTIC		TEST CONDITIONS	TYPICAL VALUES	UNITS
For Each Transistor				
Input Admittance,	$Y_{11}\ \frac{b_{11}}{g_{11}}$	I_C=1 mA, V_{CE}=5 V	4	mmho
			0.75	
Output Admittance,	$Y_{22}\ \frac{b_{22}}{g_{22}}$		2.7	mmho
			0.13	
Forward Transfer Admittance,	$Y_{21}\ \frac{Y_{21}}{\theta_{21}}$		29.3	mmho
			−33	degrees
Reverse Transfer Admittance,	$Y_{12}\ \frac{Y_{12}}{\theta_{12}}$		0.38	mmho
			−97	degrees
Input Admittance,	$Y_{11}\ \frac{b_{11}}{g_{11}}$	I_C=10 mA, V_{CE}=5 V	4.8	mmho
			2.85	
Output Admittance,	$Y_{22}\ \frac{b_{22}}{g_{22}}$		2.75	
			0.9	
Forward Transfer Admittance,	$Y_{21}\ \frac{Y_{21}}{\theta_{21}}$		95	mmho
			−62	degrees
Reverse Transfer Admittance,	$Y_{12}\ \frac{Y_{12}}{\theta_{12}}$		0.39	mmho
			−97	degrees
Small-Signal Forward Current Transfer Ratio	h_{21}	I_C=1 mA, V_{CE}=5 V	7.1	
		I_C=10 mA, V_{CE}=5 V	17	
Typical Capacities @ 1 MHz, Three-Terminal Measurement				
Collector-to-Base Capacitance, C_{CB}		V_{CB}=6 V	0.3	pF
Collector-to-Substrate Capacitance, C_{CI}		V_{CI}=6 V	1.6	pF
Collector-to-Emitter Capacitance, C_{CE}		V_{CE}=6 V	0.4	pF
Emitter-to-Base Capacitance, C_{EB}		V_{EB}=3 V	0.75	pF

LINEAR 8

SPECIAL ANALOG CIRCUITS

PAGE

SPECIAL ANALOG CIRCUITS DATA SHEETS

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ICL 8048	Log Amplifier	8-60
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ICM 7242	Long-Range Fixed Timer	8-70
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LM 555C	Timer	8-3

May 1990

Timers

For Timing Delays & Oscillator Applications in Commercial, Industrial, and Military Equipment

Features:

- *Accurate timing from microseconds through hours*
- *Astable and monostable operation*
- *Adjustable duty cycle*
- *Output capable of sourcing or sinking up to 200 mA*
- *Output capable of driving TTL devices*
- *Normally ON and OFF outputs*
- *High-temperature stability - 0.005%/°C*
- *Directly interchangeable with SE555, NE555, MC1555, and MC1455*

Applications:

- *Precision timing*
- *Sequential timing*
- *Time-delay generation*
- *Pulse generation*
- *Pulse-width and position modulation*
- *Pulse detector*

The CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free-running frequency and duty cycle with only two external resistors and one capacitor.

The circuits of the CA555 and CA555C may be triggered by the falling edge of the wave-form signal, and the output of these circuits can source or sink up to a 200-milliampere current or drive TTL circuits.

The CA555 and CA555C are supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead TO-5 style packages with dual-in-line formed leads (DIL-CAN, S suffix), 8-lead Small Outline package (M suffix), 8-lead dual-in-line plastic packages (MINI-DIP, E suffix), and in chip form (H suffix). These types are direct replacement for industry types in packages with similar terminal arrangements e.g. SE555 and NE555, MC1555 and MC1455, respectively. The CA555 type circuits are intended for applications requiring premium electrical performance. The CA555C type circuits are intended for applications requiring less stringent electrical characteristics.

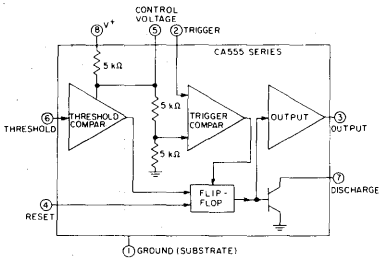


Fig. 1 - Functional diagram of the CA555 series.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE ..... 18 V
DEVICE DISSIPATION:
  Up to T_A = 55°C ..... 600 mW
  Above T_A = 55°C ..... Derate linearly 5 mW/°C
AMBIENT TEMPERATURE RANGE:
  OPERATING
    CA555 ..... -55 to +125°C
    CA555C ..... 0 to 70°C
  STORAGE ..... -65 to +150°C
LEAD TEMPERATURE (During Soldering):
  At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

*Technical Data on LM Branded types is identical to the corresponding CA Branded types.

ELECTRICAL CHARACTERISTICS, *At $T_A = 25^oC$, $V^+ = 5$ to 15 V unless otherwise specified*

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		CA555			CA555C			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
DC Supply Voltage, V^+		4.5	–	18	4.5	–	16	V
DC Supply Current (Low State)*, I^+	$V^+ = 5$ V, $R_L = \infty$	–	3	5	–	3	6	mA
	$V^+ = 15$ V, $R_L = \infty$	–	10	12	–	10	15	mA
Threshold Voltage, V_{TH}		–	$(2/3)V^+$	–	–	$(2/3)V^+$	–	V
Trigger Voltage	$V^+ = 5$ V	1.45	1.67	1.9	–	1.67	–	V
	$V^+ = 15$ V	4.8	5	5.2	–	5	–	
Trigger Current		–	0.5	–	–	0.5	–	μA
Threshold Current▲, I_{TH}		–	0.1	0.25	–	0.1	0.25	μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current		–	0.1	–	–	0.1	–	mA
Control Voltage Level	$V^+ = 5$ V	2.9	3.33	3.8	2.6	3.33	4	V
	$V^+ = 15$ V	9.6	10	10.4	9	10	11	V
Output Voltage Drop: Low State, V_{OL}	$V^+ = 5$ V, $I_{SINK} = 5$ mA	–	–	–	–	0.25	0.35	V
	$I_{SINK} = 8$ mA	–	0.1	0.25	–	–	–	
	$V^+ = 15$ V, $I_{SINK} = 10$ mA	–	0.1	0.15	–	0.1	0.25	
	$I_{SINK} = 50$ mA	–	0.4	0.5	–	0.4	0.75	V
	$I_{SINK} = 100$ mA	–	2.0	2.2	–	2.0	2.5	
	$I_{SINK} = 200$ mA	–	2.5	–	–	2.5	–	
High State, V_{OH}	$V^+ = 5$ V, $I_{SOURCE} = 100$ mA	3.0	3.3	–	2.75	3.3	–	V
	$V^+ = 15$ V, $I_{SOURCE} = 100$ mA	13.0	13.3	–	12.75	13.3	–	
	$I_{SOURCE} = 200$ mA	–	12.5	–	–	12.5	–	
Timing Error (Monostable): Initial Accuracy	$R_1, R_2 = 1$ to 100 kΩ, $C = 0.1$ μF, Tested at $V^+ = 5$ V, $V^+ = 15$ V	–	0.5	2	–	1	–	%
Frequency Drift with Temperature		–	30	100	–	50	–	p/m/°C
Drift with Supply Voltage		–	0.05	0.2	–	0.1	–	%/V
Output Rise Time, t_r		–	100	–	–	100	–	ns
Output Fall Time, t_f		–	100	–	–	100	–	ns

* When the output is in a high state, the dc supply current is typically 1 mA less than the low-state value.

▲ The threshold current will determine the sum of the values of R_1 and R_2 to be used in Fig. 16 (astable operation): the maximum total $R_1 + R_2 = 20$ MΩ.

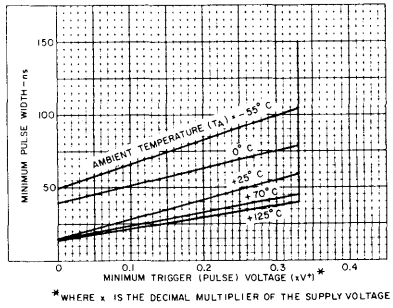


Fig.2 – Minimum pulse width vs. minimum trigger voltage.

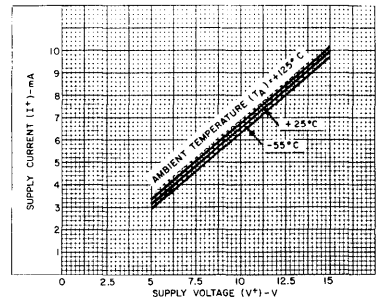


Fig.3 – Supply current vs. supply voltage.

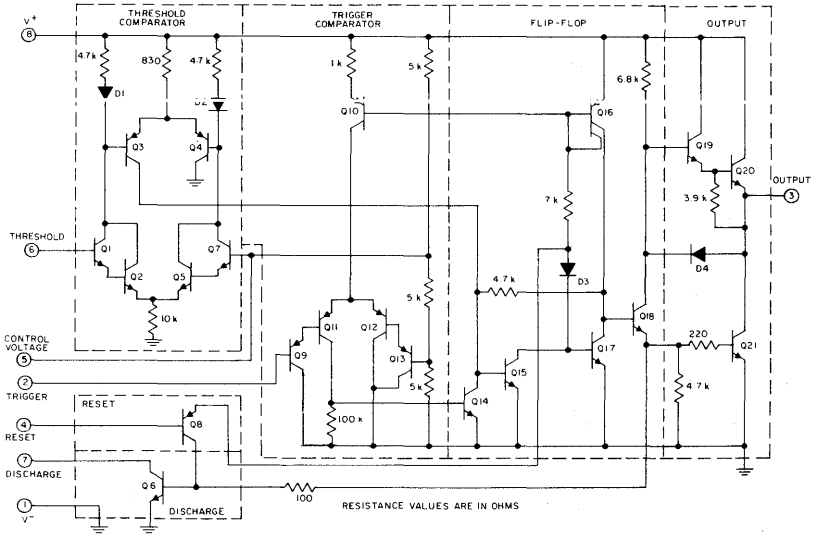
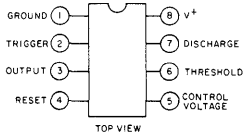
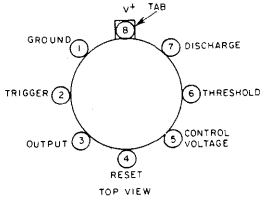


Fig.4 – Schematic diagram of the CA555 and CA555C.



a. MINI-DIP plastic package
TO-5 style package with formed leads



b. TO-5 style package

Fig.5 – Terminal assignment diagrams.

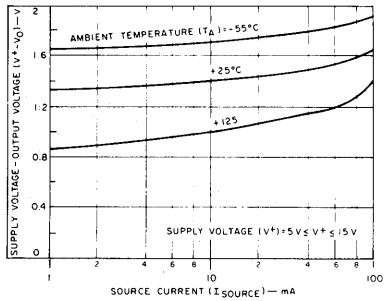


Fig.6 – Output voltage drop (high state) vs. source current.

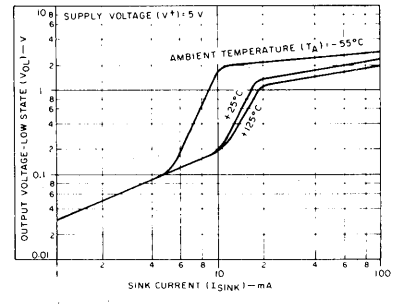


Fig.7 – Output voltage-low state vs. sink current at V^+ = 5 V.

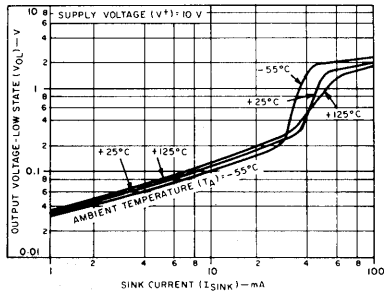


Fig.8 – Output voltage-low state vs. sink current at V^+ = 10 V.

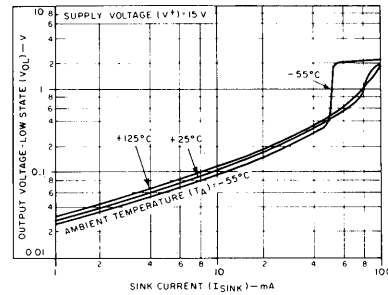


Fig.9 – Output voltage-low state vs. sink current at V^+ = 15 V.

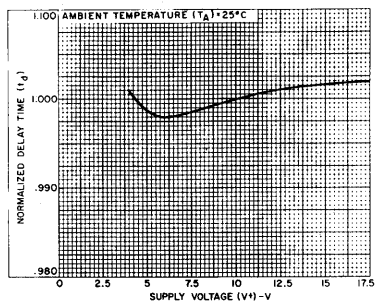


Fig.10 – Delay time vs. supply voltage.

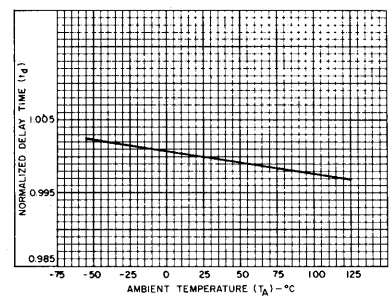


Fig.11 – Delay time vs. temperature.

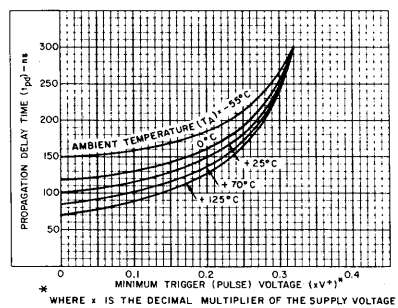


Fig.12 – Propagation delay time vs. trigger voltage.

TYPICAL APPLICATIONS

Reset Timer (Monostable Operation)

Fig.13 shows the CA555 connected as a reset timer. In this mode of operation capacitor C_T is initially held discharged by a transistor on the integrated circuit. Upon closing the "start" switch, or applying a negative trigger pulse to terminal 2, the integral timer flip-flop is "set" and releases the short circuit across C_T which drives the output voltage "high" (relay energized). The action allows the voltage across the capacitor to increase exponentially with the time constant $t = R_1C_T$. When the voltage across the capacitor equals 2/3 V^+, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state.

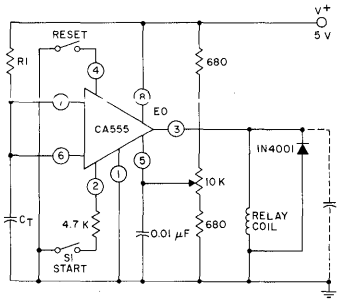


Fig.13 – Reset timer (monostable operation).

Since the charge rate and threshold level of the comparator are both directly proportional to V^+, the timing interval is relatively independent of supply voltage variations. Typically, the timing varies only 0.05% for a 1 volt change in V^+.

Applying a negative pulse simultaneously to the reset terminal (4) and the trigger terminal (2) during the timing cycle discharges C_T and causes the timing cycle to restart. Momentarily closing only the reset switch during the timing interval discharges C_T, but the timing cycle does not restart.

Fig.14 shows the typical waveforms generated during this mode of operation, and Fig.15 gives the family of time delay curves with variations in R_1 and C_T.

Repeat Cycle Timer (Astable Operation)

Fig.16 shows the CA555 connected as a repeat cycle timer. In this mode of operation, the total period is a function of both R_1 and R_2;

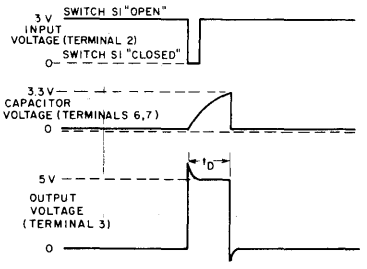


Fig.14 – Typical waveforms for reset timer.

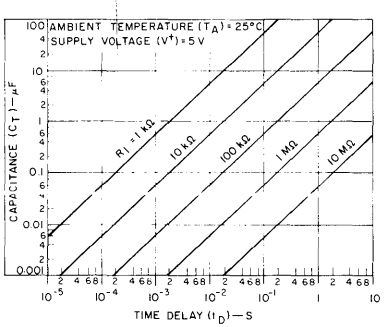


Fig.15 – Time delay vs. resistance and capacitance.

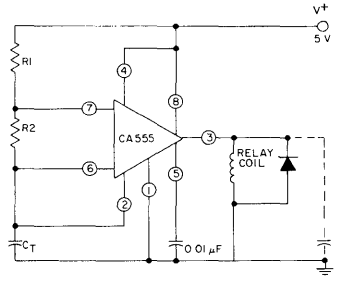


Fig.16 – Repeat cycle timer (astable operation).

$$T = 0.693(R_1 + 2R_2)C_T = t_1 + t_2$$

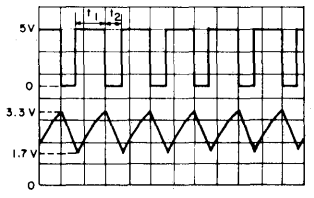
where $t_1 = 0.693(R_1 + R_2)\,C_T$

and $t_2 = 0.693(R_2)C_T$

The duty cycle is:

$$\frac{t_2}{t_1 + t_2} = \frac{R_2}{R_1 + 2R_2}$$

Typical waveforms generated during this mode of operation are shown in Fig. 17. Fig. 18 gives the family of curves of free running frequency with variations in the value of $(R_1 + 2R_2)$ and C_T.



Top Trace: Output voltage (2V/div. and 0.5 ms/div.)
Bottom Trace: Capacitor voltage (1 V/div. and 0.5 ms/div.)

Fig.17 – Typical waveforms for repeat cycle timer.

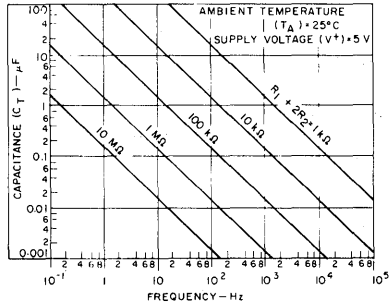


Fig.18 – Free running frequency of repeat cycle timer with variation in capacitance and resistance.

HARRIS

HA-2546

Wideband Two Quadrant Analog Multiplier

August 1989

Features

- High Speed Voltage Output 300V/μs
- Low Multiplication Error 1.6%
- Input Bias Currents 1.2μA
- Signal Input Feedthrough ..... -52dB
- Wide Signal Bandwidth 30MHz
- Wide Control Bandwidth 17MHz
- Gain Tolerance to 5 MHz 0.10dB

Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

Description

The HA-2546 is a monolithic, high speed, two quadrant, analog multiplier constructed in the Harris Dielectrically Isolated High Frequency Process. The high frequency performance of the HA-2546 rivals the best analog multipliers currently available including hybrids.

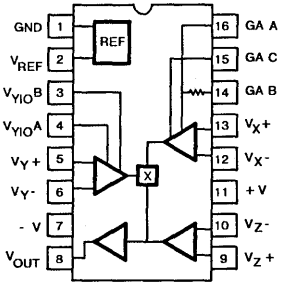
The HA-2546 has a voltage output with a 30MHz signal bandwidth, 300V/μs slew rate and a 17MHz control input bandwidth. High bandwidth and slew rate make this part an ideal component for use in video systems. The suitability for precision video applications is demonstrated further by the 0.1dB gain tolerance at 5MHz, 1.6% multiplication error, -52dB feedthrough and differential inputs with 1.2μA bias currents. The HA-2546 also has low differential gain (0.1%) and phase (0.1°) errors.

The HA-2546 is well suited for AGC circuits as well as mixer applications for sonar, radar, and medical imaging equipment. The voltage output of the HA-2546 simplifies many designs by eliminating the current-to-voltage conversion stage required for current output multipliers.

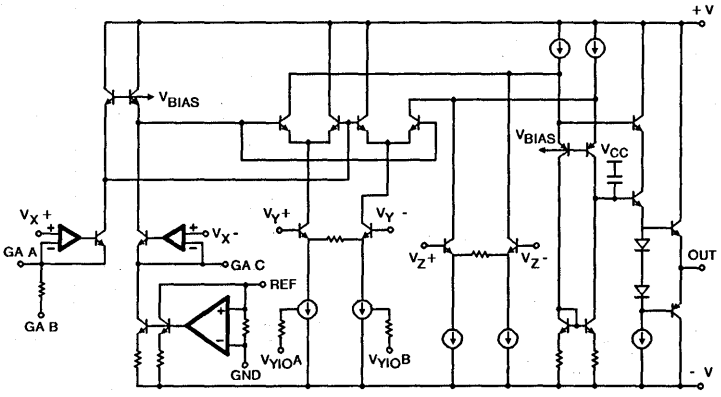
The HA-2546-9 has guaranteed operation from -40°C to +85°C. The HA-2546-5 has guaranteed operation from 0°C to +75°C. The HA-2546 is available in a 16 pin Ceramic DIP. For MIL-STD-883 compliant product and LCC packages consult the HA-2546/883 datasheet.

Pinout

HA1-2546 (CERAMIC DIP)
TOP VIEW



Simplified Schematic



8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage 6V
Output Current ..... ±60mA

Operating Temperature Range

HA-2546-9 ..... $-40^{o}C \leq T_A \leq +85^{o}C$
HA-2546-5 ..... $0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range ..... $-65^{o}C \leq T_A \leq +150^{o}C$
Maximum Junction Temperature ..... $+175^{o}C$

Electrical Specifications V+ = 15V, V- = -15V, R_L = 1K, C_L = 50pF, Unless Otherwise Specified

PARAMETER	TEMP	HA-2546-9			HA-2546-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
MULTIPLIER PERFORMANCE								
Multiplication Error (Note 2)	+25°C	-	1.6	3	-	1.6	3	%
	Full	-	3.0	7	-	3.0	7	%
Multiplication Error Drift	Full	-	-	-	-	-	-	%/°C
Differential Gain (Note 3,11)	+25°C	-	0.1	0.2	-	0.1	0.2	%
Differential Phase (Note 3,11)	+25°C	-	0.1	0.3	-	0.1	0.3	Deg.
Gain Tolerance (Note 6,11)								
DC to 5 MHz	+25°C	-	0.1	0.2	-	0.1	0.2	dB
5 MHz to 8 MHz	+25°C	-	0.18	0.3	-	0.18	0.3	dB
Scale Factor Error	Full	-	0.7	5.0	-	0.7	5.0	%
1% Amplitude Bandwidth Error	+25°C	-	6	-	-	6	-	MHz
1% Vector Bandwidth Error	+25°C	-	260	-	-	260	-	kHz
THD + N (Note 4)	+25°C	-	0.03	-	-	0.03	-	%
Voltage Noise (Note 17)								
f_o=10Hz	+25°C	-	400	-	-	400	-	$nV/\sqrt{Hz}$
f_o=100Hz	+25°C	-	150	-	-	150	-	$nV/\sqrt{Hz}$
f_o=1kHz	+25°C	-	75	-	-	75	-	$nV/\sqrt{Hz}$
Common Mode Range	+25°C	-	±9	-	-	±9	-	Volts
SIGNAL INPUT, V_Y								
Input Offset Voltage	+25°C	-	3	10	-	3	10	mV
	Full	-	8	20	-	8	20	mV
Average Offset Voltage Drift	Full	-	45	-	-	45	-	µV/°C
Input Bias Current	+25°C	-	7	15	-	7	15	µA
	Full	-	10	15	-	10	15	µA
Input Offset Current	+25°C	-	0.7	2	-	0.7	2	µA
	Full	-	1.0	3	-	1.0	3	µA
Differential Input Resistance	+25°C	-	720	-	-	720	-	kΩ
Small Signal Bandwidth (-3dB) (Note 6)	+25°C	-	30	-	-	30	-	MHz
Full Power Bandwidth (Note 5)	+25°C	-	9.5	-	-	9.5	-	MHz
Feedthrough (Note 15)	+25°C	-	-52	-	-	-52	-	dB
CMRR (Note 7)	Full	60	78	-	60	78	-	dB
V_Y TRANSIENT RESPONSE (Note 12)								
Slew Rate (Note 8)	+25°C	-	300	-	-	300	-	V/µs
Rise Time (Note 9)	+25°C	-	11	-	-	11	-	ns
Overshoot (Note 9)	+25°C	-	17	-	-	17	-	%
Propagation Delay	+25°C	-	25	-	-	25	-	ns
Settling Time (Note 8) 0.1%	+25°C	-	200	-	-	200	-	ns

Electrical Specifications (Continued) V+ = 15V, V- = -15V, R_L = 1K, C_L = 50pF, Unless Otherwise Specified

PARAMETER	TEMP	HA-2546-9			HA-2546-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
CONTROL INPUT, V_X								
Input Offset Voltage	+25°C	-	0.3	2	-	0.3	2	mV
	Full	-	3	20	-	3	20	mV
Average Offset Voltage Drift	Full	-	10	-	-	10	-	µV/°C
Input Bias Current	+25°C	-	1.2	2	-	1.2	2	µA
	Full	-	1.8	5	-	1.8	5	µA
Input Offset Current	+25°C	-	0.3	2	-	0.3	2	µA
	Full	-	0.4	3	-	0.4	3	µA
Differential Input Resistance	+25°C	-	360	-	-	360	-	kΩ
Small Signal Bandwidth (-3dB) (Note 13)	+25°C	-	17	-	-	17	-	MHz
Feedthrough (Note 16)	+25°C	-	-40	-	-	-40	-	dB
Common Mode Rejection Ratio (Note 19)	+25°C	-	80	-	-	80	-	dB
V_X TRANSIENT RESPONSE (Note 12)								
Slew Rate (Note 19)	+25°C	-	95	-	-	95	-	V/µs
Rise Time (Note 20)	+25°C	-	20	-	-	20	-	ns
Overshoot (Note 20)	+25°C	-	17	-	-	17	-	%
Propagation Delay	+25°C	-	50	-	-	50	-	ns
Settling Time (Note 19) 0.1%	+25°C	-	200	-	-	200	-	ns
V_Z CHARACTERISTICS								
Input Offset Voltage (Note 17)	+25°C	-	4	15	-	4	15	mV
	Full	-	8	20	-	8	20	mV
Open Loop Gain	+25°C	-	70	-	-	70	-	dB
Differential Input Resistance	+25°C	-	900	-	-	900	-	kΩ
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 18)	Full	-	±6.25	-	-	±6.25	-	Volts
Output Current	Full	±20	±45	-	±20	±45	-	mA
Output Resistance	+25°C	-	1	-	1	-	-	Ω
POWER SUPPLY								
PSRR (Note 10)	Full	58	63	-	58	63	-	dB
Supply Current	Full	-	23	29	-	23	29	mA

NOTES:

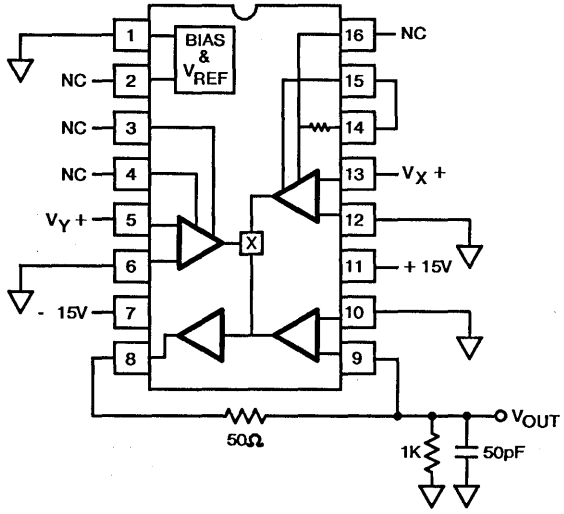
1. Absolute maximum ratings are limiting values, applied individually, beyond which the servicability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Error is percent of full scale, 1% = 50mV.
3. f_O = 3.58MHz/4.43MHz, V_Y = 300mVp-p, 0 to 1Vdc offset, V_X = 2V.
4. f_O = 10kHz, V_Y = 1Vrms, V_X = 2V.
5. V_X = 2V, Full Power Bandwidth calculated by equation:

$$FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}, \quad V_{peak} = 5V.$$

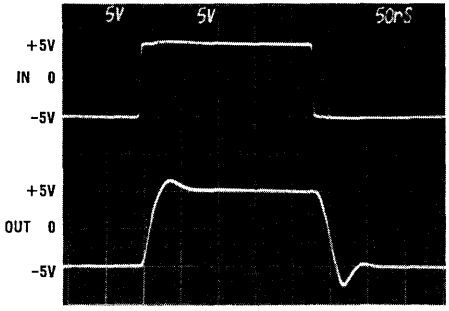
6. V_X = 2V.
7. V_Y = 0 to ±5V, V_X = 2V.
8. V_{OUT} = ±5V, V_X = 2V.
9. V_{OUT} = 0 to ± 100mV, V_X = 2V.
10. V_S = ±12V to ±15V, V_Y = 5V, V_X = 2V.
11. Guaranteed by characterization and not 100% tested.
12. See Test Circuit.
13. V_Y = 5V, V_{X-} = -1V.
15. f_O = 5MHz, V_X = 0, V_Y = 200mVrms.
16. f_O = 100kHz, V_Y = 0, V_{X+} = 200mVrms, V_{X-} = -0.5V.
17. V_X = V_Y = 0.
18. V_X = 2.5V, V_Y = ±5V.
19. V_X = 0 to 2V, V_Y = 5V.
20. V_X = 0 to 200mV, V_Y = 5V.

Test Circuits

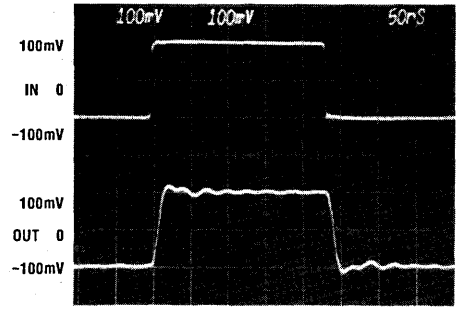
LARGE AND SMALL SIGNAL RESPONSE TEST CIRCUIT



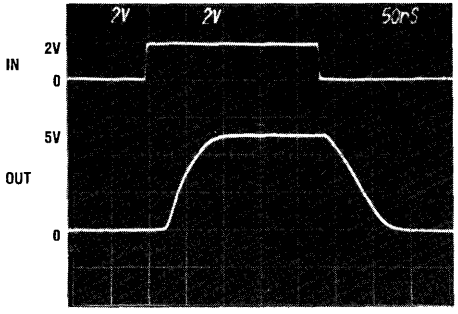
V_Y LARGE SIGNAL RESPONSE
Vertical Scale: 5V/Div. Horizontal Scale: 50ns/Div.



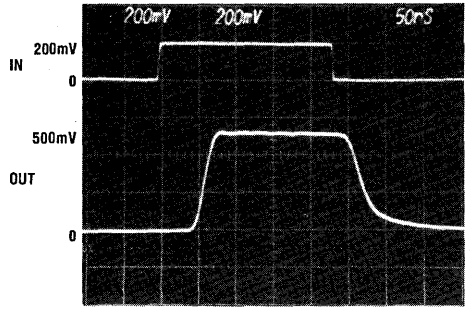
V_Y SMALL SIGNAL RESPONSE
Vertical Scale: 100mV/Div. Horizontal Scale: 50ns/Div.



V_X LARGE SIGNAL RESPONSE
Vertical Scale: 2V/Div. Horizontal Scale: 50ns/Div.

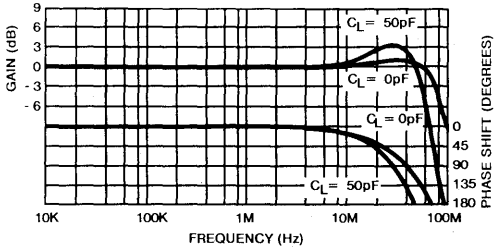


V_X SMALL SIGNAL RESPONSE
Vertical Scale: 200mV/Div. Horizontal Scale: 50ns/Div.

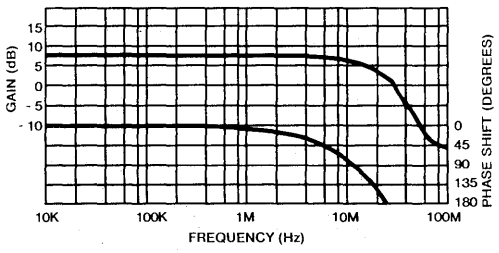


Typical Performance Curves $V_S = \pm15V$, $T_A = +25^oC$, See test circuit for multiplier configuration

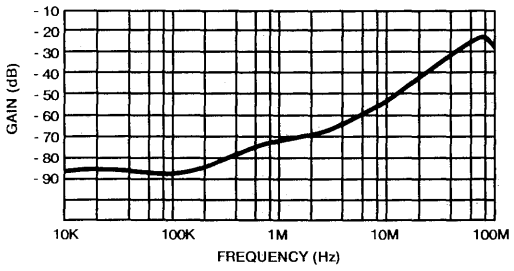
V_Y GAIN AND PHASE vs FREQUENCY
R_L = 1K, V_X = 2Vdc, V_Y = 200mVrms



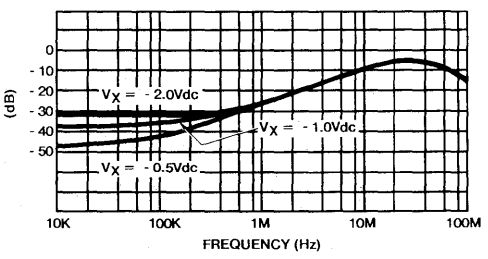
V_X GAIN AND PHASE vs FREQUENCY
R_L = 1K, V_X+ = 200mVrms, V_Y = 5Vdc, V_X- = -1Vdc



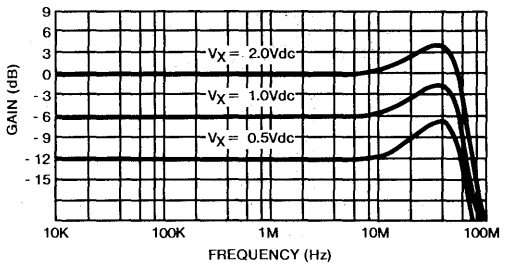
V_Y FEEDTHROUGH vs FREQUENCY
V_X = 0V, R_L = 1K, V_Y = 200mVrms



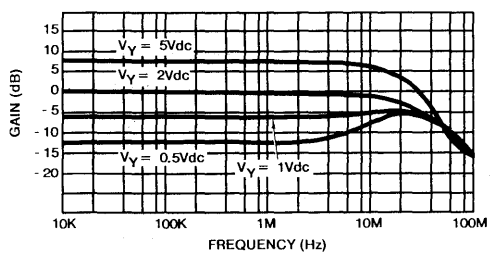
V_Y FEEDTHROUGH vs FREQUENCY
R_L = 1K, V_X+ = 200mVrms, V_Y = 0V



VARIOUS V_Y FREQUENCY RESPONSES
R_L = 1K, C_L = 50pF, V_Y = 200mVrms

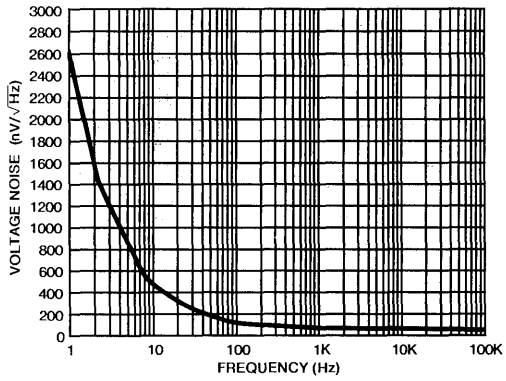


VARIOUS V_X FREQUENCY RESPONSES
V_X+ = 200mVrms, R_L = 1K, V_X- = -1Vdc

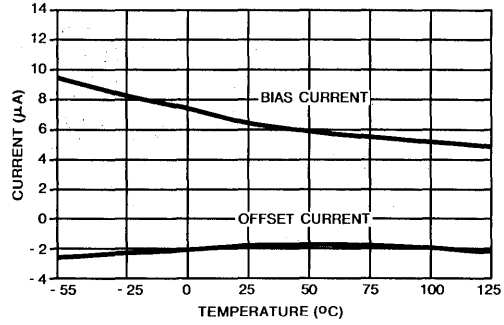


Typical Performance Curves (Continued) $V_S = \pm 15V$, $T_A = +25^oC$, See test circuit for multiplier configuration

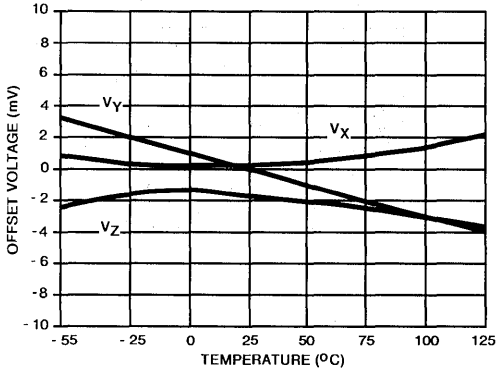
NOISE CHARACTERISTICS
$V_X = 0V$, $V_Y = 0V$



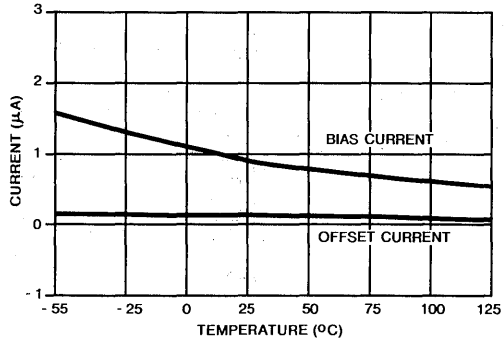
V_Y OFFSET AND BIAS CURRENT vs TEMPERATURE



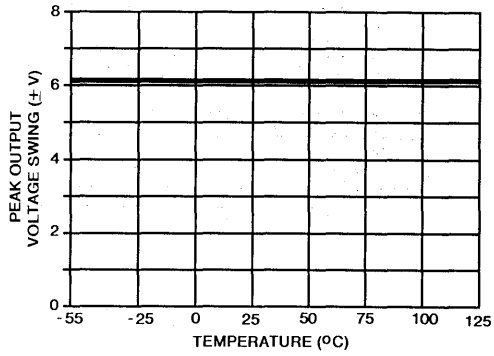
OFFSET VOLTAGE vs TEMPERATURE



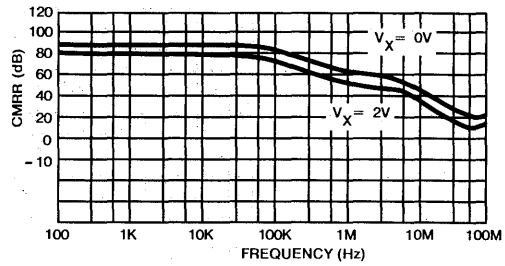
V_X OFFSET AND BIAS CURRENT vs TEMPERATURE



OUTPUT VOLTAGE SWING vs TEMPERATURE



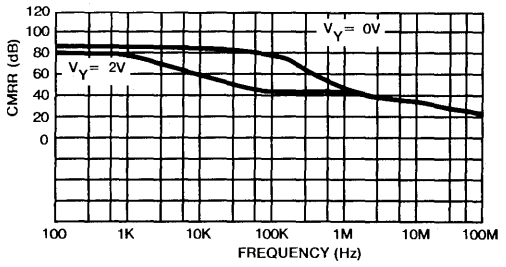
V_Y CMRR vs FREQUENCY
V_{Ycm} = 200mVrms



Typical Performance Curves (Continued) $V_S = \pm 15V$, $T_A = +25^oC$, See test circuit for multiplier configuration

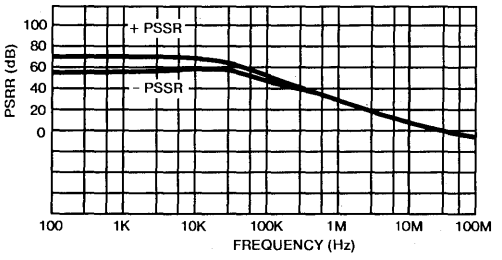
V_X COMMON MODE REJECTION RATIO vs FREQUENCY

V_X = 200mVrms

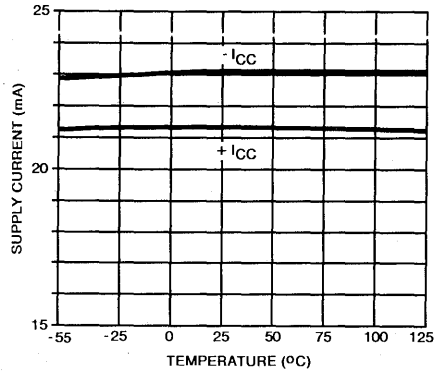


PSRR vs FREQUENCY

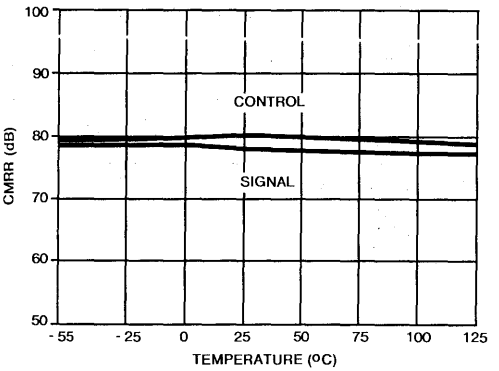
$V_Y = V_X = 0V$



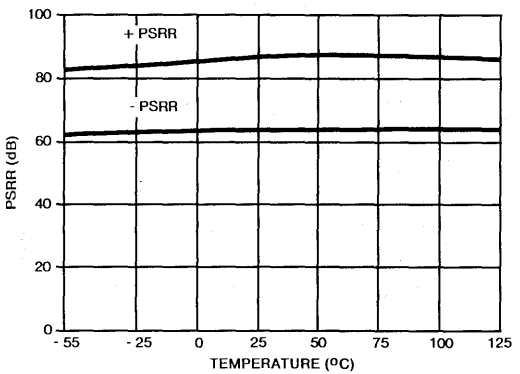
SUPPLY CURRENT vs TEMPERATURE



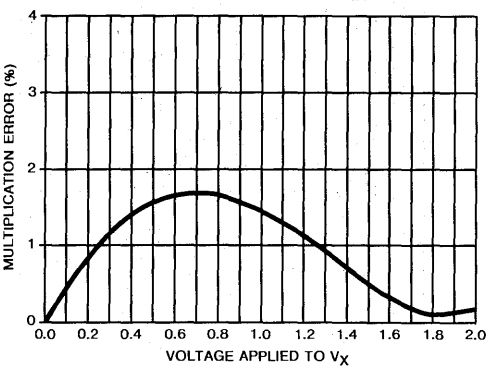
SIGNAL/CONTROL CMRR vs TEMPERATURE



PSRR vs TEMPERATURE



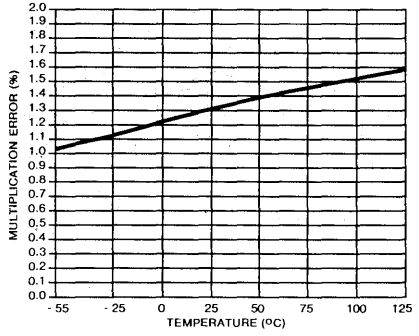
MULTIPLICATION ERROR vs V_X



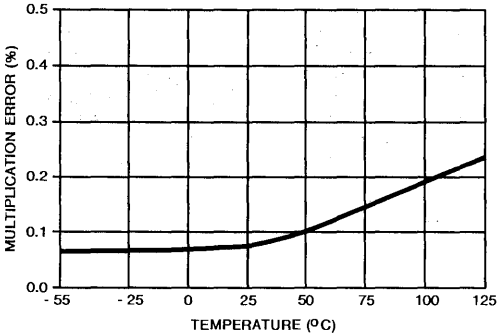
8 SPECIAL ANALOG CIRCUITS

Typical Performance Curves (Continued) $V_S = \pm 15V$, $T_A = +25^oC$, See test circuit for multiplier configuration

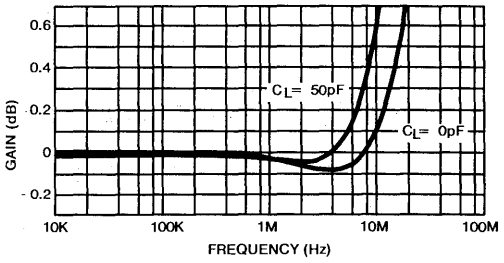
WORST CASE MULTIPLICATION ERROR vs TEMPERATURE



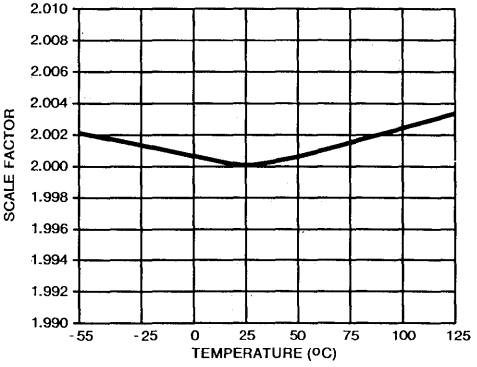
MULTIPLICATION ERROR vs TEMPERATURE
$V_Y = 5V$, $V_X = 2V$



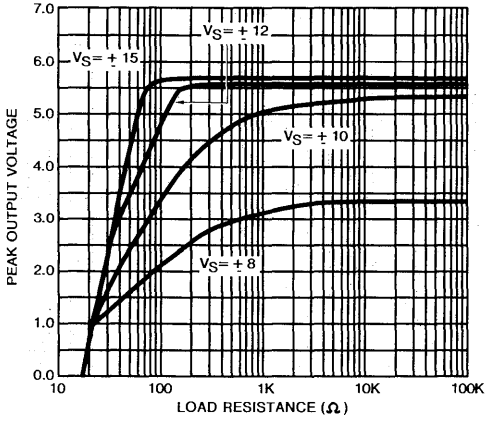
GAIN VARIATION vs FREQUENCY
$R_L = 1K$, $V_X = 2Vdc$, $V_Y = 200mVrms$



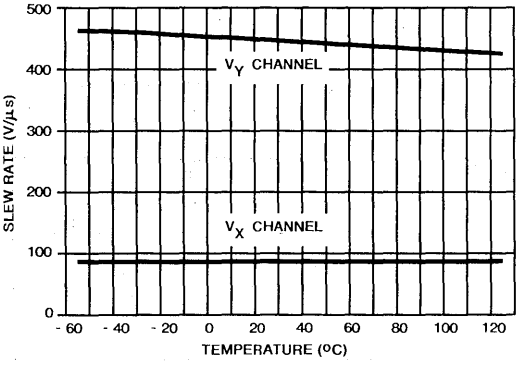
SCALE FACTOR vs TEMPERATURE



OUTPUT VOLTAGE SWING vs LOAD RESISTANCE
$f_O = 10kHz$, $V_X = 2Vdc$, THD < 0.1%

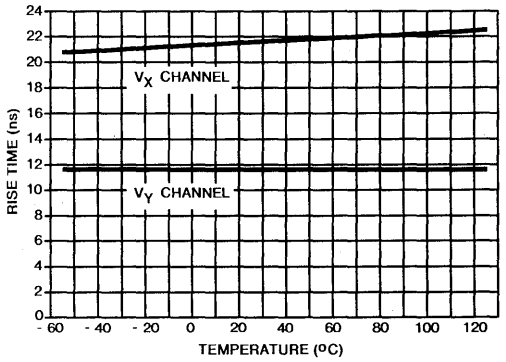


SLEW RATE vs TEMPERATURE

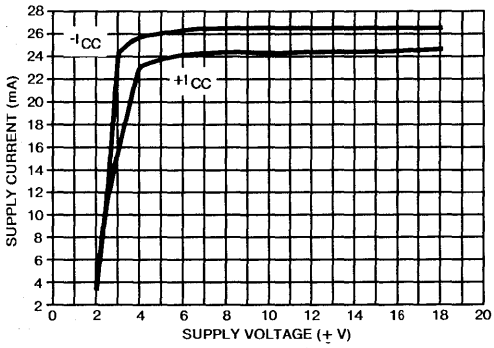


Typical Performance Curves (Continued) $V_S = \pm 15V$, $T_A = 25^oC$, See test circuit for multiplier configuration

RISE TIME vs TEMPERATURE



SUPPLY CURRENT vs SUPPLY VOLTAGE



Applications Information

Theory of Operation

The HA-2546 is a two quadrant multiplier with one differential signal channel, V_{Y+} and V_{Y-}, one differential control channel, V_{X+} and V_{X-}, and one differential input, V_{Z+} and V_{Z-}, to complete the feedback of the output amplifier. Figure 1 shows a detailed functional block diagram of the HA-2546. The differential voltages of channels V_X and V_Y are converted to differential currents. These currents are then multiplied in a circuit similar to a Gilbert Cell multiplier, producing a differential current product. The differential voltage of V_Z is converted to a differential current which sums with the product currents. The differential "product/sum" currents are converted to a single-ended current then converted to a voltage output by a transimpedance amplifier.

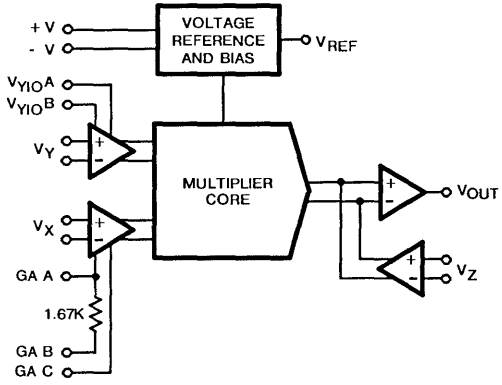


FIGURE 1.

The open loop transfer equation for the HA-2546 is:

$$V_{OUT} = A\left[\frac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})}{SF} - (V_{Z+} - V_{Z-})\right], \text{ where}$$

A = Output Amplifier Open Loop Gain
SF = Scale Factor
V_X, V_Y, V_Z = Differential Inputs

The scale factor is used to maintain the output of the multiplier within the normal operating range of ±5V. The scale factor can be defined by the user by way of an optional external resistor, R_{EXT}, and the Gain Adjust pins, Gain Adjust A (GA A), Gain Adjust B (GA B), and Gain Adjust C (GA C). The scale factor is determined as follows:

SF = 2, when GA B is shorted to GA C

SF ≈ 1.2* R_{EXT}, when R_{EXT} is connected between GA A and GA C (R_{EXT} is in kΩ)

SF ≈ 1.2* (R_{EXT} + 1.667kΩ), when R_{EXT} is connected to GA B and GA C (R_{EXT} is in kΩ)

The scale factor can be adjusted from 2 to 5. It should be noted that any adjustments to the scale factor will affect the AC performance of the control channel, V_X. The normal input operating range of V_X is equal to the scale factor voltage.

The typical multiplier configuration is shown in Figure 2. The ideal transfer function for this configuration is:

$$V_{OUT} = \begin{cases} \dfrac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})}{2} + V_{Z-} & \text{, when } (V_{X+} - V_{X-}) \geq 0 \\ 0 & \text{, when } (V_{X+} - V_{X-}) < 0 \end{cases}$$

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SPECIAL ANALOG CIRCUITS

Applications Information (Continued)

The V_{X-} pin is usually connected to ground so that when V_{X+} is negative there is no signal at the output, i.e. two quadrant operation. If the V_X input is a negative going signal the V_{X+} pin maybe grounded and the V_{X-} pin used as the input.

The V_{Y-} terminal is usually grounded allowing V_{Y+} to swing ±5 volts. The V_{Z+} terminal is usually connected directly to V_{OUT} to complete the feedback loop of the output amplifier while V_{Z-} is grounded. The scale factor is normally set to 2 by connecting GA B to GA C. Therefore the transfer function becomes:

$$V_{OUT} = \frac{(V_{X+})(V_{Y-})}{2}$$

The multiplication error is trimmed to be minimum at full scale, $V_X = 2V$ and $V_Y = 5V$. When $V_Y = 5V$, the worst case multiplication error occurs when $V_X \approx 0.65V$. See Typical Performance Curves.

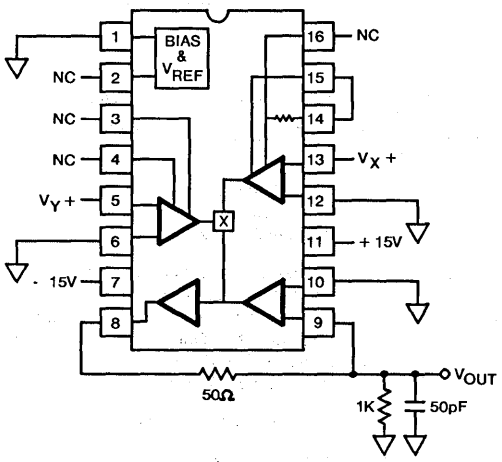


FIGURE 2.

Operation At Reduced Supply Voltages

The HA-2546 will operate over a range of supply voltages, ±8 to ±15 volts. Use of supply voltages below ±12 volts will cause degradation of electrical parameters.

Offset Adjustment

The signal channel offset voltage may be nulled by using a 20K potentiometer between V_{YIO} Adjust pins A and B and connecting the wiper to $-V_S$. Reducing the signal channel offset voltage will reduce V_X AC feedthrough and improve the multiplication error. Output offset voltage can also be nulled by connecting V_{Z-} to the wiper of a potentiometer which is tied between +V and -V.

Capacitive Drive Capability

When driving capacitive loads >20pF a 50Ω resistor should be connected between V_{OUT} and V_{Z-}, using V_{Z-} as the output (see Figure 2). This will prevent the multiplier from going unstable due to the pole created by the load capacitor and reduce gain peaking at higher frequencies.

Die Characteristics

Transistor Count		87
Die Dimensions		79.9 x 119.7 x 19 mils (2030 x 3040 x 480µm)
Substrate Potential*		V-
Process		High Frequency, Bipolar, DI
Passivation		Nitride
Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA1-2546	76	17

* The substrate maybe left floating (Insulating Die Mount) or it may be on a conductor at V- potential.

HARRIS

HA-2547

Wideband Two Quadrant Analog Multiplier

May 1990

Features

- Low Multiplication Error 1.6%
- Input Bias Currents 1.2μA
- Signal Input Feedthrough @ 5MHz ..... -50dB
- Wide Signal Bandwidth 100MHz
- Wide Control Bandwidth 22MHz

Applications

- Military Avionics
- Missile Guidance Systems
- Medical Imaging Displays
- Video Mixers
- Sonar AGC Processors
- Radar Signal Conditioning
- Voltage Controlled Amplifier
- Vector Generator

Description

The HA-2547 is a monolithic, high speed, two quadrant, analog multiplier constructed in Harris' Dielectrically Isolated High Frequency Process. The high frequency performance of the HA-2547 rivals the best analog multipliers currently available including hybrids.

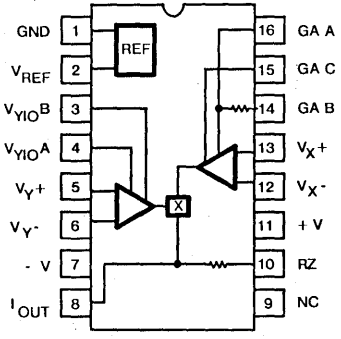
The single-ended current output of the HA-2547 has a 100MHz signal bandwidth (R_L = 50Ω) and a 22MHz control input bandwidth. High bandwidth and low distortion make this part an ideal component in video systems. The suitability for precision video applications is demonstrated further by low multiplication error (1.6%), low feedthrough (-50dB), and differential inputs with low bias currents (1.2μA). The HA-2547 is also well suited for mixer circuits as well as AGC applications for sonar, radar, and medical imaging equipment.

The current output of the HA-2547 allows it to achieve higher bandwidths than voltage output multipliers. An internal feedback resistor is provided to give an accurate current-to-voltage conversion and is trimmed to give a full scale output voltage of ±5 volts. The HA-2547 is not limited to multiplication applications only; frequency doubling and power detection are also possible.

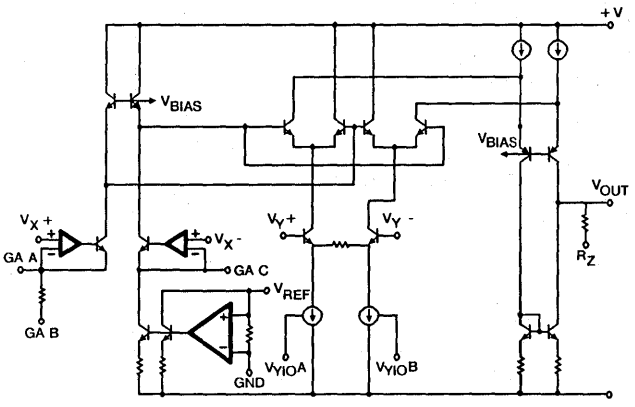
The HA-2547-9 has guaranteed operation from -40°C to +85°C, while the HA-2547-5 has guaranteed operation from 0°C to +75°C. The HA-2547 is available in a 16 pin Ceramic DIP. For MIL-STD-883 compliant product and LCC packages consult the HA-2547/883 datasheet.

Pinout

HA1-2547 (CERAMIC DIP)
TOP VIEW



Schematic



8 SPECIAL ANALOG CIRCUITS

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 35V
Differential Input Voltage..... 6V
Output Current 3mA

Operating Temperature Range

HA-2547-9..... $-40^{o}C \leq T_A \leq +85^{o}C$
HA-2547-5..... $0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range ..... $-65^{o}C \leq T_A \leq +150^{o}C$
Maximum Junction Temperature..... $+175^{o}C$

Electrical Specifications +V = +15V, -V = -15V, R_Z (Pin 10) Grounded, Unless Otherwise Specified

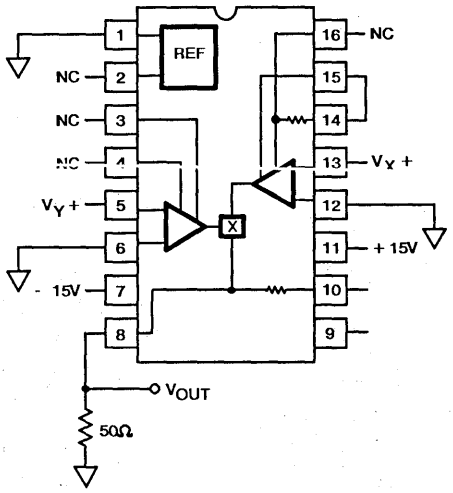
PARAMETER	TEMP	HA-2547-9			HA-2547-5			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
MULTIPLIER PERFORMANCE								
Multiplication Error (Note 2)	+25°C	-	1.6	3	-	1.6	3	%FS
	Full	-	3.0	7	-	3.0	7	%FS
Multiplication Error Drift	Full	-	0.003	-	-	0.003	-	%/°C
Scale Factor Error	Full	-	0.7	5	-	0.7	5	%
THD+N (Note 3)	+25°C	-	0.03	-	-	0.03	-	%
Output Offset Voltage (Note 4)	+25°C	-	6	15	-	6	15	mV
	Full	-	14	20	-	14	20	mV
Average Offset Voltage Drift	Full	-	-	-	-	-	-	µV/°C
SIGNAL INPUT, V_Y								
Input Offset Voltage	+25°C	-	4	10	-	4	10	mV
	Full	-	8	20	-	8	20	mV
Average Offset Voltage Drift	Full	-	35	-	-	35	-	µV/°C
Input Bias Current	+25°C	-	7	15	-	7	15	µA
	Full	-	10	15	-	10	15	µA
Input Offset Current	+25°C	-	0.7	2	-	0.7	2	µA
	Full	-	1.0	3	-	1.0	3	µA
Input Differential Resistance	+25°C	-	720	-	-	720	-	kΩ
Small Signal Bandwidth (-3dB) (Notes 5, 10)	+25°C	-	100	-	-	100	-	MHz
Feedthrough (Note 13)	+25°C	-	-50	-	-	-50	-	dB
Differential Input Range	+25°C	±5	-	-	±5	-	-	Volts
Common Mode Range	+25°C	-	±9	-	-	±9	-	Volts
CMRR (Note 6)	Full	60	78	-	60	78	-	dB
V_Y TRANSIENT RESPONSE								
Rise Time (Note 15)	+25°C	-	5	-	-	5	-	ns
Propagation Delay	+25°C	-	3	-	-	3	-	ns
CONTROL INPUT, V_X								
Input Offset Voltage	+25°C	-	1	2	-	1	2	mV
	Full	-	2	20	-	2	20	mV
Average Offset Voltage Drift	Full	-	12	-	-	12	-	µV/°C
Input Bias Current	+25°C	-	1.2	2	-	1.2	2	µA
	Full	-	1.8	5	-	1.8	5	µA
Input Offset Current	+25°C	-	0.3	2	-	0.3	2	µA
	Full	-	0.4	3	-	0.4	3	µA
Input Differential Resistance	+25°C	-	360	-	-	360	-	kΩ
Small Signal Bandwidth (-3dB) (Notes 5, 10)	+25°C	-	22	-	-	22	-	MHz
Feedthrough (Note 14)	+25°C	-	-40	-	-	-40	-	dB
Input Range (Note 12)	Full	+2	-	-	+2	-	-	Volts
Common Mode Range	+25°C	-	±9	-	-	±9	-	Volts
CMMR (Note 7)	+25°C	-	75	-	-	75	-	dB
V_X TRANSIENT RESPONSE								
Rise Time (Note 16)	+25°C	-	15	-	-	15	-	ns
Propagation Delay	+25°C	-	25	-	-	25	-	ns
OUTPUT CHARACTERISTICS								
Full Scale Output Voltage (Note 8)	Full	-	±6.25	-	-	±6.25	-	Volts
Full Scale Output Current (Note 11)	+25°C	-	2	-	-	2	-	mA
Output Resistance	+25°C	-	4	-	-	4	-	MΩ
POWER SUPPLY								
PSRR (Note 9)	Full	58	63	-	58	63	-	dB
I_{CC}	Full	-	20	29	-	20	29	mA

NOTES:

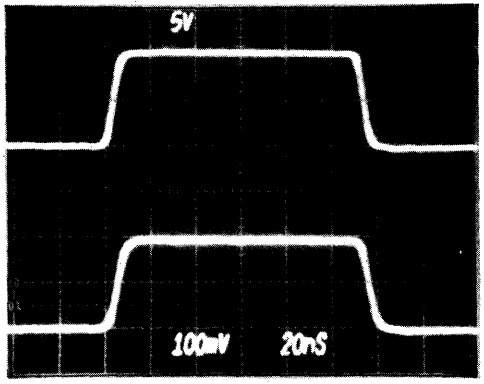
1. Absolute maximum ratings are limiting values, applied individually, beyond which the servicability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied
2. Error is percent of full scale, 1% = 50mV.
3. f_O = 10kHz, V_Y = 1Vrms, V_X = 2V.
4. V_X = 0V, V_Y = 0V.
5. R_L = 50Ω.
6. V_Y = 0 to ±5V, V_X = 2V.
7. V_X = 0 to 2V, V_Y = 5V.
8. V_Y = ±5, V_X = 2.5V.
9. V_S = ±12V to ±15V, V_Y = 5V, V_X = 2V.
10. Guaranteed by sample test and not 100% tested.
11. Output current tolerance is ±20%.
12. Scale Factor = 2. See Applications Information.
13. f_O = 5MHz, V_X = 0, V_Y = 200mVrms. Relative to full scale output.
14. f_O = 5MHz, V_Y = 0, V_X+ = 200mVrms, V_X- = -0.5V. Relative to full scale output.
15. V_Y = ±5V, V_X = 2V, R_L = 50Ω.
16. V_X = 0 to 2V, V_Y = 5V, R_L = 50Ω.

Test Circuits

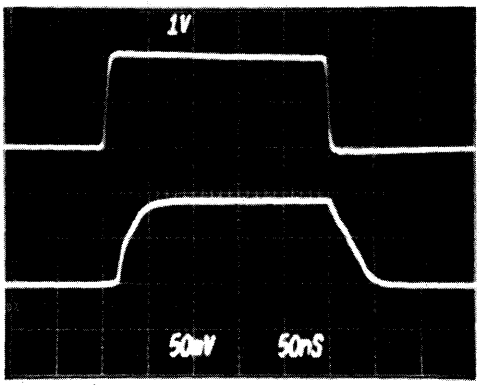
AC AND TRANSIENT RESPONSE TEST CIRCUIT



V_Y TRANSIENT RESPONSE
Vertical Scale: Top 5V/Div Bottom: 100mV/Div
Horizontal Scale: 20ns/Div

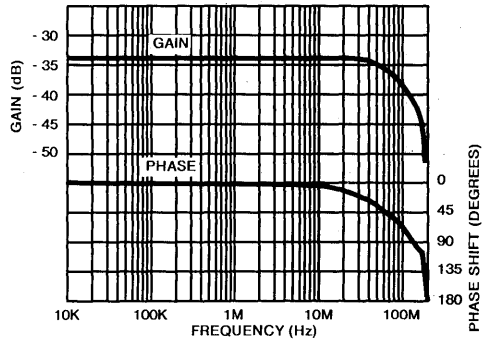


V_X TRANSIENT RESPONSE
Vertical Scale: Top 1V/Div Bottom: 50mV/Div
Horizontal Scale: 50ns/Div

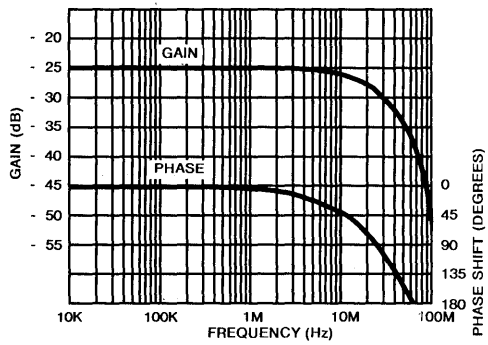


Typical Performance Curves $V_S = \pm15V$, $T_A = +25^oC$

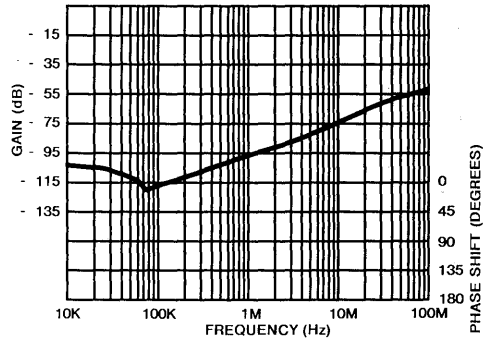
V_Y vs FREQUENCY
V_Y = 200mVrms, V_X = 2V, R_L = 50V



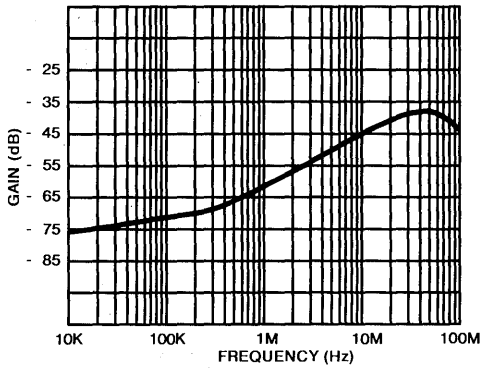
V_X vs FREQUENCY
V_{X+} = 100mVrms, V_{X-} = -1V, V_Y = 5V, R_L = 50Ω



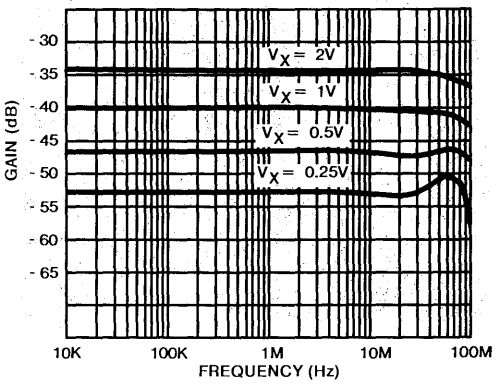
V_Y FEEDTHROUGH vs FREQUENCY
V_Y = 200mVrms, V_X = 0, R_L = 50Ω



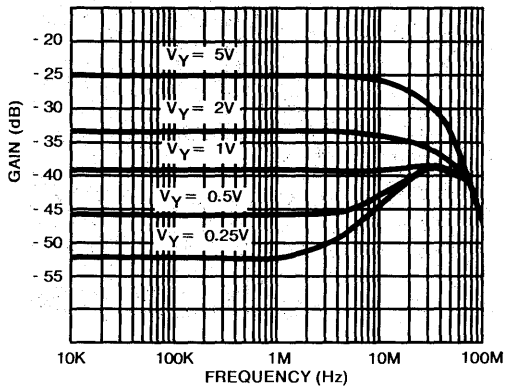
V_X FEEDTHROUGH vs FREQUENCY
V_{X+} = 200mVrms, V_{X-} = 0.5V, V_Y = 0V, R_L = 50Ω



VARIOUS V_Y FREQUENCY RESPONSES
V_Y = 200mVrms, R_L = 50Ω

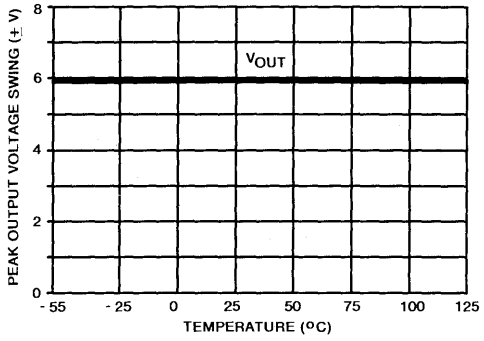


VARIOUS V_X FREQUENCY RESPONSES
V_{X+} = 100mVrms, V_{X-} = -1V, R_L = 50Ω

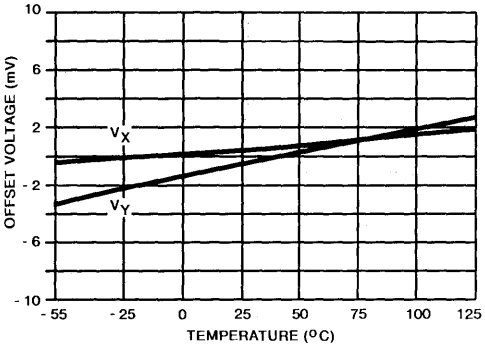


Typical Performance Curves (Continued) $V_S = \pm 15V$, $T_A = +25^oC$

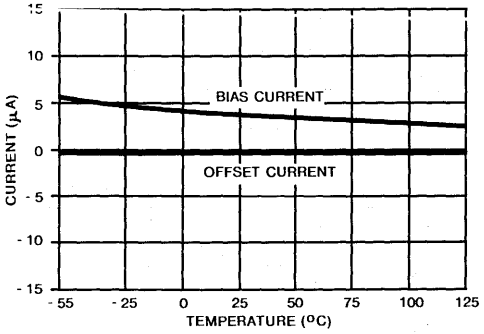
OUTPUT VOLTAGE SWING vs TEMPERATURE



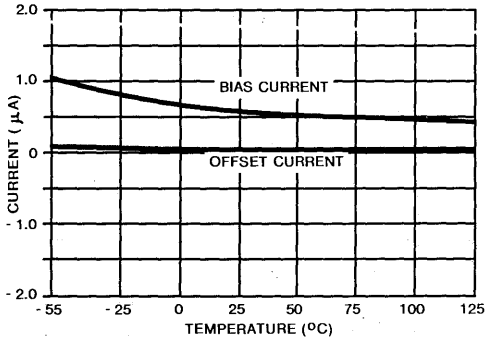
OFFSET VOLTAGE vs TEMPERATURE



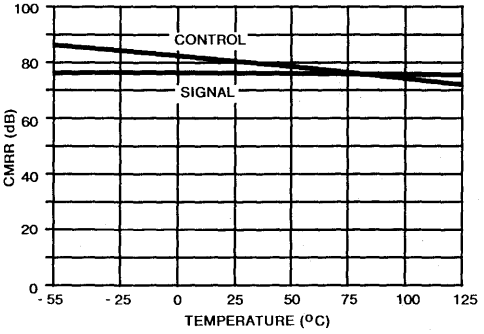
V_Y OFFSET/BIAS CURRENT vs TEMPERATURE



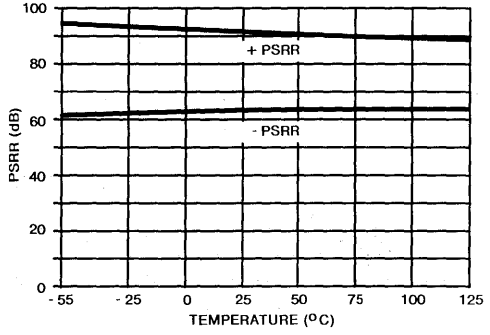
V_X OFFSET/BIAS CURRENT vs TEMPERATURE



SIGNAL/CONTROL CMRR vs TEMPERATURE

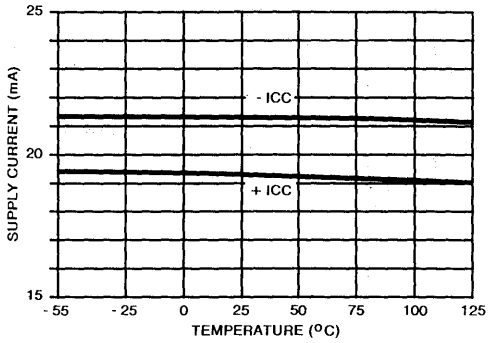


PSRR vs TEMPERATURE

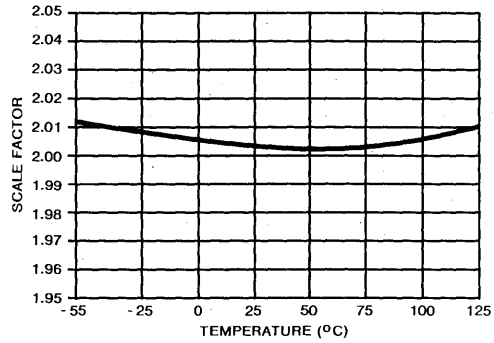


Typical Performance Curves (Continued) $V_S = \pm 15V$, $T_A = +25^oC$

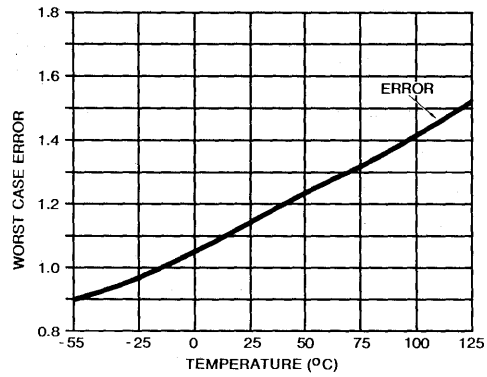
I_{CC} vs TEMPERATURE



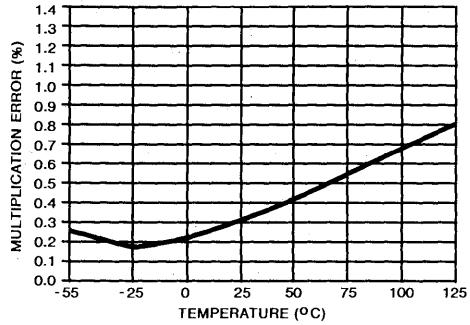
SCALE FACTOR vs TEMPERATURE



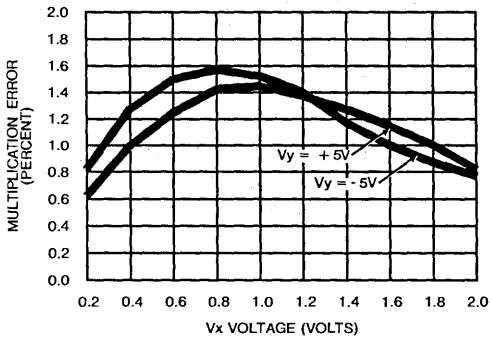
WORST CASE MULTIPLICATION ERROR vs TEMPERATURE



MULTIPLICATON ERROR vs TEMPERATURE
$V_X = 2V$, $V_Y = 5V$



MULTIPLICATION ERROR vs V_X
$V_Y = +5V$ and $-5V$



Die Characteristics

Transistor Count	75
Die Dimensions	79.9 x 119.7 x 19 mils (2030 x 3040 x 480µm)
Substrate Potential*	V-
Process	High Frequency, Bipolar, DI
Passivation	Nitride

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA1 -2547	76	17.3

* The substrate maybe left floating (Insulating Die Mount) or it may be on a conductor at V- potential.

Applications Information

Theory of Operation

The HA-2547 is a current output, two quadrant multiplier with one differential signal channel, V_{Y+} and V_{Y-}, and one differential control channel, V_{X+} and V_{X-}. Figure 1 shows a detailed functional block diagram of the HA-2547. The differential voltages of channels V_X and V_Y are converted to differential currents. These differential currents are then multiplied in a circuit similar to a Gilbert Cell multiplier, producing a differential current product. The differential product currents are then converted to a single-ended output current which is typically 2mA, ±20% at full scale (V_X = 2V , V_Y = ±5V). A trimmed internal scaling resistor, R_Z, is designed to convert the output current to an accurate voltage by grounding R_Z (pin 10). R_Z is trimmed such that at full scale output current the voltage drop across R_Z will be ±5.0 volts.

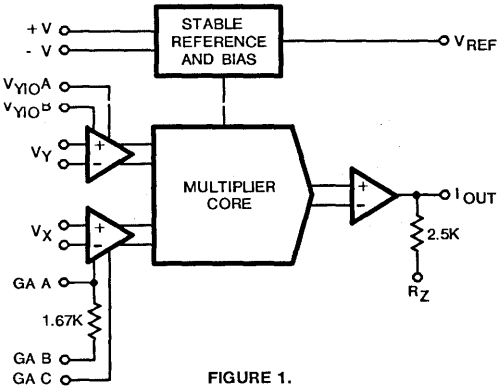


FIGURE 1.

The transfer equation for the HA-2547 is:

$$I_{OUT} \approx \frac{(V_{X+} - V_{X-})(V_{Y+} - V_{Y-})(0.4mA)}{SF} \quad \text{, where}$$

SF = Scale Factor

V_X, V_Y = Differential Inputs

The scale factor is used to maintain the output of the multiplier within the normal operating range of ±5V. The scale factor can be defined by the user by way of an optional external resistor, R_{EXT}, and the Gain Adjust pins: Gain Adjust A (GA A), Gain Adjust B (GA B), and Gain Adjust C (GA C). The scale factor is determined as follows:

SF = 2, when GA B is shorted to GA C

SF ≈ (1.2)(R_{EXT}), when R_{EXT} is connected between GA A and GA C (R_{EXT} is in kΩ)

SF ≈ (1.2)(R_{EXT} + 1.667kΩ), when R_{EXT} is connected to GA B and GA C (R_{EXT} is in kΩ).

The scale factor can be adjusted from 2 to 5. It should be noted that any adjustments to the scale factor will affect the AC performance of the control channel, V_X. The normal input operating range of V_X is equal to the scale factor value.

A typical multiplier configuration is shown in Figure 2. The ideal transfer function for this configuration is shown below, illustrating two quadrant operation:

$$V_{OUT} = \begin{cases} \dfrac{(V_{X+} - V_{X-})(V_{Y+} - V_Y)}{2} & \text{,when } (V_{X+} - V_{X-}) \geq 0 \\ 0 & \text{,when } (V_{X+} - V_{X-}) < 0 \end{cases}$$

The V_{X-} pin is usually connected to ground so that when V_{X+} is negative there is no signal at the output, i.e. two quadrant operation. If the V_X input is a negative going signal the V_{X+} pin maybe grounded and the V_{X-} pin used as the input. The V_{Y-} terminal is usually grounded allowing V_{Y+} to swing ±5 volts. R_Z is normally used as a feedback resistor for an external op amp to provide an accurate current-to-voltage conversion. The scale factor is normally set to 2 by connecting GA B to GA C. Therefore, the transfer function becomes:

$$V_{OUT} = \frac{(V_{X+})(V_{Y+})}{2}$$

The multiplication error is trimmed to be minimum at full scale, V_X = 2V and V_Y = ±5V. When V_Y = ±5V, the worst case multiplication error occurs when $V_X \approx$ 0.8V (Refer to typical performance curves).

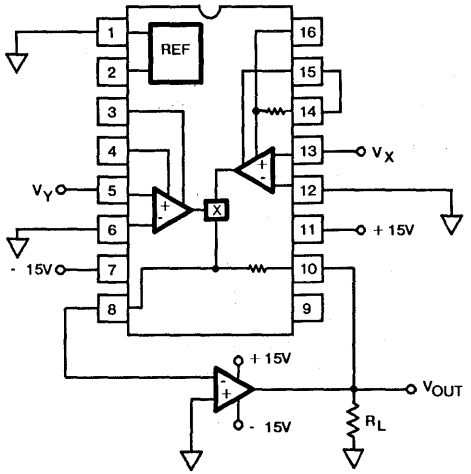


FIGURE 2.

Operation At Various Supply Voltages

The HA-2547 will operate over a range of supply voltages, ±8 to ±15 volts. Use of supply voltages below ±12 volts will cause degradation of electrical parameters.

Offset Adjustment

The signal channel offset voltage may be nulled by using a 20K potentiometer between V_{YIO} Adjust pins A and B and connecting the wiper to $-V_S$. Reducing the signal channel offset voltage will reduce V_X AC feedthrough and improve the multiplication error. Output offset voltage can also be nulled by connecting V_{Z-} to the wiper of a potentiometer which is tied between +V and -V.

HARRIS

HA-5002

Monolithic, Wideband, High Slew Rate, High Output Current Buffer

May 1990

Features

- Voltage Gain 0.995
- High Input Impedance 3000kΩ
- Low Output Impedance 3Ω
- Very High Slew Rate 1300V/μsec
- Very Wide Bandwidth 110MHz
- High Output Current ..... ±200mA
- Pulsed Output Current 400mA
- Monolithic Construction

Applications

- Line Driver
- Data Acquisition
- 110MHz Buffer
- High Power Current Booster
- High Power Current Source
- Sample and Holds
- Radar Cable Driver
- Video Products

Description

The HA-5002 is a monolithic, wideband, high slew rate, high output current, buffer amplifier.

Utilizing the advantages of the Harris D.I. technologies, the HA-5002 current buffer offers 1300V/μsec slew rate with 110MHz of bandwidth. The ±200mA output current capability is enhanced by a 3Ω output impedance.

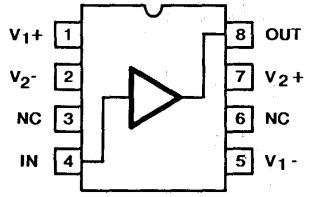
The monolithic HA-5002 will replace the hybrid LH0002 with corresponding performance increases. These characteristics range from the 3000kΩ input impedance to the increased output voltage swing. Monolithic design technologies have allowed a more precise buffer to be developed with more than an order of magnitude smaller gain error.

The HA-5002 will provide many present hybrid users with a higher degree of reliability and at the same time increase overall circuit performance.

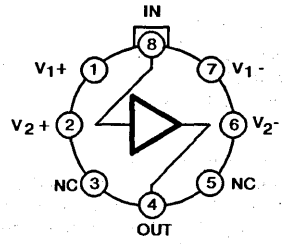
The HA-5002 is available in an 8 pin SOIC package, an 8 pin Metal Can, and 8 pin Ceramic and Plastic Mini-DIPs. For the military grade product, refer to the HA-5002/883 Data Sheet.

Pinouts

HA9P5002 (SOIC)
HA7-5002 (CERAMIC DIP)
HA3-5002 (PLASTIC DIP)
TOP VIEW

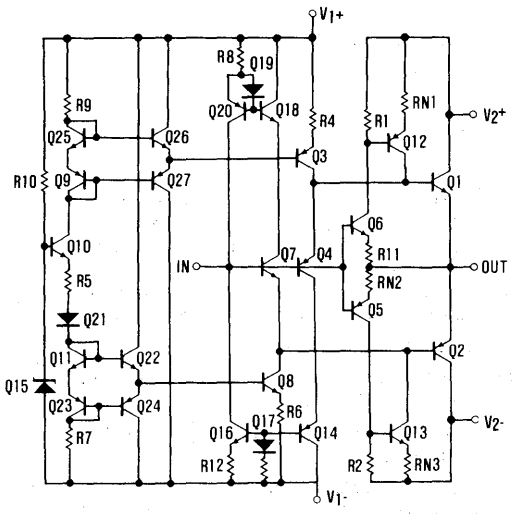


HA2-5002 TO-99 (METAL CAN)
TOP VIEW



LCC Package Available for HA-5002/883.
See HA-5002/883 Data Sheet

Schematic



Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- pins 44V
Input Voltage ..... Equal to Supplies
Output Current ..... Continuous ±200mA
Output Current ..... (50ms On, 1s Off) ±400mA
Internal Power Dissipation (Note 2)
TO-99 (+25°C) 1.13W
Mini-DIP (+25°C) 1.22W
Plastic DIP (+25°C) 1.88W

Operating Temperature Range

Maximum Junction Temperature ..... +175°C
HA-5002-2 ..... $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-5002-5 ..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
HA-5002-9 ..... $-40^{\circ}C \leq T_A \leq +85^{\circ}C$
Storage Temperature Range ..... $-65^{\circ}C \leq T_A \leq +150^{\circ}C$

Electrical Specifications V_{SUPPLY} = ±12V to ±15V, R_S = 50Ω, R_L = 1kΩ, C_L = 10pF, Unless Otherwise Specified.

PARAMETER		TEMP	HA-5002-2 MIN	HA-5002-2 TYP	HA-5002-2 MAX	HA-5002-5, -9 MIN	HA-5002-5, -9 TYP	HA-5002-5, -9 MAX	UNITS
INPUT CHARACTERISTICS									
Offset Voltage		+25°C	-	5	20	-	5	20	mV
		Full	-	10	30	-	10	30	mV
Average Offset Voltage Drift		Full	-	30	-	-	30	-	µV/°C
Bias Current		+25°C	-	2	7	-	2	7	µA
		Full	-	3.4	10	-	2.4	10	µA
Input Resistance		Full	1.5	3	-	1.5	3	-	MΩ
Input Noise Voltage (10Hz-1MHz)		+25°C	-	4	-	-	4	-	µVp-p
TRANSFER CHARACTERISTICS									
Voltage Gain (Note 7)	R_L = 100Ω	+25°C	-	0.971	-	-	0.971	-	V/V
	R_L = 1kΩ	+25°C	-	0.995	-	-	0.995	-	V/V
	R_L = 1kΩ	Full	0.990	-	-	0.980	-	-	V/V
-3dB Bandwidth (Note 4)		+25°C	-	110	-	-	110	-	MHz
AC Current Gain		+25°C	-	40	-	-	40	-	A/mA
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 100Ω	+25°C	±10	±10.7	-	±10	±11.2	-	V
	R_L = 1kΩ (Note 3)	Full	±10	±13.5	-	±10	±13.9	-	V
	R_L = 1kΩ (Note 5)	Full	±10	±10.5	-	±10	±10.5	-	V
Output Resistance		Full	-	3	10	-	3	10	Ω
Harmonic Distortion (Note 6)		+25°C	-	<0.005	-	-	<0.005	-	%
TRANSIENT RESPONSE									
Full Power Bandwidth (Note 8)		+25°C	-	11	-	-	11	-	MHz
Rise Time		+25°C	-	3.6	-	-	3.6	-	ns
Propagation Delay		+25°C	-	2	-	-	2	-	ns
Overshoot		+25°C	-	30	-	-	30	-	%
Slew Rate		+25°C	1.0	1.3	-	1.0	1.3	-	V/ns
Settling Time to 0.1%		+25°C	-	50	-	-	50	-	ns
POWER REQUIREMENTS									
Supply Current		+25°C	-	8.3	-	-	8.3	-	mA
		Full	-	-	10	-	-	10	mA
Power Supply Rejection Ratio (Note 9)		Full	54	64	-	54	64	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. See thermal constants data in Die Characteristics section.
3. V_{SUPPLY} = ±15V
4. $V_{IN} = 1V_{p-p}$
5. V_{SUPPLY} = ±12V
6. $V_{IN} = 1V_{RMS}$; f = 10kHz.
7. V_{OUT} = ±10V
8. V_{OUT} = 10Vp-p
9. ΔV_{SUPPLY} = 10V

Operating Instructions

Layout Considerations

The wide bandwidth of the HA-5002 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance.

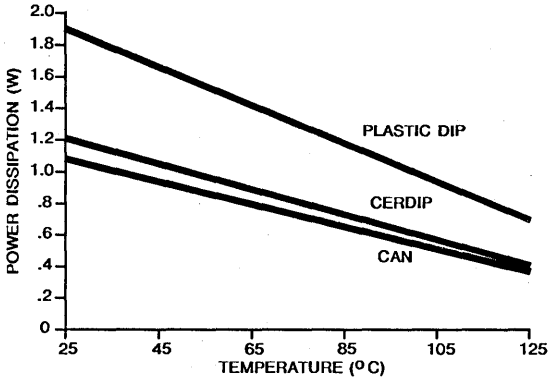
Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

Power Supply Decoupling

For optimal device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1µF will minimize high frequency variations in supply voltage, while low frequency bypassing requires larger valued capacitors since the impedance of the capacitor is dependent on frequency.

It is also recommended that the bypass capacitors be connected close to the HA-5002 (preferably directly to the supply pins).

FREE AIR POWER DISSIPATION



$$P_{dmax} = \frac{T_{jmax} - T_A}{\theta_{j-c} + \theta_{c-s} + \theta_{s-a}}$$

Where: T_{jmax} = Maximum Junction Temperature of the Device

T_A = Ambient

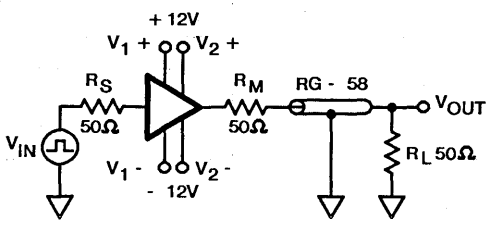
θ_{j-c} = Junction to Case Thermal Resistance

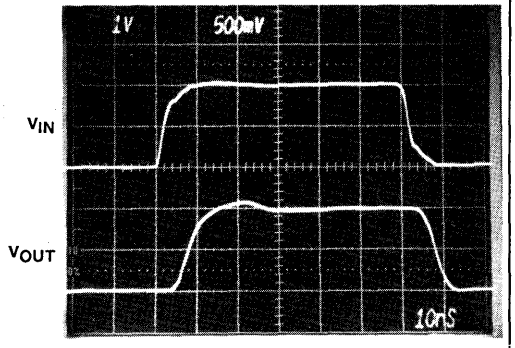
θ_{c-s} = Case to Heat Sink Thermal Resistance

θ_{s-a} = Heat Sink to Ambient Thermal Resistance

Test Circuits

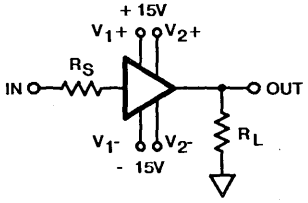
COAXIAL CABLE DRIVER - 50Ω SYSTEM



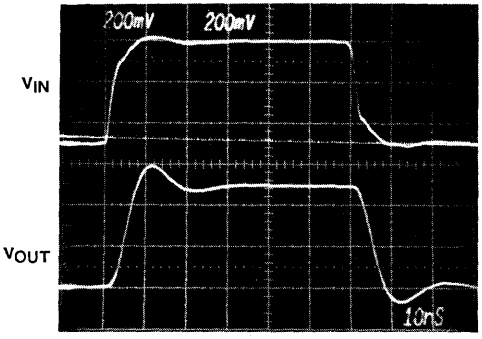


Test Circuits

LARGE AND SMALL SIGNAL RESPONSE

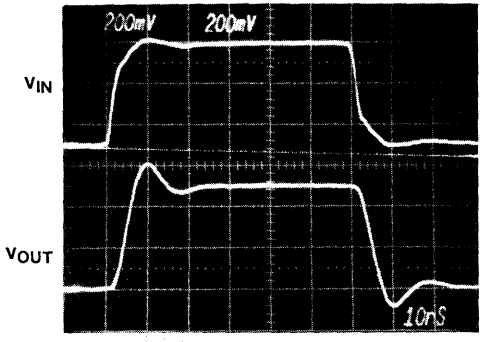


SMALL SIGNAL WAVEFORMS



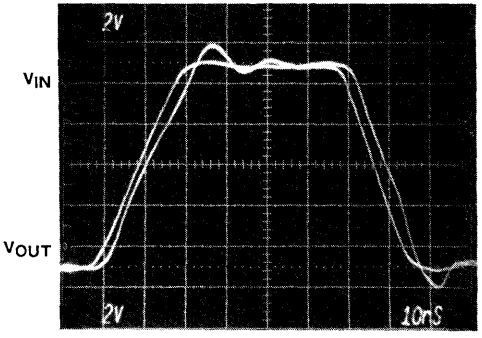
R_S = 50Ω
R_L = 100Ω

SMALL SIGNAL WAVEFORMS



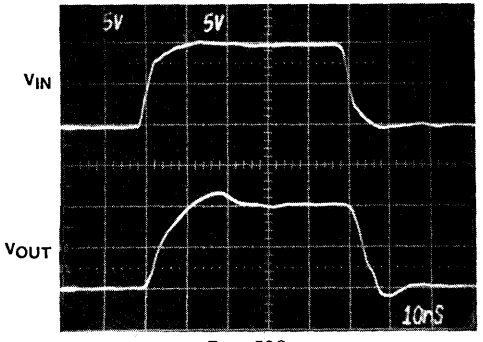
R_S = 50Ω
R_L = 1kΩ

LARGE SIGNAL WAVEFORMS



R_S = 50Ω
R_L = 1kΩ

LARGE SIGNAL WAVEFORMS

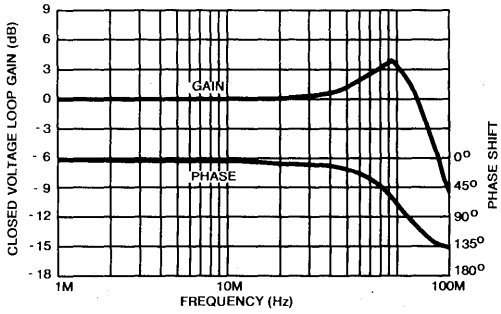


R_S = 50Ω
R_L = 1kΩ

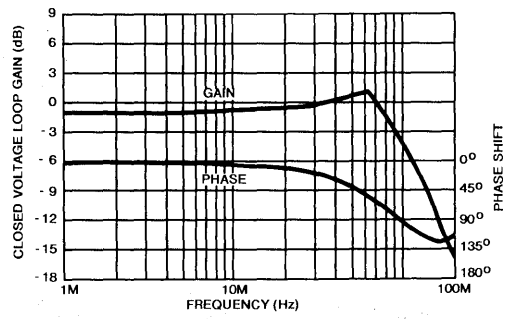
8 SPECIAL ANALOG CIRCUITS

Typical Performance Curves

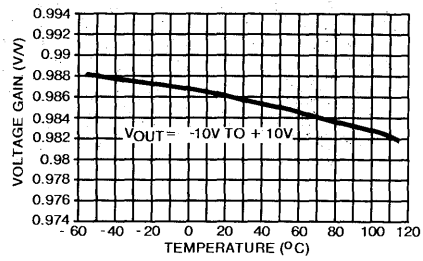
GAIN/PHASE vs. FREQUENCY
V_{CC} = ±15V, R_L = 1K, R_S = 50Ω



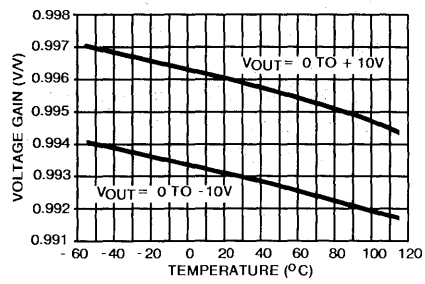
GAIN/PHASE vs. FREQUENCY
V_{CC} = ±15V, R_L = 50Ω, R_S = 50Ω



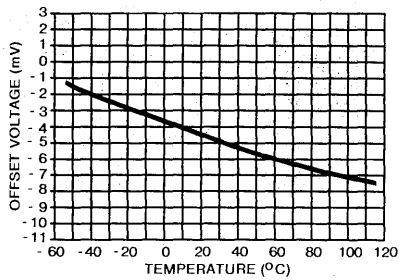
VOLTAGE GAIN vs. TEMPERATURE
V_{CC} = ±15V, R_{LOAD} = 100Ω



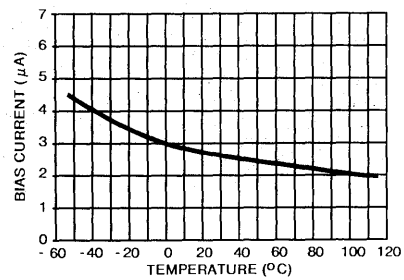
VOLTAGE GAIN vs. TEMPERATURE
V_{CC} = ±15V, R_{LOAD} = 1kΩ



OFFSET VOLTAGE vs. TEMPERATURE
V_{CC} = ±15V

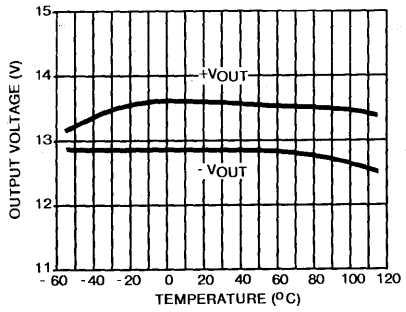


BIAS CURRENT vs. TEMPERATURE
V_{CC} = ±15V

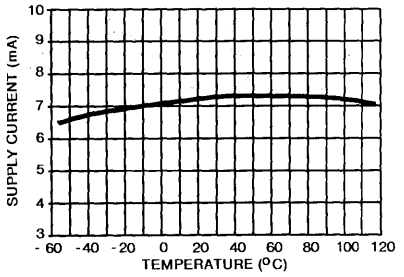


Typical Performance Curves (Continued)

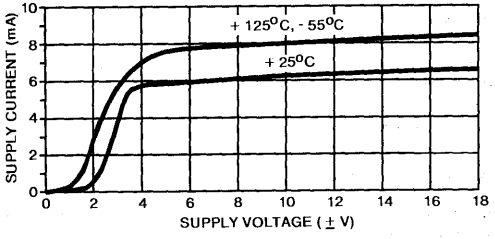
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE
V_{CC} = ±15V, R_{LOAD} = 100Ω



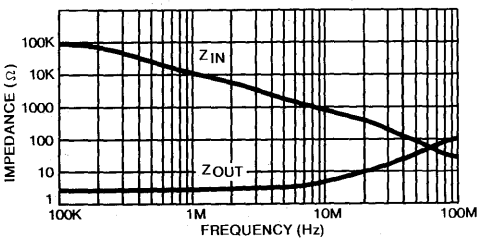
SUPPLY CURRENT vs. TEMPERATURE
V_{CC} = ±15V, I_{OUT} = 0mA



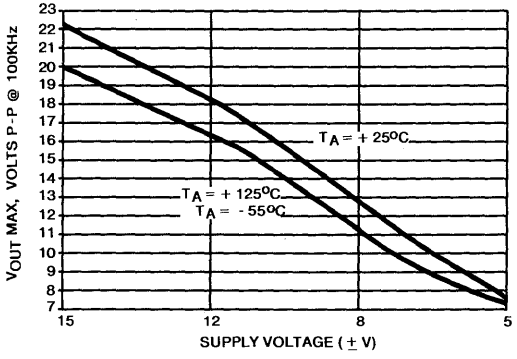
SUPPLY CURRENT vs. SUPPLY VOLTAGE
I_{OUT} = 0mA



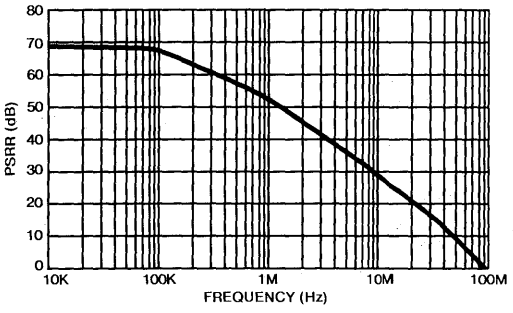
INPUT/OUTPUT IMPEDANCE vs. FREQUENCY
V_{CC} = ±15V



V_{OUT} MAXIMUM vs. V_{SUPPLY}
R_{LOAD} = 100Ω



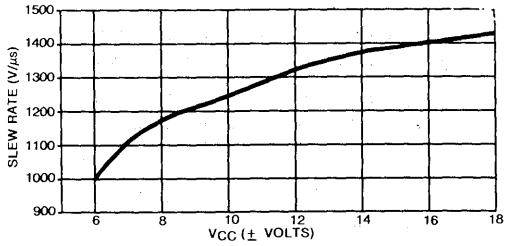
PSRR vs. FREQUENCY



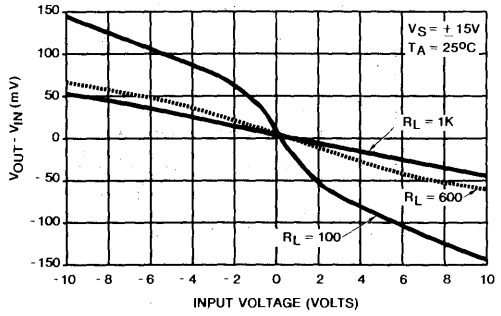
8 SPECIAL ANALOG CIRCUITS

Typical Performance Curves (Continued)

SLEW RATE vs. SUPPLY VOLTAGE



GAIN ERROR vs. INPUT VOLTAGE



Typical Applications

OPERATION AT REDUCED SUPPLY LEVELS

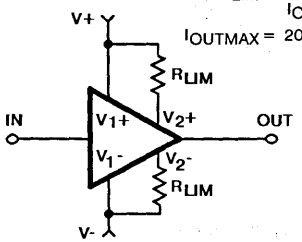
The HA-5002 can operate at supply voltage levels as low as ±5V and lower. Output swing is directly affected as well as slight reductions in slew rate and bandwidth.

SHORT CIRCUIT PROTECTION

The Output current can be limited by using the following circuit:

$$R_{LIM} = \frac{V+}{I_{OUTMAX}} = \frac{V-}{I_{OUTMAX}}$$

I_{OUTMAX} = 200mA (CONTINUOUS)



CAPACITIVE LOADING

The HA-5002 will drive large capacitive loads without oscillation but peak current limits should not be exceeded. Following the formula $I = C\frac{dv}{dt}$ implies that the slew rate or the capacitive load must be controlled to keep peak current below the maximum or use the current limiting approach as shown. The HA-5002 can become unstable with small capacitive loads (50pF) if certain precautions are not taken. Stability is enhanced by any one of the following: a source resistance in series with the input of 50Ω to 1K; increasing capacitive load to 150pF or greater; decreasing C_{LOAD} to 20pF of less; adding an output resistor of 10Ω to 50Ω; or adding feedback capacitance of 50pF or greater. Adding source resistance generally yields the best results.

Die Characteristics

Transistor Count 27

Die Dimensions ..... 80 x 81 x 19 mils (2030μm x 2050μm x 480μm)

Substrate Potential* ..... V-

Process ..... Bipolar-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
HA7-5002 Ceramic Mini-DIP	123	46
HA3-5002 Plastic DIP	80	20
HA2-5002 Metal Can	133	40
HA9P5002 SOIC	160	42

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS HA-5033

July 1990

Video Buffer

Features

- Differential Phase Error ..... 0.1 Degree
- Differential Gain Error 0.1%
- High Slew Rate 1300V/μs
- Wide Bandwidth (Small Signal) 250MHz
- Wide Power Bandwidth ..... DC to 65MHz
- Fast Rise Time 3ns
- High Output Drive ..... ±8V With 100Ω Load
- Wide Power Supply Range ..... ±5V to ±16V
- Replace Costly Hybrids

Applications

- Video Buffer
- High Frequency Buffer
- Isolation Buffer
- High Speed Line Driver
- Impedance Matching
- Current Boosters
- High Speed A/D Input Buffers
- For Further Application Ideas, See App. Note 548

Description

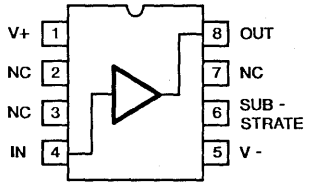
The HA-5033 is a unity gain monolithic I.C. designed for any application requiring a fast, wideband buffer. Featuring a bandwidth of 250MHz and outsanding differential phase/gain characteristics, this high performance voltage follower is an excellent choice for video circuit design. Other features, which include a minimum slew rate of 1000V/μs and high output drive capability, make the HA-5033 applicable for line driver and high speed data conversion circuits.

The high performance of this product is a result of the Harris Dielectric Isolation process. A major feature of this process is that it produces both PNP and NPN high frequency transistors which makes wide bandwidth designs, such as the HA-5033, practical. Alternative process methods typically produce a lower AC performance.

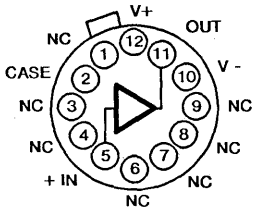
The HA-5033 is available in a 12 pin (TO-8) Metal Can or an 8 pin Plastic Mini-DIP. SOIC packaging is also available with -5 and -9 temperature options.

Pinouts

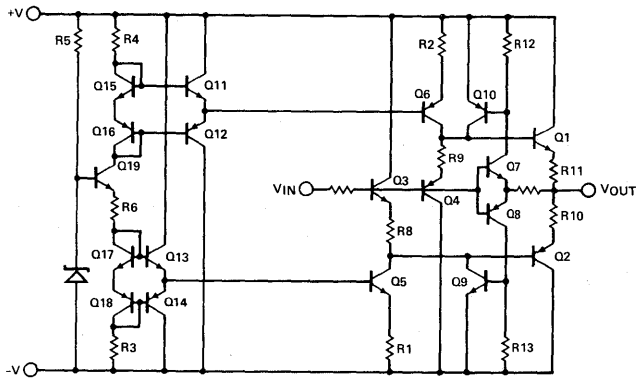
HA3-5033 (PLASTIC MINI-DIP)
HA9P5033 (SOIC)
TOP VIEW



HA2-5033 (TO-8 METAL CAN)
TOP VIEW



Schematic



8 SPECIAL ANALOG CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Pins 40V
Input Voltage ..... Equal to Supplies
Output Current (Peak) (50ms On/1 Second Off) ..... ±200mA
Internal Power Dissipation (Note 2)
TO-8 (+25°C) 1.75W
Mini-DIP (+25°C) 1.95W

Operating Temperature Ranges

HA-5033-2 ..... $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
HA-5033-5 ..... $0^{\circ}C \leq T_A \leq +75^{\circ}C$
HA-5033-9 ..... $-40^{\circ}C \leq T_A \leq +85^{\circ}C$
Storage Temperature Range ..... $-65^{\circ}C \leq T_A \leq +150^{\circ}C$
Maximum Junction Temperature ..... +175°C

Electrical Specifications $V_{SUPPLY} = \pm 12V$, $R_S = 50\Omega$, $R_L = 100\Omega$, $C_L = 10pF$, Unless Otherwise Specified.

PARAMETER	TEMP	HA-5033-2 MIN	HA-5033-2 TYP	HA-5033-2 MAX	HA-5033-5 MIN	HA-5033-5 TYP	HA-5033-5 MAX	NOTE 10 HA-5033-9 MAX	UNITS
INPUT CHARACTERISTICS									
Offset Voltage	+25°C	-	5	15	-	5	15	15	mV
	Full	-	6	25	-	6	25	30	mV
Average Offset Voltage Drift	Full	-	33	-	-	33	-	-	µV/°C
Bias Current	+25°C	-	20	35	-	20	35	35	µA
	Full	-	30	50	-	30	50	50	µA
Input Resistance	+25°C	-	1.5	-	-	1.5	-	-	MΩ
Input Capacitance	+25°C	-	1.6	-	-	1.6	-	-	pF
Input Noise Voltage (Note 3)	+25°C	-	20	-	-	20	-	-	µVp-p
TRANSFER CHARACTERISTICS									
Voltage Gain									
$R_L = 100\Omega$	+25°C	0.93	-	-	0.93	-	-	-	V/V
$R_L = 1k\Omega$	+25°C	0.93	0.99	-	0.93	0.99	-	-	V/V
$R_L = 100\Omega$	Full	0.92	-	-	0.92	-	-	-	V/V
-3dB Bandwidth	+25°C	-	250	-	-	250	-	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing									
$R_L = 100\Omega$	Full	+8	±10	-	±8	±10	-	-	V
$R_L = 1k\Omega$ (Note 4)	Full	±11	±12	-	±11	±12	-	-	V
Output Current	+25°C	±80	±100	-	±80	±100	-	-	mA
Output Resistance	+25°C	-	5	-	-	5	-	-	Ω
Full Power Bandwidth									
(Note 5)	+25°C	-	65	-	-	65	-	-	MHz
(Note 7)	+25°C	15.9	-	-	15.9	-	-	-	MHz
TRANSIENT RESPONSE									
Rise Time (Note 6)	+25°C	-	3	-	-	3	-	-	ns
Propagation Delay	+25°C	-	1	-	-	1	-	-	ns
Overshoot	+25°C	-	10	-	-	10	-	-	%
Slew Rate (Note 7)	+25°C	1	1.3	-	1	1.3	-	-	V/ns
Settling Time to 0.1%	+25°C	-	50	-	-	50	-	-	ns
Differential Phase Error (Note 8)	+25°C	-	0.1	-	-	0.1	-	-	Degree
Differential Gain Error (Note 8)	+25°C	-	0.1	-	-	0.1	-	-	%
POWER SUPPLY CHARACTERISTICS									
Supply Current	+25°C	-	21	25	-	21	25	25	mA
	Full	-	21	30	-	21	30	30	mA
Power Supply Rejection Ratio	Full	54	-	-	54	-	-	-	dB
Harmonic Distortion (Note 9)	+25°C	-	<0.1	-	-	<0.1	-	-	%

NOTES:

1. Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. TO-8: $\theta_{ja} = 101^{\circ}C/W$, $\theta_{jc} = 33^{\circ}C/W$ Recommended heat sinks for the TO-8: Thermalloy 2240A, $\theta_{sa} = 27^{\circ}C/W$, IERC Up-TO-8-48CB, $\theta_{sa} = 10^{\circ}C/W$. Mini-DIP: $\theta_{ja} = 91^{\circ}C/W$, $\theta_{sa} = 40^{\circ}C/W$.
3. 10Hz to 1MHz
4. $\pm V_{SUPPLY} = \pm 15V$
5. $V_{OUT} = 1V_{RMS}$, $R_L = 1k\Omega$
6. $V_{OUT} = 500mV$
7. $\pm V_{SUPPLY} = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L = 1k\Omega$.
8. Differential gain and phase error are non-linear signal distortions found in video systems and are defined as follows: Differential gain error is defined as the change in amplitude at the color subcarrier frequency as the picture signal is varied from blanking to white level. Differential phase error is defined as the change in the phase of the color subcarrier as the picture signal is varied from blanking to white level. Differential gain and phase error were too small to be measured with a Tektronix 520A NTSC Vector Scope.
9. $V_{IN} = 1V_{RMS}$
10. Typical and minimum specification for the -9 version are the same as those for the -5 version.

Operating Instructions

Layout Considerations

The wide bandwidth of the HA-5033 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance. This ground plane shielding can also incorporate the metal case of the HA-5033 since pin #2 is internally tied to the package. This feature allows the user to make metal to metal contact between the ground plane and the package, which extends shielding, provides additional heat sinking and eliminates the use of a socket, IC sockets contribute inter-lead capacitance which limits device bandwidth and should be avoided.

For the epoxy Mini-DIP, pin 6 can be tied to either supply, grounded, or simply not used. But to optimize device performance and improve isolation, it is recommended that this pin be grounded.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

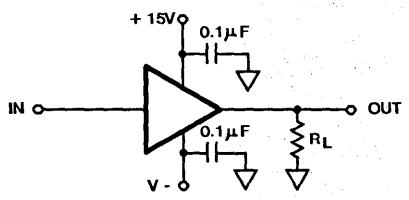
Power Supply Decoupling

For optimum device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01 to 0.1μF will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1μF or larger will optimize low frequency performance.

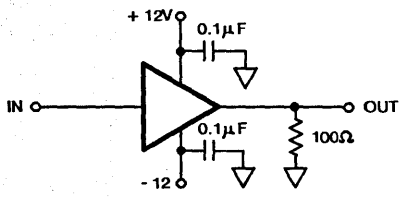
It is also recommended that the bypass capacitors be connected close to the HA-5033 (preferably directly to the supply pins).

Test Circuits

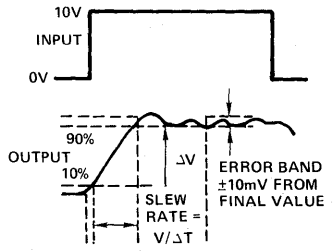
SLEW RATE AND SETTLING TIME



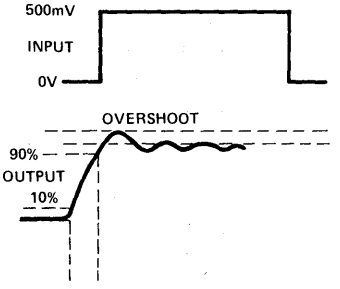
TRANSIENT RESPONSE



SETTLING TIME



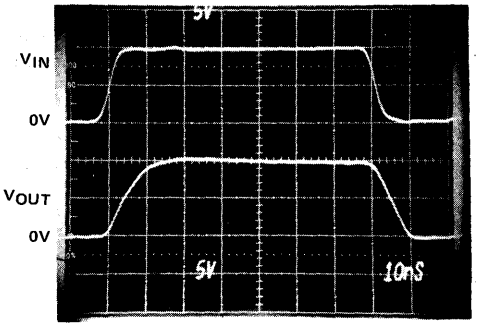
RISE TIME



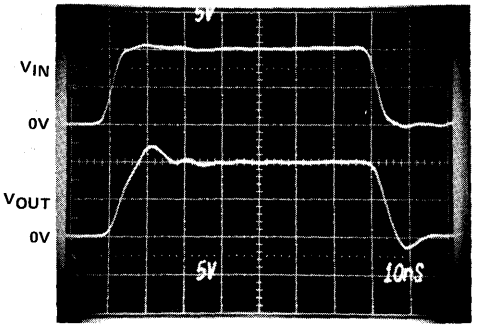
NOTE: Measured on both positive and negative transitions.

Test Circuits (Continued)

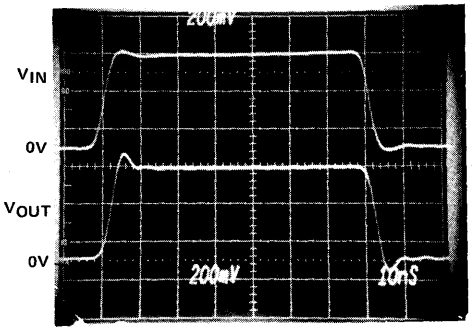
+10V RESPONSE
$T_A = +25^oC$, $R_S = 50\Omega$, $R_L = 100\Omega$



+10V RESPONSE
$T_A = +25^oC$, $R_S = 50\Omega$, $R_L = 1k\Omega$

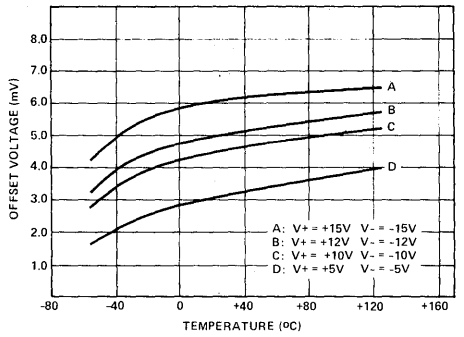


+0.5V PULSE RESPONSE
$T_A = +25^oC$, $R_S = 50\Omega$, $R_L = 100\Omega$

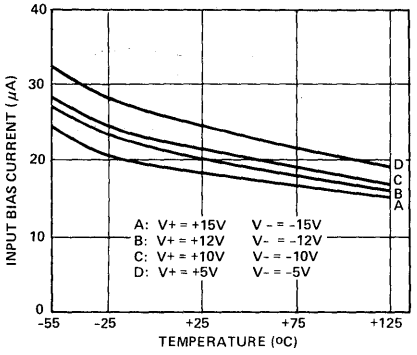


Typical Performance Curves

INPUT OFFSET VOLTAGE vs. TEMPERATURE vs. SUPPLY VOLTAGE

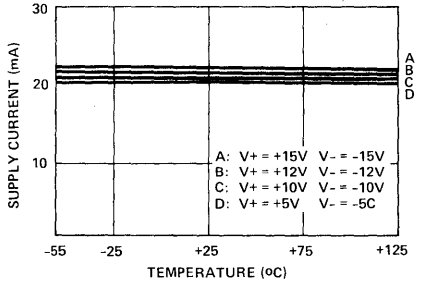


INPUT BIAS CURRENT vs. TEMPERATURE vs. SUPPLY VOLTAGE

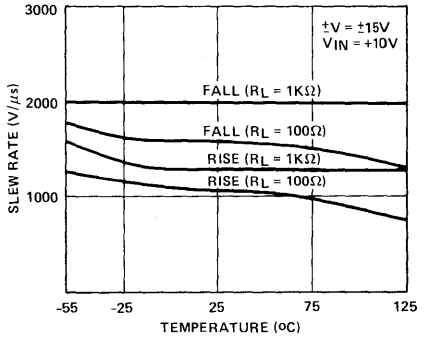


Typical Performance Curves (Continued)

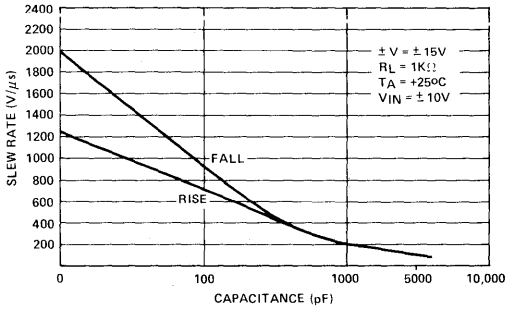
SUPPLY CURRENT vs. TEMPERATURE vs. SUPPLY VOLTAGE



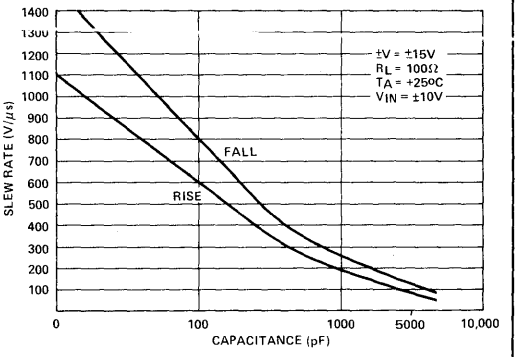
SLEW RATE vs. TEMPERATURE



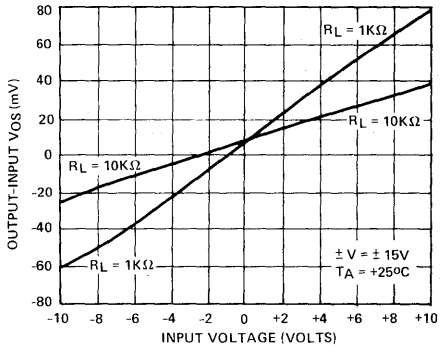
SLEW RATE vs. LOAD CAPACITANCE (R_L = 1kΩ)



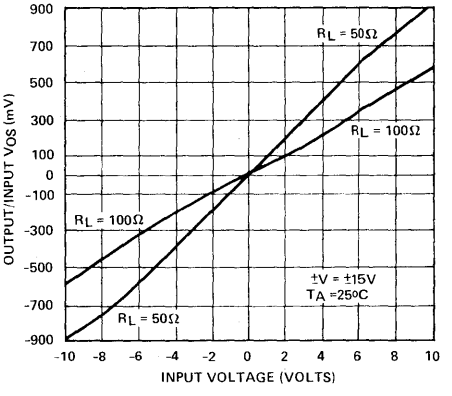
SLEW RATE vs. LOAD CAPACITANCE (R_L = 100Ω)



GAIN ERROR vs. INPUT VOLTAGE

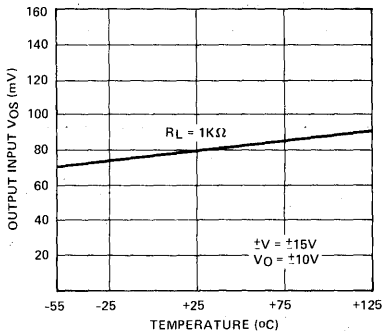


GAIN ERROR vs. INPUT VOLTAGE

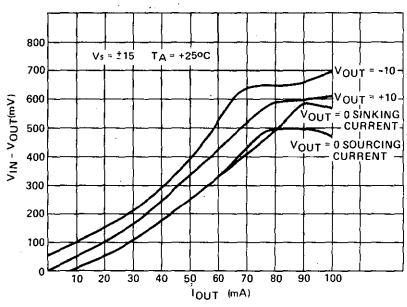


Typical Performance Curves (Continued)

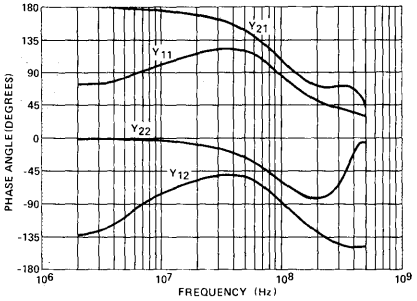
GAIN ERROR vs. TEMPERATURE



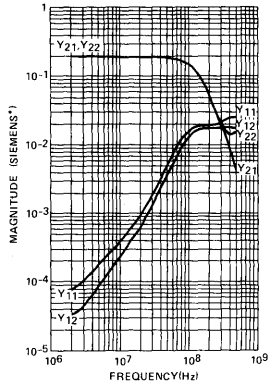
V_{IN} - V_{OUT} vs. I_{OUT}



Y - PARAMETERS PHASE vs. FREQUENCY

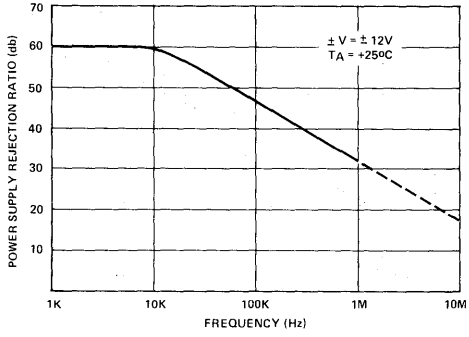


Y - PARAMETER MAGNITUDE vs. FREQUENCY

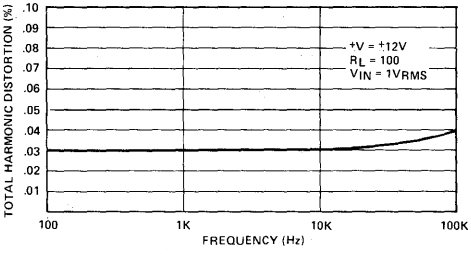


* Siemens = Ω -1

POWER SUPPLY REJECTION RATIO vs. FREQUENCY

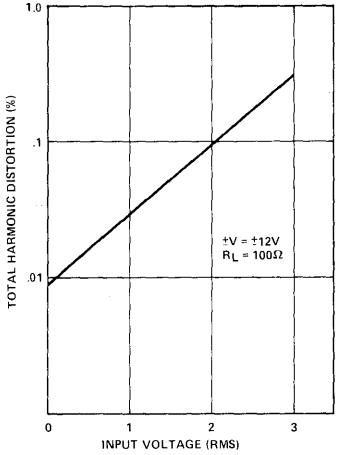


TOTAL HARMONIC DISTORTION vs. FREQUENCY

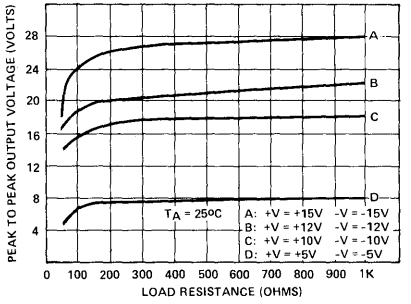


Typical Performance Curves (Continued)

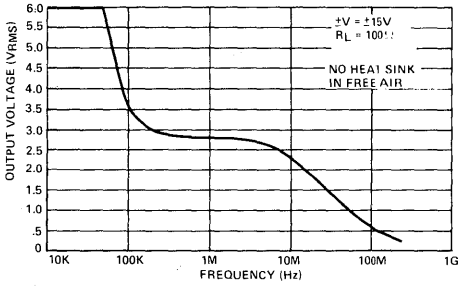
TOTAL HARMONIC DISTORTION vs. RMS INPUT VOLTAGE



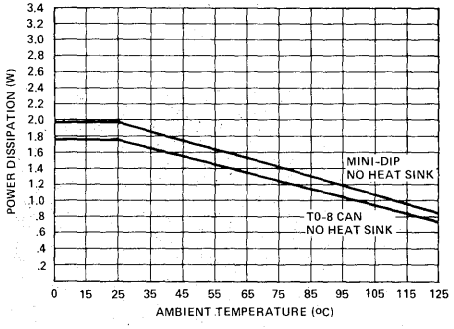
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE vs. SUPPLY VOLTAGE



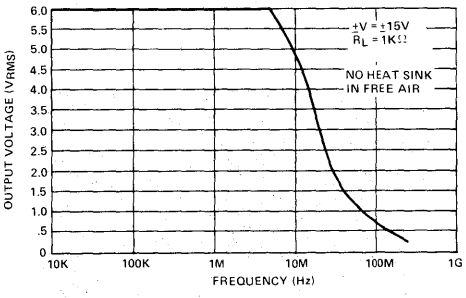
OUTPUT SWING vs. FREQUENCY*



MAXIMUM POWER DISSIPATION vs. AMBIENT TEMPERATURE



OUTPUT SWING vs. FREQUENCY*

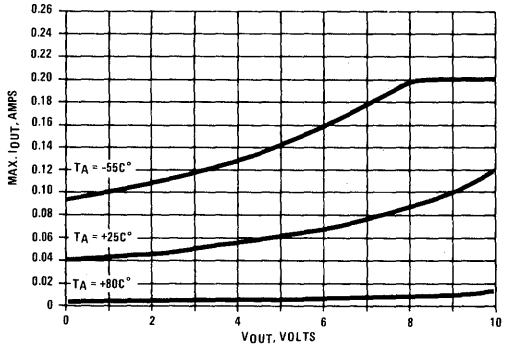


8 SPECIAL ANALOG CIRCUITS

Typical Performance Curves (Continued)

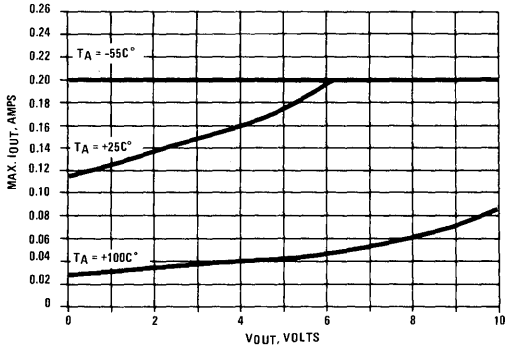
HA-5033 SOA, TO-8, NO SINK

T_J = +175, I_{CC} = 30mA, V_{CC} = ±15, θ_{ja} = 101°C/W



HA-5033, TO-8, AAVID 5792 θ_{sa} = 25°C/W

T_J = +175, I_{CC} = 30mA, V_{CC} = ±15, θ_{jc} = 33°C/W



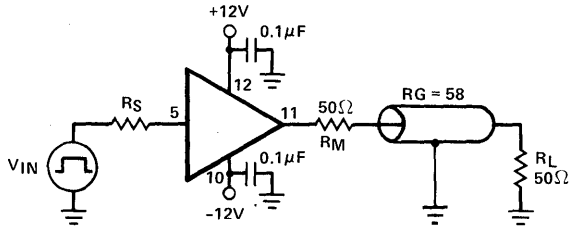
* This curve was obtained by noting the output voltage necessary to produce an observable distortion for a given frequency. If higher distortion is acceptable, then a higher output voltage for a given frequency can be obtained.

However, operating the HA-5033 with increased distortion (to the right of curve shown), will also be accompanied by an increase in supply current. The resulting increase in chip temperature must be considered and heat sinking will be necessary to prevent thermal runaway.

This characteristic is the result of the output transistor operation. If the signal amplitude or signal frequency or both are increased beyond the curve shown, the NPN, PNP output transistors will approach a condition of being simultaneously on. Under this condition, thermal runaway can occur.

Typical Applications (Also See Application Note 548)

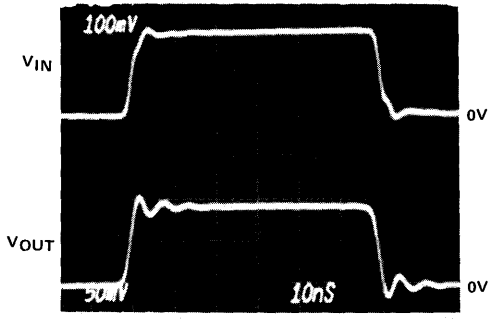
VIDEO COAXIAL LINE DRIVER - 50V SYSTEM



POSITIVE PULSE RESPONSE

T_A = +25°C, R_S = 50Ω, R_M = R_L = 50Ω

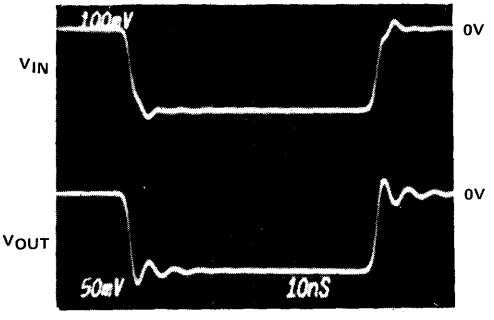
$$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = \tfrac{1}{2}\, V_{IN}$$



NEGATIVE PULSE RESPONSE

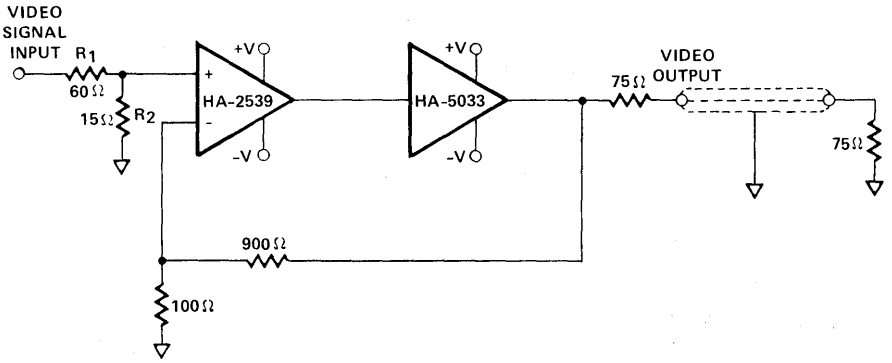
T_A = +25°C, R_S = 50Ω, R_M = RL = 50Ω

$$V_O = V_{IN}\left(\frac{R_L}{R_L + R_M}\right) = \tfrac{1}{2}\, V_{IN}$$



Typical Applications (Continued)

VIDEO GAIN BLOCK



Die Characteristics

Transistor Count 20

Die Dimensions ..... 50 x 66 x 19mils
(1270 x 1660 x 480µm)

Substrate Potential* ..... V-

Process ..... High Frequency Bipolar-DI

Passivation ..... Nitride

*The substrate may be left floating (Insulating Die Mount) or it may be mounted on a conductor at V- potential.

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICL8013
Four Quadrant Analog Multiplier

GENERAL DESCRIPTION

The ICL8013 is a four quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op-amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to trim gain accuracy, offset voltage and feedthrough performance. The high accuracy, wide bandwidth, and increased versatility of the ICL8013 make it ideal for all multiplier applications in control and instrumentation systems. Applications include RMS measuring equipment, frequency doublers, balanced modulators and demodulators, function generators, and voltage controlled amplifiers.

FEATURES

- **Accuracy of ±0.5% ("A" Version)**
- **Full ±10V Input Voltage Range**
- **1MHz Bandwidth**
- **Uses Standard ±15V Supplies**
- **Built-in Op Amp Provides Level Shifting, Division and Square Root Functions**

ORDERING INFORMATION

Part Number	Multiplication Error	Temperature Range	Package
ICL8013AM TX	±0.5% } MAX	−55°C to +125°C	10-LEAD TO-100
ICL8013BM TX	±1% } MAX	−55°C to +125°C	
ICL8013CM TX	±2% } MAX	−55°C to +125°C	
ICL8013AC TX	±5% } MAX	0°C to +70°C	
ICL8013BC TX	±1% } MAX	0°C to +70°C	
ICL8013CC TX	±2% } MAX	0°C to +70°C	

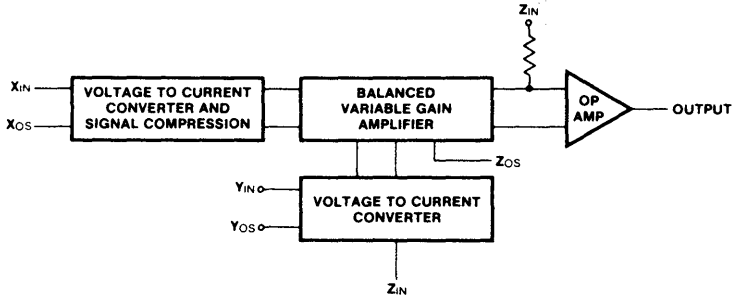


Figure 1: Functional Diagram (Multiplexer)

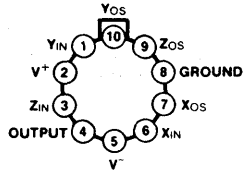


Figure 2: Pin Configuration

302085-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Power Dissipation (Note 1) 500mW
Input Voltages
(X_{IN}, Y_{IN}, Z_{IN}, X_{OS}, Y_{OS}, Z_{OS}) ..... V_{SUPPLY}

Operating Temperature Range:
ICL8013XC ..... 0°C to +70°C
ICL8013XM ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: Derate at 6.8mW/°C for operation at ambient temperature above 75°C.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified $T_A = 25°C$, $V_{SUPPLY} = \pm 15V$, Gain and Offset Potentiometers Externally Trimmed)

Parameter		Test Conditions	ICL8013A			ICL8013B			ICL8013C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Multiplier Function				$\frac{XY}{10}$			$\frac{XY}{10}$			$\frac{XY}{10}$		
Multiplication Error		$-10<X<10$ $-10<Y<10$			0.5			1.0			2.0	% Full Scale
Divider Function				$\frac{10Z}{X}$			$\frac{10Z}{X}$			$\frac{10Z}{X}$		
Division Error		$X=-10$ $X=-1$		0.3 1.5			0.3 1.5			0.3 1.5		% Full Scale % Full Scale
Feedthrough		$X=0, Y=\pm 10V$ $Y=0, X=\pm 10V$			50 50			100 100			200 150	mV mV
Non-Linearity	X Input	$X=20V_{p-p}$ $Y=\pm 10Vdc$		±0.5			±0.5			±0.8		%
	Y Input	$Y=20V_{p-p}$ $X=\pm 10Vdc$		±0.2			±0.2			±0.3		%
Frequency Response Small Signal Bandwidth (−3dB)				1.0			1.0			1.0		MHz
Full Power Bandwidth				750			750			750		kHz
Slew Rate				45			45			45		V/μs
1% Amplitude Error				75			75			75		kHz
1% Vector Error (0.5° Phase Shift)				5			5			5		kHz
Settling Time (to ±2% of Final Value) Overload Recovery (to ±2% of Final Value)		$V_{IN} = \pm 10V$		1 1			1 1			1 1		μs μs
Output Noise		5 Hz to 10 kHz 5 Hz to 5 MHz		0.6 3			0.6 3			0.6 3		mV rms mV rms
Input Resistance	X Input	$V_{IN} = 0V$		10			10			10		MΩ
	Y Input			6			6			6		MΩ
	Z Input			36			36			36		kΩ
Input Bias Current	X or Y Input	$V_{IN} = 0V$		2	5			7.5			10	μA
	Z Input			25			25			25		μA
Power Supply Variation	Multiplication Error			0.2			0.2			0.2		%/%
	Output Offset				50			75			100	mV/V
	Scale Factor			0.1			0.1			0.1		%/%
Quiescent Current				3.5	6.0		3.5	6.0		3.5	6.0	mA

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Unless otherwise specified $T_A = 25°C$, $V_{SUPPLY} = \pm 15V$, Gain and Offset Potentiometers Externally Trimmed) (Continued)

Parameter		Test Conditions	ICL8013A			ICL8013B			ICL8013C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
The Following Specifications Apply Over the Operating Temperature Ranges												
Multiplication Error		$-10V < X_{IN} < 10V$, $-10V < Y_{IN} < 10V$		1.5			2			3		% Full Scale
Average Temperature Coefficients	Accuracy			0.06			0.06			0.06		%/°C
	Output Offset			0.2			0.2			0.2		mV/°C
	Scale Factor			0.04			0.04			0.04		%/°C
Input Bias Current	X or Y Input	$V_{IN} = 0V$			5			5			10	μA
	Z Input				25			25			35	μA
Input Voltage (X, Y, or Z)					±10			±10			±10	V
Output Voltage Swing		$R_L \geq 2k\Omega$ $C_L < 1000pF$		±10			±10			±10		V

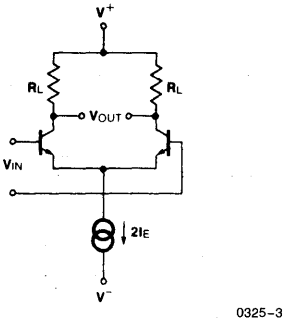


Figure 3: Differential Amplifier

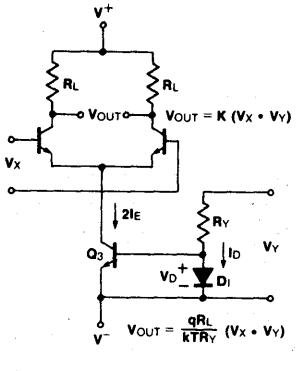


Figure 4: Transconductance Multiplier

DETAILED DESCRIPTION

The fundamental element of the ICL8013 multiplier is the bipolar differential amplifier of Figure 3.

The small signal differential voltage gain of this circuit is given by

$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R_L}{r_e}$$

Substituting $r_e = \frac{1}{g_m} = \frac{kT}{qI_E}$

$$V_{OUT} = V_{IN}\frac{R_L}{r_e} = V_{IN} \bullet \frac{qI_E R_L}{kT}$$

The output voltage is thus proportional to the product of the input voltage V_{IN} and the emitter current I_E. In the simple transconductance multiplier of Figure 4, a current source comprising Q_3, D_1, and R_Y is used. If V_Y is large compared with the drop across D_1, then

$$I_D \sim \frac{V_Y}{R_Y} = 2I_E \text{ and}$$

$$V_{OUT} = \frac{qR_L}{kTR_Y}(V_X \bullet V_Y)$$

There are several difficulties with this simple modulator:

1: V_Y must be positive and greater than V_D.

2: Some portion of the signal at V_X will appear at the output unless $I_E = 0$.

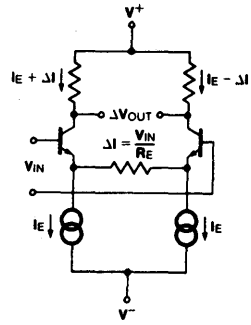
3: V_X must be a small signal for the differential pair to be linear.

4: The output voltage is not centered around ground.

The first problem relates to the method of converting the V_Y voltage to a current to vary the gain of the V_X differential pair. A better method, Figure 5, uses another differential pair but with considerable emitter degeneration. In this cir-

NOTE: All typical values have been characterized but are not tested.

cuit the differential input voltage appears across the common emitter resistor, producing a current which adds or subtracts from the quiescent current in either collector. This type of voltage to current converter handles signals from 0 volts to ±10 volts with excellent linearity.

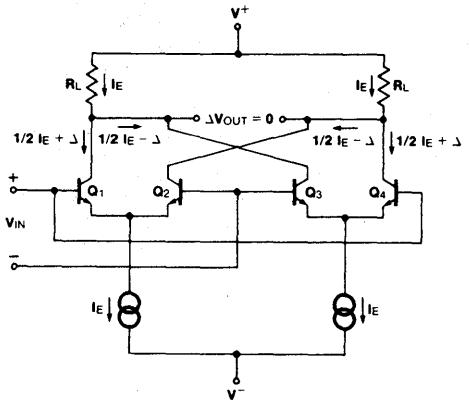


0325-5

Figure 5: Voltage to Current Converter

The second problem is called feedthrough; i.e. the product of zero and some finite input signal does not produce zero output voltage. The circuit whose operation is illustrated by Figures 6A, B, and C overcomes this problem and forms the heart of many multiplier circuits in use today.

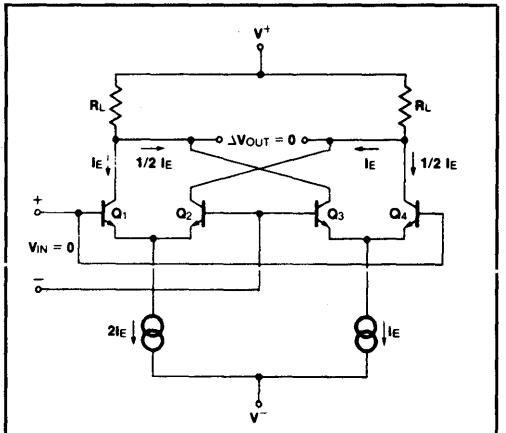
This circuit is basically two matched differential pairs with cross coupled collectors. Consider the case shown in 6A of exactly equal current sources biasing the two pairs. With a small positive signal at V_{IN}, the collector current of Q_1 and Q_4 will increase but the collector currents of Q_2 and Q_3 will decrease by the same amount. Since the collectors are cross coupled the current through the load resistors remains unchanged and independent of the V_{IN} input voltage.



0325-6

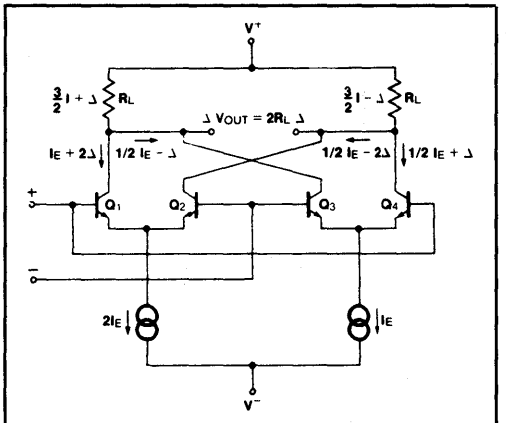
Figure 6A: Input Signal with Balanced Current Sources $\Delta V_{OUT} = 0V$

In Figure 6B, notice that with $V_{IN} = 0$ any variation in the ratio of biasing current sources will produce a common mode voltage across the load resistors. The differential output voltage will remain zero. In Figure 6C we apply a differential input voltage with unbalanced current sources. If I_{E1} is twice I_{E2}, the gain of differential pair Q_1 and Q_2 is twice the gain of pair Q_3 and Q_4. Therefore, the change in cross coupled collector currents will be unequal and a differential output voltage will result. By replacing the separate biasing current sources with the voltage to current converter of Figure 5 we have a balanced multiplier circuit capable of four quadrant operation (Figure 7).



0325-7

Figure 6B: No Input Signal with Unbalanced Current Sources $\Delta V_{OUT} = 0V$



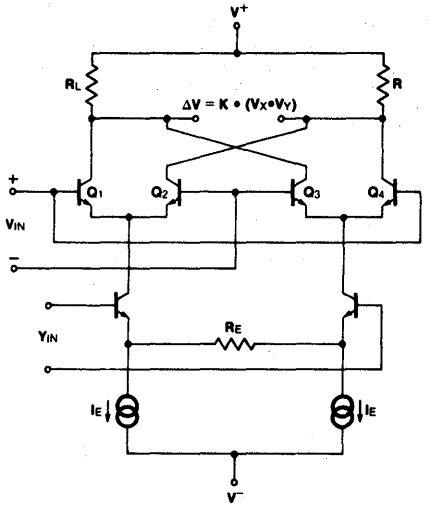
0325-8

Figure 6C: Input Signal with Unbalanced Current Sources, Differential Output Voltage

8 SPECIAL ANALOG CIRCUITS

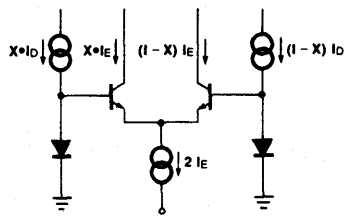
NOTE: All typical values have been characterized but are not tested.

This circuit of Figure 7 still has the problem that the input voltage V_{IN} must be small to keep the differential amplifier in the linear region. To be able to handle large signals, we need an amplitude compression circuit.



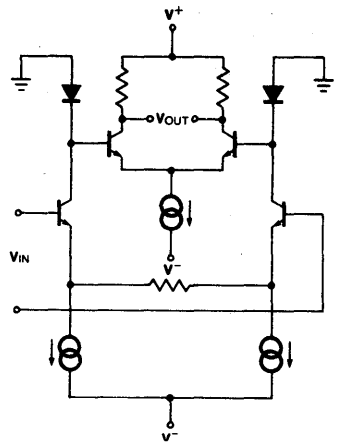
0325-9

Figure 7: Typical Four Quadrant Multiplier-Modulator



0325-10

Figure 8A: Current Gain Cell



0325-11

Figure 8B: Voltage Gain with Signal Compression

Figure 4 showed a current source formed by relying on the matching characteristics of a diode and the emitter base junction of a transistor. Extension of this idea to a differential circuit is shown in Figure 8A. In a differential pair, the input voltage splits the biasing current in a logarithmic ratio. (The usual assumption of linearity is useful only for small signals.) Since the input to the differential pair in Figure 8A is the difference in voltage across the two diodes, which in turn is proportional to the log of the ratio of drive currents, it follows that the ratio of diode currents and the ratio of collector currents are linearly related and independent of amplitude. If we combine this circuit with the voltage to current converter of Figure 5, we have Figure 8B. The output of the differential amplifier is now proportional to the input voltage over a large dynamic range, thereby improving linearity while minimizing drift and noise factors.

The complete schematic is shown in Figure 9. The differential pair Q_3 and Q_4 form a voltage to current converter whose output is compressed in collector diodes Q_1 and Q_2. These diodes drive the balanced cross-coupled differential amplifier Q_7/Q_8 Q_{14}/Q_{15}. The gain of these amplifiers is modulated by the voltage to current converter Q_9 and Q_{10}. Transistors Q_5, Q_6, Q_{11}, and Q_{12} are constant current sources which bias the voltage to current converter. The output amplifier comprises transistors Q_{16} through Q_{27}.

NOTE: All typical values have been characterized but are not tested.

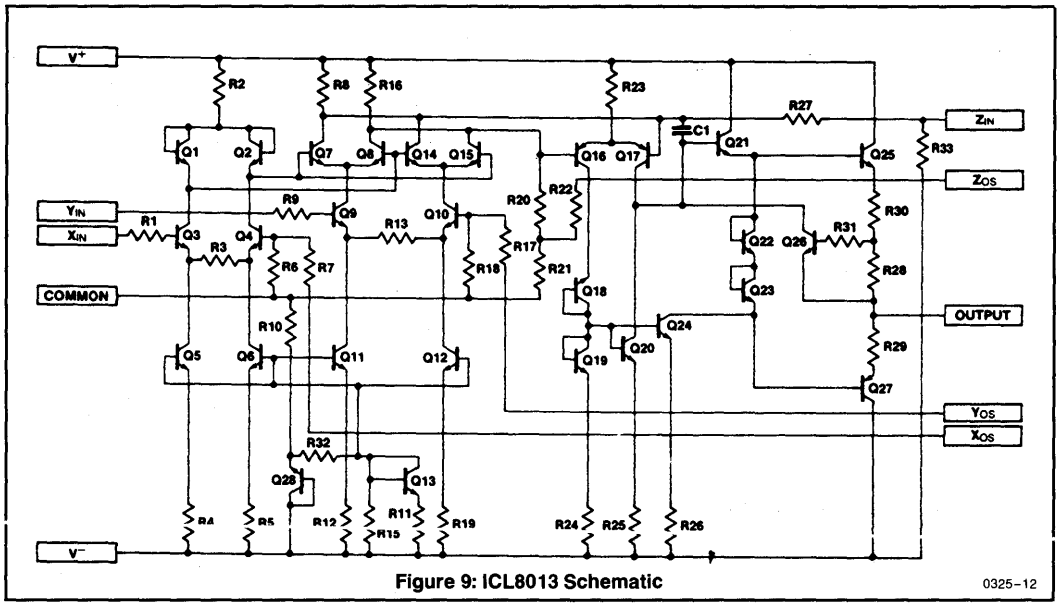
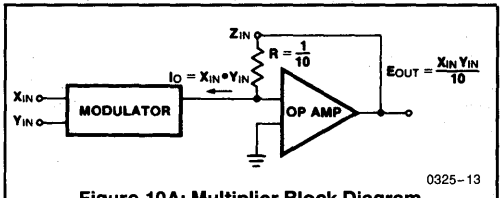


Figure 9: ICL8013 Schematic

0325-12

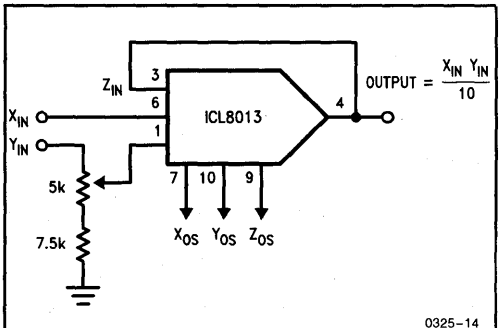
MULTIPLICATION

In the standard multiplier connection, the Z terminal is connected to the op amp output. All of the modulator output current thus flows through the feedback resistor R27 and produces a proportional output voltage.



0325-13

Figure 10A: Multiplier Block Diagram



0325-14

Figure 10B: Actual Circuit Connection

Multiplier Trimming Procedure

1. Set $X_{IN} = Y_{IN} = 0V$ and adjust Z_{OS} for zero Output.
2. Apply a $\pm 10V$ low frequency ($\leq 100Hz$) sweep (sine or triangle) to Y_{IN} with $X_{IN} = 0V$, and adjust X_{OS} for minimum output.
3. Apply the sweep signal of Step 2 to X_{IN} with $Y_{IN} = 0V$ and adjust Y_{OS} for minimum Output.
4. Readjust Z_{OS} as in Step 1, if necessary.
5. With $X_{IN} = 10.0V$ DC and the sweep signal of Step 2 applied to Y_{IN}, adjust the Gain potentiometer for Output $= Y_{IN}$. This is easily accomplished with a differential scope plug-in (A + B) by inverting one signal and adjusting Gain control for (Output $- Y_{IN}$) = Zero.

DIVISION

If the Z terminal is used as an input, and the output of the op-amp connected to the Y input, the device functions as a divider. Since the input to the op-amp is at virtual ground, and requires negligible bias current, the overall feedback forces the modulator output current to equal the current produced by Z.

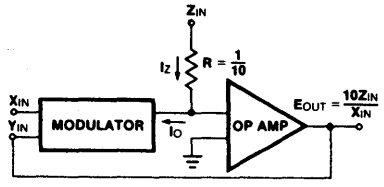
$$\text{Therefore } I_O = X_{IN} \bullet Y_{IN} = \frac{Z_{IN}}{R} = 10Z_{IN}$$

$$\text{Since } Y_{IN} = E_{OUT},\ E_{OUT} = \frac{10Z_{IN}}{X_{IN}}$$

8 SPECIAL ANALOG CIRCUITS

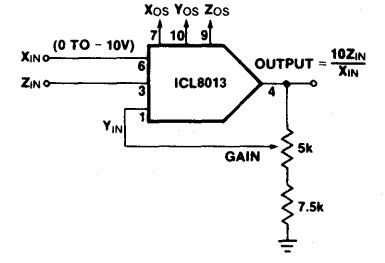
NOTE: All typical values have been characterized but are not tested.

Note that when connected as a divider, the X input must be a negative voltage to maintain overall negative feedback.



0325-15

Figure 11A: Division Block Diagram



0325-16

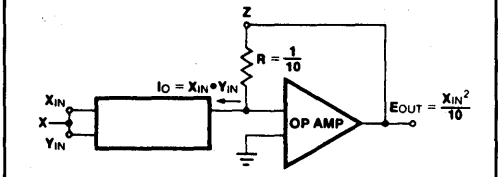
Figure 11B: Actual Circuit Connection

Divider Trimming Procedure

1. Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 (X_{OS}, Y_{OS}, Z_{OS}) for zero volts.
2. With $Z_{IN}=0V$, trim Z_{OS} to hold the Output constant, as X_{IN} is varied from $-10V$ through $-1V$.
3. With $Z_{IN}=0V$ and $X_{IN}=-10.0V$ adjust Y_{OS} for zero Output voltage.
4. With $Z_{IN}=X_{IN}$ (and/or $Z_{IN}=-X_{IN}$) adjust X_{OS} for minimum worst-case variation of Output, as X_{IN} is varied from $-10V$ to $-1V$.
5. Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.
6. With $Z_{IN}=X_{IN}$ (and/or $Z_{IN}=-X_{IN}$) adjust the gain control until the output is the closest average around $+10.0V$ ($-10V$ for $Z_{IN}=-X_{IN}$) as X_{IN} is varied from $-10V$ to $-3V$.

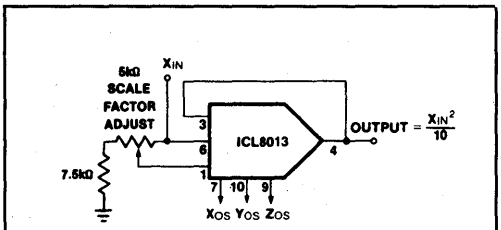
SQUARING

The squaring function is achieved by simply multiplying with the two inputs tied together. The squaring circuit may also be used as the basis for a frequency doubler since $\cos^2\omega t=\frac{1}{2}(\cos 2\omega t+1)$.



0325-17

Figure 12A: Squarer Block Diagram



0325-18

Figure 12B: Actual Circuit Connection

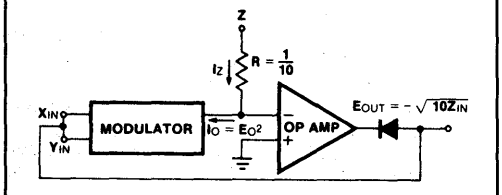
SQUARE ROOT

Tying the X and Y inputs together and using overall feedback from the Op Amp results in the square root function. The output of the modulator is again forced to equal the current produced by the Z input.

$$I_O=X_{IN}\bullet Y_{IN}=(-E_{OUT})^2=10Z_{IN}$$

$$E_{OUT}=-\sqrt{10Z_{IN}}$$

The output is a negative voltage which maintains overall negative feedback. A diode in series with the Op Amp output prevents the latchup that would otherwise occur for negative input voltages.



0325-19

Figure 13A: Square Root Block Diagram

NOTE: All typical values have been characterized but are not tested.

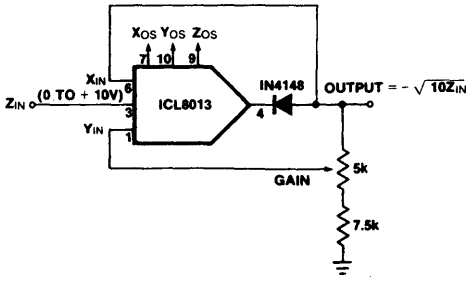


Figure 13B: Actual Circuit Connection

Square Root Trimming Procedure

1. Connect the ICL8013 in the *Divider* configuration.
2. Adjust Z_{OS}, Y_{OS}, X_{OS}, and Gain using Steps 1 through 6 of Divider Trimming Procedure.
3. Convert to the Square Root configuration by connecting X_{IN} to the Output and inserting a diode between Pin 4 and the Output node.
4. With $Z_{IN} = 0V$ adjust Z_{OS} for zero Output voltage.

VARIABLE GAIN AMPLIFIER

Most applications for the ICL8013 are straight forward variations of the simple arithmetic functions described above. Although the circuit description frequently disguises the fact, it has already been shown that the frequency doubler is nothing more than a squaring circuit. Similarly the variable gain amplifier is nothing more than a multiplier, with the input signal applied at the X input and the control voltage applied at the Y input.

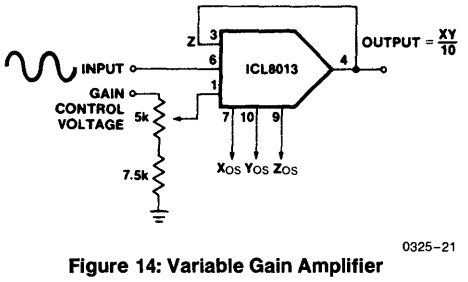


Figure 14: Variable Gain Amplifier

TYPICAL APPLICATIONS

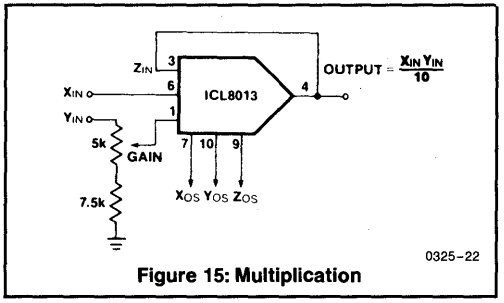


Figure 15: Multiplication

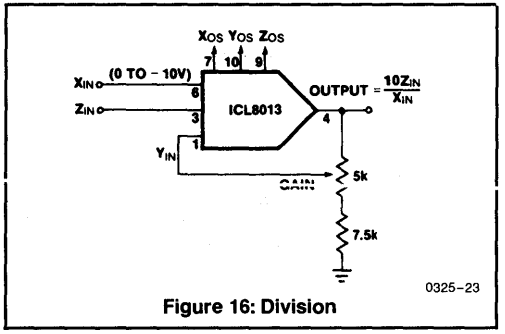


Figure 16: Division

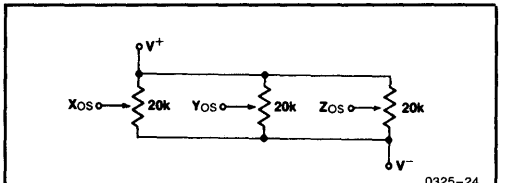


Figure 17: Potentiometers for Trimming Offset and Feedthrough

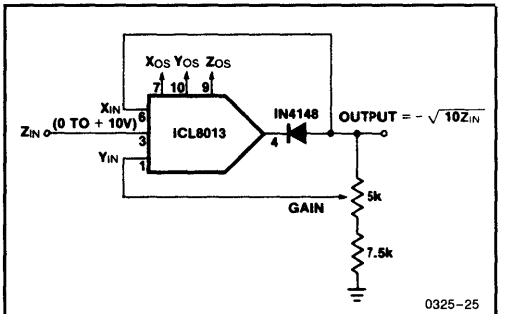
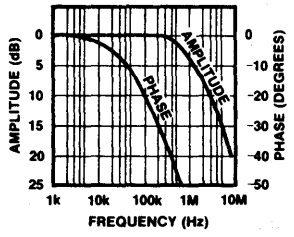


Figure 18: Square Root

NOTE: All typical values have been characterized but are not tested.

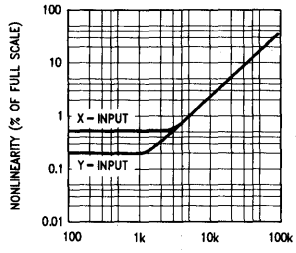
TYPICAL PERFORMANCE CHARACTERISTICS

AMPLITUDE AND PHASE AS A FUNCTION OF FREQUENCY



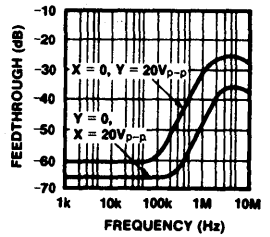
0325-26

NONLINEARITY AS A FUNCTION OF FREQUENCY



0325-27

FEEDTHROUGH AS A FUNCTION OF FREQUENCY



0325-28

DEFINITION OF TERMS

Multiplication/Division Error: This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

Feedthrough: With either input at zero, the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

Nonlinearity: The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and the other swept through its nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICL8038
Precision Waveform Generator/Voltage Controlled Oscillator

GENERAL DESCRIPTION

The ICL8038 Waveform Generator is a monolithic integrated circuit capable of producing high accuracy sine, square, triangular, sawtooth and pulse waveforms with a minimum of external components. The frequency (or repetition rate) can be selected externally from .001Hz to more than 300kHz using either resistors or capacitors, and frequency modulation and sweeping can be accomplished with an external voltage. The ICL8038 is fabricated with advanced monolithic technology, using Schottky-barrier diodes and thin film resistors, and the output is stable over a wide range of temperature and supply variations. These devices may be interfaced with phase locked loop circuitry to reduce temperature drift to less than 250ppm/°C.

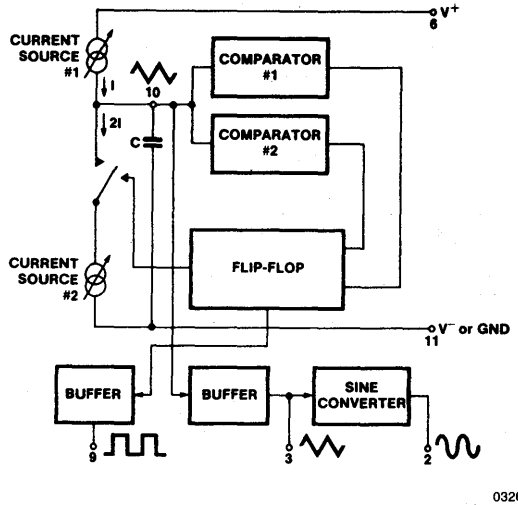
FEATURES

- **Low Frequency Drift With Temperature — 250ppm/°C**
- **Simultaneous Sine, Square, and Triangle Wave Outputs**
- **Low Distortion — 1% (Sine Wave Output)**
- **High Linearity — 0.1% (Triangle Wave Output)**
- **Wide Operating Frequency Range — 0.001Hz to 300kHz**
- **Variable Duty Cycle — 2% to 98%**
- **High Level Outputs — TTL to 28V**
- **Easy to Use — Just A Handful of External Components Required**

ORDERING INFORMATION

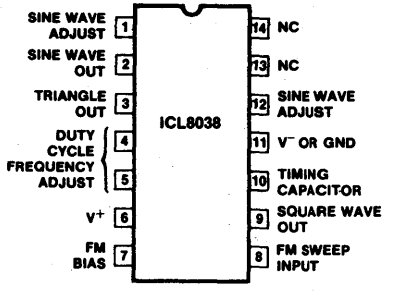
Part Number	Stability	Temp. Range	Package
ICL8038CCPD	250ppm/°C typ	0°C to +70°C	14 pin DIP
ICL8038CCJD	250ppm/°C typ	0°C to +70°C	14 pin CERDIP
ICL8038BCJD	180ppm/°C typ	0°C to +70°C	14 pin CERDIP
ICL8038ACJD	120ppm/°C typ	0°C to +70°C	14 pin CERDIP
ICL8038BMJD*	350ppm/°C max	−55°C to +125°C	14 pin CERDIP
ICL8038AMJD*	250ppm/°C max	−55°C to +125°C	14 pin CERDIP

*Add /883B to part number if 883 processing is required.



0326-1

Figure 1: Functional Diagram



0326-2

Figure 2: Pin Configuration (Outline dwg JD)

8 SPECIAL ANALOG CIRCUITS

302600-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^- to V^+) 36V
Power Dissipation[1] 750mW
Input Voltage (any pin) ..... V^- to V^+
Input Current (Pins 4 and 5) 25mA
Output Sink Current (Pins 3 and 9) 25mA
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range:
8038AM, 8038BM ..... −55°C to +125°C
8038AC, 8038BC, 8038CC ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE 1: Derate ceramic package at 12.5mW/°C for ambient temperatures above 100°C.

ELECTRICAL CHARACTERISTICS

($V_{SUPPLY} = \pm 10V$ or $+20V$, $T_A = 25°C$, $R_L = 10k\Omega$, Test Circuit Unless Otherwise Specified)

Symbol	General Characteristics	8038CC			8038BC(BM)			8038AC(AM)			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{SUPPLY}	Supply Voltage Operating Range										
V^+	Single Supply	+10		+30	+10		30	+10		30	V
V^+, V^-	Dual Supplies	±5		±15	±5		±15	±5		±15	V
I_{SUPPLY}	Supply Current ($V_{SUPPLY} = \pm 10V$)[2]										
	8038AM, 8038BM					12	15		12	15	mA
	8038AC, 8038BC, 8038CC		12	20		12	20		12	20	mA
Frequency Characteristics (all waveforms)											
f_{max}	Maximum Frequency of Oscillation	100			100			100			kHz
f_{sweep}	Sweep Frequency of FM Input		10			10			10		kHz
	Sweep FM Range[3]		35:1			35:1			35:1		
	FM Linearity 10:1 Ratio		0.5			0.2			0.2		%
$\Delta f/\Delta T$	Frequency Drift With Temperature[5] 8038 AC, BC, CC 0°C to 70°C		250			180			120		ppm/°C
	8038 AM, BM, −55°C to 125°C						350			250	ppm/°C
$\Delta f/\Delta V$	Frequency Drift With Supply Voltage (Over Supply Voltage Range)		0.05			0.05			0.05		%/V
Output Characteristics											
I_{OLK}	**Square-Wave** Leakage Current ($V_9 = 30V$)			1			1			1	μA
V_{SAT}	Saturation Voltage ($I_{SINK} = 2mA$)		0.2	0.5		0.2	0.4		0.2	0.4	V
t_r	Rise Time ($R_L = 4.7k\Omega$)		180			180			180		ns
t_f	Fall Time ($R_L = 4.7k\Omega$)		40			40			40		ns
ΔD	Typical Duty Cycle Adjust (Note 6)	2		98	2		98	2		98	%
$V_{TRIANGLE}$	**Triangle/Sawtooth/Ramp** Amplitude ($R_{TRI} = 100k\Omega$)	0.30	0.33		0.30	0.33		0.30	0.33		xV_{SUPPLY}
	Linearity		0.1			0.05			0.05		%
Z_{OUT}	Output Impedance ($I_{OUT} = 5mA$)		200			200			200		Ω
V_{SINE}	**Sine-Wave** Amplitude ($R_{SINE} = 100k\Omega$)	0.2	0.22		0.2	0.22		0.2	0.22		xV_{SUPPLY}
THD	THD ($R_S = 1M\Omega$)[4]		2.0	5		1.5	3		1.0	1.5	%
THD	THD Adjusted (Use Figure 6)		1.5			1.0			0.8		%

NOTES: 2. R_A and R_B currents not included.
3. $V_{SUPPLY} = 20V$; R_A and $R_B = 10k\Omega$, $f \cong 10kHz$ nominal; can be extended 1000 to 1. See Figures 7a and 7b.
4. $82k\Omega$ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R_A and R_B.)
5. Figure 3, pins 7 and 8 connected, $V_{SUPPLY} = \pm 10V$. See Typical Curves for T.C. vs V_{SUPPLY}.
6. Not tested, typical value for design purposes only.

NOTE: All typical values have been characterized but are not tested.

TEST CONDITIONS

Parameter		R_A	R_B	R_L	C_1	SW_1	Measure
Supply Current		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Current into Pin 6
Sweep FM Range(1)		10kΩ	10kΩ	10kΩ	3.3nF	Open	Frequency at Pin 9
Frequency Drift with Temperature		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 3
Frequency Drift with Supply Voltage(2)		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Output Amplitude: (Note 4)	Sine	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 2
	Triangle	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 3
Leakage Current (off)(3)		10kΩ	10kΩ		3.3nF	Closed	Current into Pin 9
Saturation Voltage (on)(3)		10kΩ	10kΩ		3.3nF	Closed	Output (low) at Pin 9
Rise and Fall Times (Note 5)		10kΩ	10kΩ	4.7kΩ	3.3nF	Closed	Waveform at Pin 9
Duty Cycle Adjust: (Note 5)	MAX	50kΩ	~1.6kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
	MIN	~25kΩ	50kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Triangle Waveform Linearity		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 3
Total Harmonic Distortion		10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 2

NOTES: 1. The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 (f_{hi}) and then connecting pin 8 to pin 6 (f_{lo}). Otherwise apply Sweep Voltage at pin 8 ($\frac{2}{3}$ V_{SUPPLY} + 2V) ≤ V_{SWEEP} ≤ V_{SUPPLY} where V_{SUPPLY} is the total supply voltage. In Figure 7b, pin 8 should vary between 5.3V and 10V with respect to ground.

2. $10V \leq V^+ \leq 30V$, or $\pm 5V \leq V_{SUPPLY} \leq \pm 15V$.
3. Oscillation can be halted by forcing pin 10 to +5 volts or −5 volts.
4. Output Amplitude is tested under static conditions by forcing pin 10 to 5.0V then to −5.0V.
5. Not tested; for design purposes only.

DEFINITION OF TERMS:

Supply Voltage (V_{SUPPLY}). The total supply voltage from V^+ to V^-

Supply Current. The supply current required from the power supply to operate the device, excluding load currents and the currents through R_A and R_B.

Frequency Range. The frequency range at the square wave output through which circuit operation is guaranteed.

Sweep FM Range. The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to pin 8. For correct operation, the sweep voltage should be within the range

$$(\tfrac{2}{3} V_{SUPPLY} + 2V) < V_{SWEEP} < V_{SUPPLY}$$

FM Linearity. The percentage deviation from the best-fit straight line on the control voltage versus output frequency curve.

Output Amplitude. The peak-to-peak signal amplitude appearing at the outputs.

Saturation Voltage. The output voltage at the collector of Q_{23} when this transistor is turned on. It is measured for a sink current of 2mA.

Rise and Fall Times. The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.

Triangle Waveform Linearity. The percentage deviation from the best-fit straight line on the rising and falling triangle waveform.

Total Harmonic Distortion. The total harmonic distortion at the sine-wave output.

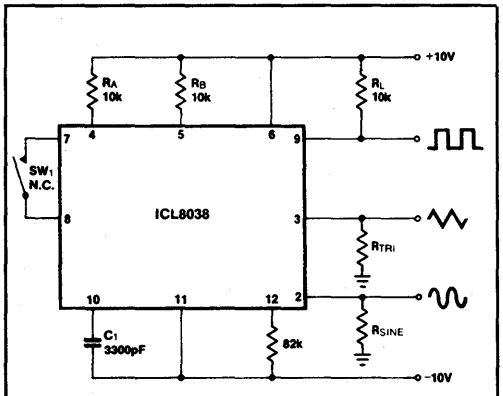
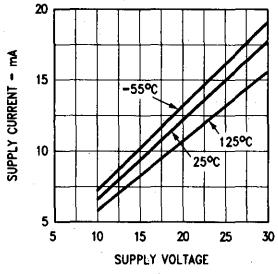


Figure 3: Test Circuit

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS



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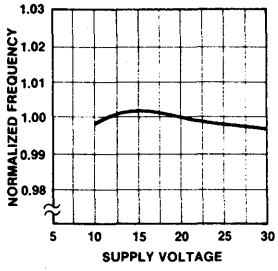
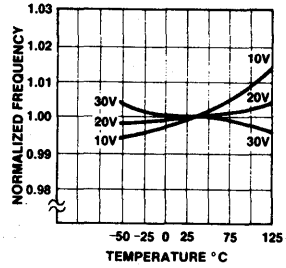


0326-5



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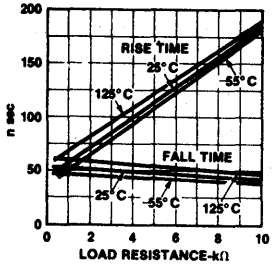
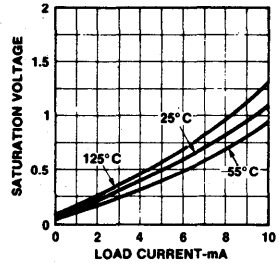
Performance of the Square-Wave Output

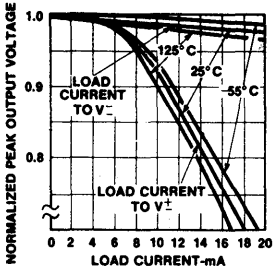


0326-7

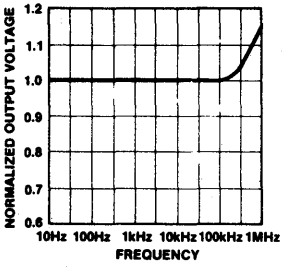


0326-8

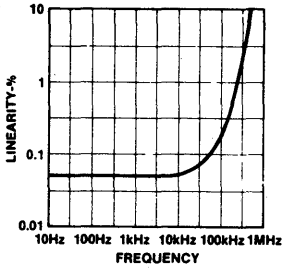
Performance of Triangle-Wave Output



0326-9

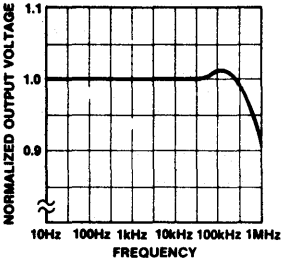


0326-10

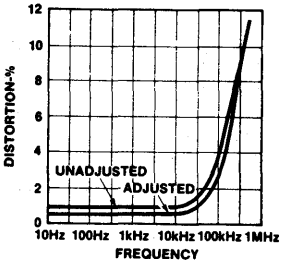


0326-11

Performance of Sine-Wave Output

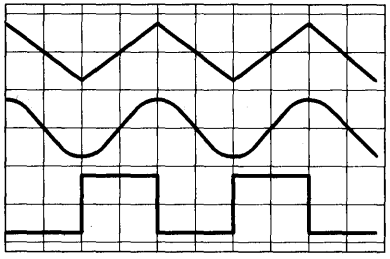


0326-12



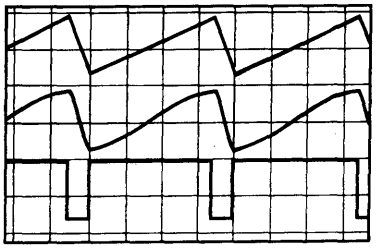
0326-13

NOTE: All typical values have been characterized but are not tested.



0326-14

Square-Wave Duty Cycle—50%



0326-15

Square-Wave Duty Cycle—80%

Figure 4: Phase Relationship of Waveforms

DETAILED DESCRIPTION (See Figure 1)

An external capacitor C is charged and discharged by two current sources. Current source #2 is switched on and off by a flip-flop, while current source #1 is on continuously. Assuming that the flip-flop is in a state such that current source #2 is off, and the capacitor is charged with a current I, the voltage across the capacitor rises linearily with time. When this voltage reaches the level of comparator #1 (set at ⅔ of the supply voltage), the flip-flop is triggered, changes states, and releases current source #2. This current source normally carries a current 2I, thus the capacitor is discharged with a net-current I and the voltage across it drops linearly with time. When it has reached the level of comparator #2 (set at ⅓ of the supply voltage), the flip-flop is triggered into its original state and the cycle starts again.

Four waveforms are readily obtainable from this basic generator circuit. With the current sources set at I and 2I respectively, the charge and discharge times are equal. Thus a triangle waveform is created across the capacitor and the flip-flop produces a square-wave. Both waveforms are fed to buffer stages and are available at pins 3 and 9.

The levels of the current sources can, however, be selected over a wide range with two external resistors. Therefore, with the two currents set at values different from I and 2I, an asymmetrical sawtooth appears at terminal 3 and pulses with a duty cycle from less than 1% to greater than 99% are available at terminal 9.

The sine-wave is created by feeding the triangle-wave into a non-linear network (sine-converter). This network provides a decreasing shunt-impedance as the potential of the triangle moves toward the two extremes.

WAVEFORM TIMING

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 5. Best results are obtained by keeping the timing resistors R_A and R_B separate (a). R_A controls the rising portion of the triangle and sine-wave and the 1 state of the square-wave.

The magnitude of the triangle-waveform is set at ⅓ V_{SUPPLY}; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times \frac{1}{3} \times V_{SUPPLY} \times R_A}{0.22 \times V_{SUPPLY}} = \frac{R_A \times C}{0.66}$$

The falling portion of the triangle and sine-wave and the 0 state of the square-wave is:

$$t_2 = \frac{C \times V}{I} = \frac{C \times \frac{1}{3} V_{SUPPLY}}{2(0.22)\frac{V_{SUPPLY}}{R_B} - 0.22\frac{V_{SUPPLY}}{R_A}} = \frac{R_A R_B C}{0.66(2R_A - R_B)}$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty-cycle is to be varied over a small range about 50% only, the connection shown in Figure 5b is slightly more convenient.

With two separate timing resistors, the frequency is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{R_A C}{0.66}\left(1 + \frac{R_B}{2R_A - R_B}\right)}$$

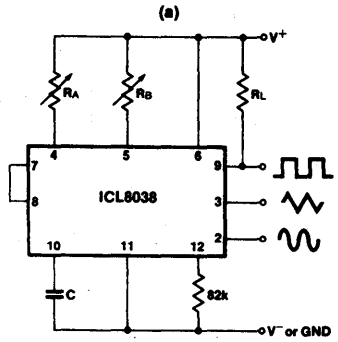
or, if $R_A = R_B = R$

$$f = \frac{0.33}{RC} \text{ (for Figure 5a)}$$

8

SPECIAL ANALOG CIRCUITS

NOTE: All typical values have been characterized but are not tested.



0326-16

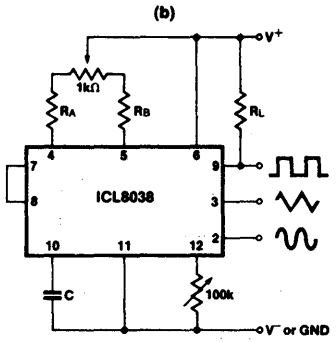


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Figure 5: Possible Connections for the External Timing Resistors

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the fact that both currents *and* thresholds are direct, linear functions of the supply voltage and thus their effects cancel.

To minimize *sine-wave* distortion the 82kΩ resistor between pins 11 and 12 is best made variable. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 6; this configuration allows a typical reduction of sine-wave distortion close to 0.5%.

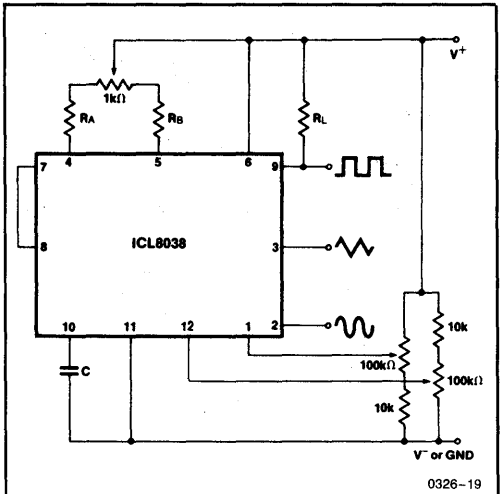

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Figure 6: Connection to Achieve Minimum Sine-Wave Distortion

SELECTING R_A, R_B and C

For any given output frequency, there is a wide range of RC combinations that will work, however certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I>5mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will, therefore, be obtained with charging currents of 10μA to 1mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{R_1 \times (V^+ - V^-)}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{0.22(V^+ - V^-)}{R_A}$$

R_1 and R_2 are shown in Figure 13.

A similar calculation holds for R_B.

The capacitor value should be chosen at the upper end of its possible range.

WAVEFORM OUT LEVEL CONTROL AND POWER SUPPLIES

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (±5 to ±15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between V^+ and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square-wave output can be made TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a much higher voltage.

NOTE: All typical values have been characterized but are not tested.

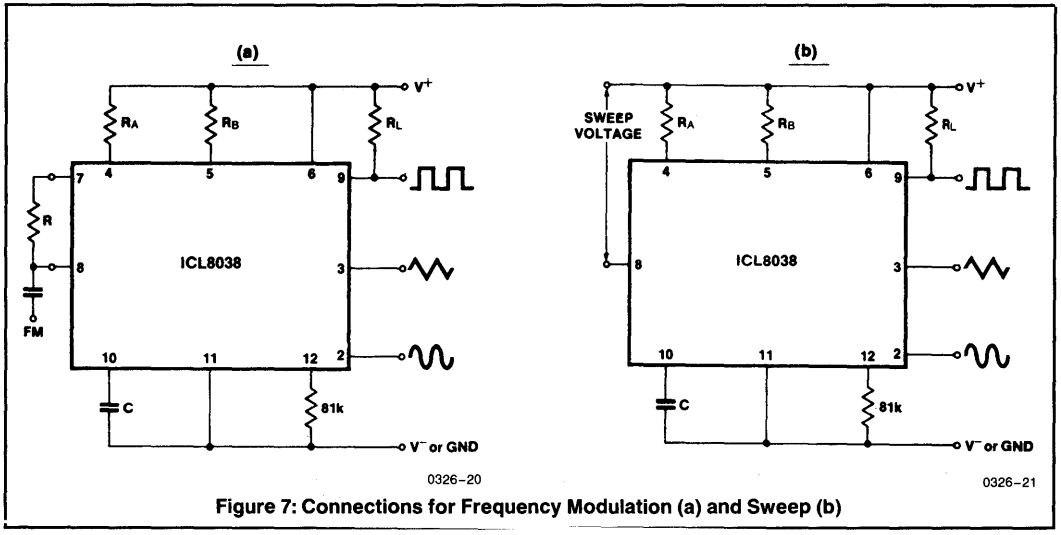


Figure 7: Connections for Frequency Modulation (a) and Sweep (b)

FREQUENCY MODULATION AND SWEEPING

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from V+). By altering this voltage, frequency modulation is performed. For small deviations (e.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing DC decoupling with a capacitor as shown in Figure 7a. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance from about 8kΩ (pins 7 and 8 connected together), to about (R+8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 7b). In this way the entire bias for the current sources is created by the modulating signal, and a very large (e.g. 1000:1) sweep range is created (f=0 at $V_{sweep}=0$). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept down from V+ by (⅓ V_{SUPPLY} − 2V).

APPLICATIONS

The sine wave output has a relatively high output impedance (1kΩ Typ). The circuit of Figure 8 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the ICL8038 oscillation. Figure 9 shows a FET switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

To obtain a 1000:1 Sweep Range on the ICL8038 the voltage across external resistors R_A and R_B must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of R_A and R_B by a few hundred millivolts. The Circuit of Figure 10 achieves this by using a diode to lower the effective supply voltage on the ICL8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

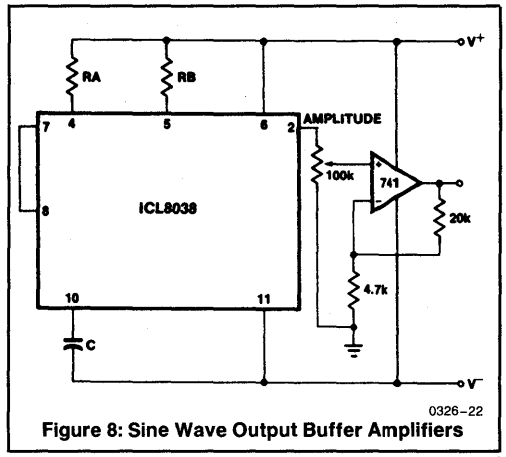


Figure 8: Sine Wave Output Buffer Amplifiers

The linearity of input sweep voltage versus output frequency can be significantly improved by using an op amp as shown in Figure 11.

USE IN PHASE-LOCKED LOOPS

Its high frequency stability makes the ICL8038 an ideal building block for a phase-locked loop as shown in Figure 12. In this application the remaining functional blocks, the

8 SPECIAL ANALOG CIRCUITS

NOTE: All typical values have been characterized but are not tested.

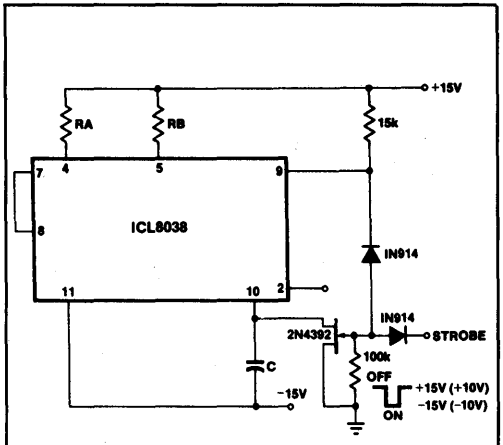


Figure 9: Strobe-Tone Burst Generator

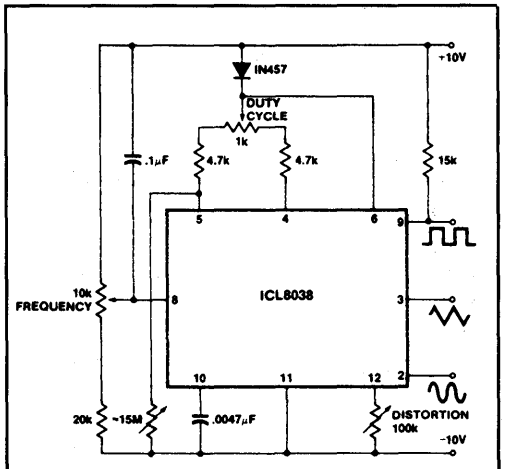


Figure 10: Variable Audio Oscillator, 20Hz to 20kHz

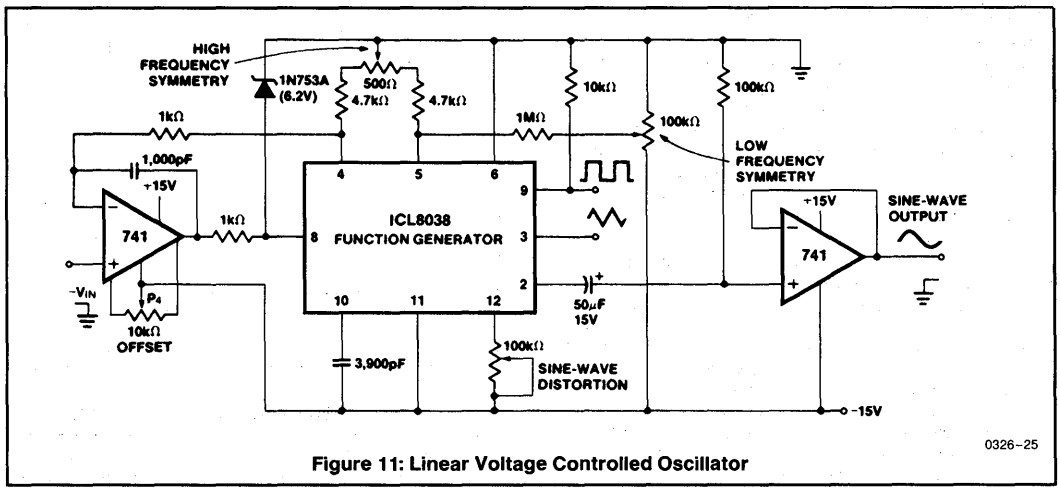


Figure 11: Linear Voltage Controlled Oscillator

phase-detector and the amplifier, can be formed by a number of available IC's (e.g. MC4344, NE562, HA2800, HA2820)

In order to match these building blocks to each other, two steps must be taken. First, two different supply voltages are used and the square wave output is returned to the supply of the phase detector. This assures that the VCO input voltage will not exceed the capabilities of the phase detector. If a smaller VCO signal is required, a simple resistive voltage divider is connected between pin 9 of the waveform generator and the VCO input of the phase-detector.

Second, the DC output level of the amplifier must be made compatible to the DC level required at the FM input of the waveform generator (pin 8, 0.8V+). The simplest solution here is to provide a voltage divider to V^+ (R_1, R_2 as shown) if the amplifier has a lower output level, or to ground if its level is higher. The divider can be made part of the low-pass filter.

This application not only provides for a free-running frequency with very low temperature drift, but it also has the unique feature of producing a large reconstituted sinewave signal with a frequency identical to that at the input.

For further information, see Harris Application Note A013, "Everything You Always Wanted to Know About The ICL8038."

NOTE: All typical values have been characterized but are not tested.

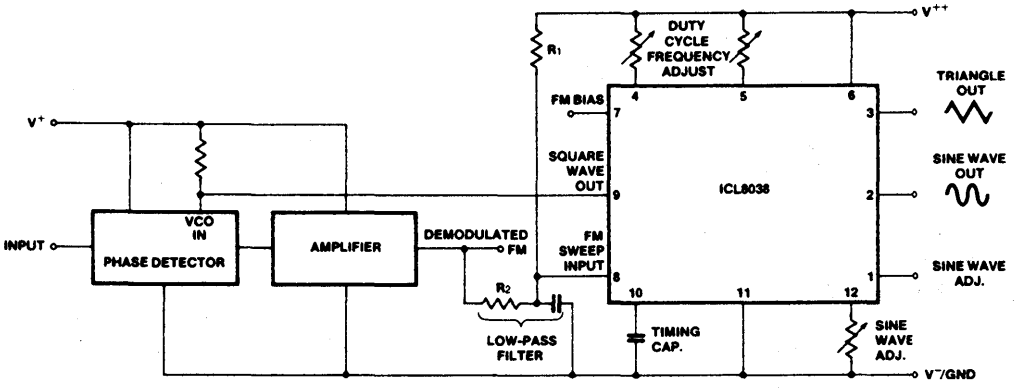


Figure 12: Waveform Generator Used as Stable VCO in a Phase-Locked Loop

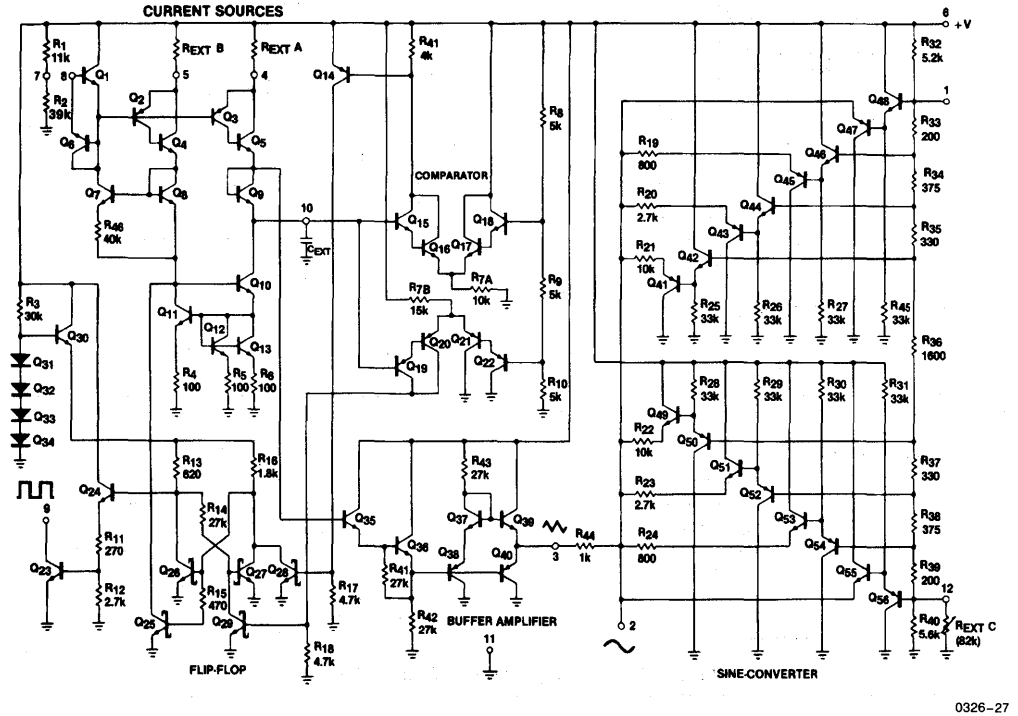


Figure 13: Detailed Schematic

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

ICL8048/ICL8049
Log/Antilog Amplifier

GENERAL DESCRIPTION

The 8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1 volt of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

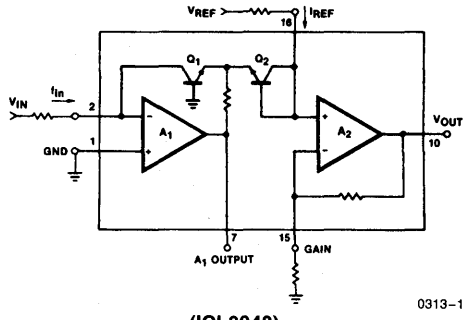
The 8049 is the antilogarithmic counterpart of the 8048; it nominally generates one decade of output voltage for each 1 volt change at the input.

FEATURES

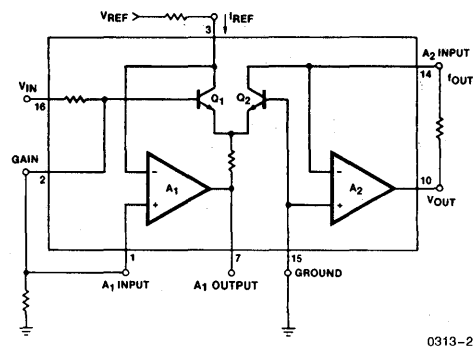
- 1½% Full Scale Accuracy
- Temperature Compensated for 0°C to +70°C Operation
- Scale Factor 1V/Decade, Adjustable
- 120dB Dynamic Current Range (8048)
- 60dB Dynamic Voltage Range (8048 & 8049)
- Dual JFET-Input Op-Amps

ORDERING INFORMATION

Part Number	Error (25°C)	Temperature Range	Package
ICL8048BCJE	30mV	0°C to +70°C	16 Pin CERDIP
ICL8048CCJE	60mV	0°C to +70°C	16 Pin CERDIP
ICL8049BCJE	10mV	0°C to +70°C	16 Pin CERDIP
ICL8049CCJE	25mV	0°C to +70°C	16 Pin CERDIP

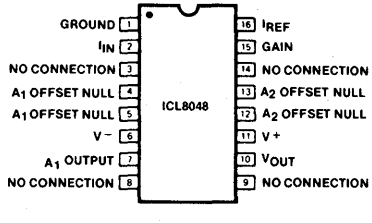


(ICL8048)



(ICL8049)

Figure 1: Functional Diagram



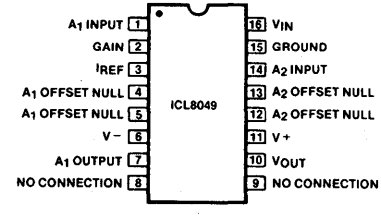


Figure 2: Pin Configurations (Outline Dwg JE)

302800-002

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (ICL8048)

Supply Voltage ..... ±18V
I_{IN} (Input Current) 2mA
I_{REF} (Reference Current) 2mA
Voltage between Offset Null and V+ ..... ±0.5V
Power Dissipation 750mW
Operating Temperature Range ..... 0°C to +70°C
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (ICL8048)

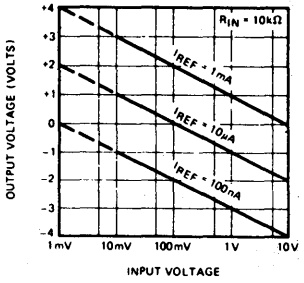
$V_S = \pm 15V$, $T_A = 25°C$, $I_{REF} = 1mA$, scale factor adjusted for 1V/decade unless otherwise specified.

Parameter	Test Conditions	8048BC			8048CC			Units
		Min	Typ	Max	Min	Typ	Max	
Dynamic Range I_{IN} (1nA – 1mA) V_{IN} (10mV – 10V)	 $R_{IN} = 10k\Omega$	 120 60			 120 60			 dB dB
Error, % of Full Scale	$T_A = 25°C$, $I_{IN} = 1nA$ to 1mA		.20	0.5		.25	1.0	%
Error, % of Full Scale	$T_A = 0°C$ to +70°C, $I_{IN} = 1nA$ to 1mA		.60	1.25		.80	2.5	%
Error, Absolute Value	$T_A = 25°C$, $I_{IN} = 1nA$ to 1mA		12	30		14	60	mV
Error, Absolute Value	$T_A = 0°C$ to +70°C $I_{IN} = 1nA$ to 1mA		36	75		50	150	mV
Temperature Coefficient of V_{OUT}	$I_{IN} = 1nA$ to 1mA		0.8			0.8		mV/°C
Power Supply Rejection Ratio	Referred to Output		2.5			2.5		mV/V
Offset Voltage (A_1 & A_2)	Before Nulling		15	25		15	50	mV
Wideband Noise	At Output, for $I_{IN} = 100\mu A$		250			250		μV(RMS)
Output Voltage Swing	$R_L = 10k\Omega$	±12	±14		±12	±14		V
	$R_L = 2k\Omega$	±10	±13		±10	±13		V
Power Consumption			150	200		150	200	mW
Supply Current			5	6.7		5	6.7	mA

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

TRANSFER FUNCTION FOR VOLTAGE INPUTS



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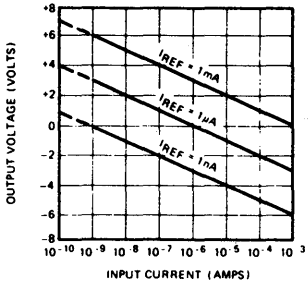
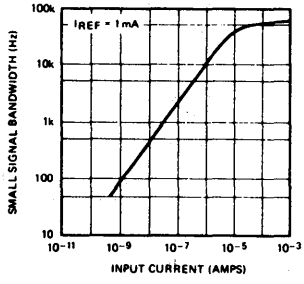
TRANSFER FUNCTION FOR CURRENT INPUTS



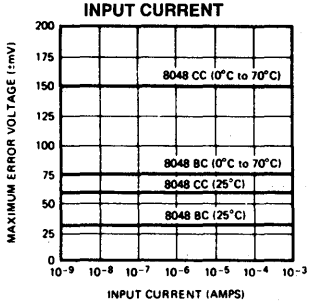
0313-6

SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT CURRENT



0313-7

MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT CURRENT



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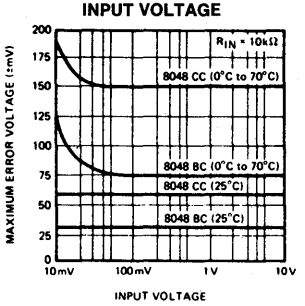
MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT VOLTAGE



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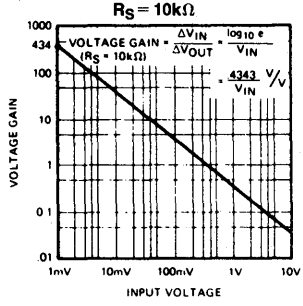
SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE FOR $R_S = 10k\Omega$



0313-10

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (ICL8049)

Supply Voltage ..... ±18V
V_{IN} (Input Voltage) ..... ±15V
I_{REF} (Reference Current) 2mA
Voltage between Offset Null and V^+ ..... ±0.5V
Power Dissipation 750mW
Operating Temperature Range ..... 0°C to +70°C
Output Short Circuit Duration ..... Indefinite
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

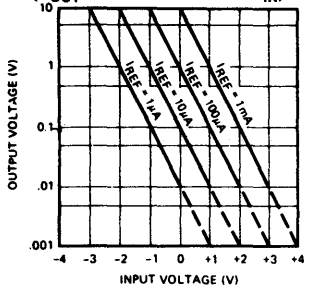
ELECTRICAL CHARACTERISTICS (ICL8049)

$V_S = \pm 15V$, $T_A = 25°C$, $I_{REF} = 1mA$, scale factor adjusted for 1 decade (out) per volt (in), unless otherwise specified.

Parameter	Test Conditions	8049BC			8049CC			Units
		Min	Typ	Max	Min	Typ	Max	
Dynamic Range (V_{OUT})	$V_{OUT} = 10mV$ to 10V	60			60			dB
Error, Absolute Value	$T_A = 25°C$, $0V \le V_{IN} \le 2V$		3	15		5	25	mV
Error, Absolute Value	$T_A = 0°C$ to +70°C, $0V \le V_{IN} \le 3V$		20	75		30	150	mV
Temperature Coefficient, Referred to V_{IN}	$V_{IN} = 3V$		0.38			0.55		mV/°C
Power Supply Rejection Ratio	Referred to Input, for $V_N = 0V$		2.0			2.0		μV/V
Offset Voltage (A_1 & A_2)	Before Nulling		15	25		15	50	mV
Wideband Noise	Referred to Input, for $V_{IN} = 0V$		26			26		μV(RMS)
Output Voltage Swing	$R_L = 10k\Omega$	±12	±14		±12	±14		V
	$R_L = 2k\Omega$	±10	±13		±10	±13		V
Power Consumption			150	200		150	200	mW
Supply Current			5	6.7		5	6.7	mA

TYPICAL PERFORMANCE CHARACTERISTICS

TRANSFER FUNCTION (V_{OUT} AS A FUNCTION OF V_{IN})



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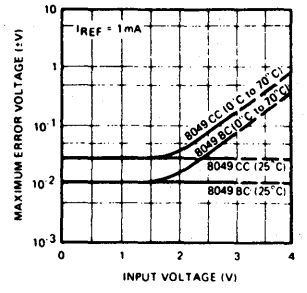
MAXIMUM ERROR VOLTAGE REFERRED TO THE INPUT AS A FUNCTION OF V_{IN}



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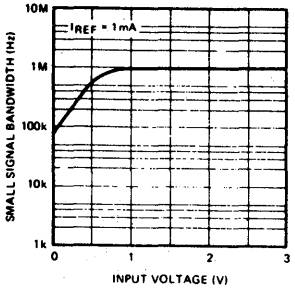
NOTE: All typical values have been characterized but are not tested.

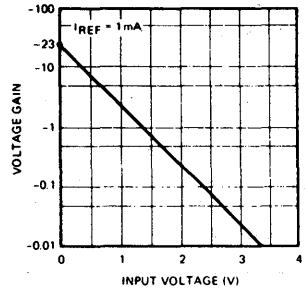
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT VOLTAGE



0313-13

SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE



0313-14

ICL8048 DETAILED DESCRIPTION

The ICL8048 relies for its operation on the well-known exponential relationship between the collector current and the base-emitter voltage of a transistor:

$$I_C = I_S[e^{qV_{BE}/kT} - 1] \quad (1)$$

For base-emitter voltages greater than 100mV, Eq. (1) becomes

$$I_C = I_S e^{qV_{BE}/kT} \quad (2)$$

From Eq. (2), it can be shown that for two identical transistors operating at different collector currents, the V_{BE} difference (ΔV_{BE}) is given by:

$$\Delta V_{BE} = -2.303 \times \frac{kT}{q} \log_{10}\left[\frac{I_{C1}}{I_{C2}}\right] \quad (3)$$

Referring to Figure 3, it is clear that the potential at the collector of Q_2 is equal to the ΔV_{BE} between Q_1 and Q_2. The output voltage is ΔV_{BE} multiplied by the gain of A_2:

$$V_{OUT} = -2.303\left(\frac{R_1+R_2}{R_2}\right)\left(\frac{kT}{q}\right)\log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \quad (4)$$

The expression $2.303 \times \frac{kT}{q}$ has a numerical value of 59mV at 25°C; thus in order to generate 1 volt/decade at the output, the ratio $(R_1+R_2)/R_2$ is chosen to be 16.9. For this scale factor to hold constant as a function of temperature, the $(R_1+R_2)/R_2$ term must have a 1/T characteristic to compensate for kT/q.

In the ICL8048 this is achieved by making R_1 a thin film resistor, deposited on the monolithic chip. It has a nominal value of 15.9kΩ at 25°C, and its temperature coefficient is carefully designed to provide the necessary compensation. Resistor R_2 is external and should be a low T.C. type; it should have a nominal value of 1kΩ to provide 1 volt/decade, and must have an adjustment range of ±20% to allow for production variations in the absolute value of R_1.

ICL8048 OFFSET AND SCALE FACTOR ADJUSTMENT

A log amp, unlike an op-amp, cannot be offset adjusted by simply grounding the input. This is because the log of zero approaches minus infinity; reducing the input current to zero starves Q_1 of collector current and opens the feedback loop around A_1. Instead, it is necessary to zero the offset voltage of A_1 and A_2 separately, and then to adjust the scale factor. Referring to Figure 3, this is done as follows:

1) Temporarily connect a 10kΩ resistor (R_0) between pins 2 and 7. With no input voltage, adjust R_4 until the output of A_1 (pin 7) is zero. Remove R_0.

   Note that for a current input, this adjustment is not necessary since the offset voltage of A_1 does not cause any error for current-source inputs.

2) Set $I_{IN} = I_{REF} = 1$mA. Adjust R_5 such that the output of A_2 (pin 10) is zero.

3) Set $I_{IN} = 1\mu$A, $I_{REF} = 1$mA. Adjust R_2 for $V_{OUT} = 3$ volts (for a 1 volt/decade scale factor) or 6 volts (for a 2 volt/decade scale factor).

Step #3 determines the scale factor. Setting $I_{IN} = 1\mu$A optimizes the scale factor adjustment over a fairly wide dynamic range, from 1mA to 1nA. Clearly, if the 8048 is to be used for inputs which only span the range 100μA to 1mA, it would be better to set $I_{IN} = 100\mu$A in Step #3. Similarly, adjustment for other scale factors would require different I_{IN} and V_{OUT} values.

NOTE: All typical values have been characterized but are not tested.

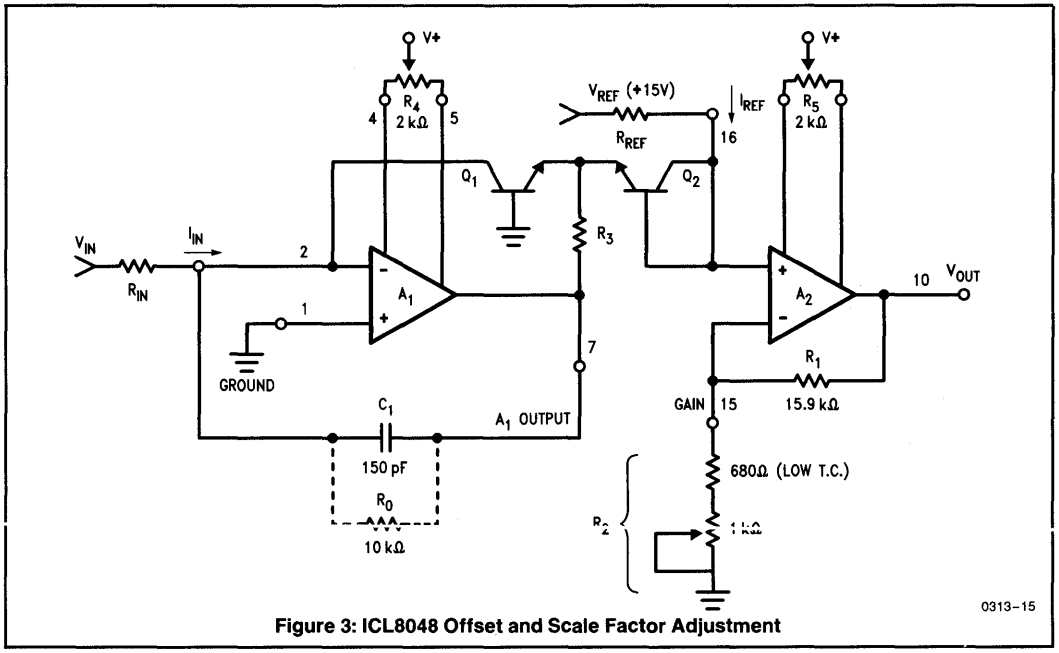


Figure 3: ICL8048 Offset and Scale Factor Adjustment

ICL8049 DETAILED DESCRIPTION

The ICL8049 relies on the same logarithmic properties of the transistor as the ICL8048. The input voltage forces a specific ΔV_{BE} between Q_1 and Q_2 (Figure 4). This V_{BE} difference is converted into a difference of collector currents by the transistor pair. The equation governing the behavior of the transistor pair is derived from (2) on the previous page and is as follows:

$$\frac{I_{C_1}}{I_{C_2}} = \exp\left[\frac{q\Delta V_{BE}}{kT}\right]$$

When numerical values for q/kT are put into this equation, it is found that a ΔV_{BE} of 59mV (at 25°C) is required to change the collector current ratio by a factor of ten. But for ease of application, it is desirable that a 1 volt change at the input generate a tenfold change at the output. The required input attenuation is achieved by the network comprising R_1 and R_2. In order that scale factors other than one decade per volt may be selected, R_2 is external to the chip. It should have a value of 1kΩ, adjustable ±20%, for one decade per volt. R_1 is a thin film resistor deposited on the monolithic chip; its temperature characteristics are chosen to compensate the temperature dependence of equation 5, as explained on the previous page.

The overall transfer function is as follows:

$$\frac{I_{OUT}}{I_{REF}} = \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{qV_{IN}}{kT}\right] \quad (6)$$

Substituting $V_{OUT} = I_{OUT} \times R_{OUT}$ gives:

$$V_{OUT} = R_{OUT}\, I_{REF} \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{qV_{IN}}{kT}\right] \quad (7)$$

For voltage references equation 7 becomes

$$V_{OUT} = V_{REF} \times \frac{R_{OUT}}{R_{REF}} \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{qV_{IN}}{kT}\right] \quad (8)$$

ICL8049 OFFSET AND SCALE FACTOR ADJUSTMENT

As with the log amplifier, the antilog amplifier requires three adjustments. The first step is to null out the offset voltage of A_2. This is accomplished by reverse biasing the base-emitter of Q_2. A_2 then operates as a unity gain buffer with a grounded input. The second step forces $V_{IN} = 0$; the output is adjusted for $V_{OUT} = 10V$. This step essentially "anchors" one point on the transfer function. The third step applies a specific input and adjusts the output to the correct voltage. This sets the scale factor. Referring to Figure 4, the exact procedure for 1 decade/volt is as follows:

1) Connect the input (pin #16) to +15V. This reverse biases the base-emitter of Q_2. Adjust R_7 for $V_{OUT} = 0V$. Disconnect the input from +15V.
2) Connect the input to Ground. Adjust R_4 for $V_{OUT} = 10V$. Disconnect the input from Ground.
3) Connect the input to a precise 2V supply and adjust R_2 for $V_{OUT} = 100mV$.

The procedure outlined above optimizes the performance over a 3 decade range at the output (i.e., V_{OUT} from 10mV to 10V). For a more limited range of output voltages, for example 1V to 10V, it would be better to use a precise 1 volt supply and adjust for $V_{OUT} = 1V$. For other scale factors and/or starting points, different values for R_2 and R_{REF} will be needed, but the same basic procedure applies.

NOTE: All typical values have been characterized but are not tested.

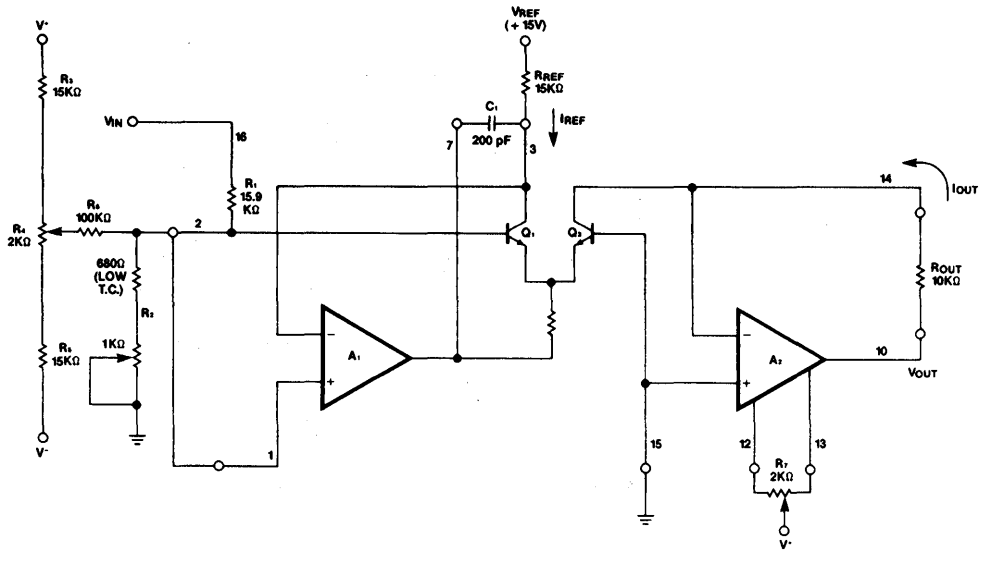


Figure 4: ICL8049 Offset and Scale Factor Adjustment

APPLICATIONS INFORMATION

ICL8048 Scale Factor Adjustment

The scale factor adjustment procedures outlined previously for the ICL8048 and ICL8049, are primarily directed towards setting up 1 volt (ΔV_{OUT}) per decade (ΔI_{IN} or ΔV_{IN}) for the log amp, or one decade (ΔV_{OUT}) per volt (ΔV_{IN}) for the antilog amp.

This corresponds to K = 1 in the respective transfer functions:

$$\text{Log Amp: } V_{OUT} = -K \log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \quad (9)$$

$$\text{Antilog Amp: } V_{OUT} = R_{OUT} I_{REF} 10^{\frac{-V_{IN}}{K}} \quad (10)$$

By adjusting R_2 (Figure 3 and Figure 4) the scale factor "K" in equation 9 and 10 can be varied. The effect of changing K is shown graphically in Figure 5 for the log amp, and Figure 6 for the antilog amp. The nominal value of R_2 required to give a specific value of K can be determined from equation 11. It should be remembered that R_1 has a ±20% tolerance in absolute value, so that allowance shall be made for adjusting the nominal value of R_2 by ±20%.

$$R_2 = \frac{941}{(K - .059)}\ \Omega \quad (11)$$

ICL8048 Automatic Offset Nulling Circuit

The ICL8048 is fundamentally a logarithmic current amplifier. It can be made to act as a voltage amplifier by placing a resistor between the current input and the voltage source but, since $I_{IN} = (V_{IN} - V_{OFFSET})/R_{IN}$, this conversion is accurate only when V_{IN} is much greater than the offset voltage. A substantial reduction of V_{OFFSET} would allow voltage operation over a 120 dB range.

Figure 101 shows the ICL8048 in an automatic offset nulling configuration using the ICL7650S. The extremely low offset voltage of the ICL7650S forces its non-inverting input (and thus pin 2 of the ICL8048) to the same potential as its inverting input by nulling the first stage of the log amp. Since V_{OFFSET} is now within a few microvolts of ground potential, R_{IN} can perform its voltage to current conversion much more accurately, and without an offset trimmer pot. Step 1 of the offset and scale factor adjustment is eliminated, simplifying calibration.

NOTE: The ICL7650S op amp has a maximum supply voltage of ±8 volts. The ICL8048 will operate at this voltage, but I_{REF} must be limited to 200 microamps or less for proper calibration and operation. Best performance will be achieved when the ICL7560S has a ±3–8V supply and the ICL8048 is at its recommended ±15V supply. See A053 for a method of powering the ICL7650S from a ±15V source.

Frequency Compensation

Although the op-amps in both the ICL8048 and the ICL8049 are compensated for unity gain, some additional frequency compensation is required. This is because the log transistors in the feedback loop add to the loop gain. In the 8048, 150pF should be connected between Pins 2 and 7 (Figure 3). In the 8049, 200pF between Pins 3 and 7 is recommended (Figure 4).

NOTE: All typical values have been characterized but are not tested.

EFFECT OF VARYING "K" ON THE ANTILOG AMPLIFIER

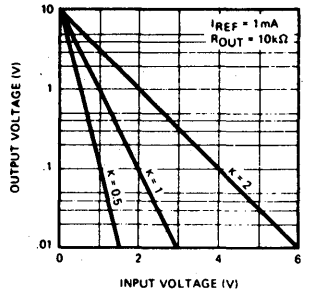


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Figure 5

EFFECT OF VARYING "K" ON THE LOG AMPLIFIER

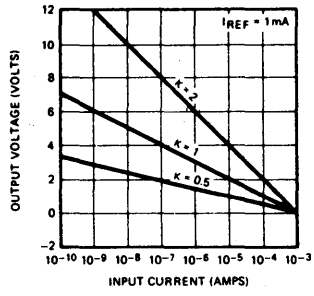

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Figure 6

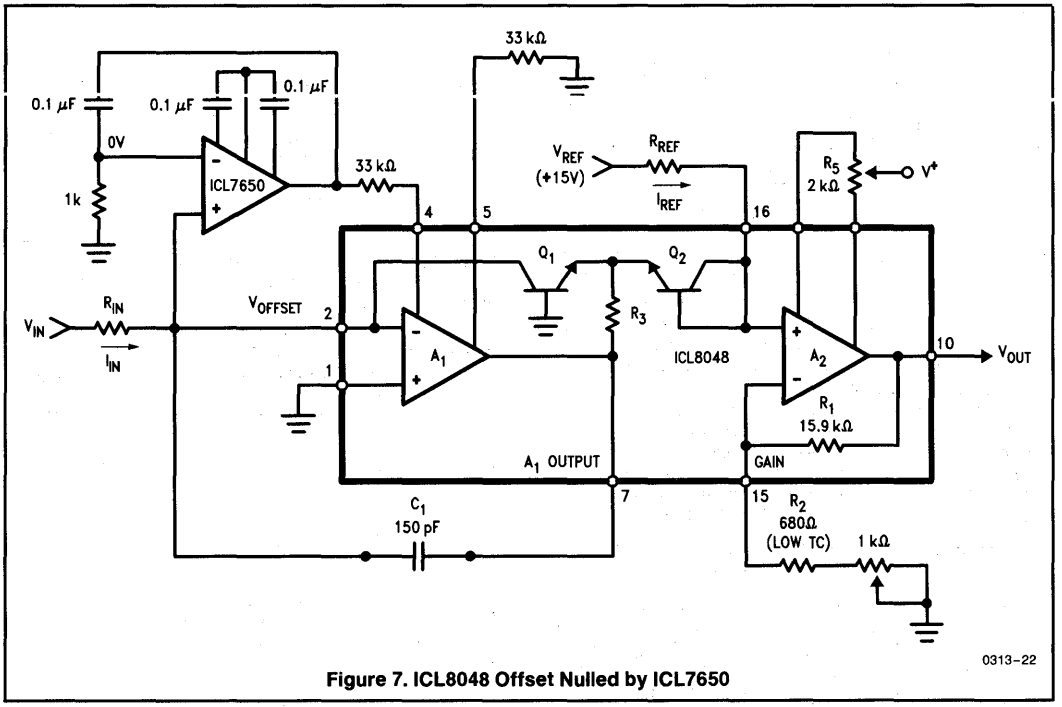

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Figure 7. ICL8048 Offset Nulled by ICL7650

Error Analysis

Performing a meaningful error analysis of a circuit containing log and antilog amplifiers is more complex than dealing with a similar circuit involving only op-amps. In this data sheet every effort has been made to simplify the analysis task, without in any way compromising the validity of the resultant numbers.

The key difference in making error calculations in log/antilog amps, compared with op-amps, is that the gain of the former is a function of the input signal level. Thus, it is necessary, when referring errors from output to input, or vice versa, to check the input voltage level, then determine the gain of the circuit by referring to the graphs given in the Typical Performance Characteristics section.

The various error terms in the log amplifier, the ICL8048, are Referred To the Output (RTO) of the device. The error terms in the antilog amplifier, the ICL8049, are Referred To the Input (RTI) of the device. The errors are expressed in this way because in the majority of systems a number of log amps interface with an antilog amp, as shown in Figure 8.

NOTE: All typical values have been characterized but are not tested.

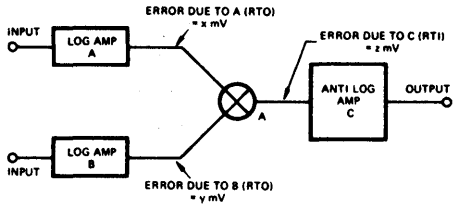


Figure 8 0313-19

It is very straightforward to estimate the system error at node (A) by taking the square root of the sum-of-the squares of the errors of each contributing block.

$$\text{Total Error} = \sqrt{x^2+y^2+z^2} \text{ at (A)}$$

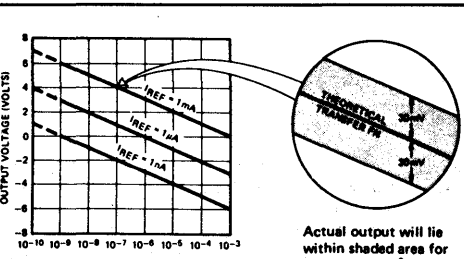
If required, this error can be referred to the system output through the voltage gain of the antilog circuit, using the voltage gain versus input voltage plot.

The numerical values of x, y, and z in the above equation are obtained from the maximum error voltage plots. For example, with the ICL8048BC, the maximum error at the output is 30mV at 25°C. This means that the measured output will be within 30mV of the theoretical transfer function, provided the unit has been adjusted per the procedures described previously. Figure 9 illustrates this point.

To determine the maximum error over the operating temperature range, the 0 to 70°C absolute error values given in the table of electrical characteristics should be used. For intermediate temperatures, assume a linear increase in the error between the 25°C value and the 70°C value.

For the antilog amplifier, the only difference is that the error refers to the input, i.e., the horizontal axis. It will be noticed that the maximum error voltage of the ICL8049, over the temperature range, is strongly dependent on the input voltage. This is because the output amplifier, A_2, has an offset voltage drift which is directly transmitted to the output. When this error is referred to the input, it must be divided by the voltage gain, which is input voltage dependent. At $V_{IN}=3V$, for example, errors at the output are multiplied by 1/.023 (=43.5) when referred to the input.

TRANSFER FUNCTION FOR CURRENT INPUTS



0313-20

Figure 9

It is important to note that both the ICL8048 and the ICL8049 require positive values of I_{REF}, and the input (ICL8048) or output (ICL8049) currents (or voltages) respectively must also be positive. Application of negative I_{IN} to the ICL8048 or negative I_{REF} to either circuit will cause malfunction, and if maintained for long periods, would lead to device degradation. Some protection can be provided by placing a diode between pin 7 and ground.

SETTING UP THE REFERENCE CURRENT

In both the ICL8048 and the ICL8049 the input current reference pin (I_{REF}) is not a true virtual ground. For the ICL8048, a fraction of the output voltage is seen on Pin 16 (Figure 3). This does not constitute an appreciable error provided V_{REF} is much greater than this voltage. A 10V or 15V reference satisfies this condition. For the ICL8049, a fraction of the input voltage appears on Pin 3 (Figure 4), placing a similar restraint on the value of V_{REF}.

Alternatively, I_{REF} can be provided from a true current source. One method of implementing such a current source is shown in Figure 10.

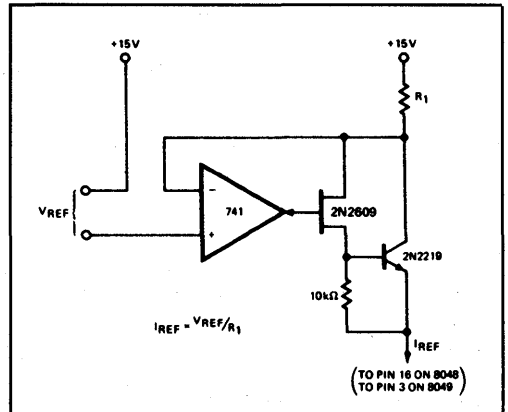
LOG OF RATIO CIRCUIT, DIVISION

The 8048 may be used to generate the log of a ratio by modulating the I_{REF} input. The transfer function remains the same, as defined by equation 9:

$$V_{OUT} = -K\log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \quad (9)$$

Clearly it is possible to perform division using just one ICL8048, followed by an ICL8049. For multiplication, it is generally necessary to use two log amps, summing their outputs into an antilog amp.

To avoid the problems caused by the I_{REF} input not being a true virtual ground (discussed in the previous section), the circuit of Figure 10 is again recommended if the I_{REF} input is to be modulated.



0313-21

Figure 10

NOTE: All typical values have been characterized but are not tested.

DEFINITION OF TERMS

In the definitions which follow, it will be noted that the various error terms are referred to the output of the log amp, and to the input of the antilog amp. The reason for this is explained on the previous page.

DYNAMIC RANGE The dynamic range of the ICL8048 refers to the range of input voltages or currents over which the device is guaranteed to operate. For the ICL8049 the dynamic range refers to the range of output voltage over which the device is guaranteed to operate.

ERROR, ABSOLUTE VALUE The absolute error is a measure of the deviation from the theoretical transfer function, after performing the offset and scale factor adjustments as outlined, (ICL8048) or (ICL8049). It is expressed in mV and referred to the linear axis of the transfer function plot. Thus, in the case of the ICL8048, it is a measure of the deviation from the theoretical output voltage for a given input current or voltage. For the ICL8049 it is a measure of the deviation from the theoretical input voltage required to generate a specific output voltage.

The absolute error specification is guaranteed over the dynamic range.

ERROR, % OF FULL SCALE The error as a percentage of full scale can be obtained from the following relationship:

$$\text{Error, \% of Full Scale} = \frac{100 \times \text{Error, absolute value}}{\text{Full Scale Output Voltage}}$$

TEMPERATURE COEFFICIENT OF V_{OUT} OR V_{IN} For the ICL8048 the temperature coefficient refers to the drift with temperature of V_{OUT} for a constant input current.

For the ICL8049 it is the temperature drift of the input voltage required to hold a constant value of V_{OUT}.

POWER SUPPLY REJECTION RATIO The ratio of the voltage change in the linear axis of the transfer function (V_{OUT} for the ICL8048, V_{IN} for the ICL8049) to the change in the supply voltage, assuming that the log axis is held constant.

WIDEBAND NOISE For the ICL8048, this is the noise occurring at the output under the specified conditions. In the case of the ICL8049, the noise is referred to the input.

SCALE FACTOR For the log amp, the scale factor (K) is the voltage change at the output for a decade (i. e. 10:1) change at the input. For the antilog amp, the scale factor is the voltage change required at the input to cause a one decade change at the output. See equations 9 and 10.

APPLICATION NOTES

For further applications assistance, see

A007 "The ICL8048/8049 Monolithic Log-Antilog Amplifiers"

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

HARRIS · RCA · GE · INTERSIL

ICM7242
Long-Range Fixed Timer

GENERAL DESCRIPTION

The ICM7242 is a CMOS timer/counter circuit consisting of an RC oscillator followed by an 8-bit binary counter. It will replace the 2242 in most applications, with a significant reduction in the number of external components.

Three outputs are provided. They are the oscillator output, and buffered outputs from the first and eighth counters.

FEATURES

- **Replaces The 2242 in Most Applications**
- **Timing From Microseconds to Days**
- **Cascadeable**
- **Monostable or Astable Operation**
- **Wide Supply Voltage Range: 2 – 16 volts**
- **Low Supply Current: 115μA @ 5 volts**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7242IPA	−25°C to +85°C	8 pin MINI-DIP
ICM7242CBA	0°C to +70°C	8 pin S.O.I.C.

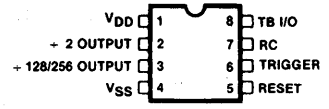


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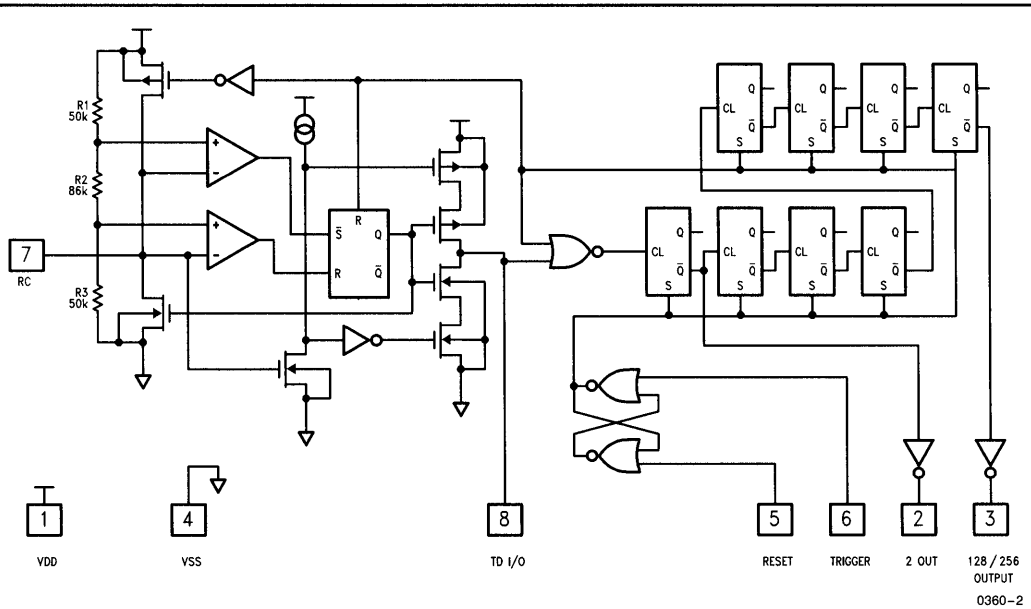
Figure 1: Pin Configuration (Outline Drawing PA)



0360-2

Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to V_{SS}) 18V
Input Voltage [1]
Terminals (Pins 5, 6, 7, 8) ... (V_{SS} −0.3V) to (V_{DD} +0.3V)
Maximum continuous output current
(each output) 50mA
Power Dissipation[2] 200mW
Operating Temperature Range
ICM7242I ..... −25°C to +85°C
ICM7242C ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTES: 1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same supply be applied to the device before its supply is established and, that in multiple supply systems, the supply to the ICM7242 be turned on first.
2. Derate at −2mW/°C above 25°C.

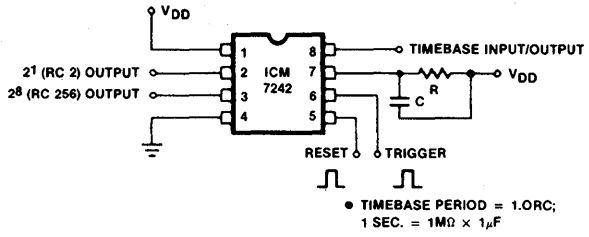
ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, T_A = +25°C, R = 10kΩ, C = 0.1μF, V_{SS} = 0V unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{DD}	Guaranteed Supply Voltage		2		16	V
I_{DD}	Supply Current	Reset		125		μA
		Operating, R = 10kΩ, C = 0.1μF		340	800	μA
		Operating, R = 1MΩ, C = 0.1μF		220	600	μA
		TB Inhibited, RC Connected to V_{SS}		225		μA
	Timing Accuracy			5		%
Δf/ΔT	RC Oscillator Frequency Temperature Drift	Independent of RC Components		250		ppm/°C
V_{OTB}	Time Base Output Voltage	I_{SOURCE} = 100μA		3.5		V
		I_{SINK} = 1.0mA		0.40		V
I_{TBLK}	Time Base Output Leakage Current	RC = Ground			25	μA
V_{TRIG}	Trigger Input Voltage	V_{DD} = 5V		1.6	2.0	V
		V_{DD} = 15V		3.5	4.5	V
V_{RST}	Reset Input Voltage	V_{DD} = 5V		1.3	2.0	V
		V_{DD} = 15V		2.7	4.0	V
I_{TRIG}, I_{RST}	Trigger/Reset Input Current			10		μA
f_t	Max Count Toggle Rate	V_{DD} = 2V } Counter/Divider Mode	2	1		MHz
		V_{DD} = 5V } Counter/Divider Mode		6		MHz
		V_{DD} = 15V } Counter/Divider Mode		13		MHz
		50% Duty Cycle Input with Peak to Peak Voltages Equal to V_{DD} and V_{SS}				
V_{SAT}	Output Saturation Voltage	All Outputs except TB Output		0.22	0.4	V
		V_{DD} = 5V, I_{OUT} = 3.2mA				
I_{SOURCE}	Output Sourcing Current 7242	V_{DD} = 5V		300		μA
		Terminals 2 & 3, V_{OUT} = 1V				
C_t	MIN Timing Capacitor (Note 1)		10			pF
R_t	Timing Resistor Range (Note 1)	V_{DD} = 2–16V	1K		22M	Ω

NOTE: 1. For Design only, not tested.

NOTE: All typical values have been characterized but are not tested.

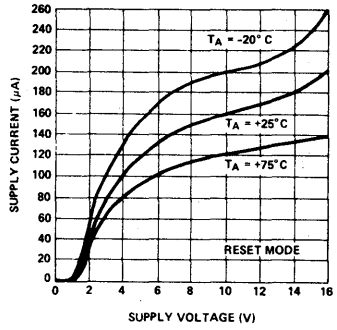


NOTE: OUTPUTS ÷2¹ AND ÷2⁸ ARE INVERTERS AND HAVE ACTIVE PULLUPS.

Figure 3: Test Circuit

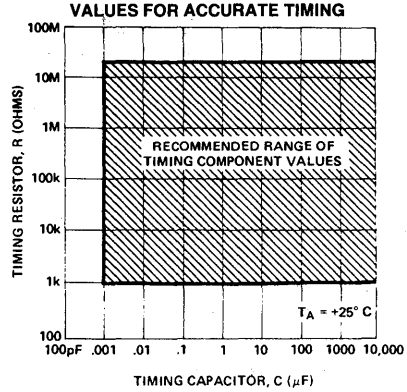
TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



0360-4

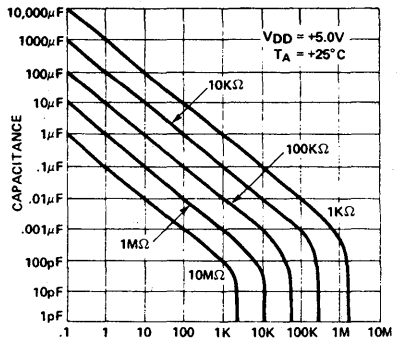
RECOMMENDED RANGE OF TIMING COMPONENT VALUES FOR ACCURATE TIMING



DIMENSIONS IN INCHES AND MILLIMETERS

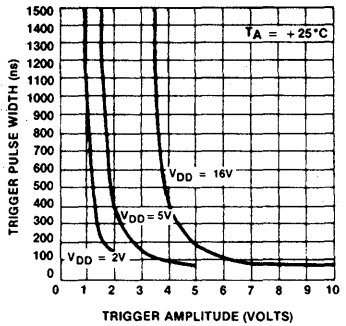
0360-5

TIMEBASE FREE RUNNING FREQUENCY AS A FUNCTION OF R AND C



0360-6

MINIMUM TRIGGER PULSE WIDTH AS A FUNCTION OF TRIGGER AMPLITUDE

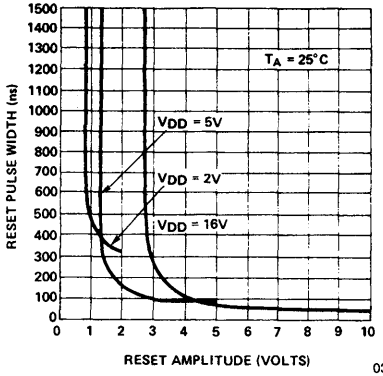


0360-7

NOTE: All typical values have been characterized but are not tested.

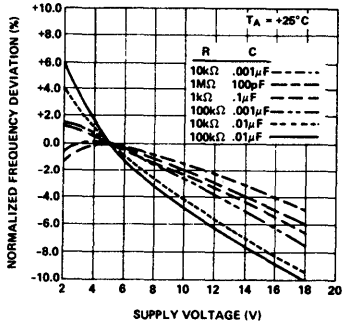
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

MINIMUM RESET PULSE WIDTH AS A FUNCTION OF RESET AMPLITUDE



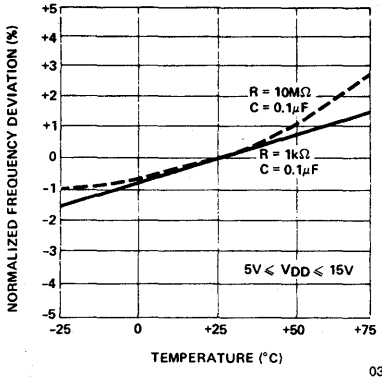
0360-8

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



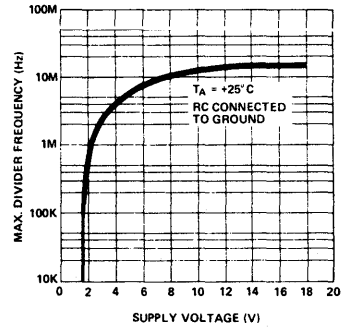
0360-9

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



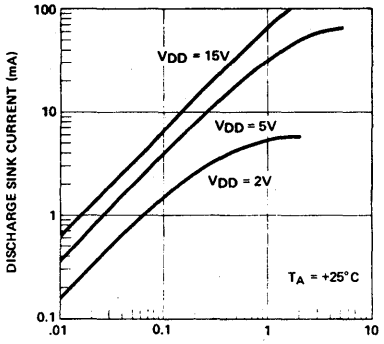
0360-10

MAXIMUM DIVIDER FREQUENCY vs. SUPPLY VOLTAGE



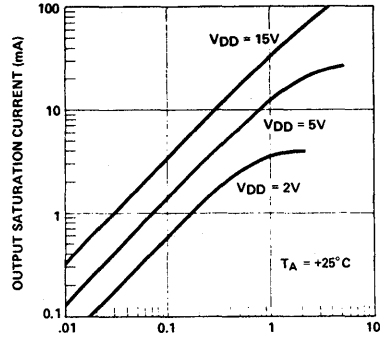
0360-11

DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



0360-12

OUTPUT SATURATION CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



0360-13

8 SPECIAL ANALOG CIRCUITS

NOTE: All typical values have been characterized but are not tested.

OPERATING CONSIDERATIONS

Shorting the RC terminal or output terminals to V_{DD} may exceed dissipation ratings and/or maximum DC current limits (especially at high supply voltages).

There is a limitation of 50pF maximum loading on the TB I/O terminal if the timebase is being used to drive the counter section. If higher value loading is used, the counter sections may miscount.

For greatest accuracy, use timing component values shown in the graph under typical performance characteristics. For highest frequency operation it will be desirable to use very low values for the capacitor; accuracy will decrease for oscillator frequencies in excess of 200KHz.

The timing capacitor should be connected between the RC pin and the positive supply rail, V_{DD}, as shown in Figure 3. When system power is turned off, any charge remaining on the capacitor will be discharged to ground through a large internal diode between the RC node and V_{SS}. Do NOT reference the timing capacitor to ground, since there is no high-current path in this direction to safely discharge the capacitor when power is turned off. The discharge current from such a configuration could potentially damage the device.

When driving the counter section from an external clock, the optimum drive waveform is a square wave with an amplitude equal to supply voltage. If the clock is a very slow ramp triangular, sine wave, etc., it will be necessary to "square up" the waveform; this can be done by using two CMOS inverters in series, operating from the same supply voltage as the ICM7242.

The ICM7242 is a non-programmable timer whose principal applications will be very low frequency oscillators and long range timers; it makes a much better low frequency oscillator/timer than a 555 or ICM7555, because of the on-chip 8-bit counter. Also, devices can be cascaded to produce extremely low frequency signals.

Because outputs will not be AND'd, output inverters are used instead of open drain N-channel transistors, and the external resistors used for the 2242 will not be required for the ICM7242. The ICM7242 will, however, plug into a socket for the 2242 having these resistors.

The timing diagram for the ICM7242 is shown in Figure 4. Assuming that the device is in the RESET mode, which occurs on powerup or after a positive signal on the RESET terminal (if TRIGGER is low), a positive edge on the trigger input signal will initiate normal operation. The discharge transistor turns on, discharging the timing capacitor C, and all the flip-flops in the counter chain change states. Thus, the outputs on terminals 2 and 3 change from high to low states. After 128 negative timebase edges, the $\div 2^8$ output returns to the high state.

To use the 8-bit counter without the timebase, terminal 7 (RC) should be connected to ground and the outputs taken from terminals 2 and 3.

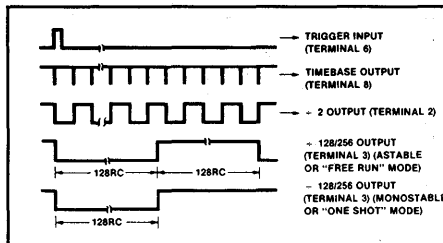


Figure 4: Timing Diagrams of Output Waveforms for the ICM7242. (Compare with Figure 8)

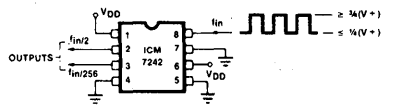


Figure 5: Using the ICM7242 as a Ripple Counter (Divider)

The ICM7242 may be used for a very low frequency square wave reference. For this application the timing components are more convenient than those that would be required by a 555 timer. For very low frequencies, devices may be cascaded (see Figure 6).

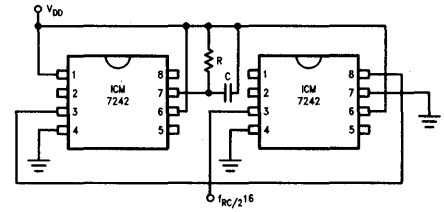


Figure 6: Low Frequency Reference (Oscillator)

For monostable operation the $\div 2^8$ output is connected to the RESET terminal. A positive edge on TRIGGER initiates the cycle (NOTE: TRIGGER overrides RESET).

The ICM7242 is superior in all respects to the 2242 except for initial accuracy and oscillator stability. This is primarily due to the fact that high value p⁻ resistors have been used on the ICM7242 to provide the comparator timing points.

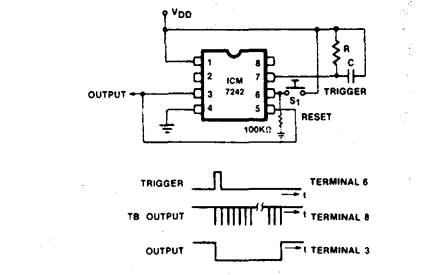


Figure 7: Monostable Operation

NOTE: All typical values have been characterized but are not tested.

COMPARING THE ICM7242 WITH THE 2242

	ICM7242	2242
a. Operating Voltage	2 – 16V	4 – 15V
b. Operating Temp. Range	−25°C to +85°C	0°C to +70°C
c. Supply Current V_{DD} = 5V	0.7mA Max.	7mA Max.
d. Pullup Resistors		
TB Output	No	Yes
÷2 Output	No	Yes
÷256 Output	No	Yes
e. Toggle Rate	3.0MHz	0.5MHz
f. Resistor to Inhibit Oscillator	No	Yes
g. Resistor in Series with Reset for Monostable Operation	No	Yes
h. Capacitor TB Terminal for HF Operation	No	Sometimes

By selection of R and C, a wide variety of sequence timing can be realized. A typical flow chart for a machine tool controller could be as follows:

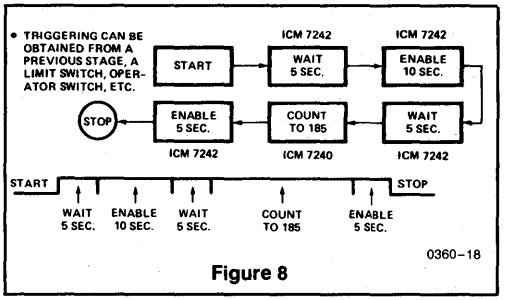


Figure 8

By cascading devices, use of low cost CMOS AND/OR gates and appropriate RC delays between stages, numerous sequential control variations can be obtained. Typical applications include injection molding machine controllers, phonograph record production machines, automatic sequencers (no metal contacts or moving parts), milling machine controllers, process timers, automatic lubrication systems, etc.

SEQUENCE TIMING

- **Process Control**
- **Machine Automation**
- **Electro—Pneumatic Drivers**
- **Multi—Operation (Serial or Parallel Controlling)**

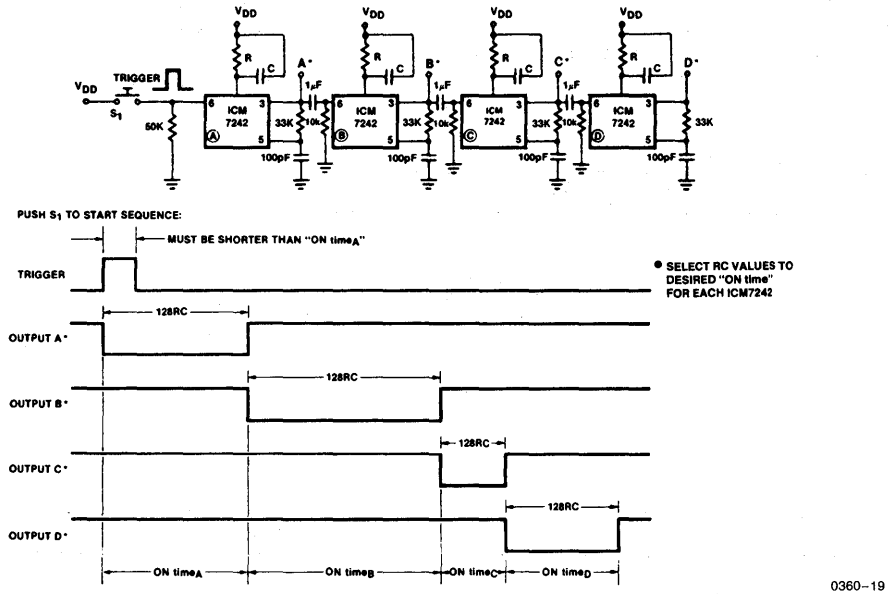


Figure 9: Sequence Timer

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR
HARRIS · RCA · GE · INTERSIL

ICM7555/ICM7556
General Purpose Timer

GENERAL DESCRIPTION

The ICM7555/6 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low THRESHOLD, $\overline{\text{TRIGGER}}$ and $\overline{\text{RESET}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the ICM7555/6 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V^+ and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar 555/6 devices, the CONTROL VOLTAGE terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

FEATURES

- **Exact Equivalent in Most Cases for SE/NE555/556 or TLC555/556**
- **Low Supply Current — 60μA Typ. (ICM7555) 120μA Typ. (ICM7556)**
- **Extremely Low Trigger, Threshold and Reset Currents — 20pA Typical**
- **High Speed Operation — 1MHz Typical**
- **Wide Operation Supply Voltage Range Guaranteed 2 to 18 Volts**
- **Normal Reset Function - No Crowbarring of Supply During Output Transition**
- **Can Be Used With Higher Impedance Timing Elements Than Regular 555/6 for Longer RC Time Constants**
- **Timing From Microseconds Through Hours**
- **Operates in Both Astable and Monostable Modes**
- **Adjustable Duty Cycle**
- **High Output Source/Sink Driver Can Drive TTL/CMOS**
- **Typical Temperature Stability of 0.005% Per °C at 25°C**
- **Outputs Have Very Low Offsets, HI and LO**

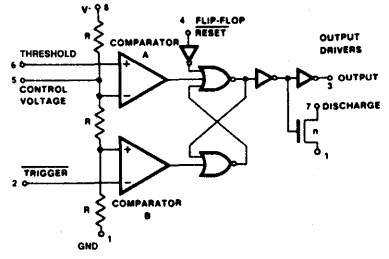
ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7555CBA	0°C to +70°C	8 Lead SOIC
ICM7555IPA	−25°C to +85°C	8 Lead MiniDip
ICM7555ITV	−25°C to +85°C	TO-99 Can
ICM7555MTV*	−55°C to +125°C	TO-99 Can
ICM7556IPD	−25°C to +85°C	14 Lead Plastic DIP
ICM7556MJD*	−55°C to +125°C	14 Lead CERDIP

*Add /883B to part number if 883B processing is desired.

APPLICATIONS

- **Precision Timing**
- **Pulse Generation**
- **Sequential Timing**
- **Time Delay Generation**
- **Pulse Width Modulation**
- **Pulse Position Modulation**
- **Missing Pulse Detector**



0363-1

This Functional Diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs. R = 100kΩ, ±20% typ.

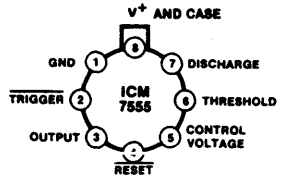
Figure 1: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

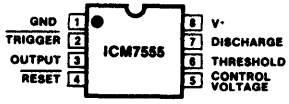
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +18 Volts
Input Voltage: $\overline{\text{Trigger}}$,
Control Voltage, Threshold, $\overline{\text{Reset}}$[1] .... $V^+ + 0.3V$ to GND −0.3V
Output Current 100mA
Power Dissipation[2] ICM7556 ..... 300mW
ICM7555 ..... 200mW
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Operating Temperature Range[2]
ICM7555/6 CX ..... 0°C to +70°C
ICM7555/6 IX ..... −25°C to +85°C
ICM7555/6 MX ..... −55°C to +125°C

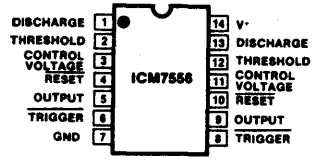
NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



(OUTLINE DRAWING TV)



(OUTLINE DRAWING PA)



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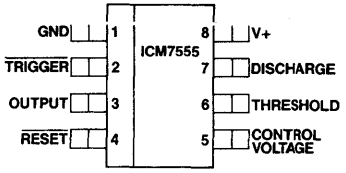


0363-3

(OUTLINE DRAWING BA)

0363-2

Figure 2: Pin Configuration (Top View)

NOTES 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than $V^+ + 0.3V$ or less than $V^- - 0.3V$ may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power-supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.

2: Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20 mW at 125°C. Below 125°C power dissipation may be increased to 300 mW at 25°C. Derating factor is approximately 3 mW/°C (7556) or 2 mW/°C (7555).

NOTE: All typical values have been characterized but are not tested.

ICM7555
ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	ICM7555C,I,M			ICM7555M			Units
			$T_A = 25°C$			$-55°C \le T_A \le +125°C$			
			Min	Typ	Max	Min	Typ	Max	
I^+	Static Supply Current	$V_{DD} = 5V$ $V_{DD} = 15V$		40 60	200 300			300 300	µA µA
	Monostable Timing Accuracy	RA = 10k, C = 0.1µF, $V_{DD} = 5V$		2		858		1161	% µs
	Drift with Temp*	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$					150 200 250		ppm/°C ppm/°C ppm/°C
	Drift with Supply*	$V_{DD} = 5$ to 15V		0.5			0.5		%/V
	Astable Timing Accuracy	RA = RB = 10k, C = 0.1µF, $V_{DD} = 5V$		2		1717		2323	% µs
	Drift with Temp*	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$					150 200 250		ppm/°C ppm/°C ppm/°C
	Drift with Supply*	$V_{DD} = 5V$ to 15V		0.5			0.5		%/V
V_{TH}	Threshold Voltage	$V_{DD} = 15V$	62	67	71	61		72	% V_{DD}
V_{TRIG}	Trigger Voltage	$V_{DD} = 15V$	28	32	36	27		37	% V_{DD}
I_{TRIG}	Trigger Current	$V_{DD} = 15V$			10			50	nA
I_{TH}	Threshold Current	$V_{DD} = 15V$			10			50	nA
V_{CV}	Control Voltage	$V_{DD} = 15V$	62	67	71	61		72	% V_{DD}
V_{RST}	Reset Voltage	$V_{DD} = 2$ to 15V	0.4		1.0	0.2		1.2	V
I_{RST}	Reset Current	$V_{DD} = 15V$			10			50	nA
I_{DIS}	Discharge Leakage	$V_{DD} = 15V$			10			50	nA
V_{OL}	Output Voltage Drop	$V_{DD} = 15V$, $I_{sink} = 20mA$ $V_{DD} = 5V$, $I_{sink} = 3.2mA$		0.4 0.2	1.0 0.4			1.25 0.5	V V
V_{OH}	Output Voltage Drop	$V_{DD} = 15V$, $I_{source} = 0.8mA$ $V_{DD} = 5V$, $I_{source} = 0.8mA$	14.3 4.0	14.6 4.3		14.2 3.8			V V
V_{DIS}	Discharge Output Voltage Drop	$V_{DD} = 5V$, $I_{SINK} = 15mA$ $V_{DD} = 15V$, $I_{sink} = 15mA$		0.2	0.4			0.6 0.4	V V
V^+	Supply Voltage*	Functional Oper.	2.0		18.0	3.0		16.0	V
t_R	Output Rise Time*	RL = 10M, CL = 10pF, $V_{DD} = 5V$		75					ns
t_F	Output Fall Time*	RL = 10M, CL = 10pF, $V_{DD} = 5V$		75					ns
f_{MAX}	Oscillator Frequency*	$V_{DD} = 5V$, RA = 470Ω, RB = 270Ω C = 200pF		1					MHz

*These parameters are based upon characterization data and are not tested.

NOTE: All typical values have been characterized but are not tested.

ICM7556

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, unless otherwise specified.

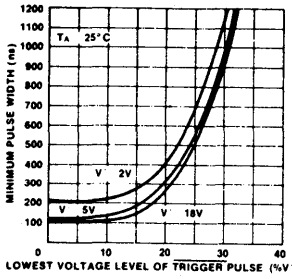
Symbol	Parameter	Test Conditions	ICM7556I,M $T_A = 25°C$			ICM7556M $-55°C \le T_A \le +125°C$			Units
			Min	Typ	Max	Min	Typ	Max	
I^+	Static Supply Current	$V_{DD} = 5V$ $V_{DD} = 15V$		80 120	400 600			600 600	µA µA
	Monostable Timing Accuracy	$RA = 10k, C = 0.1\mu F, V_{DD} = 5V$		2		858		1161	% µs
	Drift with Temp*	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$					150 200 250		ppm/°C ppm/°C ppm/°C
	Drift with Supply*	$V_{DD} = 5V$ to 15V		0.5			0.5		%/V
	Astable Timing Accuracy	$RA = RB = 10k, C = 0.1\mu F, V_{DD} = 5V$		2		1717		2323	% µs
	Drift with Temp*	$V_{DD} = 5V$ $V_{DD} = 10V$ $V_{DD} = 15V$					150 200 250		ppm/°C ppm/°C ppm/°C
	Drift with Supply*	$V_{DD} = 5V$ to 15V		0.5			0.5		% V
V_{TH}	Threshold Voltage	$V_{DD} = 15V$	62	67	71	61		72	% V_{DD}
V_{TRIG}	Trigger Voltage	$V_{DD} = 15V$	28	32	36	27		37	% V_{DD}
I_{TRIG}	Trigger Current	$V_{DD} = 15V$			10			50	nA
I_{TH}	Threshold Current	$V_{DD} = 15V$			10			50	nA
V_{CV}	Control Voltage	$V_{DD} = 15V$	62	67	71	61		72	% V_{DD}
V_{RST}	Reset Voltage	$V_{DD} = 2V$ to 15V	0.4		1.0	0.2		1.2	V
I_{RST}	Reset Current	$V_{DD} = 15V$			10			50	nA
I_{DIS}	Discharge Leakage	$V_{DD} = 15V$			10			50	nA
V_{OL}	Output Voltage Drop	$V_{DD} = 15V, I_{sink} = 20mA$ $V_{DD} = 5V, I_{sink} = 3.2mA$		0.4 0.2	1.0 0.4			1.25 0.5	V V
V_{OH}	Output Voltage Drop	$V_{DD} = 15V, I_{source} = 0.8mA$ $V_{DD} = 5V, I_{source} = 0.8mA$	14.3 4.0	14.6 4.3		14.2 3.8			V V
V_{DIS}	Discharge Output Voltage Drop	$V_{DD} = 5V, I_{sink} = 15mA$ $V_{DD} = 15V, I_{sink} = 15mA$		0.2	0.4			0.6 0.4	V V
V^+	Supply Voltage*	Functional Oper.	2.0		18.0	3.0		16.0	V
t_R	Output Rise Time*	$RL = 10M, CL = 10pF, V_{DD} = 5V$		75					ns
t_F	Output Fall Time*	$RL = 10M, CL = 10pF, V_{DD} = 5V$		75					ns
f_{MAX}	Oscillator Frequency*	$V_{DD} = 5V, RA = 470\Omega,$ $RB = 270\Omega, C = 200pF$		1					MHz

*These parameters are based upon characterization data and are not tested.

NOTE: All typical values have been characterized but are not tested.

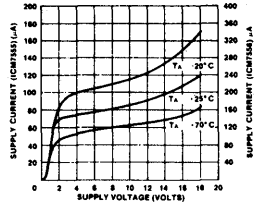
TYPICAL PERFORMANCE CHARACTERISTICS

MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING



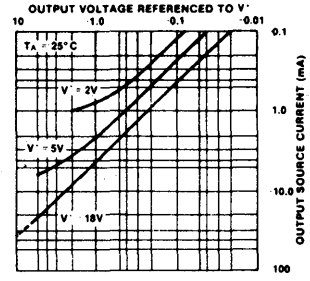
0363-4

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



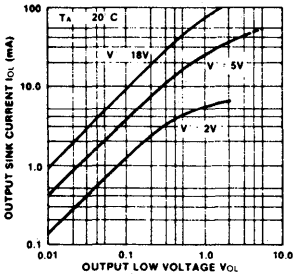
0363-5

OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



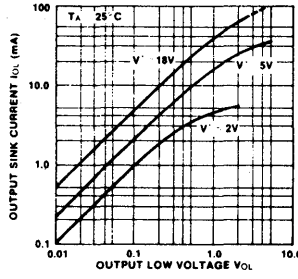
0363-6

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



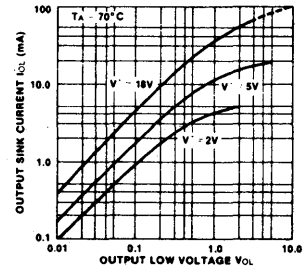
0363-7

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



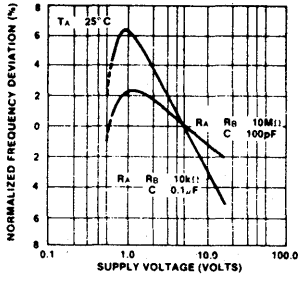
0363-8

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



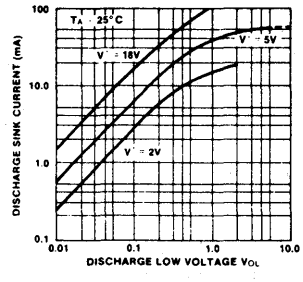
0363-9

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE



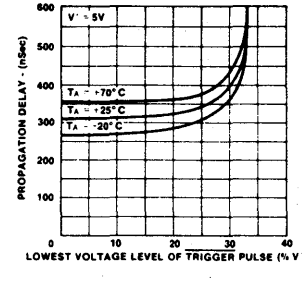
0363-10

DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE



0363-11

PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE

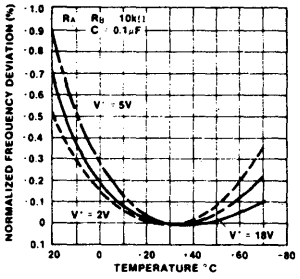


0363-12

NOTE: All typical values have been characterized but are not tested.

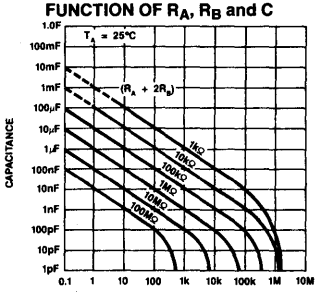
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE



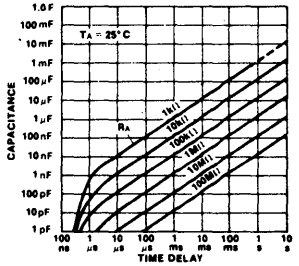
0363-13

FREE RUNNING FREQUENCY AS A FUNCTION OF R_A, R_B and C



0363-14

TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF R_A AND C

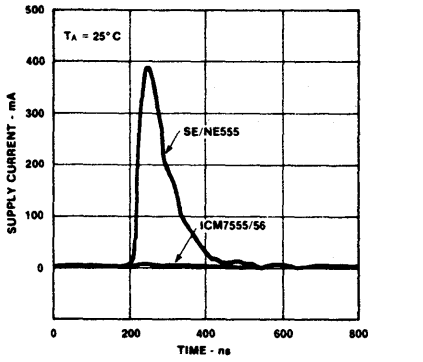


0363-15

APPLICATION NOTES

GENERAL

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economies in the external component count using the ICM7555/6. Because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The 7555/6 devices produce no such transients. See Figure 3.



0363-16

Figure 3: Supply Current Transient Compared with a Standard Bipolar 555 During an Output Transition

The ICM7555/6 produces supply current spikes of only 2 – 3mA instead of 300 – 400mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications 2 capacitors can be saved using an ICM7555, and 3 capacitors with an ICM7556.

POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 4 and 5.

OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 volts or more the ICM7555/6 will drive at least 2 standard TTL loads.

ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 4. The output swings from rail to rail, and is a true 50% duty cycle square wave. (Trip points and output swings are symmetrical). Less than a 1% frequency variation is observed, over a voltage range of +5 to +15V.

$$f = \frac{1.44}{RC}$$

The timer can also be connected as shown in Figure 4b. In this circuit, the frequency is:

$$f = 1.44/(R_A + 2R_B)C$$

The duty cycle is controlled by the values of R_A and R_B, by the equation:

$$D = R_B/(R_A + 2R_B)$$

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative $\overline{\text{TRIGGER}}$ pulse to pin 2, the internal flip flop is set which releases the short circuit across the external capacitor and drives the OUTPUT high. The voltage across the capacitor now increases exponentially with a time constant $t = R_AC$. When the voltage across the capacitor equals $\frac{2}{3}$ V^+, the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{TRIGGER}}$ must return to a high state before the OUTPUT can return to a low state.

$$t_{output} = -\ln(\tfrac{1}{3})\, R_AC = 1.1\, R_AC$$

8

SPECIAL ANALOG CIRCUITS

NOTE: All typical values have been characterized but are not tested.

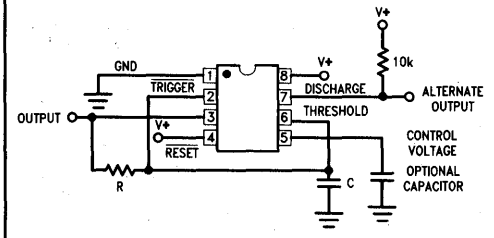


Figure 4a: Astable Operation

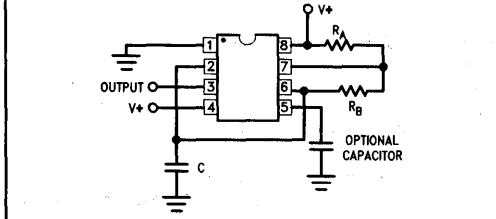


Figure 4b:

CONTROL VOLTAGE

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and $\overline{\text{TRIGGER}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

$\overline{\text{RESET}}$

The $\overline{\text{RESET}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e. 0.6 to 0.7 volts. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{RESET}}$ function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

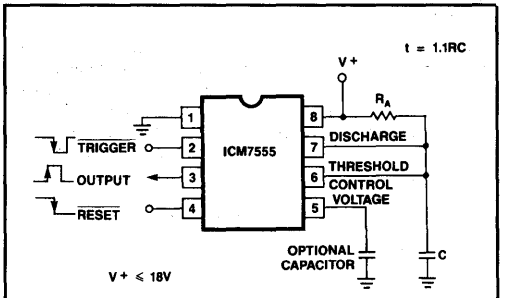


Figure 5: Monostable Operation

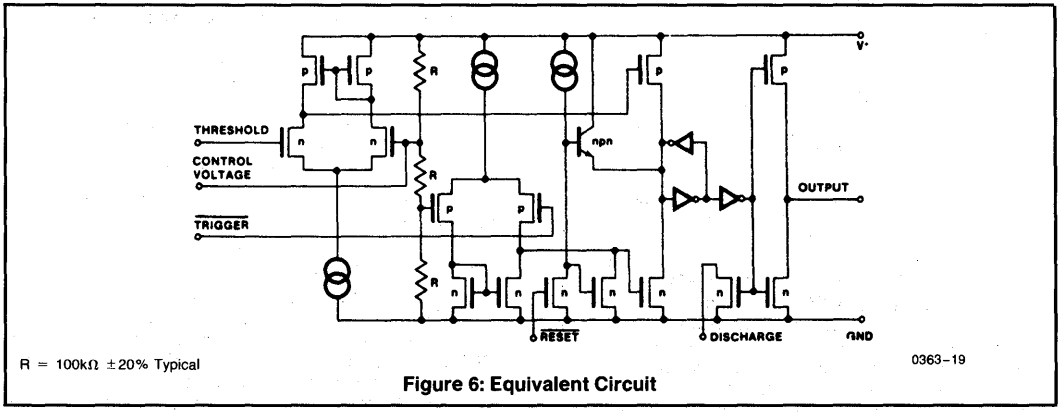


Figure 6: Equivalent Circuit

NOTE: All typical values have been characterized but are not tested.

TRUTH TABLE

Threshold Voltage	$\overline{\text{Trigger}}$ Voltage	$\overline{\text{RESET}}$	Output	Discharge Switch
DON'T CARE	DON'T CARE	LOW	LOW	ON
$>\frac{2}{3}(V^+)$	$>\frac{1}{3}(V^+)$	HIGH	LOW	ON
$<\frac{2}{3}(V^+)$	$>\frac{1}{3}(V^+)$	HIGH	STABLE	STABLE
DON'T CARE	$<\frac{1}{3}(V^+)$	HIGH	HIGH	OFF

NOTE: $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

NOTE: All typical values have been characterized but are not tested.

LINEAR 9

HARRIS QUALITY AND RELIABILITY

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THE IMPROVEMENT PROCESS	9-3
DESIGNING FOR MANUFACTURABILITY	9-5
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Introduction

Success in the integrated circuit industry means more than simply meeting or exceeding the demands of today's market. It also includes anticipating and accepting the challenges of the future. It results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force — from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added on or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of The Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX programs and working with manufacturing to establish control charts, Quality professionals are involved in the measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs — with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

The Improvement Process

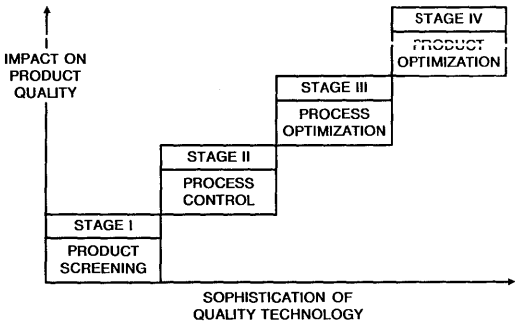


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage II to Stage III, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Wafer Fab	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Junction Depth	X	
	- Sheet Resistivities	X	
	- Defect Density	X	X
	- Critical Dimensions	X	X
	- Visual Inspection	X	X
	- Lot Acceptance		X
	• Process		
	- Film Thickness	X	X
	- Implant Dosages	X	
	- Capacitance Voltage Changes	X	X
	- Conformance to Specification	X	X
	• Equipment		
	- Repeatability	X	X
	- Profiles	X	X
	- Calibration		X
	- Preventive Maintenance	X	X
Assembly	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Documentation Check		X
	- Dice Inspection	X	X
	- Wire Bond Pull Strength/Controls	X	X
	- Die Sear Controls		X
	- Pre-Seal Visual	X	X
	- Fine/Gross Leak	X	X
	- PIND Test	X	
	- Lead Finish Visuals, Thickness	X	X
	- Die Shear		X
	- Solderability		X
	• Process		
	- Operator Quality Performance	X	X
	- Saw Controls	X	
	- Die Attach Temperatures	X	X
	- Seal Parameters	X	
	- Seal Temperature Profile	X	X
	- Sta-Bake Profile	X	
	- Temp Cycle Chamber Temperature	X	X
	- ESD Protection	X	X
	- Plating Bath Controls	X	
	- Mold Parameters	X	X
Test	• JAN Self-Audit		X
	• Temperature/Humidity	X	X
	• ESD Controls	X	
	• Temperature Test Calibration	X	
	• Test System Calibration	X	
	• Test Procedures		X
	• Control Unit Compliance	X	
	• Lot Acceptance Conformance	X	
	• Group A Lot Acceptance		X
Probe	• JAN Self-Audit		X
	• Wafer Repeat Correlation	X	
	• Visual Requirements	X	X
	• Documentation	X	X
	• Process Performance	X	X

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (CONTINUED)

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Burn-In	• JAN Self-Audit		X
	• Functionality Board Check	X	
	• Oven Temperature Controls	X	
	• Procedural Conformance		X
Brand	• JAN Self-Audit		X
	• ESD Controls	X	X
	• Brand Permanency	X	X
	• Temperature/Humidity	X	X
	• Procedural Conformance		X
QCI Inspection	• JAN Self-Audit		X
	• Group B Conformance		X
	• Group C and D Conformance		X

Designing For Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment.

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).

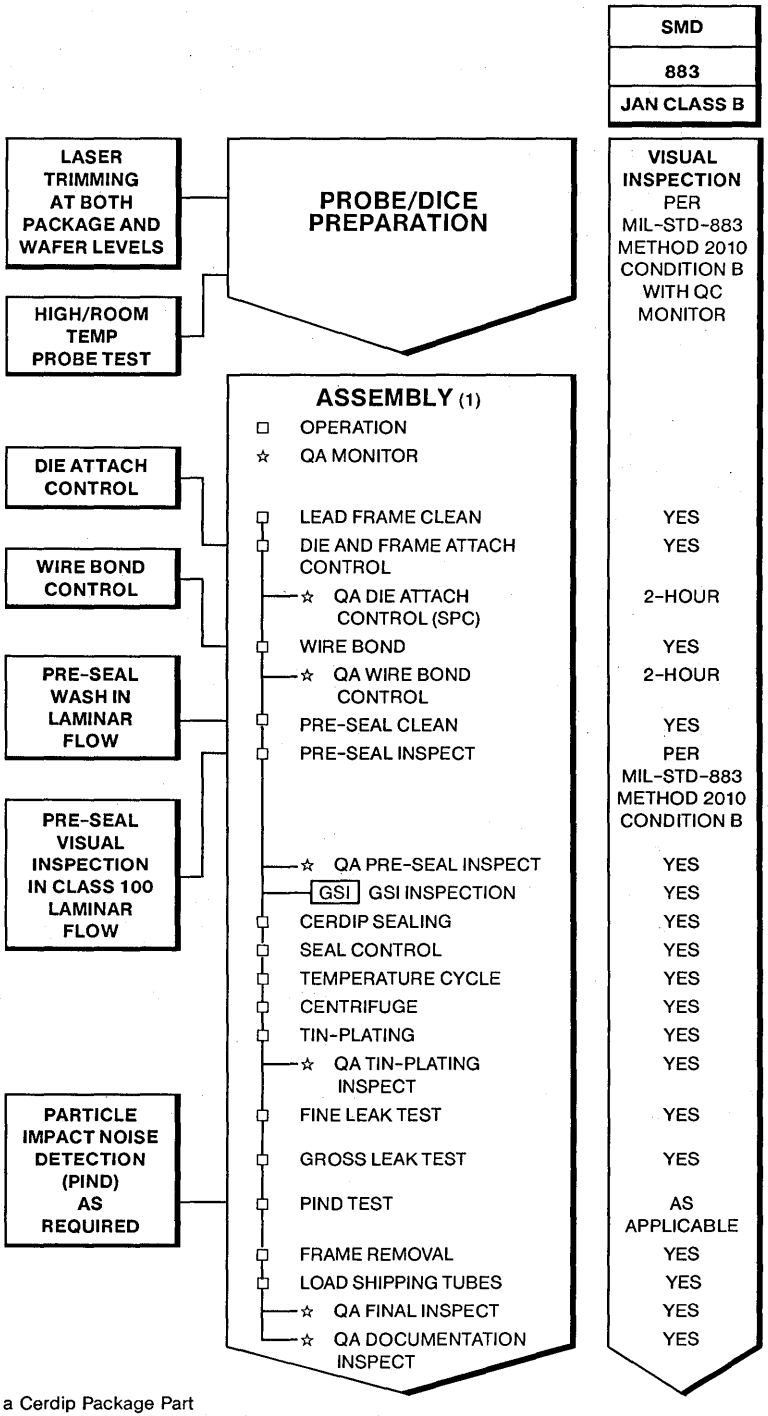
TABLE 2. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

Special Testing

Harris Semiconductor offers several standard screen flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than +25°C. The flows shown on pages 9-6 and 9-7 indicate the Harris standard screening processes. In addition, Harris can supply products tested to customer specifications both for electrical requirements and for non-standard environmental stress screening. Consult your field sales representative for details.

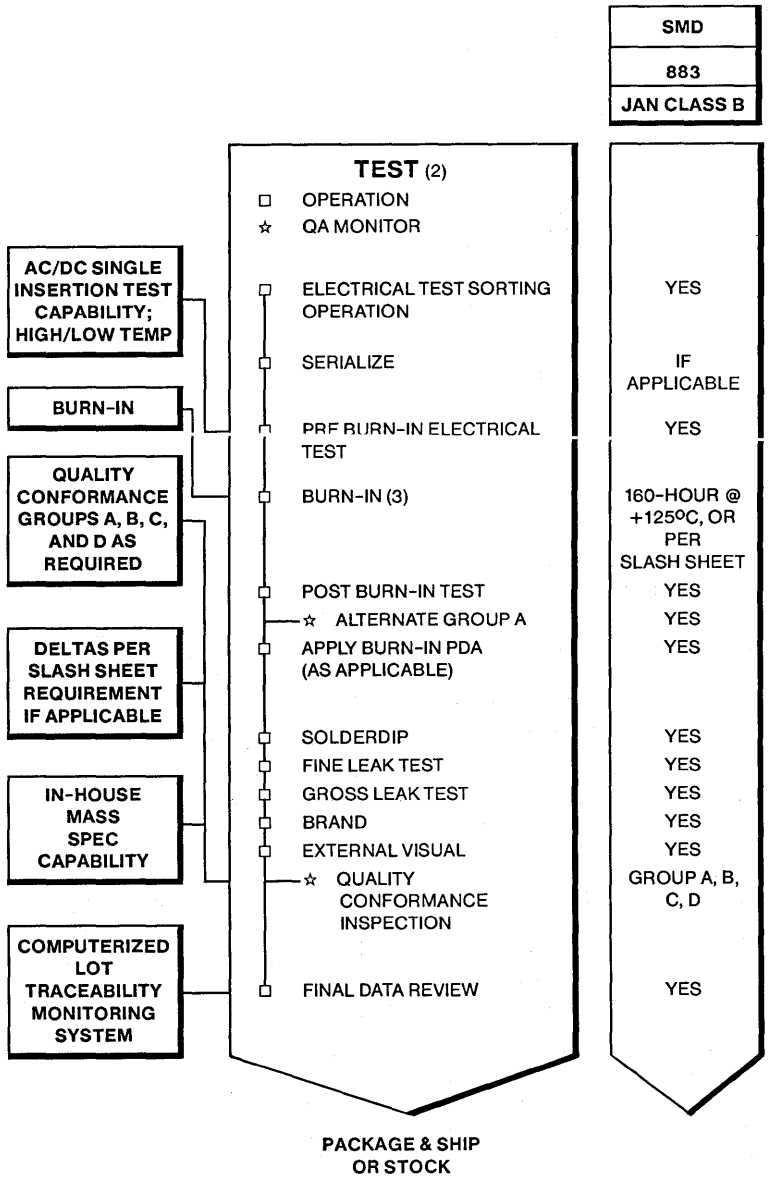
Harris Semiconductor Standard Processing Flows



(1) Example for a Cerdip Package Part

Harris Semiconductor Standard Processing Flows

(Continued)



(2) -55°C TO +125°C

(3) Burn-In test temperatures can be increased and time reduced per regression tables in Mil-Std-883, Method 1015.

TABLE 3. SUMMARIZING CONTROL APPLICATIONS

FAB			
• Diffusion - Junction Depth - Sheet Resistivities - Oxide Thickness - Implant Dose Calibration - Uniformity	• Thin Film - Film Thickness - Uniformity - Refractive Index - Film Composition	• Photo Resist - Critical Dimension - Resist Thickness - Etch Rates	• Measurement Equipment - Critical Dimension - Film Thickness - 4 Point Probe - Ellipsometer
ASSEMBLY			
• Pre-Seal - Die Prep Visuals - Yields - Die Attach Heater Block - Die Shear - Wire Pull - Saw Blade Wear - Pre-Cap Visuals	• Post-Seal - Internal Package Moisture - Tin Plate Thickness - PIND Defect Rate - Solder Thickness - Leak Tests - Module Rm. Solder Pot Temp. - Seal - Temperature Cycle	• Measurement - XRF - Radiation Counter - Thermocouples - GM-Force Measurement	
TEST			
	- Handlers/Test Systems - Defect Pareto Charts - Lot % Defective - ESD Failures per Month	- Monitor Failures - Lead Strengthening Quality - After Burn-In PDA	
OTHER			
• IQC - Vendor Performance - Material Criteria - Quality Levels	• Environment - Water Quality - Clean Room Control	• IQC Measurement/Analysis - XRF - ADE - 4 Point Probe - Chemical Analysis Equipment	

Controlling and Improving the Manufacturing Process - SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use over 1,000 Shewhart control charts to determine the normal variabilities in processes, materials, and products. Critical process variables are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that a variable is outside the process control limits or indicates a trend toward the limit. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

But SPC is only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost.

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at reducing the number of defects by studying the key variables controlling the process, and optimizing the procedures or design to yield the best result. This approach is a more time-

TABLE 4. HARRIS I.C. DESIGN TOOLS

	PRODUCTS	
DESIGN STEP	ANALOG	DIGITAL
Functional Simulation	Slice	Silos Proteous Socrates
Parametric Simulation	Slice Monte Carlo	Slice
Schematic Capture	Note 1	Daisy SDA-Mass Comp
Functional Checking	Note 1	SDA-LVS
Rules Checking	Calma-DRC	Harris Dash
Parasitic Extraction	Note 1	SDA-LVS

NOTE 1. Tools are in Development.

consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in MIL-STD-883 and MIL-M-38510 are used by our quality inspectors.

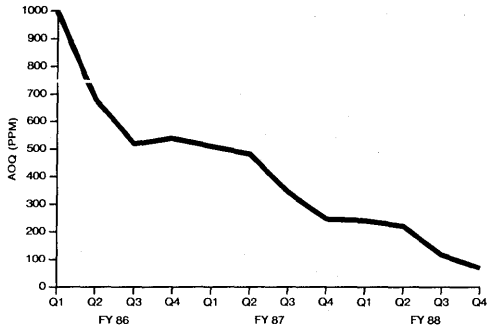


FIGURE 2. DEFECTIVE PARTS PER MILLION

The focus on this quality parameter has resulted in a continuous improvement over the past three years. AOQ has improved from 1,000 PPM to less than 100 PPM, and the goal for 1989 is to continue improvement toward a goal of 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of the University of Tennessee, private consultants, and internally developed programs, training of over 2,000 engineers, supervisors, and operators/technicians has been completed.

Nearly 1,000 operators, 100 supervisors, and more than 800 engineers have been trained in SPC methods, providing them with tools to improve the overall level of uniformity of Harris products. Almost 300 engineers have received training in DOX methods: learning to evaluate changes in process operations, set up new processes, select or accept new equipment, evaluate materials, select vendors, compare two or more pieces of equipment, and compare two or more process techniques.

Over the past four years, Harris has also deployed a comprehensive training program for hourly operators and supervisors in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	LENGTH	TOPICS COVERED
SPC	Manufacturing Operators	8 Hours	Basic Philosophy, Statistical Calculations Graphing Techniques, Pareto Charts, Control Charts
SPC	Manufacturing Supervisors	21 Hours	Basic Philosophy, Statistical Calculations Graphing Techniques, Pareto Charts, Control Charts, Testing for Inspector Agreement, Cause & Effect Diagrams, 1 & 2 Sample Methods
SPC	Engineers and Managers	48 Hours	Basic Philosophy, Graphical Methods, Control Charts, Rational Subgrouping, Variance Components, 1 & 2 Sample Methods, Pareto Charts, Cause & Effect Diagrams
DOX (Design of Experiments)	Engineers and Managers	88 Hours	Factorial Designs, Fractional Factorial Designs, Blocking Designs, Variance Components, Computer Usage, Normal Probability Plotting
RSM (Response Surface Methods)	Engineers and Managers	40 Hours	Steepest Ascent, Central Composite Designs, Box-Behnken Designs, Computer Usage, Contour Plotting, Second Order Response Surfaces
Continuous Improvement Methods	Manufacturing Supervisors	12 Hours	Basic Philosophy, Pareto Analysis, Imagineering, Run Charts, Cause & Effect Diagrams, Histograms, Ideas of Control Charts
SPC- The Essentials	Department-Level Work Groups	20 Hours	Basic Philosophy, of Continous Improvement, Imagineering Pareto Charts, Cause & Effect Diagrams, Flow Charts, Graphical Display, Control Charts, Ideas of Experiment

Incoming Materials

With statistical procedures in place to improve quality in the manufacturing operation, the impact of silicon, chemicals, gases, and other materials used in processing the product has become more measurable. Quality and consistency are important; it is logical to feed the manufacturing line with materials manufactured by vendors using equivalent statistical controls.

In order to ensure optimum quality of materials purchased from vendors, Harris initiated and coordinated an aggressive program to link key suppliers to our manufacturing operations. This network is formed by certifying strategic vendors who meet the highest quality standards while demonstrating a commitment to the use of statistical controls in their manufacturing operations.

SPC seminars, development of open working relationships, understanding of manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. Certified suppliers have passed stringent quality and SPC audits, while continuing to supply material with 100% conformance to Harris requirements.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors, who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts - Oxygen - Resistivity • Control Charts Related to - Enhanced Gettering - Total Thickness Variation - Total Indicated Reading - Particulates • Certificate of Analysis for all Critical Parameters
Chemicals/Photoresists/ Gases	• Chemicals - Assay - Major Contaminants • Molding Compounds - Spiral Flow - Thermal Characteristics • Gases - Impurities • Photoresists - Viscosity - Film Thickness - Solids - Pinholes	• Certificate of Analysis on all Critical Parameters • Control Charts - Assay - Contaminants - Water - Selected Parameters • Control Charts - Assay - Contaminants • Control Charts on - Photospeed - Thickness - UV Absorbance - Filterability - Water - Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts - Assay - Contaminants - Dimensional Characteristics • Certificate of Analysis for all Critical Parameters
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Lead Integrity • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

Manufacturing Science - CAM, JIT

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened — in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

A key adjunct to the CAM activity is Just In Time (JIT) material management. This is more than an inventory reduction technique: in many cases it involves reorganization of facilities and people. The essential concept is to form work units that are responsible for doing the whole job rather than bits of it. An employee has control over equipment, maintenance, cleanliness, scheduling, material, quality, and improvements.

In one Harris example, a photoresist flow consisting of several steps was previously organized in the classical departmentalized way. The inspection and etch areas were in different serial locations from the deposition and alignment areas. Work piled up at the slowest operation (inspection), and quality problems detected there were decoupled from the areas producing them by 20 to 30 feet and at least one day. Rework rates were very high; scrap was unacceptable.

When the area was reorganized into GT (group technology) cells (a basic concept of JIT), the inspection and alignment areas were physically coupled and people were organized into teams. The whole job (finished, defect-free wafers) was assigned to the GT cell (see Figure 3). Rework rates decreased 70%, scrap rates decreased 45%, and probe yields increased by 50%. This is only one of hundreds of examples of how JIT has improved our factory performance.

The JIT program/system works. This cultural change is vital and the benefits derived are impressive.

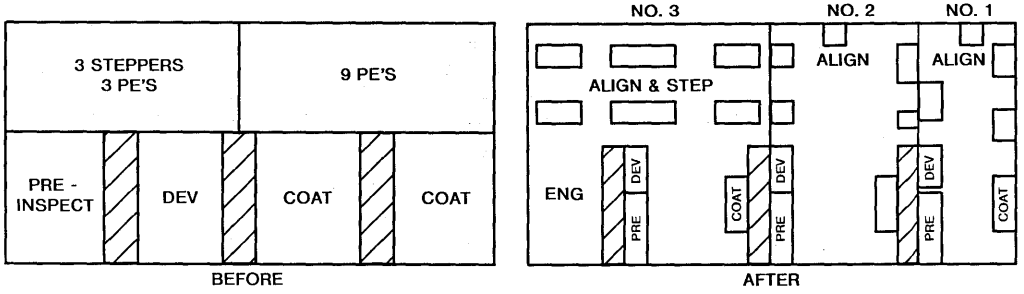


FIGURE 3. GROUP TECHNOLOGY CELL

Measurement

Analytical Services Laboratory

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies. The capabilities of each area are shown below.

SPECTROSCOPIC METHODS: Colorimetry, Optical Emission, Ultraviolet Visible, Fourier Transform-Infrared, Flame Atomic Absorption, Furnace Organic Carbon Analyzer, Mass Spectrometer.

CHROMATOGRAPHIC METHODS: Gas Chromatography, Ion Chromatography.

THERMAL METHODS: Differential Scanning Colorimetry, Thermogravimetric Analysis, Thermomechanical Analysis.

PHYSICAL METHODS: Profilometry, Microhardness, Rheometry.

CHEMICAL METHODS: Volumetric, Gravimetric, Specific Ion Electrodes.

ELECTRON MICROSCOPE: Transmission Electron Microscopy, Scanning Electron Microscope.

X-RAY METHODS: Energy Dispersive X-ray Analysis (SEM), Wavelength Dispersive X-ray Analysis (SEM), X-ray Fluorescence Spectrometry, X-ray Diffraction Spectrometry.

SURFACE ANALYSIS METHODS: Scanning Auger Microprobe, Electron Spectroscope/Chemical Analysis, Secondary Ion Mass Spectrometry, Ion Scattering Spectrometry, Ion Microprobe.

The department also maintains ongoing working arrangements with commercial, university, and equipment manufacturers' technical service laboratories, and can obtain any materials analysis in cases where instrumental capabilities are not available in our own facility.

Calibration Laboratory

Another important resource in the product assurance system is Harris Semiconductor's Calibration Lab. This area is responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both the production and engineering areas. The accuracy of instruments used at Harris in calibration is traceable to the National Bureau of Standards. The lab maintains a system which conforms to the current revision of MIL-STD-45662, "Calibration System Requirements."

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Failure Analysis Laboratory

The Failure Analysis Laboratory's capabilities encompass the isolation and identification of all failure modes/failure mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. Research vital to understanding the basic physics of the failure is also undertaken.

Failure analysis is a method of enhancing product reliability and determining corrective action. It is the final and crucial step used to isolate potential reliability problems that may have occurred during reliability stressing. Accurate analysis results are imperative to assess effective corrective actions. To ensure the integrity of the analysis, correlation of the failure mechanism to the initial electrical failure is essential.

A general failure analysis procedure has been established in accordance with the current revision of MIL-STD-883, Section 5003. The analysis procedure was designed on the premise that each step should provide information on the failure without destroying information to be obtained from subsequent steps. The exact steps for an analysis are determined as the situation dictates. Records are maintained by laboratory personnel and contain data, the failure analyst's notes, and the formal Product Analysis Report.

Reliability

Reliability Assessment and Enhancement

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing process. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life. Product reliability is maintained through the following sources: Qualifications, In-Line Reliability Monitors, Failure Analysis.

Qualifications

Qualifications at Harris de-emphasize the sole dependence on production product which is only available late in the development cycle. The focus is primarily on the use of test vehicles to establish design ground rules for the product and the process that will eliminate any wearout mechanisms during the useful life of the product. However, to comply with the military requirements concerning reliability, product qualifications are performed.

In-line Reliability Monitors

In-line reliability monitors provide immediate feedback to manufacturing regarding the quality of workmanship, quality of raw materials, and the ultimate reliability implications. The rudimentary implementation of this monitoring is the "First Line of Defense," which is a pass/fail acceptance procedure based on control charts and trend analysis. The second level of monitoring is referred to as the "Early Warning System" and incorporates wafer level reliability concepts for extensive diagnostic and characterization capabilities of various components that may impact the device reliability or stability. The quick feedback from these schemes allows more accurate correlation to process steps and corrective actions.

Failure Analysis

Failure analysis of various product failures provides a means for determining critical failure mechanisms. This information is used to identify those mechanism that should be detectable by qualification procedures or in-line monitors. Failure analysis involves elaborate confirmation of the failure mechanism creating the product malfunction.

Reliability Fundamentals

Reliability, by its nature, is a mixture of engineering and probability statistics. This combination has derived a vocabulary of terms essential for describing the reliability of a device or system. Since reliability involves a measurement of time, it is necessary to accelerate the failures which may occur. This, then, introduces terms like "activation energy" and "acceleration factor," which are needed to relate results of stressing to normal operating conditions (see Table 7). Also, to assess product reliability requires failures. Therefore, only a statistical sample can be used to determine the model of the failure distribution for the entire population of product.

TABLE 7. FAILURE RATE PRIMER

GLOSSARY OF TERMS

TERMS/DEFINITION	UNITS/DESCRIPTION
FAILURE RATE λ For Semiconductors, usually expressed in FITs. Represents useful life failure rate (which implies a constant failure rate). FITs are not applicable for infant mortality or wearout failure rate expressions.	**FIT - Failure In Time** 1 FIT - 1 failure in 10^9 device hours. Equivalent to 0.0001%/1000 hours FITs = $\frac{\text{\# Failures}}{\text{\# Devices x \# hours stress x AF}} \times 10^9 \times m$ m - Factor to establish Confidence Interval 10^9 - Establishes in terms of FITs AF - Acceleration Factor at temperature for a given failure mechanism
MTTF - Mean Time To Failure For semiconductors, MTTF is the average or mean life expectancy of a device. If an exponential distribution is assumed then the mean time to fail of the population will be when 63% of the parts have failed.	Mean Time is measured usually in hours or years. 1 Year = 8760 hours When working with a constant failure rate the MTTF can be calculated by taking the reciprocal of the failure rate. MTTF = $1/\lambda$ (exponential model) Example: =10 FITs at +55°C The MTTF is: MTTF = $1/\lambda = 0.1 \times 10^9$ hours = 100M hours
CONFIDENCE INTERVAL (C. I.) Establishes a Confidence Interval for failure rate predictions. Usually the upper limit is most significant in expressing failure rates.	Example: "10 FITs @ a 95% C. I. @ 55°C" means *only* that you are 95% certain the the FITs <10 at +55°C use conditions.

Failure Rate Calculations

Reliability data for products may be composed of several different failure mechanisms and requires careful combining of diverse failure rates into one comprehensive failure rate. Calculating the failure rate is further complicated because failure mechanisms are thermally accelerated at varying rates and thereby have differing accelerating factors. Additionally, this data is usually obtained a variety of life tests at unique stress temperatures. The equation below accounts for these considerations and then inserts a statistical factor to obtain the confidence interval for the failure rate.

$$FIT = \left(\sum_{i=1}^{B} \frac{X_i}{\sum_{j=1}^{K} TDH_j \; AF_{ij}} \right) \times 10^9 \quad \times M$$

B = # of distinct possible failure mechanisms

K = # of life tests being combined

X_i = # of failures for a given failure mechanism i = 1, 2, . . . B

TDG_j = Total device hours of test time (unaccelerated) for Life Test$_j$

AF_{ij} = Acceleration factor for appropriate failure mechanism i = 1, 2, . . . K

M = Statistical factor for calculating the upper confidence limit (M is a function of the total number of failures and an estimate of the standard deviation of the failure rates)

In the failure rate calculation, Acceleration Factors (AF_{ij}) are used to derate the failure rate from thermally accelerated Life Test conditions to a failure rate indicative of use temperatures. Though no standards exist, a temperature of +55°C has been popular and allows some comparison of product failure rates. All Harris Semiconductor Reliability Reports will derate to +55°C at both the 60% and 95% confidence intervals.

Acceleration Factors

The Acceleration Factors (AF) are determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and is an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP \left[\frac{E_a}{K} \left(\frac{1}{T_{use}} - \frac{1}{T_{stress}} \right) \right]$$

AF = Acceleration Factor

E_a = Thermal Activation Energy in eV from Table 8

K = Boltzmann's Constant (8.62×10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature. With the use of the Arrhenius Equation, the thermal Activation Energy (E_a) term is a major influence on the result. This term is usually empirically derived and can vary widely.

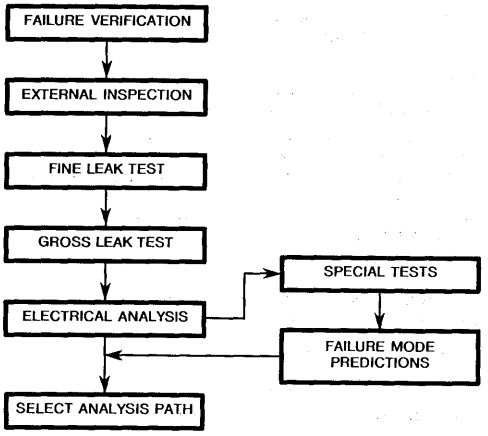


FIGURE 4. NON-DESTRUCTIVE

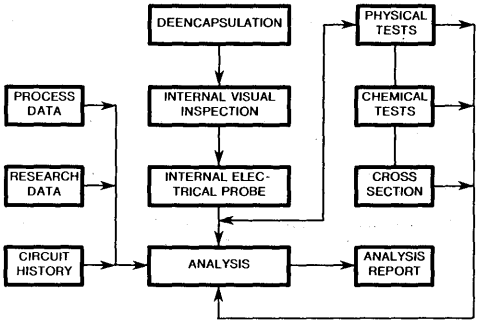


FIGURE 5. DESTRUCTIVE

Activation Energy

To determine the Activation Energy (E_a) of a mechanism (see Table 8) you must run at least two (preferably more) tests at different stresses (temperature and/or voltage). The stresses will provide the time to failure (Tf) for the populations which will allow the simultaneous solution for the Activation Energy by putting the experimental results into the following equations.

$$\ln (t_{f1}) = C + \frac{E_a}{KT_1}$$

$$\ln (t_{f2}) = C + \frac{E_a}{KT_2}$$

Then, by subtracting the two equations, the Activation Energy becomes the only variable, as shown.

$$\ln(t_{f1}) - \ln(t_{f2}) = E_a/k(1/T1-1/T2)$$

$$E_a = K^* ((\ln(t_{f1}) - \ln(t_{f2}))/(1/T1 - 1/T2))$$

The Activation Energy may be estimated by graphical analysis plots. Plotting ln time and ln temperature then provides a convenient nomogram that solves (estimates) the Activation Energy.

Table 9 is a summary of military generic groups by process descriptions.

All Harris Reliability Reports from qualifications and Group C1 (all high temperature operating life tests) will provide the data on all factors necessary to calculate and verify the reported failure rate (in FITs) using the methods outlined in this primer.

TABLE 8. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3 - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3 - 0.5eV	HTOL & voltage stress screens.	Vendor Statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress tesing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5 - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistcal Process Control of assembly processes proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles Statistical Process Control or photoresist-/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test (EWS) and HTOL.	Statistical Process Control of C-V data, oxide/ interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL & oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

Qualification Procedures

New products are reliably introduced to market by the proper use of design techniques and strict adherence to process layout ground rules. Each design is reviewed from its conception through early production to ensure compliance to minimum failure rate standards. Ongoing monitoring of reliability performance is accomplished through compliance to 883C and standard Quality Conformance Inspection as defined in Method 5005.

New process/product qualifications have two major requirements imposed. First is a check to verify the proper use of process methodology, design techniques, and layout ground rules. Second is a series of stress tests designed to accelerate failure mechanisms and demonstrate the reliability of integrated circuits.

From the earliest stages of a new product's life, the design phase, through layout, and in every step of the manufacturing process, reliability is an integral part of every Harris Semiconductor product. This kind of attention to detail "from the ground up" is the reason why our customers can expect the highest quality for any application.

TABLE 9. HIGH TEMPERATURE OPERATING LIFE TEST SUMMARY

GROUP C

GENERIC GROUP	GROUP NAME	PROCESS DESCRIPTION	QUANTITY	QUANTITY FAILURE	HOURS @ 125°C	FAILURE RATE FITs @ 55°C 60% CI
D-49-3	Op. Amplifiers	Std. Linear, DI w/NiCr resistors	3482	6	3,215,708	62
D-49-4	Op. Amplifiers	Std. Linear, DI w/NiCr resistors	324	1	429,945	17
D-53	High Voltage Op. Amplifiers	High voltage DI	315	0	284,943	20
D-56	Data Acquisition	High beta high frequency, DI, NiCr	1022	5	1,868,349	100
F-103	Telecommunications	SAJI IVA	199	0	403,960	5
F-81-3	A/D Converters	SAJI IVA	201	0	183,222	10
F-81-4	A/D Converters	SAJI IVA	217	1	328,000	12
F-82	Switches & Mux	DI Al Gate & Si Gate MOS	121	0	82,836	23
F-99-3	Active Filters	SAJI IVA	196	1	184,262	24
F-99-4	Active Filters	SAJI IVA	407	1	470,324	9
G-85	Op. Amplifiers	Std. Linear, MOS, & High Frequency JFET	532	1	535,728	11
G-86	Comparators	Combination, Std. Linear & MOS	154	0	153,400	25
G-94-3	Switches & Mux	DI Al & Si Gate Linear CMOS	4351	41	7,443,054	103
G-94-4	Switches & Mux	DI Al & Si Gate Linear CMOS	906	0	889,816	20
C-41-4	CMOS RAMs	SAJI CMOS	2418	19	2,247,526	31
C-41-5	CMOS RAMs	SAJI CMOS	1104	10	1,105,094	53
C-42-4	CMOS PROMs & HPALs	SAJI CMOS	2645	28	4,074,728	61
C-105-4	Microprocessor and Peripherals	SAJI CMOS	3638	12	4,099,002	17

NOTE: All infant mortality failures (up to 168 hours or equivalent) have been removed from products sampled.

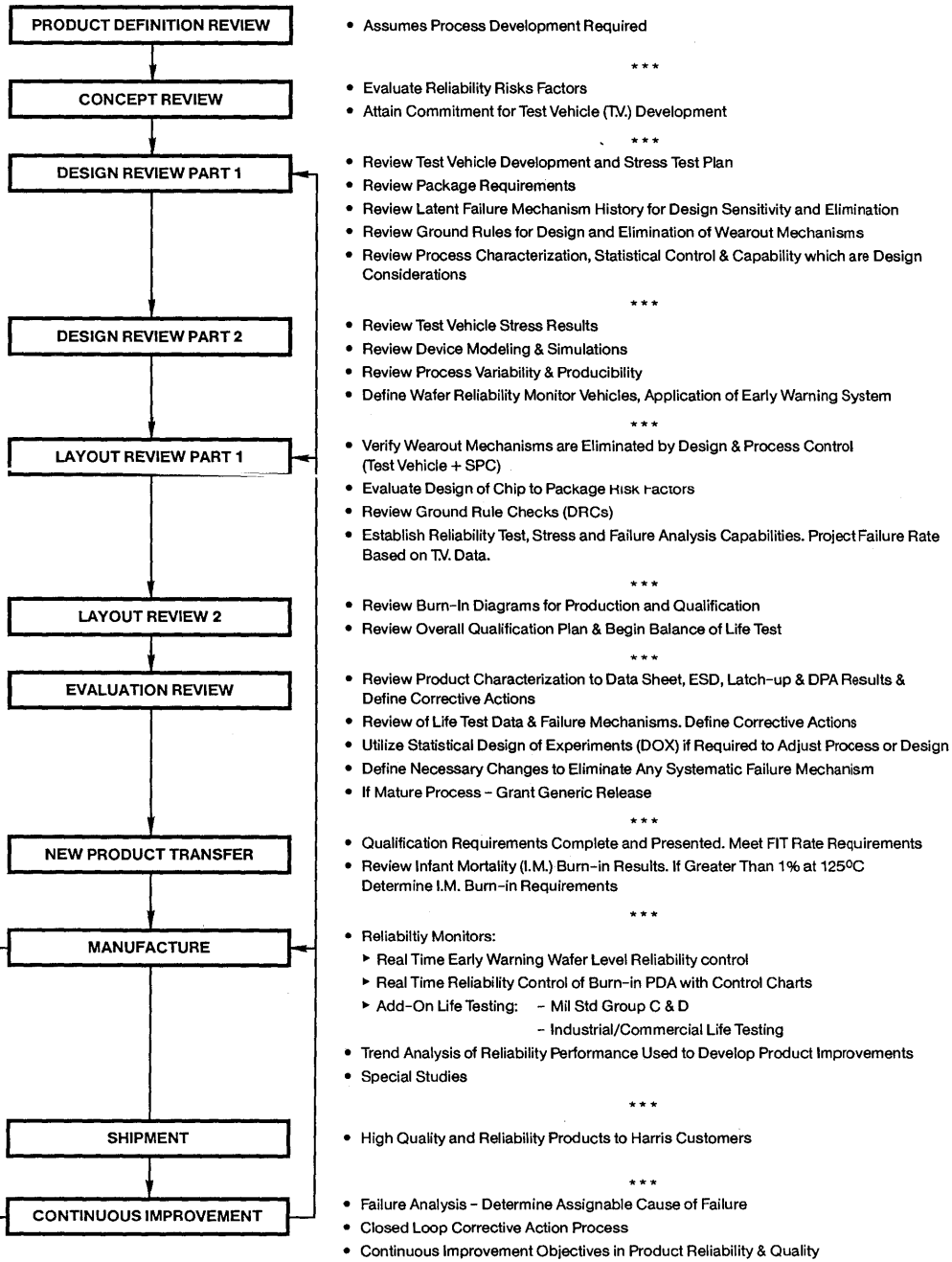


FIGURE 6. NEW PROCESS PRODUCT DEVELOPMENT AND LIFE CYCLE

LINEAR 10

APPLICATION NOTE ABSTRACTS

AN#	TITLE	ABSTRACTS
509	A Simple Comparator Using The HA-2620	Performance characteristics, application schematics, output parameter control methods.
514	The HA-2400 PRAM Four Channel Operational Amplifier	HA-2400 PRogrammable Analog Microcircuit description, frequency compensation, applications (analog multiplexer, non-inverting programmable gain amplifier, inverting programmable gain amplifier, programmable attenuator, programmable adder-subtractor, phase selector, phase detector, synchronous rectifier, balanced modulator, integrator, ramp generator, track and hold, sample and hold, sine wave oscillator, multivibrator, active filter, programmable power supply, comparator, multiplying D/A converter).
515	Operational Amplifier Stability: Input Capacitance Considerations	Input capacitance and stability, capacitive feedback compensation, guidelines for compensation requirements.
517	Applications of a Monolithic Sample and Hold/ Gated Op Amp	General Sample and Hold information and fourteen specific applications, including filtered Sample & Hold DAC de-glitcher, Integrate-Hold-Reset, gated op amp, etc.
519	Operational Amplifiers Noise Prediction.	Noise model and equations, procedure for computing total output noise, example, broadband noise measurement, spot noise prediction techniques, typical spot noise curves, popcorn noise discussion.
525	HA-5190/5195 Fast Settling Operational Amplifier	Internal schematic, prototyping considerations, frequency compensation, performance enhancement methods, applications.
526	HA-5190/5195 Video Applications	Video applications, video response tests, S/N ratio measurements, power supply requirements temperature considerations, design hints, prototyping tips, RF AGC amplifier, DC gain controlled video amplifier.
538	Monolithic Sample/Hold Combines Speed and Precision	Description and electrical specifications for the HA-5320 Sample/Hold Amplifiers, explanation of errors sources, and HA-5320 applications.
540	HA-5170 Precision Low Noise J-FET Input Operational Amplifier	Internal design and technology, J-FET noise discussion, trimming of offset voltage, single op amp Instrumentation Amplifier, sine wave oscillator, high impedance transducer interface, current source/sink and current sense circuits.
541	Using HA-2539/2540 Very High Slew-Rate Wideband Operational Amplifiers	Prototyping considerations, output short circuit protection, offset voltage adjustment, frequency compensation, composite amplifier scheme, DC error reduction, boosting output current, increasing output signal swing, cascade amplifier, video gain block, high frequency oscillator, wideband signal splitter.
544	Micropower Op Amp Family, HA-514X, HA-515X	Operation, noise performance, applications (remote sensor loop transmitter, charge pool power supply, low power microphone preamplifier, AGC with squelch control, Wein bridge oscillator, bar code scanner, monostable multivibrator).

Application Note Abstracts (Continued)

AN#	TITLE	ABSTRACTS
546	A Method of Calculating HA-2625 Gain Bandwidth Product vs. Temperature	A method of calculating Gain Bandwidth product performance versus temperature for the HA-2625 Op Amp.
548	A Designer's Guide for the HA-5033 Video Buffer	Operation, video performance, video parameter specifications, Y parameters, applications (flash converter pre-driver, coaxial line driver, video gain block, high speed sample and hold, audio drivers, crystal oscillator).
550	Using the HA-2541	Prototyping guidelines, thermal considerations and heat sinking, performance enhancements, applications (Wein bridge oscillator, high power gain stage, video stage with clamp, multiplexer/demultiplexer, disk drive write amplifier, gain programmable amp, composite amp).
551	Recommended Test Procedures for Operational Amplifiers	Operational amplifier test procedures for offset voltage, bias current, offset current, power supply rejection ratio, common mode rejection ratio, output voltage swing, output current, open loop gain, slew rate, full power bandwidth, transient response, settling time, GBP, phase margin, noise voltage and current, and channel seperation.
552	Using the HA-2542	Prototyping guidelines, thermal considerations and heat sinking, performance enhancements, applications (multi-channel security system, unbalanced coaxial driver, flash converter driver, programmable power supply, bridge load driver, high current stage, differential line driver, DC motor speed control).
553	Using the HA-5147/5137/5127	Construction and operation, low noise design applications (instrumentation amplifier bridge sensor, multiplexer, precision threshold detector, audio driver, NAB amplifier, multivibrator, programmable gain stage, log amp, professional mixer).
554	Low Noise Family HA-5101/5102/5104/5111/5112/5114	Low noise design, operation, applications (Electronic scales, programmable attentuator, Baxandal circuit, RIAA amplifier, NAB preamplifier, microphone amplifier, standard and simple biquads, professional mixer.
555	Ultra Low Bias Amplifier, HA-5180	Construction, layout hints, low noise design, applications (Sample and Hold, precision sample and hold, pH probe, light sensor, photo diode sensor, precision integrator, time, atomic particle counter circuit).
556	Thermal Safe-Operating-Areas for High Current Op Amps	Thermal management equations and curves indicating areas of V_{OUT} and I_{OUT} safe operation. Also, the effects of packaging and heat sinking are examined.
A007	Using the 8048/8049 Monolithic Log-Anti-Log Amplifier	Describes in detail the operation of the 8048 logarithmetic amplifier, and its counterpart, the 8049 anti-log amp.
A011	A Precision Four Quadrant Multiplier - The 8013	Describes, in detail, the operation of the 8013 analog multiplier. Included are multiplication, division, and square root applications.
A013	Everything You Always Wanted to Know About the 8038	This note includes 17 of the most asked questions regarding the use of the 8038.
A027	Power Supply Design Using the ICL8211 and ICL8212	Explains the operation of the ICL8211/12 and describes various power supply configurations. Included are positive and negative voltage regulators, constant current source, programmable current source, current limiting, voltage crowbarring, power supply window detector, etc.
A051	Principles and Applications of the ICL7660 CMOS Voltage Converter	Describes internal operation of the ICL7660. Includes a wide range of possible applications.
A053	The ICL7650 - A New Era in Glitch-Free Chopper Stabilizer Amplifiers	A brief discussion of the internal operation of the ICL7650, followed by an extensive applications section including amplifiers, comparators, log-amps, pre-amps, etc.

Application Note Abstracts (Continued)

AN#	TITLE	ABSTRACTS
ICAN5015	CA3010	Discussion of internal operation and applications.
ICAN5213	CA3015	Discussion of internal operation and applications.
ICAN5269	FM Receivers	Discusses integrated circuits for FM broadcast receivers
ICAN5290	General Purpose Op Amps	Discusses various uses of op amps
ICAN5296	CA3018	Transistor Array
ICAN5337	CA3028	RF amplifiers in the HF and VHF ranges.
ICAN5380	FM IF Amplifiers	Discusses differential amplifier configurations.
ICAN5766	CA3020	Multipurpose wideband power amplifiers
ICAN6048	CA3094	Programmable power switch/amplifier.
ICAN6077	CA3094	OTA with power capability.
ICAN6157	CA3085	Monolithic voltage regulators.
ICAN6182	CA3059	Zero-voltage switches.
ICAN6386	CA3130	Understanding BiMOS op amps.
ICAN6459	CA3130	Why and how to use the BiMOS op amp.
ICAN6525	IC Handling	Guide to IC handling.
ICAN6668	CA3080	High performance OTA.
ICAN6669	CA3240	BiMOS op amp mates directly to system sensors.
ICAN6732	Noise Measurement	Measurement of burst noise and "popcorn" noise in ICs.
ICAN6818	CA3280	OTA simplifies complex analog designs.
ICAN6915	CA1524	Pulse-width modulators.
ICAN7127	CA3420	BiMOS amplifier circumvents low voltage limitations.
ICAN7174	CA1524	Pulse-width modulator in an electronic scale.
ICAN7304	SCR Protection	Discusses SCR Protection Circuits for ICs.
ICAN8636	Video Devices	Discusses advanced video speed switches, multiplexers, crosspoints and buffer amplifiers.
ICAN8707	CA3450	Single chip video line driver-high speed op amp.
ICAN8811	CA5470	BiMOS-E process enhances quad op amp.
ICE-402	Operating Considerations	Discusses operating considerations for solid state devices.
MM2539 MM2540 MM5102 MM5104 MM5112 MM5114 MM5190	Spice Operational Amplifier Macro-Models	Describes the macro-model for these HA-type op amps. Includes a schematic, the SPICE net listing, and simulation curves. Available in a kit which includes a diskette compatible with SPICE and all application notes.

LINEAR 11

PACKAGING INFORMATION

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SOIC Packaging Information

Commercial Signal Processing
Linear Products Offered in SOIC

This table is provided as a guide for selecting devices which are available in Small Outline Packages. Enhanced electrical grades of these devices are available, or planned, as standard offerings. Devices in development at the time of printing are included for future consideration, and are denoted by an '*'. Please consult your nearest Harris Sales Office, Representative or Distributor for the most current information on packaging and availability.

LINEAR SOIC PRODUCT OFFERINGS

PRODUCT	DESCRIPTION	LEAD COUNT	BODY WIDTH (MILS)	OPERATING TEMPERATURE (°C)			
				0/+70	-25/+85	-40/+85	-55/+125
SINGLE OPERATIONAL AMPLIFIERS							
CA3078	Micropower Bipolar	8	150	X	-	-	X
CA3080	Transconductance Amplifier	8	150	X	-	-	X
CA3100	Broadband BiMOS	8	150	-	-	X	-
CA3130	General Purpose BiMOS	8	150	-	-	X	-
CA3140	General Purpose BiMOS	8	150	-	-	-	X
CA3260 *	General Purpose BiMOS	8	150	-	-	-	X
CA3440 *	Nano Power BiMOS	8	150	-	-	-	X
CA3450 *	High Speed High Output	16	300	-	-	-	-
CA5130	General Purpose +5V BiMOS	8	150	-	X	-	X
CA5130A *	General Purpose +5V BiMOS	8	150	-	-	-	X
CA5160 *	General Purpose +5V BiMOS	8	150	-	-	-	X
CA5420 *	Low Bias +5V BiMOS	8	150	-	-	-	X
HA-2505 *	General Purpose	8	150	X	-	X	-
HA-2515 *	High Slew Rate	8	150	X	-	X	-
HA-2525 *	High Slew Rate	8	150	X	-	X	-
HA-2529 *	High Slew Rate High Output	8	150	X	-	X	-
HA-2539	Broadband High Slew Rate	14	150	X	-	X	-
HA-2540	Broadband Fast Settling	14	150	X	-	X	-
HA-2541 *	Broadband Unity Gain	14	150	X	-	-	-
HA-2542 *	Broadband High Output	14	150	X	-	-	-
HA-2544	Video Unity Gain	8	150	X	-	X	-
HA-2548 *	Precision High Speed	8	150	X	-	-	-
HA-2605	General Purpose	8	150	X	-	X	-
HA-2625	Broadband	8	150	X	-	X	-
HA-5004 *	100MHz Current Feedback	14	150	X	-	-	-
HA-5101	Low Noise Unity Gain	8	150	X	-	X	-
HA-5111	Low Noise Broadband	8	150	X	-	X	-
HA-5127 *	Low Noise Precision	8	150	X	-	-	-
HA-5137 *	Low Noise Precision	8	150	X	-	-	-
HA-5141	Low Power Bipolar	8	150	X	-	X	-
HA-5147 *	Precision Broadband	8	150	X	-	-	-
HA-5221 *	Broadband Precision	8	150	X	-	X	-
HA-5195	Fast Settling Wideband	14	150	X	-	X	-
HFA-0001 *	Ultra High Slew Rate	16	300	X	-	X	-
HFA-0002 *	Ultra Wideband Low Noise	8	150	X	-	X	-
HFA-0005 *	Ultra Wideband Unity Gain	8	150	X	-	X	-
ICL7611	Prog. Low Power CMOS	8	150	X	-	-	-
ICL7612	Prog. Low Power CMOS	8	150	X	-	-	-
ICL7650S *	Chopper-Stabilized	14	150	X	X	-	-
ICL7652S *	Chopper-Stab. Low Noise	14	150	X	X	-	-
ICL8021	Prog. Low Power Bipolar	8	150	X	-	-	-

* Product in Development, Lead Count and Body Dimensions may change.

SOIC Packaging Information

LINEAR SOIC PRODUCT OFFERINGS (Continued)

PRODUCT	DESCRIPTION	LEAD COUNT	BODY WIDTH (MILS)	OPERATING TEMPERATURE (°C)			
				0/+70	-25/+85	-40/+85	-55/+125
DUAL OPERATIONAL AMPLIFIERS							
CA158	General Purpose	8	150	-	-	-	X
CA258	General Purpose	8	150	-	X	-	-
CA358	General Purpose	8	150	X	-	-	-
CA2904	General Purpose	8	150	-	-	X	-
CA3240 *	General Purpose BiMOS	16	300	-	X	-	-
CA3280	Transconductance Amplifier	20	300	X	-	-	X
CA5260	General Purpose +5V BiMOS	8	150	-	-	-	X
HA-5102	Low Noise Unity Gain	16	300	X	-	X	-
HA-5112	Low Noise Broadband	16	300	X	-	X	-
HA-5142	Low Power Bipolar	16	300	X	-	X	-
HA-5222 *	Broadband Precision	16	300	X	-	X	-
ICL7621	Low Power CMOS	8	150	X	-	-	-
QUAD OPERATIONAL AMPLIFIERS							
CA124	General Purpose	14	150	-	-	-	X
CA224	General Purpose	14	150	-	-	X	-
CA324	General Purpose	14	150	X	-	-	-
CA5470	Broadband +5V BiMOS	14	150	-	-	-	X
HA-4741	General Purpose	16	300	X	-	X	-
HA-5104	Low Noise Unity Gain	16	300	X	-	X	-
HA-5114	Low Noise Broadband	16	300	X	-	X	-
HA-5134 *	Precision Low Noise	16	300	X	-	-	-
HA-5144	Low Power Bipolar	16	300	X	-	X	-
LM2902	General Purpose	14	150	-	-	X	-
DIFFERENTIAL AMPLIFIERS							
CA3028	Differential/Cascode	8	150	-	-	-	X
CA3053	Differential/Cascode	8	150	-	-	-	X
CA3102	Dual High Frequency	14	150	-	-	-	X
VIDEO BUFFER/CURRENT AMPLIFIERS							
HA-5002	High Slew Rate	8	150	X	-	X	-
HA-5033	Broadband High Slew Rate	8	150	X	-	X	-
COMPARATORS							
CA139	General Purpose	14	150	-	-	-	X
CA239	General Purpose	14	150	-	X	-	-
CA339	General Purpose	14	150	X	-	-	-
CA3290 *	Low Power BiMOS	14	150	-	-	-	X
HA-4905 *	130ns Bipolar Quad	16	300	X	-	-	-
LM2901	General Purpose	14	150	-	-	X	-
LM3302	General Purpose	14	150	-	-	X	-

* Product in Development, Lead Count and Body Dimensions may change.

SOIC Packaging Information

LINEAR SOIC PRODUCT OFFERINGS (Continued)

PRODUCT	DESCRIPTION	LEAD COUNT	BODY WIDTH (MILS)	OPERATING TEMPERATURE (°C)			
				0/+70	-25/+85	-40/+85	-55/+125
SAMPLE & HOLDS							
HA-2425 *	3.2µs Monolithic S/H	14	150	X	-	-	-
HA-5320 *	1.0µs Precision Monolithic	14	150	X	-	-	-
HA-5330 *	0.5µs Precision Monolithic	14	150	X	-	-	-
HA-5340 *	0.7µs Low Distortion Monolithic	14	150	X	-	X	-
ARRAYS							
CA3039	General Purpose Diode	14	150	-	-	-	X
CA3046	General Purpose N-P-N Transistor	14	150	-	-	-	X
CA3081	High Current N-P-N Transistor	16	300	-	-	-	X
CA3082	High Current N-P-N Transistor	16	300	-	-	-	X
CA3083	High Current N-P-N Transistor	16	300	-	-	-	X
CA3086	General Purpose N-P-N Transistor	14	150	-	-	-	X
CA3096	N-P-N/P-N-P Transistor	16	300	-	-	-	X
CA3127	High Frequency N-P-N Transistor	16	300	-	-	-	X
CA3146	High Voltage N-P-N Transistor	14	150	-	-	X	-
CA3183	High Voltage N-P-N Transistor	16	300	-	-	X	-
CA3227	High Frequency N-P-N Transistor	16	300	-	-	-	X
CA3246 *	High Frequency N-P-N Transistor	14	150	-	-	X	-
POWER MANAGEMENT ICs							
CA3094	Prog. Power Switch/Amplifier	8	150	-	-	-	X
ICL7660	CMOS Voltage Converter	8	150	X	-	-	-
ICL7660S	CMOS Voltage Converter	8	150	X	X	-	-
ICL7662 *	CMOS High Voltage Converter	8	150	X	-	-	-
ICL7663S	CMOS Prog. Pos. Voltage Reg.	8	150	X	X	-	-
ICL7665S	CMOS Over/Under Voltage Det.	8	150	X	X	-	-
ICL7665SA *	CMOS Over/Under Voltage Det.	8	150	X	X	-	-
ICL7667	Dual Power MOS Driver	8	150	X	-	-	-
ICL7673	Battery Backup Switch	8	150	X	-	-	-
ICL8211	Programmable Voltage Detector	8	150	X	-	-	-
ICL8212	Programmable Voltage Detector	8	150	X	-	-	-
SPECIAL ANALOG FUNCTION ICs							
CA555	555 Timer	8	150	X	-	-	X
HA-2406	4 Channel Multiplexed Amplifier	16	300	X	-	X	-
HA-2546 *	Wideband Analog Multiplier	16	300	X	-	X	-
ICM7555	CMOS General Purpose Timer	8	150	X	X	-	-
ICM7556 *	Dual ICM7555 Timer	14	150	-	X	-	-

* Product in Development, Lead Count and Body Dimensions may Change.

FOR PRODUCTS WITH PREFIX OF:	THE SOIC PACKAGE CODE IS:	THE TAPE AND REEL CODE IS:
'CA'	'M' Suffix	'M96' Suffix
'HA' or 'HFA'	'9P' Prefix	'-T' Suffix
'ICL' or 'ICM'	'B' Suffix	'-T' Suffix

CA-Type Packaging Information

Linear (CA Series)

Linear ICs are available in a wide variety of package designs. These packages are identified by suffix letters indicated in the chart below. When ordering Linear devices, it is important that the appropriate suffix letter be affixed to the type number as indicated on the price schedule.

PACKAGE	CA SERIES
Dual-In-Line Ceramic	D
Dual-In-Line Plastic	E
Frit-Seal Dual-In-Line Ceramic	F
Quad-In-Line Plastic	Q
Dual-In-Line Formed Lead TO-5	S
TO-5 Style Package	T
Small Outline (SO) Plastic	M

Extra Value Screening

Linear product with extra value screening has an X added to the standard type number in the price list, and is also branded as such. A white dot will indicate location of Pin 1.

Example:

A CA3080E with Extra Value screening is designated CA3080EX in the price list. It is branded CA3080EX plus a white dot at pin number 1.

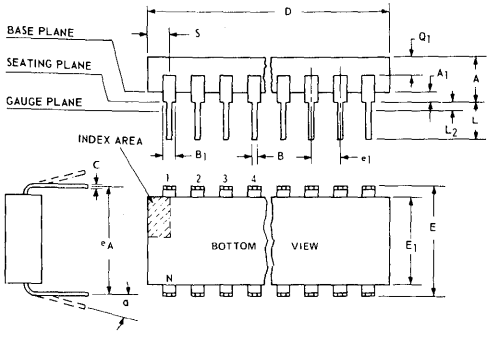
Tape & Reel for Small-Outline Packages

With the introduction of small-outline packages, Harris now offers its customers the convenient tape and reel style packaging. Small-outline devices, which can be tape and reeled, are denoted with the suffix "M96" or "AM96" in the linear and high speed logic product lines. Devices must be ordered in multiples of quantities listed below. Any returns must be full and unopened reels.

LEAD COUNT	TAPE WIDTH IN mm	REEL SIZE INCHES	DEVICES PER REEL
8	12	13	2500
14	16	13	2500
16	16	13	2500
20	24	13	1000
24	24	13	1000

Package Outlines

Dual-In-Line Frit-Seal Ceramic Packages



NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 in. (0.33 mm).
2. Leads within 0.005 in. (0.12 mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. a applies to spread leads prior to installation.
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(F) Suffix (JEDEC MO-001-AB)
14-Lead Dual-In-Line
Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.155	0.200	3.94	5.08	
A_1	0.020	0.050	0.51	1.27	
B	0.014	0.020	0.356	0.508	
B_1	0.050	0.065	1.27	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.745	0.770	18.93	19.55	
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	
L_2	0.000	0.030	0.00	0.76	
a	0°	15°	0°	15°	4
N	14		14		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	
S	0.065	0.090	1.66	2.28	

92SS-4296R3

(F) Suffix (JEDEC MO-001-AC)
16-Lead Dual-In-Line
Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.155	0.200	3.94	5.08	
A_1	0.020	0.050	0.51	1.27	
B	0.014	0.020	0.356	0.508	
B_1	0.035	0.065	0.89	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.745	0.785	18.93	19.93	
E	0.300	0.325	7.62	8.25	
E_1	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	
L_2	0.000	0.030	0.00	0.76	
a	0°	15°	0°	15°	4
N	16		16		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	
S	0.015	0.060	0.39	1.52	

92CM-15967R4

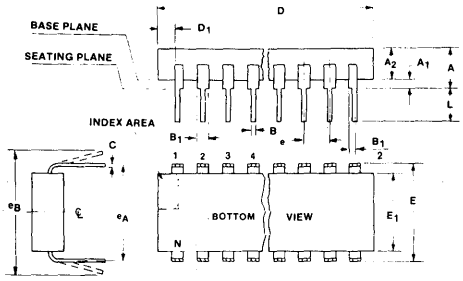
(F) Suffix
18-Lead Dual-In-Line
Frit-Seal Ceramic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.155	0.200	3.94	5.08	
A_1	0.020	0.050	0.508	1.27	
B	0.014	0.020	0.356	0.508	
B_1	0.035	0.065	0.89	1.65	
C	0.008	0.012	0.204	0.304	1
D	0.845	0.885	21.47	22.47	
E_1	0.240	0.260	6.10	6.60	
e_1	0.100 TP		2.54 TYP		2
e_A	0.300 TP		7.62 TYP		2, 3
L	0.125	0.150	3.18	3.81	
α	0°	15°	0°	15°	4
N	18		18		5
N_1	0		0		6
S	0.015	0.060	0.39	1.52	

92CS-30630

Package Outlines

Dual-In-Line Plastic Packages



(E) Suffix (JEDEC MS-001-AB)
8-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.348	0.430	8.84	10.92	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	8		8		11

92CS-39998

(E) Suffix (JEDEC MS-001-AC)
14-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.725	0.795	18.42	20.19	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

92CS-39901

(E) Suffix (JEDEC MS-001-AA)
16-Lead Dual-In-Line Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.745	0.840	18.93	21.33	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

92CS-39900

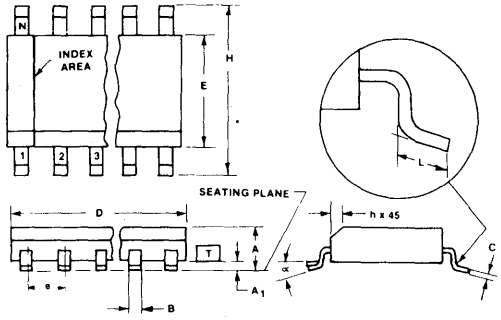
Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

   $1, N, \frac{N}{2}, \frac{N}{2}+1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

Package Outlines

Small-Outline (SO) Packages



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "T" is a reference datum.
4. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

(M) SUFFIX (JEDEC MS-012AA)
8-Lead Dual-In-Line
Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.1890	0.1968	4.80	5.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-39432

(M) SUFFIX (JEDEC MS-012AB)
14-Lead Dual-In-Line
Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38924R1

(M) SUFFIX (JEDEC MS-012AC)
16-Lead Dual-In-Line
Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-38925R1

(M) SUFFIX (JEDEC MS-013AA)
16-Lead Dual-In-Line
Surface-Mount Plastic Package

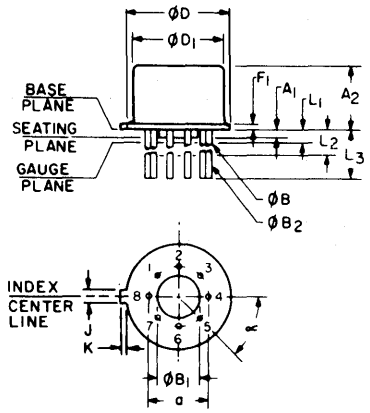
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.0192	0.35	0.49	
C	0.0091	0.0125	0.23	0.32	
D	0.3977	0.4133	10.10	10.50	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

92CS-39433

Package Outlines

TO-5 Style Packages



NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. **Leads at gauge plane within 0.007 in. (0.178 mm) radius of True Position (TP) at maximum material condition.**
2. **ϕB applies between L_1 and L_2. ϕB_2 applies between L_2 and 0.500 in. (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500 in. (12.70 mm).**
3. **Measure from Max. ϕD.**
4. **N_1 is the quantity of allowable missing leads.**
5. **N is the maximum quantity of lead positions.**

(T) Suffix (JEDEC MO-006-AF)
10-Lead TO-5 Style

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
a	0.230 TP		5.84 TP		2
A_1	0	0	0	0	
A_2	0.165	0.185	4.19	4.70	
ϕ_B	0.016	0.019	0.407	0.482	3
ϕB_1	0	0	0	0	
ϕB_2	0.016	0.021	0.407	0.533	3
ϕD	0.335	0.370	8.51	9.39	
ϕD_1	0.305	0.335	7.75	8.50	
F_1	0.020	0.040	0.51	1.01	
j	0.028	0.034	0.712	0.863	
k	0.029	0.045	0.74	1.14	4
L_1	0.000	0.050	0.00	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	36° TP		36° TP		
N	10		10		6
N_1	1		1		5

92CS-15835

(T) Suffix (JEDEC MO-002-AL)
8-Lead TO-5 Style

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
a	0.200 TP		5.88 TP		2
A_1	0.010	0.050	0.26	1.27	
A_2	0.165	0.185	4.20	4.69	
ϕ_B	0.016	0.019	0.407	0.482	3
ϕB_1	0.125	0.160	3.18	4.06	
ϕB_2	0.016	0.021	0.407	0.482	3
ϕD	0.335	0.370	8.51	9.39	
ϕD_1	0.305	0.335	7.75	8.50	
F_1	0.020	0.040	0.51	1.01	
j	0.028	0.034	0.712	0.863	
k	0.029	0.045	0.74	1.14	4
L_1	0.000	0.050	0.00	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	45° TP		45° TP		
N	8		8		6
N_1	3		3		5

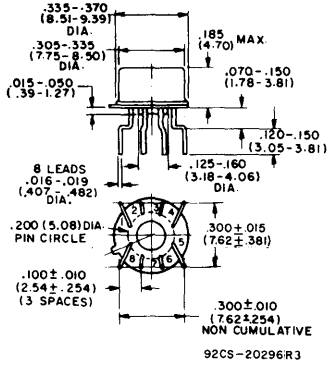
(T) Suffix (JEDEC MO-006-AG)
12-Lead TO-5 Style

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
a	0.230 TP		5.84 TP		2
A_1	0	0	0	0	
A_2	0.165	0.185	4.19	4.70	
ϕ_B	0.016	0.019	0.407	0.482	3
ϕB_1	0	0	0	0	
ϕB_2	0.016	0.021	0.407	0.533	3
ϕD	0.335	0.370	8.51	9.39	
ϕD_1	0.305	0.335	7.75	8.50	
F_1	0.020	0.040	0.51	1.01	
j	0.028	0.034	0.712	0.863	
k	0.029	0.045	0.74	1.14	4
L_1	0.000	0.050	0.00	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	30° TP		30° TP		
N	12		12		6
N_1	1		1		5

Package Outlines

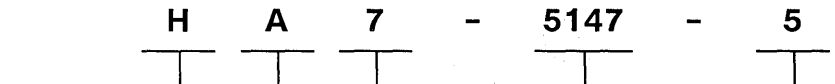
TO-5 Style Packages (Continued)

(S) Suffix
8-Lead TO-5 Style with
Dual-In-Line Formed Leads (DILCAN)



HA/HFA/HV-Type Packaging Information

HARRIS PRODUCT CODE EXAMPLE



PREFIX:
H: Harris

FAMILY:
A: Analog

PACKAGE:
1: Dual-In-Line Ceramic
2: Metal Can
3: Dual-In-Line Plastic
4P: Plastic Leaded Chip Carrier
7: Mini-DIP, Ceramic
9P: Small Outline
0: Chip Form

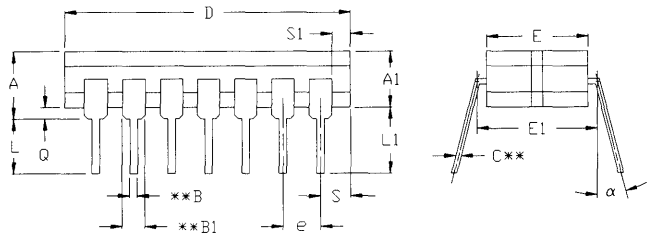
PART NUMBER

TEMPERATURE:
2: -55°C to +125°C
4: -25°C to +85°C
5: 0°C to +75°C
7: Dash-7 High Reliability Commercial Product 0°C to +75°C, includes 96 hour Burn-In
9: -40°C to +85°C

These products are available fully screened to Mil-Std-883C. Contact a Harris Sales Office for a copy of the /883 data sheet.

Package Outlines

1- .300 CERAMIC DUAL-IN-LINE

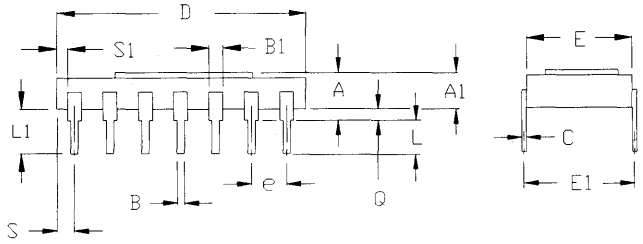


PKG CODE	LEAD COUNT	DIM A	DIM A1	DIM B	DIM B1	DIM C	DIM D	DIM E	DIM E1	DIM e	DIM L	DIM L1	DIM S	DIM S1	DIM Q	DIM α
1-	8	–	.140	.016	.050	.008	.375	.245	.290	.100	.125	.150	–	.005	.015	0°
	SSI	.200	.160	.023	.065	.015	.395	.265	.310	BSC	.150	–	.055	–	.060	15°
1-	14	–	.140	.016	.050	.008	.753	.265	.290	.100	.125	.150	–	.005	.015	0°
	MSI	.200	.170	.023	.065	.015	.785	.285	.310	BSC	.180	–	.098	–	.060	15°
1-	14	–	.140	.016	.050	.008	.753	.285	.300	.100	.125	.150	–	.005	.015	0°
	LSI	.200	.170	.023	.065	.015	.785	.305	.320	BSC	.180	–	.098	–	.060	15°
1-	16*	–	.140	.016	.050*	.008	.753	.265	.290	.100	.125	.150	–	.005	.015	0°
	MSI	.200	.170	.023	.065*	.015	.785	.285	.310	BSC	.180	–	.080	–	.060	15°
1-	16*	–	.140	.016	.050*	.008	.753	.285	.300	.100	.125	.150	–	.005	.015	0°
	LSI	.200	.170	.023	.065	.015	.785	.305	.320	BSC	.180	–	.080	–	.060	15°

*End leads are half leads where B remains the same and B1 is $\frac{0.035}{0.045}$

**Solder dip finish add +0.003 inches

1- .300 SIDEBRAZE DUAL-IN-LINE

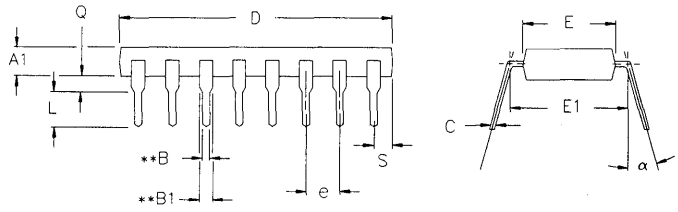


PKG CODE	LEAD COUNT	DIM A	DIM A1	DIM B	DIM B1	DIM C	DIM D	DIM E	DIM E1	DIM e	DIM L	DIM L1	DIM S	DIM S1	DIM Q
1-	8	.101	–	.016	.040	.008	.380	.280	.290	.100	.125	.150	.015	–	.005
	LSI	.150	–	.023	.060	.015	.400	.300	.310	BSC	180	–	.060	.055	–
1-	14	.101	–	.016	.040	.008	.738	.280	.290	.100	.125	.150	.015	–	.005
	LSI	.150	–	.023	.060	.015	.758	.300	.310	BSC	.180	–	.060	.098	–

**Solder dip finish add +0.003 inches

Package Outlines

3- .300 PLASTIC DUAL-IN-LINE

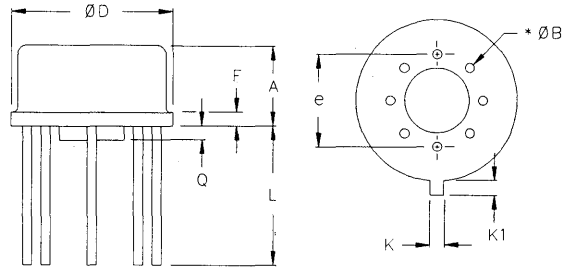


PKG CODE	LEAD COUNT	DIM A1	DIM B	DIM B1	DIM C	DIM D	DIM E	DIM E1	DIM e	DIM L	DIM S	DIM Q	DIM α
3-	8	.125 .140	.016 .023	.050 .070	.008 .015	.370 .390	.245 .265	.290 .310	.090 .110	.110 .150	.030 .050	.020 .040	0° 15°
3-	14	.125 .140	.016 .023	.050 .070	.008 .015	.750 .770	.245 .265	.290 .310	.090 .110	.110 .150	.030 .050	.020 .040	0° 15°
3-	16*	.125 .140	.016 .023	.050 .070	.008 .015	.750 .770	.245 .265	.290 .310	.090 .110	.110 .150	.025 .035	.020 .040	0° 15°

*End leads are half leads where B remains the same and B1 is $\frac{0.035}{0.045}$

**Solder dip finish add +0.003 inches

2- TO-99 METAL CAN

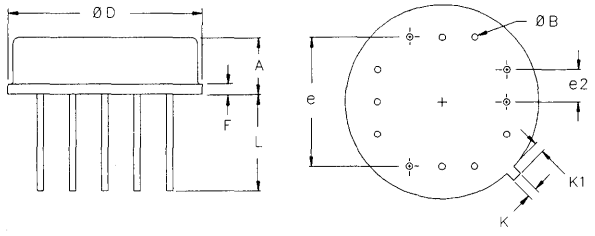


PKG CODE	LEAD COUNT	DIM A	DIM ϕB	DIM ϕD	DIM e	DIM F	DIM K	DIM K1	DIM L	DIM Q
2-	8 TO-99	.165 .185	.016 .018	.345 .365	.190 .210	.020 .040	.028 .034	.028 .040	.505 .550	.015 .040

*Solder dip finish add +0.003 inches

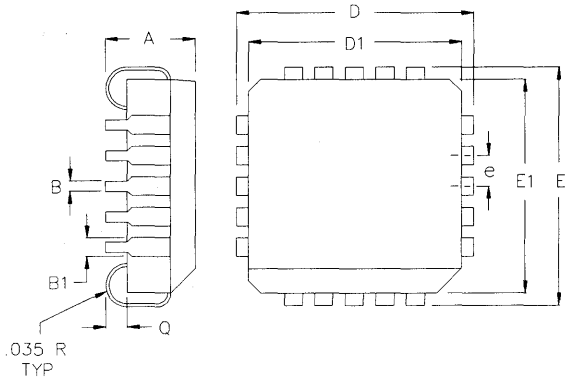
Package Outlines

2- TO-8 METAL CAN



PKG CODE	LEAD COUNT	DIM A	DIM ϕB	DIM ϕD	DIM e	DIM F	DIM K	DIM K1	DIM L	DIM Q
2-	12	.130	.016	.585	.400	.100	.020	.027	.027	.500
	TO-8	.150	.021	.615	BSC	BSC	.040	.034	.045	.550

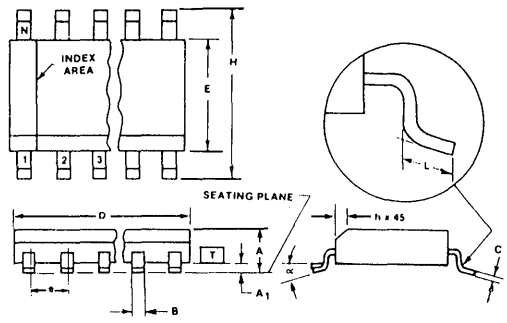
4P PLASTIC LEADED CHIP CARRIER



PKG CODE	LEAD COUNT	DIM A	DIM B	DIM B1	DIM D/E	DIM D1/E1	DIM e	DIM Q
4P	20	.165	.013	.026	.385	.350	.050	.020
		.180	.021	.032	.395	.356	BSC	–

Package Outlines

9P Small-Outline (SO) Packages



NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "T" is a reference datum.
4. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

JEDEC MS-012AA
8-Lead Dual-In-Line
Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.1890	0.1968	4.80	5.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9 92CS-39432

JEDEC MS-012AB
14-Lead Dual-In-Line
Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.3367	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9 92CS-38924R1

JEDEC MS-012AC
16-Lead Dual-In-Line, Narrow Body
Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9 92CS-38925R1

JEDEC MS-013AA
16-Lead Dual-In-Line, Wide Body
Surface-Mount Plastic Package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0926	0.1043	2.35	2.65	
A_1	0.0040	0.0118	0.10	0.30	
B	0.0138	0.0192	0.35	0.49	
C	0.0091	0.0125	0.23	0.32	
D	0.3977	0.4133	10.10	10.50	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		
H	0.394	0.419	10.00	10.65	
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9 92CS-39433

ICL/ICM-Type Packaging Information

Ordering Information

Device Family Prefixes

PREFIX	DEVICE FAMILY
ICL	Linear IC
ICM	Microperipheral IC
LM	National Semiconductor Alternate Source

Temperature Range Designators

SUFFIX	TEMPERATURE RANGE
C	Commercial: 0°C to +70°C
I	Industrial: Either -25°C to +85°C or -40°C to +85°C (Specified on Datasheet)
M	Military: -55°C to +125°C

Package Type Designators

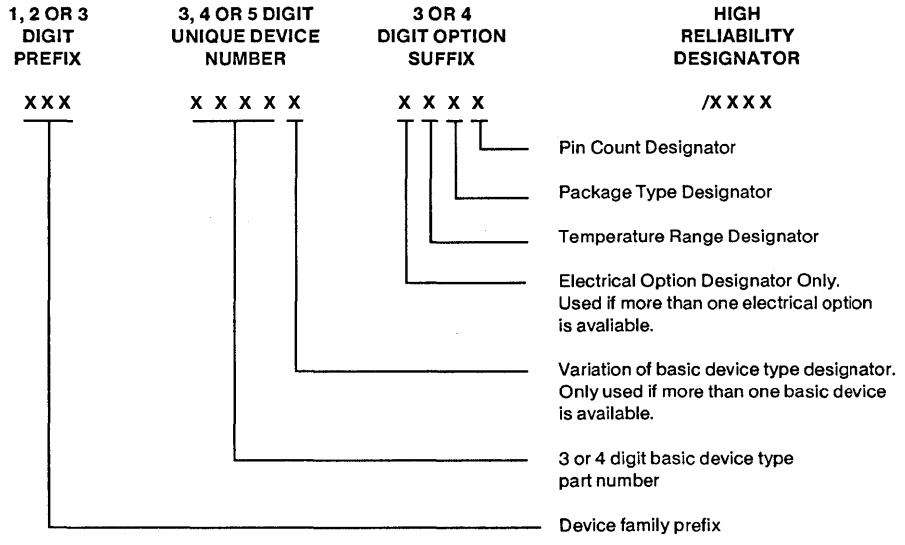
SUFFIX	PACKAGE
B	Small Outline IC (SOIC)
J	Ceramic Dual-In-Line
P	Plastic Dual-In-Line
T	TO-99, TO-100

Pin Count Designator

SUFFIX	PIN COUNT	DIAMETER
A	8	
B	10	
C	12	
D	14	
E	16	
V	8	(0.200" pin circle, isolated case)
W	10	(0.230" pin circle, isolated case)
X	10	(0.230" pin circle, case to pin 5)
Y	8	(0.200" pin circle, case to pin 4)
Z	8	(0.230" pin circle, case to pin 5)

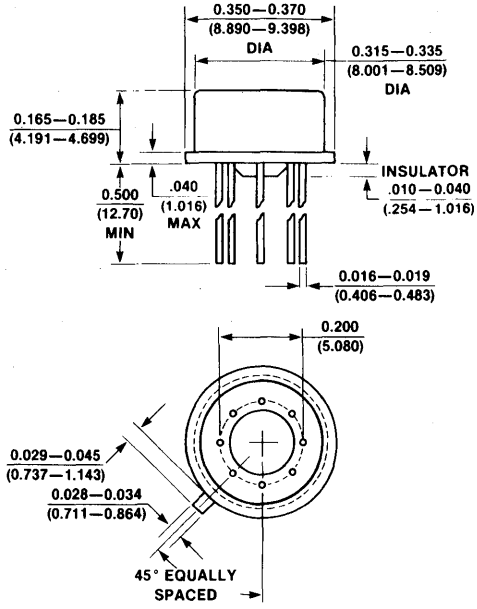
Part Numbering System

All Intersil Part Numbers consist of a Device Family Prefix, a Basic Numeric Part Number, and an Option Suffix, as follows:

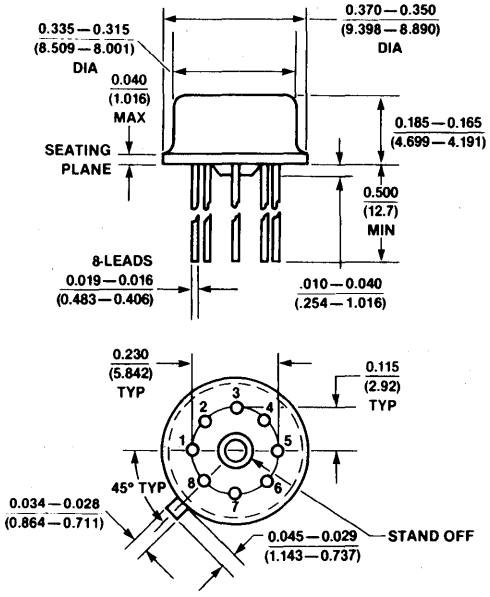


Package Outlines

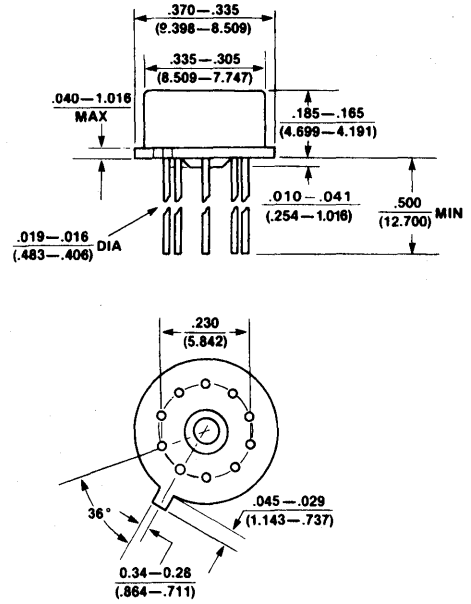
TV TY 8 LEAD TO-99 METAL CAN



TZ 8 LEAD 0.230 PCD TO-99 METAL CAN



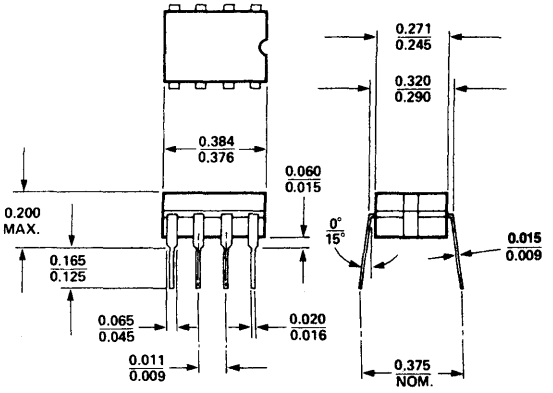
TW TX 10 LEAD TO-100 METAL CAN



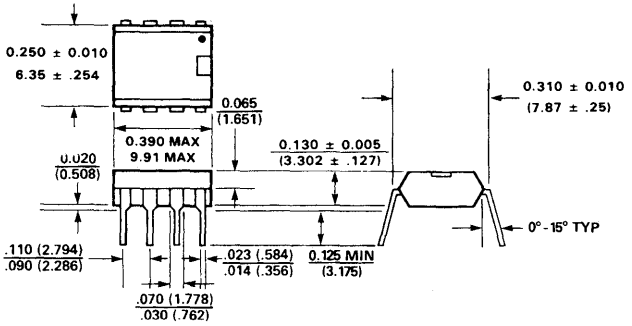
All dimensions given in inches (millimeters)

Package Outlines

JA 8 LEAD CERAMIC DUAL-IN-LINE



PA 8 LEAD PLASTIC DUAL-IN-LINE

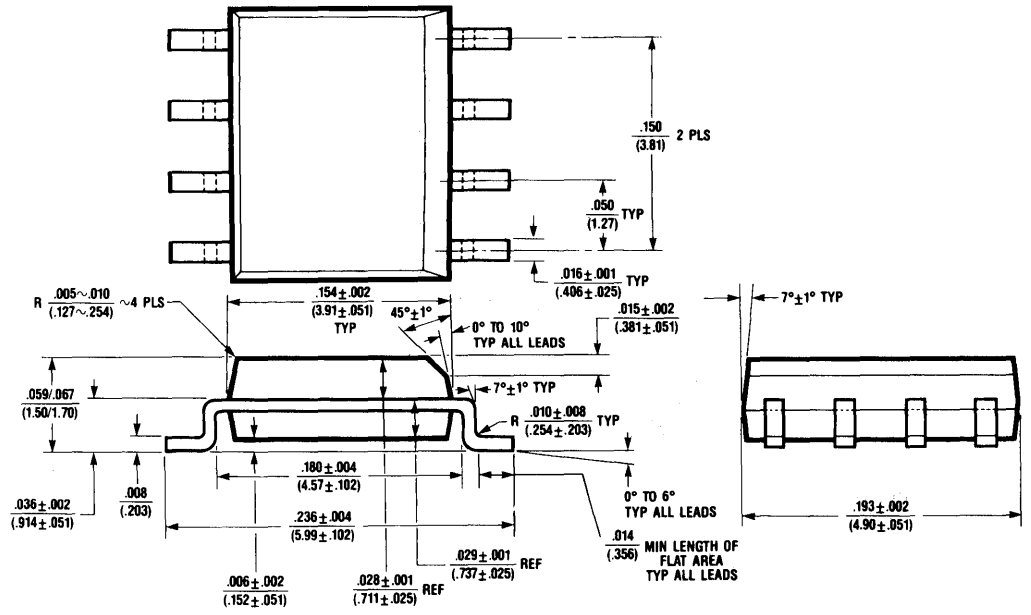


11 PACKAGING

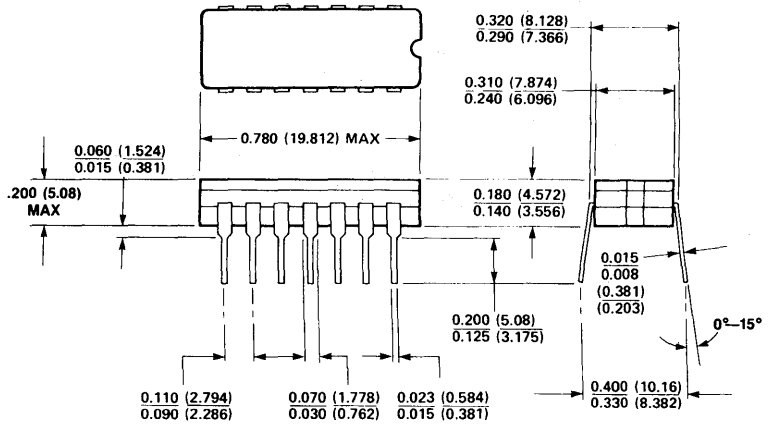
All dimensions given in inches / (millimeters)

Package Outlines

BA 8 LEAD SOIC



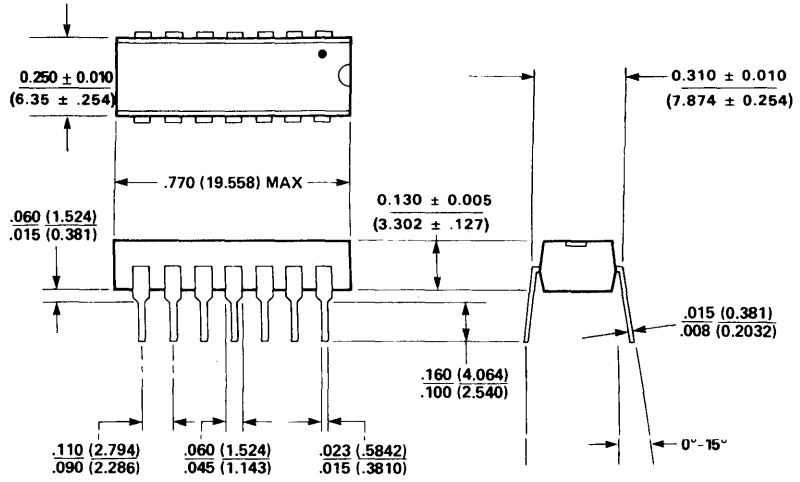
JD 14 LEAD CERAMIC DUAL-IN-LINE



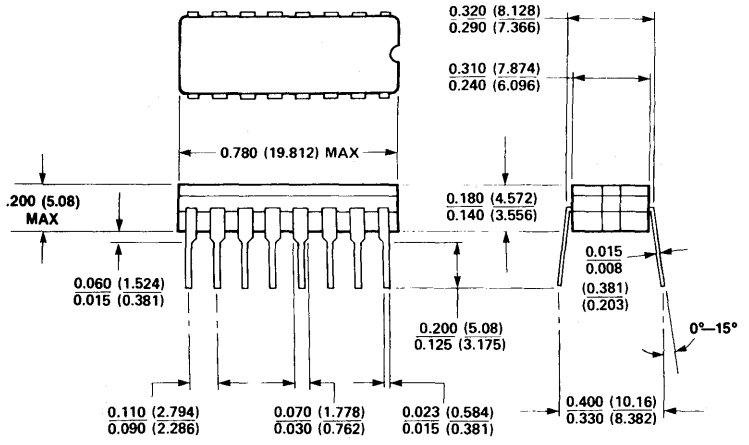
All dimensions given in inches (millimeters)

Package Outlines

PD 14 LEAD PLASTIC DUAL-IN-LINE



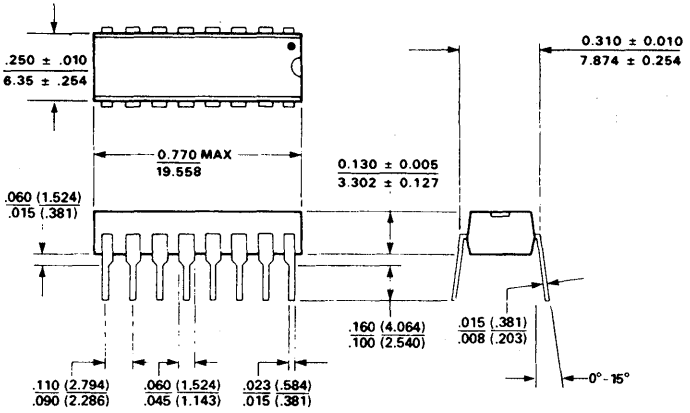
JE 16 LEAD CERAMIC DUAL-IN-LINE



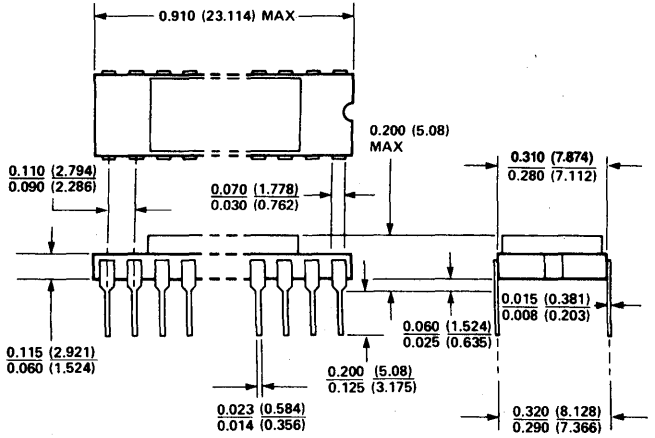
All dimensions given in inches (millimeters)

Package Outlines

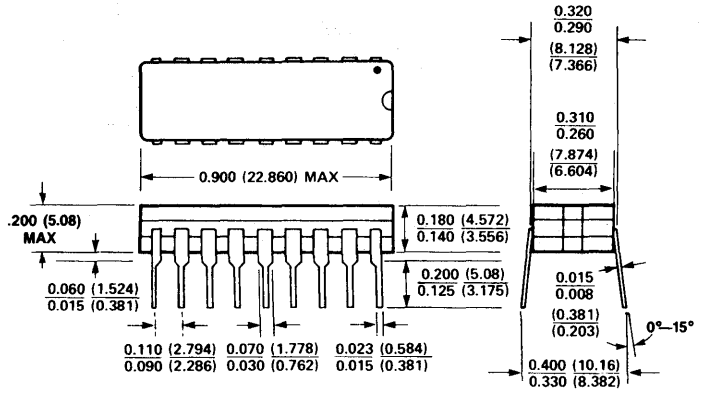
PE 16 LEAD PLASTIC DUAL-IN-LINE



DN 18 LEAD CERAMIC DUAL-IN-LINE



JN 18 LEAD CERAMIC DUAL-IN-LINE



All dimensions given in inches (millimeters)

LINEAR 12

SALES OFFICE INFORMATION

A complete and current listing of all Harris Sales, Representative and Distributor locations worldwide is available. Please order the "Harris Sales Listing" from the Literature Center (see page i).

HARRIS COUNTRY HEADQUARTERS LOCATIONS:

U.S. HEADQUARTERS
Harris Semiconductor
1301 Woody Burke Road
Melbourne, Florida 32902
TEL: (407) 724-3000

EUROPEAN HEADQUARTERS
Harris Semiconductor
Mercure Centre
Rue de la Fusse 100
Brussels, Belgium 1130
TEL: (32) 2-246-2111

SOUTH ASIA
Harris Semiconductor H.K. Ltd
13/F Fourseas Building
208-212 Nathan Road
Tsimshatsui, Kowloon
Hong Kong
TEL: (852) 3-723-6339

NORTH ASIA
Harris K.K.
Shinjuku NS Bldg. Box 6153
2-4-1 Nishi-Shinjuku
Shinjuku-Ku, Tokyo 163 Japan
TEL: 81-3-345-8911

HARRIS TECHNICAL ASSISTANCE AVAILABILITY:

UNITED STATES

CALIFORNIA	Costa Mesa ..... 714-433-0600 San Jose ..... 408-922-0977 Woodland Hills 818-992-0686
FLORIDA	Melbourne 407-724-3576
GEORGIA	Norcross 404-246-4660
ILLINOIS	Itasca 708-250-0070
MASSACHUSETTS	Burlington 617-221-1850
NEW JERSEY	Mt. Laurel ..... 609-727-1909 Rahway 201-381-4210
TEXAS	Dallas 214-733-0800

INTERNATIONAL

FRANCE	Paris 33-1-346-54046
GERMANY	Munich 49-8-963-8130
ITALY	Milano 39-2-262-22141
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