1996 POWER MOSFET DATABOOK SUPPLEMENT HARRIS DB 316

NEW PRODUCT AND UPDATED PRODUCT DATASHEETS

POWER MOSFET DATABOOK SUPPLEMENT

JANUARY 1996

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HARRIS POWER MOSFET PRODUCTS

Harris Semiconductor is a pioneer in the development and production of discrete power products for the most demanding applications in this world and beyond. This databook fully describes Harris Semiconductor's recently introduced Power MOSFETs and updates to other device types.

Included are complete datasheets with product descriptions, product selection charts, quality and reliability information, and packaging and ordering information. Harris' AnswerFax system is detailed in Section 10 showing how users may request the latest datasheets and have them delivered immediately via their own fax machine.

This databook contains the datasheets of recently introduced products and also updates some of the datasheets in the POWER MOSFET DATABOOK DB223B. These datasheets contain the detailed specification for these products. In addition to the datasheets, Section 1 lists page numbers for this databook and for DB223B. Section 2 provides selection charts for all the Power MOSFETs Harris manufactures. Section 3 through 7 contain the datasheets, each section representing a major product category. Section 7 highlights the new small outline products introduced in the SOP-8 package. Packaging information detailing the dimensions of the packages is provided in Section 9. Tape and Reel information is also provided in Section 9.

Datasheet sections provide definitive ratings and characteristics for each major category of devices. Datasheets for individual devices are organized in numeric/alphanumeric sequence in each section. Because some devices are grouped to show similarity of functions or data, some individual types numbers may be out of sequence. The complete list of Harris Power MOSFETs are located in Section 1, General Information Alphanumeric Index, Section 1.

HARRIS
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POWER MOSFETs

FOR COMMERCIAL AND HIGH RELIABILITY APPLICATIONS

POWER MOSFETs 1

GENERAL INFORMATION

Alpha Numeric Product Index

Alpha Numeric Product Index (Continued)

Alpha Numeric Product Index (Continued)

Alpha Numeric Product Index (Continued)

		DB223B PAGE	DB316 PAGE
IRFF113	3.0A, 80V, 0.800Ω, N-Channel Power MOSFET	4-423	-
IRFF113R	3.0A, 80V, 0.800Ω, Avalanche Rated, N-Channel Power MOSFET	4-423	-
IRFF120	6.0A, 100V, 0.300Ω, N-Channel Power MOSFET	4-428	-
IRFF120R	6.0A, 100V, 0.300Ω, Avalanche Rated, N-Channel Power MOSFET	4-428	-
IRFF121	6.0A, 80V, 0.300Ω, N-Channel Power MOSFET	4-428	-
IRFF121R	6.0A, 80V, 0.300Ω, Avalanche Rated, N-Channel Power MOSFET	4-428	-
IRFF122	5.0A, 100V, 0.400Ω, N-Channel Power MOSFET	4-428	-
IRFF122R	5.0A, 100V, 0.400Ω, Avalanche Rated, N-Channel Power MOSFET	4-428	-
IRFF123	5.0A, 80V, 0.400Ω, N-Channel Power MOSFET	4-428	-
IRFF123R	5.0A, 80V, 0.400Ω, Avalanche Rated, N-Channel Power MOSFET	4-428	-
IRFF130	8.0A, 100V, 0.180Ω, N-Channel Power MOSFET	4-433	-
IRFF130R	8.0A, 100V, 0.180Ω, Avalanche Rated, N-Channel Power MOSFET	4-433	-
IRFF131	8.0A, 80V, 0.180Ω, N-Channel Power MOSFET	4-433	-
IRFF131R	8.0A, 80V, 0.180Ω, Avalanche Rated, N-Channel Power MOSFET	4-433	-
IRFF132	7.0A, 100V, 0.250Ω, N-Channel Power MOSFET	4-433	-
IRFF132R	7.0A, 100V, 0.250Ω, Avalanche Rated, N-Channel Power MOSFET	4-433	-
IRFF133	7.0A, 80V, 0.250Ω, N-Channel Power MOSFET	4-433	-
IRFF133R	7.0A, 80V, 0.250Ω, Avalanche Rated, N-Channel Power MOSFET	4-433	-
IRFF210	2.2A, 200V, 1.500Ω, N-Channel Power MOSFET	4-438	-
IRFF210R	2.2A, 200V, 1.500Ω, Avalanche Rated, N-Channel Power MOSFET	4-438	-
IRFF211	2.2A, 150V, 1.500Ω, N-Channel Power MOSFET	4-438	-
IRFF211R	2.2A, 150V, 1.500Ω, Avalanche Rated, N-Channel Power MOSFET	4-438	-
IRFF212	1.8A, 200V, 2.400Ω, N-Channel Power MOSFET	4-438	-
IRFF212R	1.8A, 200V, 2.400Ω, Avalanche Rated, N-Channel Power MOSFET	4-438	-
IRFF213	1.8A, 150V, 2.400Ω, N-Channel Power MOSFET	4-438	-
IRFF213R	1.8A, 150V, 2.400Ω, Avalanche Rated, N-Channel Power MOSFET	4-438	-
IRFF220	3.5A, 200V, 0.800Ω, N-Channel Power MOSFET	4-443	-
IRFF220R	3.5A, 200V, 0.800Ω, Avalanche Rated, N-Channel Power MOSFET	4-443	-
IRFF221	3.5A, 150V, 0.800Ω, N-Channel Power MOSFET	4-443	-
IRFF221R	3.5A, 150V, 0.800Ω, Avalanche Rated, N-Channel Power MOSFET	4-443	-
IRFF222	3.0A, 200V, 1.200Ω, N-Channel Power MOSFET	4-443	-
IRFF222R	3.0A, 200V, 1.200Ω, Avalanche Rated, N-Channel Power MOSFET	4-443	-
IRFF223	3.0A, 150V, 1.200Ω, N-Channel Power MOSFET	4-443	-
IRFF223R	3.0A, 150V, 1.200Ω, Avalanche Rated, N-Channel Power MOSFET	4-443	-
IRFF230	5.5A, 200V, 0.400Ω, N-Channel Power MOSFET	4-448	-
IRFF230R	5.5A, 200V, 0.400Ω, Avalanche Rated, N-Channel Power MOSFET	4-448	-
IRFF231	5.5A, 150V, 0.400Ω, N-Channel Power MOSFET	4-448	-

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Alpha Numeric Product Index (Continued)

		DB223B PAGE	DB316 PAGE
RFG40N10	40.0A, 100V, 0.040Ω, Avalanche Rated, N-Channel Power MOSFET	4-731	-
RFG40N10LE	40.0A, 100V, 0.040Ω, Avalanche Rated, Logic Level, ESD Protected, N-Channel Power MOSFET	-	5-51
RFG45N06	45.0A, 60V, 0.028Ω, Avalanche Rated, N-Channel Power MOSFET	-	3-33
RFG50N05	50.0A, 50V, 0.022Ω, Avalanche Rated, N-Channel Power MOSFET	4-750	-
RFG50N05L	50.0A, 50V, 0.022Ω, Avalanche Rated, Logic Level, N-Channel Power MOSFET	6-119	-
RFG50N06	50.0A, 60V, 0.022Ω, Avalanche Rated, N-Channel Power MOSFET	-	3-39
RFG60P03	60.0A, 30V, 0.027Ω, Avalanche Rated, P-Channel Power MOSFET	-	4-51
RFG60P05E	30.0A, 50V, 0.030Ω, Avalanche Rated, P-Channel Power MOSFET	-	4-57
RFG60P06E	30.0A, 60V, 0.030Ω, Avalanche Rated, P-Channel Power MOSFET	-	4-63
RFG70N06	70.0A, 60V, 0.014Ω, Avalanche Rated, N-Channel Power MOSFET	-	3-51
RFG75N05E	75.0A, 50V, 0.008Ω, Avalanche Rated, N-Channel Power MOSFET	4-773	-
RFH10N45	10.0A, 450V, 0.600Ω, N-Channel Power MOSFET	4-645	-
RFH10N50	10.0A, 500V, 0.600Ω, N-Channel Power MOSFET	4-645	-
RFH12N35	12.0A, 350V, 0.380Ω, N-Channel Power MOSFET	4-666	-
RFH12N40	12.0A, 400V, 0.380Ω, N-Channel Power MOSFET	4-666	-
RFH25N18	25.0A, 180V, 0.150Ω, N-Channel Power MOSFET	4-707	-
RFH25N20	25.0A, 200V, 0.150Ω, N-Channel Power MOSFET	4-707	-
RFH25P08	25.0A, 80V, 0.150Ω, P-Channel Power MOSFET	5-183	-
RFH25P10	25.0A, 100V, 0.150Ω, P-Channel Power MOSFET	5-183	-
RFH30N12	30.0A, 120V, 0.075Ω, N-Channel Power MOSFET	4-715	-
RFH30N15	30.0A, 150V, 0.075Ω, N-Channel Power MOSFET	4-715	-
RFH35N08	35.0A, 80V, 0.055Ω, N-Channel Power MOSFET	4-723	-
RFH35N10	35.0A, 100V, 0.055Ω, N-Channel Power MOSFET	4-723	-
RFH45N05	45.0A, 50V, 0.040Ω, N-Channel Power MOSFET	4-742	-
RFH45N06	45.0A, 60V, 0.040Ω, N-Channel Power MOSFET	4-742	-
RFH75N05E	75.0A, 50V, 0.008Ω, Avalanche Rated, N-Channel Power MOSFET	4-773	-
RFK25N18	25.0A, 180V, 0.150Ω, N-Channel Power MOSFET	4-711	-
RFK25N20	25.0A, 200V, 0.150Ω, N-Channel Power MOSFET	4-711	-
RFK25P08	25.0A, 80V, 0.150Ω, P-Channel Power MOSFET	5-183	-
RFK25P10	25.0A, 100V, 0.150Ω, P-Channel Power MOSFET	5-183	-
RFK30N12	30.0A, 120V, 0.075Ω, N-Channel Power MOSFET	4-719	-
RFK30N15	30.0A, 150V, 0.075Ω, N-Channel Power MOSFET	4-719	-
RFK35N08	35.0A, 80V, 0.055Ω, N-Channel Power MOSFET	4-727	-
RFK35N10	35.0A, 100V, 0.055Ω, N-Channel Power MOSFET	4-727	-
RFK45N05	45.0A, 50V, 0.040Ω, N-Channel Power MOSFET	4-746	-
RFK45N06	45.0A, 60V, 0.040Ω, N-Channel Power MOSFET	4-746	-

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Alpha Numeric Product Index (Continued)

Product Index by Family

Product Index by Family (Continued)

N-CHANNEL POWER MOSFET DATA SHEETS

Product Index by Family (Continued)

Product Index by Family (Continued)

Product Index by Family (Continued)

Product Index by Family (Continued)

1 GENERAL INFORMATION

Product Index by Family (Continued)

Product Index by Family (Continued)

Product Index by Family (Continued)

Product Index by Family (Continued)

Product Index by Family (Continued)

P-CHANNEL POWER MOSFET DATA SHEETS

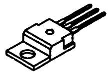
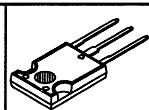
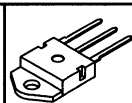
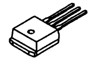
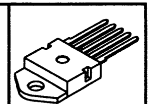
Product Index by Family (Continued)

SMALL OUTLINE PRODUCTS

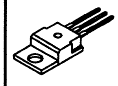
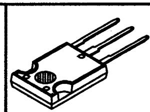
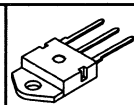
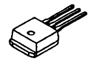
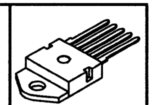
POWER MOSFETs 2

POWER MOSFET PRODUCT SELECTION GUIDE

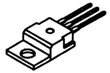
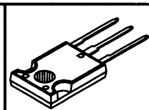
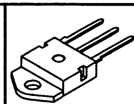
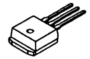
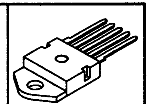
N-CHANNEL MOSFETs

MAXIMUM RATINGS			 TO-251AA	 TO-252AA	 TO-220AB	 TO-247	 4 PIN DIP	 TO-218AC	 TO-262AA	 TO-263AB	 MS-012AA	 MO-093
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)										
30	3.5	2 x 0.06									RF1K49086	
30	6.3	0.03									RF1K49157	
30	70	0.010			RFP70N03				RF1S70N03	RF1S70N03SM		
50	4.0	0.800			RFP4N05							
50	13	0.120			BUZ71A							
50	14	0.100			BUZ71							
50	14	0.100	RFD14N05	RFD14N05SM	RFP14N05							
50	15	0.140			RFP15N05							
50	16	0.047	RFD16N05	RFD16N05SM								
50	25	0.047			RFP25N05							
50	30	0.040			BUZ11							
50	50	0.022			RFP50N05	RFG50N05						
50	75	0.008				RFG75N05E		RFH75N05E				
50	100	0.008										RFA100N05E
60	0.10	3.200					IRFD1Z3					
60	0.50	2.400					IRFD1Z1					
60	4.0	0.800			RFP4N06							
60	12	0.150	RFD3055	RFD3055SM	RFP3055							
60	14	0.100	RFD14N06	RFD14N06SM	RFP14N06							
60	15	0.140			RFP15N06							
60	16	0.047	RFD16N06	RFD16N06SM								
60	25	0.047			RFP25N06				RF1S25N06	RF1S25N06SM		
60	34	0.080				IRFP153						
60	40	0.055				IRFP151						
60	45	0.028			RFP45N06	RFG45N06			RF1S45N06	RF1S45N06SM		
60	50	0.022			RFP50N06	RFG50N06			RF1S50N06	RF1S50N06SM		
60	70	0.014			RFP70N06	RFG70N06			RF1S70N06	RF1S70N06SM		

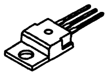
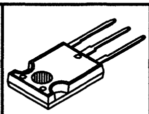
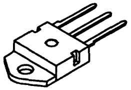
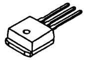
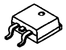
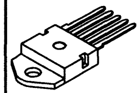
N-CHANNEL MOSFETs (Continued)

MAXIMUM RATINGS												
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	TO-251AA	TO-252AA	TO-220AB	TO-247	4 PIN DIP	TO-218AC	TO-262AA	TO-263AB	MS-012AA	MO-093
80	0.80	0.800					IRFD113					
80	1.0	0.600					IRFD111					
80	1.0	0.400					IRFD123					
80	1.3	0.300					IRFD121					
80	2.0	1.050			RFP2N08							
80	4.9	0.740			IRF513							
80	5.6	0.540			IRF511							
80	8.0	0.360			IRF523							
80	8.4	0.270	IRFU121	IRFR121								
80	9.2	0.270			IRF521							
80	12	0.200			RFP12N08							
80	12	0.230			IRF533							
80	14	0.160			IRF531							
80	18	0.100			RFP18N08							
80	25	0.100			IRF543							
80	27	0.099				IRFP143						
80	28	0.077			IRF541							
80	31	0.077				IRFP141						
100	0.40	3.200					IRFD1Z2					
100	0.50	2.400					IRFD1Z0					
100	0.80	0.800					IRFD112					
100	1.0	0.600					IRFD110					
100	1.1	0.400					IRFD122					
100	1.3	0.300					IRFD120					
100	2.0	1.050			RFP2N10							
100	4.7	0.540	IRFU110	IRFR110								
100	4.9	0.740			IRF512							

N-CHANNEL MOSFETs (Continued)

MAXIMUM RATINGS												
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	TO-251AA	TO-252AA	TO-220AB	TO-247	4 PIN DIP	TO-218AC	TO-262AA	TO-263AB	MS-012AA	MO-093
100	5.6	0.540			IRF510							
100	8.0	0.360			IRF522							
100	8.4	0.270	IRFU120	IRFR120								
100	9.0	0.250			BUZ72A							
100	9.2	0.270			IRF520							
100	12	0.230			IRF532							
100	12	0.200			RFP12N10							
100	12	0.200			BUZ20							
100	14	0.160			IRF530							
100	18	0.100			RFP18N10							
100	19	0.100			BUZ21							
100	22	0.080			RFP22N10							
100	25	0.100			IRF542							
100	27	0.099				IRFP142						
100	28	0.077			IRF540							
100	31	0.077				IRFP140						
100	34	0.080				IRFP152						
100	40	0.040			RFP40N10	RFG40N10						
100	40	0.055				IRFP150						
120	2.0	1.750			RFP2N12							
120	10	0.300			RFP10N12							
120	15	0.150			RFP15N12							
150	0.45	2.400					IRFD213					
150	0.60	1.500					IRFD211					
150	0.70	1.200					IRFD223					
150	0.80	0.800					IRFD221					
150	2.0	1.750			RFP2N15							

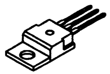
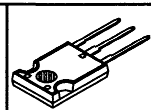
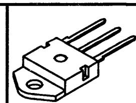
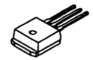
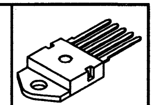
N-CHANNEL MOSFETs (Continued)

MAXIMUM RATINGS												
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	TO-251AA	TO-252AA	TO-220AB	TO-247	4 PIN DIP	TO-218AC	TO-262AA	TO-263AB	MS-012AA	MO-093
150	2.6	2.400			IRF613							
150	3.3	1.500			IRF611							
150	4.0	1.200			IRF623							
150	4.6	0.800	IRFU221	IRFR221								
150	5.0	0.800			IRF621							
150	8.0	0.600			IRF633							
150	9.0	0.400			IRF631							
150	10	0.300			RFP10N15							
150	15	0.150			RFP15N15							
150	16	0.220			IRF643							
150	18	0.180			IRF641							
150	18	0.220				IRFP243						
150	20	0.180				IRFP241						
150	27	0.120				IRFP253						
150	33	0.085				IRFP251						
180	3.0	3.500			RFP2N18							
180	12	0.250			RFP12N18							
180	25	0.150						RFH25N18				
200	0.45	2.400					IRFD212					
200	0.60	1.500					IRFD210					
200	0.70	1.200					IRFD222					
200	0.80	0.800					IRFD220					
200	2.0	3.500			RFP2N20							
200	2.6	2.400			IRF612							
200	3.3	1.500			IRF610							
200	3.8	1.200	IRFU222	IRFR222								
200	4.0	1.200			IRF622							

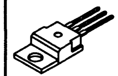
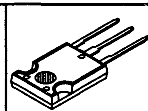
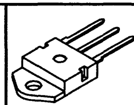
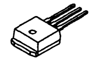
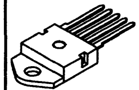
N-CHANNEL MOSFETs (Continued)

MAXIMUM RATINGS													
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	TO-251AA	TO-252AA	TO-220AB	TO-247	4 PIN DIP	TO-218AC	TO-262AA	TO-263AB	MS-012AA	MO-093
200	4.6	0.800	IRFU220	IRFR220								
200	5.0	0.800			IRF620							
200	5.8	0.600			BUZ73A							
200	8.0	0.600			IRF632							
200	9.0	0.400			IRF630							
200	9.5	0.400			BUZ32							
200	12	0.250			RFP12N20							
200	16	0.220			IRF642							
200	18	0.180			IRF640							
200	18	0.220				IRFP242						
200	20	0.180				IRFP240						
200	25	0.150						RFH25N20				
200	27	0.120				IRFP252						
200	33	0.085				IRFP250						
250	2.0	2.000			IRF614							
250	2.2	2.000	IRFU214	IRFR214								
250	13	0.340			IRF645							
250	14	0.280			IRF644							
250	14	0.340				IRFP245						
250	15	0.280				IRFP244						
275	13	0.340			IRF647							
275	14	0.340				IRFP247						
275	14	0.280			IRF646							
275	15	0.280				IRFP246						
350	0.30	5.000					IRFD313					
350	0.40	2.500					IRFD323					
350	0.40	3.600					IRFD311					

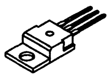
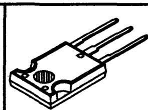
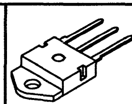
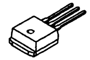
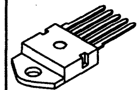
N-CHANNEL MOSFETs (Continued)

MAXIMUM RATINGS												
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	TO-251AA	TO-252AA	TO-220AB	TO-247	4 PIN DIP	TO-218AC	TO-262AA	TO-263AB	MS-012AA	MO-093
350	0.50	1.800					IRFD321					
350	1.7	5.000			IRF713							
350	2.0	3.600			IRF711							
350	2.8	2.500			IRF723							
350	3.1	1.800	IRFU321	IRFR321								
350	3.3	1.800			IRF721							
350	4.0	2.000			RFP4N35							
350	4.5	1.500			IRF733							
350	5.5	1.000			IRF731							
350	7.0	0.750			RFP7N35							
350	8.0	0.800			IRF743							
350	8.7	0.800				IRFP343						
350	10	0.550			IRF741							
350	11	0.550				IRFP341						
350	12	0.380						RFH12N35				
350	14	0.400				IRFP353						
350	16	0.300				IRFP351						
400	0.30	5.000					IRFD312					
400	0.40	2.500					IRFD322					
400	0.40	3.600					IRFD310					
400	0.50	1.800					IRFD320					
400	1.7	5.000			IRF712							
400	2.0	3.600			IRF710							
400	2.6	2.500	IRFU322	IRFR322	BUZ76A							
400	2.8	2.500			IRF722							
400	3.0	1.800			BUZ76							
400	3.1	1.800	IRFU320	IRFR320								

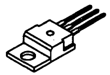
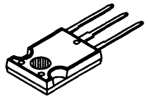
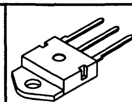
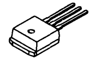
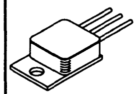
N-CHANNEL MOSFETs (Continued)

MAXIMUM RATINGS												
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	TO-251AA	TO-252AA	TO-220AB	TO-247	4 PIN DIP	TO-218AC	TO-262AA	TO-263AB	MS-012AA	MO-093
400	3.3	1.800			IRF720							
400	4.0	2.000			RFP4N40							
400	4.5	1.500			IRF732							
400	4.5	1.500			BUZ60B							
400	5.5	1.000			IRF730							
400	5.5	1.000			BUZ60							
400	7.0	0.750			RFP7N40							
400	8.0	0.800			IRF742							
400	8.7	0.800				IRFP342						
400	10	0.550			IRF740							
400	11	0.550				IRFP340						
400	11.5	0.400						BUZ351				
400	12	0.380						RFH12N40				
400	14	0.400				IRFP352						
400	16	0.300				IRFP350						
450	2.0	4.000			IRF823							
450	2.5	3.000	IRFU421	IRFR421	IRF821							
450	3.0	3.000			RFP3N45							
450	4.0	2.000			IRF833							
450	4.5	1.500			IRF831							
450	6.0	1.250			RFP6N45							
450	7.0	1.100			IRF843							
450	7.7	1.100				IRFP443						
450	8.0	0.850			IRF841							
450	8.8	0.850				IRFP441						
450	10	0.600						RFH10N45				
450	12	0.500				IRFP453						

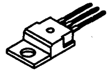
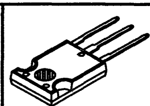
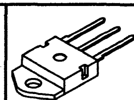
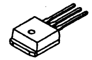
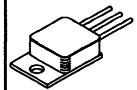
N-CHANNEL MOSFETs (Continued)

MAXIMUM RATINGS												
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	TO-251AA	TO-252AA	TO-220AB	TO-247	4 PIN DIP	TO-218AC	TO-262AA	TO-263AB	MS-012AA	MO-093
450	14	0.400				IRFP451						
500	1.5	7.000	IRFU410	IRFR410								
500	2.0	4.000			IRF822							
500	2.2	4.000	IRFU422	IRFR422								
500	2.5	3.000	IRFU420	IRFR420	IRF820							
500	3.0	3.000			RFP3N50							
500	4.0	2.000			BUZ42							
500	4.0	2.000			IRF832							
500	4.5	1.500			IRF830							
500	4.5	1.500			BUZ41A							
500	6.0	1.250			RFP6N50							
500	7.0	1.100			IRF842							
500	7.7	1.100				IRFP442						
500	8.0	0.850			IRF840							
500	8.8	0.850				IRFP440						
500	10	0.600						RFH10N50				
500	12	0.500				IRFP452						
500	14	0.400				IRFP450						
600	5.4	1.600			IRFBC42							
600	5.9	1.600				IRFPC42						
600	6.2	1.200			IRFBC40							
600	6.8	1.200				IRFPC40						
1000	3.9	4.200				IRFPG42						
1000	4.3	3.500			RFP4N100	IRFPG40						

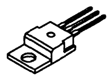
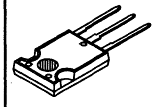
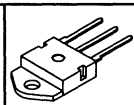
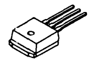
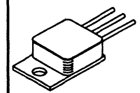
P-CHANNEL MOSFETs

MAXIMUM RATINGS			 TO-251AA	 TO-252AA	 TO-220AB	 TO-247	 4 PIN DIP	 TO-218AC	 TO-262AA	 TO-263AB	 TO-254AA
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)									
30	60	0.027			RFP60P03	RFG60P03			RF1S60P03	RF1S60P03SM	
50	8.0	0.300	RFD8P05	RFD8P05SM	RFP8P05						
50	15	0.150	RFD15P05	RFD15P05SM	RFP15P05						
50	30	0.065			RFP30P05	RFG30P05			RF1S30P05	RF1S30P05SM	
50	60	0.030				RFG60P05E					
60	0.60	1.600					IRFD9113				
60	0.80	0.800					IRFD9123				
60	2.5	1.600			IRF9513						
60	3.0	1.200			IRF9511						
60	5.0	0.800			IRF9523						
60	6.0	0.600			IRF9521						
60	8.0	0.300	RFD8P06E	RFD8P06ESM	RFP8P06E						
60	10	0.400			IRF9533						
60	12	0.300			IRF9531						
60	15	0.300			IRF9543						
60	15	0.150	RFD15P06	RFD15P06SM	RFP15P06						
60	16	0.300				IRFP9143					
60	19	0.200			IRF9541	IRFP9141					
60	25	0.150				IRFP9151					RFF60P06
60	30	0.065			RFP30P06	RFG30P06			RF1S30P06	RF1S30P06SM	
60	60	0.030				RFG60P06E					
80	2.0	3.500			RFP2P08						

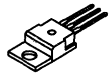
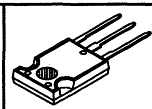
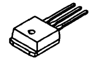
P-CHANNEL MOSFETs (Continued)

MAXIMUM RATINGS											
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	 TO-251AA	 TO-252AA	 TO-220AB	 TO-247	 4 PIN DIP	 TO-218AC	 TO-262AA	 TO-263AB	 TO-254AA
80	6.0	0.600			RFP6P08						
80	8.0	0.400			RFP8P08						
80	12	0.300			RFP12P08						
80	25	0.150						RFH25P08			
100	0.70	1.200					IRFD9110				
100	1.0	0.600					IRFD9120				
100	2.0	3.500			RFP2P10						
100	2.5	1.600			IRF9512						
100	3.0	1.200			IRF9510						
100	3.1	1.200	IRFU9110	IRFR9110							
100	5.0	0.800			IRF9522						
100	5.6	0.600	IRFU9120	IRFR9120							
100	6.0	0.600			RFP6P10						
100	6.0	0.600			IRF9520						
100	8.0	0.400			RFP8P10						
100	10	0.400			IRF9532						
100	12	0.300			IRF9530						
100	12	0.300			RFP12P10						
100	15	0.300			IRF9542						
100	16	0.300				IRFP9142					
100	19	0.200			IRF9540	IRFP9140					
100	25	0.150				IRFP9150		RFH25P10			
120	10	0.500			RFP10P12						

P-CHANNEL MOSFETs (Continued)

MAXIMUM RATINGS											
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	TO-251AA	TO-252AA	TO-220AB	TO-247	4 PIN DIP	TO-218AC	TO-262AA	TO-263AB	TO-254AA
150	0.45	2.400					IRFD9223				
150	3.0	2.400			IRF9623						
150	3.5	1.500			IRF9621						
150	5.5	1.200			IRF9633						
150	6.5	0.800			IRF9631						
150	9.0	0.700			IRF9643						
150	10	0.500			RFP10P15						
150	10	0.700				IRFP9243					
150	11	0.500			IRF9641						
150	12	0.500				IRFP9241					
200	0.60	1.500					IRFD9220				
200	3.0	2.400			IRF9622						
200	3.5	1.500			IRF9620						
200	3.6	1.500	IRFU9220	IRFR9220							
200	5.5	1.200			IRF9632						
200	6.5	0.800			IRF9630						
200	9.0	0.700			IRF9642						
200	10	0.700				IRFP9242					
200	11	0.500			IRF9640						
200	12	0.500				IRFP9240					

N-CHANNEL LOGIC LEVEL DEVICES

MAXIMUM RATINGS										
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	TO-251AA	TO-252AA	TO-220AB	TO-247	4 PIN DIP	TO-262AA	TO-263AB	MS-012AA
12	2.5/3.5	0.05/0.13 (COMP N&P)								RF1K49092
12	3.5	2 X 0.05								RF1K49090
30	3.5	2 X 0.06								RF1K49088
30	6.3	2 X 0.03								RF1K49156
30	16	0.022	RFD16N03L	RFD16N03LSM						
30	45	0.022			RFP45N03L			RF1S45N03L	RF1S45N03LSM	
50	4.0	0.800			RFP4N05L					
50	14	0.100	RFD14N05L	RFD14N05LSM	RFP14N05L					
50	15	0.140			RFP15N05L					
50	16	0.047	RFD16N05L	RFD16N05LSM						
50	25	0.047			RFP25N05L					
50	50	0.022			RFP50N05L	RFG50N05L				
60	2.0	0.160					RFW2N06RLE			
60	4.0	0.800	RFD4N06L	RFD4N06LSM	RFP4N06L					
60	12	0.135	RFD12N06RLE	RFD12N06RLESM	RFP12N06RLE					
60	12	0.15	RFD3055LE	RFD3055LESM	RFP3055LE					
60	14	0.100	RFD14N06L	RFD14N06LSM	RFP14N06L					
60	15	0.140			RFP15N06L					
60	16	0.047	RFD16N06LE	RFD16N06LESM						
60	17	0.100			RFP17N06L					
60	23	0.065			RFP23N06LE			RF1S23N06LE	RF1S23N06LESM	
60	25	0.085			RFP25N06L					
60	30	0.047			RFP30N06LE			RF1S30N06LE	RF1S30N06LESM	
60	45	0.028			RFP45N06LE	RFG45N06LE		RF1S45N06LE	RF1S45N06LESM	
60	50	0.022			RFP50N06LE	RFG50N06LE		RF1S50N06LE	RF1S50N06LESM	
80	2.0	1.050			RFP2N08L					

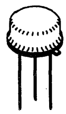
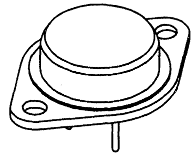
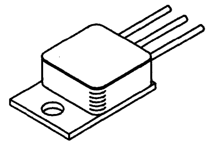
N-CHANNEL LOGIC LEVEL DEVICES (Continued)

MAXIMUM RATINGS										
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	TO-251AA	TO-252AA	TO-220AB	TO-247	4 PIN DIP	TO-262AA	TO-263AB	MS-012AA
80	3.0	0.800	RFD3N08L	RFD3N08LSM						
80	12	0.200			RFP12N08L					
80	15	0.140			RFP15N08L					
100	2.0	1.050			RFP2N10L					
100	7.0	0.300	RFD7N10LE	RFD7N10LESM	RFP7N10LE					
100	30	0.200			RFP12N10L					
100	40	0.040			RFP40N10LE	RFG40N10LE		RF1S40N60LE	RF1S40N10LESM	
120	2.0	1.750			RFP2N12L					
120	10	0.300			RFP10N12L					
150	2.0	1.750			RFP2N15L					
150	10	0.300			RFP10N15L					
180	2.0	3.500			RFP2N18L					
180	8.0	0.500			RFP8N18L					
200	2.0	3.500			RFP2N20L					
200	8.0	0.500			RFP8N10L					

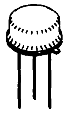
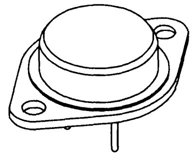
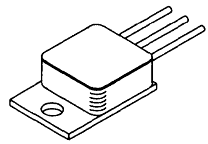
P-CHANNEL LOGIC LEVEL DEVICES

MAXIMUM RATINGS						
BV_{DSS} (V)	I_D (A)	$r_{DS(ON)}$ (Ω)	TO-251AA	TO-252AA	TO-220AB	MS-012AA
12	3.5	2 x 0.13				RF1K49093
30	10	0.200	RFD10P03L	RFD10P03LSM	RFP10P03L	

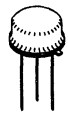
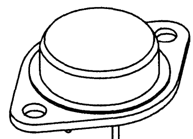
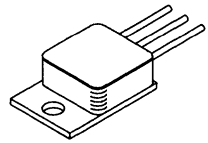
HERMETIC N-CHANNEL

MAXIMUM RATINGS			PACKAGE		
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ (Ω)	 TO-205AF	 TO-204	 TO-254AA
50	2.0	0.95	RFL2N05		
50	15.0	0.14		RFM15N05	
60	2.0	0.95	RFL2N06		
60	12.0	0.25		2N6755	
60	15.0	0.14		RFM15N06	
60	25.0	0.025			RFF70N06
60	33.0	0.08		IRF153	
60	40.0	0.055		IRF151	
80	1.0	1.2	RFL1N08		
80	3.0	0.8	IRFF113		
80	3.5	0.6	IRFF111		
80	5.0	0.4	IRFF123		
80	6.0	0.3	IRFF121		
80	7.0	0.25	IRFF133		
80	8.0	0.36		IRF123	
80	8.0	0.18	IRFF131		
80	9.2	0.27		IRF121	
80	12.0	0.23		IRF133	
80	12.0	0.2		RFMI2N08	
80	14.0	0.16		IRF131	
80	18.0	0.1		RFM18N08	
80	25.0	0.1		IRF143	
80	28.0	0.077		IRF141	
100	1.0	1.2	RFL1N10		
100	3.0	0.8	IRFF112		
100	3.5	0.6	IRFF110		
100	3.5	0.6	2N6782 (Note 1)		
100	5.0	0.4	IRFF122		
100	6.0	0.3	2N6788 (Note 1)		
100	6.0	0.3	IRFF120		
100	7.0	0.25	IRFF132		
100	8.0	0.18	IRFF130		
100	8.0	0.36		IRF122	
100	8.0	0.18	2N6796 (Note 1)		

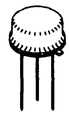
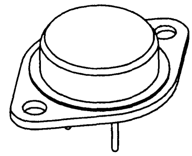
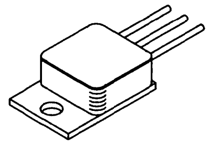
HERMETIC N-CHANNEL (Continued)

MAXIMUM RATINGS			PACKAGE		
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ (Ω)	 TO-205AF	 TO-204	 TO-254AA
100	9.2	0.27		IRF120	
100	12.0	0.2		RFM12N10	
100	12.0	0.23		IRF132	
100	14.0	0.16		IRF130	
100	14.0	0.18		2N6756 (Note 1)	
100	18.0	0.1		RFM18N10	
100	25.0	0.1		IRF142	
100	28.0	0.077		IRF140	
100	33.0	0.08		IRF152	
100	34.0	0.07			2N7224 (Notes 1, 2)
100	40.0	0.055		IRF150	
120	1.0	1.9	RFL1N12		
120	4.0	0.4	RFL4N12		
120	10.0	0.3		RFM10N12	
120	15.0	0.15		RFM15N12	
150	1.0	1.9	RFL1N15		
150	1.8	2.4	IRFF213		
150	2.2	1.5	IRFF211		
150	3.0	1.2	IRFF223		
150	3.5	0.8	IRFF221		
150	4.0	0.4	RFL4N15		
150	4.0	1.2		IRF223	
150	4.5	0.6	IRFF233		
150	5.0	0.8		IRF221	
150	5.5	0.4	IRFF231		
150	8.0	0.6		2N6757	
150	8.0	0.6		IRF233	
150	9.0	0.4		IRF231	
150	10.0	0.3		RFM10N15	
150	15.0	0.15		RFM15N15	
150	16.0	0.22		IRF243	
150	18.0	0.18		IRF241	
150	25.0	0.12		IRF253	
150	25.0	0.12		2N6765	

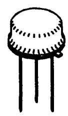
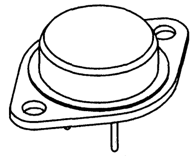
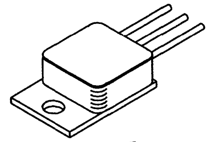
HERMETIC N-CHANNEL (Continued)

MAXIMUM RATINGS			PACKAGE		
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ (Ω)	 TO-205AF	 TO-204	 TO-254AA
150	30.0	0.085		IRF251	
180	1.0	3.65	RFL1N18		
180	12.0	0.25		RFM12N18	
180	25.0	0.15		RFK25N18	
200	1.0	3.65	RFL1N20		
200	1.8	2.4	IRFF212		
200	2.2	1.5	IRFF210		
200	2.3	1.5	2N6784 (Note 1)		
200	3.0	1.2	IRFF222		
200	3.5	0.8	2N6790 (Note 1)		
200	3.5	0.8	IRFF220		
200	4.0	1.2		IRF222	
200	4.5	0.6	IRFF232		
200	5.0	0.8		IRF220	
200	5.5	0.4	IRFF230		
200	5.5	0.4	2N6798 (Note 1)		
200	8.0	0.6		IRF232	
200	9.0	0.4		IRF230	
200	9.0	0.4		2N6758 (Note 1)	
200	12.0	0.25		RFM12N20	
200	16.0	0.22		IRF242	
200	18.0	0.18		IRF240	
200	25.0	0.15		RFK25N20	
200	25.0	0.12		IRF252	
200	27.4	0.1			2N7225 (Notes 1, 2)
200	30.0	0.085		2N6766 (Note 1)	
200	30.0	0.085		IRF250	
250	13.0	0.34		IRF245	
250	14.0	0.28		IRF244	
275	13.0	0.34		IRF247	
275	14.0	0.28		IRF246	
350	1.2	5	IRFF313		
350	1.4	3.6	IRFF311		
350	2.0	2.5	IRFF323		

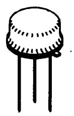
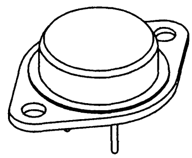
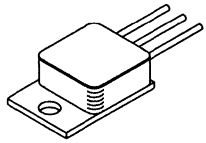
HERMETIC N-CHANNEL (Continued)

MAXIMUM RATINGS			PACKAGE		
					
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ (Ω)	TO-205AF	TO-204	TO-254AA
350	2.5	1.8	IRFF321		
350	2.8	2.5		IRF323	
350	3.0	1.5	IRFF333		
350	3.3	1.8		IRF321	
350	3.5	1	IRFF331		
350	4.0	2		RFM4N35	
350	4.5	1.5		2N6759	
350	4.5	1.5		IRF333	
350	5.5	1		IRF331	
350	7.0	0.75		RFM7N35	
350	8.3	0.8		IRF343	
350	10.0	0.55		IRF341	
350	12.0	0.5		RFM12N35	
350	12.0	0.4		2N6767	
350	13.0	0.4		IRF353	
350	15.0	0.3		IRF351	
400	1.2	5	IRFF312		
400	1.3	3.6	2N6786 (Note 1)		
400	1.4	3.6	IRFF310		
400	2.0	2.5	IRFF322		
400	2.0	1.8	2N6792 (Note 1)		
400	2.5	1.8	IRFF320		
400	2.8	2.5		IRF322	
400	3.0	1.5	IRFF332		
400	3.0	1	2N6800 (Note 1)		
400	3.3	1.8		IRF320	
400	3.5	1	IRFF330		
400	4.0	2		RFM4N40	
400	4.5	1.5		IRF332	
400	5.5	1		IRF330	
400	5.5	1		2N6760 (Note 1)	
400	7.0	0.75		RFM7N40	
400	8.3	0.8		IRF342	
400	10.0	0.55		IRF340	

HERMETIC N-CHANNEL (Continued)

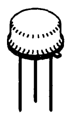
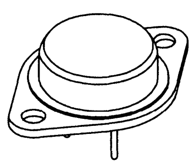
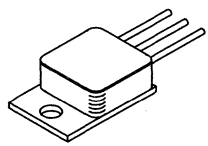
MAXIMUM RATINGS			PACKAGE		
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ (Ω)	 TO-205AF	 TO-204	 TO-254AA
400	12.0	0.5		RFM12N40	
400	13.0	0.4		IRF352	
400	14.0	0.3		2N6768	
400	14.0	0.315			2N7227 (Notes 1, 2)
400	15.0	0.3		IRF350	
450	1.4	4	IRFF423		
450	1.6	3	IRFF421		
450	2.2	4		IRF423	
450	2.3	2	IRFF433		
450	2.5	3		IRF421	
450	2.8	1.5	IRFF431		
450	3.0	3		RFM3N45	
450	4.0	2		2N6761	
450	4.0	2		IRF433	
450	4.5	1.5		IRF431	
450	6.0	1.25		RFM6N45	
450	7.0	1.1		IRF443	
450	8.0	0.85		IRF441	
450	10.0	0.6		RFM10N45	
450	11.0	0.5		IRF453	
450	11.0	0.5		2N6769	
450	13.0	0.4		IRF451	
500	1.4	4	IRFF422		
500	1.5	3	2N6794 (Note 1)		
500	1.6	3	IRFF420		
500	2.2	4		IRF422	
500	2.3	2	IRFF432		
500	2.5	3		IRF420	
500	2.8	1.5	IRFF430		
500	3.0	3		RFM3N50	
500	3.5	1.5	2N6802 (Note 1)		
500	4.0	2		IRF432	
500	4.5	1.5		2N6762 (Note 1)	
500	4.5	1.5		IRF430	

HERMETIC N-CHANNEL (Continued)

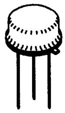
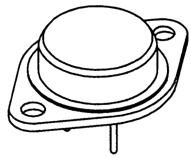
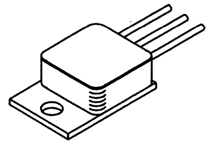
MAXIMUM RATINGS			PACKAGE		
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ (Ω)	 TO-205AF	 TO-204	 TO-254AA
500	7.0	1.1		IRF442	
500	8.0	0.85		IRF440	
500	8.3	0.8		BUZ45A	
500	9.6	0.6		BUZ45	
500	10.0	0.5		BUZ45B	
500	10.0	0.6		RFM10N50	
500	11.0	0.5		IRF452	
500	12.0	0.415			2N7228 (Notes 1, 2)
500	12.0	0.4		2N6770 (Note 1)	
500	13.0	0.4		IRF450	
600	5.4	1.6		IRFAC42	
600	6.2	1.2		IRFAC40	

NOTES:
1. QPL Approved Type.
2. Avaliable in JANTX and JANTXV Reliability Levels only.

HERMETIC LOGIC LEVEL N-CHANNEL

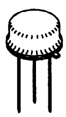
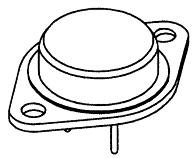
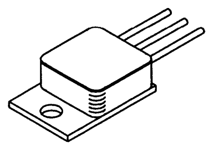
MAXIMUM RATINGS			PACKAGE		
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ (Ω)	 TO-205AF	 TO-204	 TO-254AA
50	2.0	0.95	RFL2N05L		
50	15.0	0.14		RFM15N05L	
60	2.0	0.95	RFL2N06L		
60	15.0	0.14		RFM15N06L	
80	1.0	1.2	RFL1N08L		
80	12.0	0.2		RFM12N08L	
100	1.0	1.2	RFL1N10L		
100	1.7	1.4	2N6901 (Note)		
100	12.0	0.2		RFM12N10L	

HERMETIC LOGIC LEVEL N-CHANNEL (Continued)

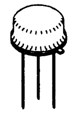
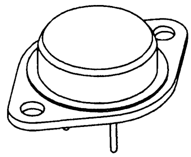
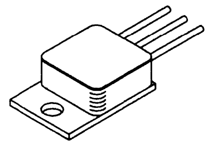
MAXIMUM RATINGS			PACKAGE		
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ (Ω)	 TO-205AF	 TO-204	 TO-254AA
100	12.0	0.2		2N6902 (Note)	
120	1.0	1.9	RFL1N12L		
120	10.0	0.3		RFM10N12L	
150	1.0	1.9	RFL1N15L		
150	10.0	0.3		RFM10N15L	
180	1.0	3.65	RFL1N18L		
180	8.0	0.5		RFM8N18L	
200	1.0	3.65	2N6903 (Note)		
200	1.0	3.65	RFL1N20L		
200	8.0	0.6		2N6904 (Note)	
200	8.0	0.5		RFM8N20L	

NOTE: QPL Approved Type.

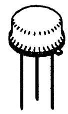
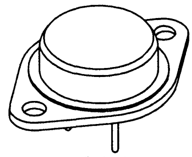
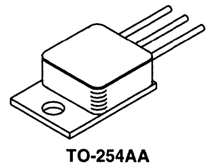
HERMETIC P-CHANNEL

MAXIMUM RATINGS			PACKAGE		
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ (Ω)	 TO-205AF	 TO-204	 TO-254AA
60	3.5	0.8	IRFF9123		
60	4.0	0.6	IRFF9121		
60	5.5	0.4	IRFF9133		
60	6.5	0.3	IRFF9131		
60	10.0	0.4		IRF9133	
60	12.0	0.3		IRF9131	
60	15.0	0.3		IRF9143	
60	19.0	0.2		IRF9141	
60	25.0	0.03			RFF60P06
60	25.0	0.15		IRF9151	
80	1.0	3.65	RFL1P08		

HERMETIC P-CHANNEL (Continued)

MAXIMUM RATINGS			PACKAGE		
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ (Ω)	 TO-205AF	 TO-204	 TO-254AA
80	6.0	0.6		RFM6P08	
80	8.0	0.4		RFM8P08	
80	12.0	0.3		RFM12P08	
80	25.0	0.15		RFK25P08	
100	1.0	3.65	RFL1P10		
100	1.2	3.65	2N6895 (Note)		
100	3.5	0.8	IRFF9122		
100	4.0	0.6	IRFF9120		
100	5.5	0.4	IRFF9132		
100	6.0	0.6		2N6896 (Note)	
100	6.5	0.3	IRFF9130		
100	6.5	0.3	2N6849 (Note)		
100	8.0	0.4		RFM8P10	
100	10.0	0.4		IRF9132	
100	11.0	0.3		2N6804	
100	12.0	0.3		RFM12P10	
100	12.0	0.3		IRF9130	
100	15.0	0.3		IRF9142	
100	19.0	0.2		IRF9140	
100	25.0	0.15		IRF9150	
100	25.0	0.15		RFK25P10	
100	25.0	0.2		2N6898 (Note)	
120	5.0	1		RFM5P12	
120	10.0	0.5		RFM10P12	
150	2.0	2.4	IRFF9223		
150	2.5	1.5	IRFF9221		
150	3.5	1.2	IRFF9233		
150	4.0	0.8	IRFF9231		
150	5.0	1		RFM5P15	
150	5.5	1.2		IRF9233	
150	6.5	0.8		IRF9231	

HERMETIC P-CHANNEL (Continued)

MAXIMUM RATINGS			PACKAGE		
BV_{DSS} (V)	I_{DS} (A)	$r_{DS(ON)}$ (Ω)	 TO-205AF	 TO-204	 TO-254AA
150	9.0	0.7		IRF9243	
150	10.0	0.5		RFM10P15	
150	11.0	0.5		IRF9241	
200	2.0	2.4	IRFF9222		
200	2.5	1.5	IRFF9220		
200	3.5	1.2	IRFF9232		
200	4.0	0.8	IRFF9230		
200	4.0	0.8	2N6851 (Note)		
200	5.5	1.2		IRF9232	
200	6.5	0.8		IRF9230	
200	9.0	0.7		IRF9242	
200	11.0	0.5		IRF9240	

NOTE: QPL Approved Type.

POWER MOSFETs 3

N-CHANNEL POWER MOSFETs

HARRIS SEMICONDUCTOR

RFD14N05, RFD14N05SM, RFP14N05

14A, 50V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 14A, 50V
- $r_{DS(ON)} = 0.100\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFD14N05, RFD14N05SM, and RFP14N05 N-channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

PACKAGING AVAILABILITY

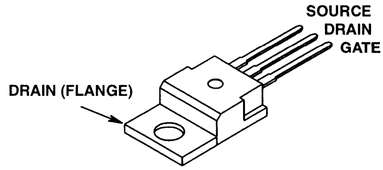
PART NUMBER	PACKAGE	BRAND
RFD14N05	TO-251AA	F14N05
RFD14N05SM	TO-252AA	F14N05
RFP14N05	TO-220AB	RFP14N05

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD14N05SM9A.

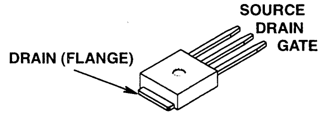
Formerly developmental type TA09770.

Packaging

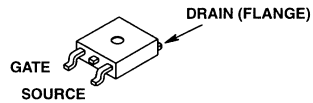
JEDEC TO-220AB



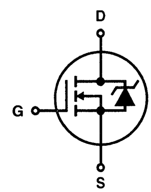
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



3 N-CHANNEL POWER MOSFETS

Absolute Maximum Ratings $T_C = +25^oC$

		RFD14N05, RFD14N05SM, RFP14N05	UNITS
Drain-Source Voltage	V_{DSS}	50	V
Drain-Gate Voltage	V_{DGR}	50	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	14	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	48	W
Derate above +25°C		0.32	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

File Number **2268.3**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 50V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	µA
			$T_C = +150^oC$	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 14A$, $V_{GS} = 10V$		-	-	0.100	Ω
Turn-On Time	t_{ON}	$V_{DD} = 25V$, $I_D = 14A$, $R_L = 3.57\Omega$, $V_{GS} = 10V$, $R_{GS} = 25\Omega$		-	-	60	ns
Turn-On Delay Time	$t_{D(ON)}$			-	14	-	ns
Rise Time	t_R			-	26	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	45	-	ns
Fall Time	t_F			-	17	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $20V$	$V_{DD} = 40V$, $I_D = 14A$, $R_L = 2.86\Omega$	-	-	40	nC
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0V$ to $10V$		-	-	25	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $2V$		-	-	1.5	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	570	-	pF
Output Capacitance	C_{OSS}			-	185	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	50	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	3.125	$^oC/W$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO-251 and TO-252		-	-	100	$^oC/W$
		TO-220		-	-	80	$^oC/W$

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 14A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 14A$, $dI_{SD}/dt = 100A/\mu s$	-	-	125	ns

Typical Performance Curves

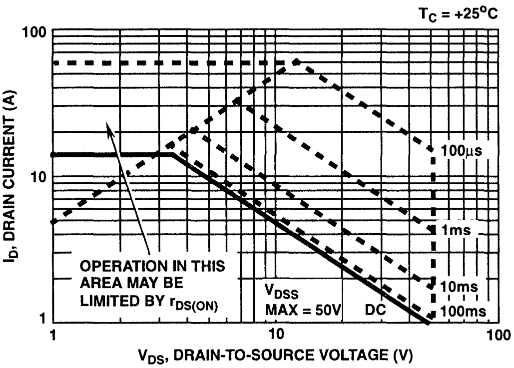


FIGURE 1. SAFE OPERATING AREA CURVE

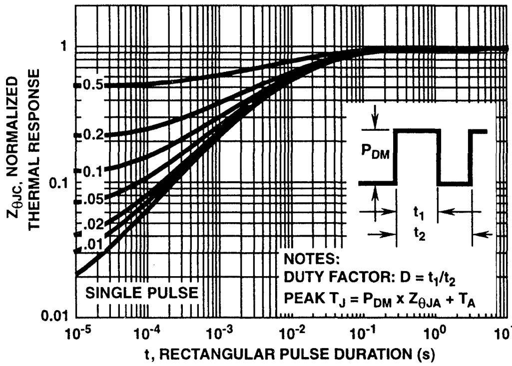


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

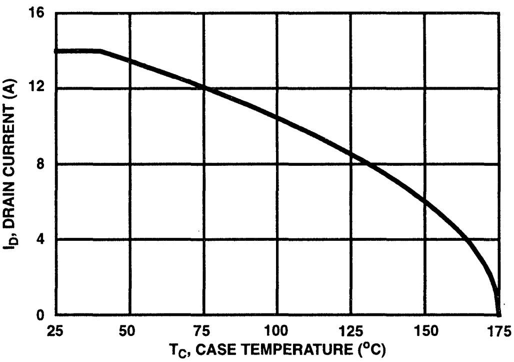


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

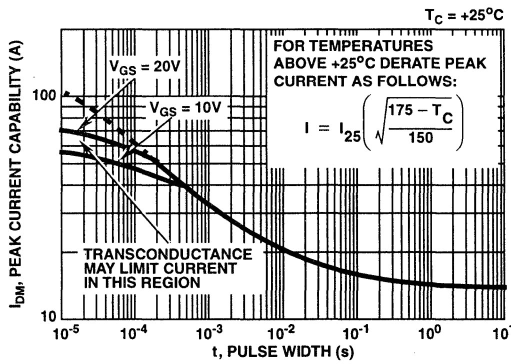


FIGURE 4. PEAK CURRENT CAPABILITY

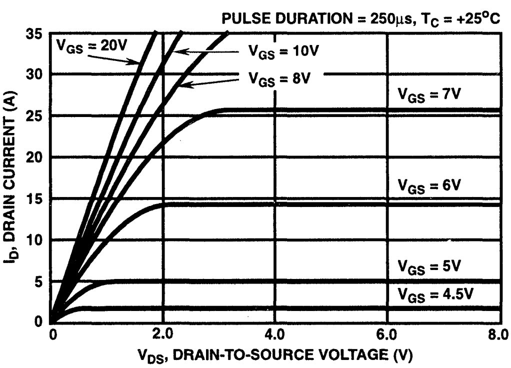


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

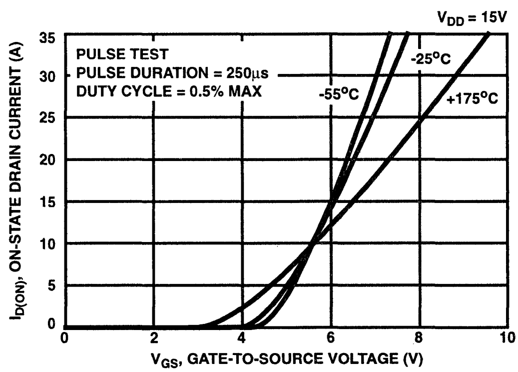


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

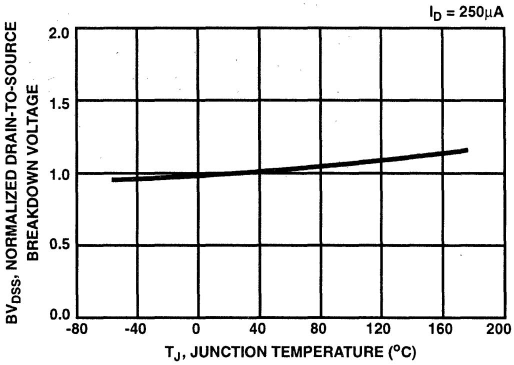


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

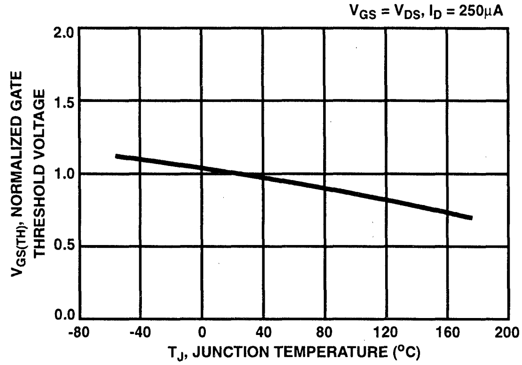


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

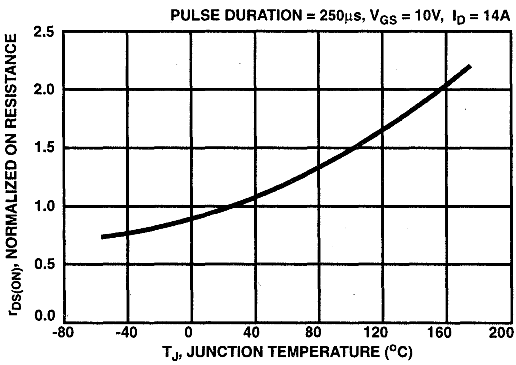


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

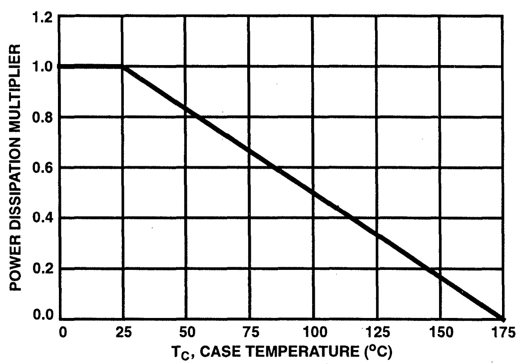


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

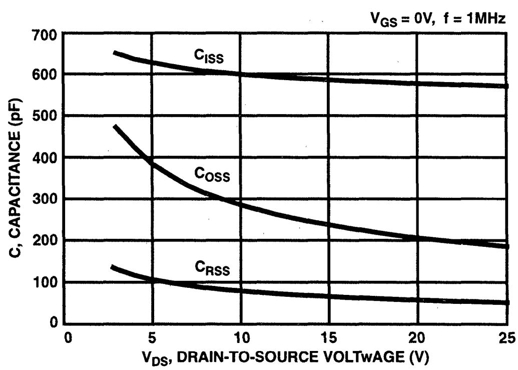


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

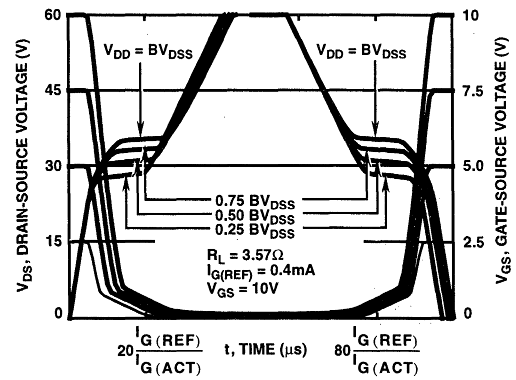


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

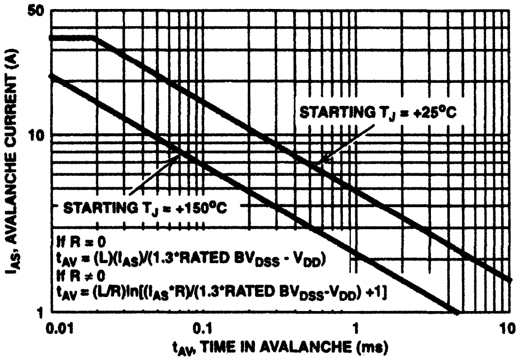


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING.
REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

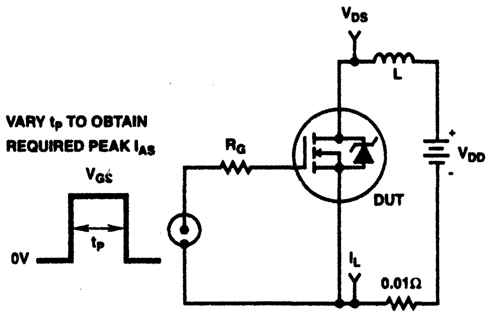


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

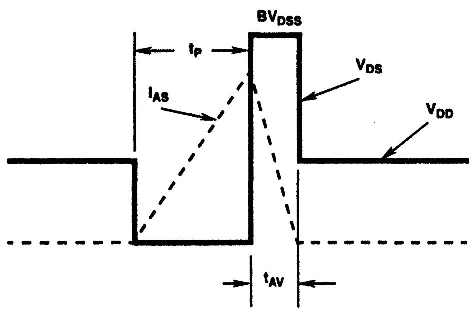


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

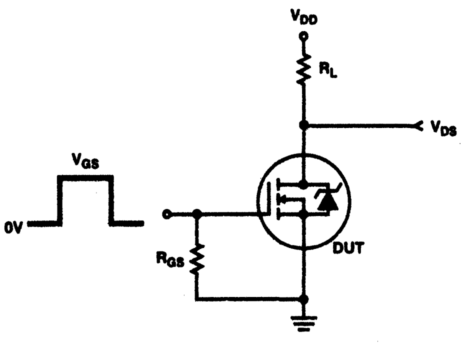


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

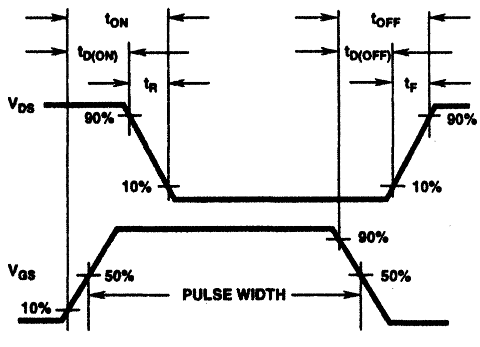


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

3
N-CHANNEL POWER MOSFETs

Temperature Compensated PSPICE Model for the RFD14N05, RFD14N05SM, RFP14N05

```
.SUBCKT RFP14N05 2 1 3 ;     rev 9/12/94

CA 12 8 8.84e-10
CB 15 14 9.34e-10
CIN 6 8 5.2e-10

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 62.87
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.34e-9
LSOURCE 3 7 3.79e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 2.2e-3
RGATE 9 20 5.64
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 42.3e-3
RVTO 18 19 RVTOMOD 1

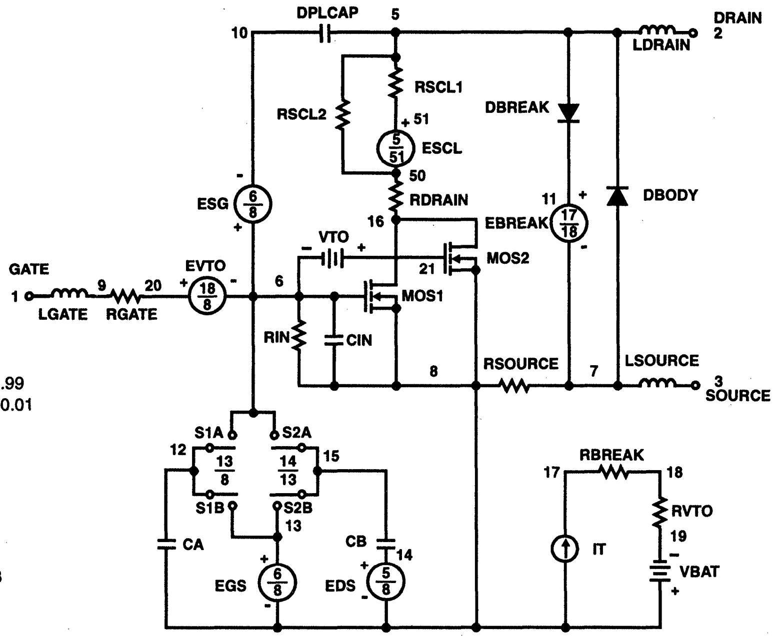
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.82

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/50,6))}

.MODEL DBDMOD D (IS = 1.5e-13 RS = 10.9e-3 TRS1 = 2.3e-3 TRS2 = -1.75e-5 CJO = 6.84e-10 TT = 4.2e-8)
.MODEL DBKMOD D (RS = 4.15e-1 TRS1 = 3.73e-3 TRS2 = -3.21e-5)
.MODEL DPLCAPMOD D (CJO = 26.2e-11 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 3.91 KP = 12.68 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 7.73e-4 TC2 = 2.12e-6)
.MODEL RDSMOD RES (TC1 = 5.0e-3 TC2 = 2.53e-5)
.MODEL RSCLMOD RES (TC1 = 2.05e-3 TC2 = 1.35e-5)
.MODEL RVTOMOD RES (TC1 = -4.44e-3 TC2 = -6.45e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.29 VOFF= -3.29)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.29 VOFF= -5.29)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.25 VOFF= 2.75)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.75 VOFF= -2.25)

.ENDS
```



NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFD14N06, RFD14N06SM, RFP14N06

14A, 60V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 14A, 60V
- $r_{DS(ON)} = 0.100\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFD14N06, RFD14N06SM, and RFP14N06 N-channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

PACKAGING AVAILABILITY

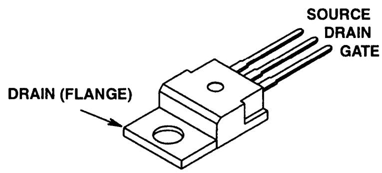
PART NUMBER	PACKAGE	BRAND
RFD14N06	TO-251AA	F14N06
RFD14N06SM	TO-252AA	F14N06
RFP14N06	TO-220AB	RFP14N06

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD14N06SM9A.

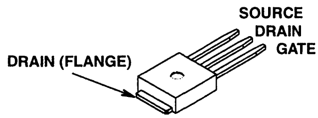
Formerly developmental type TA09770.

Packaging

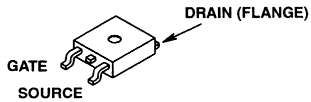
JEDEC TO-220AB



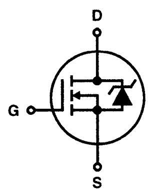
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		RFD14N06, RFD14N06SM, RFP14N06	UNITS
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage	V_{DGR}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	14	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	48	W
Derate above +25°C		0.32	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4002.1**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = +25°C	-	-	1	μA
			T_C = +150°C	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 14A, V_{GS} = 10V		-	-	0.100	Ω
Turn-On Time	t_{ON}	V_{DD} =30V, I_D = 7A, R_L = 4.3Ω, V_{GS} = 10V, R_{GS} = 25Ω		-	-	60	ns
Turn-On Delay Time	$t_{D(ON)}$			-	14	-	ns
Rise Time	t_R			-	26	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	45	-	ns
Fall Time	t_F			-	17	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 48V, I_D = 14A, R_L = 3.42Ω	-	-	40	nC
Gate Charge at 10V	$Q_{G(10)}$	V_{GS} = 0V to 10V		-	-	25	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to 2V		-	-	1.5	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	570	-	pF
Output Capacitance	C_{OSS}			-	185	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	50	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	3.125	°C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO-251 and TO-252		-	-	100	°C/W
		TO-220		-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 14A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 14A, dI_{SD}/dt = 100A/μs	-	-	125	ns

Typical Performance Curves

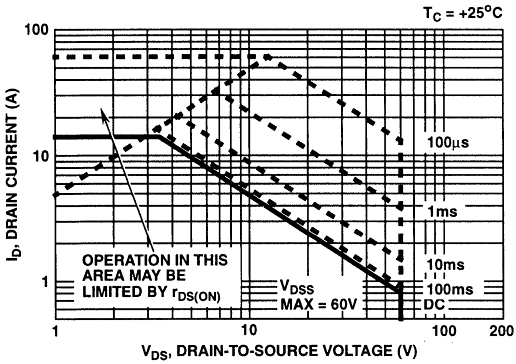


FIGURE 1. SAFE OPERATING AREA CURVE

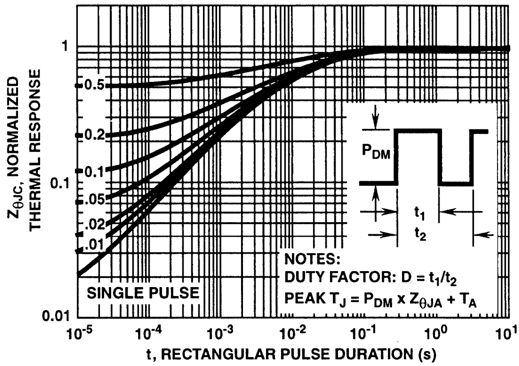


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

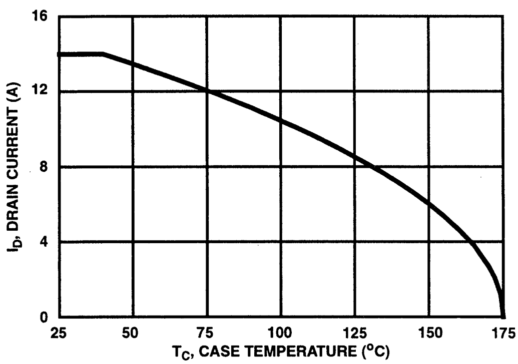


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

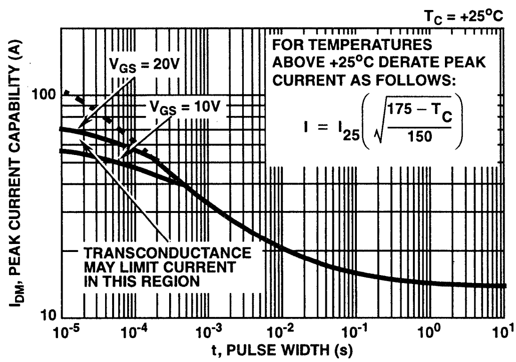


FIGURE 4. PEAK CURRENT CAPABILITY

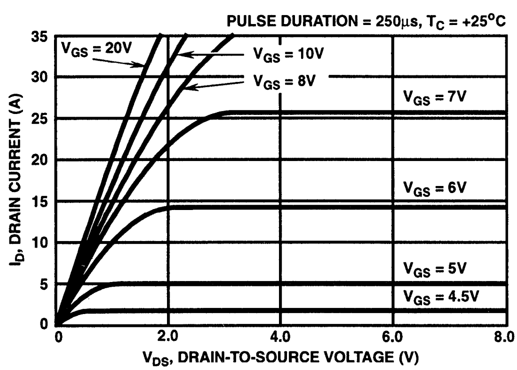


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

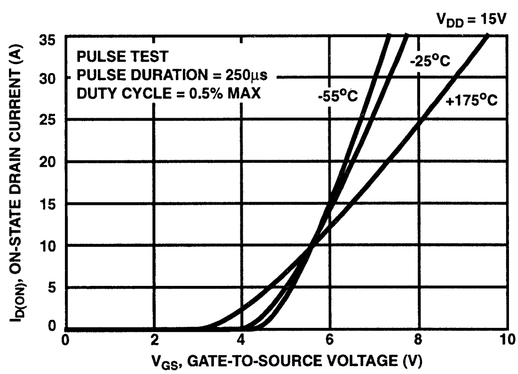


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

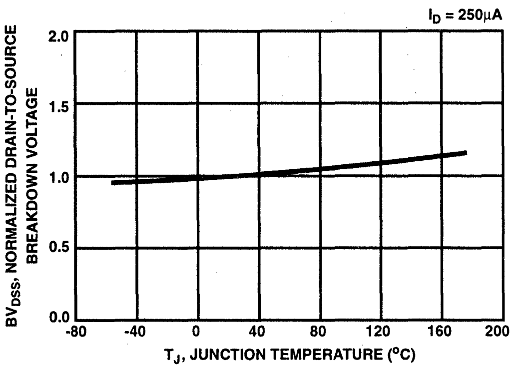


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

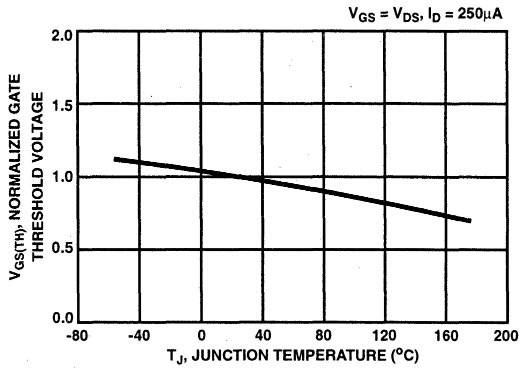


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

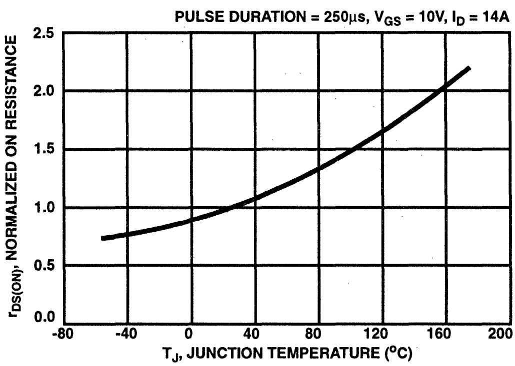


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

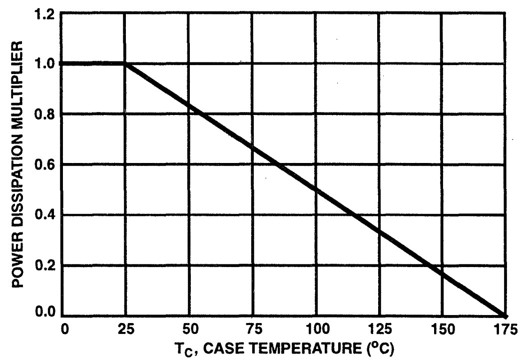


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

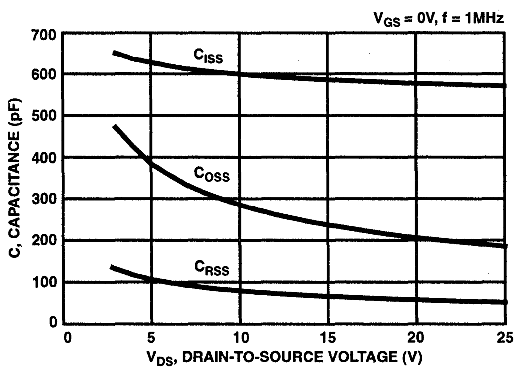


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

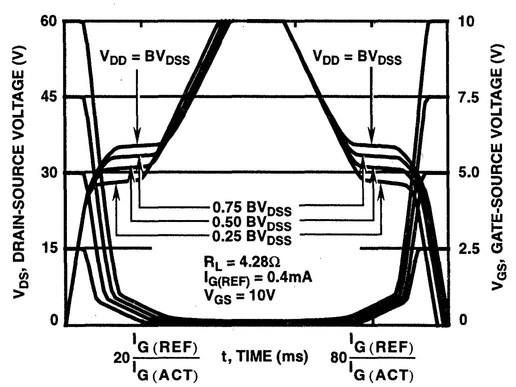


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

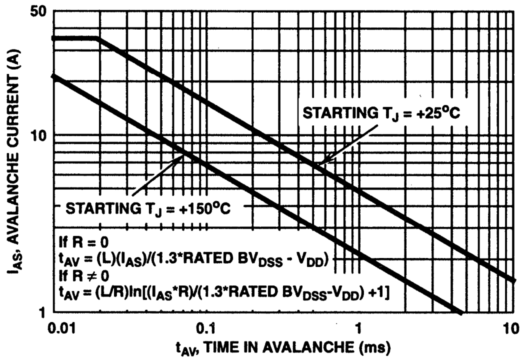


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING.
REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

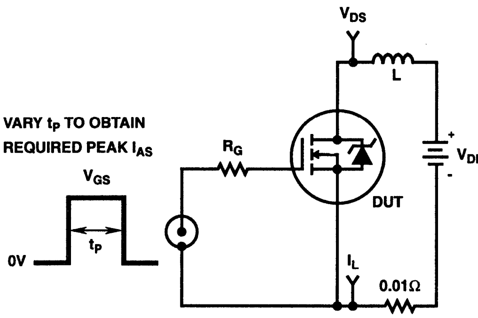


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

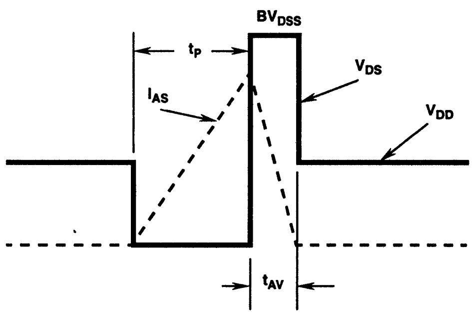


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

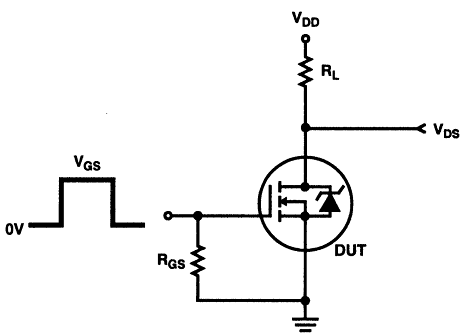


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

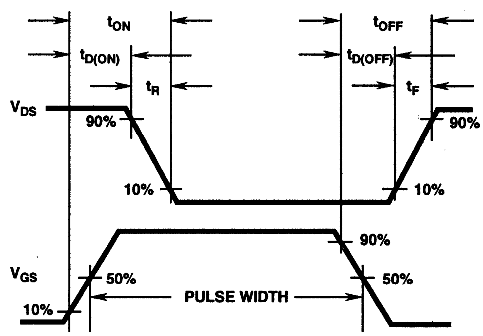
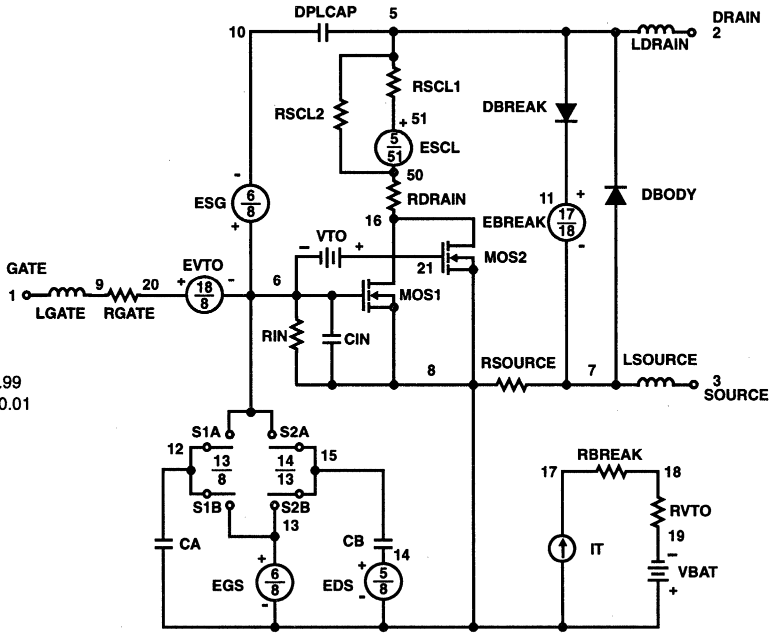


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD14N06, RFD14N06SM, RFP14N06




```
.SUBCKT RFP14N06 2 1 3 ;     rev 9/12/94

CA 12 8 8.84e-10
CB 15 14 9.34e-10
CIN 6 8 5.2e-10

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 62.87
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.34e-9
LSOURCE 3 7 3.79e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 2.2e-3
RGATE 9 20 5.64
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 42.3e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.82

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/50,6))}

.MODEL DBDMOD D (IS = 1.5e-13 RS = 10.9e-3 TRS1 = 2.3e-3 TRS2 = -1.75e-5 CJO = 6.84e-10 TT = 4.2e-8)
.MODEL DBKMOD D (RS = 4.15e-1 TRS1 = 3.73e-3 TRS2 = -3.21e-5)
.MODEL DPLCAPMOD D (CJO = 26.2e-11 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 3.91 KP = 12.68 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 7.73e-4 TC2 = 2.12e-6)
.MODEL RDSMOD RES (TC1 = 5.0e-3 TC2 = 2.53e-5)
.MODEL RSCLMOD RES (TC1 = 2.05e-3 TC2 = 1.35e-5)
.MODEL RVTOMOD RES (TC1 = -4.44e-3 TC2 = -6.45e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.29 VOFF= -3.29)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.29 VOFF= -5.29)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.25 VOFF= 2.75)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.75 VOFF= -2.25)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFD16N05, RFD16N05SM

16A, 50V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 16A, 50V
- $r_{DS(ON)} = 0.047\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFD16N05 and RFD16N05SM N-channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

PACKAGING AVAILABILITY

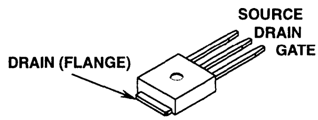
PART NUMBER	PACKAGE	BRAND
RFD16N05	TO-251AA	F16N05
RFD16N05SM	TO-252AA	F16N05

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD16N05SM9A.

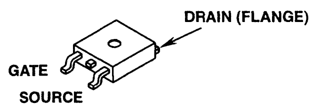
Formerly developmental type TA09771.

Packaging

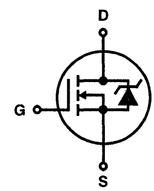
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



3

N-CHANNEL POWER MOSFETs

Absolute Maximum Ratings $T_C = +25^oC$

		RFD16N05, RFD16N05SM	UNITS
Drain-Source Voltage	V_{DSS}	50	V
Drain-Gate Voltage	V_{DGR}	50	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	16	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	72	W
Derate above +25°C		0.48	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

File Number **2267.3**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 50V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	µA
			$T_C = +150^oC$	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 16A$, $V_{GS} = 10V$		-	-	0.047	Ω
Turn-On Time	t_{ON}	$V_{DD} = 25V$, $I_D = 8A$, $R_L = 3.125\Omega$, $V_{GS} = 10V$, $R_{GS} = 25\Omega$		-	-	65	ns
Turn-On Delay Time	$t_{D(ON)}$			-	14	-	ns
Rise Time	t_R			-	30	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	55	-	ns
Fall Time	t_F			-	30	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $20V$	$V_{DD} = 40V$, $I_D = 16A$, $R_L = 2.5\Omega$	-	-	80	nC
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0V$ to $10V$		-	-	45	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $2V$		-	-	2.2	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, $f = 1MHz$		-	900	-	pF
Output Capacitance	C_{OSS}			-	325	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	100	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	2.083	$^oC/W$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO-251 and TO-252		-	-	100	$^oC/W$

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 16A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 16A$, $dI_{SD}/dt = 100A/\mu s$	-	-	125	ns

Typical Performance Curves

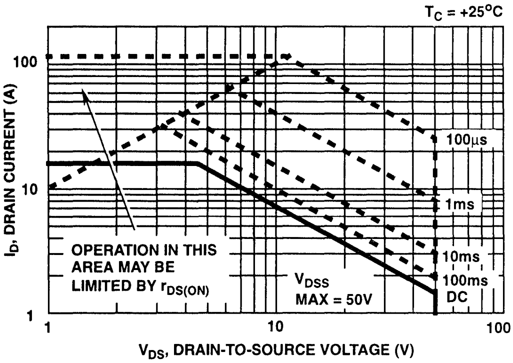


FIGURE 1. SAFE OPERATING AREA CURVE

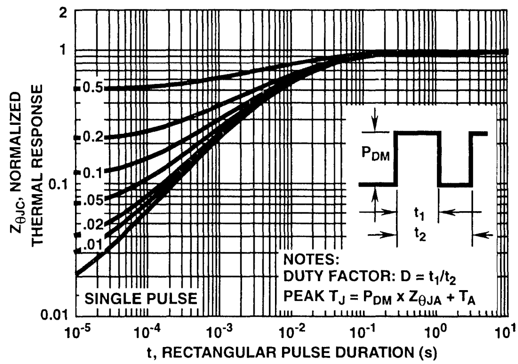


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

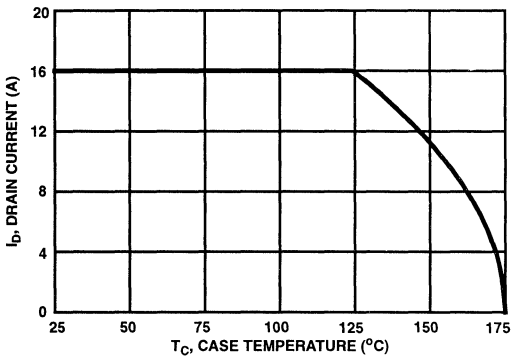


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

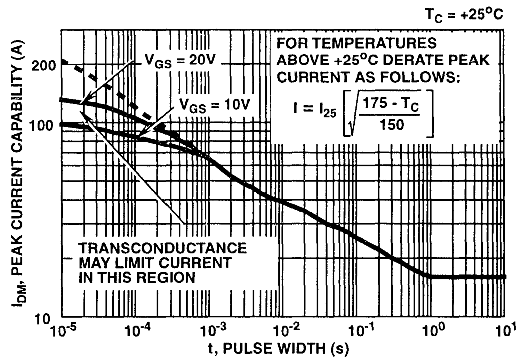


FIGURE 4. PEAK CURRENT CAPABILITY

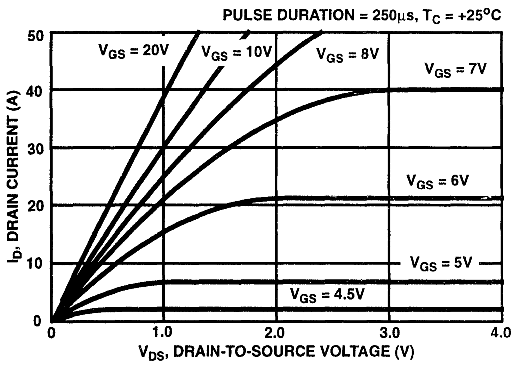


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

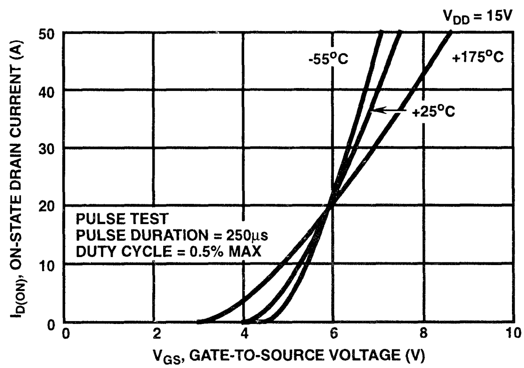


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

3

N-CHANNEL POWER MOSFETs

Typical Performance Curves (Continued)

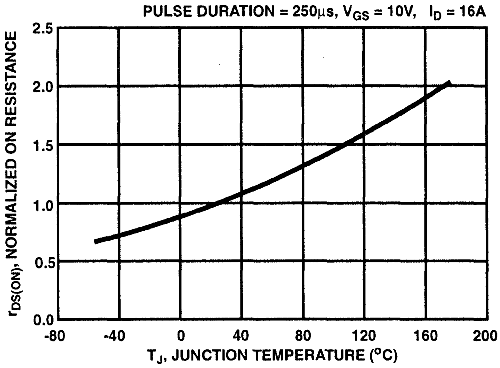


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

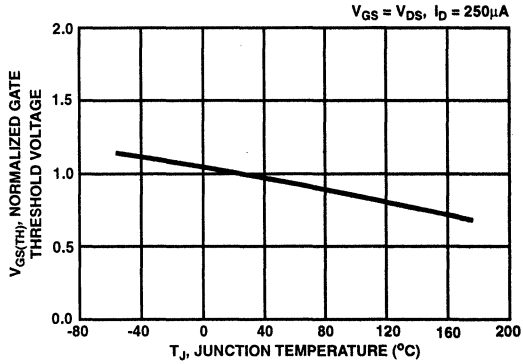


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

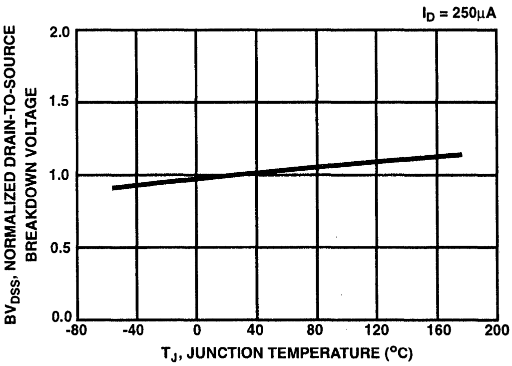


FIGURE 9. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

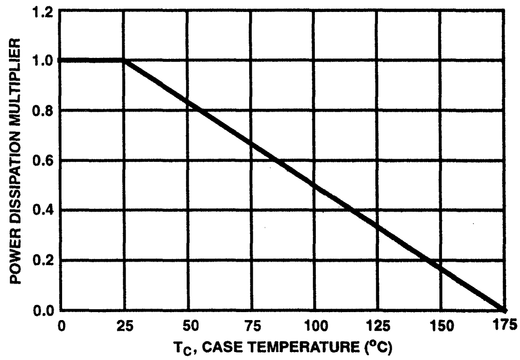


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

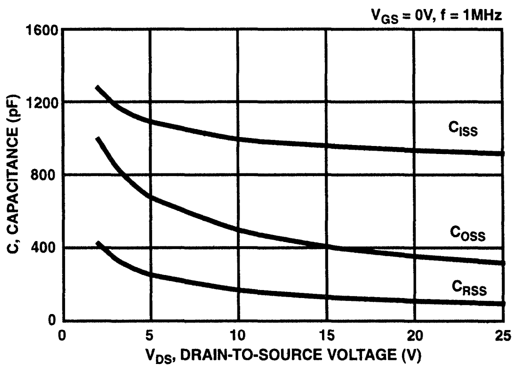


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

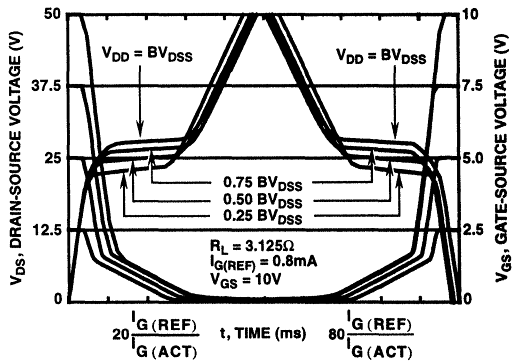


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

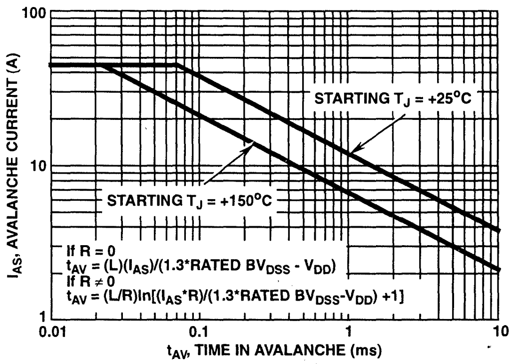


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING.
REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

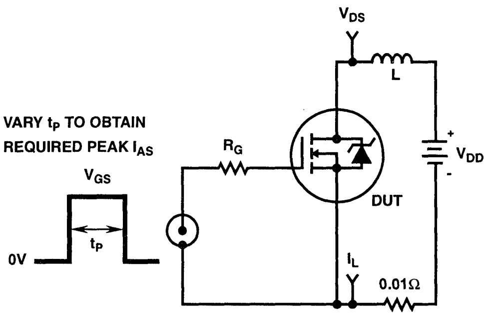


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

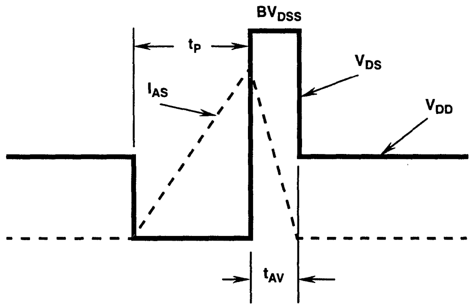


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

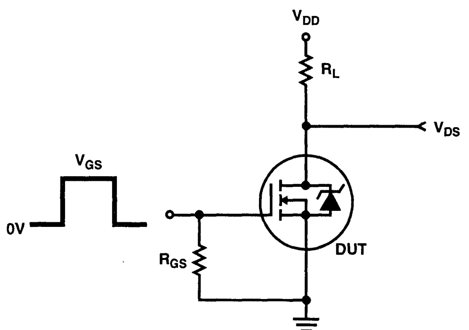


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

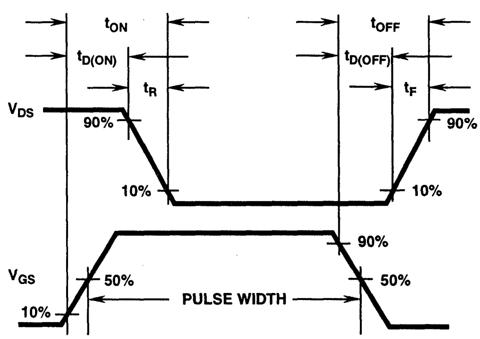
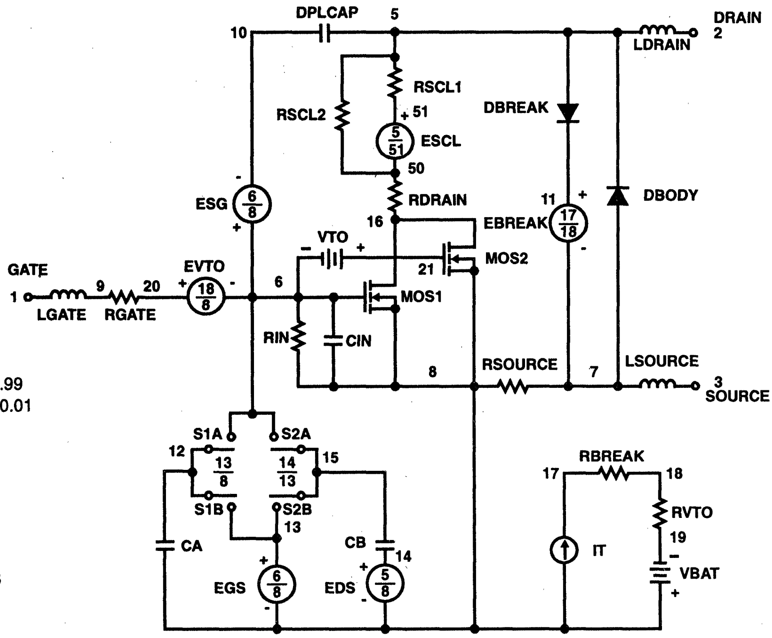


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

3

N-CHANNEL POWER MOSFETs

Temperature Compensated PSPICE Model for the RFD16N05, RFD16N05SM




```
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CA  12  8  1.788e-10
CB  15  14  1.875e-10
CIN  6  8  8.33e-10

DBODY  7  5  DBDMOD
DBREAK  5 11  DBKMOD
DPLCAP 10  5  DPLCAPMOD

EBREAK  11  7  17  18  64.89
EDS  14  8  5  8  1
EGS  13  8  6  8  1
ESG  6  10  6  8  1
EVTO  20  6  18  8  1

IT  8  17  1

LDRAIN  2  5  1e-9
LGATE 1  9  4.56e-9
LSOURCE  3  7  4.13e-9

MOS1  16  6  8  8  MOSMOD  M = 0.99
MOS2  16  21  8  8  MOSMOD  M = 0.01

RBREAK  17  18  RBKMOD  1
RDRAIN  50  16  RDSMOD  0.4e-3
RGATE  9  20  3.0
RIN  6  8  1e9
RSCL1  5  51  RSCLMOD 1e-6
RSCL2  5  50  1e3
RSOURCE  8  7  RDSMOD  21.5e-3
RVTO  18  19  RVTOMOD  1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT  8  19  DC  1
VTO  21  6  0.82

ESCL  51 50  VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/94,7))}

.MODEL DBDMOD D (IS = 2.5e-13  RS = 7.1e-3  TRS1 = 3.04e-3  TRS2 = -10e-6  CJO = 1.12e-9  TT = 5.6e-8)
.MODEL DBKMOD D (RS = 2.51e-1  TRS1 = -6.57e-4  TRS2 = 1.66e-6)
.MODEL DPLCAPMOD D (CJO = 6.1e-10  IS = 1e-30  N = 10)
.MODEL MOSMOD NMOS (VTO = 3.96  KP = 16.68  IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u)
.MODEL RBKMOD RES (TC1 = 1.07e-3  TC2 = -7.19e-7)
.MODEL RDSMOD RES (TC1 = 5.45e-3  TC2 = 1.66e-5)
.MODEL RSCLMOD RES (TC1 = 1.25e-3  TC2 = 17e-6)
.MODEL RVTOMOD RES (TC1 = -5.15e-3  TC2 = -4.83e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -5.25  VOFF= -3.25)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -3.25  VOFF= -5.25)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 0.56  VOFF= 5.56)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 5.56  VOFF= 0.56)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFD16N06, RFD16N06SM

16A, 60V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 16A, 60V
- $r_{DS(ON)} = 0.047\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFD16N06 and RFD16N06SM N-channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

PACKAGING AVAILABILITY

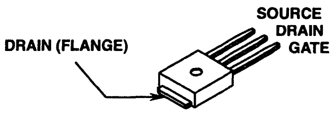
PART NUMBER	PACKAGE	BRAND
RFD16N06	TO-251AA	F16N06
RFD16N06SM	TO-252AA	F16N06

NOTE: When ordering, use the entire part number. Add suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD16N06SM9A.

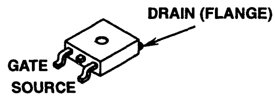
Formerly developmental type TA09771.

Packaging

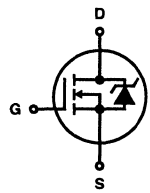
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		RFD16N06, RFD16N06SM	UNITS
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage	V_{DGR}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	16	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	72	W
Derate above +25°C		0.48	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	μA
			$T_C = +150^oC$	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 16A$, $V_{GS} = 10V$		-	-	0.047	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30V$, $I_D = 8A$, $R_L = 3.75\Omega$, $V_{GS} = 10V$, $R_{GS} = 25\Omega$		-	-	65	ns
Turn-On Delay Time	$t_{D(ON)}$			-	14	-	ns
Rise Time	t_R			-	30	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	55	-	ns
Fall Time	t_F			-	30	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $20V$	$V_{DD} = 48V$, $I_D = 16A$, $R_L = 3\Omega$	-	-	80	nC
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0V$ to $10V$		-	-	45	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $2V$		-	-	2.2	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, $f = 1MHz$		-	900	-	pF
Output Capacitance	C_{OSS}			-	325	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	100	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	2.083	°C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO-251 and TO-252		-	-	100	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 16A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 16A$, $dI_{SD}/dt = 100A/\mu s$	-	-	125	ns

Typical Performance Curves

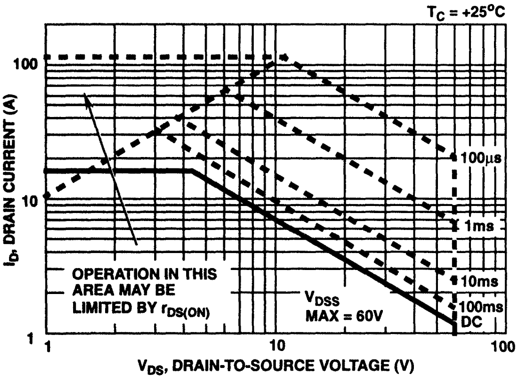


FIGURE 1. SAFE OPERATING AREA CURVE

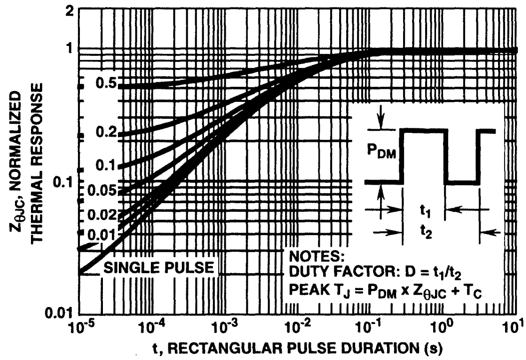


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

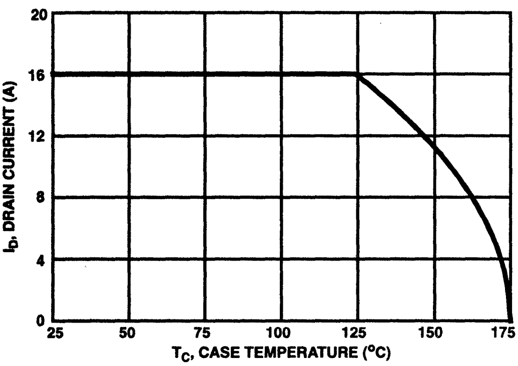


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

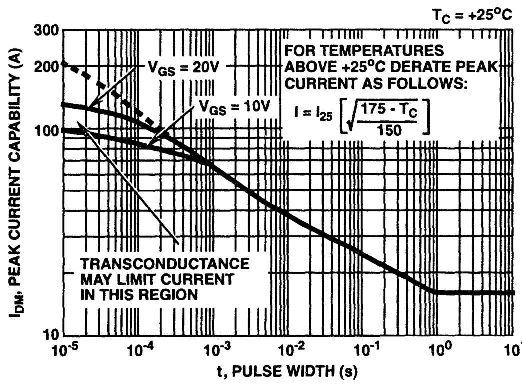


FIGURE 4. PEAK CURRENT CAPABILITY

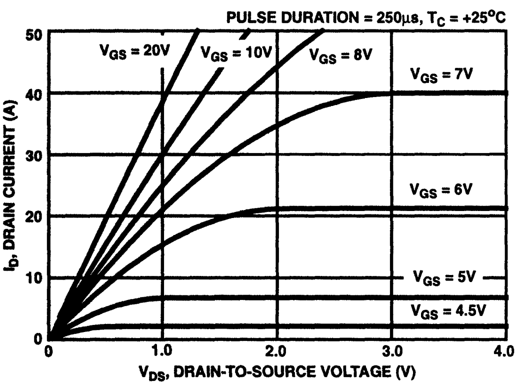


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

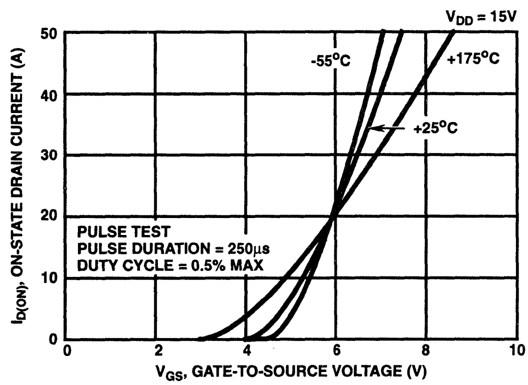


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

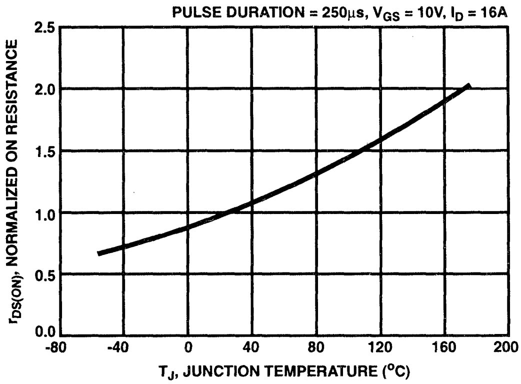


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

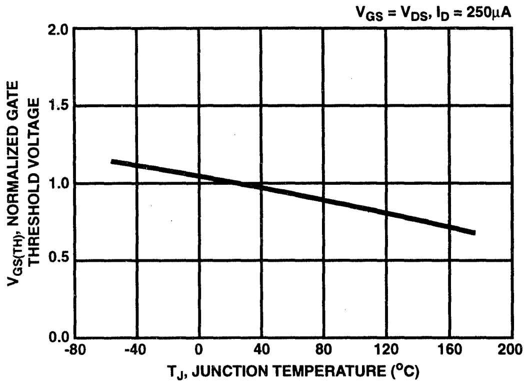


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

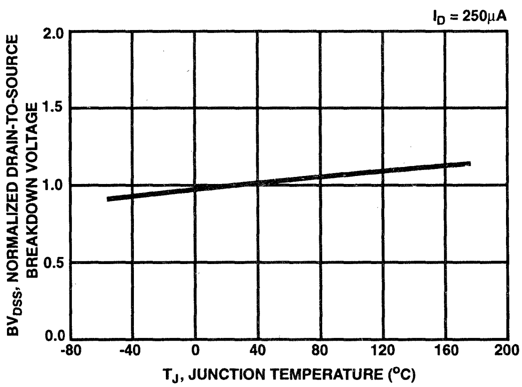


FIGURE 9.. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

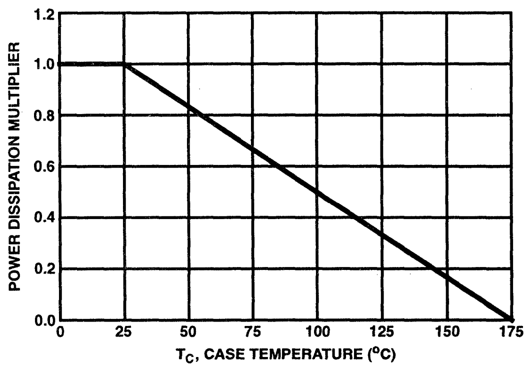


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

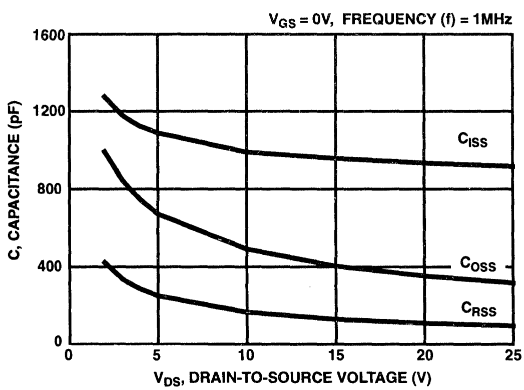


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

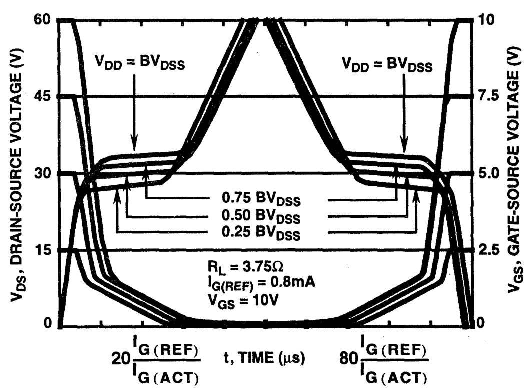


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

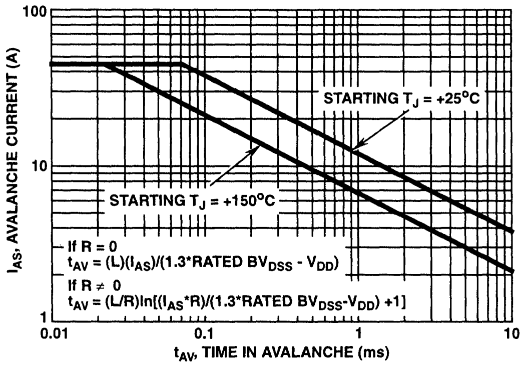


FIGURE13. UNCLAMPED INDUCTIVE SWITCHING.
REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

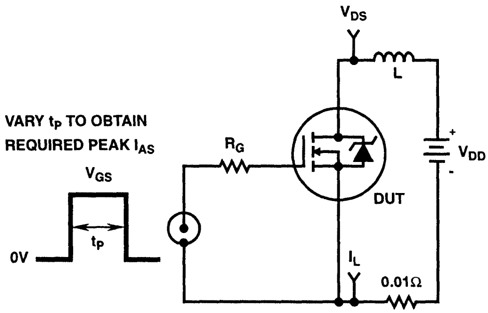


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

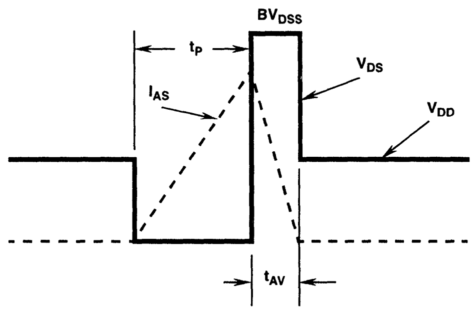


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

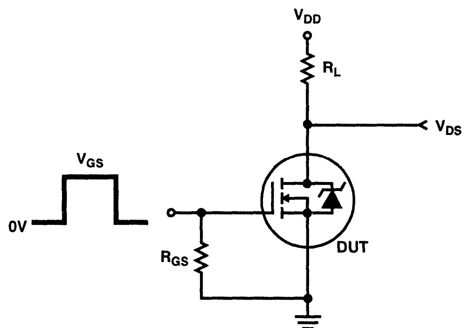


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

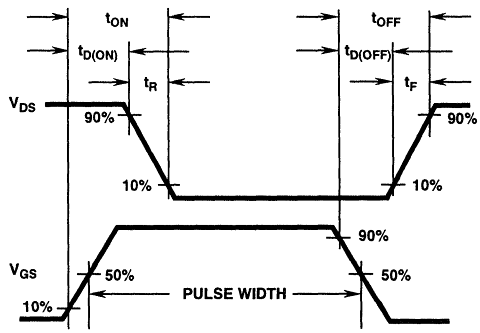
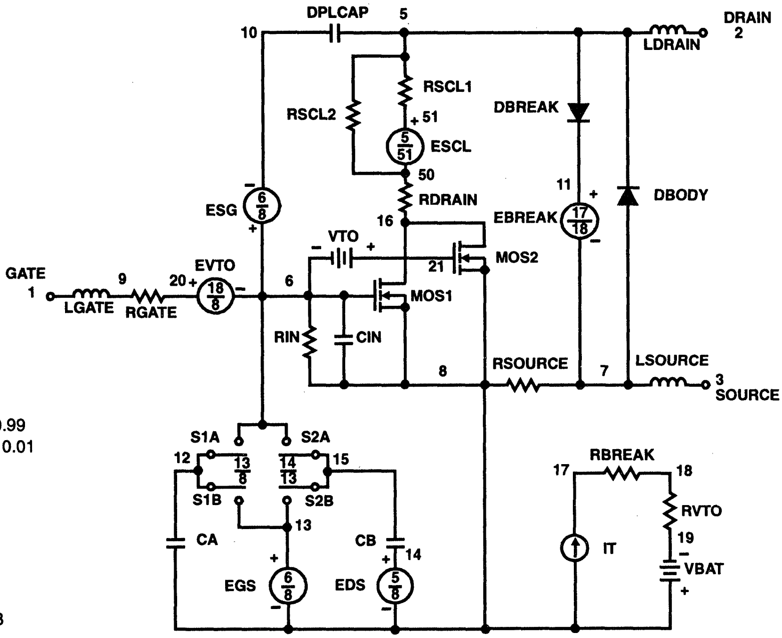


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD16N06, RFD16N06SM




```
.SUBCKT RFD16N06 2 1 3 ;    rev 10/31/94
CA 12 8 1.788e-10
CB 15 14 1.875e-10
CIN 6 8 8.33e-10

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 64.89
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.56e-9
LSOURCE 3 7 4.13e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 0.4e-3
RGATE 9 20 3.0
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 21.5e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.82

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/94,7))}

.MODEL DBDMOD D (IS = 2.5e-13 RS = 7.1e-3 TRS1 = 3.04e-3 TRS2 = -10e-6 CJO = 1.12e-9 TT = 5.6e-8)
.MODEL DBKMOD D (RS = 2.51e-1 TRS1 = -6.57e-4 TRS2 = 1.66e-6)
.MODEL DPLCAPMOD D (CJO = 6.1e-10 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 3.96 KP = 16.68 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 1.07e-3 TC2 = -7.19e-7)
.MODEL RDSMOD RES (TC1 = 5.45e-3 TC2 = 1.66e-5)
.MODEL RSCLMOD RES (TC1 = 1.25e-3 TC2 = 17e-6)
.MODEL RVTOMOD RES (TC1 = -5.15e-3 TC2 = -4.83e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.25 VOFF= -3.25)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.25 VOFF= -5.25)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.56 VOFF= 5.56)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 5.56 VOFF= 0.56)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

HARRIS
SEMICONDUCTOR

RFP25N06, RF1S25N06, RF1S25N06SM

25A, 60V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 25A, 60V
- $r_{DS(ON)} = 0.047\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFP25N06, RF1S25N06, and RF1S25N06SM N-Channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

PACKAGE AVAILABILITY

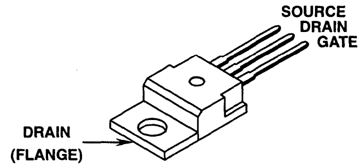
PART NUMBER	PACKAGE	BRAND
RFP25N06	TO-220AB	RFP25N06
RF1S25N06	TO-262AA	F1S25N06
RF1S25N06SM	TO-263AB	F1S25N06

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S25N06SM9A.

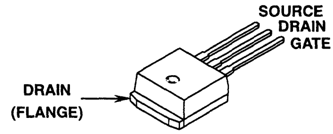
Formerly developmental type TA09771.

Packages

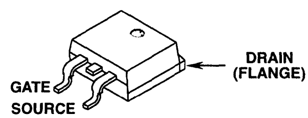
JEDEC TO-220AB



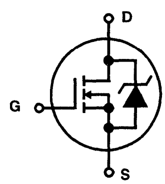
JEDEC TO-262AA



JEDEC TO-263AB



Symbol



Absolute Maximum Ratings $T_C = +25°C$, Unless Otherwise Specified

		RFP25N06, RF1S25N06, RF1S25N06SM	UNITS
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage	V_{DGR}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	25	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25°C$	P_D	72	W
Derate above +25°C		0.48	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **1492.3**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = +25°C	-	-	1	μA
			T_C = +150°C	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 25A, V_{GS} = 10V		-	-	0.047	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 12.5A, R_L = 2.4Ω, V_{GS} = 10V, R_{GS} = 10Ω		-	-	60	ns
Turn-On Delay Time	$t_{D(ON)}$			-	14	-	ns
Rise Time	t_R			-	30	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	45	-	ns
Fall Time	t_F			-	22	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to 20V	V_{DD} = 48V, I_D = 25A, R_L = 1.92Ω	-	-	80	nC
Gate Charge at 10V	$Q_{G(10)}$	V_{GS} = 0V to 10V		-	-	45	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to 2V		-	-	3	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	975	-	pF
Output Capacitance	C_{OSS}			-	330	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	95	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	2.083	°C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 25A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 25A, dI_{SD}/dt = 100A/μs	-	-	125	ns

Typical Performance Curves

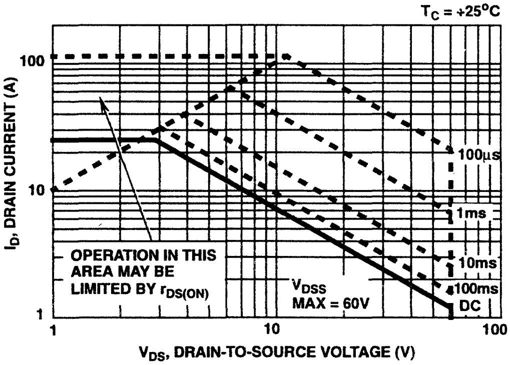


FIGURE 1. SAFE OPERATING AREA CURVE

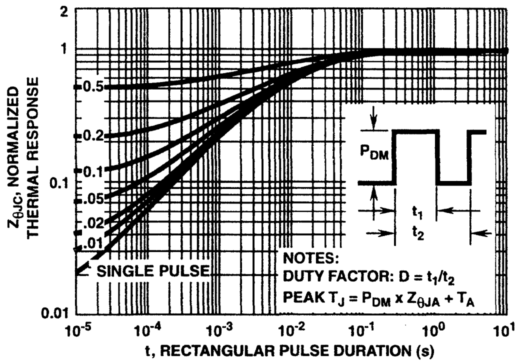


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

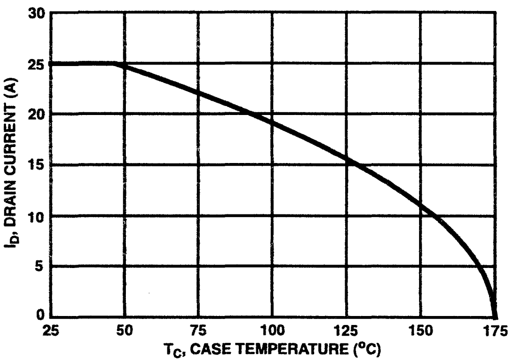


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

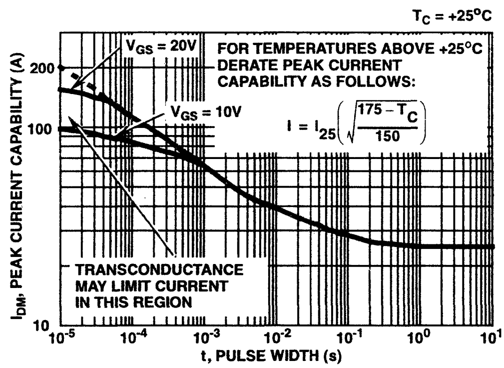


FIGURE 4. PEAK CURRENT CAPABILITY

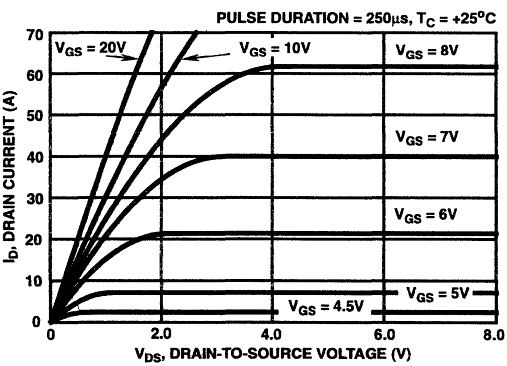


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

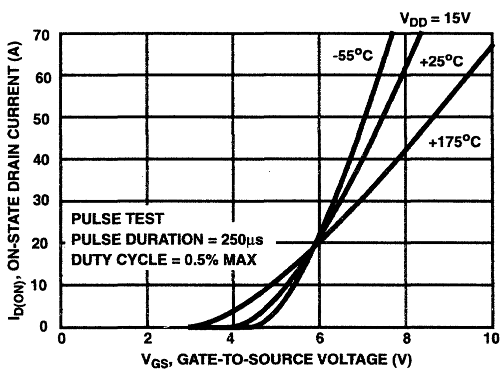


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

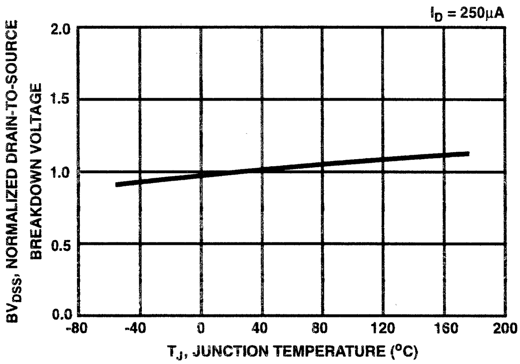


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

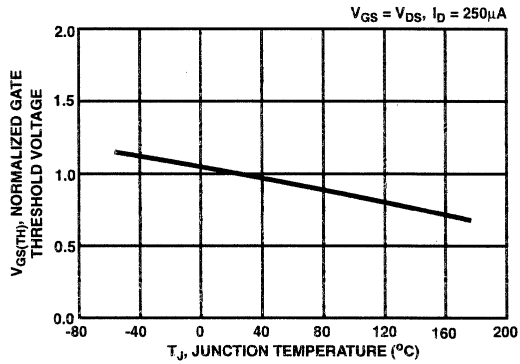


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

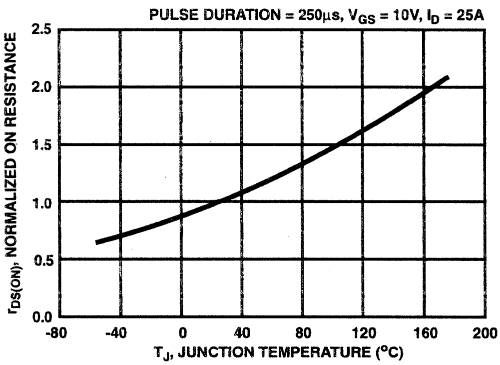


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

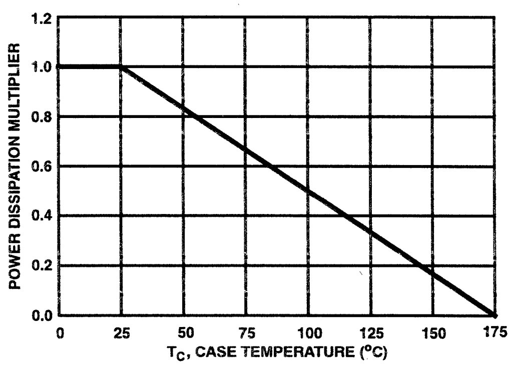


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

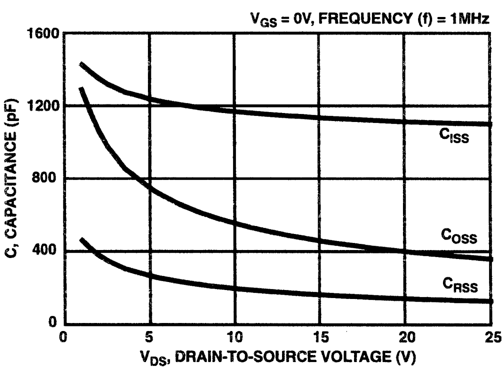


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

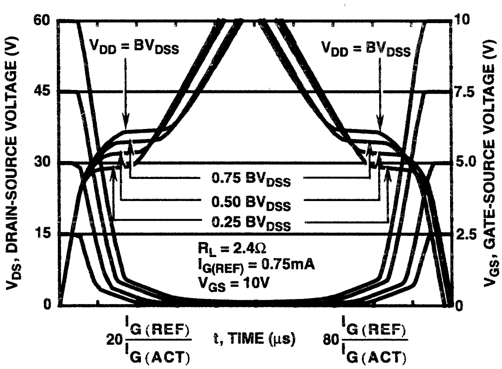


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

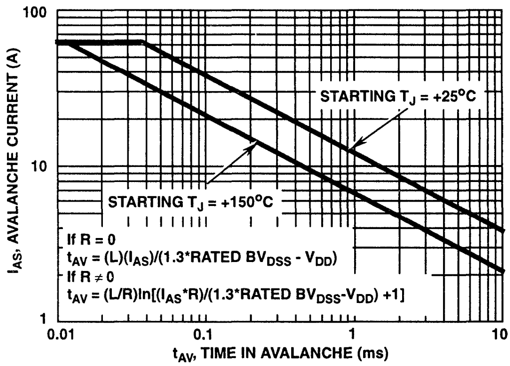


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING.
REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

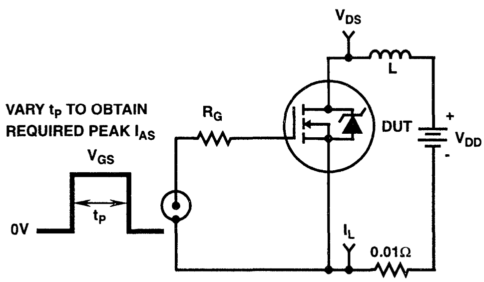


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

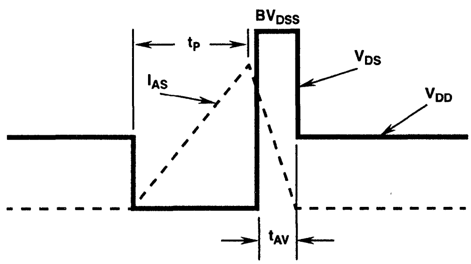


FIGURE 15. UNCLAMPED ENERGY WAVEFORM

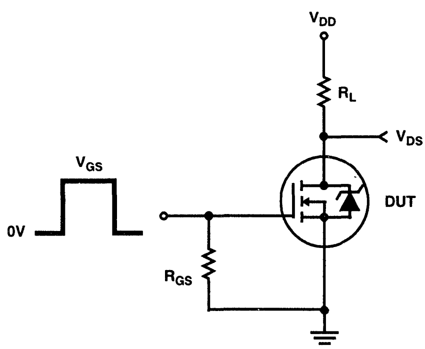


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

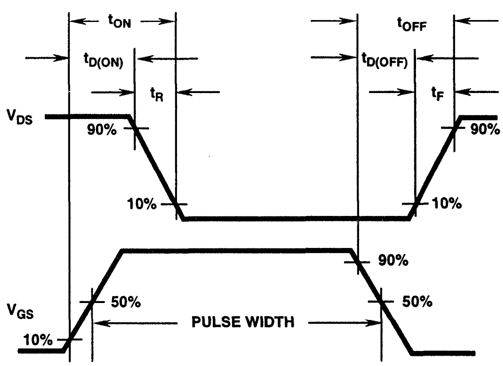


FIGURE 17. RESISTIVE SWITCHING WAVEFORM

3
N-CHANNEL POWER MOSFETs

Temperature Compensated PSPICE Model for the RFP25N06, RF1S25N06, RF1S25N06SM

.SUBCKT RFP25N06 2 1 3 ; rev 8/19/94

CA 12 8 1.83e-9
CB 15 14 1.98e-9
CIN 6 8 9.7e-10

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 65.9
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

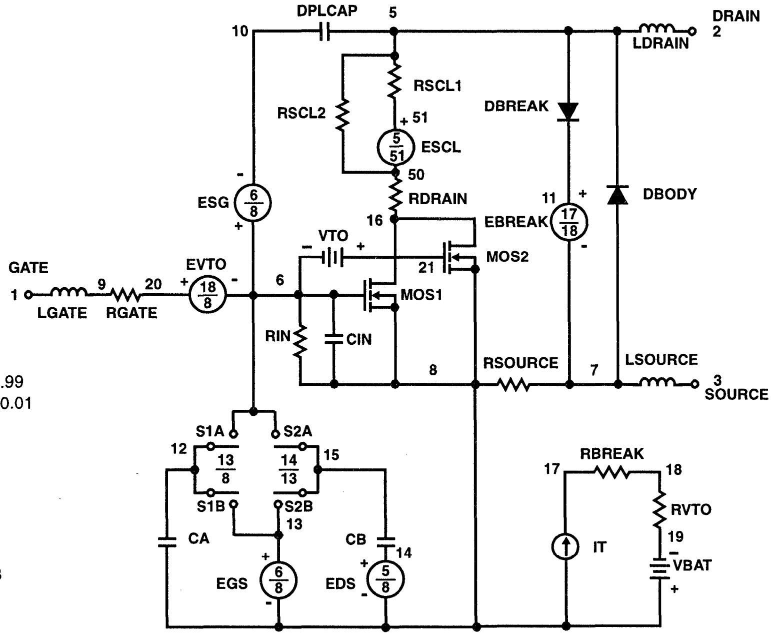
LDRAIN 2 5 1e-9
LGATE 1 9 4.92e-9
LSOURCE 3 7 4.5e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 1.1e-3
RGATE 9 20 2.88
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 20.3e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.764



ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/108,6))}

.MODEL DBDMOD D (IS = 2.32e-13 RS = 5.72e-3 TRS1 = 2.56e-3 TRS2 = -5.13e-6 CJO = 1.18e-9 TT = 5.62e-8)
.MODEL DBKMOD D (RS = 2.00e-1 TRS1 = 3.33e-4 TRS2 = 2.68e-6)
.MODEL DPLCAPMOD D (CJO = 6.55e-10 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 3.89 KP = 15.03 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 1.04e-3 TC2 = -1.04e-6)
.MODEL RDSMOD RES (TC1 = 5.85e-3 TC2 = 1.77e-5)
.MODEL RSCLMOD RES (TC1 = 2.0e-3 TC2 = 1.5e-6)
.MODEL RVTOMOD RES (TC1 = -5.35e-3 TC2 = -3.77e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.04 VOFF= -3.04)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.04 VOFF= -5.04)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.02 VOFF= 1.98)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.98 VOFF= -3.02)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFG45N06, RFP45N06, RF1S45N06, RF1S45N06SM

45A, 60V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 45A, 60V
- $r_{DS(ON)} = 0.028\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFG45N06, RFP45N06, RF1S45N06, RF1S45N06SM N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

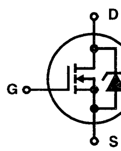
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFG45N06	TO-247	RFG45N06
RFP45N06	TO-220AB	RFP45N06
RF1S45N06	TO-262AA	F1S45N06
RF1S45N06SM	TO-263AB	F1S45N06

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S45N06SM9A.

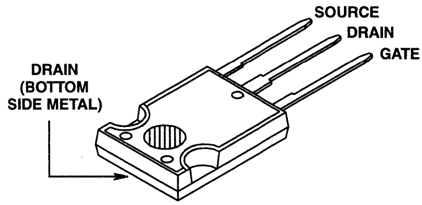
Formerly developmental type TA49028.

Symbol

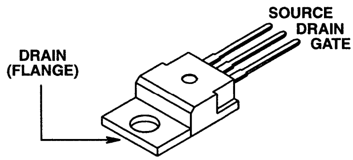


Packages

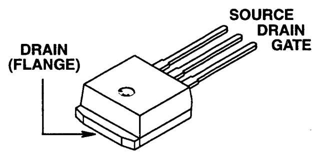
JEDEC STYLE TO-247



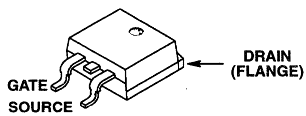
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = +25^oC$

		RFG45N06, RFP45N06 RF1S45N06, RF1S45N06SM	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	45	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Maximum Avalanche Current	I_{AM}	125	A
Power Dissipation			
$T_C = +25^oC$	P_D	131	W
Derate above +25°C	P_T	0.877	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	μA
			$T_C = +150^oC$	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 45A$, $V_{GS} = 10V$		-	-	0.028	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30V$, $I_D = 45A$ $R_L = 0.667\Omega$, $V_{GS} = +10V$ $R_{GS} = 3.6\Omega$		-	-	120	ns
Turn-On Delay Time	$t_{D(ON)}$			-	12	-	ns
Rise Time	t_R			-	74	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	37	-	ns
Fall Time	t_F			-	16	-	ns
Turn-Off Time	t_{OFF}			-	-	80	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0$ to $20V$	$V_{DD} = 48V$, $I_D = 45A$, $R_L = 1.07\Omega$	-	125	150	nC
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0$ to $10V$		-	67	80	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0$ to $2V$		-	3.7	4.5	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz		-	2050	-	pF
Output Capacitance	C_{OSS}			-	600	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	200	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.14	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	$^oC/W$

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 45A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 45A$, $dI_{SD}/dt = 100A/\mu s$	-	-	125	ns

Typical Performance Curves

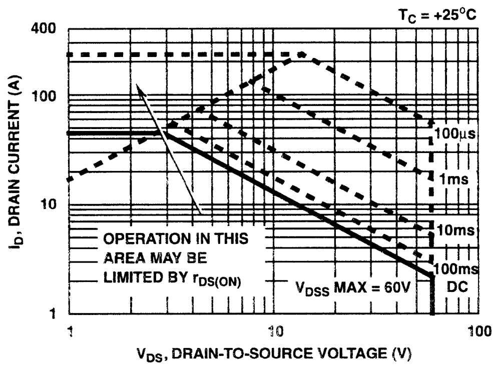


FIGURE 1. SAFE- OPERATING AREA CURVE

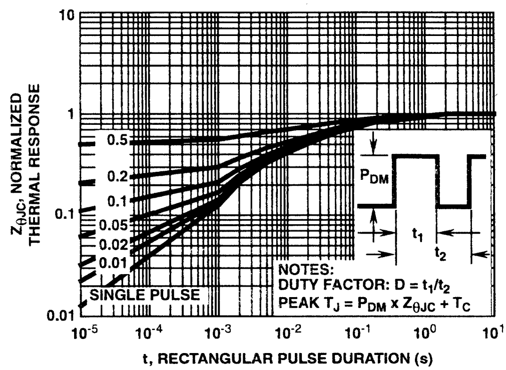


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

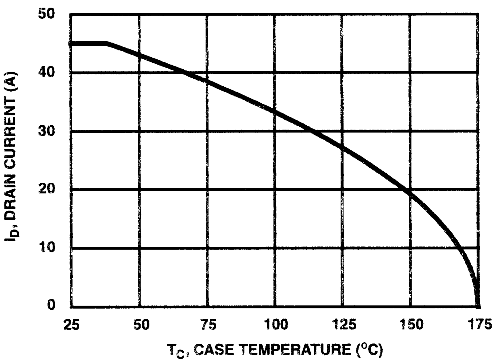


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

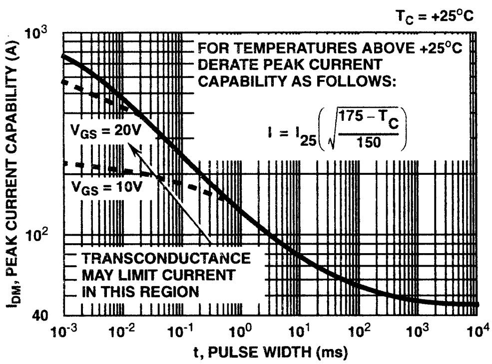


FIGURE 4. PEAK CURRENT CAPABILITY

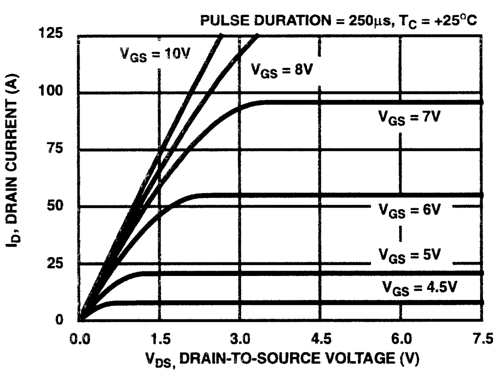


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

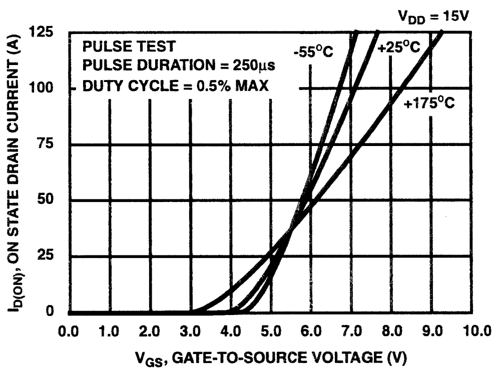


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

3
N-CHANNEL POWER MOSFETs

Typical Performance Curves (Continued)

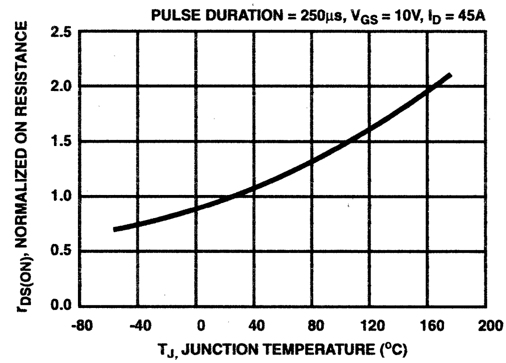


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

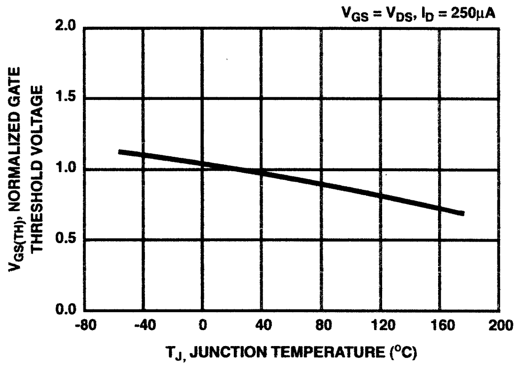


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

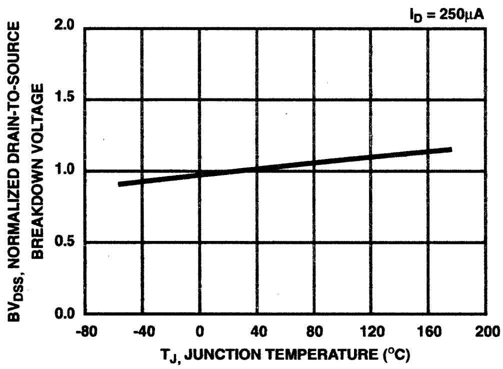


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

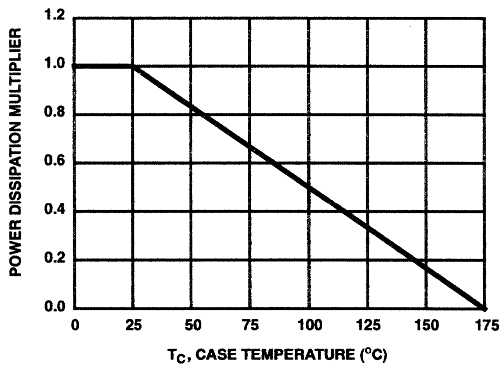


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

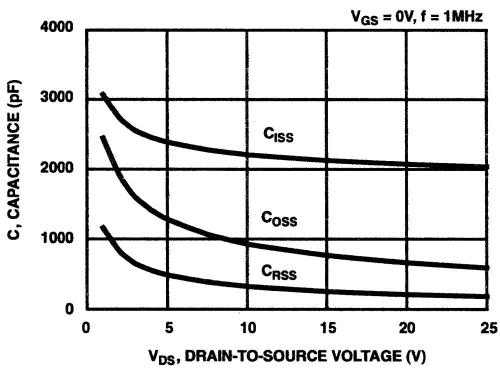


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

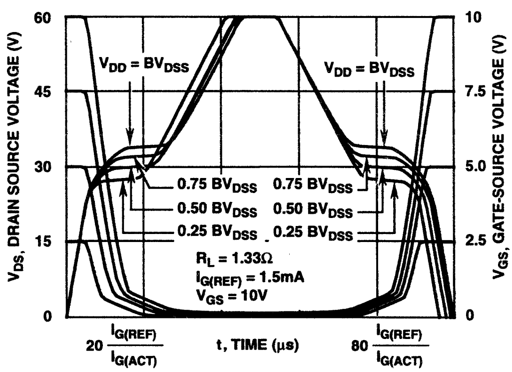


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

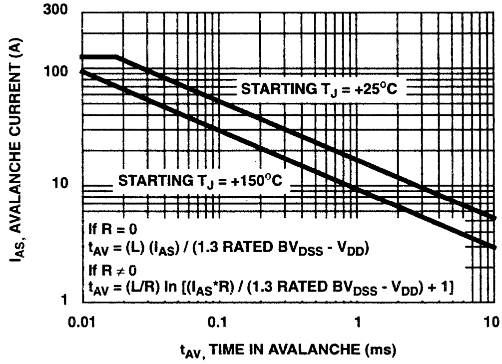


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

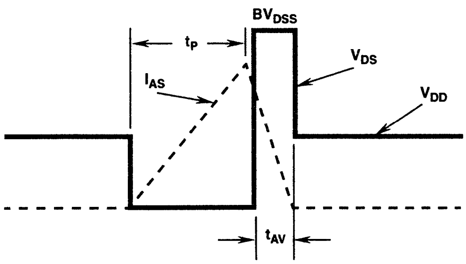


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

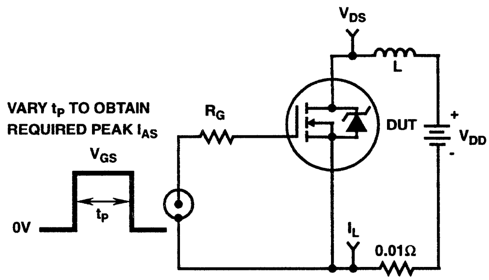


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

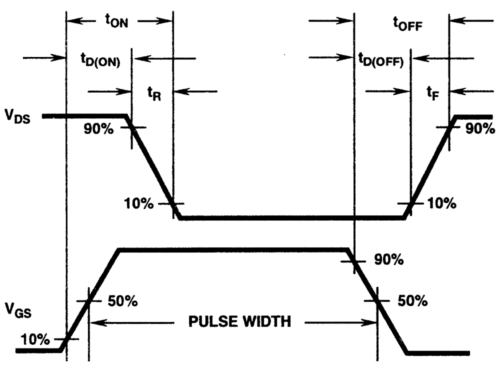


FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

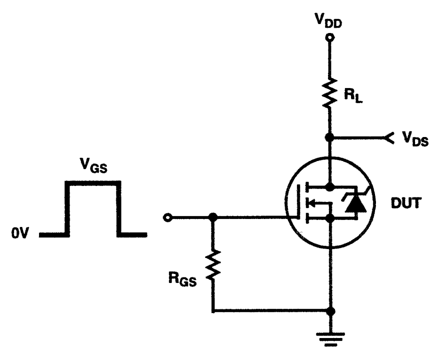


FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

3
N-CHANNEL POWER MOSFETS

Temperature Compensated PSPICE Model for the RFG45N06, RFP45N06, RF1S45N06, RF1S45N06SM

.SUBCKT RFP45N06 2 1 3

REV 1/18/93

*NOM TEMP = +25°C

CA 12 8 3.49E-9
CB 15 14 3.8E-9
CIN 6 8 2E-9

DBODY 7 5 DBDMOD
DBREAK 5 11DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 66.5
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

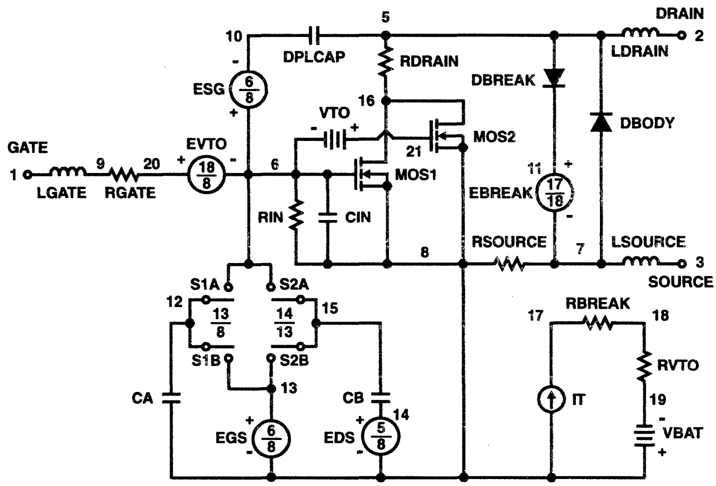
LDRAIN 2 5 1E-9
LGATE 1 9 5.65E-9
LSOURCE 3 7 4.13E-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 3.58E-3
RGATE 9 20 0.681
RIN 6 8 1E9
RSOURCE 8 7 RDSMOD 13.6E-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.92



.MODEL DBDMOD D (IS=8.2E-13 RS=7.86E-3 TRS1=2.26E-3 TRS2=2.90E-6 CJO=2.07E-9 TT=5.72E-8)
.MODEL DBKMOD D (RS=1.93E-1 TRS1=5.13E-4 TRS2=-2.15E-5)
.MODEL DPLCAPMOD D (CJO=1.25E-9 IS=1E-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.862 KP=55.57 IS=1E-30 N=10 TOX=1 L=1U W=1U)
.MODEL RBKMOD RES (TC1=1.12E-3 TC2=-5.18E-7)
.MODEL RDSMOD RES (TC1=4.64E-3 TC2=1.58E-5)
.MODEL RVTOMOD RES (TC1=-4.27E-3 TC2=-6.55E-6)
.MODEL S1AMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-6.5 VOFF=-1.7)
.MODEL S1BMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-1.7 VOFF=-6.5)
.MODEL S2AMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=-3.0 VOFF=2)
.MODEL S2BMOD VSWITCH (RON=1E-5 ROFF=0.1 VON=2.0 VOFF=-3.0)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options;** authors, William J. Hepp and C. Frank Wheatley.

RFG50N06, RFP50N06, RF1S50N06, RF1S50N06SM

HARRIS SEMICONDUCTOR

50A, 60V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 50A, 60V
- $r_{DS(ON)} = 0.022\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFG50N06, RFP50N06, RF1S50N06, and RF1S50N06SM N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

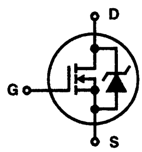
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFG50N06	TO-247	RFG50N06
RFP50N06	TO-220AB	RFP50N06
RF1S50N06	TO-262AA	F1S50N06
RF1S50N06SM	TO-263AB	F1S50N06

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S50N06SM9A.

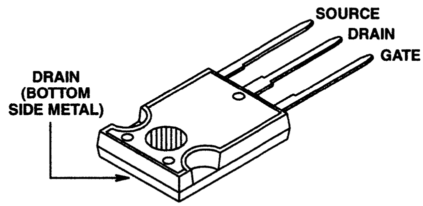
Formerly developmental type TA49018.

Symbol

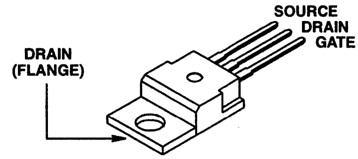


Packages

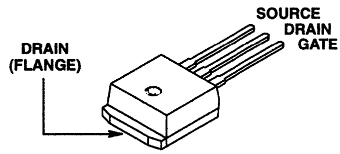
JEDEC STYLE TO-247



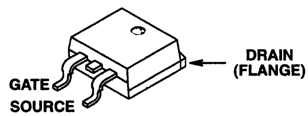
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = +25°C$

		RFG50N06, RFP50N06 RF1S50N06, RF1S50N06SM	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	50	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Maximum Avalanche Current	I_{AM}	125	A
Power Dissipation			
$T_C = +25°C$	P_D	131	W
Derate above +25°C	P_T	0.877	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	µA
			$T_C = +150^oC$	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 50A$, $V_{GS} = 10V$		-	-	0.022	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30V$, $I_D = 50A$, $R_L = 0.6\Omega$, $V_{GS} = +10V$, $R_{GS} = 3.6\Omega$		-	-	95	ns
Turn-On Delay Time	$t_{D(ON)}$			-	12	-	ns
Rise Time	t_R			-	55	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	37	-	ns
Fall Time	t_F			-	13	-	ns
Turn-Off Time	t_{OFF}			-	-	75	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0$ to $20V$	$V_{DD} = 48V$, $I_D = 50A$, $R_L = 0.96\Omega$	-	125	150	nC
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0$ to $10V$		-	67	80	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0$ to $2V$		-	3.7	4.5	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	2020	-	pF
Output Capacitance	C_{OSS}			-	600	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	200	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.14	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 50A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 50A$, $dI_{SD}/dt = 100A/\mu s$	-	-	125	ns

Typical Performance Curves

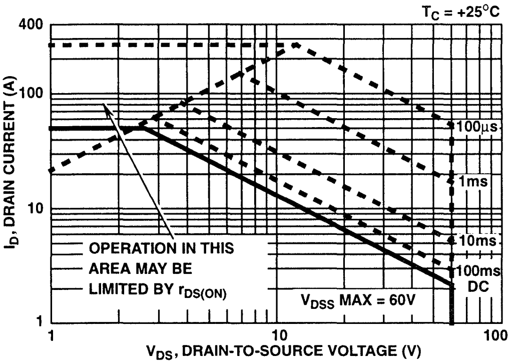


FIGURE 1. SAFE OPERATING AREA CURVE

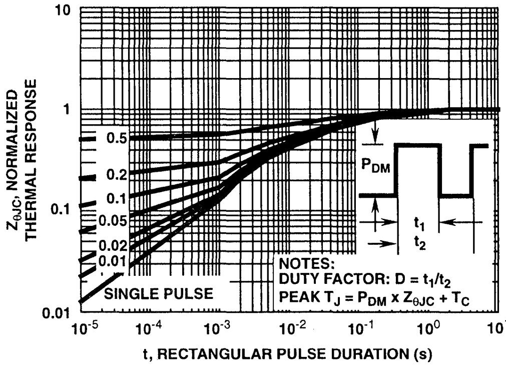


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

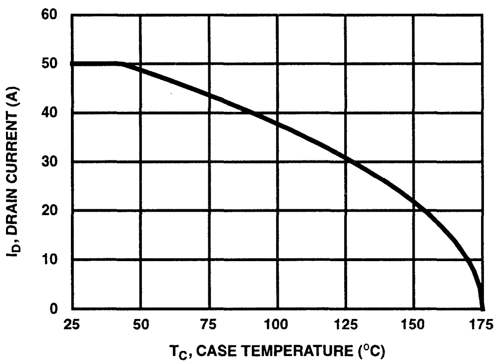


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

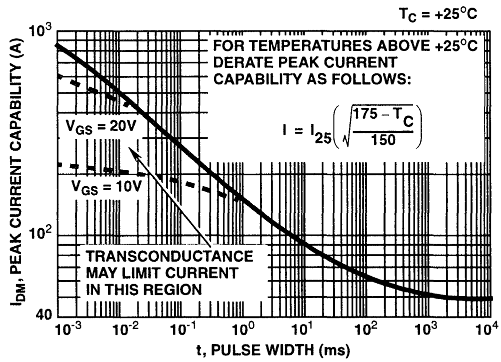


FIGURE 4. PEAK CURRENT CAPABILITY

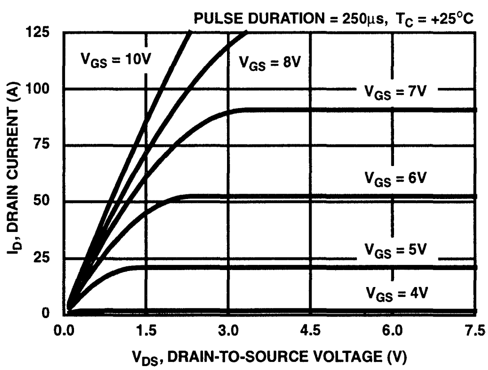


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

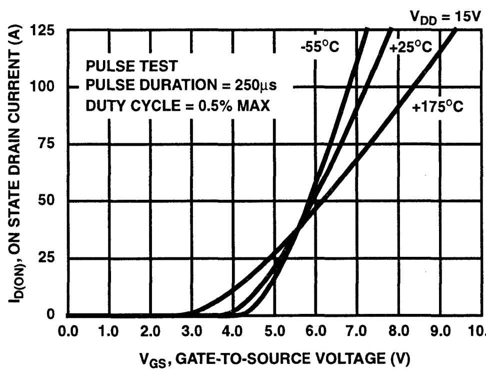


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

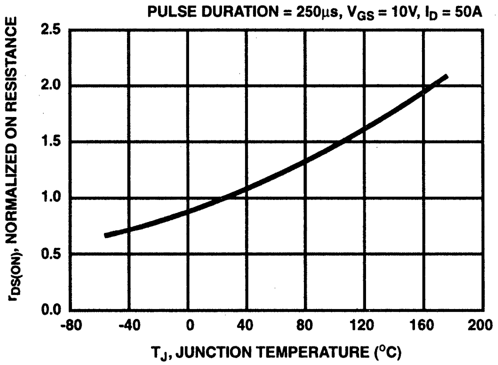


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

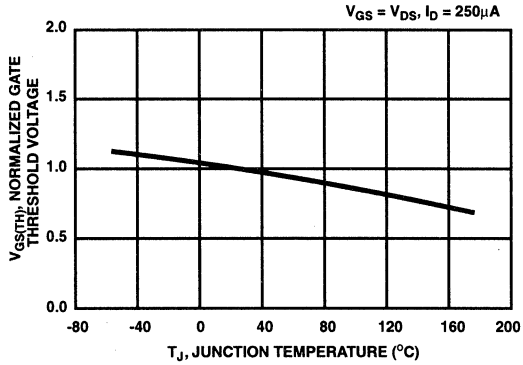


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

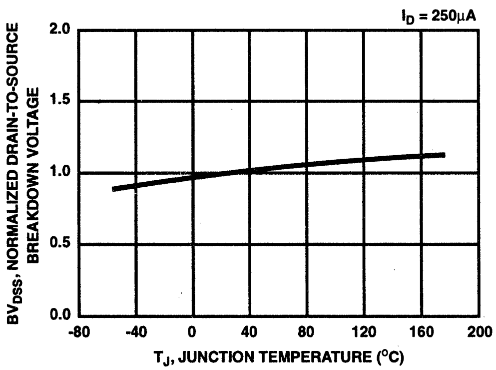


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

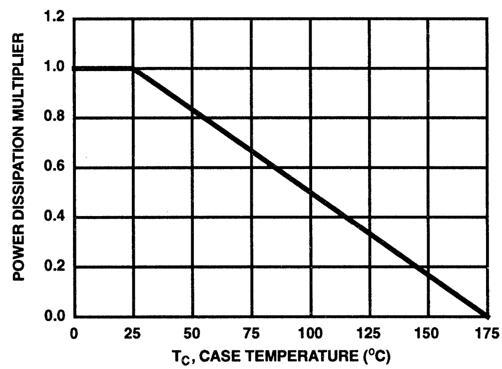


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

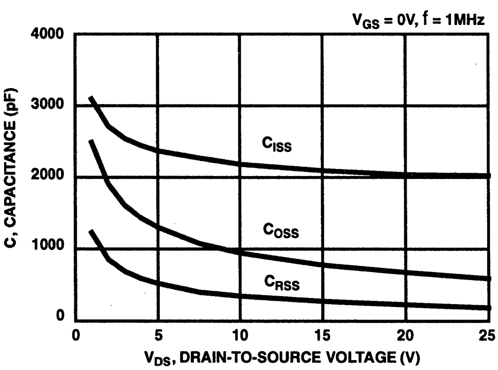


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

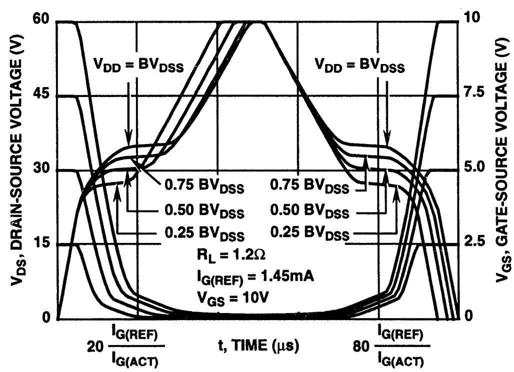


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

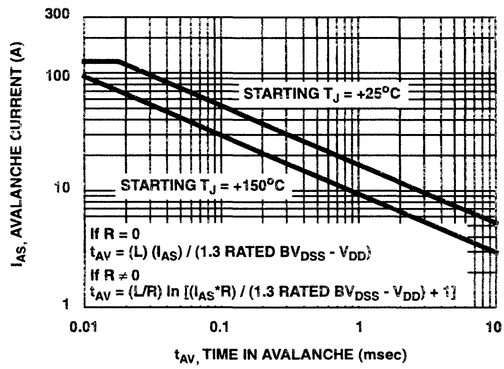


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

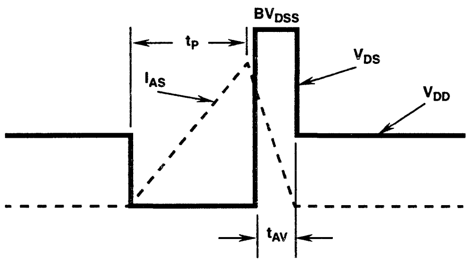


FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

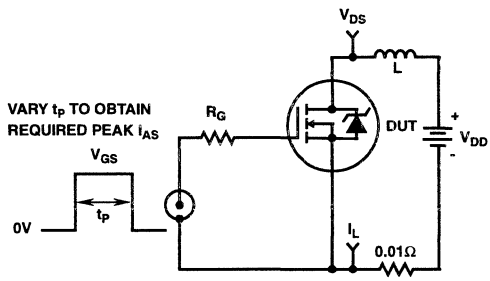


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

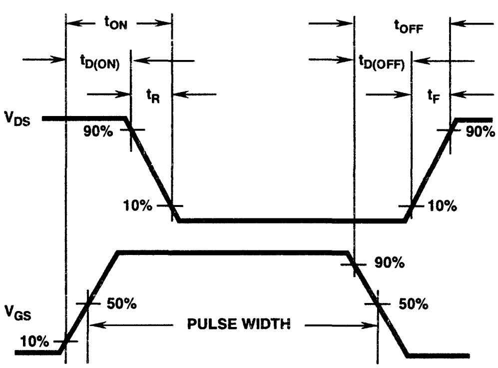


FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

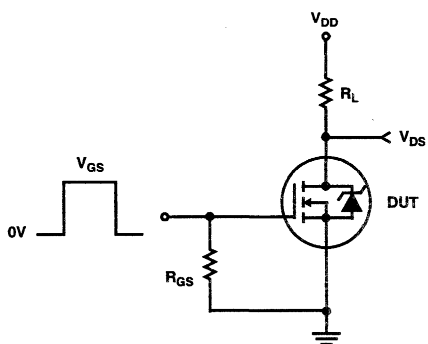


FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

Temperature Compensated PSPICE Model for the RFG50N06, RFP50N06, RF1S50N06, RF1S50N06SM

.SUBCKT RFP50N06 2 1 3
REV 2/22/93
* NOM TEMP = +25°C

CA 12 8 3.68e-9
CB 15 14 3.625e-9
CIN 6 8 1.98e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 64.59
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

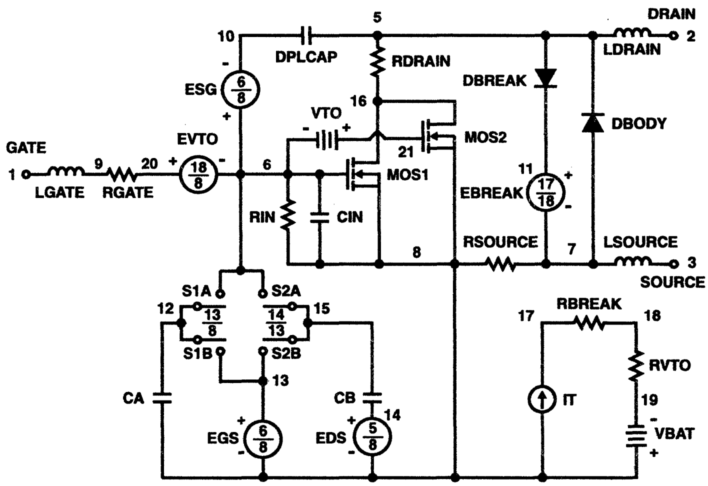
LDRAIN 2 5 1e-9
LGATE 1 9 5.65e-9
LSOURCE 3 7 4.13e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 1e-4
RGATE 9 20 0.690
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 12e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.678



.MODEL DBDMOD D (IS=9.851e-13 RS=4.91e-3 TRS1=2.07e-3 TRS2=2.51e-7 CJO=2.05e-9 TT=4.33e-8)
.MODEL DBKMOD D (RS=1.98e-1 TRS1=-2.35e-3 TRS2=-3.83e-6)
.MODEL DPLCAPMOD D (CJO=1.42e-9 IS=1e-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.65 KP=35 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=1.23e-3 TC2=-2.34e-6)
.MODEL RDSMOD RES (TC1=5.01e-3 TC2=1.49e-5)
.MODEL RVTOMOD RES (TC1=-5.03e-3 TC2=-5.16e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.75 VOFF=-2.5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.5 VOFF=-6.75)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.7 VOFF=2.3)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=2.3 VOFF=-2.7)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authors, William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFP70N03, RF1S70N03, RF1S70N03SM

70A, 30V, Avalanche Rated N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 70A, 30V
- $r_{DS(ON)} = 0.010\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve (Single Pulse)
- +175°C Operating Temperature

Description

The RFP70N03, RF1S70N03, and RF1S70N03SM N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

PACKAGE AVAILABILITY

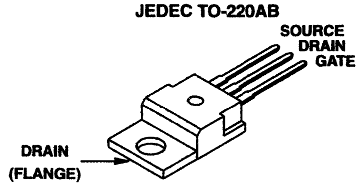
PART NUMBER	PACKAGE	BRAND
RFP70N03	TO-220AB	RFP70N03
RF1S70N03	TO-262AA	F1S70N03
RF1S70N03SM	TO-263AB	F1S70N03

NOTE: When ordering use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, e.g. RF1S70N03SM9A.

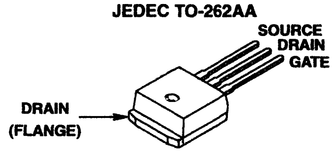
Formerly developmental type TA49025.

Packages

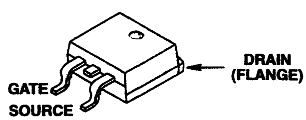
JEDEC TO-220AB



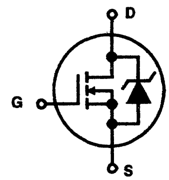
JEDEC TO-262AA



JEDEC TO-263AB



Symbol



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		RFP70N03, RF1S70N03, RF1S70N03SM	UNITS
Drain-Source Voltage	V_{DSS}	30	V
Drain-Gate Voltage	V_{DGR}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current			
RMS Continuous	I_D	70	A
Pulsed Drain Current	I_{DM}	200	A
Single Pulse Avalanche Rating	E_{AS}	(Refer to UIS Curve)	
Power Dissipation			
$T_C = +25^oC$	P_D	150	W
Above $T_C = +25^oC$, Derate Linearly	P_T	1.0	W/°C
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number 3404.2

Electrical Specifications At Case Temperature (T_C) = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V	T_C = 25°C	-	-	1	μA
		V_{GS} = 0V	T_C = 150°C	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 70A, V_{GS} = 10V		-	-	0.010	Ω
Turn-On Time	t_{ON}	V_{DD} = 15V, I_D = 70A		-	-	80	ns
Turn-On Delay Time	$t_{D(ON)}$	R_L = 0.214Ω, V_{GS} = +10V		-	20	-	ns
Rise Time	t_R	R_{GS} = 2.5Ω		-	20	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	40	-	ns
Fall Time	t_F			-	25	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to 20V	V_{DD} = 24V, I_D = 70A, R_L = 0.343Ω	-	215	260	nC
Gate Charge at 10V	$Q_{G(10)}$	V_{GS} = 0 to 10V		-	120	145	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0 to 2V		-	6.5	8.0	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V		-	3300	-	pF
Output Capacitance	C_{OSS}	f = 1MHz		-	1750	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	750	-	pF
Thermal Resistance Junction to Case	$R_{θJC}$			-	-	1.0	°C/W
Thermal Resistance Diode Junction to Ambient	$R_{θJA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Diode Forward Voltage	V_{SD}	I_{SD} = 70A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 70A, dI_{SD}/dt = 100A/μs	-	-	125	ns

Typical Performance Curves

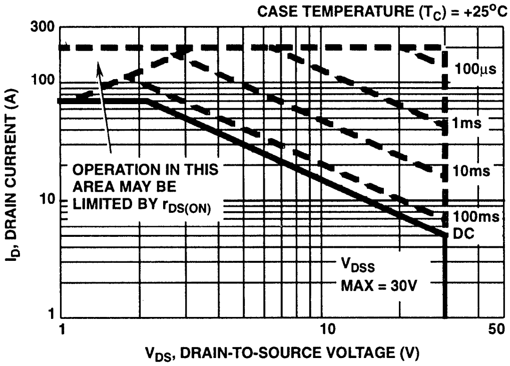


FIGURE 1. SAFE-OPERATING AREA CURVE

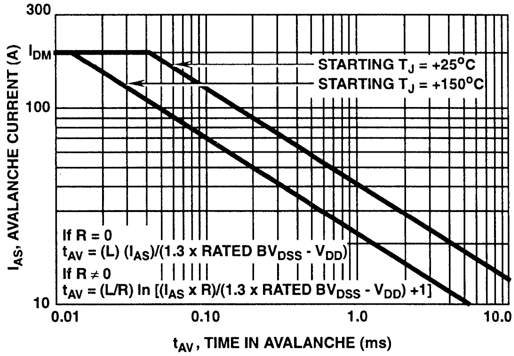


FIGURE 2. UNCLAMPED INDUCTIVE-SWITCHING

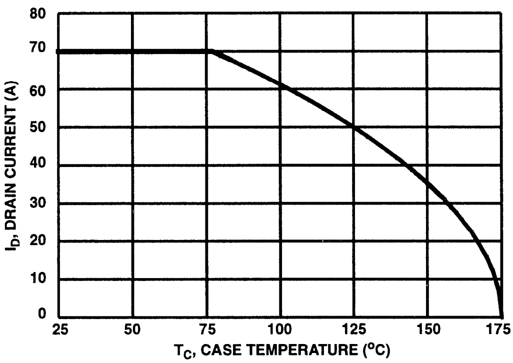


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

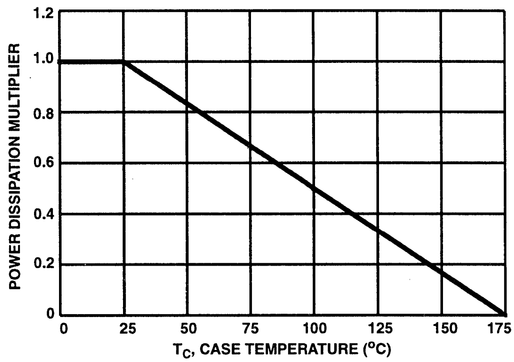


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

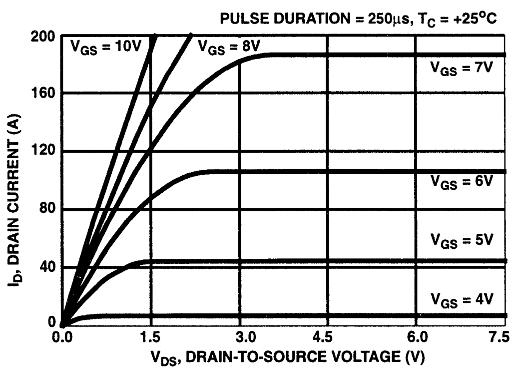


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

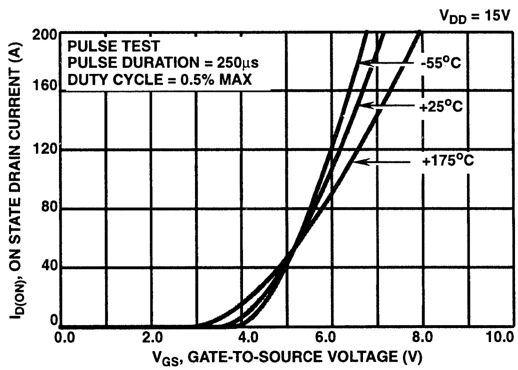


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

3
N-CHANNEL POWER MOSFETs

Typical Performance Curves (Continued)

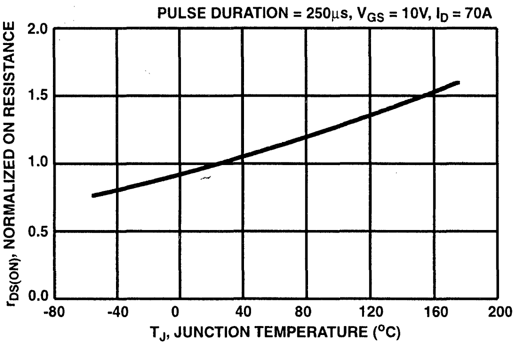


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

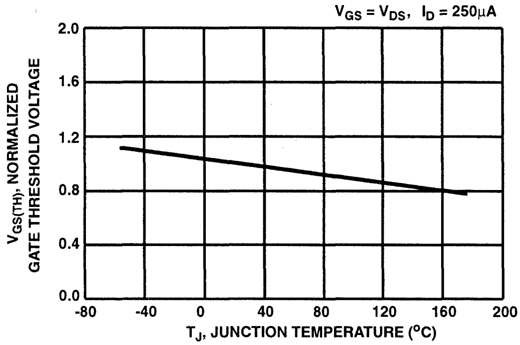


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

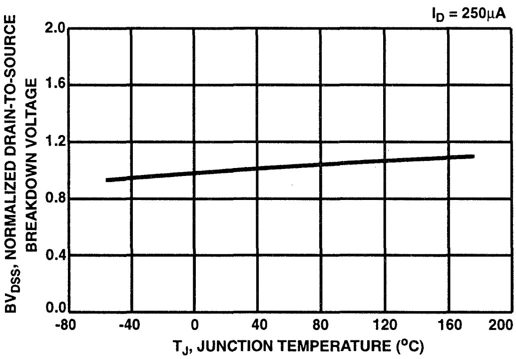


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

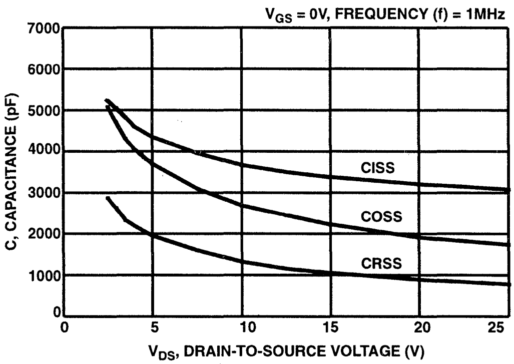


FIGURE 10. TYPICAL CAPACITANCE vs VOLTAGE

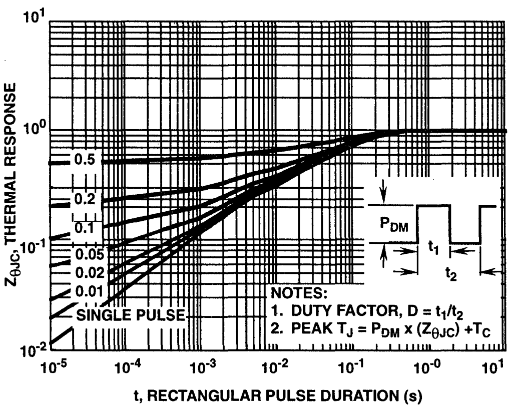


FIGURE 11. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

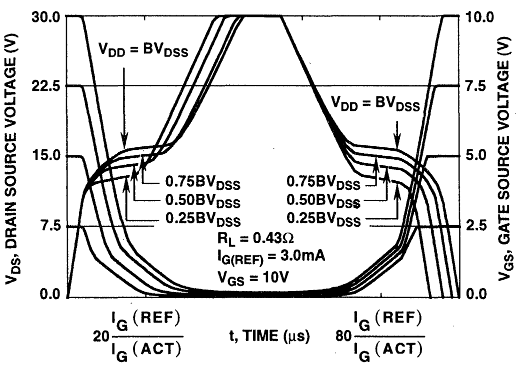


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Test Circuits and Waveforms

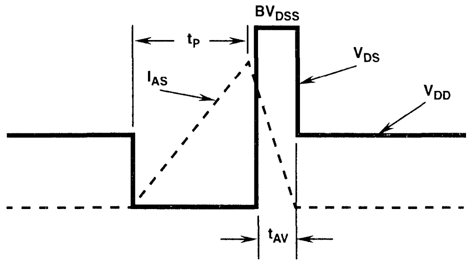


FIGURE 13. UNCLAMPED ENERGY WAVEFORMS

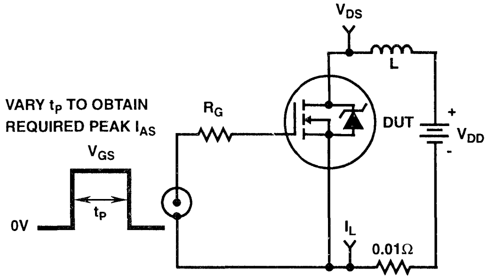


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

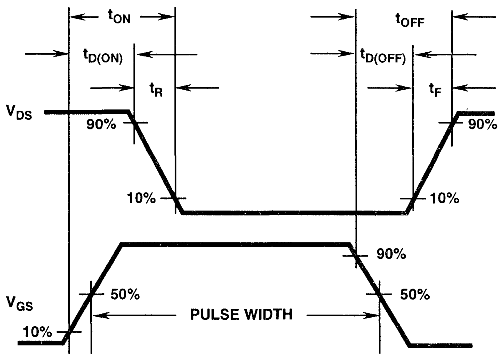


FIGURE 15. RESISTIVE SWITCHING WAVEFORMS

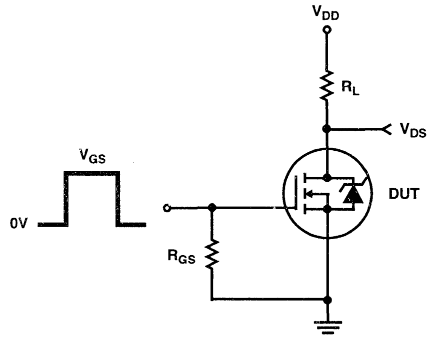


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

PSPICE Model for the RFP70N03, RF1S70N03, RF1S70N03SM

.SUBCKT RFP70N03 2 1 3 ; rev 9/16/92
*NOM TEMP = 25°C

CA 12 8 6.09e-9
CB 15 14 6.05e-9
CIN 6 8 3.40e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 35.4
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

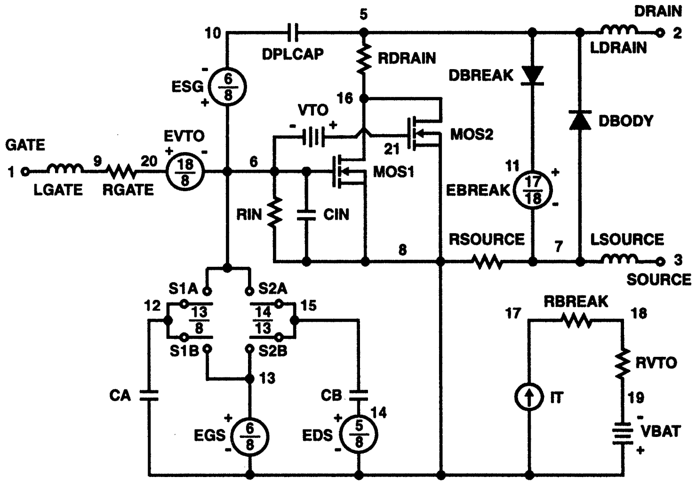
LDRAIN 2 5 1e-9
LGATE 1 9 3.10e-9
LSOURCE 3 7 1.82e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 30.7e-6
RGATE 9 20 0.890
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 3.92e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.605



.MODEL DBDMOD D (IS=7.91e-12 RS=3.87e-3 TRS1=2.71e-3 TRS2=2.50e-7 CJO=4.84e-9 TT=4.51e-8)
.MODEL DBKMOD D (RS=3.9e-2 TRS1=1.05e-4 TRS2=3.11e-5)
.MODEL DPLCAPMOD D (CJO=4.8e-9 IS=1e-30 N=10)
.MODEL MOSMOD NMOS (VTO=3.46 KP=47 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=8.46e-4 TC2=-8.48e-7)
.MODEL RDSMOD RES (TC1=2.23e-3 TC2=6.56e-6)
.MODEL RVTOMOD RES (TC1=-3.29e-3 TC2=3.49e-7)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-8.35 VOFF=-6.35)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-6.35 VOFF=-8.35)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.0 VOFF=3.0)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.0 VOFF=-2.0)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

RFG70N06, RFP70N06, RF1S70N06, RF1S70N06SM

70A, 60V, Avalanche Rated, N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 70A, 60V
- $r_{DS(on)} = 0.014\Omega$
- *Temperature Compensated* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve (Single Pulse)
- +175°C Operating Temperature

Description

The RFG70N06, RFP70N06, RF1S70N06 and RF1S70N06SM are N-channel power MOSFETs manufactured using the Mega-FET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

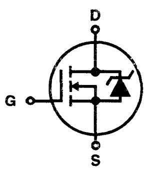
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFG70N06	TO-247	RFG70N06
RFP70N06	TO-220AB	RFP70N06
RF1S70N06	TO-262AA	F1S70N06
RF1S70N06SM	TO-263AB	F1S70N06

NOTE: When ordering use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, e.g. RF1S70N06SM9A.

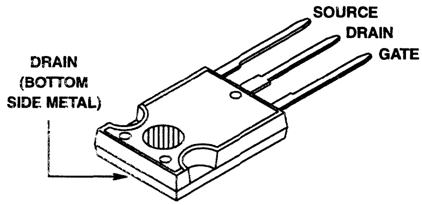
Formerly developmental type TA49007.

Symbol

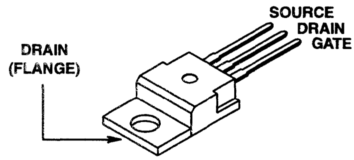


Packages

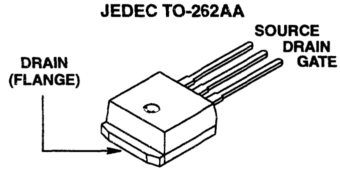
JEDEC STYLE TO-247



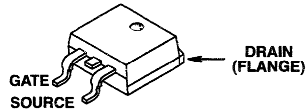
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = +25^oC$, Unless Otherwise Specified

		RFG70N06, RFP70N06 RF1S70N06, RF1S70N06SM	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	70	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	150	W
Derate above +25°C		1.0	W/°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

File Number **3206.3**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		2	-	4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	µA
			$T_C = +150^oC$	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 70A$, $V_{GS} = 10V$		-	-	0.014	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30V$, $I_D = 70A$ $R_L = 0.43\Omega$, $V_{GS} = +10V$ $R_{GS} = 2.5\Omega$		-	-	125	ns
Turn-On Delay Time	$t_{D(ON)}$			-	12	-	ns
Rise Time	t_R			-	50	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	40	-	ns
Fall Time	t_F			-	15	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $20V$	$V_{DD} = 48V$, $I_D = 70A$, $R_L = 0.68\Omega$	-	185	215	nC
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0V$ to $10V$		-	100	115	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $2V$		-	5.5	6.5	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$ f = 1MHz		-	3000	-	pF
Output Capacitance	C_{OSS}			-	900	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	300	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.0	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 70A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 70A$, $dI_{SD}/dt = 100A/\mu s$	-	-	125	ns

Typical Performance Curves

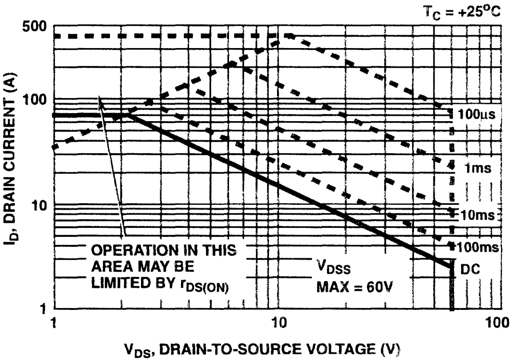


FIGURE 1. SAFE OPERATING AREA CURVE

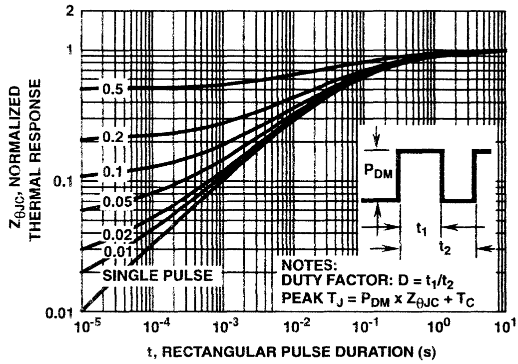


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

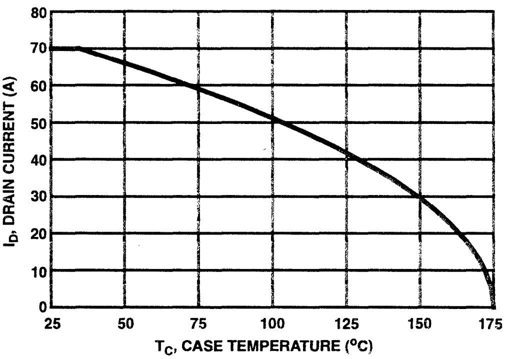


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

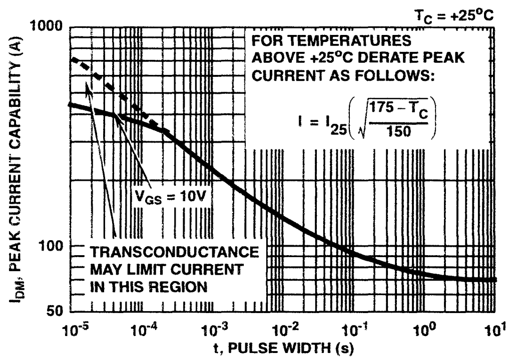


FIGURE 4. PEAK CURRENT CAPABILITY

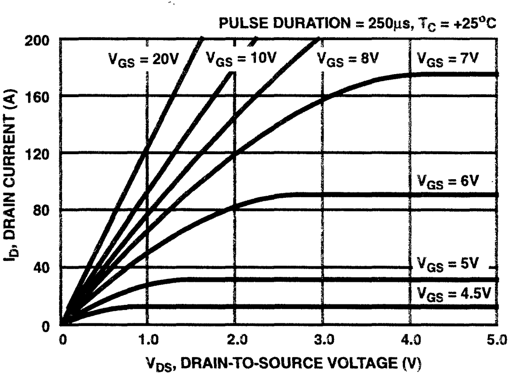


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

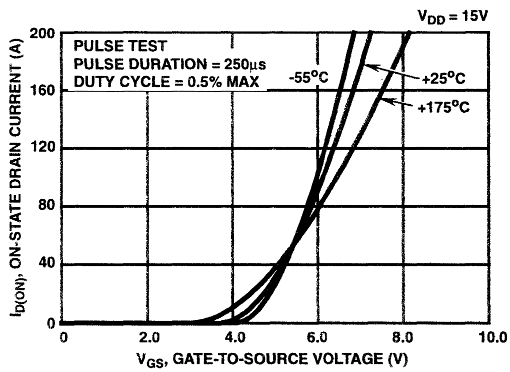


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

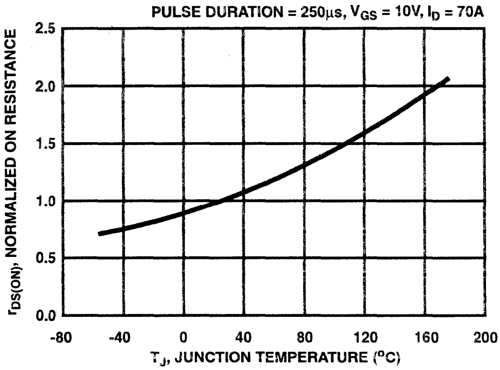


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

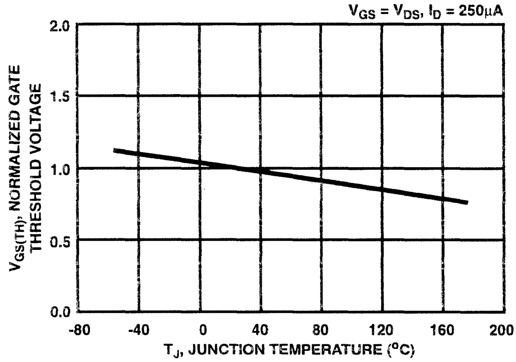


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

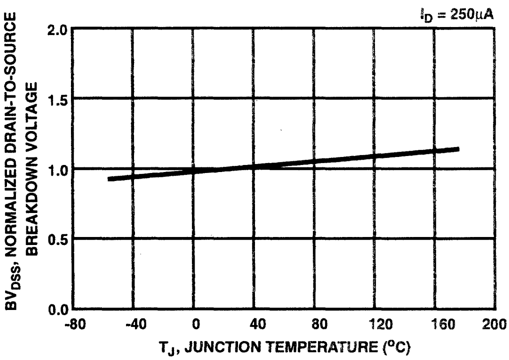


FIGURE 9. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

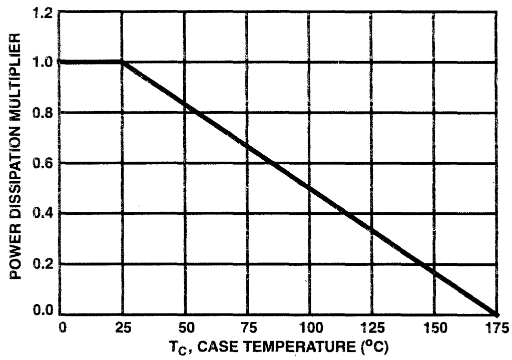


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

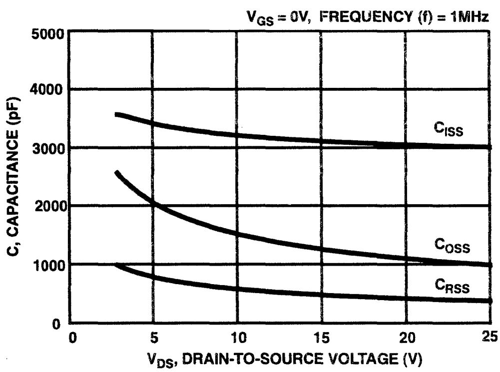


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

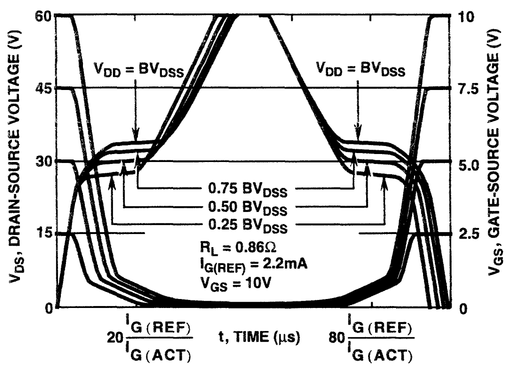


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

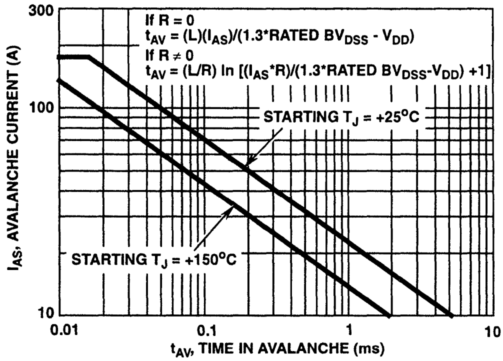


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

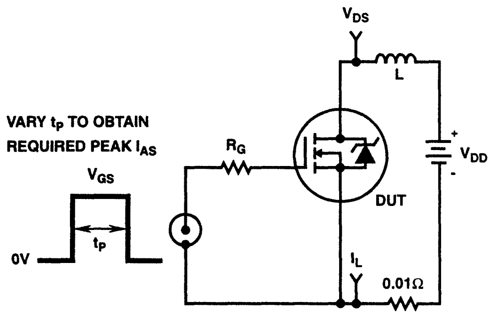


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

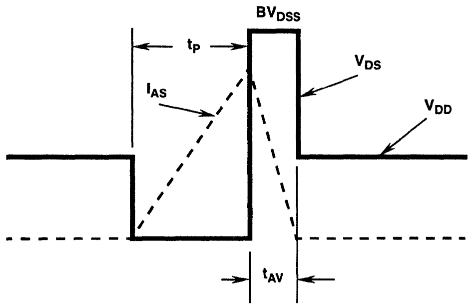


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

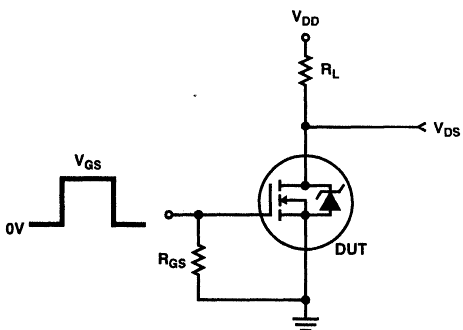


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

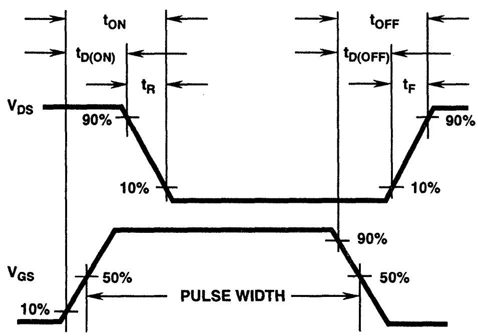


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFG70N06, RFP70N06, RF1S70N06, RF1S70N06SM

```
.SUBCKT RFG70N06 2 1 3 ;     rev 3/20/92

CA 12 8 5.56e-9
CB 15 14 5.30e-9
CIN 6 8 2.63e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 65.18
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

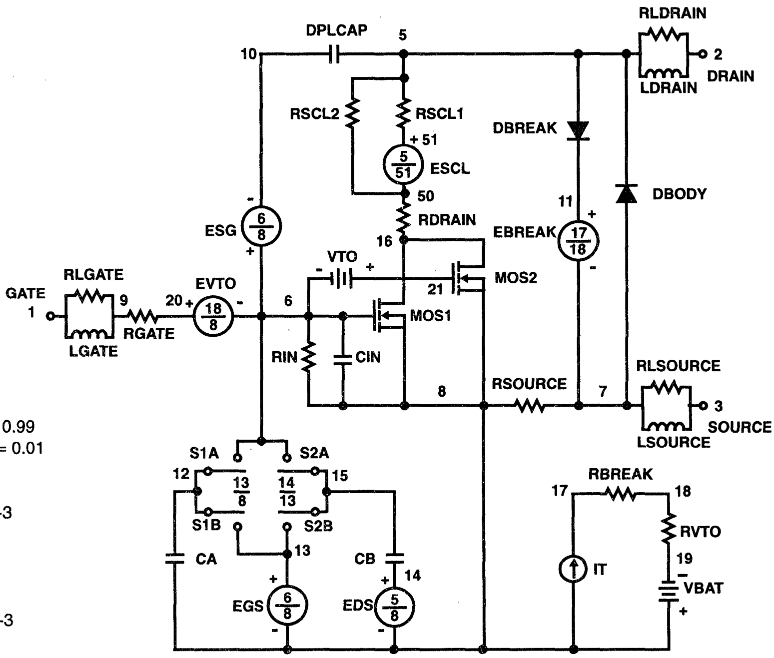
LDRAIN 2 5 1e-9
LGATE 1 9 3.10e-9
LSOURCE 3 7 1.82e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 4.66e-3
RLDRAIN 2 5 10
RGATE 9 20 1.21
RLGATE 1 9 31
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 3.92e-3
RLSOURCE 3 7 18.2
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.605
```




```
.MODEL DBDMOD D (IS = 7.91e-12 RS = 3.87e-3 TRS1 = 2.71e-3 TRS2 = 2.50e-7 CJO = 4.84e-9 TT = 4.51e-8)
.MODEL DBKMOD D (RS = 3.9e-2 TRS1 =1.05e-4 TRS2 = 3.11e-5)
.MODEL DPLCAPMOD D (CJO = 4.8e-9 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 3.46 KP = 47 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 8.46e-4 TC2 = -8.48e-7)
.MODEL RDSMOD RES (TC1 = 2.23e-3 TC2 = 6.56e-6)
.MODEL RVTOMOD RES (TC1 = -3.29e-3 TC2 = 3.49e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -8.35 VOFF= -6.35)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.35 VOFF= -8.35)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.0 VOFF= 3.0)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 3.0 VOFF= -2.0)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFF70N06

25A†, 60V, Hermetically Packaged, Avalanche Rated N-Channel Enhancement-Mode Power MOSFET

December 1995

Features

- 25A†, 60V
- $r_{DS(ON)} = 0.025\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +150°C Operating Temperature
- Reliability Screened

Description

The RFF70N06 N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Reliability screening is available as either commercial or TX/TXV equivalent of MIL-S-19500. Contact Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFF70N06	TO-254AA	RFF70N06

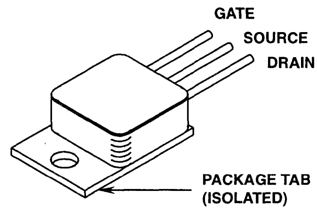
When ordering, use the entire part number.

Formerly developmental type TA49007.

Commercial Version: RFG70N06.

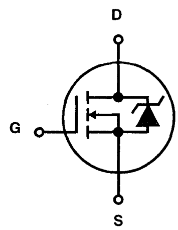
Package

JEDEC TO-254AA



CAUTION: Beryllia Warning per MIL-S-19500 refer to package specifications.

Symbol



Absolute Maximum Ratings $T_C = +25°C$

		RFF70N06	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	25†	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25°C$	P_D	100	W
Derate above +25°C		0.80	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	°C
Lead Temperature (During Soldering) (Distance >0.063in. (1.6mm) from Case, 10s Max.)	T_L	300	°C

† Current is limited by the package capability.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4073.1**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		2.0	3.0	4.5	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48V$,	$T_C = +25^oC$	-	-	25	µA
		$V_{GS} = 0V$	$T_C = +125^oC$	-	-	250	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$	$T_C = +25^oC$	-	-	100	nA
			$T_C = +125^oC$	-	-	100	µA
On Resistance	$r_{DS(ON)}$	$I_D = 25A$, $V_{GS} = 10V$		-	-	0.025	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30V$, $I_D = 25A$		-	-	240	ns
Turn-On Delay Time	$t_{D(ON)}$	$R_L = 1.2\Omega$, $V_{GS} = 10V$		-	25	70	ns
Rise Time	t_R	$R_{GS} = 2.35\Omega$		-	70	170	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	60	150	ns
Fall Time	t_F			-	25	65	ns
Turn-Off Time	t_{OFF}			-	-	215	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0$ to $20V$	$V_{DD} = 30V$,	-	-	260	nC
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0$ to $10V$	$I_D = 25A$,	-	-	145	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0$ to $2V$	$R_L = 1.2\Omega$	-	-	7	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$		-	3100	-	pF
Output Capacitance	C_{OSS}	f = 1MHz		-	900	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	300	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.25	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	48	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 25A$	-	1.1	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 25A$, $dI_{SD}/dt = 100A/\mu s$	-	190	300	ns

Typical Performance Curves

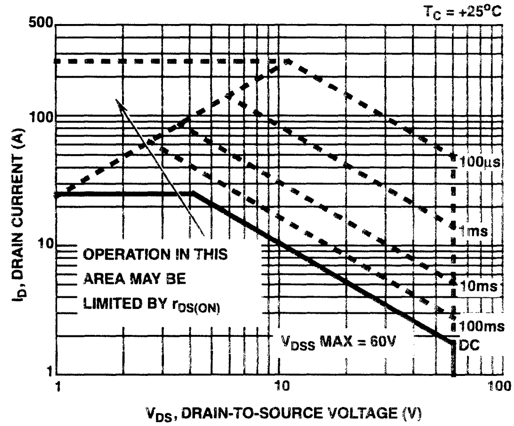


FIGURE 1. SAFE OPERATING AREA CURVE

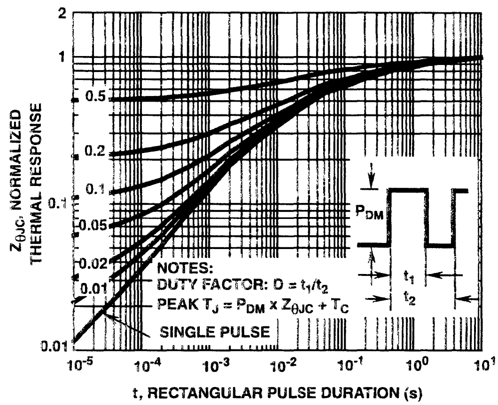


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

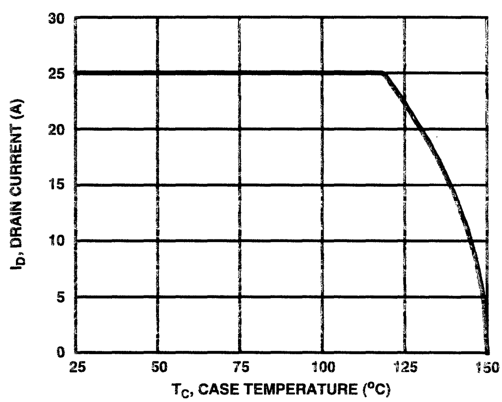


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

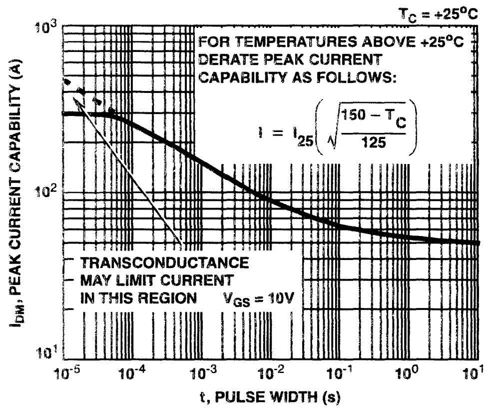


FIGURE 4. PEAK CURRENT CAPABILITY

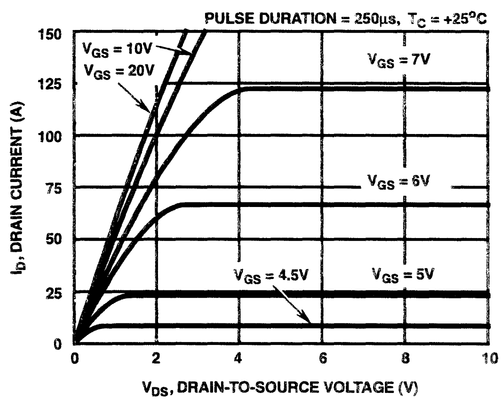


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

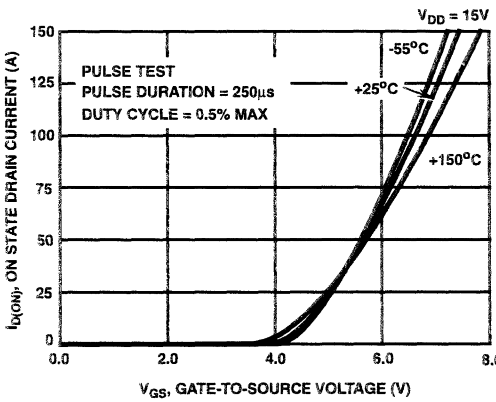


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

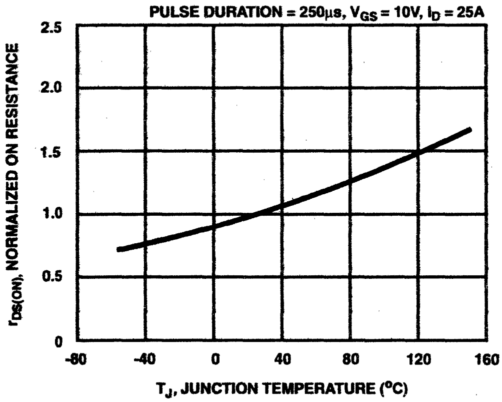


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

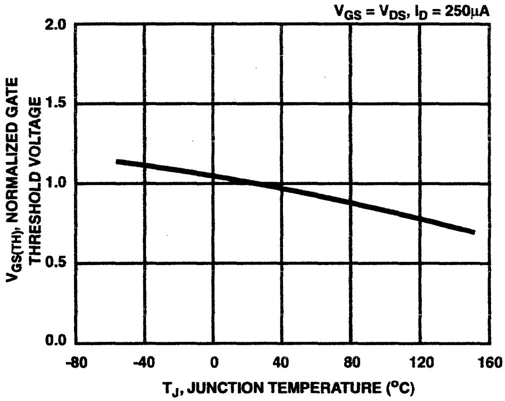


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

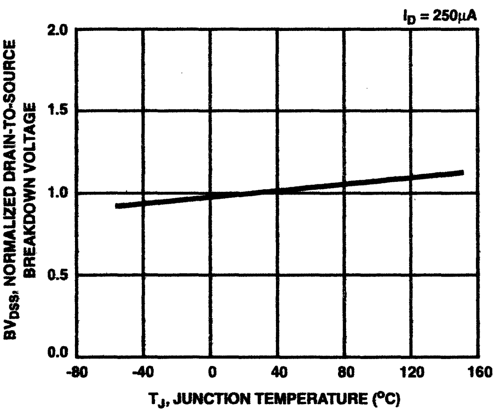


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

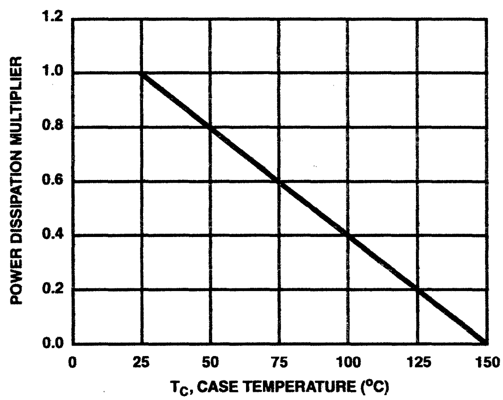


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

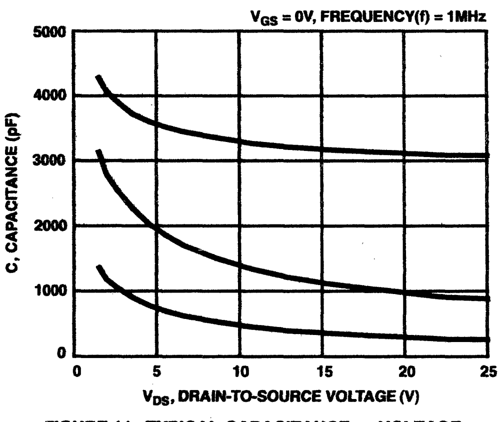


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

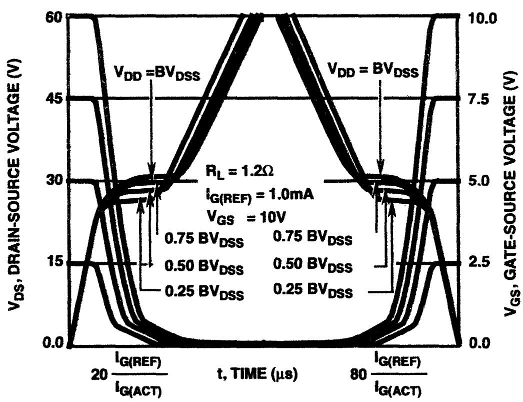


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

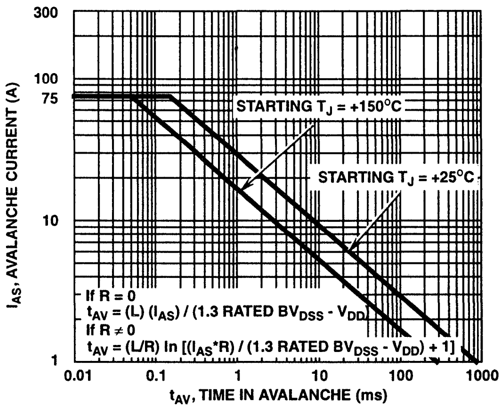


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

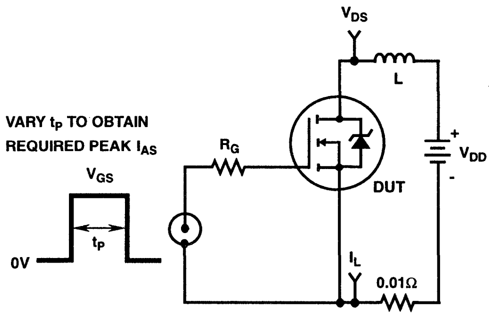


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

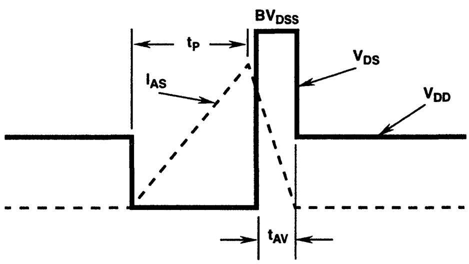


FIGURE 15. UNCLAMPED ENERGY WAVEFORM

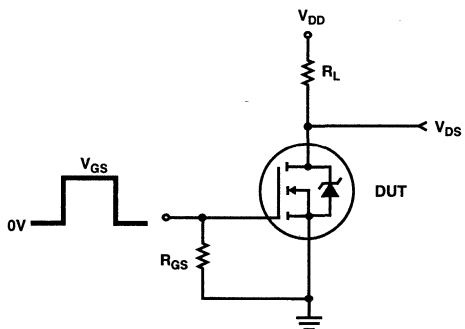


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

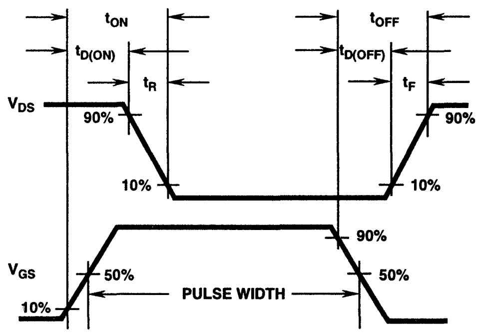


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

3

N-CHANNEL POWER MOSFETs

Test Circuits and Waveforms (Continued)

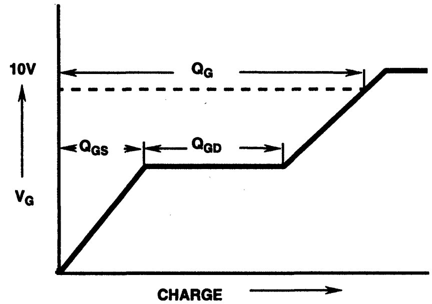


FIGURE 18. BASIC GATE CHARGE WAVEFORM

Temperature Compensated PSPICE Model for the RFF70N06

```
SUBCKT RFF70N06 2 1 3 ;     rev 5/29/95

CA 12 8 5.20e-9
CB 15 14 5.20e-9
CIN 6 8 2.80e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 68.7
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRESH 6 21 19 8 1
EZTEMPCO 20 6 18 22 1

IT 8 17 1

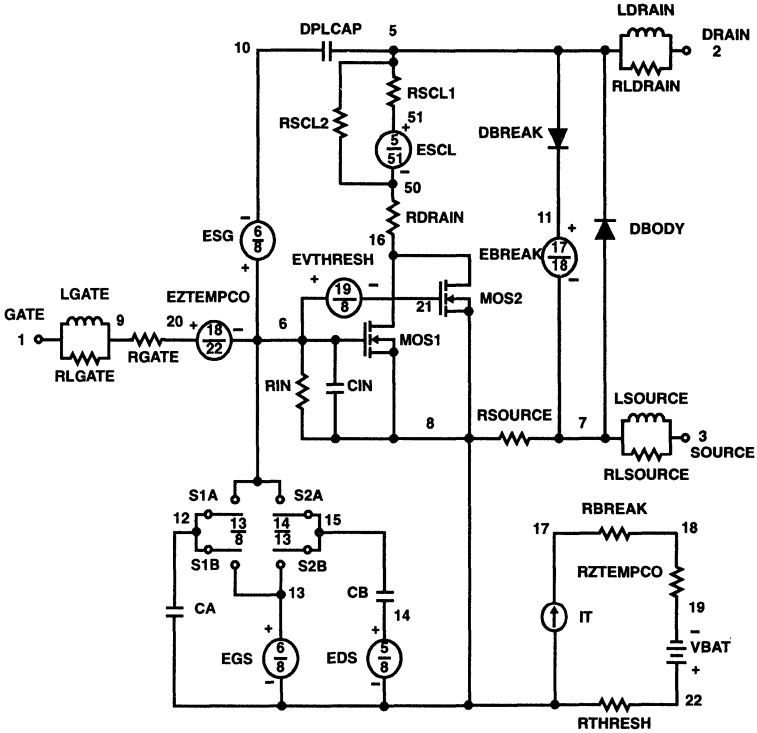
LDRAIN 2 5 1e-9
LGATE 1 9 6.04e-9
LSOURCE 3 7 2.24e-9

MOS1 16 6 8 8 MSTRONG M = 0.9
MOS2 16 21 8 8 MWEAK M = 0.01

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 8.03e-3
RGATE 9 20 1
RIN 6 8 1e9
RLDRAIN 2 5 10
RLGATE 1 9 60.4
RLSOURCE 3 7 22.4
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 7.20
RTHRESH 22 8 RTHRESMOD 1
RZTEMPCO 18 19 RZTEMPCOMOD

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1
```




```
ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*250),3))}

.MODEL DBDMOD D (IS = 1e-12 RS = 11.01e-3 TRS1 = 1.75e-3 TRS2 = -0.06e-6 CJO = 2.70e-9 TT = 7.82e-8 M = 0.45)
.MODEL DBREAKMOD D (RS = 88e-3 TRS1 = 1.50e-3 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 2.60e-9 IS = 1e-30 N = 10 M=0.7)
.MODEL MSTRONG NMOS (VTO = 3.85 KP = 47.2 IS = 1e-30 N = 10 TOX = 1L = 1u W = 1u)
.MODEL MWEAK NMOS (VTO = 3.09 KP = 47.2 IS = 1e-30 N = 10 TOX = 1L = 1u W = 1u)
.MODEL RBREAKMOD RES (TC1 = 1e-3 TC2 = 0)
.MODEL RDRAINMOD RES (TC1 = 7e-3 TC2 = 1.90e-5)
.MODEL RDSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RSCLMOD RES (TC1 = 0 TC2 = 0)
.MODEL RTHRESHMOD RES (TC1 = -3.10e-3 TC2 = -1e-5)
.MODEL RZTEMPCOMOD RES (TC1 = -2.25e-3 TC2 = -5.75e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.0 VOFF= -4.0)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.0 VOFF= -6.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.0 VOFF= 2.0)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.0 VOFF= -2.0)

.ENDS
```

NOTE:

1. For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.

Screening Information

Screening is performed in accordance with the latest revision in effect of MIL-S-19500, (Screening Information Table).

Delta Tests and Limits (JANTX/JANTXV Equivalent)

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$, $T_C = 25^oC$	±20 (Note 1)	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80% Rated Value, $T_C = 25^oC$	±25 (Note 1)	μA
On Resistance	$r_{DS(ON)}$	$T_C = +125^oC$ at Rated I_D	±20% (Note 2)	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	$I_D = 1.0mA$, $T_C = 25^oC$	±20% (Note 2)	V

NOTES:

1. Or 100% of Initial Reading (whichever is greater)
2. Of Initial Reading

Screening Information

TEST	JANTX/JANTXV EQUIVALENT
Gate Stress	$V_{GS} = 30V$, $t = 250\mu s$
Pind	Optional
PDA	10%
Pre Burn-in Test (Note 1)	MIL-S-19500 Group A, Subgroup 2 (All Static Tests at 25°C)
Steady State Gate Bias (Gate Stress)	MIL-STD-750, Method 1042, Condition B V_{GS} = 80% of Rated Value, $T_A = 150^oC$, Time = 48 hours
Interim Electrical Tests (Note 1)	All Delta Parameters Listed in the Delta Tests and Limits Table
Steady State Reverse Bias (Drain Stress)	MIL-STD-750, Method 1042, Condition A V_{DS} = 80% of Rated Value, $T_A = 150^oC$, Time = 168 hours
Final Electrical Tests (Note 1)	MIL-S-19500, Group A, Subgroup 2

NOTE:

1. Test limits are identical pre and post burn-in.

Additional Screening Tests

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safe Operating Area	SOA	$V_{DS} = 48V$, $t = 10ms$	4.8	A
Unclamped Inductive Switching	I_{AS}	$V_{GS(PEAK)} = 15V$, $L = 0.1mH$	75	A
Thermal Response	ΔV_{SD}	$t_H = 100ms$; $V_H = 25V$; $I_H = 4A$	220	mV
Thermal Impedance	ΔV_{SD}	$t_H = 500ms$; $V_H = 25V$; $I_H = 4A$	330	mV

Data Packages - Harris Power Transistors

TX and TXV Equivalents

1. TX/TXV Equivalent - Standard Data Package
   - A. Certificate of Compliance
   - B. Assembly Flow Chart
   - C. Preconditioning - Attributes Data Sheet
   - D. Group A - Attributes Data Sheet
   - E. Group B - Attributes Data Sheet
   - F. Group C - Attributes Data Sheet

2. TX/TXV Equivalent - Optional Data Package
   - A. Certificate of Compliance
   - B. Assembly Flow Chart
   - C. Preconditioning
     - Attributes Data Sheet
     - Precondition Lot Traveler
     - Pre and Post Burn-In Read and Record Data
   - D. Group A
     - Attributes Data Sheet
     - Group A Lot Traveler
   - E. Group B
     - Attributes Data Sheet
     - Group B Lot Traveler
     - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup B3)
     - Bond Strength Data (Subgroup B3)
     - Pre and Post High Temperature Operating Life Read and Record Data (Subgroup B6)
   - F. Group C
     - Attributes Data Sheet
     - Group C Lot Traveler
     - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup C6)
     - Bond Strength Data (Subgroup C6)

POWER MOSFETs 4

P-CHANNEL POWER MOSFETs

HARRIS SEMICONDUCTOR IRFU9110, IRFR9110

3.1A, 100V, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 3.1A, 100V
- $r_{DS(ON)} = 1.200\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The IRFU9110 and IRFR9110 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specific level of energy in the avalanche breakdown mode of operation. These are P-Channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

PACKAGING AVAILABILITY

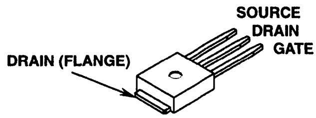
PART NUMBER	PACKAGE	BRAND
IRFU9110	TO-251AA	IF9110
IRFR9110	TO-252AA	IF9110

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., IRFR91109A.

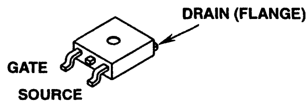
Formerly developmental type TA17541.

Packaging

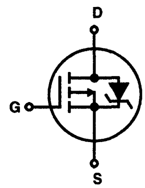
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		IRFU9110, IRFR9110	UNITS
Drain Source Voltage	V_{DSS}	-100	V
Drain Gate Voltage	V_{DGR}	-100	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	3.1	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	25	W
Derate above $+25^oC$		0.2	$W/^oC$
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	^oC
Soldering Temperature of Leads for 10s	T_L	260	^oC

4 P-CHANNEL POWER MOSFETs

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4001.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		-100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -100V, V_{GS} = 0V	T_C = +25°C	-	-	-1	μA
			T_C = +150°C	-	-	-50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 1.9A, V_{GS} = -10V		-	-	1.200	Ω
Turn-On Time	t_{ON}	V_{DD} = -50V, I_D = 4A, R_L = 11Ω, V_{GS} = -10V, R_{GS} = 24Ω		-	-	50	ns
Turn-On Delay Time	$t_{D(ON)}$			-	10	-	ns
Rise Time	t_R			-	27	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	15	-	ns
Fall Time	t_F			-	17	-	ns
Turn-Off Time	t_{OFF}			-	-	50	ns
Total Gate Charge	Q_G	V_{GS} = 0 to -10V	V_{DD} = -80V, I_D = 3.1A, R_L = 25.8Ω	-	-	8.7	nC
Gate-to-Drain Charge	Q_{GD}			-	-	4.1	nC
Gate-to-Source Charge	Q_{GS}			-	-	2.2	nC
Input Capacitance	C_{ISS}	V_{DS} = -25V, V_{GS} = 0V, f = 1MHz		-	290	-	pF
Output Capacitance	C_{OSS}			-	94	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	18	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	5.00	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	100	°C/W

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = -3.1A	-	-	-5.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = -4.0A, dI_{SD}/dt = -100A/μs	-	105	160	ns
Reverse Recovery Charge	Q_{RR}			0.51	1.0	μC

Typical Performance Curves

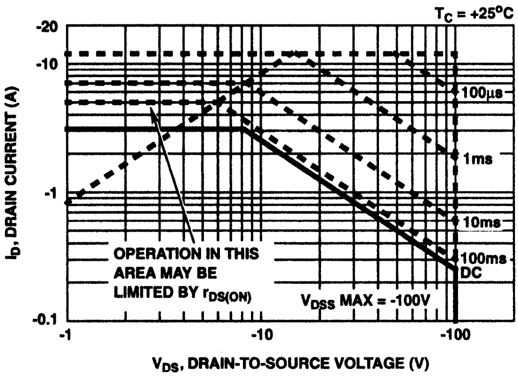


FIGURE 1. SAFE OPERATING AREA CURVE

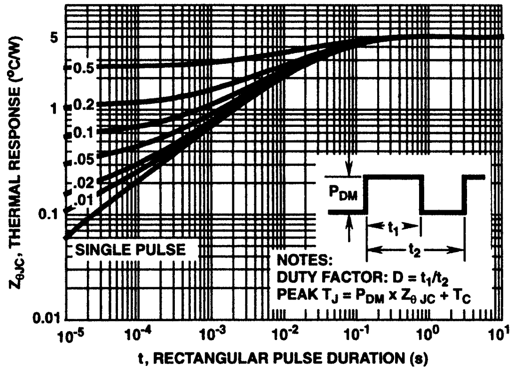


FIGURE 2. MAXIMUM TRANSIENT THERMAL IMPEDANCE

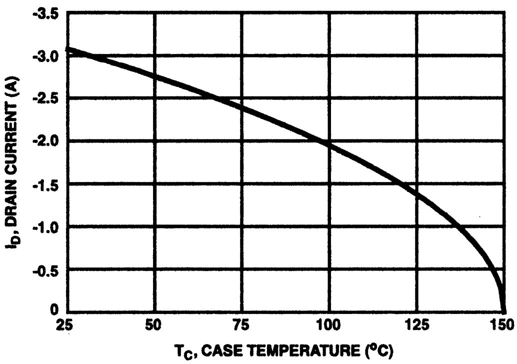


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

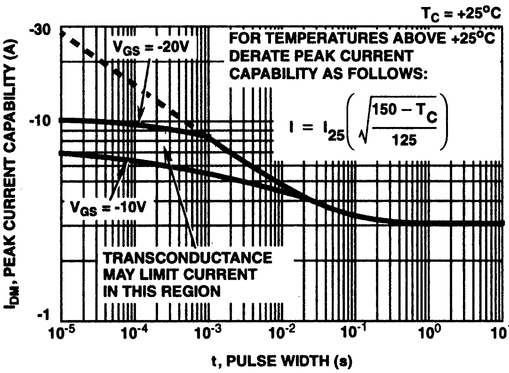


FIGURE 4. PEAK CURRENT CAPABILITY

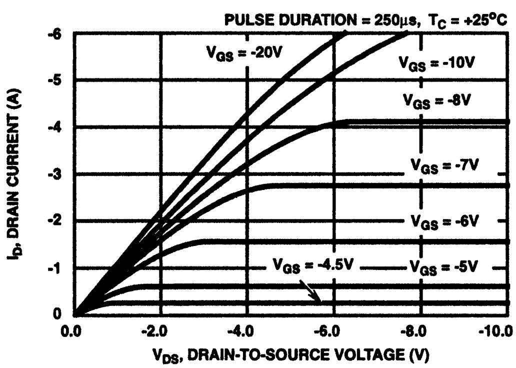


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

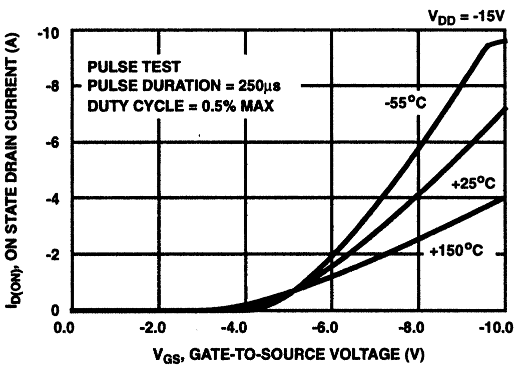


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

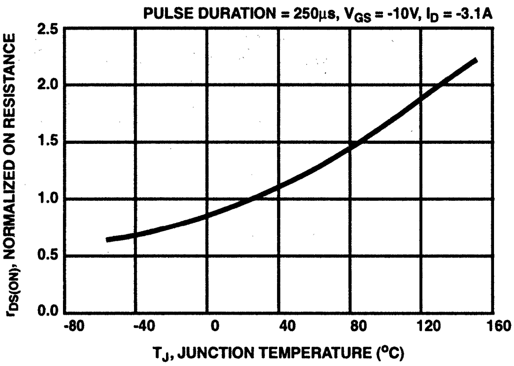


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

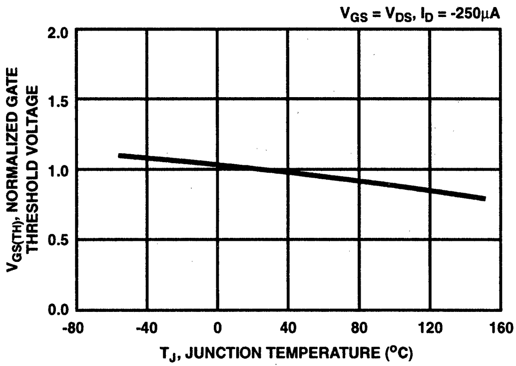


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

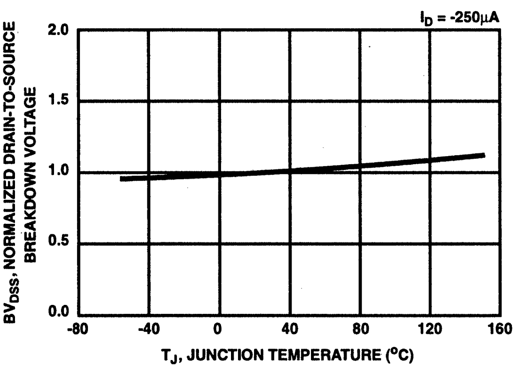


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

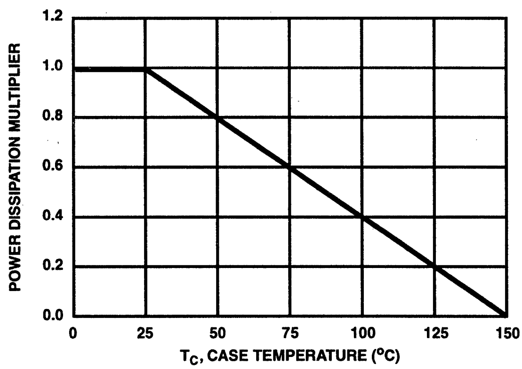


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

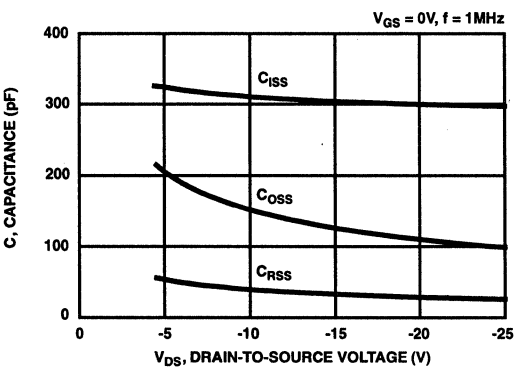


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

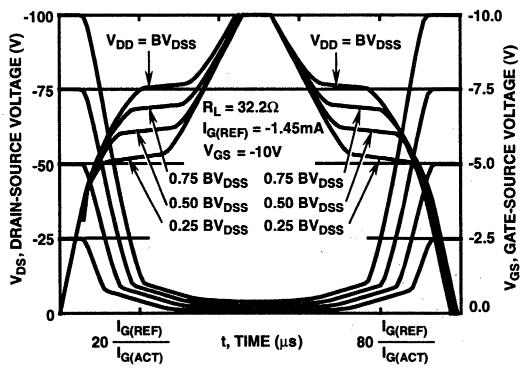


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

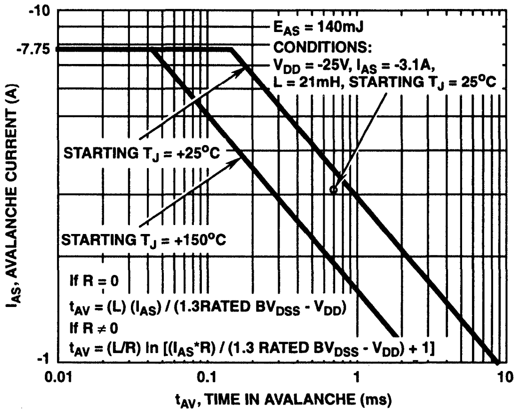


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

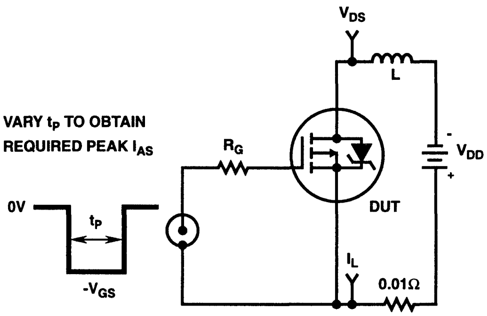


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

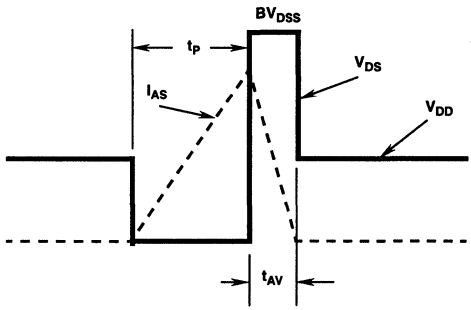


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

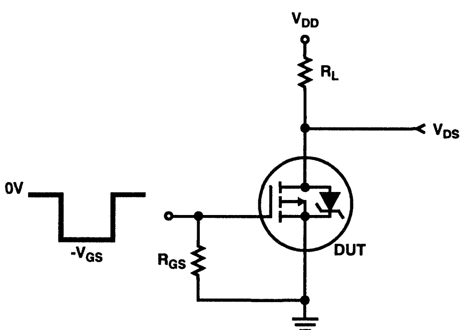


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

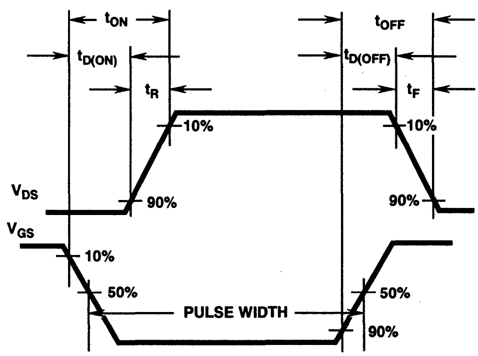
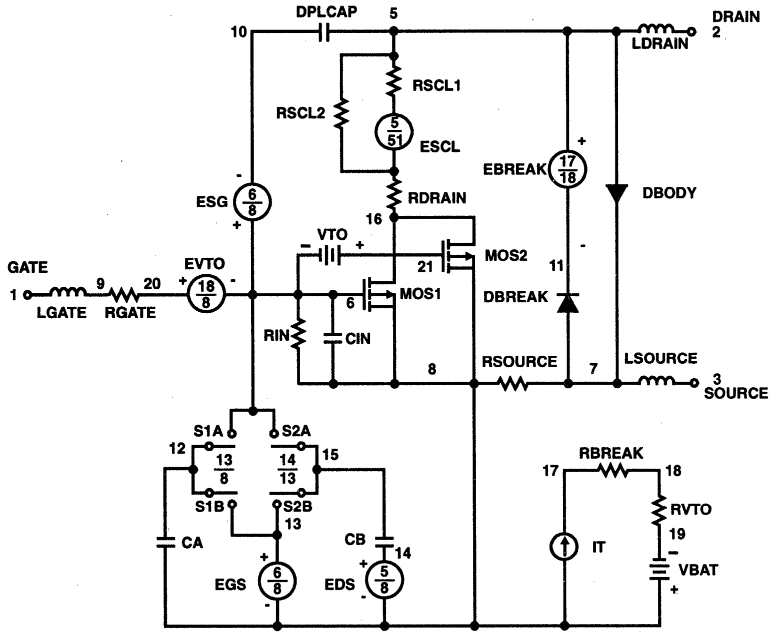


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSpice Model Listing for the IRFU9110, IRFR9110




```
.SUBCKT IRFU9110  2  1  3          REV 9/21/94

CA 12 8 3.49e-10
CB 15 14 3.52e-10
CIN 6 8 2.71e-10
DBODY 5  7  DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18  -131.4
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 2.9e-9
LSOURCE 3 7 2.9e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 497e-3
RGATE 9 20 2.68
RIN 6 8 1e9
RSCL1  5  51  RSCLMOD  1e-6
RSCL2  5  50  1e3
RSOURCE 8 7 RDSMOD 348e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.9

ESCL  51  50  VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/6.3,6))}

.MODEL DBDMOD D (IS=1.23e-14 RS=8.74e-2 TRS1=-1.95e-3 TRS2=-9.30e-6 CJO=3.72e-10 TT=1.45e-7)
.MODEL DBKMOD D (RS=2.76 TRS1=8.39e-4 TRS2=-1.87e-5)
.MODEL DPLCAPMOD D (CJO=1.31e-10 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.68 KP=0.98 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=7.25e-4 TC2=2.03e-6)
.MODEL RDSMOD RES (TC1=6.95e-3 TC2=3.07e-5)
.MODEL RSCLMOD  RES (TC1=1e-3  TC2=0)
.MODEL RVTOMOD RES (TC1=3.46e-3 TC2=5.67e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=5.03 VOFF=3.03)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.03 VOFF=5.03)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.30 VOFF=-5.30)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-5.30 VOFF=-0.30)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR IRFU9120, IRFR9120

5.6A, 100V, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- **5.6A, 100V**
- **$r_{DS(ON)}$ = 0.600Ω**
- ***Temperature Compensating* PSPICE Model**
- **Peak Current vs Pulse Width Curve**
- **UIS Rating Curve**

Description

The IRFU9120 and IRFR9120 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specific level of energy in the avalanche breakdown mode of operation. These are P-Channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

PACKAGE AVAILABILITY

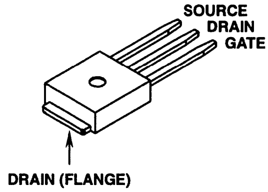
PART NUMBER	PACKAGE	BRAND
IRFU9120	TO-251AA	IF9120
IRFR9120	TO-252AA	IF9120

NOTE: When ordering use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, e.g., IRFR91209A.

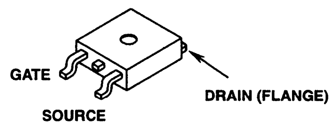
Formerly developmental type TA17501.

Package

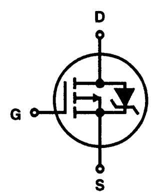
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		IRFU9120, IRFR9120	UNITS
Drain Source Voltage	V_{DSS}	-100	V
Drain Gate Voltage	V_{DGR}	-100	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	5.6	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	42	W
Derate above $+25^oC$		0.33	W/^{o}C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	^{o}C
Soldering Temperature of Leads for 10s	T_L	260	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number 3987.2

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		-100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	-1	μA
			$T_C = +150^oC$	-	-	-50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 3.4A$, $V_{GS} = -10V$		-	-	0.600	Ω
Turn-On Time	t_{ON}	$V_{DD} = -50V$, $I_D = 6.8A$ $R_L = 7.1\Omega$, $V_{GS} = -10V$ $R_{GS} = 18\Omega$		-	-	60	ns
Turn-On Delay Time	$t_{D(ON)}$			-	9.6	-	ns
Rise Time	t_R			-	29	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	21	-	ns
Fall Time	t_F			-	25	-	ns
Turn-Off Time	t_{OFF}			-	-	60	ns
Total Gate Charge	Q_G	$V_{GS} = 0V$ to $-10V$	$V_{DD} = -80V$, $I_D = 5.6A$, $R_L = 14.3\Omega$	-	-	18	nC
Gate-to-Drain Charge	Q_{GD}			-	-	9	nC
Gate-to-Source Charge	Q_{GS}			-	-	3	nC
Input Capacitance	C_{ISS}	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz		-	485	-	pF
Output Capacitance	C_{OSS}			-	170	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	45	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	3.00	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	100	$^oC/W$

Source-Drain Diode Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = -5.6A$	-	-	-6.3	V
Reverse Recovery Time	t_{RR}	$I_{SD} = -6.8A$, $dI_{SD}/dt = -100A/\mu s$	-	130	150	ns
Reverse Recovery Charge	Q_{RR}		-	0.70	1.4	μC

Typical Performance Curves

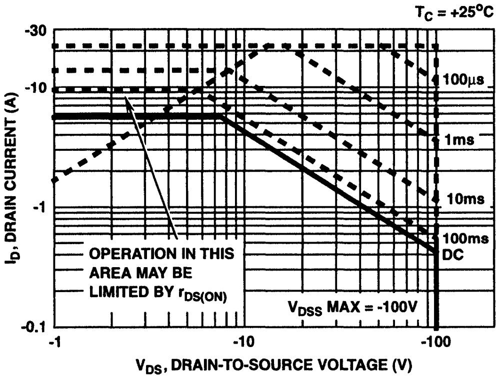


FIGURE 1. SAFE OPERATING AREA CURVE

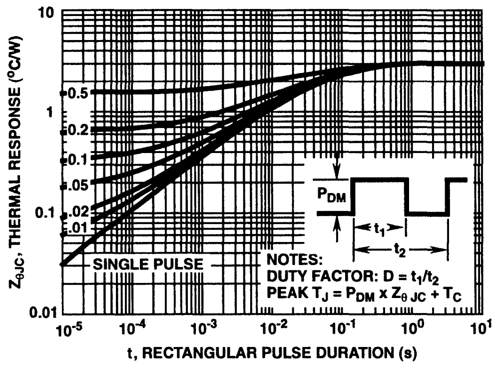


FIGURE 2. MAXIMUM TRANSIENT THERMAL IMPEDANCE

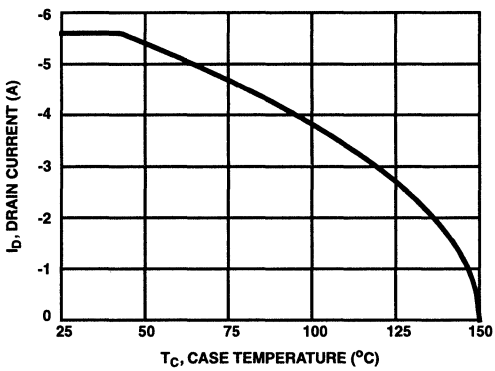


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

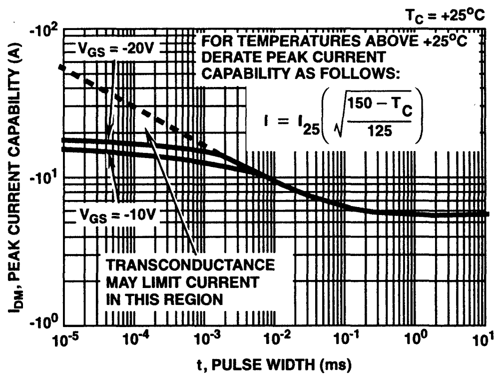


FIGURE 4. PEAK CURRENT CAPABILITY

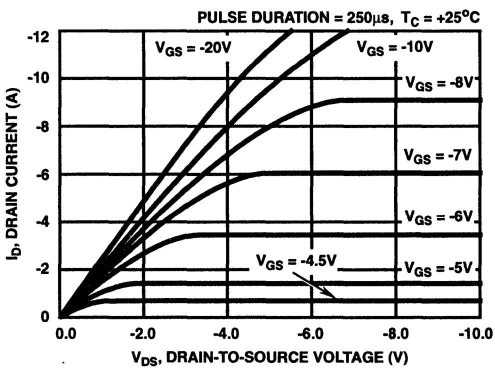


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

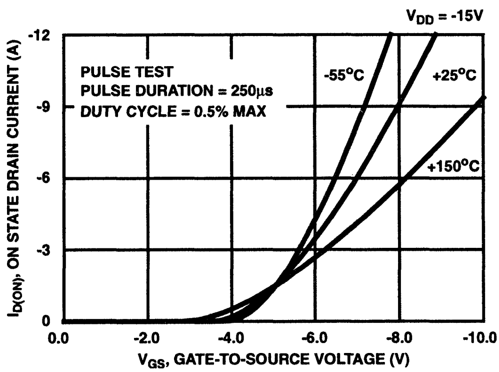


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

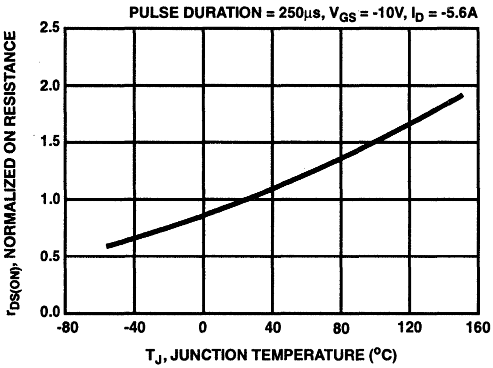


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

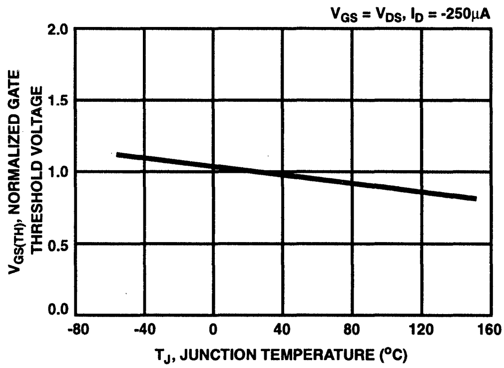


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

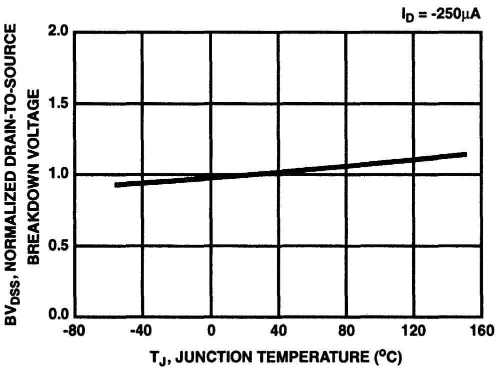


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

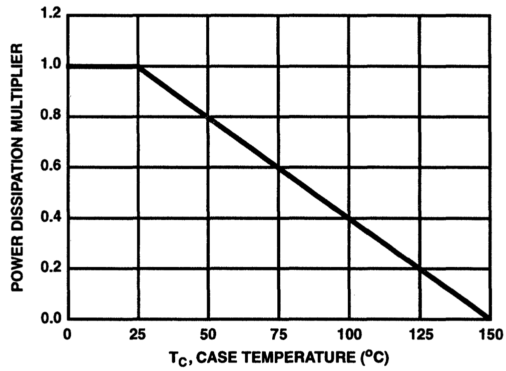


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

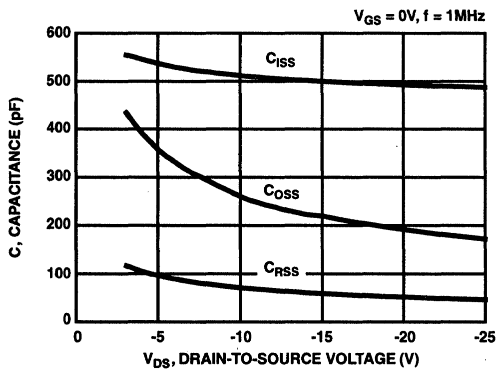


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

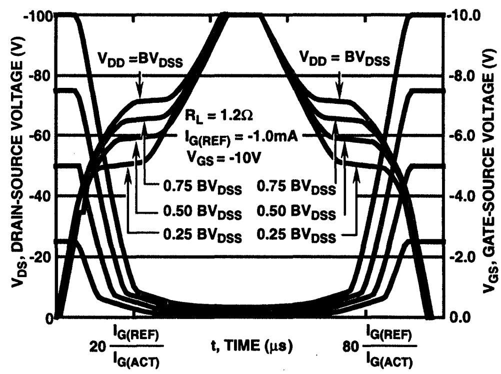


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

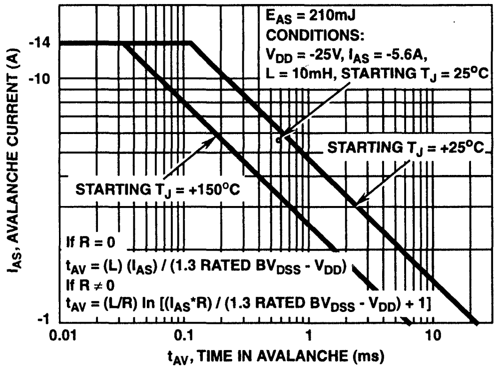


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

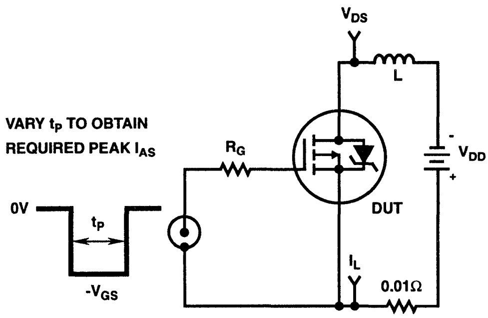


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

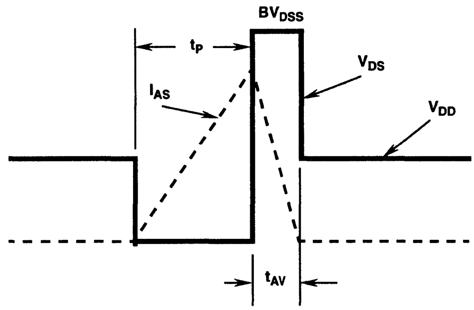


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

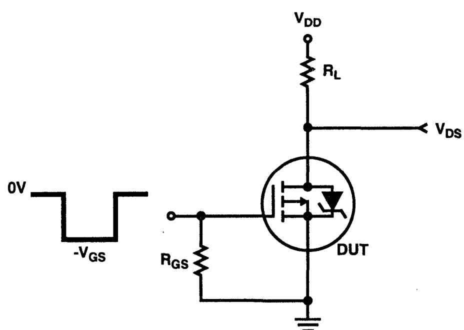


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

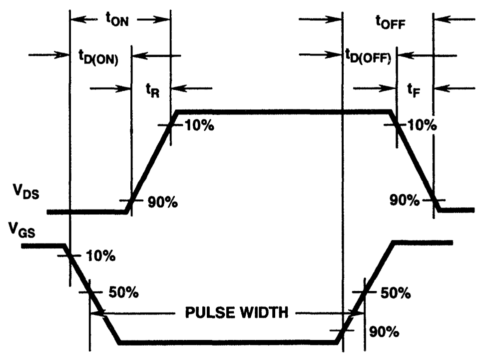


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the IRFU9120, IRFR9120

```
.SUBCKT IRFU9120  2  1  3          REV 9/16/94

CA 12 8 618.9e-12
CB 15 14 633.9e-12
CIN 6 8 441.1e-12

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -127.38
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 2.609e-9
LSOURCE 3 7 2.609e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 245.6e-3
RGATE 9 20 2.69
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 123.96e-3
RVTO 18 19 RVTOMOD 1

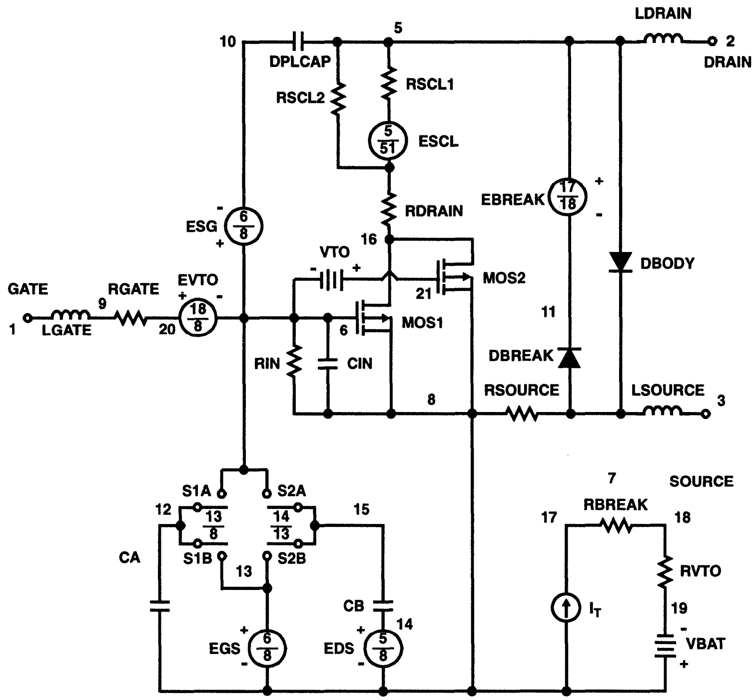
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.77

ESCL 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/13.2,6))}

.MODEL DBDMOD D (IS=5.1e-14 RS=9.4e-2 TRS1=-2.2e-3 TRS2=-5.2e-6 CJO=6.43e-10 TT=9.7e-8)
.MODEL DBKMOD D (RS=1.45 TRS1=3.84e-4 TRS2=-9.83e-6)
.MODEL DPLCAPMOD D (CJO=235e-12 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.49 KP=1.58 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=1.01e-3 TC2=1.05e-6)
.MODEL RDSMOD RES (TC1=6.23e-3 TC2=1.23e-5)
.MODEL RSCLMOD  RES (TC1=2.05e-3  TC2=-0.35e-5)
.MODEL RVTOMOD RES (TC1=-3.46e-3 TC2=3.33e-7)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=6.3 VOFF=4.3)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=4.3 VOFF=6.3)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.0 VOFF=-4.0)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.0 VOFF=1.0)

.ENDS
```



NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

HARRIS
SEMICONDUCTOR

IRFR9220, IRFU9220

3.6A, 200V, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 3.6A, 200V
- $r_{DS(ON)} = 1.500\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The IRFU9220 and IRFR9220 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specific level of energy in the avalanche breakdown mode of operation. These are P-Channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

PACKAGE AVAILABILITY

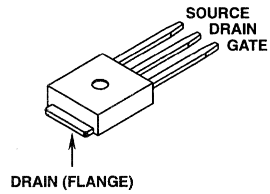
PART NUMBER	PACKAGE	BRAND
IRFU9220	TO-251AA	IF9220
IRFR9220	TO-252AA	IF9220

NOTE: When ordering use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, e.g., IRFR92209A.

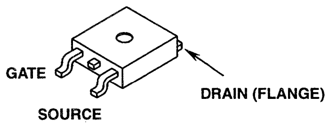
Formerly developmental type TA17502.

Packages

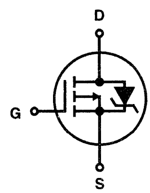
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

	IRFU9220, IRFR9220	UNITS
Drain Source Voltage . . . . . V_{DSS}	-200	V
Drain Gate Voltage . . . . . V_{DGR}	-200	V
Gate Source Voltage . . . . . V_{GS}	±20	V
Drain Current		
RMS Continuous . . . . . I_D	3.6	A
Pulsed Drain Current . . . . . I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating . . . . . E_{AS}	Refer to UIS Curve	
Power Dissipation		
$T_C = +25^oC$ . . . . . P_D	42	W
Derate above $+25^oC$	0.33	W/^{o}C
Operating and Storage Temperature . . . . . T_{STG}, T_J	-55 to +150	^{o}C
Soldering Temperature of Leads for 10s . . . . . T_L	260	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		-200	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -200V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	-1	µA
			$T_C = +150^oC$	-	-	-50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 2.2A$, $V_{GS} = -10V$		-	-	1.500	Ω
Turn-On Time	t_{ON}	$V_{DD} = -100V$, $I_D = 3.9A$ $R_L = 24\Omega$, $V_{GS} = -10V$ $R_{GS} = 18\Omega$		-	-	50	ns
Turn-On Delay Time	$t_{D(ON)}$			-	8.8	-	ns
Rise Time	t_R			-	27	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	7.3	-	ns
Fall Time	t_F			-	19	-	ns
Turn-Off Time	t_{OFF}			-	-	50	ns
Total Gate Charge	Q_G	$V_{GS} = 0$ to $-10V$	$V_{DD} = -160V$, $I_D = 3.9A$, $R_L = 41\Omega$	-	20	-	nC
Gate-to-Drain Charge	Q_{GD}			-	11	-	nC
Gate-to-Source Charge	Q_{GS}			-	3.3	-	nC
Input Capacitance	C_{ISS}	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz		-	550	-	pF
Output Capacitance	C_{OSS}			-	110	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	33	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	3.00	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	100	°C/W

Source-Drain Diode Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = -3.6A$	-	-	-6.3	V
Reverse Recovery Time	t_{RR}	$I_{SD} = -3.6A$, $dI_{SD}/dt = -100A/\mu s$	-	150	300	ns
Reverse Recovery Charge	Q_{RR}			0.97	2.0	µC

Typical Performance Curves

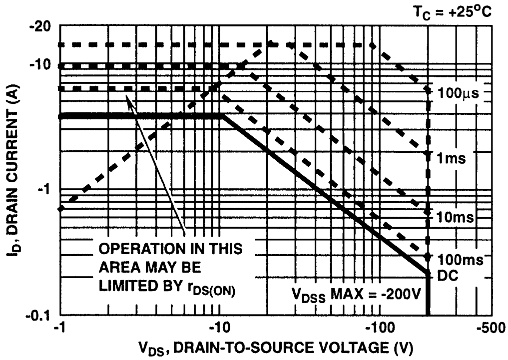


FIGURE 1. SAFE OPERATING AREA CURVE

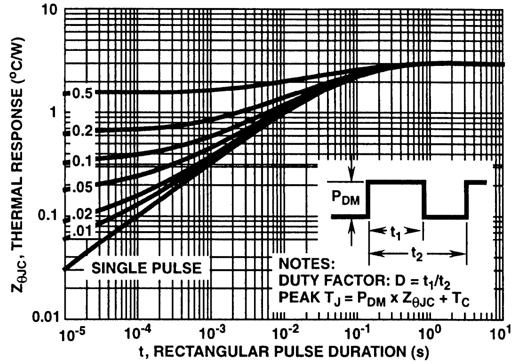


FIGURE 2. MAXIMUM TRANSIENT THERMAL IMPEDANCE

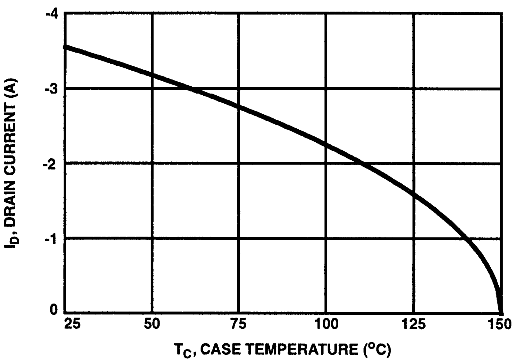


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

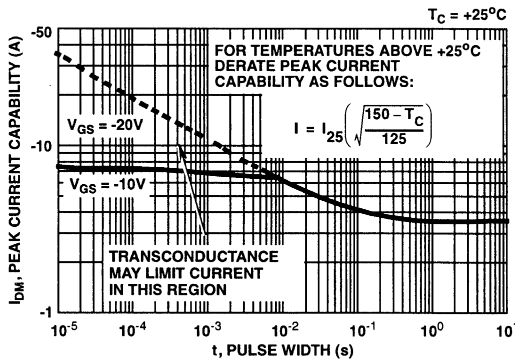


FIGURE 4. PEAK CURRENT CAPABILITY

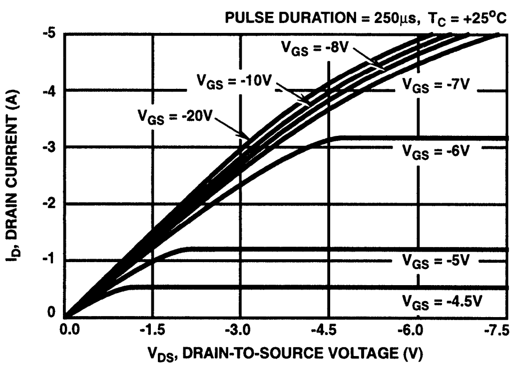


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

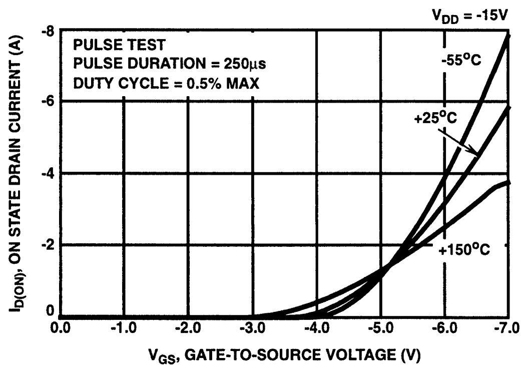


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

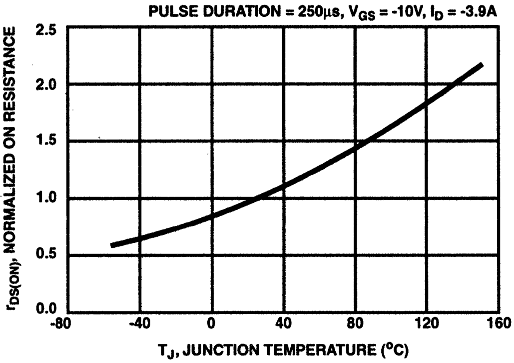


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

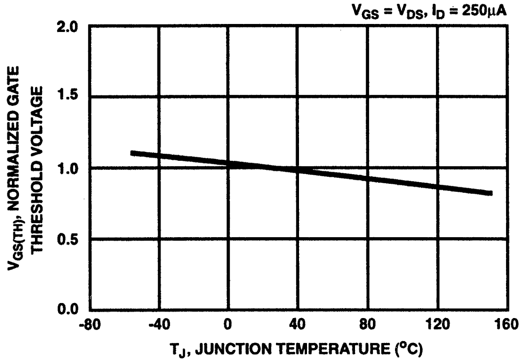


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

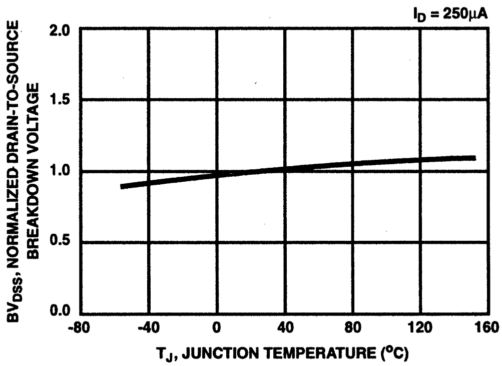


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

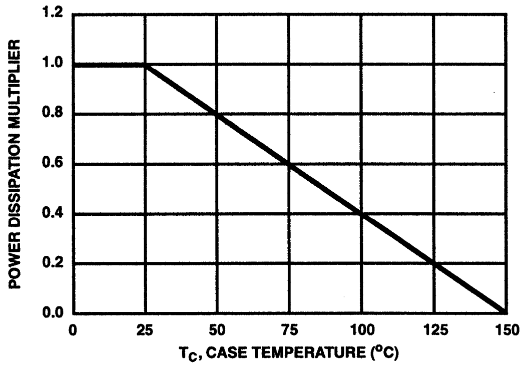


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

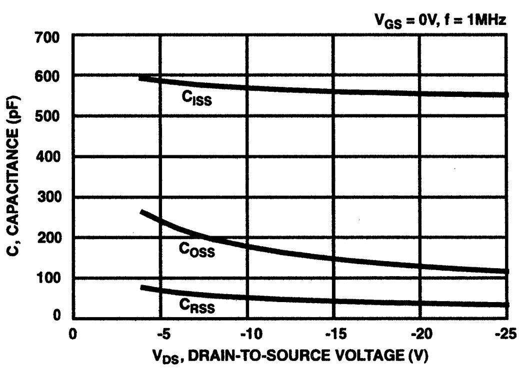


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

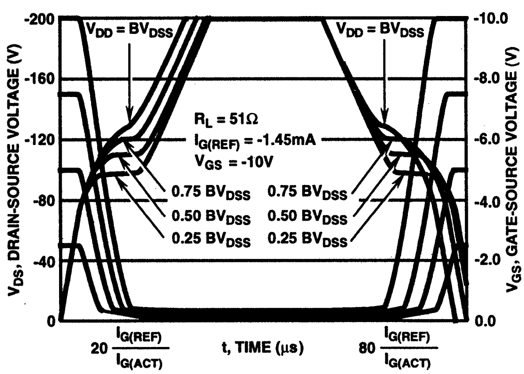


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

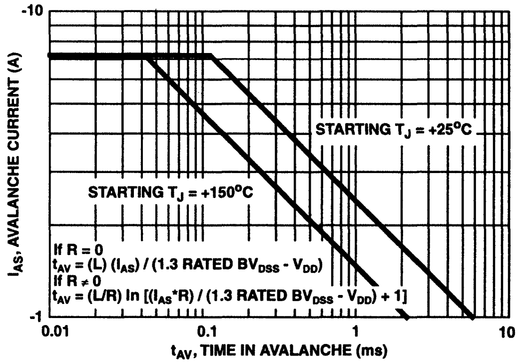


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

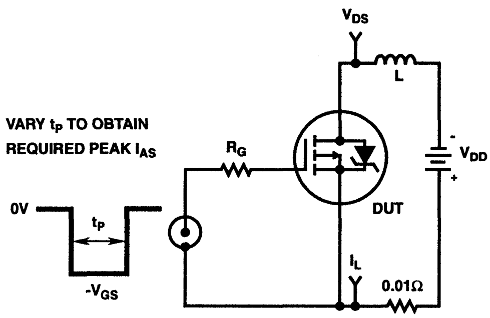


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

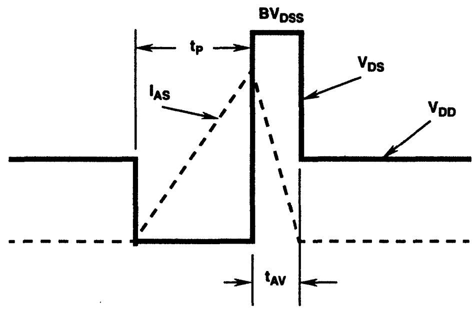


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

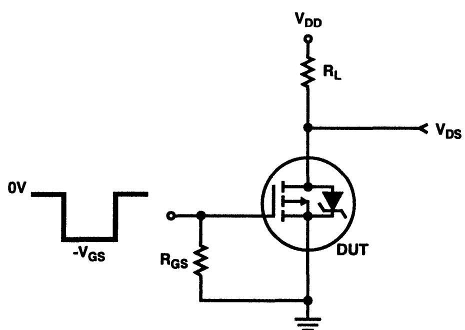


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

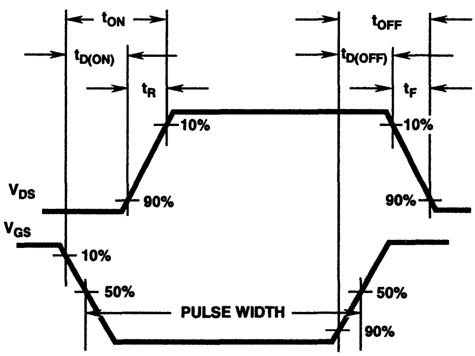


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

4
P-CHANNEL POWER MOSFETs

Temperature Compensated PSPICE Model for the IRFU9220, IRFR9220

.SUBCKT IRFU9220 2 1 3 REV 9/6/94

CA 12 8 723e-12
CB 15 14 733e-12
CIN 6 8 517e-12

DBODY 5 7 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 7 11 17 18 -244.4
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

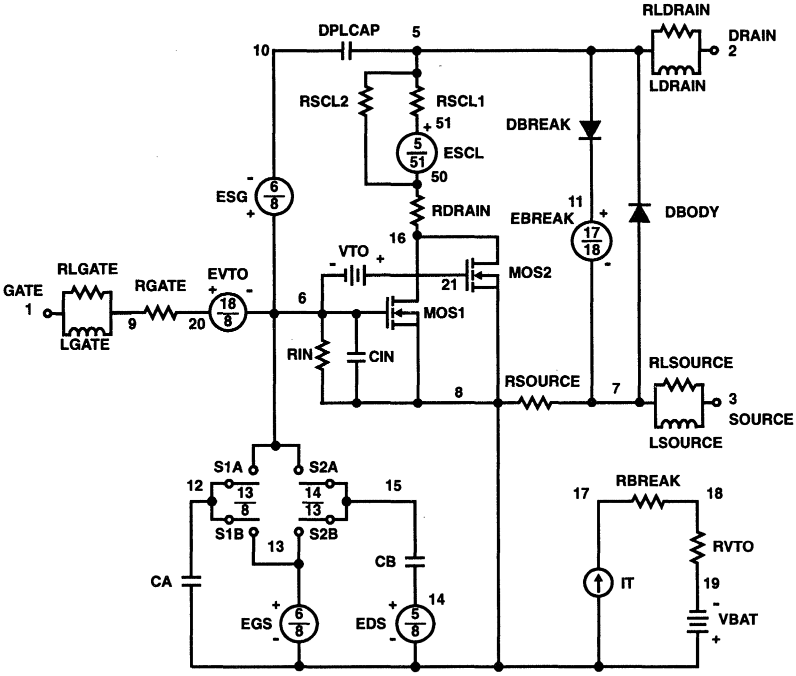
LDRAIN 2 5 1e-9
LGATE 1 9 2.609e-9
LSOURCE 3 7 2.609e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 1.194
RGATE 9 20 2.17
RIN 6 8 1e9
RLDRAIN 2 5 10
RLGATE 1 9 26.09
RLSOURCE 3 7 26.09
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 90.1e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.77



ESCL 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/4.6,6))}

.MODEL DBDMOD D (IS=2.56e-14 RS=8.09e-2 TRS1=-2.45e-3 TRS2=-1.33e-5 CJO=4.21e-10 TT=1.17e-7)
.MODEL DBKMOD D (RS=5.07 TRS1=-1.05e-3 TRS2=1.28e-5)
.MODEL DPLCAPMOD D (CJO=170e-12 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.58 KP=1.38 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=1.1e-3 TC2=-2.73e-6)
.MODEL RDSMOD RES (TC1=6.95e-3 TC2=2.23e-5)
.MODEL RSCLMOD RES (TC1=2.40e-3 TC2=-1.5e-5)
.MODEL RVTOMOD RES (TC1=-3.27e-3 TC2=-1.33e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=5.29 VOFF=3.29)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.29 VOFF=5.29)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.1 VOFF=-4.9)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4.9 VOFF=0.1)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFD8P06E, RFD8P06ESM, RFP8P06E

8A, 60V, ESD Rated, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 8A, 60V
- $r_{DS(ON)} = 0.300\Omega$
- *Temperature Compensating* PSPICE Model
- 2kV ESD Protected
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RFD8P06E, RFD8P06ESM and RFP8P06E P-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers and emitter switches for bipolar transistors. These transistors can be operated directly from integrated circuits.

The RFD8P06E, RFD8P06ESM and RFP8P06E incorporate ESD protection and are designed to withstand 2kV (Human Body Model) of ESD.

PACKAGE AVAILABILITY

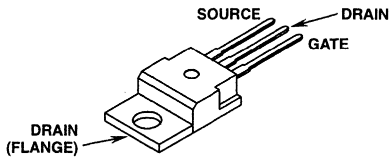
PART NUMBER	PACKAGE	BRAND
RFP8P06E	TO-220AB	RFP8P06E
RFD8P06ESM	TO-252AA	D8P06E
RFD8P06E	TO-251AA	D8P06E

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, i.e. RFD8P06ESM9A.

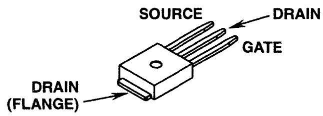
Formerly developmental type TA49044.

Packages

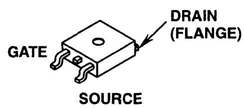
JEDEC TO-220AB



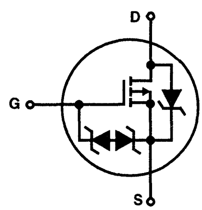
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		RFD8P06E, RFD8P06ESM, RFP8P06E	UNITS
Drain Source Voltage	V_{DSS}	-60	V
Drain Gate Voltage	V_{DGR}	-60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	8	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	48	W
Derate above $+25^oC$		0.32	$W/^oC$
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	ESD	2	kV
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	^oC
Soldering Temperature of Leads for 10s	T_L	260	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V		-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA		-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -60V, V_{GS} = 0V	T_C = +25°C	-	-	-1.0	µA
			T_C = +150°C	-	-	-50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	10	µA
On Resistance	$r_{DS(ON)}$	I_D = 8A, V_{GS} = -10V		-	-	0.300	Ω
Turn-On Time	t_{ON}	V_{DD} = -30V, I_D = 8A R_L = 3.75Ω, V_{GS} = -10V R_{GS} = 2.5Ω		-	-	70	ns
Turn-On Delay Time	$t_{D(ON)}$			-	15	-	ns
Rise Time	t_R			-	30	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	40	-	ns
Fall Time	t_F			-	25	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to -20V	V_{DD} = -48V, I_D = 8A, R_L = 6Ω	-	30	36	nC
Gate Charge at 10V	$Q_{G(-10)}$	V_{GS} = 0 to -10V		-	15	18	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0 to -2V		-	1.15	1.5	nC
Input Capacitance	C_{ISS}	V_{DS} = -25V, V_{GS} = 0V f = 1MHz		-	600	-	pF
Output Capacitance	C_{OSS}			-	160	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	35	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-220		-	-	3.125	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220		-	-	80	°C/W
		TO-251, TO-252		-	-	100	°C/W

Source-Drain Diode and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = -8A	-	-	-1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = -8A, dI_{SD}/dt = -100A/µs	-	-	125	ns

Typical Performance Curves

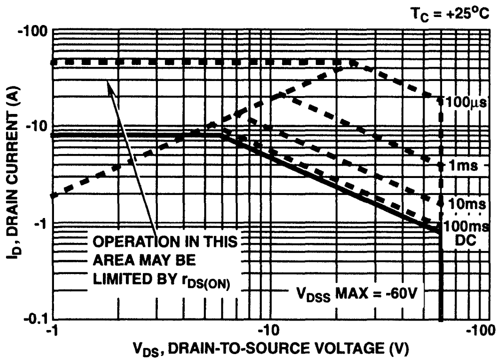


FIGURE 1. SAFE OPERATING AREA CURVE

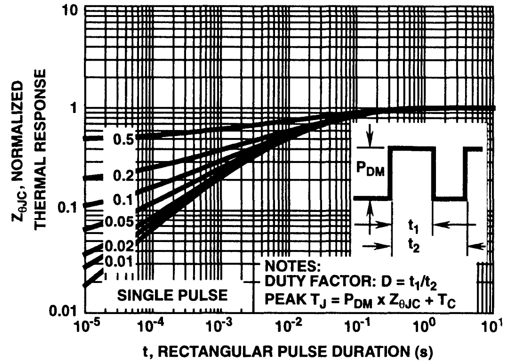


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

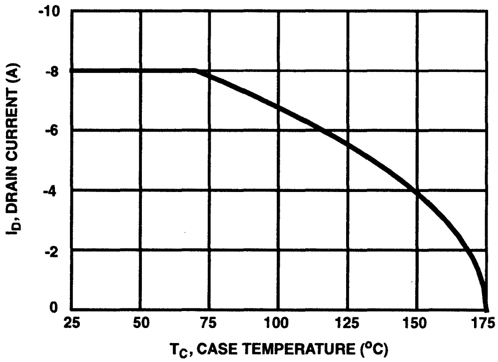


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

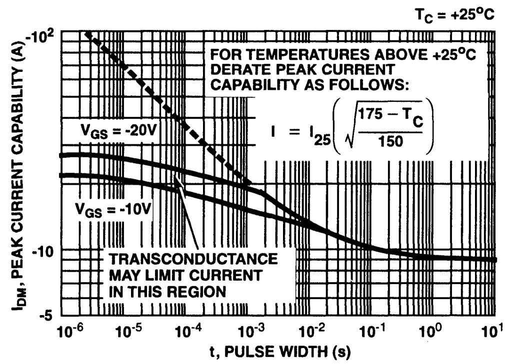


FIGURE 4. PEAK CURRENT CAPABILITY

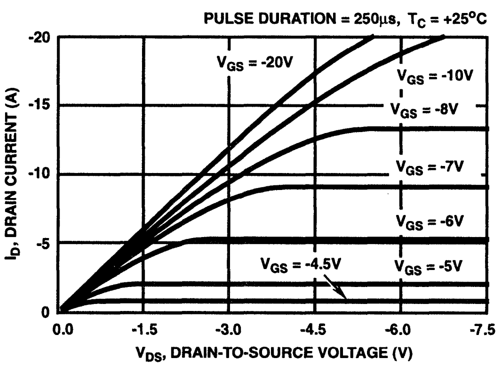


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

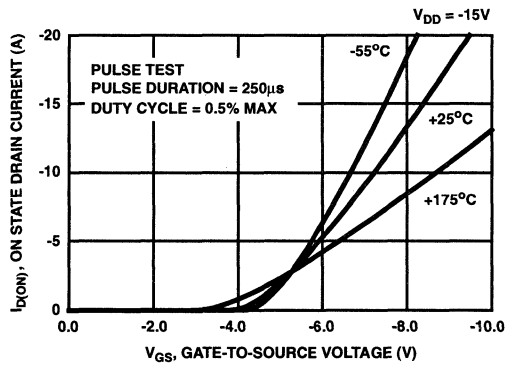


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

4

P-CHANNEL POWER MOSFETS

Typical Performance Curves (Continued)

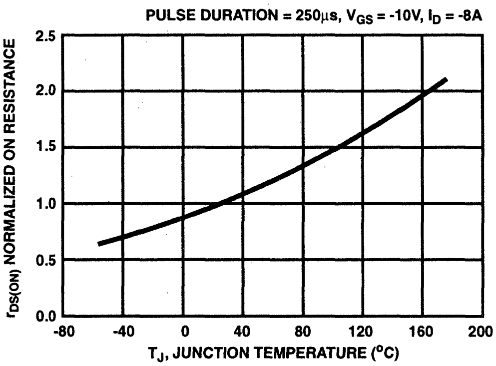


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

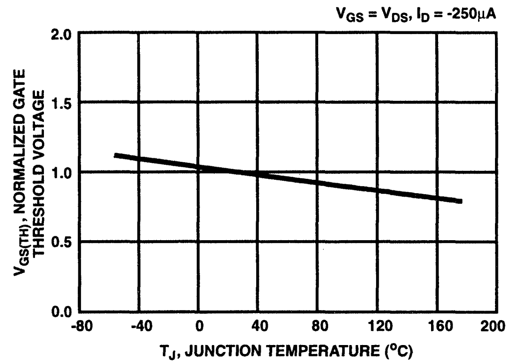


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

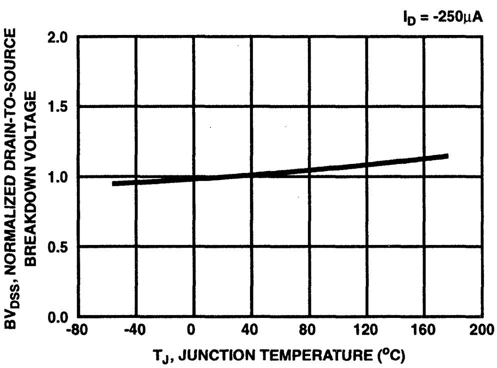


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

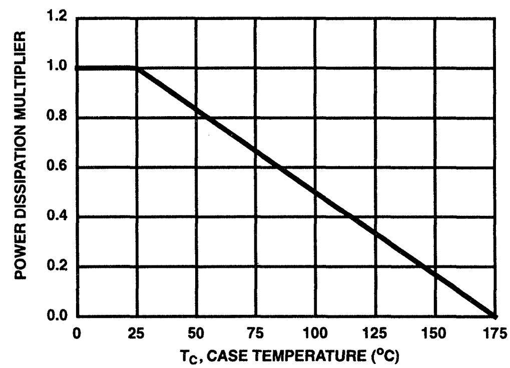


FIGURE 10. NORMALIZED POWER DISSIPATIION vs TEMPERATURE DERATING CURVE

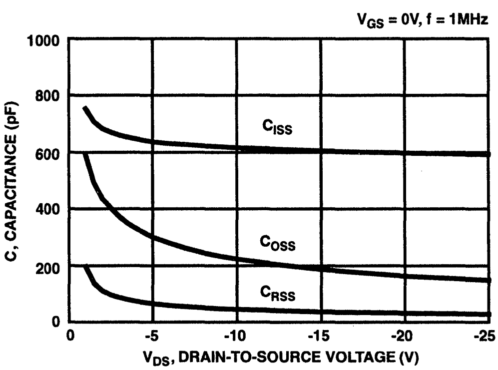


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

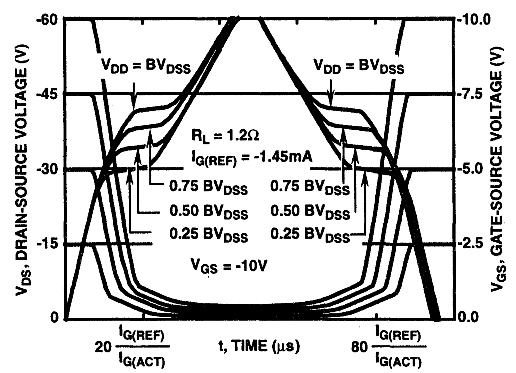


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

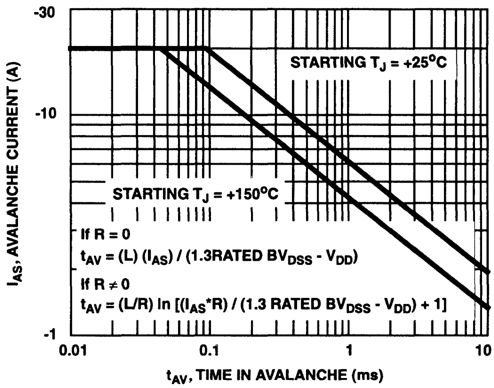


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

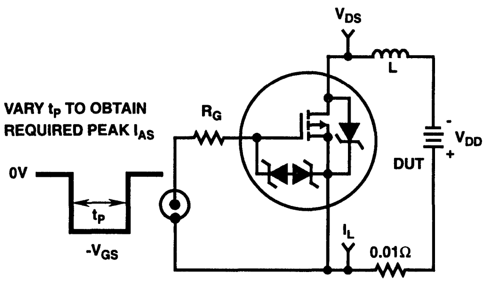


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

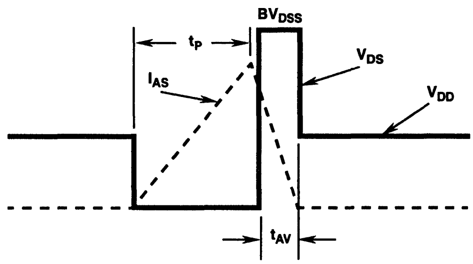


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

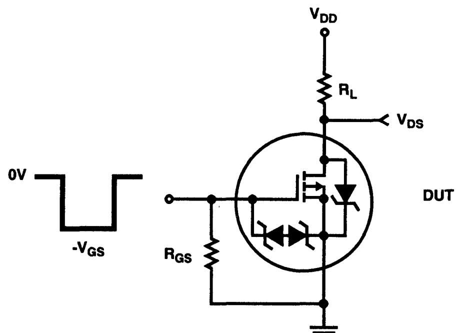


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

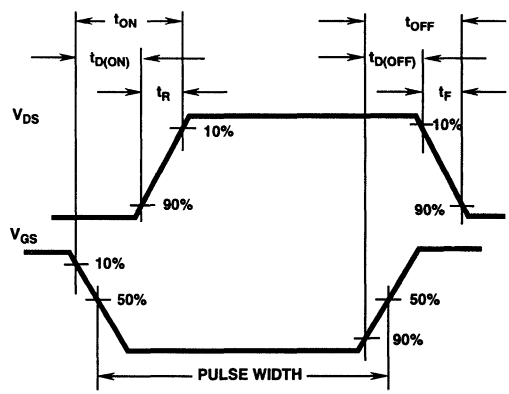


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD8P06E, RFD8P06ESM, RFP8P06E

.SUBCKT RFP8P06E 2 1 3 REV 6/23/94

CA 12 8 7.24e-10
CB 15 14 8.04e-10
CIN 6 8 6.00e-10

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -79.2
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 6 8 1
EVTO 20 6 8 18 1

IT 8 17 1

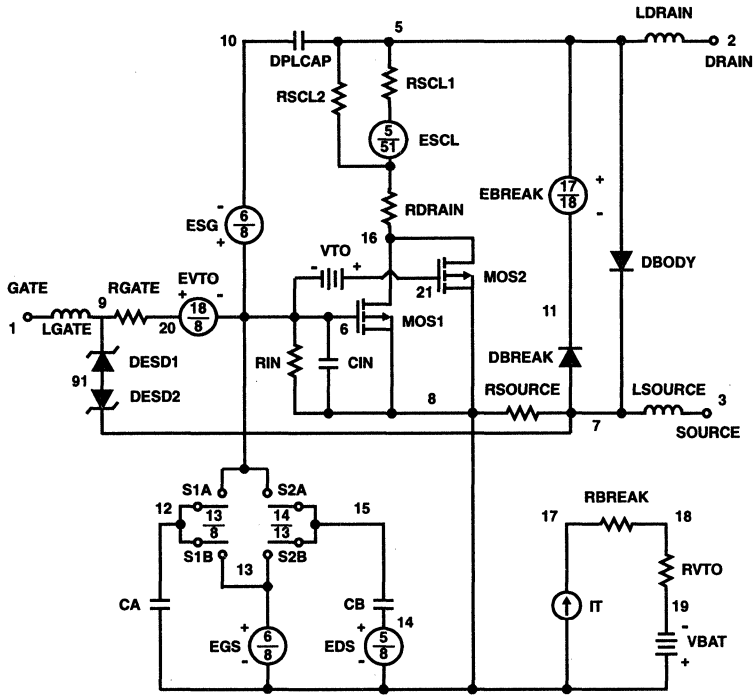
LDRAIN 2 5 1e-10
LGATE 1 9 2.92e-9
LSOURCE 3 7 2.92e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 95.2e-3
RGATE 9 20 3.95
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 143.6e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.804



ESCL 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/22,9))}

.MODEL DBDMOD D (IS=4.15e-15 RS=5.54e-2 TRS1=-1.32e-3 TRS2=-2.48e-6 CJO=6.06e-10 TT=7.50e-8)
.MODEL DBKMOD D (RS=4.66e-1 TRS1=1.58e-3 TRS2=-7.49e-6)
.MODEL DESD1MOD D (BV=20.2 TBV1=-1.25e-3 TBV2=5.79e-7 RS=36 NBV=50 IBV=7e-6)
.MODEL DESD2MOD D (BV=25.4 TBV1=-8.3e-4 TBV2=8.9e-7 NBV=50 IBV=7e-6)
.MODEL DPLCAPMOD D (CJO=2.49e-10 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.824 KP=5.163 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=9.48e-4 TC2=-1.42e-7)
.MODEL RDSMOD RES (TC1=5.40e-3 TC2=1.25e-5)
.MODEL RSCLMOD RES (TC1=1.75e-3 TC2=3.90e-6)
.MODEL RVTOMOD RES (TC1=-3.55e-3 TC2=-3.43e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=5.10 VOFF=3.10)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.10 VOFF=5.10)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=2.1 VOFF=-2.9)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-2.9 VOFF=2.1)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFD15P05, RFD15P05SM, RFP15P05

15A, 50V, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 15A, 50V
- $r_{DS(ON)} = 0.150\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RFD15P05, RFD15P05SM, and RFP15P05 P-Channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

PACKAGING AVAILABILITY

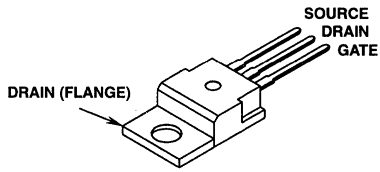
PART NUMBER	PACKAGE	BRAND
RFD15P05	TO-251AA	F15P05
RFD15P05SM	TO-252AA	F15P05
RFP15P05	TO-220AB	RFP15P05

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD15P05SM9A.

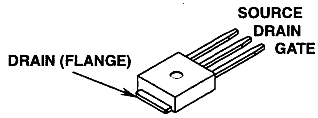
Formerly developmental type TA09833.

Packaging

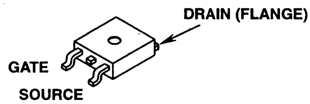
JEDEC TO-220AB



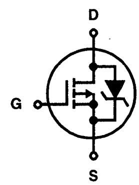
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		RFD15P05, RFD15P05SM, RFP15P05	UNITS
Drain Source Voltage	V_{DSS}	-50	V
Drain Gate Voltage	V_{DGR}	-50	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	15	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	80	W
Derate above $+25^oC$		0.533	$W/^oC$
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	^oC
Soldering Temperature of Leads for 10s	T_L	260	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2387.3**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		-50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -50V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	-1	μA
			$T_C = +150^oC$	-	-	-50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 15A$, $V_{GS} = -10V$		-	-	0.150	Ω
Turn-On Time	t_{ON}	$V_{DD} = -25V$, $I_D = 7.5A$ $R_L = 3.3\Omega$, $V_{GS} = -10V$ $R_{GS} = 12.5\Omega$		-	-	60	ns
Turn-On Delay Time	$t_{D(ON)}$			-	16	-	ns
Rise Time	t_R			-	30	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	50	-	ns
Fall Time	t_F			-	20	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $-20V$	$V_{DD} = -40V$, $I_D = 15A$, $R_L = 2.67\Omega$	-	-	150	nC
Gate Charge at -10V	$Q_{G(-10)}$	$V_{GS} = 0V$ to $-10V$		-	-	75	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $-2V$		-	-	3.5	nC
Input Capacitance	C_{ISS}	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz		-	1150	-	pF
Output Capacitance	C_{OSS}			-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	56	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-220AB, TO-251AA, TO-252AA		-	-	1.875	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251AA, TO-252AA		-	-	100	$^oC/W$
		TO-220AB		-	-	80	$^oC/W$

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = -15A$	-	-	-1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = -15A$, $dI_{SD}/dt = -100A/\mu s$	-	-	125	ns

Typical Performance Curves

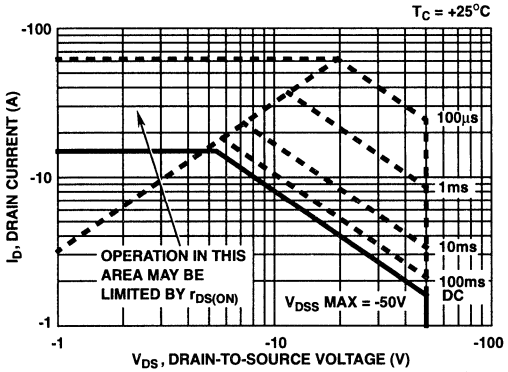


FIGURE 1. SAFE OPERATING AREA CURVE

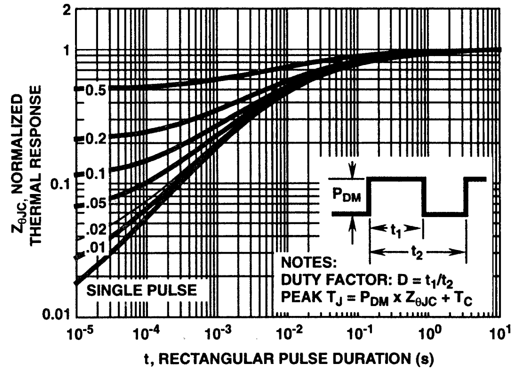


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

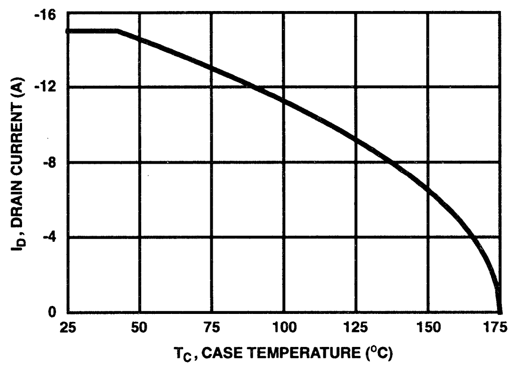


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

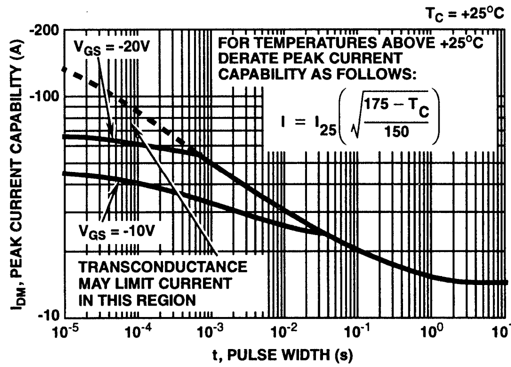


FIGURE 4. PEAK CURRENT CAPABILITY

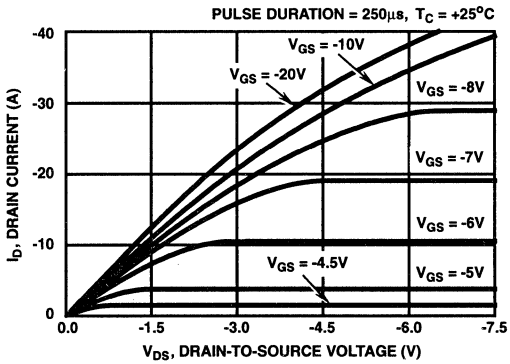


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

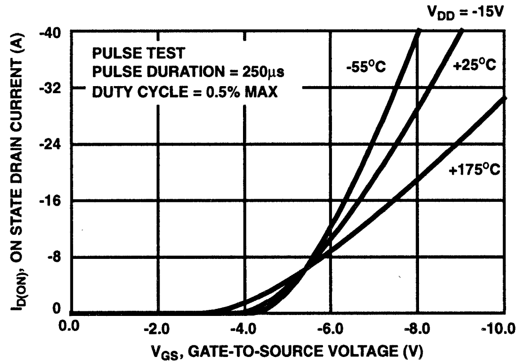


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

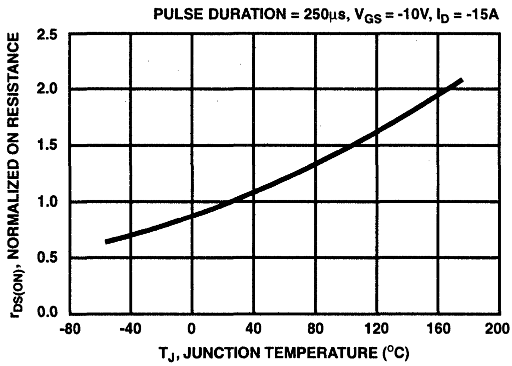


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

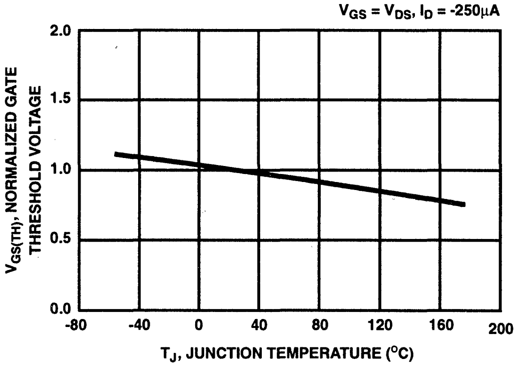


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

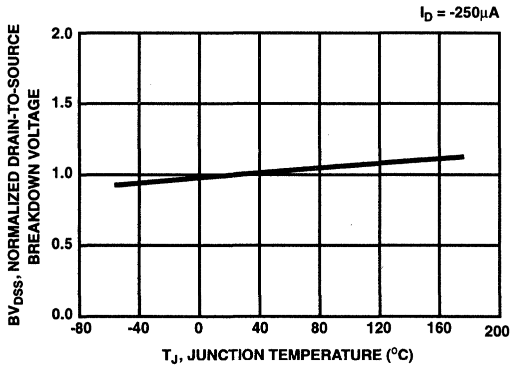


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

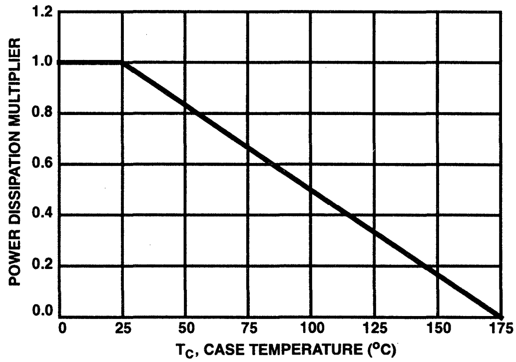


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

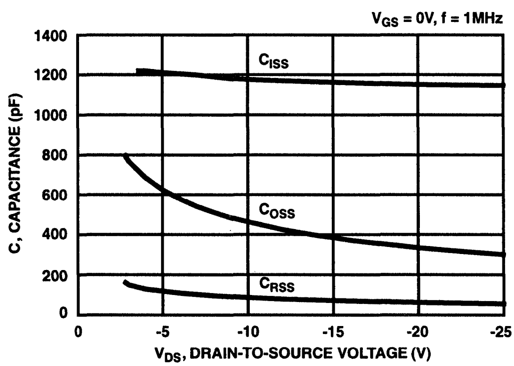


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

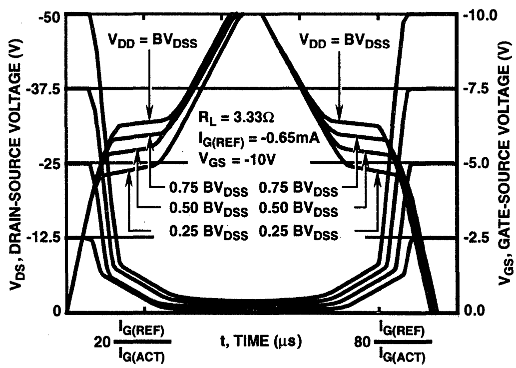


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

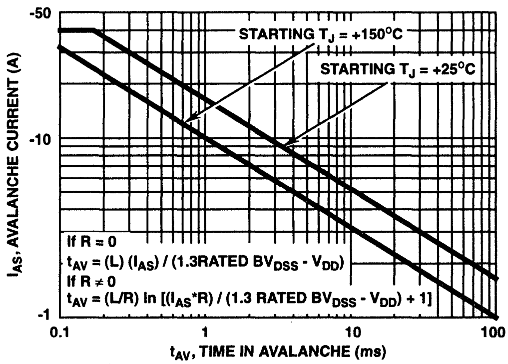


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

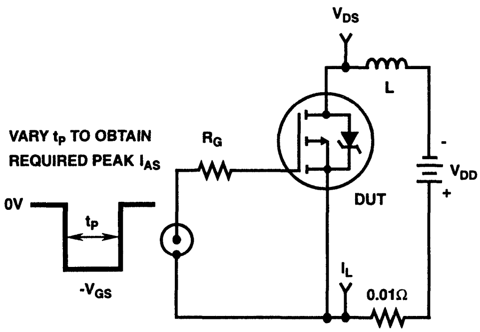


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

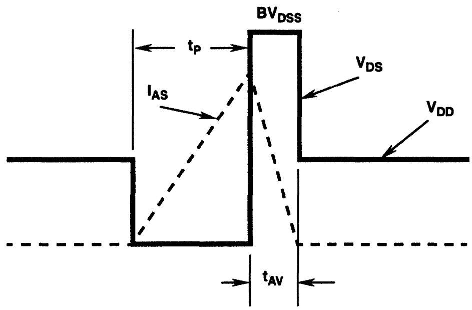


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

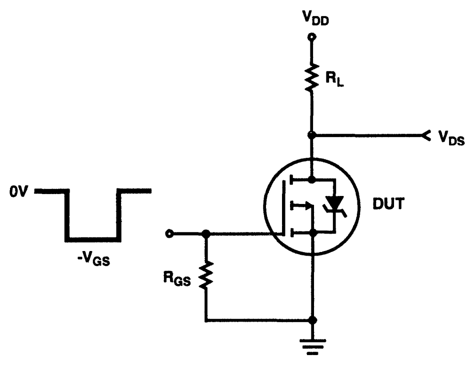


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

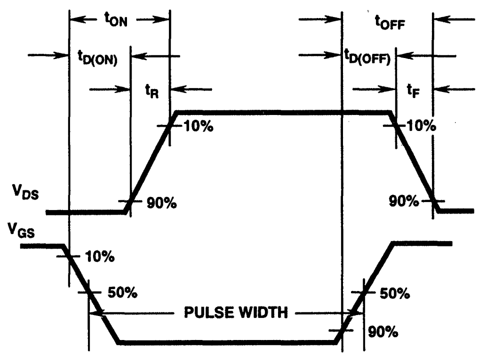


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD15P05, RFD15P05SM, RFP15P05

.SUBCKT RFP15P05 2 1 3 REV 9/06/94

CA 12 8 1.6e-9
CB 15 14 1.47e-9
CIN 6 8 1.09e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -73.0
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

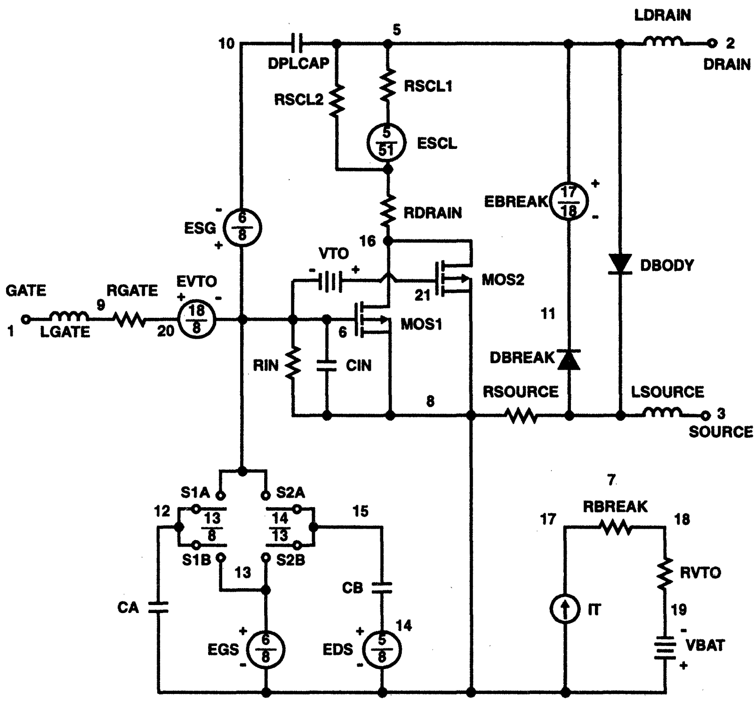
LDRAIN 2 5 1e-9
LGATE 1 9 6.73e-9
LSOURCE 3 7 6.69e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 63.6e-3
RGATE 9 20 7.37
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 46.5e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.65



ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/35,4))}

.MODEL DBDMOD D (IS = 1.27e-13 RS = 1.62e-2 TRS1 = 1.35e-3 TRS2 = -4.33e-6 CJO = 1.25e-9 TT = 7.97e-8)
.MODEL DBKMOD D (RS = 2.54e-1 TRS1 = 4.54e-3 TRS2 = -1.12e-5)
.MODEL DPLCAPMOD D (CJO = 285e-12 IS = 1e-30 N = 10)
.MODEL MOSMOD PMOS (VTO = -3.78 KP = 6.97 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 9.15e-4 TC2 = -4.0e-7)
.MODEL RDSMOD RES (TC1 = 5.47e-3 TC2 = 1.37e-5)
.MODEL RSCLMOD RES (TC1 = 1.9e-3 TC2 = -7.5e-6)
.MODEL RVTOMOD RES (TC1 = -3.71e-3 TC2 = -2.41e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 3.65 VOFF = 1.65)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.65 VOFF = 3.65)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.60 VOFF = -4.40)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.40 VOFF = 0.60)

.ENDS
NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFD15P06, RFD15P06SM, RFP15P06

15A, 60V, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 15A, 60V
- $r_{DS(ON)} = 0.150\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RFD15P06, RFD15P06SM, and RFP15P06 P-Channel power MOSFETs are manufactured using the MegaFET process. This process which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

PACKAGING AVAILABILITY

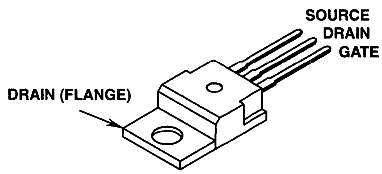
PART NUMBER	PACKAGE	BRAND
RFD15P06	TO-251AA	F15P06
RFD15P06SM	TO-252AA	F15P06
RFP15P06	TO-220AB	RFP15P06

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in the tape and reel, i.e., RFD15P06SM9A.

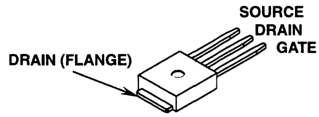
Formerly developmental type TA09833.

Packaging

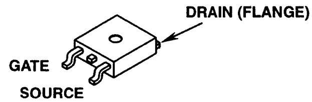
JEDEC TO-220AB



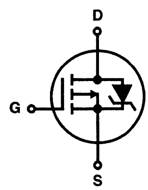
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		RFD15P06, RFD15P06SM, RFP15P06	UNITS
Drain Source Voltage	V_{DSS}	-60	V
Drain Gate Voltage	V_{DGR}	-60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	15	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	80	W
Derate above $+25^oC$		0.533	$W/^oC$
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	^oC
Soldering Temperature of Leads for 10s	T_L	260	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3988.1**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	-1	µA
			$T_C = +150^oC$	-	-	-50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 15A$, $V_{GS} = -10V$		-	-	0.150	Ω
Turn-On Time	t_{ON}	$V_{DD} = -30V$, $I_D = 7.5A$, $R_L = 4.0\Omega$, $V_{GS} = -10V$, $R_{GS} = 12.5\Omega$		-	-	60	ns
Turn-On Delay Time	$t_{D(ON)}$			-	16	-	ns
Rise Time	t_R			-	30	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	50	-	ns
Fall Time	t_F			-	20	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $-20V$	$V_{DD} = -48V$, $I_D = 15A$, $R_L = 3.20\Omega$	-	-	150	nC
Gate Charge at -10V	$Q_{G(-10)}$	$V_{GS} = 0V$ to $-10V$		-	-	75	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $-2V$		-	-	3.5	nC
Input Capacitance	C_{ISS}	$V_{DS} = -25V$, $V_{GS} = 0V$, f = 1MHz		-	1150	-	pF
Output Capacitance	C_{OSS}			-	300	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	56	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-220AB, TO-251AA, TO-252AA		-	-	1.875	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-251AA, TO-252AA		-	-	100	$^oC/W$
		TO-220AB		-	-	80	$^oC/W$

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = -15A$	-	-	-1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = -15A$, $dI_{SD}/dt = -100A/\mu s$	-	-	125	ns

Typical Performance Curves

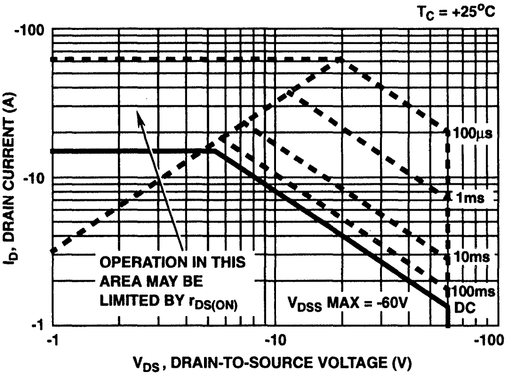


FIGURE 1. SAFE OPERATING AREA CURVE

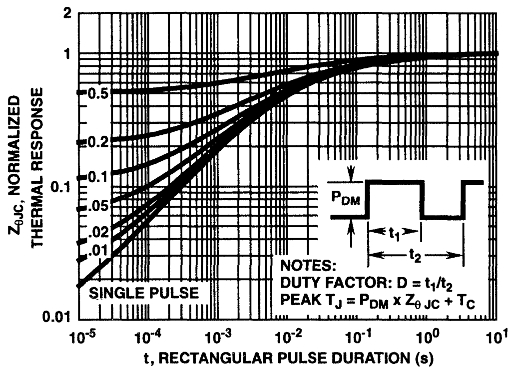


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

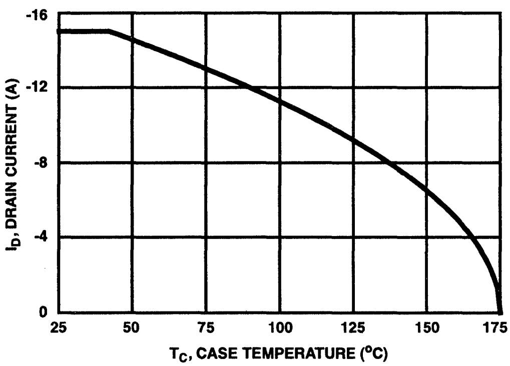


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

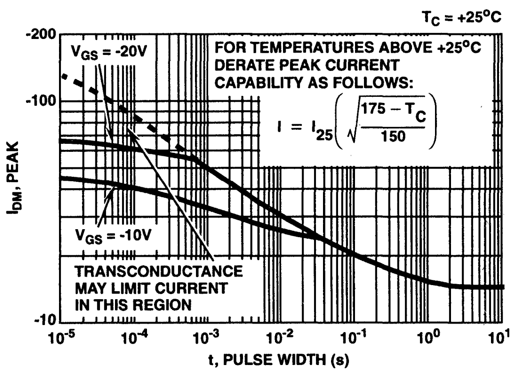


FIGURE 4. PEAK CURRENT CAPABILITY

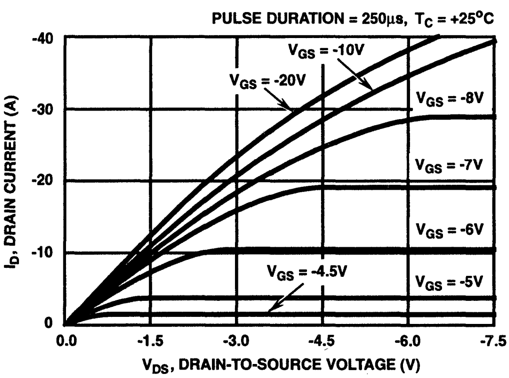


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

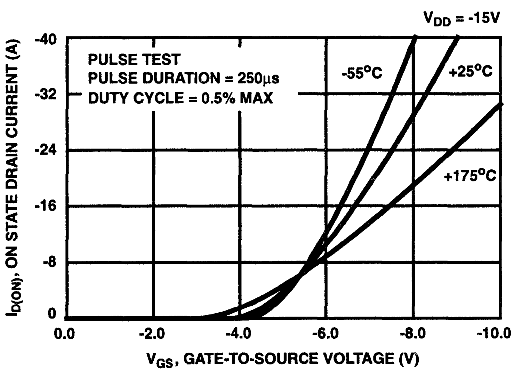


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

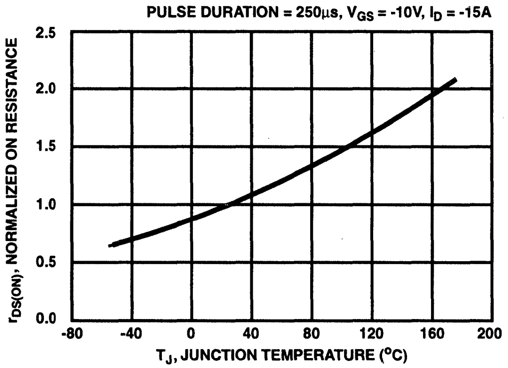


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

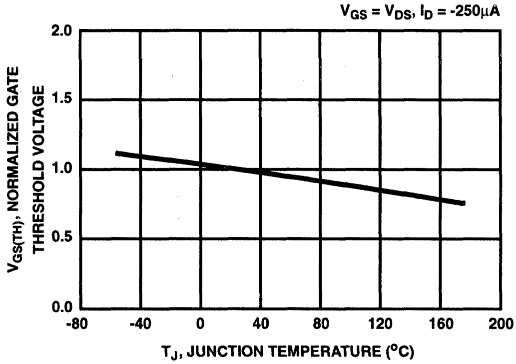


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

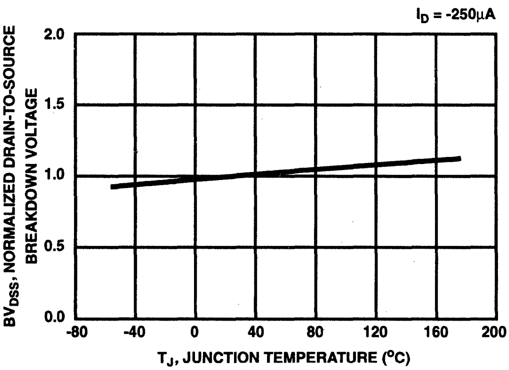


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

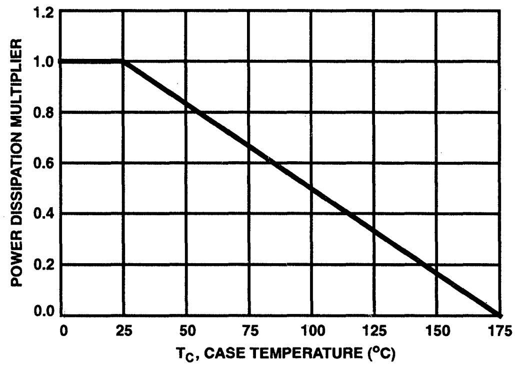


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

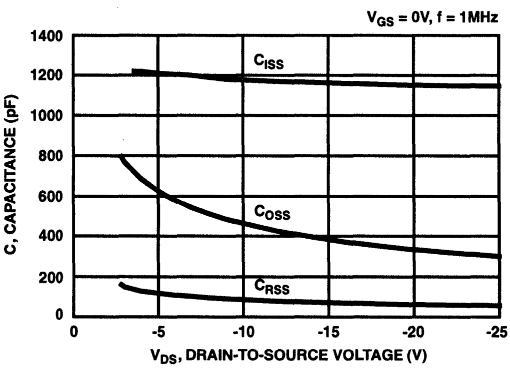


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

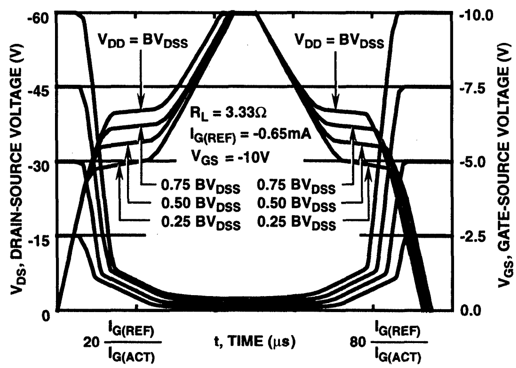


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

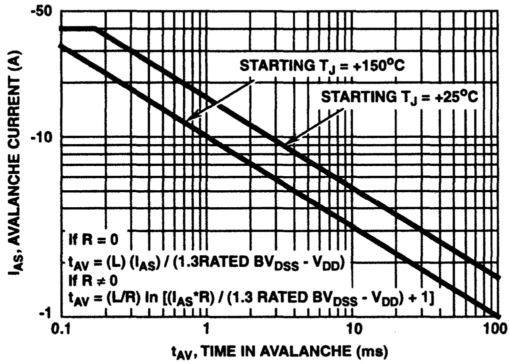


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

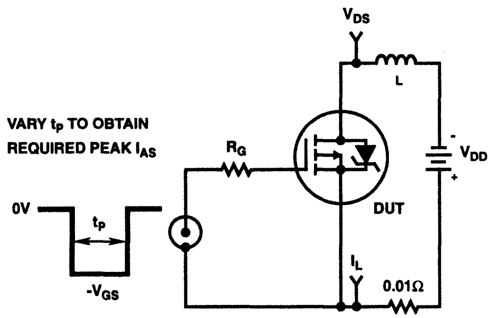


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

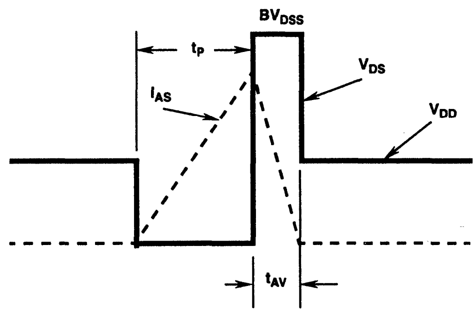


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

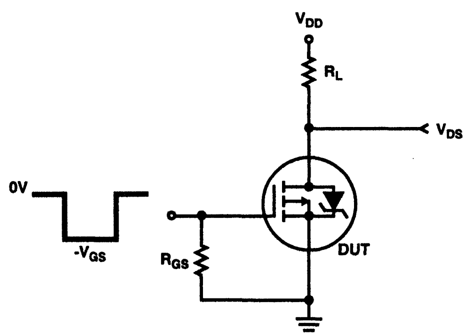


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

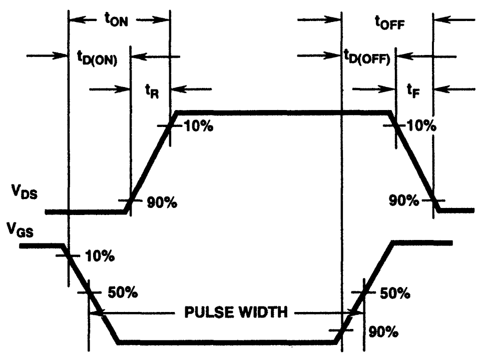
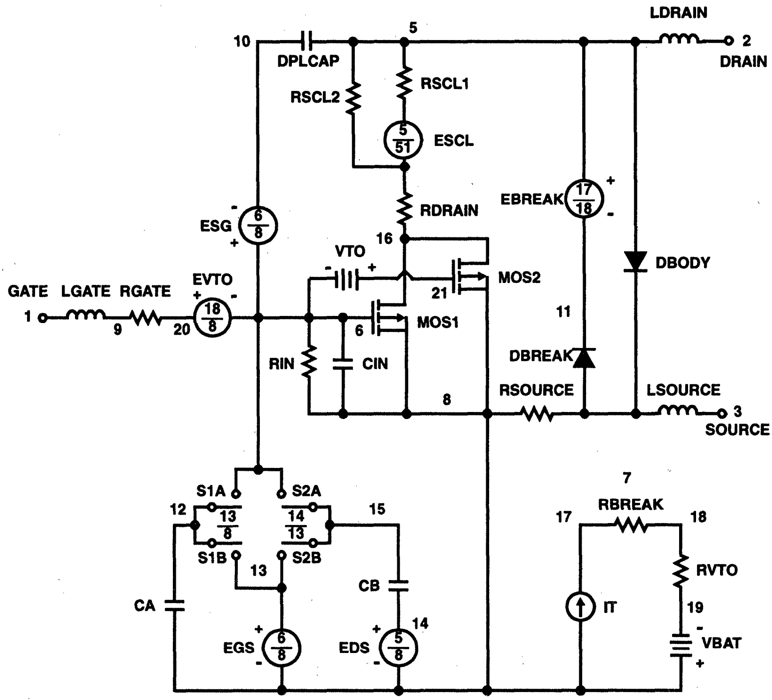


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD15P06, RFD15P06SM, RFP15P06




```
.SUBCKT RFP15P06 2 1 3     REV 9/06/94

CA 12 8 1.6e-9
CB 15 14 1.47e-9
CIN 6 8 1.09e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -73.0
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 6.73e-9
LSOURCE 3 7 6.69e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 63.6e-3
RGATE 9 20 7.37
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 46.5e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.65

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/35,4))}

.MODEL DBDMOD D (IS = 1.27e-13 RS = 1.62e-2 TRS1 = 1.35e-3 TRS2 = -4.33e-6 CJO = 1.25e-9 TT = 7.97e-8)
.MODEL DBKMOD D (RS = 2.54e-1 TRS1 = 4.54e-3 TRS2 = -1.12e-5)
.MODEL DPLCAPMOD D (CJO = 285e-12 IS = 1e-30 N = 10)
.MODEL MOSMOD PMOS (VTO = -3.78 KP = 6.97 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 9.15e-4 TC2 = -4.0e-7)
.MODEL RDSMOD RES (TC1 = 5.47e-3 TC2 = 1.37e-5)
.MODEL RSCLMOD RES (TC1 = 1.9e-3 TC2 = -7.5e-6)
.MODEL RVTOMOD RES (TC1 = -3.71e-3 TC2 = -2.41e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 3.65 VOFF = 1.65)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.65 VOFF = 3.65)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.60 VOFF = -4.40)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.40 VOFF = 0.60)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFG30P05, RFP30P05, RF1S30P05, RF1S30P05SM

30A, 50V, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- **30A, 50V**
- **$r_{DS(ON)} = 0.065\Omega$**
- ***Temperature Compensating* PSPICE Model**
- **Peak Current vs Pulse Width Curve**
- **UIS Rating Curve**
- **+175°C Operating Temperature**

Description

The RFG30P05, RFP30P05, RF1S30P05, and RF1S30P05SM P-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

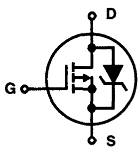
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFG30P05	TO-247	RFG30P05
RFP30P05	TO-220AB	RFP30P05
RF1S30P05	TO-262AA	F1S30P05
RF1S30P05SM	TO-263AB	F1S30P05

NOTE: When ordering use the entire part number.

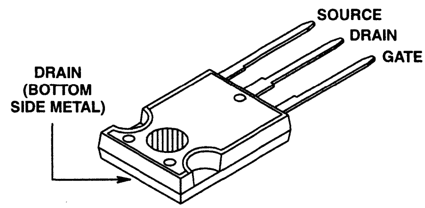
Formerly developmental type TA09834.

Symbol

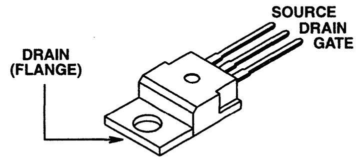


Packages

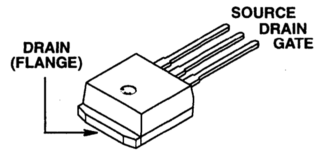
JEDEC STYLE TO-247



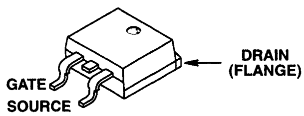
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = +25^oC$

		RFG30P05, RFP30P05 RF1S30P05, RF1S30P05SM	UNITS
Drain Source Voltage	V_{DSS}	-50	V
Drain Gate Voltage	V_{DGR}	-50	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous	I_D	30	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	120	W
Derate above +25°C		0.8	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

File Number **2436.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V		-50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA		-2	-	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -50V, V_{GS} = 0V	T_C = +25°C	-	-	-1	µA
			T_C = +150°C	-	-	-50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 30A, V_{GS} = -10V		-	-	0.065	Ω
Turn-On Time	t_{ON}	V_{DD} = -25V, I_D = 15A, R_L = 1.67Ω, V_{GS} = -10V, R_{GS} = 6.25Ω		-	-	80	ns
Turn-On Delay Time	$t_{D(ON)}$			-	15	-	ns
Rise Time	t_R			-	23	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	28	-	ns
Fall Time	t_F			-	18	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to -20V	V_{DD} = -40V, I_D = 30A, R_L = 1.33Ω	-	140	170	nC
Gate Charge at -10V	$Q_{G(-10)}$	V_{GS} = 0 to -10V		-	70	85	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0 to -2V		-	5.5	6.6	nC
Input Capacitance	C_{ISS}	V_{DS} = -25V, V_{GS} = 0V, f = 1MHz		-	3200	-	pF
Output Capacitance	C_{OSS}			-	800	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	175	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.25	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = -30A	-	-	-1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = -30A, dI_{SD}/dt = -100A/µs	-	-	150	ns

Typical Performance Curves

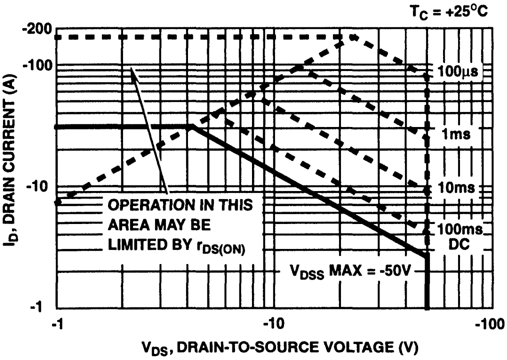


FIGURE 1. SAFE OPERATING AREA CURVE

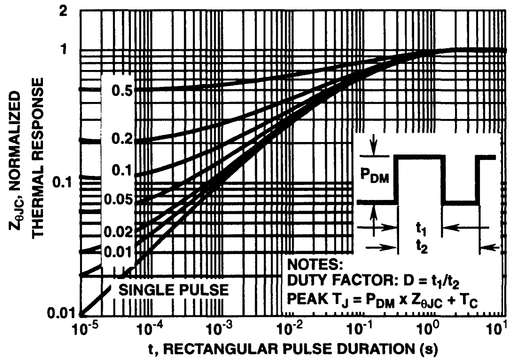


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

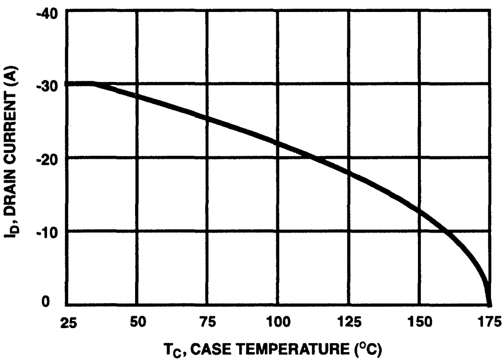


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

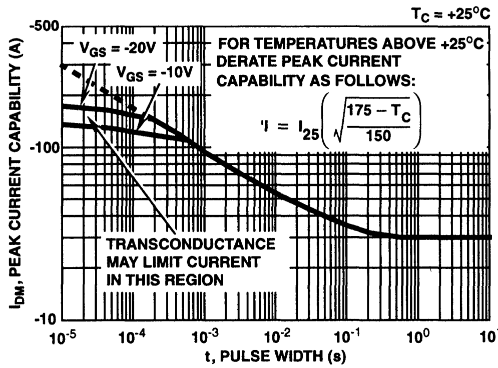


FIGURE 4. PEAK CURRENT CAPABILITY

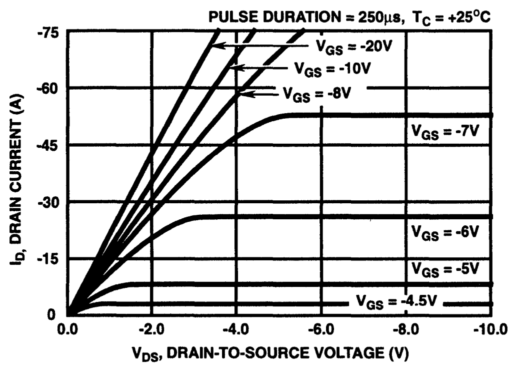


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

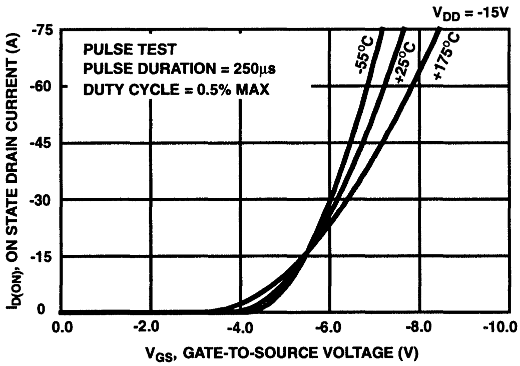


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

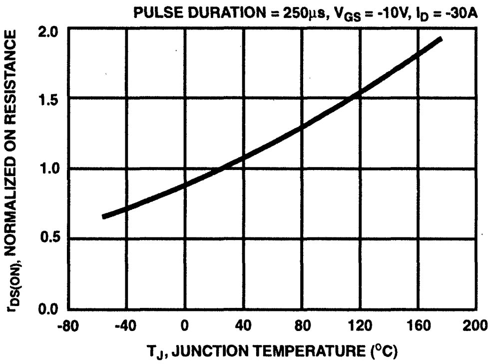


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

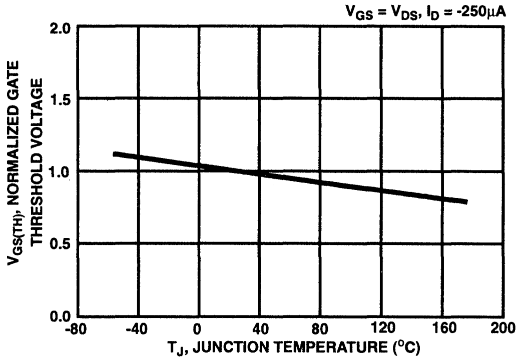


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

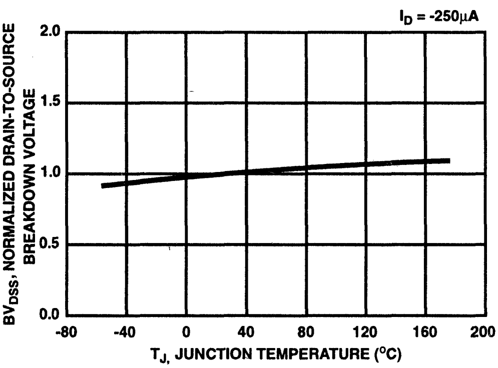


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

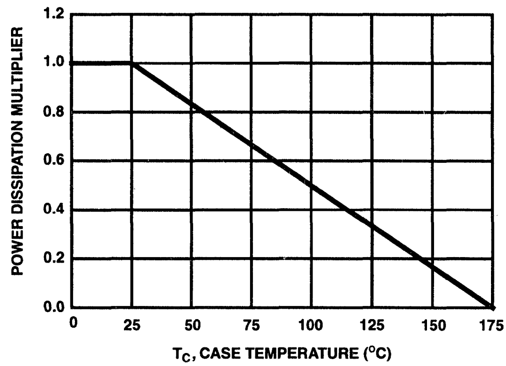


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

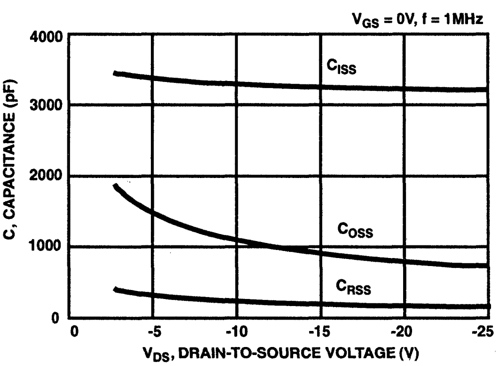


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

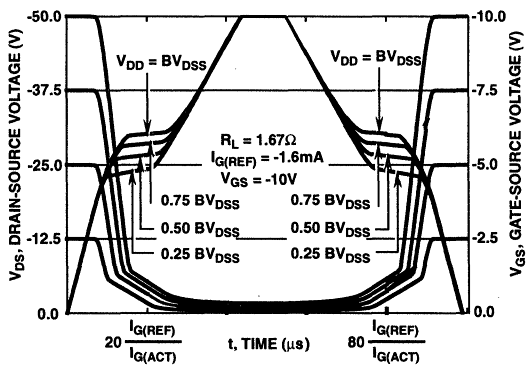


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

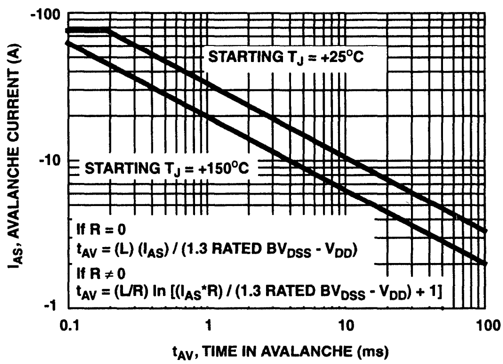


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

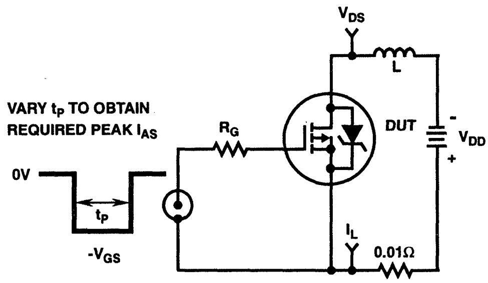


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

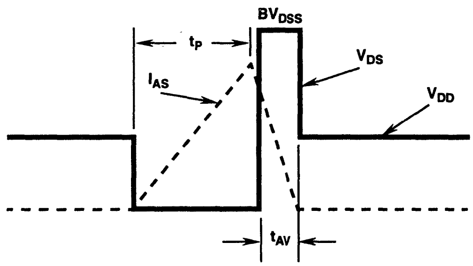


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

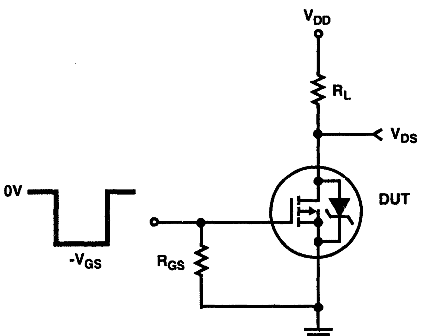


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

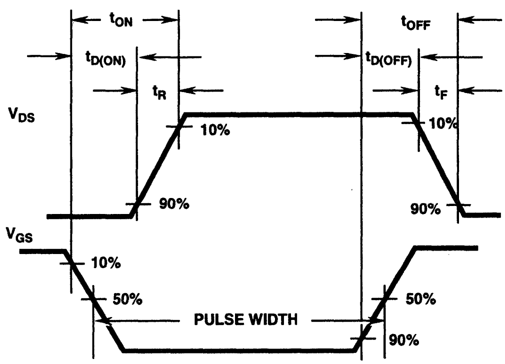
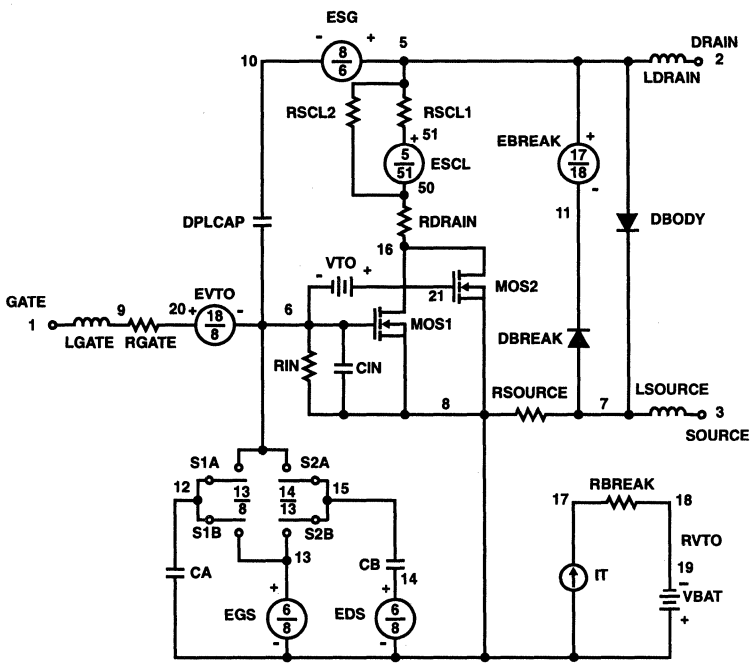


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFG30P05, RFP30P05, RF1S30P05, RF1S30P05SM

.SUBCKT RFP30P05 2 1 3;
REV 8/21/94



CA 12 8 3.23e-9
CB 15 14 3.23e-9
CIN 6 8 3.08e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -77.3
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.92e-9
LSOURCE 3 7 4.60e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 39.85e-3
RGATE 9 20 2.34
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 2.56e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.81

ESCL 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/114,5))}

.MODEL DBDMOD D (IS=4.7e-13 RS=1.31e-2 TRS1=1.39e-4 TRS2=-4.77e-6 CJO=2.85e-9 TT=8.81e-8)
.MODEL DBKMOD D (RS=2.23e-1 TRS1=1.97e-3 TRS2=-2.37e-5)
.MODEL DPLCAPMOD D (CJO=0.78e-9 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.75 KP=10.83 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=9.08e-4 TC2=-1.72e-6)
.MODEL RDSMOD RES (TC1=5.01e-3 TC2=1.02e-5)
.MODEL RSCLMOD RES (TC1=2.09e-3 TC2=5.88e-7)
.MODEL RVTOMOD RES (TC1=-2.99e-3 TC2=1.40e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.4 VOFF=1.4)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.4 VOFF=3.4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.2 VOFF=-3.8)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.8 VOFF=1.2)

.ENDS

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authors, William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFG30P06, RFP30P06, RF1S30P06, RF1S30P06SM

30A, 60V, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFETs

March 1995

Features

- 30A, 60V
- $r_{DS(ON)} = 0.065\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFG30P06, RFP30P06, RF1S30P06, and RF1S30P06SM P-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

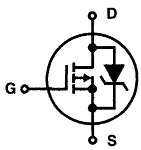
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFG30P06	TO-247	RFG30P06
RFP30P06	TO-220AB	RFP30P06
RF1S30P06	TO-262AA	F1S30P06
RF1S30P06SM	TO-263AB	F1S30P06

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S30P06SM9A.

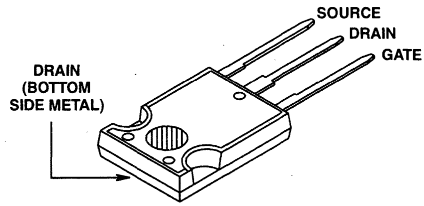
Formerly developmental type TA09834.

Symbol

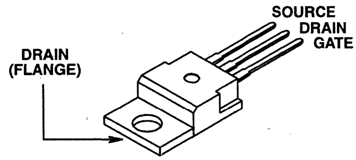


Packages

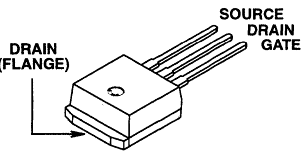
JEDEC STYLE TO-247



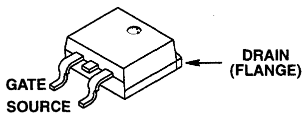
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = +25°C$

		RFG30P06, RFP30P06 RF1S30P06, RF1S30P06SM	UNITS
Drain Source Voltage	V_{DSS}	-60	V
Drain Gate Voltage	V_{DGR}	-60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	30	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25°C$	P_D	120	W
Derate above +25°C	P_T	0.9	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

File Number **2437.1**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		-2	-	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -60V, V_{GS} = 0V	T_C = +25°C	-	-	-1	μA
			T_C = +150°C	-	-	-50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 30A, V_{GS} = -10V		-	-	0.065	Ω
Turn-On Time	t_{ON}	V_{DD} = -30V, I_D = 15A, R_L = 2.00Ω, V_{GS} = -10V, R_{GS} = 6.25Ω		-	-	80	ns
Turn-On Delay Time	$t_{D(ON)}$			-	15	-	ns
Rise Time	t_R			-	23	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	28	-	ns
Fall Time	t_F			-	18	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to -20V	V_{DD} = -48V, I_D = 30A, R_L = 1.6Ω	-	140	170	nC
Gate Charge at -10V	$Q_{G(-10)}$	V_{GS} = 0 to -10V		-	70	85	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0 to -2V		-	5.5	6.6	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	3200	-	pF
Output Capacitance	C_{OSS}			-	800	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	175	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.11	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = -30A	-	-	-1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = -30A, dI_{SD}/dt = -100A/μs	-	-	150	ns

Typical Performance Curves

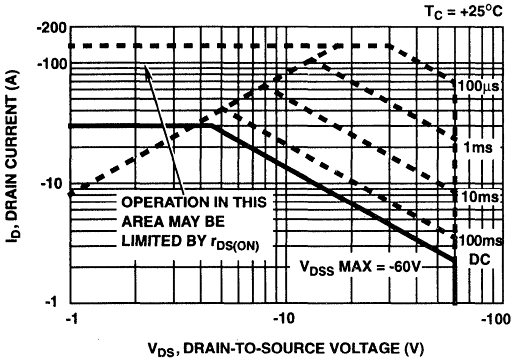


FIGURE 1. SAFE OPERATING AREA CURVE

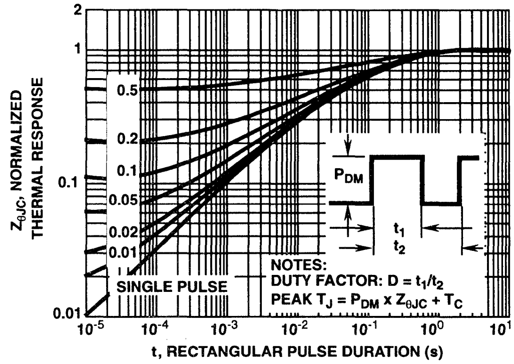


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

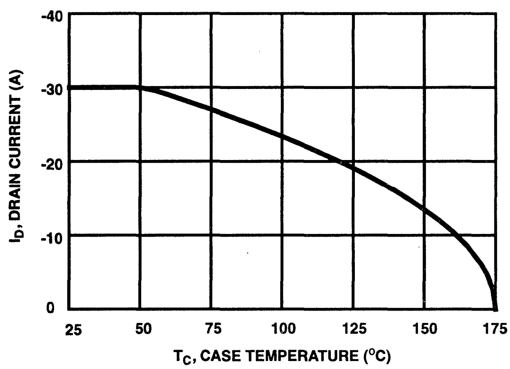


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

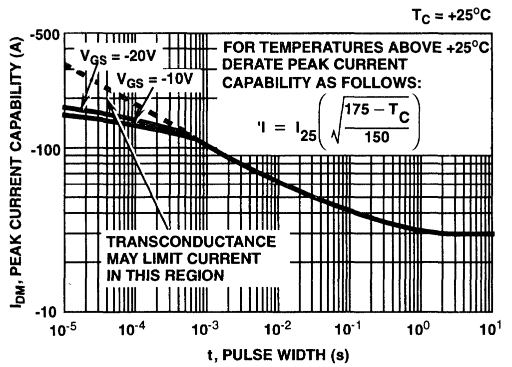


FIGURE 4. PEAK CURRENT CAPABILITY

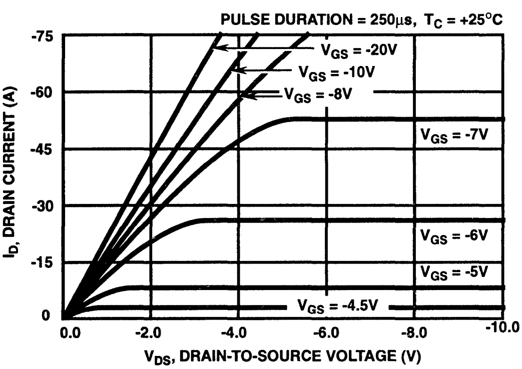


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

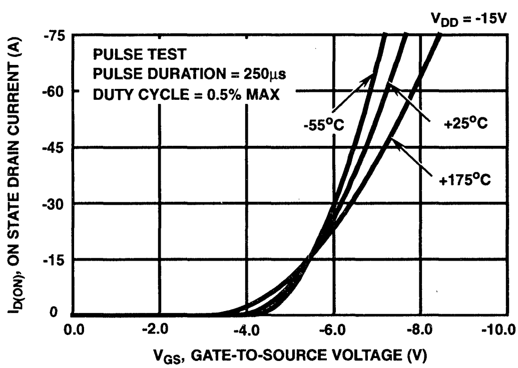


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

4

P-CHANNEL POWER MOSFETs

Typical Performance Curves (Continued)

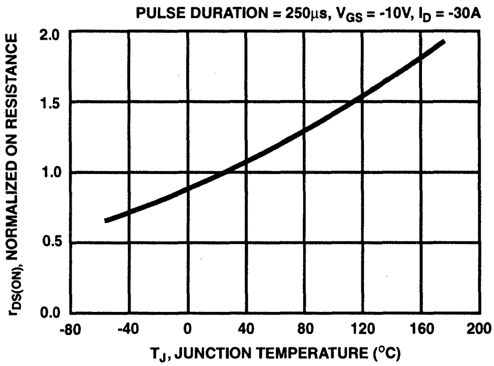


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

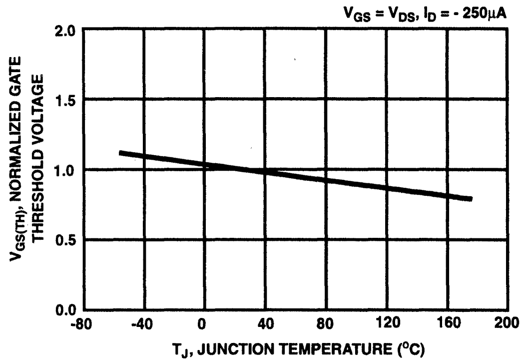


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

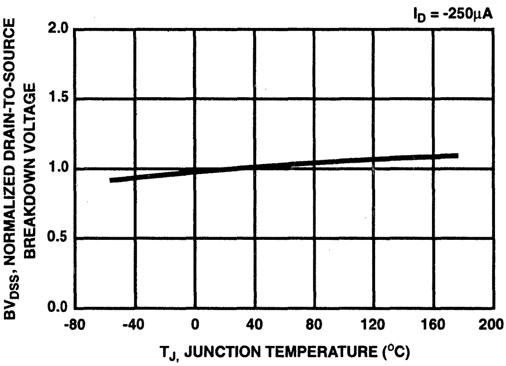


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

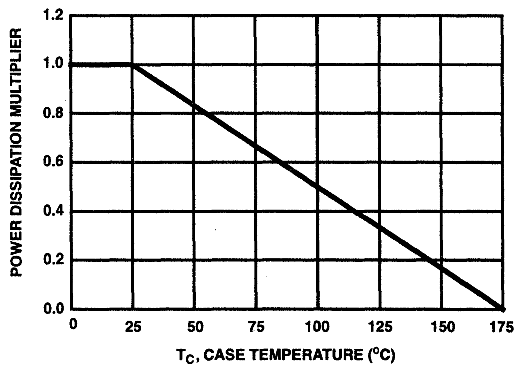


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

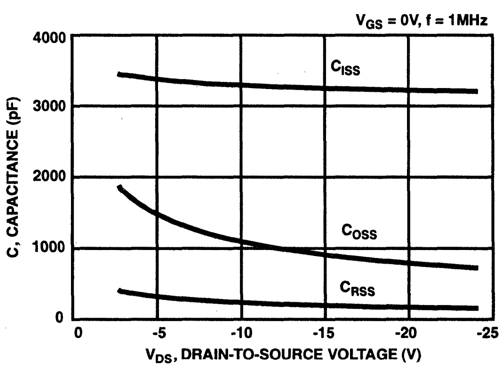


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

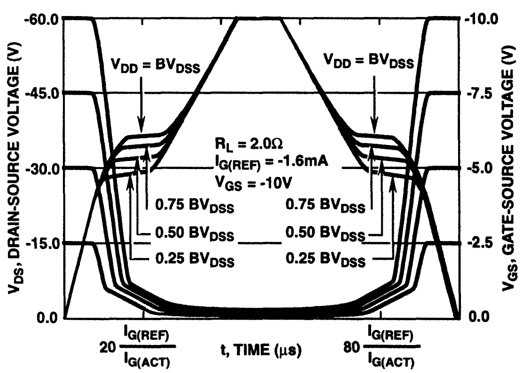


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

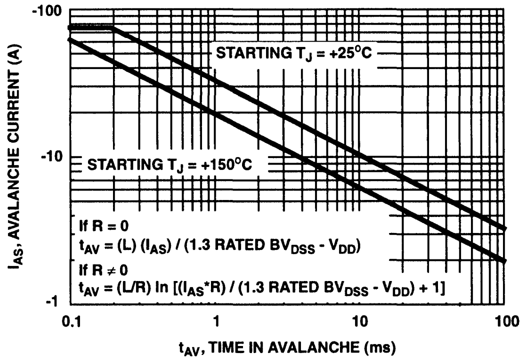


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

Test Circuits and Waveforms

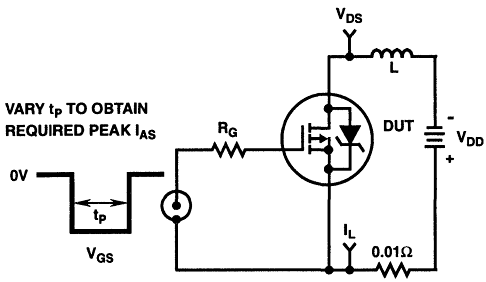


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

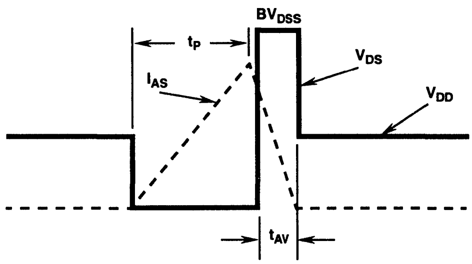


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

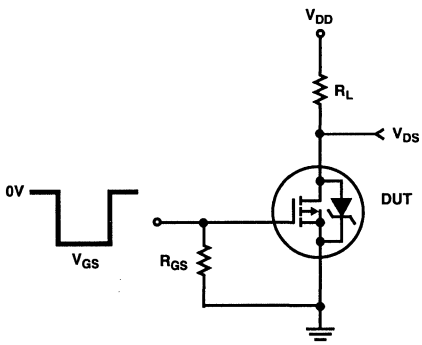


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

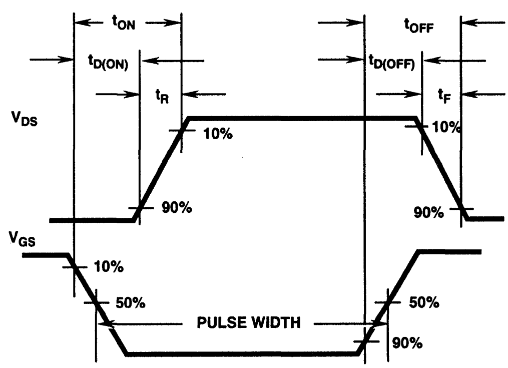


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFG30P06, RFP30P06, RF1S30P06, RF1S30P06SM

```
.SUBCKT RFP30P06 2 1 3;
REV 8/21/94

CA 12 8 3.23e-9
CB 15 14 3.23e-9
CIN 6 8 3.08e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -77.3
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.92e-9
LSOURCE 3 7 4.60e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 39.85e-3
RGATE 9 20 2.34
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 2.56e-3
RVTO 18 19 RVTOMOD 1

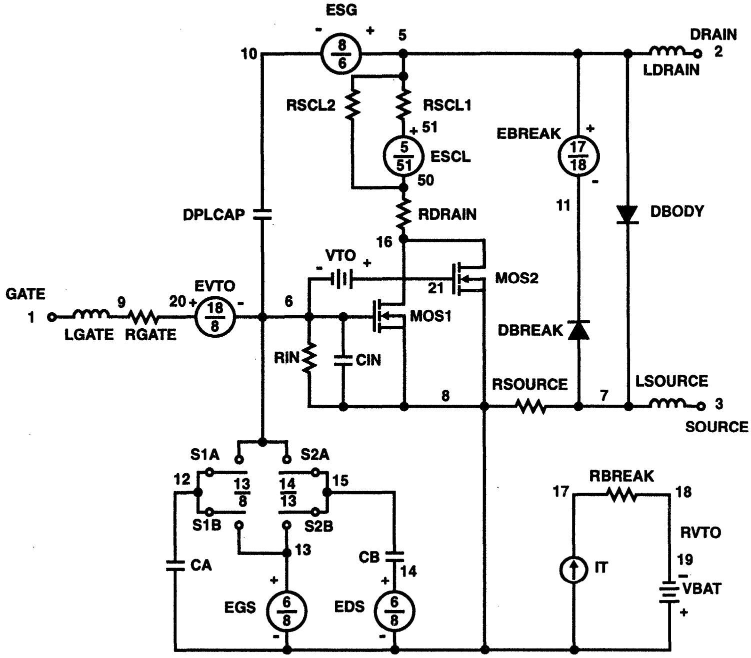
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.81

ESCL 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/114,5))}

.MODEL DBDMOD D (IS=4.7e-13 RS=1.31e-2 TRS1=1.39e-4 TRS2=-4.77e-6 CJO=2.85e-9 TT=8.81e-8)
.MODEL DBKMOD D (RS=2.23e-1 TRS1=1.97e-3 TRS2=-2.37e-5)
.MODEL DPLCAPMOD D (CJO=0.78e-9 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.75 KP=10.83 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=9.08e-4 TC2=-1.72e-6)
.MODEL RDSMOD RES (TC1=5.01e-3 TC2=1.02e-5)
.MODEL RSCLMOD RES (TC1=2.09e-3 TC2=5.88e-7)
.MODEL RVTOMOD RES (TC1=-2.99e-3 TC2=1.40e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=3.4 VOFF=1.4)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.4 VOFF=3.4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.2 VOFF=-3.8)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.8 VOFF=1.2)

.ENDS
```



NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authors, William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFG60P03, RFP60P03, RF1S60P03, RF1S60P03SM

60A, 30V, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 60A, 30V
- $r_{DS(ON)} = 0.027\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFG60P03, RFP60P03, RF1S60P03 and RF1S60P03SM P-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

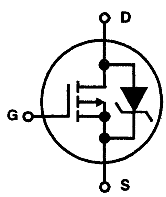
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFG60P03	TO-247	RFG60P03
RFP60P03	TO-220AB	RFP60P03
RF1S60P03	TO-262AA	F1S60P03
RF1S60P03SM	TO-263AB	F1S60P03

NOTE: When ordering use the entire part number.

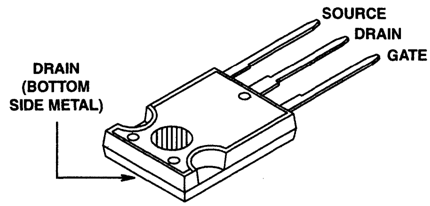
Formerly developmental type TA49045.

Symbol

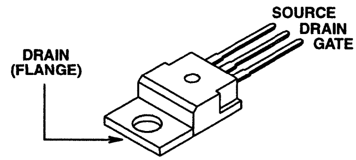


Packages

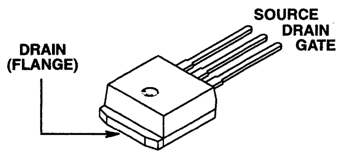
JEDEC STYLE TO-247



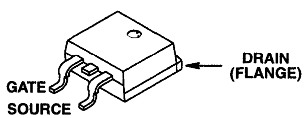
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = +25^oC$

		RFG60P03, RFP60P03, RF1S60P03, RFS60P03SM	UNITS
Drain Source Voltage	V_{DSS}	-30	V
Drain Gate Voltage	V_{DGR}	-30	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	60	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	176	W
Derate above +25°C	P_T	1.17	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

File Number **3951.1**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		-30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		-2	-	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	-1	µA
			$T_C = +150^oC$	-	-	-50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 60A$, $V_{GS} = -10V$		-	-	0.027	Ω
Turn-On Time	t_{ON}	$V_{DD} = -15V$, $I_D = 60A$ $R_L = 0.25\Omega$, $V_{GS} = -10V$ $R_{GS} = 2.5\Omega$		-	-	140	ns
Turn-On Delay Time	$t_{D(ON)}$			-	20	-	ns
Rise Time	t_R			-	75	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	35	-	ns
Fall Time	t_F			-	40	-	ns
Turn-Off Time	t_{OFF}			-	-	115	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0$ to $-20V$	$V_{DD} = -24V$, $I_D = 60A$, $R_L = 0.4\Omega$	-	190	230	nC
Gate Charge at 10V	$Q_{G(-10)}$	$V_{GS} = 0$ to $-10V$		-	100	120	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0$ to $-2V$		-	7.5	9	nC
Input Capacitance	C_{ISS}	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz		-	3000	-	pF
Output Capacitance	C_{OSS}			-	1500	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	525	-	pF
Thermal Resistance, Junction to Case	$R_{\theta JC}$			-	-	0.85	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = -60A$	-	-	-1.75	V
Reverse Recovery Time	t_{RR}	$I_{SD} = -60A$, $dI_{SD}/dt = -100A/\mu s$	-	-	200	ns

Typical Performance Curves

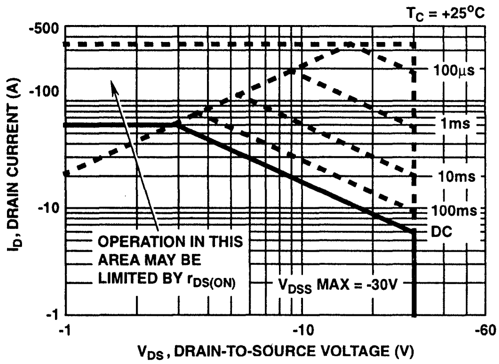


FIGURE 1. SAFE OPERATING AREA CURVE

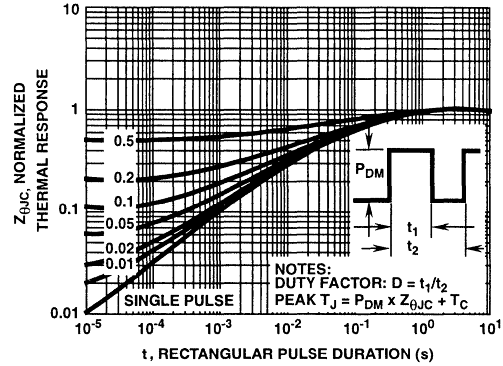


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

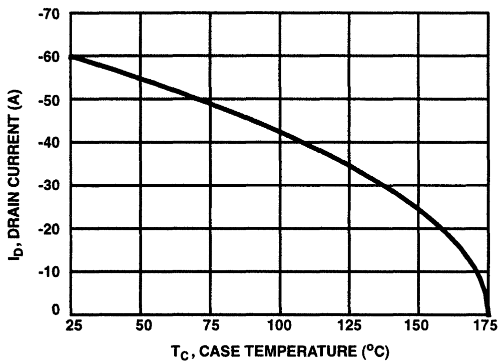


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

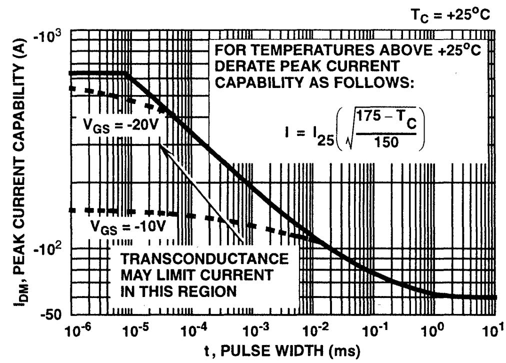


FIGURE 4. PEAK CURRENT CAPABILITY

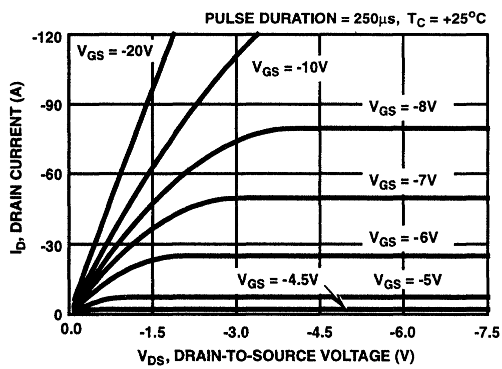


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

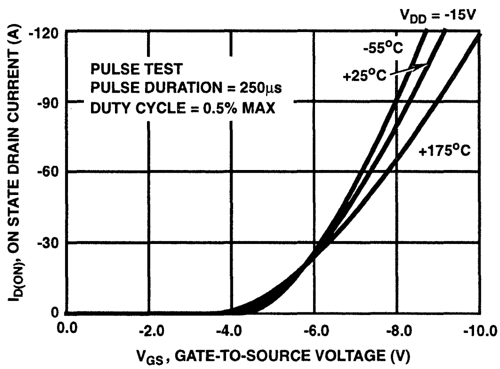


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

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P-CHANNEL POWER MOSFETs

Typical Performance Curves (Continued)

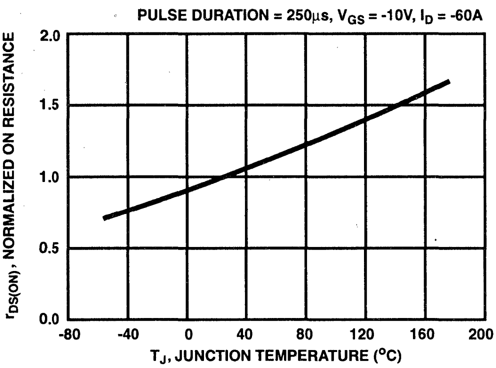


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

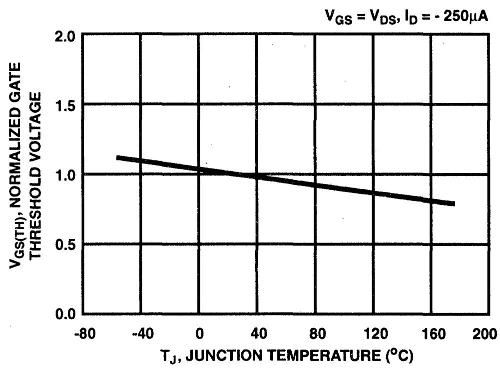


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

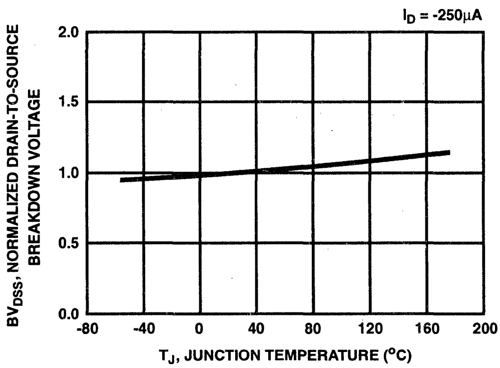


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

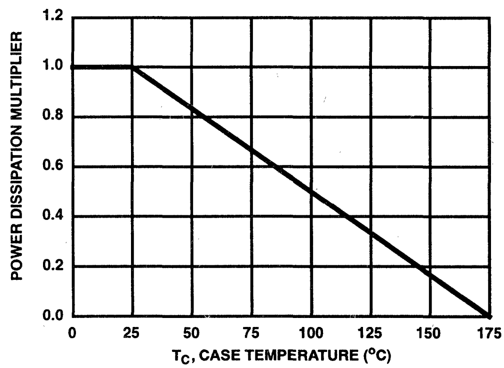


FIGURE 10. NORMALIZED SWITCHING WAVEFORMS

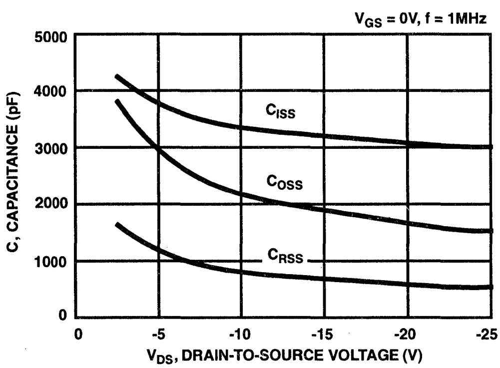


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

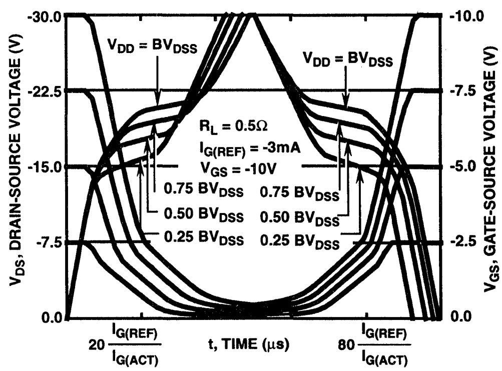


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

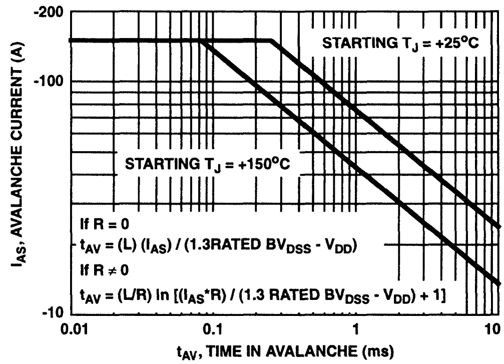


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

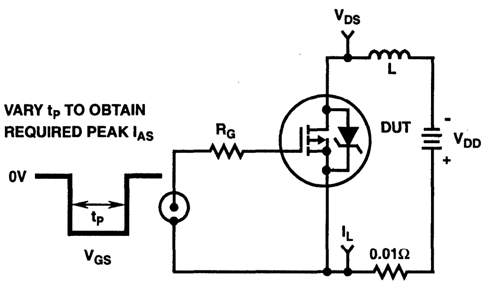


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

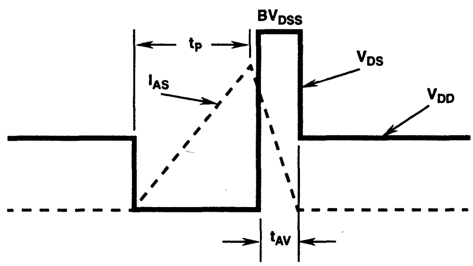


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

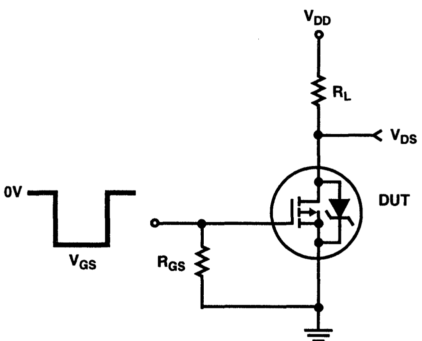


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

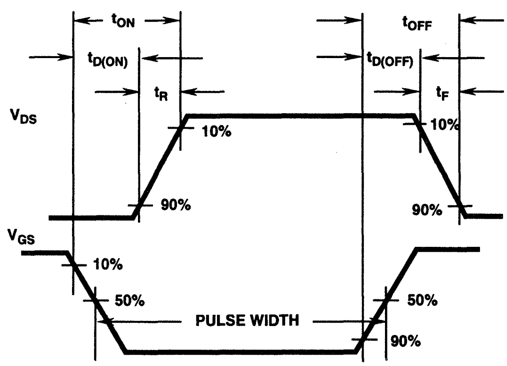
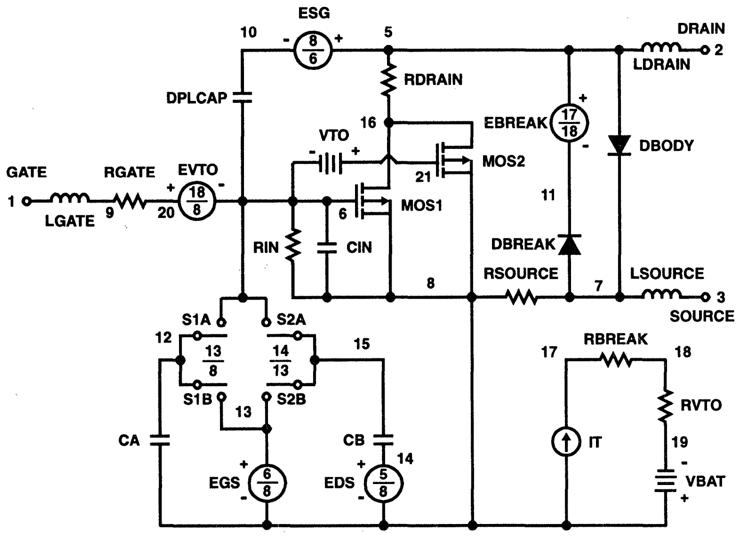


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFG60P03, RFP60P03, RF1S60P03, RF1S60P03SM




```
.SUBCKT RFP60P03  2  1  3                                    REV 6/21/94

CA 12 8 5.01e-9
CB 15 14 3.9e-9
CIN 6 8 3.09e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -36.59
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.92e-9
LSOURCE 3 7 2.36e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 1e-4
RGATE 9 20 3.25
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 11.28e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.92

.MODEL DBDMOD D (IS=4.21e-13 RS=1e-2 TRS1=-2.69e-4 TRS2=-1.33e-6 CJO=5.05e-9 TT=5.33e-8)
.MODEL DBKMOD D (RS=3.80e-2 TRS1=-4.76e-4 TRS2=-4.17e-12)
.MODEL DPLCAPMOD D (CJO=4.05e-9 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.98 KP=16.27 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=8.05e-4 TC2=1.48e-6)
.MODEL RDSMOD RES (TC1=2.80e-3 TC2=2.62e-6)
.MODEL RVTOMOD RES (TC1=-3.34e-3 TC2=1.46e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=7.5 VOFF=4.5)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=4.5 VOFF=7.5)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.43 VOFF=-3.57)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.57 VOFF=1.43)

.ENDS
```

NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authors, William J. Hepp and C. Frank Wheatley.

RFG60P05E

HARRIS SEMICONDUCTOR

60A, 50V, ESD Rated, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFET

December 1995

Features

- 60A, 50V
- $r_{DS(ON)} = 0.030\Omega$
- *Temperature Compensating* PSPICE Model
- 2kV ESD Rated
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFG60P05E P-Channel power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

PACKAGE AVAILABILITY

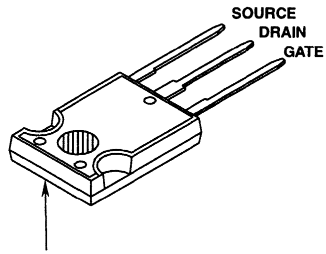
PART NUMBER	PACKAGE	BRAND
RFG60P05E	TO-247	RFG60P05E

NOTE: When ordering use the entire part number.

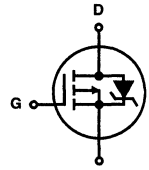
Formerly developmental type TA09835.

Package

JEDEC STYLE TO-247



Symbol



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P-CHANNEL POWER MOSFETs

Absolute Maximum Ratings $T_C = +25^oC$

		RFG60P05E	UNITS
Drain Source Voltage	V_{DSS}	-50	V
Drain Gate Voltage	V_{DGR}	-50	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	60	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	E_{SD}	2	KV
Power Dissipation			
$T_C = +25^oC$	P_D	215	W
Derate above +25°C		1.43	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2745.4**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		-50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		-2	-	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -50V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	-1	µA
			$T_C = +150^oC$	-	-	-50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 60A$, $V_{GS} = -10V$		-	-	0.030	Ω
Turn-On Time	t_{ON}	$V_{DD} = -25V$, $I_D = 30A$ $R_L = 0.83\Omega$, $V_{GS} = -10V$ $R_{GS} = 2.5\Omega$		-	-	125	ns
Turn-On Delay Time	$t_{D(ON)}$			-	20	-	ns
Rise Time	t_R			-	60	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	65	-	ns
Fall Time	t_F			-	20	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0$ to $-20V$	$V_{DD} = -40V$, $I_D = 60A$, $R_L = 0.67\Omega$	-		450	nC
Gate Charge at -10V	$Q_{G(-10)}$	$V_{GS} = 0$ to $-10V$		-		225	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0$ to $-2V$		-		15	nC
Input Capacitance	C_{ISS}	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz		-	7200	-	pF
Output Capacitance	C_{OSS}			-	1700	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	325	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.70	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = -60A$	-	-	-1.75	V
Reverse Recovery Time	t_{RR}	$I_{SD} = -60A$, $dI_{SD}/dt = -100A/\mu s$	-	-	200	ns

Typical Performance Curves

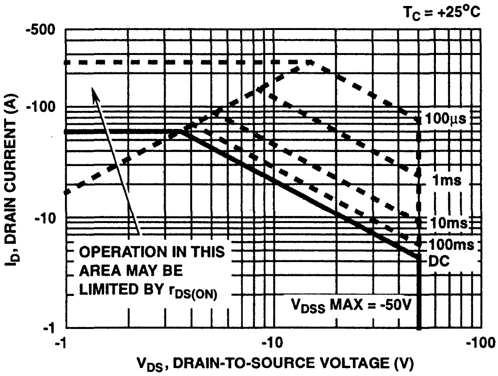


FIGURE 1. SAFE OPERATING AREA CURVE

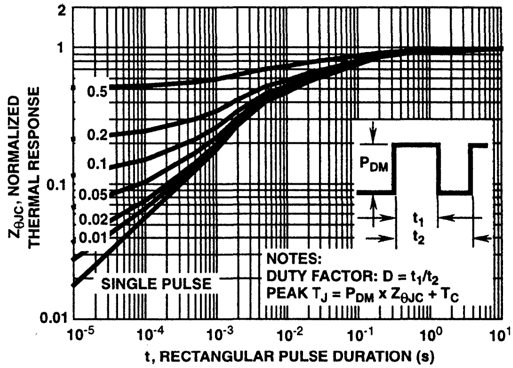


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

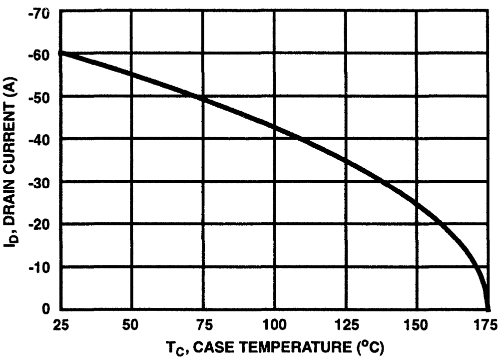


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

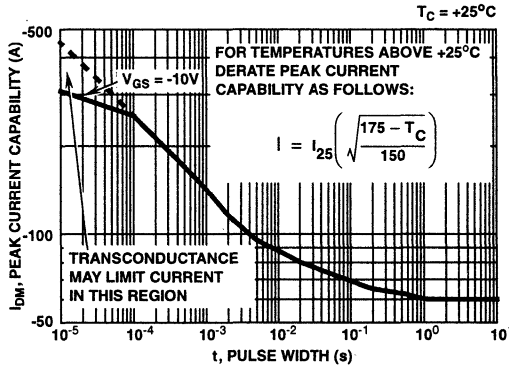


FIGURE 4. PEAK CURRENT CAPABILITY

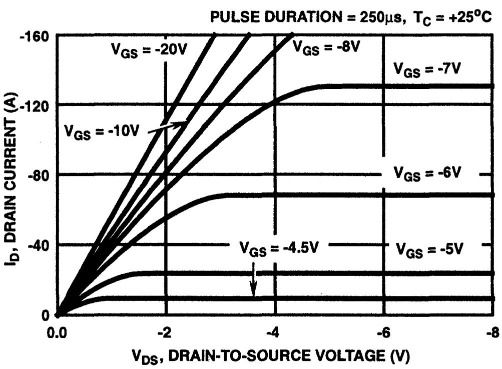


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

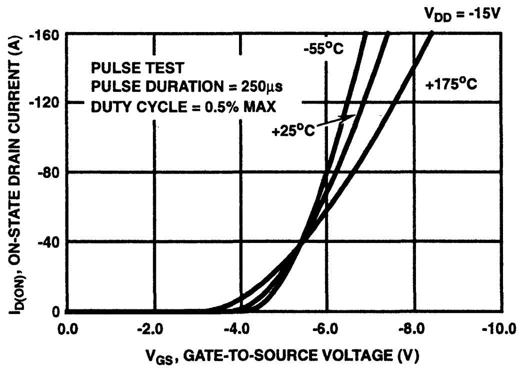


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

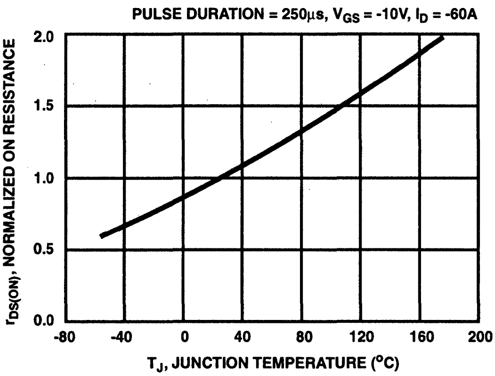


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

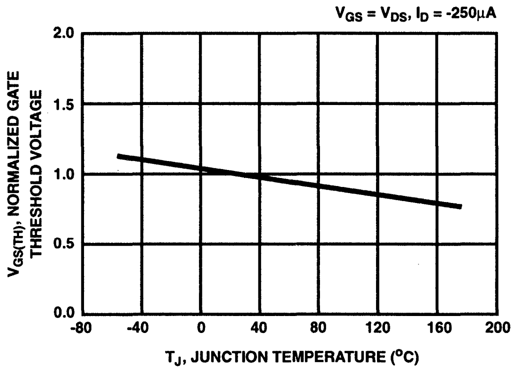


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

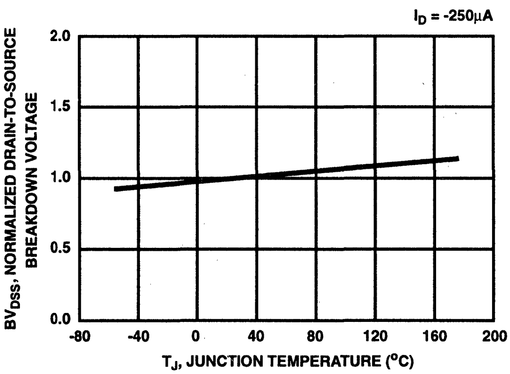


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

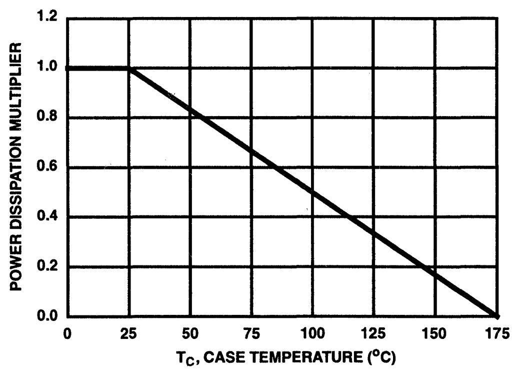


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

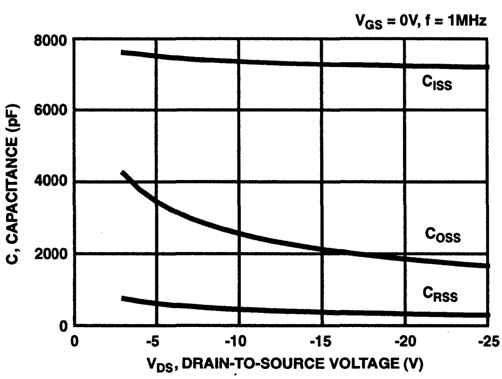


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

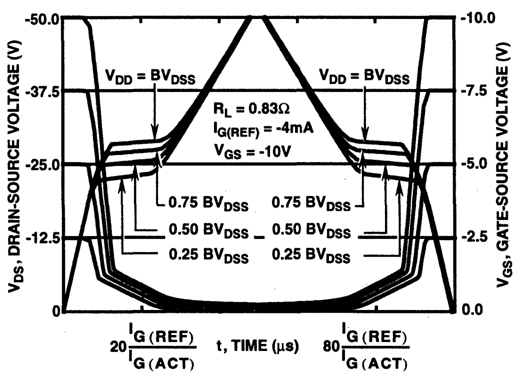


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

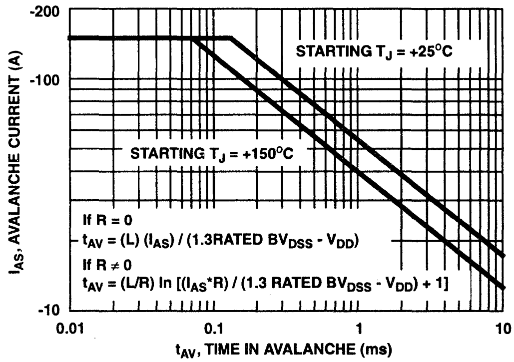


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

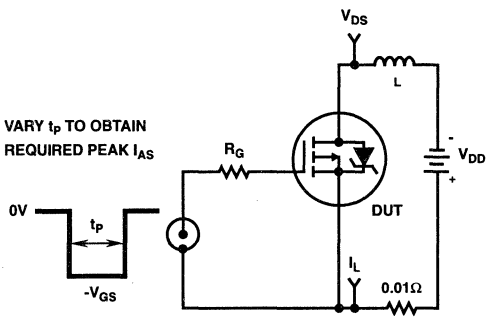


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

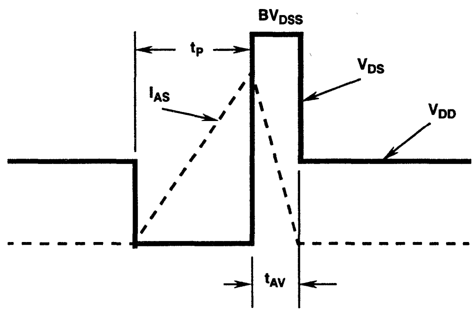


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

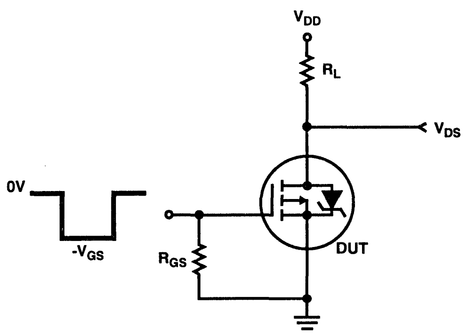


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

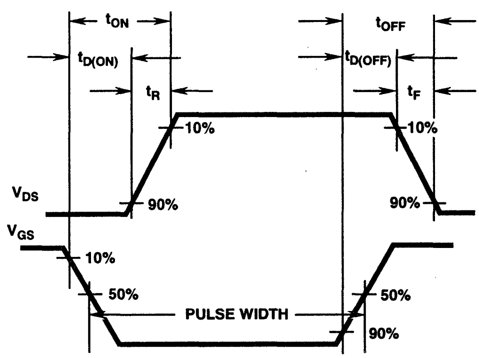


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

4
P-CHANNEL POWER MOSFETs

Temperature Compensated PSPICE Model for the RFG60P05E

.SUBCKT RFG60P05E 2 1 3; REV 9/20/94

CA 12 8 1.01e-8
CB 15 14 1.05e-8
CIN 6 8 6.9e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -76.35
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

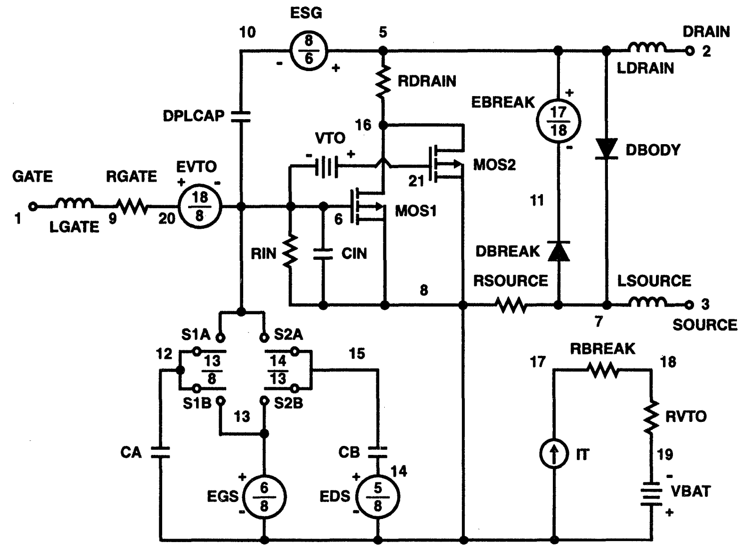
LDRAIN 2 5 1e-9
LGATE 1 9 7.9e-9
LSOURCE 3 7 4.18e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 12.83e-3
RGATE 9 20 1.5
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 3.25e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.83



.MODEL DBDMOD D (IS = 1.24e-12 RS = 4.72e-3 TRS1 = 1.43e-3 TRS2 = -4.91e-7 CJO = 6.98e-9 TT = 1.5e-7)
.MODEL DBKMOD D (RS = 1.11e-1 TRS1 = 1.34e-3 TRS2 = 4.46e-12)
.MODEL DPLCAPMOD D (CJO = 15e-10 IS = 1e-30 N = 10)
.MODEL MOSMOD PMOS (VTO = -3.71 KP = 31.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 9.42e-4 TC2 = 0)
.MODEL RDSMOD RES (TC1 = 5.85e-3 TC2 = 7.69e-6)
.MODEL RVTOMOD RES (TC1 = -3.39e-3 TC2 = 1.07e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 4.6 VOFF = 2.6)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.6 VOFF = 4.6)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.16 VOFF = -3.84)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.84 VOFF = 1.16)

.ENDS
For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options;** written by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFG60P06E

60A, 60V, ESD Rated, Avalanche Rated, P-Channel Enhancement-Mode Power MOSFET

January 1996

Features

- 60A, 60V
- $r_{DS(ON)} = 0.030\Omega$
- *Temperature Compensating* PSPICE Model
- 2kV ESD Rated
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFG60P06E P-Channel power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

The RFG60P06E incorporates ESD protection an is designed to withstand 2kV (Human Body Model) of ESD.

PACKAGE AVAILABILITY

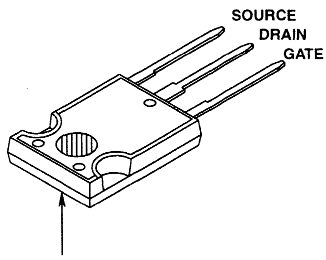
PART NUMBER	PACKAGE	BRAND
RFG60P06E	TO-247	RFG60P06E

NOTE: When ordering use the entire part number RFG60P06E.

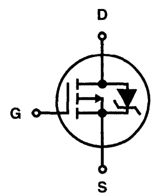
Formerly developmental type TA09835.

Package

JEDEC STYLE TO-247



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		RFG60P06E	UNITS
Drain Source Voltage	V_{DSS}	-60	V
Drain Gate Voltage	V_{DGR}	-60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	60	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	E_{SD}	2	KV
Power Dissipation			
$T_C = +25^oC$	P_D	215	W
Derate above +25°C		1.43	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		-2	-	-4	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	-1	µA
			$T_C = +150^oC$	-	-	-50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 60A$, $V_{GS} = -10V$		-	-	0.030	Ω
Turn-On Time	t_{ON}	$V_{DD} = -30V$, $I_D = 30A$ $R_L = 1.0\Omega$, $V_{GS} = -10V$ $R_{GS} = 2.5\Omega$		-	-	125	ns
Turn-On Delay Time	$t_{D(ON)}$			-	20	-	ns
Rise Time	t_R			-	60	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	65	-	ns
Fall Time	t_F			-	20	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0$ to $-20V$	$V_{DD} = -48V$, $I_D = 60A$, $R_L = 0.8\Omega$	-	-	450	nC
Gate Charge at -10V	$Q_{G(-10)}$	$V_{GS} = 0$ to $-10V$		-	-	225	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0$ to $-2V$		-	-	15	nC
Input Capacitance	C_{ISS}	$V_{DS} = -25V$, $V_{GS} = 0V$ f = 1MHz		-	7200	-	pF
Output Capacitance	C_{OSS}			-	1700	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	325	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	0.70	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = -60A$	-	-	-1.75	V
Reverse Recovery Time	t_{RR}	$I_{SD} = -60A$, $dI_{SD}/dt = -100A/\mu s$	-	-	200	ns

Typical Performance Curves

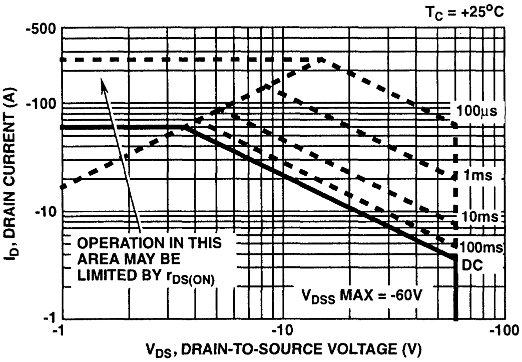


FIGURE 1. SAFE OPERATING AREA CURVE

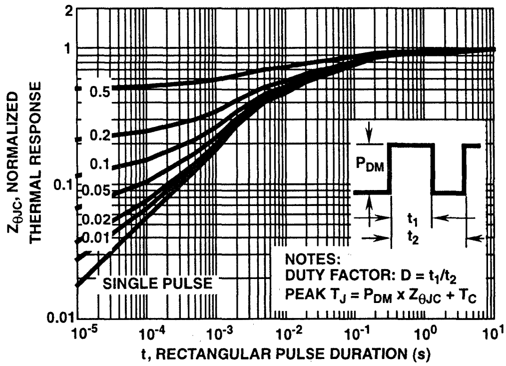


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

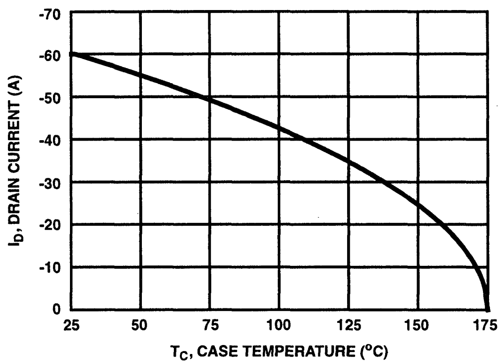


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

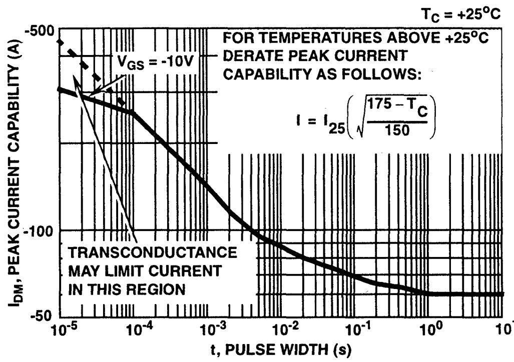


FIGURE 4. PEAK CURRENT CAPABILITY

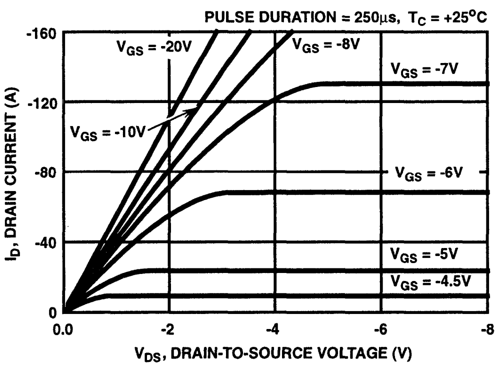


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

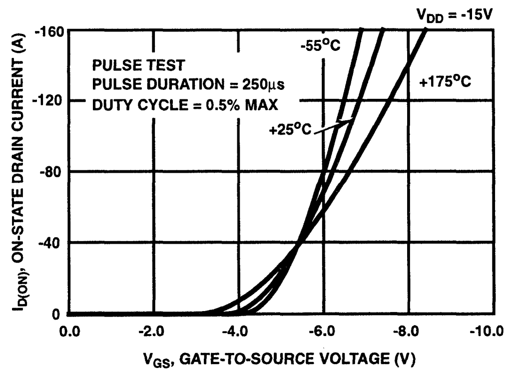


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

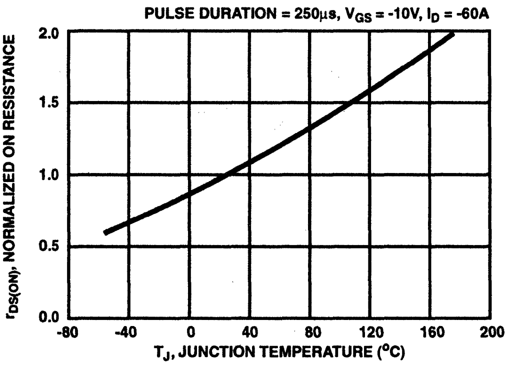


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

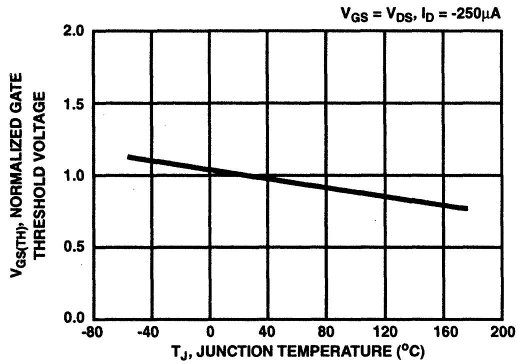


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

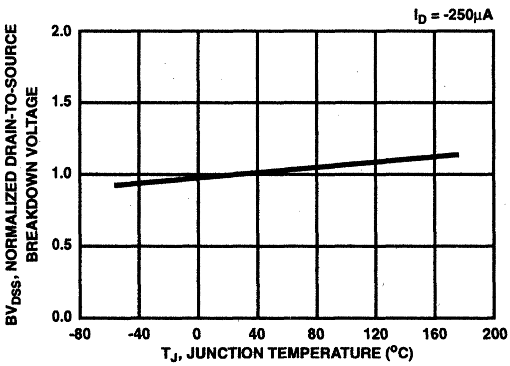


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

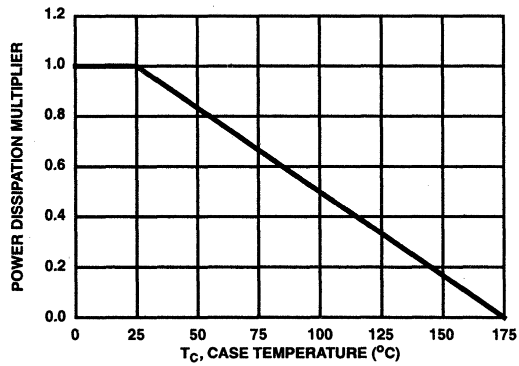


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

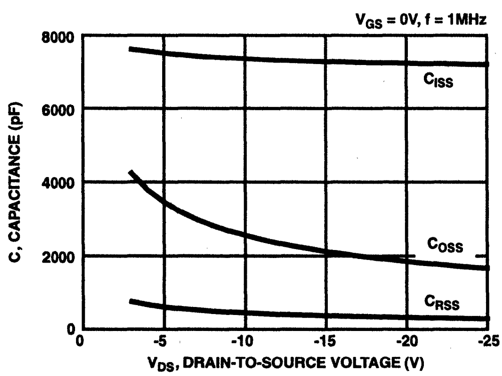


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

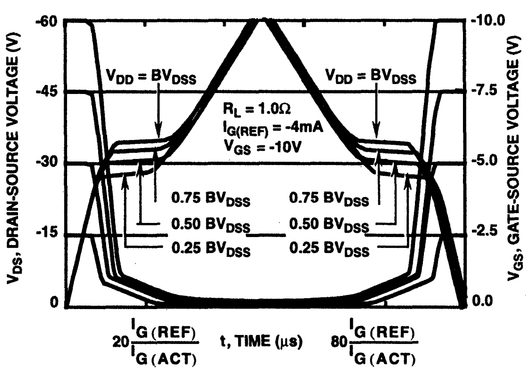


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

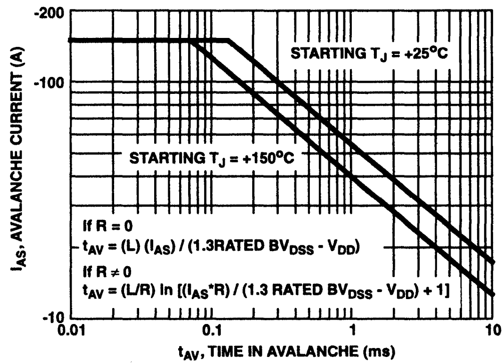


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

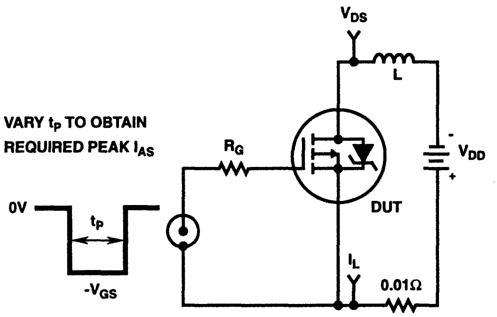


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

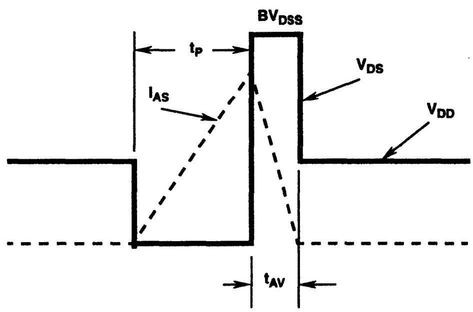


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

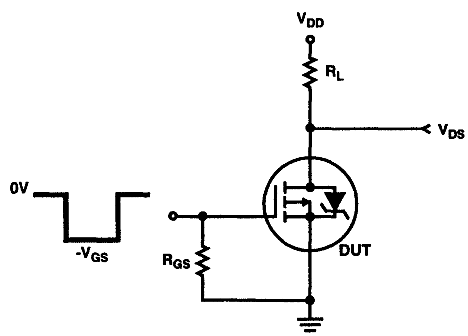


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

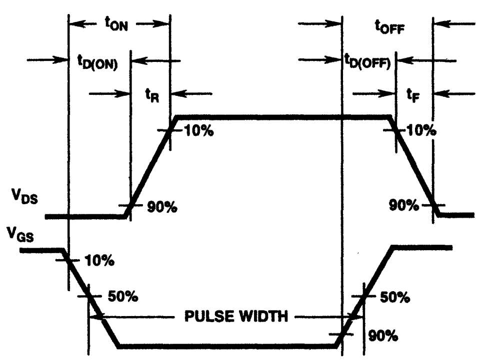


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFG60P06E

```
.SUBCKT  RFG60P06E   2 1 3;      REV 9/20/94

CA 12 8 1.01e-8
CB 15 14 1.05e-8
CIN 6 8 6.9e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 6 DPLCAPMOD

EBREAK 5 11 17 18 -76.35
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 5 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 7.9e-9
LSOURCE 3 7 4.18e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

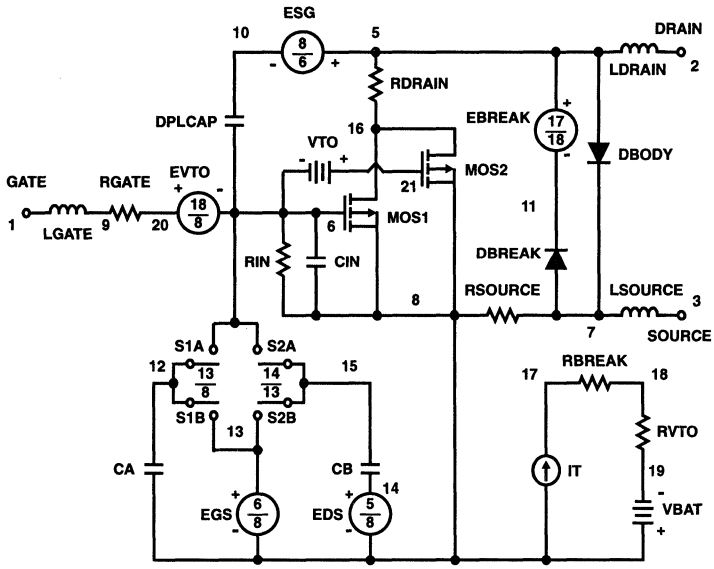
RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 12.83e-3
RGATE 9 20 1.5
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 3.25e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.83

.MODEL DBDMOD D (IS=1.24e-12 RS=4.72e-3 TRS1=1.43e-3 TRS2=-4.91e-7 CJO=6.98e-9 TT=1.5e-7)
.MODEL DBKMOD D (RS=1.11e-1 TRS1=1.34e-3 TRS2=4.46e-12)
.MODEL DPLCAPMOD D (CJO=15e-10 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.71 KP=31.5 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=9.42e-4 TC2=0)
.MODEL RDSMOD RES (TC1=5.85e-3 TC2=7.69e-6)
.MODEL RVTOMOD RES (TC1=-3.39e-3 TC2=1.07e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=4.6 VOFF=2.6)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=2.6 VOFF=4.6)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.16 VOFF=-3.84)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.84 VOFF=1.16)

.ENDS
```



NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFF60P06

25A†, 60V, Hermetically Packaged, Avalanche Rated P-Channel Enhancement-Mode Power MOSFET

December 1995

Features

- 25A†, 60V
- $r_{DS(ON)} = 0.030\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +150°C Operating Temperature
- Reliability Screened

Description

The RFF60P06 P-Channel power MOSFET is manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits gives optimum utilization of silicon, resulting in outstanding performance. It was designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Reliability screening is available as either commercial or TX/TXV equivalent of MIL-S-19500. Contact Harris Semiconductor High-Reliability Marketing group for any desired deviations from the data sheet.

PACKAGING AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFF60P06	TO-254AA	RFF60P06

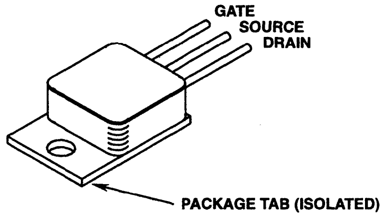
NOTE: When ordering, use the entire part number.

Formerly developmental type TA09835.

Commercial Version: RFG60P06E.

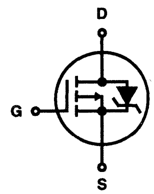
Package

TO-254AA



CAUTION: Beryllia Warning per MIL-S-19500 refer to package specifications.

Symbol



4

P-CHANNEL POWER MOSFETs

Absolute Maximum Ratings $T_C = +25^oC$

		RFF60P06	UNITS
Drain Source Voltage	V_{DSS}	-60	V
Drain Gate Voltage	V_{DGR}	-60	V
Gate Source Voltage	V_{GS}	±20	V
Drain Current			
RMS Continuous	I_D	25†	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Single Pulse Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	125	W
Derate above +25°C		1.0	W/°C
Operating and Storage Temperature	T_J, T_{STG}	-55 to +150	°C
Lead Temperature (During Soldering) (Distance >0.063in. (1.6mm) from Case, 10s Max.)	T_L	300	°C

† Current is limited by the package capability

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **3975.1**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		-60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		-2.0	-3.0	-4.5	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -48V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	-25	µA
			$T_C = +125^oC$	-	-	-250	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$	$T_C = +25^oC$	-	-	100	nA
			$T_C = +125^oC$	-	-	100	µA
On Resistance	$r_{DS(ON)}$	$I_D = 25A$, $V_{GS} = -10V$		-	-	0.030	Ω
Turn-On Time	t_{ON}	$V_{DD} = -30V$, $I_D = 25A$, $R_L = 1.2\Omega$, $V_{GS} = -10V$, $R_{GS} = 2.35\Omega$		-	-	195	ns
Turn-On Delay Time	$t_{D(ON)}$			-	25	70	ns
Rise Time	t_R			-	50	125	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	80	200	ns
Fall Time	t_F			-	30	75	ns
Turn-Off Time	t_{OFF}			-	-	275	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0$ to $-20V$	$V_{DD} = -30V$, $I_D = 25A$, $R_L = 1.2\Omega$	-	-	450	nC
Gate Charge at -10V	$Q_{G(-10)}$	$V_{GS} = 0$ to $-10V$		-	-	225	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0$ to $-2V$		-	-	15	nC
Input Capacitance	C_{ISS}	$V_{DS} = -25V$, $V_{GS} = 0V$, f = 1MHz		-	7200	-	pF
Output Capacitance	C_{OSS}			-	1800	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	400	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.0	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	48	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = -25A$	-	-1.1	-1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = -25A$, $dI_{SD}/dt = -100A/\mu s$	-	130	200	ns

Typical Performance Curves

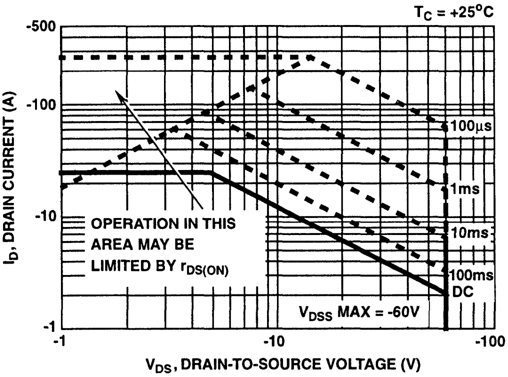


FIGURE 1. SAFE OPERATING AREA CURVE

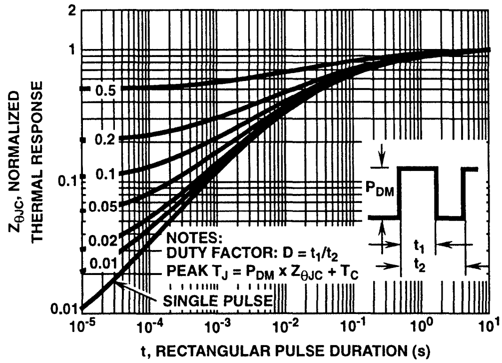


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

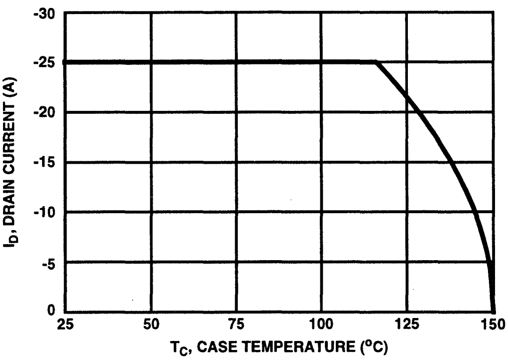


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

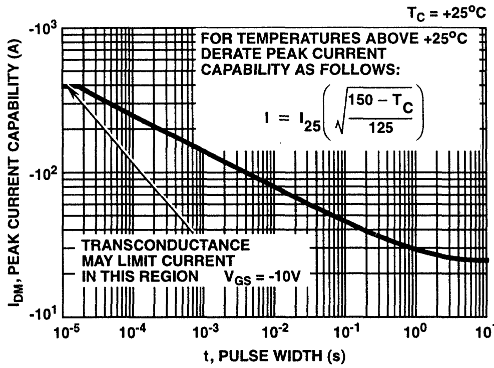


FIGURE 4. PEAK CURRENT CAPABILITY

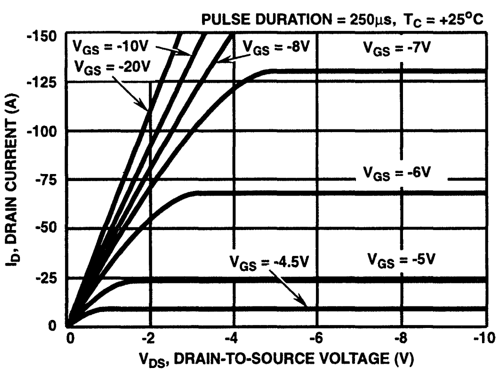


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

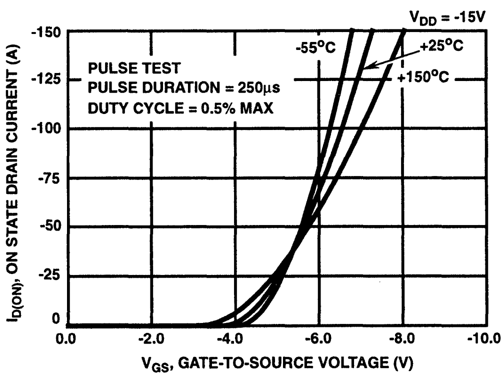


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

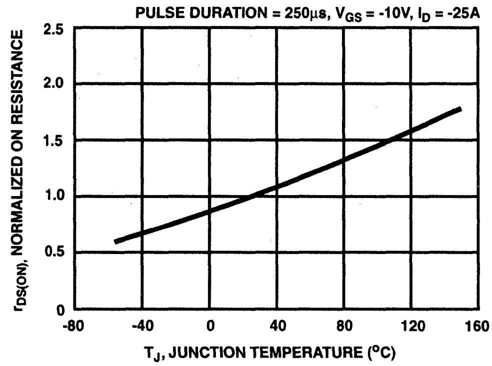


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

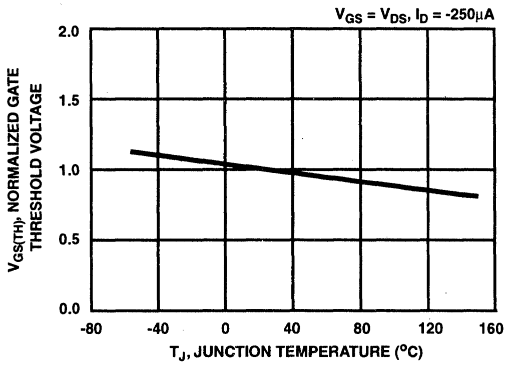


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

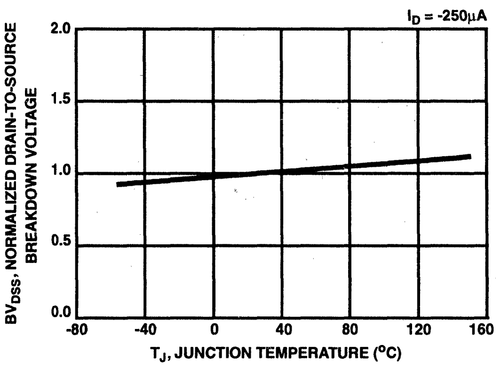


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

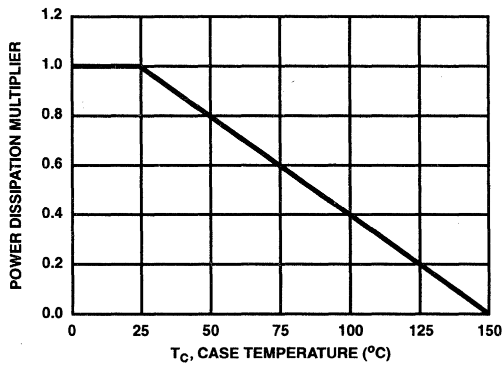


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE.

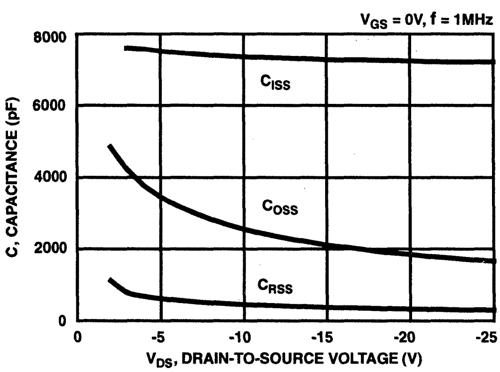


FIGURE 11. TYPICAL CAPACITANCE vs VOLTAGE

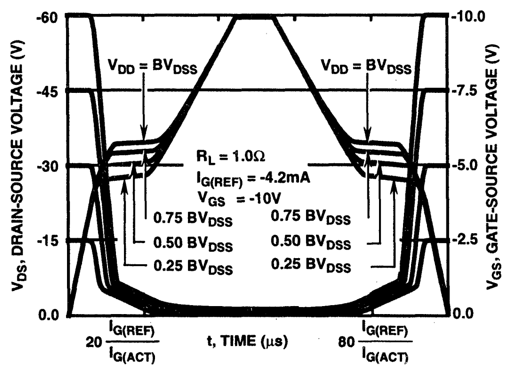


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO APPLICATION NOTE AN7254 AND AN7260

Typical Performance Curves (Continued)

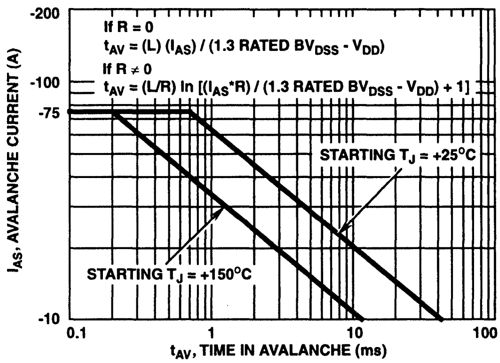


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

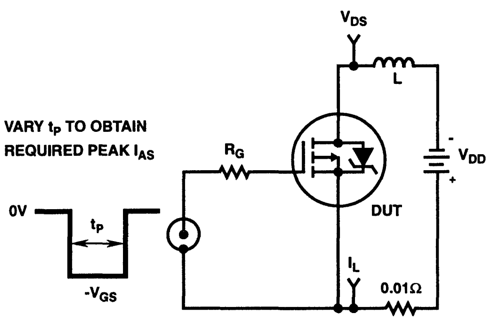


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

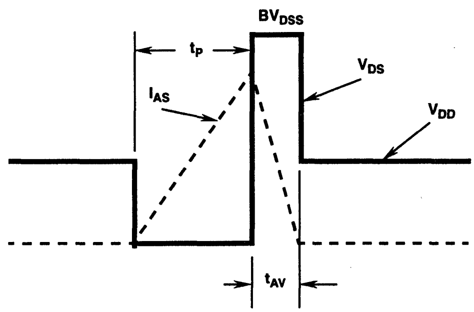


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

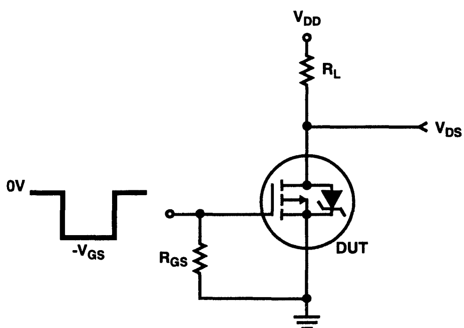


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

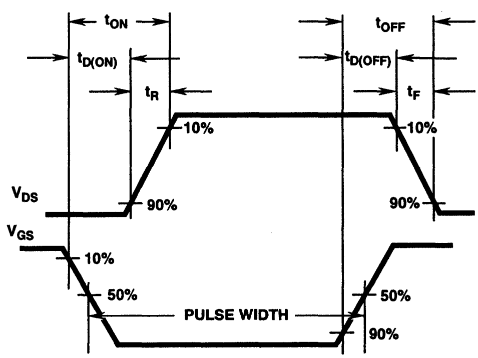


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Test Circuits and Waveforms (Continued)

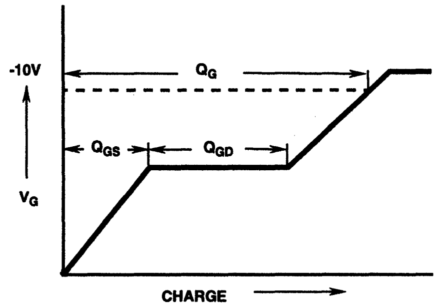


FIGURE 18. BASIC GATE CHARGE WAVEFORM

Data Packages - Harris Power Transistors

TX and TXV Equivalents

1. TX/TXV Equivalent - Standard Data Package
   - A. Certificate of Compliance
   - B. Assembly Flow Chart
   - C. Preconditioning - Attributes Data Sheet
   - D. Group A - Attributes Data Sheet
   - E. Group B - Attributes Data Sheet
   - F. Group C - Attributes Data Sheet
2. TX/TXV Equivalent - Optional Data Package
   - A. Certificate of Compliance
   - B. Assembly Flow Chart
   - C. Preconditioning
     - Attributes Data Sheet
     - Precondition Lot Traveler
     - Pre and Post Burn-In Read and Record Data
   - D. Group A
     - Attributes Data Sheet
     - Group A Lot Traveler
   - E. Group B
     - Attributes Data Sheet
     - Group B Lot Traveler
     - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup B3)
     - Bond Strength Data (Subgroup B3)
     - Pre and Post High Temperature Operating Life Read and Record Data (Subgroup B6)
   - F. Group C
     - Attributes Data Sheet
     - Group C Lot Traveler
     - Pre and Post Read and Record Data for Intermittent Operating Life (Subgroup C6)
     - Bond Strength Data (Subgroup C6)

Temperature Compensated PSPICE Model for the RFF60P06

```
.SUBCKT RFF60P06  2  1  3                    REV 9/20/94

CA 12 8 1.01e-8
CB 15 14 1.05e-8
CIN 6 8 6.9e-9

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 5 11 17 18 -76.35
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 7.9e-9
LSOURCE 3 7 4.18e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

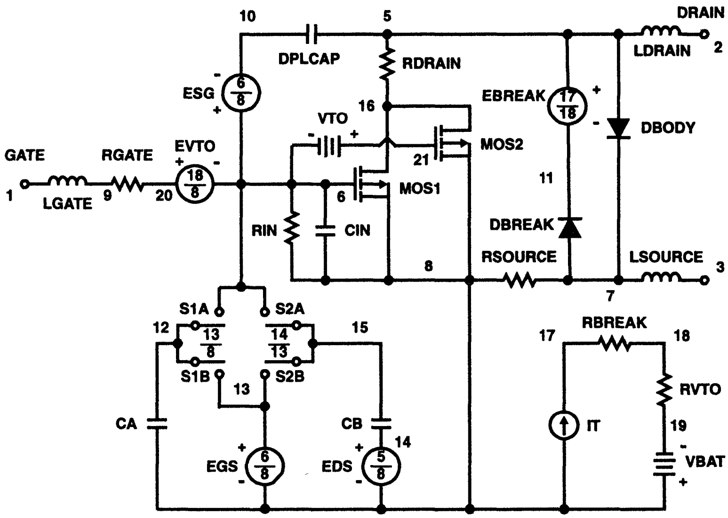
RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 12.83e-3
RGATE 9 20 1.55
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 3.25e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.83

.MODEL DBDMOD D (IS=1.24e-12 RS=4.72e-3 TRS1=1.43e-3 TRS2=-4.91e-7 CJO=6.98e-9 TT=1.5e-7)
.MODEL DBKMOD D (RS=1.11e-1 TRS1=1.34e-3 TRS2=4.46e-12)
.MODEL DPLCAPMOD D (CJO=15e-10 IS=1e-30 N=10)
.MODEL MOSMOD PMOS (VTO=-3.71 KP=31.5 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL RBKMOD RES (TC1=9.42e-4 TC2=0)
.MODEL RDSMOD RES (TC1=5.85e-3 TC2=7.69e-6)
.MODEL RVTOMOD RES (TC1=-3.39e-3 TC2=1.07e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=4.6 VOFF=2.6)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=2.6 VOFF=4.6)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=1.16 VOFF=-3.84)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-3.84 VOFF=1.16)

.ENDS
```



NOTE: For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

Screening Information

Screening is performed in accordance with the latest revision in effect of MIL-S-19500, (Screening Information Table).

Delta Tests and Limits (JANTX/JANTXV Equivalent)

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±20V, T_C = 25°C	±20 (Note 1)	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80% Rated Value, T_C = 25°C	±25 (Note 1)	μA
On Resistance	$r_{DS(ON)}$	T_C = +125°C at Rated I_D	±20% (Note 2)	Ω
Gate Threshold Voltage	$V_{GS(TH)}$	I_D = 1.0mA, T_C = 25°C	±20% (Note 2)	V

NOTES:

1. Or 100% of Initial Reading (whichever is greater).
2. Of Initial Reading.

Screening Information

TEST	JANTX/JANTXV EQUIVALENT
Gate Stress	V_{GS} = -30V, t = 250μs
Pind	Optional
PDA	10%
Pre Burn-In Test (Note 1)	MIL-S-19500 Group A, Subgroup 2 (All Static Tests at 25°C)
Steady State Gate Bias (Gate Stress)	MIL-STD-750, Method 1042, Condition B V_{GS} = 80% of Rated Value, T_A = 150°C, Time = 48 hours
Interim Electrical Tests (Note 1)	All Delta Parameters Listed in the Delta Tests and Limits Table
Steady State Reverse Bias (Drain Stress)	MIL-STD-750, Method 1042, Condition A V_{DS} = 80% of Rated Value, T_A = 150°C, Time = 168 hours
Final Electrical Tests (Note 1)	MIL-S-19500, Group A, Subgroup 2

NOTE:

1. Test limits are identical pre and post burn-in.

Additional Screening Tests

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNITS
Safe Operating Area	SOA	V_{DS} = -48V, t = 10ms	8.0	A
Unclamped Inductive Switching	I_{AS}	$V_{GS(PEAK)}$ = -15V, L = 0.1mH	75	A
Thermal Response	ΔV_{SD}	t_H = 100ms; V_H = 25V, I_H = 4A	142	mV
Thermal Impedance	ΔV_{SD}	t_H = 500ms; V_H = 25V, I_H = 4A	182	mV

POWER MOSFETs 5

LOGIC LEVEL POWER MOSFETs

HARRIS SEMICONDUCTOR

RFD3055LE, RFD3055LESM, RFP3055LE

12A, 60V, ESD Rated, Avalanche Rated, Logic Level N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 12A, 60V
- $r_{DS(ON)} = 0.150\Omega$
- 2kV ESD Protected
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RFD3055LE, RFD3055LESM, and RFP3055LE are N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

The RFD3055LE, RFD3055LESM, and RFP3055LE incorporate ESD protection and are designed to withstand 2kV (Human Body Model) of ESD.

PACKAGE AVAILABILITY

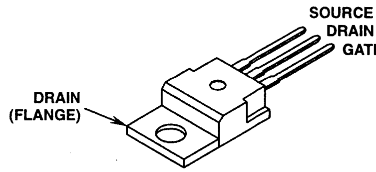
PART NUMBER	PACKAGE	BRAND
RFD3055LE	TO-251AA	F3055L
RFD3055LESM	TO-252AA	F3055L
RFP3055LE	TO-220AB	FP3055LE

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-252 variant in tape and reel, e.g. RFD3055LESM9A.

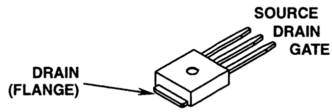
Formerly developmental type TA49158.

Packages

JEDEC TO-220AB



JEDEC TO-251AA



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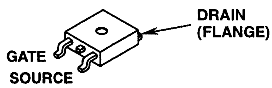
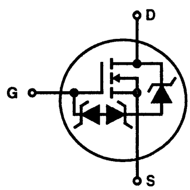


Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		RFD3055LE, RFD3055LESM, RFP3055LE	UNITS
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage	V_{DGR}	60	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current			
Continuous	I_D	12	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	48	W
Derate above $+25^oC$		0.323	$W/^oC$
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	^oC
Soldering Temperature of Leads for 10s	T_L	260	^oC
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	ESD	2	kV

File Number **4044.1**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	µA
			$T_C = +150^oC$	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 10V$		-	-	10	µA
On Resistance	$r_{DS(ON)}$	$I_D = 12A$, $V_{GS} = 5V$		-	-	0.150	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30V$, $I_D = 12A$, $R_L = 2.5\Omega$, $V_{GS} = 5V$, $R_{GS} = 5\Omega$		-	-	120	ns
Turn-On Delay Time	$t_{D(ON)}$			-	10	-	ns
Rise Time	t_R			-	70	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	25	-	ns
Fall Time	t_F			-	30	-	ns
Turn-Off Time	t_{OFF}			-	-	85	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $10V$	$V_{DD} = 48V$, $I_D = 12A$, $R_L = 4\Omega$	-	28	35	nC
Gate Charge at 5V	$Q_{G(5)}$	$V_{GS} = 0V$ to $5V$		-	15	18	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $1V$		-	1.0	1.2	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	850	-	pF
Output Capacitance	C_{OSS}			-	170	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	100	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	3.1	°C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO-251, TO-252, TO-220		-	-	80	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 12A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 12A$, $dI_{SD}/dt = 100A/\mu s$	-	-	100	ns

Typical Performance Curves

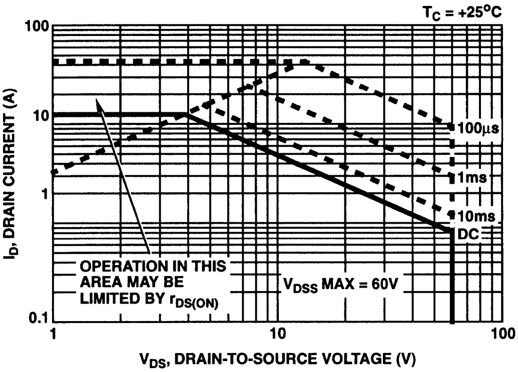


FIGURE 1. SAFE OPERATING AREA CURVE

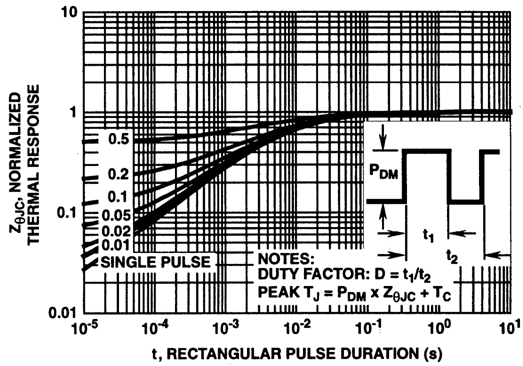


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

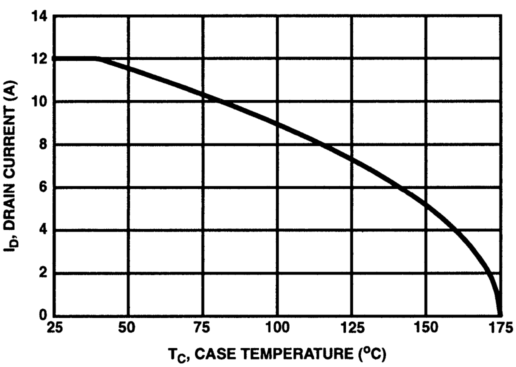


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

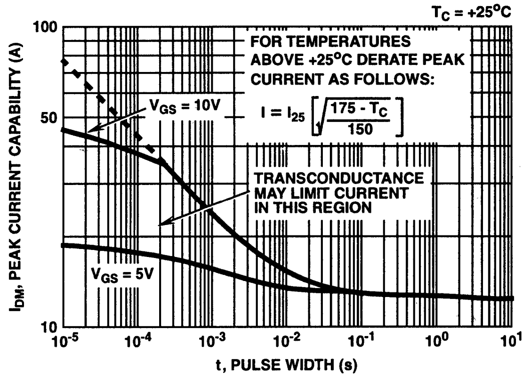


FIGURE 4. PEAK CURRENT CAPABILITY

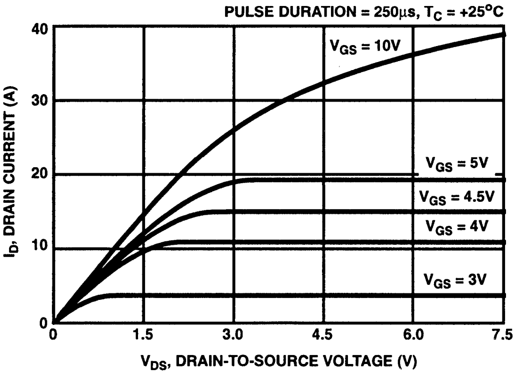


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

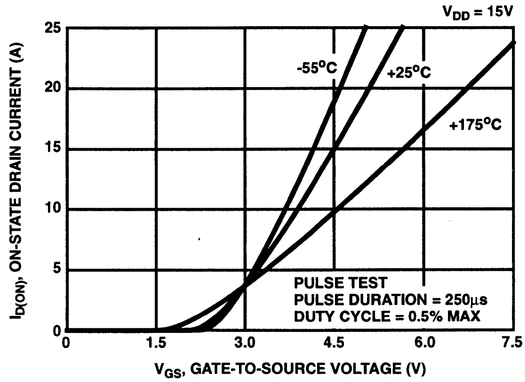


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

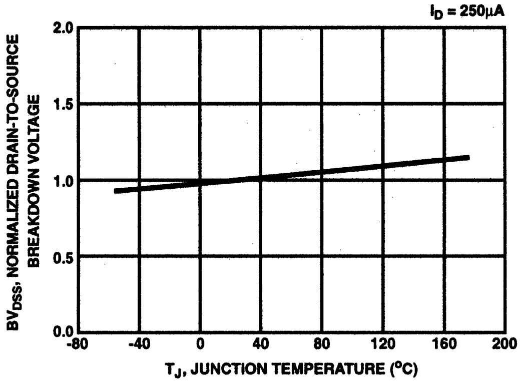


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

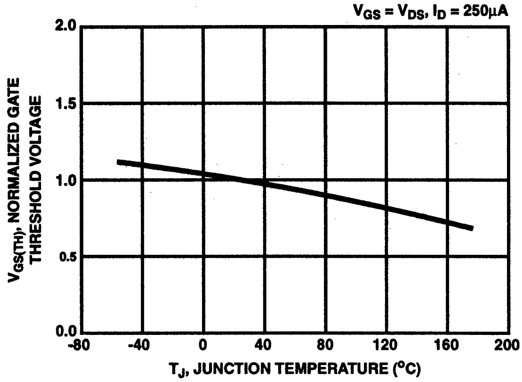


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

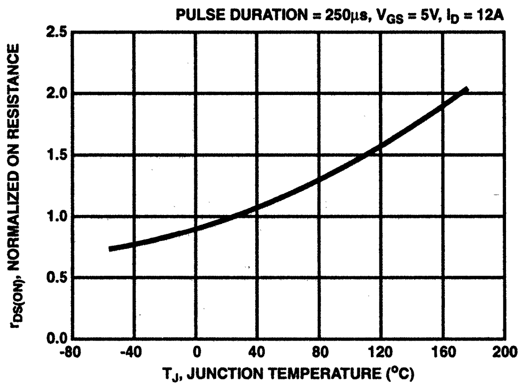


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

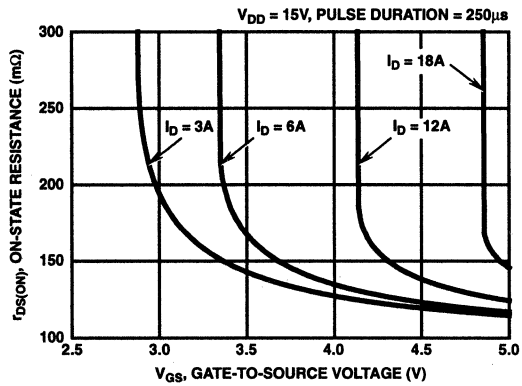


FIGURE 10. TYPICAL $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

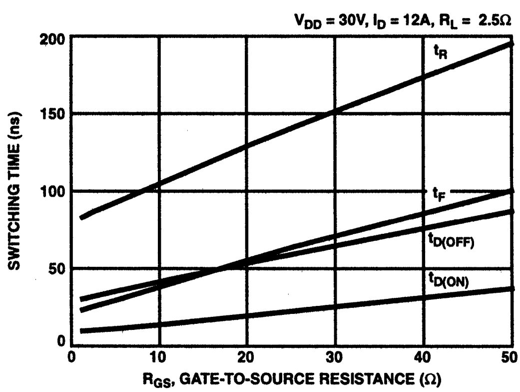


FIGURE 11. TYPICAL SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

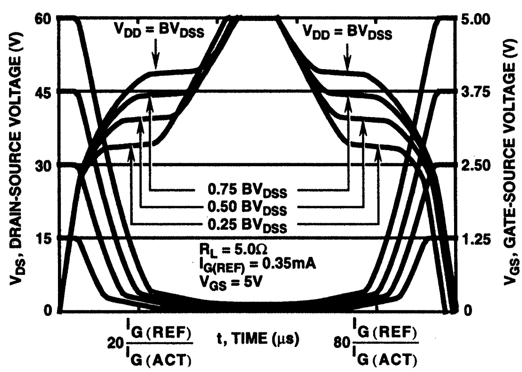


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

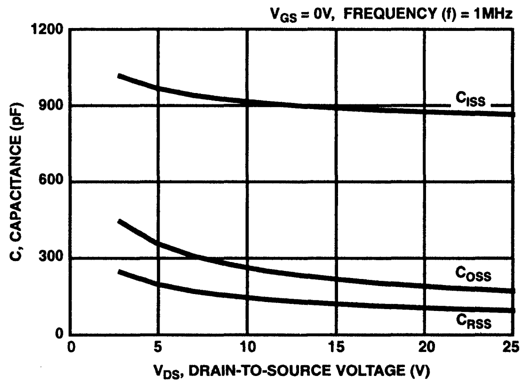


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

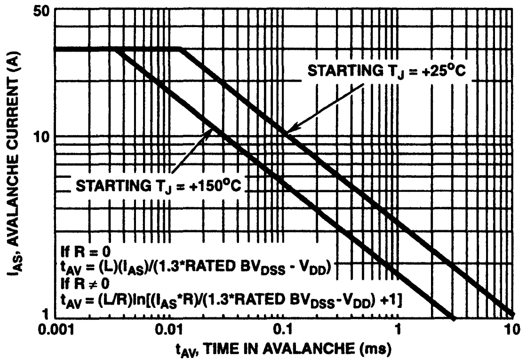


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

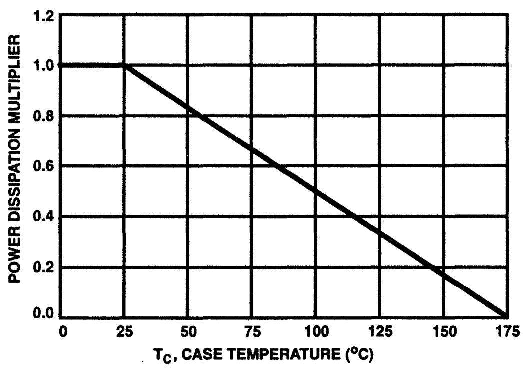


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms

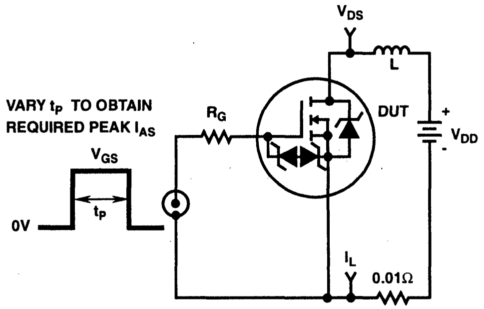


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

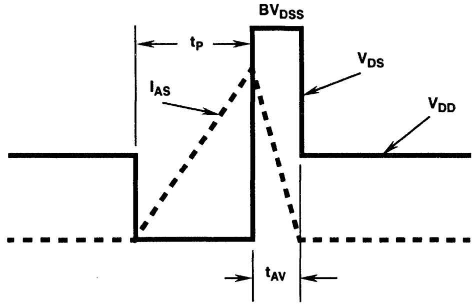


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

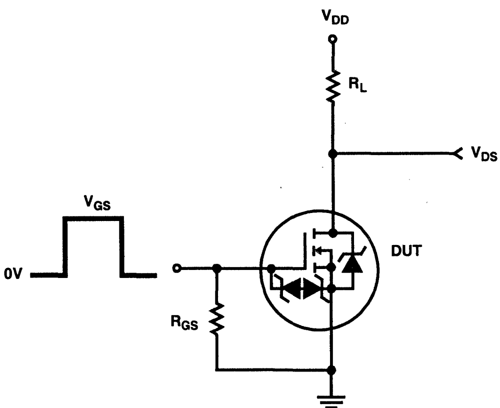


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

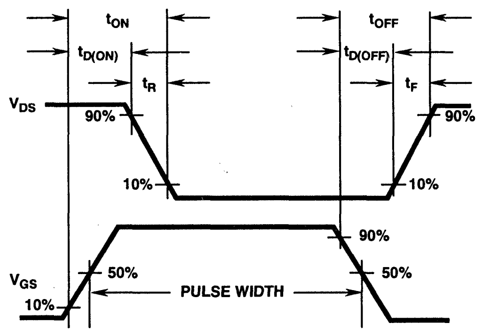


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD3055LE, RFD3055LESM, RFP3055LE

```
.SUBCKT RFD3055LE 2 1 3 ;    rev 1/30/95

CA 12 8 1.68e-9
CB 15 14 1.78e-9
CIN 6 8 0.769e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 64.28
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.6e-9
LSOURCE 3 7 4.6e-9

MOS1 16 6 8 8 MOSMOD M=0.99
MOS2 16 21 8 8 MOSMOD M=0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 0.176e-3
RLDRAIN 2 5 10
RGATE 9 20 9.84
RLGATE 1 9 46
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 76.56e-3
RLSOURCE 3 7 46
RVTO 18 19 RVTOMOD 1

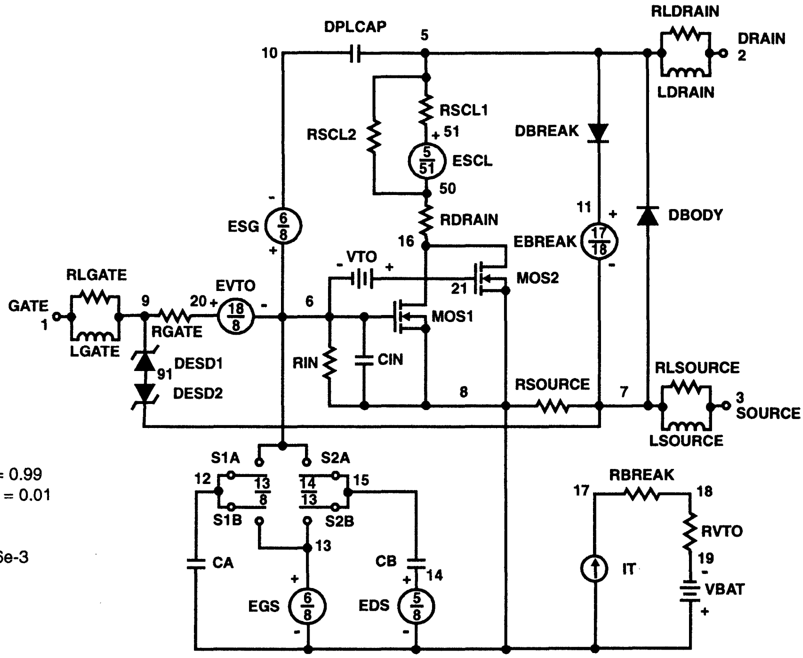
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.516

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/31.7,6))}

.MODEL DBDMOD D (IS = 3.61e-13 RS = 1.78e-2 TRS1 = 1.70e-2 TRS2 = -4.69e-6 CJO = 3.88e-10 TT = 3.6e-8)
.MODEL DBKMOD D (RS = 0.4731 TRS1 = -2.19e-3 TRS2 = 4.7e-5)
.MODEL DESD1MOD D (BV = 13.5 NBV = 17.5 IBV = 2.5e-4 RS = 22.2 TRS1 = 0 TRS2 = 0)
.MODEL DESD2MOD D (BV = 12.86 NBV = 22 IBV = 2.5e-4 RS = 0 TRS1 = 0 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 0.48e-9 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 2.082 KP = 18.36 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 1.06e-3 TC2 = -6.22e-7)
.MODEL RDSMOD RES (TC1 = 4.48e-3 TC2 = 1.77e-5)
.MODEL RSCLMOD RES (TC1 = 3.55e-3 TC2 = 0.20e-5)
.MODEL RVTOMOD RES (TC1 = -1.85e-3 TC2 = -4.13e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.4 VOFF= -2.4)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.4 VOFF= -4.4)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.85 VOFF= 2.15)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.15 VOFF= -2.85)

.ENDS
```



NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

RFD3N08L, RFD3N08LSM

HARRIS SEMICONDUCTOR

3A, 80V, Avalanche Rated, Logic Level N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 3A, 80V
- $r_{DS(ON)} = 0.800\Omega$
- *Temperature Compensating* PSPICE Model
- On-Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFD3N08L and RFD3N08LSM are N-Channel enhancement mode silicon gate power field effect transistors specifically designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, and solenoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3V to 5V range, thereby facilitating true on-off power control from logic circuit supply voltages.

PACKAGING AVAILABILITY

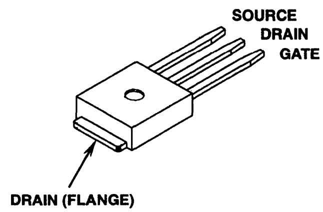
PART NUMBER	PACKAGE	BRAND
RFD3N08L	TO-251AA	F3N08L
RFD3N08LSM	TO-252AA	F3N08L

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, i.e., RFD3N08LSM9A.

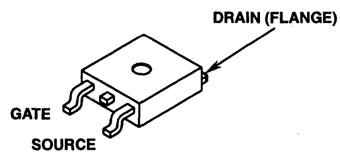
Formerly developmental type TA09922.

Packages

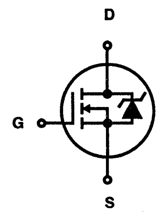
TO-251AA



TO-252AA



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		RFD3N08L RFD3N08LSM	UNITS
Drain-Source Voltage	V_{DSS}	80	V
Drain-Gate Voltage	V_{DGR}	80	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current			
Continuous	I_D	3	A
Pulsed	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	30	W
Derate above +25°C		0.2	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2836.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V		80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, I_D = 250µA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V	T_C = +25°C	-	-	1	µA
			T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 3A, V_{GS} = 5V		-	-	0.800	Ω
Turn-On Time	t_{ON}	V_{DD} = 40V, I_D = 3A, R_L = 13.3Ω, V_{GS} = 5V, R_{GS} = 25Ω		-	-	75	ns
Turn-On Delay Time	$t_{D(ON)}$			-	15	-	ns
Rise Time	t_R			-	45	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	22	-	ns
Fall Time	t_F			-	15	-	ns
Turn-Off Time	t_{OFF}			-	-	45	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 64V, I_D = 3A, R_L = 21.3Ω	-	6.8	8.5	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0V to 5V		-	3.8	4.8	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to 1V		-	0.18	0.24	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	125	-	pF
Output Capacitance	C_{OSS}			-	55	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	15	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	5.0	°C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$			-	-	100	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 3A	-	-	1.25	V
Reverse Recovery Time	t_{RR}	I_{SD} = 3A, dI_{SD}/dt = 100A/µs	-	-	85	ns

Typical Performance Curves

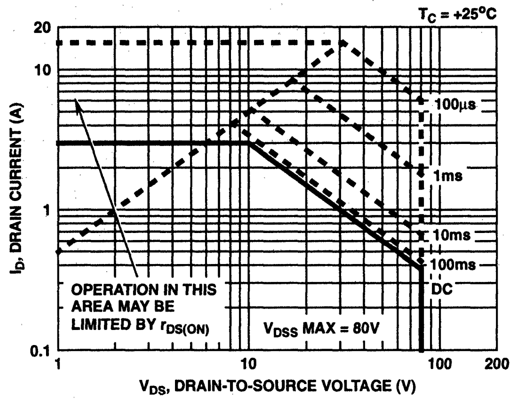


FIGURE 1. SAFE OPERATING AREA CURVE

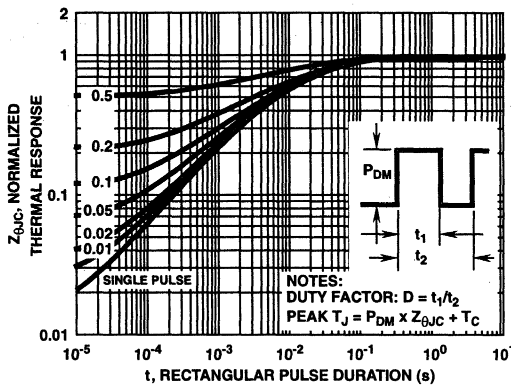


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

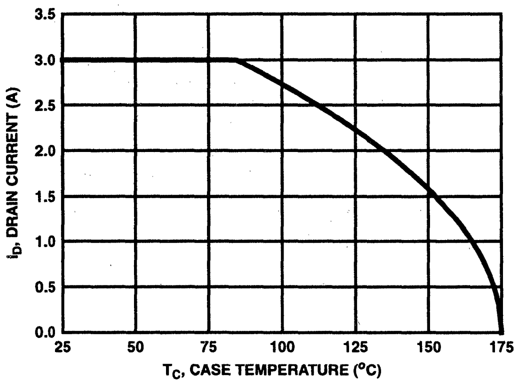


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

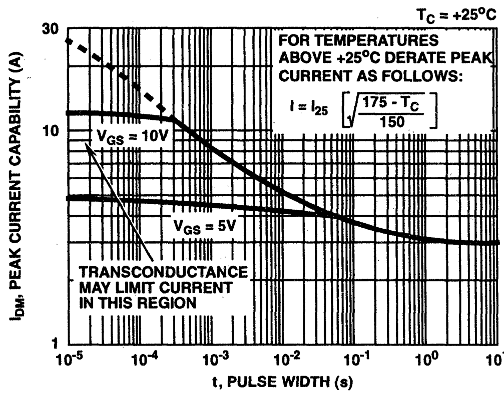


FIGURE 4. PEAK CURRENT CAPABILITY

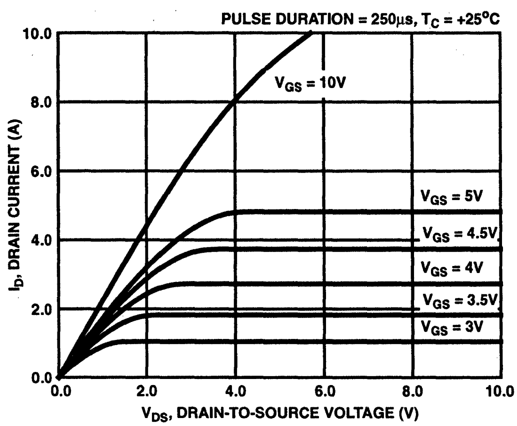


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

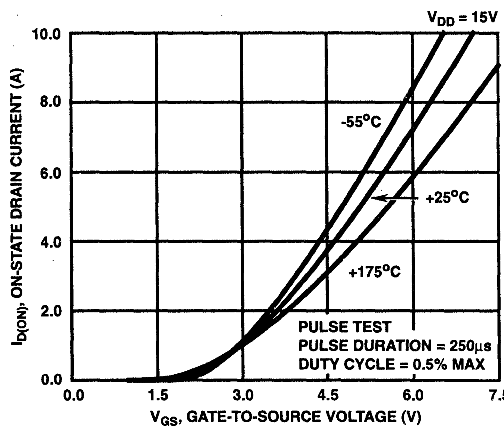


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

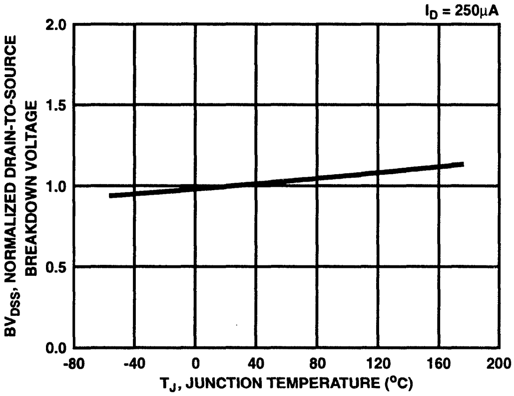


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

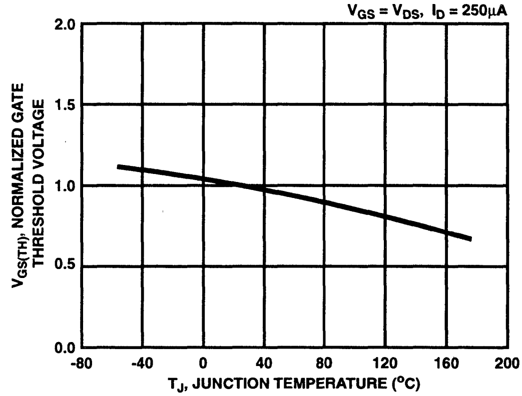


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

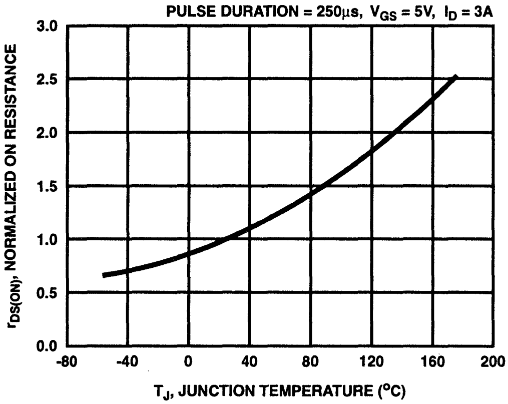


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

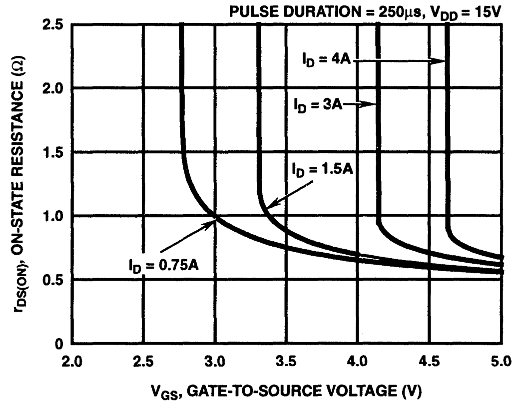


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

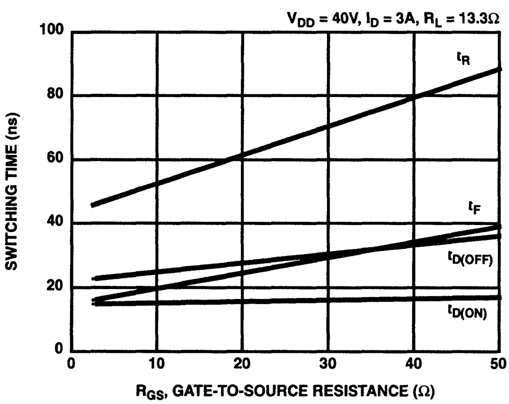


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

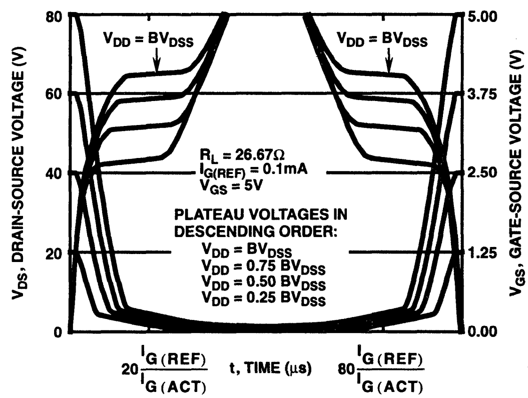


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

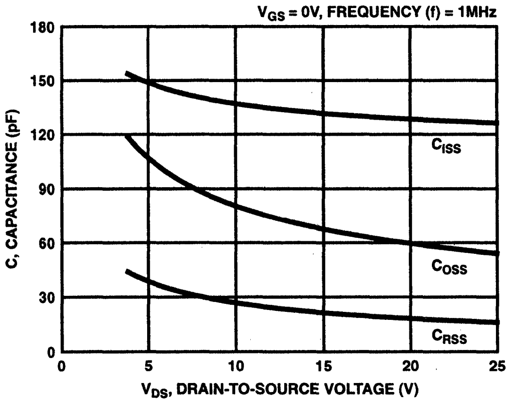


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

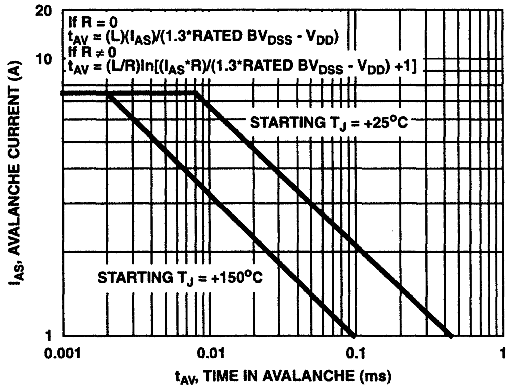


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

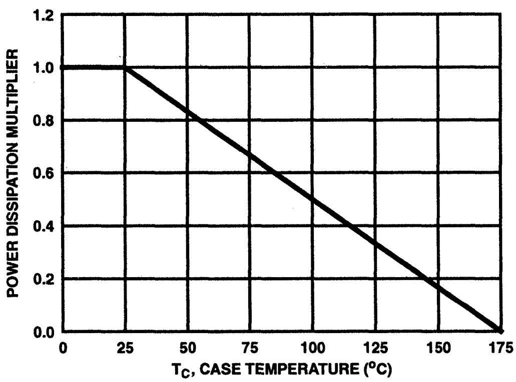


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms

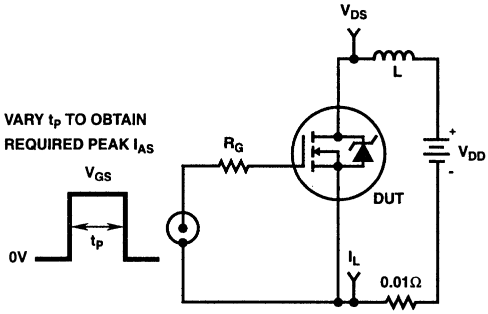


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

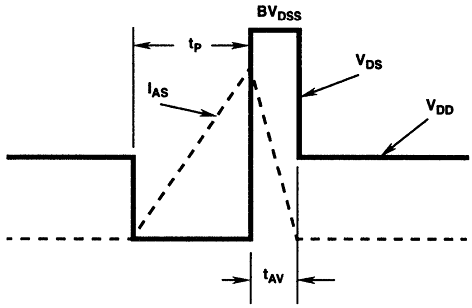


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

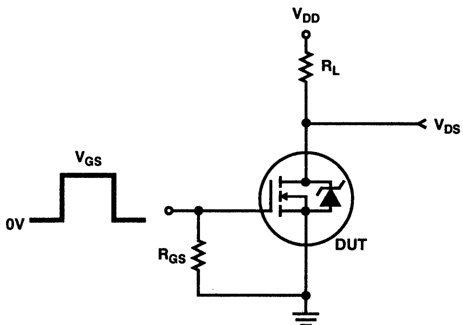


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

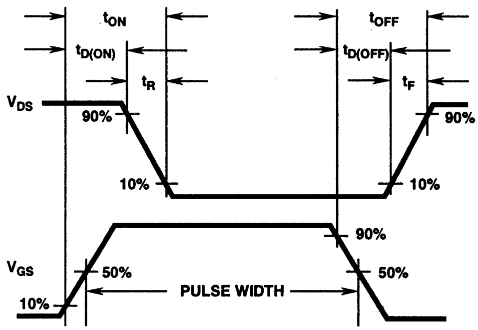
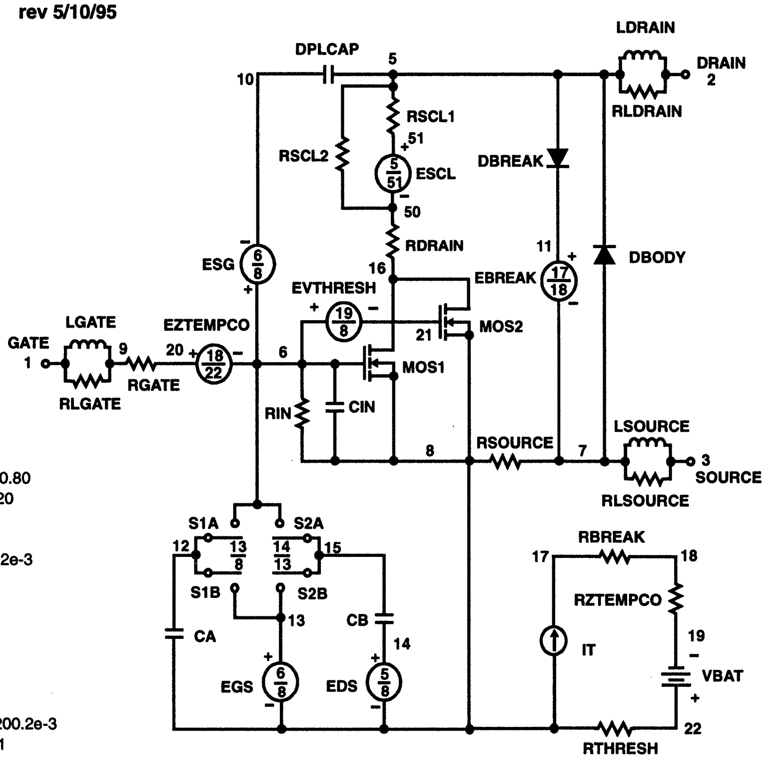


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD3N08L, RFD3N08LSM

SUBCKT RFD3N08L 2 1 3 ;   rev 5/10/95




```
CA 12 8 4.10e-10
CB 15 14 3.25e-10
CIN 6 8 1.10e-10

DBODY 7 5 DBDMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 93.57
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRESH 6 21 19 8 1
EZTEMPCO 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 5.8e-9
LSOURCE 3 7 5.8e-9

MOS1 16 6 8 8 MSTRONG M = 0.80
MOS2 16 21 8 8 MWEAK M = 0.20

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 174.2e-3
RGATE 9 20 24.9
RIN 6 8 1e9
RLDRAIN 2 5 10
RLGATE 1 9 58
RLSOURCE 3 7 58
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 200.2e-3
RTHRESH 22 8 RTHRESHMOD 1
RZTEMPCO 18 19 RZTEMPCOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*10),6))}

.MODEL DBDMOD D (IS = 9.90e-14 RS = 6.00e-2 TRS1 = 1.42e-3 TRS2 = -3.58e-6 CJO = 1.40e-10 TT = 5.75e-8 M = 0.4)
.MODEL DBREAKMOD D (RS = 2.32 TRS1 = 1.03e-3 TRS2 = -6.17e-11)
.MODEL DPLCAPMOD D (CJO = 1.13e-10 IS = 1e-30 N = 10 M=0.6)
.MODEL MSTRONG NMOS (VTO = 1.773 KP = 1.70 IS = 1e-30 N = 10 TOX = 1L = 1u W = 1u)
.MODEL MWEAK NMOS (VTO = 1.496 KP = 2.09 IS = 1e-30 N = 10 TOX = 1L = 1u W = 1u)
.MODEL RBREAKMOD RES (TC1 = 8.19e-4 TC2 = 5.9e-7)
.MODEL RDRAINMOD RES (TC1 = 1.55e-2 TC2 = 8.58e-5)
.MODEL RDSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RSCLMOD RES (TC1 = 0 TC2 = 0)
.MODEL RTHRESHMOD RES (TC1 = -5.0e-4 TC2 = -6.0e-6)
.MODEL RZTEMPCOMOD RES (TC1 = -1.19e-3 TC2 = 1.12e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.2 VOFF= -3.2)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.2 VOFF= -5.2)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.60 VOFF= 4.4)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 4.4 VOFF= -0.60)

.ENDS
```

NOTE:

1. For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET** Featuring Global Temperature Options; IEEE Power Electronics Specialist Conference Records, 1991.

HARRIS SEMICONDUCTOR

RFD14N05L, RFD14N05LSM, RFP14N05L

14A, 50V, Avalanche Rated, Logic Level N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 14A, 50V
- $r_{DS(ON)} = 0.100\Omega$
- *Temperature Compensating* PSPICE Model
- Can be Driven Directly from CMOS, NMOS, and TTL circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFD14N05L, RFD14N05LSM, and RFP14N05L are N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

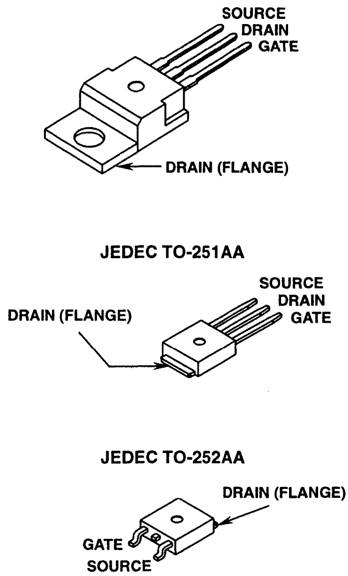
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFD14N05L	TO-251AA	14N05L
RFD14N05LSM	TO-252AA	14N05L
RFP14N05L	TO-220AB	FP14N05L

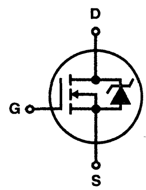
NOTE: When ordering, use the entire part number. Add the suffix 9A, to obtain the TO-252AA variant in tape and reel, i.e. RFD14N05LSM9A.

Formerly developmental type TA09870.

Packaging



Symbol



Absolute Maximum Ratings $T_C = +25°C$

		RFD14N05L, RFD14N05LSM, RFP14N05L	UNITS
Drain-Source Voltage	V_{DSS}	50	V
Drain-Gate Voltage	V_{DGR}	50	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current			
RMS Continuous	I_D	14	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25°C$	P_D	48	W
Derate above +25°C		0.32	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **2246.2**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		50	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 50V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	µA
			$T_C = +150^oC$	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 10V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 14A$, $V_{GS} = 5V$		-	-	0.100	Ω
Turn-On Time	t_{ON}	$V_{DD} = 25V$, $I_D = 7A$, $R_L = 3.57\Omega$, $V_{GS} = 5V$, $R_{GS} = 0.6\Omega$		-	-	60	ns
Turn-On Delay Time	$t_{D(ON)}$			-	13	-	ns
Rise Time	t_R			-	24	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	42	-	ns
Fall Time	t_F			-	16	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $10V$	$V_{DD} = 40V$, $I_D = 14A$, $R_L = 2.86\Omega$	-	-	40	nC
Gate Charge at 5V	$Q_{G(5)}$	$V_{GS} = 0V$ to $5V$		-	-	25	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $1V$		-	-	1.5	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	670	-	pF
Output Capacitance	C_{OSS}			-	185	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	50	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	3.125	°C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO -251 and TO-252		-	-	100	°C/W
		TO-220		-	-	80	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 14A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 14A$, $dI_{SD}/dt = 100A/\mu s$	-	-	125	ns

Typical Performance Curves

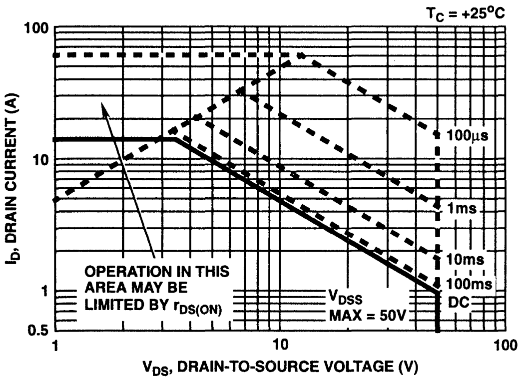


FIGURE 1. SAFE OPERATING AREA CURVE

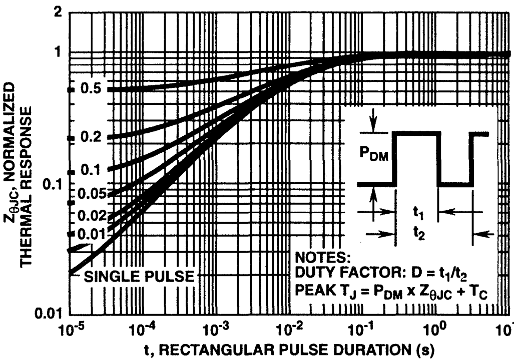


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

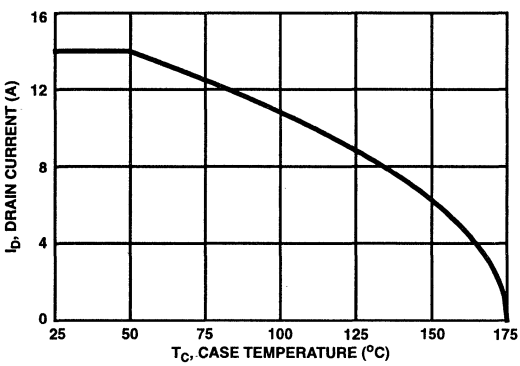


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

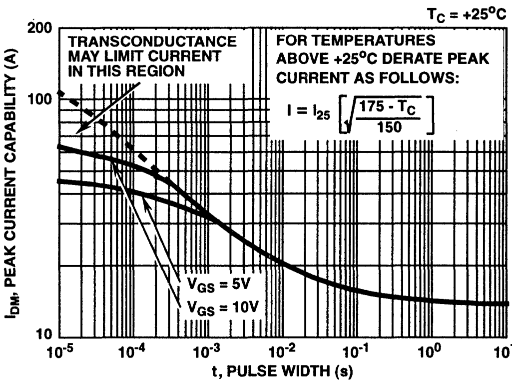


FIGURE 4. PEAK CURRENT CAPABILITY

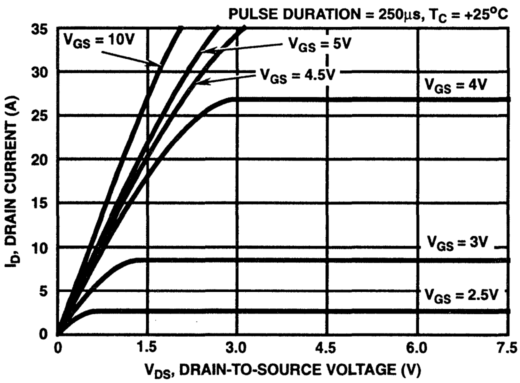


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

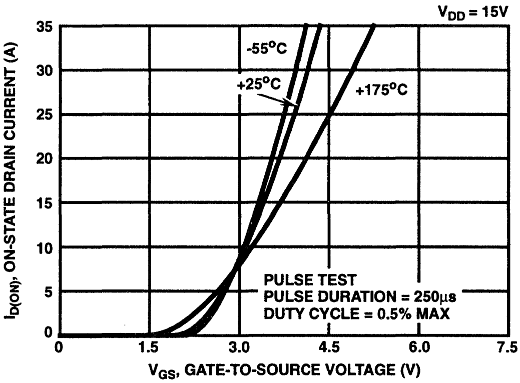


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

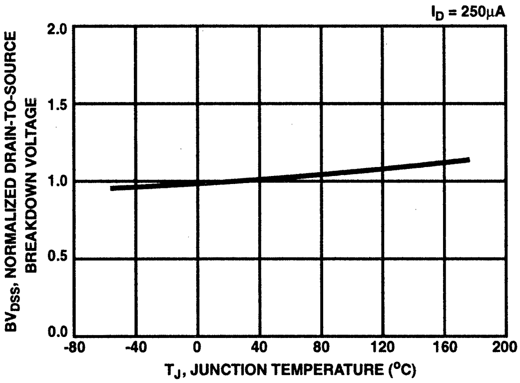


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

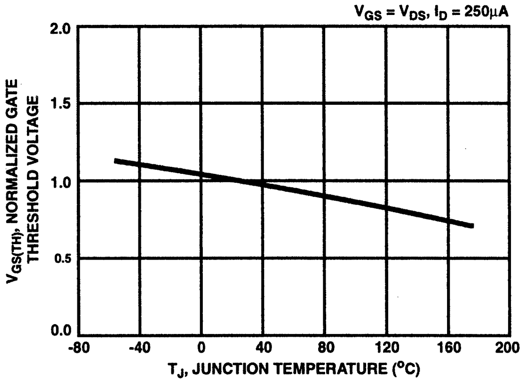


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

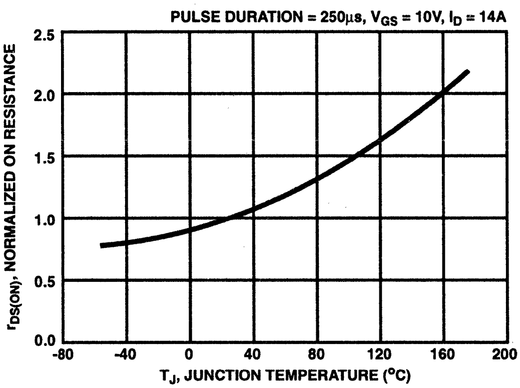


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

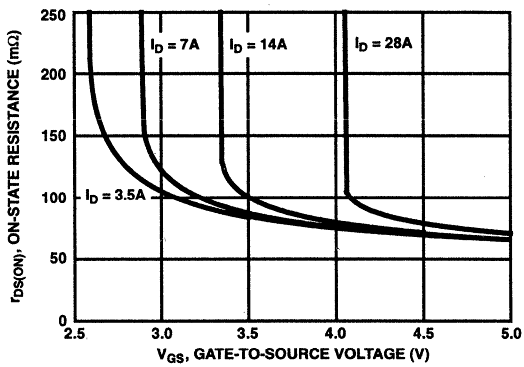


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

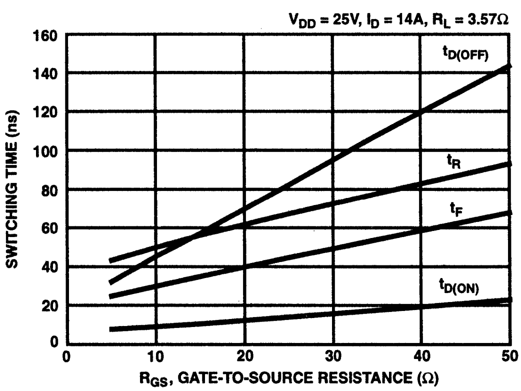


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

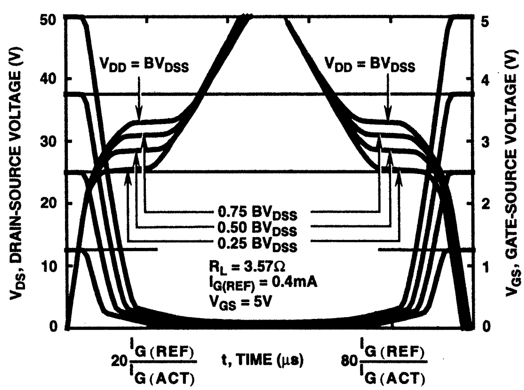


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

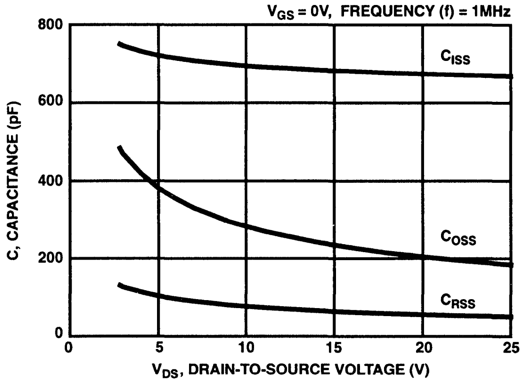


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

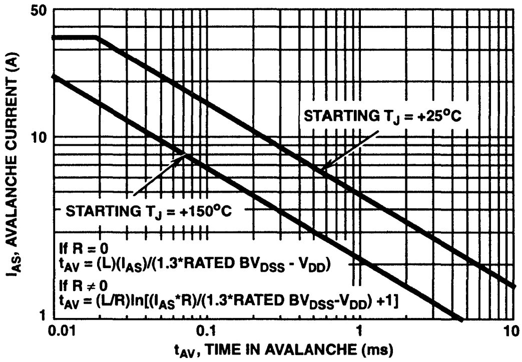


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

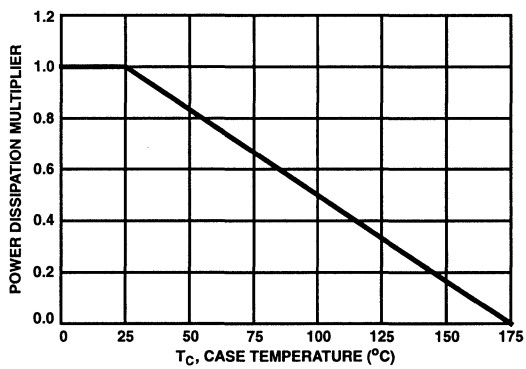


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

5
LOGIC LEVEL POWER MOSFETS

Test Circuits and Waveforms

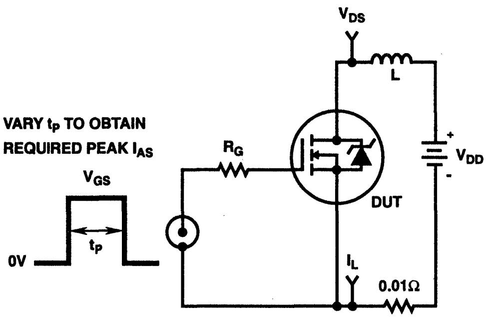


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

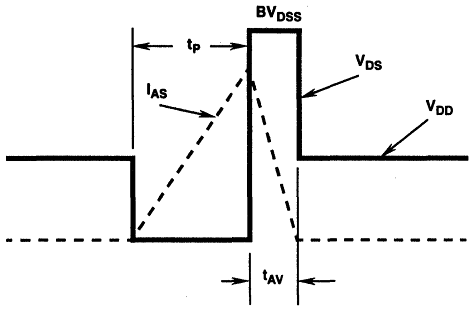


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

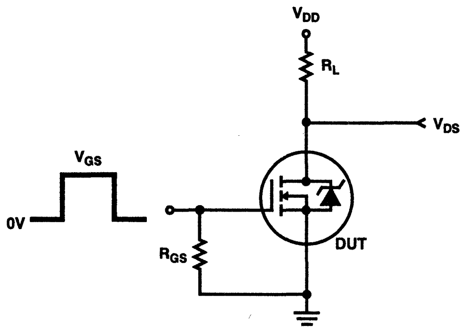


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

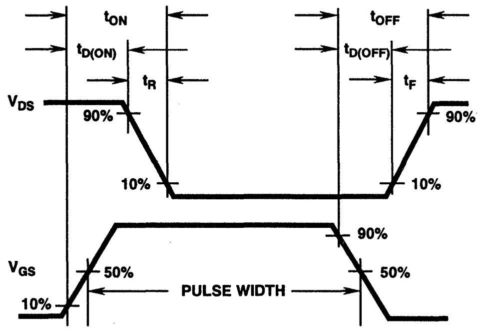
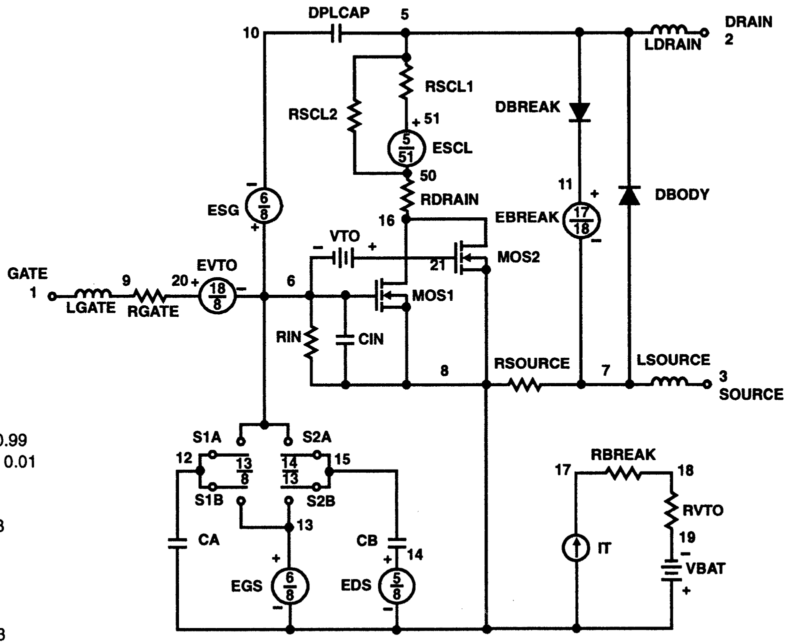


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD14N05L, RFD14N05LSM, RFP14N05L

.SUBCKT RFP14N05L 2 1 3 ; rev 9/15/94



CA 12 8 1.464e-9
CB 15 14 1.64e-9
CIN 6 8 6.17e-10

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 65.35
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 5.68e-9
LSOURCE 3 7 5.35e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 33.1e-3
RGATE 9 20 5.85
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 14.3e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.485

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/46,7))}

.MODEL DBDMOD D (IS = 2.23e-13 RS = 1.15e-2 TRS1 = 1.64e-3 TRS2 = 7.89e-6 CJO = 6.83e-10 TT = 3.68e-8)
.MODEL DBKMOD D (RS = 3.8e-1 TRS1 = 1.89e-3 TRS2 = 1.13e-5)
.MODEL DPLCAPMOD D (CJO = 25.7e-11 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 1.935 KP = 18.89 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 7.18e-4 TC2 = 1.53e-6)
.MODEL RDSMOD RES (TC1 = 4.45e-3 TC2 = 2.9e-5)
.MODEL RSCLMOD RES (TC1 = 2.8e-3 TC2 = 6.0e-6)
.MODEL RVTOMOD RES (TC1 = -1.7e-3 TC2 = -2.0e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.55 VOFF= -1.55)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.55 VOFF= -3.55)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.55 VOFF= 2.45)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.45 VOFF= -2.55)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFD14N06L, RFD14N06LSM, RFP14N06L

14A, 60V, Avalanche Rated, Logic Level N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 14A, 60V
- $r_{DS(ON)} = 0.100\Omega$
- *Temperature Compensating* PSPICE Model
- Can be Driven Directly from CMOS, NMOS, and TTL Circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFD14N06L, RFD14N06LSM, and RFP14N06L are N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

PACKAGE AVAILABILITY

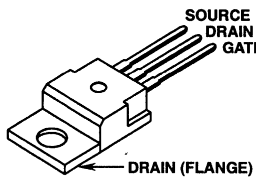
PART NUMBER	PACKAGE	BRAND
RFD14N06L	TO-251AA	14N06L
RFD14N06LSM	TO-252AA	14N06L
RFP14N06L	TO-220AB	FP14N06L

NOTE: When ordering, use the entire part number. Add the suffix 9A, to obtain the TO-252AA variant in tape and reel, i.e. RFD14N06LSM9A.

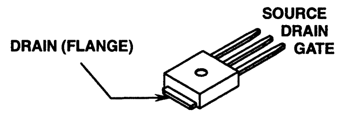
Formerly developmental type TA09870.

Packaging

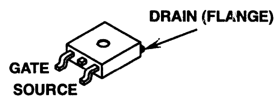
JEDEC TO-220AB



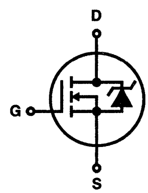
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		RFD14N06L, RFD14N06LSM, RFP14N06L	UNITS
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage	V_{DGR}	60	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current			
RMS Continuous	I_D	14	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	48	W
Derate above +25°C		0.32	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

File Number **4088**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = +25°C	-	-	1	μA
			T_C = +150°C	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 14A, V_{GS} = 5V		-	-	0.100	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 7A, R_L = 4.28Ω, V_{GS} = 5V, R_{GS} = 0.6Ω		-	-	60	ns
Turn-On Delay Time	$t_{D(ON)}$			-	13	-	ns
Rise Time	t_R			-	24	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	42	-	ns
Fall Time	t_F			-	16	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 48V, I_D = 14A, R_L = 3.43Ω	-	-	40	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0V to 5V		-	-	25	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to 1V		-	-	1.5	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	670	-	pF
Output Capacitance	C_{OSS}			-	185	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	50	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	3.125	°C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO-251 and TO-252		-	-	100	°C/W
		TO-220		-	-	80	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 14A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 14A, dI_{SD}/dt = 100A/μs	-	-	125	ns

Typical Performance Curves

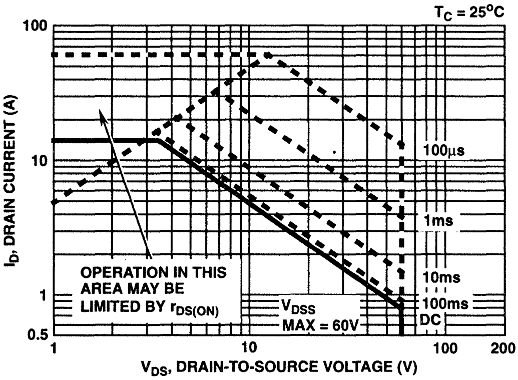


FIGURE 1. SAFE OPERATING AREA CURVE

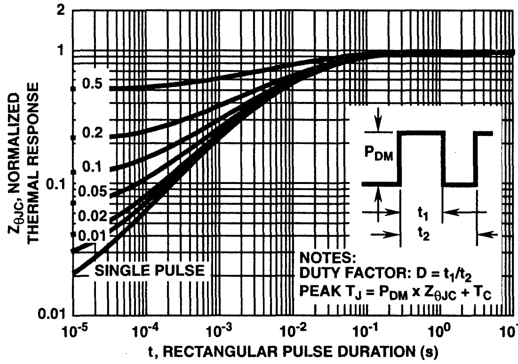


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

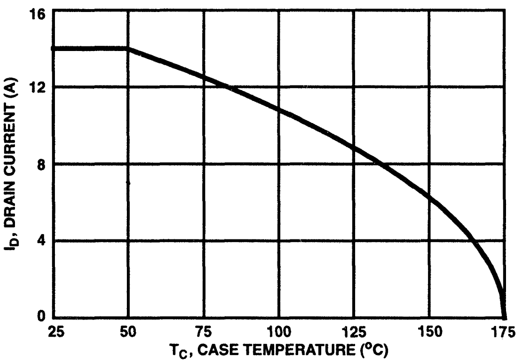


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

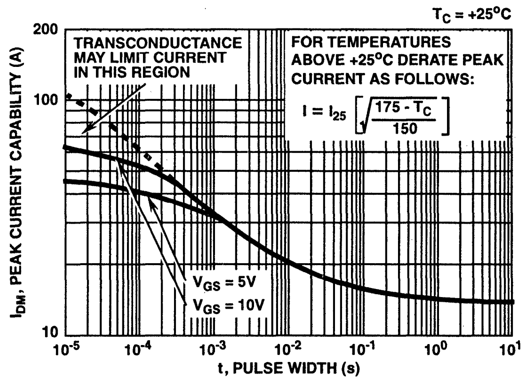


FIGURE 4. PEAK CURRENT CAPABILITY

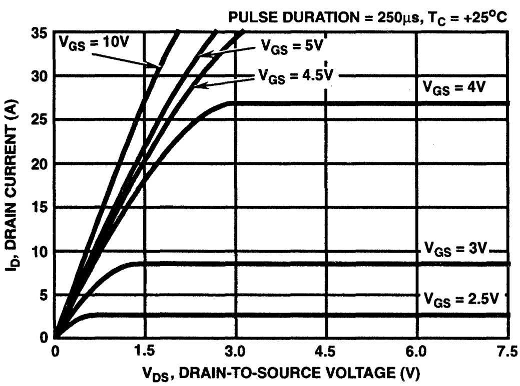


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

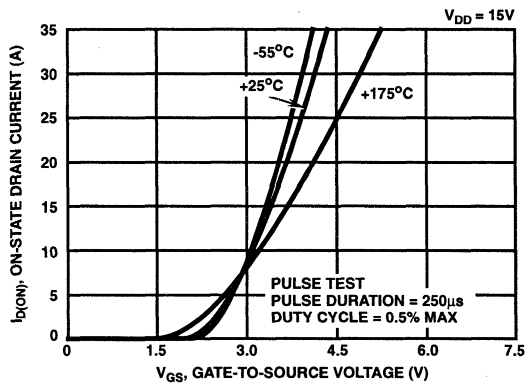


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

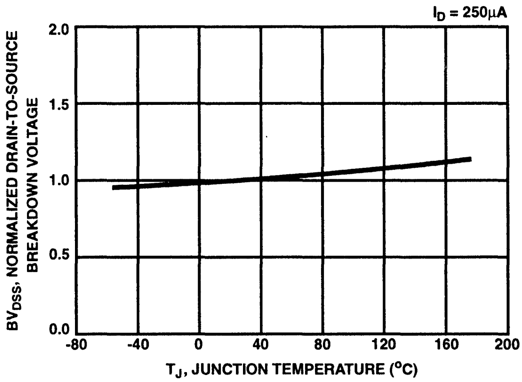


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

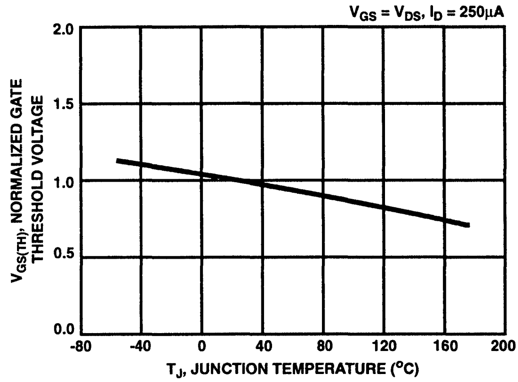


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

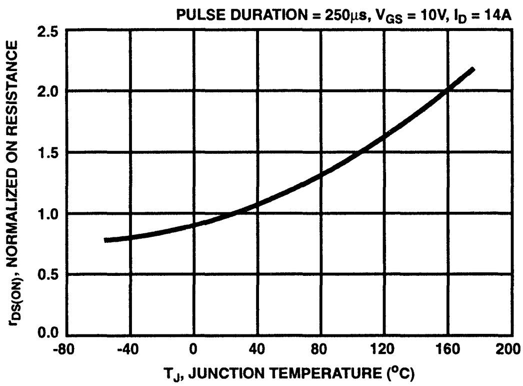


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

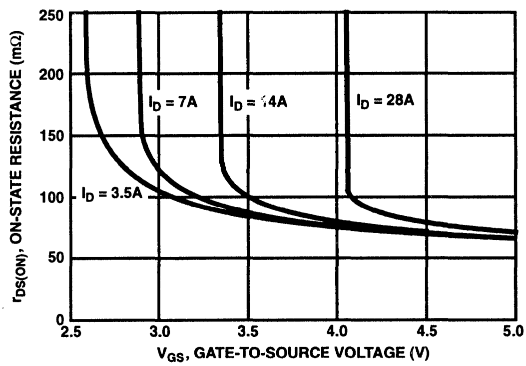


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

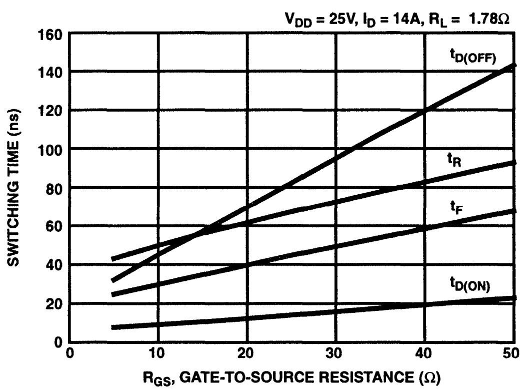


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

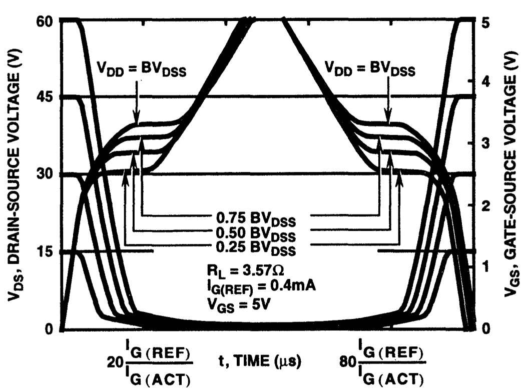


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

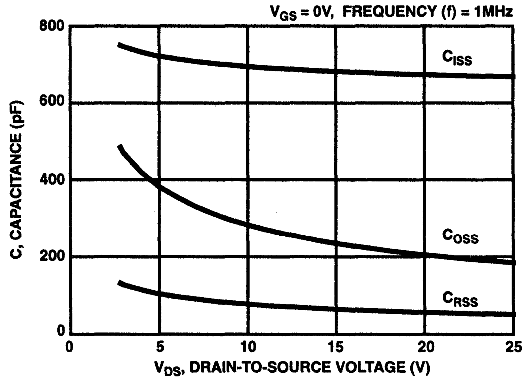


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

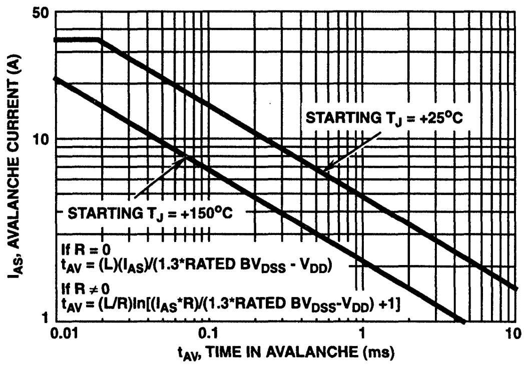


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

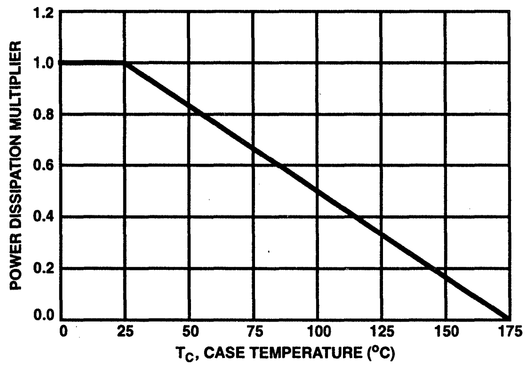


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms

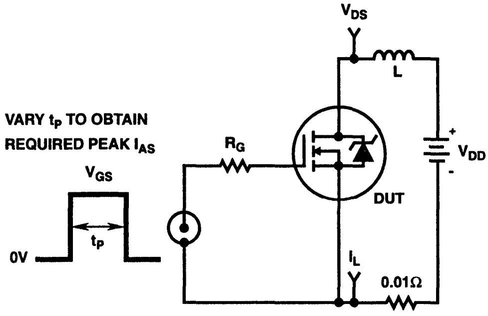


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

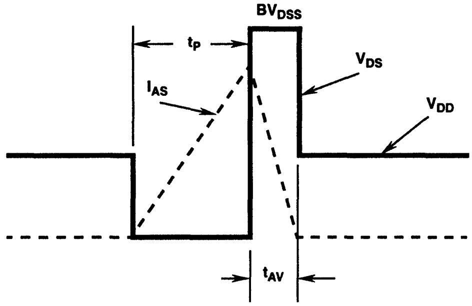


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

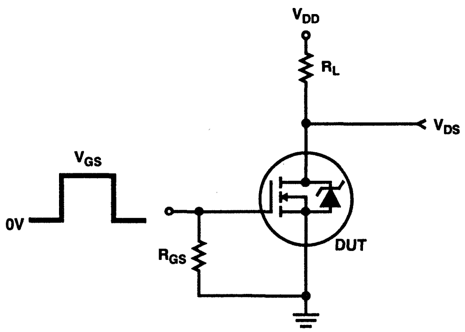


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

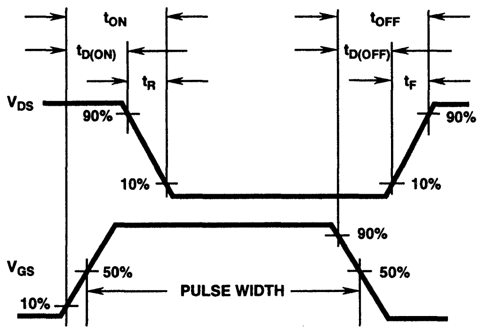
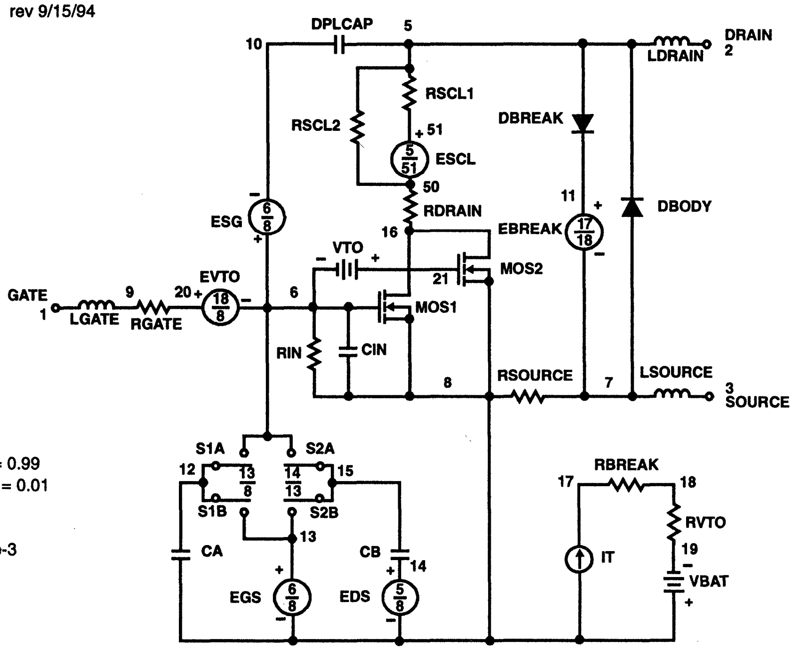


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD14N06L, RFD14N06LSM, RFP14N06L




```
.SUBCKT RFP14N06L 2 1 3 ;     rev 9/15/94
CA 12 8 1.464e-9
CB 15 14 1.64e-9
CIN 6 8 6.17e-10

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 65.35
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 5.68e-9
LSOURCE 3 7 5.35e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 33.1e-3
RGATE 9 20 5.85
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 14.3e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.485

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/46,7))}

.MODEL DBDMOD D (IS = 2.23e-13 RS = 1.15e-2 TRS1 = 1.64e-3 TRS2 = 7.89e-6 CJO = 6.83e-10 TT = 3.68e-8)
.MODEL DBKMOD D (RS = 3.8e-1 TRS1 = 1.89e-3 TRS2 = 1.13e-5)
.MODEL DPLCAPMOD D (CJO = 25.7e-11 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 1.935 KP = 18.89 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 7.18e-4 TC2 = 1.53e-6)
.MODEL RDSMOD RES (TC1 = 4.45e-3 TC2 = 2.9e-5)
.MODEL RSCLMOD RES (TC1 = 2.8e-3 TC2 = 6.0e-6)
.MODEL RVTOMOD RES (TC1 = -1.7e-3 TC2 = -2.0e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.55 VOFF= -1.55)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.55 VOFF= -3.55)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.55 VOFF= 2.45)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.45 VOFF= -2.55)

.ENDS
```

For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; authored by William J. Hepp and C. Frank Wheatley.

HARRIS SEMICONDUCTOR

RFD16N03L, RFD16N03LSM

16A, 30V, Avalanche Rated N-Channel Logic Level Enhancement-Mode Power MOSFETs

December 1995

Features

- 16A, 30V
- $r_{DS(ON)} = 0.022\Omega$
- *Temperature Compensating* PSPICE Model
- Can be Driven Directly from CMOS, NMOS, and TTL Circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFD16N03L and RFD16N03LSM are N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

PACKAGE AVAILABILITY

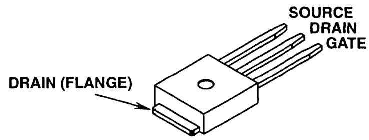
PART NUMBER	PACKAGE	BRAND
RFD16N03L	TO-251AA	16N03L
RFD16N03LSM	TO-252AA	16N03L

NOTE: When ordering, use the entire part number. Add the suffix 9A, to obtain the TO-252AA variant in tape and reel, e.g. RFD16N03LSM9A.

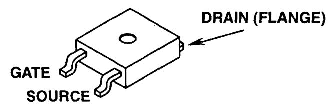
Formerly developmental type TA49030.

Packaging

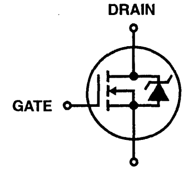
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



5

LOGIC LEVEL POWER MOSFETs

Absolute Maximum Ratings $T_C = +25°C$

		RFD16N03L, RFD16N03LSM	UNITS
Drain-Source Voltage	V_{DSS}	30	V
Drain-Gate Voltage	V_{DGR}	30	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current			
RMS Continuous	I_D	16	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25°C$	P_D	90	W
Derate above +25°C		0.606	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number 4013.1

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	μA
			$T_C = +150^oC$	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 10V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 16A$, $V_{GS} = 5V$		-	-	0.022	Ω
Turn-On Time	t_{ON}	$V_{DD} = 15V$, $I_D = 16A$, $R_L = 0.93\Omega$, $V_{GS} = 5V$, $R_{GS} = 5\Omega$		-	-	120	ns
Turn-On Delay Time	$t_{D(ON)}$			-	15	-	ns
Rise Time	t_R			-	95	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	25	-	ns
Fall Time	t_F			-	27	-	ns
Turn-Off Time	t_{OFF}			-	-	80	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $10V$	$V_{DD} = 24V$, $I_D = 16A$, $R_L = 1.5\Omega$	-	50	60	nC
Gate Charge at 5V	$Q_{G(5)}$	$V_{GS} = 0V$ to $5V$		-	30	36	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $1V$		-	1.5	1.8	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	1650	-	pF
Output Capacitance	C_{OSS}			-	575	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	200	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	1.65	$^oC/W$
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO-251 and TO-252		-	-	100	$^oC/W$

Source-Drain Diode Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 16A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 16A$, $dI_{SD}/dt = 100A/\mu s$	-	-	75	ns

Typical Performance Curves

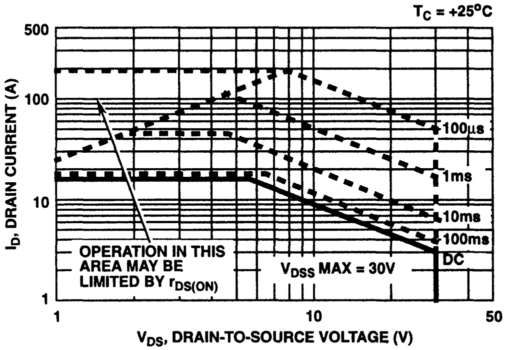


FIGURE 1. SAFE OPERATING AREA CURVE

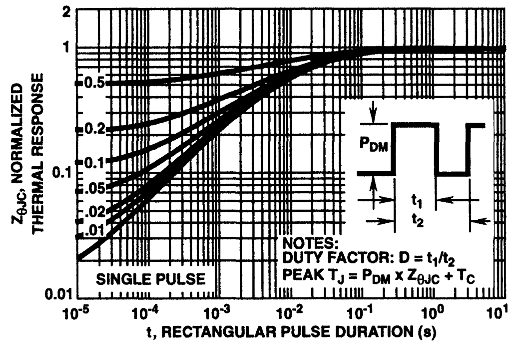


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

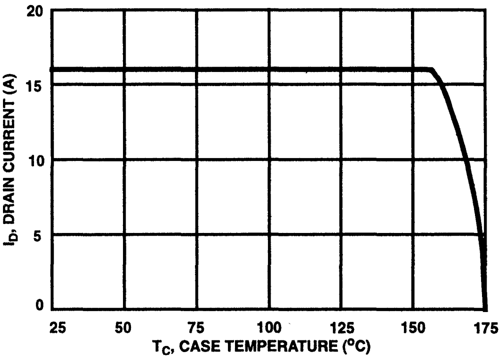


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

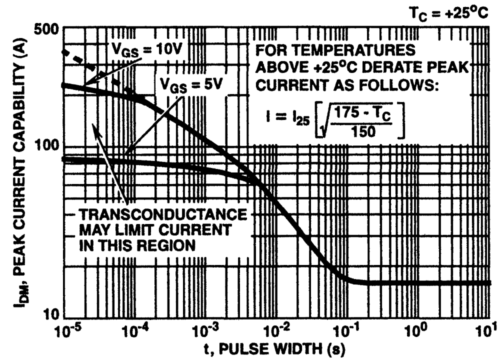


FIGURE 4. PEAK CURRENT CAPABILITY

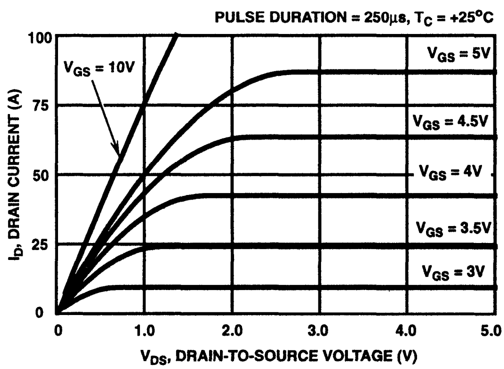


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

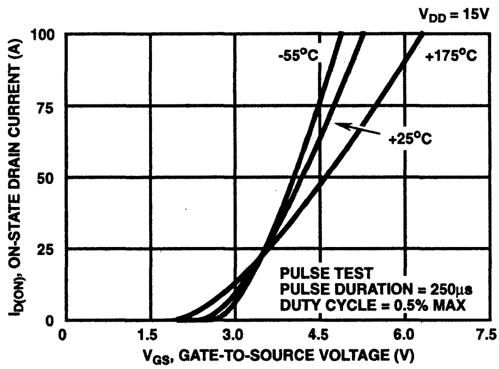


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

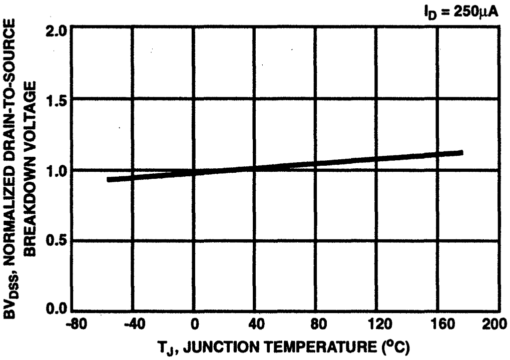


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

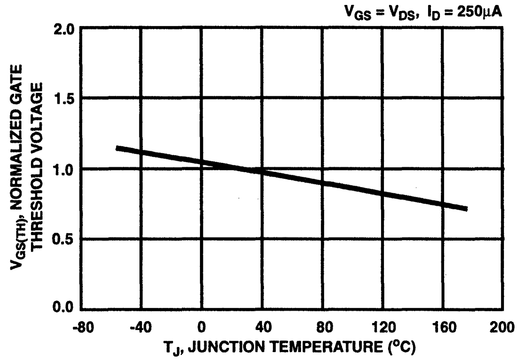


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

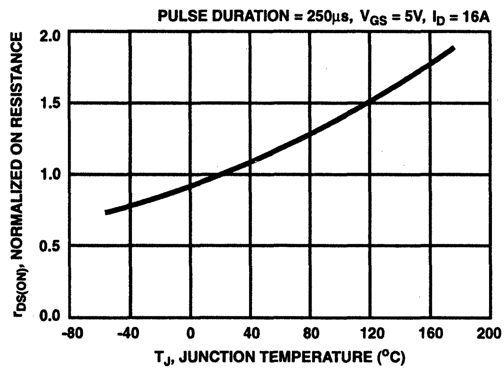


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

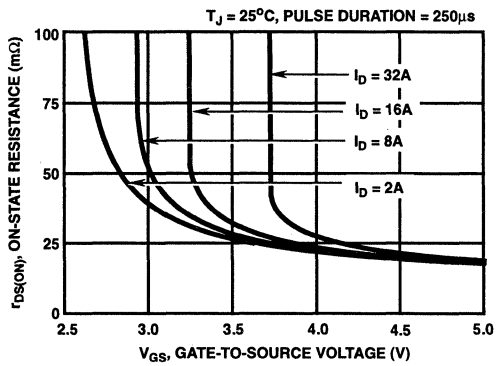


FIGURE 10. TYPICAL $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

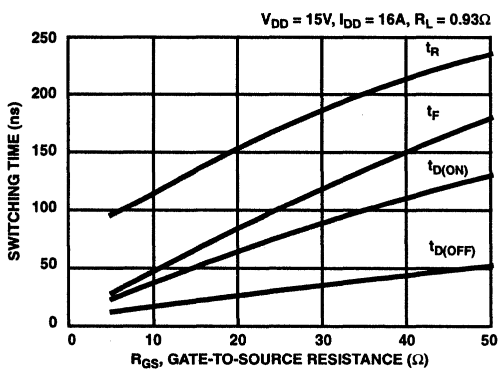


FIGURE 11. TYPICAL SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

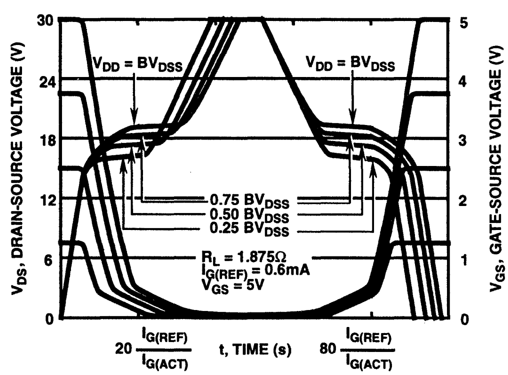


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

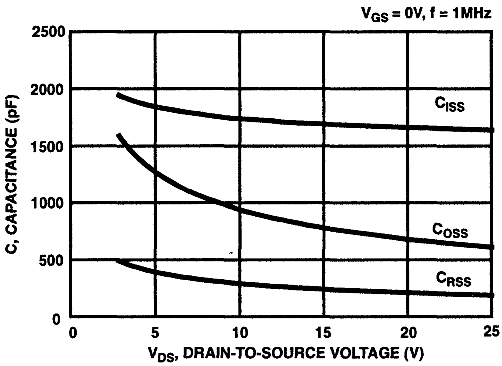


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

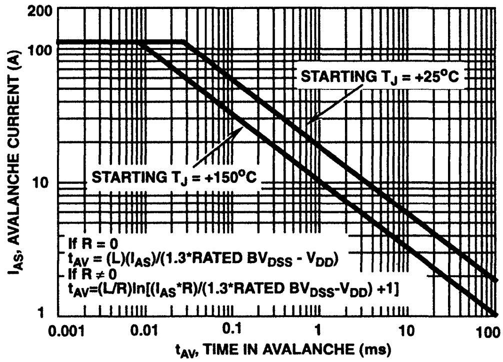


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

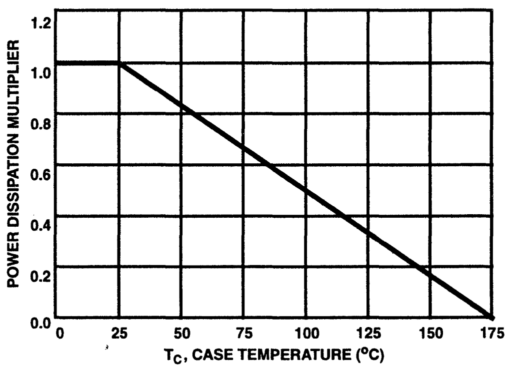


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

5

LOGIC LEVEL POWER MOSFETs

Test Circuits and Waveforms

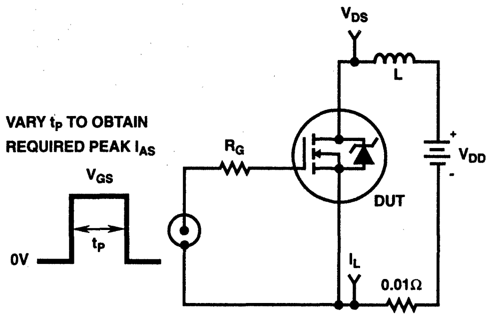


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

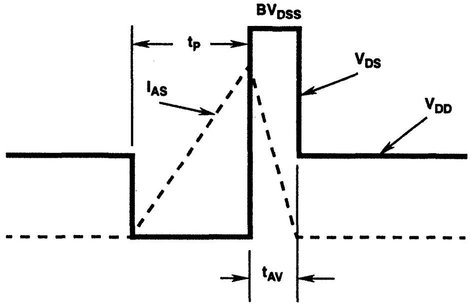


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

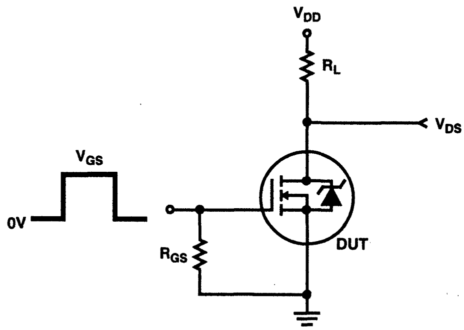


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

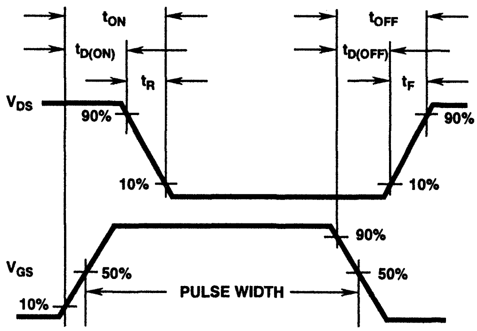
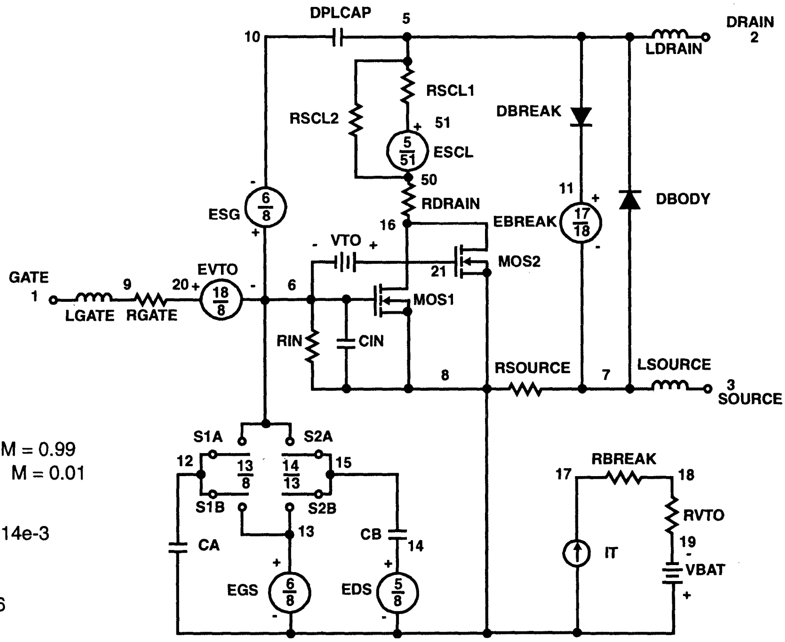


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFD16N03L, RFD16N03LSM

.SUBCKT RFD16N03L 2 1 3; rev 12/12/94




```
CA 12 8 2.55e-9
CB 15 14 2.64e-9
CIN 6 8 1.45e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 33.3

EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 3.4e-9
LSOURCE 3 7 3.4e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 0.14e-3
RGATE 9 20 0.89
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 10.31e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.583

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/176,6))}

.MODEL DBDMOD D (IS = 3.61e-13 RS = 5.06e-3 TRS1 = 3.05e-3 TRS2 = 7.57e-6 CJO = 2.16e-9 TT = 2.18e-8)
.MODEL DBKMOD D (RS = 1.66e-1 TRS1 = -2.97e-3 TRS2 = 7.57e-6)
.MODEL DPLCAPMOD D (CJO = 0.96e-9 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 2.313 KP = 53.82 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 8.95e-4 TC2 = -1e-7)
.MODEL RDSMOD RES (TC1 = 3.92e-3 TC2 = 1.29e-5)
.MODEL RSCLMOD RES (TC1 = 2.03e-3 TC2 = 0.45e-5)
.MODEL RVTOMOD RES (TC1 = -2.27e-3 TC2 = -5.75e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.82 VOFF= -2.82)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.82 VOFF= -4.82)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.67 VOFF= 2.33)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.33 VOFF= -2.67)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

RFP23N06LE, RF1S23N06LE, RF1S23N06LESM

23A, 60V, ESD Rated, Avalanche Rated, Logic Level N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- 23A, 60V
- $r_{DS(ON)} = 0.065\Omega$
- 2kV ESD Protected
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFP23N06LE, RF1S23N06LE, and RF1S23N06LESM are N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

PACKAGE AVAILABILITY

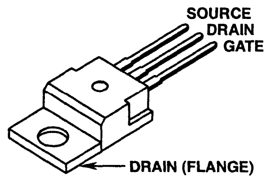
PART NUMBER	PACKAGE	BRAND
RFP23N06LE	TO-220AB	FP23N06L
RF1S23N06LE	TO-262AA	F23N06LE
RF1S23N06LESM	TO-263AB	F23N06LE

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB variant in tape and reel, i.e. RF1S23N06LESM9A.

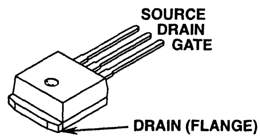
Formerly developmental type TA49165.

Packaging

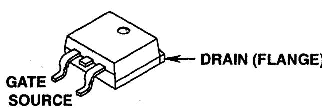
JEDEC TO-220AB



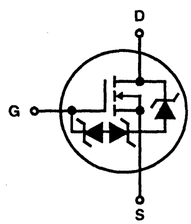
JEDEC TO-262AA



JEDEC TO-263AB



Symbol



Absolute Maximum Ratings ($T_C = +25°C$)

		RFP23N06LE, RF1S23N06LE, RF1S23N06LESM	UNITS
Drain-Source Voltage	V_{DSS}	60	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	60	V
Gate-Source Voltage (Note)	V_{GS}	±10	V
Drain Current			
Continuous	I_D	23	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25°C$	P_D	75	W
Derate above +25°C		0.5	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	ESD	2	kV

NOTE: May be exceeded if gate current is limited to 1mA.

File Number 4077.1

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60V, V_{GS} = 0V	T_C = +25°C	-	-	1	μA
			T_C = +150°C	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	10	μA
On Resistance	$r_{DS(ON)}$	I_D = 23A, V_{GS} = 5V		-	-	0.065	Ω
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 23A, R_L = 1.30Ω, V_{GS} = 5V, R_{GS} = 2.5Ω		-	-	160	ns
Turn-On Delay Time	$t_{D(ON)}$			-	12	-	ns
Rise Time	t_R			-	93	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	28	-	ns
Fall Time	t_F			-	38	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 48V, I_D = 23A, R_L = 2.09Ω	-	38	48	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0V to 5V		-	20	25	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to 1V		-	0.90	1.2	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	850	-	pF
Output Capacitance	C_{OSS}			-	250	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	75	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	2.00	°C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 23A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 23A, dI_{SD}/dt = 100A/μs	-	-	85	ns

Typical Performance Curves

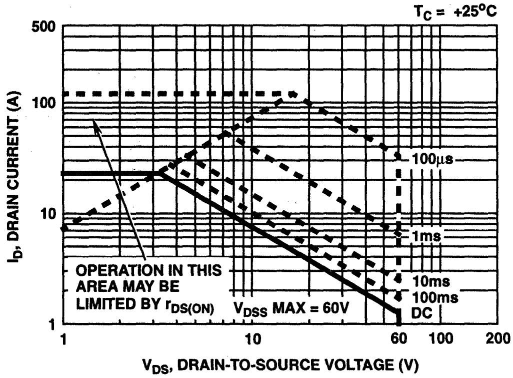


FIGURE 1. SAFE OPERATING AREA CURVE

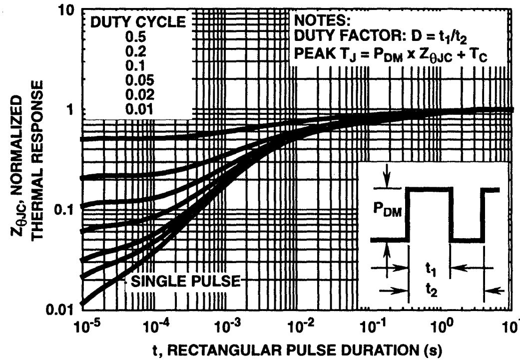


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

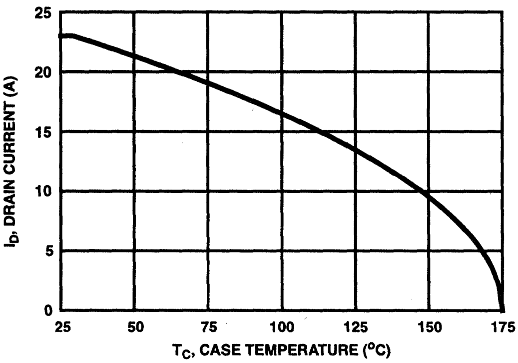


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

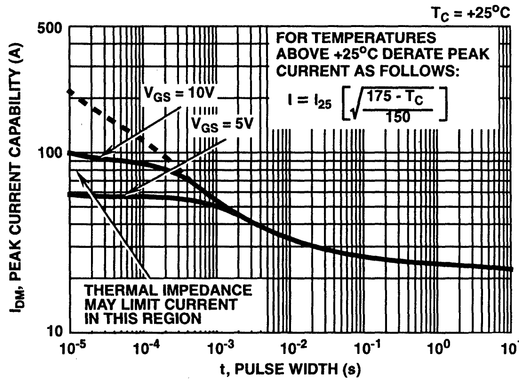


FIGURE 4. PEAK CURRENT CAPABILITY

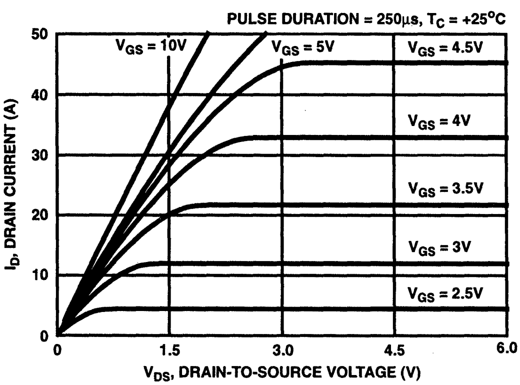


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

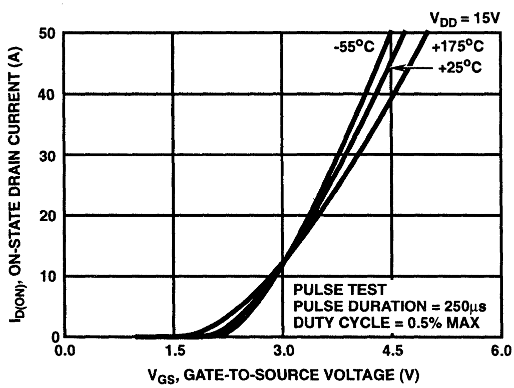


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

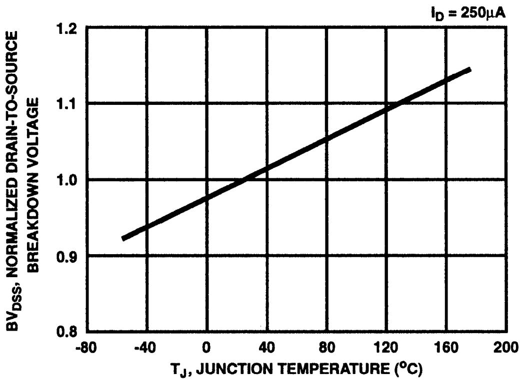


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

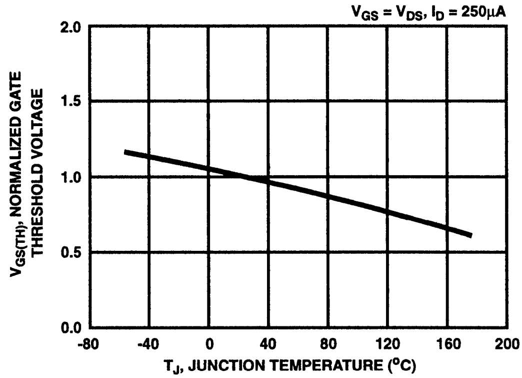


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

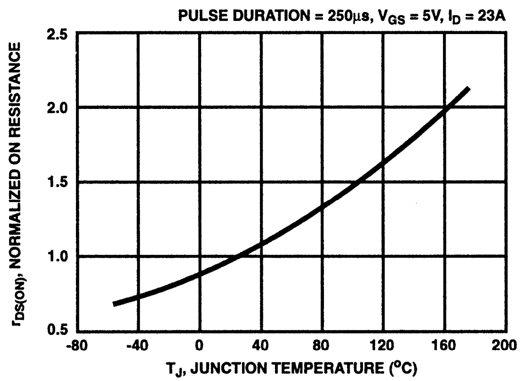


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

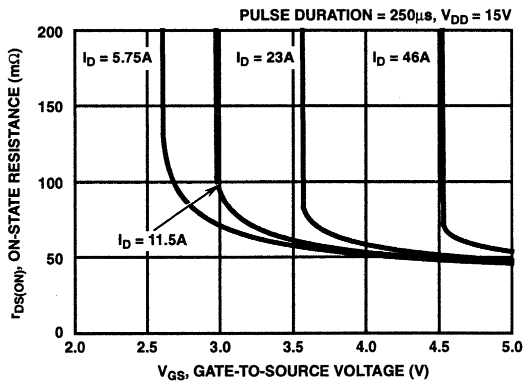


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

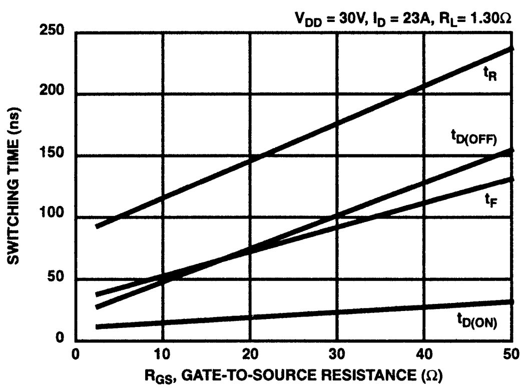


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

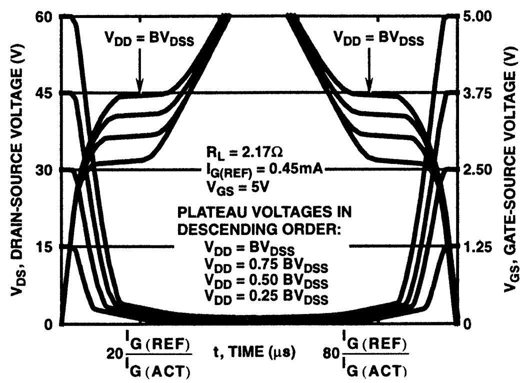


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

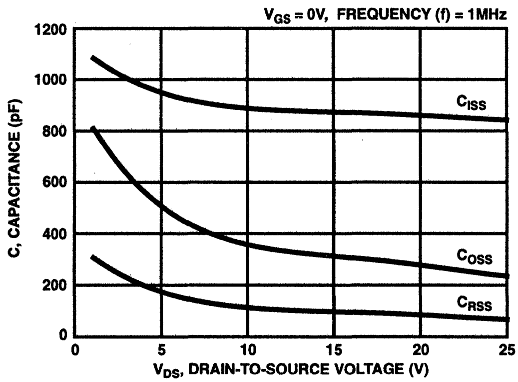


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

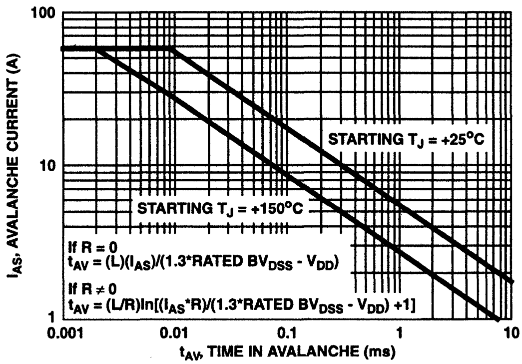


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

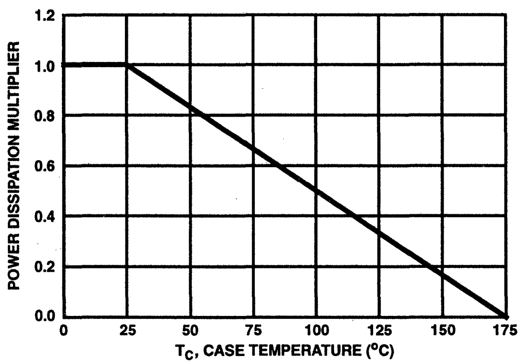


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Example Waveforms

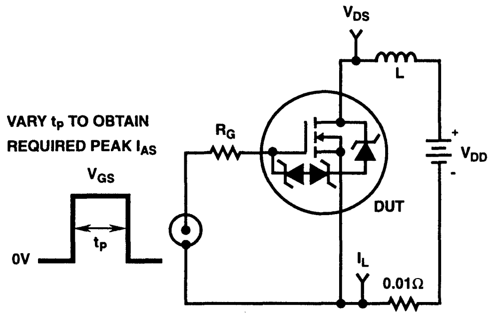


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

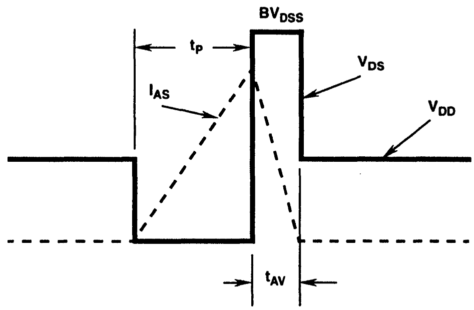


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

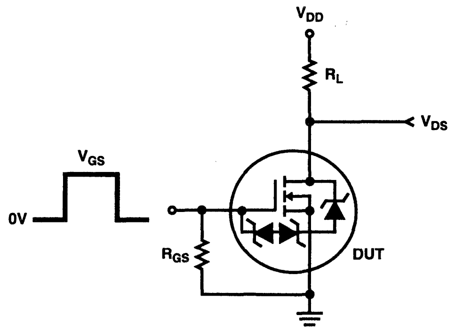


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

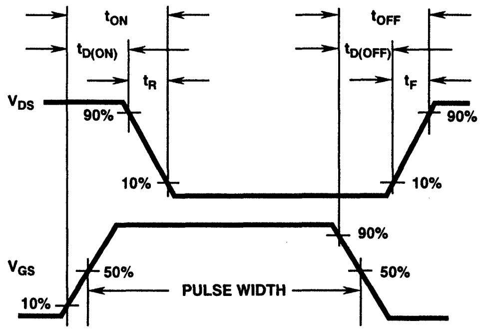


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFP23N06LE, RF1S23N06LE, RF1S23N06LESM

SUBCKT 23N06LE 2 1 3 ; rev 9/27/95

CA 12 8 2.60e-9
CB 15 14 2.55e-9
CIN 6 8 7.75e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 66.01
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

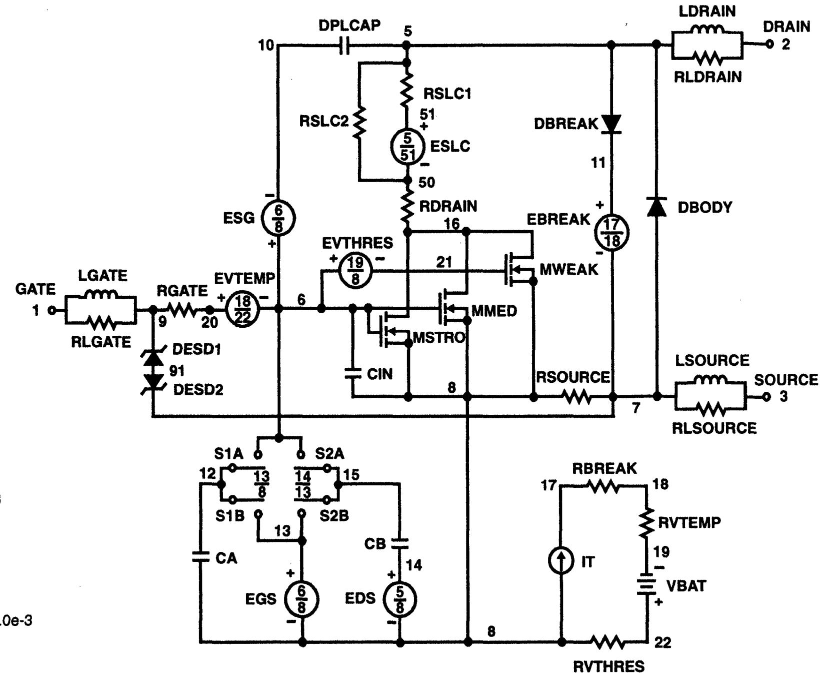
LDRAIN 2 5 1e-9
LGATE 1 9 5.15e-9
LSOURCE 3 7 5.15e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 15e-3
RGATE 9 20 2.5
RLDRAIN 2 5 10
RLGATE 1 9 51.5
RLSOURCE 3 7 51.5
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 20.0e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1



ESLC 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*78),7.5))}

.MODEL DBODYMOD D (IS = 3.18e-13 RS = 9.14e-3 TRS1 = 1.84e-3 TRS2 = 9.51e-7 CJO = 7.22e-10 TT = 4.96e-8 M = 0.44)
.MODEL DBREAKMOD D (RS = 1.39e-1 TRS1 = -5.20e-4 TRS2 = -4.16e-6)
.MODEL DESD1MOD D (BV = 12.35 TBV1 = 0 TBV2 = 0 RS = 45 TRS1 = 1.2e-6 TRS2 = 0)
.MODEL DESD2MOD D (BV = 12.36 TBV1 = 0 TBV2 = 0 RS = 0 TRS1 = 1.2e-6 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 5e-10 IS = 1e-30 N = 10 M = 0.60)
.MODEL MMEDMOD NMOS (VTO = 1.59 KP = 1.75 S = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 2.5)
.MODEL MSTROMOD NMOS (VTO = 1.90 KP = 29 S = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.378 KP = 0.075 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 25 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 9.99e-4 TC2 = 7.71e-12)
.MODEL RDRAINMOD RES (TC1 = 1.27e-2 TC2 = 4.73e-5)
.MODEL RSLCMOD RES (TC1 = 2.41e-3 TC2 = 5.10e-6)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -1.11e-3 TC2 = -4.33e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.34e-3 TC2 = 1.12e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.7 VOFF = -1.7)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.7 VOFF = -4.7)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.2 VOFF = 1.8)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.8 VOFF = -1.2

.ENDS

NOTE:

1. For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options;** IEEE Power Electronics Specialist Conference Records, 1991.

HARRIS SEMICONDUCTOR

RFP30N06LE, RF1S30N06LE, RF1S30N06LESM

30A, 60V, ESD Rated, Avalanche Rated, Logic Level N-Channel Enhancement-Mode Power MOSFETs

July 1995

Features

- 30A, 60V
- $r_{DS(ON)} = 0.047\Omega$
- 2kV ESD Protected
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RFP30N06LE, RF1S30N06LE and RF1S30N06LESM are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

These transistors incorporate ESD protection and are designed to withstand 2kV (Human Body Model) of ESD.

PACKAGE AVAILABILITY

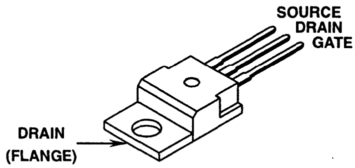
PART NUMBER	PACKAGE	BRAND
RFP30N06LE	TO-220AB	F30N06LE
RF1S30N06LE	TO-262AA	1S30N06L
RF1S30N06LESM	TO-263AB	1S30N06L

NOTE: When ordering use the entire part number. Add suffix, 9A, to obtain the TO-263 variant in tape and reel i.e. RF1S30N06LESM9A.

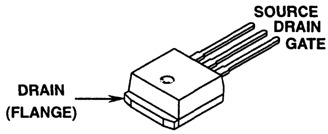
Formerly developmental type TA49027.

Packages

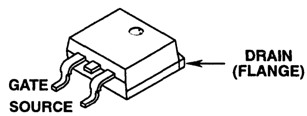
JEDEC TO-220AB



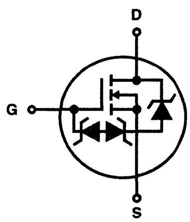
JEDEC TO-262AA



JEDEC TO-263AB



Symbol



Absolute Maximum Ratings $T_C = +25^oC$

		RFP30N06LE, RF1S30N06LE, RF1S30N06LESM	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage	V_{GS}	+10, -8	V
Drain Current			
RMS Continuous	I_D	30	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	96	W
Derate above $+25^oC$		0.645	$W/^oC$
Electrostatic Discharge Rating, MIL-STD-883, Category B(2)	ESD	2	kV
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	^oC
Soldering Temperature of Leads for 10s	T_L	260	^oC

File Number **3629.1**

Electrical Specifications $T_C = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		60	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V$, $V_{GS} = 0V$	$T_C = +25^oC$	-	-	1	µA
			$T_C = +150^oC$	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = +10, -8V$		-	-	10	µA
On Resistance	$r_{DS(ON)}$	$I_D = 30A$, $V_{GS} = 5V$		-	-	0.047	Ω
Turn-On Time	t_{ON}	$V_{DD} = 30V$, $I_D = 30A$, $R_L = 1\Omega$, $V_{GS} = 5V$, $R_{GS} = 2.5\Omega$		-	-	140	ns
Turn-On Delay Time	$t_{D(ON)}$			-	11	-	ns
Rise Time	t_R			-	88	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	30	-	ns
Fall Time	t_F			-	40	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $10V$	$V_{DD} = 48V$, $I_D = 30A$, $R_L = 1.6\Omega$	-	51	62	nC
Gate Charge at 5V	$Q_{G(5)}$	$V_{GS} = 0V$ to $5V$		-	28	34	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $1V$		-	1.8	2.6	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, $f = 1MHz$		-	1350	-	pF
Output Capacitance	C_{OSS}			-	290	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	85	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	1.55	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	80	$^oC/W$

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 30A$	-	-	1.5	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 30A$, $dI_{SD}/dt = 100A/\mu s$	-	-	125	ns

Typical Performance Curves

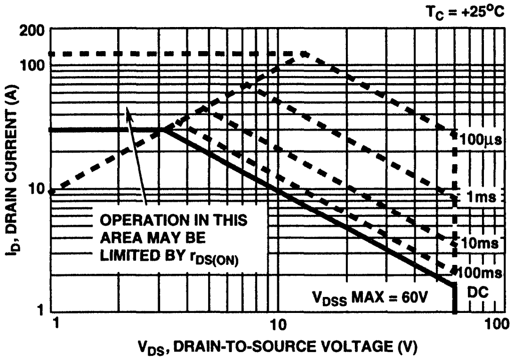


FIGURE 1. SAFE OPERATING AREA CURVE

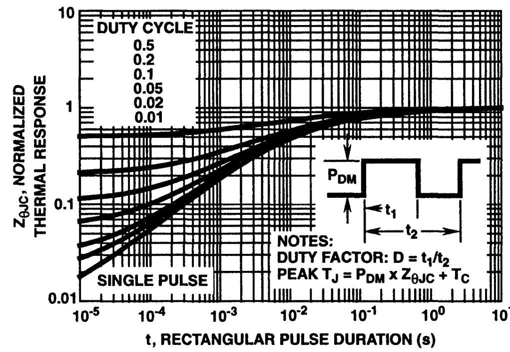


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

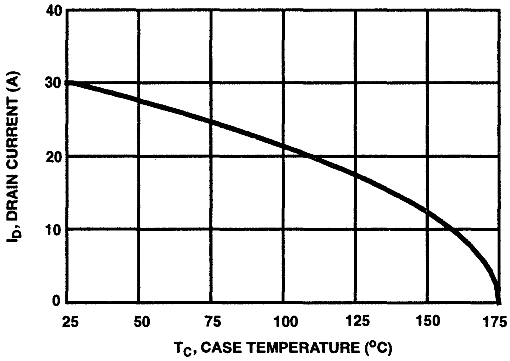


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

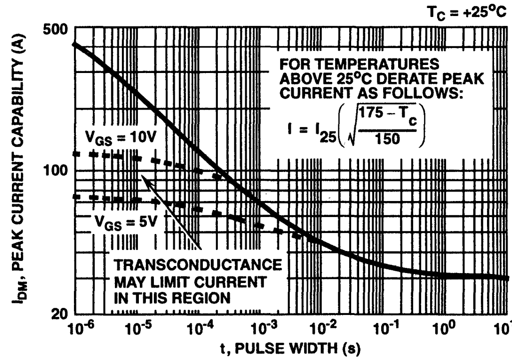


FIGURE 4. PEAK CURRENT CAPABILITY

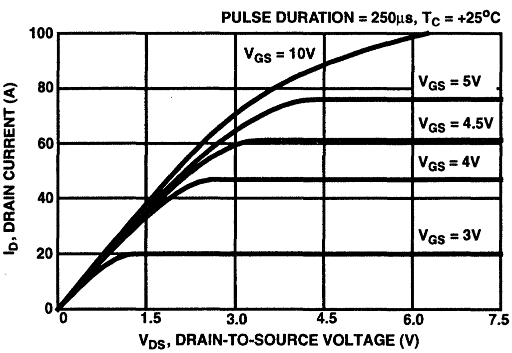


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

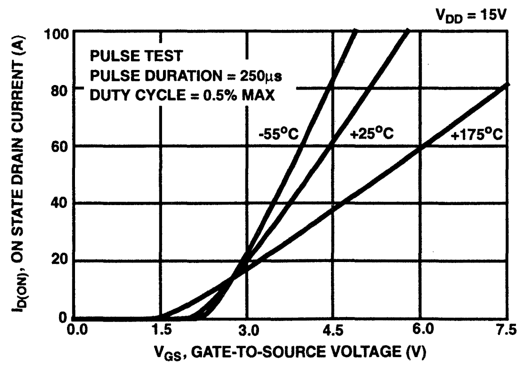


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

5 LOGIC LEVEL POWER MOSFETS

Typical Performance Curves (Continued)

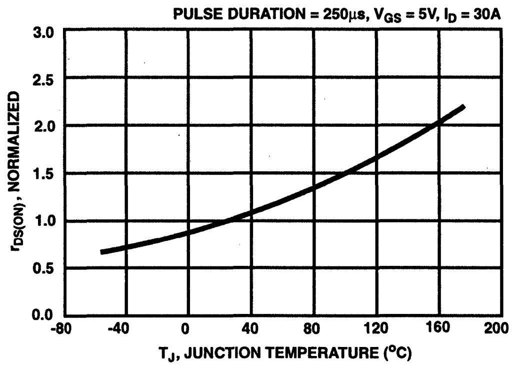


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

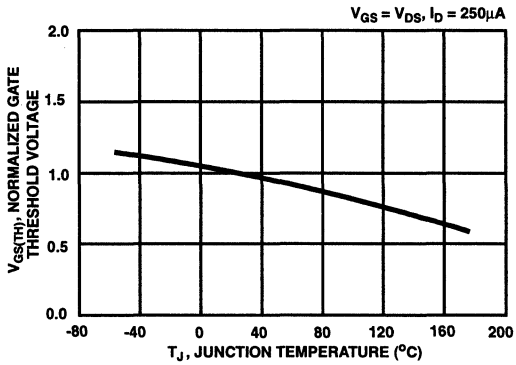


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

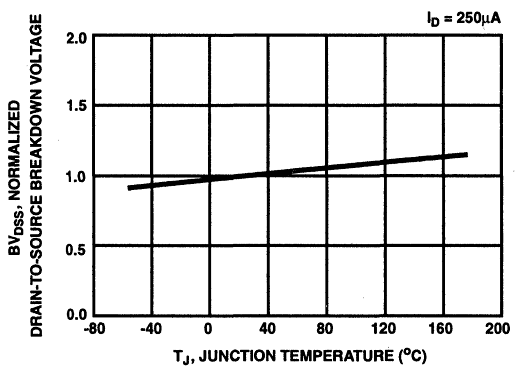


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

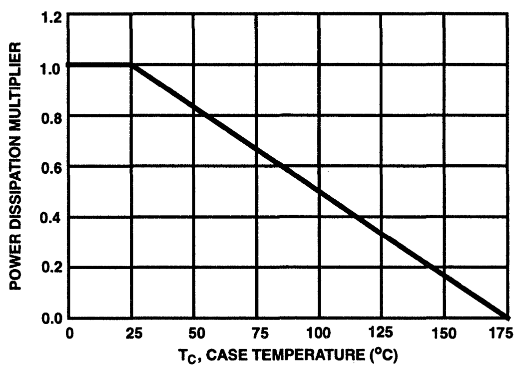


FIGURE 10. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

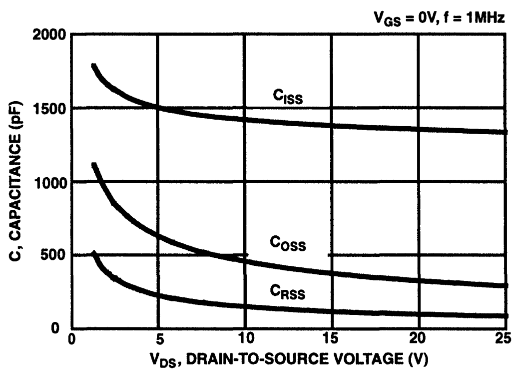


FIGURE 11. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

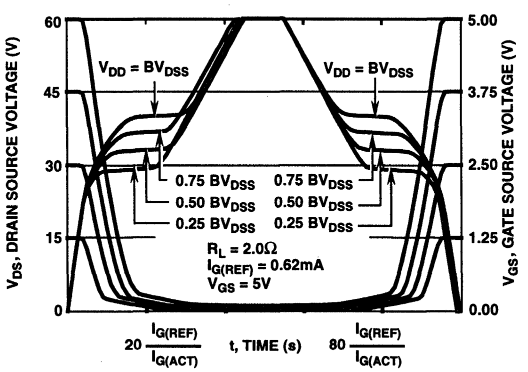


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

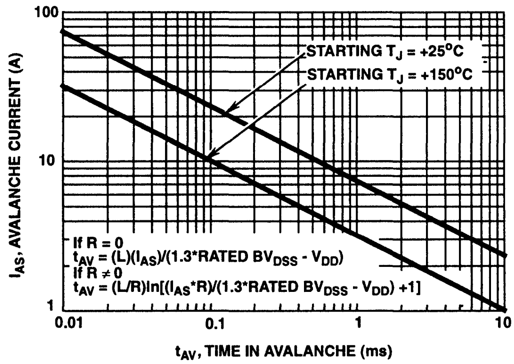


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING

Test Circuits and Waveforms

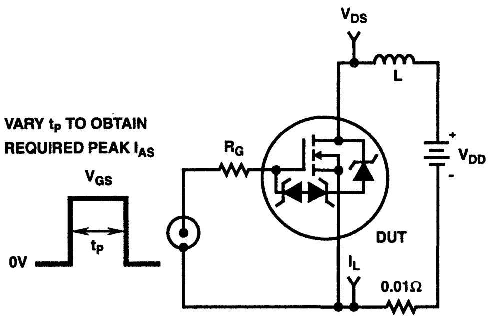


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

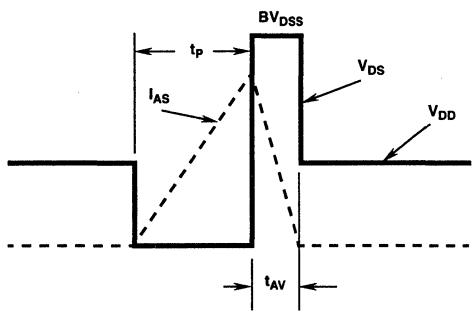


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

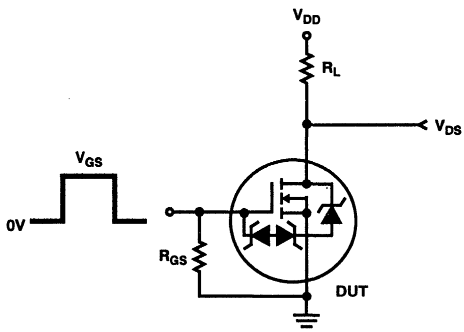


FIGURE 16. RESISTIVE SWITCHING TEST CIRCUIT

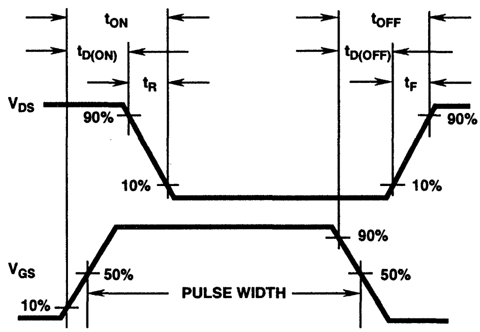
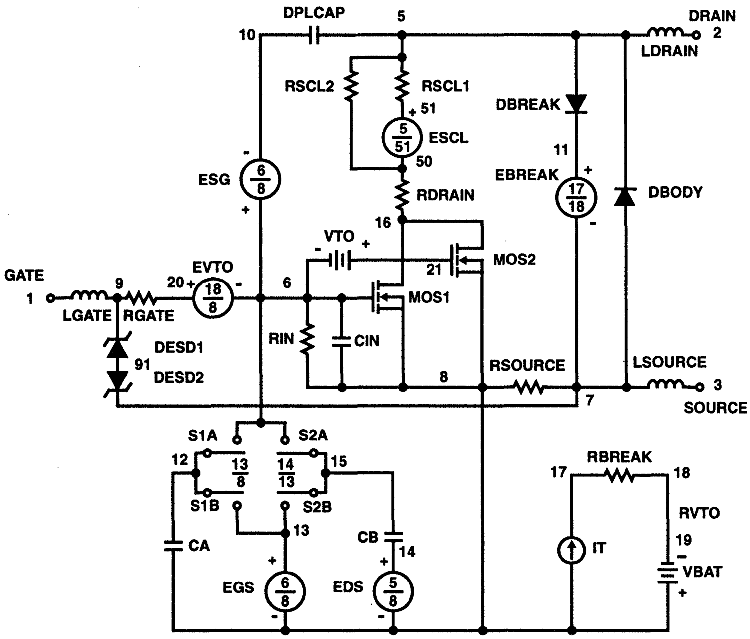


FIGURE 17. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFP30N06LE, RF1S30N06LE, RF1S30N06LESM




```
SUBCKT RFP30N06LE 2 1 3;     rev 6/2/93
CA 12 8 1 3.34e-9
CB 15 14 3.44e-9
CIN 6 8 0 1.343e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 75.39
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 7.22e-9
LSOURCE 3 7 6.31e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 11.86e-3
RGATE 9 20 2.52
RIN 6 8 1e9
RSCL1 5 51 RSLVCMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 26.6e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.5

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/89,7))

.MODEL DBDMOD D (IS = 3.80e-13 RS = 1.12e-2 TRS1 = 1.61e-3 TRS2 = 6.08e-6 CJO = 1.05e-9 TT = 3.84e-8)
.MODEL DBKMOD D (RS = 1.82e-1 TRS1 = 7.50e-3 TRS2 = -4.0e-5)
.MODEL DESD1MOD D (BV = 13.54 TBV1 = 0 TBV2 = 0 RS = 45.5 TRS1 = 0 TRS2 = 0)
.MODEL DESD2MOD D (BV = 11.46 TBV1 = -7.576e-4 TBV2 = -3.0e-6 RS = 0 TRS1 = 0 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 0.591e-9 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 1.94 KP = 139.2 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 1.07e-3 TC2 = -3.03e-7)
.MODEL RDSMOD RES (TC1 = 5.38e-3 TC2 = 1.64e-5)
.MODEL RSLVCMOD RES (TC1 = 1.75e-3 TC2 = 3.90e-6)
.MODEL RVTOMOD RES (TC1 = -2.15e-3 TC2 = -5.43e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.05 VOFF = -1.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.5 VOFF = -4.05)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.2 VOFF = 2.8)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.8 VOFF = -2.2)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records 1991.

HARRIS SEMICONDUCTOR

RFG40N10LE, RFP40N10LE, RF1S40N10LE, RF1S40N10LESM

40A, 100V, ESD Rated, Avalanche Rated, Logic Level N-Channel, Enhancement-Mode Power MOSFETs

December 1995

Features

- 40A, 100V
- $r_{DS(ON)} = 0.040\Omega$
- 2kV ESD Protected
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFG40N10LE, RFP40N10LE, RF1S40N10LE, and RF1S40N10LESM are N-channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

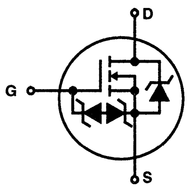
PACKAGE AVAILABILITY

PART NUMBER	PACKAGE	BRAND
RFG40N10LE	TO-247	FG40N10L
RFP40N10LE	TO-220AB	FP40N10L
RF1S40N10LE	TO-262AA	F40N10LE
RF1S40N10LESM	TO-263AB	F40N10LE

NOTE: When ordering, use the entire part number. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, i.e. RF1S40N10LESM9A.

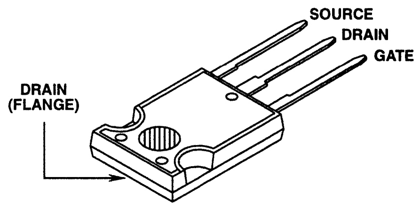
Formerly developmental type TA49163.

Symbol

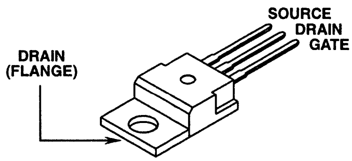


Packages

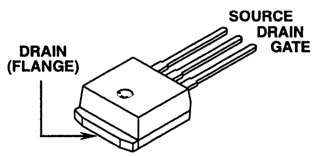
JEDEC STYLE TO-247



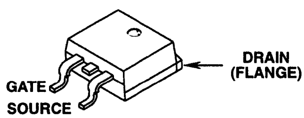
JEDEC TO-220AB



JEDEC TO-262AA



JEDEC TO-263AB



Absolute Maximum Ratings $T_C = +25^oC$

		RFG40N10LE, RFP40N10LE, RF1S40N10LE, RF1S40N10LESM	UNITS
Drain-Source Voltage	V_{DSS}	100	V
Drain-Gate Voltage ($R_{GS} = 1M\Omega$)	V_{DGR}	100	V
Gate-Source Voltage (Note)	V_{GS}	±10	V
Continuous Drain Current	I_D	40	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25^oC$	P_D	150	W
Derate above +25°C		1.00	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	ESD	2	kV

NOTE: May be exceeded if gate current is limited to 1mA.

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V		100	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} =100V, V_{GS} = 0V	T_C = +25°C	-	-	1	µA
			T_C = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	10	µA
On Resistance	$r_{DS(ON)}$	I_D = 40A, V_{GS} = 5V		-	-	0.040	Ω
Turn-On Time	t_{ON}	V_{DD} = 50V, I_D = 40A, R_L = 1.25Ω, V_{GS} = 5V, R_{GS} = 2.5Ω		-	-	200	ns
Turn-On Delay Time	$t_{D(ON)}$			-	22	-	ns
Rise Time	t_R			-	140	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	70	-	ns
Fall Time	t_F			-	65	-	ns
Turn-Off Time	t_{OFF}			-	-	165	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 80V, I_D = 40A, R_L = 2.0Ω	-	145	180	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0V to 5V		-	85	105	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to 1V		-	3	4	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	3000	-	pF
Output Capacitance	C_{OSS}			-	500	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	200	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	1.0	°C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	TO-247		-	-	30	°C/W
		TO-220, TO-262, and TO-263		-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 40A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 40A, dI_{SD}/dt = 100A/µs	-	-	205	ns

Typical Performance Curves

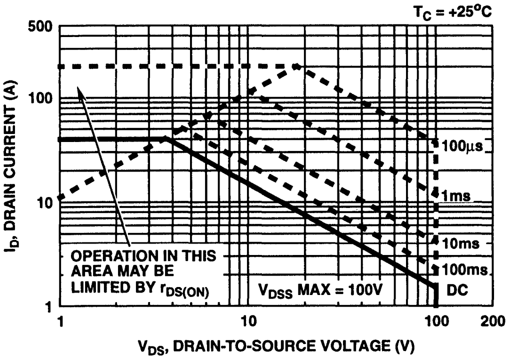


FIGURE 1. SAFE OPERATING AREA CURVE

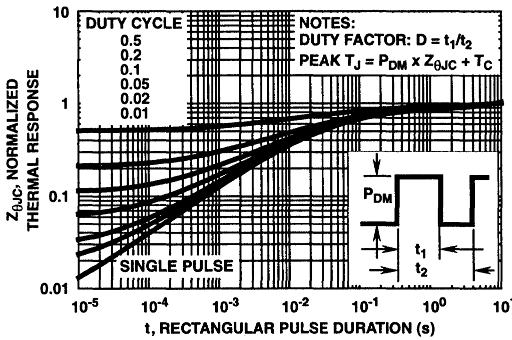


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

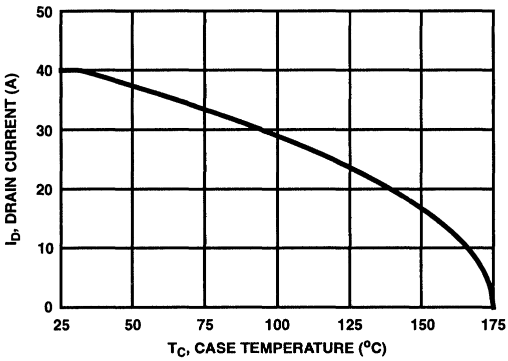


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

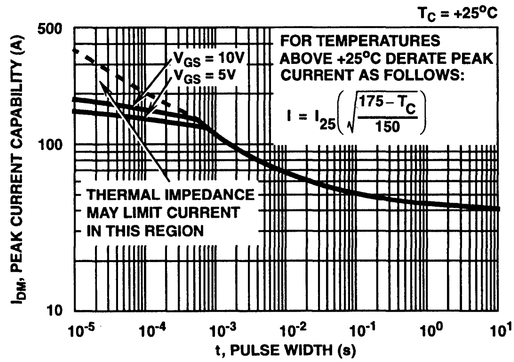


FIGURE 4. PEAK CURRENT CAPABILITY

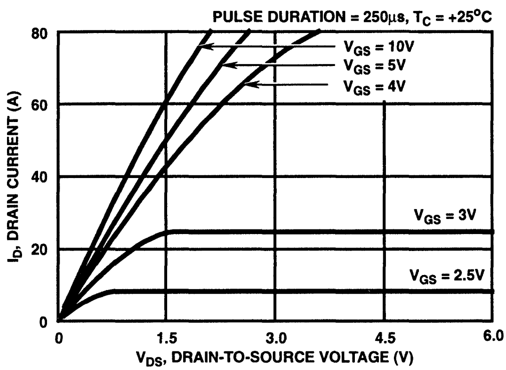


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

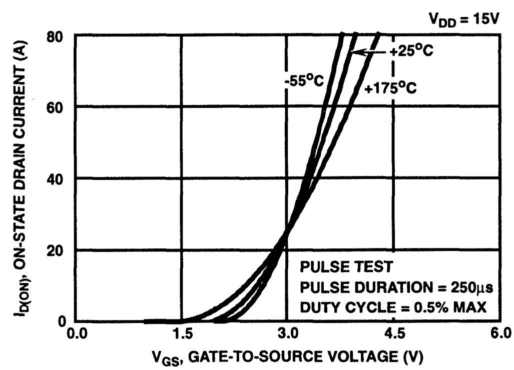


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

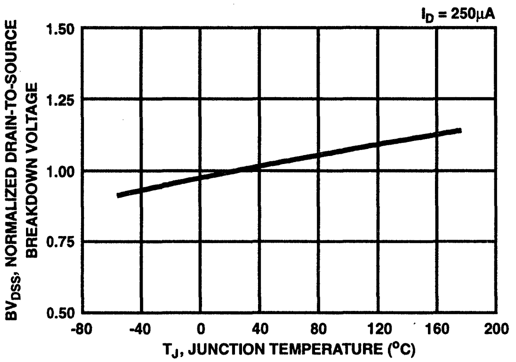


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

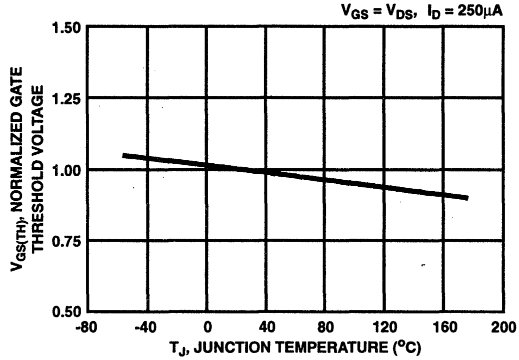


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

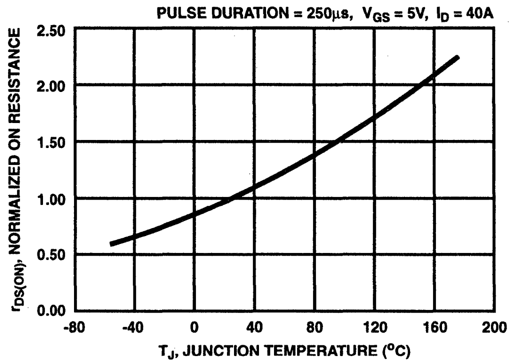


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

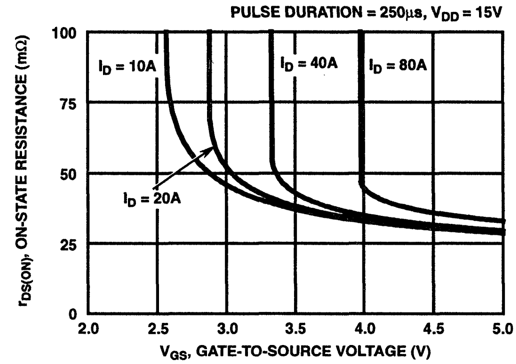


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

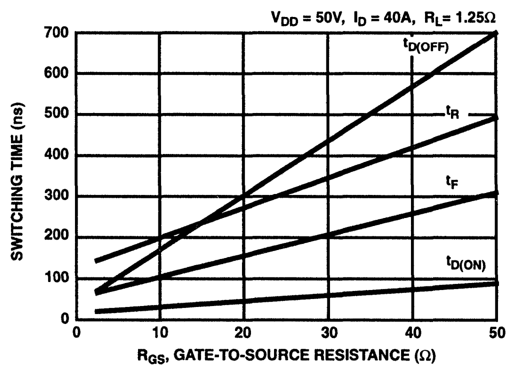


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

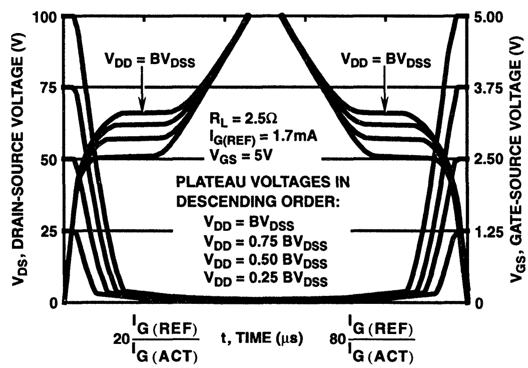


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

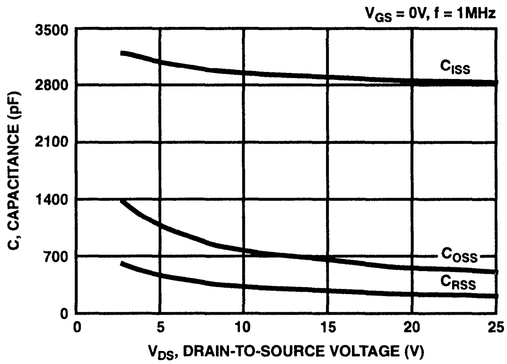


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

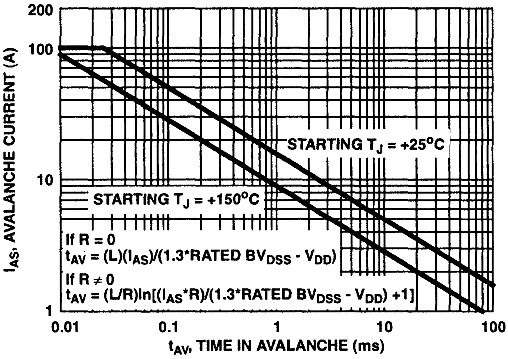


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

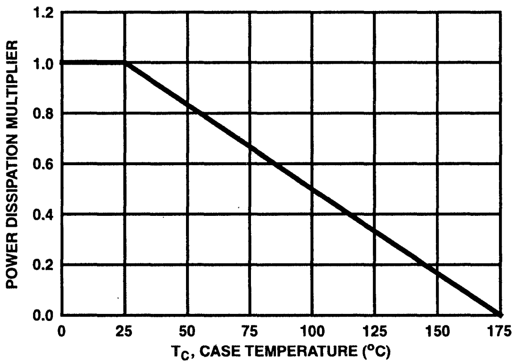


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms

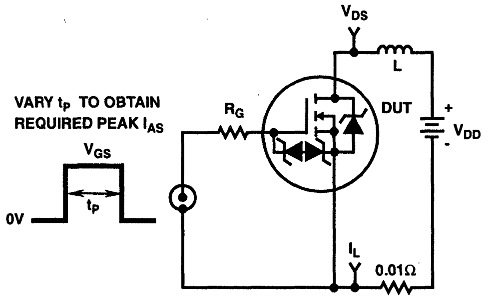


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

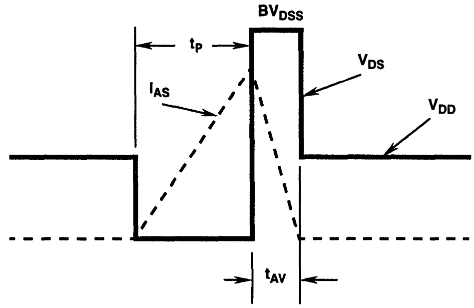


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

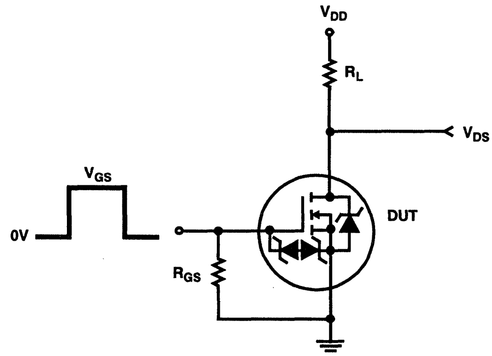


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

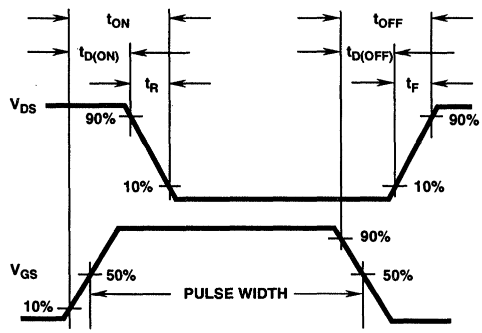


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RFG40N10LE, RFP40N10LE, RF1S40N10LE, RF1S40N10LESM

SUBCKT 40N10LE 2 1 3 ;   rev 8/15/95

```
CA 12 8 11.0e-9
CB 15 14 10.4e-9
CIN 6 8 2.62e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 114.7
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 7.05e-9
LSOURCE 3 7 3.79e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 19.13e-3
RGATE 9 20 1.19
RLDRAIN 2 5 10
RLGATE 1 9 70.5
RLSOURCE 3 7 37.9
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 1e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

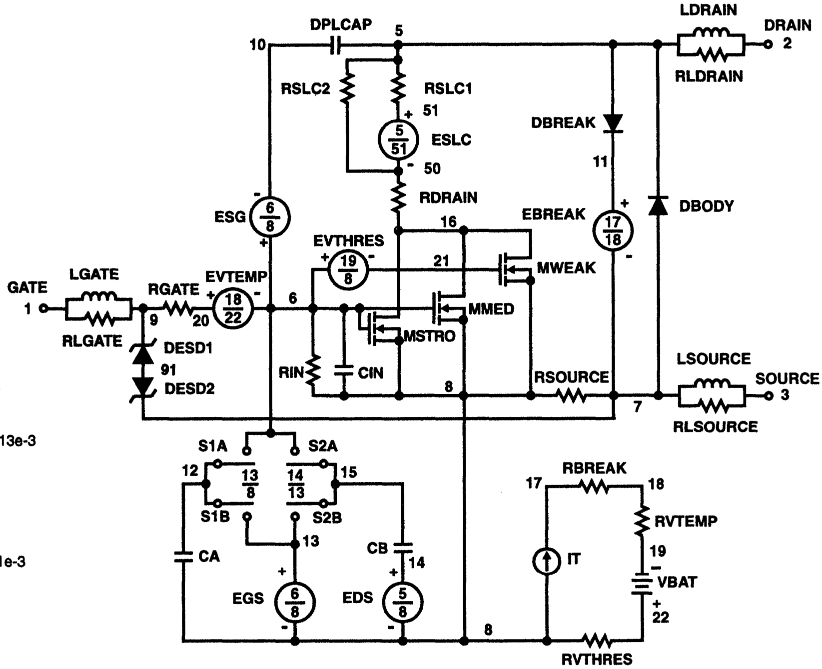
S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*115),4))}

.MODEL DBODYMOD D (IS = 2.0e-12 RS = 9.60e-3 TRS1 = 1.3e-3 TRS2 = -1.16e-7 CJO = 1.50e-9 TT = 1.05e-7 M = 0.5)
.MODEL DBREAKMOD D (RS = 1.92e-1 TRS1 = 1.60e-3 TRS2 = 3.47e-6)
.MODEL DESD1MOD D (BV = 12.43 TBV1 = 0 TBV2 = 0 RS = 57 TRS1 = 0 TRS2 = 0)
.MODEL DESD2MOD D (BV = 12.45 TBV1= -1.5e-5 TBV2 = 1e-7 RS = 0 TRS1 = 0 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 1.25e-9 IS = 1e-30 N = 10 M = 0.55)
.MODEL MMEDMOD NMOS (VTO = 1.50 KP = 0.40 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.19)
.MODEL MSTROMOD NMOS (VTO = 1.83 KP = 37.00 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 1.335 KP = 0.08 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 11.9 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.04e-3 TC2 = -6.00e-7)
.MODEL RDRAINMOD RES (TC1 = 7.33e-3 TC2 = 2.00e-5)
.MODEL RSLCMOD RES (TC1 = 2.25-3 TC2 = 0)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -0.8e-3 TC2 = -2.5e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.98e-3 TC2 = 1.38e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.25 VOFF = -1.25)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.25 VOFF = -4.25)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.35 VOFF = 1.65)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.65 VOFF = -0.35)

.ENDS
```



NOTE:

1. For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options;** IEEE Power Electronics Specialist Conference Records, 1991.

RFP45N03L, RF1S45N03L, RF1S45N03LSM

HARRIS SEMICONDUCTOR

45A, 30V, Avalanche Rated N-Channel Logic Level Enhancement-Mode Power MOSFETs

December 1995

Features

- 45A, 30V
- $r_{DS(ON)} = 0.022\Omega$
- *Temperature Compensating* PSPICE Model
- Can be Driven Directly from CMOS, NMOS, and TTL Circuits
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- +175°C Operating Temperature

Description

The RFP45N03L, RF1S45N03L, and RF1S45N03LSM are N-Channel power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI circuits, gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers and relay drivers. These transistors can be operated directly from integrated circuits.

PACKAGE AVAILABILITY

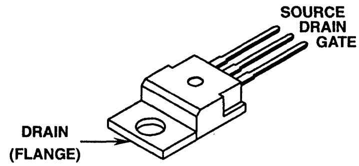
PART NUMBER	PACKAGE	BRAND
RFP45N03L	TO-220AB	FP45N03L
RF1S45N03L	TO-262AA	F45N03L
RF1S45N03LSM	TO-263AB	F45N03L

NOTE: When ordering, use the entire part number; e.g. RFP45N03L. Add the suffix, 9A, to obtain the TO-263AB variant in tape and reel, e.g. RF1S45N03LSM9A.

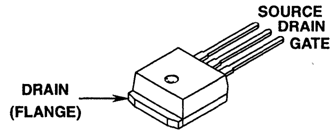
Formerly developmental type TA49030.

Packages

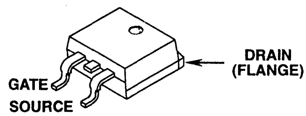
JEDEC TO-220AB



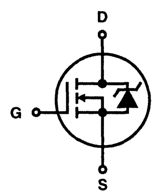
JEDEC TO-262AA



JEDEC TO-263AB



Symbol



Absolute Maximum Ratings $T_C = +25°C$

		RFP45N03L, RF1S45N03L, RF1S45N03LSM	UNITS
Drain-Source Voltage	V_{DSS}	30	V
Drain-Gate Voltage	V_{DGR}	30	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current			
Continuous	I_D	45	A
Pulsed Drain Current	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_C = +25°C$	P_D	90	W
Derate above +25°C		0.606	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number 4005.1

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	T_C = +25°C	-	-	1	μA
			T_C = +150°C	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 45A, V_{GS} = 5V		-	-	0.022	Ω
Turn-On Time	t_{ON}	V_{DD} = 15V, I_D = 45A, R_L = 0.33Ω, V_{GS} = 5V, R_{GS} = 5Ω		-	-	260	ns
Turn-On Delay Time	$t_{D(ON)}$			-	15	-	ns
Rise Time	t_R			-	160	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	20	-	ns
Fall Time	t_F			-	20	-	ns
Turn-Off Time	t_{OFF}			-	-	60	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 24V, I_D = 45A, R_L = 0.533Ω	-	50	60	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0V to 5V		-	30	36	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to 1V		-	1.5	1.8	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	1650	-	pF
Output Capacitance	C_{OSS}			-	575	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	200	-	pF
Thermal Resistance Junction-to-Case	$R_{\theta JC}$			-	-	1.65	°C/W
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$			-	-	80	°C/W

Source-Drain Diode Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 45A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 45A, dI_{SD}/dt = 100A/μs	-	-	125	ns

Typical Performance Curves

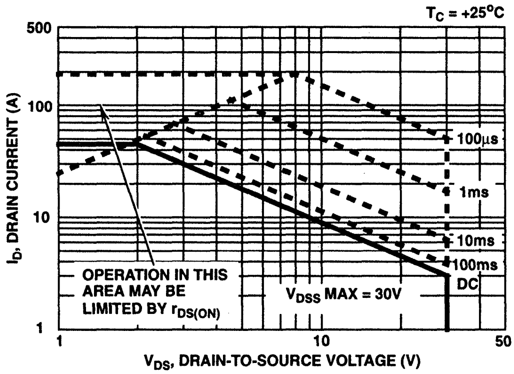


FIGURE 1. SAFE OPERATING AREA CURVE

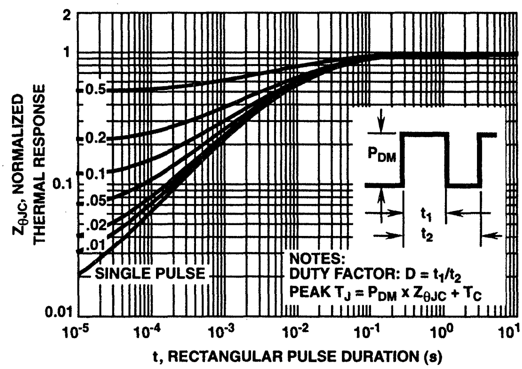


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

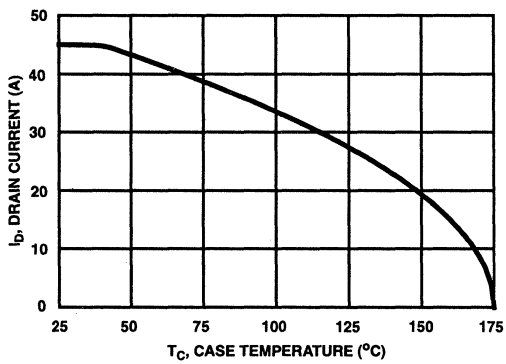


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

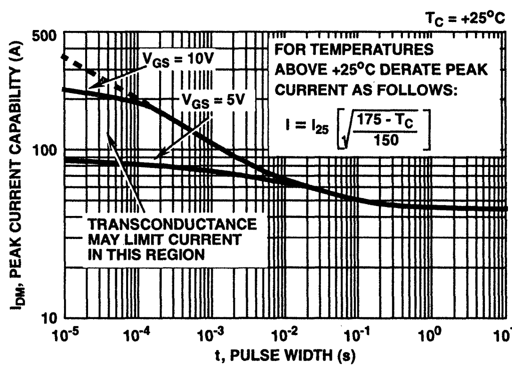


FIGURE 4. PEAK CURRENT CAPABILITY

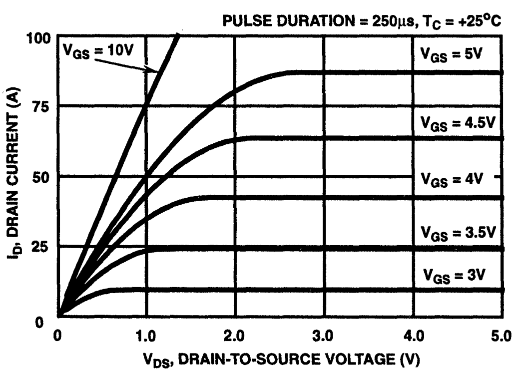


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

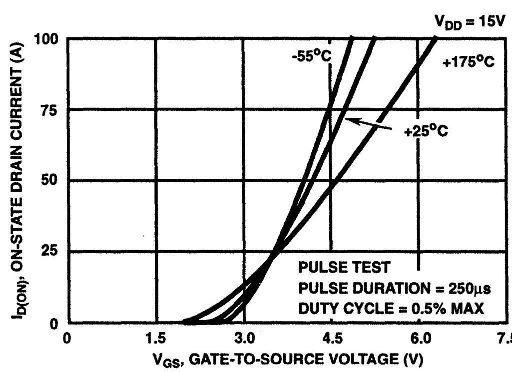


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

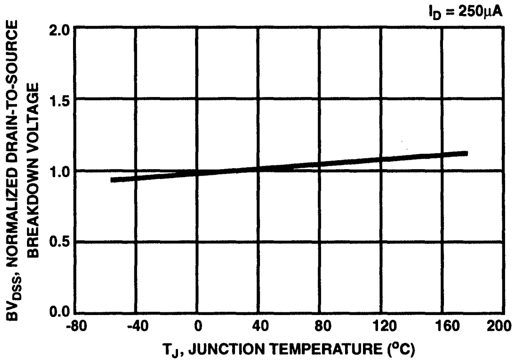


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

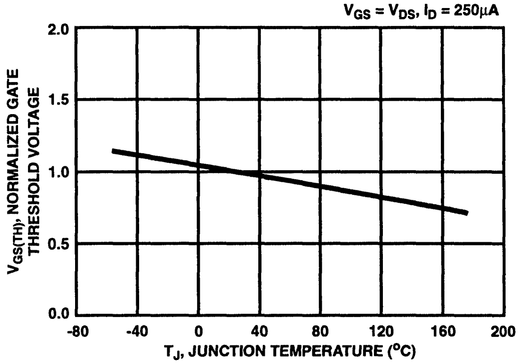


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

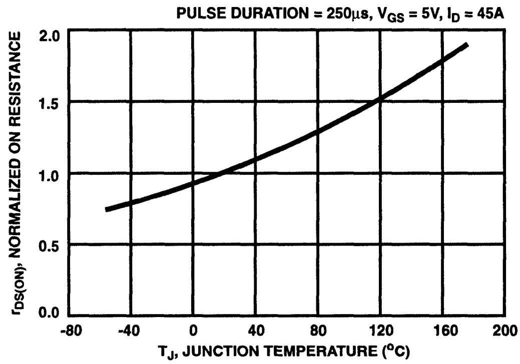


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

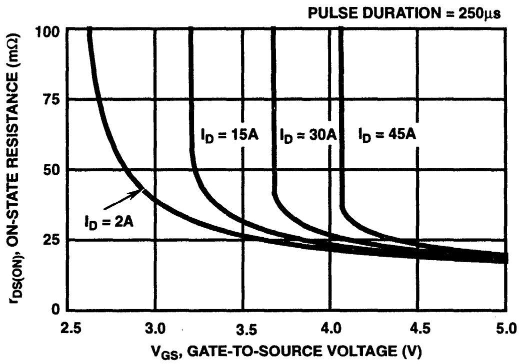


FIGURE 10. TYPICAL $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

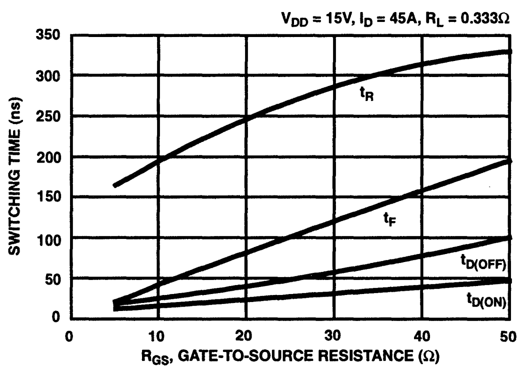


FIGURE 11. TYPICAL SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

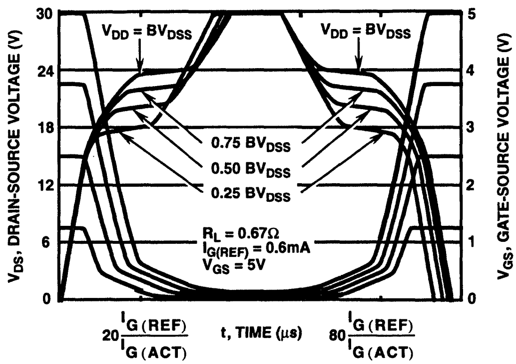


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

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LOGIC LEVEL POWER MOSFETs

Typical Performance Curves (Continued)

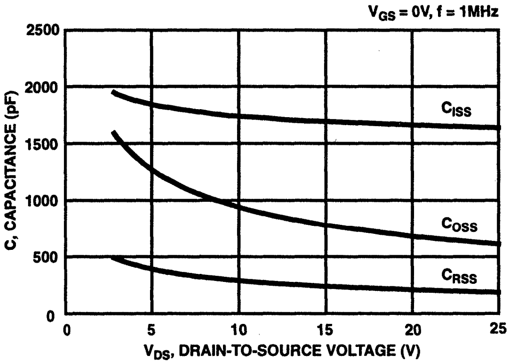

FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

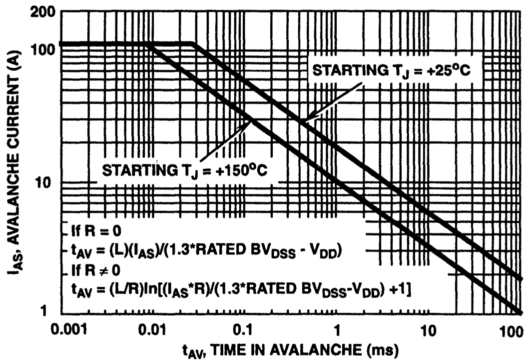

FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

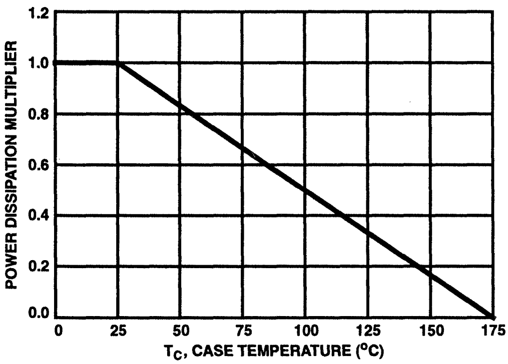

FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms

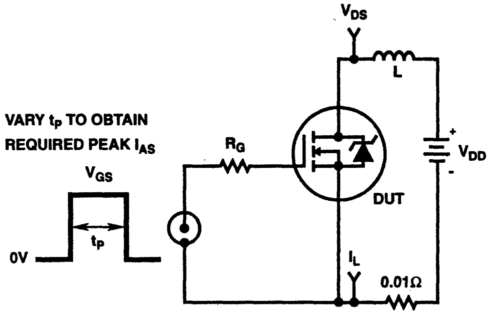

FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

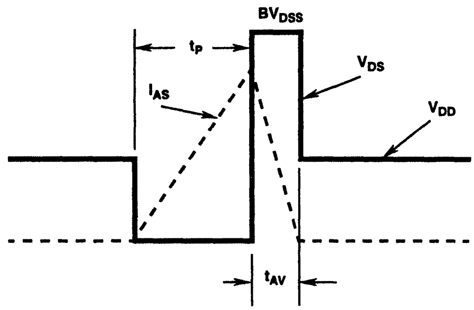

FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

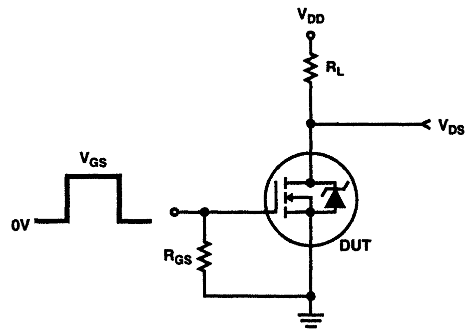

FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

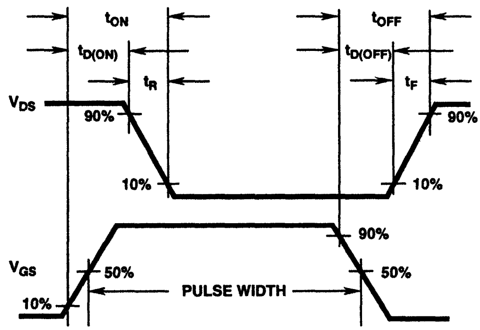

FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

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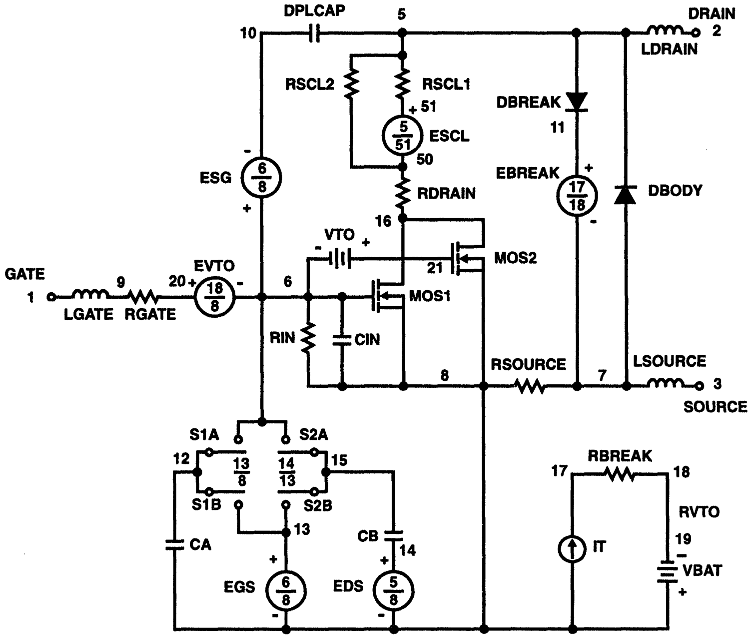
LOGIC LEVEL POWER MOSFETS

Temperature Compensated PSPICE Model for the RFP45N03L, RF1S45N03L, RF1S45N03LSM




```
.SUBCKT RFP45N03L 2 1 3 ;    rev 11/22/94

CA 12 8 2.55e-9
CB 15 14 2.64e-9
CIN 6 8 1.45e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 33.3
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 4.9e-9
LSOURCE 3 7 4.9e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 50 16 RDSMOD 0.14e-3
RGATE 9 20 0.89
RIN 6 8 1e9
RSCL1 5 51 RSCLMOD 1e-6
RSCL2 5 50 1e3
RSOURCE 8 7 RDSMOD 10.31e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.583

ESCL 51 50 VALUE = {(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)*1e6/176,6))}

.MODEL DBDMOD D (IS = 3.61e-13 RS = 5.06e-3 TRS1 = 3.05e-3 TRS2 = 7.57e-6 CJO = 2.16e-9 TT = 2.18e-8)
.MODEL DBKMOD D (RS = 1.66e-1 TRS1 = -2.97e-3 TRS2 = 7.57e-6)
.MODEL DPLCAPMOD D (CJO = 0.96e-9 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 2.313 KP = 53.82 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 8.95e-4 TC2 = -1e-7)
.MODEL RDSMOD RES (TC1 = 3.82e-3 TC2 = 1.17e-5)
.MODEL RSCLMOD RES (TC1 = 2.03e-3 TC2 = 0.45e-5)
.MODEL RVTOMOD RES (TC1 = -2.27e-3 TC2 = -5.75e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.82 VOFF= -2.82)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.82 VOFF= -4.82)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.67 VOFF= 2.33)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.33 VOFF= -2.67)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; written by William J. Hepp and C. Frank Wheatley.

POWER MOSFETs 6

INTELLIGENT DISCRETES

PAGE

INTELLIGENT DISCRETE DATA SHEET

6

INTELLIGENT DISCRETES

RLD03N06CLE, RLD03N06CLESM, RLP03N06CLE

0.3A, 60V, ESD Rated, Current Limited, Voltage Clamped Logic Level N-Channel Enhancement-Mode Power MOSFETs

December 1995

Features

- **0.30A, 60V**
- **$r_{DS(ON)} = 6.0\Omega$**
- **Built in Current Limit I_{LIMIT} 0.140 to 0.210A at 150°C**
- **Built in Voltage Clamp**
- ***Temperature Compensating* PSPICE Model**
- **2kV ESD Protected**
- **Controlled Switching Limits EMI and RFI**

Description

The RLD03N06CLE, RLD03N06CLESM and RLP03N06CLE are intelligent monolithic power circuits which incorporate a lateral bipolar transistor, resistors, zener diodes and a power MOS transistor. The current limiting of these devices allow it to be used safely in circuits where a shorted load condition may be encountered. The drain-source voltage clamping offers precision control of the circuit voltage when switching inductive loads. The "Logic Level" gate allows this device to be fully biased on with only 5.0V from gate to source, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

The RLD03N06CLE, RLD03N06CLESM and RLP03N06CLE incorporate ESD protection and are designed to withstand 2kV (Human Body Model) of ESD.

PACKAGING AVAILABILITY

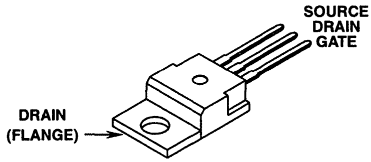
PART NUMBER	PACKAGE	BRAND
RLD03N06CLE	TO-251AA	03N06C
RLD03N06CLESM	TO-252AA	03N06C
RLP03N06CLE	TO-220AB	03N06CLE

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, i.e. RLP03N06CLESM9A.

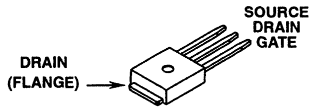
Formerly developmental type TA49026.

Packages

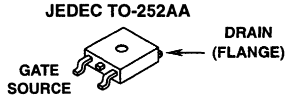
JEDEC TO-220AB



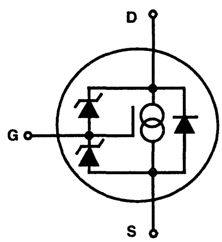
JEDEC TO-251AA



JEDEC TO-252AA



Symbol



Absolute Maximum Ratings $T_C = +25°C$

		RLD03N06CLE, RLD03N06CLESM, RLP03N06CLE	UNITS
Drain Source Voltage	V_{DSS}	60	V
Drain Gate Voltage	V_{DGR}	60	V
Gate Source Voltage (Note)	V_{GS}	+5.5	V
Reverse Voltage Gate Bias Not Allowed			
Drain Current			
RMS Continuous	I_D	Self Limited	
Power Dissipation			
$T_C = +25°C$	P_D	30	W
Derate above +25°C	P_T	0.2	W/°C
Electrostatic Discharge Rating MIL-STD-883, Category B(2)	ESD	2	KV
Operating and Storage Temperature	T_{STG}, T_J	-55 to +175	°C

NOTE: May be exceeded if current is limited to 10mA.

File Number **3948.2**

Electrical Specifications T_C = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		60	-	85	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		1	-	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 45V, V_{GS} = 0V	T_J = +25°C	-	-	50	μA
			T_J = +150°C	-	-	200	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = 5V	T_J = +25°C	-	-	5	μA
			T_J = +150°C	-	-	20	μA
On Resistance	$r_{DS(ON)}$	I_D = 0.100A, V_{GS} = 5V	T_J = +25°C	-	-	6.0	Ω
			T_J = +150°C	-	-	12.0	Ω
Limiting Current	$I_{DS(LIMIT)}$	V_{DS} = 15V, V_{GS} = 5V	T_J = +25°C	280	-	420	mA
			T_J = +150°C	140	-	210	mA
Turn-On Time	t_{ON}	V_{DD} = 30V, I_D = 0.10A, R_L = 300Ω, V_{GS} = 5V, R_{GS} = 25Ω		-	-	7.5	μs
Turn-On Delay Time	$t_{D(ON)}$			-	-	2.5	μs
Rise Time	t_R			-	-	5.0	μs
Turn-Off Delay Time	$t_{D(OFF)}$			-	-	7.5	μs
Fall Time	t_F			-	-	5.0	μs
Turn-Off Time	t_{OFF}			-	-	12.5	μs
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	100	-	pF
Output Capacitance	C_{OSS}			-	65	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	3.0	-	pF
Thermal Resistance Junction to Case	$R_{\theta JC}$			-	-	5.0	°C/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	TO-220 Package		-	-	80	°C/W
		TO-251 and TO-252 Packages		-	-	100	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 0.1A	-	-	1.5	V
Reverse Recovery Time	t_{RR}	I_{SD} = 0.1A, dI_{SD}/dt = 100A/μs	-	-	1.0	ms

Typical Performance Curves

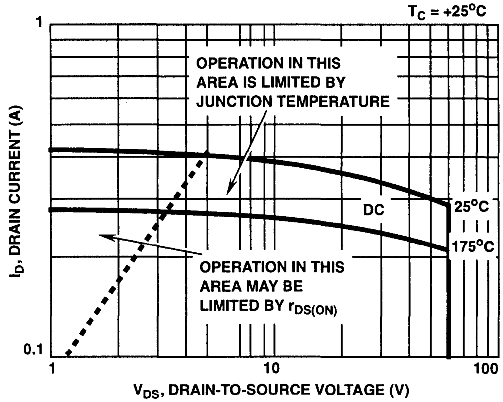


FIGURE 1. SAFE OPERATING AREA CURVE

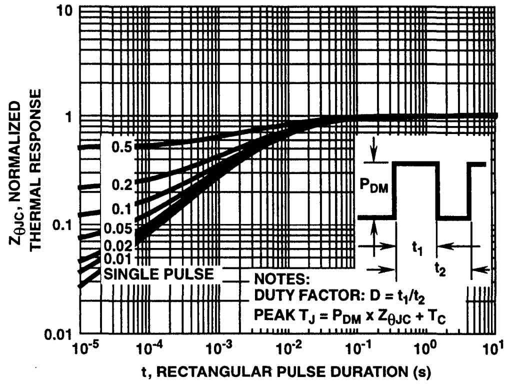


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

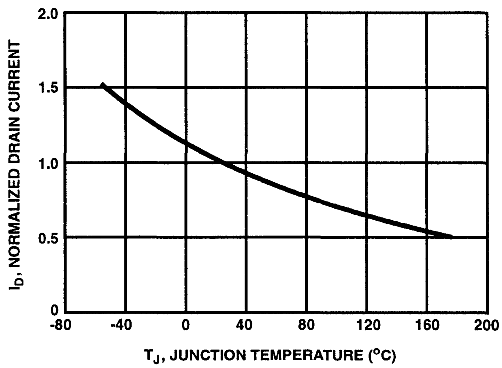


FIGURE 3. TYPICAL NORMALIZED DRAIN CURRENT vs JUNCTION TEMPERATURE

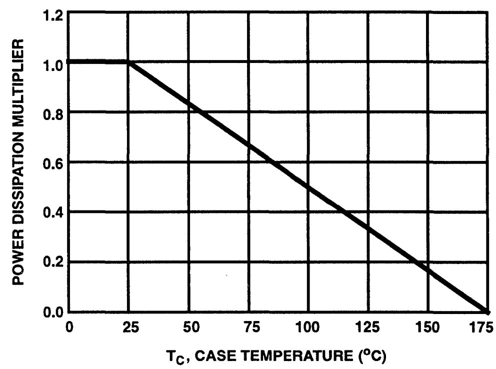


FIGURE 4. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

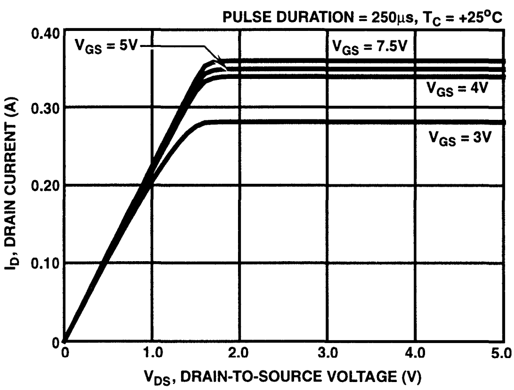


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

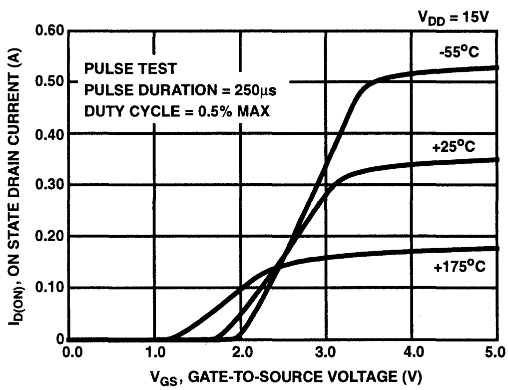


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

6

INTELLIGENT DISCRETES

Typical Performance Curves (Continued)

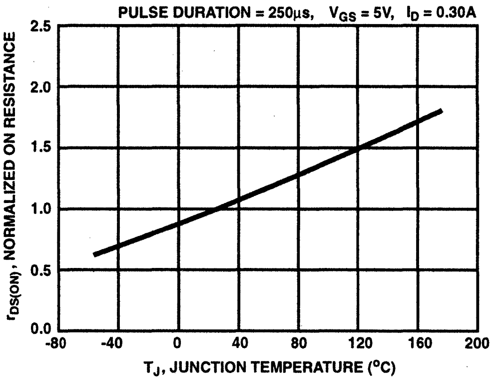


FIGURE 7. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

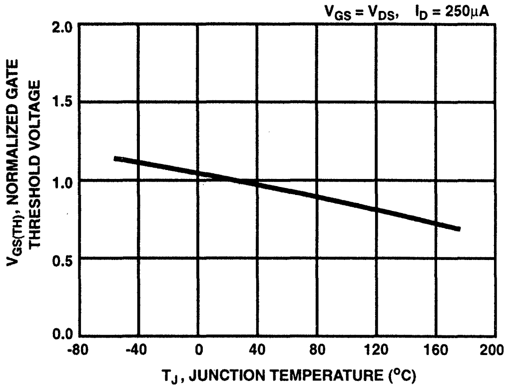


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs TEMPERATURE

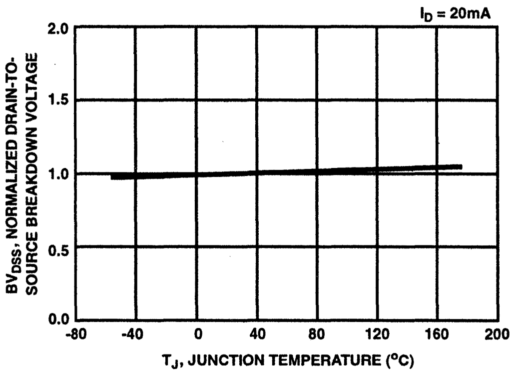


FIGURE 9. NORMALIZED DRAIN SOURCE BREAKDOWN VOLTAGE vs TEMPERATURE

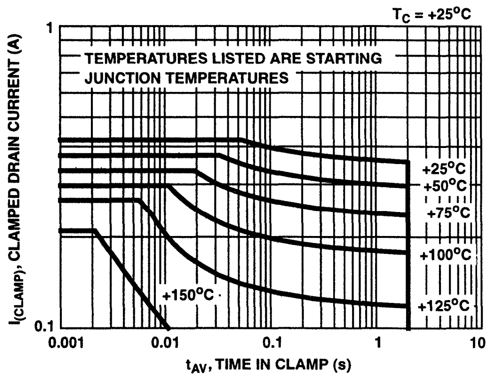


FIGURE 10. SELF-CLAMPED INDUCTIVE SWITCHING

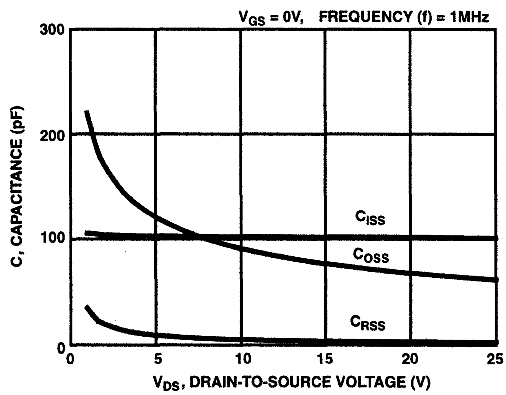


FIGURE 11. TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

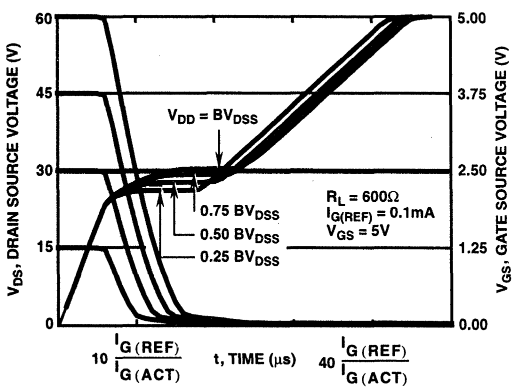


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Test Circuit and Waveform

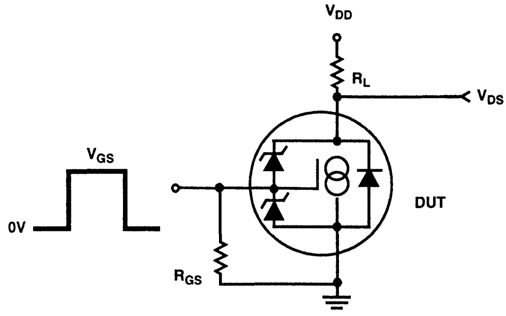


FIGURE 13. RESISTIVE SWITCHING TEST CIRCUIT

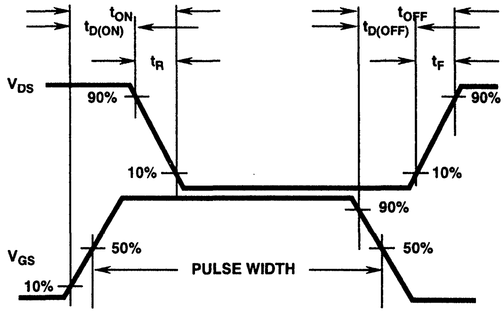


FIGURE 14. RESISTIVE SWITCHING WAVEFORMS

Detailed Description

Temperature Dependence of Current Limiting and Switching Speed Performance

The RLD03N06CLE, RLD03N06CLESM and RLP03N06CLE are a monolithic power device which incorporates a Logic Level power MOSFET transistor with a current sensing scheme and control circuitry to enable the device to self limit the drain source current flow. The current sensing scheme supplies current to a resistor that is connected across the base to emitter of a bipolar transistor in the control section. The collector of this bipolar transistor is connected to the gate of the power MOSFET transistor. When the ratiometric current from the current sensing reaches the value required to forward bias the base emitter junction of this bipolar transistor, the bipolar "turns on". A resistor is incorporated in series with the gate of the power MOSFET transistor allowing the bipolar transistor to adjust the drive on the gate of the power MOSFET transistor to a voltage which then maintains a constant current in the power MOSFET transistor. Since both the ratiometric current sensing scheme and the base emitter unction voltage of the bipolar transistor vary with temperature, the current at which the device limits is a function of temperature. This dependence is shown in Figure 3.

The resistor in series with the gate of the power MOSFET transistor also results in much slower switching performance than in standard power MOSFET transistors. This is an advantage where fast switching can cause EMI or RFI. The switching speed is very predictable.

DC Operation

The limit on the drain to source voltage for operation in current limiting on a steady state (DC) basis is shown in the equation below. The dissipation in the device is simply the applied drain to source voltage multiplied by the limiting current. This device, like most power MOSFET devices today, is limited to 175°C. The maximum voltage allowable can, therefore, be expressed as shown in Equation 1:

$$V_{DS} = \frac{(150^\circ C - T_{AMBIENT})}{I_{LM} \bullet (R_{\theta JC} + R_{\theta JA})} \qquad \text{(EQ. 1)}$$

The results of this equation are plotted in Figure 15 for various heatsinks.

Duty Cycle Operation

In many applications either the drain to source voltage or the gate drive is not available 100% of the time. The copper header on which the RLD03N06CLE, RLD03N06CLESM and RLP03N06CLE is mounted has a very large thermal storage capability, so for pulse widths of less then 1ms, the temperature of the header can be considered a constant, thereby the junction temperature can be calculated simply as shown in Equation 2:

$$T_C = (V_{DS} \bullet I_D \bullet D \bullet R_{\theta CA}) + T_{AMBIENT} \qquad \text{(EQ. 2)}$$

Generally the heat storage capability of the silicon chip in a power transistor is ignored for duty cycle calculations. Making this assumption, limiting junction temperature to 175°C and using the T_C calculated in Equation 2, the expression for maximum V_{DS} under duty cycle operation is shown in Equation 3:

$$V_{DS} = \frac{150^\circ C - T_C}{I_{LM} \bullet D \bullet R_{\theta JC}} \qquad \text{(EQ. 3)}$$

These values are plotted as Figures 16 through 21 for various heatsink thermal resistances.

Limited Time Operations

Protection for a limited period of time is sufficient for many applications. As stated above the heat storage in the silicon chip can usually be ignored for computations of over 10 ms, thereby the thermal equivalent circuit reduces to a simple enough circuit to allow easy computation on the limiting conditions. The variation in limiting current with temperature complicates the calculation of junction temperature, but a simple straight line approximation of the variation is accurate enough to allow meaningful computations. The curves shown as Figures 22 through 25 (RLP03N06CLE) and Figure 26 through 29 (RLD03N06CLE and RLD03N06CLESM) give an accurate indication of how long the specified voltage can be applied to the device in the current limiting mode without exceeding the maximum specified 175°C junction temperature. In practice this tells you how long you have to alleviate the condition causing the current limiting to occur.

Performance Curves

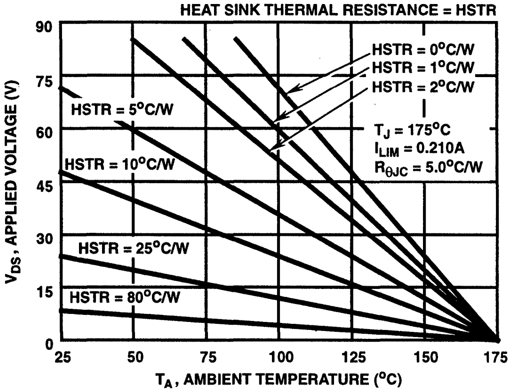


FIGURE 15. DC OPERATION IN CURRENT LIMITING

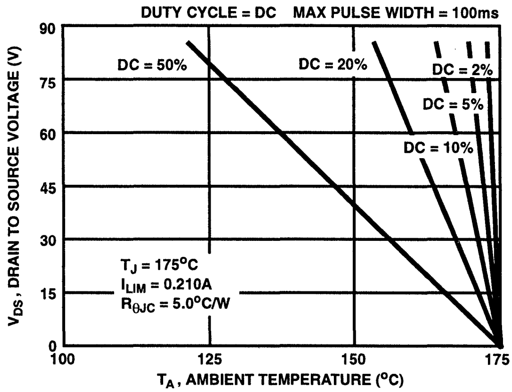


FIGURE 16. MAXIMUM V_{DS} vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HEATSINK THERMAL RESISTANCE = 1°C/W)

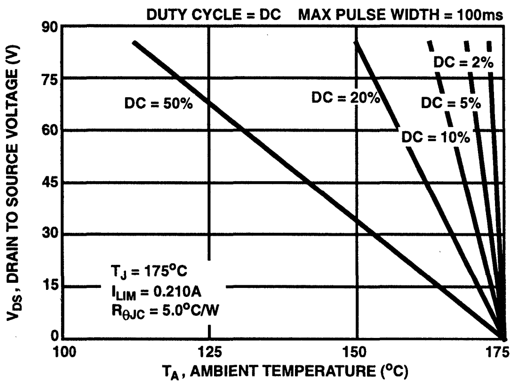


FIGURE 17. MAXIMUM V_{DS} vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 2°C/W)

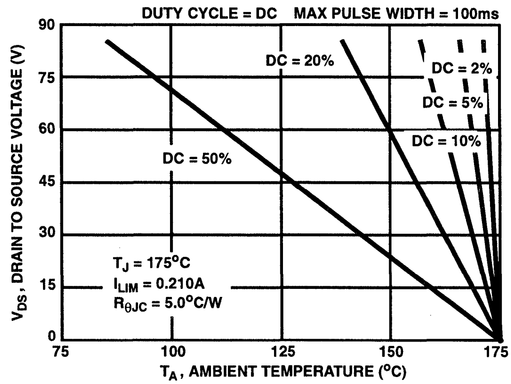


FIGURE 18. MAXIMUM V_{DS} vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 5°C/W)

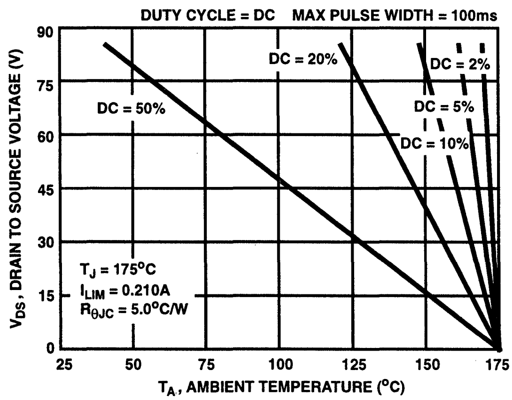


FIGURE 19. MAXIMUM V_{DS} vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 10°C/W)

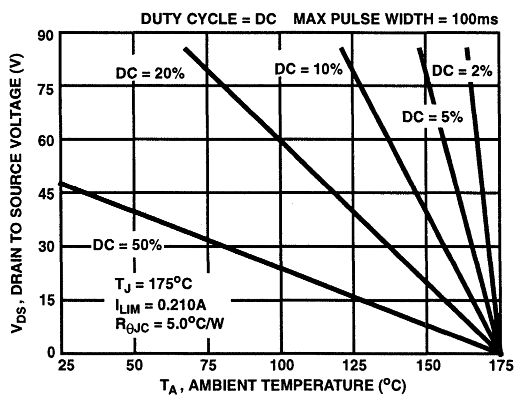


FIGURE 20. MAXIMUM V_{DS} vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 25°C/W)

Performance Curves (Continued)

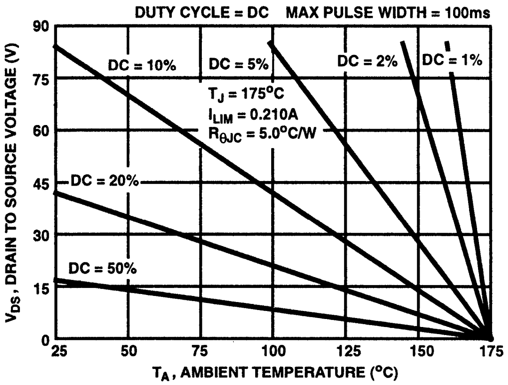


FIGURE 21. MAXIMUM V_{DS} vs AMBIENT TEMPERATURE IN CURRENT LIMITING. (HSTR = 80°C/W)

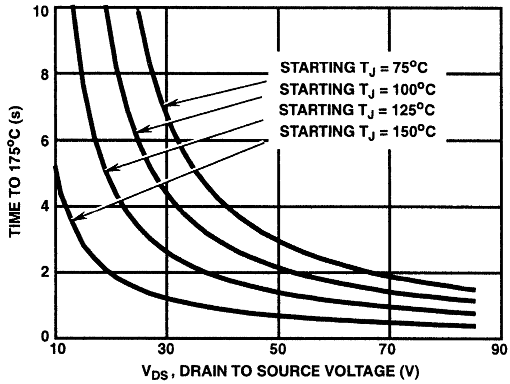


FIGURE 22. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 25°C/W) (HEATSINK THERMAL CAPACITANCE = 0.5J/°C)

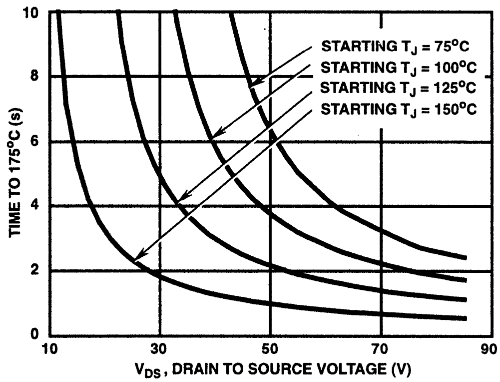


FIGURE 23. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 10°C/W) (HEATSINK THERMAL CAPACITANCE = 1.0J/°C)

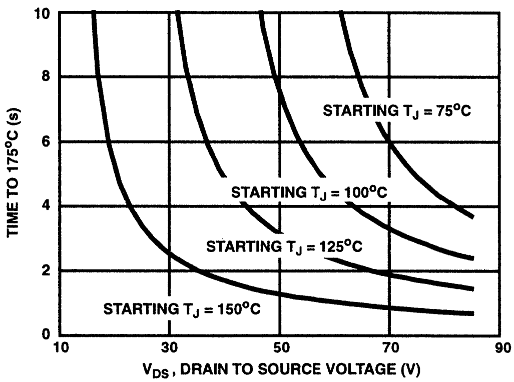


FIGURE 24. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 5°C/W) (HEATSINK THERMAL CAPACITANCE = 2.0J/°C)

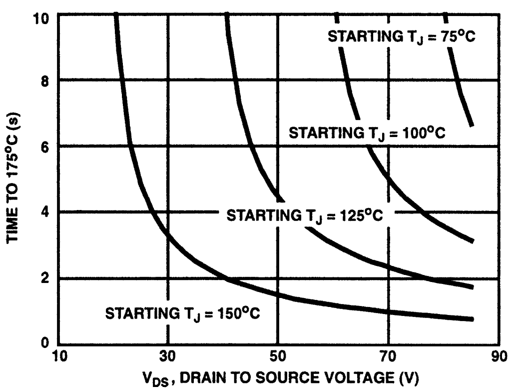


FIGURE 25. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 2°C/W) (HEATSINK THERMAL CAPACITANCE = 4J/°C)

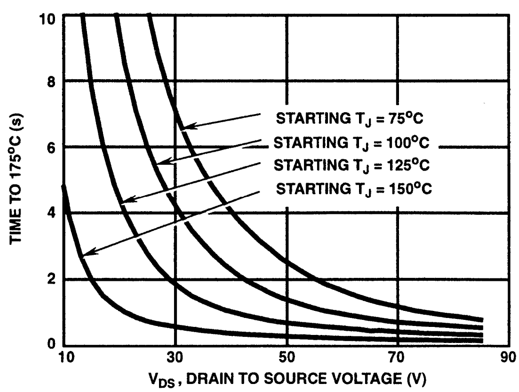


FIGURE 26. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 25°C/W) (HEATSINK THERMAL CAPACITANCE = 0.5J/°C)

Performance Curves (Continued)

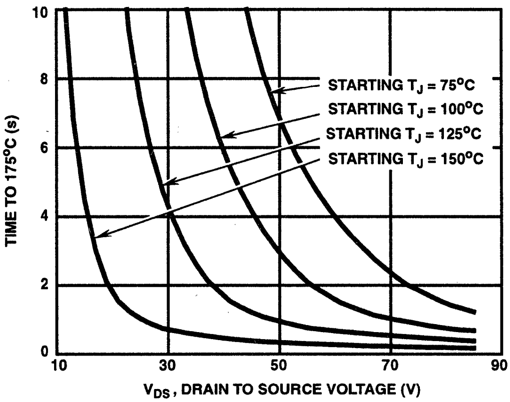


FIGURE 27. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 10°C/W) (HEATSINK THERMAL CAPACITANCE = 1.0J/°C)

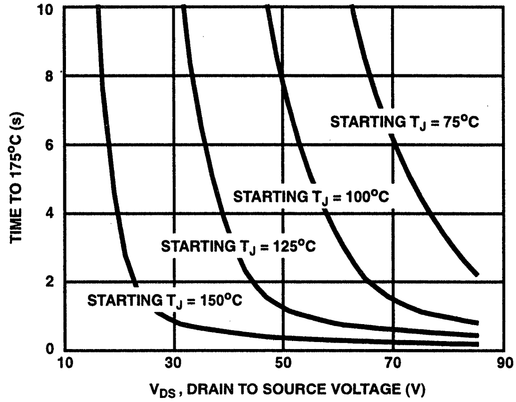


FIGURE 28. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 5°C/W) (HEATSINK THERMAL CAPACITANCE = 2.0J/°C)

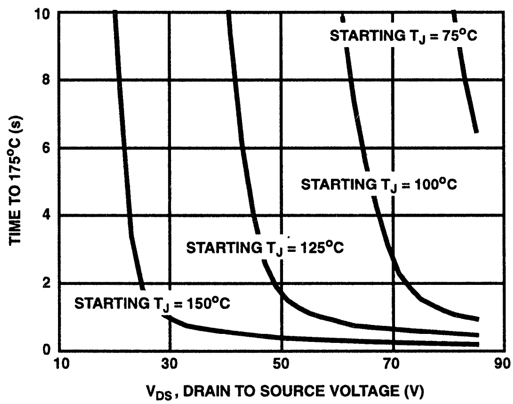
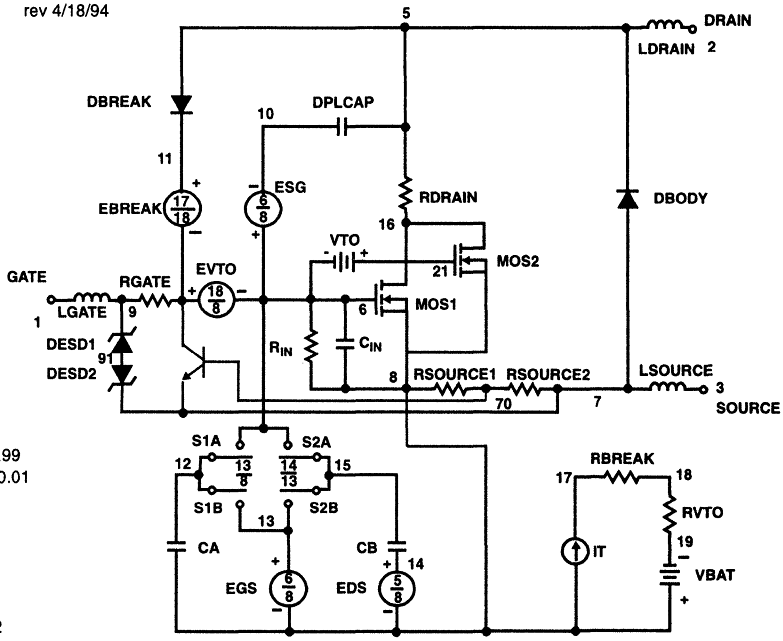


FIGURE 29. TIME TO 175°C IN CURRENT LIMITING (HEATSINK THERMAL RESISTANCE = 2°C/W) (HEATSINK THERMAL CAPACITANCE = 4J/°C)

Temperature Compensated PSPICE Model for the RLD03N06CLE, RLD03N06CLESM, RLP03N06CLE



SUBCKT RLD03N06CLE 2 1 3; rev 4/18/94
CA 12 8 1 0.547e-9
CB 15 14 0.547e-9
CIN 6 8 0 0.301e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DESD1 91 9 DESD1MOD
DESD2 91 7 DESD2MOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 20 17 18 66.5
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 2.96e-9
LSOURCE 3 7 2.96e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

QCONTROL 20 70 7 QMOD 1

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 1.123
RGATE 9 20 3200
RIN 6 8 1e9
RSOURCE1 8 70 RDSMOD 1.12
RSOURCE2 70 7 RSMOD 2.16
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.22

.MODEL DBDMOD D (IS = 7.97e-17 RS = 1.82 TRS1 = 3.91e-3 TRS2 = 1.24e-5 CJO = 3.00e-10 TT = 1.83e-7)
.MODEL DBKMOD D (RS = 3150 TRS1 =0 TRS2 = 0)
.MODEL DESD1MOD D (BV = 13.54 TBV1 = 0 TBV2 = 0 RS = 45.5 TRS1 = 0 TRS2 = 0)
.MODEL DESD2MOD D (BV = 11.46 TBV1 = -7.576e-4 TBV2 = -3.0e-6 RS = 0 TRS1 = 0 TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 74.2e-12 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 1.67 KP = 3.40 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL QMOD NPN (BF =5)
.MODEL RBKMOD RES (TC1 = 4e-4 TC2 = 1.13e-8)
.MODEL RDSMOD RES (TC1 = 6.80e-3 TC2 = 6.5e-6)
.MODEL RSMOD RES (TC1 = 2.95e-3 TC2 = -1e-6)
.MODEL RVTOMOD RES (TC1 = -2.22e-3 TC2 = -1.95e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3 VOFF = -1)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1 VOFF = -3)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.85 VOFF = 2.15)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.15 VOFF = -2.85)

.ENDS

NOTE:

1. For further discussion of the PSPICE model consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records 1991.

POWER MOSFETs 7

SMALL OUTLINE PRODUCTS

HARRIS SEMICONDUCTOR

RF1K49086

3.5A, 30V, Avalanche Rated, Dual N-Channel Enhancement-Mode Power MOSFET

December 1995

Features

- 3.5A, 30V
- $r_{DS(ON)} = 0.060\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RF1K49086 Dual N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low-voltage bus switches. This device can be operated directly from integrated circuits.

PACKAGING AVAILABILITY

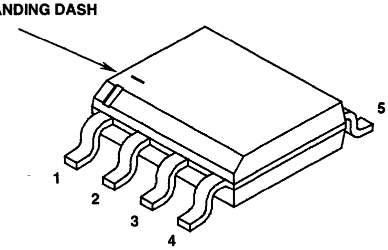
PART NUMBER	PACKAGE	BRAND
RF1K49086	MS-012AA	RF1K49086

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4908696.

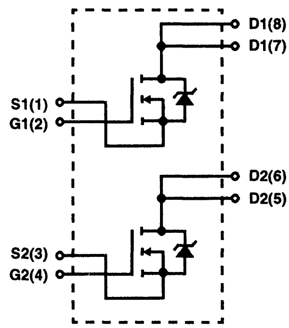
Formerly developmental type TA49086.

Packaging

JEDEC MS-012AA (SOP-8)



Symbol



Absolute Maximum Ratings $T_A = +25^oC$

		RF1K49086	UNITS
Drain-Source Voltage	V_{DSS}	30	V
Drain-Gate Voltage	V_{DGR}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous (Pulse Width = 5s)	I_D	3.5	A
Pulsed	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_A = +25^oC$	P_D	2	W
Derate above $+25^oC$		0.016	W/^{o}C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	^{o}C
Soldering Temperature of Leads for 10s	T_L	260	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications $T_A = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		1	-	3	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30V$, $V_{GS} = 0V$	$T_A = +25^oC$	-	-	1	µA
			$T_A = +150^oC$	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 3.5A$	$V_{GS} = 10V$	-	-	0.060	Ω
			$V_{GS} = 4.5V$	-	-	0.132	Ω
Turn-On Time	t_{ON}	$V_{DD} = 15V$, $I_D = 3.5A$, $R_L = 4.29\Omega$, $V_{GS} = 10V$, $R_{GS} = 25\Omega$		-	-	50	ns
Turn-On Delay Time	$t_{D(ON)}$			-	10	-	ns
Rise Time	t_R			-	30	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	60	-	ns
Fall Time	t_F			-	45	-	ns
Turn-Off Time	t_{OFF}			-	-	130	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $20V$	$V_{DD} = 24V$, $I_D = 3.5A$, $R_L = 6.86\Omega$	-	35	45	nC
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0V$ to $10V$		-	13	17	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $2V$		-	2.3	2.9	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	575	-	pF
Output Capacitance	C_{OSS}			-	275	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	100	-	pF
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	Pulse Width = 1s Device mounted on FR-4 material		-	-	62.5	$^oC/W$

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 3.5A$	-	-	1.25	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 3.5A$, $dI_{SD}/dt = 100A/\mu s$	-	-	45	ns

Typical Performance Curves

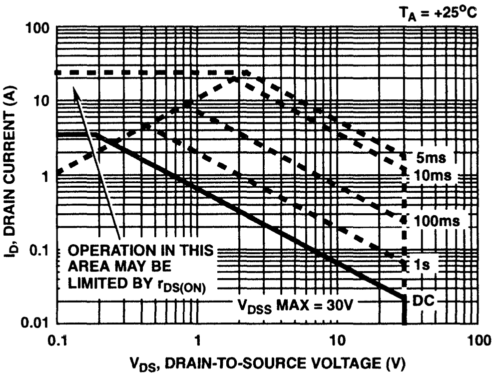


FIGURE 1. SAFE OPERATING AREA CURVE

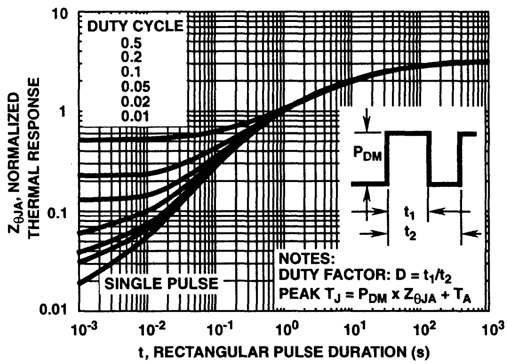


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

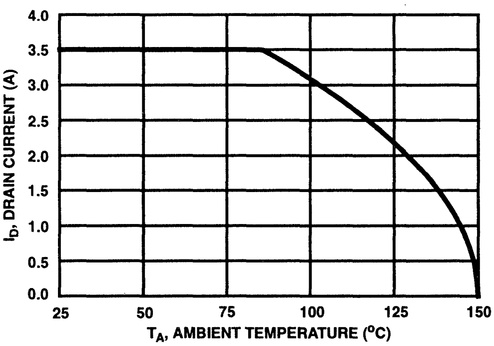


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

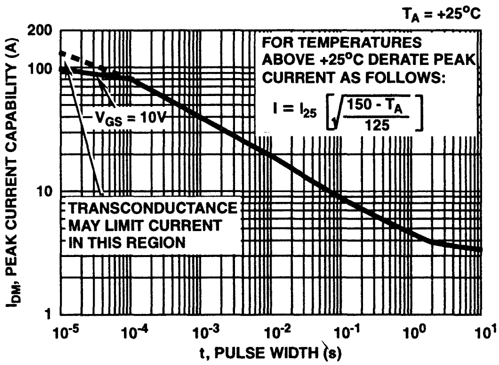


FIGURE 4. PEAK CURRENT CAPABILITY

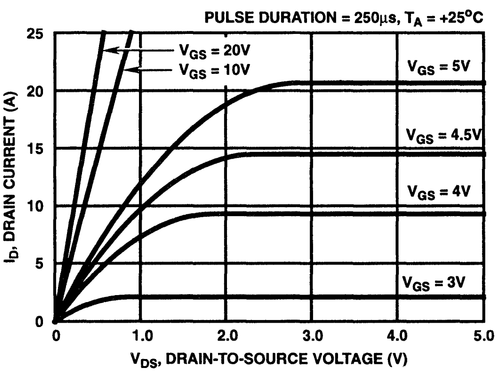


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

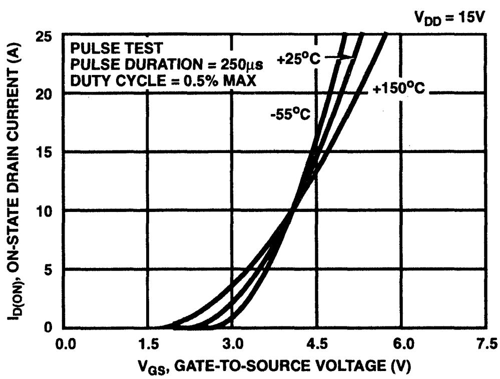


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

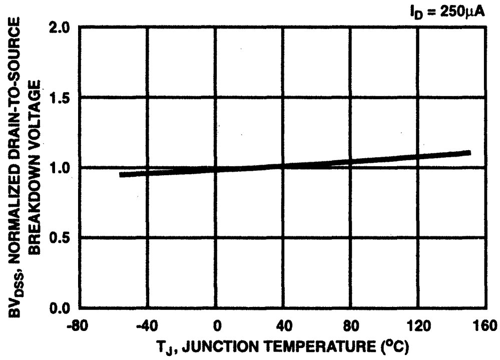


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

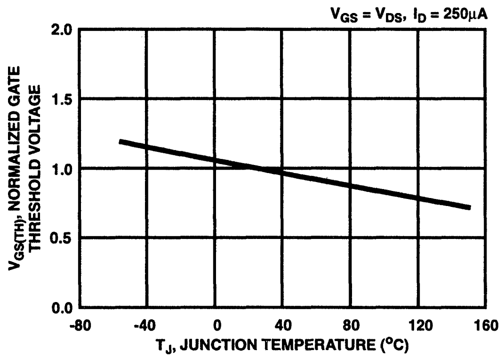


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

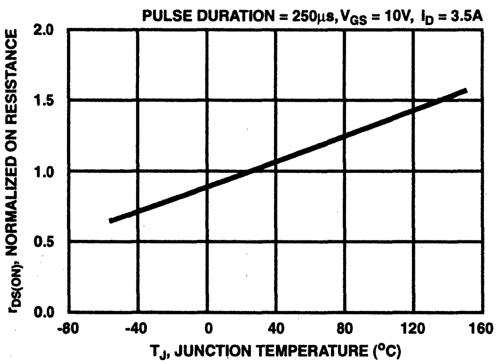


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

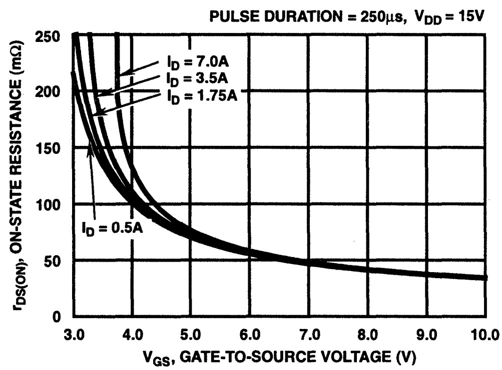


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

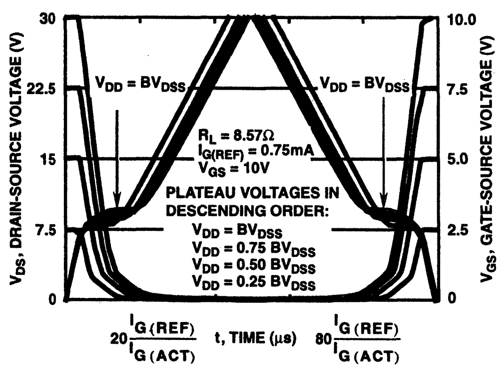


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

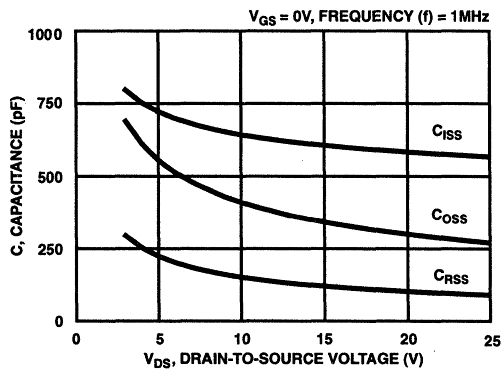


FIGURE 12. TYPICAL CAPACITANCE vs VOLTAGE

Typical Performance Curves (Continued)

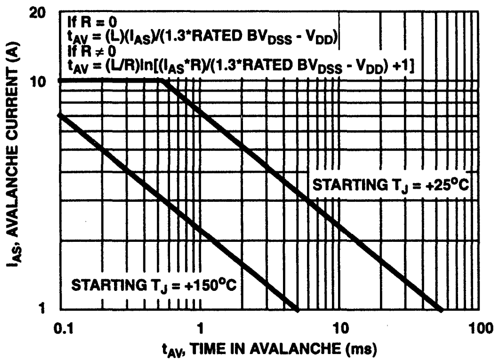


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

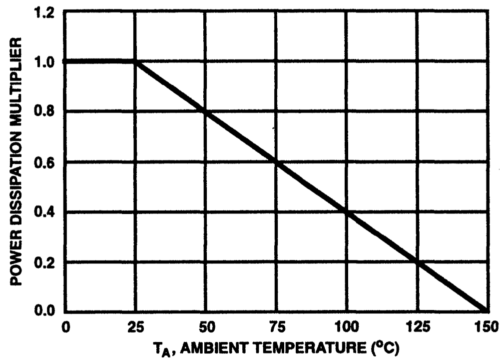


FIGURE 14. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms

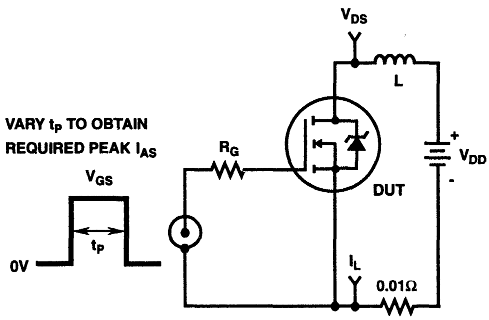


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

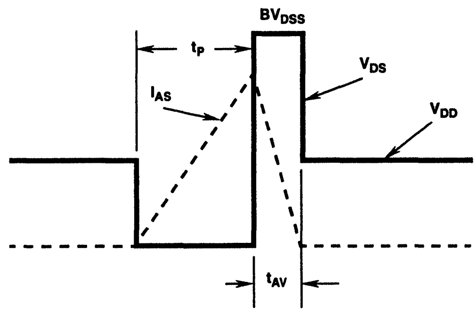


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

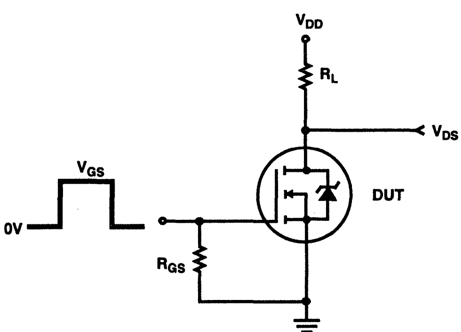


FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

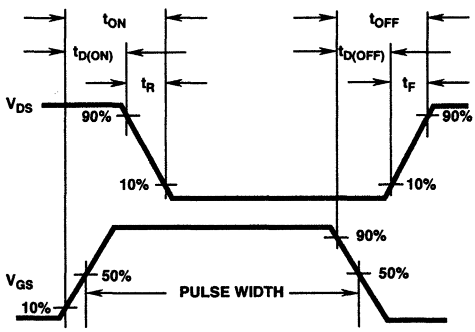
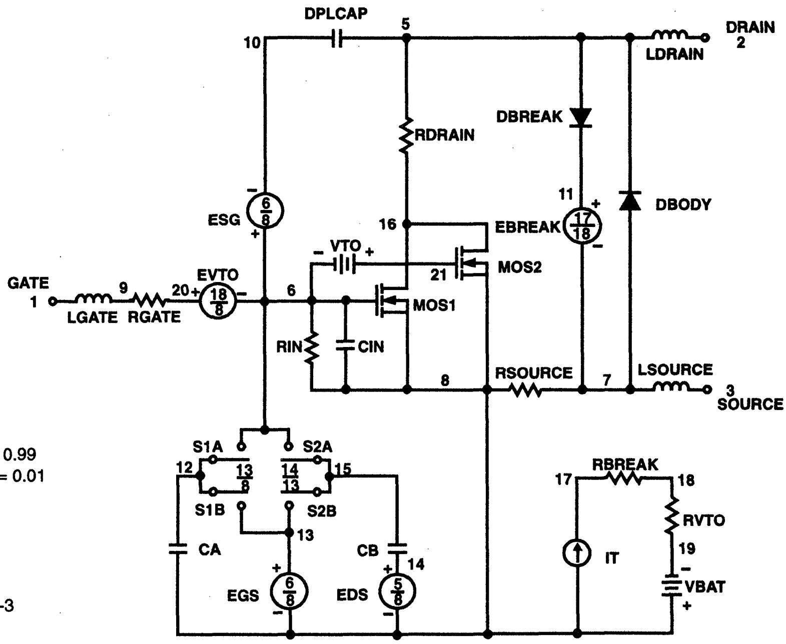


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RF1K49086

SUBCKT RF1K49086 2 1 3 ;   rev 12/15/94

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CA 12 8 1.75e-9
CB 15 14 1.80e-9
CIN 6 8 1.20e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 33.29
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 1.233e-9
LSOURCE 3 7 0.452e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 1e-4
RGATE 9 20 1.83
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 13.5e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.1

.MODEL DBDMOD D (IS = 2.50e-13 RS = 1.35e-2 TRS1 = 4.31e-5 TRS2 = 2.15e-5 CJO = 9.33e-10 TT = 2.08e-8)
.MODEL DBKMOD D (RS = 1.14 TRS1 = 2.23e-3 TRS2 = -8.91e-6)
.MODEL DPLCAPMOD D (CJO = 7.99e-10 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 2.15 KP = 6.25 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 7.74e-4 TC2 = 1.13e-6)
.MODEL RDSMOD RES (TC1 = 4.5e-3 TC2 = -7.45e-7)
.MODEL RVTOMOD RES (TC1 = -4.16e-3 TC2 = 2.16e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -7.15 VOFF= -5.15)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5.15 VOFF= -7.15)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.6 VOFF= 2.4)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.4 VOFF= -2.6)

.ENDS
```

NOTE:

1. For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options;** IEEE Power Electronics Specialist Conference Records, 1991.

Soldering Precautions

The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100°C. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5°C per second when changing from preheating to soldering.
4. The peak temperature in the soldering process should be at least 30°C higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time must not exceed 260°C for 10 seconds on the leads and case of the device.
6. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

HARRIS SEMICONDUCTOR

RF1K49088

3.5A, 30V, Avalanche Rated, Logic Level, Dual N-Channel Enhancement-Mode Power MOSFET

December 1995

Features

- 3.5A, 30V
- $r_{DS(ON)} = 0.060\Omega$
- *Temperature Compensating* PSPICE Model
- On-Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RF1K49088 Dual N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low-voltage bus switches. This product achieves full-rated conduction at a gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

PACKAGING AVAILABILITY

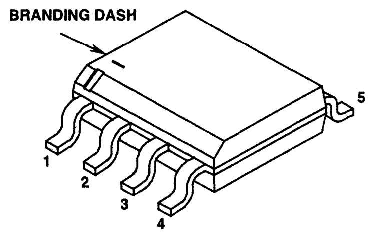
PART NUMBER	PACKAGE	BRAND
RF1K49088	MS-012AA	RF1K49088

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4908896.

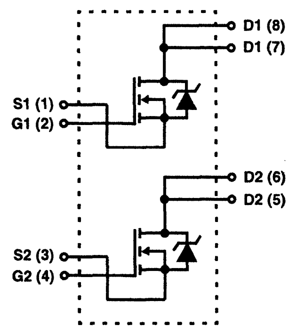
Formerly developmental type TA49088.

Packaging

JEDEC MS-012AA (SOP-8)



Symbol



Absolute Maximum Ratings $T_A = +25^oC$

		RF1K49088	UNITS
Drain-Source Voltage	V_{DSS}	30	V
Drain-Gate Voltage	V_{DGR}	30	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current			
Continuous (Pulse Width ≥ 5s)	I_D	3.5	A
Pulsed	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_A = +25^oC$	P_D	2	W
Derate above $+25^oC$		0.016	W/^{o}C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	^{o}C
Soldering Temperature of Leads for 10s	T_L	260	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

File Number **3952.2**

Electrical Specifications $T_A = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30V$, $V_{GS} = 0V$	$T_A = +25^oC$	-	-	1	µA
			$T_A = +150^oC$	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 10V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 3.5A$, $V_{GS} = 5V$		-	-	0.060	Ω
Turn-On Time	t_{ON}	$V_{DD} = 15V$, $I_D = 3.5A$, $R_L = 4.29\Omega$, $V_{GS} = 5V$, $R_{GS} = 25\Omega$		-	-	100	ns
Turn-On Delay Time	$t_{D(ON)}$			-	18	-	ns
Rise Time	t_R			-	60	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	53	-	ns
Fall Time	t_F			-	47	-	ns
Turn-Off Time	t_{OFF}			-	-	125	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $10V$	$V_{DD} = 24V$, $I_D = 3.5A$, $R_L = 6.86\Omega$	-	24	30	nC
Gate Charge at 5V	$Q_{G(5)}$	$V_{GS} = 0V$ to $5V$		-	13	17	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $1V$		-	0.8	1.0	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	750	-	pF
Output Capacitance	C_{OSS}			-	275	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	100	-	pF
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	Pulse width = 1 second Device mounted on FR-4 material		-	-	62.5	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 3.5A$	-	-	1.25	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 3.5A$, $dI_{SD}/dt = 100A/\mu s$	-	-	50	ns

Typical Performance Curves

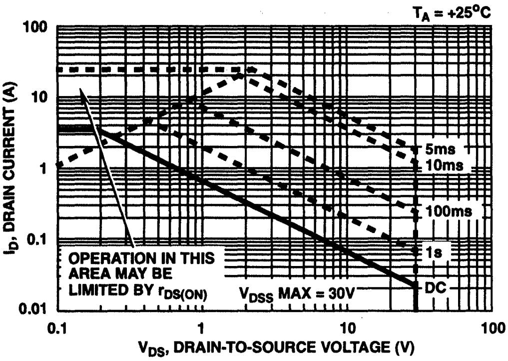


FIGURE 1. SAFE OPERATING AREA CURVE

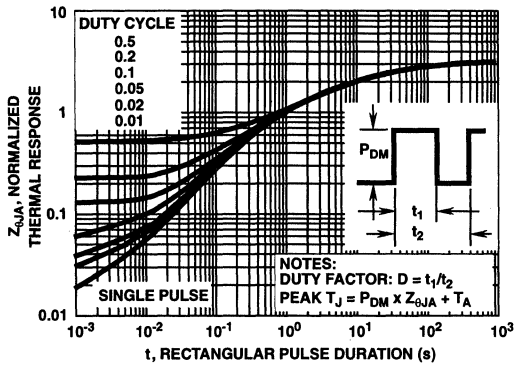


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

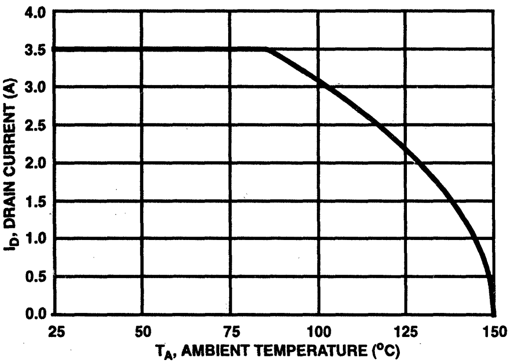


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

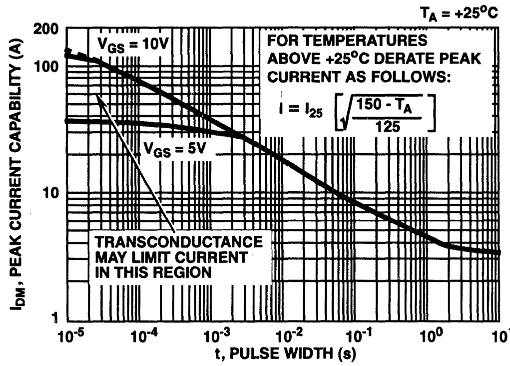


FIGURE 4. PEAK CURRENT CAPABILITY

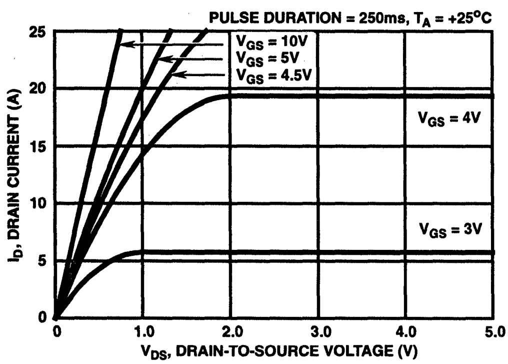


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

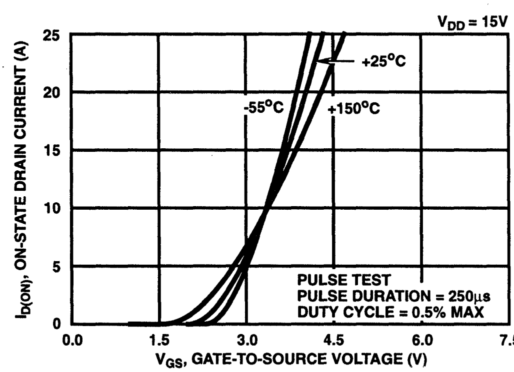


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

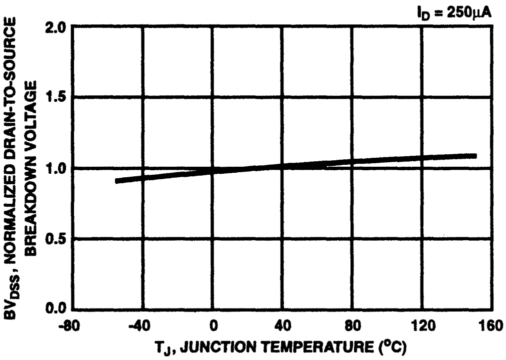


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

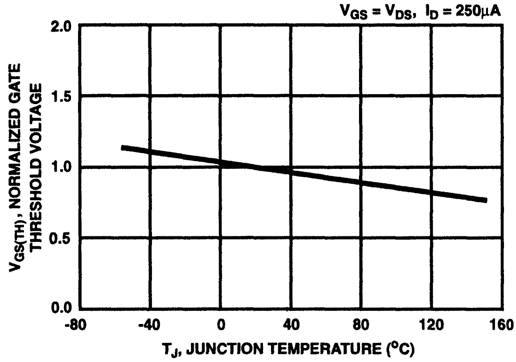


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

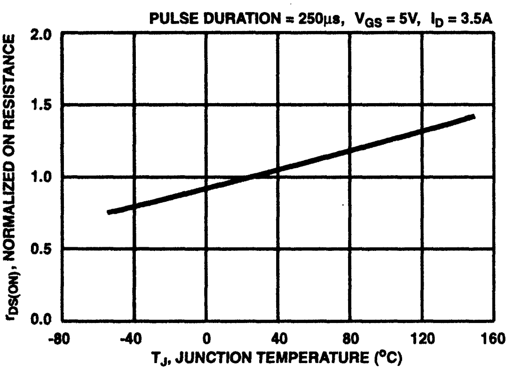


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

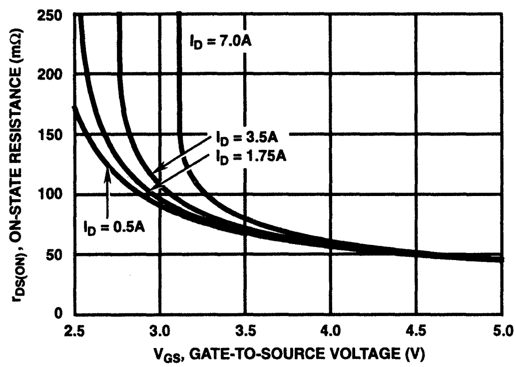


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

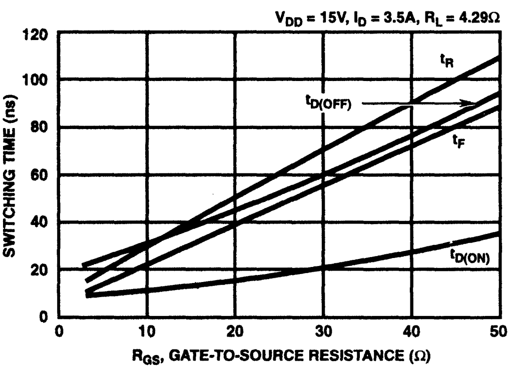


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

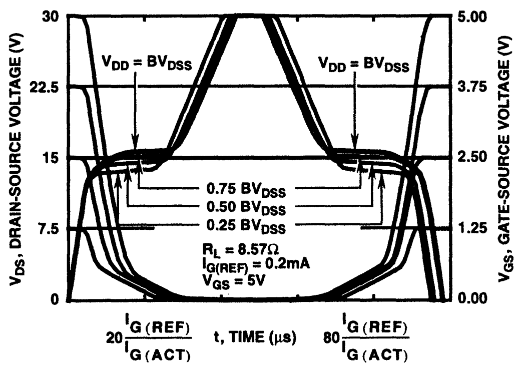


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

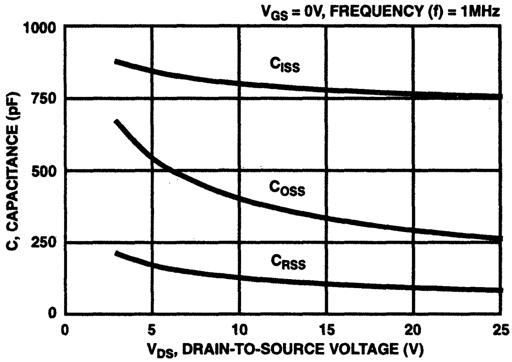


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

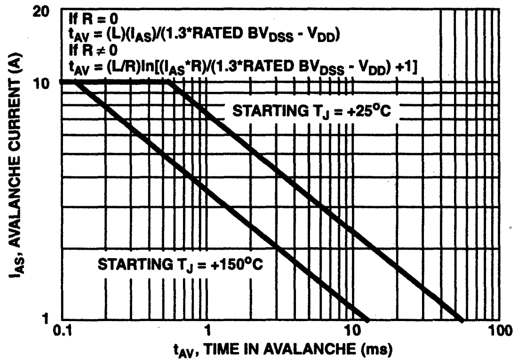


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

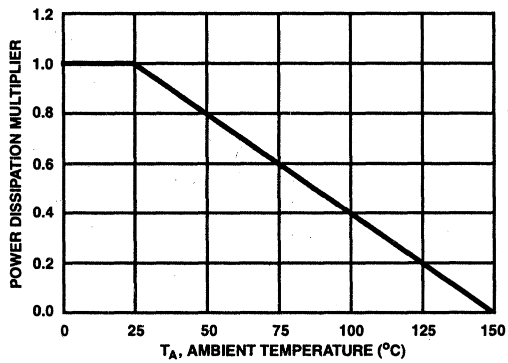


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms

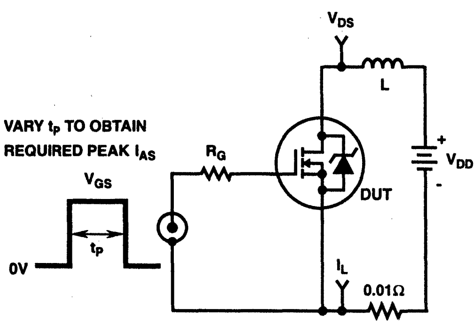


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

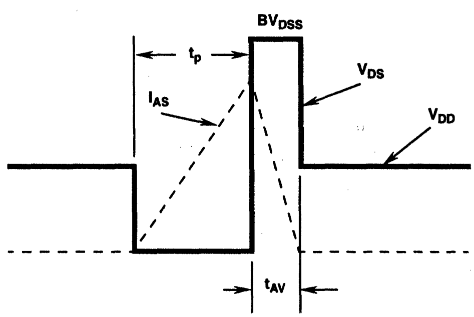


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

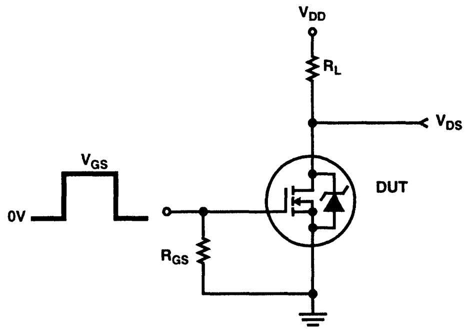


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

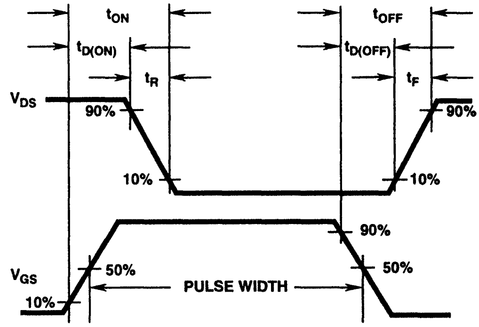


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Soldering Precautions

The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100°C. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5°C per second when changing from preheating to soldering.
4. The peak temperature in the soldering process should be at least 30°C higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time must not exceed 260°C for 10 seconds on the leads and case of the device.
6. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

Temperature Compensated PSPICE Model for the RF1K49088

```
SUBCKT RF1K49088 2 1 3;     rev 7/21/94

CA 12 8 1.081e-9
CB 15 14 1.138e-9
CIN 6 8 0.673e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 34.1
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 1.233e-9
LSOURCE 3 7 0.452e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 1.408e-3
RGATE 9 20 3.33
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 20e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.211
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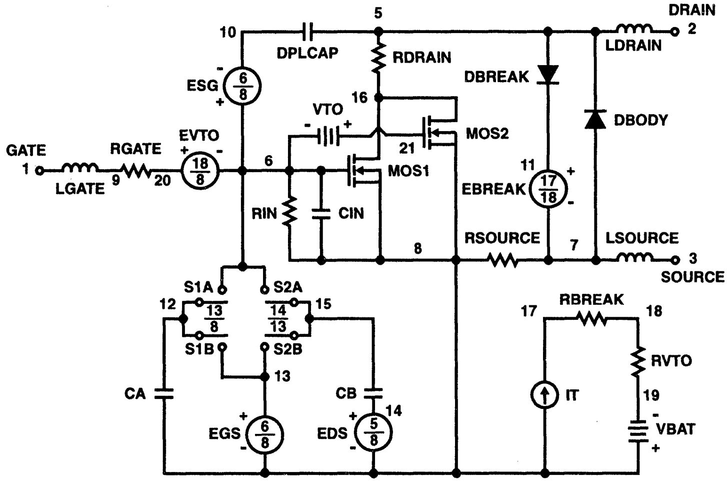


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.MODEL DBDMOD D (IS = 2.82e-13 RS = 1.72e-2 TRS1 = 1.58e-3 TRS2 = 1.23e-7 CJO = 9.19e-10 TT = 2.03e-8)
.MODEL DBKMOD D (RS = 2.65e-1 TRS1 = 5.00e-3 TRS2 = 7.09e-5)
.MODEL DPLCAPMOD D (CJO = 0.42e-9 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 2.01 KP = 15.01 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 1.02e-3 TC2 = -1.98e-6)
.MODEL RDSMOD RES (TC1 = 3.50e-3 TC2 = 3.70e-6)
.MODEL RVTOMOD RES (TC1 = -2.53e-3 TC2 = 8.13e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.2 VOFF= -3.8)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.8 VOFF= -6.2)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.4 VOFF= 4.1)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 4.1 VOFF= -1.4)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.

HARRIS SEMICONDUCTOR

RF1K49090

December 1995

3.5A, 12V, Avalanche Rated, Logic Level, Dual N-Channel Enhancement-Mode Power MOSFET

Features

- 3.5A, 12V
- $r_{DS(ON)} = 0.050\Omega$
- *Temperature Compensating* PSPICE Model
- On-Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RF1K49090 Dual N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low-voltage bus switches. This product achieves full-rated conduction at a gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

PACKAGING AVAILABILITY

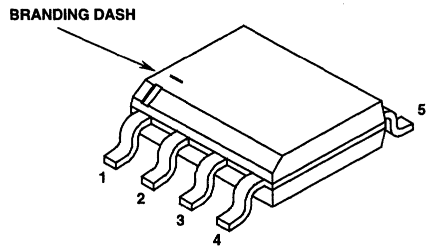
PART NUMBER	PACKAGE	BRAND
RF1K49090	MS-012AA	RF1K49090

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4909096.

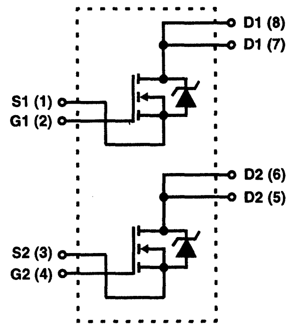
Formerly developmental type TA49090.

Packaging

JEDEC MS-012AA (SOP-8)



Symbol



Absolute Maximum Ratings $T_A = +25^oC$

		RF1K49090	UNITS
Drain-Source Voltage	V_{DSS}	12	V
Drain-Gate Voltage	V_{DGR}	12	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current			
Continuous (Pulse width = 5s)	I_D	3.5	A
Pulsed	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_A = +25^oC$	P_D	2	W
Derate above $+25^oC$		0.016	$W/^oC$
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	^oC
Soldering Temperature of Leads for 10s	T_L	260	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications T_A = +25°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250µA, V_{GS} = 0V		12	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250µA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 12V, V_{GS} = 0V	T_A = +25°C	-	-	1	µA
			T_A = +150°C	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 3.5A, V_{GS} = 5V		-	-	0.050	Ω
Turn-On Time	t_{ON}	V_{DD} = 6V, I_D = 3.5A, R_L = 1.71Ω, V_{GS} = 5V, R_{GS} = 25Ω		-	-	100	ns
Turn-On Delay Time	$t_{D(ON)}$			-	18	-	ns
Rise Time	t_R			-	60	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	50	-	ns
Fall Time	t_F			-	60	-	ns
Turn-Off Time	t_{OFF}			-	-	140	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 9.6V, I_D = 3.5A, R_L = 2.74Ω	-	20	25	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0V to 5V		-	12	15	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to 1V		-	0.9	1.2	nC
Input Capacitance	C_{ISS}	V_{DS} = 10V, V_{GS} = 0V, f = 1MHz		-	750	-	pF
Output Capacitance	C_{OSS}			-	700	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	275	-	pF
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	Pulse width = 1s Device mounted on FR-4 material		-	-	62.5	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 3.5A	-	-	1.25	V
Reverse Recovery Time	t_{RR}	I_{SD} = 3.5A, dI_{SD}/dt = 100A/µs	-	-	60	ns

Typical Performance Curves

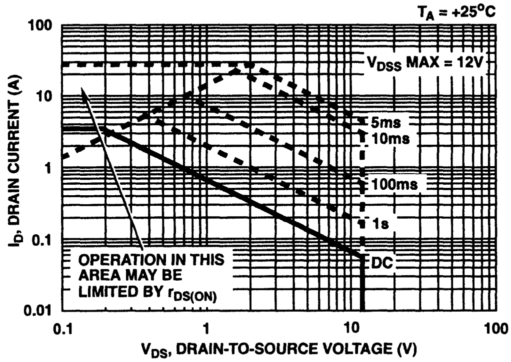


FIGURE 1. SAFE OPERATING AREA CURVE

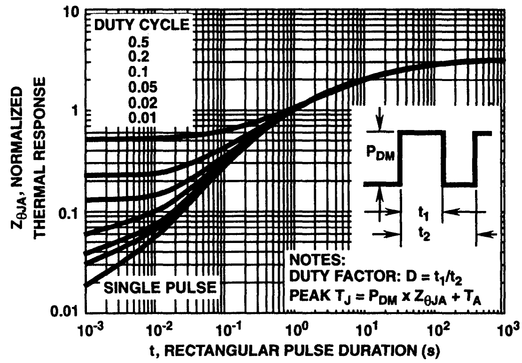


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

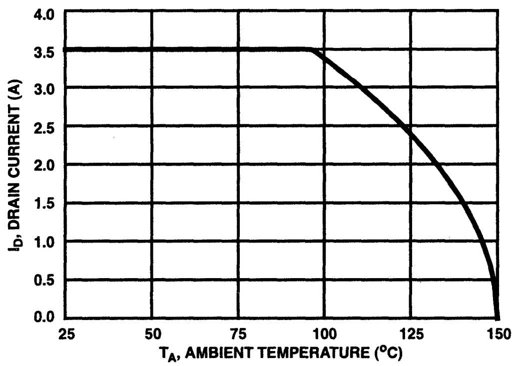


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

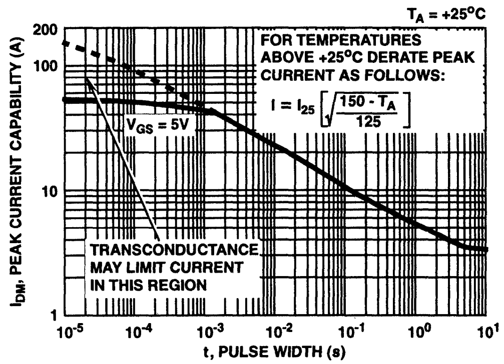


FIGURE 4. PEAK CURRENT CAPABILITY

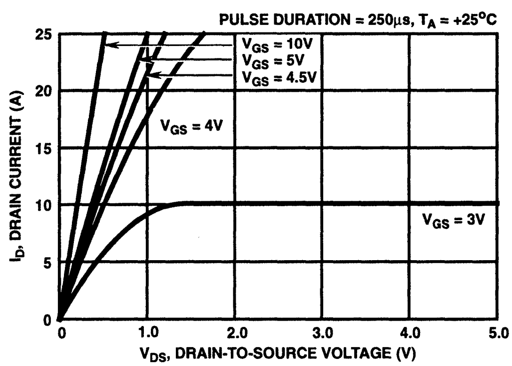


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

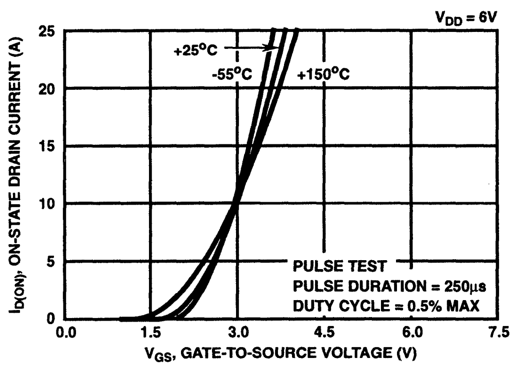


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

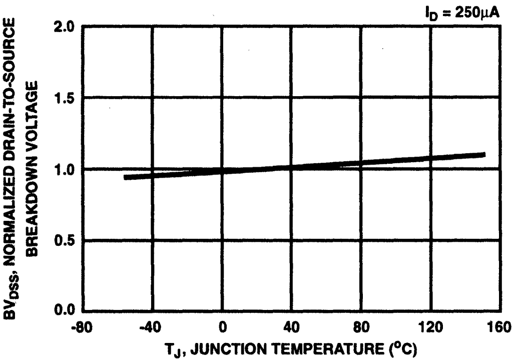


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

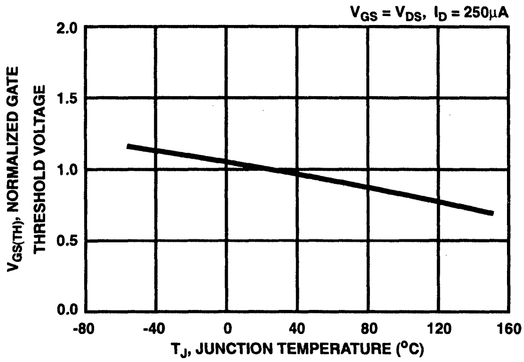


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

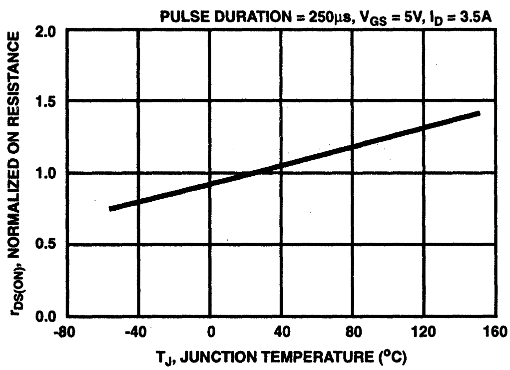


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

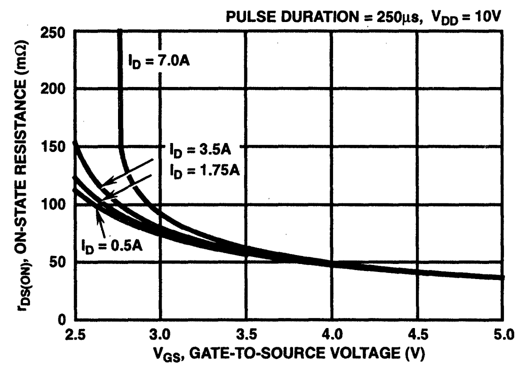


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

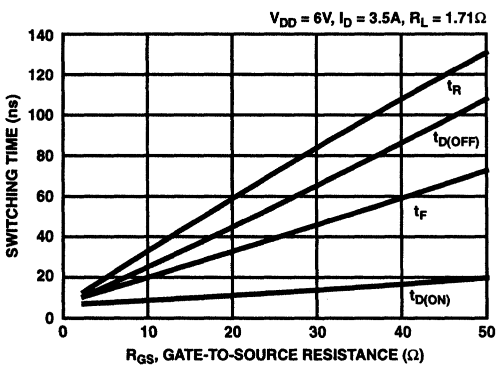


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

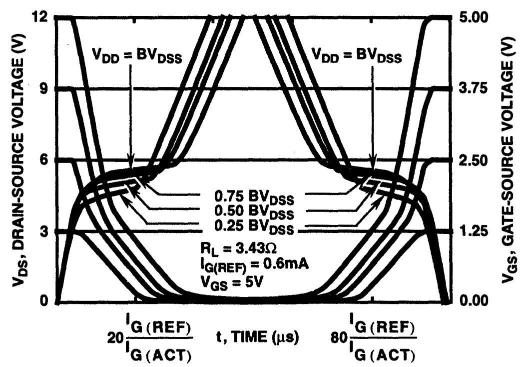


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

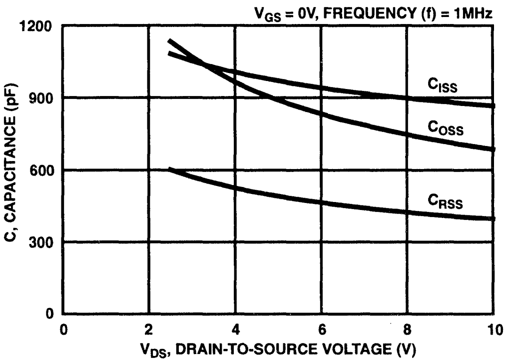


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

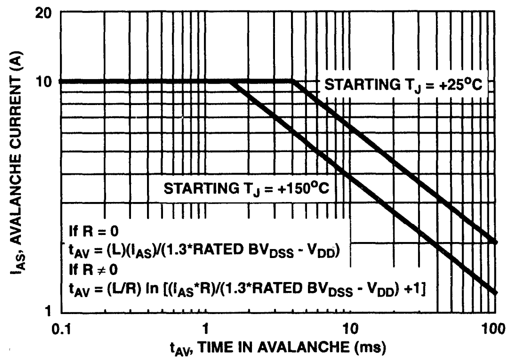


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

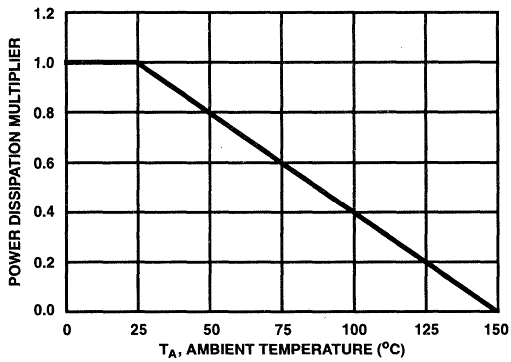


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

7

SMALL OUTLINE PRODUCTS

Test Circuits and Waveforms

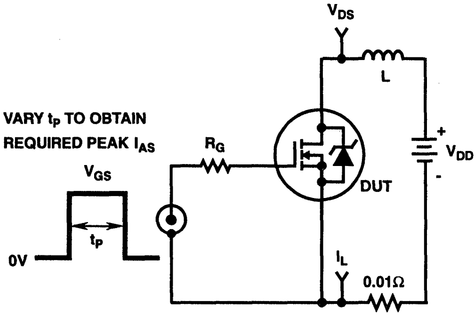


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

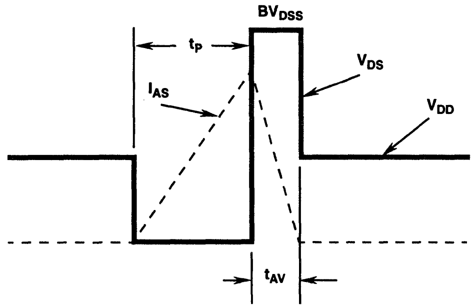


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

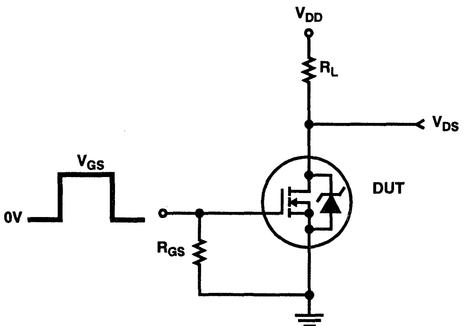


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

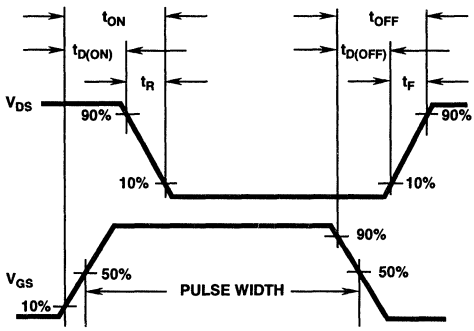


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Soldering Precautions

The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100°C. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5°C per second when changing from preheating to soldering.
4. The peak temperature in the soldering process should be at least 30°C higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time must not exceed 260°C for 10 seconds on the leads and case of the device.
6. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

Temperature Compensated PSPICE Model for the RF1K49090

```
SUBCKT RF1K49090 2 1 3 ;     rev 9/6/94

CA 12 8 9.77e-10
CB 15 14 9.19e-10
CIN 6 8 7.81e-10

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 14.89
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

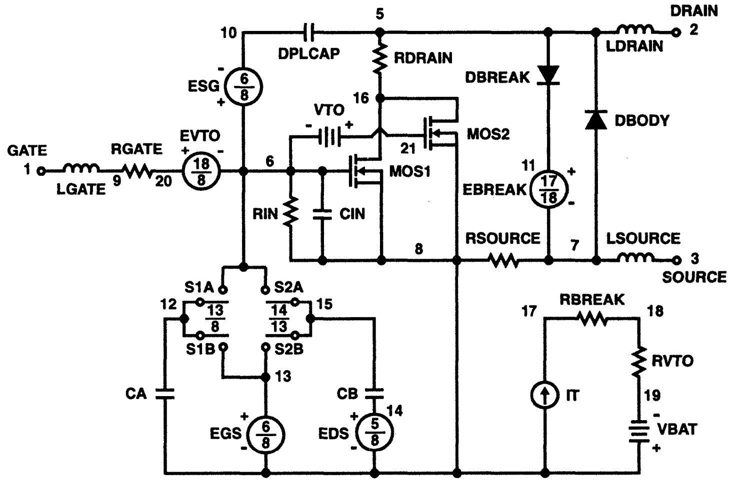
LDRAIN 2 5 1e-9
LGATE 1 9 1.233e-9
LSOURCE 3 7 0.452e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 4.91e-3
RGATE 9 20 2.74
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 5e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.3215
```




```
.MODEL DBDMOD D (IS = 7.00e-13 RS = 2.15e-2 TRS1 = 0.5e-3 TRS2 = 3.68e-6 CJO = 1.28e-9 TT = 1.8e-8)
.MODEL DBKMOD D (RS = 1.28e-1 TRS1 = 1.69e-3 TRS2 = -2.0e-6)
.MODEL DPLCAPMOD D (CJO = 0.84e-9 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 1.63 KP = 11.55 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 9.15e-4 TC2 = 3.13e-7)
.MODEL RDSMOD RES (TC1 = 7.00e-4 TC2 = 5.00e-6)
.MODEL RVTOMOD RES (TC1 = -2.155e-3 TC2 = -2.7e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.05 VOFF= -4.05)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.05 VOFF= -6.05)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.72 VOFF= 4.28)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 4.28 VOFF= -0.72)

.ENDS
```

NOTE:

1. For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.

HARRIS SEMICONDUCTOR

RF1K49092

3.5A/2.5A, 12V, Avalanche Rated, Logic Level, Complementary Enhancement-Mode Power MOSFET

December 1995

Features

- 3.5A, 12V (N-Channel)
  2.5A, 12V (P-Channel)
- $r_{DS(ON)} = 0.050\Omega$ (N-Channel)
  $r_{DS(ON)} = 0.130\Omega$ (P-Channel)
- *Temperature Compensating* PSPICE Model
- On-Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RF1K49092 complementary power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low-voltage bus switches. This product achieves full-rated conduction at a gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

PACKAGING AVAILABILITY

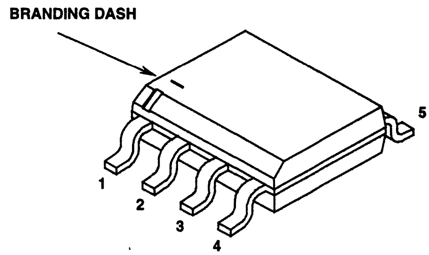
PART NUMBER	PACKAGE	BRAND
RF1K49092	MS-012AA	RF1K49092

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4909296.

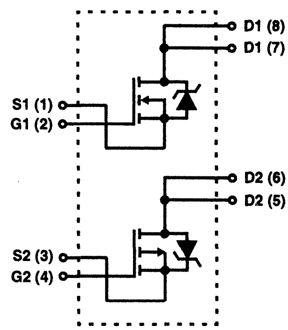
Formerly developmental type TA49092.

Packaging

JEDEC MS-012AA (SOP-8)



Symbol



Absolute Maximum Ratings $T_A = +25^oC$

	RF1K49092 N-CHANNEL	RF1K49092 P-CHANNEL	UNITS
Drain-Source Voltage .... V_{DSS}	12	-12	V
Drain-Gate Voltage .... V_{DGR}	12	-12	V
Gate-Source Voltage .... V_{GS}	±10	±10	V
Drain Current			
Continuous (Pulse Width = 5s).......... I_D	3.5	2.5	A
Pulsed .... I_{DM}	Refer to Peak Current Curve	Refer to Peak Current Curve	
Pulsed Avalanche Rating.......... E_{AS}	Refer to UIS Curve	Refer to UIS Curve	
Power Dissipation			
$T_A = +25^oC$.......... P_D	2	2	W
Derate above $+25^oC$	0.016	0.016	W/^{o}C
Operating and Storage Temperature.......... T_{STG}, T_J	-55 to +150	-55 to +150	^{o}C
Soldering Temperature of Leads for 10s .... T_L	260	260	^{o}C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

File Number **3968.2**

N-Channel Electrical Specifications $T_A = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		12	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 12V$, $V_{GS} = 0V$	$T_A = +25^oC$	-	-	1	μA
			$T_A = +150^oC$	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 10V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 3.5A$, $V_{GS} = 5V$		-	-	0.050	Ω
Turn-On Time	t_{ON}	$V_{DD} = 6V$, $I_D = 3.5A$, $R_L = 1.71\Omega$, $V_{GS} = 5V$, $R_{GS} = 25\Omega$		-	-	100	ns
Turn-On Delay Time	$t_{D(ON)}$			-	18	-	ns
Rise Time	t_R			-	60	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	50	-	ns
Fall Time	t_F			-	60	-	ns
Turn-Off Time	t_{OFF}			-	-	140	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $10V$	$V_{DD} = 9.6V$, $I_D = 3.5A$, $R_L = 2.74\Omega$	-	20	25	nC
Gate Charge at 5V	$Q_{G(5)}$	$V_{GS} = 0V$ to $5V$		-	12	15	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $1V$		-	0.9	1.2	nC
Input Capacitance	C_{ISS}	$V_{DS} = 10V$, $V_{GS} = 0V$, f = 1MHz		-	750	-	pF
Output Capacitance	C_{OSS}			-	700	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	275	-	pF
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	Pulse width = 1s Device mounted on FR-4 material		-	-	62.5	$^oC/W$

N-Channel Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 3.5A$	-	-	1.25	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 3.5A$, $dI_{SD}/dt = 100A/\mu s$	-	-	70	ns

P-Channel Electrical Specifications $T_A = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		-12	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		-1	-	-2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12V$, $V_{GS} = 0V$	$T_A = +25^oC$	-	-	-1	μA
			$T_A = +150^oC$	-	-	-50	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 10V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 2.5A$, $V_{GS} = -5V$		-	-	0.130	Ω
Turn-On Time	t_{ON}	$V_{DD} = -6V$, $I_D = 2.5A$, $R_L = 2.40\Omega$, $V_{GS} = -5V$, $R_{GS} = 25\Omega$		-	-	115	ns
Turn-On Delay Time	$t_{D(ON)}$			-	25	-	ns
Rise Time	t_R			-	65	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	40	-	ns
Fall Time	t_F			-	45	-	ns
Turn-Off Time	t_{OFF}			-	-	110	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $-10V$	$V_{DD} = -9.6V$, $I_D = 2.5A$, $R_L = 3.84\Omega$	-	19	24	nC
Gate Charge at -5V	$Q_{G(-5)}$	$V_{GS} = 0V$ to $-5V$		-	10	14	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $-1V$		-	0.8	1.1	nC
Input Capacitance	C_{ISS}	$V_{DS} = -10V$, $V_{GS} = 0V$, f = 1MHz		-	775	-	pF
Output Capacitance	C_{OSS}			-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	150	-	pF
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	Pulse width = 1s Device mounted on FR-4 material		-	-	62.5	$^oC/W$

P-Channel Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = -2.5A$	-	-	-1.25	V
Reverse Recovery Time	t_{RR}	$I_{SD} = -2.5A$, $dI_{SD}/dt = -100A/\mu s$	-	-	55	ns

Typical Performance Curves (N-Channel)

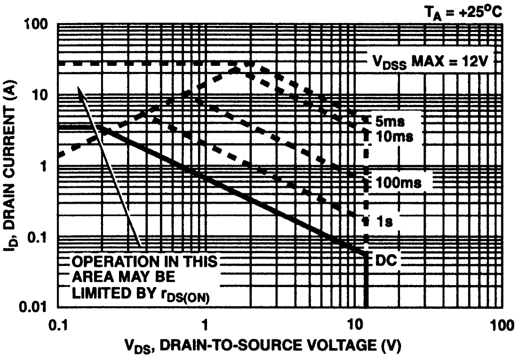


FIGURE 1. SAFE OPERATING AREA CURVE

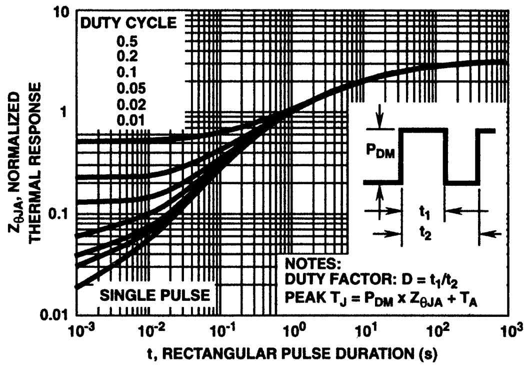


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

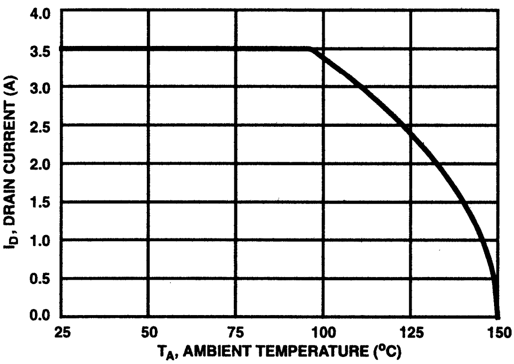


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

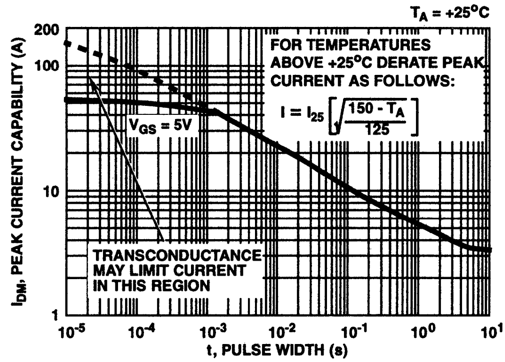


FIGURE 4. PEAK CURRENT CAPABILITY

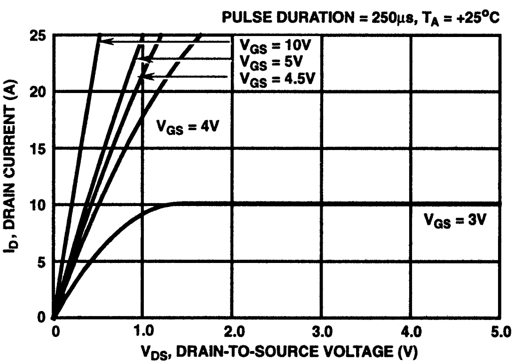


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

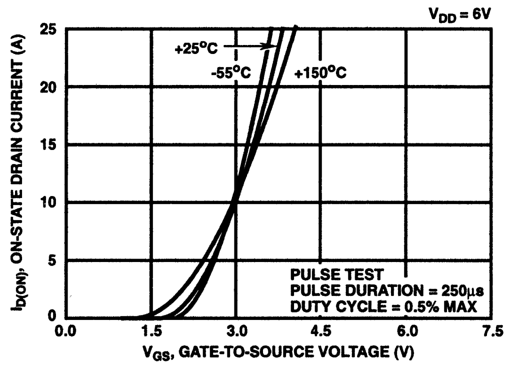


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (N-Channel) (Continued)

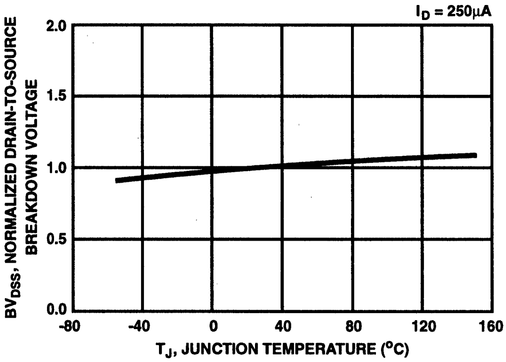


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

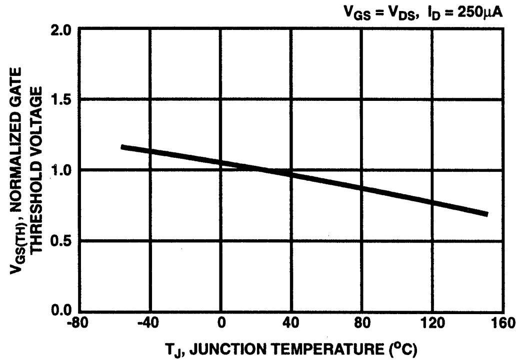


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

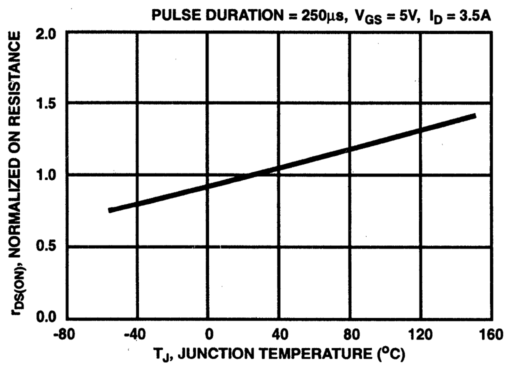


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

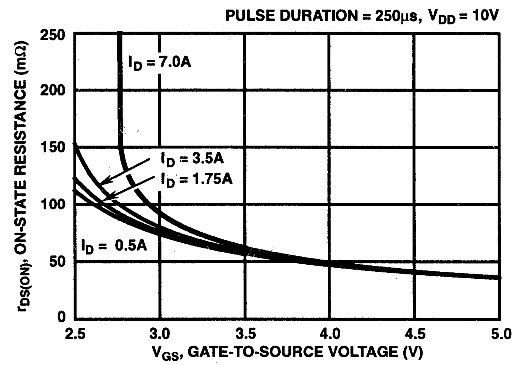


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

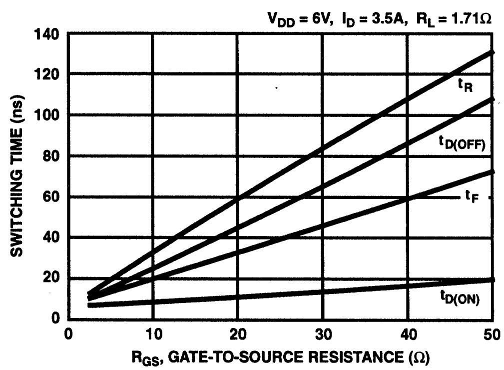


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

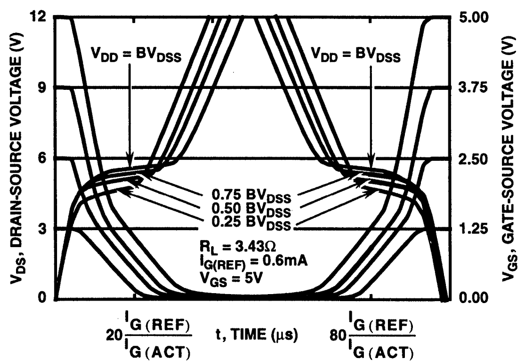


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (N-Channel) (Continued)

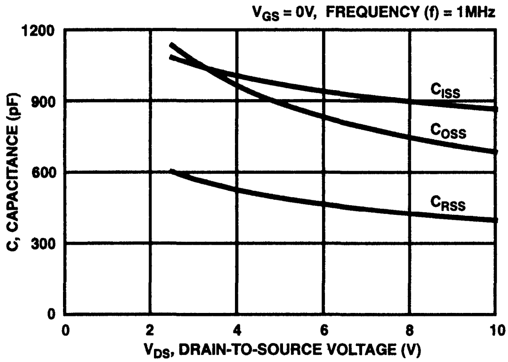


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

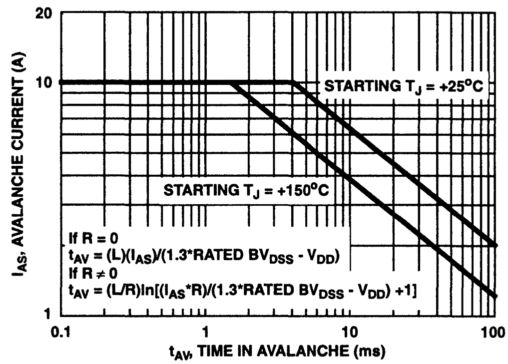


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

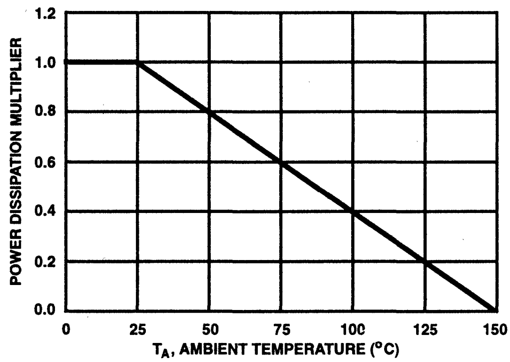


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms (N-Channel)

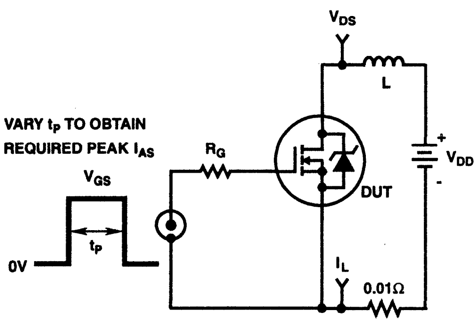


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

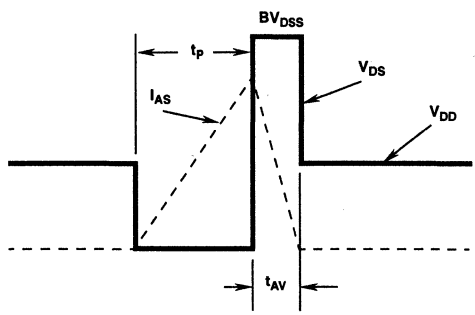


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (N-Channel) (Continued)

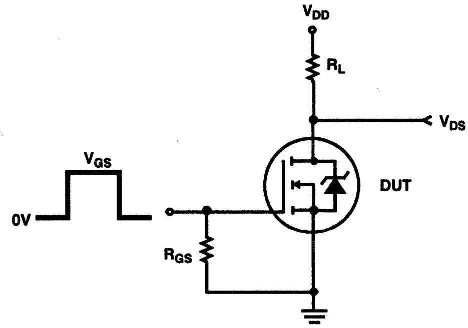


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

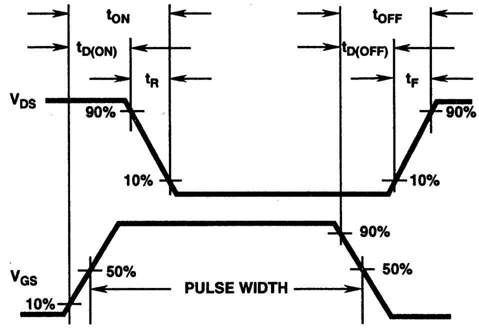


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Typical Performance Curves (P-Channel)

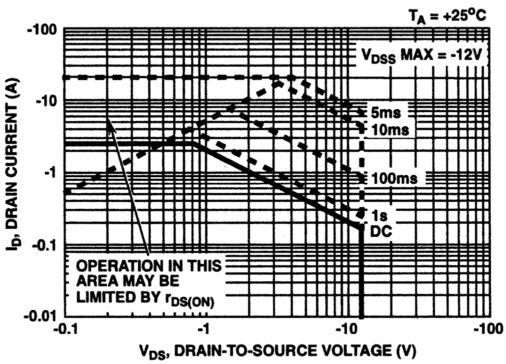


FIGURE 20. SAFE OPERATING AREA CURVE

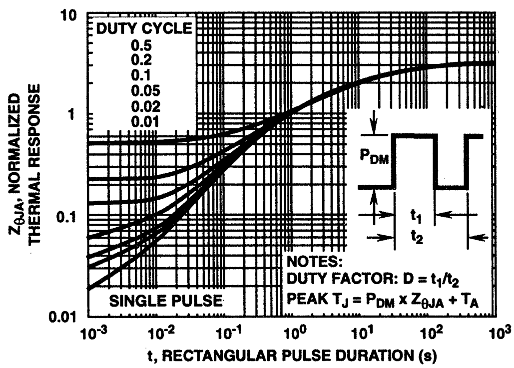


FIGURE 21. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

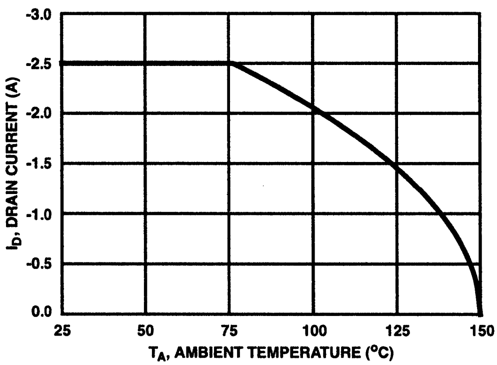


FIGURE 22. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

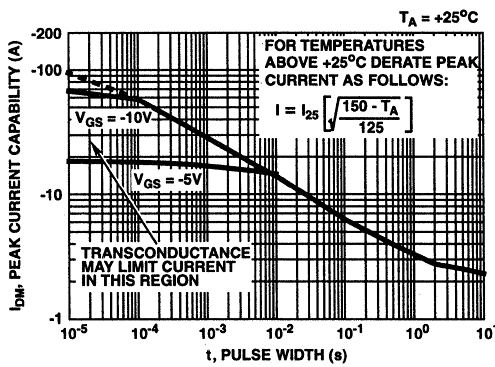


FIGURE 23. PEAK CURRENT CAPABILITY

Typical Performance Curves (P-Channel) (Continued)

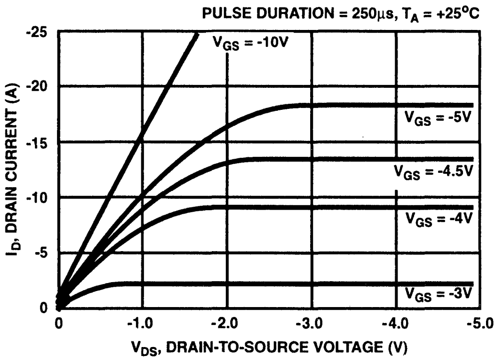


FIGURE 24. TYPICAL SATURATION CHARACTERISTICS

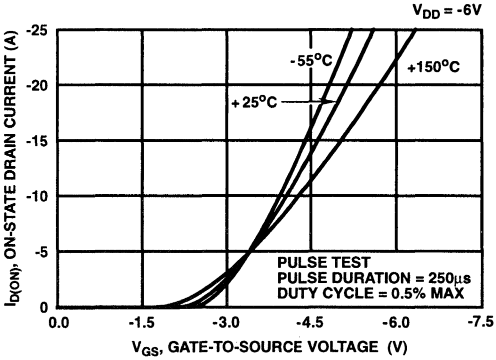


FIGURE 25. TYPICAL TRANSFER CHARACTERISTICS

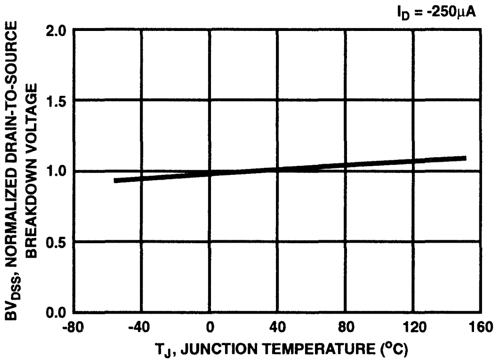


FIGURE 26. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

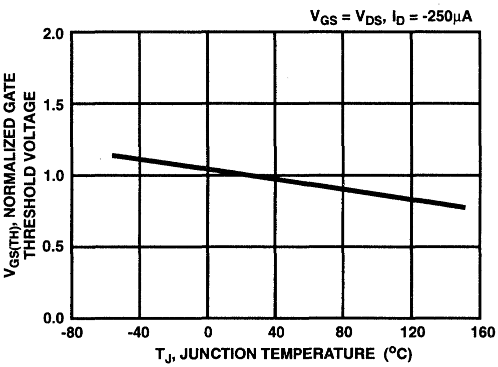


FIGURE 27. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

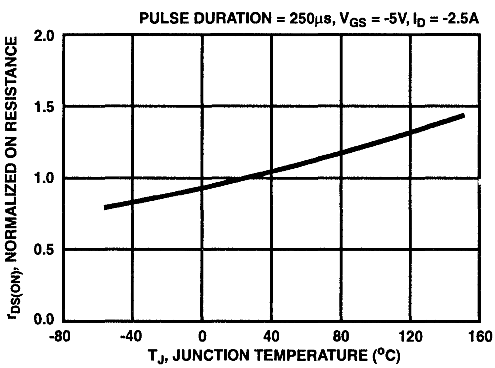


FIGURE 28. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

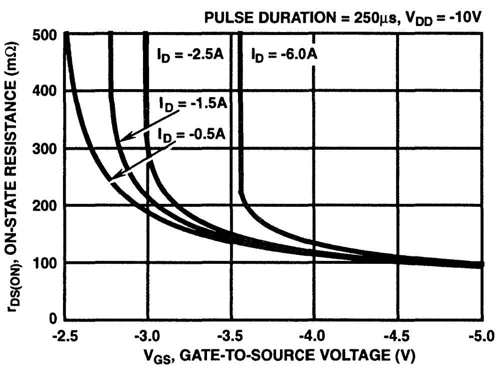


FIGURE 29. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

Typical Performance Curves (P-Channel) (Continued)

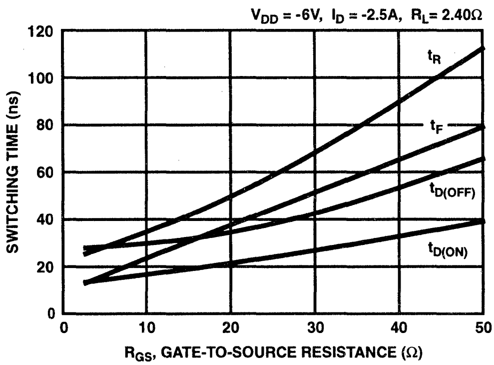


FIGURE 30. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

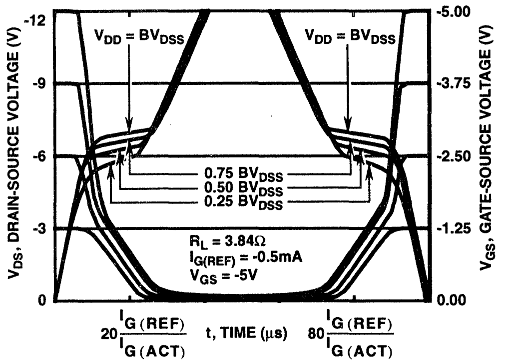


FIGURE 31. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

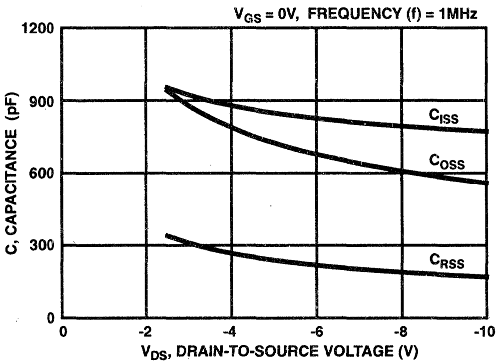


FIGURE 32. TYPICAL CAPACITANCE vs VOLTAGE

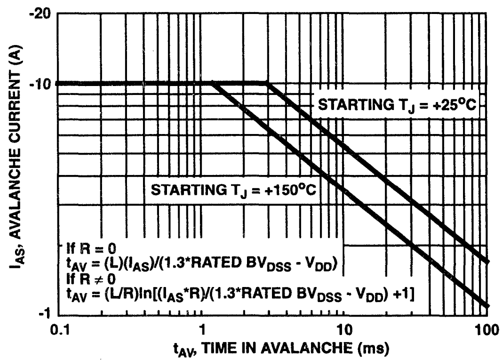


FIGURE 33. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

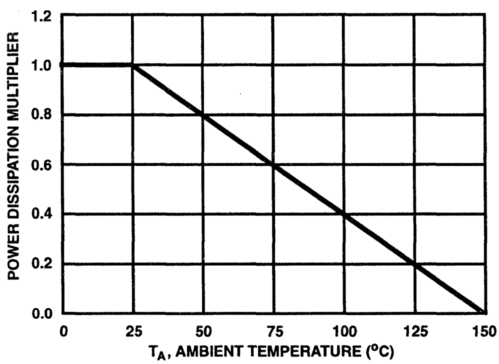


FIGURE 34. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms (P-Channel)

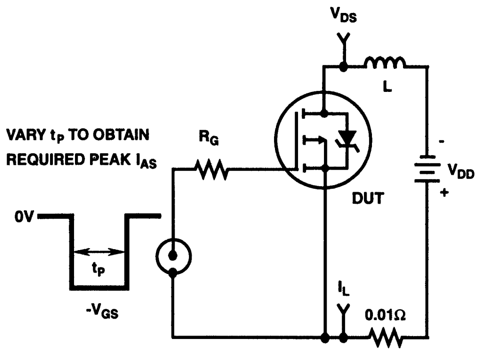


FIGURE 35. UNCLAMPED ENERGY TEST CIRCUIT

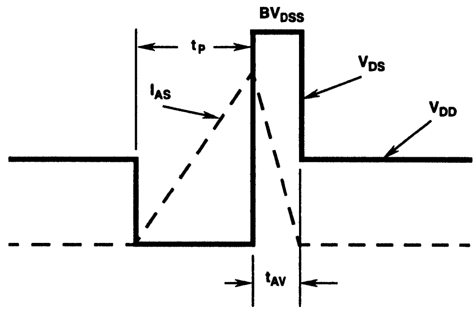


FIGURE 36. UNCLAMPED ENERGY WAVEFORMS

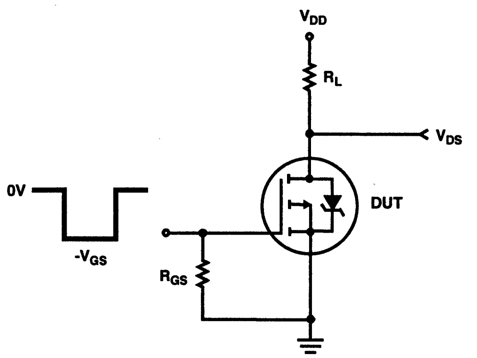


FIGURE 37. RESISTIVE SWITCHING TEST CIRCUIT

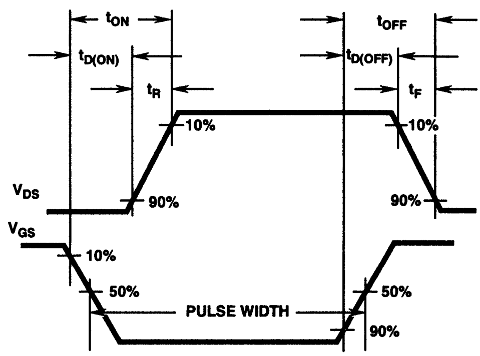


FIGURE 38. RESISTIVE SWITCHING WAVEFORMS

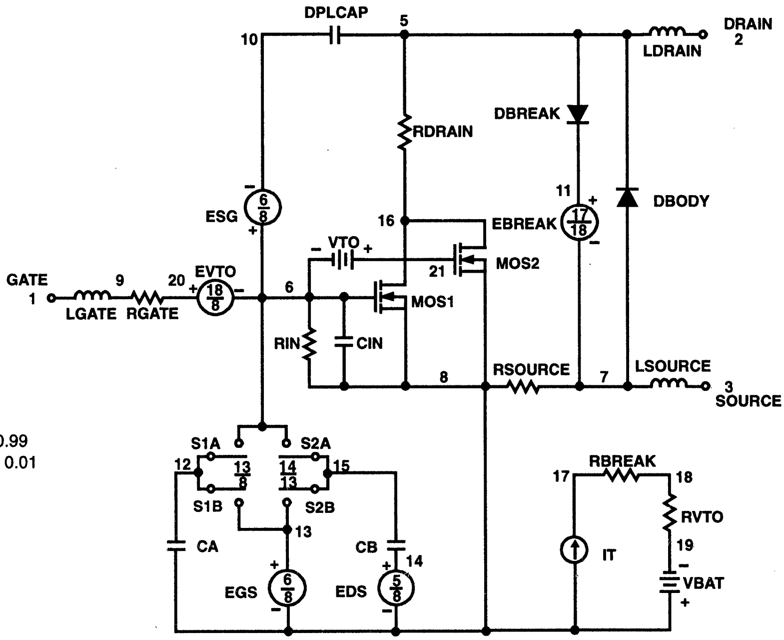
Soldering Precautions

The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100°C. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5°C per second when changing from preheating to soldering.
4. The peak temperature in the soldering process should be at least 30°C higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time must not exceed 260°C for 10 seconds on the leads and case of the device.
6. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

Temperature Compensated PSPICE Model for the N-Channel RF1K49092

SUBCKT RF1K49092 2 1 3; N-Channel Model rev 9/6/94



CA 12 8 9.77e-10
CB 15 14 9.19e-10
CIN 6 8 7.81e-10

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 14.89
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 1.233e-9
LSOURCE 3 7 0.452e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 4.91e-3
RGATE 9 20 2.74
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 5e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.3215

.MODEL DBDMOD D (IS = 7.00e-13 RS = 2.15e-2 TRS1 = 0.5e-3 TRS2 = 3.68e-6 CJO = 1.28e-9 TT = 1.8e-8)
.MODEL DBKMOD D (RS = 1.28e-1 TRS1 = 1.69e-3 TRS2 = -2.0e-6)
.MODEL DPLCAPMOD D (CJO = 0.84e-9 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 1.63 KP = 11.55 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 9.15e-4 TC2 = 3.13e-7)
.MODEL RDSMOD RES (TC1 = 7.00e-4 TC2 = 5.00e-6)
.MODEL RVTOMOD RES (TC1 = -2.155e-3 TC2 = -2.7e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.05 VOFF= -4.05)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.05 VOFF= -6.05)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.72 VOFF= 4.28)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 4.28 VOFF= -0.72)

.ENDS

NOTE:

1. For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.

Temperature Compensated PSPICE Model for the P-Channel RF1K49092

```
SUBCKT RF1K49092 2 1 3 ; P-Channel Model rev 10/24/94

CA 12 8 8.75e-10
CB 15 14 8.65e-10
CIN 6 8 7.65e-10

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 5 11 17 18 -23.75
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 1.233e-9
LSOURCE 3 7 0.452e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

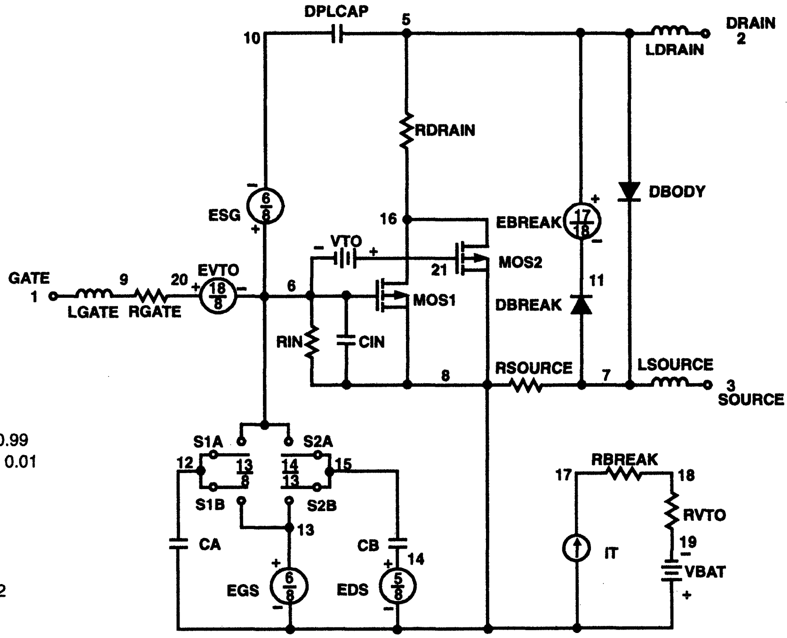
RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 7.36e-3
RGATE 9 20 6.1
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 4.56e-2
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 -0.558

.MODEL DBDMOD D (IS = 3.0e-13 RS = 4.4e-2 TRS1 = 1.0e-3 TRS2 = -7.37e-6 CJO = 1.27e-9 TT = 2.2e-8)
.MODEL DBKMOD D (RS = 7.84e-2 TRS1 = -4.27e-3 TRS2 = 5.77e-5)
.MODEL DPLCAPMOD D (CJO = 2.85e-10 IS = 1e-30 N = 10)
.MODEL MOSMOD PMOS (VTO = -2.1423 KP = 9.206 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 9.61e-4 TC2 = -1.09e-6)
.MODEL RDSMOD RES (TC1 = 2.10e-3 TC2 = 6.99e-6)
.MODEL RVTOMOD RES (TC1 = -1.82e-3 TC2 = 1.47e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 5.47 VOFF= 3.47)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 3.47 VOFF= 5.47)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.05 VOFF= -3.95)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.95 VOFF= 1.05)

.ENDS
```



NOTE:

1. For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991.

HARRIS SEMICONDUCTOR

RF1K49093

2.5A, 12V, Avalanche Rated, Logic Level, Dual P-Channel Enhancement-Mode Power MOSFET

December 1995

Features

- 2.5A, 12V
- $r_{DS(ON)} = 0.130\Omega$
- *Temperature Compensating* PSPICE Model
- On-Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RF1K49093 Dual P-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It is designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low-voltage bus switches. This product achieves full-rated conduction at a gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

PACKAGE AVAILABILITY

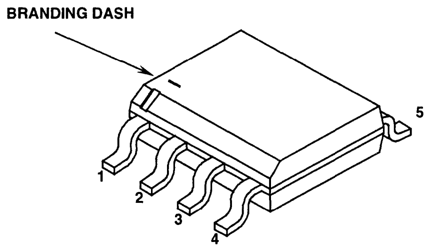
PART NUMBER	PACKAGE	BRAND
RF1K49093	MS-012AA	RF1K49093

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4909396.

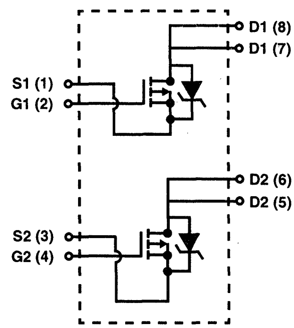
Formerly developmental type TA49093.

Packaging

JEDEC MS-012AA (SOP-8)



Symbol



Absolute Maximum Ratings $T_A = +25^oC$

		RF1K49093	UNITS
Drain-Source Voltage	V_{DSS}	-12	V
Drain-Gate Voltage	V_{DGR}	-12	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current			
Continuous (Pulse width = 5s)	I_D	2.5	A
Pulsed	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_A = +25^oC$	P_D	2	W
Derate above +25°C		0.016	W/°C
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	°C
Soldering Temperature of Leads for 10s	T_L	260	°C

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD handling procedures.

File Number 3969.2

Electrical Specifications $T_A = +25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		-12	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		-1	-	-2	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12V$, $V_{GS} = 0V$	$T_A = +25^oC$	-	-	-1	µA
			$T_A = +150^oC$	-	-	-50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm10V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 2.5A$, $V_{GS} = -5V$		-	-	0.130	Ω
Turn-On Time	t_{ON}	$V_{DD} = -6V$, $I_D = 2.5A$, $R_L = 2.40\Omega$, $V_{GS} = -5V$, $R_{GS} = 25\Omega$		-	-	115	ns
Turn-On Delay Time	$t_{D(ON)}$			-	25	-	ns
Rise Time	t_R			-	65	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	40	-	ns
Fall Time	t_F			-	45	-	ns
Turn-Off Time	t_{OFF}			-	-	110	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $-10V$	$V_{DD} = -9.6V$, $I_D = 2.5A$, $R_L = 3.84\Omega$	-	19	24	nC
Gate Charge at -5V	$Q_{G(-5)}$	$V_{GS} = 0V$ to $-5V$		-	10	14	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $-1V$		-	0.8	1.1	nC
Input Capacitance	C_{ISS}	$V_{DS} = -10V$, $V_{GS} = 0V$, f = 1MHz		-	775	-	pF
Output Capacitance	C_{OSS}			-	550	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	150	-	pF
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	Pulse width = 1 second Device mounted on FR-4 material		-	-	62.5	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = -2.5A$	-	-	-1.25	V
Reverse Recovery Time	t_{RR}	$I_{SD} = -2.5A$, $dI_{SD}/dt = -100A/\mu s$	-	-	55	ns

Typical Performance Curves

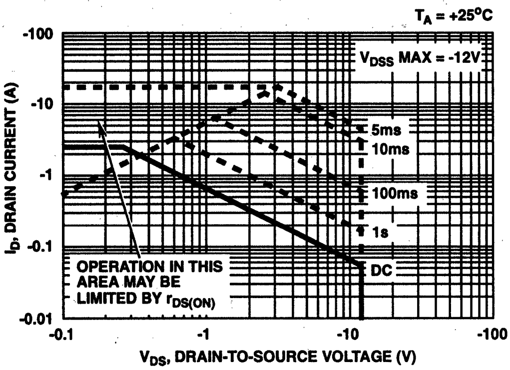


FIGURE 1. SAFE OPERATING AREA CURVE

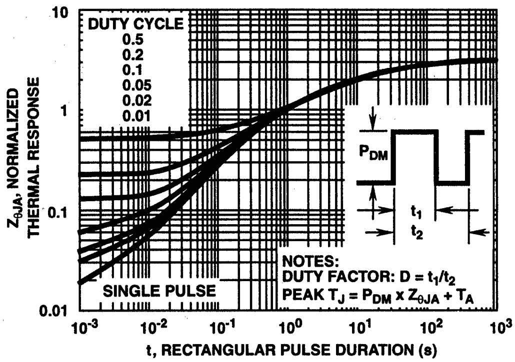


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

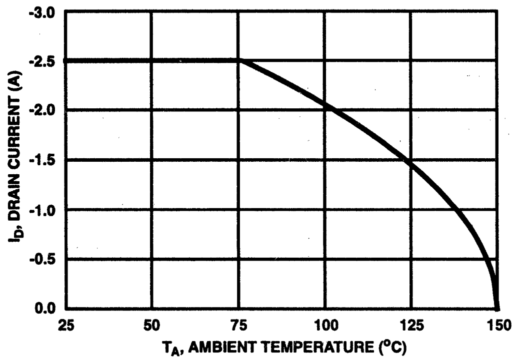


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

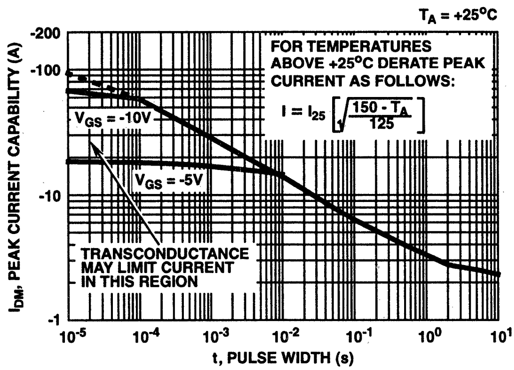


FIGURE 4. PEAK CURRENT CAPABILITY

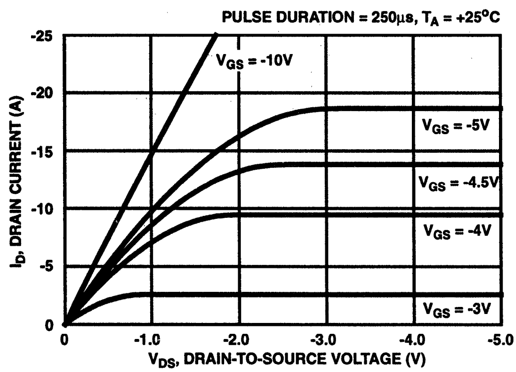


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

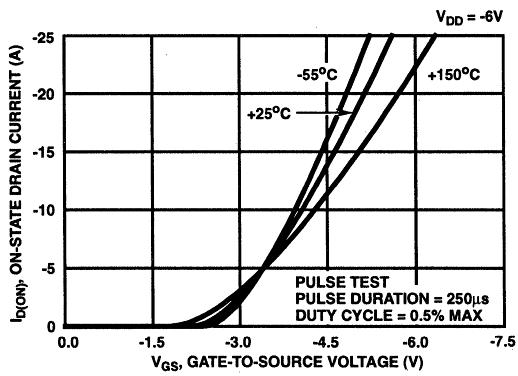


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

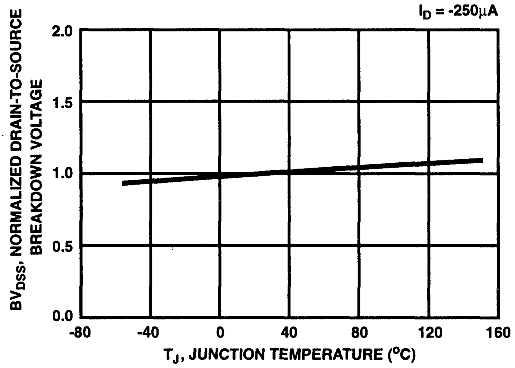


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

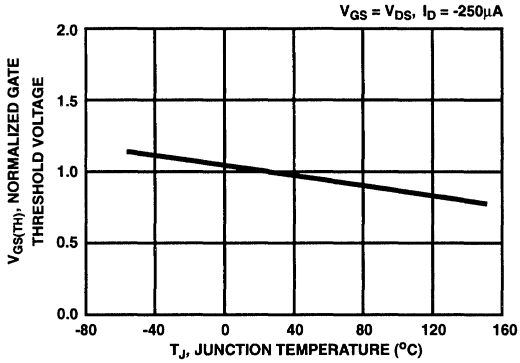


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

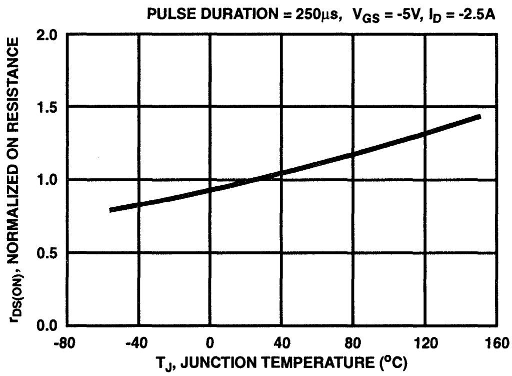


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

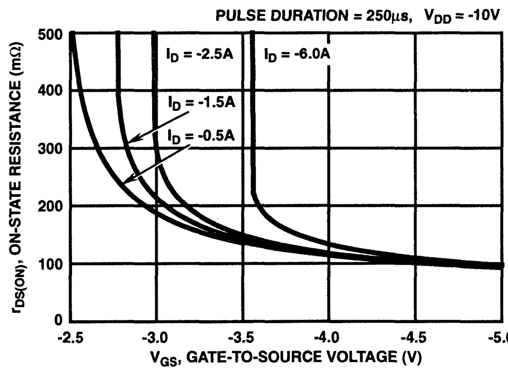


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

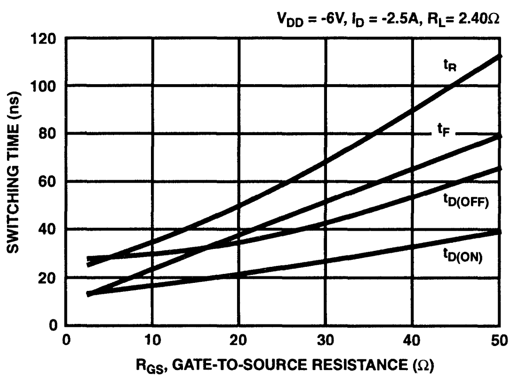


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

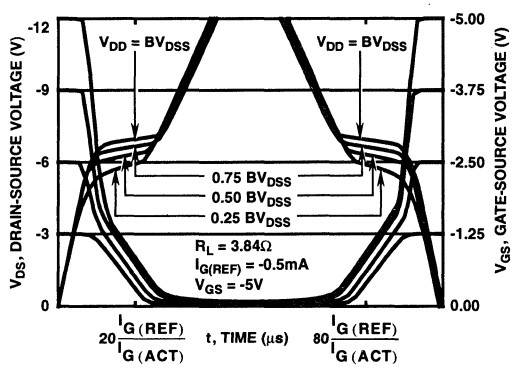


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

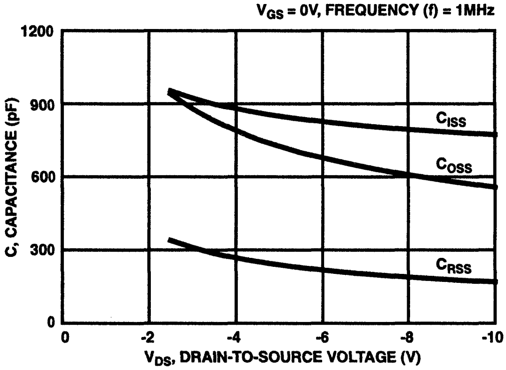


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

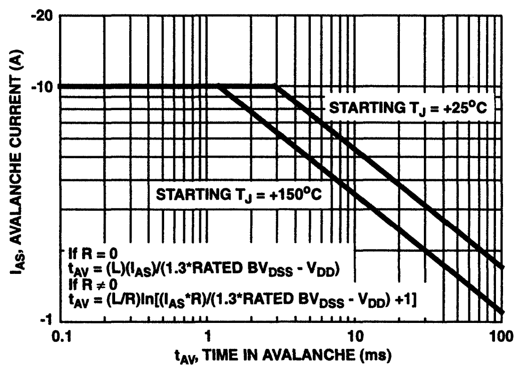


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

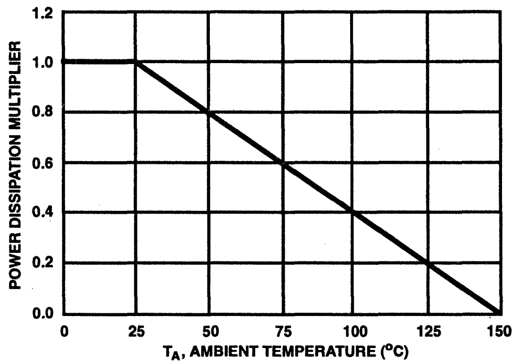


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms

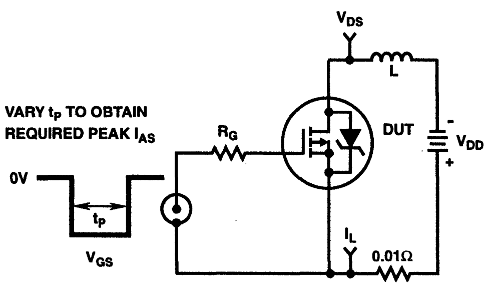


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

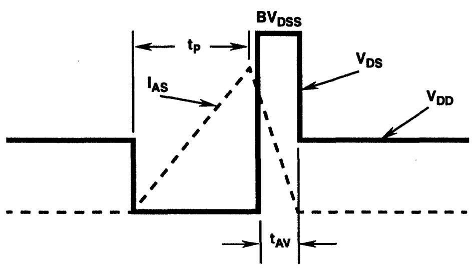


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

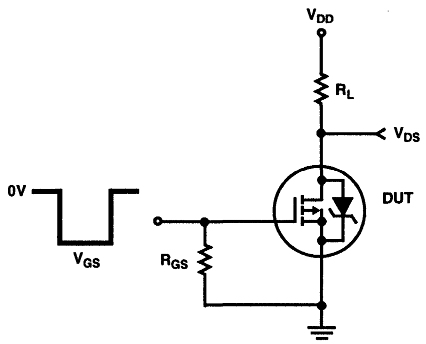


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

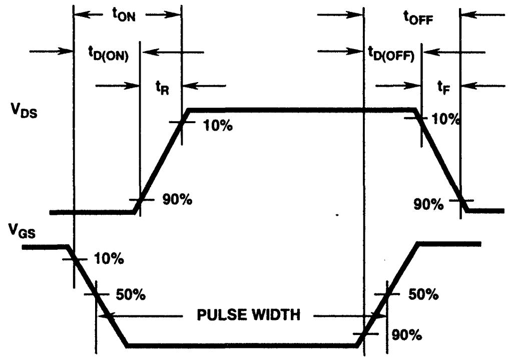


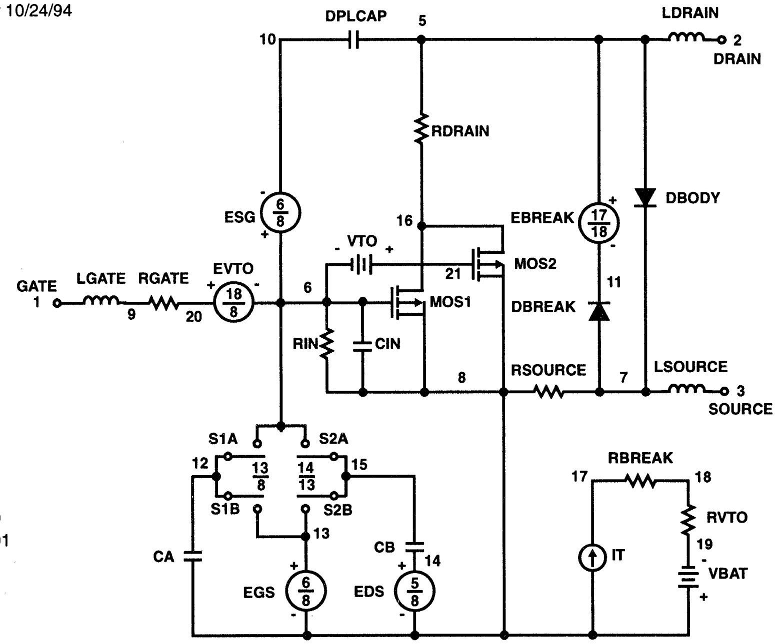
FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

Soldering Precautions

The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100°C. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5°C per second when changing from preheating to soldering.
4. The peak temperature in the soldering process should be at least 30°C higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time must not exceed 260°C for 10 seconds on the leads and case of the device.
6. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

Temperature Compensated PSPICE Model for the RF1K49093




```
SUBCKT RF1K49093 2 1 3;     rev 10/24/94

CA 12 8 8.75e-10
CB 15 14 8.65e-10
CIN 6 8 7.65e-10

DBODY 5 7 DBDMOD
DBREAK 7 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 5 11 17 18 -23.75
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 8 6 1
EVTO 20 6 8 18 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 1.233e-9
LSOURCE 3 7 0.452e-9

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 7.36e-3
RGATE 9 20 6.1
RIN 6 8 1e9
RSOURCE 8 7 RDSMOD 4.56e-2
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6  -0.558

.MODEL DBDMOD D (IS = 3.0e-13  RS = 4.4e-2  TRS1 = 1.0e-3  TRS2 = -7.37e-6  CJO = 1.27e-9  TT = 2.2e-8)
.MODEL DBKMOD D (RS = 7.84e-2  TRS1 = -4.27e-3  TRS2 = 5.77e-5)
.MODEL DPLCAPMOD D (CJO = 2.85e-10  IS = 1e-30  N = 10)
.MODEL MOSMOD PMOS (VTO = -2.1423  KP = 9.206  IS = 1e-30  N = 10  TOX = 1  L = 1u  W = 1u)
.MODEL RBKMOD RES (TC1 = 9.61e-4  TC2 = -1.09e-6)
.MODEL RDSMOD RES (TC1 = 2.10e-3  TC2 = 6.99e-6)
.MODEL RVTOMOD RES (TC1 = -1.82e-3  TC2 = 1.47e-7)
.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 5.47  VOFF= 3.47)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 3.47  VOFF= 5.47)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VCN = 1.05  VOFF= -3.95)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -3.95  VOFF= 1.05)

.ENDS
```

NOTE:

1. For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options;** IEEE Power Electronics Specialist Conference Records, 1991.

HARRIS SEMICONDUCTOR

RF1K49156

6.3A, 30V, Avalanche Rated, Logic Level, Single N-Channel Enhancement-Mode Power MOSFET

December 1995

Features

- 6.3A, 30V
- $r_{DS(ON)} = 0.030\Omega$
- *Temperature Compensating* PSPICE Model
- On-Resistance vs Gate Drive Voltage Curves
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RF1K49156 Single N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It was designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low-voltage bus switches. This product achieves full-rated conduction at a gate bias in the 3V - 5V range, thereby facilitating true on-off power control directly from logic level (5V) integrated circuits.

PACKAGING AVAILABILITY

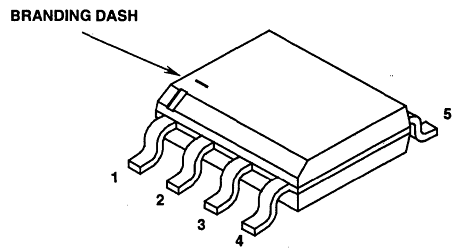
PART NUMBER	PACKAGE	BRAND
RF1K49156	MS-012AA	RF1K49156

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e., RF1K4915696.

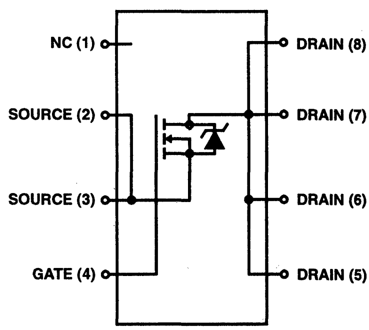
Formerly developmental type TA49156.

Packaging

JEDEC MS-012AA, (SOP-8)



Symbol



Absolute Maximum Ratings $T_A = +25^oC$

		RF1K49156	UNITS
Drain-Source Voltage	V_{DSS}	30	V
Drain-Gate Voltage	V_{DGR}	30	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current			
Continuous (Pulse width = 1s)	I_D	6.3	A
Pulsed	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_A = +25^oC$	P_D	2	W
Derate above $+25^oC$		0.016	$W/^oC$
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	^oC
Soldering Temperature of Leads for 10s	T_L	260	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

Electrical Specifications T_A = +25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V		30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA		1	-	2	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	T_A = +25°C	-	-	1	μA
			T_A = +150°C	-	-	50	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V		-	-	100	nA
On Resistance	$r_{DS(ON)}$	I_D = 6.3A, V_{GS} = 5V		-	-	0.030	Ω
Turn-On Time	t_{ON}	V_{DD} = 15V, I_D = 6.3A, R_L = 2.38Ω, V_{GS} = 5V, R_{GS} = 25Ω		-	-	165	ns
Turn-On Delay Time	$t_{D(ON)}$			-	35	-	ns
Rise Time	t_R			-	100	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	150	-	ns
Fall Time	t_F			-	95	-	ns
Turn-Off Time	t_{OFF}			-	-	300	ns
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 24V, I_D = 6.3A, R_L = 3.81Ω	-	52	65	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0V to 5V		-	29	37	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0V to 1V		-	1.8	2.3	nC
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz		-	2030	-	pF
Output Capacitance	C_{OSS}			-	625	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	105	-	pF
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	Pulse Width = 1s Device Mounted on FR-4 Material		-	-	62.5	°C/W

Source-Drain Diode Ratings and Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 6.3A	-	-	1.05	V
Reverse Recovery Time	t_{RR}	I_{SD} = 6.3A, dI_{SD}/dt = 100A/μs	-	-	58	ns

Typical Performance Curves

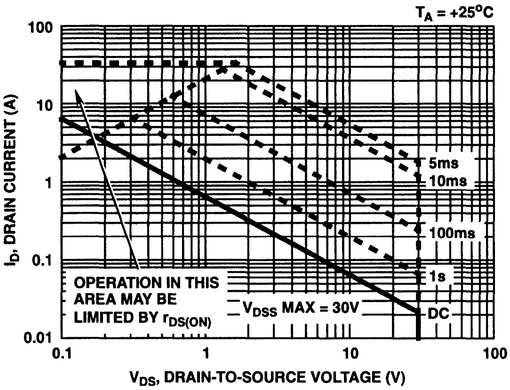


FIGURE 1. SAFE OPERATING AREA CURVE

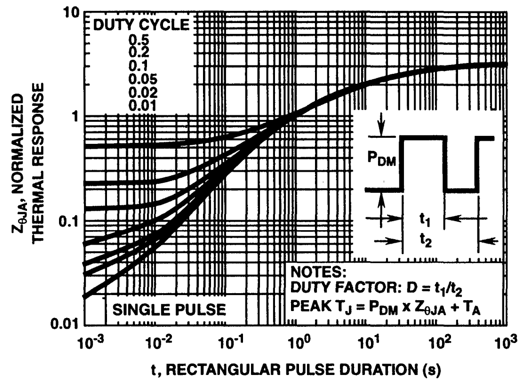


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

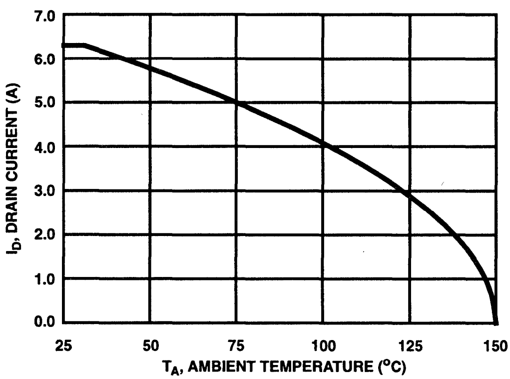


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

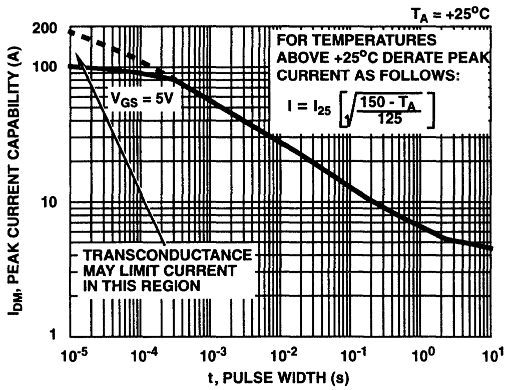


FIGURE 4. PEAK CURRENT CAPABILITY

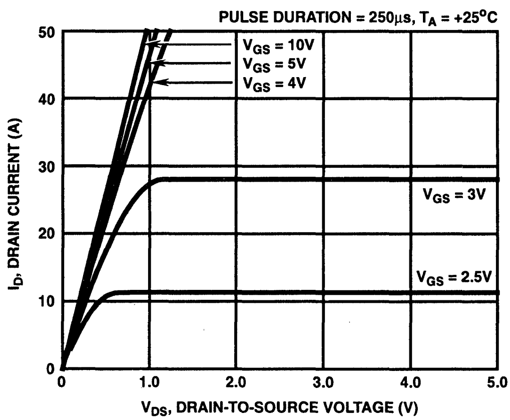


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

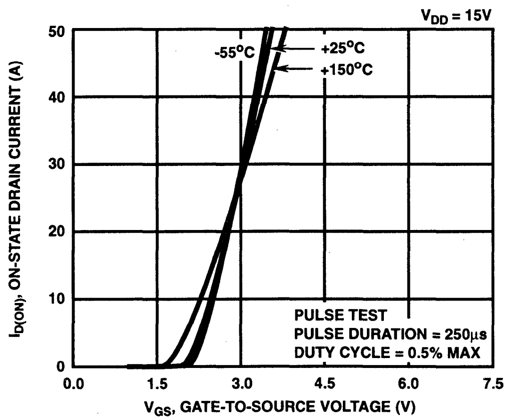


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

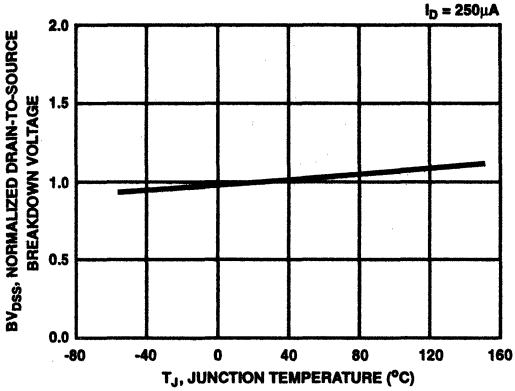


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

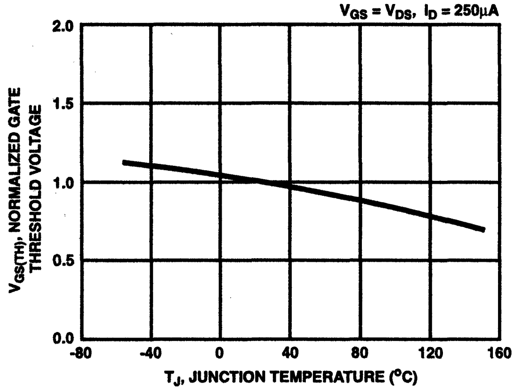


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

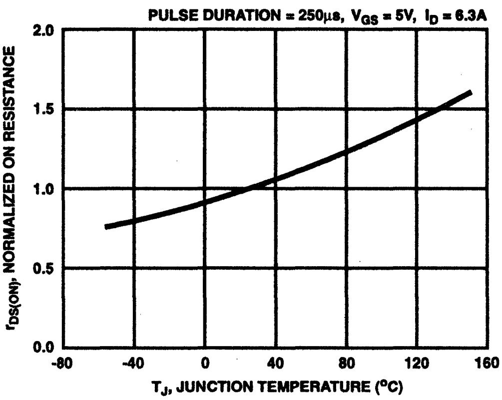


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

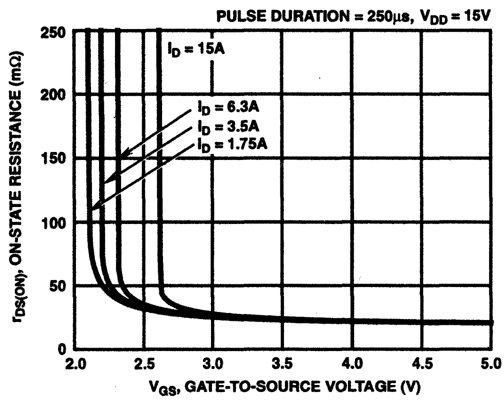


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

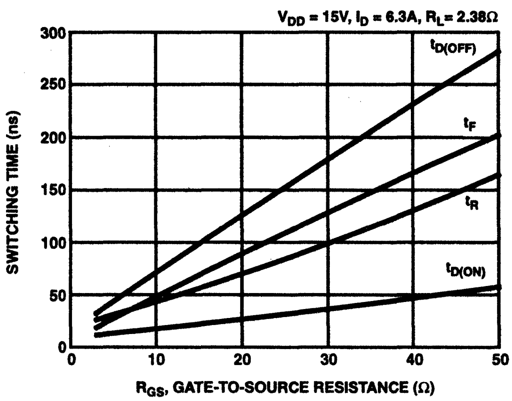


FIGURE 11. SWITCHING TIME AS A FUNCTION OF GATE RESISTANCE

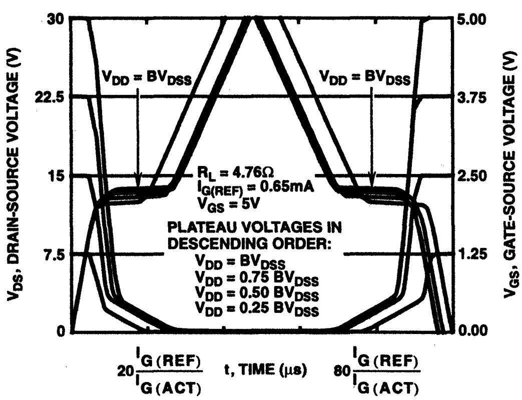


FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

Typical Performance Curves (Continued)

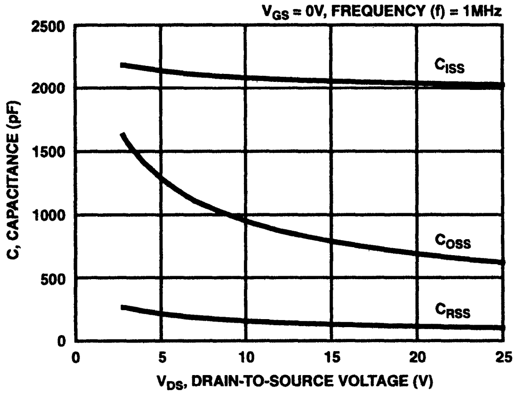


FIGURE 13. TYPICAL CAPACITANCE vs VOLTAGE

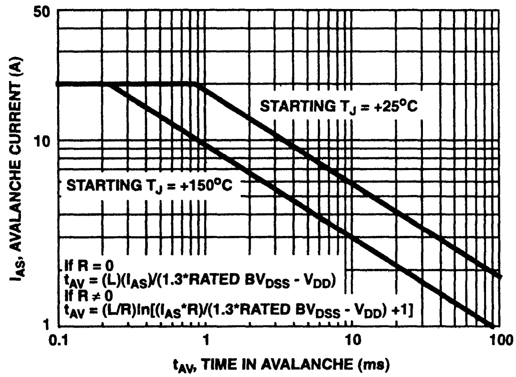


FIGURE 14. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

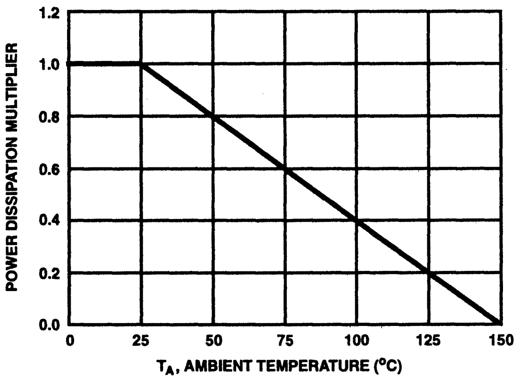


FIGURE 15. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Waveforms

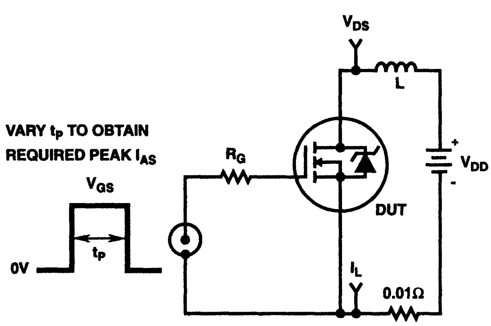


FIGURE 16. UNCLAMPED ENERGY TEST CIRCUIT

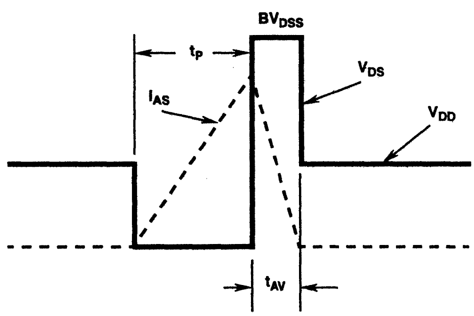


FIGURE 17. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

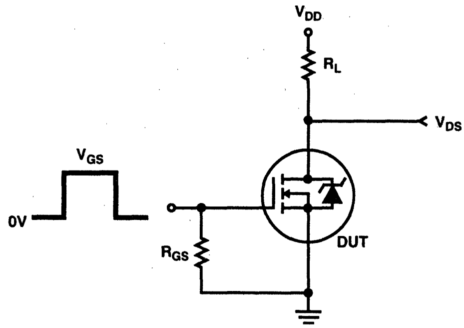


FIGURE 18. RESISTIVE SWITCHING TEST CIRCUIT

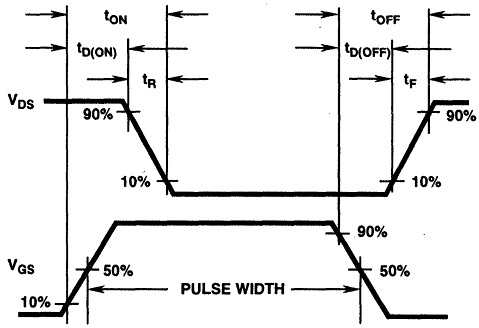


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

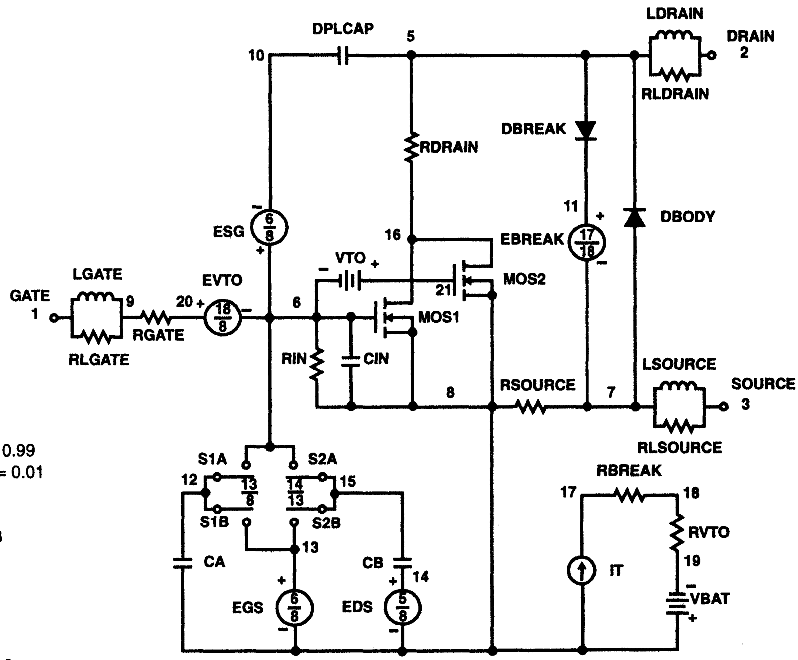
Soldering Precautions

The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100°C. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5°C per second when changing from preheating to soldering.
4. The peak temperature in the soldering process should be at least 30°C higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time must not exceed 260°C for 10 seconds on the leads and case of the device.
6. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

Temperature Compensated PSPICE Model for the RF1K49156

SUBCKT RF1K49156 2 1 3 ; rev 2/7/95



CA 12 8 2.953e-9
CB 15 14 2.810e-9
CIN 6 8 1.925e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 35.64
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTO 20 6 18 8 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 1.04e-9
LSOURCE 3 7 2.37e-10

MOS1 16 6 8 8 MOSMOD M = 0.99
MOS2 16 21 8 8 MOSMOD M = 0.01

RBREAK 17 18 RBKMOD 1
RDRAIN 5 16 RDSMOD 2.43e-3
RGATE 9 20 1.639
RIN 6 8 1e9
RLDRAIN 2 5 10
RLGATE 1 9 10.4
RLSOURCE 3 7 2.37
RSOURCE 8 7 RDSMOD 15.8e-3
RVTO 18 19 RVTOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 8 19 DC 1
VTO 21 6 0.453

.MODEL DBDMOD D (IS = 1.80e-12 RS = 1.50e-2 TRS1 = 3.70e-3 TRS2 = -2.23e-5 CJO = 2.63e-9 TT = 2.44e-8)
.MODEL DBKMOD D (RS = 4.15e-1 TRS1 = 6.50e-3 TRS2 = -3.80e-5)
.MODEL DPLCAPMOD D (CJO = 5.25e-10 IS = 1e-30 N = 10)
.MODEL MOSMOD NMOS (VTO = 1.92 KP = 136 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBKMOD RES (TC1 = 9.25e-4 TC2 = 5.61e-7)
.MODEL RDSMOD RES (TC1 = 3.62e-3 TC2 = 1.03e-5)
.MODEL RVTOMOD RES (TC1 = -1.85e-3 TC2 = -6.00e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.55 VOFF= -2.55)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.55 VOFF= -4.55)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.25 VOFF= 3.75)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 3.75 VOFF= -1.25)

.ENDS

NOTE:

1. For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options;** IEEE Power Electronics Specialist Conference Records, 1991.

HARRIS SEMICONDUCTOR

RF1K49157

6.3A, 30V, Avalanche Rated, Single N-Channel Enhancement-Mode Power MOSFET

December 1995

Features

- 6.3A, 30V
- $r_{DS(ON)} = 0.030\Omega$
- *Temperature Compensating* PSPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Description

The RF1K49157 Single N-Channel power MOSFET is manufactured using an advanced MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits, gives optimum utilization of silicon, resulting in outstanding performance. It was designed for use in applications such as switching regulators, switching converters, motor drivers, relay drivers, and low-voltage bus switches. This device can be operated directly from integrated circuits.

PACKAGING AVAILABILITY

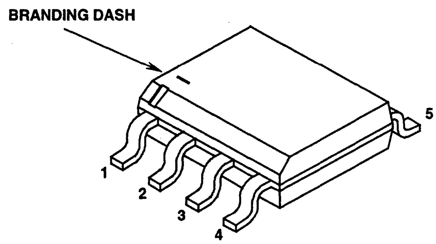
PART NUMBER	PACKAGE	BRAND
RF1K49157	MS-012AA	RF1K49157

NOTE: When ordering, use the entire part number. For ordering in tape and reel, add the suffix 96 to the part number, i.e. RF1K4915796.

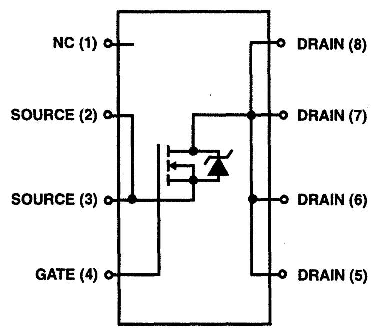
Formerly developmental type TA49157.

Package

JEDEC MS-012AA (SOP-8)



Symbol



Absolute Maximum Ratings $T_A = +25^oC$

		RF1K49157	UNITS
Drain-Source Voltage	V_{DSS}	30	V
Drain-Gate Voltage	V_{DGR}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous (Pulse width = 1s)	I_D	6.3	A
Pulsed	I_{DM}	Refer to Peak Current Curve	
Pulsed Avalanche Rating	E_{AS}	Refer to UIS Curve	
Power Dissipation			
$T_A = +25^oC$	P_D	2	W
Derate above $+25^oC$		0.016	W/^oC
Operating and Storage Temperature	T_{STG}, T_J	-55 to +150	^oC
Soldering Temperature of Leads for 10s	T_L	260	^oC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper ESD Handling Procedures.

File Number **4012.2**

Electrical Specifications $T_A = +25^oC$, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$		30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$		1	-	3	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 30V$, $V_{GS} = 0V$	$T_A = +25^oC$	-	-	1	µA
			$T_A = +150^oC$	-	-	50	µA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	100	nA
On Resistance	$r_{DS(ON)}$	$I_D = 6.3A$	$V_{GS} = 10V$	-	-	0.030	Ω
			$V_{GS} = 4.5V$	-	-	0.060	Ω
Turn-On Time	t_{ON}	$V_{DD} = 15V$, $I_D = 6.3A$, $R_L = 2.38\Omega$, $V_{GS} = 10V$, $R_{GS} = 25\Omega$		-	-	85	ns
Turn-On Delay Time	$t_{D(ON)}$			-	22	-	ns
Rise Time	t_R			-	43	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	125	-	ns
Fall Time	t_F			-	85	-	ns
Turn-Off Time	t_{OFF}			-	-	265	ns
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 0V$ to $20V$	$V_{DD} = 24V$, $I_D = 6.3A$, $R_L = 3.81\Omega$	-	70	88	nC
Gate Charge at 10V	$Q_{G(10)}$	$V_{GS} = 0V$ to $10V$		-	38	48	nC
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 0V$ to $2V$		-	2.8	3.5	nC
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz		-	1575	-	pF
Output Capacitance	C_{OSS}			-	700	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	200	-	pF
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	Pulse width = 1s Device mounted on FR-4 material		-	-	62.5	$^oC/W$

Source-Drain Diode Ratings and Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Forward Voltage	V_{SD}	$I_{SD} = 6.3A$	-	-	1.25	V
Reverse Recovery Time	t_{RR}	$I_{SD} = 6.3A$, $dI_{SD}/dt = 100A/\mu s$	-	-	60	ns

Typical Performance Curves

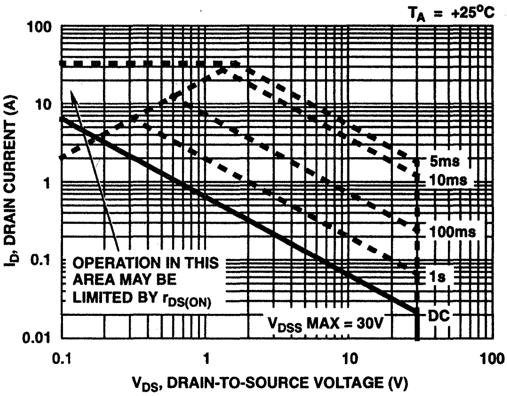


FIGURE 1. SAFE OPERATING AREA CURVE

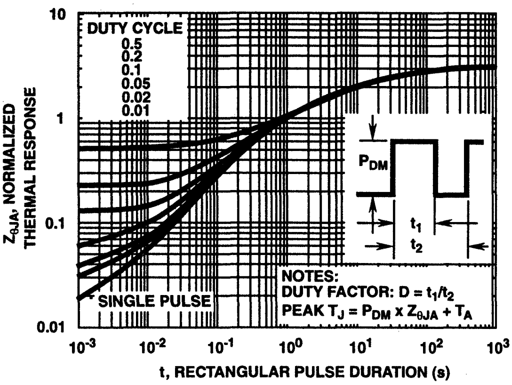


FIGURE 2. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

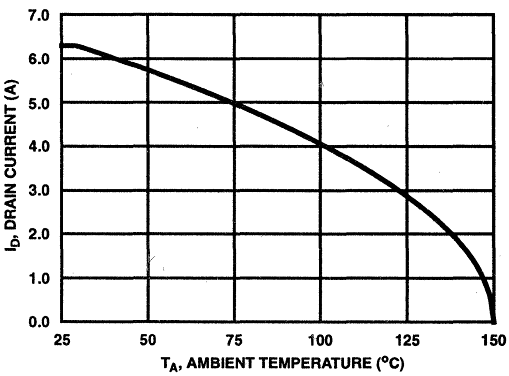


FIGURE 3. MAXIMUM CONTINUOUS DRAIN CURRENT vs TEMPERATURE

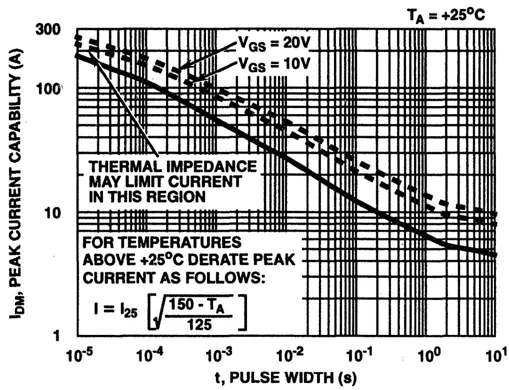


FIGURE 4. PEAK CURRENT CAPABILITY

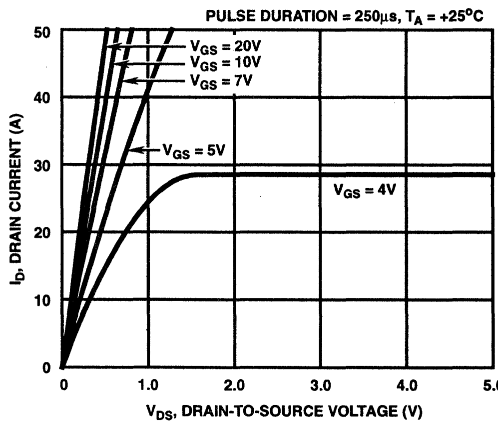


FIGURE 5. TYPICAL SATURATION CHARACTERISTICS

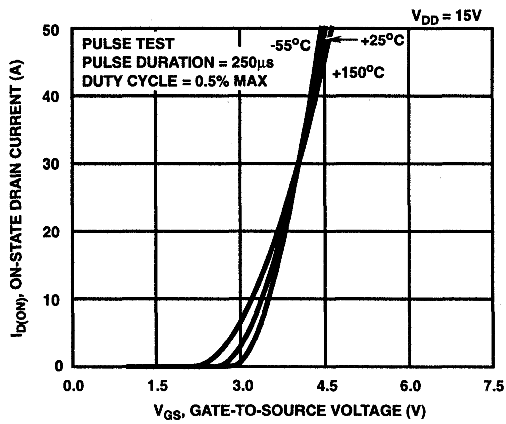


FIGURE 6. TYPICAL TRANSFER CHARACTERISTICS

Typical Performance Curves (Continued)

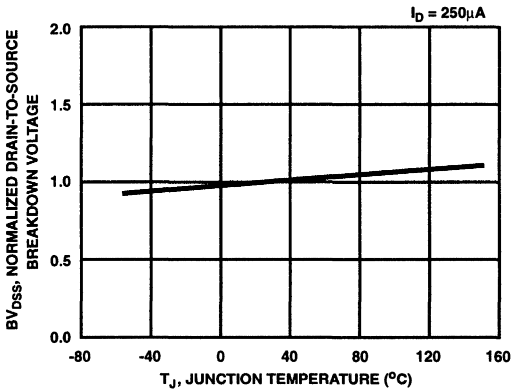


FIGURE 7. NORMALIZED DRAIN-SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

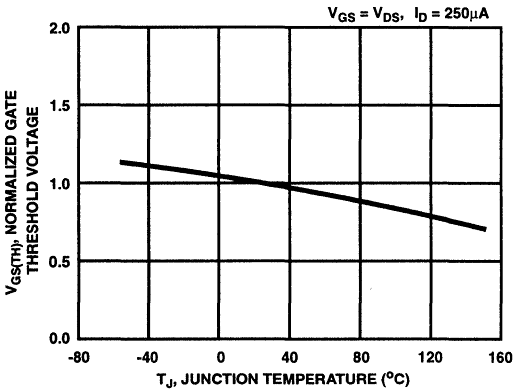


FIGURE 8. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

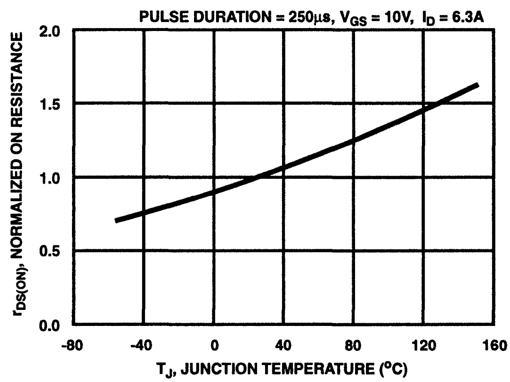


FIGURE 9. NORMALIZED $r_{DS(ON)}$ vs JUNCTION TEMPERATURE

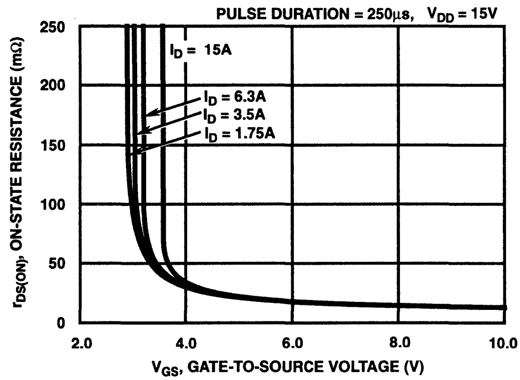


FIGURE 10. $r_{DS(ON)}$ FOR VARYING CONDITIONS OF GATE VOLTAGE AND DRAIN CURRENT

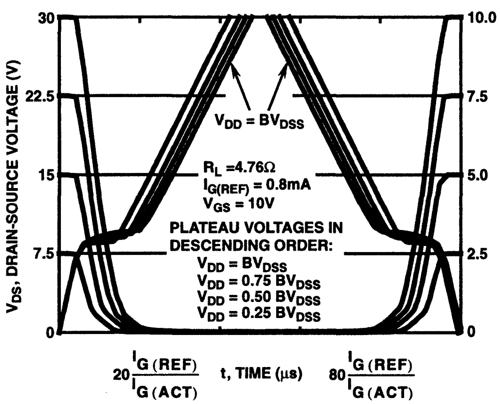


FIGURE 11. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT. REFER TO HARRIS APPLICATION NOTES AN7254 AND AN7260

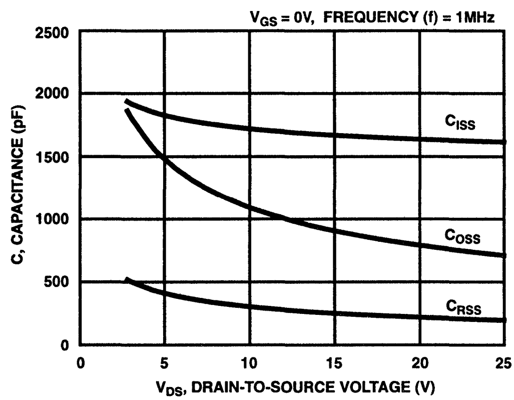


FIGURE 12. TYPICAL CAPACITANCE vs VOLTAGE

Typical Performance Curves (Continued)

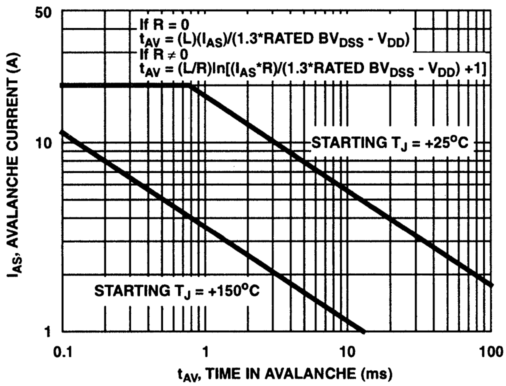


FIGURE 13. UNCLAMPED INDUCTIVE SWITCHING. REFER TO HARRIS APPLICATION NOTES AN9321 AND AN9322

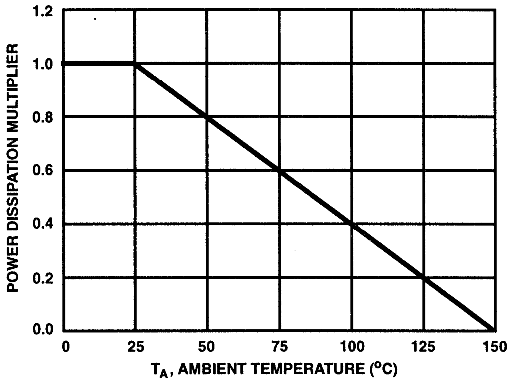


FIGURE 14. NORMALIZED POWER DISSIPATION vs TEMPERATURE DERATING CURVE

Test Circuits and Example Waveforms

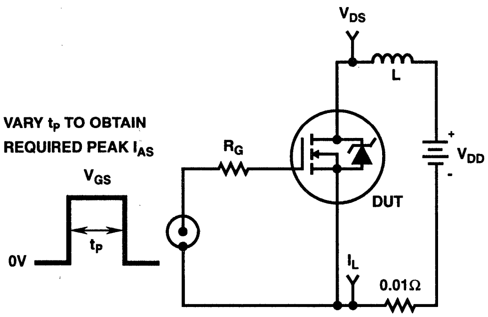


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

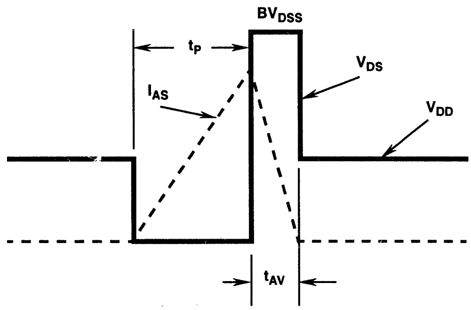


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

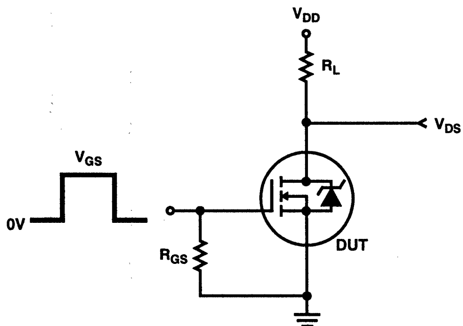


FIGURE 17. RESISTIVE SWITCHING TEST CIRCUIT

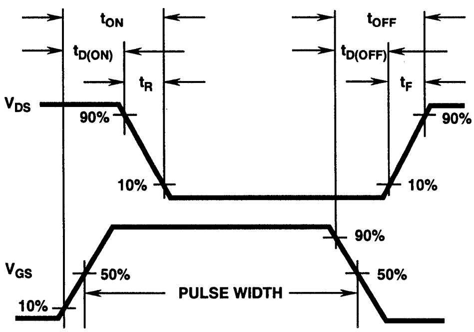
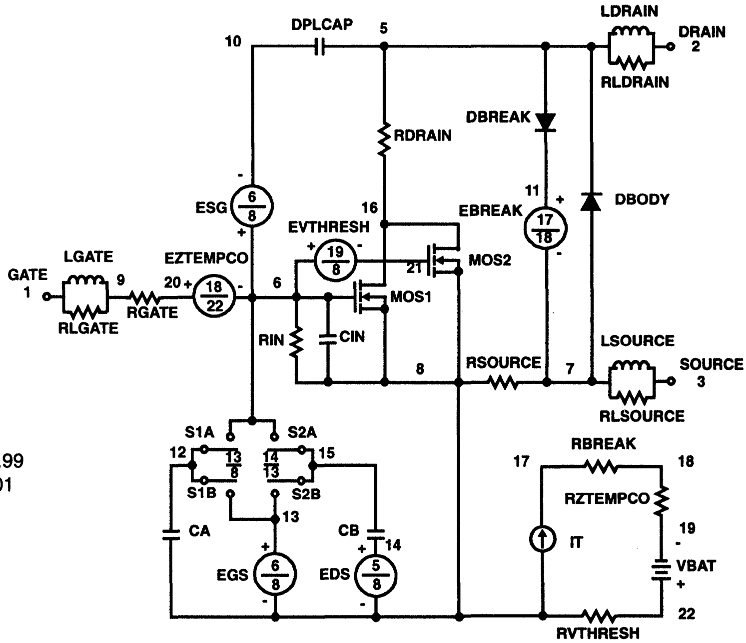


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

Temperature Compensated PSPICE Model for the RF1K49157

SUBCKT RF1K49157 2 1 3 ;   rev 3/14/95



CA 12 8 1.834e-9
CB 15 14 1.72e-9
CIN 6 8 1.416e-9

DBODY 7 5 DBDMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 34.89
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRESH 6 21 19 8 1
EZTEMPCO 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.0e-9
LGATE 1 9 1.04e-9
LSOURCE 3 7 0.237e-9

MOS1 16 6 8 8 MSTRONG M = 0.99
MOS2 16 21 8 8 MWEAK M = 0.01

RBREAK 17 18 RBREAKMOD 1
RDRAIN 5 16 RDRAINMOD 4.39e-3
RGATE 9 20 1.53
RIN 6 8 1e9
RLDRAIN 2 5 1.0
RLGATE 1 9 10.4
RLSOURCE 3 7 0.237
RSOURCE 8 7 RSOURCEMOD 4.44e-3
RTHRESH 22 8 RTHRESMOD 1
RZTEMPCO 18 19 RZTEMPCOMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

.MODEL DBDMOD D (IS = 1.14e-12 RS = 6.01e-3 TRS1 = 1.05e-4 TRS2 = -2.46e-5 CJO = 2.62e-9 TT = 2.44e-8)
.MODEL DBREAKMOD D (RS = 4.89e-1 TRS1 = 2.11e-3 TRS2 = -3.19e-6)
.MODEL DPLCAPMOD D (CJO = 1.007e-9 IS = 1e-30 N = 10)
.MODEL MSTRONG NMOS (VTO = 2.567 KP = 33.21 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAK NMOS (VTO=2.0225 KP = 33.21 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL RBREAKMOD RES (TC1 = 9.59e-4 TC2 = -2.87e-7)
.MODEL RDRAINMOD RES (TC1 = 8.08e-3 TC2 = 1.6e-5)
.MODEL RSOURCEMOD RES (TC1=0 TC2=0)
.MODEL RTHRESHMOD RES (TC1=-6.4e-4 TC2=-8.1e-6)
.MODEL RZTEMPCOMOD RES (TC1 = -2.43e-3 TC2 = 1.57e-6)
.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.47 VOFF= -4.47)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.47 VOFF= -6.47)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.3 VOFF= 1.7)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.7 VOFF= -3.3)

.ENDS

NOTE:

1. For further discussion of the PSPICE model, consult **A New PSPICE Sub-circuit for the Power MOSFET Featuring Global Temperature Options;** IEEE Power Electronics Specialist Conference Records, 1991.

Soldering Precautions

The soldering process creates a considerable thermal stress on any semiconductor component. The melting temperature of solder is higher than the maximum rated temperature of the device. The amount of time the device is heated to a high temperature should be minimized to assure device reliability. Therefore, the following precautions should always be observed in order to minimize the thermal stress to which the devices are subjected.

1. Always preheat the device.
2. The delta temperature between the preheat and soldering should always be less than 100°C. Failure to preheat the device can result in excessive thermal stress which can damage the device.
3. The maximum temperature gradient should be less than 5°C per second when changing from preheating to soldering.
4. The peak temperature in the soldering process should be at least 30°C higher than the melting point of the solder chosen.
5. The maximum soldering temperature and time must not exceed 260°C for 10 seconds on the leads and case of the device.
6. After soldering is complete, the device should be allowed to cool naturally for at least three minutes, as forced cooling will increase the temperature gradient and may result in latent failure due to mechanical stress.
7. During cooling, mechanical stress or shock should be avoided.

POWER MOSFETs 8

HARRIS QUALITY AND RELIABILITY

Quality and Reliability Assurance

The ability to build and maintain the high levels of quality and reliability today, depends on inherent design and process capability, and not the degree of test and inspection. Both the design and production facilities for Power MOSFETs are totally new, with state-of-the-art equipment and process techniques which deliver this needed capability.

In-Process Quality Control

All critical phases of the highly automated power MOSFET manufacturing cycle have been characterized with respect to their intrinsic variability. Statistical limits have been established to give warning of abnormal process trends and fluctuations, based on this intrinsic capability. These limits are constantly tightened as the process improves and are well within the engineering specifications. The emphasis at Harris is to employ statistical methods at the point of control, rather than an inspection point at the end of a process.

Control of Outgoing Product

The quality control lot acceptance sampling of finished product is performed after manufacturing has performed 100% inspection of all specified electrical characteristics. The current sampling level is 0.1% AQL for electrical parameters, and is constantly being improved. However, due to tight parameter distributions gained through process control and inherent design capability, the average outgoing quality level (AOQ) to the customer has been in the order of 100 PPM (0.01%).

Reliability Assurance

Harris Semiconductor has a world-wide reliability program that helps to shape the direction of new product development, assures that the reliability level is maintained throughout the production cycle, and develops specific models to predict the reliability in the end-use application. In order to meet these objectives, a reliability facility is maintained at each manufacturing location for real-time feedback. A centralized reliability engineering organization develops all new test methods and supports new product/process development. Each group is fully trained in the reliability and applied statistics disciplines, as well as failure analysis, and are responsible for using these techniques to monitor and improve product capability.

The Reliability Program

The reliability-assurance program operates at all stages of production, using the following four-pronged approach.

Product Design and Development

During early development, initial product lots are characterized through accelerated reliability tests which establish the product capability. Once the design had been fine-tuned, multiple production runs are initiated and samples are subjected to a full range of standardized accelerated tests. All lots must meet pre-established reliability standards before any new design or process can be released for production.

Wafer HTRB

Harris Semiconductor has developed a totally unique in-line reliability test performed at the wafer level. Samples from each wafer lot receive a 24-hour +150°C bias life test to measure passivation integrity and surface cleanliness.

Real Time Indicators (RTI)

RTI's are short-duration accelerated-stress tests used to control the occurrence of specific failure mechanisms that can significantly affect product reliability. The stress levels are designed to induce failures, so that product-capability shifts can be detected and corrected. They are performed weekly at each manufacturing location. In this real-time method of determining reliability, a continuous flow of data is provided to indicate how well the manufacturing process is performing product.

TABLE 1. TYPICAL MOSFET RTI TESTS

TEST	CONDITIONS	PACKAGE	TYPICAL DURATION
Power Cycling	PD = 4.75W T_J = +35°C - 175°C (approx.)	Plastic	10 - 15K Cycles
Power Cycling	PD = 4.75W T_J = +35°C - 175°C (approx.)	TO-3	20 - 50K Cycles
D-S Bias Life	T_A = +150°C 80% of Drain Source	All	168 Hours
G-S Bias Life	G - S = 16V T_A = +150°C	All	168 Hours

Requalification Program (RQP)

Each product is requalified every six to twelve months to the same matrix of tests required for the initial production release. This operation measures the changes in the total capability of each MOSFET family to meet the original reliability design objectives. Table 2 is typical of the data generated for RQP.

TABLE 2. ACCELERATED POWER MOSFET TEST RELIABILITY SUMMARY

PACKAGE	TEST AND CONDITIONS	DURATION	CUM. HOURS OR CYCLES	% NON-FUNCTIONAL
All	Bias Life Drain-Source = 80% of rated T_A = +150°C	500 Hours	300,000	0.33
All	Bias Life Gate-Source = 16V, T_A = +150°C	500 Hours	270,000	0.00
All	Operating Life T_A = +150°C, Free Air	500 Hours	230,000	0.00
TO-31 TO-39	Thermal Cycling -65°C to +150°C	400 Cycles	133,600	0.30
TO-220	Thermal Shock -65°C to +150°C	400 Cycles	100,000	0.00
TO-31 TO-39	Power Cycling Delta T_J = +78°C PD = 56W (TO-3) or 2W (TO-39)	20,000 Cycles	5,480K	0.73
TO-220	Power Cycling Delta T_J = +135°C, PD = 4.75W	10,000 Cycles	1,850K	0.00
TO-220	Pressure Cooker	24 Hours	3,072	0.00

FAILURE RATE IN %/1000 HOURS AT 60% UCL			
TEST	**T_A = +125°C**	**T_A = +90°C**	**T_A = +75°C**
Bias Life	0.09	0.005	0.001
Operating Life	0.07	0.004	0.001

NOTE: Failure rate based on nonfunctional performance in an operating mode, extrapolated from +150°C data using 1.0eV activation energy.

Advanced Power Package Construction Method Raises TO-252 Reliability To New Heights

This technical backgrounder is intended to show how Harris redesigned the TO-252 surface-mount power package into the most reliable package of its type in the industry.

Surface-Mount Packaging Introduction

The continuing development of surface-mount technology (SMT) as a replacement for conventional through-hole mounting of electronic components on single-sided printed circuit boards has led to a host of advantages for electronics equipment manufacturers. From an integrated circuit standpoint, SMT allows manufacturers to optimize packaging density since ICs can be mounted on both sides of a board. SMT also offers thrifty and efficient use of material resources by permitting circuit boards to be smaller, closer component spacing, lower assembly costs and more compact and lighter system housings. Semiconductor companies have steadily promoted SMT growth by creating a variety of high-density, high lead-count ICs designed to be easily assembled onto the smaller footprints of SM circuit boards.

Most circuit boards perform functions in addition to the signal processing and logic operations handled by ICs. To interface with and drive off-board components such as amplifiers, motors, printer hammers, relays and the like, requires power devices mounted on SM boards in close proximity to their signal sources. But SMT power devices are not as simple to use as their IC partners. Because of the reduced size of SM boards, the confined space alloted for the package and the greater dissipation of a power device, attention to thermal management and heat sinking take on greater significance.

To squeeze a power device into the confined area demanded by SM boards, semiconductor manufacturers have developed the plastic TO-252 package, popularly known as the D-pak (see Figure 1). With its gull-wing leads and metal back designed to pull heat from the device inside, the TO-252 offers to designers a high-power SM package. Unlike the variety of IC packages that designers can choose among, the TO-252 has become the workhorse package for SM power MOSFETs and rectifiers. Since it is widely used and applied in applications in which device failure is more probable because of internal heat generation, it is vital that TO-252-packaged power devices meet the highest standards for reliable operation.

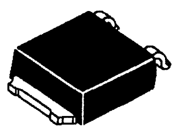


FIGURE 1. TO-252

While today's TO-252-packaged power devices are manufactured to meet extremely high reliability standards, that has not always been the case. In the recent past, all the leading power semiconductor suppliers of the TO-252 have been hampered by manufacturing problems that are rooted in the package's size, materials and fabrication methods.These problems can be inadvertently passed on to users who don't detect them until after the devices have been assembled into boards.

Like its competitors, Harris Semiconductor has experienced problems with the package. When unexplained problems arose on customer production lines, the company launched an exhaustive year-long investigation into the TO-252 that encompassed every detail of its manufacturing process, materials, fabrication, process control and testing. The result of this comprehensive effort, undertaken with the assistance of a number of customers who produce computer, automotive and cellular telephone products, is a vastly improved method for building and testing TO-252-packaged power devices. Extensive monitoring and testing of tens of thousands of production line devices reveal that the redesigned TO-252 is a robust power package capable of surviving extremely demanding thermal environments during assembly onto boards and under operating conditions.

Since no process is ever perfect, Harris Semiconductor offers this report to power designers and production personnel to increase awareness of problems that may occur using plastic, surface-mount power devices. By understanding the structural foundation of the package and the improvements incorporated in the Harris manufacturing process, users can have increased confidence that the company's TO-252 power devices will provide unmatched service and reliability in any application and environment for which the devices are intended.

The TO-252 Problem

When a TO-252-packaged power device fails after it has been assembled into a SM circuit board, the most likely conclusion that a user might draw is that the semiconductor die has cracked from thermal stresses induced by their soldering process. However, research indicates that the die was likely damaged during the manufacturing process and that the thermal shock of soldering only exacerbates the problem. There is no evidence to conclude that a user's mounting or assembly methods are the root of the problem. Die cracking is a generic problem in the TO-252 and can affect any manufacturer. The smaller the semiconductor die (its physical dimensions) the less likely it is to crack.

The root cause of die cracking stems from the materials and physical configuration of the TO-252 and the size of the die put into the package. In the manufacturing process, the die is attached to the header by a thin layer of solder (see Figure 2). The solder serves to reduce the thermal coefficient of expansion mismatch between the silicon die and the copper header.

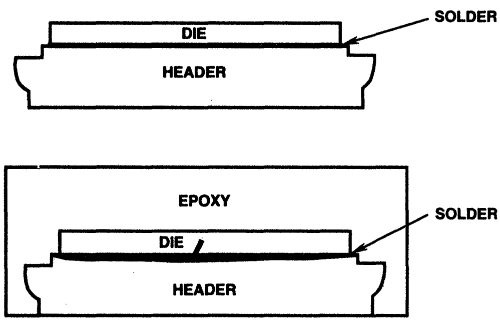


FIGURE 2.

The next step is to put an epoxy encapsulation over the die and header to form the package's molded outer shell (Figure 2). The shrinking of the mold epoxy compound forces the header to deflect, but in the opposite direction from the die attach process (concave on the top, convex on the bottom). This type of stress puts tension on the bottom of the die which can lead to cracking because the die is not as resistant to stress in this direction. Deflection of the header is more pronounced under epoxy curing than during die attach, resulting in greater forces on the die.

Slight cracks in the die may result from the shrinking mold compound but they usually do not result in electrical failure of the device. It is the thermal shock of wave soldering during board assembly that forces the cracks to open wider and lead to eventual failure.

The TO-252 Solution

After identifying the primary cause of failed devices, engineers at Harris initiated an extensive program to redesign the TO-252 by changing materials and increasing the strength of mechanical components. This involved experimentation with different components supported by a sophisticated computer-aided design technique called Finite Element Analysis (FEA).

Initial analysis showed that the standard 20-mil thick header could bow by 1- to 2-mils during epoxy curing. This bowing puts excessive tension on the backside of the die, making it more susceptible to cracking. After many experiments, it became clear that the amount of deflection with a 20-mil header could not be compensated for with solder thickness, assembly methods or low-stress epoxies. Through FEA, it was determined that increasing the header thickness to 35-mils would eliminate most of the deflection. To achieve a 35-mil thickness without retooling all the mount and mold equipment, it was decided to use a pedestal of 35-mils under the die.

FEA is an extremely valuable tool that permits the modeling of a device's critical package elements, materials, headers, overcoat material, oxides and others. It provides solutions for reducing stress at dissimilar material junctions, thus, minimizing device failure. The real benefit of FEA is its ability to simulate complex packaging relationships in a fast and accurate way. The stress models produced by FEA can be generated faster and at lower cost than by actually constructing and modifying physical models. FEA models point the way to the most favorable solutions which can then be implemented with actual materials.

FEA also came into play to help determine the best epoxy compound to use. The epoxy is probably the most critical element in the problem of cracked die because its curing generates the forces that cause the header to bow. And the bowing of the header produces the tension that cracks the die. To solve the problem, engineers selected an improved epoxy which balances stress vs. power cycling reliability. They then tested the new compound with the largest die that fit in the TO-252 to ensure that no cracking occurred.

At this point, the critical elements for solving the problem had fallen into place: increase the header thickness to 35 mils, go to an improved epoxy to reduce tension on the die and improve the process control over the thickness of the solder between the die and header. One other change in the manufacturing process was made to prevent any unnecessary shock to the die when the completed package is separated from the strip that holds a whole run of devices together. The conventional way to separate devices is called frame shear, a mechanical method that shears the strip away and can transfer forces from the package's heatsink to the die, possibly leading to cracking. In place of frame shear, Harris employs a less stressful method of device separation. In this technique, a shallow groove (10 mils deep) is cut into the heatsink portion of the package to reduce the force on the header and die when separating the package from the strip.

After hundreds of thousands of devices were fabricated with the new process, Harris engineers pulled tens of thousands off the line and subjected them to a grueling reliability test. The test is called solder shock and requires that the devices be fully immersed in a liquid solder bath at a temperature of 260°C for 10 seconds. Solder shock closely simulates the conditions that the package is subjected to when a user wave solders the part into a SM circuit board. The thermal shock of the solder bath is intended to increase the stress on the header and cause sufficient movement to make any existing crack wider detectable via electrical testing.

Harris has run solder shock tests on over 24,000 TO-252-packaged devices during the past year and no device has ever failed. Over 15,000 devices were chemically decapsulated and correlated to solder shock results. No die cracks were ever found when examined under high-power magnification. In addition, the company has sold more than 4.7 million devices without having any reports or returns due to a cracked die. This record of reliability is unmatched by any other manufacturer of TO-252-packaged power semiconductors and should give users confidence that the company offers the manufacturing and engineering capabilities to produce the highest quality products for today's complex electronic systems.

POWER MOSFETs 9

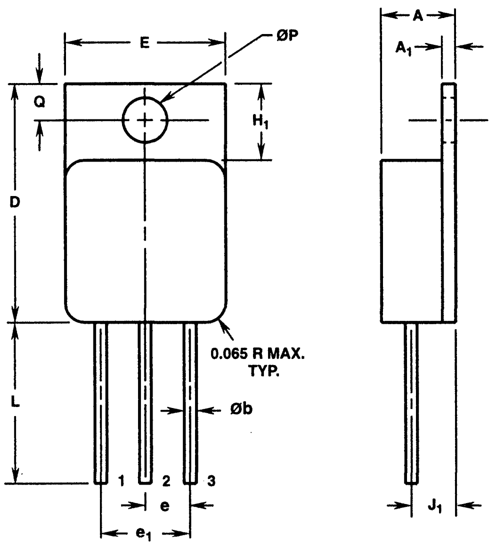
PACKAGING AND ORDERING INFORMATION

PAGE

ORDERING INFORMATION

To order any part in this databook, use the full part number on the data sheet.

Hermetic Metal Packages



TO-254AA

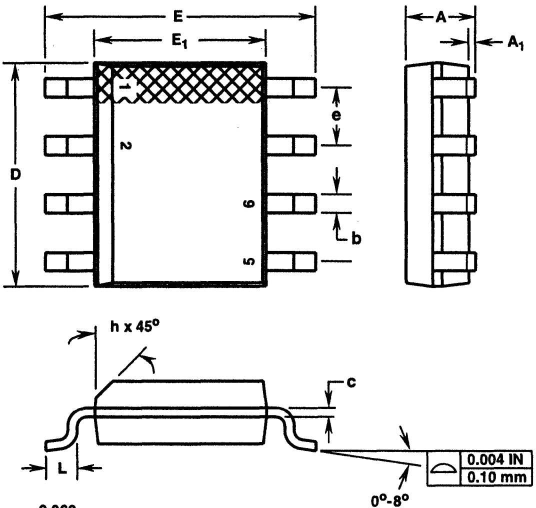
3 LEAD JEDEC TO-254AA HERMETIC METAL PACKAGE

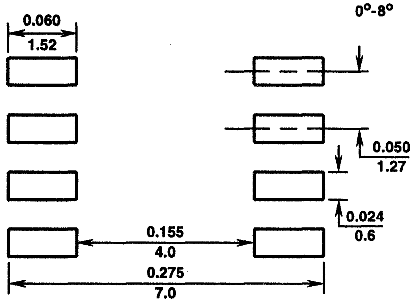
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.249	0.260	6.33	6.60	-
A_1	0.040	0.050	1.02	1.27	-
Øb	0.035	0.045	0.89	1.14	2, 3
D	0.790	0.800	20.07	20.32	-
E	0.535	0.545	13.59	13.84	-
e	0.150 TYP		3.81 TYP		4
e_1	0.300 BSC		7.62 BSC		4
H_1	0.245	0.265	6.23	6.73	-
J_1	0.140	0.160	3.56	4.06	4
L	0.520	0.560	13.21	14.22	-
ØP	0.139	0.149	3.54	3.78	-
Q	0.110	0.130	2.80	3.30	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC outline TO-254AA dated 11-86.
2. Add typically 0.002 inches (0.05mm) for solder coating.
3. Lead dimension (without solder).
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Die to base BeO isolated, terminals to case ceramic isolated.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

Plastic Packages





MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE-MOUNTED APPLICATIONS

MS-012AA

8 LEAD JEDEC MS-012AA SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.0532	0.0688	1.35	1.75	-
A_1	0.004	0.0098	0.10	0.25	-
b	0.013	0.020	0.33	0.51	-
c	0.0075	0.0098	0.19	0.25	-
D	0.189	0.1968	4.80	5.00	2
E	0.2284	0.244	5.80	6.20	-
E_1	0.1497	0.1574	3.80	4.00	3
e	0.050 BSC		1.27 BSC		-
H	0.0099	0.0196	0.25	0.50	-
L	0.016	0.050	0.40	1.27	4

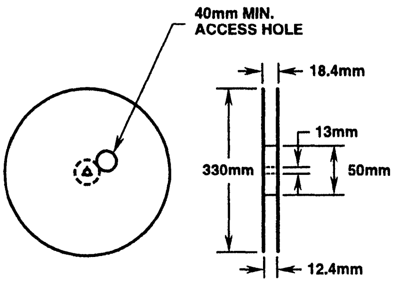
NOTES:

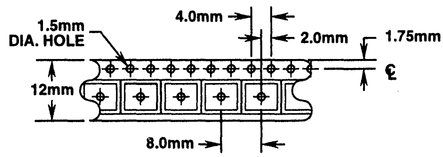
1. All dimensions are within allowable dimensions of Rev. C of JEDEC MS-012AA outline dated 5-90.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006 inches (0.15mm) per side.
3. Dimension "E_1" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 0.010 inches (0.25mm) per side.
4. "L" is the length of terminal for soldering.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. Controlling dimension: Millimeter.
7. Revision 4 dated 9-6-95.

Plastic Packages

MS-012AA

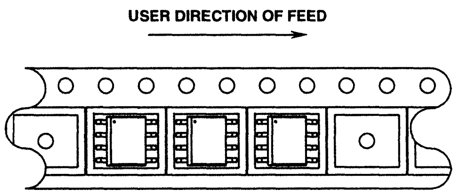
12mm TAPE AND REEL

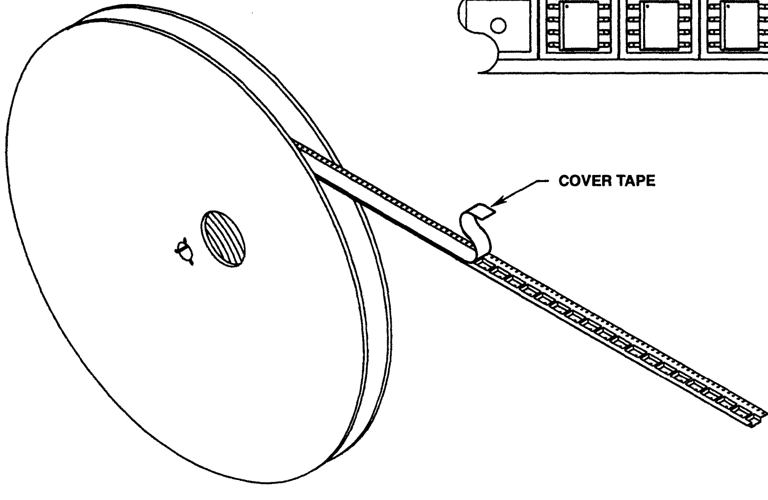




GENERAL INFORMATION

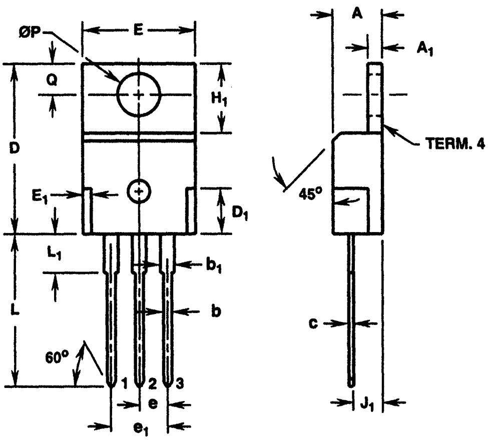
1. USE "96" SUFFIX ON PART NUMBER.
2. 2500 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.





Revision 4 dated 9-95

Plastic Packages



TO-220AB

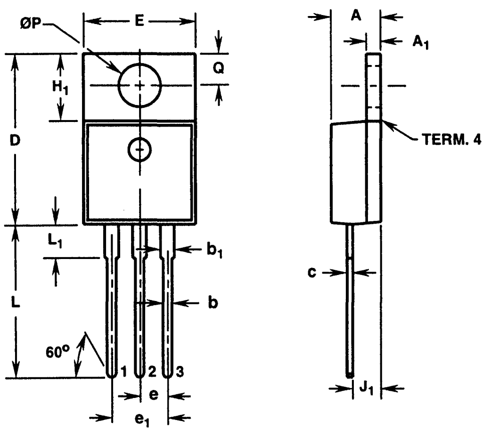
3 LEAD JEDEC TO-220AB PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 1 dated 1-93.

Plastic Packages



TO-220AB (ALTERNATE VERSION)

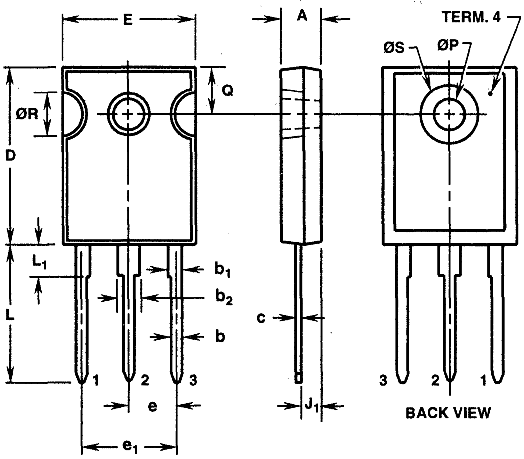
3 LEAD JEDEC TO-220AB PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	2, 4
b	0.030	0.034	0.77	0.86	2, 4
b_1	0.045	0.055	1.15	1.39	2, 4
c	0.018	0.022	0.46	0.55	2, 4
D	0.590	0.610	14.99	15.49	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	3
ØP	0.149	0.153	3.79	3.88	-
Q	0.105	0.115	2.66	2.92	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Dimension (without solder).
3. Solder finish uncontrolled in this area.
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 10-95.

Plastic Packages



TO-247

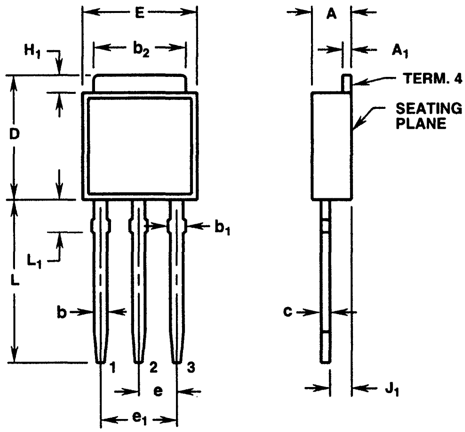
3 LEAD JEDEC STYLE TO-247 PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.180	0.190	4.58	4.82	-
b	0.046	0.051	1.17	1.29	2, 3
b_1	0.060	0.070	1.53	1.77	1, 2
b_2	0.095	0.105	2.42	2.66	1, 2
c	0.020	0.026	0.51	0.66	1, 2, 3
D	0.800	0.820	20.32	20.82	-
E	0.605	0.625	15.37	15.87	-
e	0.219 TYP		5.56 TYP		4
e_1	0.438 BSC		11.12 BSC		4
J_1	0.090	0.105	2.29	2.66	5
L	0.620	0.640	15.75	16.25	-
L_1	0.145	0.155	3.69	3.93	1
ØP	0.138	0.144	3.51	3.65	-
Q	0.210	0.220	5.34	5.58	-
ØR	0.195	0.205	4.96	5.20	-
ØS	0.260	0.270	6.61	6.85	-

NOTES:

1. Lead dimension and finish uncontrolled in L_1.
2. Lead dimension (without solder).
3. Add typically 0.002 inches (0.05mm) for solder coating.
4. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
5. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
6. Controlling dimension: Inch.
7. Revision 1 dated 1-93.

Plastic Packages



TO-251AA

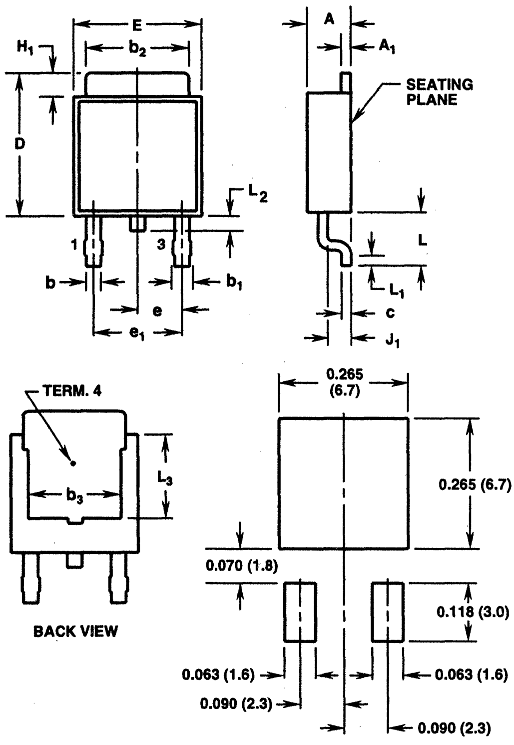
3 LEAD JEDEC TO-251AA PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	3, 4
b	0.028	0.032	0.72	0.81	3, 4
b_1	0.033	0.040	0.84	1.01	3
b_2	0.205	0.215	5.21	5.46	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		5
e_1	0.180 BSC		4.57 BSC		5
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	6
L	0.355	0.375	9.02	9.52	-
L_1	0.075	0.090	1.91	2.28	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-251AA outline dated 9-88.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 10-95.

Plastic Packages



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

TO-252AA

SURFACE MOUNT JEDEC TO-252AA PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b_1	0.033	0.040	0.84	1.01	4
b_2	0.205	0.215	5.21	5.46	4, 5
b_3	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.290	6.86	7.36	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e_1	0.180 BSC		4.57 BSC		7
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L_1	0.020	-	0.51	-	4, 6
L_2	0.025	0.040	0.64	1.01	3
L_3	0.170	-	4.32	-	2

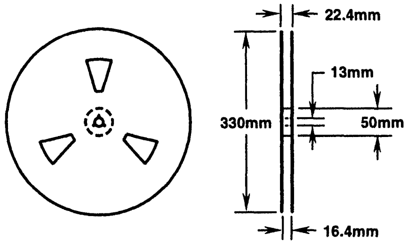
NOTES:

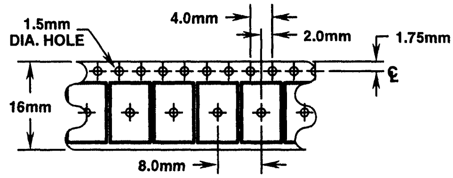
1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
2. L_3 and b_3 dimensions establish a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 5 dated 10-95.

Plastic Packages

TO-252AA

16mm TAPE AND REEL

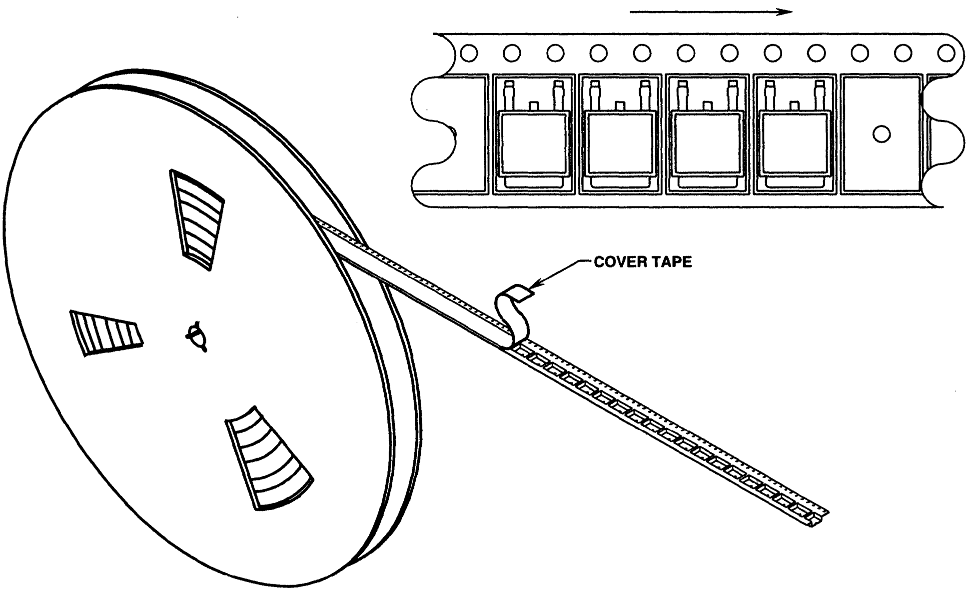




GENERAL INFORMATION

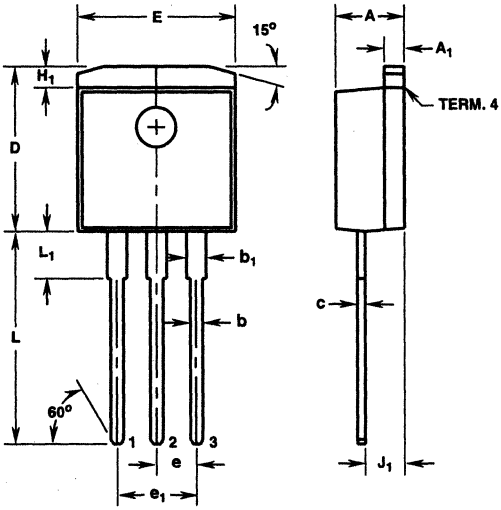
1. USE "9A" SUFFIX ON PART NUMBER.
2. 2500 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

USER DIRECTION OF FEED



Revision 5 dated 10-95

Plastic Packages



TO-262AA

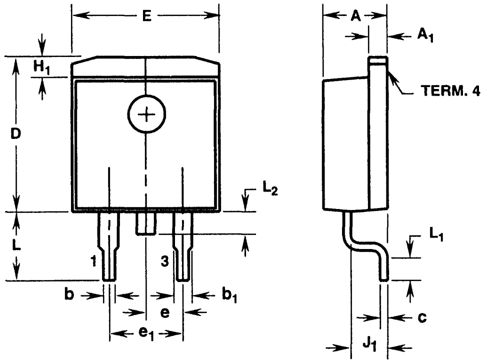
3 LEAD JEDEC TO-262AA PLASTIC PACKAGE

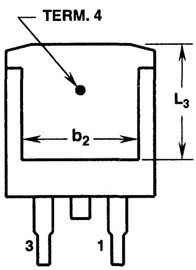
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	3, 4
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	3, 4
c	0.018	0.022	0.46	0.55	3, 4
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	6
L	0.530	0.550	13.47	13.97	-
L_1	0.110	0.130	2.80	3.30	2

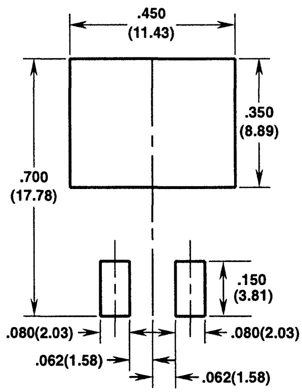
NOTES:

1. These dimensions are within allowable dimensions of Rev. A of JEDEC TO-262AA outline dated 6-90.
2. Solder finish uncontrolled in this area.
3. Dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder plating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 4 dated 10-95.

Plastic Packages







MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

TO-263AB

SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b_1	0.045	0.055	1.15	1.39	4, 5
b_2	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e_1	0.200 BSC		5.08 BSC		7
H_1	0.045	0.055	1.15	1.39	-
J_1	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L_1	0.090	0.110	2.29	2.79	4, 6
L_2	0.050	0.070	1.27	1.77	3
L_3	0.315	-	8.01	-	2

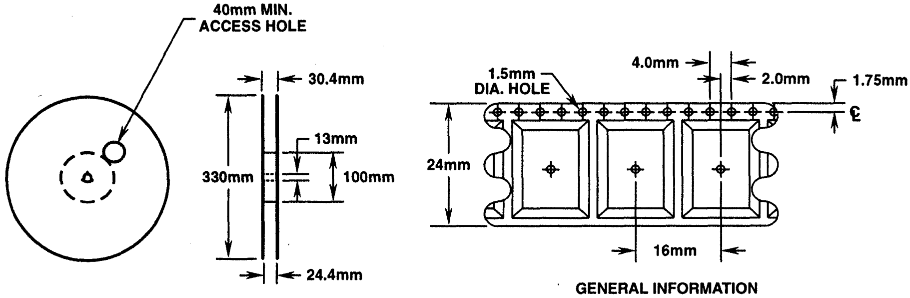
NOTES:

1. These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
2. L_3 and b_2 dimensions established a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 7 dated 10-95.

Plastic Packages

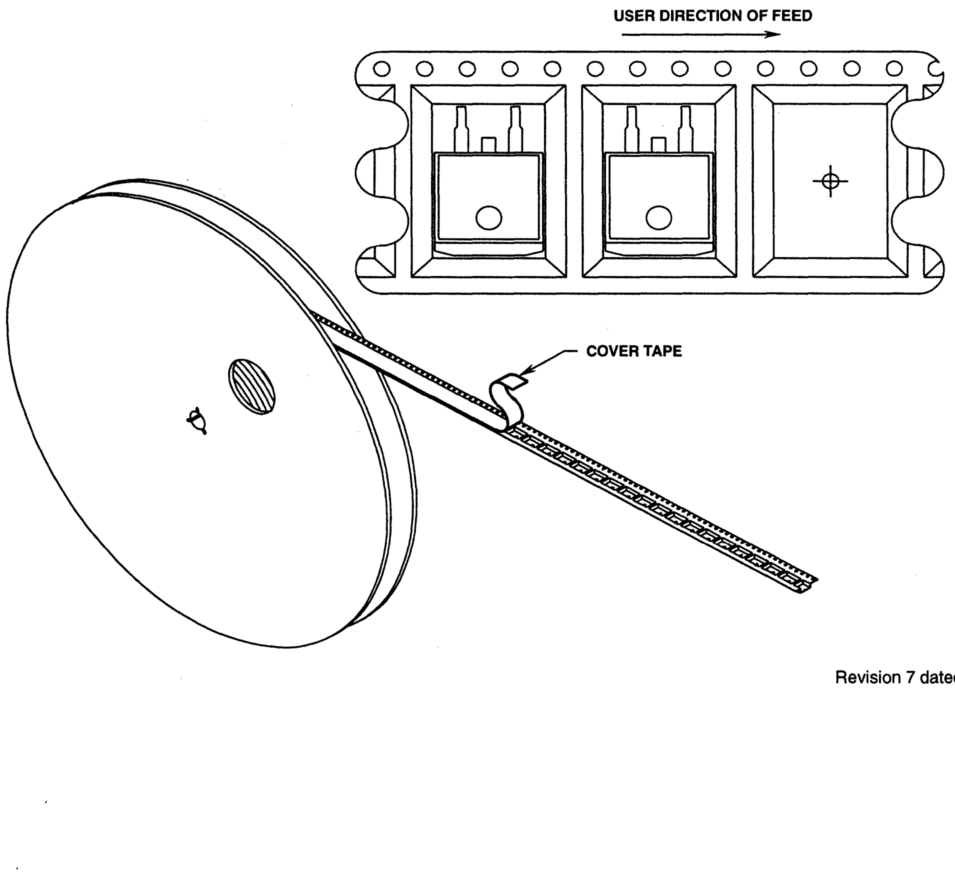
TO-263AB

24mm TAPE AND REEL



GENERAL INFORMATION

1. USE "9A" SUFFIX ON PART NUMBER.
2. 800 PIECES PER REEL.
3. ORDER IN MULTIPLES OF FULL REELS ONLY.
4. MEETS EIA-481 REVISION "A" SPECIFICATIONS.



Revision 7 dated 10-95

POWER MOSFETs 10

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Your Map to Harris AnswerFAX

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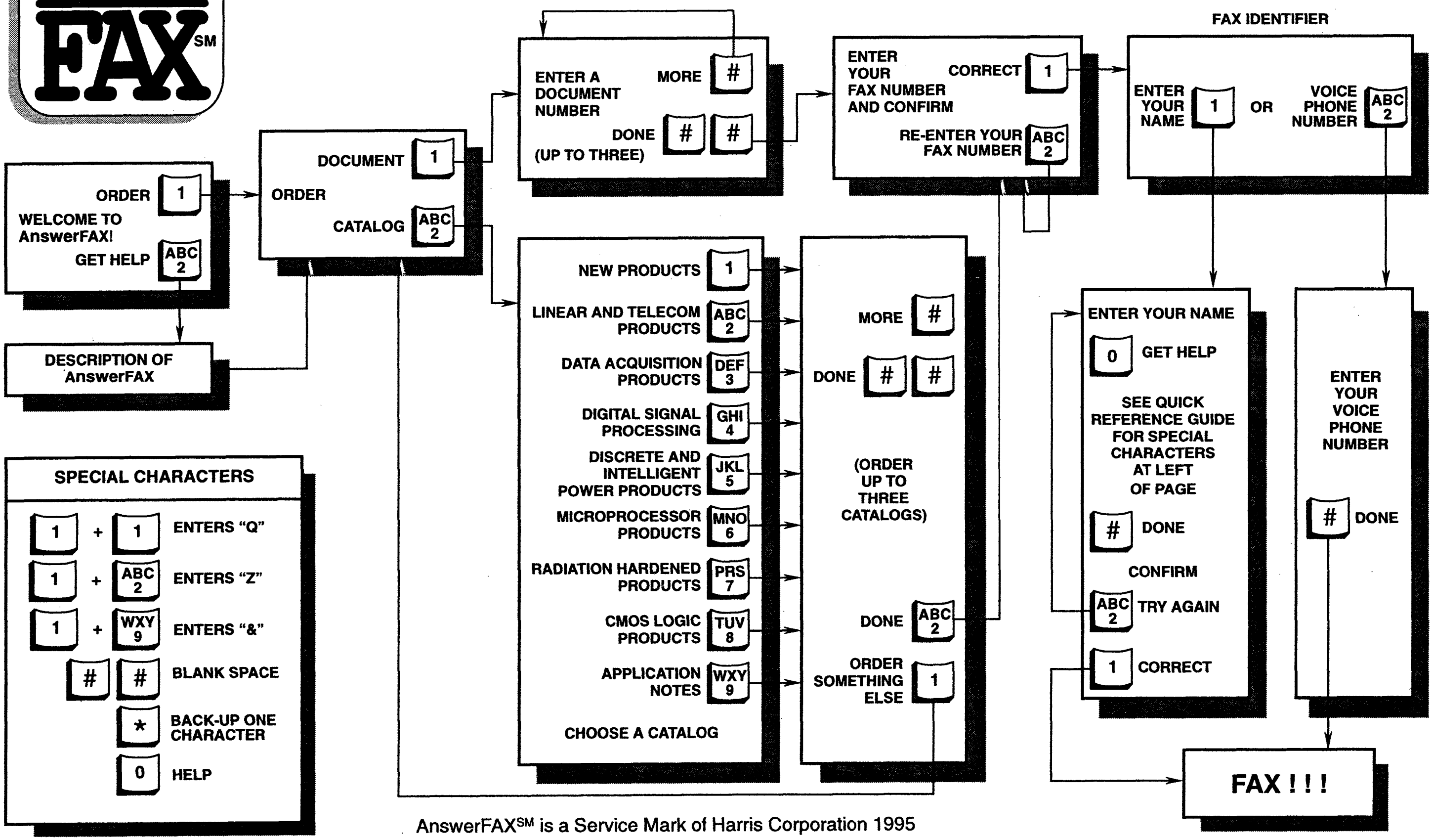

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	DB316	**POWER MOSFET DATABOOK SUPPLEMENT** (1996: 380pp) This databook contains the datasheets of recently introduced products and also updates some of the datasheets in the POWER MOSFET DATABOOK DB223B. These datasheets contain the detailed specification for these products.
	DB235B	**RADIATION HARDENED** (1993: 2,232pp) Harris technologies used include dielectric isolation (DI), Silicon-on-Sapphire (SOS), and Silicon-on-Insulator (SOI). The Harris radiation-hardened products include the CD4000, HCS/HCTS and ACS/ACTS logic families, SRAMs, PROMs, op amps, analog multiplexers, the 80C85/80C86 microprocessor family, analog switches, gate arrays, standard cells and custom devices.
	DB260.2	**CDP6805 CMOS MICROCONTROLLERS & PERIPHERALS** (1995: 436pp) This data book represents the full line of Harris Semiconductor CDP6805 products for commercial applications and supersedes previously published CDP6805 data books under the Harris, GE, RCA or Intersil names.
	DB301B	**DATA ACQUISITION** (1994: 1,104pp) Product specifications on A/D converters (display, integrating, successive approximation, flash); D/A converters, switches, multiplexers, and other products.
	DB302B	**DIGITAL SIGNAL PROCESSING** (1994: 528pp) Product specifications on one-dimensional and two-dimensional filters, signal synthesizers, multipliers, special function devices (such as address sequencers, binary correlators, histogrammer).
	DB303	**MICROPROCESSOR PRODUCTS** (1992: 1,156pp) For commercial and military applications. Product specifications on CMOS microprocessors, peripherals, data communications, and memory ICs.
	DB304.1	**INTELLIGENT POWER ICs** (1994: 946pp) This data book includes a complete set of data sheets for product specifications, application notes with design details for specific applications of Harris products, and a description of the Harris quality and high reliability program.
	DB309.1	**MCT/IGBT/DIODES** (1995: 706pp) This MCT/IGBT/Diodes Databook represents the full line of these products made by Harris Semiconductor Discrete Power Products for commercial applications.
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	DB450.4	**TRANSIENT VOLTAGE SUPPRESSION DEVICES** (1995: 400pp) Product specifications of Harris varistors and surgectors. Also, general informational chapters such as: "Voltage Transients - An Overview," "Transient Suppression - Devices and Principles," "Suppression - Automotive Transients."
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	DB312	**ANALOG MILITARY DATA BOOK SUPPLEMENT** (1994: 432pp) The 1994 Military Data Book Supplement, combined with the 1989 Analog Military Product Data Book, contain detailed technical information on the extensive line of Harris Semiconductor Linear and Data Acquisition products for Military (MIL-STD-883, DESC SMD and JAN) applications and supersedes all previously published Linear and Data Acquisition Military data books. For applications requiring Radiation Hardened products, please refer to the 1993 Harris Radiation Hardened Product Data Book (document #DB235B)
	PSG201.23	**PRODUCT SELECTION GUIDE** (1996: 840pp) Key product information on all Harris Semiconductor devices. Sectioned (Linear, Data Acquisition, Digital Signal Processing, Telecom, Intelligent Power, Discrete Power, Digital Microprocessors and Hi-Rel/Military and Rad Hard) for easy use and includes cross references and alphanumeric part number index.
	SG103	**CMOS LOGIC SELECTION GUIDE** (1994: 288pp) This product selection guide contains technical information on Harris Semiconductor High Speed 54/74 CMOS Logic Integrated Circuits for commercial, industrial and military applications. It covers Harris' High Speed CMOS Logic HC/HCT Series, AC/ACT Series, BiCMOS Interface Logic FCT Series and CMOS Logic CD4000B Series.
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97244	**(General MOSFETs)** AN7244	Understanding Power MOSFETs (4 pages) AN7244.2
97254	**(General MOSFETs)** AN7254	Switching Waveforms Of The L2FET: A 5 Volt Gate-Drive Power MOSFET (8 pages) AN7254.2
97260	**(General MOSFETs)** AN7260	Power MOSFET Switching Waveforms: A New Insight (7 pages) AN7260.2
97332	**(General MOSFETs)** AN7332	The Application Of Conductivity-Modulated Field-Effect Transistors (5 pages) AN7332.1
98610	**(General MOSFETs)** AN8610	Spicing-Up Spice II Software for Power MOSFET Modeling (8 pages)
99209	**(General MOSFETs)** AN9209	A Spice-2 Subcircuit Representation for Power MOSFETs, Using Empirical Methods (4 pages)
99210	**(General MOSFETs)** AN9210	A New PSpice Subcircuit for the Power MOSFET Featuring Global Temperature Options (12 pages)
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797338	**(General MOSFETs & MCTs)** MM PWRDEV	Harris Power MOSFET and MCT Spice Model Library (71 pages) or Call Harris Semiconductor (407) 724-7237 and request by mail. MMPWRDEV.1

For more information, see the AnswerFAX map on page 10-2 and choose catalog item #5, "Discrete and Intelligent Power Products".

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