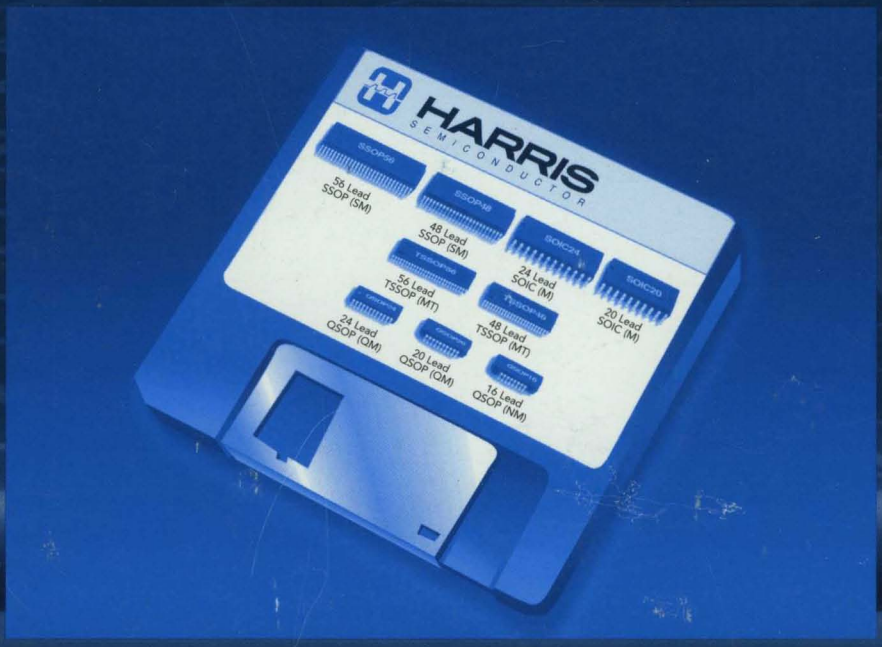
State-of-the Art 3V and 5V CMOS Logic Technology

INTRODUCING LPT/FCT EXPANSION

CMOS Logic From Harris

1997



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Printed in USA, 1/1997

Harris State-of-the-Art 3V and 5V CMOS Logic Technology

Looking for the latest, most advanced technology? Look to the leader in CMOS logic -- Harris Semiconductor. As the inventors of CMOS logic, we continue to bring you the most complete logic solutions.

Harris' new LPT (low power technology) logic family is the most advanced 3.3V CMOS logic family available. Our 3.3V LPT products give you lower power than the LVT family, faster speeds than the LCX family, plus low switching noise. This family also has the distinction of being the industry's first high speed, 3.3V CMPS offering with 5V tolerant I/O. The 5V I/O breakthrough is ideal for system designs requiring transitions from 5V to 3.3V operation voltages, as well as designs with a combination of 5V and 3.3V components.

Harris' expanded FCT portfolio now includes 16-bit devices, more functions and faster speed grades with as low as 3.2ns propagation delay. Our FCT bus interface logic gives you even more advantages over ABT, FAST, and BCT families. With Harris FCT devices you get internal output resisters, advanced packaging options such as QSOP and TSSOP, TTL compatible outputs, low standby current and low switching noise.

The Harris LPT and FCT families supply tremendous value for a broad base of applications including notebook computers, PDAs, other portable electronics, telecommunications, video servers, imaging equipment, graphics workstations, and set top boxes. DRAM and Microprocessors migrate to 3.3V, Interface logic will be necessary to support the new designs

This data book fully describes Harris Semiconductor's LPT and FCT CMOS Logic ICs. It includes a complete set of data sheets for product specifications, application notes and techbriefs with design details for specific applications of Harris products, and a description of the Harris Quality and Reliability program. Section 12, Harris' On-Line Services, describes how our customers have access to the most recent technical updates.

It is our intention to provide you with the most up-to-date information on LPT and FCT products. For complete, current and detailed technical specifications on any Harris devices, please contact the nearest Harris sales representative or distributor office listed in Section 13; or direct literature requests to:

Harris Semiconductor Data Services Department
P.O. Box 883, MS 53-204
Melbourne, FL 32902
Phone: 1-800-442-7747
Fax: 407-724-7240

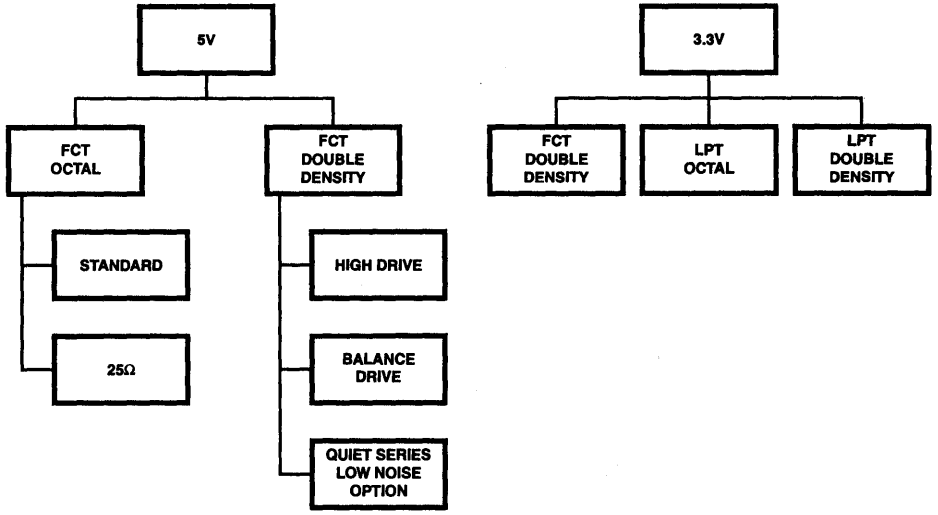
For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (PSG201; ordering information above).

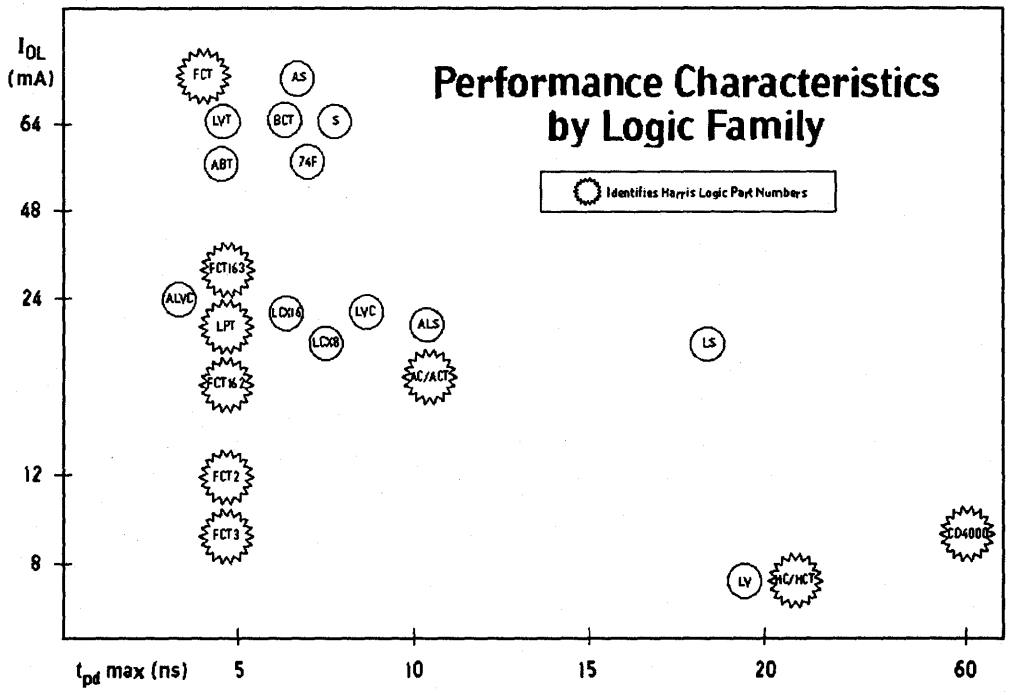
See Section 12 for Harris' On-Line Services

HARRIS SEMICONDUCTOR

LPT/FCT Product Portfolio

BUS INTERFACE FAMILY TREES





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HARRIS IS #1 IN EXPERIENCE

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- **World's Fastest FCT Devices: Propagation Delays as Low as 3.2ns**
- **3.3V Devices with 5V Tolerant I/O**
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- **Multiple Functions and Speed Grades**
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BROADEST CMOS LOGIC PORTFOLIO						
FAMILY	**HARRIS**	**MOTOROLA**	**TI**	**NATIONAL**	**PHILIPS**	**IDT**
HC/HCT	√	√	√	√	√	-
AC/ACT	√	√	√	√	-	-
CD4000	√	√	-	√	√	-
FCT	√	-	-	-	-	√
3 Volt	√	√	√	√	√	√
Military	√	-	√	√	-	√

3V AND 5V LOGIC TECHNOLOGY

FOR COMMERCIAL APPLICATIONS

New Product Selection Trees 1

General Information 2

3.3V LPT CMOS Logic with 5V Tolerant I/O 3

Octal 5V FCT CMOS Logic and 5V FCT with 25Ω Series Resistor 4

Double Density 5V FCT CMOS Logic Balanced and High Drive Output 5

Double Density 5V FCT CMOS Logic Quiet Series 6

3.3V FCT CMOS Logic 7

FCT BiCMOS Logic 8

Application Notes and Tech Briefs 9

Harris Quality and Reliability 10

Packaging Information 11

Harris' On-Line Services 12

Sales Offices 13

CMOS LOGIC 1

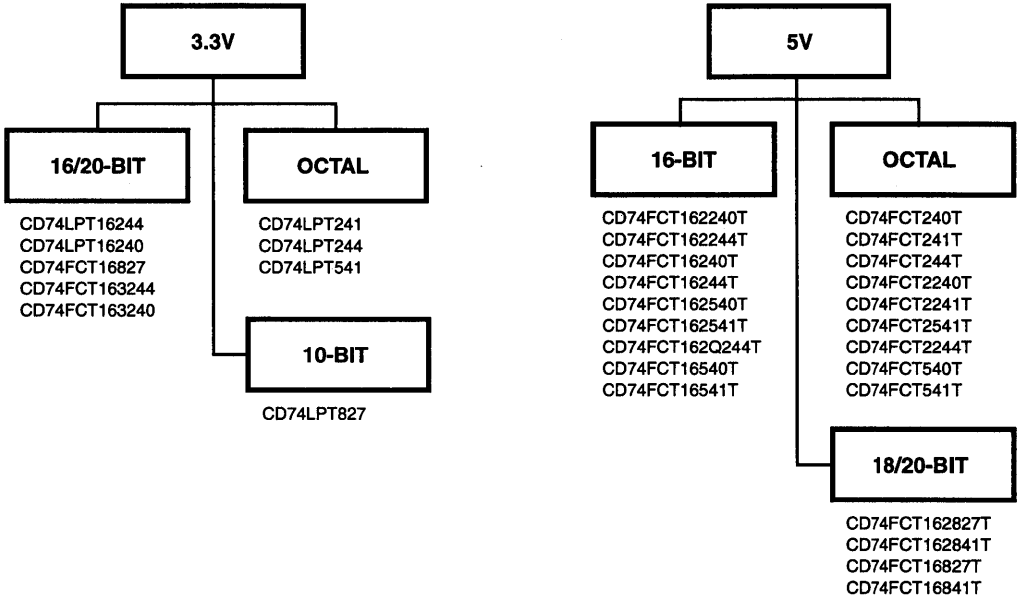
NEW PRODUCT SELECTION TREES

PAGE

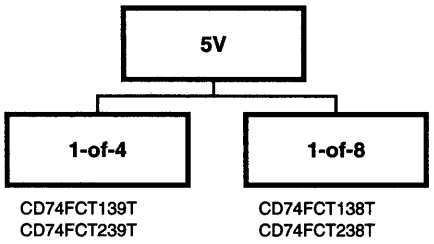
Fast CMOS Selection Trees 1-3
BUFFERS 1-3
DECODERS 1-3
LATCHES 1-4
MULTIPLEXERS 1-4
REGISTERS 1-5
TRANSCEIVERS 1-6

Fast CMOS Selection Trees

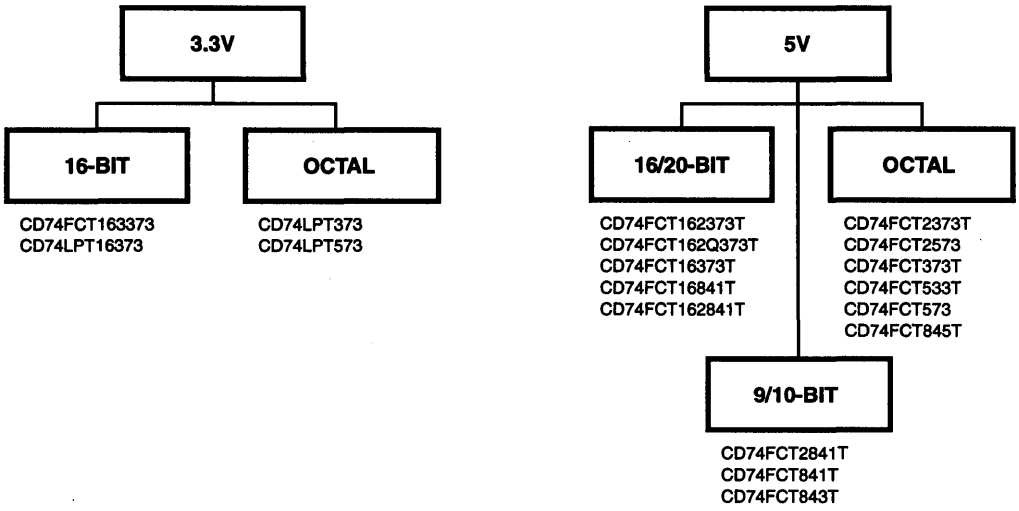
BUFFERS



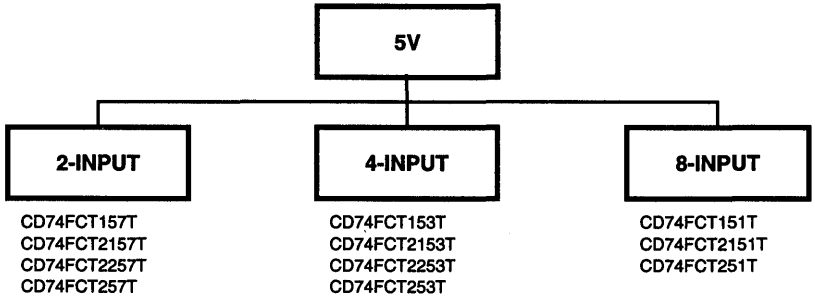
DECODERS



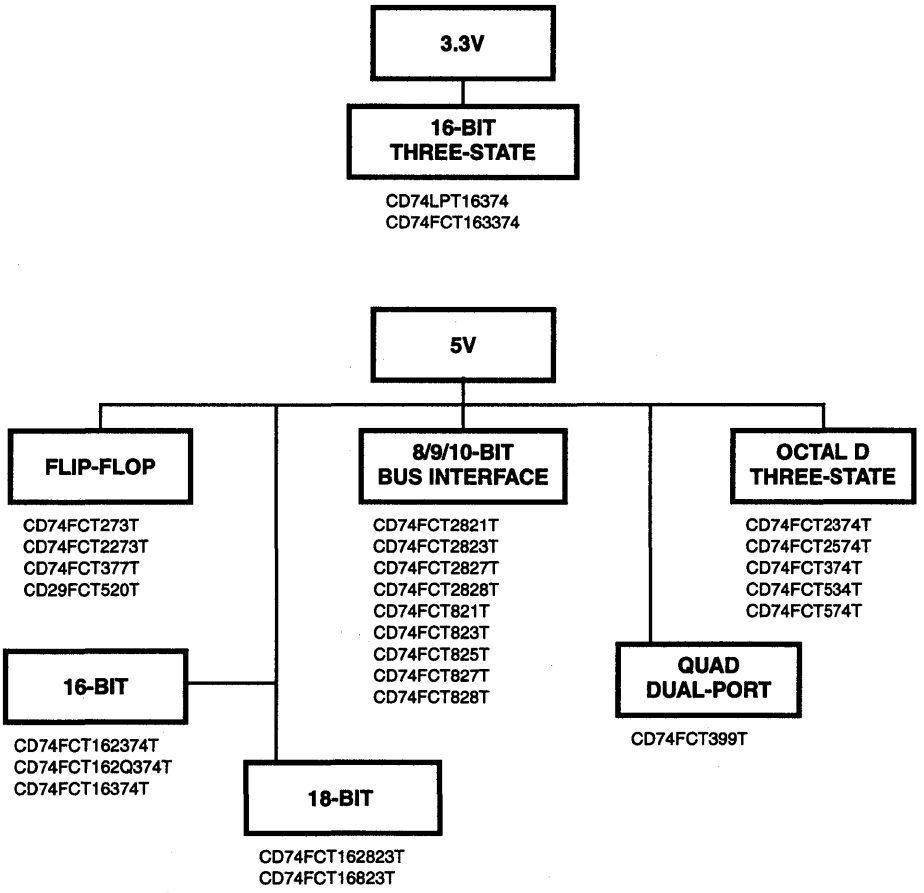
LATCHES



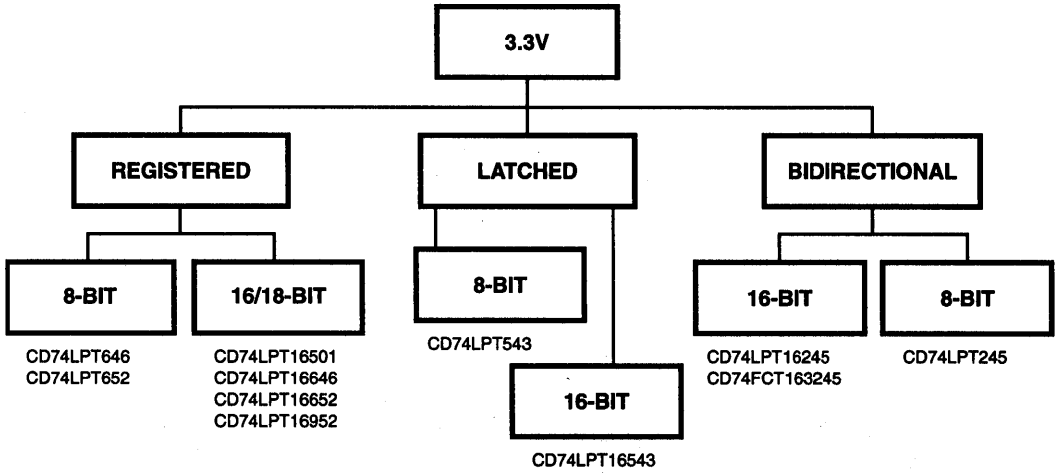
MULTIPLEXERS

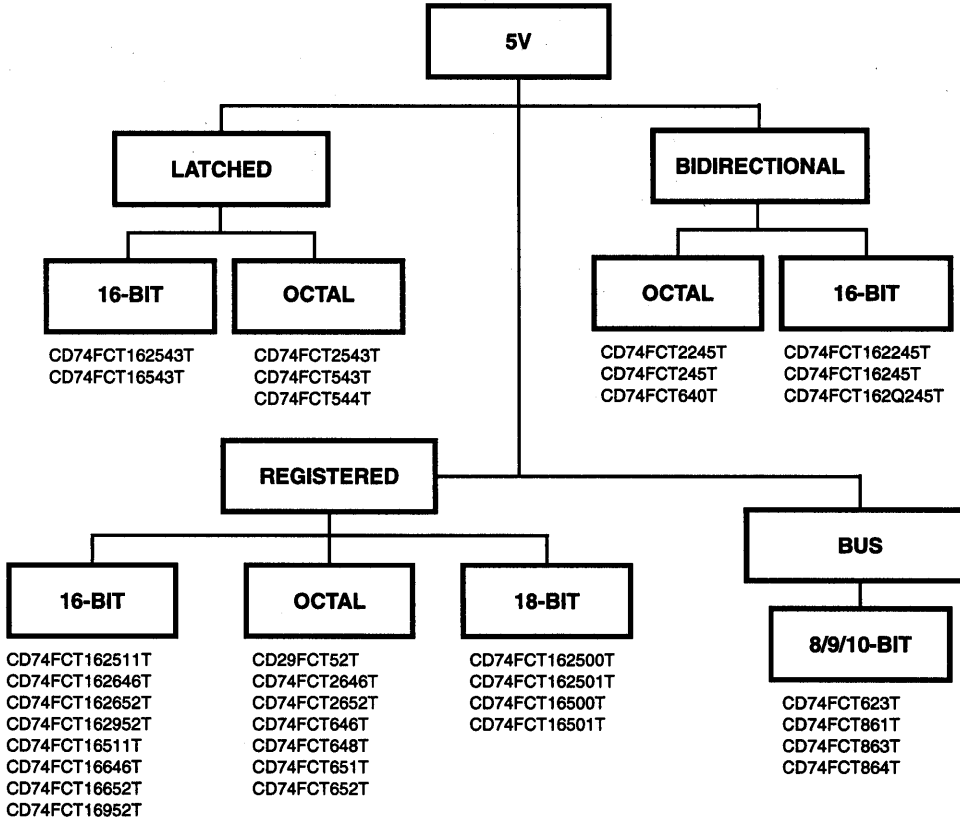


REGISTERS


3.3V
16-BIT THREE-STATE
CD74LPT16374
CD74FCT163374
5V
FLIP-FLOP
CD74FCT273T
CD74FCT2273T
CD74FCT377T
CD29FCT520T
8/9/10-BIT BUS INTERFACE
CD74FCT2821T
CD74FCT2823T
CD74FCT2827T
CD74FCT2828T
CD74FCT821T
CD74FCT823T
CD74FCT825T
CD74FCT827T
CD74FCT828T
OCTAL D THREE-STATE
CD74FCT2374T
CD74FCT2574T
CD74FCT374T
CD74FCT534T
CD74FCT574T
16-BIT
CD74FCT162374T
CD74FCT162Q374T
CD74FCT16374T
18-BIT
CD74FCT162823T
CD74FCT16823T
QUAD DUAL-PORT
CD74FCT399T

TRANSCEIVERS





CMOS LOGIC 2

GENERAL INFORMATION

	PAGE
Alpha Numeric Product Index	2-3
Product Index by Family	2-9
Competitive Nomenclature Comparison Guide	2-13
CMOS Technical Overview	2-15

Alpha Numeric Product Index

		PAGE
CD29FCT520T	Fast CMOS Multilevel Pipeline Register	4-13
CD29FCT52T	Fast CMOS Registered Transceiver	4-7
CD74FCT138T	Fast CMOS 1-of-8 Decoder	4-19
CD74FCT139T	Fast CMOS Dual 1-of-4 Decoder	4-26
CD74FCT151T	8-Input Multiplexer	4-31
CD74FCT153T	High-Speed CMOS Dual 4-Input Multiplexer	4-36
CD74FCT157T	Fast CMOS Quad 2-Input Multiplexer	4-41
CD74FCT162240T	Fast CMOS 16-Bit Buffer/Line Driver	5-3
CD74FCT162244T	Fast CMOS 16-Bit Buffer/Line Driver	5-10
CD74FCT162245T	Fast CMOS 16-Bit Bidirectional Transceiver	5-17
CD74FCT162373T	Fast CMOS 16-Bit Transparent Latch	5-24
CD74FCT162374T	Fast CMOS 16-Bit Register (Three-State)	5-31
CD74FCT16240T	Fast CMOS 16-Bit Buffer/Line Driver	5-3
CD74FCT16244T	Fast CMOS 16-Bit Buffer/Line Driver	5-10
CD74FCT16245T	Fast CMOS 16-Bit Bidirectional Transceiver	5-17
CD74FCT162500T	Fast CMOS 18-Bit Registered Transceiver	5-38
CD74FCT162501T	Fast CMOS 18-Bit Registered Transceiver	5-44
CD74FCT162511T	Fast CMOS 16-Bit Registered/Latched Transceiver with Parity	5-52
CD74FCT162540T	Fast CMOS 16-Bit Buffer/Line Driver	5-61
CD74FCT162541T	Fast CMOS 16-Bit Octal Buffer/Line Driver	5-68
CD74FCT162543T	Fast CMOS 16-Bit Latched Transceiver	5-75
CD74FCT162646T	Fast CMOS 16-Bit Registered Transceiver	5-82
CD74FCT162652T	Fast CMOS 16-Bit Registered Transceiver	5-90
CD74FCT162823T	Fast CMOS 18-Bit Register	5-97

Alpha Numeric Product Index (Continued)

		PAGE
CD74FCT162827T	Fast CMOS 20-Bit Buffer	5-104
CD74FCT162841T	Fast CMOS 20-Bit Transparent Latch	5-111
CD74FCT162952T	Fast CMOS 16-Bit Registered Transceiver	5-117
CD74FCT162Q244T	Fast, Low Noise CMOS 16-Bit Buffer/Line Driver	6-3
CD74FCT162Q245T	Fast CMOS 16-Bit Bidirectional Transceiver	6-8
CD74FCT162Q373T	Fast CMOS 16-Bit Transparent Latch	6-14
CD74FCT162Q374T	Fast CMOS 16-Bit Register (Three-State)	6-20
CD74FCT163240	Fast CMOS 3.3V 16-Bit Octal Buffer/Line Driver	7-3
CD74FCT163244	Fast CMOS 3.3V 16-Bit Buffer/Line Driver	7-9
CD74FCT163245	Fast CMOS 3.3V 16-Bit Bidirectional Transceiver	7-15
CD74FCT163373	Fast CMOS 3.3V 16-Bit Transparent Latch	7-21
CD74FCT163374	Fast CMOS CMOS 3.3V 6-Bit Register (Three-State)	7-27
CD74FCT16373T	Fast CMOS 16-Bit Transparent Latch	5-24
CD74FCT16374T	Fast CMOS 16-Bit Register (Three-State)	5-31
CD74FCT16500T	Fast CMOS 18-Bit Registered Transceiver	5-38
CD74FCT16501T	Fast CMOS 18-Bit Registered Transceiver	5-44
CD74FCT16511T	Fast CMOS 16-Bit Registered/Latched Transceiver with Parity	5-52
CD74FCT16540T	Fast CMOS 16-Bit Buffer/Line Driver	5-61
CD74FCT16541T	Fast CMOS 16-Bit Octal Buffer/Line Driver	5-68
CD74FCT16543T	Fast CMOS 16-Bit Latched Transceiver	5-75
CD74FCT16646T	Fast CMOS 16-Bit Registered Transceiver	5-82
CD74FCT16652T	Fast CMOS 16-Bit Registered Transceiver	5-90
CD74FCT16823T	Fast CMOS 18-Bit Register	5-97
CD74FCT16827T	Fast CMOS 20-Bit Buffer	5-104

Alpha Numeric Product Index (Continued)

		PAGE
CD74FCT16841T	Fast CMOS 20-Bit Transparent Latch	5-111
CD74FCT16952T	Fast CMOS 16-Bit Registered Transceiver	5-117
CD74FCT2151T	Fast CMOS 8-Input Multiplexer	4-31
CD74FCT2153T	High-Speed CMOS Dual 4-Input Multiplexer	4-36
CD74FCT2157T	Fast CMOS Quad 2-Input Multiplexer	4-41
CD74FCT2240T	Fast CMOS Octal Buffer and Line Driver	4-46
CD74FCT2241T	Fast CMOS Octal Buffer and Line Driver	4-46
CD74FCT2244T	Fast CMOS Octal Buffer and Line Driver	4-46
CD74FCT2245T	Fast CMOS Octal Bidirectional Transceiver	4-53
CD74FCT2253T	High-Speed CMOS Dual 4-Input Multiplexer	4-36
CD74FCT2257T	Fast CMOS Quad 2-Input Multiplexer	4-41
CD74FCT2273T	Fast CMOS Octal D Flip-Flop with Master Reset	4-59
CD74FCT2373T	Fast CMOS Octal Transparent Latch	4-62
CD74FCT2374T	Fast CMOS Octal D Register (Three-State)	4-69
CD74FCT238T	Fast CMOS 1-of-8 Decoder	4-19
CD74FCT239T	Fast CMOS Dual 1-of-4 Decoder	4-26
CD74FCT240T	Fast CMOS Octal Buffer and Line Driver	4-46
CD74FCT241T	Fast CMOS Octal Buffer and Line Driver	4-46
CD74FCT244T	Fast CMOS Octal Buffer and Line Driver	4-46
CD74FCT245T	Fast CMOS Octal Bidirectional Transceiver	4-53
CD74FCT251T	Fast CMOS 8-Input Multiplexer	4-31
CD74FCT253T	High-Speed CMOS Dual 4-Input Multiplexer	4-36
CD74FCT2541T	Fast CMOS Octal Buffer and Line Driver	4-46
CD74FCT2543T	Fast CMOS Latched Transceiver	4-90

Alpha Numeric Product Index (Continued)

		PAGE
CD74FCT2573T	Fast CMOS Octal Transparent Latch	4-62
CD74FCT2574T	Fast CMOS Octal D Register (Three-State)	4-69
CD74FCT257T	Fast CMOS Quad 2-Input Multiplexer	4-41
CD74FCT2646T	Fast CMOS Octal Registered Transceiver	4-101
CD74FCT2652T	Fast CMOS Octal Registered Transceiver	4-101
CD74FCT273T	Fast CMOS Octal D Flip-Flop with Master Reset	4-59
CD74FCT2821T	Fast CMOS Bus Interface Register	4-110
CD74FCT2823T	Fast CMOS Bus Interface Register	4-110
CD74FCT2827T	Fast CMOS 10-Bit Buffer	4-117
CD74FCT2828T	Fast CMOS 10-Bit Buffer	4-117
CD74FCT2841T	Fast CMOS Bus Interface Latch	4-123
CD74FCT373T	Fast CMOS Octal Transparent Latch	4-62
CD74FCT374T	Fast CMOS Octal D Register (Three-State)	4-69
CD74FCT377T	Fast CMOS Octal D Flip-Flop with Clock Enable	4-75
CD74FCT399T	Fast CMOS Quad Dual-Port Register	4-80
CD74FCT521T	Fast CMOS 8-Bit Identity Comparator	4-85
CD74FCT533T	Fast CMOS Octal Transparent Latch	4-62
CD74FCT534T	Fast CMOS Octal D Register (Three-State)	4-69
CD74FCT540T	Fast CMOS Octal Buffer and Line Driver	4-46
CD74FCT541T	Fast CMOS Octal Buffer and Line Driver	4-46
CD74FCT543T	Fast CMOS Latched Transceiver	4-90
CD74FCT544T	Fast CMOS Latched Transceiver	4-90
CD74FCT573T	Fast CMOS Octal Transparent Latch	4-62
CD74FCT574T	Fast CMOS Octal D Register (Three-State)	4-69

Alpha Numeric Product Index (Continued)

		PAGE
CD74FCT623T	Fast CMOS Octal Bus Transceiver (Three-State)	4-96
CD74FCT640T	Fast CMOS Octal Bidirectional Transceiver	4-53
CD74FCT646T	Fast CMOS Octal Registered Transceiver	4-101
CD74FCT648T	Fast CMOS Octal Registered Transceiver	4-101
CD74FCT651T	Fast CMOS Octal Registered Transceiver	4-101
CD74FCT652T	Fast CMOS Octal Registered Transceiver	4-101
CD74FCT821T	Fast CMOS Bus Interface Register	4-110
CD74FCT823T	Fast CMOS Bus Interface Register	4-110
CD74FCT825T	Fast CMOS Bus Interface Register	4-110
CD74FCT827T	Fast CMOS 10-Bit Buffer	4-117
CD74FCT828T	Fast CMOS 10-Bit Buffer	4-117
CD74FCT841T	Fast CMOS Bus Interface Latch	4-123
CD74FCT843T	Fast CMOS Bus Interface Latch	4-123
CD74FCT845T	Fast CMOS Bus Interface Latch	4-123
CD74FCT861T	Fast CMOS Bus Transceiver	4-129
CD74FCT863T	Fast CMOS Bus Transceiver	4-129
CD74FCT864T	Fast CMOS Bus Transceiver	4-129
CD74LPT16240	Fast CMOS 3.3V 16-Bit Buffer/Line Driver	3-2
CD74LPT16244	Fast CMOS 3.3V 16-Bit Buffer/Line Driver	3-8
CD74LPT16245	Fast CMOS 3.3V 16-Bit Bidirectional Transceiver	3-14
CD74LPT16373	Fast CMOS 3.3V 16-Bit Transparent Latch	3-20
CD74LPT16374	Fast CMOS 3.3V 16-Bit Register (Three-State)	3-26
CD74LPT16501	Fast CMOS 18-Bit Registered Transceiver	3-32
CD74LPT16543	Fast CMOS 16-Bit Latched Transceiver	3-40

Alpha Numeric Product Index (Continued)

		PAGE
CD74LPT16646	Fast CMOS 3.3V 16-Bit Registered Transceiver	3-46
CD74LPT16652	Fast CMOS 16-Bit Registered Transceiver	3-53
CD74LPT16827	Fast CMOS 3.3V 20-Bit Buffer	3-60
CD74LPT16952	Fast CMOS 3.3V 16-Bit Registered Transceiver	3-66
CD74LPT241	Fast CMOS 3.3V 8-Bit Buffer/Line Driver	3-72
CD74LPT244	Fast CMOS 3.3V 8-Bit Buffer/Line Driver	3-78
CD74LPT245	Fast CMOS 3.3V 8-Bit Bidirectional Transceiver	3-84
CD74LPT373	Fast CMOS 3.3V 8-Bit Transparent Latches	3-90
CD74LPT541	Fast CMOS 3.3V 8-Bit Buffer/Line Driver	3-96
CD74LPT543	Fast CMOS 3.3V 8-Bit Latched Transceiver	3-102
CD74LPT573	Fast CMOS 3.3V 8-Bit Transparent Latch	3-108
CD74LPT646	Fast CMOS 3.3V 8-Bit Registered Transceiver	3-114
CD74LPT652	Fast CMOS 3.3V 8-Bit Registered Transceiver	3-114
CD74LPT827	Fast CMOS 3.3V 10-Bit Buffer	3-122

Product Index by Family

PAGE

3.3V FCT CMOS LOGIC

CD74FCT163240	Fast CMOS 3.3V 16-Bit Octal Buffer/Line Driver	7-3
CD74FCT163244	Fast CMOS 3.3V 16-Bit Buffer/Line Driver	7-9
CD74FCT163245	Fast CMOS 3.3V 16-Bit Bidirectional Transceiver	7-15
CD74FCT163373	Fast CMOS 3.3V 16-Bit Transparent Latch	7-21
CD74FCT163374	Fast CMOS CMOS 3.3V 6-Bit Register (Three-State)	7-27

3.3V LPT CMOS LOGIC WITH 5V TOLERANT I/O

CD74LPT16240	Fast CMOS 3.3V 16-Bit Buffer/Line Driver	3-3
CD74LPT16244	Fast CMOS 3.3V 16-Bit Buffer/Line Driver	3-9
CD74LPT16245	Fast CMOS 3.3V 16-Bit Bidirectional Transceiver	3-15
CD74LPT16373	Fast CMOS 3.3V 16-Bit Transparent Latch	3-21
CD74LPT16374	Fast CMOS 3.3V 16-Bit Register (Three-State)	3-27
CD74LPT16501	Fast CMOS 18-Bit Registered Transceiver	3-33
CD74LPT16543	Fast CMOS 16-Bit Latched Transceiver	3-41
CD74LPT16646	Fast CMOS 3.3V 16-Bit Registered Transceiver	3-47
CD74LPT16652	Fast CMOS 16-Bit Registered Transceiver	3-54
CD74LPT16827	Fast CMOS 3.3V 20-Bit Buffer	3-61
CD74LPT16952	Fast CMOS 3.3V 16-Bit Registered Transceiver	3-67
CD74LPT241	Fast CMOS 3.3V 8-Bit Buffer/Line Driver	3-73
CD74LPT244	Fast CMOS 3.3V 8-Bit Buffer/Line Driver	3-79
CD74LPT245	Fast CMOS 3.3V 8-Bit Bidirectional Transceiver	3-85
CD74LPT373	Fast CMOS 3.3V 8-Bit Transparent Latch	3-91
CD74LPT541	Fast CMOS 3.3V 8-Bit Buffer/Line Driver	3-97
CD74LPT543	Fast CMOS 3.3V 8-Bit Latched Transceiver	3-103
CD74LPT573	Fast CMOS 3.3V 8-Bit Transparent Latch	3-109
CD74LPT646, CD74LPT652	Fast CMOS 3.3V 8-Bit Registered Transceivers	3-115
CD74LPT827	Fast CMOS 3.3V 10-Bit Buffer	3-123

DOUBLE DENSITY 5V FCT CMOS LOGIC BALANCED AND HIGH DRIVE OUTPUT

CD74FCT16240T, CD74FCT162240T	Fast CMOS 16-Bit Buffer/Line Drivers	5-3
CD74FCT16244T, CD74FCT162244T	Fast CMOS 16-Bit Buffer/Line Drivers	5-10
CD74FCT16245T, CD74FCT162245T	Fast CMOS 16-Bit Bidirectional Transceivers	5-17
CD74FCT16373T, CD74FCT162373T	Fast CMOS 16-Bit Transparent Latches	5-24
CD74FCT16374T, CD74FCT162374T	Fast CMOS 16-Bit Registers (Three-State)	5-31

Product Index by Family (Continued)

		PAGE
CD74FCT16500T, CD74FCT162500T	Fast CMOS 18-Bit Registered Transceivers	5-38
CD74FCT16501T, CD74FCT162501T	Fast CMOS 18-Bit Registered Transceivers	5-44
CD74FCT16511T, CD74FCT162511T	Fast CMOS 16-Bit Registered/Latched Transceivers with Parity	5-51
CD74FCT16540T, CD74FCT162540T	Fast CMOS 16-Bit Buffer/Line Drivers	5-60
CD74FCT16541T, CD74FCT162541T	Fast CMOS 16-Bit Octal Buffer/Line Drivers	5-67
CD74FCT16543T, CD74FCT162543T	Fast CMOS 16-Bit Latched Transceivers	5-74
CD74FCT16646T, CD74FCT162646T	Fast CMOS 16-Bit Registered Transceivers	5-81
CD74FCT16652T, CD74FCT162652T	Fast CMOS 16-Bit Registered Transceivers	5-89
CD74FCT16823T, CD74FCT162823T	Fast CMOS 18-Bit Registers	5-96
CD74FCT16827T, CD74FCT162827T	Fast CMOS 20-Bit Buffers	5-103
CD74FCT16841T, CD74FCT162841T	Fast CMOS 20-Bit Transparent Latches	5-110
CD74FCT16952T, CD74FCT162952T	Fast CMOS 16-Bit Registered Transceivers	5-116

DOUBLE DENSITY 5V FCT CMOS LOGIC QUIET SERIES

CD74FCT162Q244T	Fast, Low Noise CMOS 16-Bit Buffer/Line Driver	6-3
CD74FCT162Q245T	Fast CMOS 16-Bit Bidirectional Transceiver	6-8
CD74FCT162Q373T	Fast CMOS 16-Bit Transparent Latch	6-14
CD74FCT162Q374T	Fast CMOS 16-Bit Register (Three-State)	6-20

FCT BiCMOS LOGIC

CD74FCT240, CD74FCT240AT, CD74FCT244, CD74FCT244AT	BiCMOS FCT Interface Logic, Octal Buffers/Line Drivers, Three-State	8-23
CD54FCT245, CD74FCT245	BiCMOS FCT Interface Logic, Octal-Bus Tranceivers, Three-State	8-28
CD74FCT273	BiCMOS FCT Interface Logic, Octal D Flip-Flop with Reset	8-33
CD74FCT373, CD74FCT373AT	BiCMOS FCT Interface Logic, Octal Transparent Latches, Three-State	8-38
CD74FCT374	BiCMOS FCT Interface Logic, Octal D-Type Flip-Flop, Three-State	8-43
CD74FCT540, CD74FCT541	BiCMOS FCT Interface Logic, Octal Buffers/Line Drivers, Three-State	8-48
CD74FCT543	BiCMOS FCT Interface Logic, Octal Register/Transceiver, Three-State	8-53

Product Index by Family (Continued)

		PAGE
CD74FCT564, CD74FCT574	BiCMOS FCT Interface Logic, Octal D-Type Flip-Flops, Three-State	8-58
CD74FCT573, CD74FCT573AT	BiCMOS FCT Interface Logic, Octal Transparent Latches, Three-State	8-62
CD74FCT646	BiCMOS FCT Interface Logic, Octal Bus Transceiver/Register, Three-State	8-67
CD74FCT651, CD74FCT652	BiCMOS FCT Interface Logic, Octal Bus Transceivers/Registers, Three-State	8-72
CD74FCT653, CD74FCT654	FCT Interface Logic, Octal Bus Transceivers/ Registers, Open Drain (A Side), Three-State (B Side)	8-77
CD74FCT821A, CD74FCT822A	BiCMOS FCT Interface Logic, 10- Bit D-Type Flip-Flops, Three-State	8-83
CD74FCT823A, CD74FCT824A	BiCMOS FCT Interface Logic, 9-Bit D-Type Flip-Flops, Three-State	8-88
CD74FCT841A, CD74FCT842A	BiCMOS FCT Interface Logic, 10-Bit Transparent Latches, Three-State	8-93
CD74FCT843A, CD74FCT844A	BiCMOS FCT Interface Logic, 9-Bit Transparent Latches, Three-State	8-98
CD74FCT861A	BiCMOS FCT Interface Logic, 10-Bit Bus Transceiver, Three-State	8-103
CD74FCT863A	BiCMOS FCT Interface Logic, 9-Bit Bus Transceiver, Three-State	8-108

OCTAL 5V FCT CMOS LOGIC AND 5V FCT WITH 25Ω SERIES RESISTOR

CD29FCT52T	Fast CMOS Registered Transceiver	4-7
CD29FCT520T	Fast CMOS Multilevel Pipeline Register	4-13
CD74FCT138T, CD74FCT238T	Fast CMOS 1-of-8 Decoders	4-18
CD74FCT139T, CD74FCT239T	Fast CMOS Dual 1-of-4 Decoders	4-24
CD74FCT151T, CD74FCT251T, CD74FCT2151T	Fast CMOS 8-Input Multiplexers	4-29
CD74FCT153T, CD74FCT253T, CD74FCT2153T, CD74FCT2253T	High-Speed CMOS Dual 4-Input Multiplexers	4-34
CD74FCT157T, CD74FCT257T, CD74FCT2157T, CD74FCT2257T	Fast CMOS Quad 2-Input Multiplexers	4-39
CD74FCT240T, CD74FCT241T, CD74FCT244T, CD74FCT540T, CD74FCT541T, CD74FCT2240T, CD74FCT2241T, CD74FCT2244T, CD74FCT2541T	Fast CMOS Octal Buffer and Line Drivers	4-44

Product Index by Family (Continued)

		PAGE
CD74FCT245T, CD74FCT640T, CD74FCT2245T	Fast CMOS Octal Bidirectional Transceivers	4-51
CD74FCT273T, CD74FCT2273T	Fast CMOS Octal D Flip-Flops with Master Reset	4-57
CD74FCT373T, CD74FCT533T, CD74FCT573T, CD74FCT2373T, CD74FCT2573T	Fast CMOS Octal Transparent Latches	4-62
CD74FCT374T, CD74FCT534T, CD74FCT574T, CD74FCT2374T, CD74FCT2574T	Fast CMOS Octal D Registers (Three-State)	4-69
CD74FCT377T	Fast CMOS Octal D Flip-Flop with Clock Enable	4-75
CD74FCT399T	Fast CMOS Quad Dual-Port Register	4-80
CD74FCT521T	Fast CMOS 8-Bit Identity Comparator	4-85
CD74FCT543T, CD74FCT544T, CD74FCT2543T	Fast CMOS Latched Transceivers	4-90
CD74FCT623T	Fast CMOS Octal Bus Transceiver (Three-State)	4-96
CD74FCT646T, CD74FCT648T, CD74FCT651T, CD74FCT652T, CD74FCT2646T, CD74FCT2652T	Fast CMOS Octal Registered Transceivers	4-101
CD74FCT821T, CD74FCT823T, CD74FCT825T, CD74FCT2821T, CD74FCT2823T	Fast CMOS Bus Interface Registers	4-110
CD74FCT827T, CD74FCT828T, CD74FCT2827T, CD74FCT2828T	Fast CMOS 10-Bit Buffers	4-117
CD74FCT841T, CD74FCT843T, CD74FCT845T, CD74FCT2841T	Fast CMOS Bus Interface Latches	4-123
CD74FCT861T, CD74FCT863T, CD74FCT864T	Fast CMOS Bus Transceivers	4-129

Competitive Nomenclature Comparison Guide

HARRIS CD (FCT, LPT) NOMENCLATURE

CD XX XXX XXXXXX X X X XX

Prefix Designation for Harris CMOS Digital Logic IC

TEMPERATURE RANGE
29/54/74: Refer to Individual Data Sheets for Temperature Range

LOGIC LEVEL
FCT: Bus Interface 5.0V and 3.3V Family
LPT: Low Power Technology 3.3V Family

TYPE DESIGNATION
Up to 6 Digits
XXX: 8-Bit/9-Bit/10-Bit
16XXX: 16-Bit/18-Bit/20-Bit
162XXX: 16-Bit with Balanced or High Drive Output
162QXXX: 16-Bit, 25Ω Quiet Series
163XXX: 16-Bit 3.3V FCT
2XXX: 25Ω Series Output Resistor

SPEED GRADE
Blank: Lowest Speed
A:
B:
C:
D:
E: Highest Speed
NOTE: Refer to Individual Data Sheet for Speed Grade Detail.

OUTPUT VOLTAGE
T: TTL Output Levels
Blank: Non-TTL Output Levels

PACKAGE DESIGNATOR
E: Dual-In-Line Plastic (PDIP)
EN: Narrow Dual-In-Line Plastic
H: Chip
M: 300 mil, Small Outline Plastic (SOIC)
NM: 150 mil, Small Outline Plastic (SOIC)
MT: Thin Shrink Small Outline (TSSOP)
QM: 150 mil, Shrink Small Outline Plastic (SSOP/QSOP)
SM: 209 or 300 mil, Shrink Small Outline Plastic (SSOP)

NOTE: The E and EN package options are only offered in BiCMOS technology for FCT products.

PACK DESIGNATOR
Blank: Tube
96: Tape and Reel

LPT LOGIC COMPETITIVE NOMENCLATURE

MANUFACTURER ID	TEMPERATURE	FAMILY	PART NUMBER	SPEED	OUTPUT LEVEL	PACKAGE
NATIONAL						
Blank	74	LCX	XXX 16XXX	Blank	Blank	N = PDIP WM = 300 mil SOIC QSC = QSOP MEA = 48 Ld SSOP MTD = 48 Ld TSSOP Blank = Tube X = Tape and Reel
TEXAS INSTRUMENTS (TI)						
SN	74	LVT	XXX 16XXX 162XXX	Blank A	Blank	N = PDIP DW = 300 mil SOIC DL = 48 Ld SSOP PW = 20 Ld TSSOP DGG = 48 Ld TSSOP Blank = Tube R = Tape and Reel
PERICOM						
PI	74	LPT	XXX 16XXX	Blank A C	Blank	P = PDIP S = 300 mil SOIC W = 150 mil SOIC Q = QSOP V = SSOP A = TSSOP Blank = Tube 96 = Tape and Reel

FCT LOGIC COMPETITIVE NOMENCLATURE

MANUFACTURER ID	TEMPERATURE	FAMILY	PART NUMBER	SPEED	OUTPUT LEVEL	PACKAGE
IDT						
IDT	74	FCT	XXX 16XXX 162XXX 163XXX 2XXX	Blank A B C D	T	P = PDIP SO = SOIC Q = QSOP PV = SSOP PA = TSSOP Blank = Tube X = Tape and Reel
CYPRESS						
CY	74	FCT	XXX 16XXX 162XXX 163XXX 2XXX	Blank A B C D	T	P = PDIP SO = SOIC Q = QSOP PV = SSOP PA = TSSOP Blank = Tube X = Tape and Reel
QSI						
QS	74	FCT	XXX 16XXX 162XXX 163XXX 2XXX	Blank A B C D	T	P = PDIP SO = 300 mil SOIC S1 = 150 mil SOIC Q = QSOP PV = SSOP PA = TSSOP Blank = Tube
PERICOM						
PI	74	FCT	XXX 16XXX 162XXX 163XXX 2XXX	Blank A B C D E	T	P = PDIP S = 300 mil SOIC W = 150 mil SOIC Q = QSOP V = SSOP A = TSSOP Blank = Tube X = Tape and Reel

CMOS Technical Overview

Technical Overview

New Harris Bus Interface Families

- Six New 5V or 3.3V .....74FCTXXXX Families
- Two New 3.3V .....74LPTXXXX Families

Definition of Six New FCT Logic Families

Octal 5V FCT bus interface Logic - low power direct High Drive replacements for high power FAST™ and new higher speed grades (A-D) for today's higher speed systems.

Octal 5V FCT bus interface Logic with a 25Ω output series R to match PCB trace impedance and reduce switching transients.

Double Density (16-bit) 5V FCT High Drive bus interface Logic to replace Octals in 16 through 64-bit systems at FAST™ speed; speed grades up to E (3.2ns, industry's fastest) are available to accommodate today's higher bus speeds.

Double Density 5V FCT Balanced (±24mA) Drive for reduced switching noise and ground bounce in 16 through 64-bit bus interface applications; speed grades up to E (3.2ns) are available.

Double Density QUIET 5V FCT featuring very quiet switching (0.5V ground bounce) by limiting dynamic output current. Parts also have designed-in Bus Hold and speed grades to D (3.2ns). Quiet switching and Bus Hold simplifies bus design and increases system performance reliability.

3.3V Double Density FCT designed exclusively for lower power 3.3V bus interface saving nearly 7X in power consumption compared to 5V equivalents; noise is correspondingly reduced at 5V. This is an LVC™ replacement family option for internal PCB Bus Interface.

Definition of Two New 3.3V LPT Logic Families

Octal 3.3V LPT Bus Interface logic featuring balanced drive (±24mA); a LVC™ Replacement Family.

Double Density 3.3V LPT Bus Interface featuring balanced drive (±24mA); a LVC™ Replacement Family.

Technical Features of Families

Octal 5V FCT-T Logic Products

- Meets JEDEC Std. No. 18A Std. for Description of 54/74 FCTXXX, FAST™ CMOS TTL Compatible Logic
- Modern 0.8 micron CMOS Process
- N Well, Poly Gate, Field Implant
- Double Level Planerized Metal
- 0.55 Micro-Meter L Effective for Smaller High Drive Output Geometry
- Suffix "T" Means Reduced Power/Noise 3V-3.5V Output Swing - Just Like TTL FAST™.
- High Drive 64mA/15mA (I_{OL}/I_{OH}) for Bus Interface Types; 48mA/15mA for Other Logic Types
- 100µA quiescent current in power down mode
- 200mV Typical Input Hysteresis
- I/O Capacitance of Typically 6pF/8pF
- Only 10mW/MHz Typical Operating Power for Each Output Bit Toggling
- Typical Propagation Delay ("D"-grade) of 3.44ns at 25°C; Limit is 3.8ns
- Low Output Pin Skew (FCT245T)
  - Pin-to-Pin
  - - 0.25ns Typical
  - t_{PLH}/t_{PHL}
  - - 0.1ns Typical
- Surface Mount SOIC and QSOP Packages Reduce PCB's Spare and Have Nearly 4:1 Reduced Ground Pin Inductance (Compared To DIPS) Resulting In 50% Reduced Ground Bounce and Switching Edge Ringing.
- "HOT PLUG" or Live Insertion of PCB's Containing FCT-T as the Bus Drivers or I/O Ports is a Major Plus. See Application Note AN9692.
- Ground Bounce is 1V-1.5V Peak - Modest for 3.6ns Delay Devices with 64mA Sink Current. See Application Note AN9646.

Comparing Harris FCT-T to Other Families That Have Similar FAST™ Replacement Functions and Specifications is Broken Down into 2 Classes.

- Four CMOS FCT Competitor Families, 3 of these 4 are in the Modern FCT-T High Speed Area. Harris "D" Speed is Out Front in Speed.
- Two FAST™ Replacement Power BiCMOS Families; ABT and BCT are Illustrated in Table 1. Compatibly ACT and BCT are Much Higher Power and Do Not Have the Expanded Speed Grades to Compete with Harris FCT-T.

FAST™ is a trademark of Fairchild Semiconductor.

TABLE 1. 5V LOGIC FAMILIES COMPARISON

FAMILY/FEATURES	ABT 245	BCT 245	FCT245	FCT ADVANTAGES
Technology	0.8µm BiCMOS	BiCMOS	0.8µm CMOS	More Advanced/Low Power CMOS
Operating Voltage	4.5V to 5.5V	4.5V to 5.5V	4.5V to 5.5V	More Advanced/Low Power CMOS
Operating Temp T_A	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C	More Advanced/Low Power CMOS
Speed (ns) 5.0 ± 0.5V	4.6	7	7/4.6/4.1/3.8 (Note 1)	Fastest, Multiple Speed Trading Performance with Cost
Input Hysteresis	No	No	Yes	Better Response to Slow Changing Signals
Output	TTL	TTL	TTL	Compatible
Drive ($-I_{OH}/I_{OL}$)	-32/64mA	-15/64mA	-15/64mA	Sufficient
I_{CC} Standby	32mA (Outputs Low)	90mA (Outputs Low)	100µA	Lowest Power
V_{LOP} Noise	<1V	<1V	<0.8V	Lowest with FCT2XXX
Package Offerings	DIP, SO, SSOP	DIP, SO	SO, QSOP, TQSOP, TSSOP	More and Small Packages: QSOP, MT, and TSSOP QM
Suppliers	TI, Phillips Hitachi	TI	Harris, Pericom, ASI, IDT, Cypress, Quality	More Suppliers

NOTE:

1. Speed Grades for Harris and Pericom FCT245T/A/C/D.

Octal 5V FCT Logic with 25Ω Series R at Outputs

These non-JEDEC standard products (due to reduced output drive) differ from (JEDEC) 5V FCT as follows:

- Designation is CD74FCT2XXXT; the 2 Meaning 25Ω Series R At Outputs
- I_{OL} Reduced to 12mA
- Same Switching Speed For Speed Grades Through C; No D Speed
- Dynamic Output Impedance Approximately Matches PCB's Affective Trace Z of About 25Ω
- Improved Bus Waveform Integrity
- Lower Edge Ringing; Lower Ground Bounce

Double Density 5V FCT Logic - High Drive

- Designated CD74FCT16XXXT
- Meets JEDEC Std. No. 18A; Same Specifications as Octal
- New 0.6 micron CMOS Technology; Smaller Die; Faster Speed
- Speed Grades up to "E" (3.2ns Delay)
- Surface Mount SSOP and TSSOP Packages for Low Ground Pin Inductance; Less Noise
- Multiple Ground and Power Pins to Minimize Switching Noise and Ground Bounce
- Lowest Dynamic Power of 4 Vendors of 5V Double Density Families - see Table 2.

TABLE 2. RELATIVE POWER

FAMILY	NORMALIZED POWER (30MHz)	TECHNOLOGY
Harris FCT16XXX	1	CMOS
ABT16XXX	2	BiCMOS
ACT16XXX	5	5V Output Swing CMOS
F16XXX	7	Bipolar

Double Density 5V FCT Logic with Balance Drive Output

Same as Double Density FCT except Balanced Drive features the following attributes:

- CD74FCT2XXXT Designation
- ±24mA Output Drive; Matched Output Edge Rates and Ground Source Termination for PCB Trace Drive
- Reduced Switching Noise; Ground Bounce < 0.6V
- Comparable to the Balanced output Drive of Industry CMOS ACT16XXX Products; Harris Double Density FCT162XXX is Typically 5X MW/MHz Lower due Primarily to the 5V Rail-to-Rail Swing of ACT Outputs

Double Density Quiet Series 5V FCT Logic with Bus Hold

- Designated CD74FCT162QXXXT
- ±12mA Output Drive; Output Matches Line Impedance
- "Quiet" Means an FCT Part with Minimal Output Edge Overshoot/Undershoot, Ring Back and Ground Bounce (See Tech Brief TB342)
- Bus Hold Feature; Last Active Bus State is Held During Three-State; Eliminates Floating Input Problem When No Pull-Up/Pull-Down Resistors Are Used

Double Density 3.3V FCT Logic

- Compatible with LVC™ and LCX™ Families
- Designation is CD74FCT163XXX
- Inputs can be 5V or 3V
- "Hot Plug" of PCB with 3.3V FCT is Compatible See Application Note AN9662 for details.
- Balanced ±24mA Drive
- Speed Grades up to C (4.1ns Delay)
- 50% Faster Speed than LCX™ or LVC™ Families
- Significantly Lower Operating Power Than LCX™ , LVT™, or LVC™

Octal 3.3V LPT Logic

- Advanced 0.6 micron CMOS Technology
- Balanced ±24mA Drive; Ideal for Internal PCB Bus Interface at Low Power and Low Noise
- Hysteresis at all Inputs
- 3.3V or 5V Input for 5V to 3V Translation
- 3.3V or 5V Output Bus Interface at low power
- Power Up/Down High Z
- Speed Grades up to "C" (4.1ns Delay)-Highest Speed 3.3V Logic
- Available in Low Pin Inductance SOIC and QSOP Packages; Low Ground Bounce and Switching Noise

As shown in 3.3V Family Selection (Table 3), LPT is the speed leader at 4.1ns delay in the group of four high performance 3.3V logic families.

Double Density 3.3V LPT Logic Products

All attributes of the octal 3.3V LPT products apply with 2 major differences:

- Available in SSOP and TSSOP Packages with Distributed GND and Power Pins
- Improved GND and Power Distribution Further Reduces Ground Bounce and Switching Noise

TABLE 3. 3.3V LOGIC FAMILIES COMPARISON (NOTE 2)

	GENERAL PURPOSE	HIGH PERFORMANCE	BACKPLANE DRIVING
Low Voltage Family	LVX™	LPT/LCX™/FCT/LVC™ (Note 3)	LVT™
3.3V and 5V Input	Yes	Yes	Yes
3.3V and 5V Output Interface	No	LPT/LCX™	No
5V Equivalent	HC/VHC	AC/ACQ/FAST™	ABT
Functions	Full Family	Primarily Bus Interface	Bus
Process	CMOS	CMOS (0.6 - 0.8 microns) (Note 4)	BiCMOS
t_{PD} (Max)	11.5ns	4.1ns - 6.5ns (Note 5)	5ns
Drive	±4mA	±24mA (Note 3)	+64mA/-32mA
Price (Normalized)	1	1.5	2

NOTES:

2. Data reflects 245 octal transceiver.
3. LVC has ±12mA drive at V_{CC} = 2.7V; all families have minimum ±24mA drive at V_{CC} = 3V.
4. Harris/Pericom LPT is 0.6 micron technology for fastest speed grades.
5. Harris/Pericom LPT and FCT are 4.1ns; See data sheets for t_{PD} of other families.

CMOS LOGIC 3

3.3V LPT CMOS LOGIC WITH 5V TOLERANT I/O

		PAGE
Selection Guide		3-2
Data Sheets		
CD74LPT16240	Fast CMOS 3.3V 16-Bit Buffer/Line Driver	3-3
CD74LPT16244	Fast CMOS 3.3V 16-Bit Buffer/Line Driver	3-9
CD74LPT16245	Fast CMOS 3.3V 16-Bit Bidirectional Transceiver	3-15
CD74LPT16373	Fast CMOS 3.3V 16-Bit Transparent Latch	3-21
CD74LPT16374	Fast CMOS 3.3V 16-Bit Register (Three-State)	3-27
CD74LPT16501	Fast CMOS 18-Bit Registered Transceiver	3-33
CD74LPT16543	Fast CMOS 16-Bit Latched Transceiver	3-41
CD74LPT16646	Fast CMOS 3.3V 16-Bit Registered Transceiver	3-47
CD74LPT16652	Fast CMOS 16-Bit Registered Transceiver	3-54
CD74LPT16827	Fast CMOS 3.3V 20-Bit Buffer	3-61
CD74LPT16952	Fast CMOS 3.3V 16-Bit Registered Transceiver	3-67
CD74LPT241	Fast CMOS 3.3V 8-Bit Buffer/Line Driver	3-73
CD74LPT244	Fast CMOS 3.3V 8-Bit Buffer/Line Driver	3-79
CD74LPT245	Fast CMOS 3.3V 8-Bit Bidirectional Transceiver	3-85
CD74LPT373	Fast CMOS 3.3V 8-Bit Transparent Latch	3-91
CD74LPT541	Fast CMOS 3.3V 8-Bit Buffer/Line Driver	3-97
CD74LPT543	Fast CMOS 3.3V 8-Bit Latched Transceiver	3-103
CD74LPT573	Fast CMOS 3.3V 8-Bit Transparent Latch	3-109
CD74LPT646, CD74LPT652	Fast CMOS 3.3V 8-Bit Registered Transceivers	3-115
CD74LPT827	Fast CMOS 3.3V 10-Bit Buffer	3-123

Selection Guide

3.3V LPT CMOS LOGIC WITH 5V TOLERANT I/O

PART NUMBER	DESCRIPTION	SPEED GRADE (X)				FILE #
		BLANK	A	B	C	
CD74LPT16240	Fast CMOS 3.3V 16-Bit Buffer/Line Driver	X	X			4215
CD74LPT16244	Fast CMOS 3.3V 16-Bit Buffer/Line Driver	X	X			4216
CD74LPT16245	Fast CMOS 3.3V 16-Bit Bidirectional Transceiver	X	X			4205
CD74LPT16373	Fast CMOS 3.3V 16-Bit Transparent Latch	X	X			4206
CD74LPT16374	Fast CMOS 3.3V 16-Bit Registers (Three-State)	X	X			4207
CD74LPT16501	Fast CMOS 18-Bit Registered Transceiver	X	X			4208
CD74LPT16543	Fast CMOS 16-Bit Latched Transceiver	X	X		X	4209
CD74LPT16646	Fast CMOS 3.3V 16-Bit Registered Transceiver	X	X			4210
CD74LPT16652	Fast CMOS 16-Bit Registered Transceiver	X	X			4211
CD74LPT16827	Fast CMOS 3.3V 20-Bit Buffer		X	X		4212
CD74LPT16952	Fast CMOS 3.3V 16-Bit Registered Transceiver		X	X		4213
CD74LPT241	Fast CMOS 3.3V 8-Bit Buffer/Line Driver	X	X		X	4196
CD74LPT244	Fast CMOS 3.3V 8-Bit Buffer/Line Driver	X	X		X	4197
CD74LPT245	Fast CMOS 3.3V 8-Bit Bidirectional Transceiver	X	X		X	4198
CD74LPT373	Fast CMOS 3.3V 8-Bit Transparent Latche	X	X		X	4199
CD74LPT541	Fast CMOS 3.3V 8-Bit Buffer/Line Driver	X	X		X	4200
CD74LPT543	Fast CMOS 3.3V 8-Bit Latched Transceiver	X	X		X	4256
CD74LPT573	Fast CMOS 3.3V 8-Bit Transparent Latches	X	X		X	4201
CD74LPT646	Fast CMOS 3.3V 8-Bit Registered Transceiver	X	X		X	4257
CD74LPT652	Fast CMOS 3.3V 8-Bit Registered Transceiver	X	X		X	4257
CD74LPT827	Fast CMOS 3.3V 10-Bit Buffer		X	X	X	4258

CD74LPT16240

December 1996

Fast CMOS 3.3V 16-Bit Buffer/Line Driver

Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimize Switching Noise

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT16240AMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LPT16240ASM	-40 to 85	48 Ld SSOP	M48.300-P
CD74LPT16240MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LPT16240SM	-40 to 85	48 Ld SSOP	M48.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

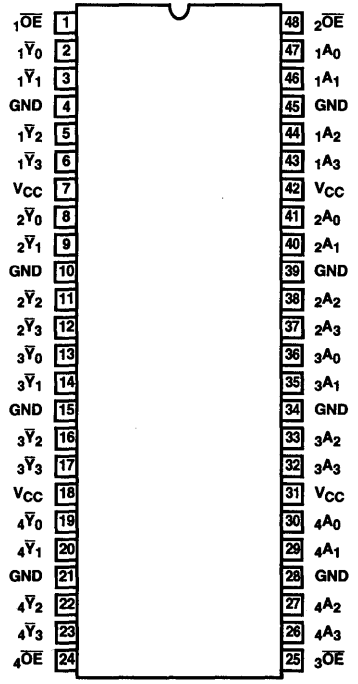
Description

The CD74LPT16240 is an inverting 16-bit buffer/line driver designed for applications driving high-capacitance loads and low impedance backplanes. This high-speed, low power device offers bus/backplane interface capability and a flow-through organization for ease of board layout. This device is designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

The CD74LPT16240 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout

CD74LPT16240
(SSOP, TSSOP)
TOP VIEW

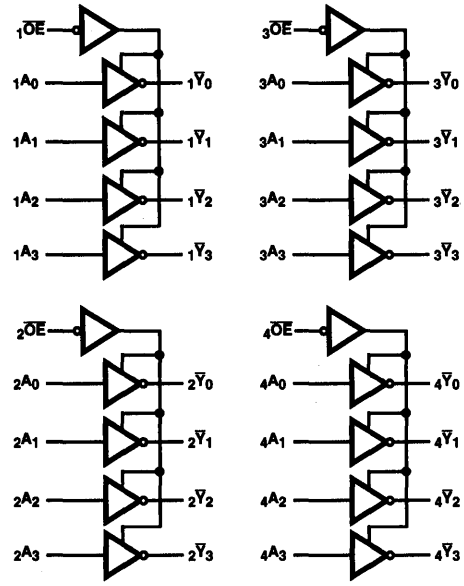


3

3.3V LPT

File Number **4215.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$x\overline{OE}$	xA_x	$x\overline{Y}_x$
L	L	H
L	H	L
H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$x\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
xA_x	Inputs
$x\overline{Y}_x$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 11)	mA

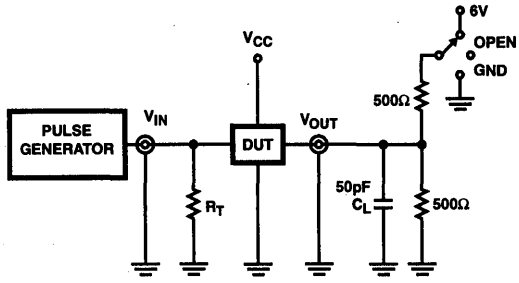
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT16240		CD74LPT16240A		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay xA_x to $x\overline{Y}_x$	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	4.9	1.5	4.8	ns
Output Enable Time $x\overline{OE}$ to $x\overline{Y}_x$	t_{PZH}, t_{PZL}		1.5	7.0	1.5	6.2	ns
Output Disable Time (Note 16) $x\overline{OE}$ to $x\overline{Y}_x$	t_{PHZ}, t_{PLZ}		1.5	7.0	1.5	5.6	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC}$ - 0.6V at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

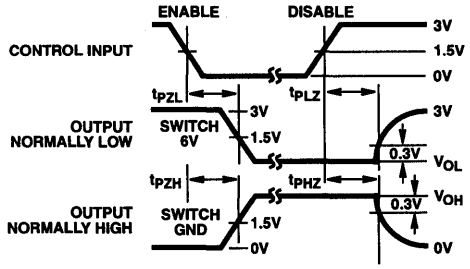


FIGURE 2. ENABLE AND DISABLE TIMING

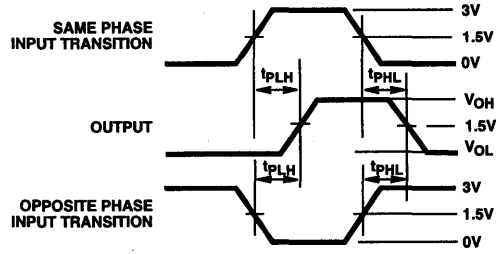


FIGURE 3. PROPAGATION DELAY

CD74LPT16244

December 1996

Fast CMOS 3.3V 16-Bit Buffer/Line Driver

Features

- **Advanced 0.6 micron CMOS Technology**
- **Compatible with LCX™ Families of Products**
- **Supports 5V Tolerant Mixed Signal Mode Operation**
  - **Input Can Be 3V or 5V**
  - **Output Can Be 3V or Connected to 5V Bus**
- **Advanced Low Power CMOS Operation**
- **Excellent Output Drive Capability:**
  - **Balanced Drives (24mA Sink and Source)**
- **Pin Compatible with Industry Standard Double-Density Pinouts**
- **Low Ground Bounce Outputs**
- **Hysteresis on All Inputs**
- **Multiple Center Pin and Distributed V_{CC}/GND Pins Minimize Switching Noise**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT16244AMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LPT16244ASM	-40 to 85	48 Ld SSOP	M48.300-P
CD74LPT16244MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LPT16244SM	-40 to 85	48 Ld SSOP	M48.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

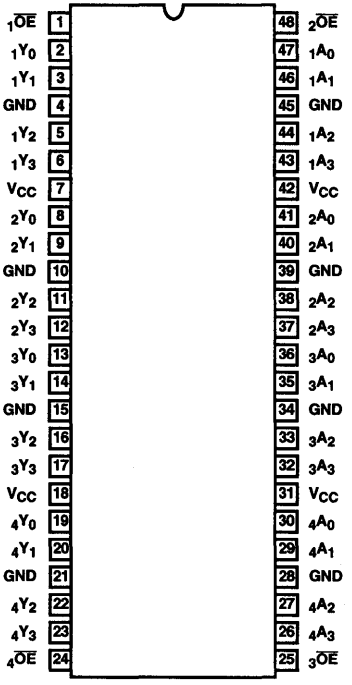
Description

The CD74LPT16244 is a 16-bit buffer/line driver designed for driving high capacitive memory loads. With its balanced-drive characteristics, this high-speed, low power device provides lower ground bounce, transmission line matching of signals, fewer line reflections and lower EMI and RFI effects. This makes it ideal for driving on-board buses and transmission lines. This device is designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

The CD74LPT16244 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout

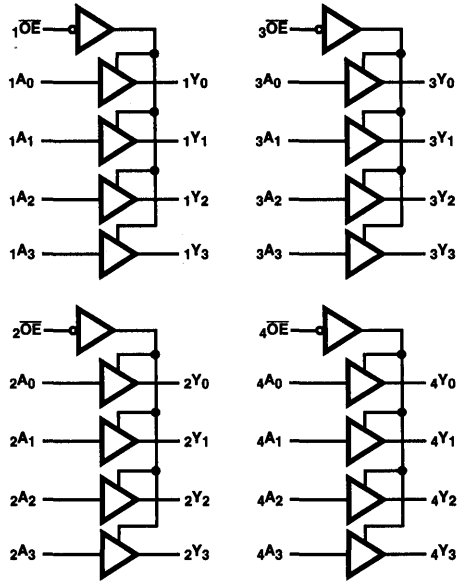
CD74LPT16244
(SSOP, TSSOP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4216.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$x\overline{OE}$	xA_x	xY_x
L	L	L
L	H	H
H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$x\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
xA_x	Inputs
xY_x	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.5	0.8	mA
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.0	3.3 (Note 11)	mA

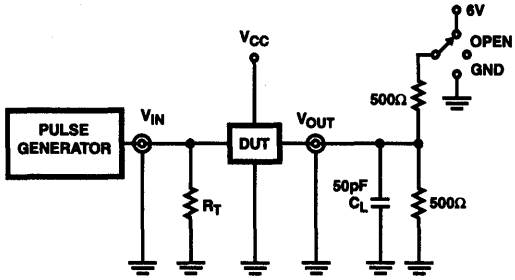
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT16244		CD74LPT16244A		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay $_xA_x$ to $_xY_x$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	5.2	1.5	4.8	ns
Output Enable Time $_x\overline{OE}$ to $_xY_x$	t_{PZH}, t_{PZL}		1.5	7.0	1.5	6.2	ns
Output Disable Time (Note 16) $_x\overline{OE}$ to $_xY_x$	t_{PHZ}, t_{PLZ}		1.5	7.0	1.5	5.6	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC}$ - 0.6V at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

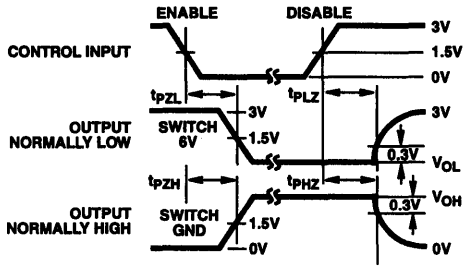


FIGURE 2. ENABLE AND DISABLE TIMING

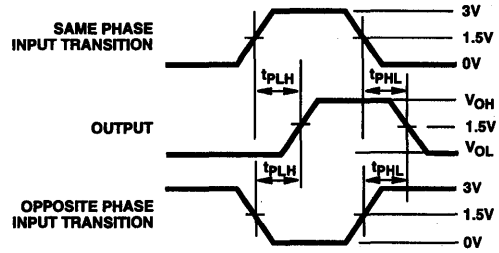


FIGURE 3. PROPAGATION DELAY

CD74LPT16245

December 1996

Fast CMOS 3.3V 16-Bit Bidirectional Transceiver

Features

- **Advanced 0.6 micron CMOS Technology**
- **Compatible with LCX™ Families of Products**
- **Supports 5V Tolerant Mixed Signal Mode Operation**
  - **Input Can Be 3V or 5V**
  - **Output Can Be 3V or Connected to 5V Bus**
- **Advanced Low Power CMOS Operation**
- **Excellent Output Drive Capability:**
  - **Balanced Drives (24mA Sink and Source)**
- **Pin Compatible with Industry Standard Double-Density Pinouts**
- **Low Ground Bounce Outputs**
- **Hysteresis on All Inputs**
- **Multiple Center Pin and Distributed V_{CC}/GND Pins Minimize Switching Noise**

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CD74LPT16245AMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LPT16245ASM	-40 to 85	48 Ld SSOP	M48.300-P
CD74LPT16245MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LPT16245SM	-40 to 85	48 Ld SSOP	M48.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

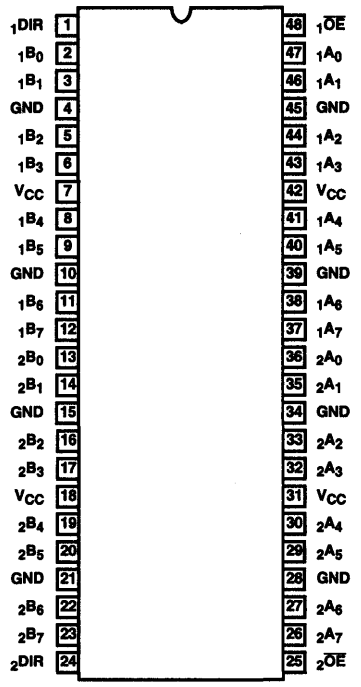
Description

The CD74LPT16245 is a 16-bit bidirectional transceiver designed for asynchronous two-way communication between data buses. The direction control input pin ($_X$DIR) determines the direction of data flow through the bidirectional transceiver. The Direction and Output Enable controls are designed to operate this device as either two independent 8-bit transceivers or one 16-bit transceiver. The output enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The CD74LPT16245 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout

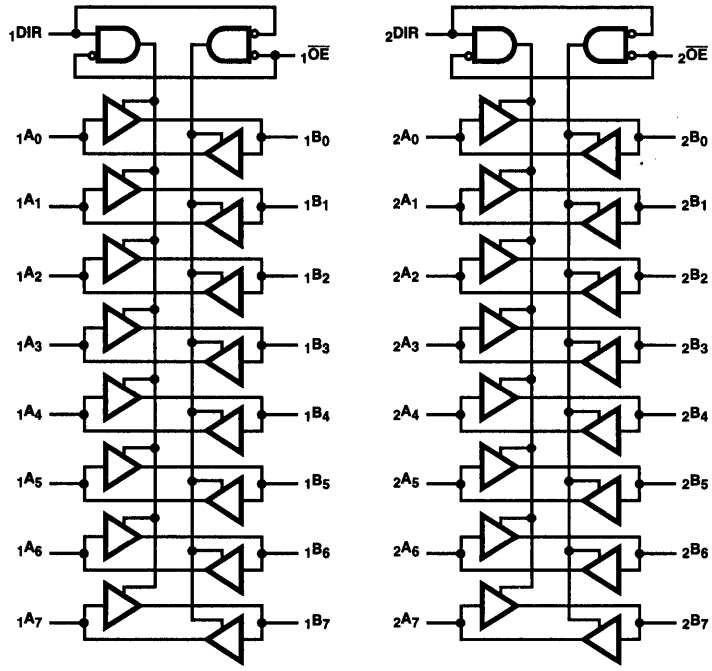
CD74LPT16245
(SSOP, TSSOP)
TOP VIEW



3 3.3V LPT

File Number **4205.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$_X\overline{OE}$	$_X$DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_X\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$_X$DIR	Direction Control Input
$_XA_X$	Side A Inputs or Three-State Outputs
$_XB_X$	Side B Inputs or Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = xDIR = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = xDIR = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.5	0.8	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = xDIR = GND 16 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.0	3.3 (Note 11)	mA

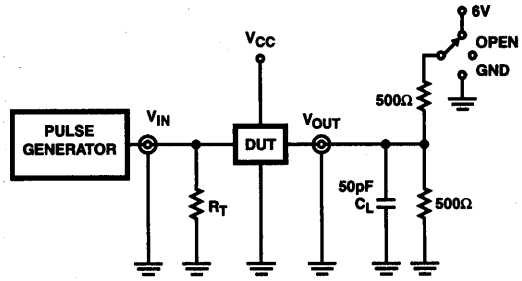
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT16245		CD74LPT16245A		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay A to B, B to A	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	5.2	1.5	4.6	ns
Output Enable Time $x\overline{OE}$ to A or B	t_{PZH}, t_{PZL}		1.5	7.2	1.5	6.2	ns
Output Disable Time (Note 16) $x\overline{OE}$ to A or B	t_{PHZ}, t_{PLZ}		1.5	7.2	1.5	5.0	ns
Output Enable Time xDIR to A or B	t_{PZH}, t_{PZL}		1.5	7.2	1.5	6.2	ns
Output Disable Time xDIR to A or B (Note 16)	t_{PHZ}, t_{PLZ}		1.5	7.2	1.5	5.0	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC} - 0.6V$ at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

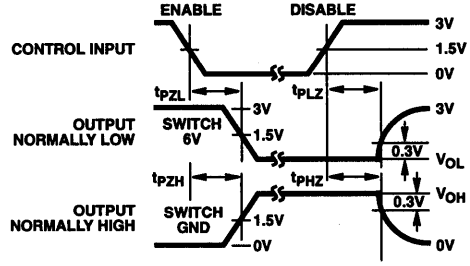


FIGURE 2. ENABLE AND DISABLE TIMING

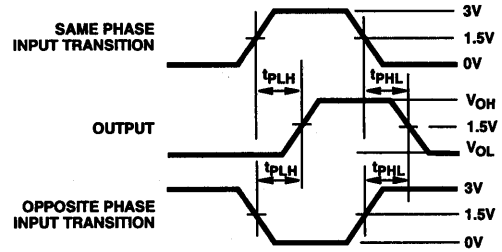


FIGURE 3. PROPAGATION DELAY

CD74LPT16373

December 1996

Fast CMOS 3.3V 16-Bit Transparent Latch

Features

- **Advanced 0.6 micron CMOS Technology**
- **Compatible with LCX™ Families of Products**
- **Supports 5V Tolerant Mixed Signal Mode Operation**
  - **Input Can Be 3V or 5V**
  - **Output Can Be 3V or Connected to 5V Bus**
- **Advanced Low Power CMOS Operation**
- **Excellent Output Drive Capability:**
  - **Balanced Drives (24mA Sink and Source)**
- **Pin Compatible with Industry Standard Double-Density Pinouts**
- **Low Ground Bounce Outputs**
- **Hysteresis on All Inputs**
- **Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT16373AMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LPT16373ASM	-40 to 85	48 Ld SSOP	M48.300-P
CD74LPT16373MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LPT16373SM	-40 to 85	48 Ld SSOP	M48.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

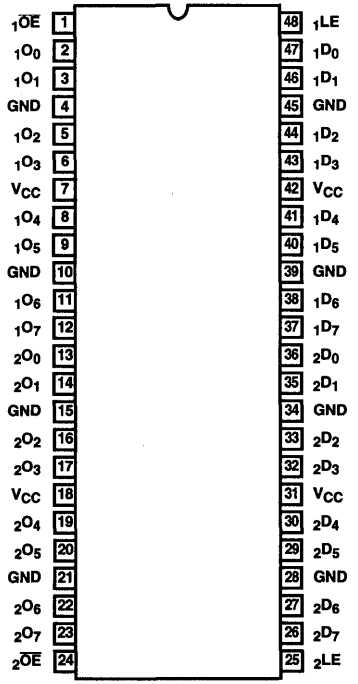
Description

The CD74LPT16373 is a 16-bit transparent latch designed with three-state outputs and is intended for bus oriented applications. The Output Enable and Latch Enable controls are organized to operate as two 8-bit latches or one 16-bit latch. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

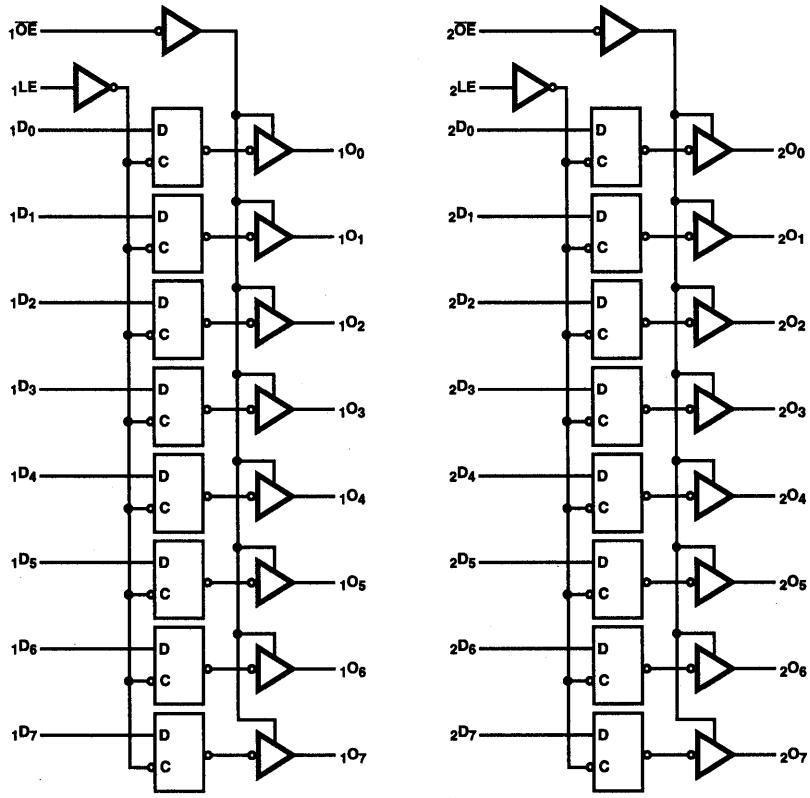
The CD74LPT16373 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout

CD74LPT16373
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$_xD_x$	$_x\overline{OE}$	$_xLE$	$_xO_x$
H	L	H	H
L	L	H	L
X	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_x\overline{OE}$	Output Enable Inputs (Active LOW)
$_xLE$	Latch Enable Inputs (Active HIGH)
$_xD_x$	Data Inputs
$_xO_x$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$				±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = VCC - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND xLE = V_{CC} One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} 16 Bits Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 11)	mA

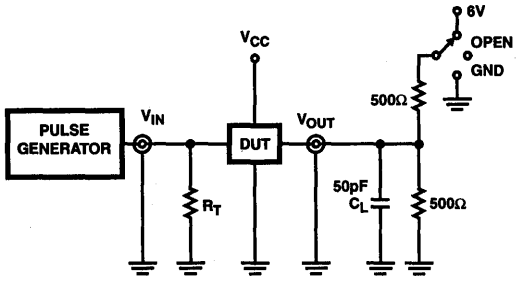
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT16373		CD74LPT16373A		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay $_XD_X$ to $_XO_X$	t_{PLH}, t_{PHL}	C_L = 50 pF, R_L = 500Ω	1.5	7.0	1.5	5.2	ns
Propagation Delay $_XLE$ to $_XO_X$	t_{PLH}, t_{PHL}		2.0	7.0	2.0	6.5	ns
Output Enable Time $_X\overline{OE}$ to $_XO_X$	t_{PZH}, t_{PZL}		1.5	7.2	1.5	6.5	ns
Output Disable Time (Note 16) $_X\overline{OE}$ to $_XO_X$	t_{PHZ}, t_{PLZ}		1.5	7.2	1.5	5.5	ns
Setup Time HIGH or LOW, $_XD_X$ to $_XLE$	t_{SU}		2.0	-	2.0	-	ns
Hold Time HIGH or LOW, $_XD_X$ to $_XLE$	t_H		1.5	-	1.5	-	ns
$_XLE$ Pulse Width HIGH (Note 16)	t_W		6.0	-	5.0	-	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC}$ - 0.6V at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

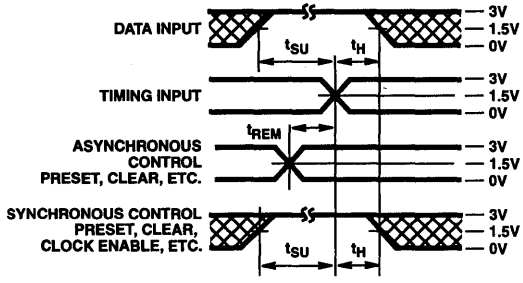


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

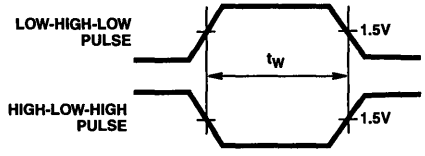


FIGURE 3. PULSE WIDTH

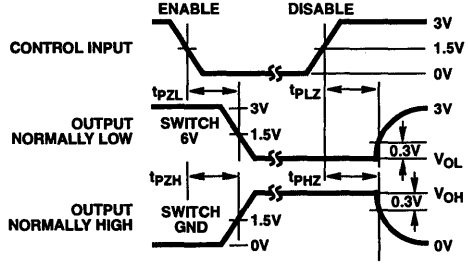


FIGURE 4. ENABLE AND DISABLE TIMING

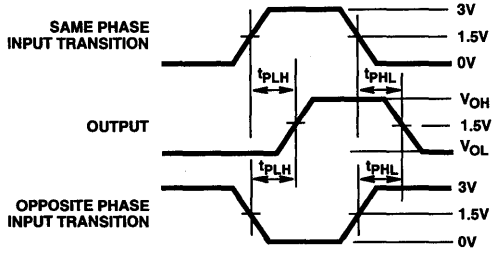


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74LPT16374

December 1996

Fast CMOS 3.3V 16-Bit Register (Three-State)

Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT16374AMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LPT16374ASM	-40 to 85	48 Ld SSOP	M48.300-P
CD74LPT16374MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74LPT16374SM	-40 to 85	48 Ld SSOP	M48.300-P

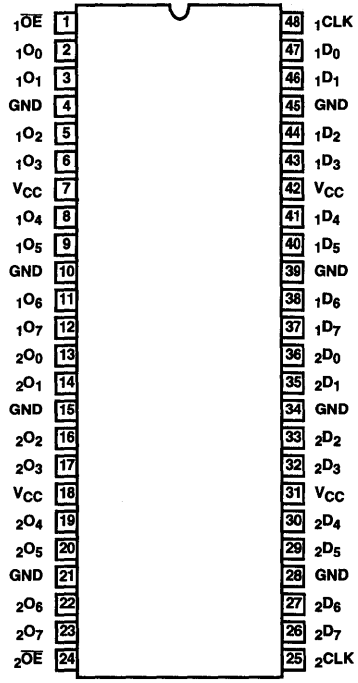
Description

The CD74LPT16374 is a 16-bit octal register designed with 16 D-type flip-flops with a buffered common clock and three-state outputs. The Output Enable ($_x\overline{OE}$) and clock ($_x$CLK) controls are organized to operate as two 8-bit registers or one 16-bit register. When $\overline{OE}$ is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

The CD74LPT16374 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout

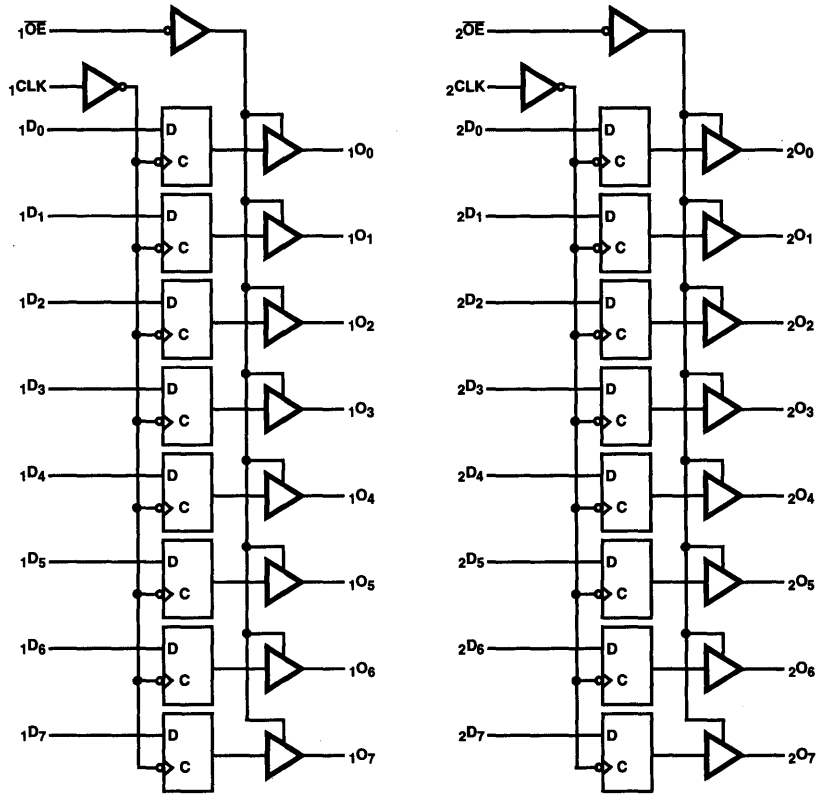
CD74LPT16374
(SSOP, TSSOP)
TOP VIEW



3 3.3V LPT

File Number **4207.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS			OUTPUTS
	$_xD_x$	$_x$CLK	$_x\overline{OE}$	$_xO_x$
High-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$_x\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$_x$CLK	Clock Inputs
$_xD_x$	Data Inputs
$_xO_x$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤4.5V		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = V_{CC} - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 11)	mA

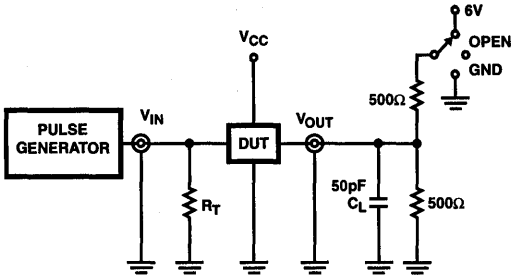
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT16374		CD74LPT16374A		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay $_xCLK_x$ to $_xO_x$	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	2.0	7.0	2.0	6.5	ns
Output Enable Time $_x\overline{OE}$ to $_xO_x$	t_{PZH}, t_{PZL}		1.5	7.2	1.5	6.5	ns
Output Disable Time (Note 16) $_x\overline{OE}$ to $_xO_x$	t_{PHZ}, t_{PLZ}		1.5	7.2	1.5	5.5	ns
Setup Time HIGH or LOW, $_xD_x$ to $_xCLK$	t_{SU}		2.0	-	2.0	-	ns
Hold Time HIGH or LOW, $_xD_x$ to $_xCLK$	t_H		1.5	-	1.5	-	ns
$_xCLK$ Pulse Width HIGH or LOW (Note 16)	t_W		7.0	-	5.0	-	ns
Output Skew (Note17)	$t_{SK(O)}$		-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC}$ - 0.6V at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

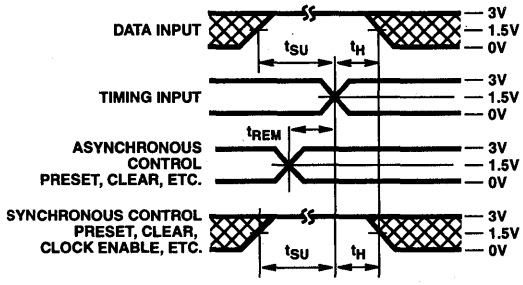


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

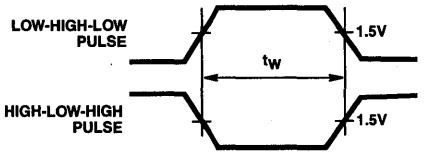


FIGURE 3. PULSE WIDTH

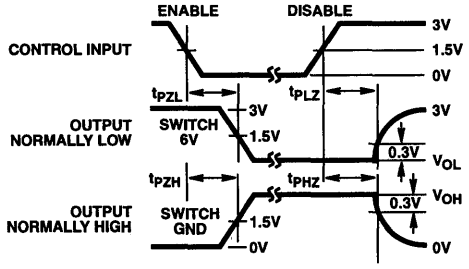


FIGURE 4. ENABLE AND DISABLE TIMING

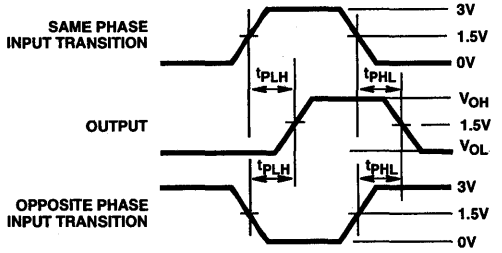


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74LPT16501

December 1996

Fast CMOS 18-Bit Registered Transceiver

Features

- **Advanced 0.6 micron CMOS Technology**
- **Compatible with LCX™ Families of Products**
- **Supports 5V Tolerant Mixed Signal Mode Operation**
  - **Input Can Be 3V or 5V**
  - **Output Can Be 3V or Connected to 5V Bus**
- **Advanced Low Power CMOS Operation**
- **Excellent Output Drive Capability:**
  - **Balanced Drives (24mA Sink and Source)**
- **Pin Compatible with Industry Standard Double-Density Pinouts**
- **Low Ground Bounce Outputs**
- **Hysteresis on All Inputs**
- **Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT16501AMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16501ASM	-40 to 85	56 Ld SSOP	M56.300-P
CD74LPT16501MT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16501SM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

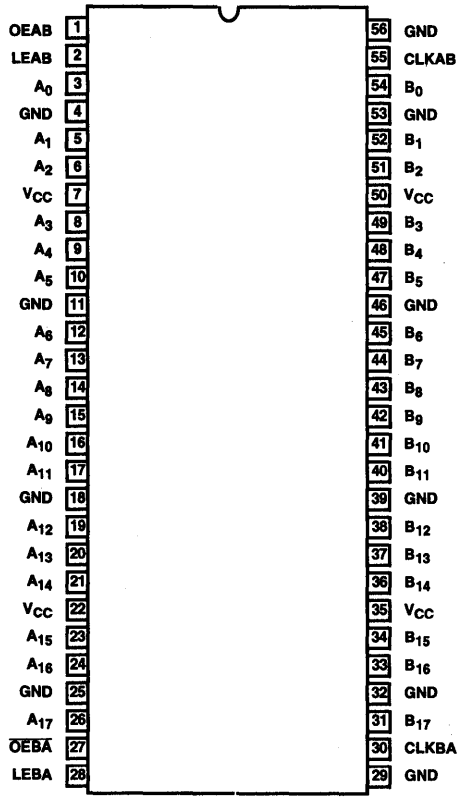
Description

The CD74LPT16501 is an 18-bit registered bus transceiver designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (OEAB and $\overline{OEBA}$), Latch Enable (LEAB and LEBA) and Clock (CLKAB and CLKBA) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using $\overline{OEBA}$, LEBA and CLKBA. This high-speed, low power device offers a flow-through organization for ease of board layout.

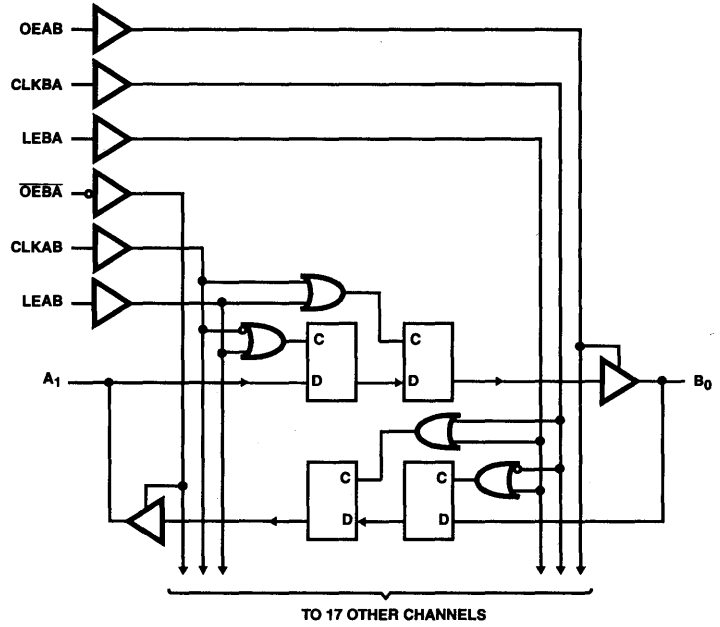
The CD74LPT16501 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3V/5.0V system.

Pinout

CD74LPT16501
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTES 1, 4)

INPUTS				OUTPUTS
OEAB	LEAB	CLKAB	A_X	B_X
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B (Note 2)
H	L	H	X	B (Note 3)

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A_X	A-to-B Data Inputs or B-to-A Three-State Outputs
B_X	B-to-A Data Inputs or A-to-B Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS		MIN	(NOTE 7) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 8)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 8)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 10)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V
Short Circuit Current (Note 9)	I_{OS}	V_{CC} = Max (Note 8), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤4.5V		-	-	±100	µA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS		MIN	(NOTE 7) TYP	MAX	UNITS
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 11)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 11)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 12)	-	2.0	30	µA
Dynamic Power Supply Current (Note 13)	I_{CCD}	V_{CC} = Max, Outputs Open OEAB = $\overline{OEBA}$ = V_{CC} or GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 15)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz (CLKAB), 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND, f_i = 5MHz One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz (CLKAB), 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND, f_i = 2.5MHz Eighteen Bits Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 14)	mA

Switching Specifications Over Operating Range (Note 16)

PARAMETER	SYMBOL	(NOTE 17) TEST CONDITIONS	CD74LPT16501		CD74LPT16501A		UNITS
			(NOTE 18) MIN	MAX	(NOTE 18) MIN	MAX	
CLKAB or CLKBA frequency	t_{MAX}	C_L = 50pF R_L = 500Ω	-	100	-	150	ns
Propagation Delay A_X to B_X or B_X to A_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.1	ns
Propagation Delay LEBA to A_X, LEAB to B_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	7.5	1.5	5.6	ns
Propagation Delay CLKBA to A_X, CLKAB to B_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	5.6	ns
Output Enable Time $\overline{OEBA}$ to A_X, OEAB to Bx	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	6.0	ns
Output Disable Time (Note 19) $\overline{OEBA}$ to A_X, OEAB to B_X	t_{PHZ} t_{PLZ}	C_L = 50pF R_L = 500Ω	1.5	7.5	1.5	5.6	ns

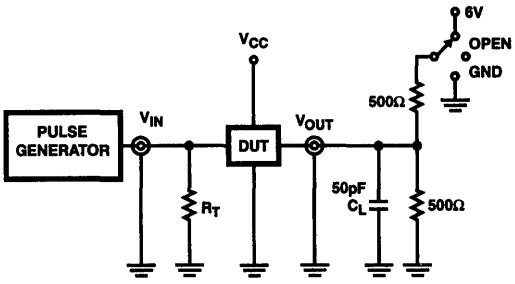
Switching Specifications Over Operating Range (Note 16) **(Continued)**

PARAMETER	SYMBOL	(NOTE 17) TEST CONDITIONS	CD74LPT16501		CD74LPT16501A		UNITS
			(NOTE 18) MIN	MAX	(NOTE 18) MIN	MAX	
Setup Time HIGH or LOW A_X to CLKAB, B_X to CLKBA	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	3.0	-	ns
Hold Time HIGH or LOW A_X to CLKAB, B_X to CLKBA	t_H	C_L = 50pF R_L = 500Ω	0	-	0	-	ns
Setup Time HIGH or LOW, A_X to LEAB, B_X to LEBA, Clock HIGH	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	3.0	-	ns
Setup Time HIGH or LOW, A_X to LEAB, B_X to LEBA, Clock LOW	t_{SU}	C_L = 50pF R_L = 500Ω	1.5	-	1.5	-	ns
Hold Time HIGH or LOW, Ax to LEAB, Bx to LEBA	t_H	C_L = 50pF R_L = 500Ω	1.5	-	1.5	-	ns
LEAB or LEBA Pulse Width HIGH (Note 19)	t_W	C_L = 50pF R_L = 500Ω	3.0	-	3.0	-	ns
CLKAB or CLKBA Pulse Width HIGH or LOW (Note 19)	t_W	C_L = 50pF R_L = 500Ω	3.0	-	3.0	-	ns
Output Skew (Note 20)	$t_{SK(O)}$	C_L = 50pF R_L = 500Ω	-	0.5	-	0.5	ns

NOTES:

6. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
7. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading, except as noted.
8. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
9. This parameter is guaranteed but not tested.
10. $V_{OH} = V_{CC}$ - 0.6V at rated current.
11. This parameter is determined by device characterization but is not production tested.
12. Per TTL driven input; all other inputs at V_{CC} or GND.
13. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
14. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
15. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
16. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
17. See test circuit and wave forms.
18. Minimum limits are guaranteed but not tested on Propagation Delays.
19. This parameter is guaranteed but not production tested.
20. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

21. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

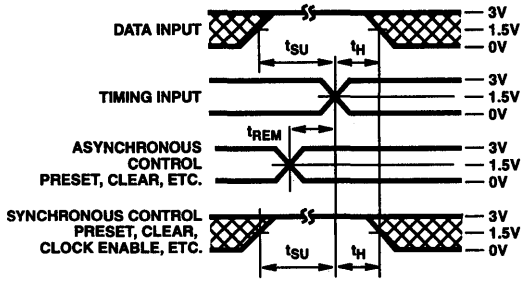


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

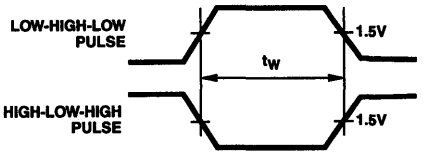


FIGURE 3. PULSE WIDTH

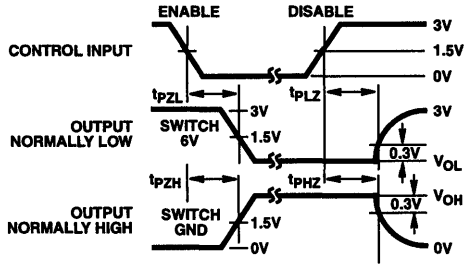


FIGURE 4. ENABLE AND DISABLE TIMING

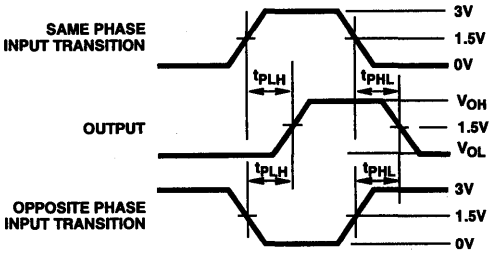


FIGURE 5. PROPAGATION DELAY

CD74LPT16543

December 1996

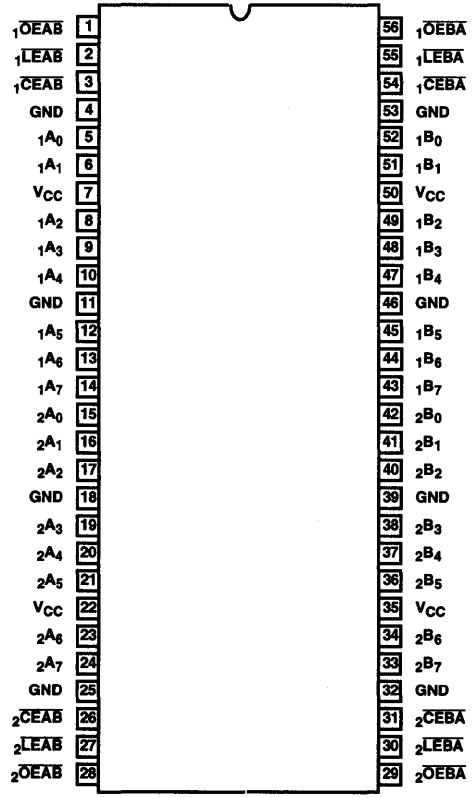
Fast CMOS 16-Bit Latched Transceiver

Features

- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Pinout

CD74LPT16543 (SSOP, TSSOP)
TOP VIEW



Description

Harris CD74LPT16543 is produced in an advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The CD74LPT16543 are 16-bit latched transceivers organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($_x\overline{CEAB}$) input must be LOW in order to enter data from xAx or to take data from xBx, as indicated in the Truth Table. With $_x\overline{CEAB}$ LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the xLEAB signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With $_x\overline{CEAB}$ and $_x\overline{OEAB}$ both LOW, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $_x\overline{CEAB}$, $_x\overline{LEAB}$, and $_x\overline{OEAB}$ inputs.

The CD74LPT16543 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

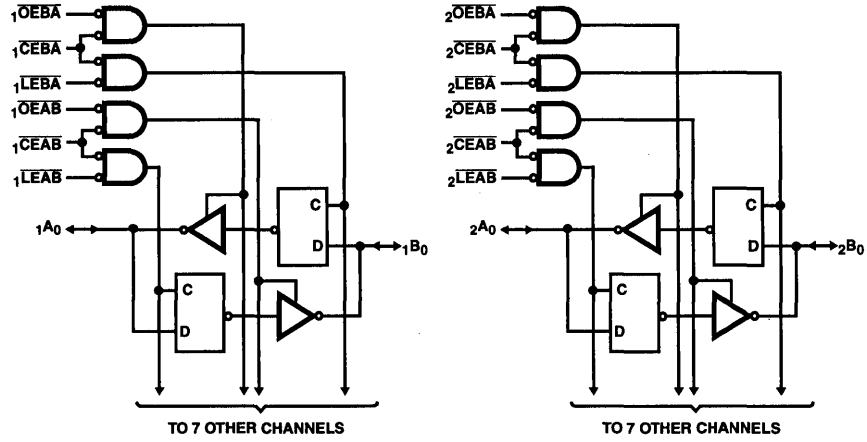
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT16543AMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16543ASM	-40 to 85	56 Ld SSOP	M56.300-P
CD74LPT16543CMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16543CSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74LPT16543MT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16543SM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4209.2**

Functional Block Diagram



TRUTH TABLE (NOTES 1, 3)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$_X\overline{CEAB}$	$_X\overline{LEAB}$	$_X\overline{OEAB}$	$_XA_X$ TO $_XB_X$	$_XB_X$
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs (Note 2)

NOTES:

1. A-to-B data flow is shown. B-to-A flow control is the same except using $_X\overline{CEBA}$, $_X\overline{LEBA}$, and $_X\overline{OEBA}$.
2. Before $_X$LEAB LOW-to-HIGH Transition
3. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care or Irrelevant
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_X\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$_X\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$_X\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$_X\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$_X\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$_X\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
$_XA_X$	A-to-B Data Inputs or B-to-A Three-State Outputs
$_XB_X$	B-to-A Data Inputs or A -to-B Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 9)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
Short Circuit Current (Note 8)	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤4.5V		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = V_{CC} - 0.6V (Note 11)	-	2.0	30	µA
Dynamic Power Supply Current (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 13)	mA

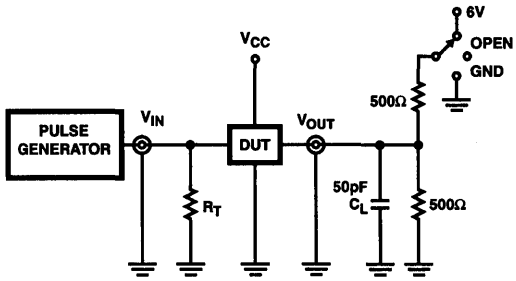
Switching Specifications Over Operating Range (Note 15)

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPT16543		CD74LPT16543A		CD74LPT16543C		UNITS
			(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	
Propagation Delay Transparent Mode $_xA_x$ to $_xB_x$ or $_xB_x$ to $_xA_x$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	ns
Propagation Delay $_x\overline{LEBA}$ to $_xA_x$ $_x\overline{LEAB}$ to $_xB_x$	t_{PLH}, t_{PHL}		2.5	12.5	2.5	8.0	2.5	7.0	ns
Output Enable Time $_x\overline{OEBA}$ or $_x\overline{OEAB}$ to $_xA_x$ or $_xB_x$	t_{PZH}, t_{PZL}		2.0	12.0	2.0	9.0	2.0	8.0	ns
Output Disable Time (Note 18) $_x\overline{OEBA}$ or $_x\overline{OEAB}$ to $_xA_x$ or $_xB_x$	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	7.5	2.0	6.5	ns
Setup Time HIGH or LOW, $_xA_x$ or $_xB_x$ to $_x\overline{LEAB}$ or $_x\overline{LEBA}$	t_{SU}		3.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, $_xA_x$ or $_xB_x$ to $_x\overline{LEAB}$ or $_x\overline{LEBA}$	t_H		2.0	-	2.0	-	2.0	-	ns
$_x\overline{LEAB}$ or $_x\overline{LEBA}$ Pulse Width LOW	t_W		5.0	-	5.0	-	5.0	-	ns
Output Skew (Note 19)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is guaranteed but not tested.
9. $V_{OH} = V_{CC}$ - 0.6V at rated current.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input; all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
15. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.
18. This parameter is guaranteed but not production tested.
19. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

20. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

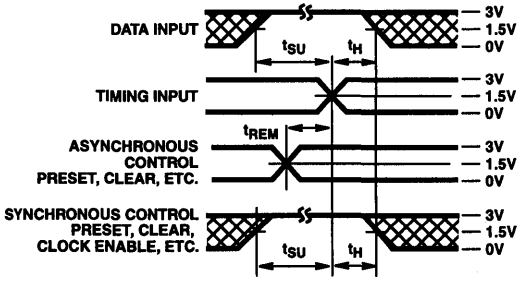


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

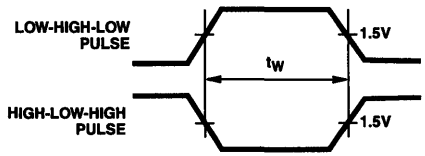


FIGURE 3. PULSE WIDTH

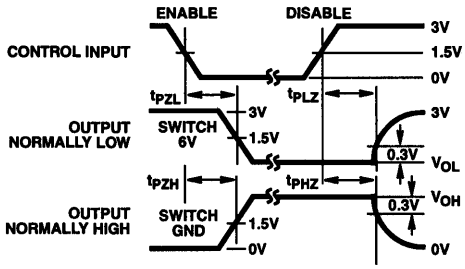


FIGURE 4. ENABLE AND DISABLE TIMING

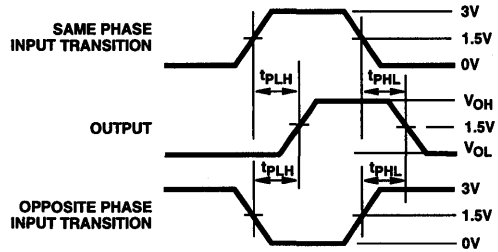


FIGURE 5. PROPAGATION DELAY

CD74LPT16646

December 1996

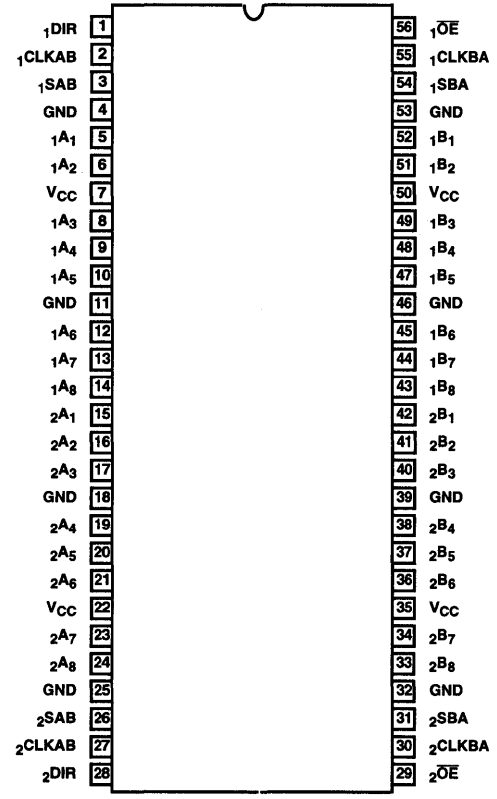
Fast CMOS 3.3V 16-Bit Registered Transceiver

Features

- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
- Input Can Be 3V or 5V
- Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability
  - Balanced Drives (24mA Sink and Source)
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Pinout

CD74LPT16646 (SSOP, TSSOP)
TOP VIEW



Description

Harris Semiconductor's CD74LPT16646 is produced in an advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The CD74LPT16646 is a 16-bit registered transceiver organized as two independent 8-bit bus transceivers designed with three-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable control ($_X\overline{OE}$) and direction pins ($_X$DIR) to control the transceiver functions. The Select ($_X$SAB and $_X$SBA) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

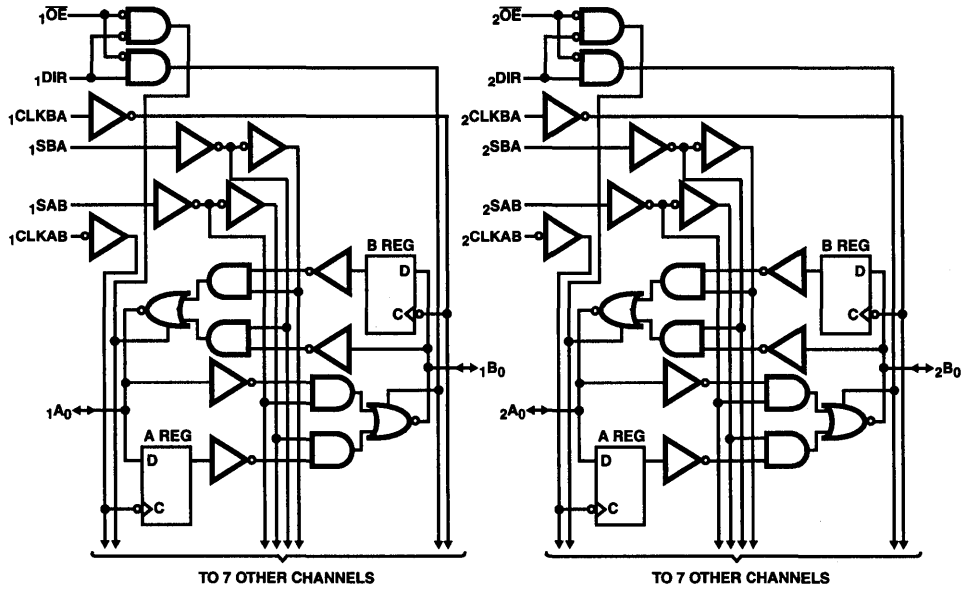
The CD74LPT16646 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT16646AMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16646ASM	-40 to 85	56 Ld SSOP	M56.300-P
CD74LPT16646MT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16646SM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the varient in the tape and reel.

Functional Block Diagram



TRUTH TABLE (NOTE 2)

FUNCTION	INPUTS						(Note 1) DATA I/O	
	$_X\overline{OE}$	$_X$DIR	$_X$CLKAB	$_X$CLKBA	$_X$SAB	$_X$SBA	$_XA_X$	$_XB_X$
Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	H	X	↑	↑	X	X		
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	L	H	H or L	X	H	X		

NOTES:

1. The data output functions may be enabled or disabled by various signals at the $_X\overline{OE}$ or $_X$DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH transition

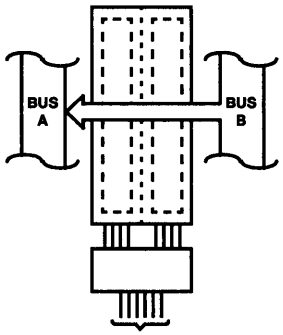


FIGURE 1. REAL-TIME TRANSFER BUS B TO A

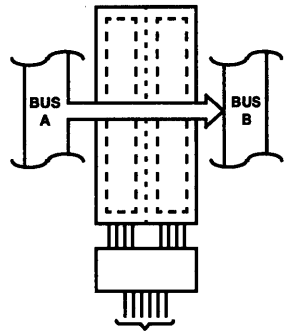


FIGURE 2. REAL-TIME TRANSFER BUS A TO B

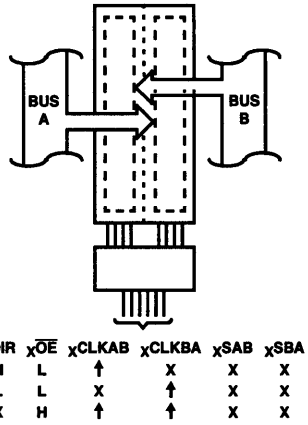


FIGURE 3. STORAGE FROM A AND/OR B

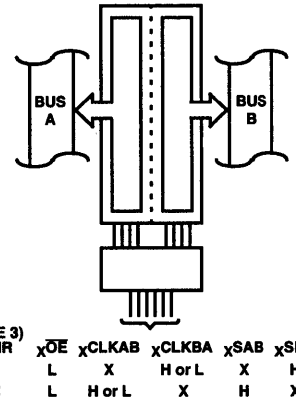


FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

NOTE:

3. Cannot transfer data to A bus and B bus simultaneously.

Pin Descriptions

PIN NAME	DESCRIPTION
$_xOE$, $_xDIR$	Output Enable Inputs (Active LOW)
$_xCLKAB$, $_xCLKBA$	Clock Pulse Inputs
$_xSAB$, $_xSBA$	Output Data Source Select Inputs
$_xA_x$	Data Register A Inputs Data Register B Outputs
$_xB_x$	Data Register B Inputs Data Register A Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 9)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
Short Circuit Current (Note 8)	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 11)	-	2.0	30	µA
Dynamic Power Supply Current (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 13)	mA

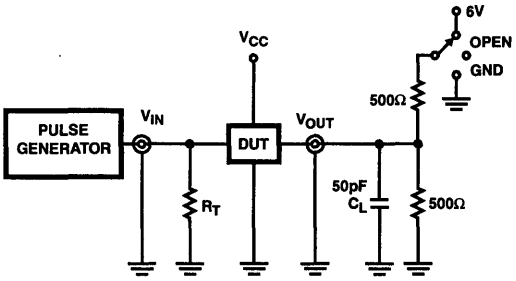
Switching Specifications Over Operating Range (Note 15)

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPT16646 (NOTE 17) MIN	CD74LPT16646 MAX	CD74LPT16646A (NOTE 17) MIN	CD74LPT16646A MAX	UNITS
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	ns
Output Enable Time $_X$DIR or $_X\overline{OE}$ to Bus	t_{PZH}, t_{PZL}		2.0	14.0	2.0	9.8	ns
Output Disable Time (Note 18) $_X$DIR or $_X\overline{OE}$ to Bus	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	6.3	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}		2.0	9.0	2.0	6.3	ns
Propagation Delay $_X$SBA or $_X$SAB to Bus	t_{PLH}, t_{PHL}		2.0	11.0	2.0	7.7	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}		4.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H		2.0	-	1.5	-	ns
Clock Pulse Width HIGH or LOW (Note 18)	t_W		6.0	-	5.0	-	ns
Output Skew (Note 19)	$t_{SK(O)}$		-	0.5	-	0.5	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is guaranteed but not tested.
9. $V_{OH} = V_{CC}$ - 0.6V at rated current.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input; all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
15. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.
18. This parameter is guaranteed but not production tested.
19. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

20. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 5. TEST CIRCUIT

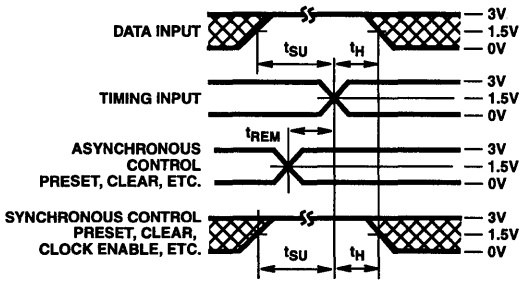


FIGURE 6. SETUP, HOLD, AND RELEASE TIMING

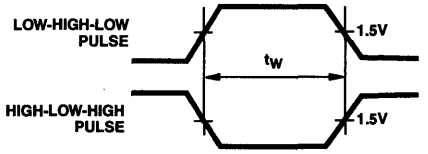


FIGURE 7. PULSE WIDTH

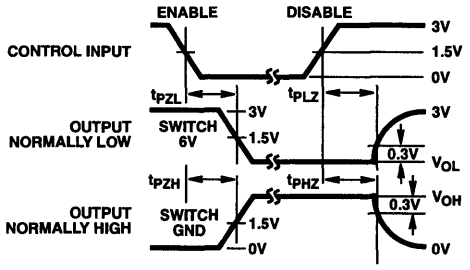


FIGURE 8. ENABLE AND DISABLE TIMING

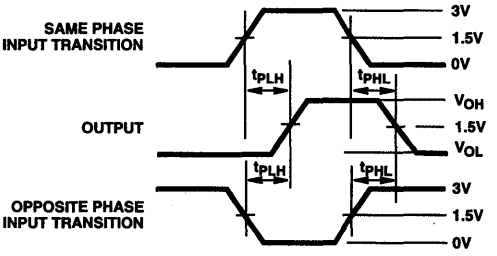


FIGURE 9. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74LPT16652

December 1996

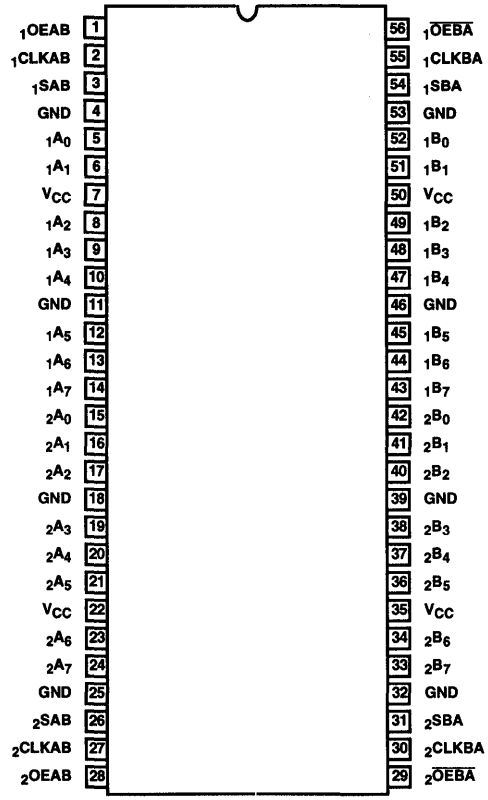
Fast CMOS 16-Bit Registered Transceiver

Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Families of Product
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise.

Pinout

CD74LPT16652 (SSOP, TSSOP)
TOP VIEW



Description

The CD74LPT16652 is a 16-bit registered transceiver organized as two independent 8-bit bus transceivers. It is designed with Three-State D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable controls ($_X$OEAB and $_X\overline{OEBA}$) to control the transceiver functions. The Select ($_X$SAB and $_X$SBA) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The CD74LPT16652 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

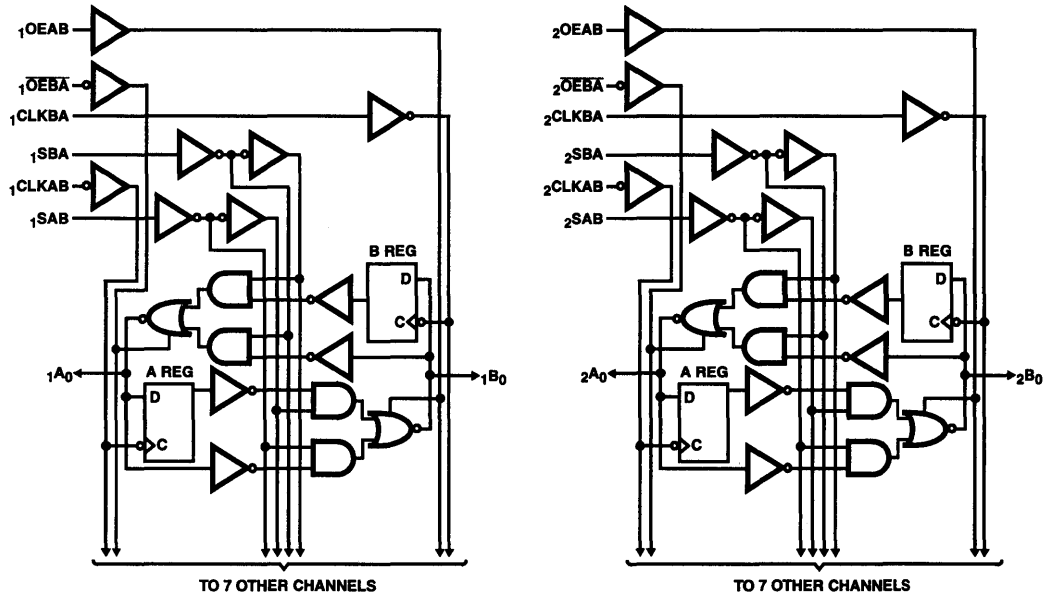
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CD74LPT16652AMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16652ASM	-40 to 85	56 Ld SSOP	M56.300-P
CD74LPT16652MT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16652SM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4211.1**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

	INPUTS						DATA I/O	
FUNCTION/OPERATION	**xOEAB**	**$x\overline{OEBA}$**	**xCLKAB**	**xCLKBA**	**xSAB**	**xSBA**	**$x^{A}x$**	**$x^{B}x$**
Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	L	H	↑	↑	X	X		
Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified (Note 2)
Store A in Both Registers	H	H	↑	↑	X (Note 3)	X	Input	Output
Hold A, Store B	L	X	H or L	↑	X	X	Unspecified (Note 2)	Input
Store B in Both Registers	L	L	↑	↑	X	X (Note 3)	Output	Input
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored A Data to B Bus	H	H	H or L	X	H	X		
Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

NOTES:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   ↑= LOW-to-HIGH transition
2. The data output functions may be enabled or disabled by various signals at the xOEAB or $x\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
3. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.

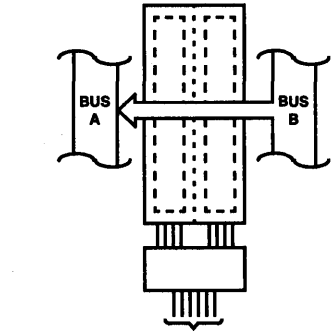


FIGURE 1. REAL-TIME TRANSFER BUS B TO A

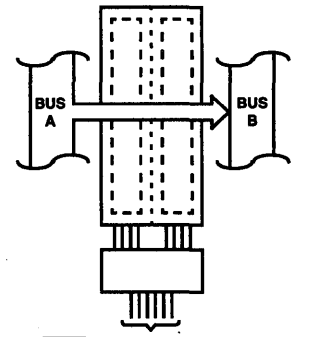


FIGURE 2. REAL-TIME TRANSFER BUS A TO B

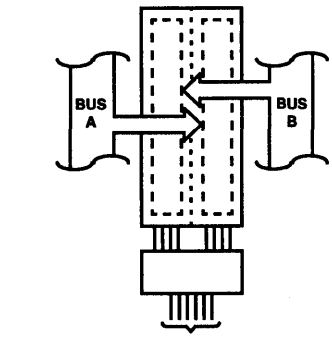


FIGURE 3. STORAGE FROM A AND/OR B

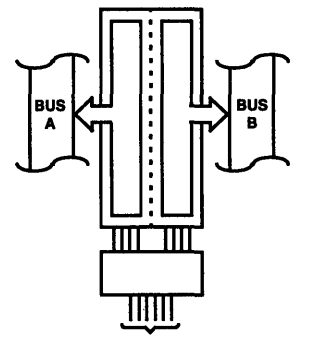


FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

Pin Descriptions

PIN NAME	DESCRIPTION
x^Ax	Data Register A Inputs Data Register B Outputs
x^Bx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
xSAB, xSBA	Output Data Source Select Inputs
xOEAB, $x\overline{OEBA}$	Output Enable Inputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 9)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
Short Circuit Current (Note 8)	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 11)	-	2.0	30	µA
Dynamic Power Supply Current (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $_X$OEBA = $_X\overline{OEBA}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $_X$OEBA = $_X\overline{OEBA}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $_X$OEBA = $_X\overline{OEBA}$ = GND 16 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 13)	mA

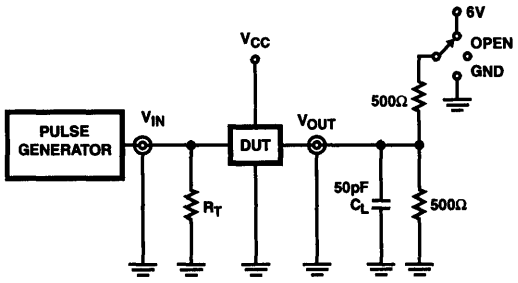
Switching Specifications Over Operating Range (Note 15)

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPT16652		CD74LPT16652A		UNITS
			(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	ns
Output Enable Time $_x$OEAB or $_x\overline{OEBA}$ to Bus	t_{PZH}, t_{PZL}		2.0	14.0	2.0	9.8	ns
Output Disable Time (Note 18) $_x$OEAB or $_x\overline{OEBA}$ to Bus	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	6.3	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}		2.0	9.0	2.0	6.3	ns
Propagation Delay $_x$SBA or $_x$SAB to Bus	t_{PLH}, t_{PHL}		2.0	11.0	2.0	7.7	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}		4.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H		2.0	-	1.5	-	ns
Clock Pulse Width HIGH or LOW (Note 18)	t_W		6.0	-	5.0	-	ns
Output Skew (Note 19)	$t_{SK(O)}$		-	0.5	-	0.5	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is guaranteed but not tested.
9. $V_{OH} = V_{CC}$ - 0.6V at rated current.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input; all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
15. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.
18. This parameter is guaranteed but not production tested.
19. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

20. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 5. TEST CIRCUIT

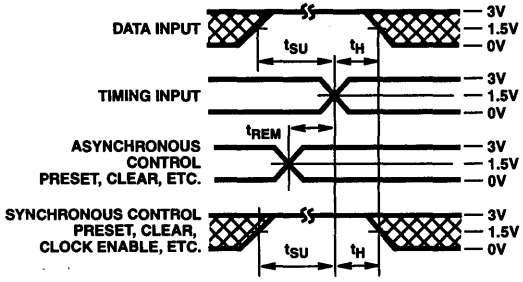


FIGURE 6. SETUP, HOLD, AND RELEASE TIMING

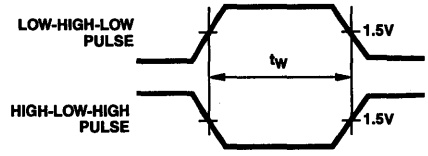


FIGURE 7. PULSE WIDTH

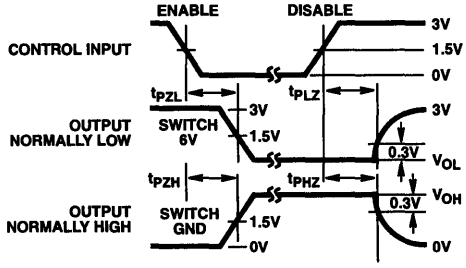


FIGURE 8. ENABLE AND DISABLE TIMING

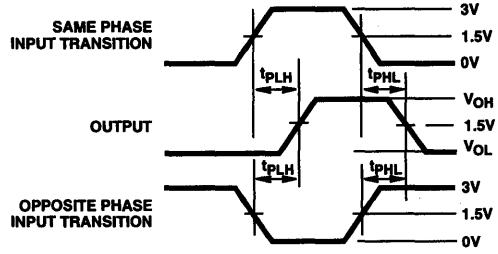


FIGURE 9. PROPAGATION DELAY

CD74LPT16827

December 1996

Fast CMOS 3.3V 20-Bit Buffer

Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Family
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT16827AMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16827ASM	-40 to 85	56 Ld SSOP	M56.300-P
CD74LPT16827BMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16827BSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

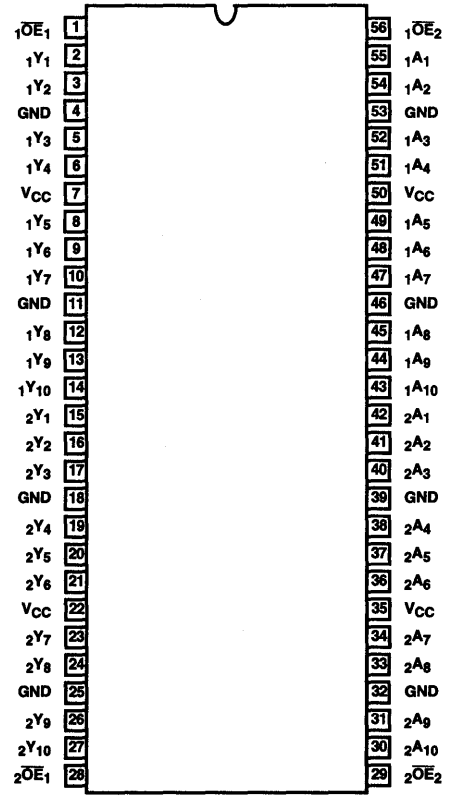
Description

The CD74LPT16827 is a 20-bit wide bus driver designed to provide buffering and high-performance bus interfacing for wide data/address paths or busses with parity. Two pair of nanded output enable controls allow the device to be operated as two 10-bit buffers or as one 20-bit buffer. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The CD74LPT16827 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout

CD74LPT16827 (SSOP, TSSOP)
TOP VIEW

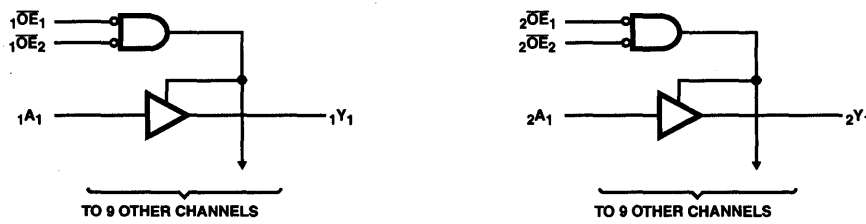


3

3.3V LPT

File Number 4212.2

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUT
$_X\overline{OE}_1$	$_X\overline{OE}_2$	$_XA_X$	$_XY_X$
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z= High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_X\overline{OE}_X$	Output Enable Inputs (Active LOW)
$_XA_X$	Data Inputs
$_XY_X$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . $-40^{o}C$ to $85^{o}C$
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^{o}C$ to $85^{o}C$, $V_{CC} = 2.7V$ to $3.6V$							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	$V_{IN} = 5.5V$	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	$V_{OUT} = 5.5V$	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, $I_{IN} = -18mA$		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	$V_{CC} = 3.3V$, $V_{IN} = V_{IH}$ or V_{IL}, $V_O = 1.5V$ (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	$V_{CC} = 3.3V$, $V_{IN} = V_{IH}$ or V_{IL}, $V_O = 1.5V$ (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -0.1mA$	$V_{CC} - 0.2$	-	-	V
			$I_{OH} = -3mA$	2.4	3.0	-	V
		$V_{CC} = 3.0V$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -8mA$	2.4 (Note 7)	3.0	-	V
			$I_{OH} = -24mA$	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 0.1mA$	-	-	0.2	V
			$I_{OL} = 16mA$	-	0.2	0.4	V
			$I_{OL} = 24mA$	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤4.5V		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = V_{CC} - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 11)	mA

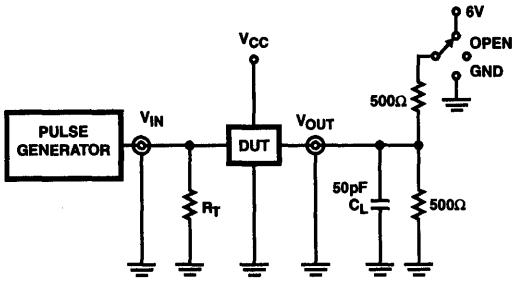
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT16827A		CD74LPT16827B		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay A_N to Y_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.0	ns
		C_L = 300pF R_L = 500Ω (Note 16)	1.5	15.0	1.5	13.0	ns
Output Enable Time $\overline{OE}_N$ to Y_N	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	9.5	1.5	8.0	ns
		C_L = 300pF R_L = 500Ω (Note 16)	1.5	23.0	1.5	15.0	ns
Output Disable Time (Note 16) $\overline{OE}_N$ to Y_N	t_{PHZ}, t_{PLZ}	C_L = 5pF R_L = 500Ω	1.5	8.5	1.5	6.0	ns
		C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	7.0	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC}$ - 0.6V at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

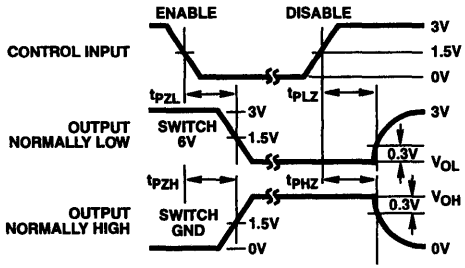


FIGURE 2. ENABLE AND DISABLE TIMING

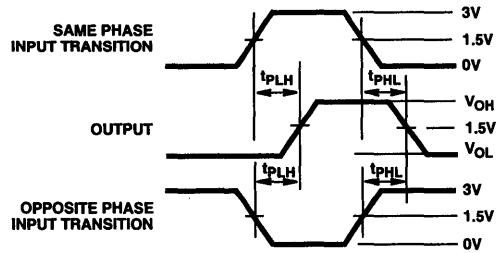


FIGURE 3. PROPAGATION DELAY

CD74LPT16952

December 1996

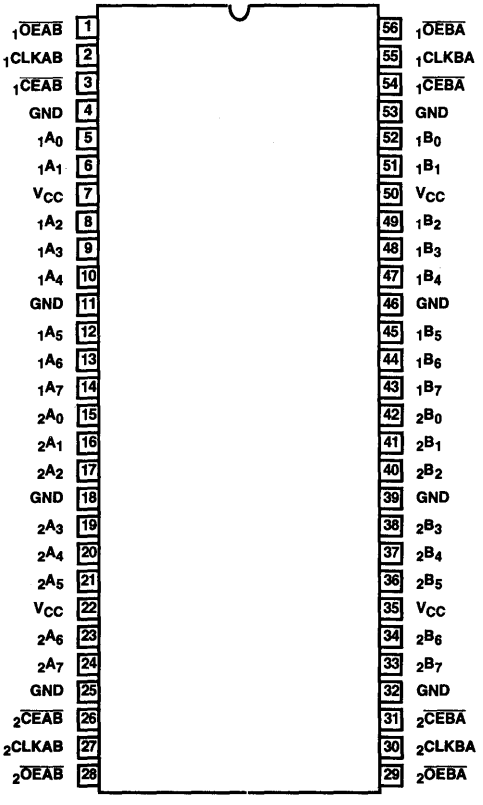
Fast CMOS 3.3V 16-Bit Registered Transceiver

Features

- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
- Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Pinout

CD74LPT16952 (SSOP, TSSOP)
TOP VIEW



Description

Harris' CD74LPT16952 is produced in an advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The CD74LPT16952 is a 16-bit registered transceiver organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($_x\overline{CEAB}$) input must be LOW in order to enter data from $_xA_x$. The data present on the A port will be clocked on the B register when $_x$CLKAB toggles from LOW-to-HIGH. The $_x\overline{OEAB}$ control performs the output enable function on the B port. Control of data from B to A is similar, but uses the $_x\overline{CEAB}$, $_x$CLKAB, and $_x\overline{OEAB}$ inputs. By connecting the control pins of the two independent transceivers together, a full 16-bit operation can be achieved. The output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74LPT16952 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

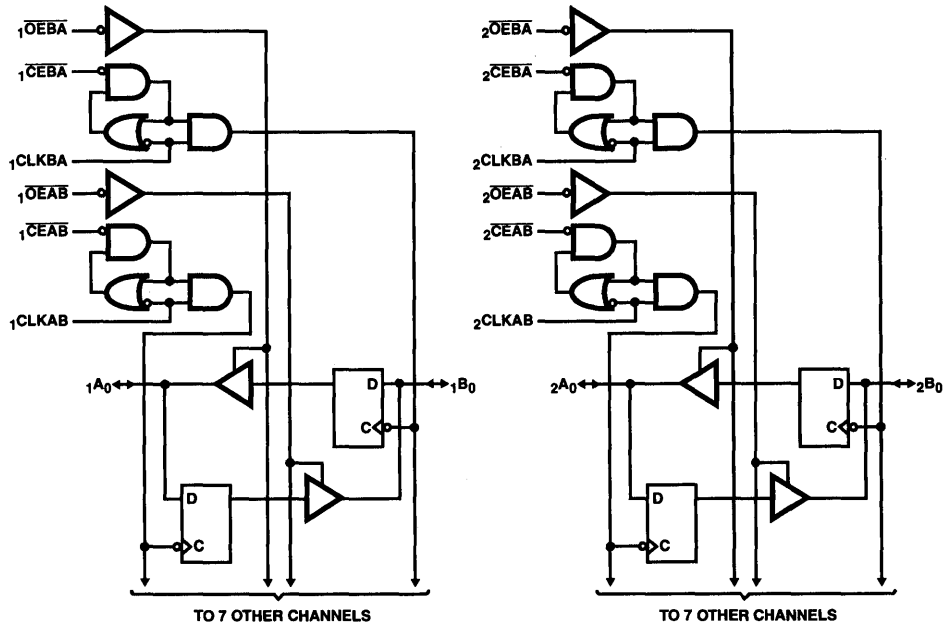
PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
CD74LPT16952AMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16952ASM	-40 to 85	56 Ld SSOP	M56.300-P
CD74LPT16952BMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74LPT16952BSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4213.2**

Functional Block Diagram



TRUTH TABLE (NOTES 1, 2)

INPUTS				OUTPUTS
$_X\overline{CEAB}$	$_X$CLKAB	$_X\overline{OEAB}$	$_XA_X$	$_XB_X$
H	X	L	X	B (Note 3)
X	L	L	X	B (Note 3)
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	High Z

NOTES:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care or Irrelevant
   ↑ = LOW-to-HIGH Transition
   Z = High Impedance
2. A-to-B data flow shown. B-to-A flow control is the same, except using $_X\overline{CEBA}$, $_X$CLKBA, and $_X\overline{OEBA}$.
3. Level of B before the indicated steady-state input conditions were established.

Pin Description

PIN NAME	DESCRIPTION
$_X\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$_X\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$_X\overline{CEAB}$	A-to-B Clock Enable Input (Active LOW)
$_X\overline{CEBA}$	B-to-A Clock Enable Input (Active LOW)
$_X$CLKAB	A-to-B Clock Input
$_X$CLKBA	B-to-A Clock Input
$_XA_X$	A-to-B Data Inputs or B-to-A Three-State Outputs
$_XB_X$	B-to-A Data Inputs or A-to-B Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 9)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
Short Circuit Current (Note 8)	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 11)	-	2.0	30	µA
Dynamic Power Supply Current (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 13)	mA

Switching Specifications Over Operating Range (Note 15)

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPT16952A (NOTE 17) MIN	CD74LPT16952A MAX	CD74LPT16952B (NOTE 17) MIN	CD74LPT16952B MAX	UNITS
Propagation Delay xCLKAB, xCLKBA to xB_x, xA_x	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	7.5	ns
Output Enable Time $x\overline{OEBA}$, $x\overline{OEAB}$ to xA_x, xB_x	t_{PZH}, t_{PZL}		1.5	10.5	1.5	8.0	ns
Output Disable Time (Note 18) $x\overline{OEBA}$, $x\overline{OEAB}$ to xA_x, xB_x	t_{PHZ}, t_{PLZ}		1.5	10.0	1.5	7.5	ns
Setup Time HIGH or LOW, xA_x, xB_x to xCLKAB, xCLKBA	t_{SU}		2.5	-	2.5	-	ns

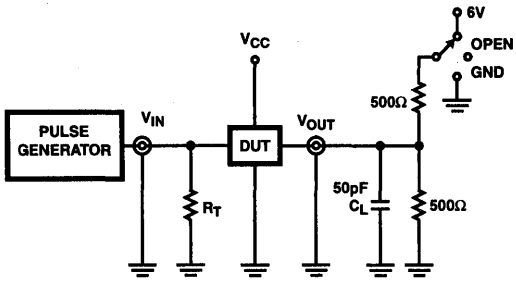
Switching Specifications Over Operating Range (Note 15) **(Continued)**

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPT16952A		CD74LPT16952B		UNITS
			(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	
Hold Time HIGH or LOW, $_xA_x$, $_xB_x$ to $_x$CLKAB, $_x$CLKBA	t_H	C_L = 50pF R_L = 500Ω	2.0	-	2.0	-	ns
Setup Time HIGH or LOW, $_x\overline{CEAB}$, $_x\overline{CEBA}$ to $_x$CLKAB, $_x$CLKBA	t_{SU}		3.0	-	3.0	-	ns
Hold Time HIGH or LOW, $_x\overline{CEAB}$, $_x\overline{CEBA}$ to $_x$CLKAB, $_x$CLKBA	t_H		2.0	-	2.0	-	ns
Pulse Width HIGH (Note 18) or LOW, $_x$CLKAB or $_x$CLKBA	t_W		3.0	-	3.0	-	ns
Output Skew (Note 19)	$t_{SK(O)}$		-	0.5	-	0.5	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is guaranteed but not tested.
9. $V_{OH} = V_{CC} - 0.6V$ at rated current.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input; all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
15. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.
18. This parameter is guaranteed but not production tested.
19. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

20. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

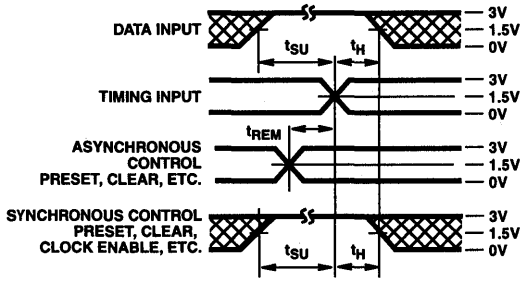


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

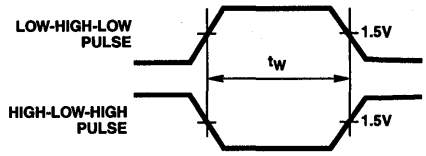


FIGURE 3. PULSE WIDTH

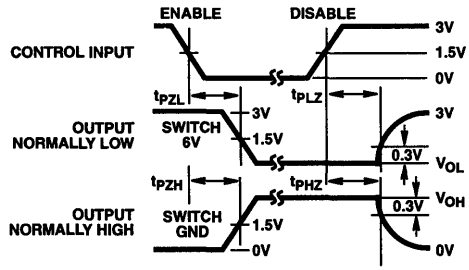


FIGURE 4. ENABLE AND DISABLE TIMING

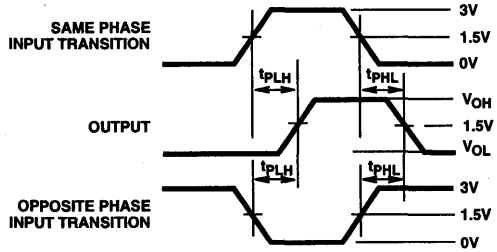


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74LPT241

December 1996

Fast CMOS 3.3V 8-Bit Buffer/Line Driver

Features

- **Advanced 0.6 micron CMOS Technology**
- **Compatible with LCX™ Families of Products**
- **Supports 5V Tolerant Mixed Signal Mode Operation**
  - **Input Can Be 3V or 5V**
  - **Output Can Be 3V or Connected to 5V Bus**
- **Advanced Low Power CMOS Operation**
- **Excellent Output Drive Capability:**
  - **Balanced Drives (24mA Sink and Source)**
- **Low Ground Bounce Outputs**
- **Hysteresis on All Inputs**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT241AM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT241AQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT241CM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT241CQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT241M	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT241QM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and ree

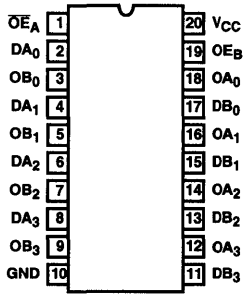
Description

The CD74LPT241 is an 8-bit buffer/line driver designed for driving high capacitive memory loads. With its balanced-drive characteristics, this high-speed, low power device provides lower ground bounce, transmission line matching of signals, fewer line reflections and lower EMI and RFI effects. This makes it ideal for driving on-board buses and transmission lines.

The CD74LPT241 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout

CD74LPT241
(SOIC, QSOP)
TOP VIEW

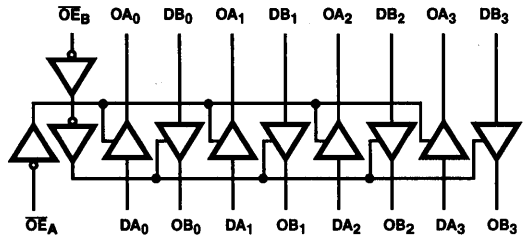


3

3.3V LPT

File Number **4196.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$\overline{OE}_A$	OE_B	D_{XX}	O_{XX}
L	H	L	L
L	H	H	H
H	L	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}_A$,OE_B	Three-State Output Enable Inputs
D_{XX}	Data Inputs
O_{XX}	Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	87
QSOP Package	110

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$				±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = VCC - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}_X$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $\overline{OE}_X$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $\overline{OE}_X$ = GND 8 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 11)	mA

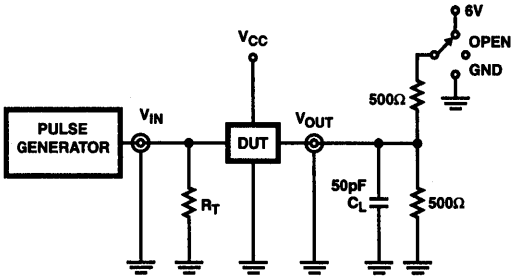
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT241 (NOTE 15) MIN	CD74LPT241 MAX	CD74LPT241A (NOTE 15) MIN	CD74LPT241A MAX	CD74LPT241C (NOTE 15) MIN	CD74LPT241C MAX	UNITS
Propagation Delay D_{XX} to O_{XX}	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	ns
Output Enable Time $\overline{OE}_A/OE_B$ to O_{XX}	t_{PHZ} t_{PZL}		1.5	8.0	1.5	6.2	1.5	5.8	ns
Output Disable Time (Note 16) $\overline{OE}_A/OE_B$ to O_{XX}	t_{PHZ} t_{PLZ}		1.5	7.0	1.5	5.6	1.5	5.2	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC} - 0.6V$ at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

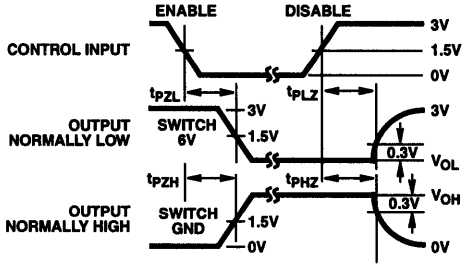


FIGURE 2. ENABLE AND DISABLE TIMING

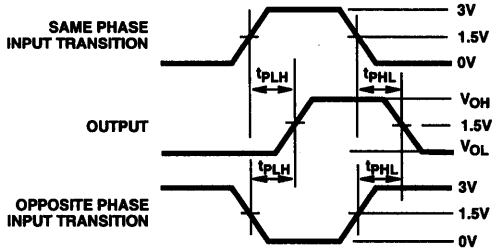


FIGURE 3. PROPAGATION DELAY

CD74LPT244

December 1996

Fast CMOS 3.3V 8-Bit Buffer/Line Driver

Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Low Ground Bounce Outputs
- Hysteresis on All Inputs

Description

The CD74LPT244 is an 8-bit buffer/line driver designed for driving high capacitive memory loads. With its balanced-drive characteristics, this high-speed, low power device provides lower ground bounce, transmission line matching of signals, fewer line reflections and lower EMI and RFI effects. This makes it ideal for driving on-board buses and transmission lines.

The CD74LPT244 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

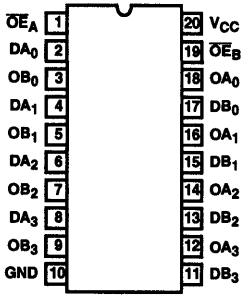
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT244AM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT244AQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT244CM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT244CQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT244M	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT244QM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

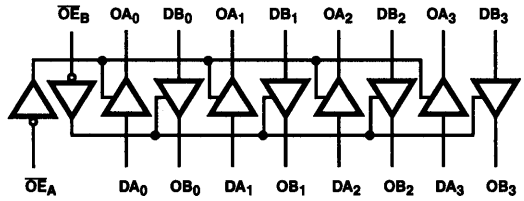
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74LPT244
(SOIC, QSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$\overline{OE}_A$	$\overline{OE}_B$	D_{XX}	O_{XX}
L	L	L	L
L	L	H	H
H	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}_A$,$\overline{OE}_B$	Three-State Output Enable Inputs (Active LOW)
D_{XX}	Data Inputs
O_{XX}	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	87
QSOP Package	110

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$				±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = VCC - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}_X$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $\overline{OE}_X$ = GND One Bit Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $\overline{OE}_X$ = GND 8 Bits Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 11)	mA

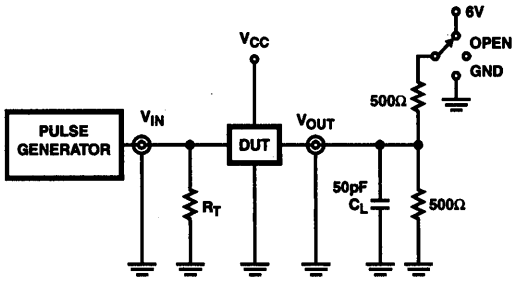
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT244		CD74LPT244A		CD74LPT244C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay D_{XX} to O_{XX}	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	ns
Output Enable Time $\overline{OE}_X$ to O_{XX}	t_{PZH} t_{PZL}		1.5	8.0	1.5	6.2	1.5	5.8	ns
Output Disable Time (Note 16) $\overline{OE}_X$ to O_{XX}	t_{PHZ} t_{PLZ}		1.5	7.0	1.5	5.6	1.5	5.2	ns
Output Disable (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC} - 0.6V$ at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

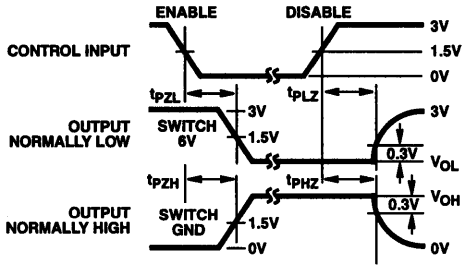


FIGURE 2. ENABLE AND DISABLE TIMING

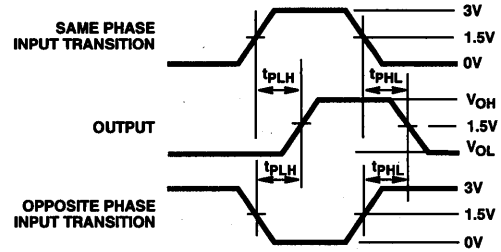


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74LPT245

December 1996

Fast CMOS 3.3V 8-Bit Bidirectional Transceiver

Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Low Ground Bounce Outputs
- Hysteresis on All Inputs

Description

The CD74LPT245 is an 8-bit bidirectional transceiver designed for asynchronous two-way communication between data buses. The transmit/receive input pin ($T/\overline{R}$) determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports, and receive (active LOW) from B ports to A ports. The output enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The CD74LPT245 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

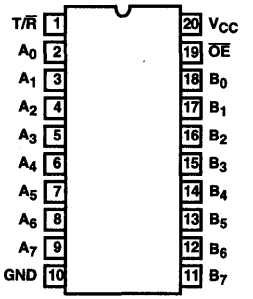
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT245AM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT245AQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT245CM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT245CQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT245M	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT245QM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

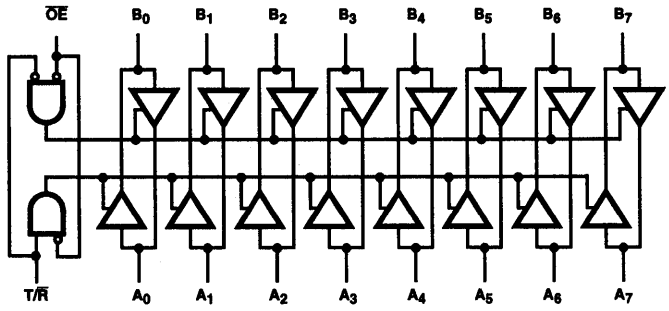
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74LPT245
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

(NOTE 1) INPUTS		(NOTE 1) OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
T/$\overline{R}$	Direction Control Input
A_7-A_0	Side A Inputs or Three-State Outputs
B_7-B_0	Side B Inputs or Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	87
QSOP Package	110

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$				±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = VCC - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $\overline{OE}$ = GND 8 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 11)	mA

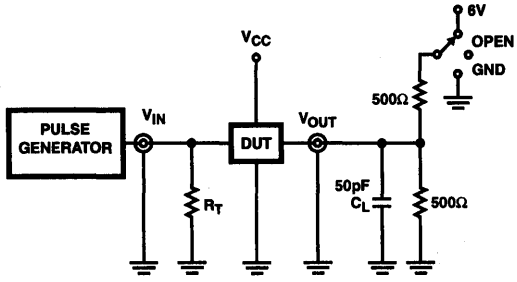
Switching Specifications Over Operating Range (NOTE 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT245		CD74LPT245A		CD74LPT245C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay A to B, B to A	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	ns
Output Enable Time $\overline{OE}$ to A or B	t_{PZH}, t_{PZL}		1.5	8.5	1.5	6.2	1.5	5.8	ns
Output Disable Time $\overline{OE}$ to A or B (Note 16)	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.0	1.5	4.8	ns
Output Enable Time T/$\overline{R}$ to A or B	t_{PZH}, t_{PZL}		1.5	8.5	1.5	6.2	1.5	5.8	ns
Output Disable Time T/$\overline{R}$ to A or B (Note 16)	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.0	1.5	4.8	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC}$ - 0.6V at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

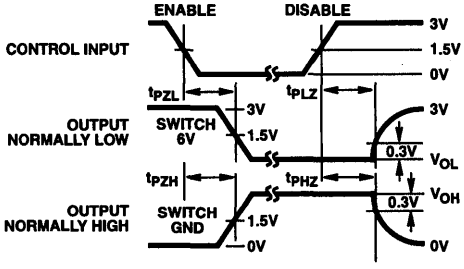


FIGURE 2. ENABLE AND DISABLE TIMING

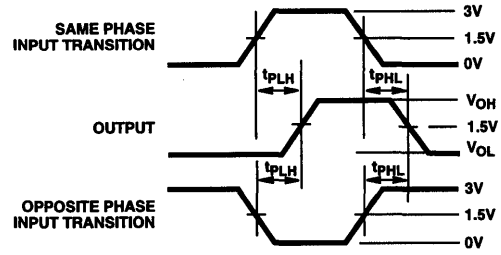


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74LPT373

December 1996

Fast CMOS 3.3V 8-Bit Transparent Latch

Features

- **Advanced 0.6 micron CMOS Technology**
- **Compatible with LCX™ Families of Products**
- **Supports 5V Tolerant Mixed Signal Mode Operation**
  - **Input Can Be 3V or 5V**
  - **Output Can Be 3V or Connected to 5V Bus**
- **Advanced Low Power CMOS Operation**
- **Excellent Output Drive Capability:**
  - **Balanced Drives (24mA Sink and Source)**
- **Low Ground Bounce Outputs**
- **Hysteresis on All Inputs**

Description

The CD74LPT373 is an 8-bit transparent latch designed with three-state outputs and is intended for bus oriented applications. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

The CD74LPT373 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

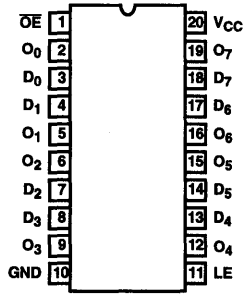
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CD74LPT373AM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT373AQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT373CM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT373CQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT373M	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT373QM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

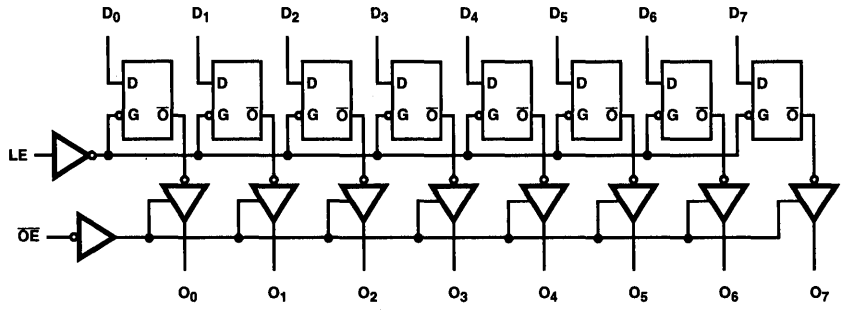
CD74LPT373
(QSOP, SOIC)
TOP VIEW



3 3.3V LPT

File Number **4199.1**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
D_N	LE	$\overline{OE}$	O_N
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
LE	Latch Enable Input (Active HIGH)
D_7-D_0	Data Inputs
O_7-O_0	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
SOIC Package 87
QSOP Package 110
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = VCC - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $\overline{OE}$ = GND 8 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 11)	mA

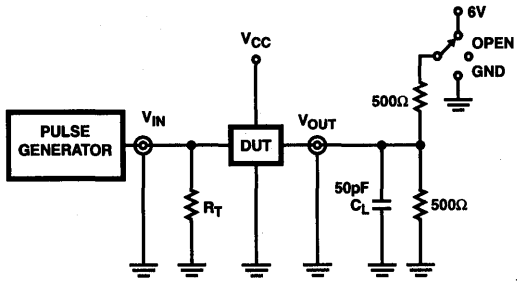
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT373		CD74LPT373A		CD74LPT373C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay D_X to O_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	ns
Propagation Delay LE to O_X	t_{PLH}, t_{PHL}		2.0	8.5	2.0	8.5	2.0	5.5	ns
Output Enable Time $\overline{OE}$ to O_X	t_{PZH}, t_{PZL}		1.5	8.5	1.5	6.5	1.5	5.5	ns
Output Disable Time (Note 16) $\overline{OE}$ to O_X	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.5	1.5	5.0	ns
Setup Time HIGH or LOW, D_X to LE	t_{SU}		2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, D_X to LE	t_H		1.5	-	1.5	-	1.5	-	ns
LE Pulse Width (Note 16) HIGH	t_W		6.0	-	5.0	-	5.0	-	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC}$ - 0.6V at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

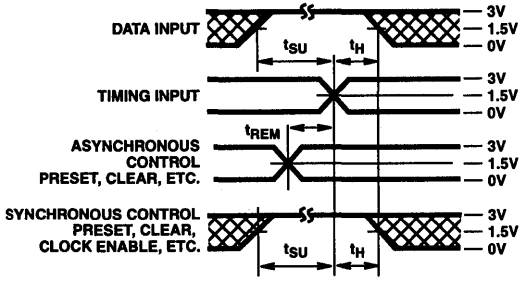


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

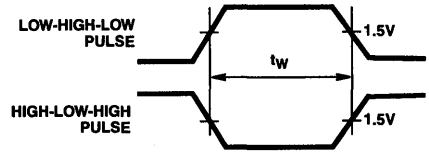


FIGURE 3. PULSE WIDTH

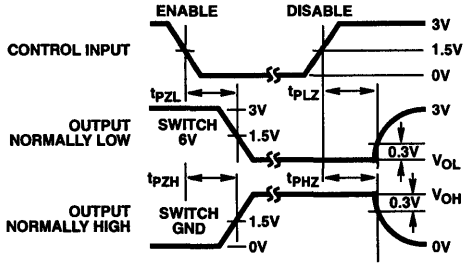


FIGURE 4. ENABLE AND DISABLE TIMING

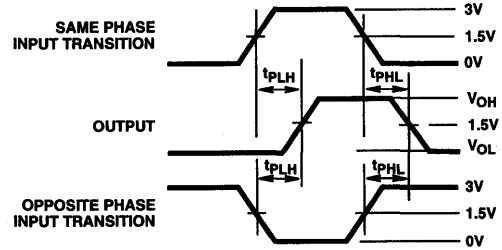


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74LPT541

December 1996

Fast CMOS 3.3V 8-Bit Buffer/Line Driver

Features

- **Advanced 0.6 micron CMOS Technology**
- **Compatible with LCX™ Families of Products**
- **Supports 5V Tolerant Mixed Signal Mode Operation**
  - **Input Can Be 3V or 5V**
  - **Output Can Be 3V or Connected to 5V Bus**
- **Advanced Low Power CMOS Operation**
- **Excellent Output Drive Capability:**
  - **Balanced Drives (24mA Sink and Source)**
- **Low Ground Bounce Outputs**
- **Hysteresis on All Inputs**

Description

The CD74LPT541 is an 8-bit buffer/line driver designed for driving high capacitive memory loads. With its balanced-drive characteristics, this high-speed, low power device provides lower ground bounce, transmission line matching of signals, fewer line reflections and lower EMI and RFI effects. This makes it ideal for driving on-board buses and transmission lines. This device offers a flow-through organization for ease of board layout.

The CD74LPT541 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

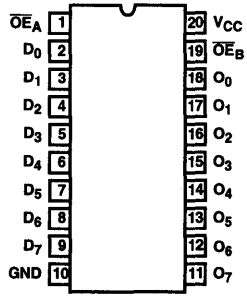
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT541AM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT541AQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT541CM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT541CQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT541M	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT541QM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

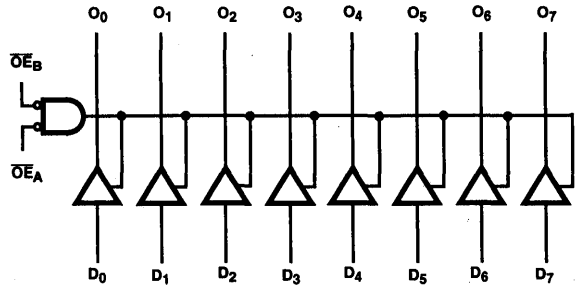
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74LPT541
(SOIC, QSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$\overline{OE}_A$	$\overline{OE}_B$	D_X	O_X
L	L	L	L
L	L	H	H
H	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}_A$,$\overline{OE}_B$	Three-State Output Enable Inputs (Active LOW)
D_X	Data Inputs
O_X	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	87
QSOP Package	110

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}_X$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $\overline{OE}_X$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $\overline{OE}_X$ = GND 8 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 11)	mA

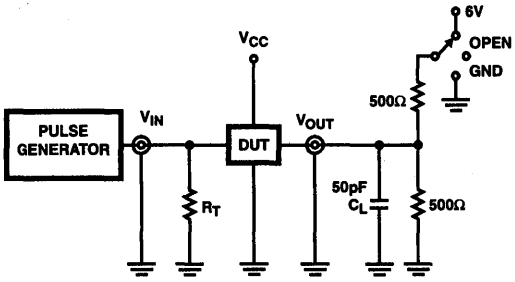
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT541		CD74LPT541A		CD74LPT541C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay D_X to O_X	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	1.5	6.0	1.5	4.8	1.5	4.1	ns
Output Enable Time $\overline{OE}_X$ to O_X	t_{PZH}, t_{PZL}		1.5	9.5	1.5	6.2	1.5	5.8	ns
Output Disable Time (Note 16) $\overline{OE}_X$ to O_X	t_{PHZ}, t_{PLZ}		1.5	6.5	1.5	5.6	1.5	5.2	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC}$ - 0.6V at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and waveforms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

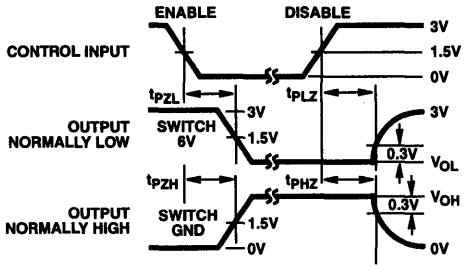


FIGURE 2. ENABLE AND DISABLE TIMING

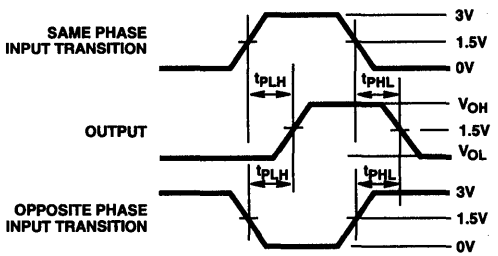


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74LPT543

December 1996

Fast CMOS 3.3V 8-Bit Latched Transceiver

Features

- **Advanced 0.6 micron CMOS Technology**
- **Compatible with LCX™ Families of Products**
- **Supports 5V Tolerant Mixed Signal Mode Operation**
  - **Input Can Be 3V or 5V**
  - **Output Can Be 3V or Connected to 5V Bus**
- **Advanced Low Power CMOS Operation**
- **Active Bus-Hold Circuitry**
- **Excellent Output Drive Capability:**
  - **Balanced Drives (24mA Sink and Source)**
- **Low Ground Bounce Outputs**
- **Hysteresis on All Inputs**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT543AM	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT543AQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT543CM	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT543CQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT543M	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT543QM	-40 to 85	24 Ld QSOP	M24.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

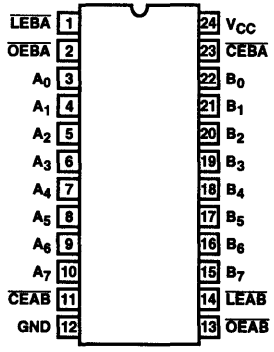
Description

The CD74LPT543 is an 8-bit wide non-inverting transceiver designed with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0-A_7 or to take data from B_0-B_7, as indicated in the Truth Table. With $\overline{CEAB}$ LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs. Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The CD74LPT543 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

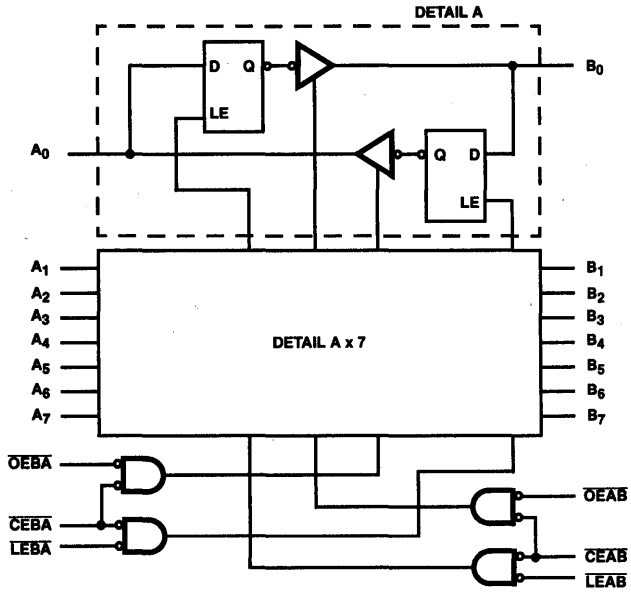
Pinout

CD74LPT543
(QSOP, SOIC)
TOP VIEW



File Number **4256**

Functional Block Diagram



TRUTH TABLE (NOTES 1, 3)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-TO-B	B_0 - B_7
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs (Note 2)

NOTES:

1. A-to-B data flow is shown. B-to-A flow control is the same except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
2. Before $\overline{LEAB}$ LOW-to-HIGH Transition
3. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care or Irrelevant
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0 - A_7	A-to-B Data Inputs or B-to-A Three-State Outputs
B_0 - B_7	B-to-A Data Inputs or B-to-A Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
SOIC Package	75
QSOP Package	100

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 9)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
Short Circuit Current (Note 8)	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 11)	-	2.0	30	µA
Dynamic Power Supply (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA} = V_{CC}$ One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA} = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA} = V_{CC}$ 8 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 13)	mA

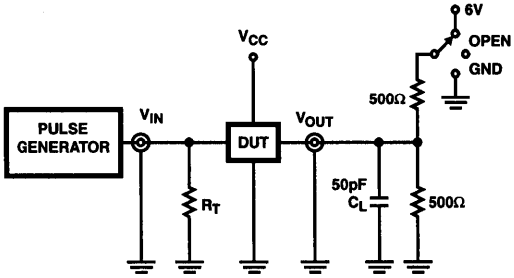
Switching Specifications Over Operating Range (NOTE 15)

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPT543		CD74LPT543A		CD74LPT543C		UNITS
			(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	(NOTE 17) MIN	MAX	
Propagation Delay Transparent Mode A_N to B_N or B_N to A_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	ns
Propagation Delay $\overline{LEBA}$ to A_N $\overline{LEAB}$ to B_N	t_{PLH}, t_{PHL}		2.5	12.5	2.5	8.0	2.5	7.0	ns
Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N	t_{PZH}, t_{PZL}		2.0	12.0	2.0	9.0	2.0	8.0	ns
Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	7.5	2.0	6.5	ns
Setup Time HIGH or LOW, AN or B_N to $\overline{LEAB}$ or $\overline{LEBA}$	t_{SU}		3.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, A_N or B_N to $\overline{LEAB}$ or $\overline{LEBA}$	t_H		2.0	-	2.0	-	2.0	-	ns
$\overline{LEAB}$ or $\overline{LEBA}$ Pulse Width LOW	t_W		5.0	-	5.0	-	5.0	-	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is guaranteed but not tested.
9. $V_{OH} = V_{CC}$ - 0.6V at rated current.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input; all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
15. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V 0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

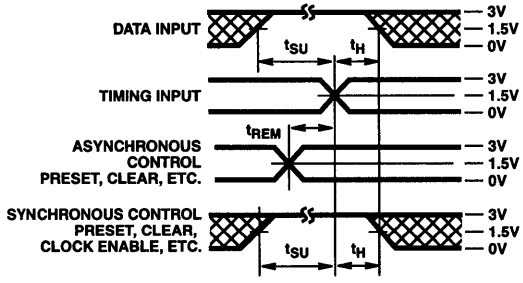


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

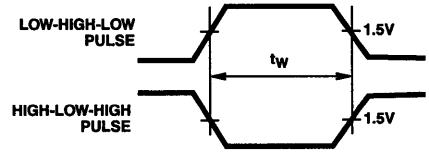


FIGURE 3. PULSE WIDTH

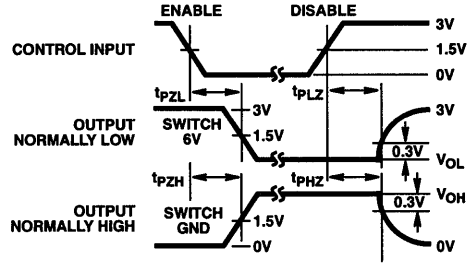


FIGURE 4. ENABLE AND DISABLE TIMING

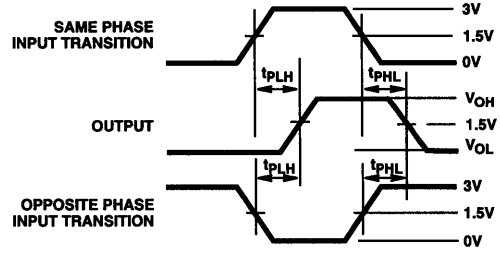


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74LPT573

December 1996

Fast CMOS 3.3V 8-Bit Transparent Latch

Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Low Ground Bounce Outputs
- Hysteresis on All Inputs

Description

The CD74LPT573 is an 8-bit transparent latch designed with three-state outputs and is intended for bus oriented applications. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

The CD74LPT573 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

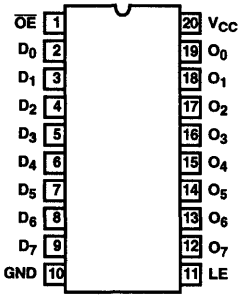
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT573AM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT573AQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT573CM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT573CQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT573M	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT573QM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

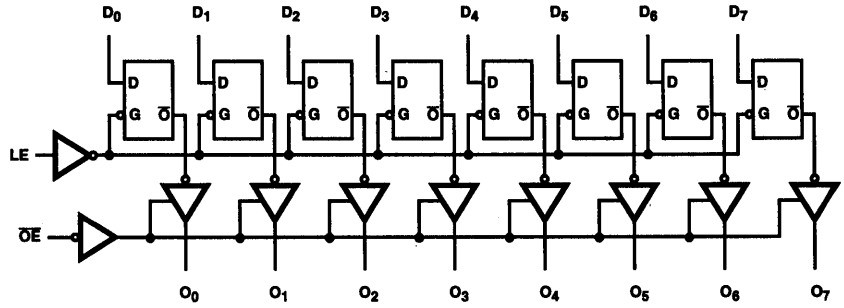
Pinout

CD74LPT573
(QSOP, SOIC)
TOP VIEW



File Number **4201.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
D_N	LE	$\overline{OE}$	O_N
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
LE	Latch Enable Input (Active HIGH)
D_7-D_0	Data Inputs
O_7-O_0	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	87
QSOP Package	110

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = VCC - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $\overline{OE}$ = GND 8 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 11)	mA

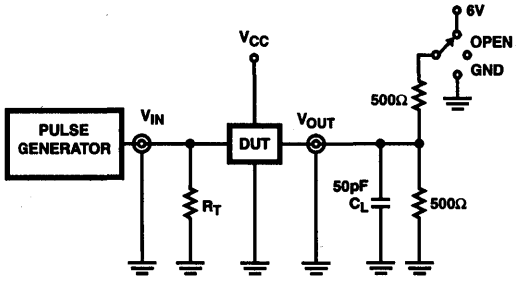
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT573 (NOTE 15) MIN	CD74LPT573 MAX	CD74LPT573A (NOTE 15) MIN	CD74LPT573A MAX	CD74LPT573C (NOTE 15) MIN	CD74LPT573C MAX	UNITS
Propagation Delay D_X to O_X	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	ns
Propagation Delay LE to O_X	t_{PLH}, t_{PHL}		2.0	12.0	2.0	8.5	2.0	5.5	ns
Output Enable Time $\overline{OE}$ to O_X	t_{PZH}, t_{PZL}		1.5	9.5	1.5	6.5	1.5	5.5	ns
Output Disable Time (Note 16) $\overline{OE}$ to O_X	t_{PHZ}, t_{PLZ}		1.5	6.5	1.5	5.5	1.5	5.0	ns
Setup Time HIGH or LOW, D_X to LE	t_{SU}		2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, D_X to LE	t_H		1.5	-	1.5	-	1.5	-	ns
LE Pulse Width HIGH (Note 16)	t_W		6.0	-	5.0	-	5.0	-	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC}$ - 0.6V at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

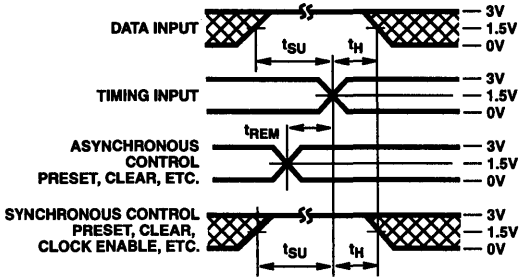


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

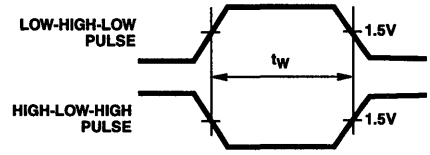


FIGURE 3. PULSE WIDTH

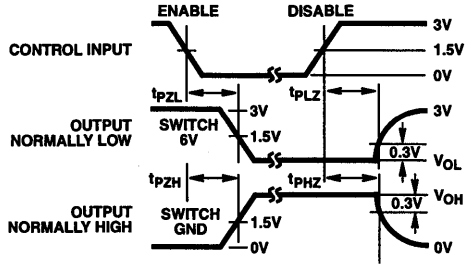


FIGURE 4. ENABLE AND DISABLE TIMING

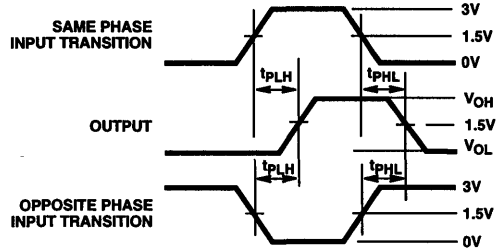


FIGURE 5. PROPAGATION DELAY

CD74LPT646, CD74LPT652

December 1996

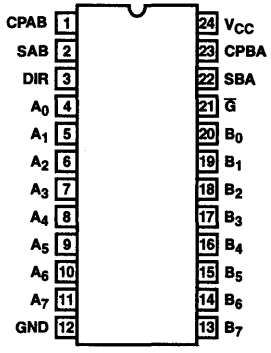
Fast CMOS 3.3V 8-Bit Registered Transceivers

Features

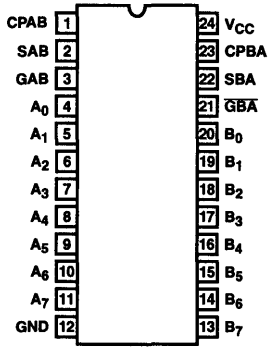
- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Low Ground Bounce Outputs
- Hysteresis on All Inputs

Pinout

CD74FCT646
(QSOP, SOIC)
TOP VIEW



CD74LPT652
(QSOP, SOIC)
TOP VIEW



Description

The CD74LPT646 and CD74LPT652 are designed with a bus transceiver with three-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The CD74LPT652 utilizes GAB and $\overline{GBA}$ signals to control the transceiver functions. The CD74LPT646 utilizes the enable control ($\overline{G}$) and direction pins (DIR) to control the transceiver functions. SAB and SBA control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The CD74LPT646 and CD74LPT652 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

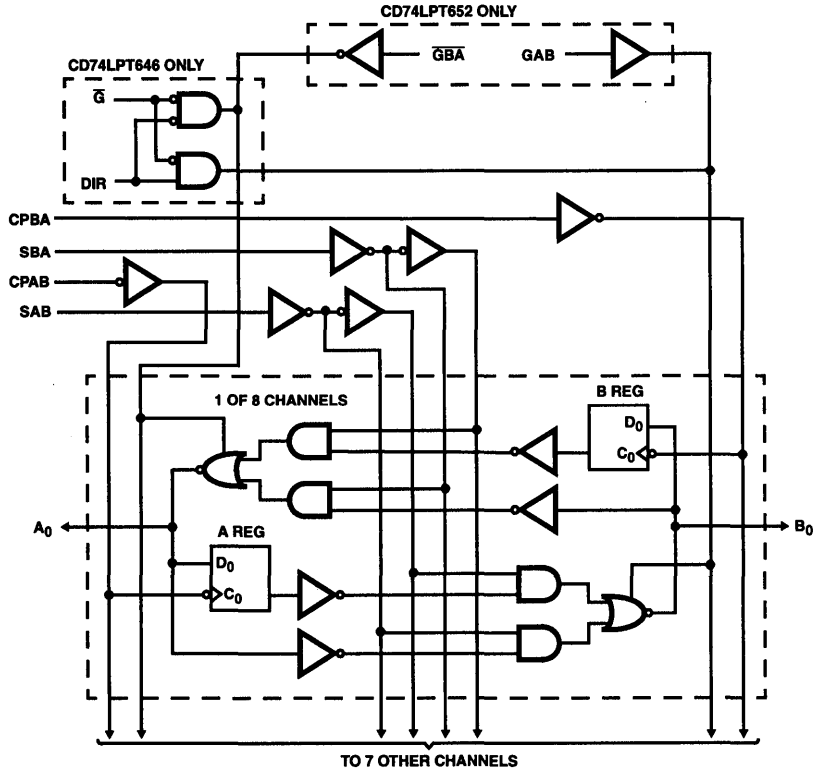
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT646QM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT646AQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT646CQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT646M	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT646AM	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT646CM	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT652QM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT652AQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT652CQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT652M	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT652AM	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT652CM	-40 to 85	24 Ld SOIC	M24.3-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Functional Block Diagram



TRUTH TABLE (CD74LPT646)

FUNCTION/OPERATION	INPUTS						DATA I/O (NOTE 1)	
	$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0 - A_7	B_0 - B_7
Isolation Store A and B Data	H H	X X	H or L ↑	H or L ↑	X X	X X	Input	Input
Real Time B Data to A Bus Stored B Data to A Bus	L L	L L	X X	X H or L	X X	L H	Output	Input
Real Time A Data to B Bus Stored A Data to B Bus	L L	H H	X H or L	X X	L H	X X	Input	Output

TRUTH TABLE (CD74LPT652)

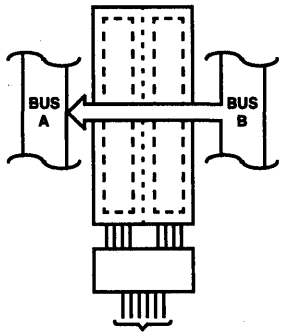
FUNCTION/OPERATION	INPUTS						(NOTES 1, 2) DATA I/O	
	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_0 - A_7	B_0 - B_7
Isolation Store A and B Data	L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input
Store A, Hold B Store A in Both Registers	X H	H H	↑ ↑	H or L ↑	X X (Note 2)	X X	Input Input	Unspecified Output (Note 1)

TRUTH TABLE (CD74LPT652) **(Continued)**

FUNCTION/OPERATION	INPUTS						(NOTES 1, 2) DATA I/O	
	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_0 - A_7	B_0 - B_7
Hold A, Store B Store B in Both Registers	L L	X L	H or L ↑	↑ ↑	X X	X X (Note 2)	Unspecified Output (Note 1)	Input Input
Real Time B Data to A Bus Stored B Data to A Bus	L L	L L	X X	X H or L	X X	L H	Output	Input
Real Time A Data to B Bus Stored A Data to B Bus	H H	H H	X H or L	X X	L H	X X	Input	Output
Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

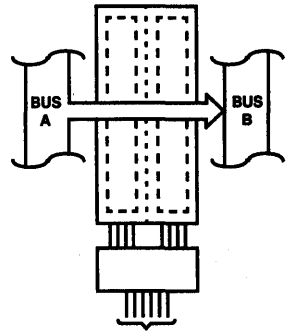
NOTES:

1. The data output functions may be enabled or disabled by various signals at the $\overline{G}$ or DIR for the CD74LPT646 type and GAB or $\overline{GBA}$ for CD74LPT652 type inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. Select Control = L: clocks can occur simultaneously.
   Select Control = H: clocks must be staggered in order to load both registers.
   H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   ↑= LOW-to-HIGH transition



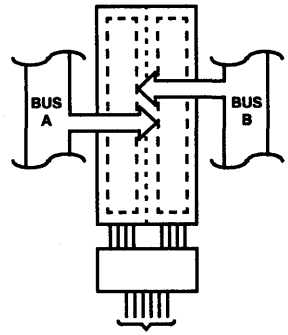
CD74LPT646	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L
CD74LPT652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L

FIGURE 1. REAL-TIME TRANSFER BUS B TO A



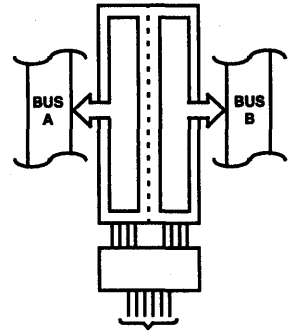
CD74LPT646	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X
CD74LPT652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	H	X	X	L	X

FIGURE 2. REAL-TIME TRANSFER BUS A TO B



CD74LPT646	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X
CD74LPT652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X

FIGURE 3. STORAGE FROM A AND/OR B



CD74LPT646 (NOTE 3)	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	H or L	X	H
	H	L	H or L	X	H	X
CD74LPT652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	L	H or L	H or L	H	H

FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

NOTE:

3. Cannot transfer data to A bus and B bus simultaneously.

Pin Descriptions

PIN NAME	DESCRIPTION
A_0 - A_7	Data Register A Inputs, Data Register B Outputs
B_0 - B_7	Data Register B Inputs, Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs (CD74LPT646)
GAB, $\overline{GBA}$	Output Enable Inputs (CD74LPT652)
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
SOIC Package	75
QSOP Package	100

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 7)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 9)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V
Short Circuit Current (Note 8)	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤4.5V		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	$V_{IN} = V_{CC}$ - 0.6V (Note 11)	-	2.0	30	µA
Dynamic Power Supply (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{G}$ = DIR = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $\overline{G}$ = DIR = GND or GAB = $\overline{GBA}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $\overline{G}$ = DIR = GND or GAB = $\overline{GBA}$ = GND 8 Bits Toggling	$V_{IN} = V_{CC}$ - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 13)	mA

Switching Specifications Over Operating Range (NOTE 15)

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPTxxx (NOTE 17) MIN	CD74LPTxxx MAX	CD74LPTxxxA (NOTE 17) MIN	CD74LPTxxxA MAX	CD74LPTxxxC (NOTE 17) MIN	CD74LPTxxxC MAX	UNITS
CD74LPT646									
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	ns
Output Enable Time $\overline{G}$, DIR to Bus	t_{PZH}, t_{PZL}		2.0	14.0	2.0	9.8	1.5	7.8	ns
Output Disable Time $\overline{G}$, DIR to Bus	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	6.3	1.5	6.3	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}		2.0	9.0	2.0	6.3	1.5	5.7	ns
Propagation Delay SBA or SAB to Bus	t_{PLH}, t_{PHL}		2.0	9.5	2.0	7.7	1.5	6.2	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}		4.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H	C_L = 50pF R_L = 500Ω	2.0	-	1.5	-	1.5	-	ns
Clock Pulse Width HIGH or LOW	t_W		6.0	-	5.0	-	5.0	-	ns

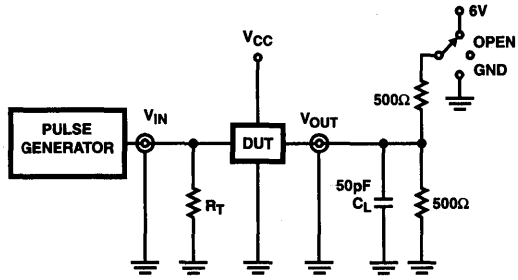
Switching Specifications Over Operating Range (NOTE 15) **(Continued)**

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	CD74LPTxxx (NOTE 17) MIN	CD74LPTxxx MAX	CD74LPTxxxA (NOTE 17) MIN	CD74LPTxxxA MAX	CD74LPTxxxC (NOTE 17) MIN	CD74LPTxxxC MAX	UNITS
CD74LPT652									
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	ns
Output Enable Time $\overline{GBA}$, GAB to Bus	t_{PZH}, t_{PZL}		2.0	14.0	2.0	9.8	1.5	7.8	ns
Output Disable Time $\overline{GBA}$, GAB to Bus	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	6.3	1.5	6.3	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}		2.0	9.0	2.0	6.3	1.5	5.7	ns
Propagation Delay SBA or SAB to Bus	t_{PLH}, t_{PHL}		2.0	9.5	2.0	7.7	1.5	6.2	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}		4.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H		2.0	-	1.5	-	1.5	-	ns
Clock Pulse Width HIGH or LOW	t_W		6.0	-	5.0	-	5.0	-	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is guaranteed but not tested.
9. $V_{OH} = V_{CC}$ - 0.6V at rated current.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input; all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (N_{CP} f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
15. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
16. See test circuit and wave forms.
17. Minimum limits are guaranteed but not tested on Propagation Delays.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 5. TEST CIRCUIT

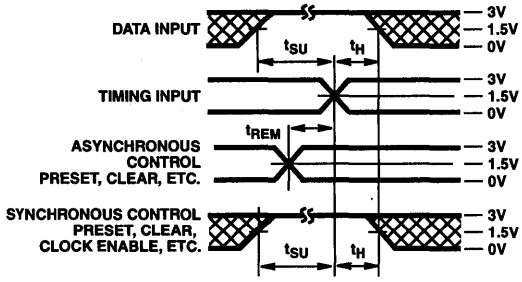


FIGURE 6. SETUP, HOLD, AND RELEASE TIMING

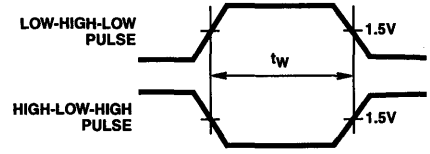


FIGURE 7. PULSE WIDTH

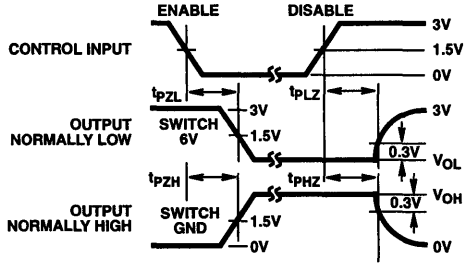


FIGURE 8. ENABLE AND DISABLE TIMING

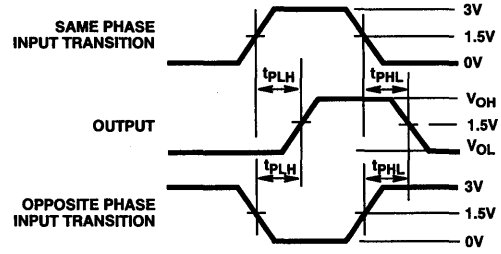


FIGURE 9. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74LPT827

December 1996

Fast CMOS 3.3V 10-Bit Buffer

Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input Can Be 3V or 5V
  - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
- Low Ground Bounce Outputs
- Hysteresis on All Inputs

Description

The CD74LPT827 is a 10-bit wide non-inverting bus driver providing high-performance bus interface buffering for wide address/data paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility. They are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs.

The CD74LPT827 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Ordering Information

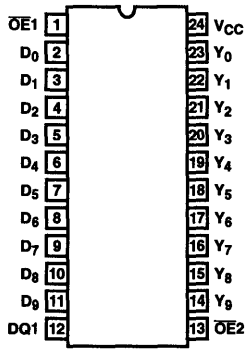
PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CD74LPT827AQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT827BQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT827CQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74LPT827AM	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT827BM	-40 to 85	24 Ld SOIC	M24.3-P
CD74LPT827CM	-40 to 85	24 Ld SOIC	M24.3-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74LPT827
(QSOP, SOIC)
TOP VIEW

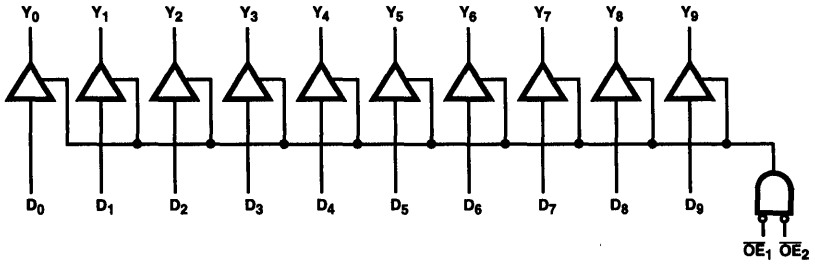


3

3.3V LPT

File Number **4258**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS			OUTPUT
	$\overline{OE}_1$	$\overline{OE}_2$	D_N	Y_N
Transparent	L	L	L	L
	L	L	H	H
Three-State	H	X	X	Z
	X	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Description

PIN NAME	DESCRIPTION
$\overline{OE}_N$	Output Enable Input (Active LOW)
D_0 - D_9	10-Bit Data Inputs
Y_0 - Y_9	10-Bit Data Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
QSOP Package	75
SOIC Package	100

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	5.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±5	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±5	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±5	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±5	µA
High Impedance Output Current (Three-State Output Pins)	I_{OZH}	V_{CC} = Max	V_{OUT} = 5.5V	-	-	±5	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±5	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 7)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = V_{CC} - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}_X$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $\overline{OE}_X$ = GND One Bit Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	0.6	2.3	mA
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $\overline{OE}_X$ = GND 10 Bits Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	2.1	4.7 (Note 11)	mA

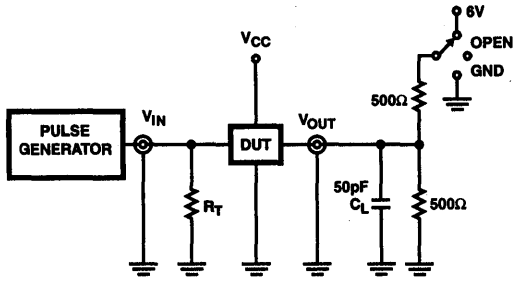
Switching Specifications Over Operating Range (NOTE 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT16827A		CD74LPT16827B		CD74LPT16827C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay D_{XX} to Y_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.0	1.5	4.4	ns
Output Enable Time $\overline{OE}_X$ to Y_X	t_{PZH}, t_{PZL}		1.5	9.5	1.5	8.0	1.5	7.0	ns
Output Disable Time (Note 16) $\overline{OE}_X$ to Y_X	t_{PHZ}, t_{PLZ}		1.5	8.5	1.5	6.0	1.5	5.7	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC}$ - 0.6V at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

17. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

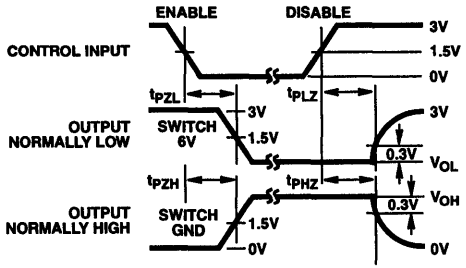


FIGURE 2. ENABLE AND DISABLE TIMING

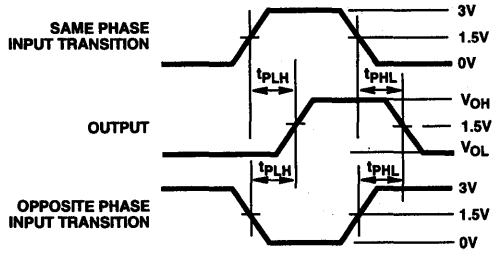


FIGURE 3. PROPAGATION DELAY

CMOS LOGIC 4

OCTAL 5V FCT CMOS LOGIC AND 5V FCT WITH 25Ω SERIES RESISTOR

		PAGE
Selection Guide		4-3
Data Sheets		
CD29FCT52T	Fast CMOS Registered Transceiver	4-7
CD29FCT520T	Fast CMOS Multilevel Pipeline Register	4-13
CD74FCT138T, CD74FCT238T	Fast CMOS 1-of-8 Decoders	4-18
CD74FCT139T, CD74FCT239T	Fast CMOS Dual 1-of-4 Decoders	4-24
CD74FCT151T, CD74FCT251T, CD74FCT2151T	Fast CMOS 8-Input Multiplexers	4-29
CD74FCT153T, CD74FCT253T, CD74FCT2153T, CD74FCT2253T	High-Speed CMOS Dual 4-Input Multiplexers	4-34
CD74FCT157T, CD74FCT257T, CD74FCT2157T, CD74FCT2257T	Fast CMOS Quad 2-Input Multiplexers	4-39
CD74FCT240T, CD74FCT241T, CD74FCT244T, CD74FCT540T, CD74FCT541T, CD74FCT2240T, CD74FCT2241T, CD74FCT2244T, CD74FCT2541T	Fast CMOS Octal Buffer and Line Drivers	4-44
CD74FCT245T, CD74FCT640T, CD74FCT2245T	Fast CMOS Octal Bidirectional Transceivers	4-51
CD74FCT273T, CD74FCT2273T	Fast CMOS Octal D Flip-Flops with Master Reset	4-57
CD74FCT373T, CD74FCT533T, CD74FCT573T, CD74FCT2373T, CD74FCT2573T	Fast CMOS Octal Transparent Latches	4-62

Octal 5V FCT CMOS Logic and 25Ω Series Resistor (Continued)

		PAGE
CD74FCT374T, CD74FCT534T, CD74FCT574T, CD74FCT2374T, CD74FCT2574T	Fast CMOS Octal D Registers (Three-State)	4-69
CD74FCT377T	Fast CMOS Octal D Flip-Flop with Clock Enable	4-75
CD74FCT399T	Fast CMOS Quad Dual-Port Register	4-80
CD74FCT521T	Fast CMOS 8-Bit Identity Comparator	4-85
CD74FCT543T, CD74FCT544T, CD74FCT2543T	Fast CMOS Latched Transceivers	4-90
CD74FCT623T	Fast CMOS Octal Bus Transceiver (Three-State)	4-96
CD74FCT646T, CD74FCT648T, CD74FCT651T, CD74FCT652T, CD74FCT2646T, CD74FCT2652T	Fast CMOS Octal Registered Transceivers	4-101
CD74FCT821T, CD74FCT823T, CD74FCT825T, CD74FCT2821T, CD74FCT2823T	Fast CMOS Bus Interface Registers	4-110
CD74FCT827T, CD74FCT828T, CD74FCT2827T, CD74FCT2828T	Fast CMOS 10-Bit Buffers	4-117
CD74FCT841T, CD74FCT843T, CD74FCT845T, CD74FCT2841T	Fast CMOS Bus Interface Latches	4-123
CD74FCT861T, CD74FCT863T, CD74FCT864T	Fast CMOS Bus Transceivers	4-129

Selection Guide

OCTAL 5V FCT CMOS LOGIC AND 5V FCT WITH 25Ω SERIES RESISTOR

PART NUMBER	DESCRIPTION	SPEED GRADE (X)						FILE #
		BLANK	A	B	C	D	E	
CD29FCT520T	Fast CMOS Multilevel Pipeline Register	-	X	X	-	-	-	4164
CD29FCT52T	Fast CMOS Registered Transceivers	-	X	X	-	-	-	4163
CD74FCT138T	Fast CMOS 1-of-8 Decoder	X	X	-	X	-	-	4158
CD74FCT139T	Fast CMOS Dual 1-of-4 Decoder	X	X	-	X	-	-	4159
CD74FCT151T	8-Input Multiplexer	X	X	-	X	-	-	4160
CD74FCT153T	High-Speed CMOS Dual 4-Input Multiplexer	X	X	-	X	-	-	4161
CD74FCT157T	Fast CMOS Quad 2-Input Multiplexer	X	X	-	X	X	-	4166
CD74FCT2151T	Fast CMOS 8-Input Multiplexer	X	X	-	X	-	-	4160
CD74FCT2153T	High-Speed CMOS Dual 4-Input Multiplexer	X	X	-	X	-	-	4161
CD74FCT2157T	Fast CMOS Quad 2-Input Multiplexer	X	X	-	X	-	-	4166
CD74FCT2240T	Fast CMOS Octal Buffer and Line Drivers	X	X	-	X	-	-	4167
CD74FCT2241T	Octal Buffer and Line Drivers	X	X	-	X	-	-	4167
CD74FCT2244T	Fast CMOS Octal Buffer and Line Drivers	X	X	-	X	-	-	4167
CD74FCT2245T	Fast CMOS Octal Bidirectional Transceivers	X	X	-	X	X	-	4168
CD74FCT2253T	High-Speed CMOS Dual 4-Input Multiplexer	X	X	-	X	-	-	4161
CD74FCT2257T	Fast CMOS Quad 2-Input Multiplexer	X	X	-	X	-	-	4166
CD74FCT2273T	Fast CMOS Octal D Flip-Flop with Master Reset	X	X	-	X	-	-	4169
CD74FCT2373T	Fast CMOS Octal Transparent Latches	X	X	-	X	-	-	4170
CD74FCT2374T	Fast CMOS Octal D Registers (Three-State)	X	X	-	X	X	-	4171
CD74FCT238T	Fast CMOS 1-of-8 Decoder	X	X	-	X	-	-	4158
CD74FCT239T	Fast CMOS Dual 1-of-4 Decoder	X	X	-	X	-	-	4159
CD74FCT240T	Fast CMOS Octal Buffer and Line Drivers	X	X	-	X	X	-	4167
CD74FCT241T	Fast CMOS Octal Buffer and Line Drivers	X	X	-	X	X	-	4167
CD74FCT244T	Fast CMOS Octal Buffer and Line Drivers	X	X	-	X	X	-	4167
CD74FCT245T	Fast CMOS Octal Bidirectional Transceivers	X	X	-	X	X	-	4168
CD74FCT251T	Fast CMOS 8-Input Multiplexer	X	X	-	X	-	-	4160

OCTAL 5V FCT CMOS LOGIC AND 5V FCT WITH 25Ω SERIES RESISTOR (Continued)

PART NUMBER	DESCRIPTION	SPEED GRADE (X)						FILE #
		BLANK	A	B	C	D	E	
CD74FCT253T	High-Speed CMOS Dual 4-Input Multiplexer	X	X	-	X	-	-	4161
CD74FCT2541T	Fast CMOS Octal Buffer and Line Drivers	X	X	-	X	-	-	4167
CD74FCT2543T	Fast CMOS Latched Transceivers	X	X	-	X	X	-	4173
CD74FCT2573T	Fast CMOS Octal Transparent Latches	X	X	-	X	-	-	4170
CD74FCT2574T	Fast CMOS Octal D Registers (Three-State)	X	X	-	X	X	-	4171
CD74FCT257T	Fast CMOS Quad 2-Input Multiplexer	X	X	-	X	-	-	4166
CD74FCT2646T	Fast CMOS Octal Registered Transceivers	X	X	-	-	-	-	4175
CD74FCT2652T	Fast CMOS Octal Registered Transceivers	X	X	-	-	-	-	4175
CD74FCT273T	Fast CMOS Octal D Flip-Flop with Master Reset	X	X	-	X	X	-	4169
CD74FCT2821T	Fast CMOS Bus Interface Registers	-	X	X	-	-	-	4176
CD74FCT2823T	Fast CMOS Bus Interface Registers	-	X	X	X	-	-	4176
CD74FCT2827T	Fast CMOS 10-Bit Buffers	-	X	X	-	-	-	4179
CD74FCT2828T	Fast CMOS 10-Bit Buffers	-	X	X	X	-	-	4179
CD74FCT2841T	Fast CMOS Bus Interface Latches	-	X	X	X	-	-	4177
CD74FCT373T	Fast CMOS Octal Transparent Latches	X	X	-	X	X	-	4170
CD74FCT374T	Fast CMOS Octal D Registers (Three-State)	X	X	-	X	X	-	4171
CD74FCT377T	Fast CMOS Octal D Flip-Flop with Clock Enable	X	X	-	X	X	-	4172
CD74FCT399T	Fast CMOS Quad Dual-Port Register	X	X	-	X	-	-	4252
CD74FCT521T	Fast CMOS 8-Bit Identity Comparator	X	X	X	X	X	-	4214
CD74FCT533T	Fast CMOS Octal Transparent Latches	X	X	-	X	-	-	4170
CD74FCT534T	Fast CMOS Octal D Registers (Three-State)	X	X	-	X	X	-	4171
CD74FCT540T	Fast CMOS Octal Buffer and Line Drivers	X	X	-	X	X	-	4167
CD74FCT541T	Fast CMOS Octal Buffer and Line Drivers	X	X	-	X	X	-	4167
CD74FCT543T	Fast CMOS Latched Transceivers	X	X	-	X	X	-	4173
CD74FCT544T	Fast CMOS Latched Transceivers	X	X	-	X	X	-	4173

OCTAL 5V FCT CMOS LOGIC AND 5V FCT WITH 25Ω SERIES RESISTOR (Continued)

PART NUMBER	DESCRIPTION	SPEED GRADE (X)						FILE #
		BLANK	A	B	C	D	E	
CD74FCT573T	Fast CMOS Octal Transparent Latches	X	X	-	X		-	4170
CD74FCT574T	Fast CMOS Octal D Registers (Three-State)	X	X	-	X	X	-	4171
CD74FCT623T	Fast CMOS Octal Bus Transceiver (Three-State)	X	X	-	X	X	-	4174
CD74FCT640T	Fast CMOS Octal Bidirectional Transceivers	X	X	-	X	X	-	4168
CD74FCT646T	Fast CMOS Octal Registered Transceivers	X	X	-	X	X	-	4175
CD74FCT648T	Fast CMOS Octal Registered Transceivers	X	X	-	X	-	-	4175
CD74FCT651T, CD74FCT2652T	Fast CMOS Octal Registered Transceivers	X	X	-	X	-	-	4175
CD74FCT652T	Fast CMOS Octal Registered Transceivers	X	X	-	X	-	-	4175
CD74FCT821T	Fast CMOS Bus Interface Registers	-	X	X	X	-	-	4176
CD74FCT823T	Fast CMOS Bus Interface Registers	-	X	X	X	-	-	4176
CD74FCT825T	Fast CMOS Bus Interface Registers	-	X	X	X	-	-	4176
CD74FCT827T	Fast CMOS 10-Bit Buffers	-	X	X	X	-	-	4179
CD74FCT828T	Fast CMOS 10-Bit Buffers	-	X	X	X	-	-	4179
CD74FCT841T	Fast CMOS Bus Interface Latches	-	X	X	X	-	-	4177
CD74FCT843T	Fast CMOS Bus Interface Latches	-	X	X	X	-	-	4177
CD74FCT845T	Fast CMOS Bus Interface Latches	-	X	X	X	-	-	4177
CD74FCT861T	Fast CMOS Bus Transceivers	-	X	X	X	-	-	4178
CD74FCT863T	Fast CMOS Bus Transceivers	-	X	X	X	-	-	4178
CD74FCT864T	Fast CMOS Bus Transceivers	-	X	X	X	-	-	4178

CD29FCT52T

December 1996

Fast CMOS Registered Transceiver

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible With Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **TTL Input and Output Levels**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Description

The CD29FCT52T is an 8-bit registered transceiver designed with two 8-bit back-to-back registers to store data flowing in both directions between two bidirectional buses. Separate clock enable and three-state output enable signals are provided for each register.

Ordering Information

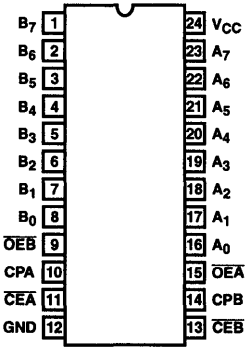
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD29FCT52ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD29FCT52ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD29FCT52BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD29FCT52BTQM	-40 to 85	24 Ld QSOP	M24.15-P

NOTE: QSOP is commonly known as SSOP.

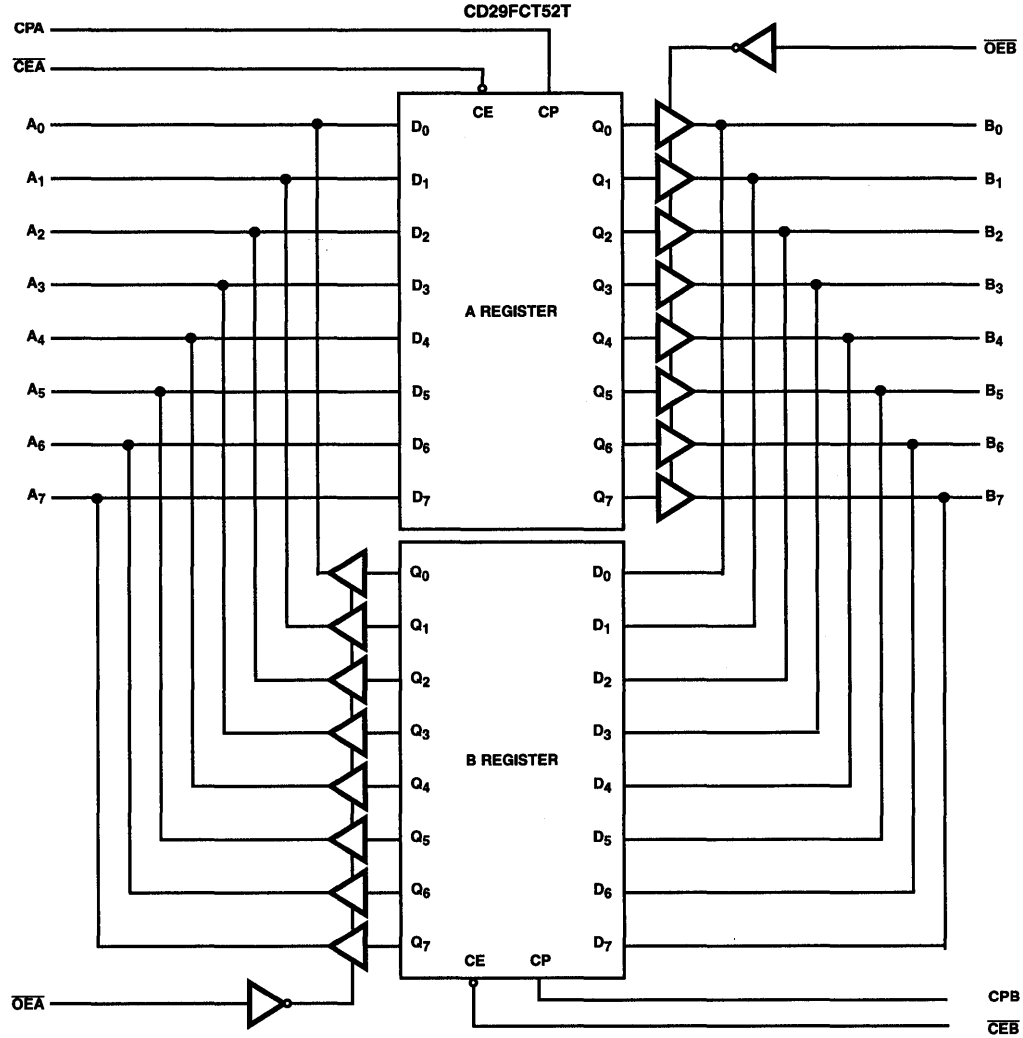
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD29FCT52T
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS			INTERNAL
	D_N	CP	$\overline{CE}$	Q_N
Hold Data	X	X	H	NC
Load Data	L	↑	L	L
	H	↑	L	H

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change
   ↑ = LOW-to-HIGH Transition

OUTPUT CONTROL TABLE

FUNCTION	$\overline{OE}$	INTERNAL	Y-OUTPUTS
		Q_N	CD29FCT52T
Disable Outputs	H	X	Z
Enable Outputs	L	L	L
	L	H	H

Pin Descriptions

PIN NAME	DESCRIPTION
A_0-A_7	A Register Inputs or B Register Outputs
B_0-B_7	B Register Inputs or A Register Outputs
CPA	Clock for A Register
CPB	Clock for B Register
$\overline{OEA}$	Output Enable for B Register
$\overline{OEB}$	Output Enable for A Register
$\overline{CEA}$	Clock Enable for A Register
$\overline{CEB}$	Clock Enable for B Register
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
SOIC Package 75
QSOP Package 100
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}		V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µ A
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OEA}$ or $\overline{OEB}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OEA}$ or $\overline{OEB}$ = GND f_i = 5MHz One Bit toggling	V_{IN} = V_{CC} V_{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2	5.5 (Note 9)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OEA}$ or $\overline{OEB}$ = GND Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.8	7.3 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6	16.3 (Note 9)	mA

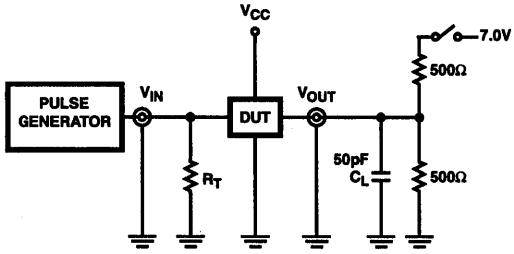
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT (NOTE 12) MIN	AT MAX	BT (NOTE 12) MIN	BT MAX	UNITS
Propagation Delay CPA, CPB, to A_N, B_N	t_{PLH}, t_{PHL}	C_L = 50 pF, R_L = 500Ω	2.0	10.0	2.0	7.5	ns
Output Enable Time $\overline{OEA}$, $\overline{OEB}$, to A_N, B_N	t_{PZH}, t_{PZL}		1.5	10.5	1.5	8.0	ns
Output Disable Time $\overline{OEA}$, $\overline{OEB}$, to A_N, B_N (Note 13)	t_{PHZ}, t_{PLZ}		1.5	10.0	1.5	7.5	ns
Set-up Time HIGH or LOW, A_N, B_N to CPA, CPB	t_{SU}		2.5	-	2.5	-	ns
Hold Time HIGH or LOW, A_N, B_N to CPA, CPB	t_H		2.0	-	1.5	-	ns
Set-up Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	t_{SU}		3.0	-	3.0	-	ns
Hold Time HIGH or LOW, $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB	t_H		2.0	-	2.0	-	ns
Pulse Width HIGH or LOW, CPA or CPB (Note 13)	t_W		3.0	-	3.0	-	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

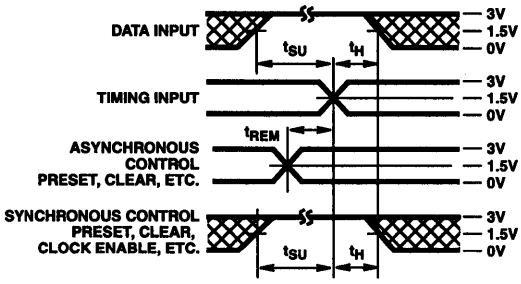


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

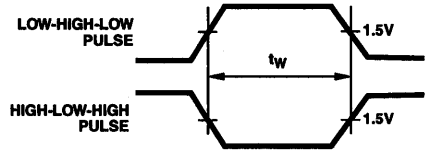


FIGURE 3. PULSE WIDTH

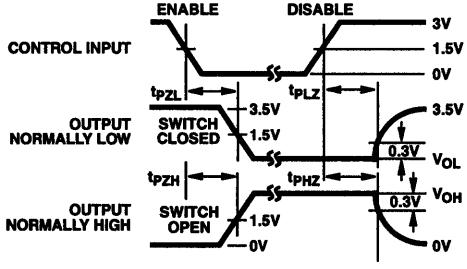


FIGURE 4. ENABLE AND DISABLE TIMING

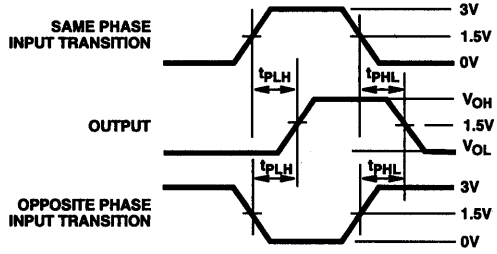


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD29FCT520T

December 1996

Fast CMOS Multilevel Pipeline Register

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pinout and Function Compatible with IDT29FCT520, QS29FCT520 and AMD's Am29520**
- **Four 8-bit High-Speed Registers**
- **Hold, Transfer, and Load Instructions**
- **Dual Two-Level or Single Four-Level Pipeline Operation**
- **TTL Input and Output Levels, Reducing Problematic Ground Bounce**
- **High Output Drive ..... I_{OL} = 48mA**
- **Extremely Low Static Power ..... 1mW (Typ)**

Description

These devices are multilevel pipeline registers containing four 8-bit positive triggered registers which can be configured as a dual 2-level or a single 4-level pipeline. These products are designed for use as temporary storage or for storage delays in pipelined systems. When data is entered into the first level (I = 2 or I = 1) of the CD29FCT520T, the existing data in the first level is moved to the second level. The I = 3 shift instruction puts the registers on hold.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD29FCT520ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD29FCT520ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD29FCT520BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD29FCT520BTQM	-40 to 85	24 Ld QSOP	M24.15-P

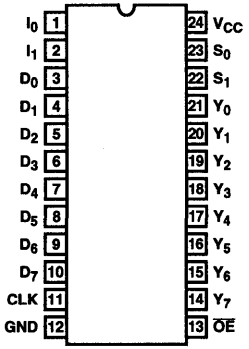
NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD29FCT520T
(QSOP, SOIC)

TOP VIEW

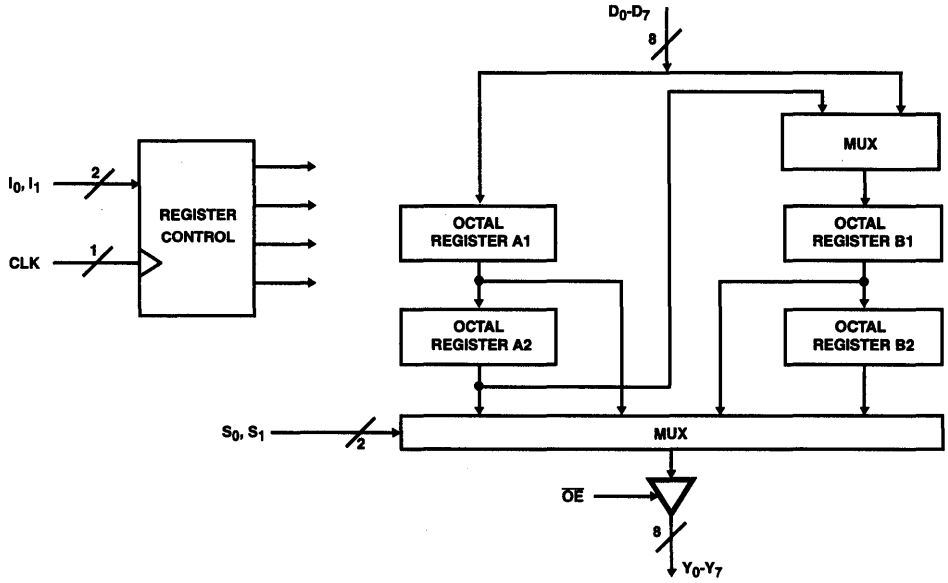


4

OCTAL 5V FCT
5V FCT 25Ω

File Number **4164.1**

Functional Block Diagram



Register Selection

S1	S0	REGISTER
0	0	B_2
0	1	B_1
1	0	A_2
1	1	A_1

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW) for Three-State Output Port
CLK	Clock Input. Enter Data into Registers on LOW-to-HIGH Transistions
I_0, I_1	Instruction Inputs
S_0, S_1	Multiplexer Select. Inputs Either Register A_1, A_2, B_1, or B_2 Data to be Avaialbe at the Output Ports
D_X	Register Inputs
Y_X	Register Outputs
GND	Ground
V_{CC}	Power

CD29FCT520T Data Loading (Note 1)

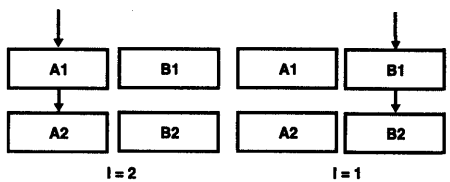


FIGURE 1. DUAL 2-LEVEL

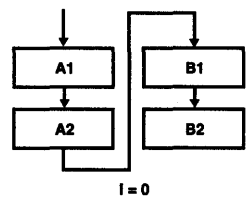


FIGURE 2. SINGLE 4-LEVEL

NOTE: I = 3 for hold.

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	75
QSOP Package	100

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	VCC = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}		V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open fcp = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND One Bit Toggling f_i = 5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.5 (Note 9)	mA
		V_{CC} = Max, Outputs Open fcp = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND Eight Bits Toggling f_i = 5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.8	7.3 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.0	16.3 (Note 9)	mA

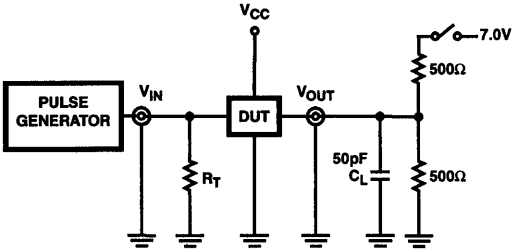
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT (NOTE 12) MIN	AT MAX	BT (NOTE 12) MIN	BT MAX	UNITS
Propagation Delay CLK to Y_X	t_{PLH}, t_{PHL}	C_L = 50 pF, R_L = 500Ω	2.0	14.0	2.0	7.5	ns
Propagation Delay S_0 or S_1 to Y_X	t_{PLH}, t_{PHL}		2.0	13.0	2.0	7.5	ns
Setup Time HIGH or LOW D_X to CLK	t_{SU}		5.0	-	2.5	-	ns
Hold Time HIGH or LOW D_X to CLK	t_H		2.0	-	2.0	-	ns
Setup Time HIGH or LOW I_0 or I_1 to CLK	t_{SU}		5.0	-	4.0	-	ns
Hold Time HIGH or LOW I_0 or I_1 to CLK	t_H		2.0	-	2.0	-	ns
Output Enable Time $\overline{OE}$ to Y_X	t_{PZH}, t_{PZL}		1.5	12.0	1.5	7.0	ns
Output Disable Time $\overline{OE}$ to Y_X (Note 13)	t_{PHZ}, t_{PLZ}		1.5	15.0	1.5	7.5	ns
Clock Pulse Width HIGH or LOW (Note 13)	t_W		7.0	-	5.5	-	ns

NOTES:

2. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
3. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. This parameter is determined by device characterization but is not production tested.
6. Per TTL driven input (V_{IN} = 3.4V, control inputs only); all other inputs at V_{CC} or GND.
7. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
8. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
9. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.
10. See test circuit and wave forms.
11. Minimum limits are guaranteed but not tested on Propagation Delays.
12. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:
C_L = Load capacitance, includes jig and probe capacitance.
R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

13. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 3. TEST CIRCUIT

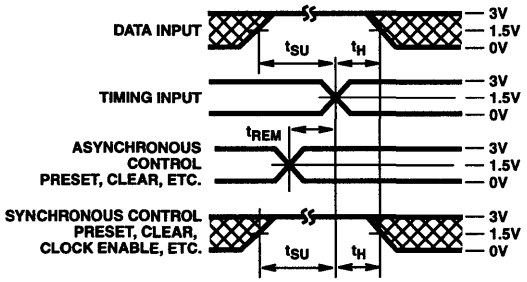


FIGURE 4. SETUP, HOLD, AND RELEASE TIMING

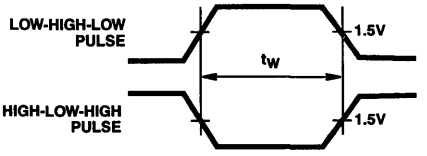


FIGURE 5. PULSE WIDTH

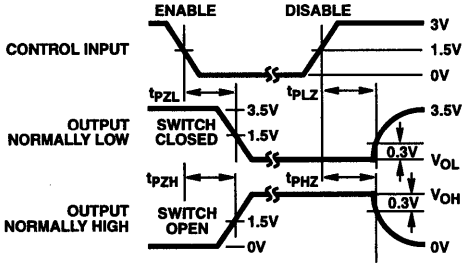


FIGURE 6. ENABLE AND DISABLE TIMING

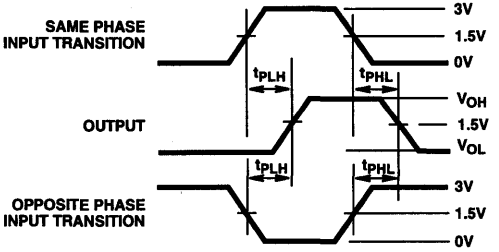


FIGURE 7. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT138T, CD74FCT238T

December 1996

Fast CMOS 1-of-8 Decoders

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **TTL Input and Output Levels**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT138TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT138ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT138CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT138TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT138ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT138CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT138TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT138ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT138CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT238TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT238ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT238CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT238TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT238ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT238CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT238TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT238ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT238CTQM	-40 to 85	16 Ld QSOP	M16.15A-P

NOTE: QSOP is commonly known as SSOP.

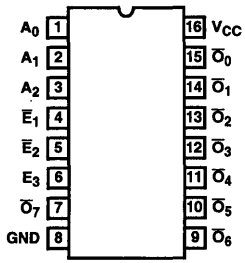
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

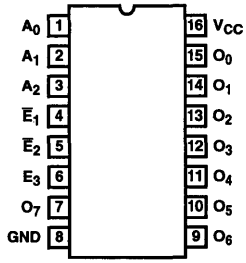
These high-speed decoders accept three binary weighted inputs (A_0, A_1, A_2) and gives eight mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_7$: CD74FCT138T) or active HIGH outputs (O_0-O_7: CD74FCT238T) when enabled. These devices contain three enable inputs, two active LOW ($\overline{E}_1$, $\overline{E}_2$) and one active HIGH (E_3). On the CD74FCT138T all outputs will be HIGH and on the CD74FCT238T all outputs will be LOW, except when $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH.

Pinouts

CD74FCT138T, (QSOP, SOIC)
TOP VIEW



CD74FCT238T (QSOP, SOIC)
TOP VIEW



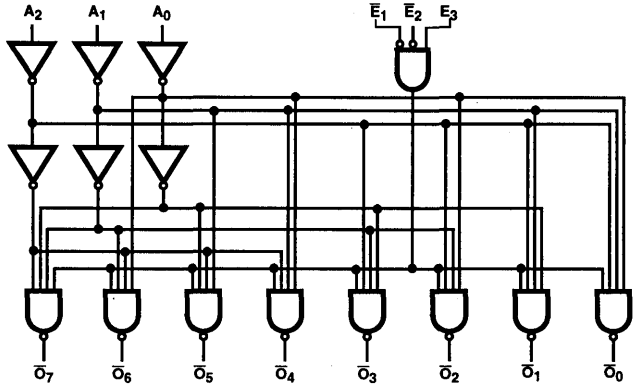
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **4158.2**

Functional Block Diagram

CD74FCT138T



CD74FCT138T TRUTH TABLE (NOTE 1)

INPUTS						OUTPUTS								
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$	FUNCTION
H	X	X	X	X	X	H	H	H	H	H	H	H	H	Disable
X	H	X	X	X	X	H	H	H	H	H	H	H	H	Disable
X	X	L	X	X	X	H	H	H	H	H	H	H	H	Disable
L	L	H	L	L	L	L	H	H	H	H	H	H	H	A2-0 = 0
L	L	H	H	L	L	H	L	H	H	H	H	H	H	A2-0 = 1
L	L	H	L	H	L	H	H	L	H	H	H	H	H	A2-0 = 2
L	L	H	H	H	L	H	H	H	L	H	H	H	H	A2-0 = 3
L	L	H	L	L	H	H	H	H	H	L	H	H	H	A2-0 = 4
L	L	H	H	L	H	H	H	H	H	H	L	H	H	A2-0 = 5
L	L	H	L	H	H	H	H	H	H	H	H	L	H	A2-0 = 6
L	L	H	H	H	H	H	H	H	H	H	H	H	L	A2-0 = 7

CD74FCT238T TRUTH TABLE (NOTE 1)

INPUTS						OUTPUTS								
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7	FUNCTION
H	X	X	X	X	X	L	L	L	L	L	L	L	L	Disable
X	H	X	X	X	X	L	L	L	L	L	L	L	L	Disable
X	X	L	X	X	X	L	L	L	L	L	L	L	L	Disable
L	L	H	L	L	L	H	L	L	L	L	L	L	L	A2-0 = 0
L	L	H	H	L	L	L	H	L	L	L	L	L	L	A2-0 = 1
L	L	H	L	H	L	L	L	H	L	L	L	L	L	A2-0 = 2
L	L	H	H	H	L	L	L	L	H	L	L	L	L	A2-0 = 3
L	L	H	L	L	H	L	L	L	L	H	L	L	L	A2-0 = 4
L	L	H	H	L	H	L	L	L	L	L	H	L	L	A2-0 = 5
L	L	H	L	H	H	L	L	L	L	L	L	H	L	A2-0 = 6
L	L	H	H	H	H	L	L	L	L	L	L	L	H	A2-0 = 7

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

Pin Descriptions

PIN NAME	DESCRIPTION
CD74FCT138T PRODUCT PIN DESCRIPTION	
A_0-A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
$\overline{O}_0$-$\overline{O}_7$	Outputs (Active LOW)
CD74FCT238T PRODUCT PIN DESCRIPTION	
A_0-A_2	Address Inputs
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
O_0-O_7	Outputs (Active HIGH)

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . $-40^{o}C$ to $85^{o}C$
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)
16 Lead SOIC (150 mil) Package	110
16 Lead SOIC (300 mil) Package	97
16 Lead QSOP Package	140

Maximum Junction Temperature . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^{o}C$ to $85^{o}C$, $V_{CC} = 5.0V \pm 5\%$							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µ A
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	–120	-225	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE $T_A = 25^{o}C$, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	0.15	0.3	mA/ MHz
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open fcp = 10MHz, 50% Duty Cycle Toggle $\overline{E1}$, $\overline{E2}$, or E3 One Bit toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	4.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.8	5.0 (Note 9)	mA

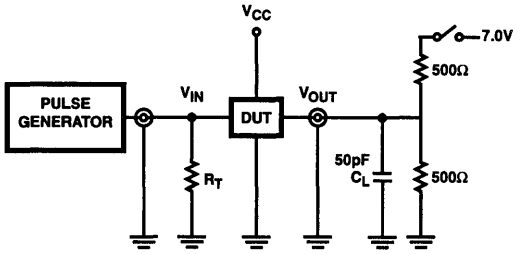
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T (NOTE 12) MIN	T MAX	AT (NOTE 12) MIN	AT MAX	CT (NOTE 12) MIN	CT MAX	UNIT
CD74FCT138T									
Propagation Delay An to $\overline{On}$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	5.8	1.5	5.1	ns
Propagation Delay $\overline{E1}$ or $\overline{E2}$ to $\overline{On}$	t_{PLH}, t_{PHL}		1.5	9.0	1.5	5.9	1.5	5.2	ns
Propagation Delay E3 to $\overline{On}$	t_{PLH}, t_{PHL}		1.5	9.0	1.5	5.9	1.5	5.2	ns
CD74FCT238T									
Propagation Delay An to On	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	5.8	1.5	5.0	ns
Propagation Delay $\overline{E1}$ or $\overline{E2}$ to On	t_{PLH}, t_{PHL}		1.5	8.0	1.5	5.9	1.5	5.0	ns
Propagation Delay E3 to On	t_{PLH}, t_{PHL}		1.5	8.0	1.5	5.9	1.5	5.0	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_O = Output Frequency
    N_O = Number of Outputs at f_O
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

13. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

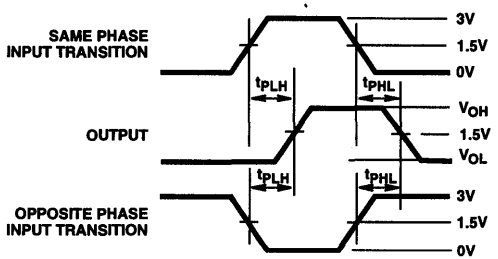


FIGURE 2. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT139T, CD74FCT239T

December 1996

Fast CMOS Dual 1-of-4 Decoders

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **TTL Input and Output Levels**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Description

These are high-speed, two independent, 1-of-4 decoders. Each decoder accepts two binary weighted inputs (A_0, A_1) and gives four mutually exclusive active LOW outputs ($\overline{O}_0$-$\overline{O}_3$: CD74FCT139T) or active HIGH outputs (O_0-O_3: CD74FCT239T). There is one active LOW enable ($\overline{E}$) for each decoder. For the CD74FCT139T all outputs are forced HIGH, and for the CD74FCT239T all outputs are forced LOW when $\overline{E}$ is HIGH.

Ordering Information

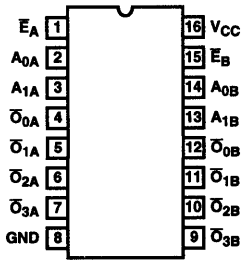
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT139TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT139ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT139CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT139TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT139ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT139CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT139TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT139ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT139CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT239TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT239ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT239CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT239TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT239ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT239CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT239TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT239ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT239CTQM	-40 to 85	16 Ld QSOP	M16.15A-P

NOTE: QSOP is commonly known as SSOP.

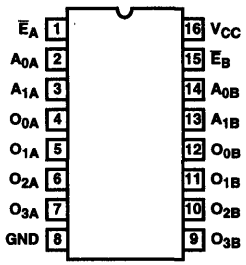
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinouts

CD74FCT139T
(QSOP, SOIC)
TOP VIEW



CD74FCT239T
(QSOP, SOIC)
TOP VIEW



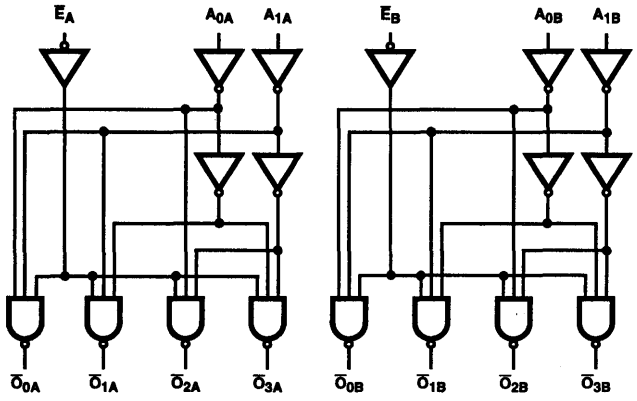
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **4159.2**

Functional Block Diagram

CD74FCT139T



CD74FCT139T TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

CD74FCT239T TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS			
$\overline{E}$	A_0	A_1	O_0	O_1	O_2	O_3
H	X	X	L	L	L	L
L	L	L	H	L	L	L
L	H	L	L	H	L	L
L	L	H	L	L	H	L
L	H	H	L	L	L	H

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care

Pin Descriptions

PIN NAME	DESCRIPTION
CD74FCT139T	
A_0, A_1	Address Inputs
$\overline{E}$	Enable Inputs (Active LOW)
$\overline{O}_0$-$\overline{O}_3$	Outputs (Active LOW)
CD74FCT239T	
A_0, A_1	Address Inputs
$\overline{E}$	Enable Inputs (Active LOW)
O_0-O_3	Outputs (Active HIGH)

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
16 Lead 150 mil SOIC Package	110
16 Lead 300 mil SOIC Package	97
16 Lead QSOP Package	140

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ± 5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-225	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.3	mA/ MHz
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open fcp = 10MHz, 50% Duty Cycle One Bit toggling	V_{IN} = V_{CC} Vin = GND	-	1.5	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.8	5.0	mA
		V_{CC} = Max, Outputs Open fcp = 10MHz, 50% Duty Cycle One Bit Toggling on Each Decoder	V_{IN} = V_{CC} V_{IN} = GND	-	3.0	7.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	3.7	9.5 (Note 9)	mA

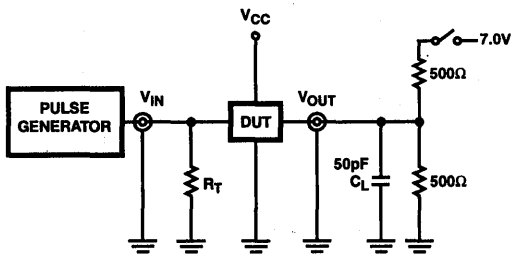
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T (NOTE 12) MIN	T MAX	AT (NOTE 12) MIN	AT MAX	CT (NOTE 12) MIN	CT MAX	UNIT
CD74FCT139T									
Propagation Delay A0 or A1 to $\overline{On}$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	5.9	1.5	5.0	ns
Propagation Delay $\overline{E}$ to $\overline{On}$	t_{PLH}, t_{PHL}		1.5	8.0	1.5	5.5	1.5	4.8	ns
CD74FCT239T									
Propagation Delay A0 or A1 to On	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	5.9	1.5	5.0	ns
Propagation Delay $\overline{E}$ to On	t_{PLH}, t_{PHL}		1.5	8.0	1.5	5.5	1.5	4.8	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_O N_O)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (Vin = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_O = Output Frequency
    N_O = Number of Outputs at f_O
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

13. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

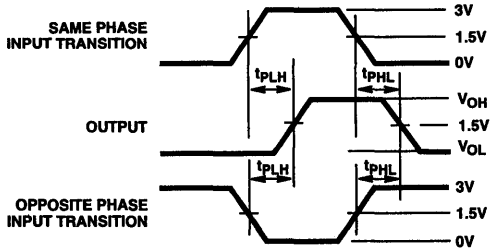


FIGURE 2. PROPAGATION DELAY

CD74FCT151T, CD74FCT251T, CD74FCT2151T

December 1996

Fast CMOS 8-Input Multiplexers

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **25Ω Series Resistor On All Outputs (FCT2151T Only)**
- **TTL Input and Output Levels**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT151TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT151ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT151CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT151TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT151ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT151CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT151TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT151ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT151CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT251TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT251ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT251CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT251TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT251ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT251CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT251TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT251ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT251CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2151TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2151ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2151CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2151TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2151ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2151CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2151TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2151ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2151CTQM	-40 to 85	16 Ld QSOP	M16.15A-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

The CD74FCT151T, CD74FCT251T, and CD74FCT2151T are high-speed 8-input multiplexers. They select one bit from a source of eight under the control of three select inputs. Both assertion and negation outputs are provided.

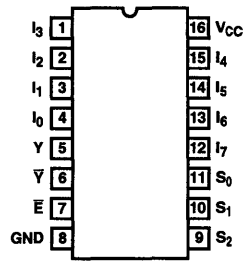
The CD74FCT151T, CD74FCT2151T have a common, active-LOW, Enable input ($\overline{E}$). When $\overline{E}$ is LOW, data from one of eight inputs is directed to the complementary outputs based on the 3-bit code applied to the Select (S_0-S_2) inputs. The CD74FCT151T, CD74FCT2151T can be used as a data routing device from one of eight sources.

The CD74FCT251T has a common Active-LOW Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, data from one of eight inputs is directed to the complementary outputs. When $\overline{OE}$ is HIGH, both outputs are switched to a high-impedance state allowing multiplexer expansion by tying several outputs together.

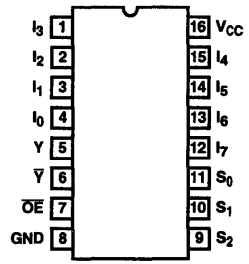
The CD74FCT2151T device has a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Pinouts

CD74FCT151, CD74FCT2151T
(QSOP, SOIC)
TOP VIEW



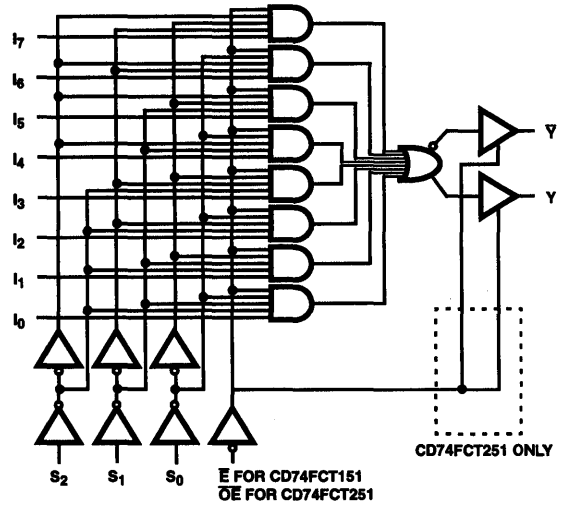
CD74FCT251
(QSOP, SOIC)
TOP VIEW



4

OCTAL 5V FCT
5V FCT 25Ω

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS				OUTPUTS	
S_2	S_1	S_0	(NOTE 2) $\overline{E}/\overline{OE}$	Y	$\overline{Y}$
X	X	X	H	L (Note 3)	H (Note 3)
X	X	X	H	Z (Note 4)	Z (Note 4)
L	L	L	L	I0	$\overline{I0}$
L	L	H	L	I1	$\overline{I1}$
L	H	L	L	I2	$\overline{I2}$
L	H	H	L	I3	$\overline{I3}$
H	L	L	L	I4	$\overline{I4}$
H	L	H	L	I5	$\overline{I5}$
H	H	L	L	I6	$\overline{I6}$
H	H	H	L	I7	$\overline{I7}$

NOTES:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care
   Z = High Impedance.
2. $\overline{E}$ for 151/2151, $\overline{OE}$ for 251.
3. 151/2151 ONLY.
4. 251 ONLY.

Pin Descriptions

PIN NAME	DESCRIPTION
I_0-I_7	Data Inputs
S_0-S_2	Select Inputs
$\overline{E}$	Enable Input (Active LOW) FCT151/2151T
$\overline{OE}$	Output Enable (Active LOW) FCT251T
Y	Data Output
$\overline{Y}$	Inverted Data Output
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)
16 Lead SOIC (150 mil) Package	110
16 Lead SOIC (300 mil)Package	97
16 Lead QSOP Package	140

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS		MIN	(NOTE 7) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}, I_{OZL}	V_{CC} = Max	V_{OUT} = 2.7V			1	µA
			V_{OUT} = 0.5V			-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 8), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	3.2	6.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	3.5	7.5 (Note 12)	

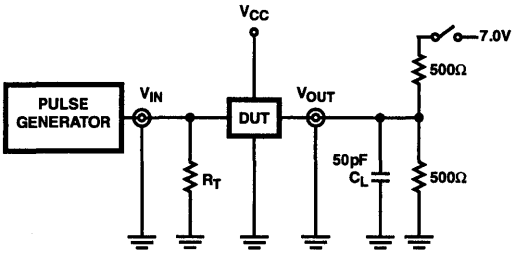
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T (NOTE 15) MIN	T MAX	AT (NOTE 15) MIN	AT MAX	CT (NOTE 15) MIN	CT MAX	UNIT
CD74FCT151T, CD74FCT2151T									
Propagation Delay $\overline{S}n$ to $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
Propagation Delay Sn to Y	t_{PLH}, t_{PHL}		1.5	10.5	1.5	6.8	1.5	5.8	ns
Propagation Delay $\overline{E}$ to $\overline{Y}$	t_{PLH}, t_{PHL}		1.5	7.0	1.5	5.6	1.5	4.8	ns
Propagation Delay $\overline{E}$ to Y	t_{PLH}, t_{PHL}		1.5	9.5	1.5	5.8	1.5	5.0	ns
Propagation Delay In to $\overline{Y}$	t_{PLH}, t_{PHL}		1.5	6.5	1.5	5.2	1.5	4.4	ns
Propagation Delay In to Y	t_{PLH}, t_{PHL}		1.5	7.5	1.5	5.5	1.5	4.7	ns
CD74FCT251T									
Propagation Delay $\overline{S}n$ to $\overline{Y}$	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
Propagation Delay Sn to Y	t_{PLH}, t_{PHL}		1.5	11.0	1.5	6.8	1.5	5.8	ns
Propagation Delay In to $\overline{Y}$	t_{PLH}, t_{PHL}		1.5	7.0	1.5	5.2	1.5	4.4	ns
Propagation Delay In to Y	t_{PLH}, t_{PHL}		1.5	7.0	1.5	5.5	1.5	4.7	ns
Output Enable Time $\overline{OE}$ to $\overline{Y}$	t_{PZH}, t_{PZL}		1.5	9.0	1.5	6.7	1.5	5.7	ns
Output Disable Time (Note 16) $\overline{OE}$ to $\overline{Y}$	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	6.0	1.5	5.0	ns
Output Enable Time $\overline{OE}$ to Y	t_{PZH}, t_{PZL}		1.5	9.0	1.5	6.7	1.5	5.7	ns
Output Disable Time(Note 16) $\overline{OE}$ to Y	t_{PHZ}, t_{PLZ}		1.5	7.0	1.5	6.0	1.5	5.0	ns

NOTES:

6. For conditions show as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
7. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
8. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (Vin = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

17. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

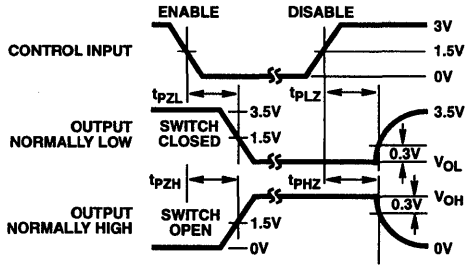


FIGURE 2. ENABLE AND DISABLE TIMING

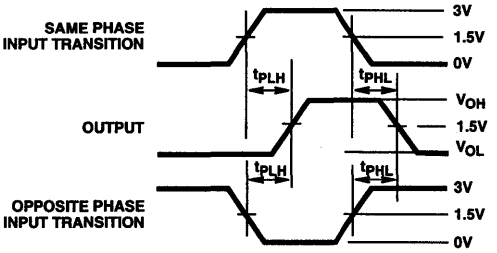


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT153T, CD74FCT253T, CD74FCT2153T, CD74FCT2253T

December 1996

High-Speed CMOS Dual 4-Input Multiplexers

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor On All Outputs (FCT2XXX Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs (25Ω Series Only)
- Extremely Low Static Power
- Hysteresis on All Inputs

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT153TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT153ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT153CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT153TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT153ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT153CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT153TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT153ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT153CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT253TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT253ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT253CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT253TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT253ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT253CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT253TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT253ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT253CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2153TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2153ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2153CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2153TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2153ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2153CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2153TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2153ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2153CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2253TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2253ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2253CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2253TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2253ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2253CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2253TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2253ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2253CTQM	-40 to 85	16 Ld QSOP	M16.15A-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

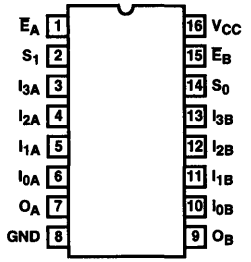
Description

The CD74FCT153T, CD74FCT253T, CD74FCT2153T and CD74FCT2253T are high-speed dual 4-input multiplexers. The CD74FCT153T and CD74FCT2153T have TTL outputs, while the CD74FCT253T and CD74FCT2253T have three-state outputs. The output buffers are designed with a poweroff disable allowing 'live insertion' of boards when used as backplane drivers.

The CD74FCT2153T and CD74FCT2253T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Pinout

CD74FCT153T, CD74FCT253T, CD74FCT2153T, CD74FCT2253T (QSOP, SOIC)
TOP VIEW

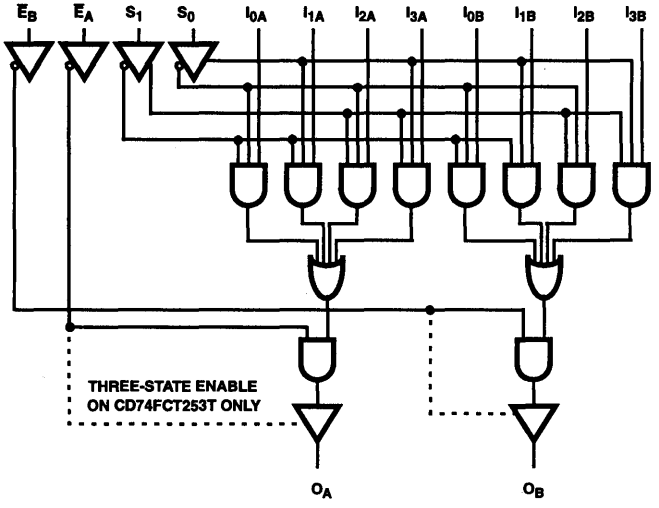


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **4161.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS				OUTPUTS			
				CD74FCT153, CD74FCT2153		CD74FCT253, CD74FCT2253	
$\overline{E}_A$	$\overline{E}_B$	S_1	S_0	O_A	O_B	O_A	O_B
H	X	X	X	L	X	Z	X
X	H	X	X	X	L	X	Z
L	L	L	L	I_{0A}	I_{0B}	I_{0A}	I_{0B}
L	L	L	H	I_{1A}	I_{1B}	I_{1A}	I_{1B}
L	L	H	L	I_{2A}	I_{2B}	I_{2A}	I_{2B}
L	L	H	H	I_{3A}	I_{3B}	I_{3A}	I_{3B}

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Description

PIN NAME	DESCRIPTION
I_{0A}-I_{3A}, I_{0B}-I_{3B}	Data Inputs
S_0, S_1	Select Inputs
$\overline{E}_A$, $\overline{E}_B$	Enable Input
O_A, O_B	Data Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
16 Lead SOIC (150 mil) Package	110
16 Lead SOIC (300 mil) Package	97
16 Lead QSOP Package	140

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ± 5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}, I_{OZL}	V_{CC} = Max	V_{OUT} = 2.7V			1	µA
			V_{OUT} = 0.5V			-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open Other Inputs at GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle Other Inputs at GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	3.2	6.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	3.5	7.5 (Note 9)	mA

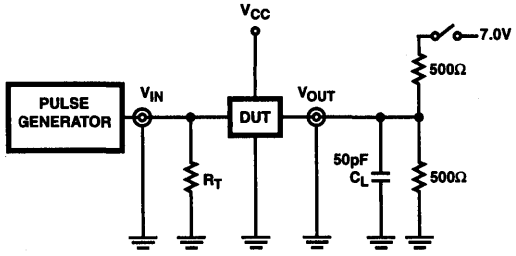
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T (NOTE 12) MIN	T MAX	AT (NOTE 12) MIN	AT MAX	CT (NOTE 12) MIN	CT MAX	UNIT
CD74FCT153T, CD74FCT2153T									
Propagation Delay Sn to O	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
Propagation Delay In to O	t_{PLH}, t_{PHL}		1.5	7.0	1.5	5.2	1.5	4.5	ns
Propagation Delay $\overline{E}$ to O	t_{PLH}, t_{PHL}		1.5	7.0	1.5	5.2	1.5	4.8	ns
CD74FCT253T, CD74FCT2253T									
Propagation Delay Sn to O	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
Propagation Delay In to O	t_{PLH}, t_{PHL}		1.5	7.0	1.5	5.2	1.5	4.5	ns
Output Enable Time $\overline{E}$ to O	t_{PZH}, t_{PZL}		1.5	9.0	1.5	6.0	1.5	5.0	ns
Output Enable Time $\overline{E}$ to O (Note 13)	t_{PHZ}, t_{PLZ}		1.5	7.0	1.5	6.0	1.5	5.0	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

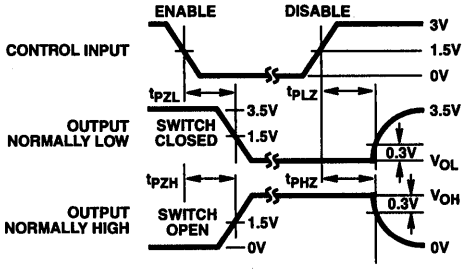


FIGURE 2. ENABLE AND DISABLE TIMING

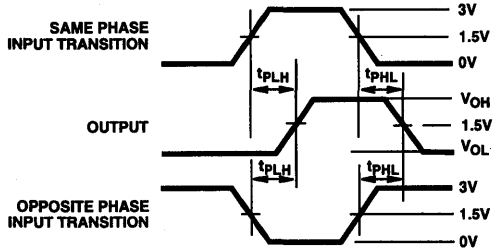


FIGURE 3. PROPAGATION DELAY

CD74FCT157T, CD74FCT257T, CD74FCT2157T, CD74FCT2257T

December 1996

Fast CMOS Quad 2-Input Multiplexers

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor On All Outputs (FCT2XXX Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs (25Ω Series Only)
- Extremely Low Static Power
- Hysteresis on All Inputs

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT157TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157DTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157TNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157ATNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157CTNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157DTNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT157TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT157ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT157CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT157DTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT257TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT257ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT257CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT257TNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT257ATNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT257CTNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT257TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT257ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT257CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2157TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2157ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2157CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2157TNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2157ATNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2157CTNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2157TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2157ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2157CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2257TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2257ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2257CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2257TNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2257ATNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2257CTNM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2257TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2257ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2257CTQM	-40 to 85	16 Ld QSOP	M16.15A-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

These devices are high-speed quad 2-input multiplexers. The common select input can be used to select four bits of data from two sources. The four buffered outputs present the selected data in the true (non-inverting) form.

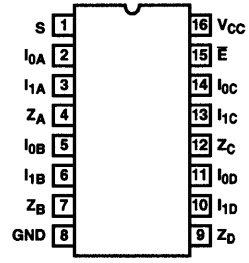
The CD74FCT157T and CD74FCT2157T have a common, active-LOW, Enable input ($\overline{E}$). When $\overline{E}$ is inactive, all four outputs are held LOW. The CD74FCT157T and CD74FCT2157T can generate any four of the 16 different funtions of two variables with one common variable. They can be used as a function generator or to move data from two different groups of registers to a common bus.

The CD74FCT257T and CD74FCT2257T have a common Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, all outputs are switched to a high-impedance state allowing the outputs to interface directly with bus-oriented systems.

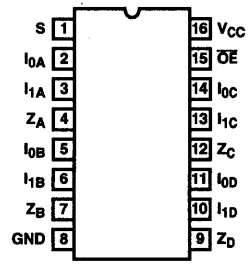
The CD74FCT2157T and CD74FCT2257T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Pinout

CD74FCT157T, 7CD74FCT2157T
(QSOP, SOIC)
TOP VIEW



CD74FCT257T, 7CD74FCT2257T
(QSOP, SOIC)
TOP VIEW



4

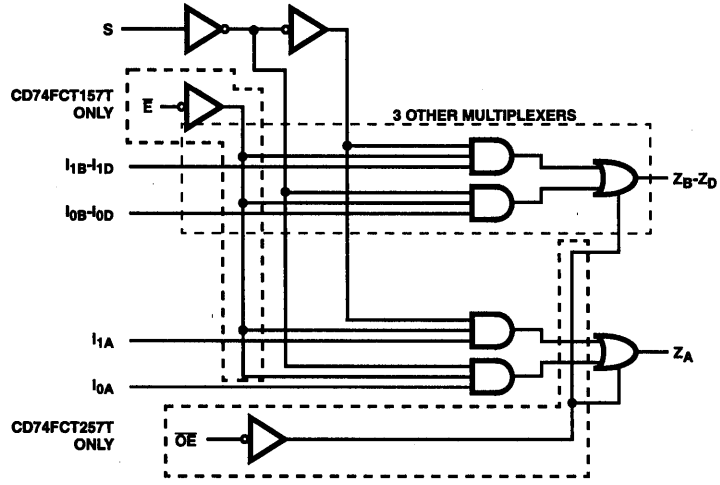
OCTAL 5V FCT
5V FCT 25Ω

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **4166.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS				OUTPUTS Z_N	
$\overline{E}/\overline{OE}$	S	I0	I1	CD74FCT157T, CD74FCT2157T	CD74FCT257T, CD74FCT2257T
H	X	X	X	L	Z
L	H	X	L	L	L
L	H	X	H	H	H
L	L	L	X	L	L
L	L	H	X	H	H

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
I_{0A}-I_{0D}	Source 0 Data Inputs
I_{1A}-I_{1D}	Source 1 Data Inputs
$\overline{E}$	Enable Input (Active LOW) CD74FCT157T, CD74FCT2157T
$\overline{OE}$	Output Enable (Active LOW) CD74FCT257T,CD74FCT2257T
S	Select Input
Z_A-Z_D	Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
SOIC Package 97
QSOP Package 140
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V			1	µA
	I_{OZL}		V_{OUT} = 0.5V			-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.5	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.8	4.5 (Note 9)	
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $\overline{E}$ or $\overline{OE}$ = GND Four Bits Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	3.5 (Note 9)	
			V_{IN} = 3.4V V_{IN} = GND	-	2.5	7.5 (Note 9)	

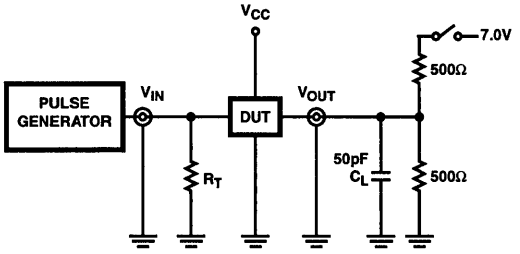
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T		AT		CT		(CD74FCT157T ONLY) DT		UNITS
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
CD74FCT157T, CD74FCT2157T											
Propagation Delay In to Z_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	5.0	1.5	4.3	1.5	3.9	ns
Propagation Delay $\overline{E}$ to Z_N	t_{PLH}, t_{PHL}		1.5	10.5	1.5	6.0	1.5	4.8	1.5	4.4	ns
Propagation Delay S to Z_N	t_{PLH}, t_{PHL}		1.5	10.5	1.5	7.0	1.5	5.2	1.5	4.6	ns
CD74FCT257T, CD74FCT2257T											
Propagation Delay In to Z_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	5.0	1.5	4.3	-	-	ns
Propagation Delay S to Z_N	t_{PLH}, t_{PHL}		1.5	10.5	1.5	7.0	1.5	5.2	-	-	ns
Output Enable Time $\overline{OE}$ to Z_N	t_{PZH}, t_{PZL}		1.5	8.5	1.5	7.0	1.5	6.0	-	-	ns
Output Disable Time $\overline{OE}$ to Z_N (Note 13)	t_{PZH}, t_{PZL}		1.5	6.0	1.5	5.5	1.5	5.0	-	-	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (Vin = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

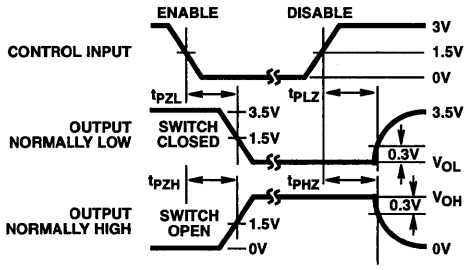


FIGURE 2. ENABLE AND DISABLE TIMING

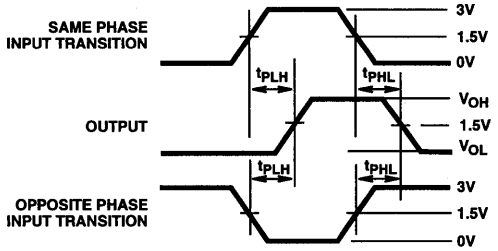


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT240T, CD74FCT241T, CD74FCT244T, CD74FCT540T, CD74FCT541T, CD74FCT2240T, CD74FCT2241T, CD74FCT2244T, CD74FCT2541T

October 1996

Fast CMOS Octal Buffer and Line Drivers

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **25Ω series resistor on all outputs (FCT2XXX only)**
- **TTL input and output levels**
- **Low ground bounce outputs**
- **Extremely low static power**
- **Hysteresis on all inputs**

Description

These devices are 8-bit wide driver circuits, designed to be used in applications requiring high-speed and high-output drive. Ideal applications would include bus drivers, memory drivers, address drivers, and system clock drivers.

The CD74FCT540T, CD74FCT541T and CD74FCT2541T provide similar driver capabilities, but have their pins physically grouped by function. All inputs are located on one side of the package, while outputs are on the opposite side, allowing for a much simpler and denser board layout.

All CD74FCT2240T, CD74FCT2241T, CD74FCT2244T, CD74FCT2541T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT240TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT240ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT240CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT240DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT240TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT240ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT240CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT240DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT241TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT241ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT241CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT241DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT241TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT241ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT241CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT241DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT244TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT244ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT244CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT244DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT244TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT244ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT244CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT244DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT540TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT540ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT540CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT540DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT540TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT540ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT540CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT540DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT541TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT541ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT541CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT541DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT541TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT541ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT541CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT541DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2240TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2240ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2240CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2240TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2240ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2241CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2241TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2241ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2241CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2241TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2241ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2241CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2244TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2244ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2244CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2244TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2244ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2244CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2541TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2541ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2541CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2541TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2541ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2541CTQM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

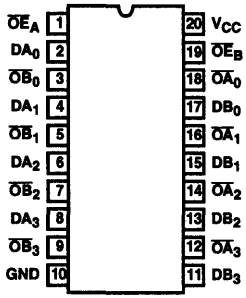
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

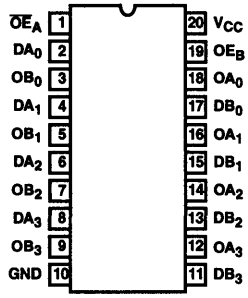
File Number **4167.1**

Pinouts

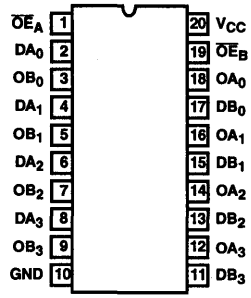
CD74FCT240T, CD74FCT2240T
(SOIC, QSOP)
TOP VIEW



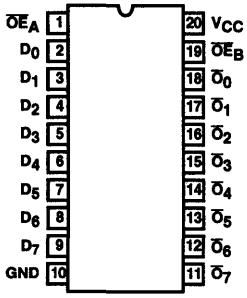
CD74FCT241T, CD74FCT2241T
(SOIC, QSOP)
TOP VIEW



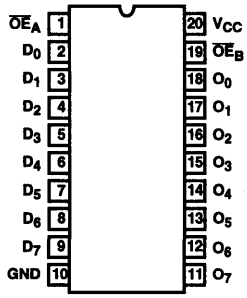
CD74FCT244T, CD74FCT2244T
(SOIC, QSOP)
TOP VIEW



CD74FCT540T
(SOIC, QSOP)
TOP VIEW

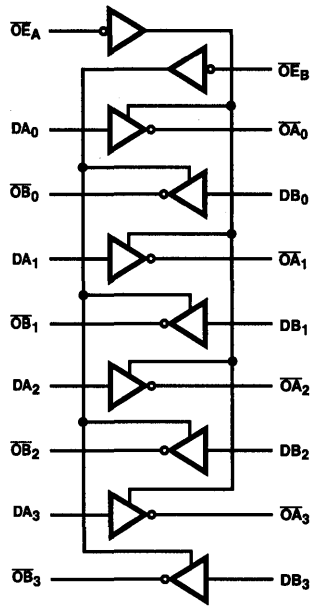


CD74FCT541T, CD74FCT2541
(SOIC, QSOP)
TOP VIEW

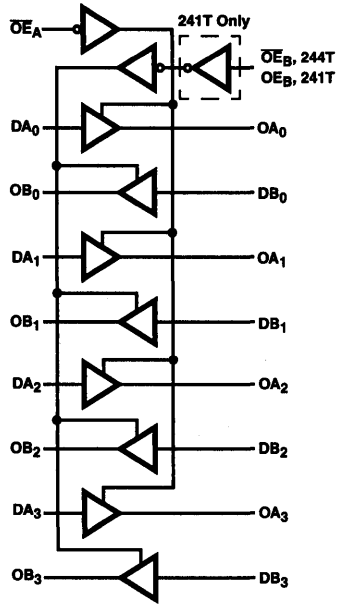


Functional Block Diagrams

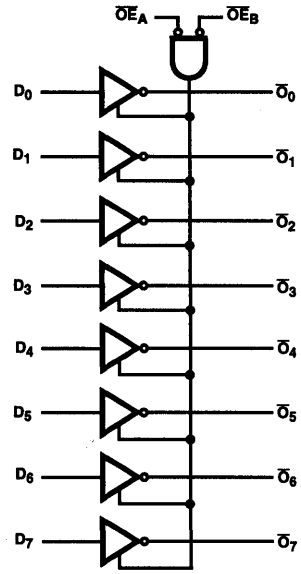
CD74FCT240T, CD74FCT2240T



CD74FCT241T, CD74FCT2241T, CD74FCT244T, CD74FCT2244T



CD74FCT540T, CD74FCT541T, CD74FCT2541T (Note)



NOTE: The logic diagram shown for the 540T, 541T, 2541T is the non-inverting option.

TRUTH TABLE (NOTE 1)

INPUTS				OUTPUTS				
$\overline{OE}_A$	$\overline{OE}_B$	(NOTE 2) OE_B	D	240	241	244	540	541
L	L	H	L	H	L	L	H	L
L	L	H	H	L	H	H	L	H
H	H	L	X	Z	Z	Z	Z	Z

NOTES:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
2. OE_B for CD74FCT241T only.

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
OE_B (NOTE 3)	3-State Output Enable Input (Active HIGH)
D_{XX}	Inputs
O_{XX}	Outputs
GND	Ground
V_{CC}	Power

NOTE:

3. OE_B for CD74FCT241T only.

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and Vcc Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
SOIC Package 87
QSOP Package 110
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V			1	µA
	I_{OZL}		V_{OUT} = 0.5V			-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 9)	-	0.5	2.5	mA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
Supply Current per Input per MHz (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}_A$ or $\overline{OE}_B$= GND or $\overline{OE}_A$ = GND, $\overline{OE}_B$ = V_{CC} One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND or $\overline{OE}_A$ = GND, $\overline{OE}_B$ = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	1.5	3.5 (Note 11)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.8	4.5 (Note 11)	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $\overline{OE}_A$ or $\overline{OE}_B$ = GND or $\overline{OE}_A$ = GND, $\overline{OE}_B$ = V_{CC} Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	3.0	6.0 (Note 11)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	5.0	14.0 (Note 11)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 13) TEST CONDITIONS	T (NOTE 14) MIN	T MAX	AT (NOTE 14) MIN	AT MAX	CT (NOTE 14) MIN	CT MAX	(NOTE 16) DT (NOTE 14) MIN	DT MAX	UNIT
CD74FCT240T, CD74FCT2240T											
Propagation Delay D_N to $\overline{O}_N$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	4.8	1.5	4.3	1.5	3.6	ns
Output Enable Time $\overline{OE}_X$ to $\overline{O}_N$	t_{PZH}, t_{PZL}		1.5	10.0	1.5	6.2	1.5	5.8	1.5	4.8	ns
Output Disable Time (Note 15) $\overline{OE}_X$ to $\overline{O}_N$	t_{PHZ}, t_{PLZ}		1.5	9.5	1.5	5.6	1.5	5.2	1.5	4.0	ns
CD74FCT241T, CD74FCT2241T											
Propagation Delay D_N to O_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	1.5	3.6	ns
Output Enable Time $\overline{OE}_A/\overline{OE}_B$ to O_N	t_{PZH}, t_{PZL}		1.5	8.0	1.5	6.2	1.5	5.8	1.5	4.8	ns
Output Disable Time (Note 15) $\overline{OE}_A/\overline{OE}_B$ to O_N	t_{PHZ}, t_{PLZ}		1.5	7.0	1.5	5.6	1.5	5.2	1.5	4.0	ns
CD74FCT244T, CD74FCT2244T											
Propagation Delay D_N to O_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	1.5	3.6	ns
Output Enable Time $\overline{OE}_X$ to O_N	t_{PZH}, t_{PZL}		1.5	8.0	1.5	6.2	1.5	5.8	1.5	4.8	ns
Output Disable Time (Note 15) $\overline{OE}_X$ to O_N	t_{PHZ}, t_{PLZ}		1.5	7.0	1.5	5.6	1.5	5.2	1.5	4.0	ns

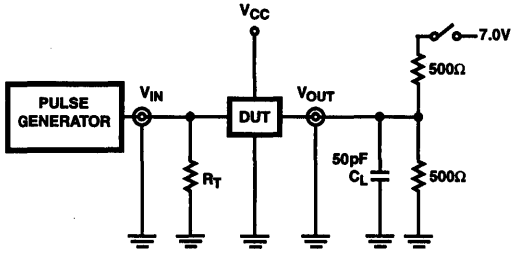
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 13) TEST CONDITIONS	T (NOTE 14) MIN	T MAX	AT (NOTE 14) MIN	AT MAX	CT (NOTE 14) MIN	CT MAX	(NOTE 16) DT (NOTE 14) MIN	DT MAX	UNIT
CD74FCT540T											
Propagation Delay D_N to $\overline{O}_N$	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	5.5	1.5	4.8	1.5	4.3	1.5	3.8	ns
Output Enable Time $\overline{OE}_X$ to $\overline{O}_N$	t_{PZH}, t_{PZL}		1.5	10.0	1.5	6.2	1.5	5.8	1.5	5.2	ns
Output Disable Time (Note 15) $\overline{OE}_X$ to $\overline{O}_N$	t_{PHZ}, t_{PLZ}		1.5	6.0	1.5	5.6	1.5	5.2	1.5	5.2	ns
CD74FCT541T, CD74FCT2541T											
Propagation Delay D_N to O_N	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	6.0	1.5	4.8	1.5	4.1	1.5	3.8	ns
Output Enable Time $\overline{OE}_X$ to O_N	t_{PZH}, t_{PZL}		1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.2	ns
Output Disable Time (Note 15) $\overline{OE}_X$ to O_N	t_{PHZ}, t_{PLZ}		1.5	6.5	1.5	5.6	1.5	5.2	1.5	5.2	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading, except as noted.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. See test circuit and wave forms.
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. This parameter is guaranteed but not production tested.
16. Suffix DT Speed for types FCT240T/241T/244T/540T/541T only.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

17. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

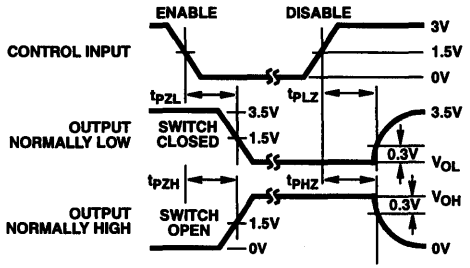


FIGURE 2. ENABLE AND DISABLE TIMING

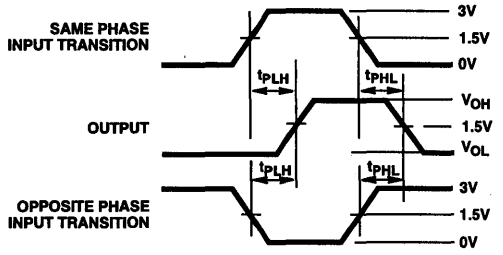


FIGURE 3. PROPAGATION DELAY

CD74FCT245T, CD74FCT640T, CD74FCT2245T

December 1996

Fast CMOS Octal Bidirectional Transceivers

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible With Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **25Ω Series Resistor on All Outputs (CD74FCT2245T)**
- **TTL input and output levels**
- **Low ground bounce outputs**
- **Extremely low static power**
- **Hysteresis on all inputs**

Description

These devices are 8-bit wide octal buffer bidirectional transceivers designed for asynchronous two-way communication between data buses. The transmit/receive ($T/\overline{R}$) input determines the direction of data flow through the bidirectional transceiver. Transmit (active HIGH) enables data from A ports to B ports, and receive (active LOW) from B ports to A ports. The output enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition

All CD74FCT2245T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

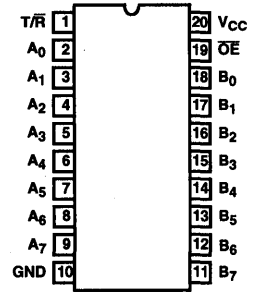
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT245ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT245ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT245CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT245CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT245DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT245DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT245TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT245TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT640ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT640ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT640CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT640CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT640DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT640DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT640TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT640TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2245ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2245ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2245CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2245CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2245TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2245TQM	-40 to 85	20 Ld QSOP	M20.15-P

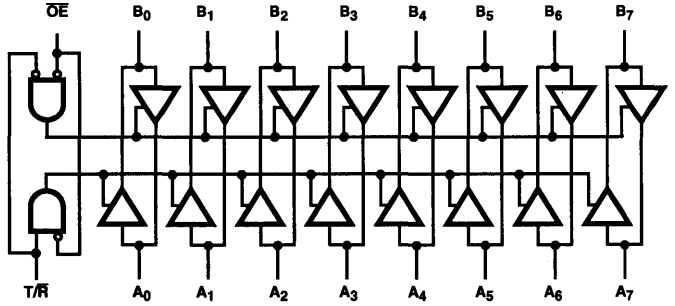
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74FCT245T, CD74FCT640T, CD74FCT2245
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram



NOTE: CD74FCT245T, CD74FCT2245T are non-inverting options. CD74FCT640T is the inverting option.

TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A (NOTE 2)
L	H	Bus A Data to Bus B (NOTE 2)
H	X	High Z State

NOTES:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance
2. CD74FCT640T is inverting from input to output.

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
T/$\overline{R}$	Transmit/Receive Input
A_0-A_7	Side A Inputs or Three-State Outputs
B_0-B_7	Side B Inputs or Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . $-40^{o}C$ to $85^{o}C$
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^{o}C/W$)
SOIC Package	87
QSOP Package	110

Maximum Junction Temperature . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^{o}C$ to $85^{o}C$, $V_{CC} = 5.0V \pm 5\%$							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 64mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 12mA (25Ω Series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	(Except I/O Pins) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input LOW Current	I_{IL}	(Except I/O Pins) V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
Input HIGH Current	I_{IH}	(I/O Pins Only) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input LOW Current	I_{IL}	(I/O Pins Only) V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
HIGH Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}		V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 6), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE $T_A = 25^{o}C$, f = 1MHz							
Input Capacitance (Note 7)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 7)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 8)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 9)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$=GND T/$\overline{R}$=GND or V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 11)	I_C	V_{CC} = Max, Outputs Open f_T = 10MHz, 50% Duty Cycle T/$\overline{R}$=$\overline{OE}$=GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	1.5	3.5 (Note 10)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.8	4.5 (Note 10)	mA
		V_{CC} = Max, Outputs Open f_T = 2.5MHz, 50% Duty Cycle T/$\overline{R}$=$\overline{OE}$=GND Eight Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	3.0	6.0 (Note 10)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	5.0	14.0 (Note 10)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	T		AT		CT		DT		UNITS
			(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	
CD74FCT245T, CD74FCT2245T											
Propagation Delay A to B, B to A	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	1.5	3.8	ns
Output Enable Time $\overline{OE}$ to A or B	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time $\overline{OE}$ to A or B (Note 14)	t_{PHZ}, t_{PLZ}	C_L = 50pF R_L = 500Ω	1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	ns
Output Enable Time T/$\overline{R}$ to A or B	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time T/$\overline{R}$ to A or B (Note 14)	t_{PHZ}, t_{PLZ}	C_L = 50pF R_L = 500Ω	1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	ns
CD74FCT640T											
Propagation Delay A to B, B to A	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2	7.0	1.5	5.0	1.5	4.4	1.5	3.7	ns
Output Enable Time $\overline{OE}$ to A or B	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	2	13.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time $\overline{OE}$ to A or B (Note 14)	t_{PHZ}, t_{PLZ}	C_L = 50pF R_L = 500Ω	2	10.0	1.5	5.0	1.5	4.8	1.5	4.3	ns

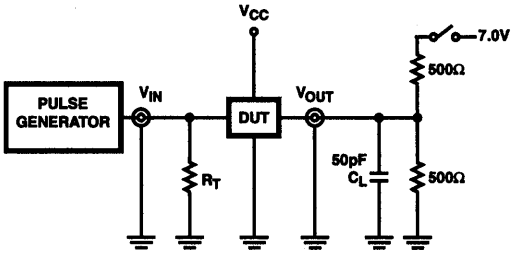
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	T		AT		CT		DT		UNITS
			(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	(NOTE 13) MIN	MAX	
Output Enable Time $T/\overline{R}$ to A or B	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	2	13.0	1.5	6.2	1.5	5.8	1.5	5.0	ns
Output Disable Time $T/\overline{R}$ to A or B (Note 14)	t_{PHZ}, t_{PLZ}	C_L = 50pF R_L = 500Ω	2	10.0	1.5	5.0	1.5	4.8	1.5	4.3	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. This parameter is determined by device characterization but is not production tested.
8. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
12. See test circuit and wave forms.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

15. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

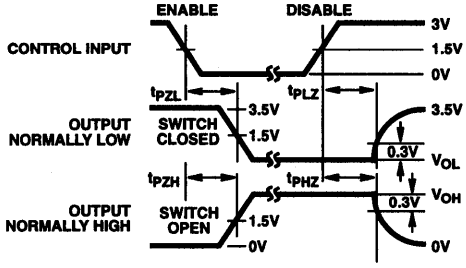


FIGURE 2. ENABLE AND DISABLE TIMING

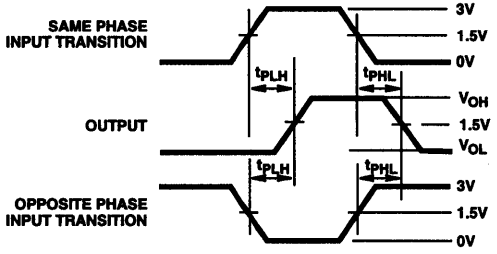


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT273T, CD74FCT2273T

December 1996

Fast CMOS Octal D Flip-Flops with Master Reset

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **25Ω Series Resistor On All Outputs (FCT2273T Only)**
- **TTL Input and Output Levels**
- **Low Ground Bounce Outputs**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT273TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT273ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT273CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT273DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT273TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT273ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT273CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT273DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2273TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2273ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2273CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2273TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2273ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2273CTQM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

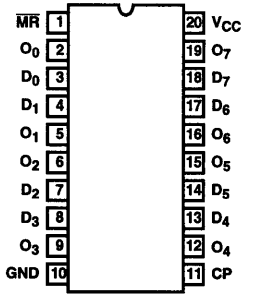
Description

The CD74FCT273T and CD74FCT2273T are 8-bit wide octal designed with eight edge-triggered D-type flip-flops with individual D inputs and O outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) load and resets (clear) all flip-flops simultaneously. The register is fully edge-triggered. The D input state, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the $\overline{MR}$ input.

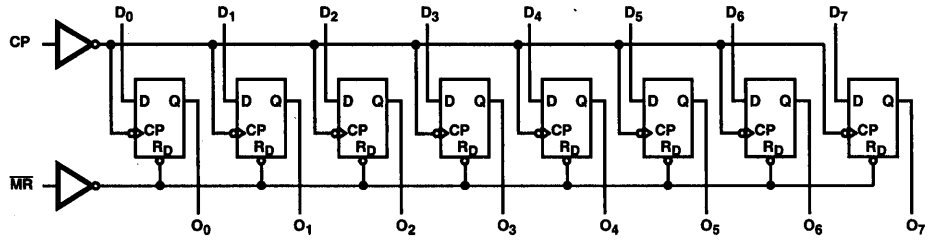
The CD74FCT2273T device has a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Pinouts

CD74FCT273T, CD74FCT2273T
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

MODE	INPUTS			OUTPUTS
	$\overline{MR}$	CP	D_N	O_N
Reset (Clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

NOTE:

1. H = High Voltage Level
   h = HIGH Voltage Level One Setup Time Prior to the LOW-to-HIGH Clock Transition
   L = Low Voltage Level
   l = LOW Voltage Level One Setup Time Prior to the LOW-to-HIGH Clock Transition
   X = Don't Care
   ↑ = LOW-to-HIGH Clock Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{MR}$	Master Reset (Active LOW)
CP	Clock Pulse Input (Active Rising Edge)
D_0-D_7	Data Inputs
O_0-O_7	Data Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	87
QSOP Package	110

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω Series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}		V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{MR}$ = V_{CC}, One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{MR}$ = V_{CC}, 50% Duty Cycle One Bit Toggling at f_i = 5MHz	V_{IN} = V_{CC} Vin = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.5 (Note 9)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{MR}$ = VCC, 50% Duty Cycle Eight Bits Toggling at f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.8	7.3 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.0	16.3 (Note 9)	mA

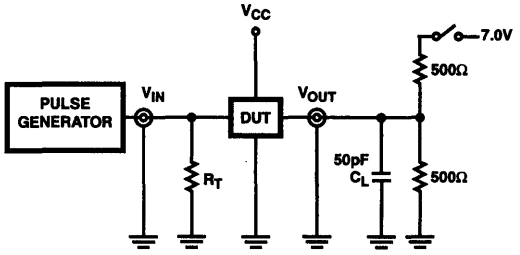
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T (NOTE 12) MIN	T MAX	AT (NOTE 12) MIN	AT MAX	CT (NOTE 12) MIN	CT MAX	DT (NOTE 14) (NOTE 12) MIN	DT (NOTE 14) MAX	UNITS
Propagation Delay CP to On	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	13.0	2.0	7.2	2.0	5.8	2.0	4.4	ns
Propagation Delay $\overline{MR}$ to On	t_{PHL}, t_{PLH}	C_L = 50pF R_L = 500Ω	2.0	13.0	2.0	7.2	2.0	6.1	2.0	5.0	ns
Setup Time, HIGH or LOW D_N to CP	t_{SU}	C_L = 50pF R_L = 500Ω	3.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time, HIGH or LOW D_N to CP	t_H	C_L = 50pF R_L = 500Ω	2.0	-	1.5	-	1.5	-	1.5	-	ns
CP Pulse Width HIGH or LOW (Note 13)	t_W	C_L = 50pF R_L = 500Ω	7.0	-	6.0	-	6.0	-	3.0	-	ns
$\overline{MR}$ Pulse Width LOW (Note 13)	t_W	C_L = 50pF R_L = 500Ω	7.0	-	6.0	-	6.0	-	3.0	-	ns
Recovery Time MR to CP (Note 13)	t_{REM}	C_L = 50pF R_L = 500Ω	4.0	-	2.0	-	2.0	-	2.0	-	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (Vin = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter guaranteed but not production tested.
14. Suffix DT applies to CD74FCT273T type only.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

15. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

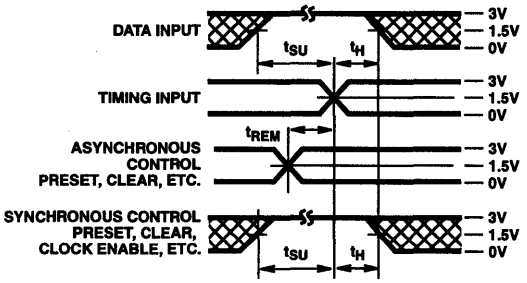


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

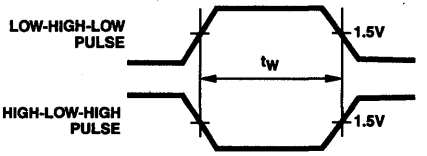


FIGURE 3. PULSE WIDTH

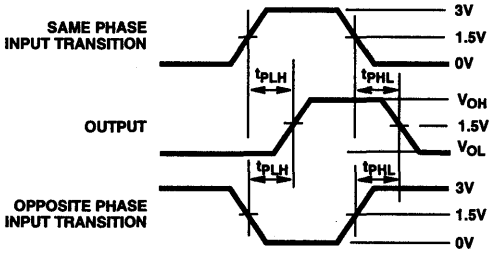


FIGURE 4. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT373T, CD74FCT533T, CD74FCT573T, CD74FCT2373T, CD74FCT2573T

December 1996

Fast CMOS Octal Transparent Latches

Features

- **Advanced 0.8 micron CMOS Technology**
- **Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **25Ω Series Resistor on All Outputs (CD74FCT2373T, CD74FCT2573T Only)**
- **TTL Input and Output Levels**
- **Low Ground Bounce Outputs**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Description

These devices are 8-bit wide octal transparent latches designed with three-state outputs and are intended for bus oriented applications. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

The CD74FCT2XXX device has a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT373ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT373ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT373CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT373CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT373DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT373DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT373TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT373TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT533ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT533ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT533CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT533CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT533TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT533TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT573ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT573ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT573CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT573CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT573DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT573DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT573TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT573TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2373ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2373ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2373CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2373CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2373TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2373TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2573ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2573ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2573CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2573CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2573TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2573TQM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

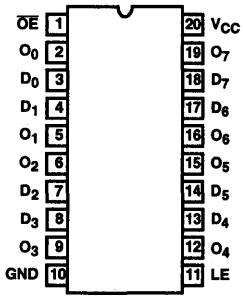
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

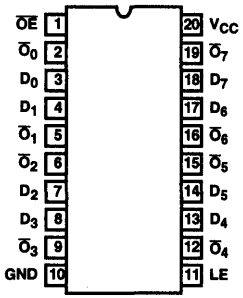
File Number **4170.2**

Pinouts

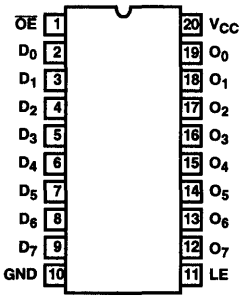
CD74FCT373T, CD74FCT2373T
(QSOP, SOIC)
TOP VIEW



CD74FCT533T
(QSOP, SOIC)
TOP VIEW

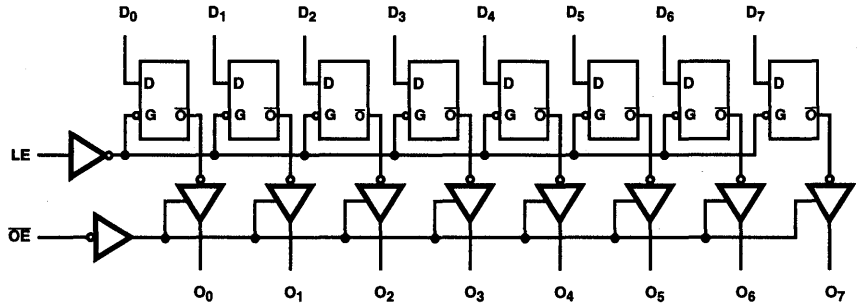


CD74FCT573T, CD74FCT2573T
(QSOP, SOIC)
TOP VIEW

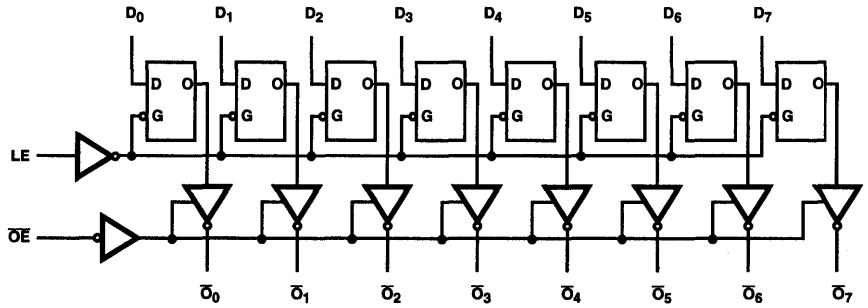


Functional Block Diagrams

CD74FCT373T, CD74FCT2373T, CD74FCT573, CD74FCT2573T



CD74FCT533T



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
D_N	LE	$\overline{OE}$	$\overline{O}_N$
CD74FCT533T			
H	H	L	L
L	H	L	H
X	X	H	Z

TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
D_N	LE	$\overline{OE}$	O_N
CD74FCT373T, CD74FCT573T, CD74FCT2373T, CD74FCT2573T			
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
LE	Latch Enable Input (Active HIGH)
D_0-D_7	Data Inputs
O_0-O_7	Three-State Outputs
$\overline{O}_0$-$\overline{O}_7$	Complementary Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	87
QSOP Package	110

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω Series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}		V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$ = GND; LE = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND; LE = V_{CC} One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	3.0 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.8	4.5 (Note 9)	mA
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $\overline{OE}$ = GND; LE = V_{CC} Eight Bits Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.0	6.0 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	5.0	14.0 (Note 9)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T (NOTE 12) MIN	T MAX	AT (NOTE 12) MIN	AT MAX	CT (NOTE 12) MIN	CT MAX	DT CD74FCT373T ONLY (NOTE 12) MIN	DT CD74FCT373T ONLY MAX	UNITS
CD74FCT373T, CD74FCT2373T											
Propagation Delay D_N to O_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	ns
Propagation Delay LE to O_N	t_{PLH}, t_{PHL}		2.0	13.0	2.0	8.5	2.0	5.5	1.5	4.9	ns
Output Enable Time $\overline{OE}$ to O_N	t_{PZH}, t_{PZL}		1.5	12.0	1.5	6.5	1.5	5.5	1.5	5.5	ns
Output Disable Time (Note 13) $\overline{OE}$ to O_N	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.5	1.5	5.0	1.5	5.0	ns
Setup Time HIGH or LOW, D_N to LE	t_{SU}		2.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, D_N to LE	t_H		1.5	-	1.5	-	1.5	-	1.5	-	ns
LE Pulse Width (Note 13) HIGH	t_W		6.0	-	5.0	-	5.0	-	4.0	-	ns
CD74FCT533T											
Propagation Delay D_N to O_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	5.2	1.5	4.2	-	-	ns
Propagation Delay LE to On	t_{PLH}, t_{PHL}		2.0	13.0	2.0	8.5	2.0	5.5			ns
Output Enable Time $\overline{OE}$ to O_N	t_{PZH}, t_{PZL}		1.5	11.0	1.5	6.5	1.5	5.5	-	-	ns
Output Disable Time (Note 13) $\overline{OE}$ to O_N	t_{PHZ}, t_{PLZ}		1.5	7.0	1.5	5.5	1.5	5.0			ns
Setup Time HIGH or LOW, D_N to LE	t_{SU}		2.0	-	2.0	-	2.0	-	-	-	ns
Hold Time HIGH or LOW, D_N to LE	t_H		1.5	-	1.5	-	1.5	-			ns
LE Pulse Width (Note 13) HIGH	t_W		6.0	-	5.0	-	5.0	-	-	-	ns

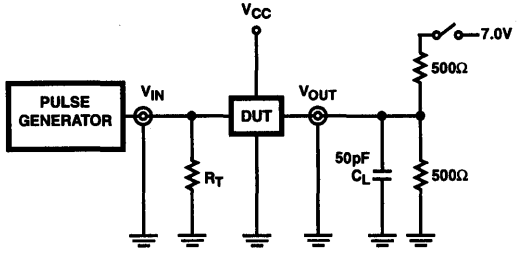
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T (NOTE 12) MIN	T MAX	AT (NOTE 12) MIN	AT MAX	CT (NOTE 12) MIN	CT MAX	DT CD74FCT373T ONLY (NOTE 12) MIN	DT CD74FCT373T ONLY MAX	UNITS
CD74FCT573T, CD2573T											
Propagation Delay D_N to $\overline{O}_N$	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	-	-	ns
Propagation Delay LE to $\overline{O}n$	t_{PLH}, t_{PHL}		2.0	12.0	2.0	8.5	2.0	5.5	-	-	ns
Output Enable Time $\overline{OE}$ to O_N	t_{PZH}, t_{PZL}		1.5	9.5	1.5	6.5	1.5	5.5	-	-	ns
Output Disable Time (Note 13) $\overline{OE}$ to O_N	t_{PHZ}, t_{PLZ}		1.5	6.5	1.5	5.5	1.5	5.0	-	-	ns
Setup Time HIGH or LOW, D_N to LE	t_{SU}		2.0	-	2.0	-	2.0	-	-	-	ns
Hold Time HIGH or LOW, D_N to LE	t_H		1.5	-	1.5	-	1.5	-	-	-	ns
LE Pulse Width (Note 13) HIGH	t_W		6.0	-	5.0	-	5.0	-	-	-	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

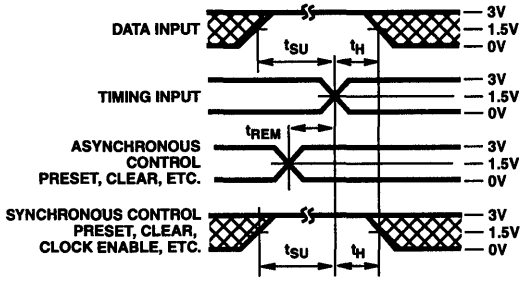


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

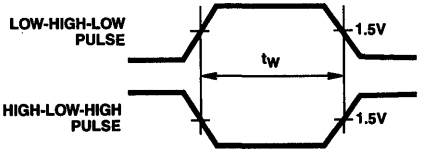


FIGURE 3. PULSE WIDTH

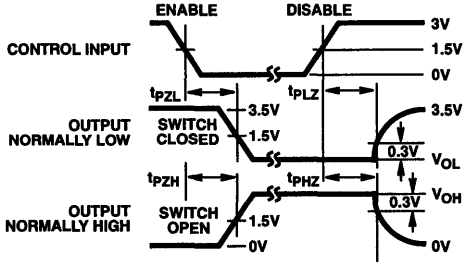


FIGURE 4. ENABLE AND DISABLE TIMING

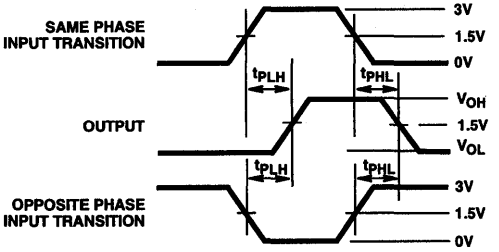


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT374T, CD74FCT534T, CD74FCT574T, CD74FCT2374T, CD74FCT2574T

December 1996

Fast CMOS Octal D Registers (Three-State)

Features

- **Advanced 0.8 micron CMOS Technology**
- **Pin Compatible With Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **25Ω Series Resistor on All Outputs (CD74FCT2374T, CD74FCT2574T only)**
- **TTL Input and Output Levels**
- **Low Ground Bounce Outputs**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Description

These devices are 8-bit wide octal registers designed with eight D-type flip-flops with a buffered common clock and buffered three-state outputs. When output enable ($\overline{OE}$) is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

All CD74FCT2574T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

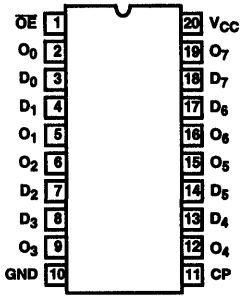
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT374ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT374ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT374CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT374CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT374DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT374DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT374TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT374TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT534ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT534ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT534CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT534CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT534DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT534DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT534TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT534TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT574ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT574ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT574CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT574CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT574DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT574DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT574TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT574TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2374ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2374ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2374CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2374CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2374TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2374TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2574ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2574ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2574CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2574CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT2574TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT2574TQM	-40 to 85	20 Ld QSOP	M20.15-P

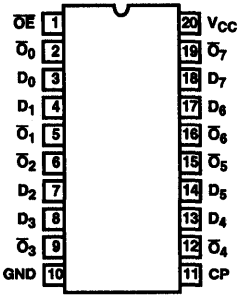
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinouts

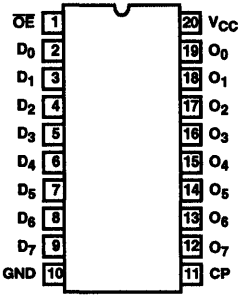
CD74FCT374T, CD74FCT2374T
(QSOP, SOIC)
TOP VIEW



CD74FCT534T
(QSOP, SOIC)
TOP VIEW

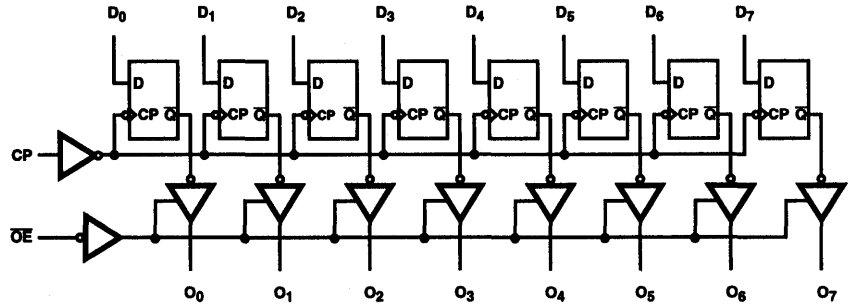


CD74FCT574T, CD74FCT2574T
(QSOP, SOIC)
TOP VIEW

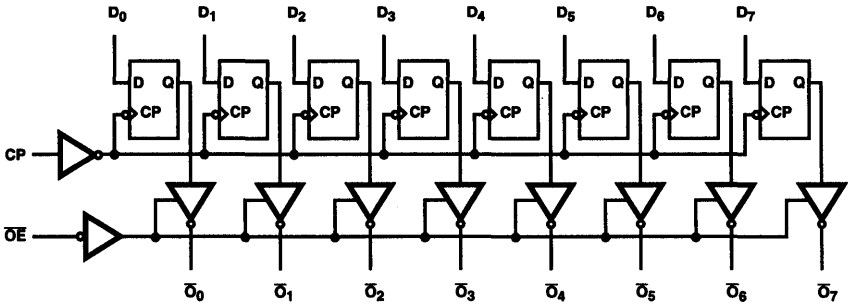


Functional Block Diagrams

CD74FCT374T, CD74FCT2374T, CD74FCT574, CD74FCT2574T



CD74FCT534T



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS			OUTPUTS	INTERNAL
	$\overline{OE}$	CP	D_N	$\overline{O}_N$	Q_N
CD74FCT534T					
High-Z	H	L	X	Z	NC
	H	H	X	Z	NC
Load Register	L	↑	L	H	L
	L	↑	H	L	H
	H	↑	L	Z	L
	H	↑	H	Z	H
CD74FCT374T, CD74FCT574T, CD74FCT2374T, CD74FCT2574T					
FUNCTION	$\overline{OE}$	CP	D_N	O_N	$\overline{Q}_N$
High-Z	H	L	X	Z	NC
	H	H	X	Z	NC
Load Register	L	↑	L	L	H
	L	↑	H	H	L
	H	↑	L	Z	H
	H	↑	H	Z	L

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change
   ↑ = LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
CP	Clock Pulse for the register. Enters data on LOW-to-HIGH transition
D_0-D_7	Data Inputs
O_0-O_7	Three-State Outputs (True)
$\overline{O}_0$-$\overline{O}_7$	Three-State Outputs (Inverted)
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	87
QSOP Package	110

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω Series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}		V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND f_i = 5MHz, One Bit toggling	V_{IN} = V_{CC} V_{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.5 (Note 9)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND f_i = 2.5MHz, Eight Bits toggling	V_{IN} = V_{CC} V_{IN} = GND	-	3.5	7.3 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.0	16.3 (Note 9)	mA

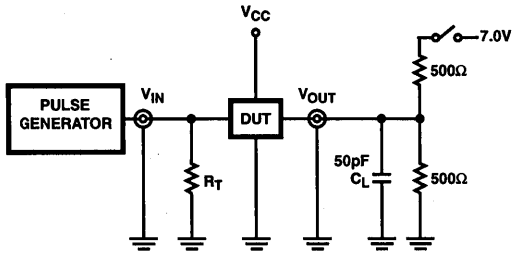
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T (NOTE 12) MIN	T MAX	AT (NOTE 12) MIN	AT MAX	CT (NOTE 12) MIN	CT MAX	DT (NOTE 12) MIN	DT MAX	UNITS
CD74FCT374T, CD74FCT534T, CD74FCT2374T											
Propagation Delay CP to O_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	6.5	2.0	5.2	2.0	4.5	ns
Output Enable Time $\overline{OE}$ to O_N	t_{PZH}, t_{PZL}		1.5	12.5	1.5	6.5	1.5	5.5	1.5	5.5	ns
Output Disable Time (Note 13) $\overline{OE}$ to O_N	t_{PHZ}, t_{PLZ}		1.5	8.0	1.5	5.5	1.5	5.0	1.5	5.0	ns
Setup Time HIGH or LOW, D_N to CP	t_{SU}		2.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, D_N to CP	t_H		1.5	-	1.5	-	1.5	-	1.0	-	ns
CP Pulse Width (Note 13) HIGH or LOW	t_W		7.0	-	5.0	-	5.0	-	3.0	-	ns
CD74FCT574T, CD74FCT2574T											
Propagation Delay CP to $\overline{O}_N$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	8.5	2.0	6.5	2.0	5.2	2.0	4.5	ns
Output Enable Time $\overline{OE}$ to O_N	t_{PZH}, t_{PZL}		1.5	10.0	1.5	6.5	1.5	5.5	1.5	5.5	ns
Output Disable Time (Note 13) $\overline{OE}$ to O_N	t_{PHZ}, t_{PLZ}		1.5	6.5	1.5	5.5	1.5	5.0	1.5	5.0	ns
Setup Time HIGH or LOW, D_N to CP	t_{SU}		2.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, D_N to CP	t_H		1.5	-	1.5	-	1.5	-	1.0	-	ns
CP Pulse Width (Note 13) HIGH or LOW	t_W		7.0	-	5.0	-	5.0	-	3.0	-	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

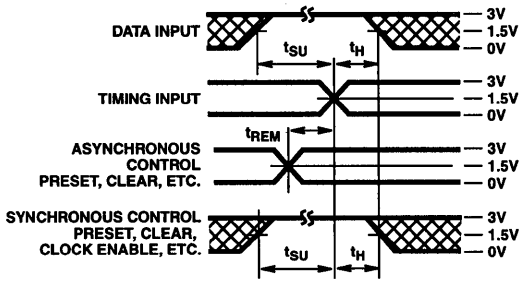


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

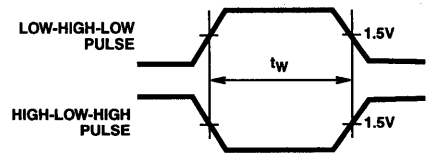


FIGURE 3. PULSE WIDTH

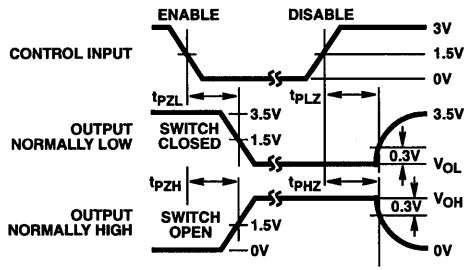


FIGURE 4. ENABLE AND DISABLE TIMING

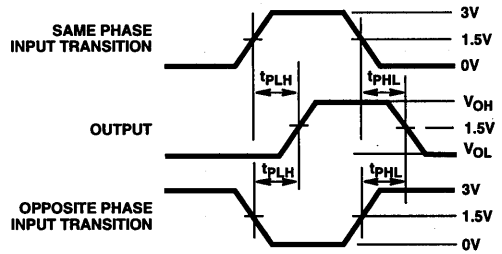


FIGURE 5. PROPAGATION DELAY

CD74FCT377T

December 1996

Fast CMOS Octal D Flip-Flop with Clock Enable

Features

- **Advanced 0.8 micron CMOS Technology**
- **The CD74FCT377T is Pin Compatible With Bipolar FAST™ Series at a Higher Speed And Lower Power Consumption**
- **TTL Input and Output Levels**
- **Octal D Flip-Flops with Clock Enable**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Description

The CD74FCT377T is an 8-bit wide octal designed with eight edge-triggered D-type flip-flops with individual D inputs and O outputs. When Clock Enable ($\overline{CE}$) is LOW, the common buffered Clock (CP) loads all flip-flops simultaneously. The register is fully edge-triggered. The D input state, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's O output. The $\overline{CE}$ input must be stable only one setup time prior to the LOW-to-HIGH transition for predictable operation.

Ordering Information

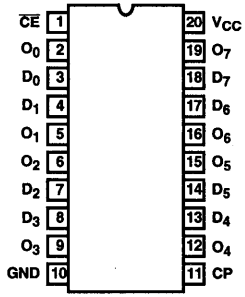
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT377ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT377ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT377CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT377CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT377DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT377DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT377TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT377TQM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

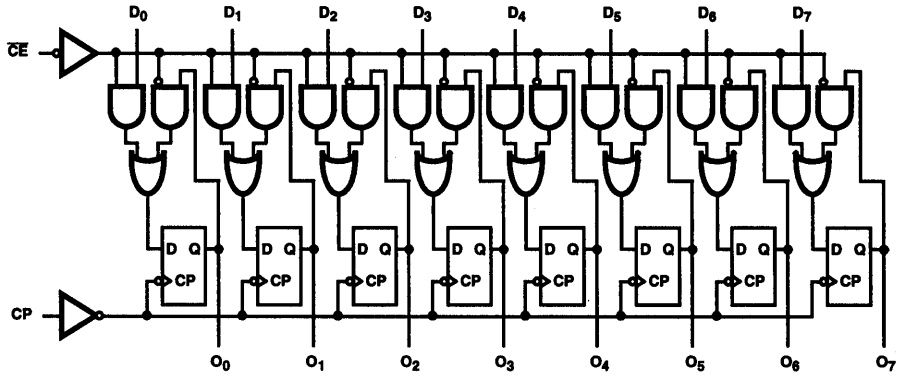
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74FCT377T
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram



TRUTH TABLE

MODE	(NOTE 1) INPUTS			(NOTE 1) OUTPUTS
	CP	$\overline{CE}$	D_N	O_N
Load "1"	↑	l	h	H
Load "0"	↑	l	l	L
Hold (Do Nothing)	↑ H	h H	X X	NC NC

NOTE:

1. H = HIGH Voltage Level
   h = HIGH Voltage Level One Setup Time Prior to the LOW-to-HIGH Clock Transition
   L = LOW Voltage Level
   l = LOW Voltage Level One Setup Time Prior to the LOW-to-HIGH Clock Transition
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Clock Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{CE}$	Clock Enable (Active LOW)
CP	Clock Pulse Input
D_0-D_7	Data Inputs
O_0-O_7	Data Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	87
QSOP Package	110

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{CE}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{CE}$ = GND, 50% Duty Cycle One Bit Toggling at f_i = 5MHz	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.5 (Note 9)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{CE}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.8	7.3 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.0	16.3 (Note 9)	mA

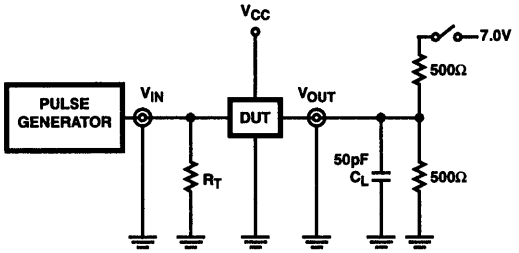
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T (NOTE 12) MIN	T MAX	AT (NOTE 12) MIN	AT MAX	CT (NOTE 12) MIN	CT MAX	DT (NOTE 12) MIN	DT MAX	UNITS
Propagation Delay CP to O_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	13.0	2.0	7.2	2.0	5.2	2.0	4.5	ns
Setup Time, HIGH or LOW, D_N to CP	t_{SU}		2.5	-	2.0	-	2.0	-	2.0	-	ns
Hold Time, HIGH or LOW, D_N to CP	t_H		2.0	-	1.5	-	1.5	-	1.5	-	ns
Setup Time HIGH or LOW, $\overline{CE}$ to CP	t_{SU}		4.0	-	3.5	-	3.5	-	2.0	-	ns
Hold Time HIGH or LOW, $\overline{CE}$ to CP	t_H		1.5	-	1.5	-	1.5	-	1.5	-	ns
Clock Pulse Width (Note 13) HIGH or LOW	t_W		7.0	-	6.0	-	6.0	-	3.0	-	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

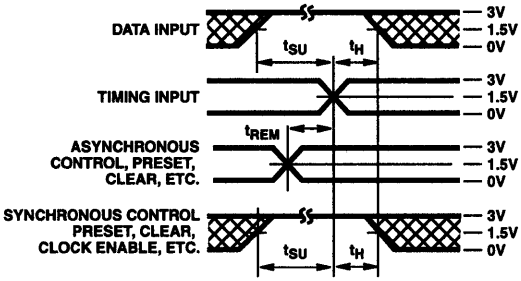


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

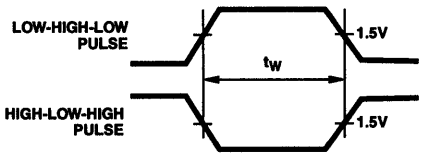


FIGURE 3. PULSE WIDTH

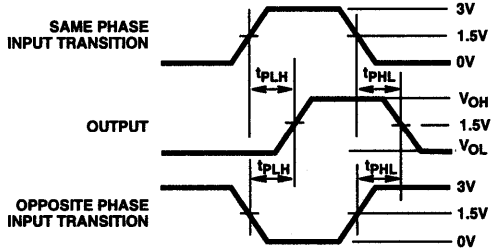


FIGURE 4. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT399T

December 1996

Fast CMOS Quad Dual-Port Register

Features

- **Advanced 0.8 micron CMOS Technology**
- **The CD74FCT399T is Pin Compatible With Bipolar FAST™ Series at a Higher Speed And Lower Power Consumption**
- **TTL Input and Output Levels**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Description

These high-speed quad dual-port registers select 4-bit wide data from one of the two sources (Ports) under control of a common Select input (S). Synchronous with the LOW-to-HIGH transition of the Clock input (CP), the selected data is transferred to a 4-bit output register. The 4-bit D-type output register is fully edge-triggered. For predictable operation, the Data inputs (I_{AX}, I_{BX}) and Select input (S) must be stable one set-up time prior to, and hold time after, the LOW-to-HIGH transition of the Clock input.

Ordering Information

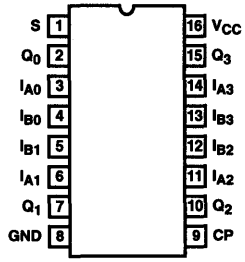
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT399ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT399CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT399TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT399ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT399CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT399TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT399ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT399CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT399TQM	-40 to 85	16 Ld QSOP	M16.15A-P

NOTE: QSOP is commonly known as SSOP.

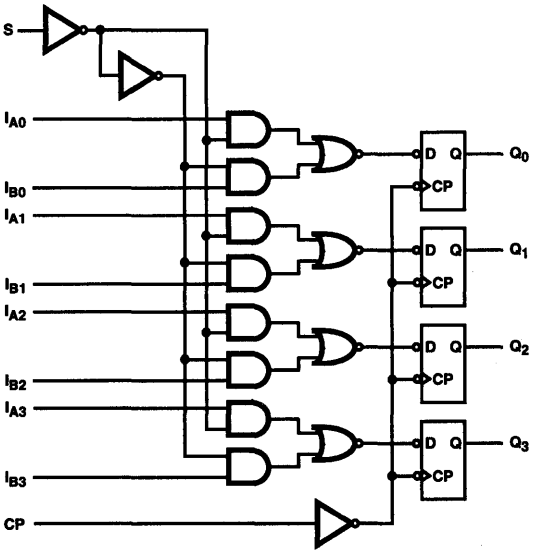
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74FCT399T
(SOIC, QSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE

INPUTS			OUTPUTS
S	I_A	I_B	Q
l	l	X	L
l	h	X	H
h	X	l	L
h	X	h	H

NOTE:

1. H = HIGH Voltage Level
   h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock trasition
   L = LOW Voltage Level
   l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock trasition
   X = Don't Care

Pin Descriptions

PIN NAME	DESCRIPTION
S	Common Select Input
CP	Clock Pulse Input
I_{A0} - I_{A3}	Data Inputs from Source A
I_{B0} - I_{B3}	Data Inputs from Source B
Q_0 - Q_3	Register True Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package (M16.15-P)	110
SOIC Package (M16.3-P)	97
QSOP Package	140

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V 5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle S = GND, 50% Duty Cycle One Bit Toggling at f_I = 5MHz	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.5 (Note 9)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle S = GND Eight Bits Toggling at f_I = 2.5MHz 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.8	7.3 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	5.0	12.3 (Note 9)	mA

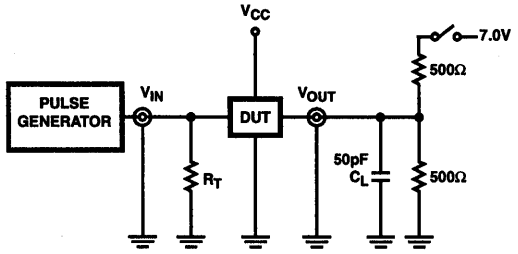
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T (NOTE 12) MIN	T MAX	AT (NOTE 12) MIN	AT MAX	CT (NOTE 12) MIN	CT MAX	UNITS
Propagation Delay CP to Q	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	3.0	10.0	2.5	7.0	2.5	5.6	ns
Setup Time, HIGH or LOW D to Q	t_{SU}		4.0	-	3.5	-	3.0	-	ns
Hold Time, HIGH or LOW D to Q	t_H		1.0	-	1.0	-	1.0	-	ns
Setup Time, HIGH or LOW S to CP	t_{SU}		9.0	-	8.5	-	3.0	-	ns
Hold Time, HIGH or LOW	t_H		0	-	0	-	0	-	ns
Clock Pulse Width (Note 13), HIGH or LOW	t_W		5.0	-	5.0	-	4.0	-	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_O
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuits and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

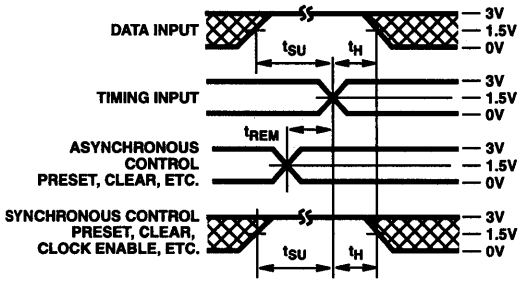


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

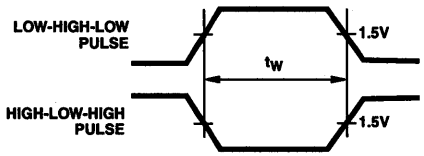


FIGURE 3. PULSE WIDTH

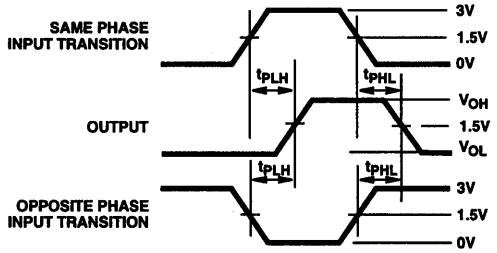


FIGURE 4. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT521T

December 1996

Fast CMOS 8-Bit Identity Comparator

Features

- **Advanced 0.8 micron CMOS Technology**
- **CD74FCT521T is Pin Compatible with Bipolar FAST™ Series at a Higher Speed And Lower Power Consumption**
- **TTL Input and Output Levels**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Description

The CD74FCT521T is an 8-bit identity comparator. When two words of up to eight bits are compared, a bit-for-bit match of the two words provides a LOW output. The comparison can be extended over multiple words by the expansion input. The expansion input $\overline{I}_{A=B}$ also serves as an active LOW enable input.

Ordering Information

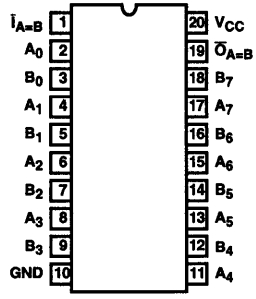
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT521ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT521BTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521BTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT521CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT521DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521DTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT521TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT521TQM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

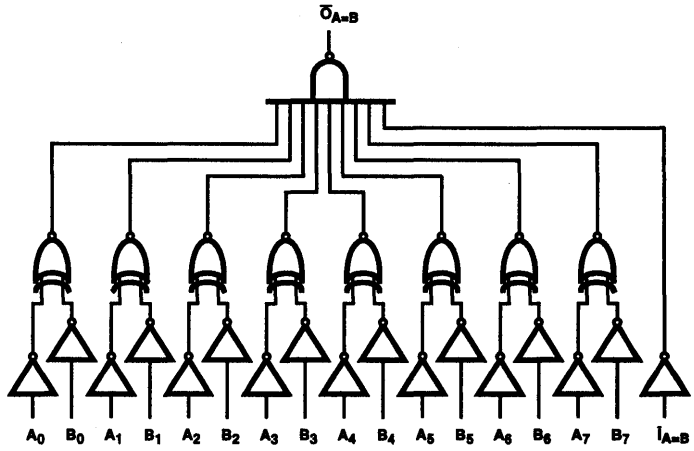
CD74FCT521T
(QSOP, SOIC)
TOP VIEW



4

OCTAL 5V FCT
5V FCT 25Ω

Functional Block Diagram



TRUTH TABLE

(NOTE 1) INPUTS		(NOTE 1) OUTPUTS
$\overline{I}_{A=B}$	A, B	$\overline{O}_{A=B}$
L	A = B (Note 2)	L
L	A ≠ B	H
H	A = B (Note 2)	H
H	A ≠ B	H

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
2. $A_0 = B_0$, $A_1 = B_1$, $A_2 = B_2$, etc.

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{I}_{A=B}$	Expansion or Enable Input (Active LOW)
$\overline{O}_{A=B}$	Identity Output (Active LOW)
A_0 - A_7	Word A Inputs
B_0 - B_7	Word B Inputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
SOIC Package	87
QSOP Package	110

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 6), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 7)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 7)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 8)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 9)	I_{CCD}	V_{CC} = Max, Outputs Open One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 11)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	1.5	3.5 (Note 10)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.8	4.5 (Note 10)	mA

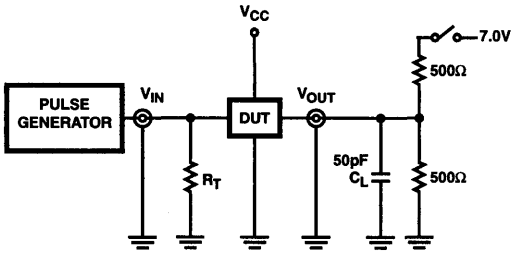
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	T (NOTE 13) MIN	T MAX	AT (NOTE 13) MIN	AT MAX	BT (NOTE 13) MIN	BT MAX	CT (NOTE 13) MIN	CT MAX	DT (NOTE 13) MIN	DT MAX	UNITS
Propagation Delay A_N or B_N to $\overline{O}_{A=B}$	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	10.0	1.5	7.2	1.5	5.5	1.5	4.5	1.5	4.2	ns
Propagation Delay $\overline{I}_{A=B}$ to $\overline{O}_{A=B}$	t_{PLH}, t_{PHL}		1.5	9.0	1.5	6.0	1.5	4.6	1.5	4.1	1.5	3.8	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. This parameter is determined by device characterization but is not production tested.
8. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
12. See test circuit and wave forms.
13. Minimum limits are guaranteed but not tested on Propagation Delays.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

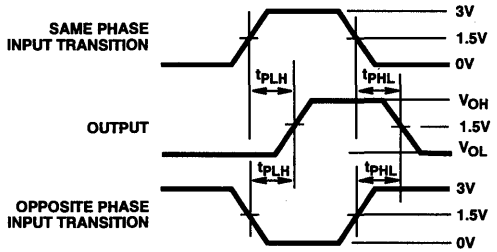


FIGURE 2. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT543T, CD74FCT544T, CD74FCT2543T

December 1996

Fast CMOS Latched Transceivers

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible With Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **25Ω Series Resistor on All Outputs (CD74FCT2543T)**
- **TTL Input and Output Levels**
- **Low Ground Bounce Outputs**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT543ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT543ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT543CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT543CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT543DTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT543DTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT543TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT543TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT544ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT544ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT544CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT544CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT544TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT544TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2543ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2543ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2543CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2543CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2543TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2543TQM	-40 to 85	24 Ld QSOP	M24.15-P

NOTE: QSOP is commonly known as SSOP.

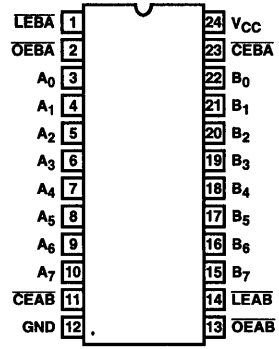
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

The devices are 8-bit wide non-inverting transceivers designed with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A_0-A_7 or to take data from B_0-B_7, as indicated in the Truth Table. With $\overline{CEAB}$ LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs. The CD74FCT543T is a non-inverting version of the CD74FCT544T.

Pinout

CD74FCT543T, CD74FCT544T, CD74FCT2543T
(QSOP, SOIC)
TOP VIEW



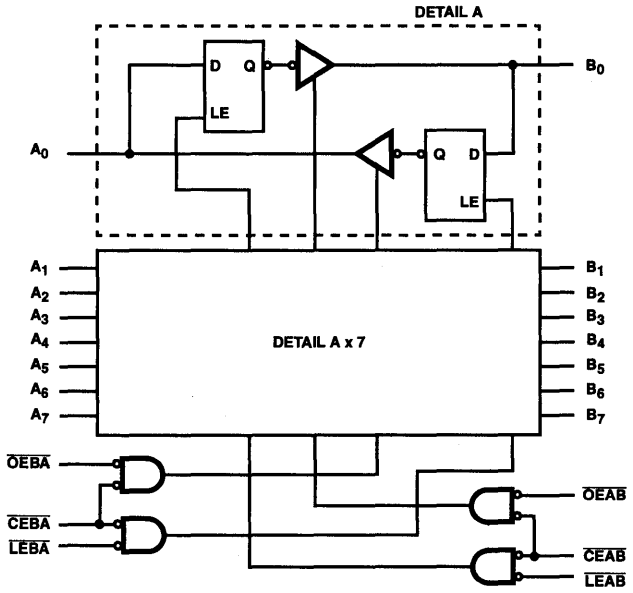
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **4173.1**

Functional Block Diagram

CD74FCT543T, CD74FCT2543T



TRUTH TABLE (NON-INVERTING)
For A-to-B (Symmetric with B-to-A) (NOTES 1, 2)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-TO-B	B_0-B_7
H	-	-	Storing	High-Z
-	H	-	Storing	-
-	-	H	-	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs (Note 3)

NOTES:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   - = Don't Care or Irrelevant
2. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.
3. Before $\overline{LEAB}$ LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0-A_7	A-to-B Data Inputs or B-to-A Three-State Outputs
B_0-B_7	B-to-A Data Inputs or A-to-B Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
SOIC Package 75
QSOP Package 100
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω Only)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max (Except I/O Pins)	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max (Except I/O Pins)	V_{IN} = GND	-	-	-1	µA
Input HIGH Current	I_{IH}	(I/O Pins Only) V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	(I/O Pins Only) V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Ouput Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V			1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V			-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Curretn per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 9)	-	0.5	2.0	mA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
Supply Current per Input per MHz (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz (LEAB) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} f_i = 5MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	1.5	3.5 (Note 11)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.5 (Note 11)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz (LEAB) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} Eight Bits Toggling f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.8	7.3 (Note 11)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.0	16.3 (Note 11)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 13) TEST CONDITIONS	T (NOTE 14) MIN	T MAX	AT (NOTE 14) MIN	AT MAX	CT (NOTE 14) MIN	CT MAX	DT (NOTE 14) MIN	DT MAX	UNITS
CD74FCT543T											
Propagation Delay Transparent Mode A_N to B_N or B_N to A_N	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	ns
Propagation Delay $\overline{LEBA}$ to A_N, $\overline{LEAB}$ to B_N	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	ns
Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N	t_{PZH}, t_{PZL}	C_L = 50 pF R_L = 500Ω	2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	ns
Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N (Note 15)	t_{PZH}, t_{PZL}	C_L = 50 pF R_L = 500Ω	2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	ns
Setup Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$	t_{SU}	C_L = 50 pF R_L = 500Ω	3.0	-	2.0	-	2.0	-	1.5	-	ns
Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$	t_H	C_L = 50 pF R_L = 500Ω	2.0	-	2.0	-	2.0	-	1.5	-	ns
$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW (Note 15)	t_W	C_L = 50 pF R_L = 500Ω	5.0	-	5.0	-	5.0	-	3.0	-	ns
CD74FCT544T, CD74FCT2543T											
Propagation Delay Transparent Mode A_N to B_N or B_N to A_N	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	-	-	ns
Propagation Delay $\overline{LEBA}$ to A_N, $\overline{LEAB}$ to B_N	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	2.5	12.5	2.5	8.0	2.5	7.0	-	-	ns

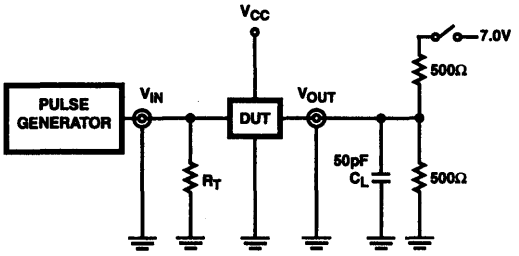
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 13) TEST CONDITIONS	T (NOTE 14) MIN	T MAX	AT (NOTE 14) MIN	AT MAX	CT (NOTE 14) MIN	CT MAX	DT (NOTE 14) MIN	DT MAX	UNITS
Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to An or Bn $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N	t_{PZH}, t_{PZL}	C_L = 50 pF R_L = 500Ω	2.0	12.0	2.0	9.0	2.0	8.0	-	-	ns
Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_N or B_N $\overline{CEBA}$ or $\overline{CEAB}$ to A_N or B_N (Note 15)	t_{PZH}, t_{PZL}	C_L = 50 pF R_L = 500Ω	2.0	9.0	2.0	7.5	2.0	6.5	-	-	ns
Setup Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$	t_{SU}	C_L = 50 pF R_L = 500Ω	3.0	-	2.0	-	2.0	-	-	-	ns
Hold Time, HIGH or LOW An or Bn to $\overline{LEBA}$ or $\overline{LEAB}$	t_H	C_L = 50 pF R_L = 500Ω	2.0	-	2.0	-	2.0	-	-	-	ns
$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW (Note 15)	t_W	C_L = 50 pF R_L = 500Ω	5.0	-	5.0	-	5.0	-	-	-	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
13. See test circuit and wave forms.
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

16. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

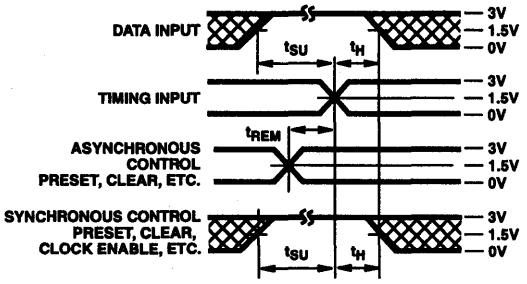


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

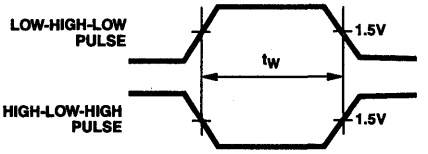


FIGURE 3. PULSE WIDTH

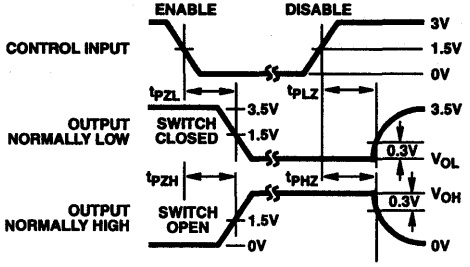


FIGURE 4. ENABLE AND DISABLE TIMING

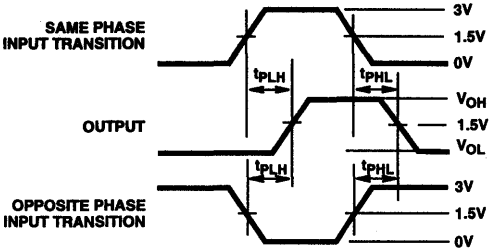


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT623T

December 1996

Fast CMOS Octal Bus Transceiver (Three-State)

Features

- **Advanced 0.8 micron CMOS Technology**
- **CD74FCT623T is Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **TTL Input and Output Levels**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Description

The CD74FCT623T is an 8-bit wide non-inverting octal transceiver designed with three-state bus-driving outputs in both the send and receive directions. Designed for asynchronous two-way operation between data buses, the control function allows for maximum flexibility in timing.

Ordering Information

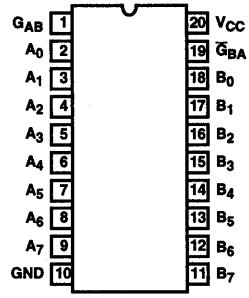
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT623TM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT623ATM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT623CTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT623DTM	-40 to 85	20 Ld SOIC	M20.3-P
CD74FCT623TQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT623ATQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT623CTQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74FCT623DTQM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74FCT623T
(QSOP, SOIC)
TOP VIEW

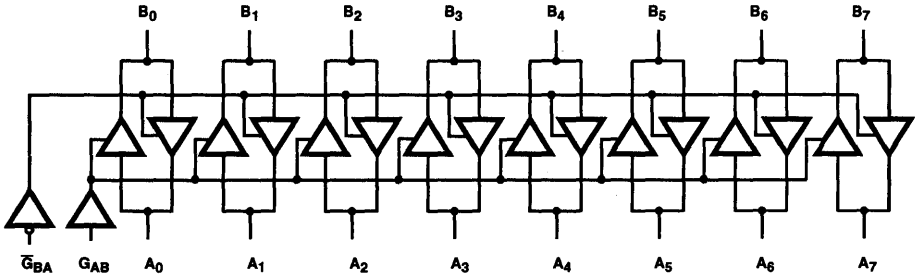


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **4174.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$\overline{G}_{BA}$	G_{AB}	
L	L	B Data to A Bus
H	H	A Data to B Bus
H	L	Z
L	H	B Data to A Bus A Data to B Bus

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance (OFF) State

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{G}_{BA}$, G_{AB}	Enable Outputs
A_0-A_7	A Bus Inputs or Three-State Outputs
B_0-B_7	B Bus Inputs or Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	87
QSOP Package	110

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}		V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max(Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.5	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{G}_{BA}$ = G_{AB} = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{G}_{BA} = G_{AB}$ = GND, 50% Duty Cycle One Bit Toggling at f_I = 5MHz	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.7	4.0 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.0 (Note 9)	mA
		V_{CC} = Max, Outputs Open fcp = 10MHz, 50% Duty Cycle $\overline{G}_{BA} = G_{AB}$ = GND, 50% Duty Cycle, Eight Bits Toggling at f_I = 2.5MHz, 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.2	6.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	5.2	14.5 (Note 9)	mA

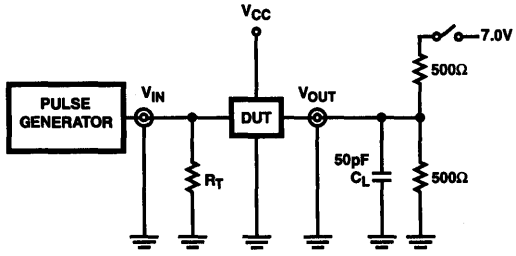
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T (NOTE 12) MIN	T MAX	AT (NOTE 12) MIN	AT MAX	CT (NOTE 12) MIN	CT MAX	DT (NOTE 12) MIN	DT MAX	UNITS
CD74FCT138T											
Propagation Delay A_N to B_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	7.5	1.5	5.5	1.5	4.8	1.5	3.8	ns
Propagation Delay B_N to A_N	t_{PLH}, t_{PHL}		1.5	7.5	1.5	5.5	1.5	4.8	1.5	3.8	ns
Output Enable Time $\overline{G}_{BA}$ to A_N	t_{PZH}, t_{PZL}		1.5	9.0	1.5	7.0	1.5	6.1	1.5	5.0	ns
Output Disable Time $\overline{G}_{BA}$ to A_N (Note 13)	t_{PHZ}, t_{PLZ}		1.5	8.0	1.5	6.5	1.5	5.6	1.5	4.3	ns
Output Enable Time G_{AB} to B_N	t_{PZH}, t_{PZL}		1.5	9.0	1.5	7.0	1.5	6.1	1.5	5.0	ns
Output Disable Time G_{AB} to B_N (Note 13)	t_{PHZ}, t_{PLZ}		1.5	8.0	1.5	6.5	1.5	5.6	1.5	4.3	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (Vin = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

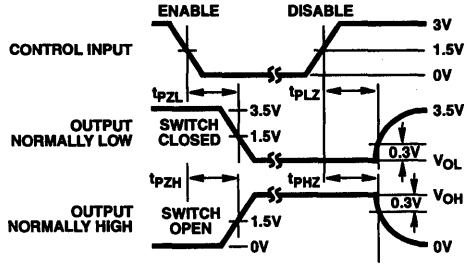


FIGURE 2. ENABLE AND DISABLE TIMING

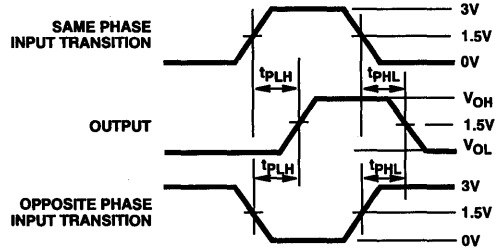


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT646T, CD74FCT648T, CD74FCT651T, CD74FCT652T, CD74FCT2646T, CD74FCT2652T

December 1996

Fast CMOS Octal Registered Transceivers

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed, Lower Power Consumption
- 25Ω Series Resistor on All Outputs (FCT2XXX Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs
- Extremely Low Static Power
- Hysteresis on All Inputs

Description

These devices are designed with a bus transceiver with three-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. The CD74FCT651T, CD74FCT652T and CD74FCT2652T utilize GAB and $\overline{GBA}$ signals to control the transceiver functions. The CD74FCT646T, CD74FCT2646T and CD74FCT648T utilize the enable control ($\overline{G}$) and direction pins (DIR) to control the transceiver functions. SAB and SBA control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The CD74FCT646T is a non-inverting option of the CD74FCT648T. The CD74FCT652T is a non-inverting option of the CD74FCT651T.

The CD74FCT2646T and CD74FCT2652T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Ordering Information

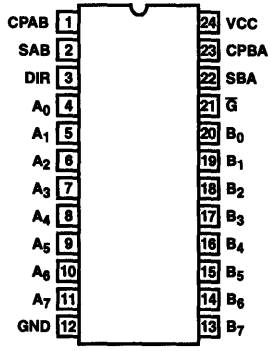
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT646ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT646ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT646CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT646CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT646DTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT646DTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT646TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT646TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT648ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT648ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT648CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT648CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT648TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT648TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT651ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT651ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT651CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT651CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT651TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT651TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT652ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT652ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT652CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT652CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT652DTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT652DTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT652TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT652TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2646ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2646ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2646TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2646TQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2652ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2652ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2652CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2652CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2652TM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2652TQM	-40 to 85	24 Ld QSOP	M24.15-P

NOTE: QSOP is commonly known as SSOP.

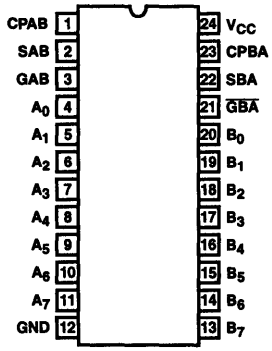
When ordering, use the entire part number. Add the suffix 96 to obtain the varient in the tape and reel.

Pinouts

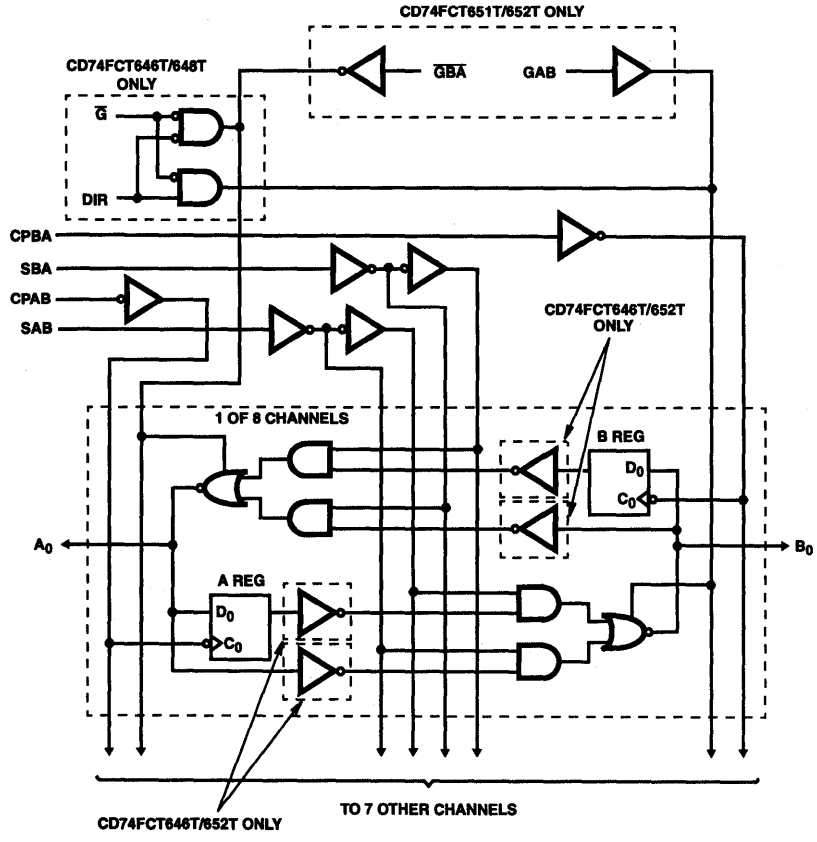
CD74FCT646T, CD74FCT648T, CD74FCT2646T
(QSOP, SOIC)
TOP VIEW



CD74FCT651T, CD74FCT652T, CD74FCT2652T
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram



CD74FCT646T, CD74FCT2646T, CD74FCT648T TRUTH TABLE

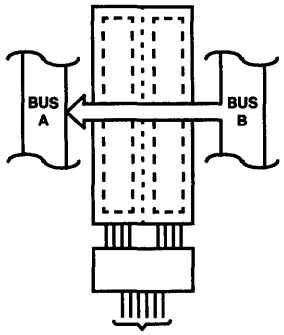
CD74FCT646T, CD74FCT2646T	CD74FCT648T	INPUTS						(NOTE 2) DATA I/O	
FUNCTION/OPERATION	FUNCTION/OPERATION	$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7
Isolation	Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	Store A and B Data	H	X	↑	↑	X	X	Input	Input
Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus	L	L	X	H or L	X	H	Output	Input
Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus	L	H	H or L	X	H	X	Input	Output

CD74FCT651T, CD74FCT652T, CD74FCT2652T TRUTH TABLE

CD74FCT651T	CD74FCT652T, CD74FCT2652T	INPUTS						(NOTE 2) DATA I/O	
FUNCTION/OPERATION	FUNCTION/OPERATION	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7
Isolation	Isolation	L	H	H or L	H or L	X	X	Input	Input
Store A and B Data	Store A and B Data	L	H	↑	↑	X	X	Input	Input
Store A, Hold B	Store A, Hold B	X	H	↑	H or L	X	X	Input	Unspecified (Note 1)
Store A in Both Registers (Note 3)	Store A in Both Registers	H	H	↑	↑	X (Note 2)	X	Input	Output
Hold A, Store B	Hold A, Store B	L	X	H or L	↑	X	X	Unspecified (Note 1)	Input
Store B in Both Registers (Note 4)	Store B in Both Registers	L	L	↑	↑	X	X (Note 2)	Output	Input
Real Time $\overline{B}$ Data to A Bus	Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus	L	L	X	H or L	X	H	Output	Input
Real Time $\overline{A}$ Data to B Bus	Real Time A Data to B Bus	H	H	X	X	L	X	Input	Output
Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus	H	H	H or L	X	H	X	Input	Output
Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

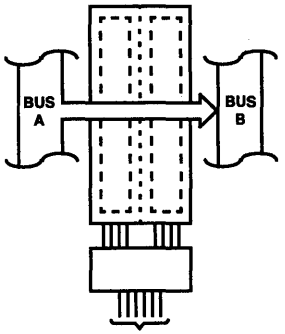
NOTES:

1. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = LOW-to-HIGH transition
3. $\overline{A}$ in B Register.
4. $\overline{B}$ in A Register.



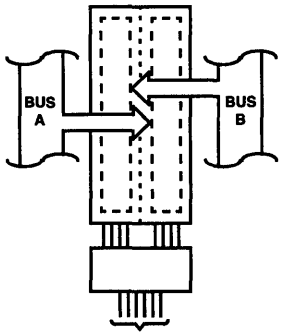
646T/648T/2646T	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L
651T/652T/2652T	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L

FIGURE 1. REAL-TIME TRANSFER BUS B TO A



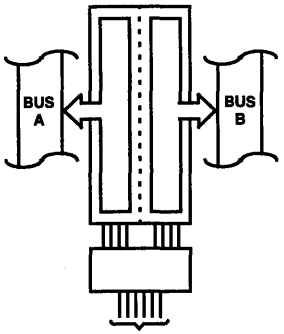
646T/648T/2646T	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X
651T/652T/2652T	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	H	X	X	L	X

FIGURE 2. REAL-TIME TRANSFER BUS A TO B



646T/648T/2646T	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X
651T/652T/2652T	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X

FIGURE 3. STORAGE FROM A AND/OR B



646T/648T/2646T (NOTE 5)	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	H or L	X	H
	H	L	H or L	X	H	X
651T/652T/2652T	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	L	H or L	H or L	H	H

FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

NOTE:

5. The CD74FCT646T and CD74FCT2646T cannot transfer data to A bus and B bus simultaneously.

Pin Descriptions

PIN NAME	DESCRIPTION
A_0-A_7	Data Register A Inputs Data Register B Outputs
B_0-B_7	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs (CD74FCT646T, CD74FCT648T, CD74FCT2646T)
GAB, $\overline{GBA}$	Output Enable Inputs (CD74FCT651T, CD74FCT652T, CD74FCT2652T)
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 6) θ_{JA} (°C/W)
SOIC Package 75
QSOP Package 100
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

6. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 7) TEST CONDITIONS		MIN	(NOTE 8) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.3	0.55	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω series)	-	0.3	0.55	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}, I_{OZL}	V_{CC} = Max	V_{OUT} = 2.7V			1	µA
			V_{OUT} = 0.5V			-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 9), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 11)	-	0.5	2	mA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 7) TEST CONDITIONS		MIN	(NOTE 8) TYP	MAX	UNITS
Supply Current per Input per MHz (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{G}$ or DIR = GND or GAB = $\overline{GBA}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	0.15	0.25	mA/MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{G}$ = DIR = GND or GAB = $\overline{GBA}$ = GND f_i = 5MHz One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	3.5 (Note 13)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.5 (Note 13)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{G}$ = DIR = GND or GAB = $\overline{GBA}$ = GND f_i = 2.5MHz, 50% Duty Cycle Eight Bits Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.8	7.3	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.0	16.3	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	T (NOTE 16) MIN	T MAX	AT (NOTE 16) MIN	AT MAX	(NOTE 18) CT (NOTE 16) MIN	CT MAX	(NOTE 18, 19) DT (NOTE 16) MIN	DT MAX	UNIT
CD74FCT646T, CD74FCT2646T, CD74FCT648T											
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	7.5	2.0	6.3	1.5	5.4	1.5	4.8	ns
Output Enable Time $\overline{G}$, DIR to Bus	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	2.0	14.0	2.0	9.8	1.5	7.8	1.5	7.3	ns
Output Disable Time $\overline{G}$, DIR to Bus (Note 17)	t_{PHZ}, t_{PLZ}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.3	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
Propagation Delay SBA or SAB to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H	C_L = 50pF R_L = 500Ω	2.0	-	1.5	-	1.5	-	1.5	-	ns
Clock Pulse Width HIGH or LOW (Note 17)	t_W	C_L = 50pF R_L = 500Ω	6.0	-	5.0	-	5.0	-	5.0	-	ns
CD74FCT651T, CD74FCT652T, CD74FCT2652T											
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.8	ns
Output Enable Time $\overline{GBA}$, GAB to Bus	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	2.0	12.5	2.0	9.8	1.5	7.8	1.5	7.3	ns

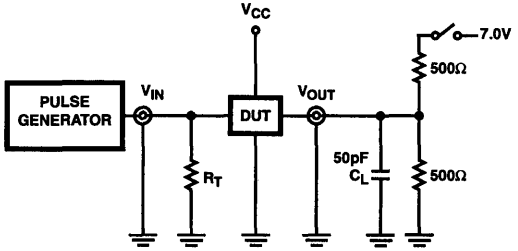
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	T (NOTE 16) MIN	T MAX	AT (NOTE 16) MIN	AT MAX	(NOTE 18) CT (NOTE 16) MIN	CT MAX	(NOTE 18, 19) DT (NOTE 16) MIN	DT MAX	UNIT
Output Disable Time $\overline{GBA}$, GAB to Bus• (Note 17)	t_{PHZ}, t_{PLZ}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	6.3	1.5	6.0	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.7	1.5	5.2	ns
Propagation Delay SBA or SAB to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.5	2.0	7.7	1.5	6.2	1.5	5.8	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H	C_L = 50pF R_L = 500Ω	2.0	-	1.5	-	1.5	-	1.5	-	ns
Clock Pulse Width HIGH or LOW (Note 17)	t_W	C_L = 50pF R_L = 500Ω	6.0	-	5.0	-	5.0	-	5.0	-	ns

NOTES:

7. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
8. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
9. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
15. See test circuit and wave forms.
16. Minimum limits are guaranteed but not tested on Propagation Delays.
17. This parameter is guaranteed but not production tested.
18. Not applicable to CD74FCT2646T, CD74FCT2652T.
19. Not applicable to CD74FCT648T.
20. Not applicable to CD74FCT651T or CD74FCT652T.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:
C_L = Load capacitance, includes jig and probe capacitance.
R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

21. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 5. TEST CIRCUIT

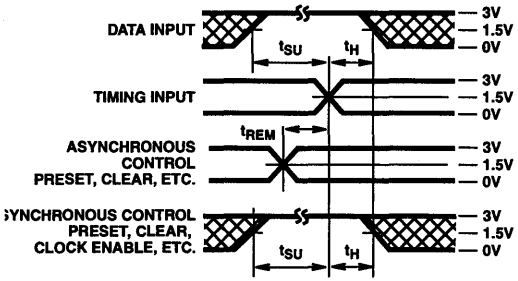


FIGURE 6. SETUP, HOLD, AND RELEASE TIMING

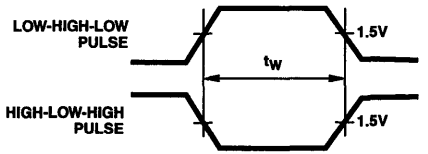


FIGURE 7. PULSE WIDTH

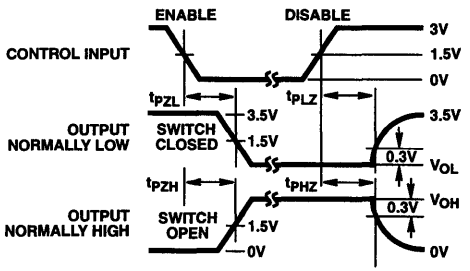


FIGURE 8. ENABLE AND DISABLE TIMING

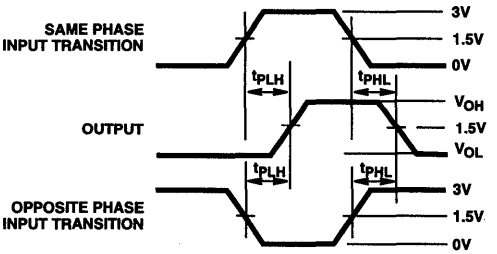


FIGURE 9. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT821T, CD74FCT823T, CD74FCT825T, CD74FCT2821T, CD74FCT2823T

December 1996

Fast CMOS Bus Interface Registers

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption**
- **25Ω Series Resistor on All Outputs (CD74FCT2821T, CD74FCT2823T Only)**
- **TTL Input and Output Levels**
- **Low Ground Bounce Outputs**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Description

The CD74FCT821T and CD74FCT2821T are 10-bit wide registers designed with ten D-type flip-flops with a buffered common clock and buffered three-state outputs. The CD74FCT823T and CD74FCT2823T are 9-bit wide registers designed with Clock Enable and Clear. The CD74FCT825T is an 8-bit wide register with all CD74FCT823T controls plus multiple enables. When output enable ($\overline{OE}$) is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

The CD74FCT2821T and CD74FCT2823T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT821ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT821ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT821BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT821BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT821CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT821CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT823ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT823ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT823BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT823BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT823CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT823CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT825ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT825ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT825BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT825BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT825CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT825CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2821ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2821ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2821BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2821BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2823ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2823ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2823BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2823BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2823CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2823CTQM	-40 to 85	24 Ld QSOP	M24.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

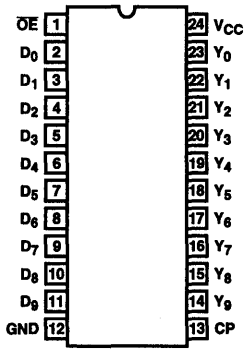
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

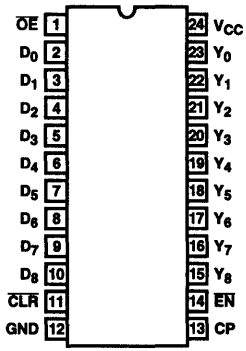
File Number **4176.2**

Pinouts

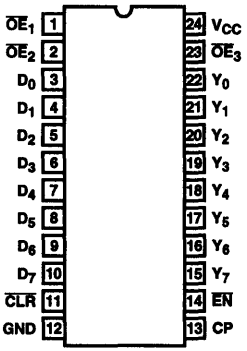
CD74FCT821T, CD74FCT2821T
(QSOP, SOIC)
TOP VIEW



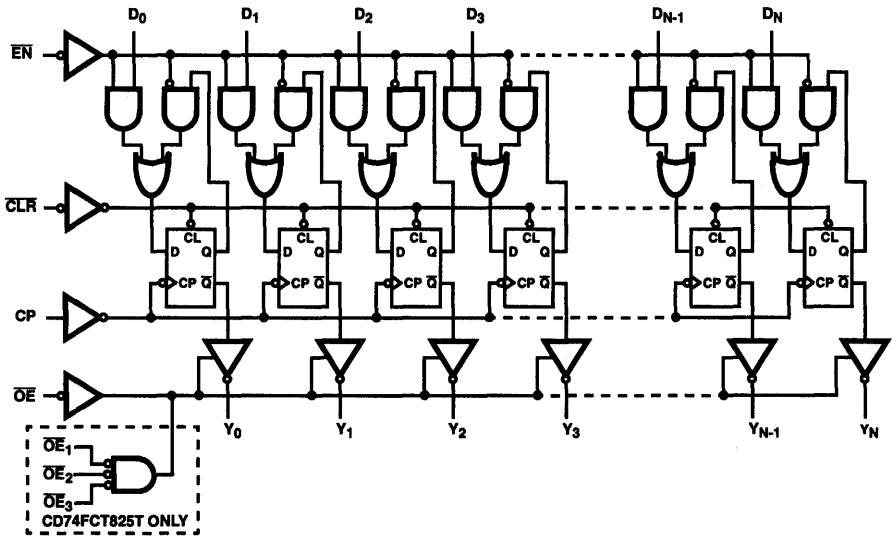
CD74FCT823, CD74FCT2823T
(QSOP, SOIC)
TOP VIEW



CD74FCT825T
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS					OUTPUTS	INTERNAL
	$\overline{CLR}$	$\overline{EN}$	$\overline{OE}$	CP	D_N	Y_N	Q_N
High-Z	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
Clear	L	X	H	X	X	Z	L
	L	X	L	X	X	L	L
Hold	H	H	H	X	X	Z	NC
	H	H	L	X	X	NC	NC
Load	H	L	H	↑	L	Z	L
	H	L	H	↑	H	Z	H
	H	L	L	↑	L	L	L
	H	L	L	↑	H	H	H

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   NC = No Change
   ↑ = LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW)
CP	Clock Pulse for the Register, Enters Data on LOW-to-HIGH Transition
D_N	Data Inputs
Y_N	Three-State Outputs
$\overline{CLR}$	Clear Input (Active LOW) (823/825/2823 Only)
$\overline{EN}$	Clock Enable Input (Active LOW)
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . $-40^{o}C$ to $85^{o}C$
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)
SOIC Package	75
QSOP Package	100

Maximum Junction Temperature . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^{o}C$ to $85^{o}C$, $V_{CC} = 5.0V \pm 5\%$							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 12mA (25Ω series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}, I_{OZL}	V_{CC} = Max	V_{OUT} = 2.7V			1	µA
			V_{OUT} = 0.5V			-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE $T_A = 25^{o}C$, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE} = \overline{EN}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	0.15	0.25	mA/ MHz

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND f_i = 5MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.5 (Note 9)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = $\overline{EN}$ = GND Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.8	7.3 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.0	16.3 (Note 9)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT (NOTE 12) MIN	AT MAX	BT (NOTE 12) MIN	BT MAX	CT (NOTE 14) (NOTE 12) MIN	CT MAX	UNIT
CD74FCT821T, CD74FCT2821T									
Propagation Delay CP to Y_N ($\overline{OE}$ = LOW)	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	ns
Setup Time HIGH or LOW, D_N to CP	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	3.0	-	3.0	-	ns
Hold Time HIGH or LOW, D_N to CP	t_H	C_L = 50pF R_L = 500Ω	2.0	-	1.5	-	1.5	-	ns
Setup Time HIGH or LOW, $\overline{EN}$ to CP	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	3.0	-	3.0	-	ns
Hold Time HIGH or LOW, $\overline{EN}$ to CP	t_H	C_L = 50pF R_L = 500Ω	2.0	-	0	-	0	-	ns
Propagation Delay $\overline{CLR}$ to Y_N	t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	14.0	1.5	9.0	1.5	8.0	ns
Recovery Time, $\overline{CLR}$ to CP (Note 13)	t_{REM}	C_L = 50pF R_L = 500Ω	6.0	-	6.0	-	6.0	-	ns
Clock Pulse Width HIGH or LOW (Note 13)	t_W	C_L = 50pF R_L = 500Ω	7.0	-	5.0	-	6.0	-	ns
$\overline{CLR}$ Pulse Width LOW (Note 13)	t_W	C_L = 50pF R_L = 500Ω	6.0	-	6.0	-	6.0	-	ns
Output Enable Time $\overline{OE}$ to Y_N	t_{PZH}	C_L = 50pF R_L = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	ns
	t_{PZL}	C_L = 300pF (Note 13) R_L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	ns
Output Disable Time $\overline{OE}$ to Y_N	t_{PHZ}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
	t_{PLZ}	C_L = 300pF (Note 13) R_L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	ns
CD74FCT823T, CD74FCT2823T, CD74FCT825T									
Propagation Delay CP to Y_N ($\overline{OE}$ = LOW)	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	ns

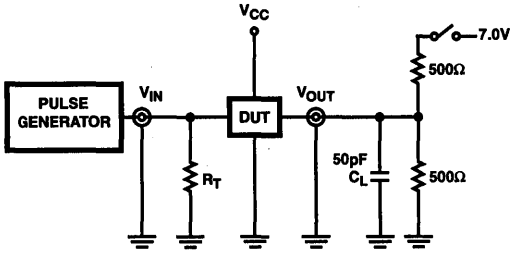
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT (NOTE 12) MIN	AT MAX	BT (NOTE 12) MIN	BT MAX	CT (NOTE 14) (NOTE 12) MIN	CT MAX	UNIT
Setup Time HIGH or LOW, D_N to CP	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	3.0	-	3.0	-	ns
Hold Time HIGH or LOW, D_N to CP	t_H	C_L = 50pF R_L = 500Ω	2.0	-	1.5	-	1.5	-	ns
Setup Time HIGH or LOW, $\overline{EN}$ to CP	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	3.0	-	3.0	-	ns
Hold Time HIGH or LOW, $\overline{EN}$ to CP	t_H	C_L = 50pF R_L = 500Ω	2.0	-	0	-	0	-	ns
Propagation Delay $\overline{CLR}$ to Y_N	t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	13.0	1.5	9.0	1.5	8.0	ns
Recovery Time, $\overline{CLR}$ to CP (Note 13)	t_{REM}	C_L = 50pF R_L = 500Ω	6.0	-	6.0	-	6.0	-	ns
Clock Pulse Width HIGH or LOW (Note 13)	t_W	C_L = 50pF R_L = 500Ω	7.0	-	5.0	-	6.0	-	ns
$\overline{CLR}$ Pulse Width LOW (Note 13)	t_W	C_L = 50pF R_L = 500Ω	6.0	-	6.0	-	6.0	-	ns
Output Enable Time $\overline{OE}$ to Y_N	t_{PZH}	C_L = 50pF R_L = 500Ω	1.5	11.5	1.5	8.0	1.5	7.0	ns
	t_{PZL}	C_L = 300pF (Note 13) R_L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	ns
Output Disable Time $\overline{OE}$ to Y_N	t_{PHZ}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
	t_{PLZ}	C_L = 300pF (Note 13) R_L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (Vin = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.
14. The CD74FCT2821CT type is not available.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

15. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

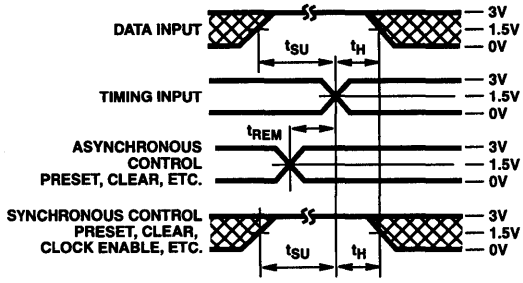


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

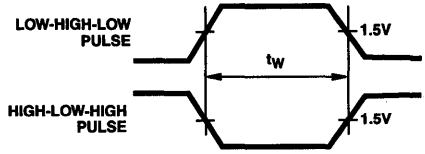


FIGURE 3. PULSE WIDTH

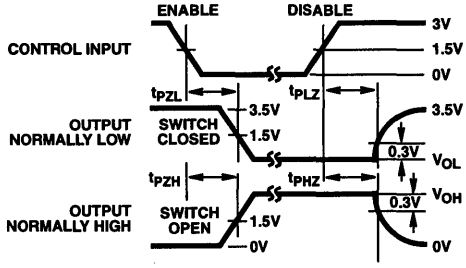


FIGURE 4. ENABLE AND DISABLE TIMING

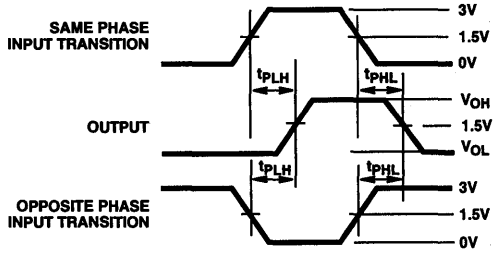


FIGURE 5. PROPAGATION DELAY

CD74FCT827T, CD74FCT828T, CD74FCT2827T, CD74FCT2828T

December 1996

Fast CMOS 10-Bit Buffers

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed And Lower Power Consumption**
- **25Ω Series Resistor on All Outputs (CD74FCT2827T, CD74FCT2828T Only)**
- **TTL Input and Output Levels**
- **Low Ground Bounce Outputs**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT827ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT827ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT827BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT827BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT827CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT827CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT828ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT828ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT828BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT828BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT828CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT828CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2827ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2827ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2827BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2827BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2828ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2828ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2828BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2828BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2828CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2828CTQM	-40 to 85	24 Ld QSOP	M24.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

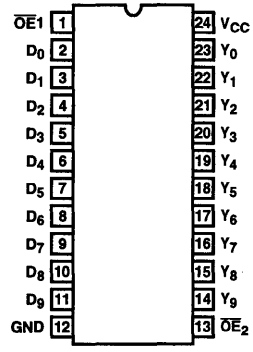
Description

These devices are 10-bit wide bus drivers providing high-performance bus interface buffering for wide address/data paths or buses carrying parity. The 10-bit buffers have NAND-ed output enables for maximum control flexibility. They are designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. The CD74FCT827T and CD74FCT2827T are non-inverting versions of the CD74FCT828T and CD74FCT2828T.

All CD74FCT2827T and CD74FCT2828T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

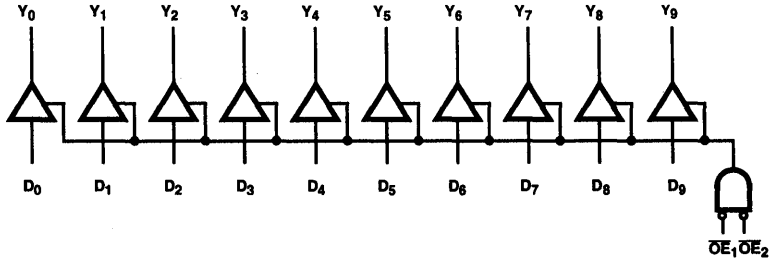
Pinout

CD74FCT827T, CD74FCT828T, CD74FCT2827T, CD74FCT2828T (QSOP, SOIC)
TOP VIEW



Functional Block Diagram

CD74FCT827T



TRUTH TABLE (NOTE 1)

FUNCTION	Inputs			Outputs
	$\overline{OE}_1$	$\overline{OE}_2$	D_N	Y_N
CD74FCT827T, CD74FCT2827T (Non-Inverting)				
Transparent	L	L	L	L
	L	L	H	H
Three-State	H	X	X	Z
	X	H	X	Z
CD74FCT828T, CD74FCT2828T (Inverting)				
Transparent	L	L	L	H
	L	L	H	L
Three-State	H	X	X	Z
	X	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OE}_N$	Output Enable Input (Active LOW)
D_0-D_9	10-Bit Data Inputs
Y_0-Y_9	10-Bit Data Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	75
QSOP Package	100

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω Series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}		V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.5	mA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}_1$ or $\overline{OE}_2$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}_1$ or $\overline{OE}_2$ = GND f_i = 5MHz One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.7	4.0 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.0 (Note 9)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}_1$ or $\overline{OE}_2$ = GND Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.2	6.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	5.2	14.5 (Note 9)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT		BT		(NOTE 14) CT		UNITS
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
CD74FCT827T, CD74FCT2827T									
Propagation Delay D_N to Y_N	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	1.5	6.5	1.5	5.0	1.5	4.4	ns
		C_L = 300 pF (Note 13) R_L = 500Ω	1.5	15.0	1.5	13.0	1.5	10.0	ns
Output Enable Time $\overline{OE}_N$ to Y_N	t_{PZH}, t_{PZL}	C_L = 50 pF R_L = 500Ω	1.5	9.5	1.5	8.0	1.5	7.0	ns
		C_L = 300 pF (Note 13) R_L = 500Ω	1.5	23.0	1.5	15.0	1.5	14.0	ns
Output Disable Time $\overline{OE}_N$ to Y_N (Note 13)	t_{PHZ}, t_{PLZ}	C_L = 5 pF (Note 13) R_L = 500Ω	1.5	8.5	1.5	6.0	1.5	5.7	ns
		C_L = 50 pF R_L = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	ns
CD74FCT828T, CD74FCT2828T									
Propagation Delay D_N to Y_N	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	1.5	6.5	1.5	5.5	1.5	4.4	ns
		C_L = 300 pF (Note 13) R_L = 500Ω	1.5	15.0	1.5	13.0	1.5	10.0	ns

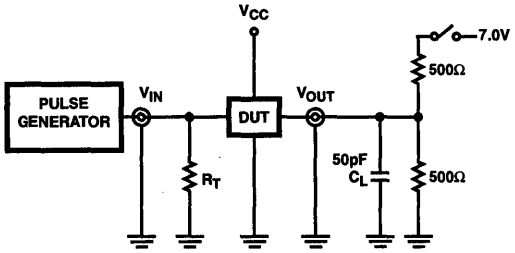
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT (NOTE 12) MIN	AT MAX	BT (NOTE 12) MIN	BT MAX	(NOTE 14) CT (NOTE 12) MIN	CT MAX	UNITS
Output Enable Time $\overline{OE}_N$ to Y_N	t_{PZH}, t_{PZL}	C_L = 50 pF, R_L = 500Ω	1.5	9.5	1.5	8.0	1.5	7.0	ns
		C_L = 300 pF (Note 13), R_L = 500Ω	1.5	23.0	1.5	15.0	1.5	14.0	ns
Output Disable Time $\overline{OE}_N$ to Y_N (Note 13)	t_{PHZ}, t_{PLZ}	C_L = 5 pF (Note 13), R_L = 500Ω	1.5	8.5	1.5	6.0	1.5	5.7	ns
		C_L = 50 pF, R_L = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.
14. All types except CD74FCT2827T.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

15. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

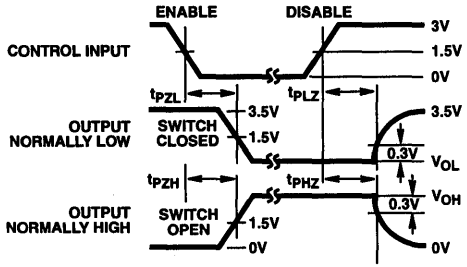


FIGURE 2. ENABLE AND DISABLE TIMING

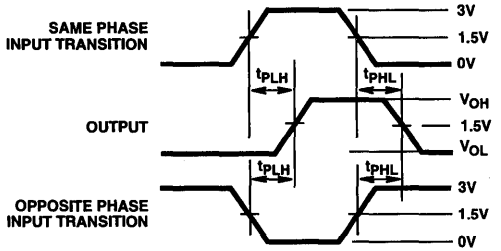


FIGURE 3. PROPAGATION DELAY

CD74FCT841T, CD74FCT843T, CD74FCT845T, CD74FCT2841T

December 1996

Fast CMOS Bus Interface Latches

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor on All Outputs (FCT2841 Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs
- Extremely Low Static Power
- Hysteresis on All Inputs

Description

These devices are buffered interface latches. These transparent latches with three-state outputs, are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state. The CD74FCT841T and CD74FCT2841T are 10-bit latches, the CD74FCT843T is a 9-bit latch, and the CD74FCT845T is an 8-bit latch.

The CD74FCT2841T device has a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

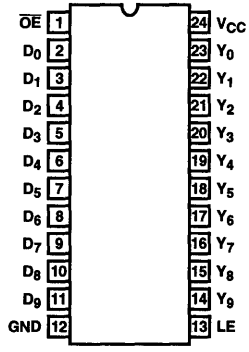
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT841ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT841ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT841BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT841BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT841CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT841CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT843ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT843ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT843BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT843BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT843CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT843CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT845ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT845ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT845BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT845BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT845CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT845CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2841ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2841ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2841BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2841BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT2841CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT2841CTQM	-40 to 85	24 Ld QSOP	M24.15-P

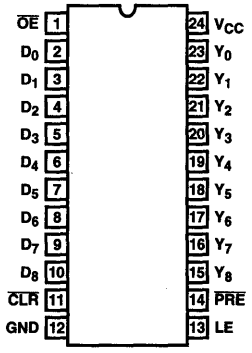
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinouts

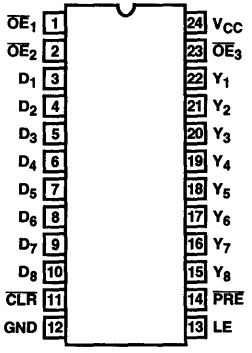
CD74FCT841T, CD74FCT2841T (QSOP, SOIC)
TOP VIEW



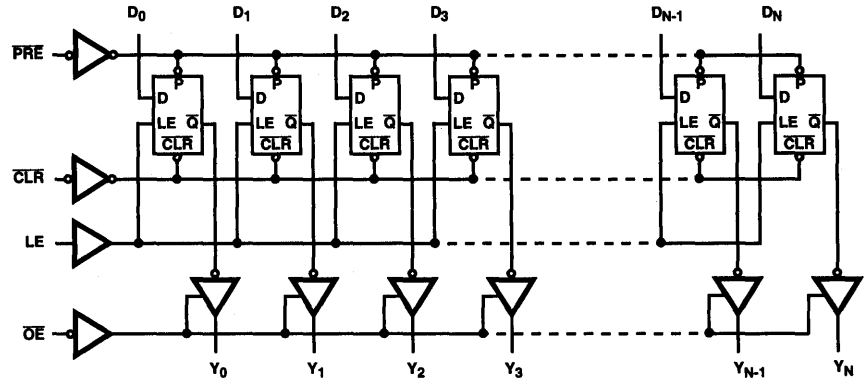
CD74FCT843T (QSOP, SOIC)
TOP VIEW



CD74FCT845T (QSOP, SOIC)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS					OUTPUTS	INTERNAL
	$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_N	Y_N	Q_N
High-Z	H	H	H	X	X	Z	X
	H	H	H	H	L	Z	L
	H	H	H	H	H	Z	H
Latched (High Z)	H	H	H	L	X	Z	NC
Transparent	H	H	L	H	L	L	L
	H	H	L	H	H	H	H
Latched	H	H	L	L	X	NC	NC
Preset	H	L	L	X	X	H	H
Clear	L	H	L	X	X	L	L
Preset	L	L	L	X	X	H	H
Latched (High Z)	L	H	H	L	X	Z	L
Latched (High Z)	H	L	H	L	X	Z	H

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   NC = No Change
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
Y_N	Three-State Latch Outputs
D_N	Latch Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Control
$\overline{CLR}$	Clear Latch
$\overline{PRE}$	Preset Latch High, Preset Overrides CLR
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	75
QSOP Package	100

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Current	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Output LOW Current	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω Series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = Vcc	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}		V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz(Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$ = GND; LE = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND; LE = V_{CC} f_i = 5MHz One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.8	4.5 (Note 9)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}$ = GND; LE = V_{CC} Eight Bits Toggling f_i = 2.5MHz, 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.0	6.0 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	5.0	14.0 (Note 9)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT (NOTE 12) MIN	AT MAX	BT (NOTE 12) MIN	BT MAX	CT (NOTE 12) MIN	CT MAX	UNITS
CD74FCT841T, CD74FCT2841T									
Propagation Delay D_N to Y_N (LE = HIGH)	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
Setup Time Data to LE	t_{SU}	C_L = 50pF R_L = 500Ω	2.5	-	2.5	-	2.5	-	ns
Hold Time Data to LE	t_H		2.5	-	2.5	-	2.5	-	ns
Propagation Delay LE to Y_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		C_L = 300pF (Note 13) R_L = 500Ω	-	16.0	-	15.5	-	15.0	ns
LE Pulse Width (HIGH)(Note 3)	t_W	C_L = 50pF R_L = 500Ω	4.0	-	4.0	-	4.0	-	ns
Output Enable Time $\overline{OE}$ to Y_N	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
Output Disable Time(Note 3) $\overline{OE}$ to Y_N	t_{PHZ}, t_{PLZ}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	6.0	1.5	5.7	ns
		C_L = 5 pF (Note 13) R_L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns
CD74FCT843T, CD74FCT845T									
Propagation Delay D_N to Y_N (LE = HIGH)	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
Setup Time Data to LE	t_{SU}	C_L = 50pF R_L = 500Ω	2.5	-	2.5	-	2.5	-	ns
Hold Time Data to LE	t_H		2.5	-	2.5	-	2.5	-	ns

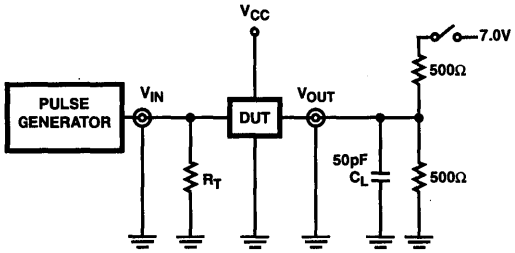
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT (NOTE 12) MIN	AT MAX	BT (NOTE 12) MIN	BT MAX	CT (NOTE 12) MIN	CT MAX	UNITS
Propagation Delay LE to Y_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0	ns
Propagation Delay $\overline{PRE}$ to Y_N	t_{PLH}	C_L = 50pF R_L = 500Ω	1.5	11.0	1.5	8.0	1.5	7.0	ns
Recovery Time $\overline{PRE}$ to Y_N	t_{REM}		1.5	11.0	1.5	10.0	1.5	9.0	ns
Propagation Delay $\overline{CLR}$ to Y_N	t_{PLH}		1.5	11.0	1.5	10.0	1.5	9.0	ns
Recovery Time(Note 13) $\overline{CLR}$ to Y_N	t_{REM}		1.5	13.0	1.5	10.0	1.5	9.0	ns
LE Pulse Width (Note 13) (HIGH)	t_W		4.0	-	4.0	-	4.0	-	ns
$\overline{PRE}$ Pulse Width (Note 13) (LOW)	t_W		5.0	-	4.0	-	4.0	-	ns
$\overline{CLR}$ Pulse Width (Note 13) (LOW)	t_W		4.0	-	4.0	-	4.0	-	ns
Output Enable Time $\overline{OE}$ to Y_N	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
Output Disable Time (Note 13) $\overline{OE}$ to Y_N	t_{PHZ}, t_{PLZ}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	6.5	1.5	5.7	ns
		C_L = 5pF (Note 13) R_L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

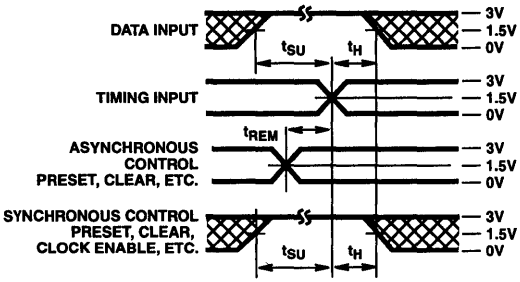


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

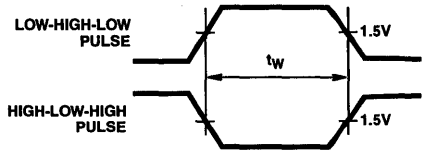


FIGURE 3. PULSE WIDTH

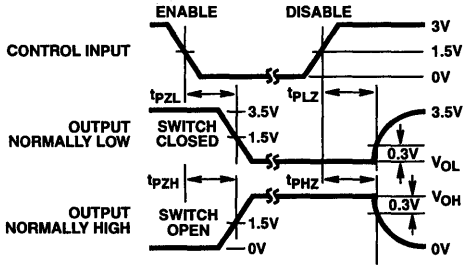


FIGURE 4. ENABLE AND DISABLE TIMING

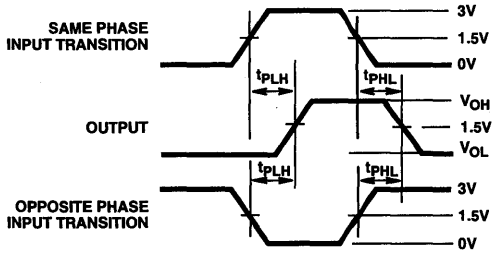


FIGURE 5. PROPAGATION DELAY

CD74FCT861T, CD74FCT863T, CD74FCT864T

December 1996

Fast CMOS Bus Transceivers

Features

- **Advanced 0.8 micron CMOS Technology**
- **These Devices are Pin Compatible With Bipolar FAST™ Series at a Higher Speed And Lower Power Consumption**
- **TTL Input and Output Levels**
- **Extremely Low Static Power**
- **Hysteresis on All Inputs**

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
CD74FCT861ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT861ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT861BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT861BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT861CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT861CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT863ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT863ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT863BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT863BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT863CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT863CTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT864ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT864ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT864BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT864BTQM	-40 to 85	24 Ld QSOP	M24.15-P
CD74FCT864CTM	-40 to 85	24 Ld SOIC	M24.3-P
CD74FCT864CTQM	-40 to 85	24 Ld QSOP	M24.15-P

NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

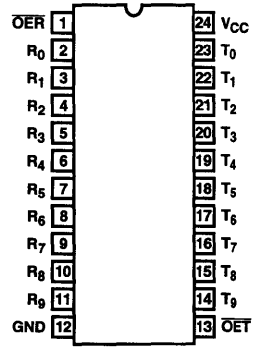
Description

The CD74FCT860T series bus transceivers provide high-performance bus interface buffering for wide data/address paths carrying parity. They are designed for high-capacitance load drive capability while providing bus loading at both inputs and outputs.

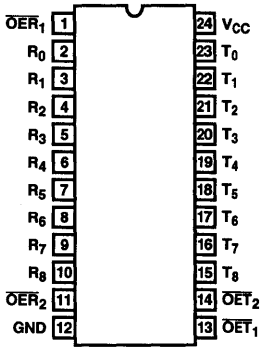
The CD74FCT861T is a 10-bit non-inverting bus transceiver. The CD74FCT863T is a 9-bit non-inverting option of the CD74FCT864T 9-bit inverting bus transceiver.

Pinouts

CD74FCT861T
(QSOP, SOIC)
TOP VIEW

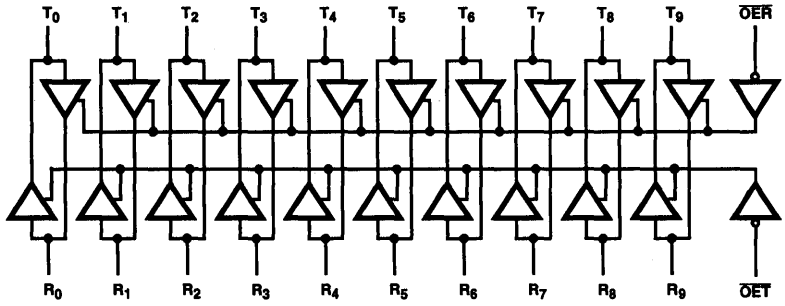


CD74FCT863T, CD74FCT864T
(QSOP, SOIC)
TOP VIEW



Functional Block Diagram

CD74FCT861T



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS				OUTPUTS	
	$\overline{OET}_N$	$\overline{OER}_N$	R_N	T_N	R_N	T_N
CD74FCT861T, CD74FCT863T (Non-Inverting)						
High-Z	H	H	X	X	Z	Z
Transmitting	L	H	L	N/A	N/A	L
Transmitting	L	H	H	N/A	N/A	H
Receiving	H	L	N/A	L	L	N/A
Receiving	H	L	N/A	H	H	N/A
CD74FCT864T (Inverting)						
High-Z	H	H	X	X	Z	Z
Transmitting	L	H	L	N/A	N/A	H
Transmitting	L	H	H	N/A	N/A	L
Receiving	H	L	N/A	L	H	N/A
Receiving	H	L	N/A	H	L	N/A

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   NA = Not Applicable
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
R_N	Receive Inputs/Outputs
T_N	Transmit Inputs/Outputs
$\overline{OER}_N$	Output Enable Receive Mode
$\overline{OET}_N$	Output Enable Transmit Mode
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
SOIC Package	75
QSOP Package	100

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}		V_{OUT} = 0.5V	-	-	-1	µA
Input HIGH Current	I_I	V_{CC} = Max, V_{IN} = V_{CC} (Max)		-	-	20	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$ = GND; LE = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND; LE = V_{CC} f_i = 5MHz One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	1.5	3.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.8	4.5 (Note 9)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND; LE = V_{CC} Eight Bits Toggling f_i = 2.5MHz 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.0	6.0 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	5.0	14.0 (Note 9)	mA

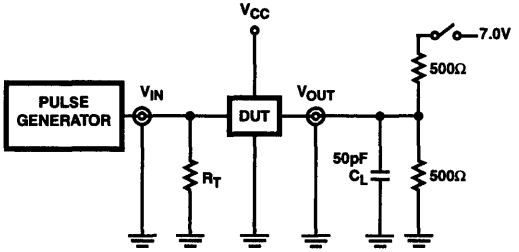
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT (NOTE 12) MIN	AT MAX	BT (NOTE 12) MIN	BT MAX	CT (NOTE 12) MIN	CT MAX	UNITS
Propagation Delay R_N to T_N or T_N to R_N	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	6.0	1.5	5.5	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	15.0	1.5	13.0	1.5	11.5	ns
Output Enable Time $\overline{OET}$ to T_N or $\overline{OER}$ to R_N	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.8	ns
		C_L = 300pF (Note 13) R_L = 500Ω	1.5	20.0	1.5	15.0	1.5	13.0	ns
Output Disable Time $\overline{OET}$ to T_N or $\overline{OER}$ to R_N (Note 13)	t_{PHZ}, t_{PLZ}	C_L = 5pF (Note 13) R_L = 500Ω	1.5	9.0	1.5	6.0	1.5	5.0	ns
		C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \leq 50\Omega$; t_f, $t_r \leq 2.5$ns.

FIGURE 1. TEST CIRCUIT

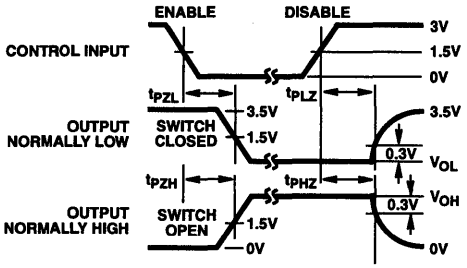


FIGURE 2. ENABLE AND DISABLE TIMING

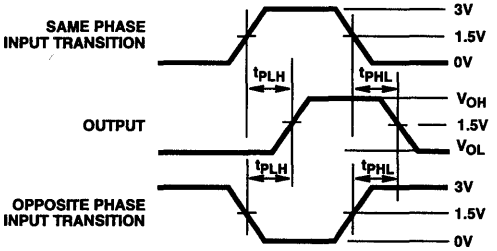


FIGURE 3. PROPAGATION DELAY

CMOS LOGIC 5

DOUBLE DENSITY 5V FCT CMOS LOGIC BALANCED AND HIGH DRIVE OUTPUT

		PAGE
Selection Guide		5-2
Data Sheets		
CD74FCT16240T, CD74FCT162240T	Fast CMOS 16-Bit Buffer/Line Drivers	5-3
CD74FCT16244T, CD74FCT162244T	Fast CMOS 16-Bit Buffer/Line Drivers	5-10
CD74FCT16245T, CD74FCT162245T	Fast CMOS 16-Bit Bidirectional Transceivers	5-17
CD74FCT16373T, CD74FCT162373T	Fast CMOS 16-Bit Transparent Latches	5-24
CD74FCT16374T, CD74FCT162374T	Fast CMOS 16-Bit Registers (Three-State)	5-31
CD74FCT16500T, CD74FCT162500T	Fast CMOS 18-Bit Registered Transceivers	5-38
CD74FCT16501T, CD74FCT162501T	Fast CMOS 18-Bit Registered Transceivers	5-44
CD74FCT16511T, CD74FCT162511T	Fast CMOS 16-Bit Registered/Latched Transceivers with Parity	5-51
CD74FCT16540T, CD74FCT162540T	Fast CMOS 16-Bit Buffer/Line Drivers	5-60
CD74FCT16541T, CD74FCT162541T	Fast CMOS 16-Bit Octal Buffer/Line Drivers	5-67
CD74FCT16543T, CD74FCT162543T	Fast CMOS 16-Bit Latched Transceivers	5-74
CD74FCT16646T, CD74FCT162646T	Fast CMOS 16-Bit Registered Transceivers	5-81
CD74FCT16652T, CD74FCT162652T	Fast CMOS 16-Bit Registered Transceivers	5-89
CD74FCT16823T, CD74FCT162823T	Fast CMOS 18-Bit Registers	5-96
CD74FCT16827T, CD74FCT162827T	Fast CMOS 20-Bit Buffers	5-103
CD74FCT16841T, CD74FCT162841T	Fast CMOS 20-Bit Transparent Latches	5-110
CD74FCT16952T, CD74FCT162952T	Fast CMOS 16-Bit Registered Transceivers	5-116

Selection Guide

DOUBLE DENSITY 5V FCT CMOS LOGIC BALANCED ANSCD HIGH DRIVE OUTPUT

PART NUMBER	DESCRIPTION	SPEED GRADE (X)						FILE#
		BLANK	A	B	C	D	E	
CD74FCT162240T	Fast CMOS 16-Bit Buffer/Line Driver	X	X	-	X	X	X	4180
CD74FCT162244T	Fast CMOS 16-Bit Buffer/Line Driver	X	X	-	X	X	X	4181
CD74FCT162245T	Fast CMOS 16-Bit Bidirectional Transceiver	X	X	-	X	X	X	4217
CD74FCT162373T	Fast CMOS 16-Bit Transparent Latches	X	X	-	X	X	X	4182
CD74FCT162374T	Fast CMOS 16-Bit Register (Three-State)	X	X	-	X	X	X	4183
CD74FCT16240T	Fast CMOS 16-Bit Buffer/Line Driver	X	X	-	X	X	X	4180
CD74FCT16244T	Fast CMOS 16-Bit Buffer/Line Driver	X	X	-	X	X	X	4181
CD74FCT16245T	Fast CMOS 16-Bit Bidirectional Transceiver	X	X	-	X	X	X	4217
CD74FCT162500T	Fast CMOS 18-Bit Registered Transceiver	-	X	-	X	X	-	4202
CD74FCT162501T	Fast CMOS 18-Bit Registered Transceiver	-	X	-	X	X	X	4184
CD74FCT162511T	Fast CMOS 16-Bit Registered/Latched Transceiver with Parity	X	X	-	-	-	-	4218
CD74FCT162540T	Fast CMOS 16-Bit Buffer/Line Driver	X	X	-	X			4185
CD74FCT162541T	Fast CMOS 16-Bit Octal Buffer/Line Driver	X	X	-	X	X	X	4186
CD74FCT162543T	Fast CMOS 16-Bit Latched Transceiver	X	X	-	X	X	X	4187
CD74FCT162646T	Fast CMOS 16-Bit Registered Transceiver	X	X	-	X	X	X	4188
CD74FCT162652T	Fast CMOS 16-Bit Registered Transceiver	X	X	-	X	X	X	4203
CD74FCT162823T	Fast CMOS 18-Bit Register	-	X	X	X	X	X	4189
CD74FCT162827T	Fast CMOS 20-Bit Buffer	-	X	X	X	X	X	4190
CD74FCT162841T	Fast CMOS 20-Bit Transparent Latch	-	X	X	X	X	X	4204
CD74FCT162952T	Fast CMOS 16-Bit Registered Transceiver	-	X	-	X	X	X	4191
CD74FCT16373T	Fast CMOS 16-Bit Transparent Latche	X	X	-	X	X	X	4182
CD74FCT16374T	Fast CMOS 16-Bit Registers (Three-State)	X	X	-	X	X	X	4183
CD74FCT16500T	Fast CMOS 18-Bit Registered Transceiver	-	X	-	X	X	-	4202
CD74FCT16501T	Fast CMOS 18-Bit Registered Transceiver	-	X	-	X	X	X	4184
CD74FCT16511T	Fast CMOS 16-Bit Registered/Latched Transceiver with Parity	X	X	-	-	-	-	4218
CD74FCT16540T	Fast CMOS 16-Bit Buffer/Line Driver	X	X	-	X	-	-	4185
CD74FCT16541T	Fast CMOS 16-Bit Octal Buffer/Line Driver	X	X	-	X	X	X	4186
CD74FCT16543T	Fast CMOS 16-Bit Latched Transceiver	X	X	-	X	X	X	4187
CD74FCT16646T	Fast CMOS 16-Bit Registered Transceiver	X	X	-	X	X	X	4188
CD74FCT16652T	Fast CMOS 16-Bit Registered Transceivers	X	X	-	X	X	-	4203
CD74FCT16823T	Fast CMOS 18-Bit Register	-	X	X	X	X	X	4189
CD74FCT16827T	Fast CMOS 20-Bit Buffer	-	X	X	X	X	X	4190
CD74FCT16841T	Fast CMOS 20-Bit Transparent Latch	-	X	X	X	X	X	4204
CD74FCT16952T	Fast CMOS 16-Bit Registered Transceiver	-	X	-	X	X	X	4191

HARRIS SEMICONDUCTOR

CD74FCT16240T, CD74FCT162240T

December 1996

Fast CMOS 16-Bit Buffer/Line Drivers

Features

- Advanced 0.6 micron CMOS Technology
- These Devices Are High-speed, Low Power Devices with High Current Drive
- V_{CC} = 5V ±10%
- Hysteresis on All Inputs
- CD74FCT16240T
  - High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA
  - Power Off Disable Outputs Permit "Live Insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- CD74FCT162240T
  - Balanced Output Drivers: ±24mA
  - Reduced System Switching Noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

Description

These devices are inverting 16-bit buffer/line drivers designed for applications driving high capacitance loads and low impedance backplanes. These high-speed, low power devices offer bus/backplane interface capability and a flow-through organization for ease of board layout. They are designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

The CD74FCT16240T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162240T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

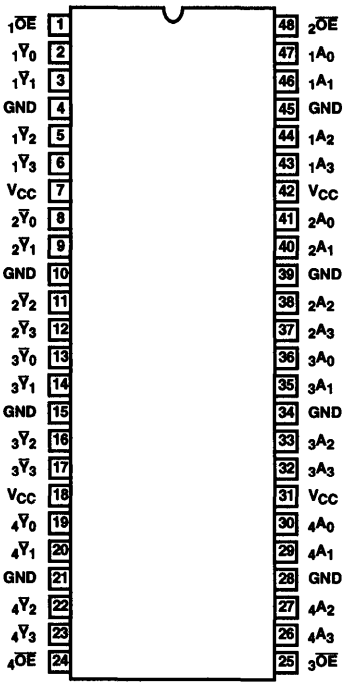
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16240ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16240ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16240CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16240CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16240DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16240DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16240ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16240ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16240TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16240TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162240ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162240ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162240CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162240CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162240DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162240DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162240ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162240ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162240TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162240TSM	-40 to 85	48 Ld SSOP	M48.300-P

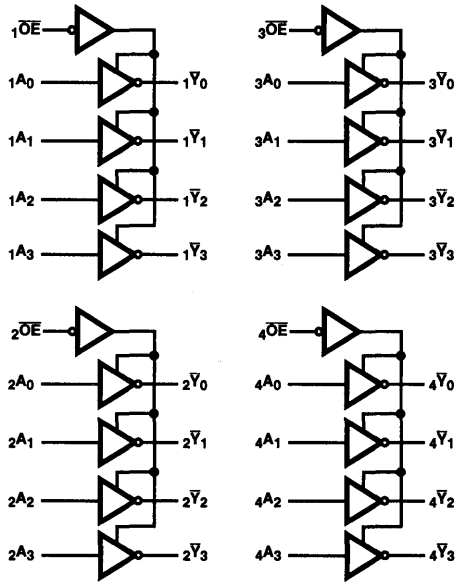
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74FCT16240T, CD74FCT162240T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
xOE	xA_x	xY_x
L	L	H
L	H	L
H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
xOE	Three-State Output Enable Inputs (Active LOW)
xA_x	Inputs
xY_x	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 8)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 5), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
CD74FCT16240T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq$ 4.5V		-	-	±100	µA
CD74FCT162240T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.6	1.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	0.9	2.3 (Note 12)	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	2.4	4.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.4	16.5 (Note 12)	mA

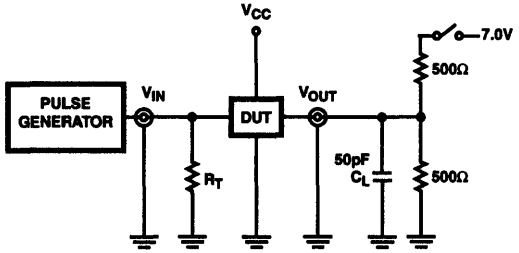
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T		AT		CT		DT		ET		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay xA_X to $x\overline{Y}_X$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	4.8	1.5	4.3	1.5	3.6	1.5	3.2	ns
Output Enable Time $x\overline{OE}$ to xA_X or $x\overline{Y}_X$	t_{PZH}, t_{PZL}		1.5	10.0	1.5	6.2	1.5	5.8	1.5	4.8	1.5	4.4	ns
Output Disable Time (Note 16) $x\overline{OE}$ to xA_X or $x\overline{Y}_X$	t_{PHZ}, t_{PLZ}		1.5	9.5	1.5	5.6	1.5	5.2	1.5	4.0	1.5	3.6	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading, except as noted.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. The test limit for this parameter is ±5μA at T_A = -55°C.
7. Pins with Bus Hold are identified in the pin description.
8. This specification does not apply to bi-directional functionalities with Bus Hold.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

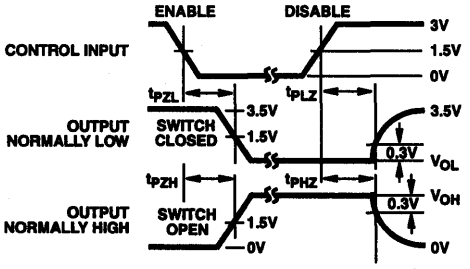


FIGURE 2. ENABLE AND DISABLE TIMING

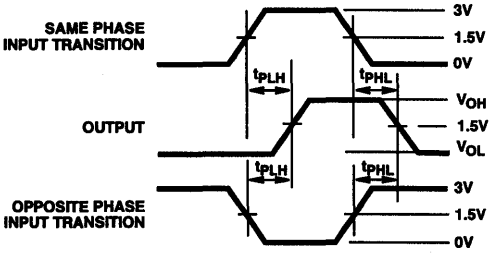


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16244T, CD74FCT162244T

December 1996

Fast CMOS 16-Bit Buffer/Line Drivers

Features

- **Advanced 0.6 micron CMOS Technology**
- **These Devices Are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16244T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162244T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**

Description

These devices are non-inverting 16-bit buffer/line drivers designed for applications driving high capacitance loads and low impedance backplanes. These high-speed, low power devices offer bus/backplane interface capability and a flow-through organization for ease of board layout. They are designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

The CD74FCT16244T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162244T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16244ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16244ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16244CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16244CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16244DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16244DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16244ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16244ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16244TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16244TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162244ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162244ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162244CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162244CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162244DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162244DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162244ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162244ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162244TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162244TSM	-40 to 85	48 Ld SSOP	M48.300-P

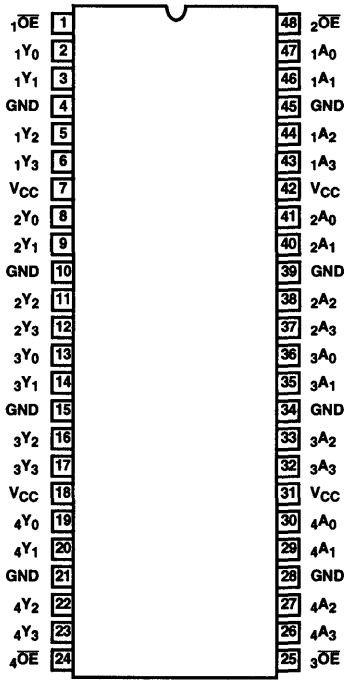
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

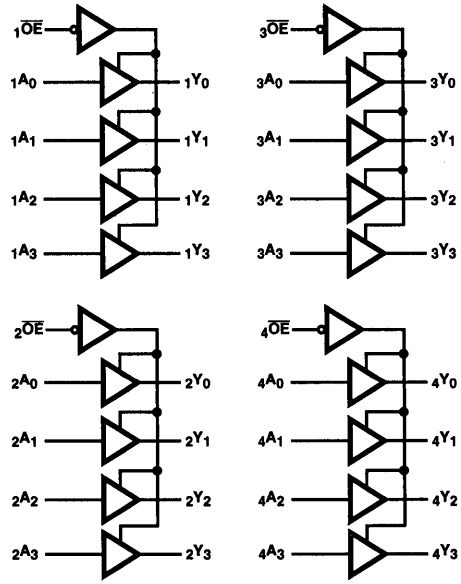
File Number **4181.1**

Pinout

CD74FCT16244T, CD74FCT162244T
(SSOP, TSSOP)



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$_{X}\overline{OE}$	$_{X}A_{X}$	$_{X}Y_{X}$
L	L	L
L	H	H
H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_{X}\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$_{X}A_{X}$	Inputs
$_{X}Y_{X}$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 8)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 5), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
CD74FCT16244T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq$ 4.5V		-	-	±100	µA
CD74FCT162244T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.6	1.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	0.9	2.3 (Note 12)	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	2.4	4.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.4	16.5 (Note 12)	mA

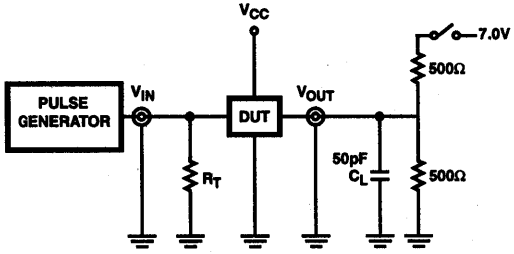
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T (NOTE 15) MIN	T MAX	AT (NOTE 15) MIN	AT MAX	CT (NOTE 15) MIN	CT MAX	DT (NOTE 15) MIN	DT MAX	ET (NOTE 15) MIN	ET MAX	UNITS
Propagation Delay $_xA_x$ to $_xY_x$	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	1.5	3.8	1.5	3.2	ns
Output Enable Time $_x\overline{OE}$ to $_xA_x$ or $_xY_x$	t_{PZH}, t_{PZL}		1.5	8.0	1.5	6.2	1.5	5.8	1.5	4.8	1.5	4.4	ns
Output Disable Time (Note 16) $_x\overline{OE}$ to $_xA_x$ or $_xY_x$	t_{PHZ}, t_{PLZ}		1.5	7.0	1.5	5.6	1.5	5.2	1.5	4.0	1.5	3.6	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading, except as noted.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. The test limit for this parameter is ±5μA at T_A = -55°C.
7. Pins with Bus Hold are identified in the pin description.
8. This specification does not apply to bi-directional functionalities with Bus Hold.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

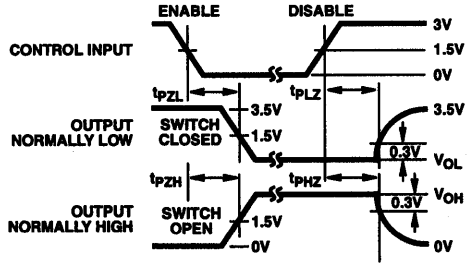


FIGURE 2. ENABLE AND DISABLE TIMING

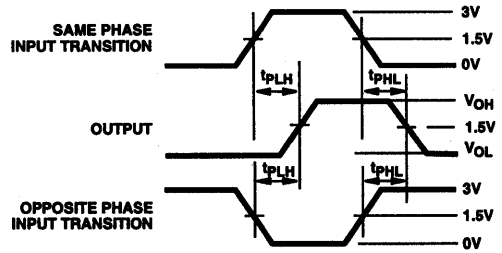


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16245T, CD74FCT162245T

December 1996

Fast CMOS 16-Bit Bidirectional Transceivers

Features

- **Advanced 0.6 micron CMOS Technology**
- **These Devices are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16245T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162245T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**

Description

These devices are 16-bit bidirectional transceivers designed for asynchronous two-way communication between data buses. The direction control input pin ($_X$DIR) determines the direction of data flow through the bidirectional transceiver. The Direction and Ouput Enable controls are designed to operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The output enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The CD74FCT16245T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers. The CD74FCT162245T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

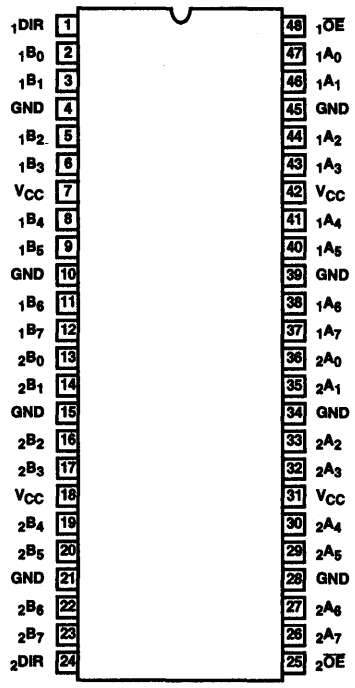
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16245ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16245ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16245CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16245CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16245DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16245DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16245ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16245ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16245TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16245TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162245ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162245ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162245CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162245CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162245DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162245DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162245ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162245ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162245TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162245TSM	-40 to 85	48 Ld SSOP	M48.300-P

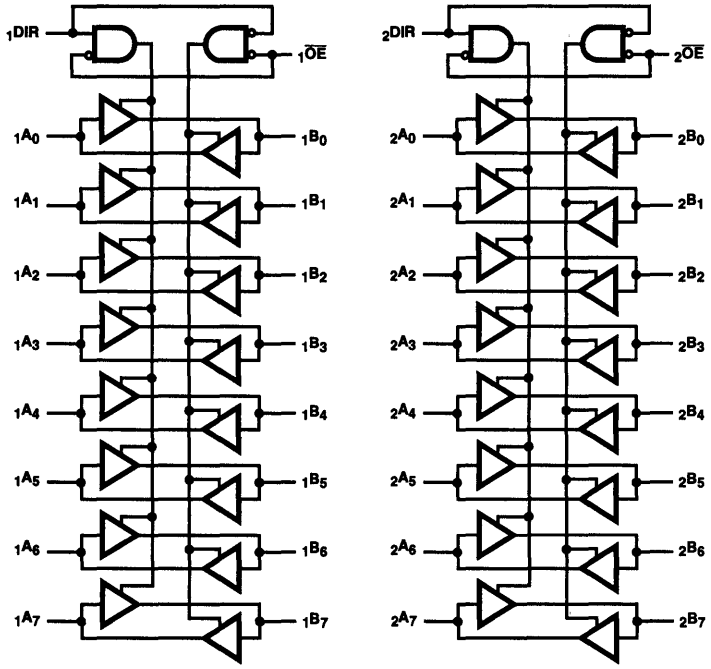
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74FCT16245T, CD74FCT162245T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$x\overline{OE}$	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$x\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
xDIR	Direction Control Input
xA_x	Side A Inputs or Three-State Outputs (Note 2)
xB_x	Side B Inputs or Three-State Outputs (Note 2)
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
TSSOP Package 94
SSOP Package 76
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 8)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 5), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
CD74FCT16245T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq$ 4.5V		-	-	±100	µA
CD74FCT162245T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = xDIR = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = xDIR = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.6	1.5 (Note 13)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	0.9	2.3 (Note 13)	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND 16 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	2.4	4.5 (Note 13)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.4	16.5 (Note 13)	mA

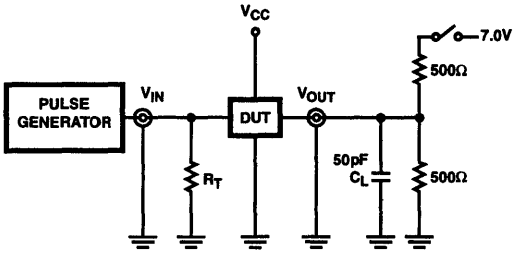
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T		AT		CT		DT		ET		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay A to B, B to A	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	1.5	3.8	1.5	3.2	ns
Output Enable Time $x\overline{OE}$ to A or B	t_{PZH}, t_{PZL}		1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.0	1.5	4.4	ns
Output Disable Time (Note 16) $x\overline{OE}$ to A or B	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	1.5	4.0	ns
Output Enable Time xDIR to A or B (Note 16)	t_{PZH}, t_{PZL}		1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.0	1.5	4.8	ns
Output Disable Time xDIR to A or B (Note 16)	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	1.5	4.0	ns
Output Skew(17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading, except as noted.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. The test limit for this parameter is ±5μA at T_A = -55°C.
7. Pins with Bus Hold are identified in the pin description.
8. This specification does not apply to bi-directional functionalities with Bus Hold.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \leq 50\Omega$; t_f, $t_r \leq 2.5$ns.

FIGURE 1. TEST CIRCUIT

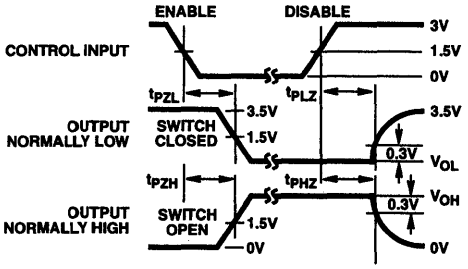


FIGURE 2. ENABLE AND DISABLE TIMING

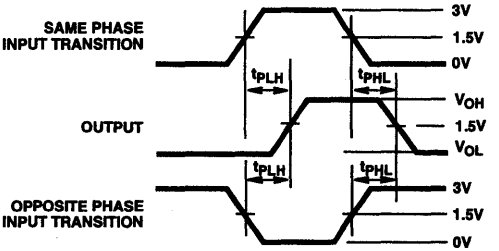


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16373T, CD74FCT162373T

December 1996

Fast CMOS 16-Bit Transparent Latches

Features

- **Advanced 0.6 micron CMOS Technology**
- **These Devices Are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16373T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162373T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**

Description

These devices are 16-bit transparent latches designed with three-state outputs and are intended for bus oriented applications. The Output Enable and Latch Enable controls are organized to operate as two 8-bit latches or one 16-bit latch. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

The CD74FCT16373T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162373T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16373ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16373ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16373CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16373CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16373DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16373DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16373ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16373ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16373TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16373TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162373ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162373ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162373CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162373CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162373DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162373DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162373ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162373ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162373TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162373TSM	-40 to 85	48 Ld SSOP	M48.300-P

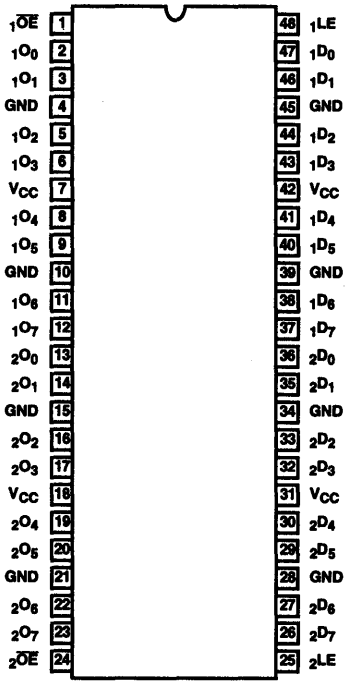
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

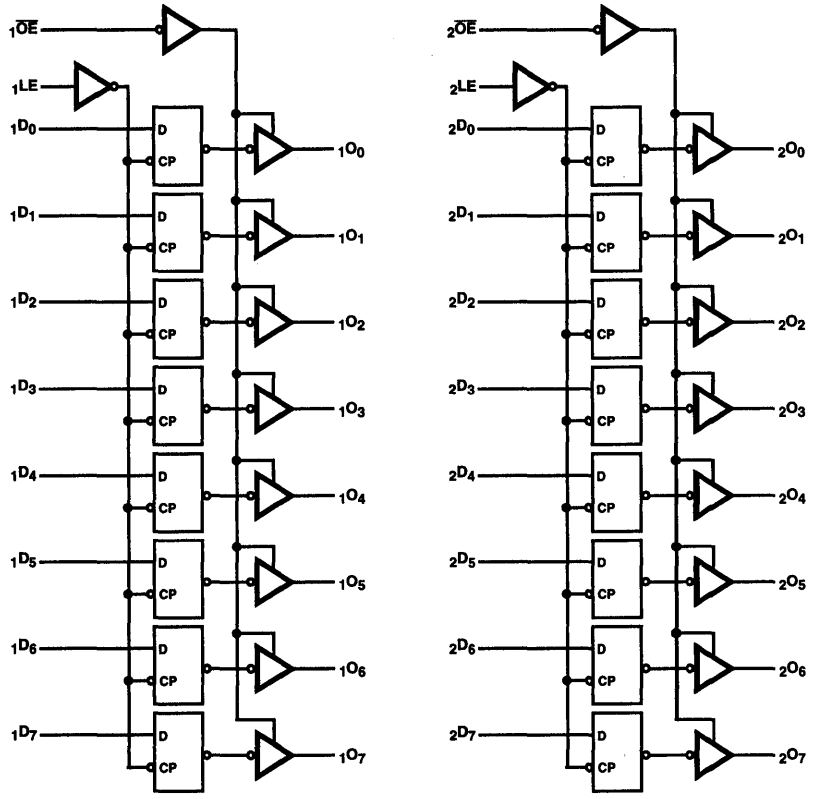
File Number **4182.1**

Pinout

CD74FCT16373T, CD74FCT162373T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$_xD_x$	$_x\overline{OE}$	$_xLE$	$_xO_x$
H	L	H	H
L	L	H	L
X	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_x\overline{OE}$	Output Enable Inputs (Active LOW)
$_xLE$	Latch Enable Inputs (Active HIGH)
$_xD_x$	Inputs
$_xO_x$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 8)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 5), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
CD74FCT16373T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq$ 4.5V		-	-	±100	µA
CD74FCT162373T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND, xLE = V_{CC} One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND, xLE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.6	1.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	0.9	2.3 (Note 12)	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND, xLE = V_{CC} 16 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	2.4	4.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.4	16.5 (Note 12)	mA

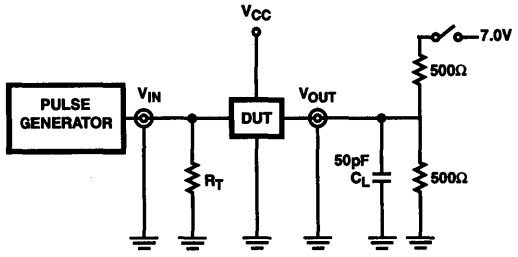
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T (NOTE 15) MIN	T MAX	AT (NOTE 15) MIN	AT MAX	CT (NOTE 15) MIN	CT MAX	DT (NOTE 15) MIN	DT MAX	ET (NOTE 15) MIN	ET MAX	UNITS
CD74FCT16373T, CD74FCT162373T													
Propagation Delay $_xD_X$ to $_xO_X$	t_{PLH}, t_{PHL}	C_L = 50 pF, R_L = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	1.5	3.4	ns
Propagation Delay $_xLE$ to $_xO_X$	t_{PLH}, t_{PHL}		2.0	13.0	2.0	8.5	2.0	5.5	1.5	4.0	1.5	3.7	ns
Output Enable Time $_x\overline{OE}$ to $_xO_X$	t_{PZH}, t_{PZL}		1.5	12.0	1.5	6.5	1.5	5.5	1.5	4.8	1.5	4.4	ns
Output Disable Time (Note 16) $x\overline{OE}$ to $_xO_X$	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.5	1.5	5.0	1.5	4.0	1.5	3.6	ns
Setup Time HIGH or LOW, $_xD_X$ to $_xLE$	t_{SU}		2.0	-	2.0	-	2.0	-	1.5	-	1.0	-	ns
Hold Time HIGH or LOW, $_xD_X$ to $_xLE$	t_H	C_L = 50 pF, R_L = 500Ω	1.5	-	1.5	-	1.5	-	1.0	-	1.0	-	ns
$_xLE$ Pulse Width HIGH (Note 16)	t_W		6.0	-	5.0	-	5.0	-	3.0	-	3.0	-	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading, except as noted.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. The test limit for this parameter is ±5μA at T_A = -55°C.
7. Pins with Bus Hold are identified in the pin description.
8. This specification does not apply to bi-directional functionalities with Bus Hold.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

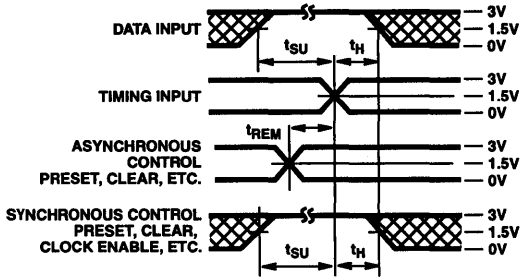


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

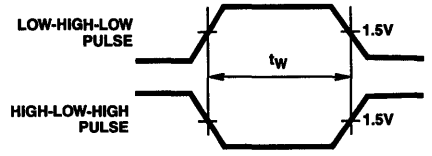


FIGURE 3. PULSE WIDTH

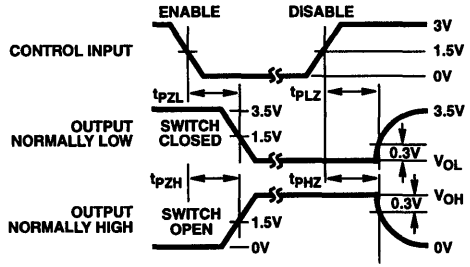


FIGURE 4. ENABLE AND DISABLE TIMING

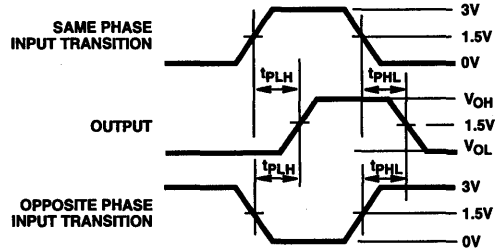


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16374T, CD74FCT162374T

December 1996

Fast CMOS 16-Bit Registers (Three-State)

Features

- Advanced 0.6 micron CMOS Technology
- These Devices are High-speed, Low Power Devices with High Current Drive
- V_{CC} = 5V ±10%
- Hysteresis on All Inputs
- CD74FCT16374T
  - High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA
  - Power Off Disable Outputs Permit "Live Insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- CD74FCT162374T
  - Balanced Output Drivers: ±24mA
  - Reduced System Switching Noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

Description

These Devices are 16-bit octal registers designed with 16 D-type flip-flops with a buffered common clock and three-state outputs. The Output Enable ($_X\overline{OE}$) and clock ($_X$CLK) controls are organized to operate as two 8-bit registers or one 16-bit register. When $\overline{OE}$ is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

The CD74FCT16374T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162374T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

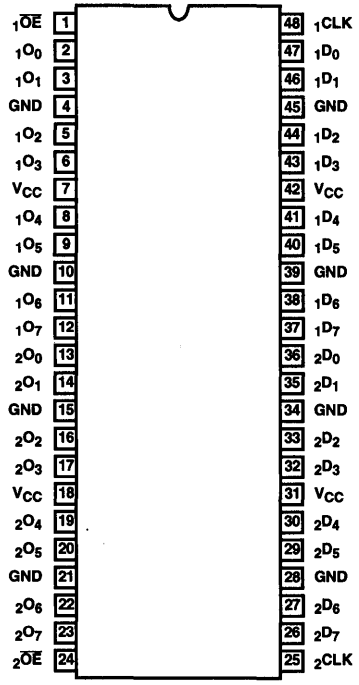
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16374ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16374ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16374CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16374CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16374DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16374DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16374ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16374ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16374TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16374TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162374ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162374ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162374CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162374CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162374DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162374DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162374ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162374ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162374TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162374TSM	-40 to 85	48 Ld SSOP	M48.300-P

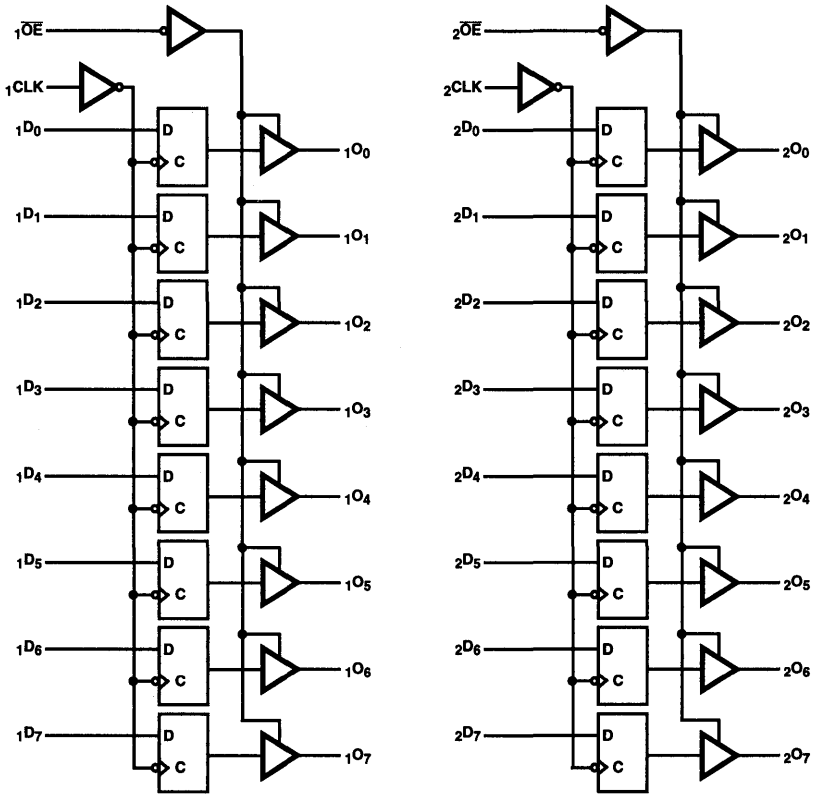
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74FCT16374T, CD74FCT162374T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS			OUTPUTS
	$_xD_x$	$_xCLK$	$_x\overline{OE}$	$_xO_x$
High-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$_x\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$_xCLK$	Clock Inputs
$_xD_x$	Inputs
$_xO_x$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 8)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 5), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
CD74FCT16374T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤ 4.5V		-	-	±100	µA
CD74FCT162374T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 11)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND f_i = 5MHz, 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.6	1.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.1	3.0 (Note 12)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.0	5.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	7.5	19.0 (Note 12)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T (NOTE 15) MIN	T MAX	AT (NOTE 15) MIN	AT MAX	CT (NOTE 15) MIN	CT MAX	DT (NOTE 15) MIN	DT MAX	ET (NOTE 15) MIN	ET MAX	UNITS
CD74FCT16374T, CD74FCT162374T													
Propagation Delay xCLK$_x$ to xO$_x$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	6.5	2.0	5.2	2.0	4.2	1.5	3.7	ns
Output Enable Time $x\overline{OE}$ to xO$_x$	t_{PZH}, t_{PZL}		1.5	12.5	1.5	6.5	1.5	5.5	1.5	4.8	1.5	4.4	ns
Output Disable Time (Note 16) $x\overline{OE}$ to xO$_x$	t_{PHZ}, t_{PLZ}		1.5	8.0	1.5	5.5	1.5	5.0	1.5	4.0	1.5	3.6	ns
Setup Time HIGH or LOW, xD$_x$ to xCLK	t_{SU}		2.0	-	2.0	-	2.0	-	2.0	-	1.5	-	ns

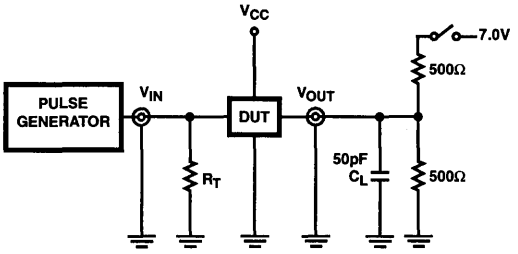
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T		AT		CT		DT		ET		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Hold Time HIGH or LOW, $_XD_X$ to $_X$CLK	t_H	C_L = 50pF, R_L = 500Ω	1.5	-	1.5	-	1.5	-	1.0	-	0.0	-	ns
$_X$CLK Pulse Width HIGH or LOW (Note 16)	t_W		7.0	-	5.0	-	5.0	-	3.0	-	3.0	-	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading, except as noted.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. The test limit for this parameter is ±5μA at T_A = -55°C.
7. Pins with Bus Hold are identified in the pin description.
8. This specification does not apply to bi-directional functionalities with Bus Hold.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

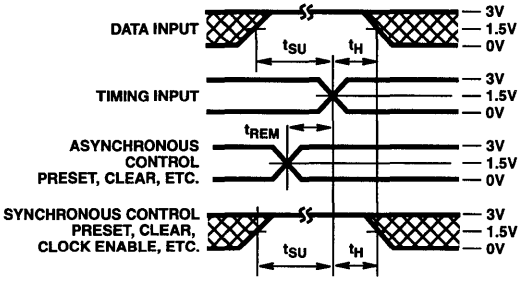


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

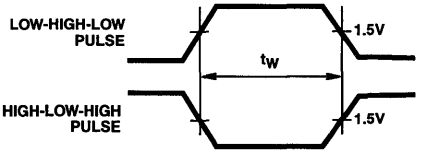


FIGURE 3. PULSE WIDTH

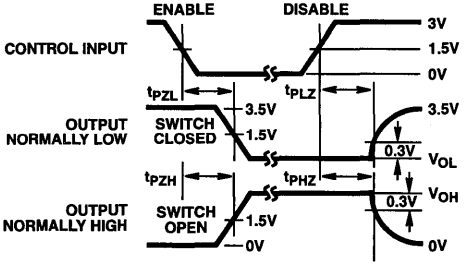


FIGURE 4. ENABLE AND DISABLE TIMING

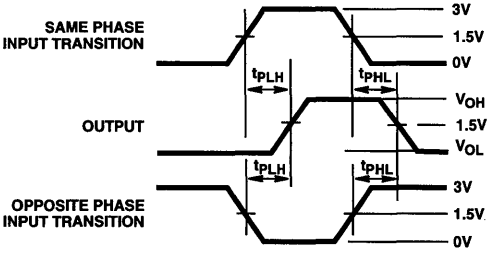


FIGURE 5. PROPAGATION DELAY

5 D.D. 5V FCT BAL. AND HIGH DRIVE

HARRIS SEMICONDUCTOR

CD74FCT16500T, CD74FCT162500T

December 1996

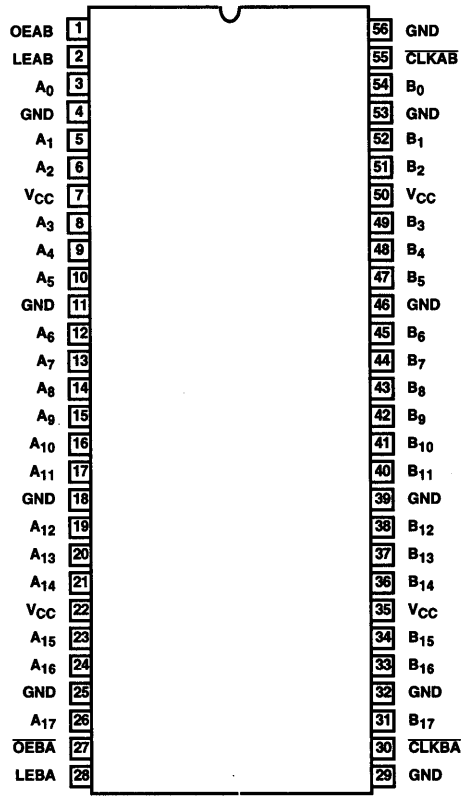
Fast CMOS 18-Bit Registered Transceivers

Features

- **These Devices are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16500T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162500T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**

Pinout

CD74FCT16500T, CD74FCT162500T
(SSOP, TSSOP)
TOP VIEW



Description

Harris' CD74FCT16500T and CD74FCT162500T are produced in an advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

These devices are 18-bit registered bus transceivers designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (OEAB and $\overline{OEBA}$, Latch Enable (LEAB and LEBA) and Clock ($\overline{CLKAB}$ and $\overline{CLKBA}$) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if $\overline{CLKAB}$ is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of $\overline{CLKAB}$, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using OEBA, LEBA and $\overline{CLKBA}$. These high-speed, low power devices offer a flow-through organization for ease of board layout.

The CD74FCT16500T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162500T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Ordering Information

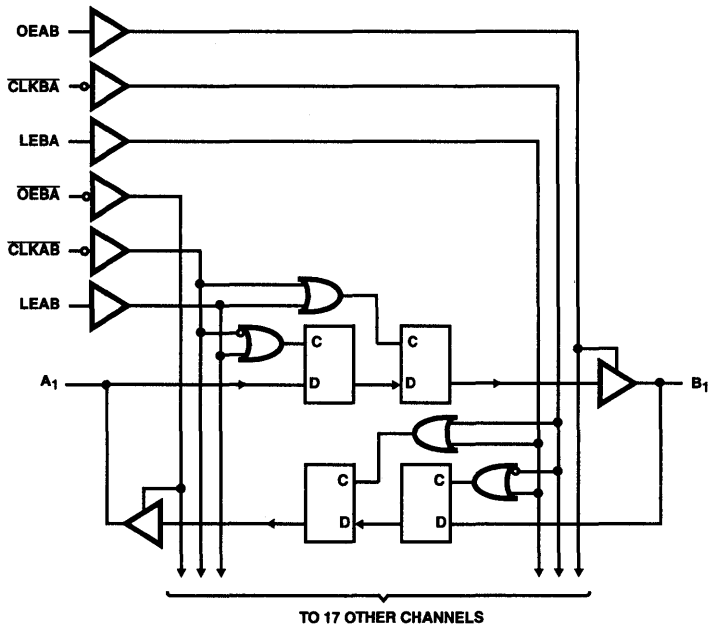
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16500ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16500ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16500CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16500CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16500DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162500ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162500ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162500CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162500CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162500DTMT	-40 to 85	56 Ld TSSOP	M56.240-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4202.1**

Functional Block Diagram



TRUTH TABLE (NOTES 1, 4)

INPUTS				OUTPUTS
OEAB	LEAB	$\overline{CLKAB}$	A_X	B_X
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B (Note 2)
H	L	L	X	B (Note 3)

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was LOW before LEAB went LOW.
4. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance
   ↓ = HIGH-to-LOW Transition

Pin Descriptions

PIN NAME	DESCRIPTION
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{CLKAB}$	A-to-B Clock Input (Active LOW)
$\overline{CLKBA}$	B-to-A Clock Input (Active LOW)
A_X	A-to-B Data Inputs or B-to-A Three-State Outputs
B_X	B-to-A Data Inputs or A-to-B Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS		MIN	(NOTE 7) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 8), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 8), V_{OUT} = 2.5		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
CD74FCT16500T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤ 4.5V		-	-	±100	µA
CD74FCT162500T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 8)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 8)		-60	-115	-150	mA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS		MIN	(NOTE 7) TYP	MAX	UNITS
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OEAB}$ = $\overline{OEBA}$ = V_{CC} or GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	75	120	µA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz ($\overline{CLKAB}$) 50% Duty Cycle $\overline{OEAB}$ = $\overline{OEBA}$ = V_{CC} LEAB = GND One Bit Toggling f_i = 5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.8	2.7 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.3	4.2 (Note 12)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz ($\overline{CLKAB}$) 50% Duty Cycle $\overline{OEAB}$ = $\overline{OEBA}$ = V_{CC} LEAB = GND 18 Bits Toggling f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.8	7.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	8.6	21.85 (Note 12)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	AT		CT		DT		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
$\overline{CLKAB}$ or $\overline{CLKBA}$ frequency	f_{MAX}	C_L = 50pF R_L = 500Ω	-	150	-	150	-	150	MHz
Propagation Delay A_X to B_X or B_X to A_X	t_{PLH}, t_{PHL}		1.5	5.1	1.5	4.6	1.5	4.1	ns
Propagation Delay LEBA to A_X, LEAB to B_X	t_{PLH}, t_{PHL}		1.5	5.6	1.5	5.3	1.5	4.6	ns
Propagation Delay $\overline{CLKBA}$ to A_X, $\overline{CLKAB}$ to B_X	t_{PLH}, t_{PHL}		1.5	5.6	1.5	5.3	1.5	4.6	ns
Output Enable Time $\overline{OEBA}$ to A_X, OEAB to Bx	t_{PZH}, t_{PZL}		1.5	6.0	1.5	5.6	1.5	5.0	ns
Output Disable Time (Note 16) $\overline{OEBA}$ to A_X, OEAB to B_X	t_{PHZ}, t_{PLZ}		1.5	5.6	1.5	5.2	1.5	4.8	ns

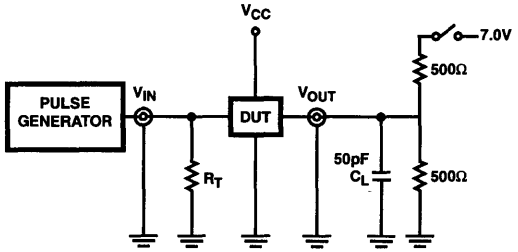
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	AT (NOTE 15) MIN	AT MAX	CT (NOTE 15) MIN	CT MAX	DT (NOTE 15) MIN	DT MAX	UNITS
Setup Time HIGH or LOW A_X to $\overline{CLKAB}$, B_X to $\overline{CLKBA}$	t_{SU}	C_L = 50pF, R_L = 500Ω	3.0	-	3.0	-	3.0	-	ns
Hold Time HIGH or LOW, A_X to $\overline{CLKAB}$, B_X to $\overline{CLKBA}$	t_H		0	-	0	-	0	-	ns
Setup Time HIGH or LOW, A_X to LEAB, B_X to LEBA Clock HIGH	t_{SU}		3.0	-	3.0	-	3.0	-	ns
Setup Time HIGH or LOW, A_X to LEAB, B_X to LEBA Clock LOW	t_{SU}		1.5	-	1.5	-	1.5	-	ns
Hold Time HIGH or LOW, Ax to LEAB, Bx to LEBA	t_H		1.5	-	1.5	-	1.5	-	ns
LEAB or LEBA Pulse Width HIGH (Note 16)	t_W		3.0	-	3.0	-	3.0	-	ns
$\overline{CLKAB}$ or $\overline{CLKBA}$ Pulse Width HIGH or LOW (Note 16)	t_W		3.0	-	3.0	-	3.0	-	ns
Output Skew for CD74FCT162500T (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

6. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
7. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading, except as noted.
8. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:
C_L = Load capacitance, includes jig and probe capacitance.
R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

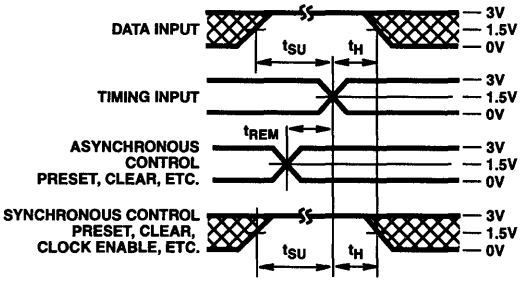


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

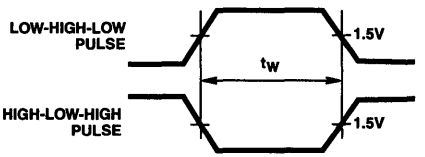


FIGURE 3. PULSE WIDTH

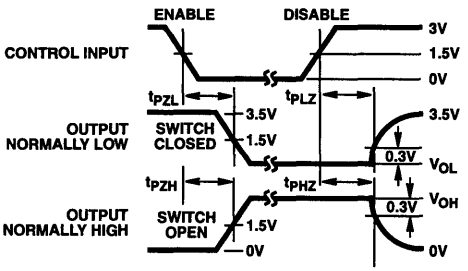


FIGURE 4. ENABLE AND DISABLE TIMING

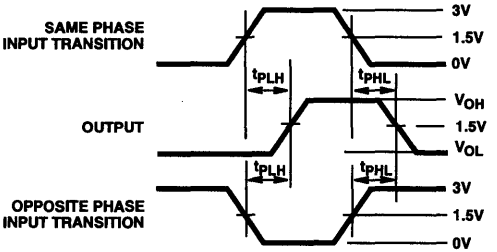


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16501T, CD74FCT162501T

December 1996

Fast CMOS 18-Bit Registered Transceivers

Features

- **Advanced 0.6 micron CMOS Technology**
- **These Devices are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16501T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162501T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**

Description

These devices are 18-bit are registered bus transceivers designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (OEAB and $\overline{OEBA}$, Latch Enable (LEAB and LEBA) and Clock (CLKAB and CLKBA) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of CLKAB, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using $\overline{OEBA}$, LEBA and CLKBA. These high-speed, low power devices offer a flow-through organization for ease of board layout.

The CD74FCT16501T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162501T has 24 mA balanced output divers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Ordering Information

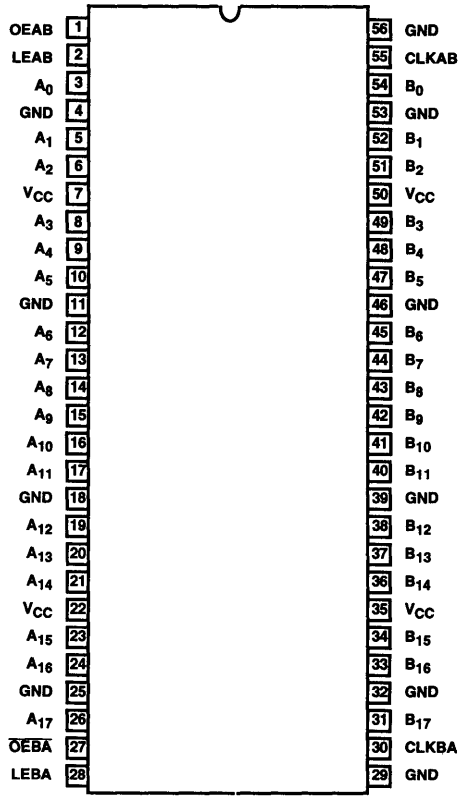
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16501ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16501ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16501CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16501CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16501DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16501DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16501ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16501ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162501ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162501ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162501CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162501CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162501DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162501DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162501ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162501ETSM	-40 to 85	56 Ld SSOP	M56.300-P

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

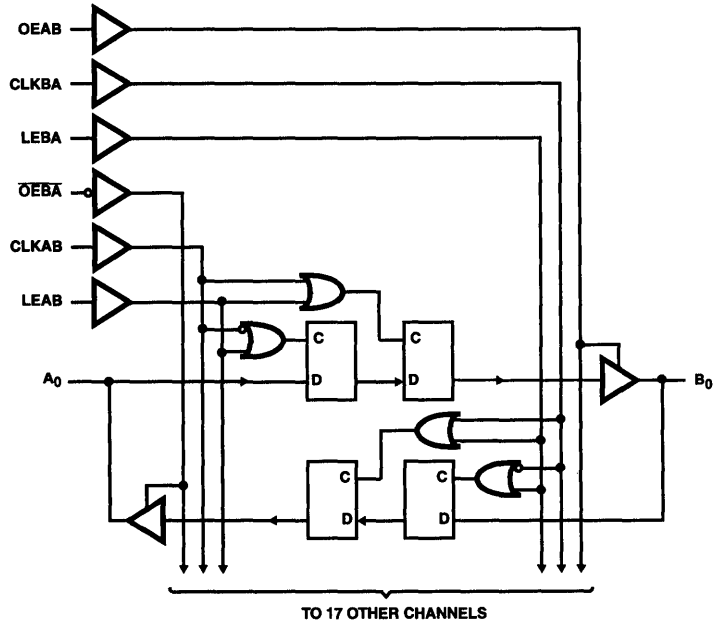
File Number **4184.1**

Pinout

CD74FCT16501T, CD74FCT162501T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTES 1, 4)

INPUTS				OUTPUTS
OEAB	LEAB	CLKAB	A_X	B_X
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B (Note 2)
H	L	H	X	B (Note 3)

NOTES:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions wer established, provided that CLKAB was LOW before LEAB went LOW.
4. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A_X	A-to-B Data Inputs or B-to-A Three-State Outputs
B_X	B-to-A Data Inputs or A-to-B Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only. . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only. . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)
SOIC Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS		MIN	(NOTE 7) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input LOW Current	I_{IL}	Standard Input, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current (Three-State) (Note 9)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 8), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 8), V_{OUT} = GND		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
CD74FCT16501T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
CD74FCT162501T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 10)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 10)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 6) TEST CONDITIONS		MIN	(NOTE 7) TYP	MAX	UNITS
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 11)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open OEAB = $\overline{OEBA}$ = V_{CC} or GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	75	120	µA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.8	1.7 (Note 13)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.3	4.2 (Note 13)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle OEAB = $\overline{OEBA}$ = V_{CC} LEAB = GND 18 Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.8	6.5 (Note 13)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	8.5	20.8 (Note 13)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	AT (NOTE 16) MIN	AT MAX	CT (NOTE 16) MIN	CT MAX	DT (NOTE 16) MIN	DT MAX	ET (NOTE 16) MIN	ET MAX	UNITS
CLKAB or CLKBA Frequency	f_{MAX}	C_L = 50pF R_L = 500Ω	-	150	-	150	-	150	-	150	MHz
Propagation Delay A_X to B_X or B_X to A_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	5.1	1.5	4.6	1.5	4.1	1.5	3.8	ns
Propagation Delay LEBA to A_X, LEAB to B_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns
Propagation Delay CLKBA to A_X, CLKAB to B_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	5.6	1.5	5.3	1.5	4.6	1.5	4.2	ns
Output Enable Time $\overline{OEBA}$ to A_X, OEAB to Bx	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	5.6	1.5	5.2	1.5	4.8	ns
Output Disable Time (Note 14) $\overline{OEBA}$ to A_X, OEAB to B_X	t_{PHZ} t_{PLZ}	C_L = 50pF R_L = 500Ω	1.5	5.6	1.5	5.2	1.5	5.2	1.5	5.2	ns
Setup Time HIGH or LOW A_X to CLKAB, B_X to CLKBA	t_{SU}	C_L = 50pF R_L = 500Ω	3.0	-	3.0	-	3.0	-	2.4	-	ns
Hold Time HIGH or LOW A_X to CLKAB, B_X to CLKBA	t_H	C_L = 50pF R_L = 500Ω	0	-	0	-	0	-	0	-	ns

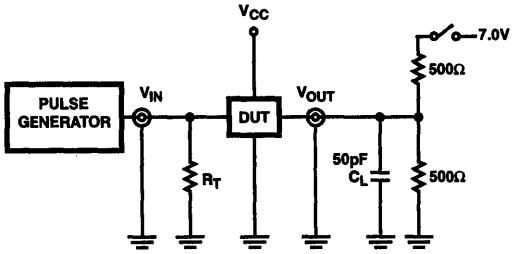
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	AT (NOTE 16) MIN	AT MAX	CT (NOTE 16) MIN	CT MAX	DT (NOTE 16) MIN	DT MAX	ET (NOTE 16) MIN	ET MAX	UNITS
Setup Time HIGH or LOW, A_X to LEAB, B_X to LEBA, Clock HIGH	t_{SU}	C_L = 50pF R_L = 500Ω	3.0	-	3.0	-	3.0	-	2.0	-	ns
Setup Time HIGH or LOW, A_X to LEAB, B_X to LEBA, Clock LOW	t_{SU}	C_L = 50pF R_L = 500Ω	1.5	-	1.5	-	1.5	-	1.5	-	ns
Hold Time HIGH or LOW, Ax to LEAB, Bx to LEBA	t_H	C_L = 50pF R_L = 500Ω	1.5	-	1.5	-	1.5	-	0.5	-	ns
LEAB or LEBA Pulse Width HIGH (Note 17)	t_W	C_L = 50pF R_L = 500Ω	3.0	-	3.0	-	3.0	-	3.0	-	ns
CLKAB or CLKBA Pulse Width HIGH or LOW (Note 17)	t_W	C_L = 50pF R_L = 500Ω	3.0	-	3.0	-	3.0	-	3.0	-	ns
Output Skew (Note 18)	$t_{SK(O)}$	C_L = 50pF R_L = 500Ω	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

6. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
7. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
8. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
9. This specification does not apply to bi-directional functionalities with Bus Hold.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
15. See test circuit and wave forms.
16. Minimum limits are guaranteed but not tested on Propagation Delays.
17. This parameter is guaranteed but not production tested.
18. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

19. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

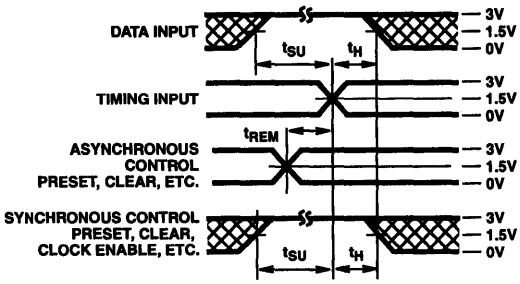


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

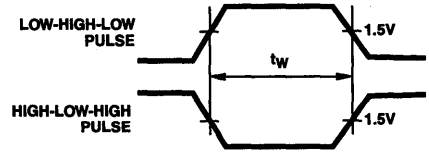


FIGURE 3. PULSE WIDTH

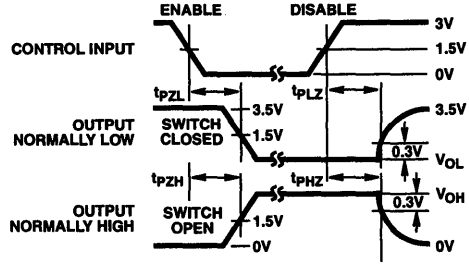


FIGURE 4. ENABLE AND DISABLE TIMING

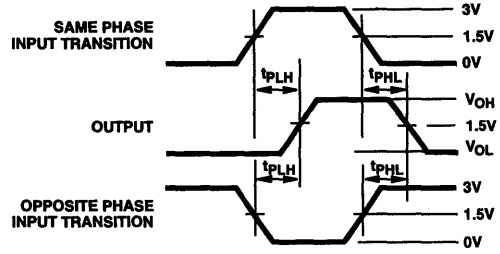


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16511T, CD74FCT162511T

Fast CMOS 16-Bit Registered/Latched Transceivers with Parity

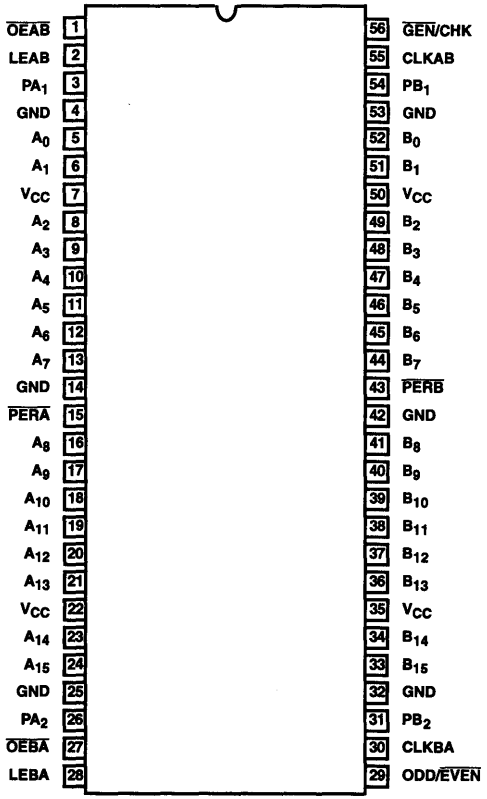
December 1996

Features

- **These Devices are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16511T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162511T**
  - **Balanced Output Drivers: ±24mA**
  - **Open Drain Parity Error Allows Wire-OR**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**

Pinout

CD74FCT16511T, CD74FCT162511T (SSOP, TSSOP)
TOP VIEW



Description

Harris' CD74FCT16511T and CD74FCT162511T are produced in an advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The CD74FCT16511T and CD74FCT162511T are high-speed, low-power 16-bit registered/latched transceiver with parity which combines D-type latches and D-type flip-flops to allow data flow in transparent, latched or clocked modes. It has a parity generator/checker in the A-to-B direction and a parity checker in the B-to-A direction. Error checking is done at the byte level with separate parity bits for each byte. One error flag for each direction (A-to-B or B-to-A) exists to indicate an error for either byte in either direction. The parity error flags which are open drain outputs, can be tied together and/or tied with flags from other devices to form a single error flag or interrupt. To disable the error flag during combinational transitions, a designer can disable the parity error flag by the $\overline{OEXX}$ control pins.

The operation in A-to-B direction is controlled by LEAB, CLKAB and $\overline{OEAB}$ control pins, and the operation in B-to-A direction is controlled by LEBA, CLKBA and $\overline{OEBA}$ control pins. $\overline{GEN}$/CHK is used to select the operation of A-to-B direction, while B-to-A direction is always in checking mode. The ODD/$\overline{EVEN}$ select is common between the two directions. Independent operation can be achieved between the two directions by using the corresponding control lines except for the ODD/$\overline{EVEN}$ control.

Ordering Information

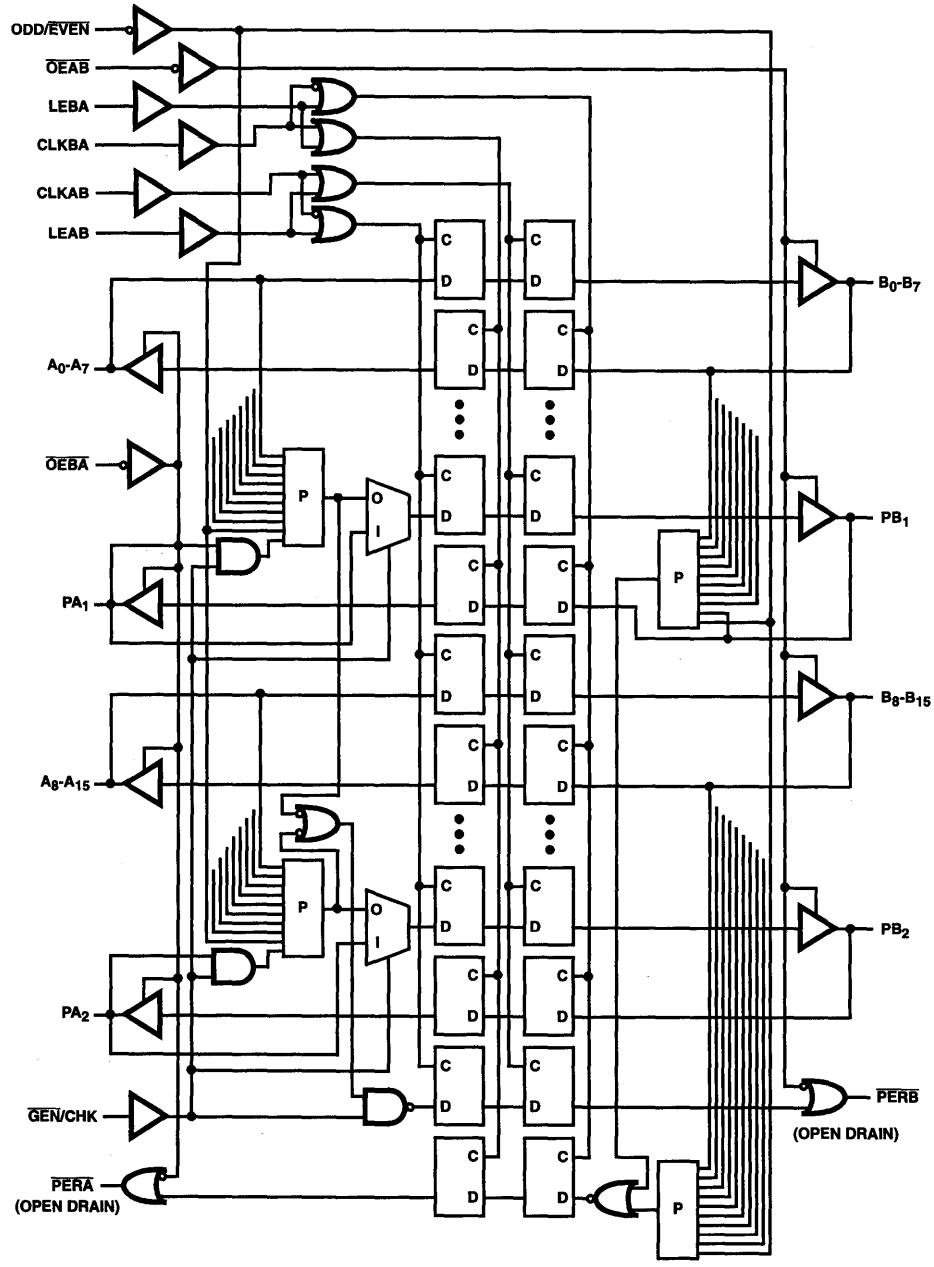
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16511ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16511TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162511ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162511ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162511TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162511TSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the varient in the tape and reel.

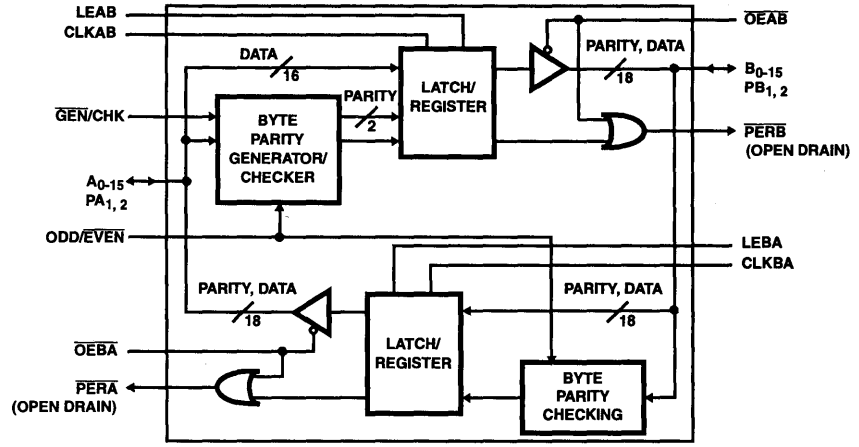
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4218.2**

Functional Block Diagram



Simplified Functional Block Diagram



TRUTH TABLE (NOTES 1, 2)

INPUTS				OUTPUT BUFFERS
$\overline{OEAB}$	LEAB	CLKAB	A_X	B_X
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L	X	B (Note 3)
L	L	H	X	B (Note 4)

NOTES:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care or Irrelevant
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition
2. A-to-B data flow is shown. B-to-A flow control is the same, except using $\overline{OEBA}$, LEBA, and CLKBA.
3. Output level before the indicated steady-state input conditions were established.
4. Output level before the indicated steady-state input conditions were established, assuming CLKAB was HIGH before LEAB went LOW.

TRUTH TABLE (PARITY GENERATION) (NOTES 5, 6, 7, 8, 9)

TOTAL NUMBER OF INPUTS THAT ARE HIGH, A_0 - A_7	ODD/$\overline{EVEN}$	PB_1
1, 3, 5 or 7	L	H
1, 3, 5 or 7	H	L
0, 2, 4, 6 or 8	L	L
0, 2, 4, 6 or 8	H	H

NOTES:

5. Conditions shown are for $\overline{GEN}$/CHK = L, $\overline{OEAB}$ = L, $\overline{OEBA}$ = H.
6. A-to-B parity generation is shown. B-to-A can check parity while A-to-B is performing generation. B-to-A will not generate parity.
7. The response shown is for LEAB = H. If LEAB = L, then CLKAB will control as an edge triggered clock.
8. Conditions shown are for the byte A0-A7. The byte A8-A15 is similar but will output the parity on PB2.
9. The error flag $\overline{PERB}$ will remain in a high state during parity generation.

TRUTH TABLE (PARITY CHECKING) (NOTES 10, 11, 12, 13)

TOTAL NUMBER OF INPUTS THAT ARE HIGH, A_0 - A_7 AND PA_1 (NOTE 14)	ODD/$\overline{EVEN}$	PB_1
1, 3, 5, 7 or 9	L	L
1, 3, 5, 7 or 9	H	H (Note 15)
0, 2, 4, 6 or 8	L	H (Note 15)
0, 2, 4, 6 or 8	H	L

10. Conditions shown are for $\overline{GEN}$/CHK = H, $\overline{OEAB}$ = L, $\overline{OEBA}$ = H.
11. A-to-B parity checking is shown. B-to-A parity checking is same but uses $\overline{OEBA}$ = L, $\overline{OEAB}$ = H and errors will be indicated on $\overline{PERA}$.
12. In parity checking mode the parity bits will be transmitted unchanged along with the corresponding data regardless of parity errors. ($PB_1 = PA_1$)
13. The response shown is for LEAB = H. If LEAB = L, then CLKAB will control as an edge triggered clock.
14. Conditions shown are for the byte A_0-A_7 and PA_1. The byte A_8-A_{15} and PA_2 is same.
15. The parity error flag $\overline{PERB}$ is a combined flag for both bytes A_0-A_7 and A_8-A_{15}. If a parity error occurs on either byte $\overline{PERB}$ will go low.

Pin Descriptions

PIN NAME	DESCRIPTION
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
$\overline{PERA}$	Parity Error (Open Drain) on A Outputs
$\overline{PERB}$	Parity Error (Open Drain) on B Outputs
A_X	A-to-B Data Inputs or B-to-A Three State Outputs
B_X	B-to-A Data Inputs or B-to-A Three State Outputs
ODD/$\overline{EVEN}$ (Note 16)	Parity Mode Selection Input
$\overline{GEN}$/CHK (Note 16)	A-to-B Port Generate or Check Mode Input
PA_X (Note 17)	A-to-B Parity Input, B-to-A Parity Output
PB_X	B-to-A Parity Input, A-to-B Parity Output
GND	Ground
V_{CC}	Power

NOTES:

16. ODD/$\overline{EVEN}$ and $\overline{GEN}$/CHK should be tied to V_{CC} or GND with no resistor for optimum results.
17. The PA_X pin input is internally disabled during parity generation. This means that when generating parity in the A-to-B direction, there is no need to add a pull-up resistor to guarantee state. The pin will still function properly as the parity output for the B-to-A direction.

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 18) θ_{JA} (°C/W)
TSSOP Package 85
SSOP Package 70
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

18. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 19) TEST CONDITIONS		MIN	(NOTE 20) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = Vcc	-	-	1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = Vcc	-	-	-1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current (I/O Pins)	I_{OS}	V_{CC} = Max (Note 21), V_{OUT} = GND		-80	-140	-225	mA
Output Drive Current (I/O Pins)	I_O	V_{CC} = Max (Note 21), V_{OUT} = 2.5V		-50	-	-180	mA
Output Leakage Current (Open Drain)	I_{OFF}	V_{CC} = Max, V_{OUT} = 4.5V		-	-	±100	µA
Input Hysteresis	V_H			-	100	-	mV
CD74FCT16511T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤ 4.5V		-	-	±100	µA
CD74FCT162511T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 21)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 21)		-60	-115	-150	mA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 19) TEST CONDITIONS		MIN	(NOTE 20) TYP	MAX	UNITS
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 22)	C_{IN}	V_{IN} = 0V		-	4.5	6.0	pF
I/O Capacitance (Note 22)	$C_{I/O}$	V_{OUT} = 0V		-	5.5	8.0	pF
Open Drain Capacitance (Note 22)	C_O	V_{OUT} = 0V		-	4.5	6.0	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CCL}, I_{CCH}, I_{CCZ}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 23)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 24)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OEAB}$ = GND $\overline{OEBA}$ = VCC One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	75	120	µA/ MHz
Total Power Supply Current (Note 26)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle LEAB = $\overline{OEAB}$ = GND $\overline{OEBA}$ = V_{CC} f_i = 5MHz One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	0.8	1.7 (Note 25)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.3	3.2 (Note 25)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz (CLKAB) 50% Duty Cycle LEAB = $\overline{OEAB}$ = GND $\overline{OEBA}$ = V_{CC} f_i = 2.5MHz 18 Bits Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	3.8	6.5 (Note 25)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	9.0	21.8 (Note 25)	mA

Switching Specifications Over Operating Range (Propagation Delays)

PARAMETER	SYMBOL	(NOTE 27) TEST CONDITIONS	T (NOTE 28) MIN	T MAX	AT (NOTE 28) MIN	AT MAX	UNITS
Propagation Delay PA_X to PB_X	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.7	ns
Propagation Delay A_X to B_X or B_X to A_X, PB_X to PA_X	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.0	ns
Propagation Delay A_X to PB_X	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	7.5	ns
Propagation Delay A_X to $\overline{PERB}$, PA_X to $\overline{PERB}$	t_{PLH} (Note 29) t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	10.5	1.5	9.0	ns
			1.5	9.5	1.5	8.0	ns
Propagation Delay B_X to $\overline{PERA}$, PB_X to $\overline{PERA}$	t_{PLH} (Note 29) t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	10.5	1.5	9.0	ns
			1.5	9.5	1.5	8.0	ns
Propagation Delay LEBA to A_X and PA_X, LEAB to B_X and PB_X	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	5.6	ns
Propagation Delay LEBA to $\overline{PERA}$, LEAB to $\overline{PERB}$	t_{PLH} (Note 29) t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	7.5	1.5	7.0	ns
			1.5	6.5	1.5	6.0	ns

Switching Specifications Over Operating Range (Propagation Delays) **(Continued)**

PARAMETER	SYMBOL	(NOTE 27) TEST CONDITIONS	T (NOTE 28) MIN	T MAX	AT (NOTE 28) MIN	AT MAX	UNITS
Propagation Delay CLKBA to A_X and PA_X CLKAB to B_X and PB_X	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	5.6	ns
Propagation Delay CLKBA to $\overline{PERA}$	t_{PLH} (Note 29) t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	7.5	1.5	7.0	ns
CLKAB to $\overline{PERB}$			1.5	6.5	1.5	6.0	ns
Output Enable Time $\overline{OEBA}$ to A_X and PA_X $\overline{OEAB}$ to B_X and PB_X	t_{PZH} t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	6.0	ns
Output Disable Time (Note 30) $\overline{OEBA}$ to Ax and PAx $\overline{OEAB}$ to Bx and PBx	t_{PHZ} t_{PLZ}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	5.6	ns
Parity ERROR Enable $\overline{OEBA}$ to $\overline{PERA}$, $\overline{OEAB}$ to $\overline{PERB}$	t_{PLZ} (Note 29) t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	6.0	1.5	6.0	ns
			1.5	6.0	1.5	6.0	ns
ODD/$\overline{EVEN}$ to $\overline{PERB}$	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	10.0	ns
			1.5	10.0	1.5	10.0	ns
ODD/$\overline{EVEN}$ to PB_X	t_{PLH} t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	10.0	ns

Switching Specifications Over Operating Range (Setup Times)

DESCRIPTION	SYMBOL	(NOTES 27, 31) CONDITIONS			T MIN	T MAX	AT MIN	AT MAX	UNITS
Setup Time HIGH or LOW A_X to CLKAB	t_{SU}	$\overline{GEN}$/CHK LOW	PB_X valid	C_L = 50pF R_L = 500Ω	6.5	-	4	-	ns
			PB_X not valid		3	-	3	-	ns
		$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	4	-	ns
			$\overline{PERB}$ not valid		3	-	3	-	ns
Setup Time PA_X to CLKAB	t_{SU}	$\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	4	-	ns
			$\overline{PERB}$ not valid		3	-	3	-	ns
Setup Time B_X to CLKBA PB_X to CLKBA	t_{SU}		$\overline{PERA}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	4	-	ns
			$\overline{PERA}$ not valid		3	-	3	-	ns
Setup Time A_X to LEAB	t_{SU}	CLKAB LOW $\overline{GEN}$/CHK LOW	PB_X valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			PB_X not valid		3	-	3	-	ns
		CLKAB LOW $\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			$\overline{PERB}$ not valid		3	-	3	-	ns
		CLKAB HIGH $\overline{GEN}$/CHK LOW	PB_X valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			PB_X not valid		3	-	3	-	ns
		CLKAB HIGH $\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			$\overline{PERB}$ not valid		3	-	3	-	ns

Switching Specifications Over Operating Range (Setup Times) **(Continued)**

DESCRIPTION	SYMBOL	(NOTES 27, 31) CONDITIONS			T		AT		UNITS
					MIN	MAX	MIN	MAX	
Setup Time PAx to LEAB	t_{SU}	CLKAB LOW $\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			$\overline{PERB}$ not valid		3	-	3	-	ns
		CLKAB HIGH $\overline{GEN}$/CHK HIGH	$\overline{PERB}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			$\overline{PERB}$ not valid		3	-	3	-	ns
Setup Time B_X to LEBA PB_X to LEBA	t_{SU}	CLKBA LOW	$\overline{PERA}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			$\overline{PERA}$ not valid		3	-	3	-	ns
		CLKAB HIGH	$\overline{PERA}$ valid	C_L = 50pF R_L = 500Ω	6.5	-	3.5	-	ns
			$\overline{PERA}$ not valid		3	-	3	-	ns

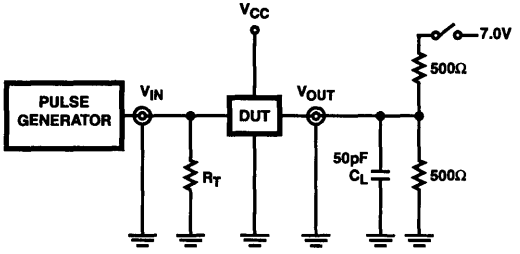
Switching Specifications Over Operating Range (Hold Times)

DESCRIPTION	SYMBOL	(NOTE 27) CONDITIONS	T		AT		UNITS
			MIN	MAX	MIN	MAX	
Hold Time HIGH or LOW A_X to LEAB, B_X to LEBA	t_H	C_L = 50pF R_L = 500Ω	1	-	1	-	ns
Hold Time HIGH or LOW PA_X to LEAB	t_H		1	-	1	-	ns
Hold Time HIGH or LOW PB_X to LEBA	t_H		1	-	1	-	ns
Hold Time A_X to CLKAB, PA_X to CLKAB	t_H		1	-	1	-	ns
Hold Time B_X to CLKBA, PB_X to CLKBA	t_H		1	-	1	-	ns
LEAB or LEBA Pulse Width HIGH (Note 30)	t_W		3	-	3	-	ns
CLKAB or CLKBA Pulse Width HIGH or LOW (Note 30)	t_W		3	-	3	-	ns

NOTES:

19. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
20. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
21. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
22. This parameter is determined by device characterization but is not production tested.
23. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
24. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
25. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
26. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
27. See test circuit and wave forms.
28. Minimum limits are guaranteed but not tested on Propagation Delays.
29. On Open Drain Outputs t_{PLH} is measured up to $V_{OUT} = V_{OL}$ + O.3V.
30. This parameter is guaranteed but not production tested.
31. "Not Valid" means the setup time indicated is not sufficient to assure proper funtioning of this output; however, the set-up time indicated will assure proper functioning of the A-to-B or B-to-A port respective to the indicated direction.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

32. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

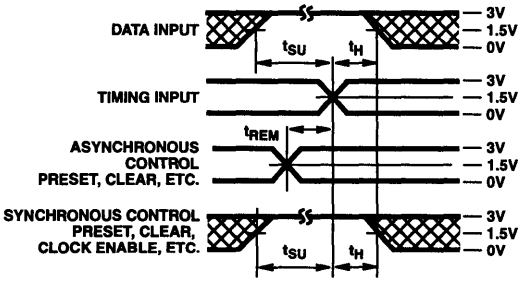


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

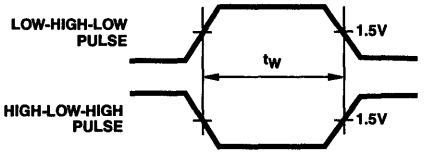


FIGURE 3. PULSE WIDTH

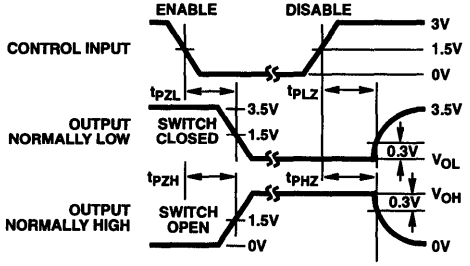


FIGURE 4. ENABLE AND DISABLE TIMING

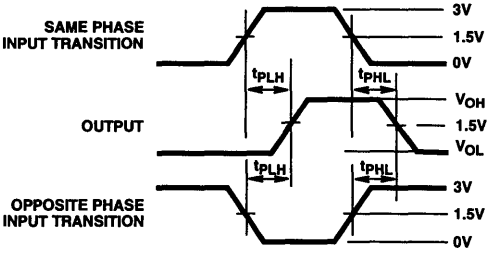


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16540T, CD74FCT162540T

December 1996

Fast CMOS 16-Bit Buffer/Line Drivers

Features

- Advanced 0.6 micron CMOS Technology
- These Devices are High-speed, Low Power Devices with High Current Drive
- V_{CC} = 5V ±10%
- Hysteresis on All Inputs
- CD74FCT16540T
  - High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA
  - Power Off Disable Outputs Permit "Live Insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- CD74FCT162540T
  - Balanced Output Drivers: ±24mA
  - Reduced System Switching Noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

Description

These devices are inverting 16-bit buffer/line drivers designed for applications driving high capacitance loads and low impedance backplanes. These high-speed, low power devices offer bus/backplane interface capability and a flow-through organization for ease of board layout. They are designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

The CD74FCT16540T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162540T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16540ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16540ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16540CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16540CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16540TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16540TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162540ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162540ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162540CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162540CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162540TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162540TSM	-40 to 85	48 Ld SSOP	M48.300-P

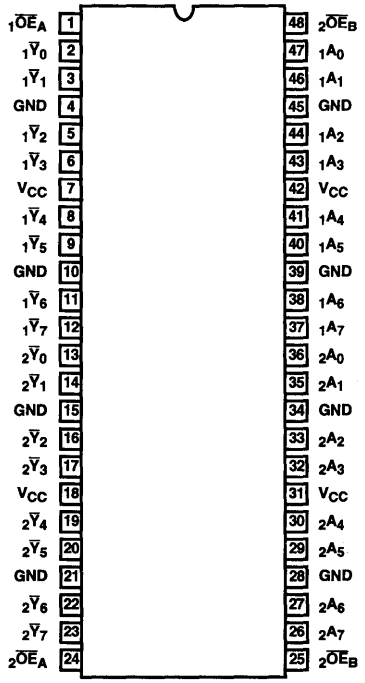
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

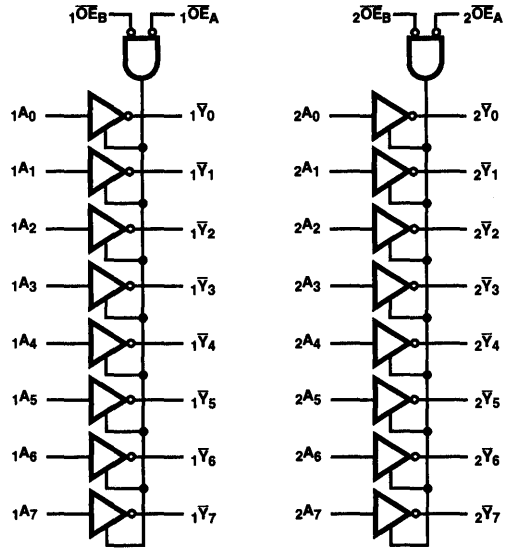
File Number 4185.1

Pinout

CD74FCT16540T, CD74FCT162540T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$_x\overline{OE}$	$_xA_x$	$_x\overline{Y}_x$
L	L	H
L	H	L
H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_x\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$_xA_x$	Inputs
$_x\overline{Y}_x$	Three-State Outputs (Active Low)
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . $-40^{o}C$ to $85^{o}C$
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^{o}C$ to $85^{o}C$, $V_{CC} = 5.0V \pm 10\%$							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 6) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 7)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 5), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
CD74FCT16540T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤ 4.5V		-	-	±100	µA
CD74FCT162540T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 9)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open x$\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle x$\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.6	1.5 (Note 11)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	0.9	2.3 (Note 11)	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz 50% Duty Cycle x$\overline{OE}$ = GND 16 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	2.4	4.5 (Note 11)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.4	16.5 (Note 11)	mA

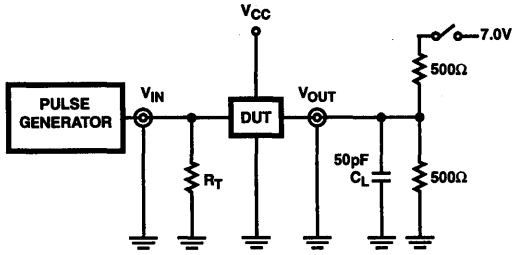
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 13) TEST CONDITIONS	T		AT		CT		UNITS
			(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	
Propagation Delay xA_x to xY_x	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	4.8	1.5	4.3	ns
Output Enable Time $x\overline{OE}$ to xAx or $x\overline{Y}x$	t_{PZH}, t_{PZL}		1.5	10.0	1.5	6.2	1.5	5.8	ns
Output Disable Time (Note 15) $x\overline{OE}$ to xAx or $x\overline{Y}x$	t_{PHZ}, t_{PLZ}		1.5	9.5	1.5	5.6	1.5	5.2	ns
Output Skew (Note 16)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading, except as noted.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. Pins with Bus Hold are identified in the pin description.
7. This specification does not apply to bi-directional functionalities with Bus Hold.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
13. See test circuit and wave forms.
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. This parameter is guaranteed but not production tested.
16. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

17. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

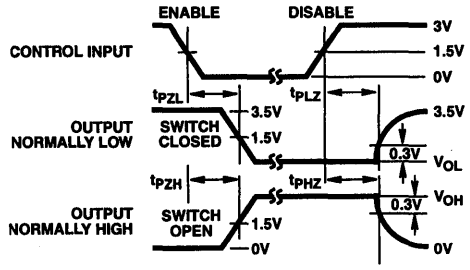


FIGURE 2. ENABLE AND DISABLE TIMING

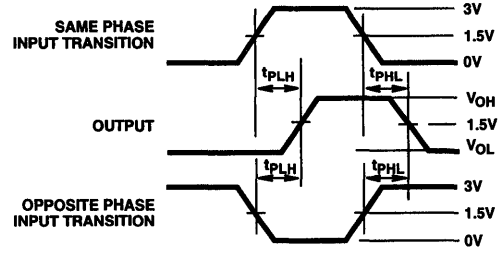


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16541T, CD74FCT162541T

December 1996

Fast CMOS 16-Bit Octal Buffer/Line Drivers

Features

- Advanced 0.6 micron CMOS Technology
- These Devices Are High-speed, Low Power Devices with High Current Drive
- V_{CC} = 5V ±10%
- Hysteresis on All Inputs
- Output Skew: ≤ .5ns
- CD74FCT16541T
  - High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA
  - Power Off Disable Outputs Permit "Live Insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- CD74FCT162541T
  - Balanced Output Drivers: ±24mA
  - Reduced System Switching Noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

Description

These devices are non-inverting 16-bit buffer/line drivers designed for applications driving high capacitance loads and low impedance backplanes. These high-speed, low power devices offer bus/backplane interface capability and a flow-through organization for ease of board layout. These devices are designed with three-state controls to operate in a Dual-Byte, or a single 16-bit word mode.

The CD74FCT16541T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162541T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

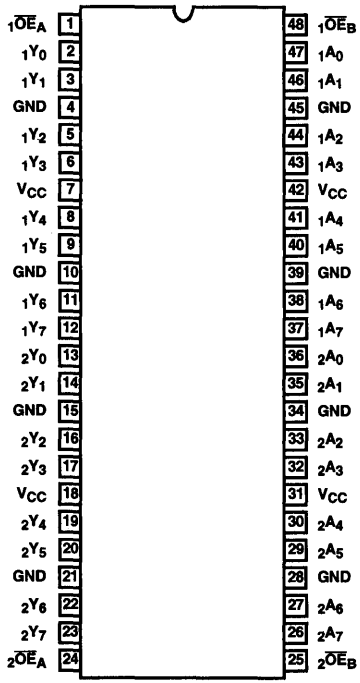
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16541ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16541ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16541CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16541CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16541DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16541DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16541ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16541ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT16541TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT16541TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162541ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162541ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162541CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162541CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162541DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162541DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162541ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162541ETSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162541TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162541TSM	-40 to 85	48 Ld SSOP	M48.300-P

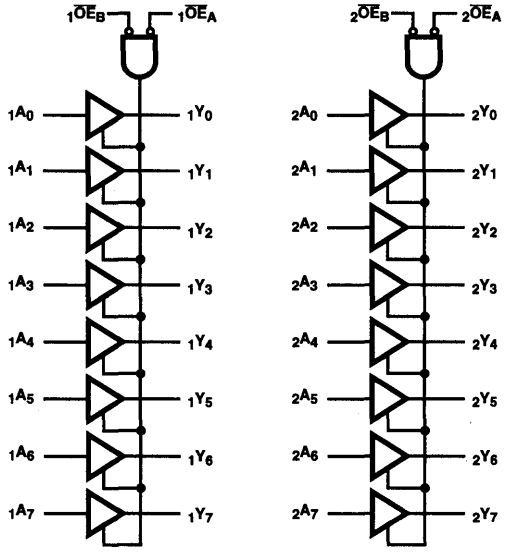
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the varient in the tape and reel.

Pinout

CD74FCT16541T, CD74FCT162541T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$_x\overline{OE}$	$_xA_x$	$_xY_x$
L	L	H
L	H	L
H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_x\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$_xA_x$	Inputs
$_xY_x$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
TSSOP Package 94
SSOP Package 76
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 6) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 7)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 5), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
CD74FCT16541T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq$ 4.5V		-	-	±100	µA
CD74FCT162541T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.6	1.5 (Note 11)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	0.9	2.3 (Note 11)	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	2.4	4.5 (Note 11)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.4	16.5 (Note 11)	mA

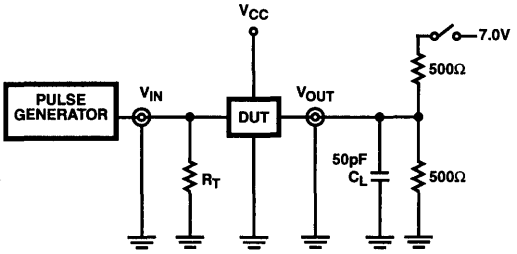
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 13) TEST CONDITIONS	T (NOTE 14) MIN	T MAX	AT (NOTE 14) MIN	AT MAX	CT (NOTE 14) MIN	CT MAX	DT (NOTE 14) MIN	DT MAX	ET (NOTE 14) MIN	ET MAX	UNITS
CD74FCT16541T, CD74FCT162541T													
Propagation Delay $_XA_X$ to $_XY_X$	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	8.0	1.5	4.8	1.5	4.3	1.5	3.6	1.5	3.2	ns
Output Enable Time $_X\overline{OE}$ to $_XA_X$ or $_XY_X$	t_{PZH}, t_{PZL}		1.5	10.0	1.5	6.2	1.5	5.8	1.5	4.8	1.5	4.4	ns
Output Disable Time (Note 15) $_X\overline{OE}$ to $_XA_X$ or $_XY_X$	t_{PHZ}, t_{PLZ}		1.5	9.5	1.5	5.6	1.5	5.2	1.5	4.0	1.5	3.6	ns
Output Skew (Note 16)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading, except as noted.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. Pins with Bus Hold are identified in the pin description.
7. This specification does not apply to bi-directional functionalities with Bus Hold.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. See test circuit and wave forms.
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. This parameter is guaranteed but not production tested.
16. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

17. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

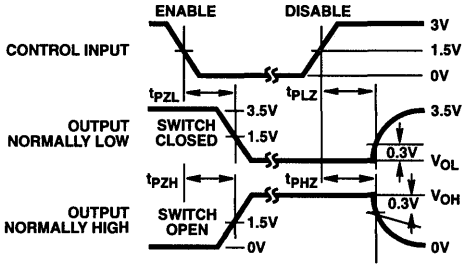


FIGURE 2. ENABLE AND DISABLE TIMING

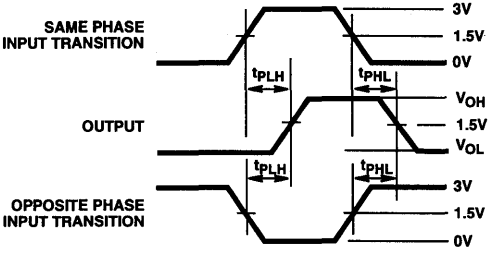


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16543T, CD74FCT162543T

December 1996

Fast CMOS 16-Bit Latched Transceivers

Features

- **Advanced 0.6 micron CMOS Technology**
- **These Devices Are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16543T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162543T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**

Description

These devices are 16-bit latched transceivers organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($_x\overline{CEAB}$) input must be LOW in order to enter data from xAx or to take data from xBx, as indicated in the Truth Table. With $_x\overline{CEAB}$ LOW, a LOW signal makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $_x\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change the A inputs. With $_x\overline{CEAB}$ and $_x\overline{OEAB}$ both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $_x\overline{CEBA}$, $_x\overline{LEBA}$, and $_x\overline{OEBA}$ inputs.

The CD74FCT16543T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162543T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications..

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16543ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16543CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16543DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16543ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16543TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16543TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162543TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162543TSM	-40 to 85	56 Ld SSOP	M56.300-P

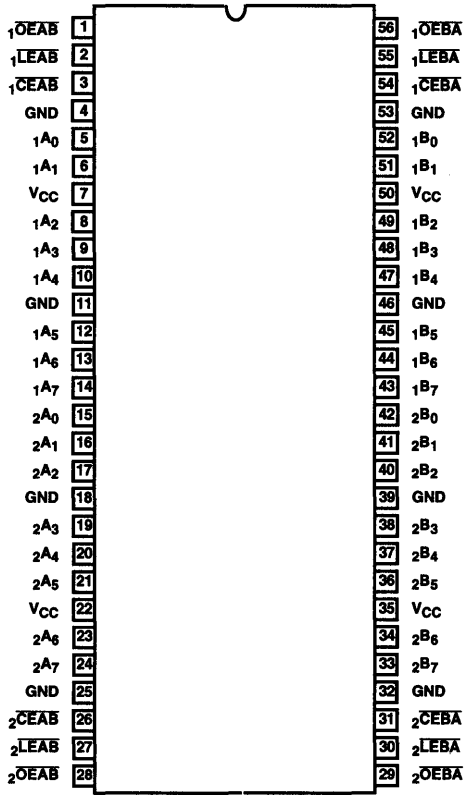
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

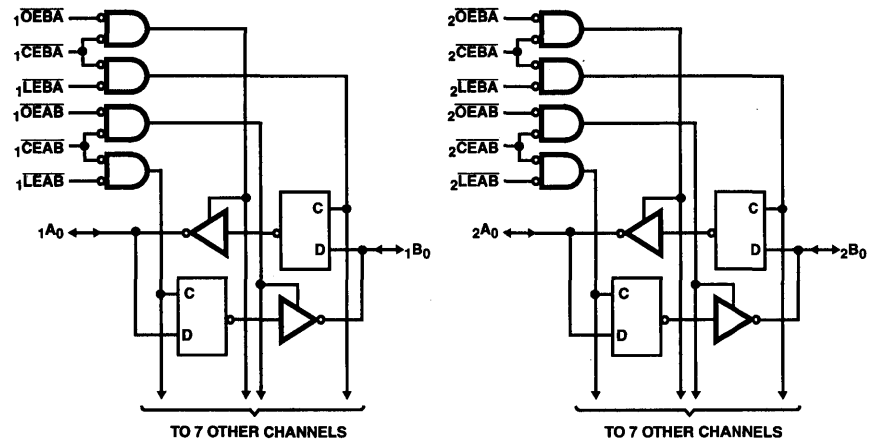
File Number **4187.1**

Pinout

CD74FCT16543T, CD74FCT162543T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTES 1, 3)

INPUTS			LATCH STATUS	OUTPUT BUFFERS
$xC\overline{EAB}$	$xL\overline{EAB}$	$xO\overline{EAB}$	xA_X TO xB_X	xB_X
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs (Note 2)

NOTES:

1. A-to-B data flow is shown. B-to-A flow control is the same except using $xC\overline{EBA}$, $xL\overline{EBA}$, and $xO\overline{EBA}$.
2. Before xLEAB LOW-to-HIGH Transition
3. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care or Irrelevant
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$xO\overline{EAB}$	A-to-B Output Enable Input (Active LOW)
$xO\overline{EBA}$	B-to-A Output Enable Input (Active LOW)
$xC\overline{EAB}$	A-to-B Enable Input (Active LOW)
$xC\overline{EBA}$	B-to-A Enable Input (Active LOW)
$xL\overline{EAB}$	A-to-B Latch Enable Input (Active LOW)
$xL\overline{EBA}$	B-to-A Latch Enable Input (Active LOW)
xA_X	A-to-B Data Inputs or B-to-A Three-State Outputs
xB_X	B-to-A Data Inputs or A-to-B Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40°C$ to $85°C$, $V_{CC} = 5.0V \pm 10\%$							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 8) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 8) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 8) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 8) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 8) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 9)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 7), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
CD74FCT16543T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq$ 4.5V		-	-	±100	µA
CD74FCT162543T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 7)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 7)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 11)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{CEAB}$ and $\overline{OEAB}$ = GND $x\overline{CEBA}$ = V_{CC} One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{LEAB}$, $x\overline{CEAB}$, and $x\overline{OEAB}$ = GND $x\overline{CEBA}$ = V_{CC} One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.6	1.5 (Note 13)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	0.9	2.3 (Note 13)	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $x\overline{LEAB}$, $x\overline{CEAB}$, and $x\overline{OEAB}$ = GND $x\overline{CEBA}$ = V_{CC} 16 Bits Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	2.4	4.5 (Note 13)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.4	16.5 (Note 13)	mA

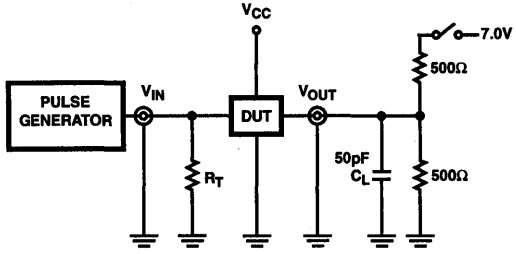
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 15) TEST CONDITIONS	T (NOTE 16) MIN	T MAX	AT (NOTE 16) MIN	AT MAX	CT (NOTE 16) MIN	CT MAX	DT (NOTE 16) MIN	DT MAX	ET (NOTE 16) MIN	ET MAX	UNITS
Propagation Delay Transparent Mode $_xA_x$ to $_xB_x$ or $_xB_x$ to $_xA_x$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.5	8.5	2.5	6.5	2.5	5.3	2.5	4.4	1.5	3.4	ns
Propagation Delay $_x\overline{LEBA}$ to $_xA_x$ $_x\overline{LEAB}$ to $_xB_x$	t_{PLH}, t_{PHL}		2.5	12.5	2.5	8.0	2.5	7.0	2.5	5.0	1.5	3.7	ns
Output Enable Time $_x\overline{OEBA}$ or $_x\overline{OEAB}$ to $_xA_x$ or $_xB_x$	t_{PZH}, t_{PZL}		2.0	12.0	2.0	9.0	2.0	8.0	2.0	5.4	1.5	4.8	ns
Output Disable Time (Note 17) $_x\overline{OEBA}$ or $_x\overline{OEAB}$ to $_xA_x$ or $_xB_x$	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	7.5	2.0	6.5	2.0	4.3	1.5	4.0	ns
Setup Time HIGH or LOW, $_xA_x$ or $_xB_x$ to $_x\overline{LEAB}$ or $_x\overline{LEBA}$	t_{SU}		3.0	-	2.0	-	2.0	-	2.0	-	1.0	-	ns
Hold Time HIGH or LOW, $_xA_x$ or $_xB_x$ to $_x\overline{LEAB}$ or $_x\overline{LEBA}$	t_H		2.0	-	2.0	-	2.0	-	1.5	-	1.0	-	ns
$_x\overline{LEAB}$ or $_x\overline{LEBA}$ Pulse Width LOW (Note 17)	t_W		5.0	-	5.0	-	5.0	-	3.0	-	3.0	-	ns
Output Skew (Note 18)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
6. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading, except as noted.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. Pins with Bus Hold are identified in the pin description.
9. This specification does not apply to bi-directional functionalities with Bus Hold.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
15. See test circuit and wave forms.
16. Minimum limits are guaranteed but not tested on Propagation Delays.
17. This parameter is guaranteed but not production tested.
18. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

19. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

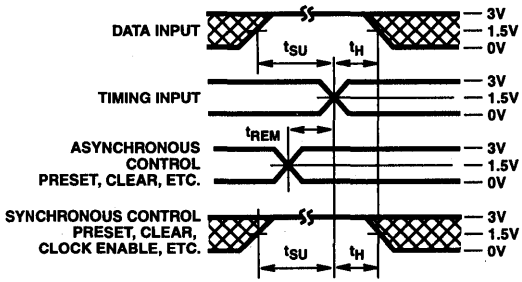


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

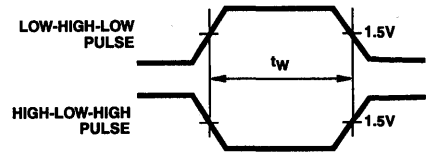


FIGURE 3. PULSE WIDTH

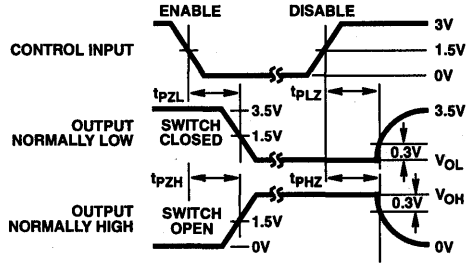


FIGURE 4. ENABLE AND DISABLE TIMING

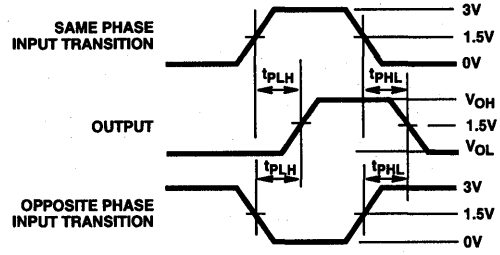


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16646T, CD74FCT162646T

December 1996

Fast CMOS 16-Bit Registered Transceivers

Features

- Advanced 0.6 micron CMOS Technology
- These Devices Are High-speed, Low Power Devices with High Current Drive
- V_{CC} = 5V ±10%
- Hysteresis on All Inputs
- CD74FCT16646T
  - High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA
  - Power Off Disable Outputs Permit "Live Insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- CD74FCT162646T
  - Balanced Output Drivers: ±24mA
  - Reduced System Switching Noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

Description

These devices are 16-bit registered transceivers organized as two independent 8-bit bus transceivers designed with three-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable control ($_X\overline{OE}$) and direction pins ($_X$DIR) to control the transceiver functions. The Select ($_X$SAB and $_X$SBA) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The CD74FCT16646T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162646T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

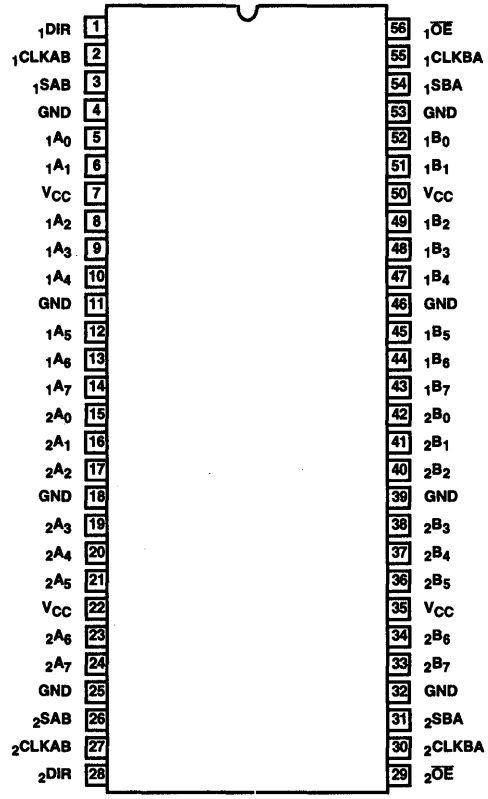
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16646ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16646ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16646CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16646CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16646DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16646DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16646ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16646ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16646TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16646TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162646ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162646ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162646CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162646CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162646DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162646DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162646ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162646ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162646TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162646TSM	-40 to 85	56 Ld SSOP	M56.300-P

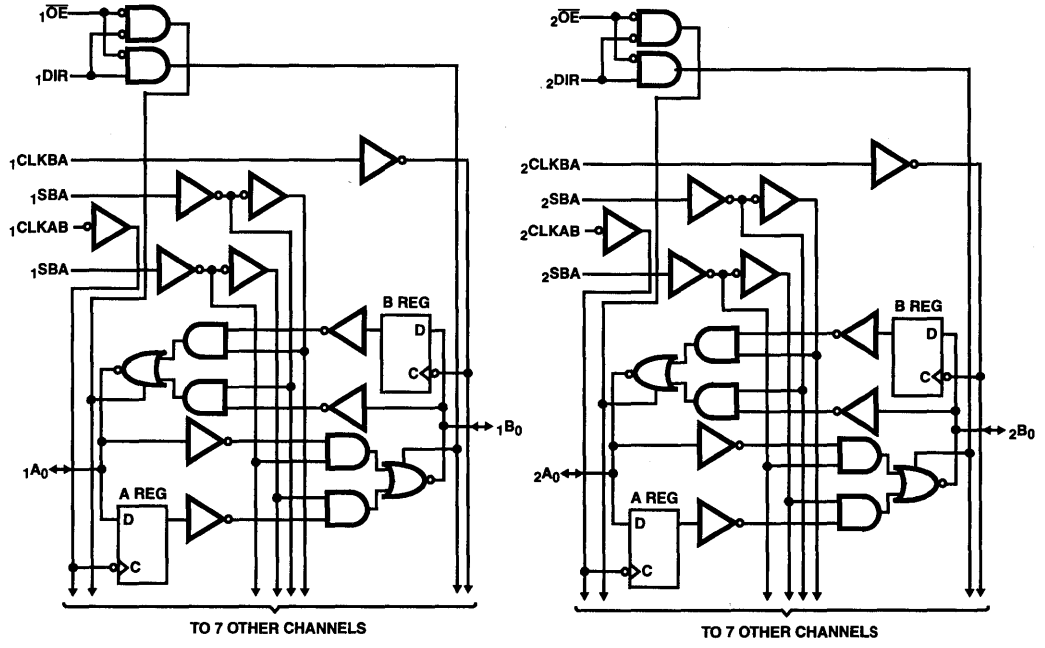
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74FCT16646T, CD74FCT162646T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION/OPERATION	INPUTS						(NOTE 2) DATA I/O	
	$_x\overline{OE}$	$_x$DIR	$_x$CLKAB	$_x$CLKBA	$_x$SAB	$_x$SBA	$_xA_x$	$_xB_x$
Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	H	X	↑	↑	X	X		
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	L	H	H or L	X	H	X		

NOTES:

1. The data output functions may be enabled or disabled by various signals at the $_x\overline{OE}$ or $_x$DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   ↑= LOW-to-HIGH transition

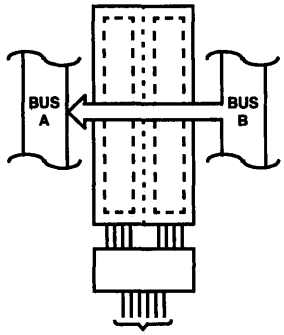


FIGURE 1. REAL-TIME TRANSFER BUS B TO A

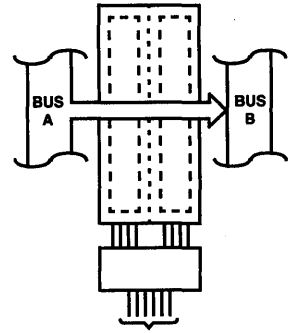


FIGURE 2. REAL-TIME TRANSFER BUS A TO B

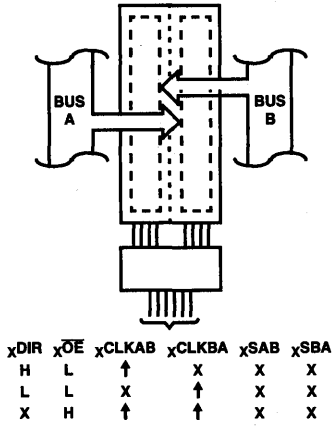


FIGURE 3. STORAGE FROM A AND/OR B

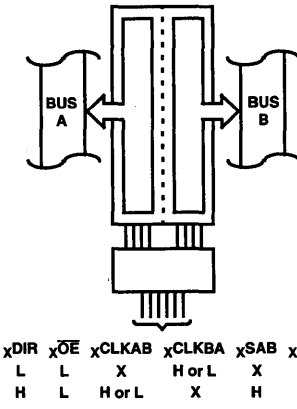


FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

Pin Descriptions

PIN NAME	DESCRIPTION
x^Ax	Data Register A Inputs Data Register B Outputs
x^Bx	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
xDIR, $x\overline{OE}$	Output Enable Inputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
TSSOP SOIC Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input, V_{CC} = Max	V_{IN} = Vcc	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O, V_{CC} = Max	V_{IN} = Vcc	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 7) V_{CC} = Max	V_{IN} = Vcc	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 7) V_{CC} = Max	V_{IN} = Vcc	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH} I_{BHL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
			V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 8)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 6), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 6), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
CD74FCT16646T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq$ 4.5V		-	-	100	µA
CD74FCT162646T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 6)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 6)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.12	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open xDIR = $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	75	120	µA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle xDIR = $x\overline{OE}$ = GND One Bit Toggling f_i = 5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.8	1.7 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.3	3.2 (Note 12)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle xDIR = $x\overline{OE}$ = GND 16 Bit Toggling f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.8	6.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	8.3	20.0 (Note 12)	mA

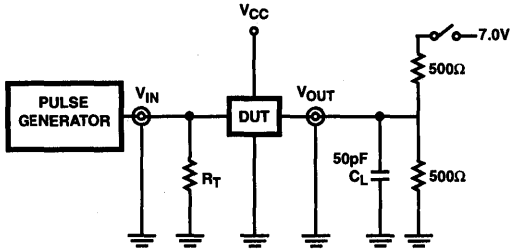
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T (NOTE 15) MIN	T MAX	AT (NOTE 15) MIN	AT MAX	CT (NOTE 15) MIN	CT MAX	DT (NOTE 15) MIN	DT MAX	ET (NOTE 15) MIN	ET MAX	UNITS
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	1.5	3.8	ns
Output Enable Time xDIR or $x\overline{OE}$ to Bus	t_{PZH}, t_{PZL}		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	1.5	4.8	ns
Output Disable Time (Note 16) xDIR or $x\overline{OE}$ to Bus	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	1.5	4.0	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	1.5	3.8	ns
Propagation Delay xSBA or xSAB to Bus	t_{PLH}, t_{PHL}		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	1.5	4.2	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}		4.0	-	2.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H		2.0	-	1.5	-	1.5	-	1.0	-	0.0	-	ns
Clock Pulse Width HIGH or LOW (Note 16)	t_W		6.0	-	5.0	-	5.0	-	3.0	-	3.0	-	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. Pins with Bus Hold are identified in the pin description.
8. This specification does not apply to bi-directional functionalities with Bus Hold.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 5. TEST CIRCUIT

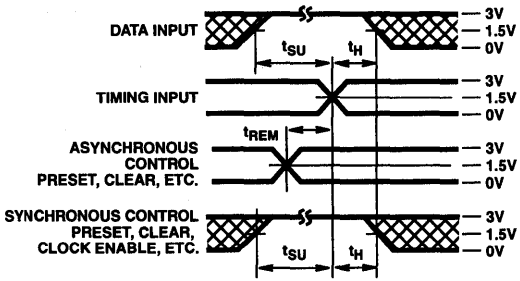


FIGURE 6. SETUP, HOLD, AND RELEASE TIMING

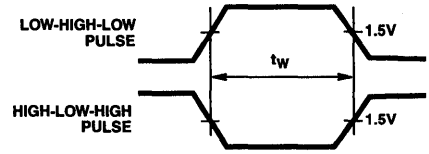


FIGURE 7. PULSE WIDTH

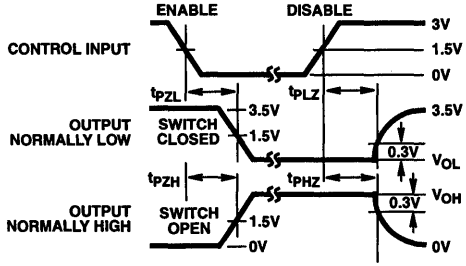


FIGURE 8. ENABLE AND DISABLE TIMING

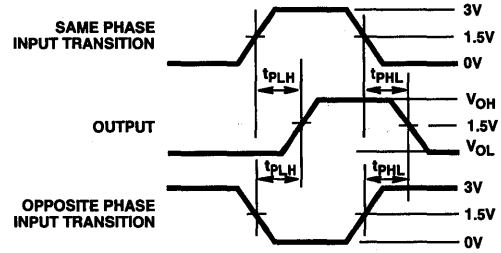


FIGURE 9. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16652T, CD74FCT162652T

December 1996

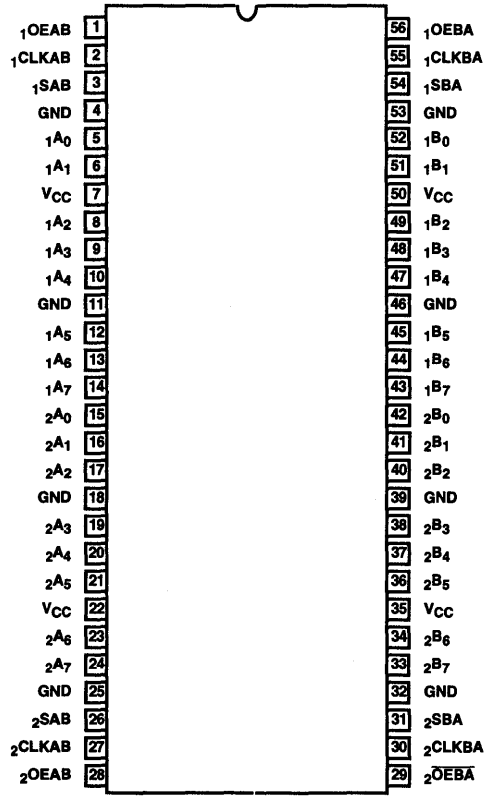
Fast CMOS 16-Bit Registered Transceivers

Features

- **These Devices are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16652T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162652T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**

Pinout

CD74FCT16652T, CD74FCT162652T
(SSOP, TSSOP)
TOP VIEW



Description

Harris' CD74FCT16652T and CD74FCT162652T are produced in an advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

These devices are 16-bit registered transceivers organized as two independent 8-bit bus transceivers designed with three-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable controls ($_X$OEAB and $_X\overline{OEBA}$) to control the transceiver functions. The Select ($_X$SAB and $_X$SBA) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The CD74FCT16652T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

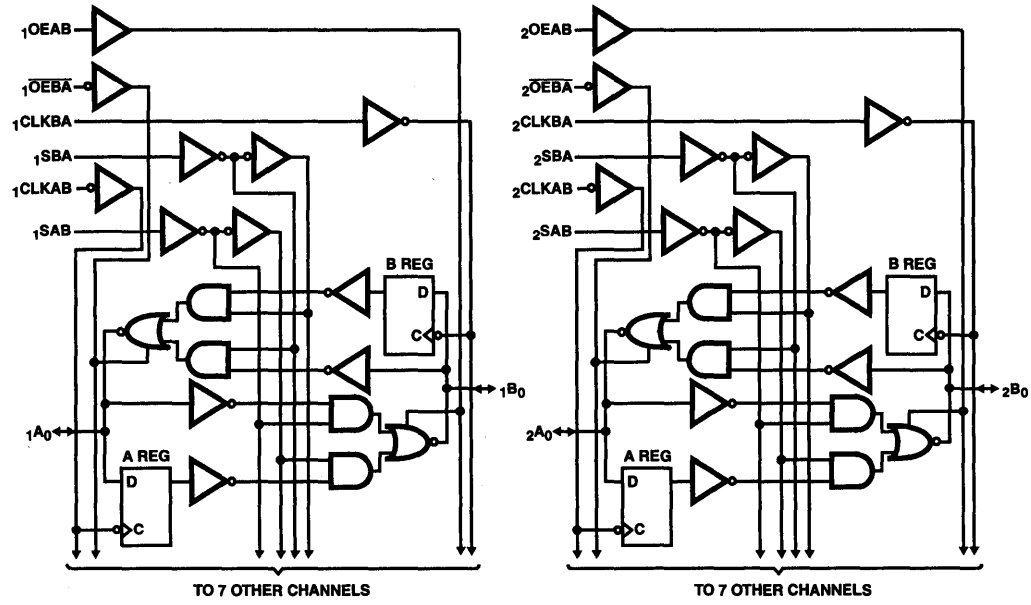
The CD74FCT162652T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16652ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16652ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16652CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16652CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16652TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16652TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162652ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162652ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162652CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162652CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162652DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162652ETSM	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162652TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162652TSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the varient in the tape and reel.

Functional Block Diagram



TRUTH TABLE

	INPUTS						DATA I/O	
FUNCTION/OPERATION	**xOEAB**	**xOEBA**	**xCLKAB**	**xCLKBA**	**xSAB**	**xSBA**	**xAx**	**xBx**
Isolation Store A and B Data	L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input
Store A, Hold B Store A in Both Registers	X H	H H	↑ ↑	H or L ↑	X X (Note 2)	X X	Input Input	Unspecified (Note 1) Output
Hold A, Store B Store B in Both Registers	L L	X L	H or L ↑	↑ ↑	X X	X X (Note 2)	Unspecified (Note 1) Output	Input Input
Real Time B Data to A Bus Stored B Data to A Bus	L L	L L	X X	X H or L	X X	L H	Output	Input
Real Time A Data to B Bus Stored A Data to B Bus	H H	H H	X H or L	X X	L H	X X	Input	Output
Stored A Data to B Bus and Stored B Data to A Bus	H	L	H or L	H or L	H	H	Output	Output

NOTES:

1. The data output functions may be enabled or disabled by various signals at the xOEAB or xOEBA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH transition

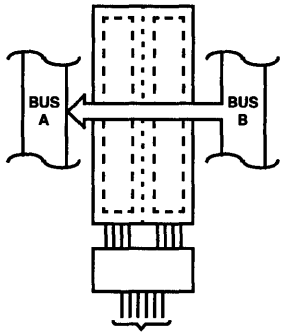


FIGURE 1. REAL-TIME TRANSFER BUS B TO A

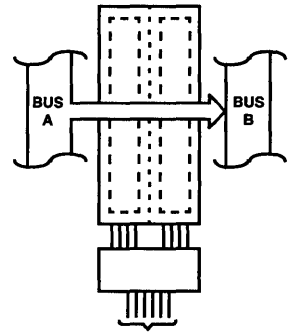


FIGURE 2. REAL-TIME TRANSFER BUS A TO B

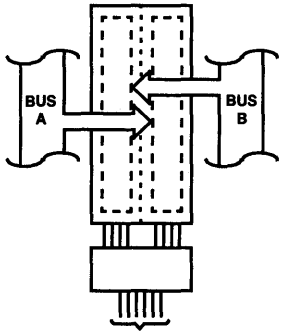


FIGURE 3. STORAGE FROM A AND/OR B

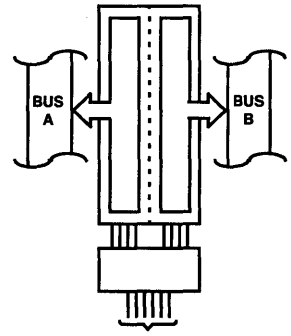


FIGURE 4. TRANSFER STORES DATA TO A AND/OR B

Pin Descriptions

PIN NAME	DESCRIPTION
$_xA_x$	Data Register A Inputs Data Register B Outputs
$_xB_x$	Data Register B Inputs Data Register A Outputs
$_x$CLKAB, $_x$CLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
$_x$OEAB, $_x\overline{OEBA}$	Output Enable Inputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . $-40^{o}C$ to $85^{o}C$
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^{o}C/W$)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^{o}C$ to $85^{o}C$, $V_{CC} = 5.0V \pm 10\%$							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = Vcc	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 6), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 6), V_{OUT} = 2.5		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
CD74FCT16652T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, $T_A = -40^{o}C$ to $85^{o}C$, $V_{CC} = 5.0V \pm 10\%$							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA
CD74FCT162652T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, $T_A = -40^{o}C$ to $85^{o}C$, $V_{CC} = 5.0V \pm 10\%$							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 6)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 6)		-60	-115	-150	mA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 7)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 7)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 8)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 9)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OEAB}$ = $x\overline{OEBA}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	75	120	µA/ MHz
Total Power Supply Current (Note 11)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{OEBA}$ = GND One Bit Toggling f_i = 5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.8	1.7 (Note 10)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.3	3.2 (Note 10)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz (xCLKBA) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{OEBA}$ = GND 16 Bits Toggling f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.8	6.5 (Note 10)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	8.3	22.0 (Note 10)	mA

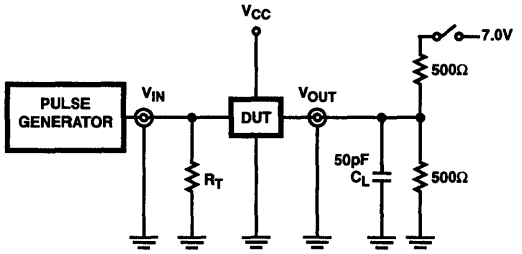
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	T (NOTE 13) MIN	T MAX	AT (NOTE 13) MIN	AT MAX	CT (NOTE 13) MIN	CT MAX	DT (NOTE 13) MIN	DT MAX	UNITS
Propagation Delay Bus to Bus	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	ns
Output Enable Time $_X$OEAB or $_X\overline{OEBA}$ to Bus	t_{PZH}, t_{PZL}		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	ns
Output Disable Time (Note 14) $_X$OEAB or $_X\overline{OEBA}$ to Bus	t_{PHZ}, t_{PLZ}		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	ns
Propagation Delay Clock to Bus	t_{PLH}, t_{PHL}		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	ns
Propagation Delay $_X$SBA or $_X$SAB to Bus	t_{PLH}, t_{PHL}		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	ns
Setup Time HIGH or LOW, Bus to Clock	t_{SU}		4.0	-	2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, Bus to Clock	t_H		2.0	-	1.5	-	1.5	-	1.0	-	ns
Clock Pulse Width HIGH or LOW (Note 14)	t_W		6.0	-	5.0	-	5.0	-	3.0	-	ns
Output Skew (Note 15)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. This parameter is determined by device characterization but is not production tested.
8. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
12. See test circuit and wave forms.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. This parameter is guaranteed but not production tested.
15. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

16. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 5. TEST CIRCUIT

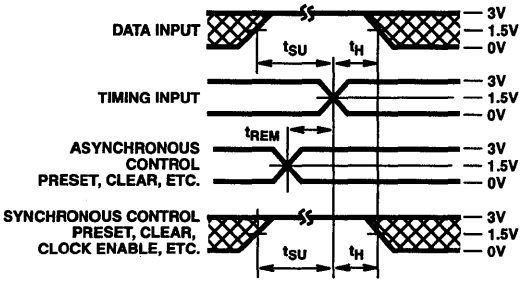


FIGURE 6. SETUP, HOLD, AND RELEASE TIMING

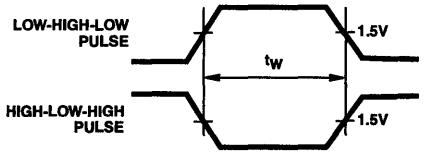


FIGURE 7. PULSE WIDTH

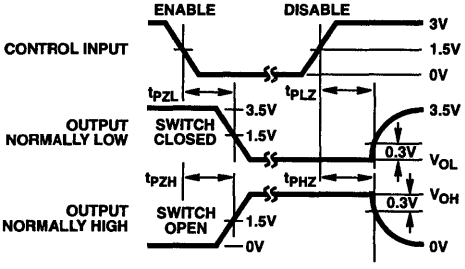


FIGURE 8. ENABLE AND DISABLE TIMING

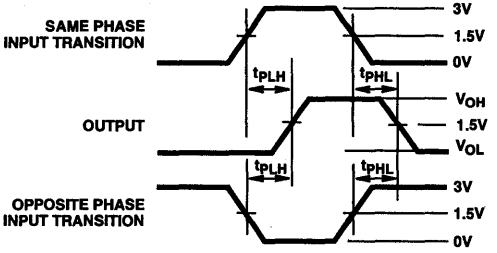


FIGURE 9. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16823T, CD74FCT162823T

December 1996

Fast CMOS 18-Bit Registers

Features

- **Advanced 0.6 micron CMOS Technology**
- **These Devices are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16823T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162823T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**

Description

These devices are 18-bit wide registers with clock enable ($_X\overline{CLKEN}$) and clear ($_X\overline{CLR}$) controls that make these devices especially suitable for parity bus interfacing in high-performance systems. The devices can be operated as two 9-bit registers or one 18-bit register using the control inputs. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The CD74FCT16823T output buffers are designed with a Power-Off disable function allowing "live insertion" of boards when the devices are used as backplane drives.

The CD74FCT162823T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16823ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16823BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16823CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16823DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16823ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16823ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162823ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162823ETSM	-40 to 85	56 Ld SSOP	M56.300-P

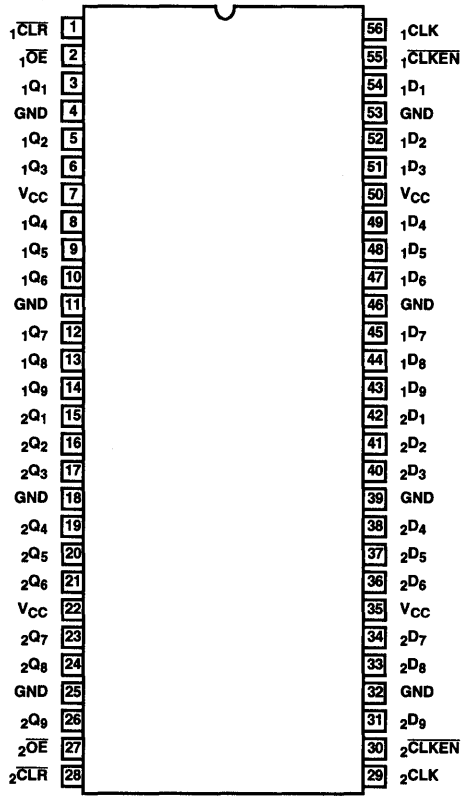
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

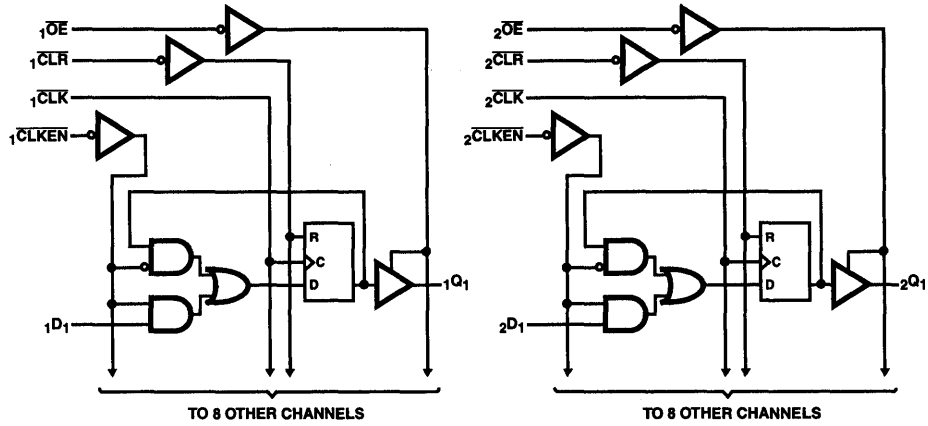
File Number **4189.2**

Pinout

CD74FCT16823T, CD74FCT162823T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS					OUTPUTS
	$_X\overline{OE}$	$_X\overline{CLR}$	$_X\overline{CLKEN}$	$_X$CLK	$_X$D$_X$	$_X$Q$_X$
High-Z	H	X	X	X	X	Z
Clear	L	L	X	X	X	L
Hold	L	H	H	X	X	Q (Note 2)
Load	H	H	L	↑	L	Z
	H	H	L	↑	H	Z
	L	H	L	↑	L	L
	L	H	L	↑	H	H

NOTES:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition
2. Output level before indicated steady-state input conditions were established.

Pin Descriptions

PIN NAME	DESCRIPTION
$_X$D$_X$	Data Inputs
$_X$CLK	Clock Inputs
$_X\overline{CLKEN}$	Clock Enable Inputs (Active LOW)
$_X\overline{CLR}$	Asynchronous Clear Inputs (Active LOW)
$_X\overline{OE}$	Output Enable Inputs (Active LOW)
$_X$Q$_X$	Three-State Outputs

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}, I_{BHL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
			V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 8)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 6), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 6), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
CD74FCT16823T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq 4.5V$		-	-	±100	µA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
CD74FCT162823T, CD74FCT162H823T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 6)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 6)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = $x\overline{CLKEN}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	75	120	µA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $x\overline{OE}$ = $x\overline{CLKEN}$ = GND f_i = 5MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.8	2.7	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.3	3.2	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $x\overline{OE}$ = $x\overline{CLKEN}$ = GND 18 Bits Toggling f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	4.2	7.1 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	9.2	22.1 (Note 12)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	AT (NOTE 15) MIN	AT MAX	BT (NOTE 15) MIN	BT MAX	CT (NOTE 15) MIN	CT MAX	DT (NOTE 15) MIN	DT MAX	ET (NOTE 15) MIN	ET MAX	UNITS
Propagation Delay xCLK to xQ_x	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	1.5	5.0	1.5	4.4	ns
		C_L = 300 pF (Note 16) R_L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	1.5	8.5	1.5	8.0	ns
Propagation Delay $x\overline{CLR}$ to xQ_x	t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	14.0	1.5	9.0	1.5	8.0	1.5	5.0	1.5	4.4	ns
Output Enable Time $x\overline{OE}$ to xQ_x	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	7.0	1.5	4.8	1.5	4.4	ns
		C_L = 300pF (Note 16) R_L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	1.5	10.0	1.5	9.0	ns

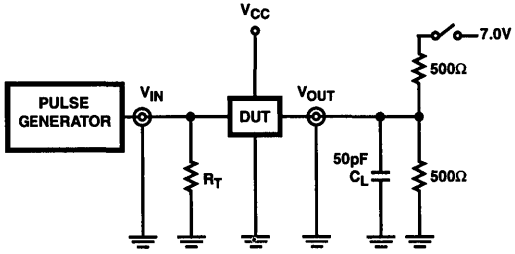
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	AT (NOTE 15) MIN	AT MAX	BT (NOTE 15) MIN	BT MAX	CT (NOTE 15) MIN	CT MAX	DT (NOTE 15) MIN	DT MAX	ET (NOTE 15) MIN	ET MAX	UNITS
Output Disable Time (Note 17) $_xOE$ to $_xQ_x$	t_{PHZ}, t_{PLZ}	C_L = 5pF (Note 16) R_L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	1.5	5.0	1.5	4.0	ns
		C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	1.5	5.0	1.5	4.0	ns
Setup Time HIGH or LOW, $_xD_x$ to $_x$CLK	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	3.0	-	3.0	-	3.0	-	1.5	-	ns
Hold Time HIGH or LOW, $_xD_x$ to $_x$CLK	t_H	C_L = 50pF R_L = 500Ω	2.0	-	1.5	-	1.5	-	1.5	-	0	-	ns
Setup Time HIGH or LOW, $_x\overline{CLKEN}$ to $_x$CLK	t_{SU}	C_L = 50pF R_L = 500Ω	4.0	-	3.0	-	3.0	-	3.0	-	2.5	-	ns
Hold Time HIGH or LOW, $_x\overline{CLKEN}$ to $_x$CLK	t_H	C_L = 50pF R_L = 500Ω	2.0	-	0	-	0	-	0	-	0	-	ns
$_x$CLK Pulse Width HIGH or LOW (Note 16)	t_W	C_L = 50pF R_L = 500Ω	7.0	-	6.0	-	6.0	-	6.0	-	3.0	-	ns
$_x\overline{CLR}$ Pulse Width LOW (Note 16)	t_W	C_L = 50pF R_L = 500Ω	6.0	-	6.0	-	6.0	-	6.0	-	3.0	-	ns
Recovery Time (Note 16) $_x\overline{CLR}$ to $_x$CLK	t_{REM}	C_L = 50pF R_L = 500Ω	6.0	-	6.0	-	6.0	-	6.0	-	3.0	-	ns
Output Skew (Note 17)	$t_{SK(O)}$	C_L = 50pF R_L = 500Ω	-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. Pins with Bus Hold are identified in the pin description.
8. This specification does not apply to bi-directional functionalities with Bus Hold.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \leq 50\Omega$; t_f, $t_r \leq 2.5$ns.

FIGURE 1. TEST CIRCUIT

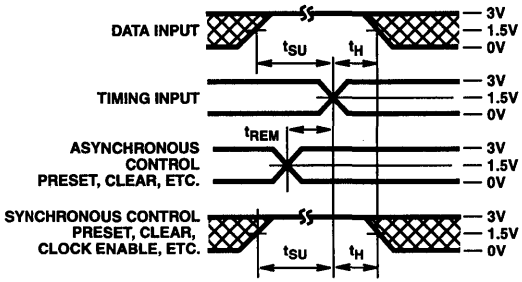


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

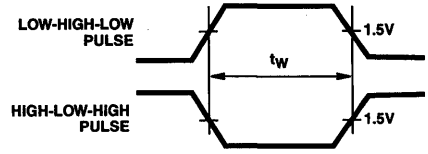


FIGURE 3. PULSE WIDTH

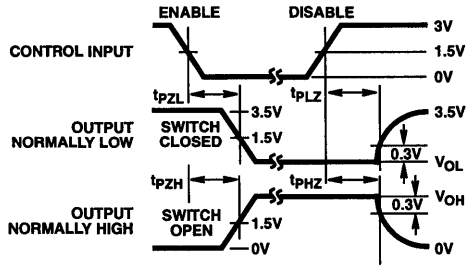


FIGURE 4. ENABLE AND DISABLE TIMING

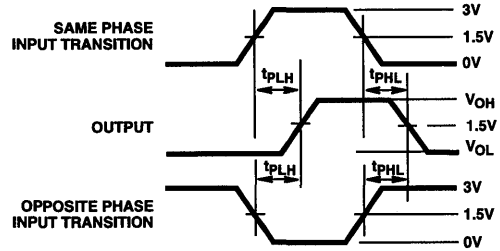


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16827T, CD74FCT162827T

December 1996

Fast CMOS 20-Bit Buffers

Features

- Advanced 0.6 micron CMOS Technology
- These Devices Are High-speed, Low Power Devices with High Current Drive
- V_{CC} = 5V ±10%
- Hysteresis on All Inputs
- CD74FCT16827T
  - High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA
  - Power Off Disable Outputs Permit "Live Insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- CD74FCT162827T
  - Balanced Output Drivers: ±24mA
  - Reduced System Switching Noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

Description

These devices are 20-bit wide bus drivers designed to provide buffering and high-performance bus interfacing for wide data/address paths or busses with parity. Two pair of nanded output enable controls allow the devices to be operated as two 10-bit buffers or as one 20-bit buffer. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The CD74FCT16827T output buffers are designed with a Power-Off disable function allowing "live insertion" of boards when the devices are used as backplane drives.

The CD74FCT162827T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

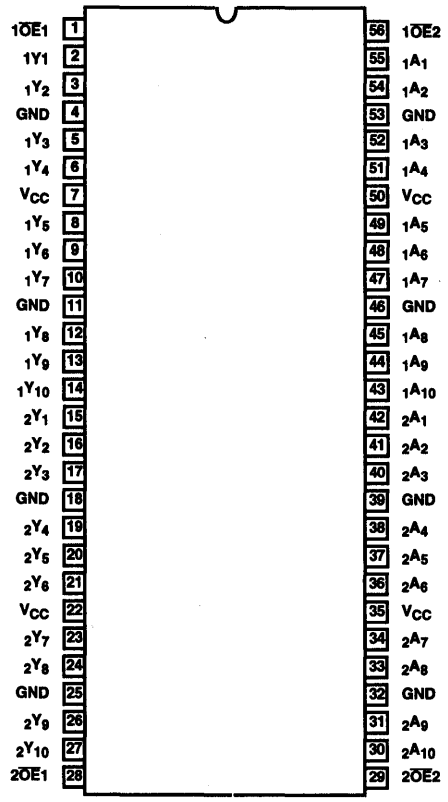
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16827ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16827BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16827CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16827DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16827ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16827ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162827ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162827ETSM	-40 to 85	56 Ld SSOP	M56.300-P

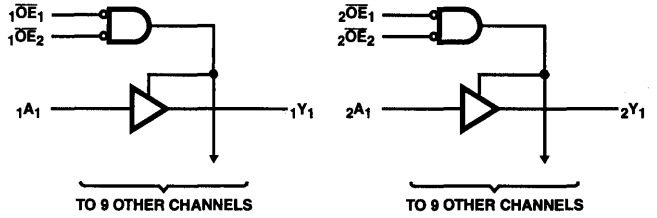
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74FCT16827T, CD74FCT162827T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$_x\overline{OE}_1$	$_x\overline{OE}_2$	$_xA_x$	$_xY_x$
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_x\overline{OE}_x$	Output Enable Inputs (Active LOW)
$_xA_x$	Data Inputs
$_xY_x$	Three-State Outputs

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 6) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 6) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 6) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 7)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 5), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
CD74FCT16827T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq$ 4.5V		-	-	±100	µA
CD74FCT162827T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 5)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 8)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 8)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 9)	-	0.5	2.5	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE1}$ = $\overline{OE2}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE1}$ = $\overline{OE2}$ = GND f_i = 5MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.6	1.5 (Note 11)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	0.9	2.3 (Note 11)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE1}$ = $\overline{OE2}$ = GND 8 Bits Toggling f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.0	5.5 (Note 11)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	8.0	20.5 (Note 11)	mA

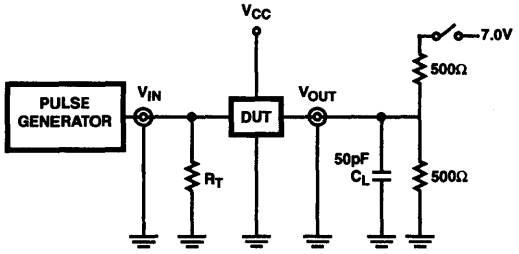
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 13) TEST CONDITIONS	AT		BT		CT		DT		ET		UNITS
			(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	(NOTE 14) MIN	MAX	
Propagation Delay xA_x to xY_x	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	5.0	1.5	4.4	1.5	3.8	1.5	3.2	ns
		C_L = 300pF (Note 15) R_L = 500Ω	1.5	15.0	1.5	13.0	1.5	10.0	1.5	7.5	1.5	7.0	ns
Output Enable Time $x\overline{OE}_x$ to xY_x	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	7.0	1.5	5.0	1.5	4.8	ns
		C_L = 300pF (Note 15) R_L = 500Ω	1.5	23.0	1.5	15.0	1.5	14.0	1.5	9.0	1.5	9.0	ns
Output Disable Time (Note 15) $\overline{OE}_N$ to Y_N	t_{PHZ}, t_{PLZ}	C_L = 5pF R_L = 500Ω	1.5	9.0	1.5	6.0	1.5	5.7	1.5	4.3	1.5	4.0	ns
		C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	7.0	1.5	6.0	1.5	4.3	1.5	4.0	ns
Output Skew (Note 16)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. Pins with Bus Hold are identified in the pin description.
7. This specification does not apply to bi-directional functionalities with Bus Hold.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
13. See test circuit and wave forms.
14. Minimum limits are guaranteed but not tested on Propagation Delays.
15. This parameter is guaranteed but not production tested.
16. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

17. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

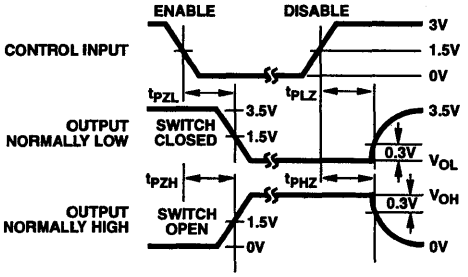


FIGURE 2. ENABLE AND DISABLE TIMING

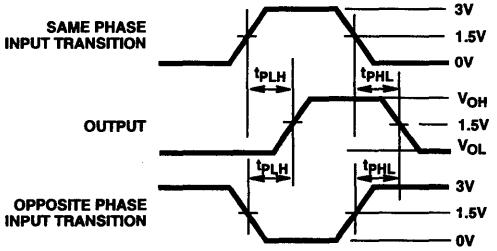


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16841T, CD74FCT162841T

December 1996

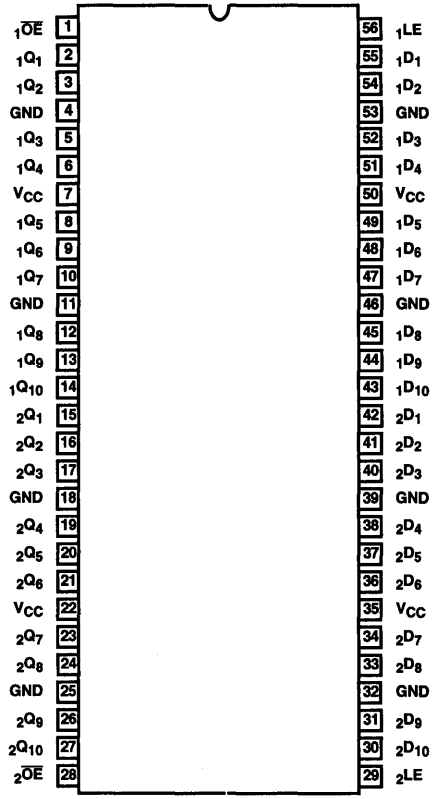
Fast CMOS 20-Bit Transparent Latches

Features

- **These Devices are High-speed, Low Power Devices with High Current Drive**
- **V_{CC} = 5V ±10%**
- **Hysteresis on All Inputs**
- **CD74FCT16841T**
  - **High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA**
  - **Power Off Disable Outputs Permit "Live Insertion"**
  - **Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C**
- **CD74FCT162841T**
  - **Balanced Output Drivers: ±24mA**
  - **Reduced System Switching Noise**
  - **Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C**

Pinouts

CD74FCT16841T, CD74FCT162841T
(SSOP, TSSOP)
TOP VIEW



Description

Harris' CD74FCT16841T and CD74FCT162841T are produced in an advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

These devices are 20-bit wide transparent latches designed to provide temporary storage of data and can be used as I/O ports, memory address latches, and bus drivers. The Output Enable and Latch Enable controls allow the devices to be operated as two 10-bit latches or one 20-bit latch. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

The output buffers are especially designed for driving high-capacitance loads and low impedance backplanes and include a Power-Off Disable function allowing "live insertion" of boards when the devices are used as backplane drivers.

The CD74FCT162841T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications..

Ordering Information

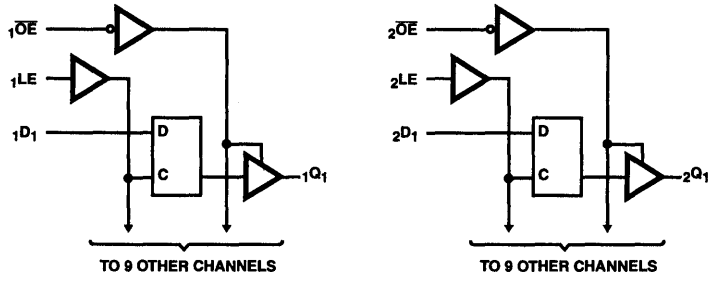
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16841ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16841ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16841BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16841BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16841CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16841CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162841ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162841ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162841BTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162841BTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162841CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162841CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16841DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16841DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16841ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16841ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162841DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162841DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162841ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162841ETSM	-40 to 85	56 Ld SSOP	M56.300-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4204.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$_xD_x$	$_xLE$	$_x\overline{OE}$	$_xQ_x$
H	H	L	H
L	H	L	L
X	L	L	Q (Note 2)
X	X	H	Z

NOTES:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
2. Output level before the $_xLE$ HIGH-to-LOW Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$_xD_x$	Data Inputs
$_xLE$	Latch Enable Input (Active LOW)
$_x\overline{OE}$	Output Enable Input (Active LOW)
$_xQ_x$	Three-State Outputs

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
TSSOP Package	85
SSOP Package	70

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 6), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 6), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
CD74FCT16841T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or V_{OUT} ≤ 4.5V		-	-	±100	µA
CD74FCT162841T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 6)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 6)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 7)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
Output Capacitance (Note 7)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 8)	-	0.5	2.5	mA
Supply Current per Input per MHz (Note 9)	I_{CCD}	V_{CC} = Max, Outputs Open $\overline{OE}$ = GND, LE = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 11)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND; LE = V_{CC} f_i = 5MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	1.7	4.0 (Note 10)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	2.0	5.0 (Note 10)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $\overline{OE}$ = GND; LE = V_{CC} Eight Bits Toggling f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.2	6.5 (Note 10)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	5.2	14.5 (Note 10)	mA

Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	AT (NOTE 13) MIN	AT MAX	BT (NOTE 13) MIN	BT MAX	CT (NOTE 13) MIN	CT MAX	DT (NOTE 13) MIN	DT MAX	ET (NOTE 13) MIN	ET MAX	UNITS
Propagation Delay $_xD_x$ to $_xQ_x$ (LE = HIGH)	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	1.5	4.2	1.5	3.4	ns
		C_L = 300pF (Note 14) R_L = 500Ω	1.5	13.0	1.5	13.0	1.5	13.0	1.5	13.0	1.5	7.5	ns
Propagation Delay $_xLE$ to $_xQ_x$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	1.5	4.0	1.5	3.7	ns
		C_L = 30pF (Note 14) R_L = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0	1.5	8.0	1.5	7.5	ns
Output Enable Time $_x\overline{OE}$ to $_xQ_x$	t_{PZH}, t_{PZL}	C_L = 50pF R_L = 500Ω	1.5	11.5	1.5	8.0	1.5	6.5	1.5	4.8	1.5	4.4	ns
		C_L = 300pF (Note 15) R_L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	1.5	9.0	1.5	9.0	ns
Output Disable Time (Note 14) $_x\overline{OE}$ to $_xQ_x$	t_{PHZ}, t_{PLZ}	C_L = 5pF (Note 14) R_L = 500Ω	1.5	7.0	1.5	6.0	1.5	5.7	1.5	4.0	1.5	3.6	ns
		C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	1.5	5.4	1.5	3.6	ns

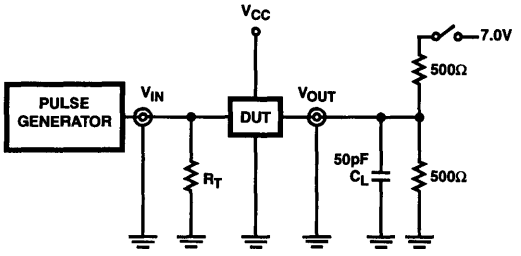
Switching Specifications Over Operating Range (Continued)

PARAMETER	SYMBOL	(NOTE 12) TEST CONDITIONS	AT (NOTE 13) MIN	AT MAX	BT (NOTE 13) MIN	BT MAX	CT (NOTE 13) MIN	CT MAX	DT (NOTE 13) MIN	DT MAX	ET (NOTE 13) MIN	ET MAX	UNITS
Setup Time HIGH or LOW, $_XD_X$ to $_X$LE	t_{SU}	C_L = 50pF, R_L = 500Ω	2.5	-	2.5	-	2.5	-	1.0	-	1.0	-	ns
Hold Time HIGH or LOW, $_XD_X$ to $_X$LE	t_H		2.5	-	2.5	-	2.5	-	1.0	-	1.0	-	ns
$_X$LE Pulse Width HIGH (Note 14)	t_W		4.0	-	4.0	-	4.0	-	4.0	-	3.0	-	ns
Output Skew (Note 15)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. This parameter is determined by device characterization but is not production tested.
8. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
10. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
11. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
12. See test circuit and wave forms.
13. Minimum limits are guaranteed but not tested on Propagation Delays.
14. This parameter is guaranteed but not production tested.
15. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

16. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

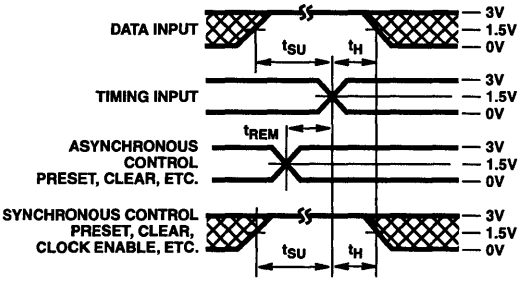


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

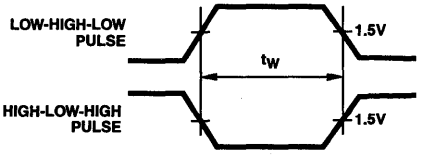


FIGURE 3. PULSE WIDTH

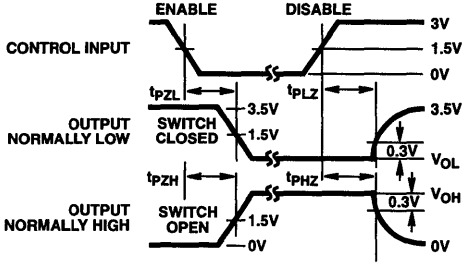


FIGURE 4. ENABLE AND DISABLE TIMING

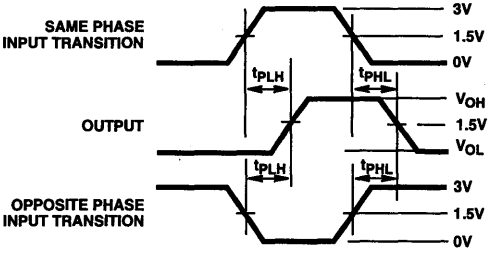


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT16952T, CD74FCT162952T

December 1996

Fast CMOS 16-Bit Registered Transceivers

Features

- Advanced 0.6 micron CMOS Technology
- These Devices Are High-speed, Low Power Devices with High Current Drive
- V_{CC} = 5V ±10%
- Hysteresis on All Inputs
- CD74FCT16952T
  - High Output Drive: I_{OH} = -32mA; I_{OL} = 64mA
  - Power Off Disable Outputs Permit "Live Insertion"
  - Typical V_{OLP} (Output Ground Bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C
- CD74FCT162952T
  - Balanced Output Drivers: ±24mA
  - Reduced System Switching Noise
  - Typical V_{OLP} (Output Ground Bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

Description

These devices are 16-bit registered transceivers organized with two sets of eight D-type latches with separate input and output controls for each set. For data flow from A-to-B, for example, the A-to-B Enable ($_X\overline{CEAB}$) input must be LOW in order to enter data from $_XA_X$. The data present on the A port will be clocked on the B register when $_X$CLKAB toggles from LOW-to-HIGH. The $_X\overline{OEAB}$ control performs the output enable function on the B port. Control of data from B-to-A is similar, but uses the $_X\overline{CEBA}$, xCLKBA, and $_X\overline{OEBA}$ inputs. By connecting the control pins of the two independent transceivers together, a full 16-bit operation can be achieved. The output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT16952T output buffers are designed with a Power-Off disable allowing "live insertion" of boards when used as backplane drivers.

The CD74FCT162952T has ±24mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT16952ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16952ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16952TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16952TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16952CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16952CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16952DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16952DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT16952ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT16952ETSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162952ATMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162952ATSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162952TMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162952TSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162952CTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162952CTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162952DTMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162952DTSM	-40 to 85	56 Ld SSOP	M56.300-P
CD74FCT162952ETMT	-40 to 85	56 Ld TSSOP	M56.240-P
CD74FCT162952ETSM	-40 to 85	56 Ld SSOP	M56.300-P

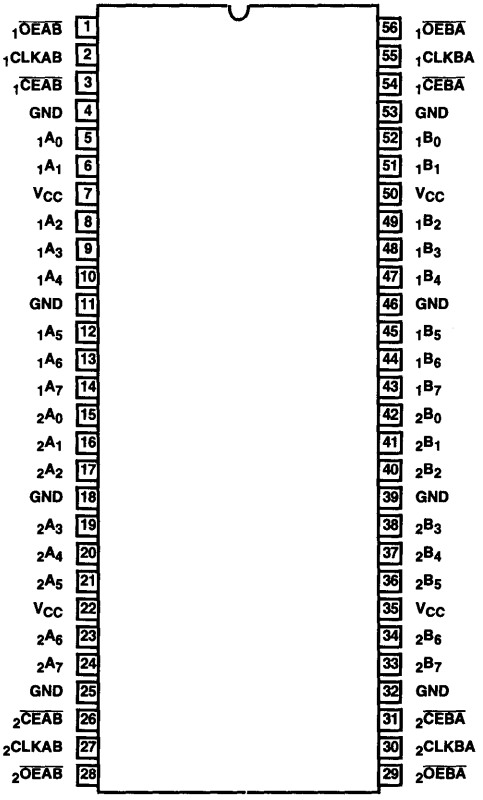
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

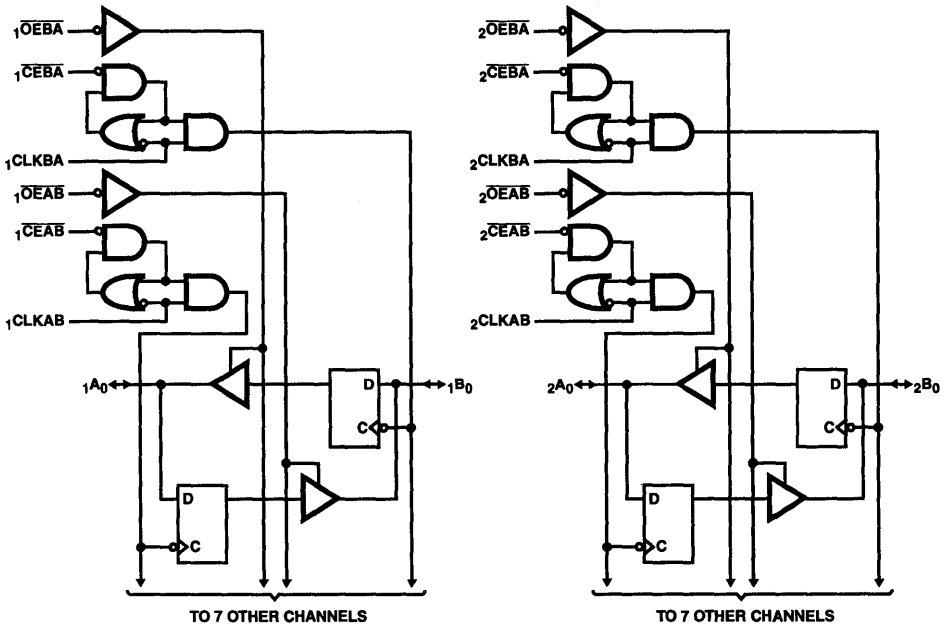
File Number **4191.1**

Pinout

CD74FCT16952T, CD74FCT162952T
(SSOP, TSSOP)
TOP VIEW



Functional Block Diagram



TRUTH TABLE (NOTES 1, 2)

INPUTS				OUTPUTS
$_X\overline{CEAB}$	$_X$CLKAB	$X\overline{OEAB}$	$_XA_X$	$_XB_X$
H	X	L	X	B (Note 3)
X	L	L	X	B (Note 3)
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	High Z

NOTES:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care or Irrelevant
   ↑ = LOW-to-HIGH Transition
   Z = High Impedance
2. A-to-B data flow shown. B-to-A flow control is the same, except using $_X\overline{CEBA}$, $_X$CLKBA, and $_X\overline{OEBA}$.
3. Level of B before the indicated steady-state input conditions were established.

Pin Descriptions

PIN NAME	DESCRIPTION
$_X\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$_X\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$_X\overline{CEAB}$	A-to-B Clock Enable Input (Active LOW)
$_X\overline{CEBA}$	B-to-A Clock Enable Input (Active LOW)
$_X$CLKAB	A-to-B Clock Input
$_X$CLKBA	B-to-A Clock Input
$_XA_X$	A-to-B Data Inputs or B-to-A Three-State Outputs
$_XB_X$	B-to-A Data Inputs or A-to-B Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage ..... -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range ..... -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only ..... -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only ..... -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
TSSOP Package 85
SSOP Package 70
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Standard I/O, V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 8) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input HIGH Current	I_{IH}	Bus Hold I/O (Note 8) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Standard I/O, V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 8) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Input LOW Current	I_{IL}	Bus Hold I/O (Note 8) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 8) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 10)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 7), V_{OUT} = GND		-80	-140	-200	mA
Output Drive Current	I_O	V_{CC} = Max (Note 7), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS		MIN	(NOTE 6) TYP	MAX	UNITS
CD74FCT16952T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.0mA	2.5	3.5	-	V
			I_{OH} = -15.0mA	2.4	3.5	-	V
			I_{OH} = -32.0mA	2.0	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	-	0.2	0.55	V
Power Down Disable	I_{OFF}	V_{CC} = 0V, V_{IN} or $V_{OUT} \leq$ 4.5V		-	-	±100	µA
CD74FCT162952T OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -24.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	-	0.3	0.55	V
Output LOW Current	I_{ODL}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 7)		60	115	150	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL}, V_{OUT} = 1.5V (Note 7)		-60	-115	-150	mA
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 10)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 10)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 11)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 12)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OEAB}$ or $x\overline{OEBA}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	75	120	µA/ MHz
Total Power Supply Current (Note 14)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{CEBA}$ = V_{CC} One Bit Toggling, f_i = 5MHz	V_{IN} = V_{CC} V_{IN} = GND	-	0.8	1.7 (Note 13)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.3	3.2 (Note 13)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz (xCLKAB) 50% Duty Cycle $x\overline{OEAB}$ = $x\overline{CEAB}$ = GND $x\overline{CEBA}$ = V_{CC} 16 Bits Toggling, f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.8	6.5 (Note 13)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	8.3	20.5 (Note 13)	mA

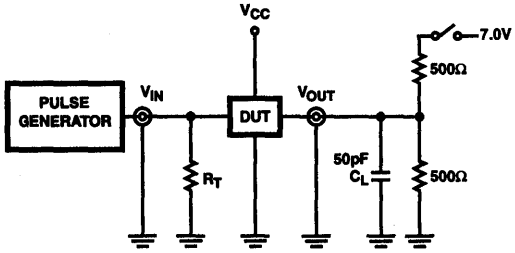
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 16) TEST CONDITIONS	AT (NOTE 17) MIN	AT MAX	CT (NOTE 17) MIN	CT MAX	DT (NOTE 17) MIN	DT MAX	ET (NOTE 17) MIN	ET MAX	UNITS
Propagation Delay $_X$CLKAB, $_X$CLKBA to $_X$B$_X$, $_X$A$_X$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	6.3	2.0	4.4	1.5	3.7	ns
Output Enable Time $_X\overline{OEBA}$, $_X\overline{OEAB}$ to $_X$A$_X$, $_X$B$_X$	t_{PZH}, t_{PZL}		1.5	10.5	1.5	7.0	1.5	4.8	1.5	4.4	ns
Output Disable Time (Note 18) $_X\overline{OEBA}$, $_X\overline{OEAB}$ to $_X$A$_X$, $_X$B$_X$	t_{PHZ}, t_{PLZ}		1.5	10.0	1.5	6.5	1.5	4.0	1.5	4.0	ns
Setup Time HIGH or LOW, $_X$A$_X$, $_X$B$_X$ to $_X$CLKAB, $_X$CLKBA	t_{SU}		2.5	-	2.5	-	2.0	-	1.5	-	ns
Hold Time HIGH or LOW, $_X$A$_X$, $_X$B$_X$ to $_X$CLKAB, $_X$CLKBA	t_H		2.0	-	1.5	-	1.0	-	0.0	-	ns
Setup Time HIGH or LOW, $_X\overline{CEAB}$, $_X\overline{CEBA}$ to $_X$CLK-AB, $_X$CLKBA	t_{SU}		3.0	-	3.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, $_X\overline{CEAB}$, $_X\overline{CEBA}$ to $_X$CLK-AB, $_X$CLKBA	t_H		2.0	-	2.0	-	1.5	-	0.0	-	ns
Pulse Width HIGH (Note 18) or LOW, $_X$CLKAB or $_X$CLKBA	t_W		3.0	-	3.0	-	3.0	-	3.0	-	ns
Output Skew (Note 19)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

5. For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
6. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading, except as noted.
7. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
8. Pins with Bus Hold are identified in the pin description.
9. This specification does not apply to bi-directional functionalities with Bus Hold.
10. This parameter is determined by device characterization but is not production tested.
11. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
12. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
13. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
14. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
15. See test circuit and wave forms.
16. Minimum limits are guaranteed but not tested on Propagation Delays.
17. This parameter is guaranteed but not production tested.
18. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

19. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

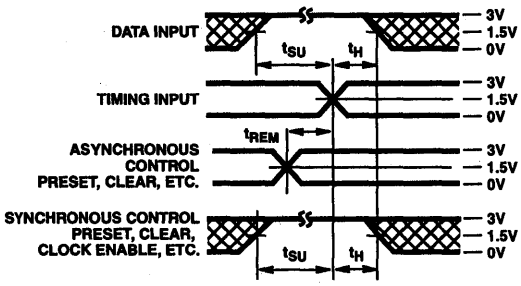


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

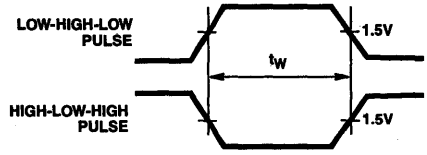


FIGURE 3. PULSE WIDTH

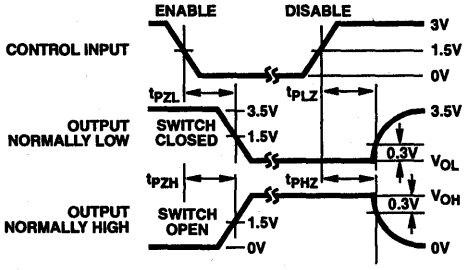


FIGURE 4. ENABLE AND DISABLE TIMING

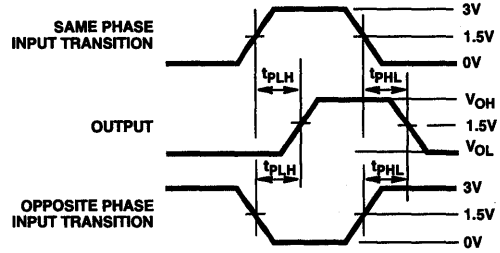


FIGURE 5. PROPAGATION DELAY

CMOS LOGIC 6

DOUBLE DENSITY 5V FCT CMOS LOGIC QUIET SERIES

PAGES

Selection Guide 6-2

Data Sheets

CD74FCT162Q244T Fast, Low Noise CMOS 16-Bit Buffer/Line Driver 6-3

CD74FCT162Q245T Fast CMOS 16-Bit Bidirectional Transceiver 6-8

CD74FCT162Q373T Fast CMOS 16-Bit Transparent Latch 6-14

CD74FCT162Q374T Fast CMOS 16-Bit Register (Three-State) 6-20

Selection Guide

DOUBLE DENSITY 5V FCT CMOS LOGIC QUIET SERIES

PART NUMBER	DESCRIPTION	SPEED GRADE (X)					FILE #
		BLANK	A	C	D	E	
CD74FCT162Q244T	Fast, Low Noise CMOS 16-Bit Buffer/Line Driver	X	X	X	X	X	4280
CD74FCT162Q245T	Fast CMOS 16-Bit Bidirectional Transceiver	X	X	X	X	X	4277
CD74FCT162Q373T	Fast CMOS 16-Bit Transparent Latch	X	X	X	X	X	4278
CD74FCT162Q374T	Fast CMOS 16-Bit Register (Three-State)	X	X	X	X	X	4279

HARRIS SEMICONDUCTOR CD74FCT162Q244T

PRELIMINARY

December 1996

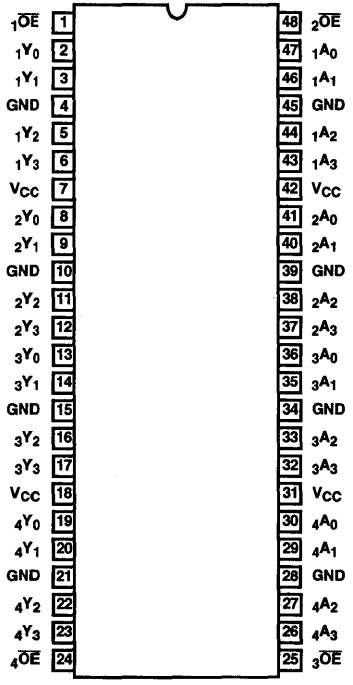
Fast, Low Noise CMOS 16-Bit Buffer/Line Driver

Features

- **Advanced 0.6 micron CMOS Technology**
- **V_{CC} = 5V ±10%**
- **Balanced Output Drivers: ±12mA**
- **Output Impedance 35Ω (Typical)**
- **Typical V_{OLP} (Output Ground Bounce) < 0.5V at V_{CC} = 5V, T_A = 25°C**
- **Bus Hold Retains Last Active Bus State During Three-State**
- **Hysteresis on All Inputs**

Pinout

CD74FCT162Q244T
(SSOP, TSSOP)
TOP VIEW



Description

The CD74FCT162Q244T is a non-inverting 16-bit buffer/line driver designed for bus interface applications where low noise operation is essential.

The CD74FCT162Q244T is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This device features a typical output impedance of 35Ω, eliminating the need for external terminating resistors for most bus interface applications. This noise suppression benefit is designated by the letter "Q" (for quiet) in the part number.

The CD74FCT162Q244T also features "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pullup/down resistors.

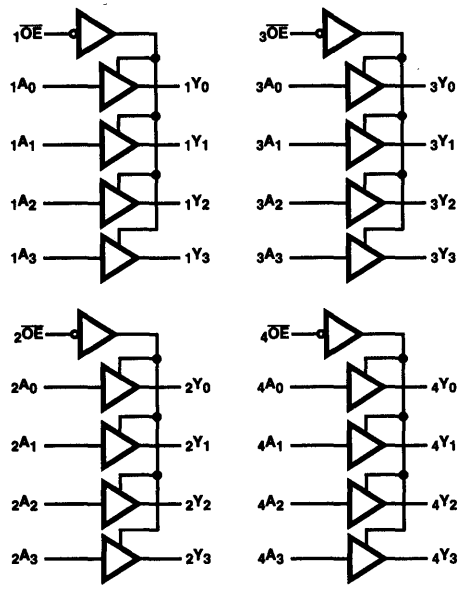
This high-speed, low power device also features a flow-through organization for ease of board layout. These devices are designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT162Q244TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q244ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q244CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q244DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q244ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q244TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q244ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q244CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q244DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q244ETSM	-40 to 85	48 Ld SSOP	M48.300-P

File Number **4280**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$_xOE$	$_xA_x$	$_xY_x$
L	L	L
L	H	H
H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   NC = No Change
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_xOE$	Three-State Output Enable Inputs (Active LOW)
$_xA_x$	Inputs (Note 2)
$_xY_x$	Three-State Outputs
GND	Ground
V_{CC}	Power

NOTE:

2. For the CD74FCT162Q244T, these pins have "Bus Hold". All other pins are standard, outputs, or I/Os.

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
	I_{BHL}		V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 9)	I_{OZH}	V_{CC} = Max	$V_{OUT} = V_{CC}$	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output Drive Current	I_O	V_{CC} = Max (Note 6), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output LOW Current	I_{ODL}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 6)		36	-	-	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 6)		-100	-166	-200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -12.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 12.0mA	-	0.4	0.55	V
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	1.5	mA

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	0.6	1.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	.9	2.3 (Note 12)	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	2.4	4.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.4	16.5 (Note 12)	mA

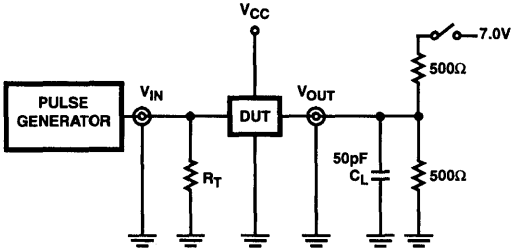
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T (NOTE 15) MIN	T MAX	AT (NOTE 15) MIN	AT MAX	CT (NOTE 15) MIN	CT MAX	DT (NOTE 15) MIN	DT MAX	ET (NOTE 15) MIN	ET MAX	UNITS
Propagation Delay xA_X to xY_X	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	1.5	3.8	1.5	3.2	ns
Output Enable Time $x\overline{OE}$ to xA_X or xY_X	t_{PZH}, t_{PZL}		1.5	8.0	1.5	6.2	1.5	5.8	1.5	4.8	1.5	4.4	ns
Output Disable Time (Note 16) $x\overline{OE}$ to xA_X or xY_X	t_{PHZ}, t_{PLZ}		1.5	7.0	1.5	5.6	1.5	5.2	1.5	4.0	1.5	4.0	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. Pins with Bus Hold are identified in the pin description.
8. This specification does not apply to bi-directional functionalities with Bus Hold.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

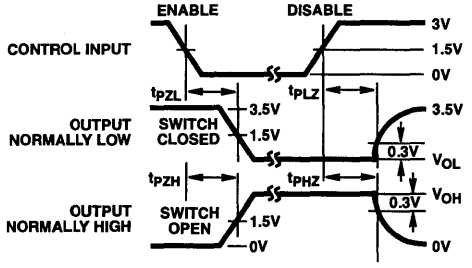


FIGURE 2. ENABLE AND DISABLE TIMING

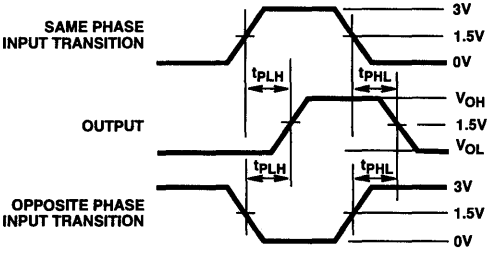


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR CD74FCT162Q245T

PRELIMINARY

December 1996

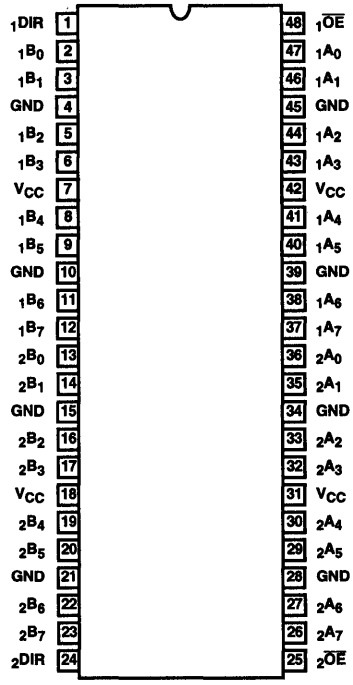
Fast CMOS 16-Bit Bidirectional Transceiver

Features

- **Advanced 0.6 micron CMOS Technology**
- **Balanced Output Drivers: ±12mA**
- **Output Impedance 35Ω (Typical)**
- **Typical V_{OLP} (Output Ground Bounce) < 0.5V at V_{CC} = 5V, T_A = 25°C**
- **Bus Hold Retains Last Active Bus State During Three-State**
- **Hysteresis on All Inputs**

Pinout

CD74FCT162Q245T
(SSOP, TSSOP)
TOP VIEW



Description

The CD74FCT162Q245T is a 16-bit bidirectional transceiver designed for asynchronous two-way communication between data buses. The direction control input pin ($_X$DIR) determines the direction of data flow through the bidirectional transceiver. The Direction and Output Enable controls are designed to operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The output enable ($\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

The CD74FCT162Q245T is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This device features a typical output impedance of 35Ω, eliminating the need for external terminating resistors for most bus interface applications. This noise suppression benefit is designated by the letter "Q" (for quiet) in the part number.

The CD74FCT162Q245T also features "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pullup/down resistors.

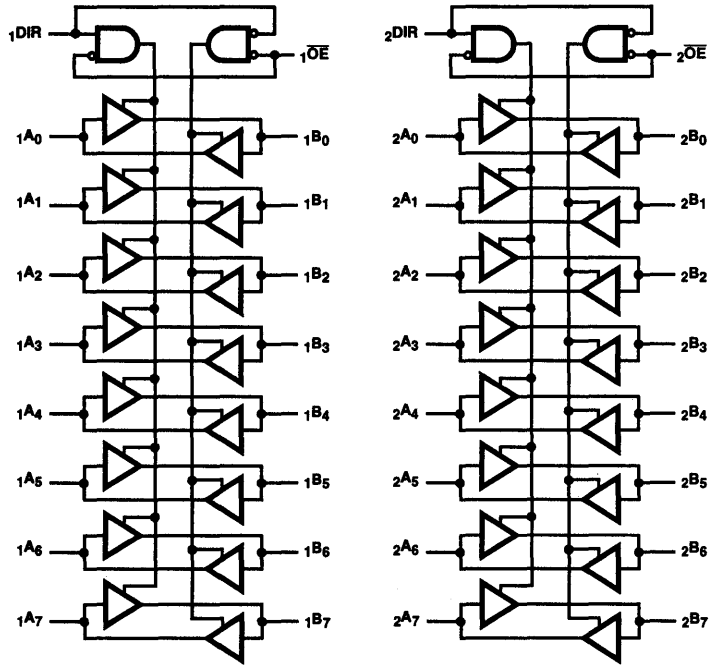
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT162Q245TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q245ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q245CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q245DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q245ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q245TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q245ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q245CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q245DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q245ETSM	-40 to 85	48 Ld SSOP	M48.300-P

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4277**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$_xOE$	$_x$DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_xOE$	Three-State Output Enable Inputs (Active LOW)
$_x$DIR	Direction Control Input
$_xA_x$	Side A Inputs or Three-State Outputs (Note 2)
$_xB_x$	Side B Inputs or Three-State Outputs (Note 2)
GND	Ground
V_{CC}	Power

NOTE:

2. For the CD74FCT162Q245T, these pins have "Bus Hold". All other pins are standard, outputs, or I/Os.

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
TSSOP Package 94
SSOP Package 76
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH} I_{BHL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
			V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 9)	I_{OZH}	V_{CC} = Max	$V_{OUT} = V_{CC}$	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output Drive Current	I_O	V_{CC} = Max (Note 6), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output LOW Current	I_{ODL}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 6)		36	-	-	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 6)		-100	-166	-200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -12.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 12mA	-	0.4	0.55	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = xDIR = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$= xDIR = GND One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	0.6	1.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	0.9	2.3 (Note 12)	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = xDIR = GND 16 Bits Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	2.4	4.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.4	16.5 (Note 12)	mA

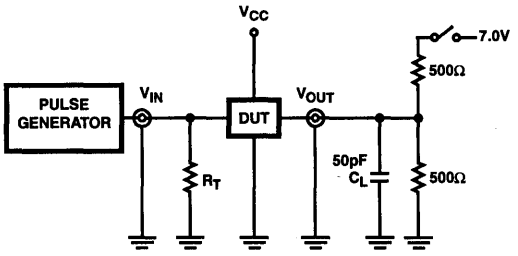
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T		AT		CT		DT		ET		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 16) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay A to B, B to A	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	1.5	3.8	1.5	3.2	ns
Output Enable Time $x\overline{OE}$ to A or B	t_{PZH}, t_{PZL}		1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.0	1.5	4.4	ns
Output Disable Time (Note 17) $x\overline{OE}$ to A or B	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	1.5	4.0	ns
Output Enable Time xDIR to A or B (Note 16)	t_{PZH}, t_{PZL}		1.5	9.5	1.5	6.2	1.5	5.8	1.5	5.0	1.5	4.8	ns
Output Disable Time xDIR to A or B (Note 16)	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.0	1.5	4.8	1.5	4.3	1.5	4.0	ns
Output Skew(17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. Pins with Bus Hold are identified in the pin description.
8. This specification does not apply to bi-directional functionalities with Bus Hold.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design..

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

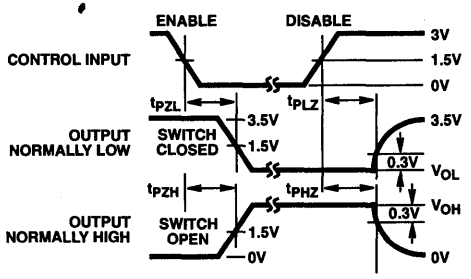


FIGURE 2. ENABLE AND DISABLE TIMING

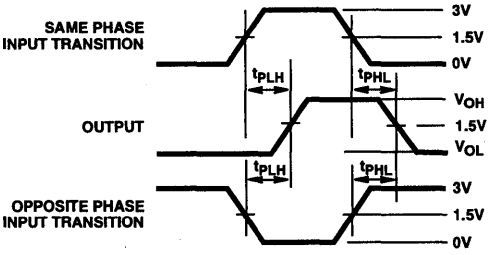


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR CD74FCT162Q373T

ADVANCE INFORMATION

December 1996

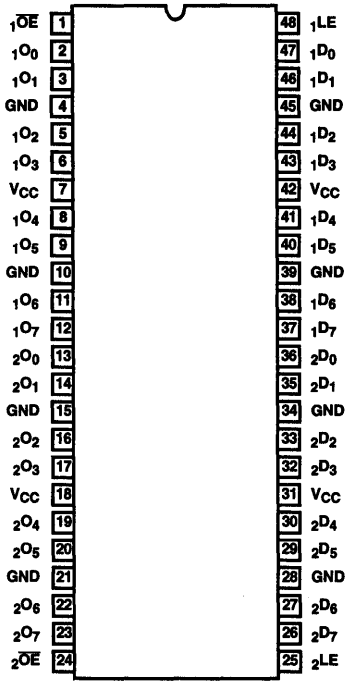
Fast CMOS 16-Bit Transparent Latch

Features

- **Advanced 0.6 micron CMOS Technology**
- **V_{CC} = 5V ±10%**
- **Balanced Output Drivers: ±12mA**
- **Output Impedance 35Ω (Typical)**
- **Typical V_{OLP} (Output Ground Bounce) < 0.5V at V_{CC} = 5V, T_A = 25°C**
- **Bus Hold Retains Last Active Bus State During Three-State**
- **Hysteresis on All Inputs**

Pinout

CD74FCT162Q373T
(SSOP, TSSOP)
TOP VIEW



Description

The CD74FCT162Q373T is a 16-bit transparent latch designed with three-state outputs and are intended for bus oriented applications. The Output Enable and Latch Enable controls are organized to operate as two 8-bit latches or one 16-bit latch. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

The CD74FCT162Q373T is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This device features a typical output impedance of 35Ω eliminating the need for external terminating resistors for most bus interface applications. This noise suppression benefit is designaated by the letter "Q" (for quiet) in the part number.

The CD74FCT162Q373T has "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors.

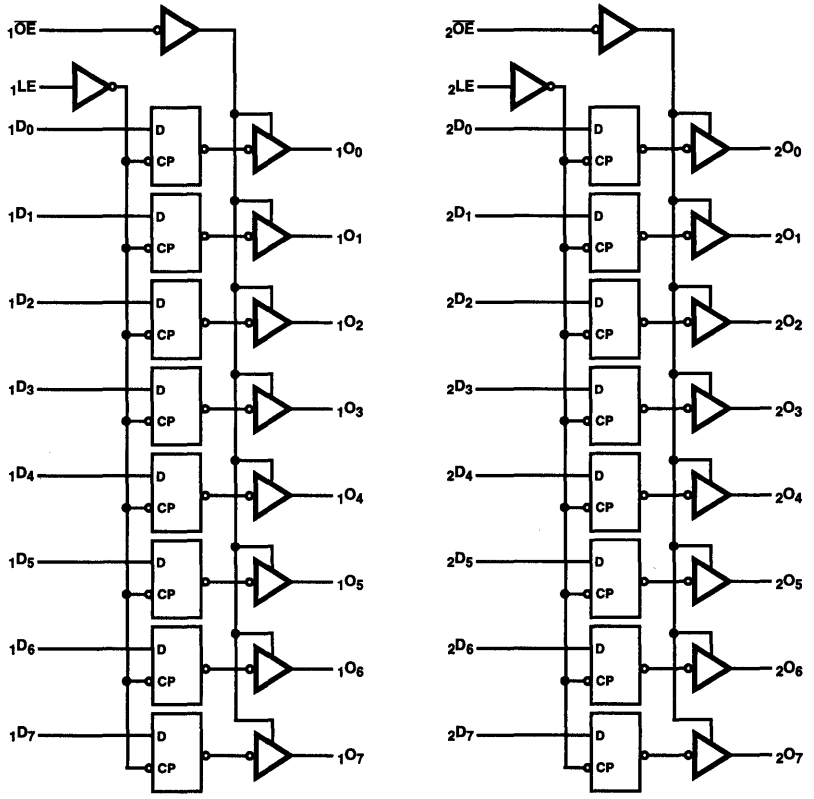
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT162Q373TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q373ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q373CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q373DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q373ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q373TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q373ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q373CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q373DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q373ETSM	-40 to 85	48 Ld SSOP	M48.300-P

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4278**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$_xD_x$	$_x\overline{OE}$	$_xLE$	$_xO_x$
H	L	H	H
L	L	H	L
X	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_x\overline{OE}$	Output Enable Inputs (Active LOW)
$_xLE$	Latch Enable Inputs (Active HIGH)
$_xD_x$	Inputs (Note 2)
$_xO_x$	Three-State Outputs
GND	Ground
V_{CC}	Power

NOTE:

2. For the CD74FCT162Q373T, these pins have "Bus Hold". All other pins are standard, outputs, or I/Os.

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH} I_{BHL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
			V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 9)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output Drive Current	I_O	V_{CC} = Max (Note 6), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output LOW Current	I_{ODL}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 6)		36	-	-	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 6)		-100	-166	-200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -12.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 12 mA	-	0.3	0.55	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND, $_xLE = V_{CC}$ One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND, $_xLE = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	0.6	1.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	0.9	2.3 (Note 12)	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz 50% Duty Cycle $x\overline{OE}$ = GND, $_xLE = V_{CC}$ 16 Bits Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND	-	2.5	5.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	6.4	16.5 (Note 12)	mA

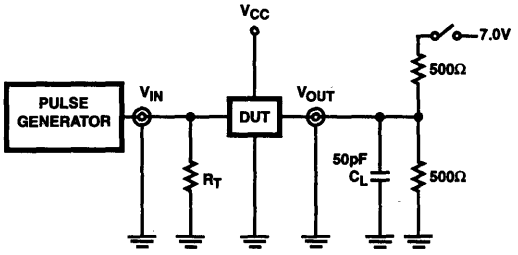
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T		AT		CT		DT		ET		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay $_XD_X$ to $_XO_X$	t_{PLH}, t_{PHL}	C_L = 50 pF, R_L = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	1.5	3.4	ns
Propagation Delay $_X$LE to $_XO_X$	t_{PLH}, t_{PHL}		2.0	13.0	2.0	8.5	2.0	5.5	1.5	4.0	1.5	4.0	ns
Output Enable Time $_X\overline{OE}$ to $_XO_X$	t_{PZH}, t_{PZL}		1.5	12.0	1.5	6.5	1.5	5.5	1.5	4.8	1.5	4.8	ns
Output Disable Time (Note 16) $_X\overline{OE}$ to $_XO_X$	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.5	1.5	5.0	1.5	4.0	1.5	4.0	ns
Setup Time HIGH or LOW, $_XD_X$ to $_X$LE	t_{SU}		2.0	-	2.0	-	2.0	-	1.5	-	1.0	-	ns
Hold Time HIGH or LOW, $_XD_X$ to $_X$LE	t_H		1.5	-	1.5	-	1.5	-	1.0	-	1.0	-	ns
$_X$LE Pulse Width HIGH (Note 16)	t_W		6.0	-	5.0	-	5.0	-	3.0	-	3.0	-	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. Pins with Bus Hold are identified in the pin description.
8. This specification does not apply to bi-directional functionalities with Bus Hold.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

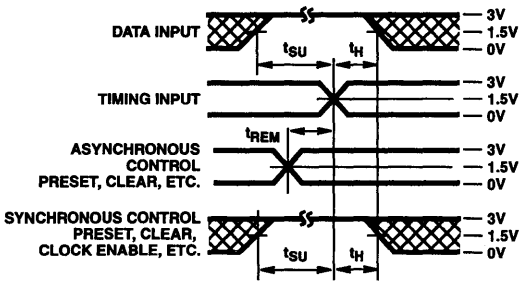


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

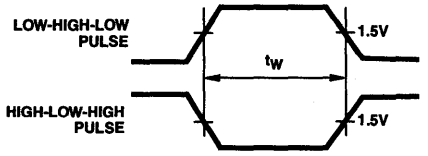


FIGURE 3. PULSE WIDTH

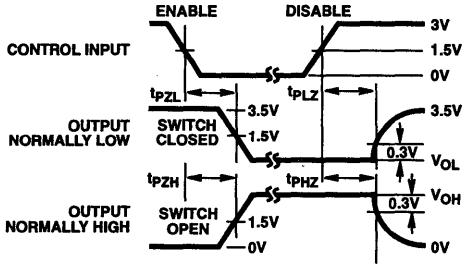


FIGURE 4. ENABLE AND DISABLE TIMING

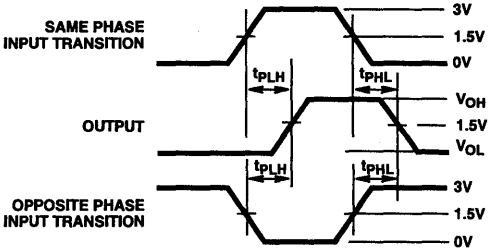


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR CD74FCT162Q374T

ADVANCE INFORMATION

December 1996

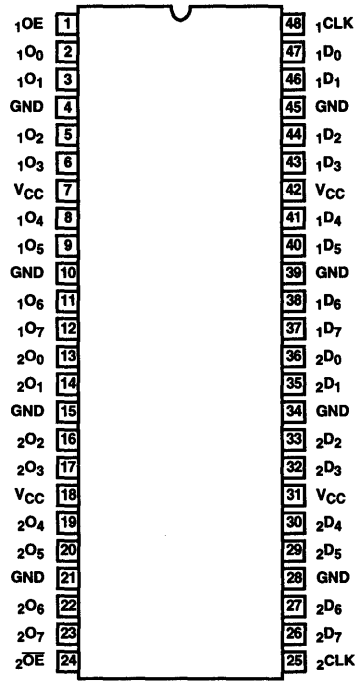
Fast CMOS 16-Bit Register (Three-State)

Features

- Advanced 0.6 micron CMOS Technology
- V_{CC} = 5V ±10%
- Balanced Output Drivers: ±12mA
- Output Impedance 35Ω (Typical)
- Typical V_{OLP} (Output Ground Bounce) < 0.5V at V_{CC} = 5V, T_A = 25°C
- Bus Hold Retains Last Active Bus State During Three-State
- Hysteresis on All Inputs

Pinout

CD74FCT162Q374T
(SSOP, TSSOP)
TOP VIEW



Description

The CD74FCT162Q374T is a 16-bit octal register designed with 16 D-type flip-flops with a buffered common clock and three-state outputs. The Output Enable ($_X\overline{OE}$) and clock ($_X$CLK) controls are organized to operate as two 8-bit registers or one 16-bit register. When $\overline{OE}$ is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the $_XO_X$ outputs on the LOW-to-HIGH transition of the clock input.

The CD74FCT162Q374T is designed with current limited resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This device features a typical output impedance of 35Ω eliminating the need for external terminating resistors for most bus interface applications. This noise suppression benefit is designaated by the letter "Q" (for quiet) in the part number.

The CD74FCT162Q374T has "Bus Hold" which retains the input's last state whenever the input goes to high-impedance preventing "floating" inputs and eliminating the need for pull-up/down resistors

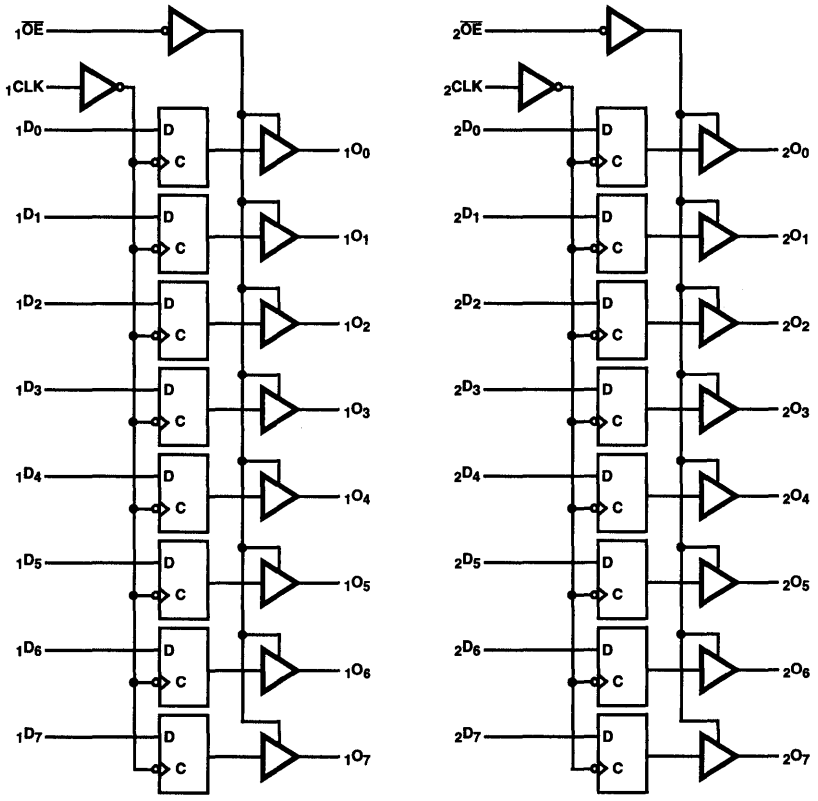
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT162Q374TMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q374ATMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q374CTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q374DTMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q374ETMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT162Q374TSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q374ATSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q374CTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q374DTSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT162Q374ETSM	-40 to 85	48 Ld SSOP	M48.300-P

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4279**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS			OUTPUTS
	$_xD_x$	$_xCLK$	$_x\overline{OE}$	$_xO_x$
High-Z	X	L	H	Z
	X	H	4H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$_x\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$_xCLK$	Clock Inputs
$_xD_x$	Inputs (Note 2)
$_xO_x$	Three-State Outputs
GND	Ground
V_{CC}	Power

NOTE:

2. For the CD74FCT162Q374T, these pins have "Bus Hold". All other pins are standard, outputs, or I/Os.

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ±10%							
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	Standard Input V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	1	µA
Input HIGH Current	I_{IH}	Bus Hold Input (Note 7) V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±100	µA
Input LOW Current	I_{IL}	Standard Input V_{CC} = Min	V_{IN} = GND	-	-	-1	µA
Input LOW Current	I_{IL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = GND	-	-	±100	µA
Bus Hold Sustain Current	I_{BHH} I_{BHL}	Bus Hold Input (Note 7) V_{CC} = Min	V_{IN} = 2.0V	-50	-	-	µA
			V_{IN} = 0.8V	50	-	-	µA
High Impedance Output Current (Three-State) (Note 9)	I_{OZH}	V_{CC} = Max	V_{OUT} = 2.7V	-	-	1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = 0.5V	-	-	-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output Drive Current	I_O	V_{CC} = Max (Note 6), V_{OUT} = 2.5V		-50	-	-180	mA
Input Hysteresis	V_H			-	100	-	mV
OUTPUT DRIVE SPECIFICATIONS Over the Operating Range							
Output LOW Current	I_{ODL}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 6)		36	-	-	mA
Output HIGH Current	I_{ODH}	V_{CC} = 5V, $V_{IN} = V_{IH}$ or V_{IL}, V_{OUT} = 1.5V (Note 6)		-100	-166	-200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -12.0mA	2.4	3.3	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 12 mA	-	0.3	0.55	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 4) TEST CONDITIONS		MIN	(NOTE 5) TYP	MAX	UNITS
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 9)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 9)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 10)	-	0.5	1.5	mA
Supply Current per Input per MHz (Note 11)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	60	100	µA/ MHz
Total Power Supply Current (Note 13)	I_C	V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND f_i = 5MHz, 50% Duty Cycle One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	0.6	1.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	1.1	3.0 (Note 12)	mA
		V_{CC} = Max, Outputs Open f_{CP} = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	3.0	5.5 (Note 12)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	7.5	19.0 (Note 12)	mA

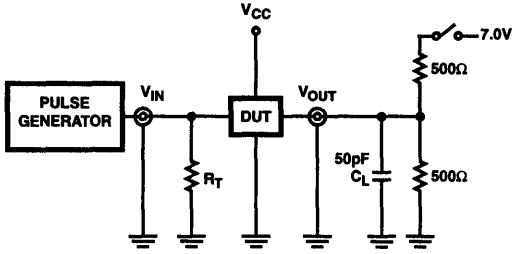
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	T		AT		CT		DT		ET		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay $_xD_X$ to $_xO_X$	t_{PLH}, t_{PHL}	C_L = 50 pF R_L = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	1.5	3.8	1.5	3.4	ns
Propagation Delay $_xLE$ to $_xO_X$	t_{PLH}, t_{PHL}		2.0	13.0	2.0	8.5	2.0	5.5	1.5	4.0	1.5	4.0	ns
Output Enable Time $_x\overline{OE}$ to $_xO_X$	t_{PZH}, t_{PZL}		1.5	12.0	1.5	6.5	1.5	5.5	1.5	4.8	1.5	4.8	ns
Output Disable Time (Note 16) $_x\overline{OE}$ to $_xO_X$	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.5	1.5	5.0	1.5	4.0	1.5	4.0	ns
Setup Time HIGH or LOW, $_xD_X$ to $_xLE$	t_{SU}		2.0	-	2.0	-	2.0	-	1.5	-	1.0	-	ns
Hold Time HIGH or LOW, $_xD_X$ to $_xLE$	t_H		1.5	-	1.5	-	1.5	-	1.0	-	3.0	-	ns
$_xLE$ Pulse Width HIGH (Note 16)	t_W		6.0	-	5.0	-	5.0	-	3.0	-	-	-	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	-	0.5	-	0.5	ns

NOTES:

4. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
5. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
6. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
7. Pins with Bus Hold are identified in the pin description.
8. This specification does not apply to bi-directional functionalities with Bus Hold.
9. This parameter is determined by device characterization but is not production tested.
10. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
12. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
13. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

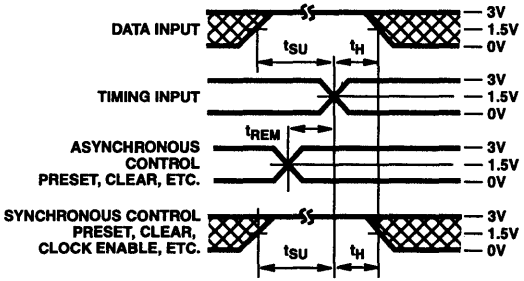


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

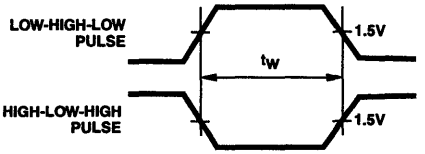


FIGURE 3. PULSE WIDTH

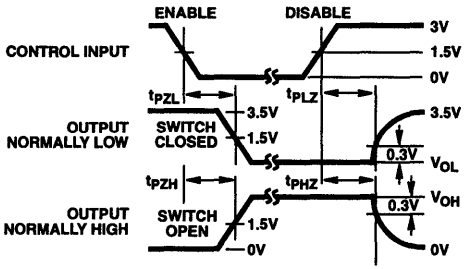


FIGURE 4. ENABLE AND DISABLE TIMING

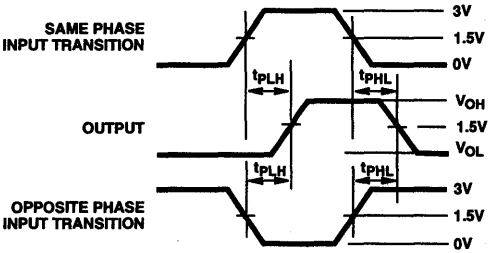


FIGURE 5. PROPAGATION DELAY

CMOS LOGIC 7

3.3V FCT CMOS LOGIC

		PAGE
Selection Guide		7-2
Data Sheets		
CD74FCT163240	Fast CMOS 3.3V 16-Bit Octal Buffer/Line Driver	7-3
CD74FCT163244	Fast CMOS 3.3V 16-Bit Buffer/Line Driver	7-9
CD74FCT163245	Fast CMOS 3.3V 16-Bit Bidirectional Transceiver	7-15
CD74FCT163373	Fast CMOS 3.3V 16-Bit Transparent Latch	7-21
CD74FCT163374	Fast CMOS CMOS 3.3V 6-Bit Register (Three-State)	7-27

Selection Guide

3.3V FCT CMOS LOGIC

PART NUMBER	DESCRIPTION	SPEED GRADE (X)			FILE #
		BLANK	A	C	
CD74FCT163240	Fast CMOS 3.3V 16-Bit Octal Buffer/Line Driver	X	X	-	4255
CD74FCT163244	Fast CMOS 3.3V 16-Bit Buffer/Line Driver	X	X	X	4192
CD74FCT163245	Fast CMOS 3.3V 16-Bit Bidirectional Transceivers	X	X	X	4193
CD74FCT163373	Fast CMOS 3.3V 16-Bit Transparent Latch	X	X	X	4194
CD74FCT163374	Fast CMOS CMOS 3.3V 6-Bit Registers (Three-State)	X	X	X	4195

HARRIS SEMICONDUCTOR

CD74FCT163240

December 1996

Fast CMOS 3.3V 16-Bit Octal Buffer/Line Driver

Features

- Advanced 0.6 micron CMOS Technology
- Advanced Low Power CMOS Operation
- Can Serve as a 5V to 3V Translator
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
  - Compatible with LVC™ Class of Products
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Inputs Can Be Driven by 3.3V or 5V Devices
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT163240AMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163240ASM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT163240MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163240SM	-40 to 85	48 Ld SSOP	M48.300-P

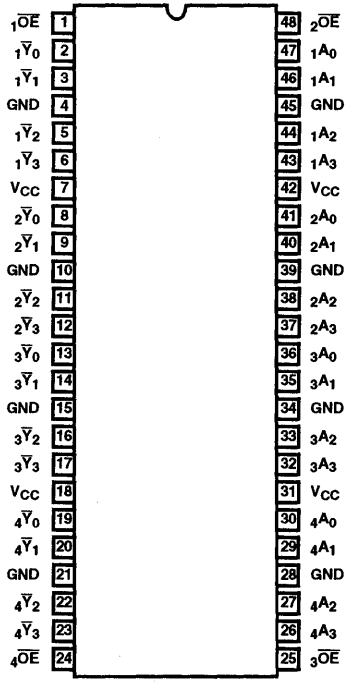
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the varient in the tape and reel.

Description

The CD74FCT163240 is an inverting 16-bit buffer/line driver designed for applications driving high-capacitance loads and low impedance backplanes. This high-speed, low power device offers bus/backplane interface capability and a flow-through organization for ease of board layout. This device is designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

Pinout

CD74FCT163240
(SSOP, TSSOP)
TOP VIEW



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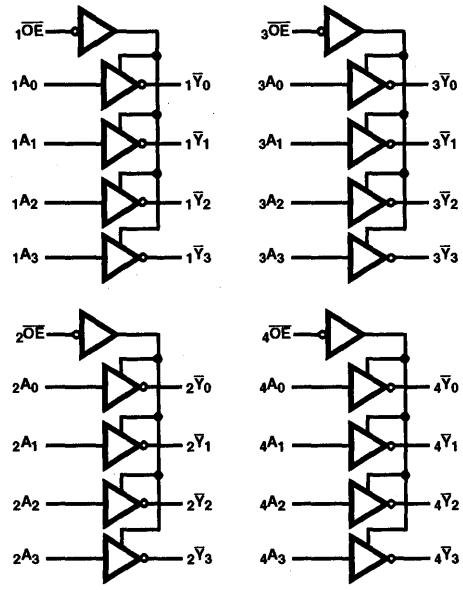
3.3V FCT

File Number 4255

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$_X\overline{OE}$	$_XA_X$	$_X\overline{Y}_X$
L	L	H
L	H	L
H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_X\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$_XA_X$	Inputs
$_X\overline{Y}_X$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . $-40^{o}C$ to $85^{o}C$
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)
SSOP Package	76
TSSOP Package	94

Maximum Junction Temperature . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^{o}C$ to $85^{o}C$, $V_{CC} = 2.7V$ to $3.6V$							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	$V_{CC} + 0.5$	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	$V_{IN} = 5.5V$	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State) (Output Pins)	I_{OZH}	V_{CC} = Max	$V_{OUT} = V_{CC}$	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, $I_{IN} = -18mA$		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	$V_{CC} = 3.3V$, $V_{IN} = V_{IH}$ or V_{IL}, $V_O = 1.5V$ (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	$V_{CC} = 3.3V$, $V_{IN} = V_{IH}$ or V_{IL}, $V_O = 1.5V$ (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -0.1mA$	$V_{CC} - 0.2$	-	-	V
			$I_{OH} = -3mA$	2.4	3.0	-	V
		$V_{CC} = 3.0V$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -8mA$	2.4 (Note 8)	3.0	-	V
			$I_{OH} = -24mA$	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 0.1mA$	-	-	0.2	V
			$I_{OL} = 16mA$	-	0.2	0.4	V
			$I_{OL} = 24mA$	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 7)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 7)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = VCC - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	0.5	0.8	mA
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	2.0	3.3 (Note 11)	mA

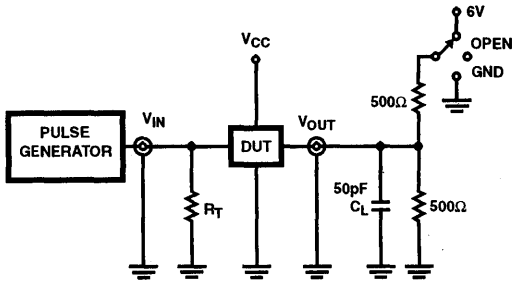
Switching Specifications Over Operating Range (NOTE 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74FCT163240		CD74FCT163240A		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay xA_X to $x\overline{Y}_X$	t_{PLH}, t_{PHL}	C_L = 50pF, R_L = 500Ω	1.5	8.0	1.5	4.8	ns
Output Enable Time $x\overline{OE}$ to $x\overline{Y}_X$	t_{PZH}, t_{PZL}		1.5	10.0	1.5	6.2	ns
Output Disable Time (Note 16) $x\overline{OE}$ to $x\overline{Y}_X$	t_{PHZ}, t_{PLZ}		1.5	9.5	1.5	5.6	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. This parameter is determined by device characterization but is not production tested.
8. $V_{OH} = V_{CC}$ - 0.6V at rated current.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (Vin = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuits and waveforms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

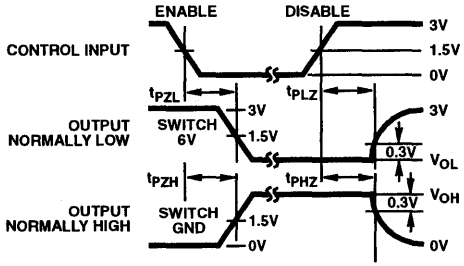


FIGURE 2. ENABLE AND DISABLE TIMING

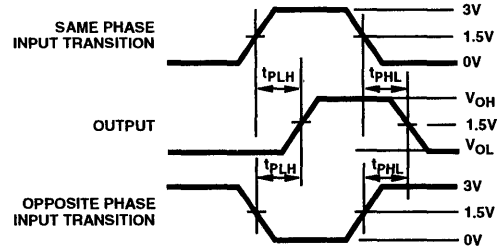


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR

CD74FCT163244

December 1996

Fast CMOS 3.3V 16-Bit Buffer/Line Driver

Features

- Advanced 0.6 micron CMOS Technology
- Advanced Low Power CMOS Operation
- Can Serve as a 5V to 3V Translator
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
  - Compatible with LVC™ Class of Products
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Inputs Can Be Driven by 3.3V or 5V Devices
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT163244AMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163244ASM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT163244CMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163244CSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT163244MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163244SM	-40 to 85	48 Ld SSOP	M48.300-P

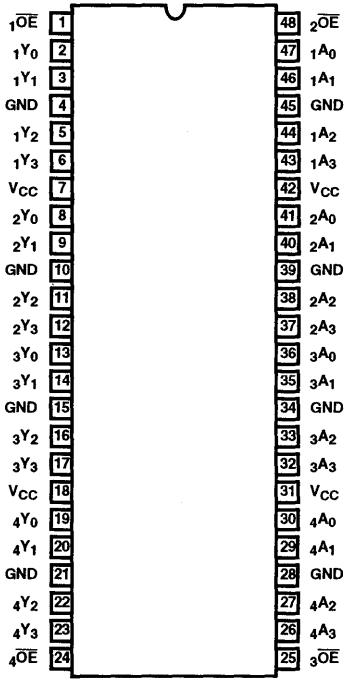
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

The CD74FCT163244 is a 16-bit buffer/line driver designed for applications driving high capacitive loads and low impedance backplanes. This high-speed, low power device offers bus/backplane interface capability and a flow-through organization for ease of board layout. This device is designed with three-state controls to operate in a Quad-Nibble, Dual-Byte, or a single 16-bit word mode.

Pinout

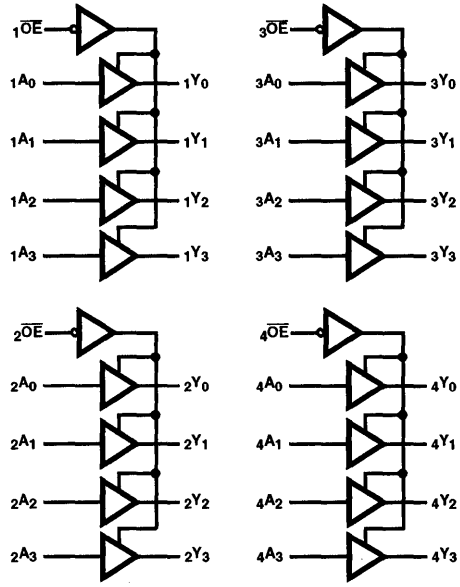
CD74FCT163244
(SSOP, TSSOP)
TOP VIEW



7 3.3V FCT

File Number **4192.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$_X\overline{OE}$	$_XA_X$	$_XY_X$
L	L	L
L	H	H
H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_X\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$_XA_X$	Inputs
$_XY_X$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	V_{CC} + 0.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State)	I_{OZH}	V_{CC} = Max	V_{OUT} = V_{CC}	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 8)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 7)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 7)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = VCC - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	0.5	0.8	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	2.0	3.3 (Note 11)	mA

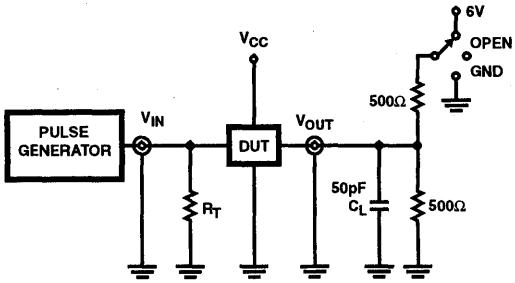
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74FCT163244		CD74FCT163244A		CD74FCT163244C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
CD74FCT16244, CD74FCT162244									
Propagation Delay $_XA_X$ to $_XY_X$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	4.8	1.5	4.1	ns
Output Enable Time $_X\overline{OE}$ to $_XY_X$	t_{PZH}, t_{PZL}		1.5	8.0	1.5	6.2	1.5	5.8	ns
Output Disable Time (Note 16) $_X\overline{OE}$ to $_XY_X$	t_{PHZ}, t_{PLZ}		1.5	7.0	1.5	5.6	1.5	5.2	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. This parameter is determined by device characterization but is not production tested.
8. $V_{OH} = V_{CC}$ - 0.6V at rated current.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuits and waveforms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $Z_{OUT} \leq 50\Omega$; t_f, $t_r \leq 2.5$ns.

FIGURE 1. TEST CIRCUIT

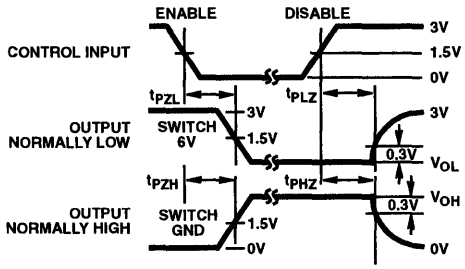


FIGURE 2. ENABLE AND DISABLE TIMING

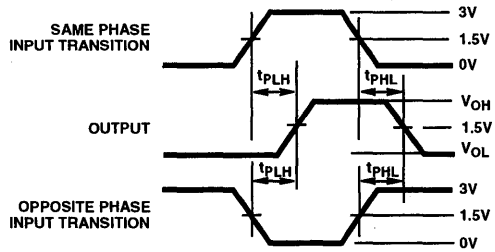


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR CD74FCT163245

December 1996

Fast CMOS 3.3V 16-Bit Bidirectional Transceiver

Features

- Advanced 0.6 micron CMOS Technology
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
  - Compatible with LVC™ Class of Products.
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Control Inputs Can Be Driven by 3.3V or 5V Devices
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT163245AMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163245ASM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT163245CMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163245CSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT163245MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163245SM	-40 to 85	48 Ld SSOP	M48.300-P

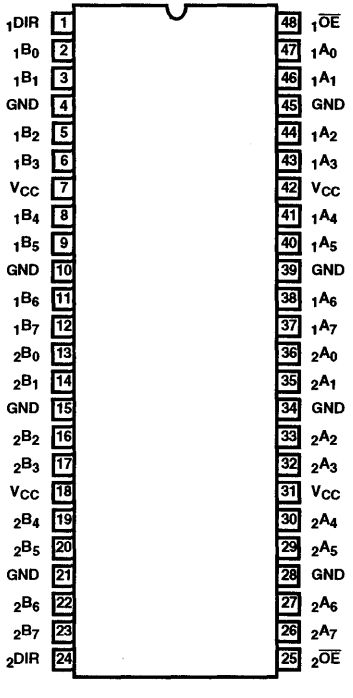
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

The CD74FCT163245 is a 16-bit bidirectional transceiver designed for asynchronous two-way communication between data buses. The direction control input pin ($_X$DIR) determines the direction of data flow through the bidirectional transceiver. The Direction and Output Enable controls are designed to operate this device as either two independent 8-bit transceivers or one 16-bit transceiver. The output enable ($_X\overline{OE}$) input, when HIGH, disables both A and B ports by placing them in HIGH Z condition.

Pinout

CD74FCT163245
(SSOP, TSSOP)
TOP VIEW

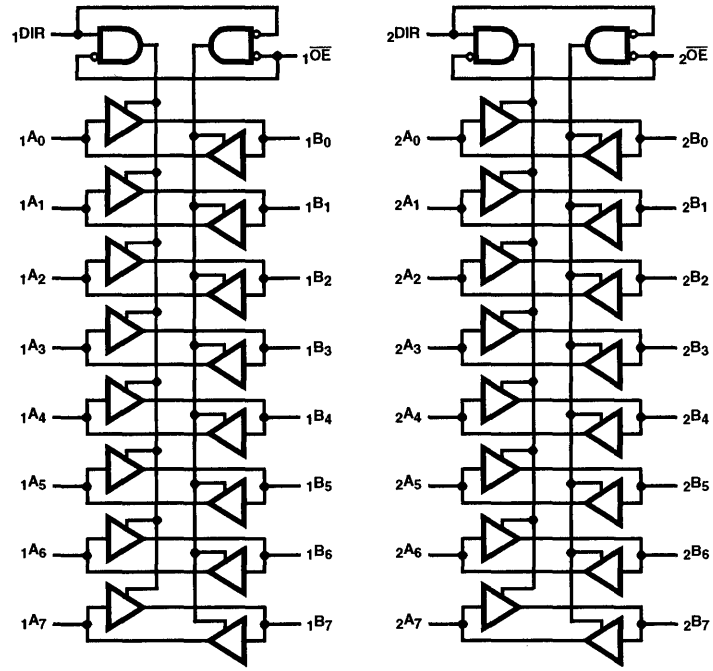


7

3.3V FCT

File Number **4193.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS		OUTPUTS
$_X\overline{OE}$	$_X$DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_X\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$_X$DIR	Direction Control Input
$_XA_X$	Side A Inputs or Three-State Outputs
$_XB_X$	Side B Inputs or Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
TSSOP Package 94
SSOP Package 76
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	V_{CC} + 0.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State)	I_{OZH}	V_{CC} = Max	V_{OUT} = V_{CC}	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 8)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 7)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 7)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = VCC - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = xDIR = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_I = 10MHz, 50% Duty Cycle $x\overline{OE}$ = xDIR = GND One Bit Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	0.5	0.8	mA
		V_{CC} = Max, Outputs Open f_I = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = xDIR = GND 16 Bits Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	2.0	3.3 (Note 11)	mA

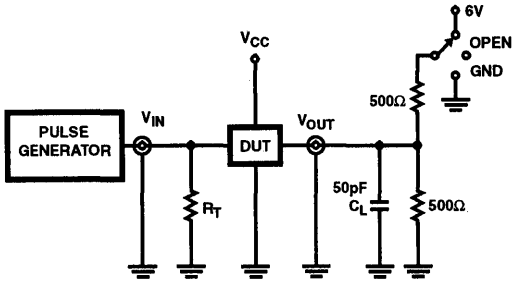
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74FCT163245		CD74FCT163245A		CD74FCT163245C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay A to B, B to A	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	7.0	1.5	4.6	1.5	4.1	ns
Output Enable Time $x\overline{OE}$ to A or B	t_{PZH}, t_{PZL}		1.5	9.5	1.5	6.2	1.5	5.8	ns
Output Disable Time (Note 16) $x\overline{OE}$ to A or B	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.0	1.5	4.8	ns
Output Enable Time xDIR to A or B	t_{PZH}, t_{PZL}		1.5	9.5	1.5	6.2	1.5	5.8	ns
Output Disable Time xDIR to A or B (Note 16)	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.0	1.5	4.8	ns
Output Skew(17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. This parameter is determined by device characterization but is not production tested.
8. $V_{OH} = V_{CC}$ - 0.6V at rated current.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuits and waveforms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

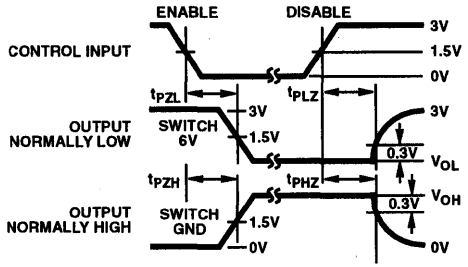


FIGURE 2. ENABLE AND DISABLE TIMING

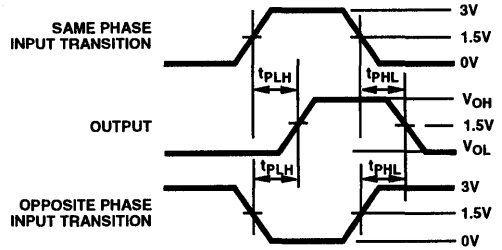


FIGURE 3. PROPAGATION DELAY

HARRIS SEMICONDUCTOR CD74FCT163373

December 1996

Fast CMOS 3.3V 16-Bit Transparent Latch

Features

- Advanced 0.6 micron CMOS Technology
- Advanced Low Power CMOS Operation
- Can Serve as a 5V to 3V Translator
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
  - Compatible with LVC™ Class of Products.
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Inputs Can Be Driven by 3.3V or 5V Devices
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT163373AMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163373ASM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT163373CMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163373CSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT163373MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163373SM	-40 to 85	48 Ld SSOP	M48.300-P

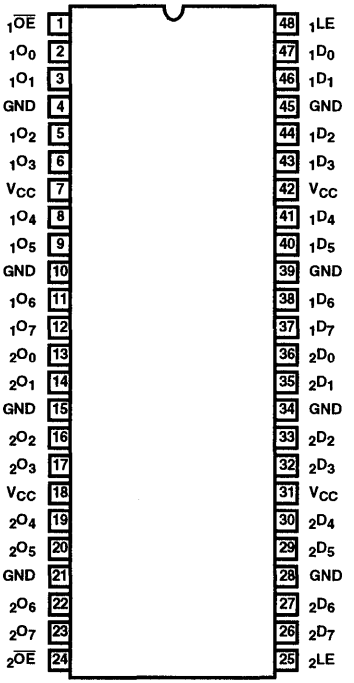
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the varient in the tape and reel.

Description

The CD74FCT163373 is a 16-bit transparent latch designed with three-state outputs and is intended for bus oriented applications. The Output Enable and Latch Enable controls are organized to operate as two 8-bit latches or one 16-bit latch. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

Pinout

CD74FCT163373
(SSOP, TSSOP)
TOP VIEW



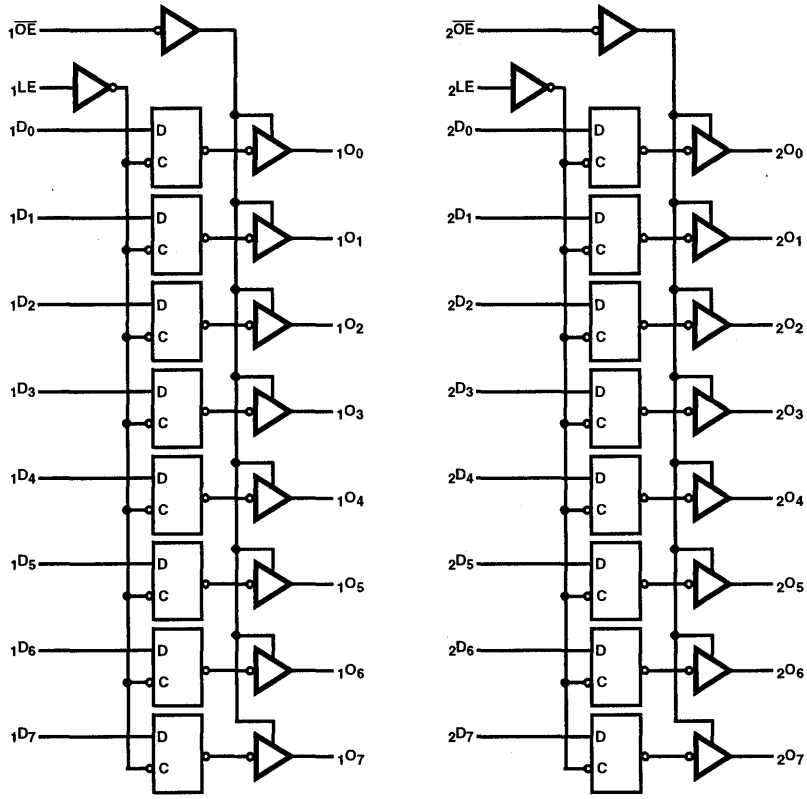
7

3.3V FCT

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4194.1**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
$_xD_x$	$_x\overline{OE}$	$_xLE$	$_xO_x$
H	L	H	H
L	L	H	L
X	H	X	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
$_x\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$_xLE$	Latch Enable Inputs (Active HIGH)
$_xD_x$	Data Inputs
$_xO_x$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . $-40^{o}C$ to $85^{o}C$
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} ($^{o}C/W$)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . $150^{o}C$
Maximum Storage Temperature Range . . . . . $-65^{o}C$ to $150^{o}C$
Maximum Lead Temperature (Soldering 10s) . . . . . $300^{o}C$
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, $T_A = -40^{o}C$ to $85^{o}C$, $V_{CC} = 2.7V$ to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	$V_{CC} + 0.5$	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	$V_{IN} = 5.5V$	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	$V_{IN} = V_{CC}$	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State)	I_{OZH}	V_{CC} = Max	$V_{OUT} = V_{CC}$	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	$V_{CC} = Min$, $I_{IN} = -18mA$		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	$V_{CC} = 3.3V$, $V_{IN} = V_{IH}$ or V_{IL}, $V_O = 1.5V$ (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	$V_{CC} = 3.3V$, $V_{IN} = V_{IH}$ or V_{IL}, $V_O = 1.5V$ (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	$V_{CC} = Min$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -0.1mA$	$V_{CC} - 0.2$	-	-	V
			$I_{OH} = -3mA$	2.4	3.0	-	V
		$V_{CC} = 3.0V$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -8mA$	2.4 (Note 8)	3.0	-	V
			$I_{OH} = -24mA$	2.0	-	-	V
Output LOW Voltage	V_{OL}	$V_{CC} = Min$, $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 0.1mA$	-	-	0.2	V
			$I_{OL} = 16mA$	-	0.2	0.4	V
			$I_{OL} = 24mA$	-	0.3	0.5	V

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 7)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 7)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = VCC - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open $x\overline{OE}$ = GND xLE = V_{CC} One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} One Bit Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	0.5	0.8	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle $x\overline{OE}$ = GND xLE = V_{CC} 16 Bits Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	2.0	3.3 (Note 11)	mA

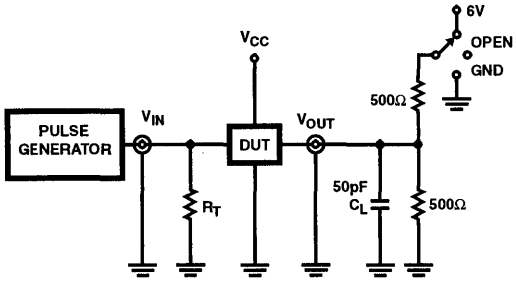
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74FCT163373		CD74FCT163373A		CD74FCT163373C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay $_xD_x$ to $_xO_x$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	5.2	1.5	4.2	ns
Propagation Delay $_xLE$ to $_xO_x$	t_{PLH}, t_{PHL}		2.0	13.0	2.0	8.5	2.0	5.5	ns
Output Enable Time $_x\overline{OE}$ to $_xO_x$	t_{PZH}, t_{PZL}		1.5	12.0	1.5	6.5	1.5	5.5	ns
Output Disable Time (Note 16) $_x\overline{OE}$ to $_xO_x$	t_{PHZ}, t_{PLZ}		1.5	7.5	1.5	5.5	1.5	5.0	ns
Setup Time HIGH or LOW, $_xD_x$ to $_xLE$	t_{SU}		2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, $_xD_x$ to $_xLE$	t_H		1.5	-	1.5	-	1.5	-	ns
$_xLE$ Pulse Width HIGH	t_W		6.0	-	5.0	-	5.0	-	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading, except as noted.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. This parameter is determined by device characterization but is not production tested.
8. $V_{OH} = V_{CC}$ - 0.6V at rated current.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuits and waveforms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

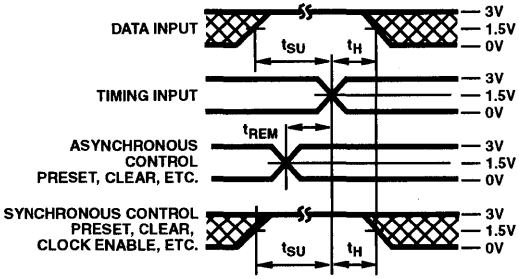


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

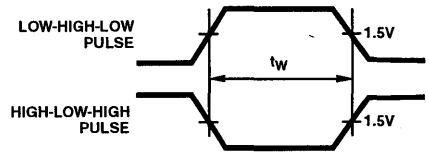


FIGURE 3. PULSE WIDTH

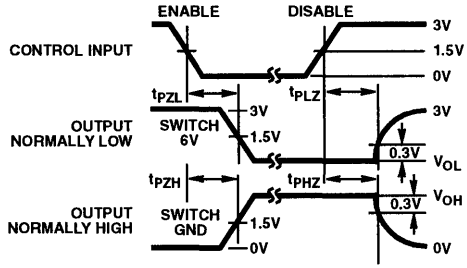


FIGURE 4. ENABLE AND DISABLE TIMING

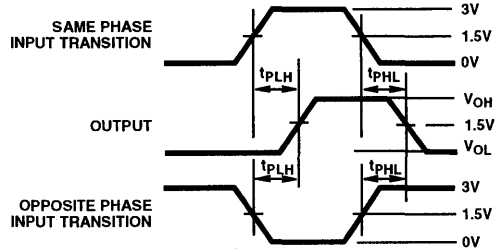


FIGURE 5. PROPAGATION DELAY

HARRIS SEMICONDUCTOR CD74FCT163374

December 1996

Fast CMOS CMOS 3.3V 6-Bit Register (Three-State)

Features

- Advanced 0.6 micron CMOS Technology
- Advanced Low Power CMOS Operation
- Can Serve as a 5V to 3V Translator
- Excellent Output Drive Capability:
  - Balanced Drives (24mA Sink and Source)
  - Compatible with LVC™ Class of Products.
- Pin Compatible with Industry Standard Double-Density Pinouts
- Low Ground Bounce Outputs
- Hysteresis on All Inputs
- Inputs Can Be Driven by 3.3V or 5V Devices
- Multiple Center Pin and Distributed V_{CC}/GND Pins Minimizing Switching Noise

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT163374AMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163374ASM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT163374CMT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163374CSM	-40 to 85	48 Ld SSOP	M48.300-P
CD74FCT163374MT	-40 to 85	48 Ld TSSOP	M48.240-P
CD74FCT163374SM	-40 to 85	48 Ld SSOP	M48.300-P

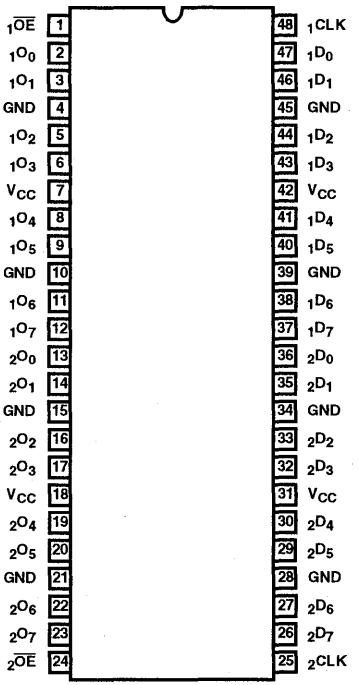
NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

The CD74FCT163374 is a 16-bit octal register designed with 16 D-type flip-flops with a buffered common clock and three-state outputs. The Output Enable ($_X\overline{OE}$) and clock ($_X$CLK) controls are organized to operate as two 8-bit registers or one 16-bit register. When $\overline{OE}$ is HIGH, the outputs are in the high-impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

Pinout

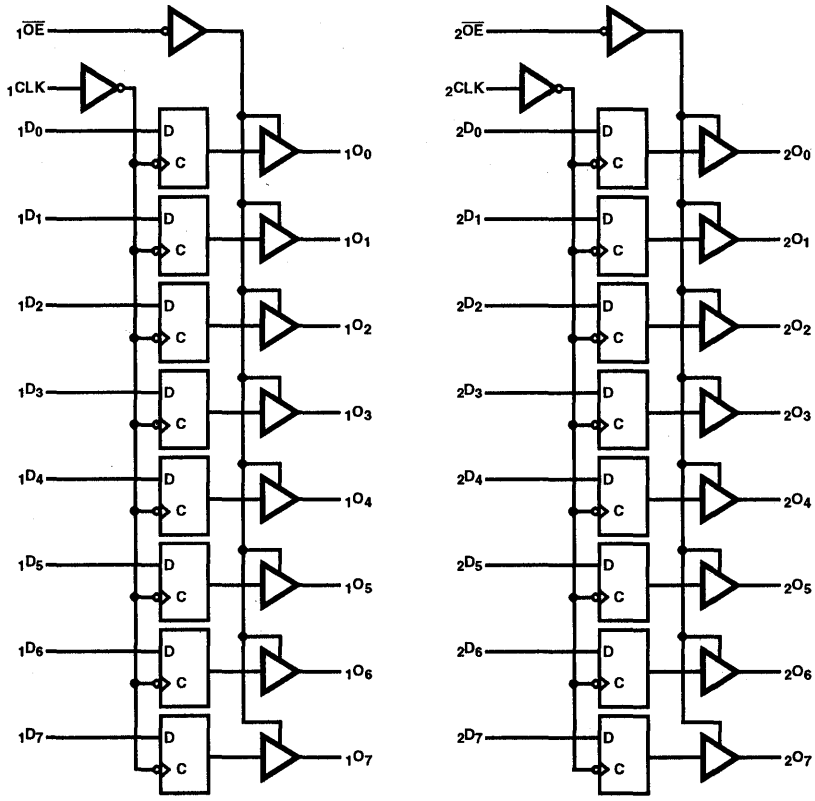
CD74FCT163374
(SSOP, TSSOP)
TOP VIEW



7
3.3V FCT

File Number **4195.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

FUNCTION	INPUTS			OUTPUTS
	$_xD_x$	$_x$CLK	$_x\overline{OE}$	$_xO_x$
High-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

Pin Descriptions

PIN NAME	DESCRIPTION
$_x\overline{OE}$	Three-State Output Enable Inputs (Active LOW)
$_x$CLK	Clock Inputs
$_xD_x$	Data Inputs
$_xO_x$	Three-State Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
TSSOP Package	94
SSOP Package	76

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 2.7V to 3.6V							
Input HIGH Voltage (Input Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.2	-	5.5	V
Input HIGH Voltage (I/O Pins)	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	V_{CC} + 0.5	V
Input LOW Voltage (Input and I/O Pins)	V_{IL}	Guaranteed Logic LOW Level		-0.5	-	0.8	V
Input HIGH Current (Input Pins)	I_{IH}	V_{CC} = Max	V_{IN} = 5.5V	-	-	±1	µA
Input HIGH Current (I/O Pins)	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	±1	µA
Input LOW Current (Input Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
Input LOW Current (I/O Pins)	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	±1	µA
High Impedance Output Current (Three-State)	I_{OZH}	V_{CC} = Max	V_{OUT} = V_{CC}	-	-	±1	µA
	I_{OZL}	V_{CC} = Max	V_{OUT} = GND	-	-	±1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Output HIGH Current	I_{ODH}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		-36	-60	-110	mA
Output LOW Current	I_{ODL}	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V (Note 5)		50	90	200	mA
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -0.1mA	V_{CC} - 0.2	-	-	V
			I_{OH} = -3mA	2.4	3.0	-	V
		V_{CC} = 3.0V, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -8mA	2.4 (Note 8)	3.0	-	V
			I_{OH} = -24mA	2.0	-	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 0.1mA	-	-	0.2	V
			I_{OL} = 16mA	-	0.2	0.4	V
			I_{OL} = 24mA	-	0.3	0.5	V

7
3.3V FCT

Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
Short Circuit Current (Note 6)	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-85	-240	mA
Input Hysteresis	V_H			-	150	-	mV
CAPACITANCE $T_A = 25^oC$, f = 1MHz							
Input Capacitance (Note 7)	C_{IN}	V_{IN} = 0V		-	4.5	6	pF
Output Capacitance (Note 7)	C_{OUT}	V_{OUT} = 0V		-	5.5	8	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	10	µA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = V_{CC} - 0.6V (Note 9)	-	2.0	30	µA
Dynamic Power Supply Current (Note 10)	I_{CCD}	V_{CC} = Max, Outputs Open x$\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	50	75	µA/ MHz
Total Power Supply Current (Note 12)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle x$\overline{OE}$ = GND One Bit Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	0.5	0.8	mA
		V_{CC} = Max, Outputs Open f_i = 2.5MHz, 50% Duty Cycle x$\overline{OE}$ = GND 16 Bits Toggling	V_{IN} = V_{CC} - 0.6V V_{IN} = GND	-	2.5	4.0 (Note 11)	mA

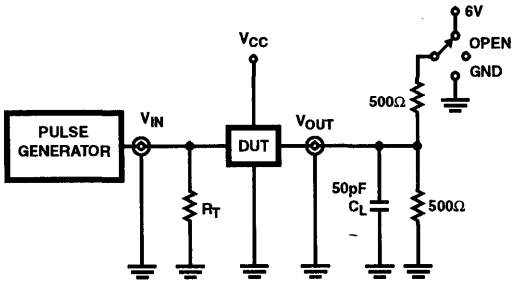
Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74FCT163374		CD74FCT163374A		CD74FCT163374C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay $_X$CLK to $_XO_X$	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	6.5	2.0	5.2	ns
Output Enable Time $_X\overline{OE}$ to $_XO_X$	t_{PZH}, t_{PZL}		1.5	12.5	1.5	6.5	1.5	5.5	ns
Output Disable Time (Note 16) $_X\overline{OE}$ to $_XO_X$	t_{PHZ}, t_{PLZ}		1.5	8.0	1.5	5.5	1.5	5.0	ns
Setup Time HIGH or LOW, $_XD_X$ to $_X$CLK	t_{SU}		2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, $_XD_X$ to $_X$CLK	t_H		1.5	-	1.5	-	1.5	-	ns
$_X$CLK Pulse Width HIGH (Note 16)	t_W		7.0	-	5.0	-	5.0	-	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 3.3V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. This parameter is determined by device characterization but is not production tested.
8. $V_{OH} = V_{CC}$ - 0.6V at rated current.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    N_{CP} = Number of Clock Inputs at f_{CP}
    f_I = Input Frequency
    N_I = Number of Inputs at f_I
    All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuits and waveforms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

18. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

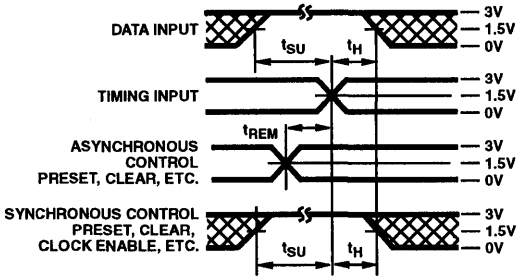


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

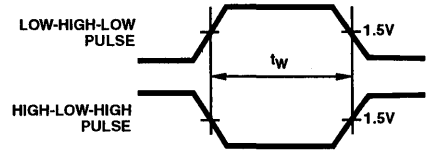


FIGURE 3. PULSE WIDTH

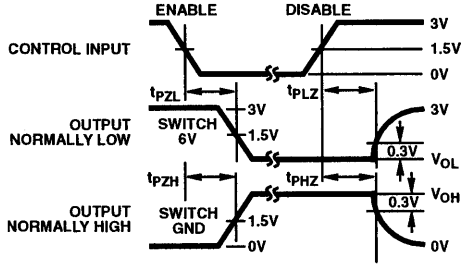


FIGURE 4. ENABLE AND DISABLE TIMING

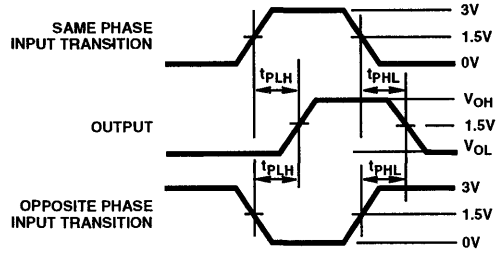


FIGURE 5. PROPAGATION DELAY

BiCMOS LOGIC 8

FCT BiCMOS LOGIC

		PAGE
Selection Guide		8-2
BiCMOS Cross-Reference Guide		8-3
BiCMOS Technical Overview		8-5
Data Sheets		
CD74FCT240, CD74FCT240AT, CD74FCT244, CD74FCT244AT	BiCMOS FCT Interface Logic, Octal Buffers/Line Drivers, Three-State	8-23
CD54FCT245, CD74FCT245	BiCMOS FCT Interface Logic, Octal-Bus Tranceivers, Three-State	8-28
CD74FCT273	BiCMOS FCT Interface Logic, Octal D Flip-Flop with Reset	8-33
CD74FCT373, CD74FCT373AT	BiCMOS FCT Interface Logic, Octal Transparent Latches, Three-State	8-38
CD74FCT374	BiCMOS FCT Interface Logic, Octal D-Type Flip-Flop, Three-State	8-43
CD74FCT540, CD74FCT541	BiCMOS FCT Interface Logic, Octal Buffers/Line Drivers, Three-State	8-48
CD74FCT543	BiCMOS FCT Interface Logic, Octal Register/Transceiver, Three-State	8-53
CD74FCT564, CD74FCT574	BiCMOS FCT Interface Logic, Octal D-Type Flip-Flops, Three-State	8-58
CD74FCT573, CD74FCT573AT	BiCMOS FCT Interface Logic, Octal Transparent Latches, Three-State	8-62
CD74FCT646	BiCMOS FCT Interface Logic, Octal Bus Transceiver/Register, Three-State	8-67
CD74FCT651, CD74FCT652	BiCMOS FCT Interface Logic, Octal Bus Transceivers/Registers, Three-State	8-72
CD74FCT653, CD74FCT654	FCT Interface Logic, Octal Bus Transceivers/ Registers, Open Drain (A Side), Three-State (B Side)	8-77
CD74FCT821A, CD74FCT822A	BiCMOS FCT Interface Logic, 10- Bit D-Type Flip-Flops, Three-State	8-83
CD74FCT823A, CD74FCT824A	BiCMOS FCT Interface Logic, 9-Bit D-Type Flip-Flops, Three-State	8-88
CD74FCT841A, CD74FCT842A	BiCMOS FCT Interface Logic, 10-Bit Transparent Latches, Three-State	8-93
CD74FCT843A, CD74FCT844A	BiCMOS FCT Interface Logic, 9-Bit Transparent Latches, Three-State	8-98
CD74FCT861A	BiCMOS FCT Interface Logic, 10-Bit Bus Transceiver, Three-State	8-103
CD74FCT863A	BiCMOS FCT Interface Logic, 9-Bit Bus Transceiver, Three-State	8-108

Selection Guide

BiCMOS LOGIC

PART NUMBER	DESCRIPTION	SPEED GRADE (X)		FILE #
		BLANK	A	
CD54FCT245	BiCMOS FCT Interface Logic Octal-Bus Tranceiver, Three-State	X		2301
CD74FCT240	BiCMOS Interface Logic, Octal Buffer/Line Driver, Three-State	X		2227
CD74FCT240AT	BiCMOS FCT Interface Logic, Octal Buffer/Line Driver, Three-State		X	2227
CD74FCT244	BiCMOS FCT Interface Logic, Octal Buffer/Line Driver, Three-State			2227
CD74FCT244AT	BiCMOS FCT Interface Logic, Octal Buffer/Line Driver, Three-State		X	2227
CD74FCT245	BiCMOS FCT Interface Logic Octal-Bus Tranceiver, Three-State	X		2301
CD74FCT273	BiCMOS FCT Interface Logic, Octal D Flip-Flop with Reset	X		2303
CD74FCT373	BiCMOS FCT Interface Logic Octal Transparent Latch, Three-State	X		2230
CD74FCT373AT	BiCMOS FCT Interface Logic Octal Transparent Latch, Three-State		X	2230
CD74FCT374	BiCMOS FCT Interface Logic, Octal D-Type Flip-Flop, Three-State	X		2305
CD74FCT540	BiCMOS FCT Interface Logic Octal Buffer/Line Driver, Three-State	X		2283
CD74FCT541	BiCMOS FCT Interface Logic Octal Buffer/Line Driver, Three-State	X		2283
CD74FCT543	BiCMOS FCT Interface Logic, Octal Register/Transceiver, Three-State	X		2397
CD74FCT564	BiCMOS FCT Interface Logic, Octal D-Type Flip-Flop, Three-State	X		2295
CD74FCT573	BiCMOS FCT Interface Logic Octal Transparent Latch, Three-State	X		2304
CD74FCT573AT	BiCMOS FCT Interface Logic Octal Transparent Latch, Three-State	X		2304
CD74FCT574	BiCMOS FCT Interface Logic, Octal D-Type Flip-Flop, Three-State	X		2245
CD74FCT646	BiCMOS FCT Interface Logic, Octal Bus Transceiver/Register, Three-State	X		2393
CD74FCT651	BiCMOS FCT Interface Logic, Octal Bus Transceiver/Register, Three-State	X		2374
CD74FCT652	BiCMOS FCT Interface Logic, Octal Bus Transceiver/Register, Three-State	X		2394
CD74FCT653	BiCMOS FCT Interface Logic, Octal Bus Transciever/Register, Open Drain (A Side), Three-State (B Side)	X		2403
CD74FCT654	BiCMOS FCT Interface Logic, Octal Bus Transcievers/Registers, Open Drain (A Side), Three-State (B Side)	X		2403
CD74FCT821A	BiCMOS FCT Interface Logic, 10-Bit D-Type Flip-Flops, Three-State		X	2390
CD74FCT822A	BiCMOS FCT Interface Logic, 10-Bit D-Type Flip-Flop, Three-State		X	2390
CD74FCT823	BiCMOS FCT Interface Logic, 9-Bit D-Type Flip-Flop, Three-State		X	2389
CD74FCT824A	BiCMOS FCT Interface Logic, 9-Bit D-Type Flip-Flop, Three-State		X	2389
CD74FCT841A	BiCMOS FCT Interface Logic, 10-Bit Transparent Latch, Three-State		X	2397
CD74FCT842A	BiCMOS FCT Interface Logic, 10-Bit Transparent Latch, Three-State		X	2397
CD74FCT843A	BiCMOS FCT Interface Logic, 9-Bit Transparent Latch, Three-State		X	2396
CD74FCT844A	BiCMOS FCT Interface Logic, 9-Bit Transparent Latch, Three-State		X	2396
CD74FCT861A	BiCMOS FCT Interface Logic, 10-Bit Bus Transceiver, Three-State		X	2392
CD74FCT863A	BiCMOS FCT Interface Logic, 9-Bit Bus Transceiver, Three-State		XS	2391

MIL Temperature Grade Substitution

All Harris BiCMOS FCT family types that were originally specified for the MIL temperature range (CD54FCTxxx) have been discontinued with 2 exceptions: CD54FCT244E and CD54FCT245E

For discontinued CCD54FCTxxx types, refer to the 74 series equivalent; i.e., CD74FCTxxx. For several types; the preferred type is the equivalent CD74FCTxxx type in the new state-of-the-art CMOS technology listed within this data book. This recommendation for substituting is highlighted on the cover page of each data sheet where applicable.

TABLE 1. CROSS OF AN IDT TYPE TO A RECOMMENDED HARRIS REPLACEMENT TYPE

IDT TYPE	HARRIS REPLACEMENT
P	E
SO	M
XXX	XXX
XXXA	XXXAT
XXXT	XXX
XXXAT	XXXAT
8XXA	8XXA

Type Numbers that cross over with one or more of the six options shown (XXX) in the above table.

240	374	646	823A	844A
244	540	651	824A	861A
245	541	652	841A	863A
273	543	821A	842A	
373	574	822A	843A	

TABLE 2. CROSS OF EQUIVALENT BIPOLAR FAST TTL TYPE TO HARRIS RECOMMENDED REPLACEMENT

BIPOLAR FAST TYPE	HARRIS REPLACEMENT
74FXXXP	CD74FCTXXXE
74FXXXS	CD74FCTXXXM

Type Numbers that cross over (XXX) in the above table.

240	374	564	821A (Note 1)
244	540	574	823A (Note 1)
245	541	646	841A (Note 1)
273	543	651	843A (Note 1)
373	544	652	

NOTE:

1. FCT equivalent types have a suffix A designation; the F types do not.

TABLE 3. CROSS OF EQUIVALENT BIPOLAR AS/TTL TYPES TO HARRIS RECOMMENDED REPLACEMENT TYPES

BIPOLAR AS/TTL TYPE	HARRIS REPLACEMENT
SN74ASXXXN	CD74FCTXXXE
SN74ASXXXDW	CD74FCTXXXM

Type Numbers that cross over (XXX) in the above table.

240	646	824A (Note 2)
244	651	841A (Note 2)
245	652	842A (Note 2)
373	821 (Note 2)	843A (Note 2)
374	822A (Note 2)	844A (Note 2)
574	823A (Note 2)	-

NOTE:

2. FCT equivalent types have a suffix A designation; the AS types do not.

TABLE 4. CROSS OF EQUIVALENT BIPOLAR ALS/TTL TYPE TO HARRIS RECOMMENDED REPLACEMENT

BIPOLAR ALS/TTL TYPE	HARRIS REPLACEMENT
SN74ALSXXXN	CD74FCTXXXE
SN74ALSXXXN-1	CD74FCTXXXE
SN74ALSXXXDW	CD74FCTXXXM
SN74ALSXXXDW-1	CD74FCTXXXM

Type Numbers that cross over (XXX) in the above table.

ALS	FCT	ALS	FCT	ALS	FCT
240A	240	564	564	842	842
244A	244	574	574	843	843
245A	245	646	646	844	844
273	273	651	651		
373	373	652	652		
374	374	653	653		
540	540	654	654		
541	541	841	841		

TABLE 5. CROSS OF EQUIVALENT TI BiCMOS BCT TYPE TO HARRIS RECOMMENDED REPLACEMENT

TI BCT TYPE	FCT TYPE
SN74BCTXXXN	CD74FCTXXXE
SN74BCTXXXDW	CD74FCTXXXM

Type Numbers that cross over (XXX) in above table.

240	540	646
244	541	651
245	543	652
373	564	
374	574	

Additional BCT/FCT Crossover Types:

BCT	FCT	BCT	FCT	BCT	FCT
29821	821A	29841	841A	29861	861A
29822	822A	29842	842A	29863	863A
29823	823A	29843	843A		
29824	824A	29844	844A		

TABLE 6. CROSS OF EQUIVALENT AMD "29" SERIES BIPOLAR OR CMOS LOGIC TYPE TO HARRIS RECOMMENDED REPLACEMENT TYPE

CATEGORY	AMD TYPE	HARRIS FCT TYPE
800 Series	AM29XXX	CD74FCTXXXA
	AM29XXXC	CD74FCTXXXA

The suffix A Harris FCT replacement types are generally faster speed than equivalent AMD "29" series types.

Type Numbers that cross over (XXX) in above table.

821	823	841	843	861
822	824	842	844	863

BiCMOS Technical Overview

Features

Harris BiCMOS FCT is a broad family of 8-bit, 9-bit and 10-bit computer-bus interface logic ICs. Harris FCT BiCMOS Bus-Interface ICs are designed to satisfy four major requirements of modern bus-oriented computer systems, namely:

- High Speed/Low Propagation Delay
- High Drive, to Meet Specified Bus-Interface Requirements for Clock and Data Lines
- Low Power Consumption (CMOS-Like)
- Minimization of Switching Noise

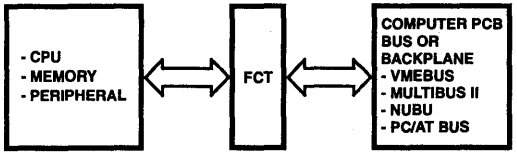


FIGURE 1. FCT AS BUS-INTERFACE ICs

NOTE: Harris offers FCT products in two speed grades: base speed (equal to FAST speeds) and higher speed (on average, 30% faster). The base speed version of each type is designated as either FCT or FCTXXXA, and the higher speed version, FCTXXXAT. The "T" was added to the suffix in order to highlight the fact that Harris FCT devices have a TTL-like output swing. Throughout this technical overview, FCT, FCTXXXA, FCTXXXAT are referred to collectively as FCT.

The Harris BiCMOS FCT Family has the lowest quiescent and operating power when compared to Bipolar and BiCMOS competing families (Figure 2). Figure 3 illustrates that FCT/A has speeds similar to Bipolar and BiCMOS families. FCTXXXAT is faster.

The many excellent features of the new Harris FCT BiCMOS bus-interface logic family are detailed in Table 1.

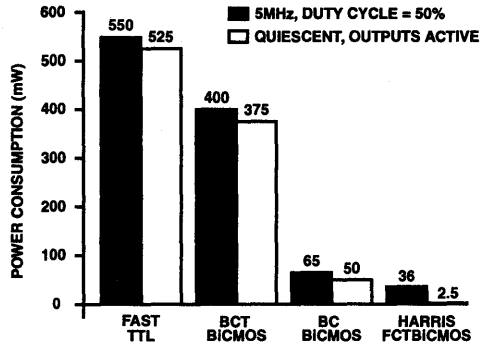


FIGURE 2. POWER CONSUMPTION COMPARISON, BUS-INTERFACE LOGIC FAMILIES

TABLE 1. FEATURES OF THE HARRIS BICMOS FCT FAMILY

FEATURES		
High Speed, Typical Delay = 3.5ns		
FCTXXXAT is faster than FAST		
Low Power	Typical Power/Function	
Quiescent	0mW	
5MHz	5.6mW	
10MHz	11.2mW	
Output Sink Current		
Buffers	.64mA, 70°C	
FF/Latches	.48mA, 70°C	
Limited Output Voltage Swing (for reduced noise generation)		
3.5V Typical		
No Diode Clamps from Inputs or Outputs to V_{CC}		
Minimized Switching Noise Design, Layout, and Packaging		
Low Ground Bounce - Typically 1.2V		
Reduced EMI Due to Slowed Output Edges		
Good Input Dynamic Noise Immunity (via isolated ground system and input hysteresis)		
ESD: ±2kV (HBM)		
No Latch-Up to Above ±300mA		
Variety of Bus-Interface Functions		
Buffers	Octal	
	10-Bit	
Flip-Flops/Registers	Octal	
	9-Bit	
	10-Bit	
	Special Registers	
Transceivers	Octal	
	9-Bit	
	10-Bit	
Latches	Octal	
	9-Bit	
	10-Bit	

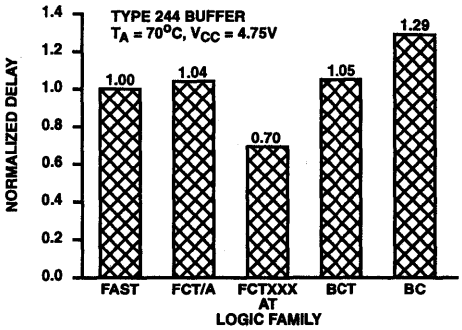


FIGURE 3. NORMALIZED PROPAGATION DELAY, AVERAGE OF t_{PLH}, t_{PHL}, t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH} MAXIMUMS (ADJUSTED FOR TEMPERATURE AND VOLTAGE WHERE NECESSARY)

Applications

Meeting Bus Standards

As illustrated in Table 2, Harris FCT BiCMOS bus-interface ICs match up ideally to the popular VMEbus, Multibus II, and other open or proprietary bus standards that require similar high speed performance and high sink-current capability.

TABLE 2. 32-BIT COMPUTER BUS STANDARDS

BUS	IEEE STD. NO.	DRIVER TECHNOLOGY
VMEbus	1014	TTL/FCT
NuBus	1196	TTL/FCT
Multibus II	1296	TTL/FCT
IBM Micro Channel Architecture (MCA)	None	TTL/FCT
Extended Industry Standard Architecture (EISA)	None	TTL/FCT
Sun Microsystems Sbus	None	CMOS/FCT

FCT vs AC/ACT Use

The Harris BiCMOS FCT bus-interface products complement the existing popular Harris AC/ACT logic family. The fundamental difference between these two families is that FCT is capable of sinking the 48mA or 64mA required for back-plane interface, while the AC/ACT family parts provide a balanced ±24mA output drive current capability in all logic and bus-interface family members. Table 3 describes the application of FCT vs AC/ACT.

TABLE 3. FCT vs AC/ACT APPLICATION

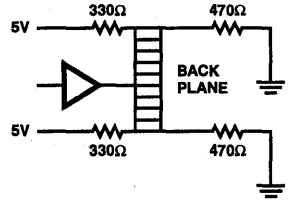
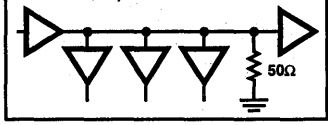
APPLICATION	FCT	AC/ACT
1. Drive Worst Case VME, Multibus II, or other backplane specified around higher power FAST TTL bus drivers. Requires 64mA sink current for clocks and strobes. 	Yes	No
2. Drive 50Ω PCB trace, coax, twisted pair, flat cable, etc. Maintain incident edge switching at both ends or any tap. (Source current of FCT is not sufficient.) 	No	Yes

TABLE 3. FCT vs AC/ACT APPLICATION (Continued)

APPLICATION	FCT	AC/ACT
3. Highest speed, lowest power, most noise immune logic system or bus interface system without line terminations	No	Yes (AC)
4. Driving memory input or CMOS Logic/ASIC inputs that require a balanced rail-to-rail logic swing	No	Yes
5. Bus Interfaces that need 24mA or less sink current	Yes	Yes
6. Interfaces between equipment with separate power supplies	Yes (No I/O Clamp Diodes)	No
7. Complete logic family including SSI (Gates) and MSI logic functions	No	Yes

FCT IC Process Technology

Harris BiCMOS FCT devices are fabricated in a 1.5mm BiCMOS process (See Figure 4). The basis of this process is a silicon-gate CMOS, double-level-metal, N-well configuration. To this, the necessary steps are added to create an additional physical layer called P ISO. The P ISO layer is used to construct uncommitted diodes and uncommitted bipolar NPN transistors. (Intrinsic diodes and bipolar transistors exist in processes that lack this additional layer, i.e. pure CMOS processes, but these devices are not uncommitted).

A heavily doped P substrate is topped with a thin epitaxial layer of lightly doped P material. The heavy doping of the substrate and small geometries within the epitaxial layer minimize the resistances encountered in these regions, thereby virtually eliminating the occurrence of latch-up. Injected currents flow through the low impedance substrate to ground without triggering any parasitic SCRs (See Latch-Up Sensitivity in this section).

The self-aligning nature of the silicon-gate process serves to reduce parasitic capacitance associated with the CMOS transistors, thereby increasing performance of the circuitry. Two levels of metallization provide for more efficient routing of interconnect, power and ground lines.

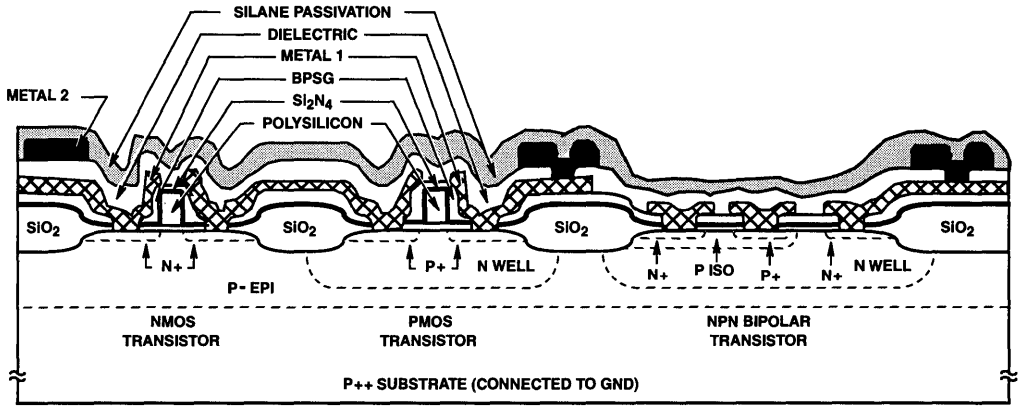


FIGURE 4. HARRIS FCT BiCMOS 1.5μm PROCESS CROSS SECTION

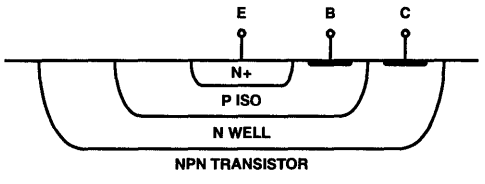


FIGURE 5. SIMPLIFIED DRAWING OF BIPOLAR NPN TRANSISTOR

Input Protection

FCT device inputs are protected by the network shown in Figure 6. This network protects the device against electrostatic discharge (up to at least 2kV for the human body model), which occurs in the normal handling of such components, as well as transients associated with normal operation in a system environment.

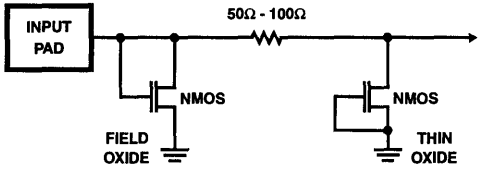


FIGURE 6. FCT INPUT PROTECTION NETWORK

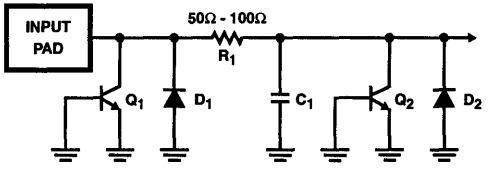


FIGURE 7. PARASITIC ELEMENTS IN THE CIRCUIT OF FIGURE 6

The operative elements in the protection mechanism are actually parasitic devices that exist in the network. These are shown in Figure 7. Whenever two N-type regions are formed within a P-type material to create an NMOS transistor, a parasitic NPN bipolar transistor results. The P-material, which is tied to ground, acts as the base. Q_1 in Figure 7 is the NPN device associated with the field oxide NMOS transistor in Figure 6, and Q_2 results from the construction of the thin oxide NMOS device. Diode D_1 and Diode D_2 are actually the base-collector junctions of transistor Q_1 and transistor Q_2, respectively, but are drawn separately for illustration. Primary protection is provided by Q_1, which will go into breakdown for positive input voltages greater than about 15V. (The gate oxide of the input inverter that follows the protection can withstand up to about 25V to 30V). For negative input voltages, diode D_1 simply conducts in the forward region. Secondary protection is provided by the remaining components, R_1, C_1, Q_2 and D_2. The combination of R_1 and C_1 will attenuate high speed transients, and Q_2/D_2 will behave in a similar manner to Q_1/D_1. The field oxide NMOS device itself would turn on if the input reached a level of about 18V.

Input Structure

The circuit diagram for the input structure of Harris BiCMOS FCT devices is shown in Figure 8.

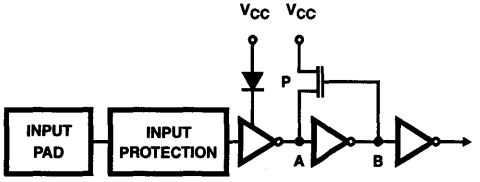


FIGURE 8. FCT INPUT STRUCTURE

The details of the input protection circuit are discussed in the preceding section. Following the input protection network is an inverter stage designed for TTL level inputs. The switchpoint of the inverter is lowered from the typical $V_{CC}/2$ value

for CMOS level inputs to a value near the middle of the range between the TTL V_{IH} and V_{IL} limits. A simple method for lowering the switchpoint of an inverter is to increase the width of the N-transistor. However, using this method alone requires a considerable increase in the size of the N-transistor. The total increase in chip area becomes significant when this is done for all inputs. So, instead of using all of this chip area, Harris has added a diode to the V_{CC} line of the inverter. The diode itself lowers the switchpoint by one diode drop, thereby allowing for a much smaller increase in the width of the N-transistor.

The diode also lowers the output high level of the input inverter by one diode drop. So, in order to reduce flow-through current in the next stage, a P-transistor pull-up is used. This device turns on after node A switches high and node B switches low, and then pulls node A all the way up to the rail.

An additional benefit of the P-transistor is that it requires a slightly higher input voltage to switch node A back low again. This input hysteresis provides added immunity against ground bounce and other similar transients on the inputs.

Output Structure

The circuit diagram for the output stage used in Harris BiCMOS FCT devices is shown in Figure 9.

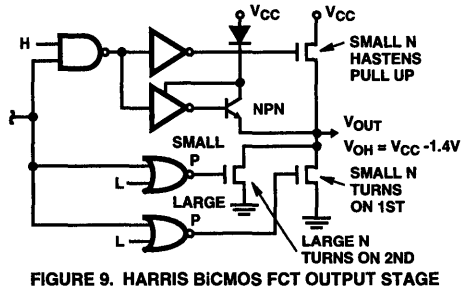


FIGURE 9. HARRIS BiCMOS FCT OUTPUT STAGE

Output Source Structure

The pull-up structure of FCT outputs is designed to eliminate the intrinsic protection diode from the output to V_{CC}, and to limit the output high voltage (V_{OH}) to 2 diode drops below V_{CC}.

The intrinsic protection diode to V_{CC} is removed by eliminating the P-transistor that would appear in a pure CMOS output structure. Instead of a P-channel pull-up, a bipolar NPN transistor in an emitter follower configuration is used. A small N-transistor is also used in parallel with the NPN, but the former drops out as the output voltage rises (i.e. as its gate to source voltage decreases). The benefits of eliminating the intrinsic diode to V_{CC} are ease of application in bus systems utilizing multiple power supplies, and in battery backed-up systems or other systems that are partially powered down. To provide protection for the outputs, a protection network is used that is similar to the input protection network, but without the series resistor.

The supply level for the collector of the NPN transistor and the inverter preceding the transistor is one diode drop below the V_{CC} level for the rest of the chip. The high level output of the inverter (i.e. the base of the NPN) is thus limited to one diode drop below V_{CC}. In turn, the high level voltage at the output pin, from the emitter of the NPN transistor, follows the base voltage minus the diode drop across the base emitter junction. The advantages of a reduced output swing are reduced ground bounce and reduced EMI generation. Both of these result from the slower edge rate produced by decreasing the change in voltage for a given change in time. More information on ground bounce and EMI is available in other sections of this overview and in the references listed at the end of the overview.

Output Sink Structure

The pull-down structure of FCT outputs (also shown in Figure 9) is designed to sink 48mA/64mA under static conditions (more on a dynamic basis), and to spread out over time the transient current associated with switching the outputs.

The distribution of transient current is achieved through the use of two, differently sized N-transistors in parallel. The logic gates driving the N-transistors are designed such that the smaller N turns on first. This smaller N-transistor discharges the capacitive load at a slower rate than the larger device, resulting in lower ground bounce. The larger N-transistor, which is needed to provide the bulk of the static drive capability, turns on after the transient current (and V_{OLP}) have already peaked (See Figure 10). For more information on ground bounce/V_{OLP} see the following section entitled Ground Bounce and Simultaneous Switching Transients.

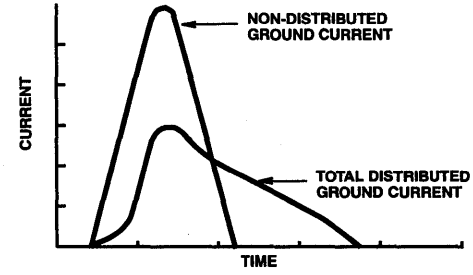


FIGURE 10A. NON-DISTRIBUTED vs TOTAL DISTRIBUTED

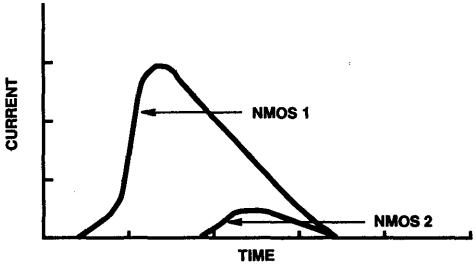


FIGURE 10B. COMPONENTS OF TOTALDISTRIBUTED CURRENT

FIGURE 10. TRANSIENT SINK CURRENT

Ground Bounce and Simultaneous Switching Transients

Ground bounce and V_{CC} bounce are caused by the transient currents associated with switching capacitive loads. These transient currents cause voltage spikes across intrinsic inductances in the output source and sink paths of digital logic devices (See Figure 11).

Figure 12 shows the case of an FCT output switching from high to low. Transient current i flows through the total intrinsic inductance to system ground, causing a peak voltage differential (V_{LMAX}) between the on-chip ground and the system ground.

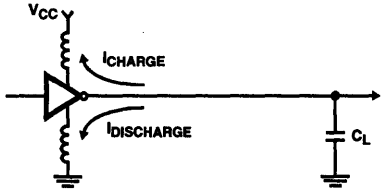


FIGURE 11. OUTPUT TRANSIENTS DUE TO LOAD CAPACITANCE

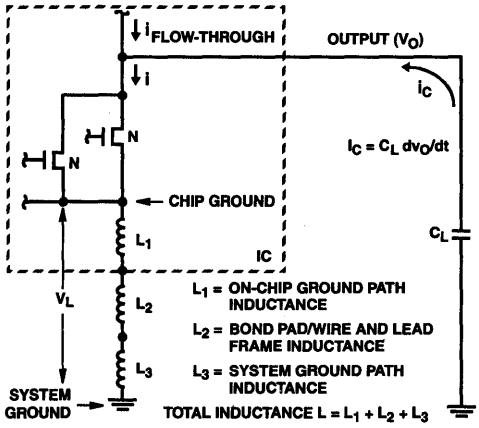


FIGURE 12. INDUCTANCES AND TRANSIENT CURRENTS RELATED TO GROUND BOUNCE

V_{LMAX} is seen as the positive peak value of the voltage waveform appearing across the inductance. This waveform (V_L) is shown in Figure 13A and is described by the following equation:

$$V_L = L\frac{di}{dt} \qquad \text{(EQ. 1)}$$

Figure 13B defines V_{LMAX} as a JEDEC standard parameter V_{OLP}; each data sheet specifies a typical value for V_{OLP} as well as a typical value for V_{OHV}, also defined in Figure 13B.

This internal ground bounce is coupled through the chip to the other outputs of the device, where the peak is measured as V_{OLP}. The magnitude of V_{OLP} for a given output depends on the magnitude of V_{LMAX} and the characteristics of the signal path for that particular output.

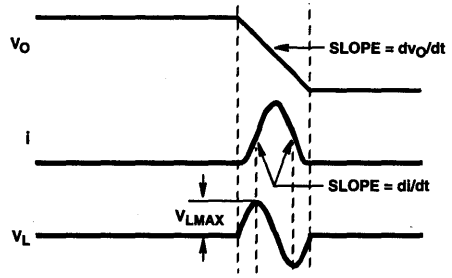
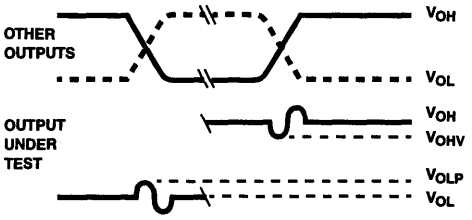


FIGURE 13A. WAVEFORMS FOR CIRCUIT OF FIGURE 12



NOTES:

1. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
2. Input pulses have the following characteristics: $P_{RR} \leq 1MHz$, $t_r = 2.5ns$, $t_f = 2.5ns$, skew 1ns.
3. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 13B. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS.

Since all of the device outputs have a common ground, the transient currents, and hence the likelihood of higher internal ground bounce, will increase with the number of outputs switching simultaneously. Also, there is mutual coupling among output signal paths which causes varying levels of V_{OLP} for a given output, depending on the particular combination of outputs that are switching simultaneously.

Worst case V_{OLP} for ICs with end pin V_{CC} and GND is measured at the output located farthest from the GND pin with all other outputs switching simultaneously from high to low. See Application Note AN9001, "Measurement of Ground and V_{CC} bounce in Advanced High Speed (AC/ACT/FCT) CMOS Logic ICs". See Section 9, "Harris' On-Line Services".

Reducing Ground Bounce

Taking another look at Equation 1 and noting that (i) itself is a function of dv_O/dt, it is seen that either a reduction in total inductance (L) or a reduction in the rate of change of the out-

put edge (dv_O/dt) will result in decreased internal ground bounce. Harris has taken steps in both of these directions to reduce ground/V_{CC} bounce and simultaneous switching transients in FCT devices.

1. Layout techniques are used to reduce on-chip inductance in the V_{CC} and ground paths, especially for the segments that are common to all outputs. (See L_1 in Figure 12).
2. Multiple bond-pads and bond-wires are used for V_{CC} and GND to reduce the inductance, in those paths, between the chip and the lead. (See L_2 in Figure 12).
3. Lead frames are modified to create a ground plane. This also reduces L_2.
4. By switching from 0V to 3.5V, Harris BiCMOS FCT outputs provide a reduction in dv_O/dt over parts that switch from 0V to 5V in the same amount of time.
5. Additionally, for high to low output transitions, the distributed pull-down structure lowers di/dt by reducing the peak amplitude and increasing the duration of the transient current waveform.

(For item 4 and item 5 above, see the output structure description under this heading).

V_{OLP} is further reduced in Harris FCT through the use of layout techniques that minimize the mutual coupling among outputs, and also between inputs and outputs.

Input Hysteresis

In addition to reducing ground bounce/V_{OLP}, Harris has increased the immunity of FCT to such transients, as well as any other ground noise, by adding hysteresis to the inputs. (See the input structure discussion earlier in this overview).

Latch-Up Sensitivity

Latch-up is an undesired state which occurs when a parasitic SCR, formed in ICs containing CMOS circuitry, is triggered. This parasitic SCR structure is shown in Figure 14. Triggering is caused by overvoltages or undervoltages (on input, output, or supply pins) which cause current to be injected into the substrate (i.e. to flow through substrate diodes). Once the device is triggered, a low impedance path is formed between V_{CC} and GND, thus allowing potentially destructive current (I_C) to flow through the chip.

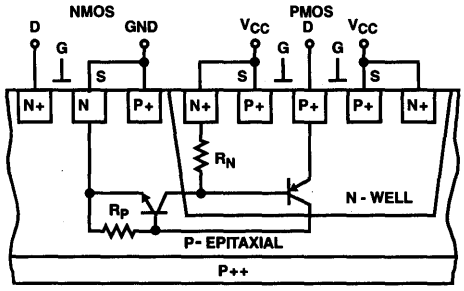


FIGURE 14A. CROSS SECTION OF CMOS STRUCTURE SHOWING SCR LATCH-UP PARASITIC TRANSISTOR

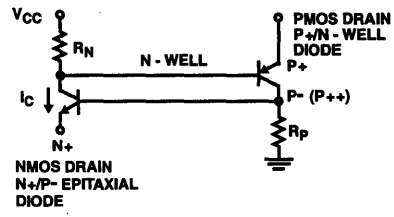


FIGURE 14B. SIMPLIFIED DIAGRAM

The Harris BiCMOS FCT process employs a thin epitaxial layer of lightly doped P material. This allows for heavier doping of the P substrate, which lowers the resistance of the substrate. The resistance of the EPI layer is limited by its small thickness and through liberal use of contacts to GND. Similarly, the N-well resistance is limited by its dimensions and through the use of contacts to V_{CC}. Lowering the resistance of these regions increases the amount of current required to produce the biasing voltages needed to turn on the bipolar transistors, thereby significantly reducing the probability of triggering a parasitic SCR.

The use of the EPI layer, contacts, and other design and layout techniques result in resistance to latch-up for transient currents up to over 400mA, typical, at any input or output. The absolute maximum DC rating, as specified in the JEDEC Standard No. 18A, is -20mA at the inputs and -50mA at the outputs.

DC Electrical Specifications

All DC and AC specifications of Harris BiCMOS FCT Bus-Interface ICs meet the industry standard JEDEC Standard No. 18A specifications.

Absolute Maximum Ratings

Note the conservative 6V absolute maximum DC supply voltage which, literally, means that Harris reliability data is based on long term operation at 6V and 125°C. For short term overvoltage and conducted transients, the supply voltage can increase to 10V or more. For the maximum rated DC input, output, V_{CC}, and ground currents shown, Harris design rules for internal chip metallization cross sections are such that there is no long term degradation of the Si-Al interconnect traces. Peak switching transient currents for V_{CC}, ground, and output traces may be higher (up to 1A) and are easily handled by the generous cross sectional area of the interconnect.

For free air power dissipation the thermal resistance of the plastic DIPs is 125°C/W, and for SOPs is 167°C/W.

Recommended Operating Conditions

All plastic packaged 74 series devices may be reliably operated over the full temperature range of 0°C to 70°C. The recommended input slew rate of 10ns/V translates to the following maximum rise and fall times:

V_{IN} = 3V; t_r, $t_f \leq$ 24ns, 10% to 90%

V_{IN} = 5V; t_r, $t_f \leq$ 40ns, 10% to 90%

Please make note of the fact that switching speeds are specified and tested for input rise and fall times of 3ns.

For practical application purposes, the switching speeds and power dissipation prediction equations (shown later in this overview) are useful for up to 10ns input rise and fall times. There exists a range of capacitive loading (up through 150pF) for which FCT outputs will be within this range.

DC Electrical Specifications

The Harris BiCMOS FCT family DC ratings are shown in the DC Electrical Specifications table. Refer to Table 4 for the by-type output sink current (I_{OL}) and output source current (I_{OH}). Note that the critical I_{CC} quiescent current is 80μA at 70°C. The JEDEC limit, and competition's specification, is 1.5mA. Clearly, for battery power or battery back-up the Harris FCT is the preferred product.

TABLE 4. TABLE 4. OUTPUT DRIVE CURRENT FOR 74FCT (0°C TO 70°C)

DEVICE NUMBER	I_{OH} (mA)	I_{OL} (mA)
74FCT240	15	64
74FCT244	15	64
74FCT245	15	64
74FCT273	15	48
74FCT373	15	48
74FCT374	15	48
74FCT540	15	64
74FCT541	15	64
74FCT543	15	64
74FCT564	15	48
74FCT574	15	48
74FCT646	15	64
74FCT651	15	64
74FCT652	15	64
74FCT653	15	64
74FCT654	15	64
74FCT821A-824A	15	48
74FCT841A-844A	15	48
74FCT861A	15	48
74FCT863A	15	48

Input Current vs Input Voltage

Figure 15 is the typical I_{IN} vs V_{IN} characteristic at $T_A = 25°C$ for FCT devices. From V_{IN} = 0V to 10V the only current flowing is leakage current (typically 100nA). At about -0.8V the input diode to ground starts to conduct. This diode clamps the input voltage at approximately -1V. Under this condition input current should be limited to -20mA DC; 1A for peak transients of a few ns. Switching Current vs Input Voltage, Figure 16, shows the typical DC switching characteristics for an FCT input. Current (between V_{CC} and ground) begins to flow at approximately 0.7V and peaks at about 1.4V. At the maximum current point the N and P transistors are both on and present the least resistance between V_{CC} and ground. Note that for a typical TTL V_{IL} of 0.25V to 0.4V, I_{CC} is below 1μA.

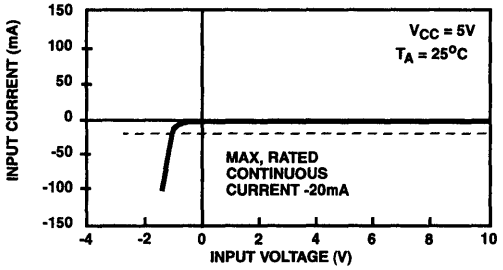


FIGURE 15. FCT INPUT CHARACTERISTIC

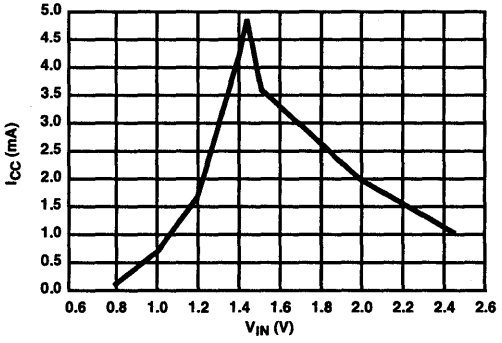


FIGURE 16. SUPPLY CURRENT vs INPUT VOLTAGE FOR FCT (TYPICAL)

Sink Current Capability (I_{OL} vs V_{OL})

Figure 17 shows the typical output sink capability of an FCT 240 under various conditions from worst case, at V_{CC} = 4.5V and $T_A = 125°C$, to best case, at V_{CC} = 5.5V and $T_A = -55°C$. At V_{OL} = 0.55V, the output voltage at which 64mA is specified (at 5V, 25°C and 4.75V, 70°C) the curves indicate typical values of 120mA and 90mA, respectively. For V_{CC} = 4.5V and 125°C, and V_{OL} = 0.55V, the curve shows a typical value of 80mA which far exceeds the 48mA specified in the DC Electrical Specifications chart.

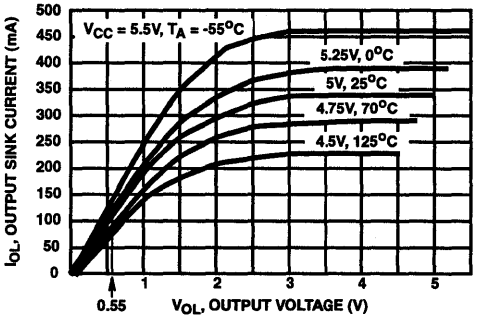


FIGURE 17. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE FOR FCT

Source Current Capability (I_{OH} vs V_{OH})

Figure 18 shows the typical output source capability under the same conditions as in Figure 17. In these curves, at V_{OH} = 2.4V the typical currents at 25°C and 70°C are -69mA and -49mA, respectively; the minimum limit is -15mA. At 125°C and V_{OH} = 2.4V the curve shows -35mA; the minimum specified value is -12mA.

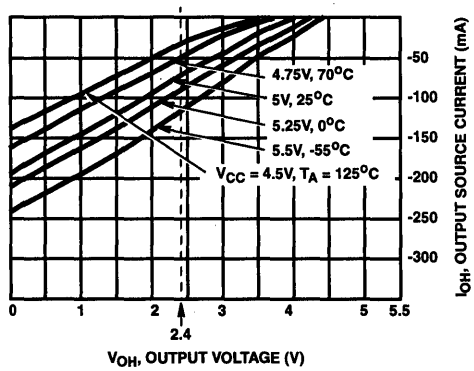


FIGURE 18. OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE FOR FCT

At the colder temperatures of 0°C and -55°C the current drive, both sink and source, is substantially higher.

The X-intercepts of Figure 18 show the FCT output voltage for CMOS input loads (defined as I_{IN} = 1µA, typically I_{IN} is a few nA). Table 5 summarizes V_{OH} for strictly CMOS loads. The data in this table is useful in FCT-to-CMOS (HC/HCT or AC/ACT) interface design, which is covered in AnswerFAX document number 7001, "System Design".

Shown in Figure 19 is the FCT test circuit. A Thevenin equivalent may be used for output loading.

TABLE 5. V_{OH} FOR CMOS LOADS; I_{OH} = 1µA (Figure 18)

V_{CC} (V)	T_A (°C)	V_{OH} (V)
4.50	125	3.5
4.75	70	3.7
5.00	25	4.0
5.25	0	4.2
5.50	-55	4.4

Dynamic Characteristics

Switching Speed

Since FCT is a low-power drop-in replacement for Fairchild Advanced Schottky TTL (FAST) 8-bit, 9-bit and 10-bit devices, the propagation delay specifications are set to equal those of the FAST family. As such, FCTXXX/A is generally the same speed as the Advanced CMOS Logic (AC/ACT) family, which should be considered a complementary, rather than competing, family. FCTXXXAT, however, is an average of 30% faster than either FAST or AC/ACT, thus creating a new speed standard that bipolar TTL cannot match. To keep switching noise under control and meet FCC emission specifications while using these extremely fast ICs, the system designer should employ transmission-line terminations, superior decoupling, and careful PC board layout.

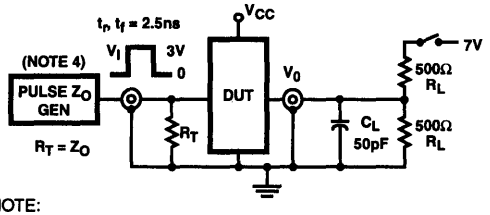
The speed of an octal interface IC is usually characterized by the propagation delay on a single channel. For example, the CD74FCT240 Octal Inverting Buffer/Line Driver is specified for a maximum t_{PHL} and t_{PLH} of 8.0ns when operating in an ambient temperature (T_A) between 0°C and 70°C. It should be noted that all FCT specifications apply to both output signal transition directions: LH/HL, ZH/ZL, and LZ/HZ, whereas FAST frequently specifies widely different t_{PLH} and t_{PHL} values. Most designers will have to use the slower of the two values in their designs. Switching-speed parameters for FCT device types match those of JEDEC standard No. 18A. Harris FCT ICs are offered primarily in the commercial (0°C to 70°C) temperature range. Two types (244E and 245E) are offered in the extended (-55°C to 125°C) temperature range. Figures 19 to 23 depict the JEDEC standard for the switching-speed test circuit and timing waveform definitions. These are the same that are used for FAST and AS but differ slightly from those used to test AC/ACT.

FCTXXXAT - Higher Speed Version

Harris offers BiCMOS FCT products in two speed grades: Base speed and higher speed. The base speed version of each type is designated as either FCTXXX or FCTXXXA (the latter for 800 or 2900 series types). The higher speed versions are designated as FCTXXXAT when the base version is FCTXXX. The "T" serves to emphasize the fact that Harris FCT devices provide a TTL-like output swing, thereby reducing ground bounce. (The Harris base speed versions also offer this feature, but since those parts and numbers have already been established, they will not be changed.) Some examples:

BASE FCT PRODUCT	HIGHER SPEED PRODUCT
CD54/74FCT245E	CD54/74FCT245ATE
CD54/74FCT245M	CD54/74FCT245ATM

Test Circuits and Waveforms



NOTE:

4. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 19. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

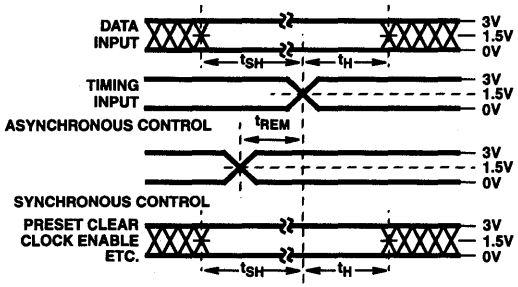


FIGURE 20. SETUP, HOLD, AND RELEASE TIMING

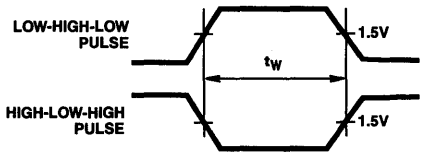


FIGURE 21. PULSE WIDTH

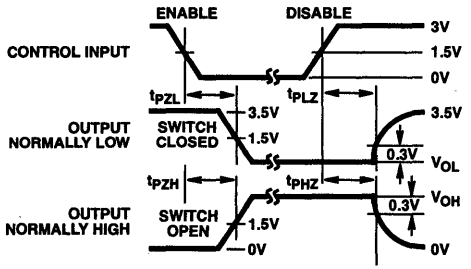


FIGURE 22. ENABLE AND DISABLE TIMING

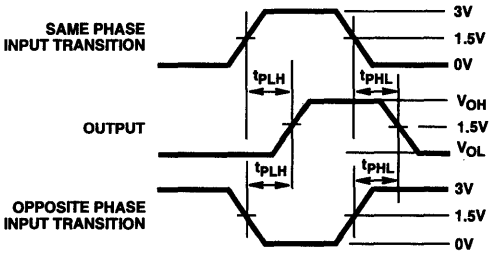


FIGURE 23. PROPAGATION DELAY

Harris BiCMOS FCTXXXAT high speed versions are, on the average, 30% faster than either FCT or FAST. Speeds are also faster than the AS, BCT, or BC bus interface families.

Speed vs Capacitive Load

Propagation delays for FCT interface types are determined using a JEDEC standard load as shown in Figure 24. The 50pF capacitor approximates a fan-out of 5-10 CMOS/TTL loads, which is reasonable for on-board operation, but probably too low for bus-interface applications. Figure 25 illustrates the effect of different capacitive loads on propagation delays. Above C_L = 50pF the delta delay is about 16ps/pF.

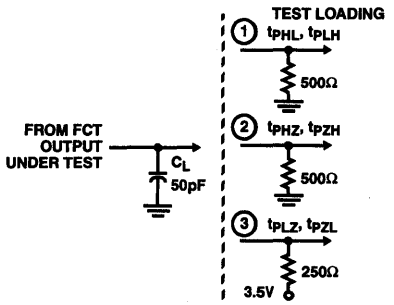


FIGURE 24. HARRIS (AND JEDEC) FCT TEST LOAD CIRCUITS

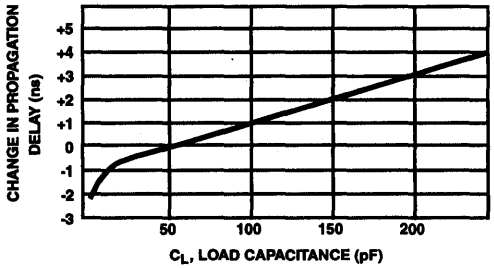


FIGURE 25. CHANGE IN PROPAGATION DELAY AS A FUNCTION OF LOAD CAPACITANCE FOR FCT

Propagation Delay vs Temperature and V_{CC}

The active delay and the delays caused by enabling and disabling outputs are plotted in Figures 26. Parameters t_{PLH}, t_{PHL}, t_{PLZ}, t_{PZL}, t_{PHZ}, t_{PZH} are shown as they vary over the temperature range of -55°C through 125°C and over the V_{CC} range of 4.50V to 5.50V. Mean data is for the FCT244 non-inverting buffer function.

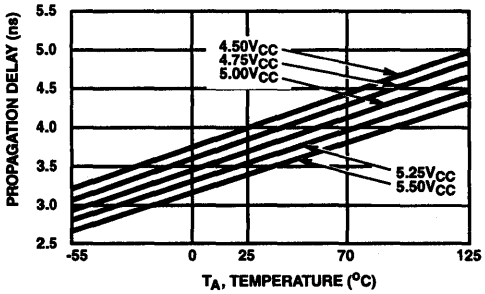


FIGURE 26A. t_{PLH}

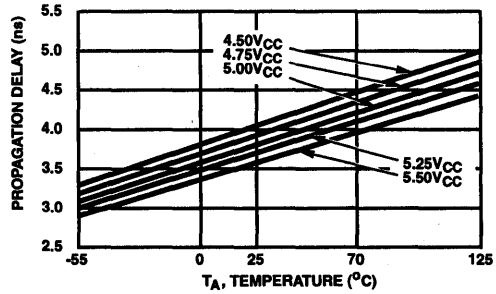


FIGURE 26B. t_{PHL}

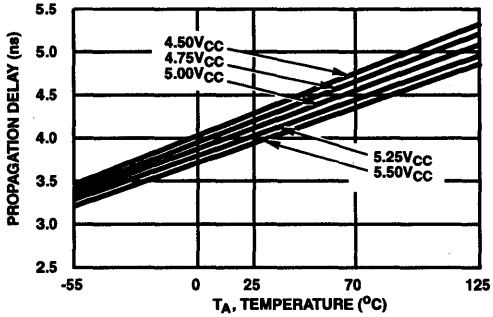


FIGURE 26C. t_{PLZ}

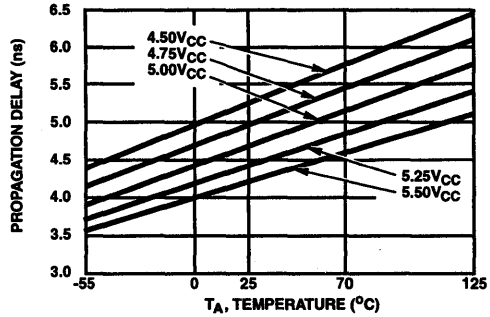


FIGURE 26D. t_{PZL}

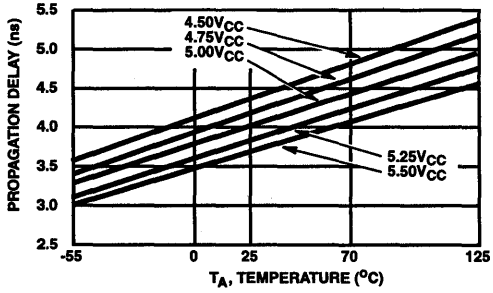


FIGURE 26E. t_{PHZ}

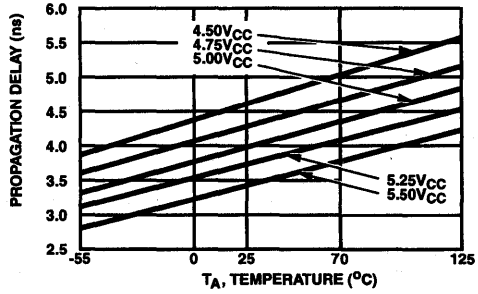


FIGURE 26F. t_{PZH}

FIGURE 26. MEAN PROPAGATION DELAY vs TEMPERATURE AND SUPPLY VOLTAGE FOR FCT

Min/Max Delay Issue and Solution

Figure 27 vividly illustrates the wide Min/Max delay spread of FCT data sheet (D/S) specifications. It is readily seen that for the CD74FCT373 part the design engineer would unhappily use a Min delay of 1.5ns and a Max delay of 8.0ns. This infers that for any two 373 octal latches making up a 16-bit-wide bus-interface, 8 bits could traverse the IC at 1.5ns while the other 8 bits take 8.0ns! This is a significant spread and can limit useful system clock frequency.

However, by making two simple adjustments to the Min/Max delays, a tighter set of useful design Min/Max delays are obtained:

1. Adjust ±0.5ns for built-in guardbands - used for test correlation of ICs, not design use.
2. Adjust for temperatures greater than 0°C and less than 70°C.

Rules for Useful Design Min/Max

1. t_P Min = D/S Min + 0.5ns + 0.01ns/°C
2. t_P Max = D/S Max - 0.5ns - 0.01ns/°C

These rules are applicable to t_{PLH}, t_{PHL}, t_{PZL}, t_{PLZ}, t_{PZH}, t_{PHZ}. In Figure 27A, the D/S and design values are shown; certainly a Min/Max range of 2.4ns to 7.4ns for a PCB operating at 50°C ±10°C is more useful than 1.5ns to 8.0ns.

Even more beneficial is application of the higher speed suffix "AT" FCT parts. As shown in Figure 27B, the design Min/Max spread is only 2.4ns to 5.1ns; this is very useful! The two design rules for Min/Max are applicable to all Harris BiCMOS FCT types.

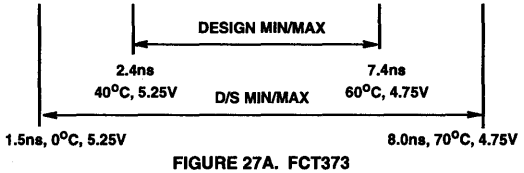


FIGURE 27A. FCT373

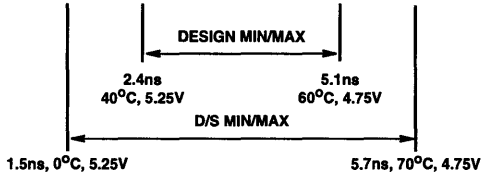


FIGURE 27B. FCT373AT

FIGURE 27. EXAMPLE SHOWING DESIGN VALUES vs DATA SHEET VALUES FOR MIN/MAX DELAYS

Delay Skew

Each 8-bit, 9-bit and 10-bit part will have propagation delay skews that fall into three categories:

- Pin to pin skew
- Simultaneous switching skew
- H-L vs L-H (edge) skew

Table 6 records the skew data for the three categories. Simultaneous switching skew is measured with 7/8 outputs switching rather than 8/8 due to the immediate availability of a good RF ground bounce fixture. Skew would be slightly larger for 8/8 switching. The largest incremental delay change occurs for 7/8 outputs switching H-L. The incremental change for the H-L skew is larger than that for the L-H skew due to output edge control circuitry.

Dynamics of Ground Bounce

Octal or 9/10-Bit bus-interface parts, when switching simultaneously, will have worst-case noise glitches on otherwise quiet outputs when N-1 of the N outputs all go HIGH or LOW at the same instant. In a practical sense, skew of the IC channels (up to 1ns) and skew of PCB interconnection (possibly 0.5ns to 1ns) will cause outputs to switch at slightly different times; therefore, this is a "Murphy's Law" exercise - what if all 7 outputs of an FCT octal (such as the popular 245 transceiver or the 373 latch) all switch H-L or L-H on top of each other? Figure 28A and Figure 28B show the ground bounce (V_{OLP}) noise glitch for Harris FCT245 and 373 types and Figure 24C shows the V_{CC} bounce (V_{OHV}) glitch for the FCT373 type - all very representative of the Harris IC and package design for minimized switching noise. In fact, the FCT373 devices used for these measurements operate at "AT" speed. Figure 29 shows the measured ground bounce of a competitor's FCT 245 IC. Ground bounce measurements for the competitor's FCT 245A are even higher. Application Note AN9001 provides a detailed description of Harris accurate Ground/V_{CC} Bounce Test PCBs and how readers may obtain one for their own measurements. (See Section 12). From the waveforms in Figures 28 and 29, a summary of useful observations is shown in Table 7.

TABLE 6. TYPICAL PROPAGATION DELAY SKEW FOR THE FCT245

OUTPUT		PROPAGATION DELAY (ns)					
		1/8 SWITCHING		7/8 SWITCHING		INCREMENT 1/8 TO 7/8	
PIN #	NAME	t_{PHL}	t_{PLH}	t_{PHL}	t_{PLH}	t_{PHL}	t_{PLH}
11	B7	5.19	5.09	6.32	5.68	1.13	0.59
12	B6	5.06	4.76	6.40	5.64	1.34	0.88
13	B5	5.14	4.75	6.40	5.60	1.26	0.85
14	B4	4.93	4.82	6.40	5.56	1.47	0.74
15	B3	5.12	4.78	6.40	5.56	1.28	0.78
16	B2	5.30	4.86	6.40	5.24	1.10	0.38
17	B1	5.22	4.86	6.40	5.24	1.18	0.38
18	B0	5.25	4.84	Quiet	Quiet	-	-
Pin to Pin Skew		0.37	0.34	0.08	0.44	-	-
Maximum Edge Skew		0.44		1.16		-	-
Maximum 1/8 to 7/8 Skew		-	-	-	-	1.47	

NOTE: V_{CC} = 5V, T_A = 25°C.

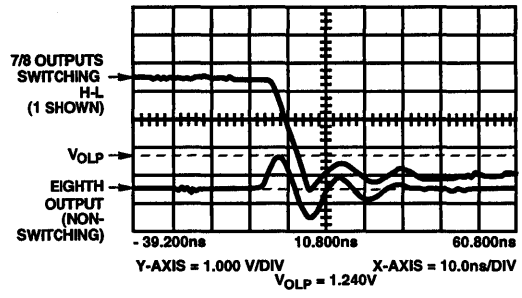


FIGURE 28A. HARRIS 245 - V_{OLP}

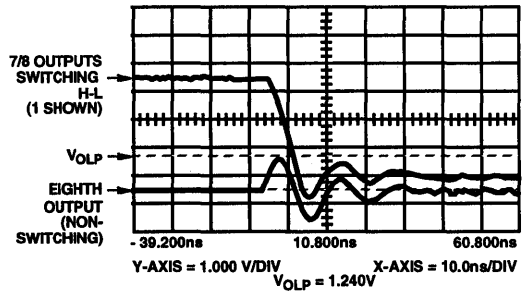


FIGURE 28B. HARRIS 245 - V_{OLP}

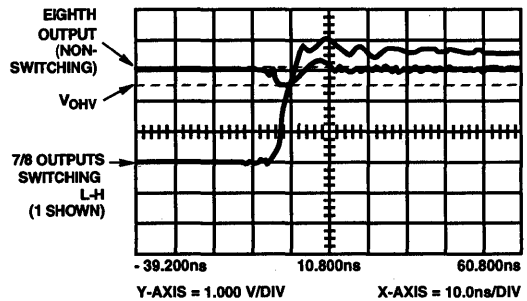


FIGURE 28C. HARRIS 373 - V_{OHV}

FIGURE 28. GROUND BOUNCE (V_{OLP}) AND V_{CC} BOUNCE (V_{OHV}) FOR HARRIS FCT

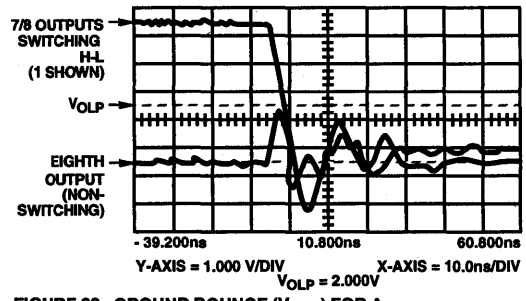


FIGURE 29. GROUND BOUNCE (V_{OLP}) FOR A COMPETITOR'S FCT

TABLE 7. SELECTED DATA FROM FIGURE 24 AND FIGURE 25

DEVICE TYPE	V_{OLP} (V)	UNDER SHOOT (V)	PULSE WIDTH AT 0.8V (ns)	V_{OHV} (V)
Harris FCT245/AT	1.24	0.83	3.0	-
Harris FCT373/AT	1.24	0.9	3.5	0.46
Competitive FCT245 Second Peak	2.00	0.85	3.0	-
	1.1	-	3.0	-

NOTES:

5. V_{OLP} exceeds D/S V_{IL} of 0.8V in all cases. Even the second peak of the competitive 245 ground bounce ringing waveform exceeds this limit.
6. Widths are under 3.5ns at 0.8V. This means that a wait time to strobe an output would be no longer than about 4ns after outputs switch H-L.
7. The one-of-seven switching outputs that is monitored for the Harris FCT device shows minimal undershoot and overshoot - illustrating benefits of designed-in ground/V_{CC} bounce minimization techniques. However, competitive H-L active output undershoots by 1.5V and falls faster - illustrating the lack of a slowing H-L edge control.

System Design Aspects of V_{OLP} and V_{OHV}

Although Harris BiCMOS FCT outputs might produce a peak ground bounce glitch of 1.25V, Harris BiCMOS FCT inputs will not respond. A built-in hysteresis circuit at each input adds about 0.2V to the input switchpoint voltage.

Power Consumption

Operating Current/Power

For Bus-Interface Logic ICs that are specified to match VME, Multibus II or other bus standards, FCT is clearly the lowest current drain family, and hence lowest heat dissipation family. Figure 30 is actual measured current up through 20MHz operation for 7/8 outputs switching into a 50pF load. Since V_{IH} is 3.5V, the I_{CC} component of FCT current drain is included; Figure 30 is a very real-world comparison of bipolar FAST, BiCMOS BCT, and Harris BiCMOS FCT. Results are very obvious for relative current drain; for example at standby (f = 0) FCT current drain is virtually zero while BCT and FAST are at 50mA and 75mA respectively. For a continuous clock, up through 20MHz, both FCT and BCT save power over FAST. Most importantly, for overall average current drain of data or address buffers, at 5MHz, FCT shows over a 2.5X savings in current, and a corresponding savings in power (or heat dissipation) in a system.

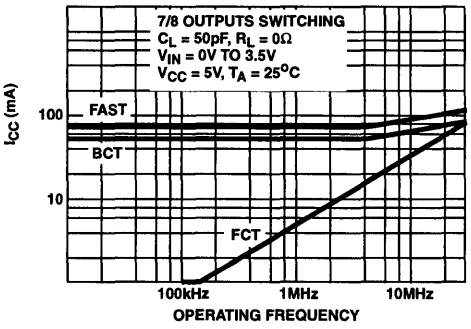


FIGURE 30. OPERATING CURRENT (I_{CC}) AS A FUNCTION OF OPERATING FREQUENCY FOR FAST, BCT, AND HARRIS FCT

Even for the Hi-Z mode, when outputs hanging on a bus are disabled, FCT saves 188X in standby or Hi-Z IC power consumption.

TABLE 8. FCT vs BCT POWER DISSIPATION COMPARISON

	I_{CC} MAXIMUM	POWER MAXIMUM
FCT	0.08mA	0.44mW
BCT	15mA	82.5mW

NOTE: V_{CC} = 5.5V, T_A = 70°C, Outputs Hi-Z, Data Sheet Values.

Power Estimating

The system designer needs to get a good handle on his PCB power consumption in order to specify his power supply, design for thermal control, and also to estimate decoupling capacitor sizes and ferrite bead currents for EMI control. Equation 2 shows the exact FCT power consumption equation per IC input or per IC function. Without going through the data sheets to extract parameters to put into this equation let's look at a concise set of values applicable to all Harris FCT types:

TABLE 9. PARAMETERS FOR CALCULATING POWER CONSUMPTION

PARAMETERS	TYPICAL V_{CC} = 5V T_A = 25°C	MAXIMUM V_{CC} = 5.25V T_A = 70°C	MAXIMUM V_{CC} = 5.5V T_A = 125°C
I_{CC}	0	80µA	500µA
ΔI_{CC}	0.4mA	1.6mA	2mA
C_{PD} (Note 1)	40pF	60pF	60pF

NOTE: Will vary somewhat with device type.

All other variables such as C_L per output, and input/output frequencies are estimates made by the system designer, remembering that average frequency (not peak) is used for power averaging.

$$P = \underbrace{I_{CC} V_{CC} + \Delta I_{CC} V_{CC} D + C_{PD} V_{CC}{}^2 f_i}_{\text{Per Input/Function}} + \underbrace{C_L (V_{CC} - 1.4V)^2 f_O}_{\text{Per Output/Function}} \quad \text{(EQ. 2)}$$

Where:

I_{CC} = Quiescent Current (From Data Sheet Ratings)

V_{CC} = Supply Voltage

f_i = Input Frequency

f_O = Output Frequency

C_{PD} = Device Equivalent Power Dissipation Capacitance; Used for Computing Internal Chip Power ≈ 40pF

C_L = Load Capacitance; Used for Computing Output Stage Power

ΔI_{CC} = Added Direct Current When V_{IN} = V_{CC} -2.1V (TTL Input High Level)

D = Duty Cycle of Input (Percent of Time High)

System Design Considerations

System Design Using Harris BiCMOS FCT

Successful system design using Harris BiCMOS FCT is assured if the fundamental DC drive and major speed considerations already covered are understood - and if "Golden Rules" of Design and PCB layout are followed. It is not enough simply to apply the static and dynamic characteristics in order to achieve excellent fault-free computer system operation, the system design engineer must also approach his hardware design task so as to stay within stringent EMI limits for conducted and radiated energy.

Ten Golden Rules for Successful Design with FCT

1. No Floating Inputs - Tie unused inputs to GND or V_{CC}. For transceiver I/O pins, return floating inputs to V_{CC} or ground via a resistor (100Ω or more) to avoid output shorts.
2. Decouple Each IC Correctly - Decoupling differs for data (non-periodic) signal ICs and clock (or periodic signal) ICs.
   A. Data/Address (non-periodic) - Place a decoupling capacitor with value C_D on same side of PCB as IC with shortest possible leads to V_{CC} and ground pins. Given a choice, put C_D closer to V_{CC} pin to minimize EMI on power buses. Placing C_D on the opposite side of the board is not as effective.

$$C_D = 9\,N\,C_{PD} + 9\sum_{1}^{N} C_L \quad \text{(EQ. 3)}$$

   N = Number of Functions in IC

   Also specify C_D to have:

   ESL < 10nH

   ESR < 0.5Ω

   B. Clock Generator and Driver ICs (Periodic Signals) - 20MHz to 40MHz periodic clocks, strobes, etc. have harmonics in the EMI band (150MHz and up) where FCC rules are stringent. Decouple periodic signal ICs with both a C_D and ferrite bead. Combination three terminal devices for this purpose are available (the Murata Erie DS 310 types, for example). Place on same side of PCB as IC.

3. Terminate Interconnects More than Six Inches in Length - VME, Multibus II, and other bus standards specify adequate Thevenin termination. Interconnects within a PCB may not need to be terminated but should be if they are six inches or more in length. This avoids reflection problems and also avoids crosstalk problems should two parallel PCB traces run alongside each other for six inches or more. A termination also keeps ground bounce noise glitches from increasing in amplitude much over 1.25V, thereby preventing these glitches from false triggering inputs.Terminations may be series, shunt, or Thevenin (See Figure 31).

4. Low-Voltage Operation - While Harris BiCMOS FCT may be operated below 4.5V, it was not designed for this purpose. Harris AC logic, operable down to V_{CC} = 1.5V is recommended for battery operation or battery backup. (References 5 and 6).

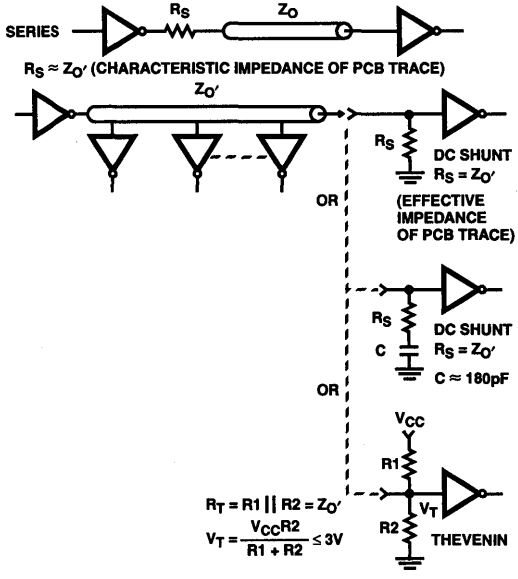


FIGURE 31. METHODS OF TERMINATION

5. Live PCB Insertion and Multi-System Interfacing is Safe With Harris BiCMOS FCT - Because Harris BiCMOS FCT (unlike other FCT) does not have input or output clamp diodes to V_{CC} there is no danger in live insertion of PCB with Harris BiCMOS FCT as buffers. With other buffers, live bus clocks or data can momentarily be loaded down causing loss of information. This problem will not occur with Harris BiCMOS FCT. Also interfacing between two systems having different power sources is facilitated.

6. Momentarily Shorting Outputs is Allowed But Restricted - If forced node testing is done, please be careful not to overheat the FCT IC (short only one output pin per package, for no more than 1s).

7. Interfacing FCT to Other Logic Families - Harris BiCMOS FCT Bus-Interface ICs interface easily to all other CMOS, Bipolar, and BiCMOS logic families directly as shown in Table 10. Note 1 applies to the interface between FCT devices and those that have CMOS switching levels (HC or AC); the only limitation is a reduced noise margin from what it would be if FCT had a full 5V swing. Harris BiCMOS FCT is intentionally designed to provide a reduced output swing. The user should understand that not swinging to 5V has overwhelming advantages, namely:

   A. Less crosstalk jeopardy

   B. Less switching noise, i.e. lower ground/V_{CC} bounce

   C. Less radiated and conducted EMI

TABLE 10. INTERFACING FCT AND OTHER LOGIC FAMILIES

	TO				
FROM	**FCT**	**HCT/ ACT**	**HC/AC**	**FAST AS ALS/LS**	**BC/FCT**
FCT	Direct	Direct	Direct (Note 8)	Direct	Direct
AC/ACT	Direct	Direct	Direct	Direct	Direct
HC/HCT	Direct	Direct	Direct	Direct	Direct
FAST AS/ALS/LS	Direct	Direct	(Note 9)	Direct	Direct
BC/BCT	Direct	Direct	(Note 9)	Direct	Direct

NOTES:

8. For Harris BiCMOS FCT to HC or AC logic families, the low logic level noise margin is 1.4V (V_{OL} < 0.1V and V_{IL}Max = 1.5V). The high logic level noise margin is as shown in Table 11.

9. For any of the TTL families (FAST, AS, ALS, LS) or the BC, BCT BiCMOS families, for low logic levels (V_{OL} to V_{IL}) there is a good noise margin of at least 1.2V. For high logic levels (V_{OH} to V_{IH}) the noise margin varies with family. If the manufacturer does not supply data like that shown in Table 11 for Harris BiCMOS FCT, then a pull-up resistor to V_{CC} at the interface is necessary.

8. Avoid Crosstalk Problems - As shown in Figure 32, if two PCB interconnect copper traces on the same layer run closely spaced in parallel for enough distance (L) without terminations, a noise glitch at B can be large enough to switch that input. Rules to avoid problematic crosstalk:

   A. For FCT keep L conservatively under six inches if runs have to be paralleled.

   B. If parallel runs exceed six inches, terminate with R_S = Z_0 of trace. Place a C of about 180pF in series with R_S to reduce power. Also a ground trace could be placed between runs.

   C. Best bet is to avoid parallel runs of over six inches. Use different PCB levels separated by a V_{CC} or ground plane.

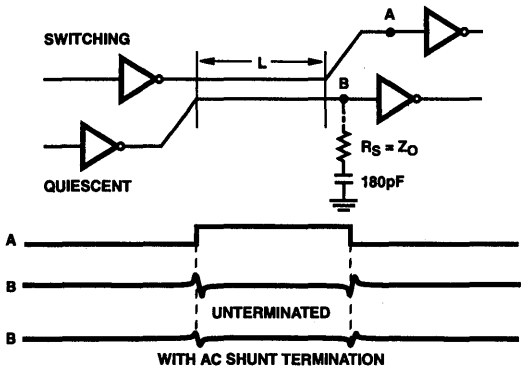


FIGURE 32. SIGNAL CROSSTALK RESULTS FROM PARALLEL TRACES AND IS REDUCED BY TERMINATION

9. Ground/V_{CC} Bounce Will Not Affect Performance with These Simple Rules:
   A. V_{CC} bounce is under 0.5V; usually not a problem.
   B. Ground bounce is about 1.25V, about half of that of competitive FCT, but above V_{IL}Max of 0.8V. Even though Harris BiCMOS FCT ground bounce is well below the input switchpoint, particularly with sufficient pulse width to false trigger an input, other system noise and/or DC offset of 0.2V to 0.3V above ground due to high DC loading could false trigger an input if the line is not terminated. Therefore, if an output with a potential for ground bounce exists, terminate with either series or shunt R_S as described in Rule 3 above. Remember, an unterminated line produces a signal of 2X amplitude at the end of the unterminated trace. This could easily cause false triggering. If ground bounce occurs at latch or flip-flop data inputs, its 3ns width at 0.8V and its centering right at the output edge (See Figure 28) is such that no extra strobe delay or system clock frequency reduction is needed.

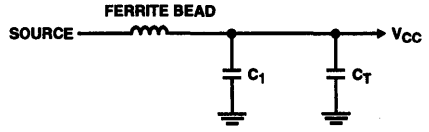
Because FCT inputs have typically 200mV of hysteresis, input dynamic noise margin remains above 0.5V in the presence of ground bouncing, i.e. internal stored data is not subject to loss for Harris BiCMOS FCT; this is a problem in competitive FCT which has 2V or more of ground bounce!

10. PCB Must Be Designed to Minimize EMI - Before initiation of the PCB layout and design, it is imperative that a comprehensive action plan to minimize EMI be put into place - realizing that high speed digital ICs are EMI spectrum generators. Whether it is FCT, AC/ACT, FAST, VLSI, ASICs or memory, with clock rates above 10MHz and switching edges below 5ns, PCB design for EMI containment will pay off in the end - designers will not have to apply painful "band-aids", or worse - scrap the PCB design, after equipment is built. Guidelines for EMI control in PCB application of FCT or like devices follow:
    A. Become familiar with EMI control measures - There are good comprehensive text books and reports available on PCB design spanning layout, decoupling, board materials, terminations, shielding, grounding, etc. Some of these are listed as references at the end of this section. Tutorial seminars are available from sources such as The Keenan Corporation listed as a reference. Absolute musts are summarized in the following notes.

TABLE 11. NOISE MARGINS FOR INTERFACING HARRIS BiCMOS FCT TO AC OR HC LOGIC

	FCT OUTPUT VOLTAGE			AC OR HC INPUT VOLTAGE		NOISE MARGIN	
LOW LOGIC LEVEL	V_{OL} < 0.1V			V_{IL} = 1.5V MAXIMUM		1.4V	
HIGH LOGIC LEVEL	V_{OH} (V)			V_{IH} (V)		NOISE MARGIN (V)	
	V_{CC} (V)	T_A (°C)	V_{OH} (V)	MINIMUM SPECIFIED	ACTUAL SWITCHING VOLTAGE	MINIMUM	ACTUAL
	4.50	125	3.5	3.15	1.90 to 2.60	0.35	0.90
	4.75	70	3.7	3.33	2.03 to 2.73	0.37	0.97
	5.00	25	4.0	3.50	2.15 to 2.85	0.50	1.15
	5.25	0	4.2	3.68	2.28 to 2.98	0.52	1.22
	5.50	-55	4.4	3.85	2.40 to 3.10	0.55	1.30

B. Decouple carefully.
   1. ICs as described in Rule 2 above.
   2. PCB power entry - each power plane area on PCB



C1 = 0.1μF RF CAPACITOR
C_{TMIN} = TANTALUM CAPACITOR EQUAL TO SUM OF ALL DECOUPLING CAPACITORS ON BOARD

FIGURE 33. DECOUPLING CAPACITORS AT POWER ENTRY POINT ON PC BOARD

C. Isolate IC block with separated power planes - On a multi-layer PCB (preferred over two-sided) use a separated V_{CC} plane for various system blocks such as high speed synchronous logic, I/O logic, memory, lower-speed logic, analog circuits. For each segmented V_{CC} area use separate power entry decoupling as illustrated in Figure 33.

D. Periodic Signal Buffers, Main Culprit - As discussed, take special care in decoupling, terminating, grouping, and laying out short ground return paths. It has been found [1-4] that most out-of-specification EMI frequency peaks are harmonics of periodic signals, and can be traced back to a violation of the "Golden Rules" covering periodic signals in the design of PCBs.

E. IC Placement - FCT as PCB I/O should be very close to the connector with its isolated V_{CC} plane. This minimizes the inductance of high current V_{CC} and ground paths. Group synchronous clocked logic and micros closely, again with a dedicated V_{CC} plane in an area close to PCB connector - but secondary to I/O. Slower speed and/or asynchronous logic should be grouped in a separate area with its own V_{CC} plane, and can be farther from connector. Likewise analog signal ICs must have separate V_{CC} and ground planes providing separate power entry.

F. Terminate - Terminations always reduce ringing on a PCB interconnect at FCT-like speed. Follow guidance of Rule 3 above.

References

[1] Harris Semiconductor, Application Note AN8906, "Noise Aspects of Applying Advanced CMOS (AC/ACT) Semiconductors," April 1989.

[2] R. Kenneth Keenan, "Decoupling and Layout of Digital Printed Circuits," The Keenan Corporation, Pinellas Park, FL.

[3] R. Kenneth Keenan, "Digital Design for Interference Specifications," The Keenan Corporation, Pinellas Park, FL.

[4] The Keenan Corporation, FCC Emissions and Power Bus Noise - 2nd Edition.

[5] Harris Semiconductor, Data Book SSD-283A, Advanced CMOS Logic ICs, October 1988.

[6] Nadolski, J. "Logic Designs for Battery-Powered or Battery Backed-Up Operation," Harris Semiconductor Application Note AN7373.

[7] JEDEC Standard No. 20, "Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High Speed CMOS Devices".

[8] JEDEC Standard No. 18A, "Standard for Description of 54/74FCTXXXX High Speed CMOS [/BiCMOS] Devices".

Family Ratings and Specifications

For specific technical information on each individual device type, refer to the apporpriate data sheet within this section.

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} ..... -0.5 to 6V
DC Input Diode Current, I_{IK} For V_I < -0.5V ..... -20mA
DC Output Diode Current, I_{OK} For V_O < -0.5V ..... -50mA
DC Output Sink Current Per Output Pin, I_O 70mA
DC Output Source Current Per Output Pin, I_O ..... -30mA
DC V_{CC}, Current, I_{CC} ..... $N(I_{OH}) + M(\Delta I_{CC})$ mA
DC Ground Current, I_{GND} ..... $N(I_{OL}) + M(\Delta I_{CC})$ mA
Where N = No. of Outputs
M = No. of Inputs

Operating Conditions

Operating Temperature Range, T_A
CD54 ..... -55°C to 125°C
CD74 ..... 0°C to 70°C
Operating Voltage Range
T_A = 0°C to 70°C (74 Series) ..... 4.75V to 5.25V
T_A = -55°C to 125°C (54 Series) ..... 4.5V to 5.5V
DC Input or Output Voltage, V_I, V_O ..... 0V to V_{CC}
Input Rise and Fall Slew Rate, dt/dv ..... 0ns/V to 10ns/V

Thermal Information

Maximum Storage Temperature, T_{STG} ..... -65°C to 150°C
Maximum Lead Temperature (During Soldering)
At Distance 1/16in. ± 1/32in. (1.59mm ± 0.79mm)
From Case for 10s Max ..... 265°C
Unit Inserted into a PC Board (Min Thickness 1/16in. or 1.59mm)
with Solder Contacting Lead Tips Only ..... 300°C
Maximum Power Dissipation per Package, P_D
Package E, EN
T_A = -55°C to 100°C 500mW
T_A = 100°C to 125°C .... Derate Linearly at 8mW/°C to 300mW
Package M
T_A = -55°C to 70°C 400mW
T_A = 70°C to 125°C ..... Derate Linearly at 6mW/°C to 70mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

74FCT Commercial Temperature Range 0°C to 70°C, V_{CC} = 4.75V Min to 5.25V Max
54FCT Inductrial Temperature Range -55°C to 125°C, V_{CC} = 4.5V Min to 5.5V Max

PARAMETERS	SYMBOL	TEST CONDITIONS V_I (V)	TEST CONDITIONS I_O (mA)	V_{CC} (V)	25°C MIN	25°C MAX	0°C TO 70°C MIN	0°C TO 70°C MAX	-55°C TO 125°C MIN	-55°C TO 125°C MAX	UNIT
High Level Input Voltage	V_{IH}	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15 (Note 10)	Min	2.4	-	2.4	-	-	-	V
			-12 (Note 10)	Min	2.4	-	-	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64 (Note 10)	Min	-	0.55	-	0.55	-	-	V
			48 (Note 10)	Min	-	0.55	-	-	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}	-	Max	-	0.1	-	1	-	1	µA
Low Level Input Current	I_{IL}	GND	-	Max	-	-0.1	-	-1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}	-	Max	-	0.5	-	10	-	10	µA
	I_{OZL}	GND	-	Max	-	-0.5	-	-10	-	-10	µA
Short Circuit Output Current (Note 8)	I_{OS}	V_{CC} or GND V_O = 0	-	Max	-60 (Note 10)	-	-60 (Note 10)	-	60 (Note 10)	-	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin, TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4 (Note 9)	-	Max	-	1.6	-	1.6	-	2	mA

NOTES:
10. Unless otherwise specified, all voltages are referenced to GND.
11. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
12. Inputs that are not measured are at V_{CC} or GND. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Chart, e.g., 1.6mA Max at 70°C.
13. Values are for FCT240 types (See Table 4 for I_{OL} and I_{OH} for other types).

CD74FCT240, CD74FCT240AT, CD74FCT244, CD74FCT244AT

BiCMOS FCT Interface Logic, Octal Buffers/Line Drivers, Three-State

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 4.1ns at V_{CC} = 5V, T_A = 25°C
- CD74FCT240, CD74FCT240AT
  - Inverting
- CD74FCT244, CD74FCT244AT
  - Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- CD74FCTXXX Types - Speed of Bipolar FAST™/AS/S
- CD74FCTXXXAT Types - 30% Faster Than FAST™/AS/S with Significantly Reduced Power Consumption
- 64mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Description

The CD74FCT240, CD74FCT240AT, CD74FCT244, and CD74FCT244AT three-state octal buffers/line drivers use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capabile of sinking 64mA.

The CD74FCT240, CD74FCT240AT, CD74FCT244, and CD74FCT244AT have active LOW output enables ($\overline{1OE}$, $\overline{2OE}$).

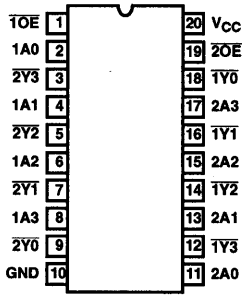
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT240E	0 to 70	20 Ld PDIP	E20.3
CD74FCT240ATE	0 to 70	20 Ld PDIP	E20.3
CD74FCT244E	0 to 70	20 Ld PDIP	E20.3
CD74FCT244ATE	0 to 70	20 Ld PDIP	E20.3
CD74FCT240M	0 to 70	20 Ld SOIC	M20.3
CD74FCT244M	0 to 70	20 Ld SOIC	M20.3
CD74FCT240SM	0 to 70	20 Ld SSOP	M20.209
CD74FCT244SM	0 to 70	20 Ld SSOP	M20.209

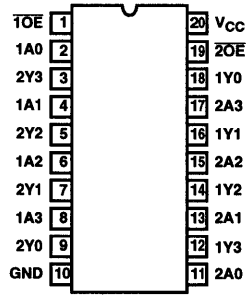
NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinouts

CD74FCT240, CD74FCT240AT
(PDIP, SOIC, SSOP)
TOP VIEW



CD74FCT244, CD74FCT244AT
(PDIP, SOIC, SSOP)
TOP VIEW



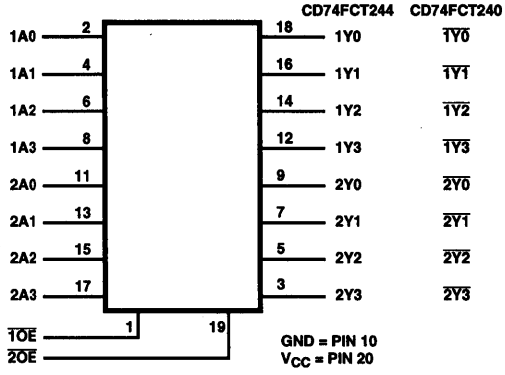
8 BiCMOS FCT PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number 2227.4

Functional Diagram



CD74FCT240, CD74FCT240AT TRUTH TABLE

CD74FCT240, CD74FCT240AT		
INPUT	INPUT	OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

CD74FCT244, CD74FCT244AT TRUTH TABLE

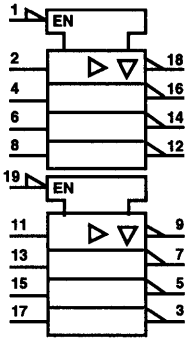
CD74FCT244, CD74FCT244AT		
INPUT	INPUT	OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	Y
L	L	L
L	H	H
H	X	Z

NOTE:

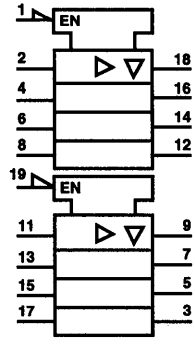
1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = HIGH Impedance

IEC Logic Symbols

CD74FCT240, CD74FCT240AT



CD74FCT244, CD74FCT244AT



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) . . . . . -0.5V to 6.0V
DC Input Diode Current, I_{IK} (for V_I < -0.5V) . . . . . -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) . . . . . -50mA
DC Output Sink Current per Output Pin, I_O 70mA
DC Output Source Current per Output Pin, I_O . . . . . -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 528mA

Operating Conditions

Operating Temperature Range . . . . . 0 to 70°C
Supply Voltage Range, V_{CC} . . . . . 4.75V to 5.25V
DC Input Voltage, V_I . . . . . 0 to V_{CC}
DC Output Voltage, V_O . . . . . 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv . . . . . 0 to 10ns/V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	135
SOIC Package	125
SSOP Package	130

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC and SSOP-Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Temperature Range, 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)						UNITS
					25°C		0°C to 70°C		(244E ONLY) -55°C to 125°C		
		V_I	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	-	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64	Min	-	0.55	-	0.55	-	-	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	-	-10	µA
Short Circuit Output Current (Note 3)	I_{OS}	V_{CC} or GND V_O = 0		Max	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	-	2	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA max at 70°C.

Switching Specifications t_r, t_f = 2.5ns, C_L = 50pF, R_L - See Figure 2

PARAMETER	SYMBOL	V_{CC} (V)	CD74FCT240, CD74FCT244			CD74FCT240AT, CD74FCT244AT			UNITS
			25°C	0°C to 70°C		25°C	0°C to 70°C		
			TYP	MIN	MAX	TYP	MIN	MAX	
Propagation Delays Data to Outputs	t_{PLH}, t_{PHL}								
CD74FCT240/AT		5 (Note 6)	5	1.5	8	4.4	1.5	5.6	ns
CD74FCT244/AT		5	4.5	1.5	6.5	3.8	1.5	5.3	µs
Output Enable Times	t_{PZL}, t_{PZH}								
CD74FCT240/AT		5	7	1.5	10	4.7	1.5	6.2	µs
CD74FCT244/AT		5	6	1.5	8	4.8	1.5	6.5	ns
Output Disable Times	t_{PLZ}, t_{PHZ}								
CD74FCT240/AT		5	6	1.5	9.5	4	1.5	5.6	µs
CD74FCT244/AT		5	5	1.5	7	4.5	1.5	5.8	µs
Power Dissipation Capacitance (Note 7)	C_{PD}								
CD74FCT240/AT		-	38 Typical			38 Typical			pF
CD74FCT244/AT		-	35 Typical			35 Typical			pF
Min (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} (Figure 1)	5	0.5	-	-	0.5	-	-	V
Max (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} (Figure 1)	5	1	-	-	1			V
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Three-State Output Capacitance	C_O	-	-	-	15	-	-	15	pF

NOTES:

6. 5V: Min is at 5.25V for 0°C to 70°C, Max is at 4.75V for 0°C to 70°C, Typ is at 5V.
7. C_{PD}, measured per function, is used to determine the dynamic power consumption. P_D (per package) = $V_{CC} I_{CC} + \Sigma (V_{CC}^2 f_i C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$ where:
   V_{CC} = Supply Voltage
   ΔI_{CC} = Flow Through Current X Unit Load
   C_L = Output Load Capacitance
   D = Duty Cycle of Input High
   f_O = Output Frequency
   f_i = Input Frequency

Test Circuits and Waveforms

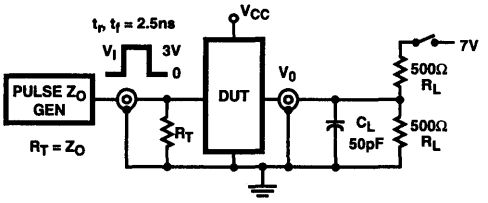


FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

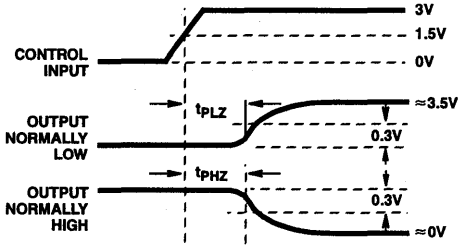


FIGURE 2. OUTPUT DISABLE TIMES

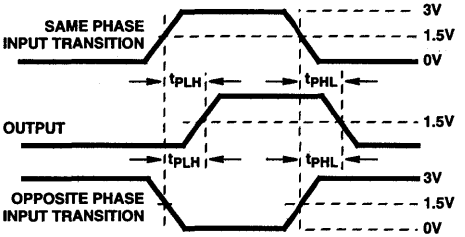


FIGURE 3. PROPAGATION DELAY TIMES

HARRIS SEMICONDUCTOR

CD54FCT245, CD74FCT245

BiCMOS FCT Interface Logic, Octal-Bus Tranceivers, Three-State

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 5.0ns at V_{CC} = 5V, T_A = 25°C
- Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 64mA Output Sink Current (74 Series)
- 48mA Output Sink Current (54 Series)
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Description

The CD54/74FCT245 octal bus transceiver uses a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48mA to 64mA.

The CD54/74FCT245 is a noninverting, three-state, bidirectional transceiver/buffer intended for two-way transmission from"A" bus to "B" bus or "B" bus to "A" bus. The logic level present on the Direction Input (DIR) determines the data direction. When the Output Enable input is HIGH, the outputs are in the high impedance state.

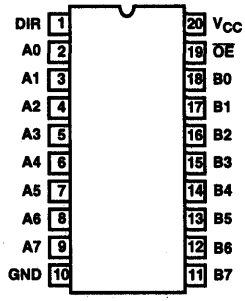
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT245E	0 to 70	20 Ld PDIP	E20.3
CD74FCT245M	0 to 70	20 Ld SOIC	M20.3
CD74FCT245SM	0 to 70	20 Ld SSOP	M20.209
CD54FCT245E	-55 to 125	20 Ld PDIP	E20.3

NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD54FCT245, CD74FCT245
(PDIP, SOIC, SSOP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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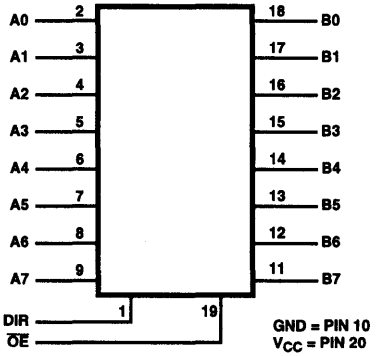
File Number **2301.2**

Functional Diagram



TRUTH TABLE (NOTE 1)

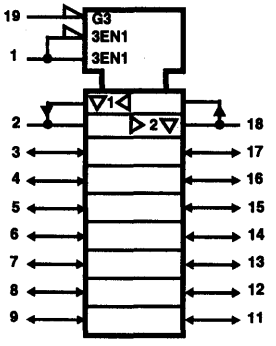
CONTROL INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Isolation

NOTES:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Irrelevant
2. To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1 MΩ resistors.

IEC Logic Symbol

CD74FCT245, CD54FCT245



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) . . . . . -0.5V to 6.0V
DC Input Diode Current, I_{IK} (for V_I < -0.5V) . . . . . -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) . . . . . -50mA
DC Output Sink Current per Output Pin, I_O 70mA
DC Output Source Current per Output Pin, I_O . . . . . -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 528mA

Operating Conditions

Operating Temperature Range (T_A) . . . . . -55°C to 125°C
Supply Voltage Range, V_{CC}
CD74 Series, T_A = 0°C to 70°C . . . . . 4.75V to 5.25V
CD54 Series, T_A = -55°C to 125°C . . . . . 4.5V to 5.5V
DC Input Voltage, V_I . . . . . 0 to V_{CC}
DC Output Voltage, V_O . . . . . 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv . . . . . 0 to 10ns/V

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
PDIP Package	125
SOIC Package	115
SSOP Package	125

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC and SSOP-Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

74FCT Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V
54FCT Extended Industrial Temperature Range -55°C to 125°C; V_{CC} Max = 5.5V, V_{CC} Min = 4.5V

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)						UNITS
					25°C		0°C TO 70°C		-55°C TO 125°C		
		V_I	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or	-15	Min	2.4	-	2.4	-	-	-	V
		V_{IL}	-12	Min	2.4	-	-	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or	64	Min	-	0.55	-	0.55	-	-	V
		V_{IL}	48	Min	-	0.55	-	-	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	-	-10	µA
Short Circuit Output Current (Note 4)	I_{OS}	V_{CC} or GND V_O = 0		Max	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 5)		Max	-	1.6	-	1.6	-	2	mA

NOTES:

4. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
5. Inputs that are not measured are at V_{CC} or GND.
6. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max at 70°C.

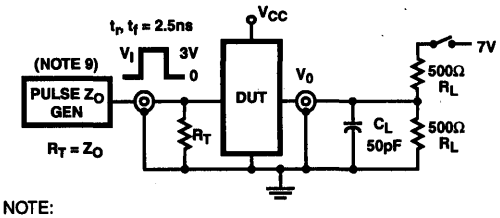
Switching Specifications t_r, t_f = 2.5ns, C_L = 50pF, R_L - See Figure 3

PARAMETER	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A)							UNITS
			25°C	0°C TO 70°C			-55°C TO 125°C			
			TYP	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delays Data to Outputs)	t_{PLH}, t_{PHL}	5	5	1.5	-	7	1.5	-	7.5	ns
Output Enable to Output	t_{PZL}, t_{PZH}	5	6	1.5	-	7.5	1.5	-	10	ns
Output Disable to Output	t_{PLZ}, t_{PHZ}	5	6	1.5	-	9.5	1.5	-	10	ns
Power Dissipation Capacitance	C_{PD}	-	49	-	49	-	-	49	-	pF
Min (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	0.5	-	-	-	-	-	-	V
Max (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1	-	-	-	-	-	-	V
Input Capacitance	C_I	-	-	-	-	10	-	-	10	pF
Input/Output Capacitance	$C_{I/O}$	-	-	-	-	15	-	-	15	pF

NOTES:

7. 5V: Min is at 5.5V, Max is at 4.5V.
   5V: Min is at 5.25V for 0°C to 70°C, Max is at 4.75V for 0°C to 70°C, Typ is at 5V.
8. C_{PD}, measured per function, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + Σ (V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

Test Circuits and Waveforms



NOTE:

9. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

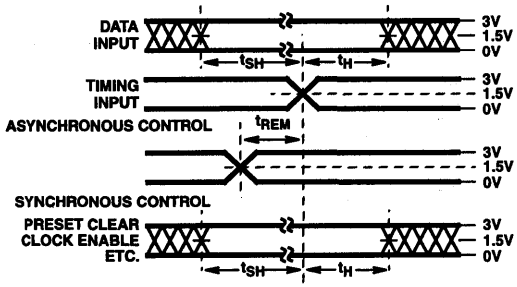


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

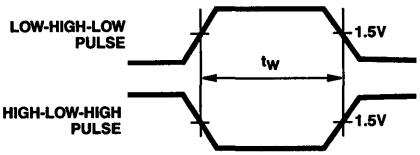


FIGURE 3. PULSE WIDTH

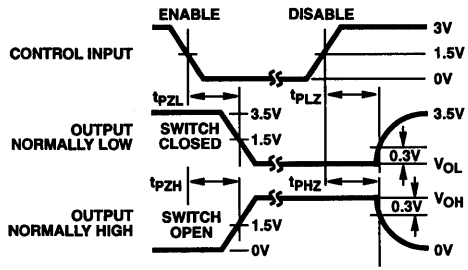


FIGURE 4. ENABLE AND DISABLE TIMING

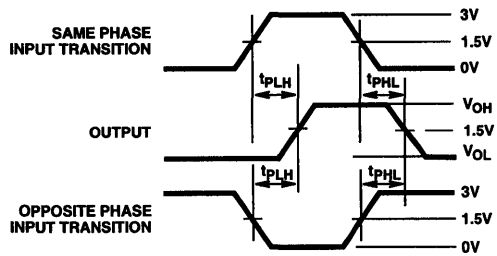
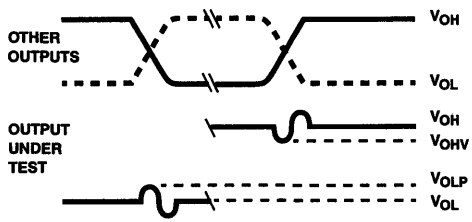


FIGURE 5. PROPAGATION DELAY



NOTES:

10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
11. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT273

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

BiCMOS FCT Interface Logic, Octal D Flip-Flop with Reset

Features

- **Buffered Inputs**
- **Typical Propagation Delay: 5.3ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF**
- **SCR Latchup Resistant BiCMOS Process and Circuit Design**
- **Speed of Bipolar FAST™/AS/S**
- **48mA Output Sink Current**
- **Output Voltage Swing Limited to 3.7V at V_{CC} = 5V**
- **Controlled Output Edge Rates**
- **Input/Output Isolation to V_{CC}**
- **BiCMOS Technology with Low Quiescent Power**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT273E	0 to 70	20 Ld PDIP	E20.3
CD74FCT273M	0 to 70	20 Ld SOIC	M20.3

NOTE: When ordering the suffix M package, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

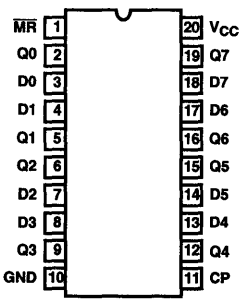
Description

The CD74FCT273 octal D flip-flop with reset uses a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

Information at the D input of the CD74FCT273 is transferred to the Q output on the positive going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CP) and common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock.

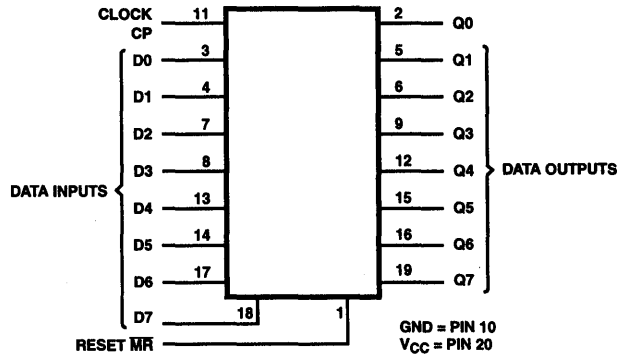
Pinout

CD74FCT273
(PDIP, SOIC)
TOP VIEW



8 BiCMOS FCT PRODUCTS

Functional Diagram



TRUTH TABLE (Note 1)

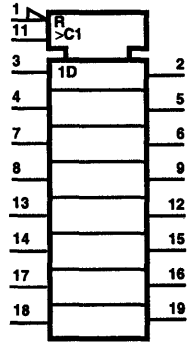
INPUTS			OUTPUTS
RESET $\overline{MR}$	CLOCK CP	DATA Dn	Qn
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

NOTE:

1. H = HIGH Voltage Level (Steady State)
   L = LOW Voltage Level (Steady State)
   X = Irrelevant
   ↑ = Transition from low to high level.
   Q0 = The level of Q before the indicated steady state input conditions were established.

IEC Logic Symbol

CD74FCT273



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) ..... -0.5V to 6V
DC Input Diode Current, I_{IK} (For V_I < -0.5V) ..... -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) ..... -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO ..... -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 400mA

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} ($^oC/W$)
PDIP Package 135
SOIC Package 125
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC-Lead Tips Only)

Operating Conditions

Operating Temperature Range (T_A) ..... 0°C to 70°C
Supply Voltage Range, V_{CC} ..... 4.75V to 5.25V
DC Input Voltage, V_I ..... 0 to V_{CC}
DC Output Voltage, V_O ..... 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv ..... 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V (Note 5)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max. at 70°C.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 4) (Note 6)

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Propagation Delays						
CP to Qn	t_{PLH}, t_{PHL}	5	7	2	13	ns
$\overline{MR}$ to Qn	t_{PLH}, t_{PHL}	5	8	2	13	ns
Power Dissipation Capacitance	C_{PD} (Note 7)	-	36	-	-	pF
Input Capacitance	C_I	-	-	-	10	pF

NOTES:

6. 5V: Min is at 5.25V for 0°C to 70°C, Max is at 4.75V for 0°C to 70°C, Typ is at 5V.
7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2 f_i C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$ where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_i = input frequency

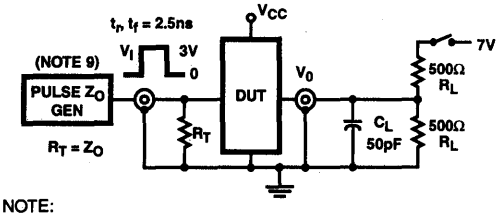
Prerequisite for Switching (Note 8)

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Data to CP Setup Time	t_{SU}	5	-	3	-	ns
Hold Time	t_H	5	-	2	-	ns
Removal Time, $\overline{MR}$ to CP	t_{REM}	5	-	4	-	ns
$\overline{MR}$ Pulse Width	t_W	5	-	7	-	ns
CP Pulse Width	t_W	5	-	7	-	ns
CP Frequency	f_{MAX}	5	-	70	-	MHz

NOTE:

8. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

9. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: t_r = t_f = 2.5ns (10% to 90%), unless otherwise specified

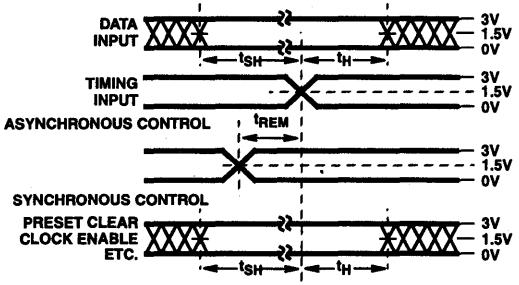


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

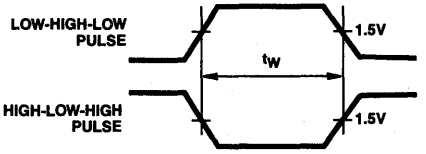


FIGURE 3. PULSE WIDTH

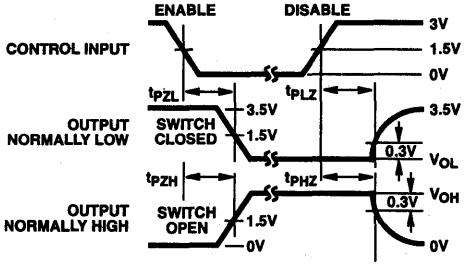


FIGURE 4. ENABLE AND DISABLE TIMING

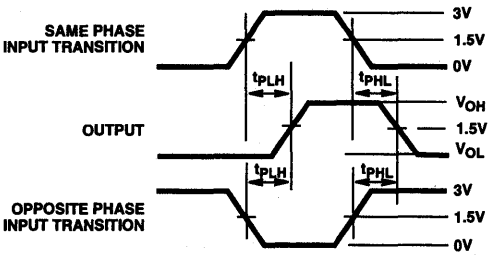
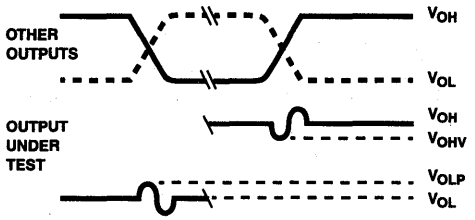


FIGURE 5. PROPAGATION DELAY



NOTES:

10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
11. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT373, CD74FCT373AT

BiCMOS FCT Interface Logic, Octal Transparent Latches, Three-State

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 3.9ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF (CD74FCT373AT)
- Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- FCTXXX Types
  - Speed of Bipolar FAST™/AS/S
- FCTXXXAT Types
  - 30% Faster than FAST™/AS/S with Significantly Reduced Power Consumption
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Description

The CD74FCT373 and CD74FCT373AT octal transparent latches use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

The CD74FCT373 and CD74FCT373AT outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the three-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The latch operation is independent of the state of the Output Enable.

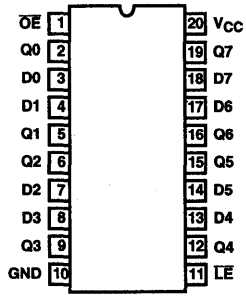
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT373E	0 to 70	20 Ld PDIP	E20.3
CD74FCT373M	0 to 70	20 Ld SOIC	M20.3
CD74FCT373SM	0 to 70	20 Ld SSOP	M20.209

NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74FCT373, CD74FCT373AT
(PDIP, SOIC, SSOP)
TOP VIEW

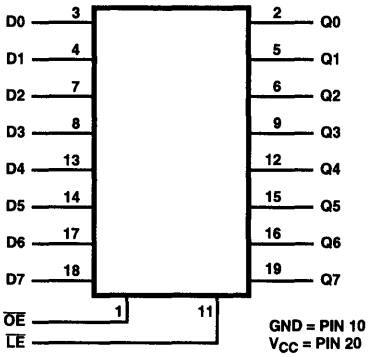


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **2230.3**

Functional Diagram



TRUTH TABLE (Note 1)

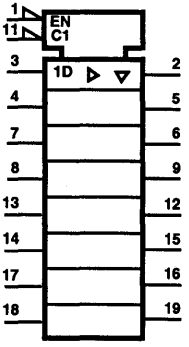
$\overline{\text{OUTPUT}}$ ENABLE	$\overline{\text{LATCH}}$ ENABLE	DATA	OUTPUT
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   l = Low voltage level one set up time prior to the high to low latch enable transition.
   h = High voltage level one set up time prior to the high to low latch enable transition.
   X = Irrelevant
   Z = High impedance

IEC Logic Symbol

CD74FCT373, CD74FCT373AT TYPES



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) ..... -0.5V to 6V
DC Input Diode Current, I_{IK} (For V_I < -0.5V) ..... -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) ..... -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO ..... -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 400mA

Operating Conditions

Operating Temperature Range (T_A) ..... 0°C to 70°C
Supply Voltage Range, V_{CC} ..... 4.75V to 5.25V
DC Input Voltage, V_I ..... 0 to V_{CC}
DC Output Voltage, V_O ..... 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv ..... 0 to 10ns/V

Thermal Information

Thermal Resistance (Typical, Note 2) ..... θ_{JA} (°C/W)
PDIP Package 135
SOIC Package 125
SSOP Package 130
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC and SSOP-Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V (Note 5)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70°C.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 4) (Note 6)

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays						
Data to Outputs						
CD74FCT373	t_{PLH}, t_{PHL}	5	5	1.5	8	ns
CD74FCT373AT	t_{PLH}, t_{PHL}	5	3.9	1.5	5.7	ns
$\overline{LE}$ to Outputs						
CD74FCT373	t_{PLH}, t_{PHL}	5	9	2	13	ns
CD74FCT373AT	t_{PLH}, t_{PHL}	5	4.4	2	7	ns
Output Enable Times						
CD74FCT373	t_{PZL}, t_{PZH}	5	7	1.5	12	ns
CD74FCT373AT	t_{PZL}, t_{PZH}	5	6	1.5	8	ns
Output Disable Times						
CD74FCT373	t_{PLZ}, t_{PHZ}	5	6	1.5	7.5	ns
CD74FCT373AT	t_{PLZ}, t_{PHZ}	5	4	1.5	5.8	ns
Power Dissipation Capacitance	C_{PD} (Note 7)	-	33	-	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1	-	-	V
Input Capacitance	C_I	-	-	-	10	pF
Three-State Output Capacitance	C_O	-	-	-	15	pF

NOTE:

6. 5V: Min is at 5.25V for 0°C to 70°C, Max is at 4.75V for 0°C to 70°C, Typ is at 5V.
7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2$ f_I C_{PD} + V_O^2 f_O C_L + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

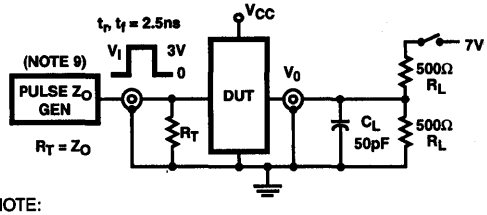
Prerequisite for Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Data to Latch Enable Setup Time	t_{SU}	5 (Note 8)	-	2	-	ns
Data to Latch Enable Hold Time	t_H	5	-	1.5	-	ns
Latch Enable Pulse Width						
CD74FCT373	t_W	5	-	6	-	ns
CD74FCT373AT	t_W	5	-	5	-	ns

NOTE:

8. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

9. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

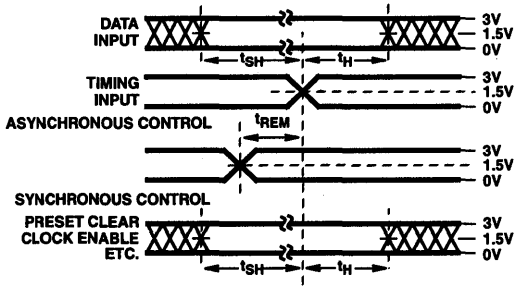


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

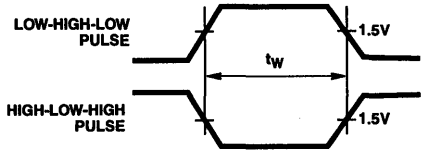


FIGURE 3. PULSE WIDTH

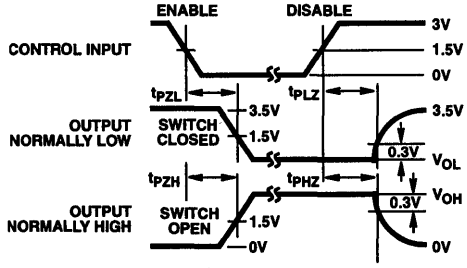


FIGURE 4. ENABLE AND DISABLE TIMING

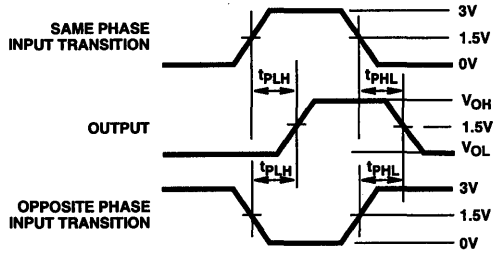
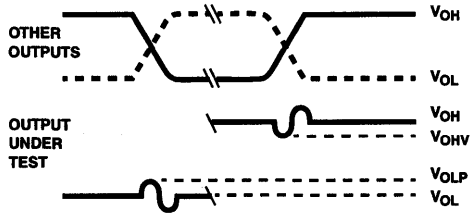


FIGURE 5. PROPAGATION DELAY



NOTES:

10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
11. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT374

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

BiCMOS FCT Interface Logic, Octal D-Type Flip-Flop, Three-State

Features

- Buffered Inputs
- Typical Propagation Delay: 6.6ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- Positive Edge Triggered
- Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT374E	0 to 70	20 Ld PDIP	E20.3
CD74FCT374M	0 to 70	20 Ld SOIC	M20.3
CD74FCT374SM	0 to 70	20 Ld SSOP	M20.209

NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

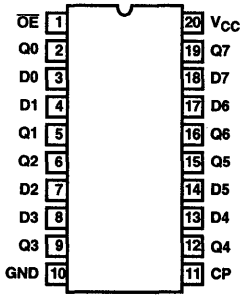
Description

The CD74FCT374 octal D-Type, three-state, positive edge triggered flip-flop uses a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

The eight flip-flops enter data into their registers on the LOW to HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the three state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The CD74FCT374 outputs are noninverted. (For flow through pin configurations, see CD74FCT564 and CD74FCT574.)

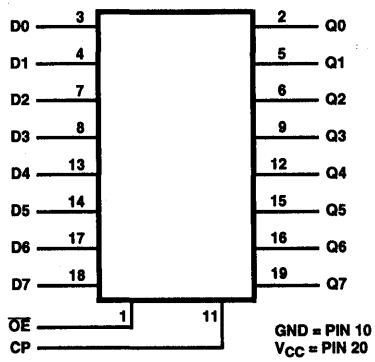
Pinout

CD74FCT374
(PDIP, SOIC, SSOP)
TOP VIEW



8 BiCMOS FCT PRODUCTS

Functional Diagram



TRUTH TABLE (Note 1)

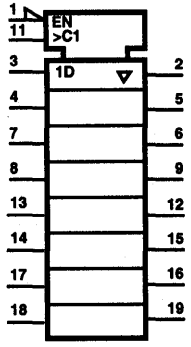
INPUTS			OUTPUTS
$\overline{OE}$	CP	Dn	Qn
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

NOTE:

1. H = HIGH Voltage Level (Steady State)
   L = LOW Voltage Level (Steady State)
   X = Immaterial
   ↑= Transition from low to high level.
   Q0 = The level of Q before the indicated steady state input conditions were established.
   Z = HIGH Impedance

IEC Logic Symbol

CD74FCT374



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) ..... -0.5V to 6V
DC Input Diode Current, I_{IK} (For V_I < -0.5V) ..... -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) ..... -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO ..... -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 400mA

Thermal Information

Thermal Resistance (Typical, Note 2) ..... θ_{JA} (°C/W)
PDIP Package 135
SOIC Package 125
SSOP Package 130
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC and SSOP-Lead Tips Only)

Operating Conditions

Operating Temperature Range (T_A) ..... 0°C to 70°C
Supply Voltage Range, V_{CC} ..... 4.75V to 5.25V
DC Input Voltage, V_I ..... 0 to V_{CC}
DC Output Voltage, V_O ..... 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V (Note 5)

PARAMETER	SYMBOL	TEST CONDITIONS			AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70°C.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 4) (Note 6)

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Propagation Delays						
Clock to Q	t_{PLH}, t_{PHL}	5	6.6	2	10	ns
Output Disable to Q	t_{PLZ}, t_{PHZ}	5	6	1.5	8	ns
Output Enable to Q	t_{PZL}, t_{PZH}	5	9	1.5	12.5	ns
Power Dissipation Capacitance	C_{PD} (Note 7)	-	33	-	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1	-	-	V
Input Capacitance	C_I	-	-	-	10	pF
Three State Output Capacitance	C_O	-	-	-	15	pF

NOTES:

6. 5V: Min is at 5.25V for 0°C to 70°C, Max is at 4.75V for 0°C to 70°C, Typ is at 5V.
7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2$ f_I C_{PD} + V_O^2 f_O C_L + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

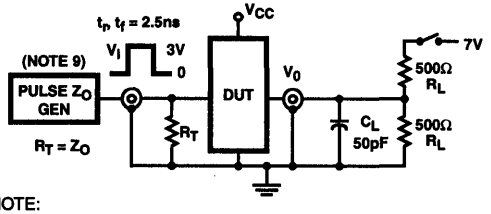
Prerequisite for Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Setup Time Data to Clock	t_{SU}	5 (Note 8)	-	2	-	ns
Data to Clock Hold Time	t_H	5	-	2	-	ns
Clock Pulse Width	t_W	5	-	7	-	ns
Maximum Clock Frequency	f_{MAX}	5	-	70	-	MHz

NOTE:

8. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

9. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

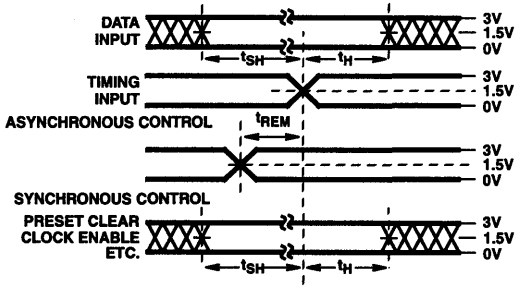


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

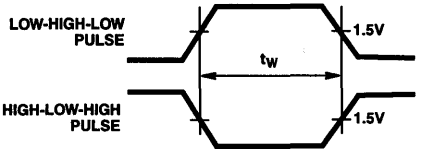


FIGURE 3. PULSE WIDTH

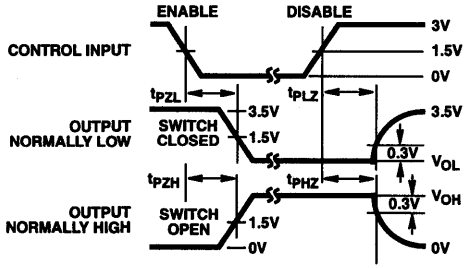


FIGURE 4. ENABLE AND DISABLE TIMING

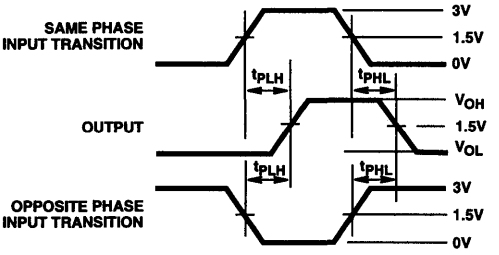
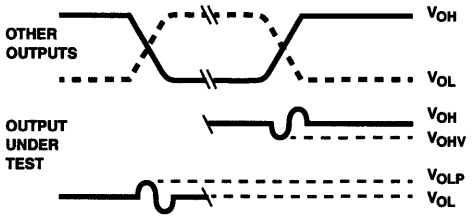


FIGURE 5. PROPAGATION DELAY



NOTES:

10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
11. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT540, CD74FCT541

BiCMOS FCT Interface Logic, Octal Buffers/Line Drivers, Three-State

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 6.4ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- CD74FCT540
  - Inverting
- CD74FCT541
  - Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 64mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Description

The CD74FCT540 and CD74FCT541 octal buffers/line drivers use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 milliamperes.

The CD74FCT540 is a three-state buffer having two active LOW output enables. The CD74FCT541 is a noninverting three state buffer having two active LOW output enables.

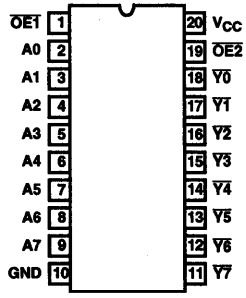
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT540E	0 to 70	20 Ld PDIP	E20.3
CD74FCT541E	0 to 70	20 Ld PDIP	E20.3
CD74FCT540M	0 to 70	20 Ld SOIC	M20.3
CD74FCT541M	0 to 70	20 Ld SOIC	M20.3
CD74FCT541SM	0 to 70	20 Ld SSOP	M20.209

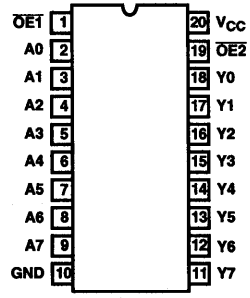
NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinouts

CD74FCT540
(PDIP, SOIC)
TOP VIEW



CD74FCT541
(PDIP, SOIC, SSOP)
TOP VIEW

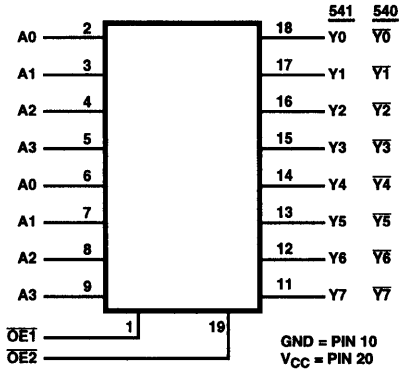


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **2383.2**

Functional Diagram



TRUTH TABLE (Note 1)

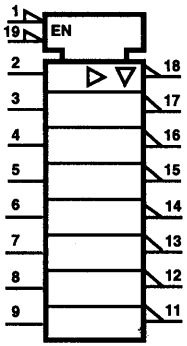
INPUTS			OUTPUTS	
$\overline{OE1}$	$\overline{OE2}$	A_n	CD74FCT540	CD74FCT541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

NOTE:

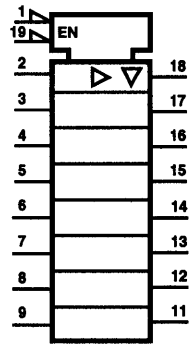
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Immaterial
   Z = HIGH Impedance

IEC Logic Symbol

CD74FCT540



CD74FCT541



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) ..... -0.5V to 6V
DC Input Diode Current, I_{IK} (For V_I < -0.5V) ..... -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) ..... -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO ..... -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 528mA

Operating Conditions

Operating Temperature Range (T_A) ..... 0°C to 70°C
Supply Voltage Range, V_{CC} ..... 4.75V to 5.25V
DC Input Voltage, V_I ..... 0 to V_{CC}
DC Output Voltage, V_O ..... 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv ..... 0 to 10ns/V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	135
SOIC Package	125
SSOP Package	130

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC and SSOP-Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V (Note 5)

PARAMETER	SYMBOL	TEST CONDITIONS			AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max. @ 70°C.

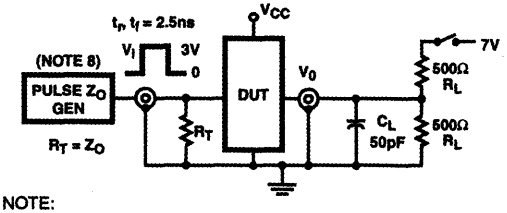
Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 3) (Note 6)

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Propagation Delays		(Note 6)				
Data to Outputs						
CD74FCT540	t_{PLH}, t_{PHL}	5	6.4	2	8.5	ns
CD74FCT541	t_{PLH}, t_{PHL}	5	6	2	8	ns
Output Disable to Output	t_{PLZ}, t_{PHZ}	5	7.1	2	9.5	ns
Output Enable to Output	t_{PZL}, t_{PZH}	5	7.5	2	10	ns
Power Dissipation Capacitance	C_{PD} (Note 7)					
CD74FCT540		-	37	-	-	pF
CD74FCT541		-	40	-	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1	-	-	V
Input Capacitance	C_I	-	-	-	10	pF
Three-State Output Capacitance	C_O	-	-	-	15	pF

NOTES:

6. 5V: Min is at 5.25V for 0°C to 70°C, Max is at 4.75V for 0°C to 70°C, Typ is at 5V.
7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2$ f_I C_{PD} + V_O^2 f_O C_L + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

Test Circuits and Waveforms



NOTE:

8. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: t_r = t_f = 2.5ns (10% to 90%), unless otherwise specified

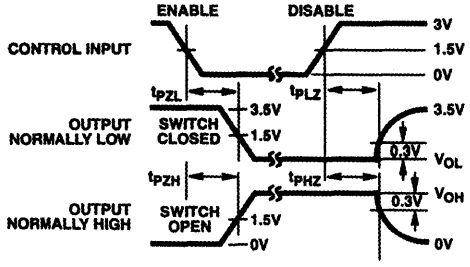


FIGURE 2. ENABLE AND DISABLE TIMING

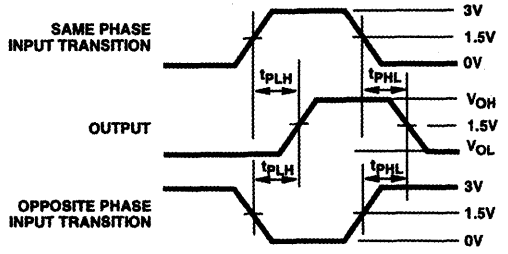
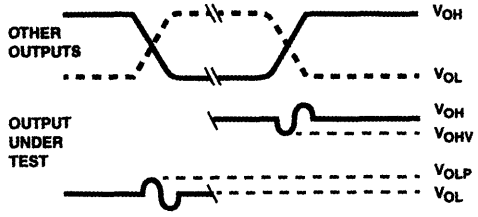


FIGURE 3. PROPAGATION DELAY



NOTES:

9. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
10. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
11. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 4. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT543

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

January 1997

BiCMOS FCT Interface Logic, Octal Register/Transceiver, Three-State

Features

- Buffered Inputs
- Typical Propagation Delay: 6.4ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- Noninverting
- Family Features
  - SCR Latchup Resistant BiCMOS Process and Circuit Design
  - Speed of Bipolar FAST™/AS/S
  - 64mA Output Sink Current
  - Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
  - Controlled Output Edge Rates
  - Input/Output Isolation to V_{CC}
  - BiCMOS Technology with Low Quiescent Power

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT543EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT543M	0 to 70	24 Ld SOIC	M24.3
CD74FCT543SM	0 to 70	24 Ld SSOP	M24.209

NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

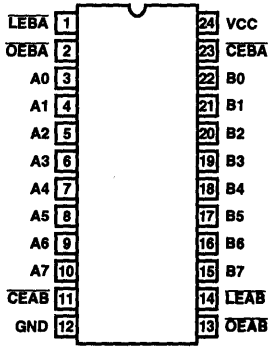
Description

The CD74FCT543 three-state, octal register/transceiver uses a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 milliamperes.

This device contains two sets of eight D-Type latches with separate input and output controls for each set. For data flow from A to B, for example, the A to B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from A0-A7 or to take data from B0-B7, as indicated in the Truth Table. With $\overline{CEAB}$ LOW, a LOW signal on the A to B Latch Enable ($\overline{LEAB}$) input makes the A to B latches transparent; a subsequent LOW to HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the three state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

Pinout

CD74FCT543
(PDIP, SOIC, SSOP)
TOP VIEW



2399.2

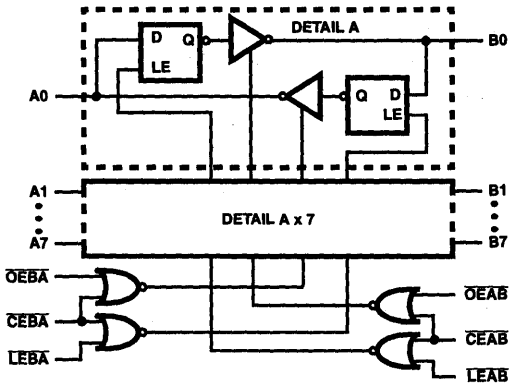
8

'CMOS FCT 'ODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Proce

FAST™ is a trademark of Fairchild Semiconductor.

Functional Diagram



TRUTH TABLE For A to B (Symmetric with B to A)

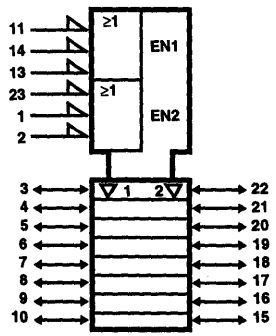
INPUTS			LATCH STATUS	OUTPUT BUFFERS
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A TO B	B0 THRU B7
H	X	X	Storing	High Z
X	H	–	Storing	-
X	-	H	-	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs (Note 1)

NOTE:

1. Before $\overline{LEAB}$ LOW to HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Immaterial
   A to B data flow shown; B to A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.

IEC Logic Symbol

CD74FCT543



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) . . . . . -0.5V to 6V
DC Input Diode Current, I_{IK} (For V_I < -0.5V) . . . . . -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) . . . . . -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO . . . . . -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 528mA

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} ($^oC/W$)
PDIP Package 75
SOIC Package 75
SSOP Package 125
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC and SSOP-Lead Tips Only)

Operating Conditions

Operating Temperature Range (T_A) . . . . . 0°C to 70°C
Supply Voltage Range, V_{CC} . . . . . 4.75V to 5.25V
DC Input Voltage, V_I . . . . . 0 to V_{CC}
DC Output Voltage, V_O . . . . . 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv . . . . . 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70°C.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 4)

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C			UNITS
			TYP	MIN	TYP	MAX	
Propagation Delays							
An ↔ Bn	t_{PLH}, t_{PHL}	5	6.4	2.5	-	8.5	ns
$\overline{LEBA}$ to An or $\overline{LEAB}$ to Bn	t_{PLH}, t_{PHL}	5	9.4	2.5	-	12.5	ns
$\overline{CEBA}$ or $\overline{CEAB}$ to An or Bn	t_{PLZ}, t_{PHZ}	5	6.8	2	-	9	ns
	t_{PZL}, t_{PZH}	5	9	2	-	12	ns
Power Dissipation Capacitance	C_{PD} (Note 6)	-	49	-	49	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	0.5	-	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1	-	-	-	V
Input Capacitance	C_I	-	-	-	-	10	pF
Input/Output Capacitance	$C_{I/O}$	-	-	-	-	15	pF

NOTE:

6. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2$ f_I C_{PD} + V_O^2 f_O C_L + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

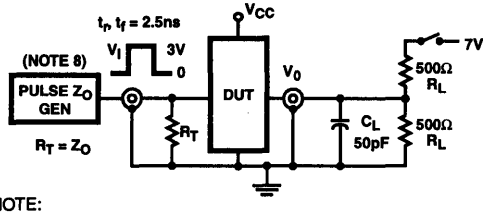
Prerequisite for Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Data to Latch Enable Setup Time	t_{SU}	5 (Note 7)	-	3	-	ns
Data to Latch Enable Hold Time	t_H	5	-	2	-	ns
Latch Enable Pulse Width	t_W	5	-	9	-	ns

NOTE:

7. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

8. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

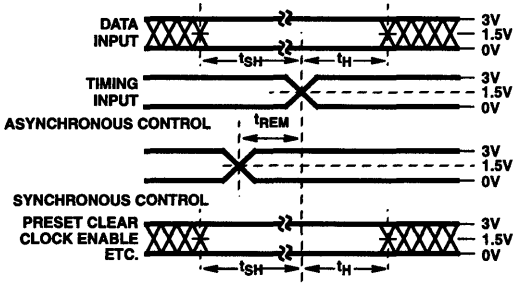


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

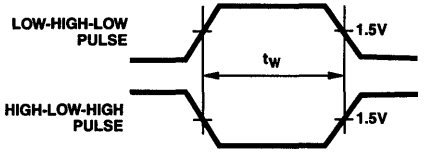


FIGURE 3. PULSE WIDTH

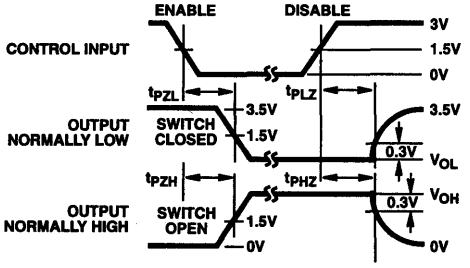


FIGURE 4. ENABLE AND DISABLE TIMING

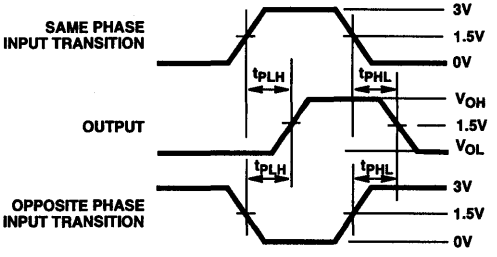
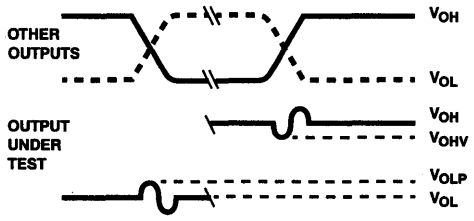


FIGURE 5. PROPAGATION DELAY



NOTES:

9. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
10. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
11. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT564, CD74FCT574

BiCMOS FCT Interface Logic, Octal D-Type Flip-Flops, Three-State

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 5.6ns at V_{CC} = 5V, T_A = 25°C
- Positive Edge Triggered
- CD74FCT564
  - Inverting
- CD74FCT574
  - Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Description

The CD74FCT564 and CD74FCT574 are octal D-Type, three-state, positive edge triggered flip-flops which use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

The eight flip-flops enter data into their registers on the LOW to HIGH transition of the clock (CP). The Output Enable ($\overline{OE}$) controls the three state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The CD74FCT564 and CD74FCT574 share the same configurations; the CD74FCT564, however, has inverted outputs and the CD74FCT574 has noninverted outputs.

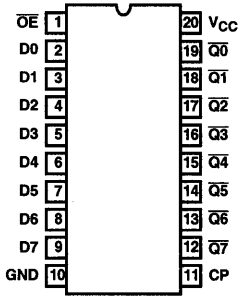
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT564E	0 to 70	20 Ld PDIP	E20.3
CD74FCT574E	0 to 70	20 Ld PDIP	E20.3
CD74FCT564M	0 to 70	20 Ld SOIC	M20.3
CD74FCT574M	0 to 70	20 Ld SOIC	M20.3
CD74FCT574SM	0 to 70	20 Ld SSOP	M20.209

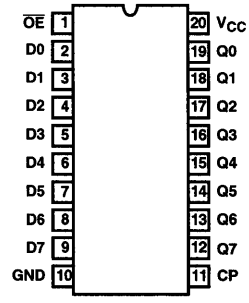
NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinouts

CD74FCT564
(PDIP, SOIC, SSOP)
TOP VIEW



CD74FCT574
(PDIP, SOIC, SSOP)
TOP VIEW

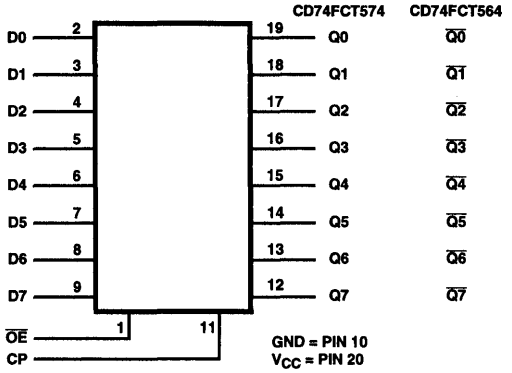


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **2295.2**

Functional Diagram



TRUTH TABLE (NOTE 1)

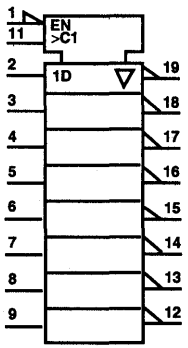
INPUTS			OUTPUTS	
			CD74FCT564	CD74FCT574
$\overline{OE}$	CP	DN	$\overline{QN}$	QN
L	↑	H	L	H
L	↑	L	H	L
L	L	X	Qo	Qo
H	X	X	Z	Z

NOTE:

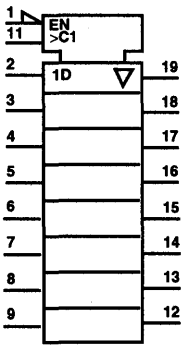
1. H = High Level (Steady State)
   L = Low Level (Steady State)
   X = Don't Care
   ↑ = Transition from low to high level
   Qo = The level of Q before the indicated steady state input conditions were established.
   Z = HIGH Impedance

IEC Logic Symbols

CD74FCT564



CD74FCT574



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) ..... -0.5V to 6V
DC Diode Current, I_{IK} (For V_I < -0.5V) ..... -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) ..... -50mA
DC Output Sink Current per Output Pin, I_O 70mA
DC Output Source Current per Output Pin, I_O ..... -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 400mA

Operating Conditions

Operating Temperature Range, T_A ..... 0°C to 70°C
Supply Voltage Range, V_{CC} ..... 4.75V to 5.25V
DC Input Voltage, V_I ..... 0 to V_{CC}
DC Output Voltage, V_O ..... 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv ..... 0 to 10ns/V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	135
SOIC Package	125
SSOP Package	130

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC and SSOP-Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS			AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.5 to 5.5	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.5 to 5.5	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_{CC} = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		MAX	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max at 70°C.

Switching Specifications Over Operating Range t_r, t_f = 2.5ns, C_L = 50pF, R_L - See Figure 4

PARAMETER		SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) 25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays							
Clock to Q	CD74FCT574	t_{PLH}, t_{PHL}	5	6.6	2	10	ns
Clock to $\overline{Q}$	CD74FCT564	t_{PLH}, t_{PHL}	5	6.6	1.5	10	ns
Output Disable to Q	CD74FCT574	t_{PLZ}, t_{PHZ}	5	6	1.5	8	ns
Output Enable to Q	CD74FCT574	t_{PZL}, t_{PZH}	5	9	1.5	12.5	ns
Output Disable to $\overline{Q}$	CD74FCT564	t_{PLZ}, t_{PHZ}	5	6	1.5	8	ns
Output Enable to $\overline{Q}$	CD74FCT564	t_{PZL}, t_{PZH}	5	9	1.5	12.5	ns
Power Dissipation Capacitance		C_{PD} (Note 6)	-	34 Typical			pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV} (Figure 1)	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP} (Figure 1)	5	1	-	-	V
Input Capacitance		C_I	-	-	-	10	pF
Three State Output Capacitance		C_O	-	-	-	15	pF

NOTE:

6. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   PD (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2$ f_i C_{PD} + V_O^2 to C_L + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_i = input frequency

Prerequisite For Switching

PARAMETER	SYMBOL	V_{CC} (V)	AMBIENT TEMPERATURE (T_A) 25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Clock Pulse Width CD74FCT574	t_W	5 (Note 7)		7	-	ns
CD74FCT564	t_W	5		7	-	ns
Setup Time Data to Clock	t_{SU}	5		2	-	ns
Data to Clock Hold Time						
CD74FCT574	t_H	5		2	-	ns
CD74FCT564	t_H	5		2	-	ns
Maximum Clock Frequency	f_{MAX}	5		70	-	MHz

NOTE:

7. 5V: minimum is at 4.5V.
   5V: minimum is at 4.75V for 0°C to 70°C.
   Typical is at 5V.

HARRIS SEMICONDUCTOR

CD74FCT573, CD74FCT573AT

BiCMOS FCT Interface Logic, Octal Transparent Latches, Three-State

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 3.9ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF (CD74FCT573AT)
- SCR Latchup Resistant BICMOS Process and Circuit Design
- FCTXXX Types
  - Speed of Bipolar FAST™/AS/S
- FCTXXXAT Types
  - 30% Faster than FAST™/AS/S with Significantly Reduced Power Consumption
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BICMOS Technology with Low Quiescent Power

Description

The CD74FCT573 and CD74FCT573AT octal transparent latches use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

The CD74FCT573 and CD74FCT573AT outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the three-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The latch operation is independent of the state of the Output Enable.

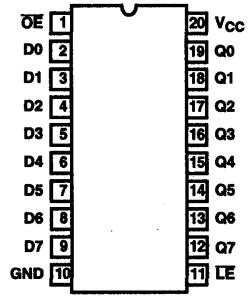
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT573ATE	0 to 70	20 Ld PDIP	E20.3
CD74FCT573M	0 to 70	20 Ld SOIC	M20.3
CD74FCT573SM	0 to 70	20 Ld SSOP	M20.209

NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinout

CD74FCT573, CD74FCT573AT
(PDIP, SOIC, SSOP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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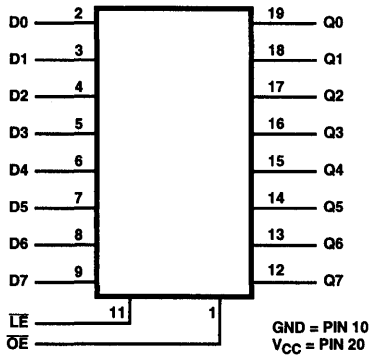
File Number 2304.2

Functional Diagram



TRUTH TABLE (Note 1)

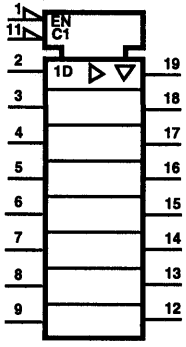
$\overline{\text{OUTPUT}}$ ENABLE	$\overline{\text{LATCH}}$ ENABLE	DATA	OUTPUT
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

NOTE:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   l = Low voltage level one set up time prior to the high to low latch enable transition.
   h = High voltage level one set up time prior to the high to low latch enable transition.
   X = Irrelevant
   Z = High Impedance

IEC Logic Symbol

CD74FCT573, CD74FCT573AT



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) . . . . . -0.5V to 6V
DC Input Diode Current, I_{IK} (For V_I < -0.5V) . . . . . -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) . . . . . -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO . . . . . -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 400mA

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
PDIP Package 135
SOIC Package 125
SSOP Package 130
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC and SSOP-Lead Tips Only)

Operating Conditions

Operating Temperature Range (T_A) . . . . . 0°C to 70°C
Supply Voltage Range, V_{CC} . . . . . 4.75V to 5.25V
DC Input Voltage, V_I . . . . . 0 to V_{CC}
DC Output Voltage, V_O . . . . . 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv . . . . . 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V (Note 5)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70°C.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 4) (Note 6)

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays						
Data to Outputs						
CD74FCT573	t_{PLH}, t_{PHL}	5	5	1.5	8	ns
CD74FCT573AT	t_{PLH}, t_{PHL}	5	3.9	1.5	5.7	ns
$\overline{LE}$ to Outputs						
CD74FCT573	t_{PLH}, t_{PHL}	5	9	2	13	ns
CD74FCT573AT	t_{PLH}, t_{PHL}	5	4.4	2	7	ns
Output Enable Times						
CD74FCT573	t_{PZL}, t_{PZH}	5	7	1.5	12	ns
CD74FCT573AT	t_{PZL}, t_{PZH}	5	6	1.5	8	ns
Output Disable Times						
CD74FCT573	t_{PLZ}, t_{PHZ}	5	6	1.5	7.5	ns
CD74FCT573AT	t_{PLZ}, t_{PHZ}	5	4	1.5	5.8	ns
Power Dissipation Capacitance	C_{PD} (Note 7)	-	34	-	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} (Figure 1)	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} (Figure 1)	5	1	-	-	V
Input Capacitance	C_I	-	-	-	10	pF
Three-State Output Capacitance	C_O	-	-	-	15	pF

NOTES:

6. 5V: Min is at 5.25V for 0°C to 70°C, Max is at 4.75V for 0°C to 70°C, Typ is at 5V.
7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = $V_{CC} I_{CC} + \Sigma(V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$ where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

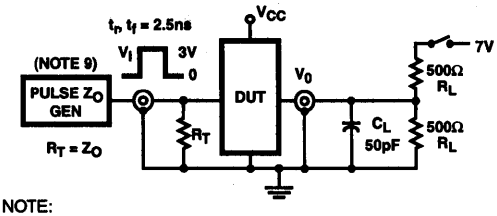
Prerequisite for Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Data to Latch Enable Setup Time	t_{SU}	5 (Note 8)	-	2	-	ns
Data to Latch Enable Hold Time	t_H	5	-	1.5	-	ns
Latch Enable Pulse Width						
CD74FCT573	t_W	5	-	6	-	ns
CD74FCT573AT	t_W	5	-	5	-	ns

NOTE:

8. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

9. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

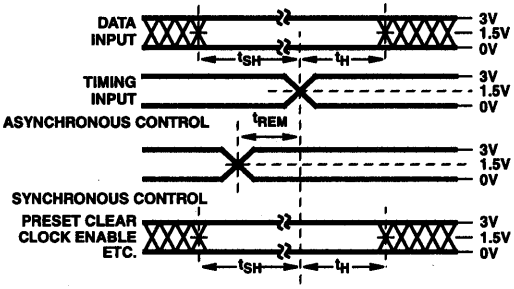


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

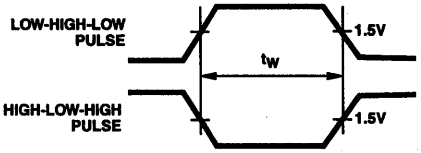


FIGURE 3. PULSE WIDTH

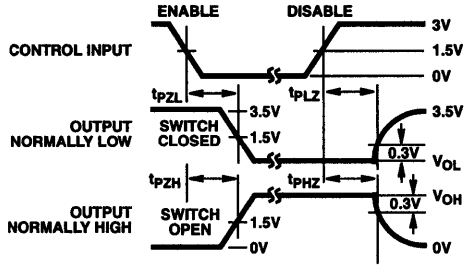


FIGURE 4. ENABLE AND DISABLE TIMING

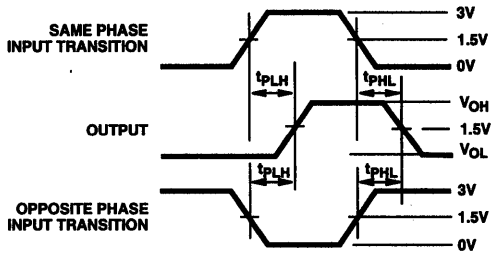
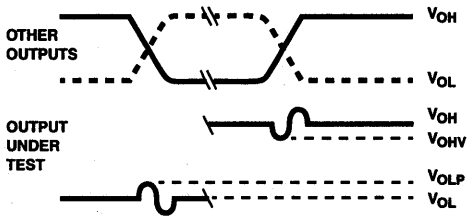


FIGURE 5. PROPAGATION DELAY



NOTES:

10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
11. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT646

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

BiCMOS FCT Interface Logic, Octal Bus Transceiver/Register, Three-State

Features

- Buffered Inputs
- Typical Propagation Delay: 6.8ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 64mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT646EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT646M	0 to 70	24 Ld SOIC	M24.3
CD74FCT646SM	0 to 70	24 Ld SSOP	M24.209

NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

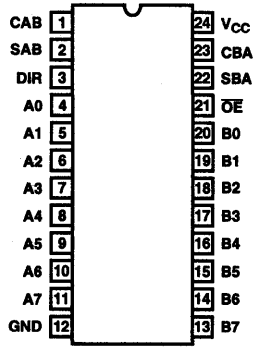
Description

The CD74FCT646 three-state octal bus transceiver/register uses a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 milliamperes.

This device is a bus transceiver with D-Type flip-flops which act as internal storage registers on the LOW to HIGH transition of either CAB or CBA clock inputs. Output Enable ($\overline{OE}$) and Direction (DIR) inputs control the transceiver functions. Data present at the high impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable ($\overline{OE}$) is LOW. In the high impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable ($\overline{OE}$) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

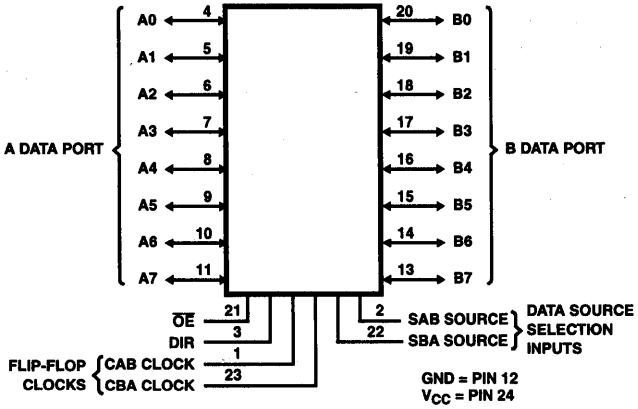
Pinout

CD74FCT646
(PDIP, SOIC, SSOP)
TOP VIEW



8 BiCMOS FCT PRODUCTS

Functional Diagram



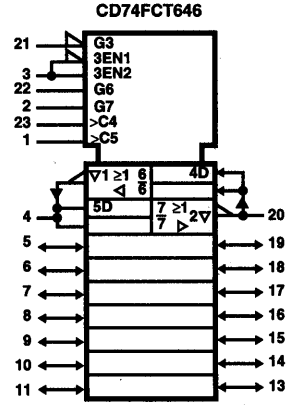
TRUTH TABLE (Note 1)

INPUTS						DATA I/O (Note 2)		OPERATION OR FUNCTION
OE	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	CD74FCT646
X	X	↑	X	X	X	Input	Not Specified	Store A, B Unspecified
X	X	X	↑	X	X	Not Specified	Input	Store B, A Unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, Hold Storage
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus

NOTES:

1. H= HIGH Voltage Level
   L = LOW Voltage Level
   ↑ = Transition from Low to High
   X = Immaterial
2. The data output functions may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low to high transition of the clock inputs. To prevent excess currents in the high Z modes, all I/O terminals should be terminated with 10kΩ resistors.

IEC Logic Symbol



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) . . . . . -0.5V to 6V
DC Diode Current, I_{IK} (For V_I < -0.5V) . . . . . -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) . . . . . -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO . . . . . -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 528mA

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
PDIP Package 75
SOIC Package 75
SSOP Package 125
Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC and SSOP-Lead Tips Only)

Operating Conditions

Operating Temperature Range, T_A . . . . . 0°C to 70°C
Supply Voltage Range, V_{CC} . . . . . 4.75V to 5.25V
DC Input Voltage, V_I . . . . . 0 to V_{CC}
DC Output Voltage, V_O . . . . . 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv . . . . . 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V (Note 6)

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 4)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 5)		Max	-	1.6	-	1.6	mA

NOTES:

4. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
5. Inputs that are not measured are at V_{CC} or GND.
6. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70°C.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 1) (Note 7)

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Propagation Delays		(Note 8)				
Store An → Bn, Store Bn → An, An → Bn, Bn → An	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
Select to Data	t_{PLH}, t_{PHL}	5	8.3	2	11	ns
Output Enable to Output	t_{PZL}, t_{PZH}	5	10.5	2	14	ns
Output Disable to Output	t_{PLZ}, t_{PHZ}	5	6.8	2	9	ns
Power Dissipation Capacitance	C_{PD} (Note 8)	-	-	-	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1	-	-	V
Input Capacitance	C_I	-	-	-	10	pF
Input/Output Capacitance	$C_{I/O}$	-	-	-	15	pF

NOTES:

7. 5V: Minimum is at 5.25V for 0°C to 70°C, Maximum is at 4.75V for 0°C to 70°C, Typical is at 5V.
8. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2$ f_I C_{PD} + V_O^2 $f_O C_L$ + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

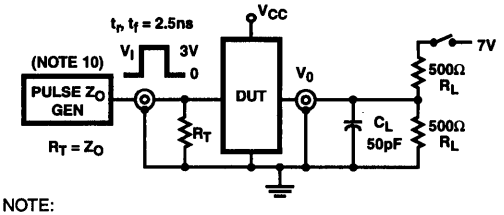
Prerequisite For Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Maximum Frequency	f_{MAX}	5 (Note 9)	-	85	-	ns
Data to Clock Setup Time	t_{SU}	5	-	4	-	ns
Data to Clock Hold Time	t_H	5	-	2	-	ns
Clock Pulse Width	t_W	5	-	6	-	ns

NOTE:

9. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

10. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

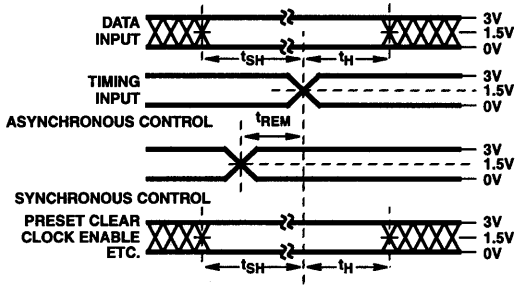


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

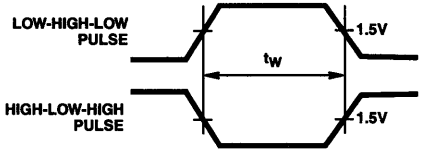


FIGURE 3. PULSE WIDTH

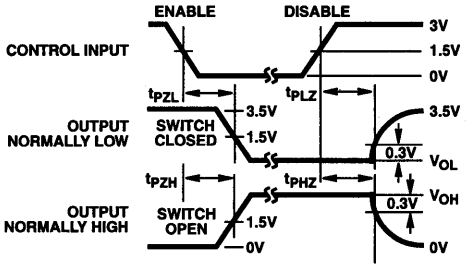


FIGURE 4. ENABLE AND DISABLE TIMING

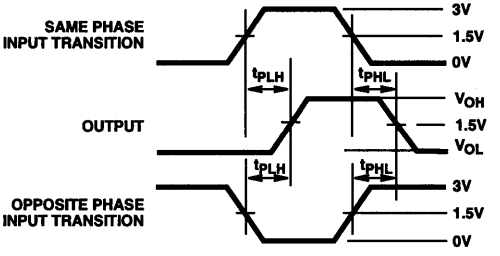
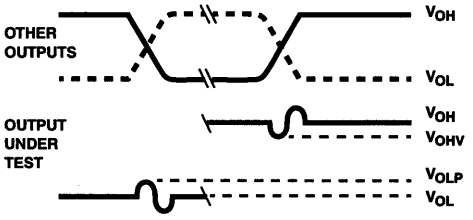


FIGURE 5. PROPAGATION DELAY



NOTES:

11. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
12. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
13. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT651, CD74FCT652

BiCMOS FCT Interface Logic, Octal Bus Transceivers/Registers, Three-State

Januyary 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- **Buffered Inputs**
- **Typical Propagation Delay: 6.8ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF**
- **CD75FCT651**
  - **Inverting**
- **CD74FCT652**
  - **Noninverting**
- **Family Features**
  - **SCR Latchup Resistant BiCMOS Process and Circuit Design**
  - **Speed of Bipolar FAST™/AS/S**
  - **64mA Output Sink Current**
  - **Output Voltage Swing Limited to 3.7V at V_{CC} = 5V**
  - **Controlled Output Edge Rates**
  - **Input/Output Isolation to V_{CC}**
  - **BiCMOS Technology with Low Quiescent Power**

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT651EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT652EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT651M	0 to 70	24 Ld SOIC	M24.3
CD74FCT652M	0 to 70	24 Ld SOIC	M24.3

NOTE: When ordering the suffix M packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

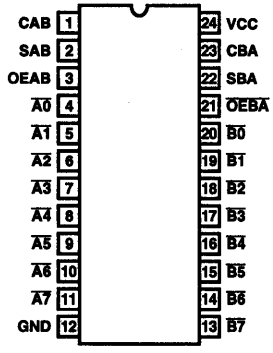
The CD74FCT651 and CD74FCT652 three-state, octal bus transceivers/registers use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64 milliamperes.

These devices consist of bus transceiver circuits, D-Type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OEAB and $\overline{OEBA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data. The following examples demonstrate the four fundamental bus management functions that can be performed with the octal bus transceivers and registers.

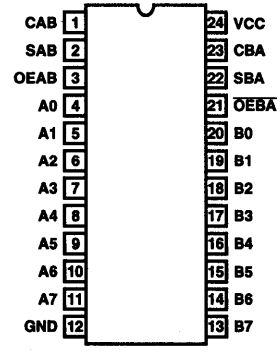
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low to high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-Type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

Pinouts

CD74FCT651 (PDIP, SOIC)
TOP VIEW



CD74FCT652 (PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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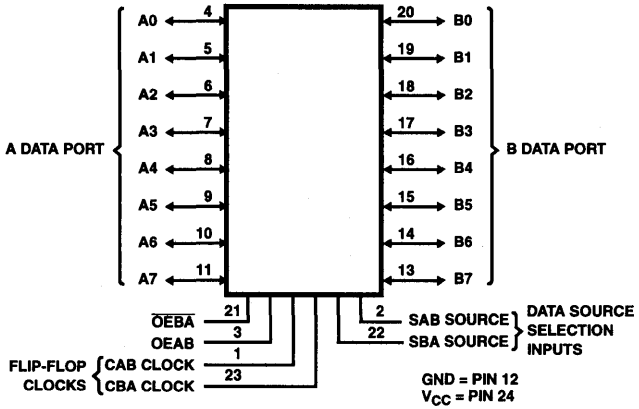
File Number **2394.2**

Functional Diagram



TRUTH TABLE

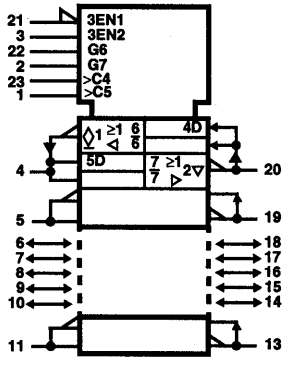
INPUTS						DATA I/O		OPERATION OR FUNCTION	
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	CD74FCT651	CD74FCT652
L	H	H or L	H or L	X	X	Input	Input	Isolation (Note 1)	Isolation (Note 1)
L	H	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified (2)	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X (3)	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified (2)	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X (3)	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus Stored B Data to A Bus

NOTES:

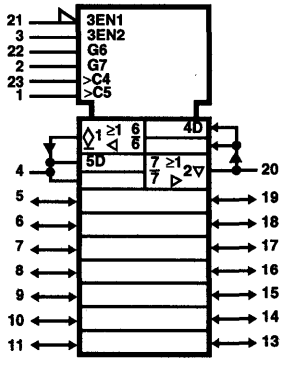
1. To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.
2. The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
3. Select control = L; clocks can occur simultaneously. Select control = H; clocks must be staggered in order to load both registers.

IEC Logic Symbol

CD74FCT651



CD74FCT652



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) . . . . . -0.5V to 6V
DC Input Diode Current, I_{IK} (For V_I < -0.5V) . . . . . -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) . . . . . -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO . . . . . -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 528mA

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
PDIP Package	75
SOIC Package	75

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC-Lead Tips Only)

Operating Conditions

Operating Temperature Range (T_A) . . . . . 0°C to 70°C
Supply Voltage Range, V_{CC} . . . . . 4.75V to 5.25V
DC Input Voltage, V_I . . . . . 0 to V_{CC}
DC Output Voltage, V_O . . . . . 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv . . . . . 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 5)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 6)		Max	-	1.6	-	1.6	mA

NOTES:

5. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
6. Inputs that are not measured are at V_{CC} or GND.
7. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70°C.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 4)

PARAMETER		SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays							
Stored $\overline{An}$ → Bn	CD74FCT651	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
Stored An → Bn	CD74FCT652	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
Stored $\overline{Bn}$ → An	CD74FCT651	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
Stored Bn → An	CD74FCT652	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
$\overline{An}$ → Bn	CD74FCT651	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
An → Bn	CD74FCT652	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
$\overline{Bn}$ → An	CD74FCT651	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
Bn → An	CD74FCT652	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
Select to Data	CD74FCT651, CD74FCT652	t_{PLH}, t_{PHL}	5	8.3	2	11	ns
Three-State Enabling Time, Bus to Output or Register to Output	CD74FCT651, CD74FCT652	t_{PZL}, t_{PZH}	5	7.5	2	10	ns
Three-State Disabling Time, Bus to Output or Register to Output	CD74FCT651, CD74FCT652	t_{PLZ}, t_{PHZ}	5	7.5	2	10	ns
Power Dissipation Capacitance		C_{PD} (Note 8)	–				pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV}	5	0.5 Typical at 25°C			V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP}	5	1 Typical at 25°C			V
Input Capacitance		C_I	-	-	-	10	pF
Input/Output Capacitance		$C_{I/O}$	-	-	-	15	pF

NOTE:

8. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$ where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

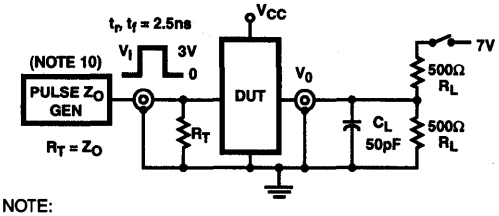
Prerequisite for Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Maximum Frequency	f_{MAX}	5 (Note 9)	-	85	-	MHz
Data to Clock Setup Time	t_{SU}	5	-	4	-	ns
Data to Clock Hold Time	t_H	5	-	2	-	ns
Clock Pulse Width	t_W	5	-	6	-	ns

NOTE:

9. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

10. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

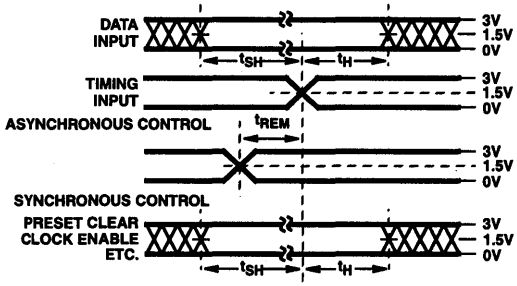


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

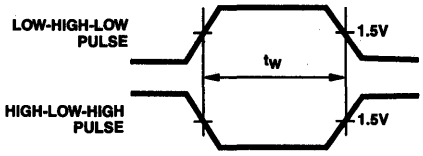


FIGURE 3. PULSE WIDTH

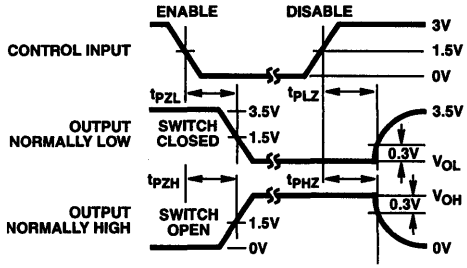


FIGURE 4. ENABLE AND DISABLE TIMING

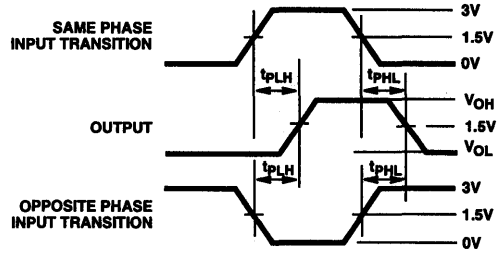
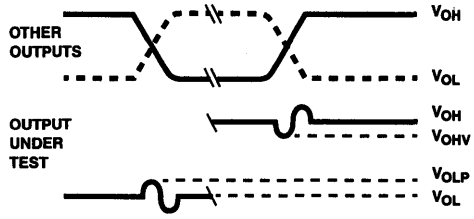


FIGURE 5. PROPAGATION DELAY



NOTES:

11. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
12. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
13. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

CD74FCT653, CD74FCT654

January 1997

FCT Interface Logic, Octal Bus Transceivers/ Registers, Open Drain (A Side), Three-State (B Side)

Features

- Buffered Inputs
- Typical Propagation Delay: 6.8ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- CD74FCT653
  - Inverting
- CD74FCT654
  - Non-Inverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 64mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT653EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT654EN	0 to 70	24 Ld PDIP	E24.3
CD74FCT653M	0 to 70	24 Ld SOIC	M24.3
CD74FCT654M	0 to 70	24 Ld SOIC	M24.3

NOTE: When ordering the suffix M packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

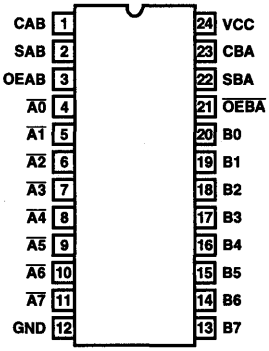
The CD74FCT653 and CD74FCT654 octal bus transceivers/registers use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 64mA.

The CD74FCT653 is an inverting type having open drains on the A output and three state outputs on the B side. The CD74FCT654 differs only in that it is a noninverting type. These devices consist of bus transceiver circuits, D-Type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables OEAB and $\overline{OEBA}$ are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data. The following examples demonstrate the four fundamental bus management functions that can be performed with the octal bus transceivers and registers.

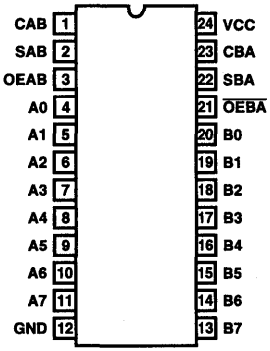
Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low to high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-Type flip-flops by simultaneously enabling OEAB and $\overline{OEBA}$. In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

Pinouts

CD74FCT653
(PDIP, SOIC)
TOP VIEW



CD74FCT654
(PDIP, SOIC)
TOP VIEW



8 BiCMOS FCT PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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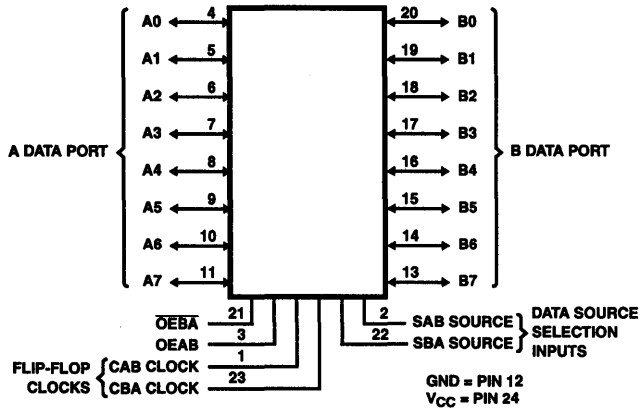
File Number 2403.2

Functional Diagram



TRUTH TABLE

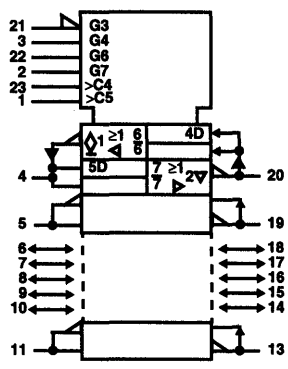
INPUTS						DATA I/O		OPERATION OR FUNCTION	
OEAB	$\overline{OEBA}$	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	CD74FCT653	CD74FCT654
L	H	H or L	H or L	X	X	Input	Input	Isolation (Note 1)	Isolation (Note 1)
L	H	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified (2)	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X (3)	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Unspecified (2)	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X (3)	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus Stored B Data to A Bus

NOTES:

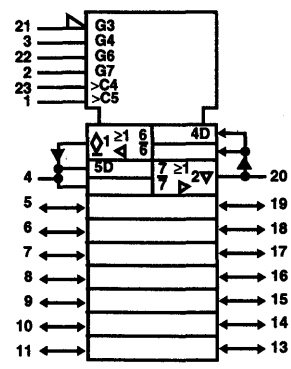
1. To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.
2. The data output functions may be enabled or disabled by various signals at the OEAB or $\overline{OEBA}$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.
3. Select control = L; clocks can occur simultaneously. Select control = H; clocks must be staggered in order to load both registers.

IEC Logic Symbols

CD74FCT653



CD74FCT654



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) ..... -0.5V to 6V
DC Diode Current, I_{IK} (For V_I < -0.5V) ..... -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) ..... -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO ..... -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 528mA

Thermal Information

Thermal Resistance (Typical, Note 4)	θ_{JA} (°C/W)
PDIP Package	75
SOIC Package	75

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC-Lead Tips Only)

Operating Conditions

Operating Temperature Range, T_A ..... 0°C to 70°C
Supply Voltage Range, V_{CC} ..... 4.75V to 5.25V
DC Input Voltage, V_I ..... 0 to V_{CC}
DC Output Voltage, V_O ..... 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv ..... 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 5)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-60	-	-60	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 6)		Max	-	1.6	-	1.6	mA

NOTES:

5. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
6. Inputs that are not measured are at VCC or GND.
7. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max at 70°C.

Switching Specifications Over Operating Range t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figures 3, 4)

PARAMETER		SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays							
Stored An → $\overline{Bn}$	CD74FCT653	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
Stored An → Bn	CD74FCT654	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
Stored $\overline{Bn}$ → An	CD74FCT653	t_{PZL}	5	6	2	8	ns
		t_{PLZ}	5	6.8	2	9	ns
Stored Bn → An	CD74FCT654	t_{PZL}, t_{PLZ}	5	6.8	2	9	ns
An → $\overline{Bn}$	CD74FCT653	t_{PLH}, t_{PHL}	5	6	2	8	ns
An → Bn	CD74FCT654	t_{PLH}, t_{PHL}	5	6.8	2	9	ns
$\overline{Bn}$ → An	CD74FCT653	t_{PZL}	5	6	2	8	ns
		t_{PLZ}	5	6.8	2	9	ns
Bn → An	CD74FCT654	t_{PZL}, t_{PLZ}	5	6.8	2	9	ns
Select to Data (B Bus)	CD74FCT653, CD74FCT654	t_{PLH}, t_{PHL}	5	8.3	2	11	ns
Select to Data (A Bus)	CD74FCT653	t_{PZL}	5	6	2	8	ns
		t_{PLZ}	5	6.8	2	9	ns
Select to Data (A Bus)	CD74FCT654	t_{PZL}, t_{PLZ}	5	6.8	2	9	ns
Three-State Enabling Times (B Bus), Bus to Output or Register to Output	CD74FCT653	t_{PZL}, t_{PZH}	5	10.5	2	14	ns
	CD74FCT654	t_{PZL}, t_{PZH}	5	11.3	2	15	ns
Three-State Disabling Time (B Bus), Bus to Output or Register to Output	CD74FCT653	t_{PLZ}, t_{PZH}	5	6.8	2	9	ns
	CD74FCT654	t_{PLZ}, t_{PZH}	5	6.8	2	9	ns
Off State Enabling Times (A Bus), Bus to Output or Register to Output	CD74FCT653	t_{PZL}	5	10.5	2	14	ns
	CD74FCT654	t_{PZL}	5	11.3	2	15	ns
Off State Disabling Time (A Bus), Bus to Output or Register to Output	CD74FCT653	t_{PLZ}	5	6.8	2	9	ns
	CD74FCT654	t_{PLZ}	5	6.8	2	9	ns

Prerequisite for Switching t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figures 3, 4)

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Maximum Frequency (B Side as Outputs)	f_{MAX}	5 (Note 8)	-	80	-	MHz
Data to Clock Setup Time	t_{SU}	5	-	4	-	ns
Data to Clock Hold Time	t_H	5	-	2	-	ns
Clock Pulse Width	t_W	5	-	6	-	ns

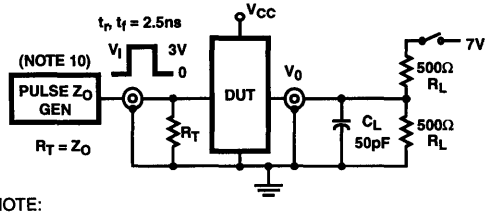
Switching t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figures 3, 4)

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Power Dissipation Capacitance	C_{PD}	-	-	-	-	pF
Min (Valley) V_{OH} (B Side) During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} (Figure 1)	5	0.5	-	-	V
Max (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} (Figure 1)	5	1	-	-	V
Input Capacitance	C_I	-	-	-	10	pF
Three-State Output Capacitance (B Side)	C_O	-	-	-	15	pF
Off-State Output Capacitance (A Side)	C_O	-	-	-	15	pF

NOTES:

8. 5V: minimum is at 4.75V for 0°C to 70°C, typical is at 5V.
9. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption. PD (per package) = $V_{CC}\, I_{CC} + \Sigma(V_{CC}^2\, f_I\, C_{PD} + V_O^2\, f_O C_L + V_{CC}\, \Delta I_{CC}\, D)$ where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

Test Circuits and Waveforms



NOTE:

10. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.
R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.
V_{IN} = 0V to 3V.
Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

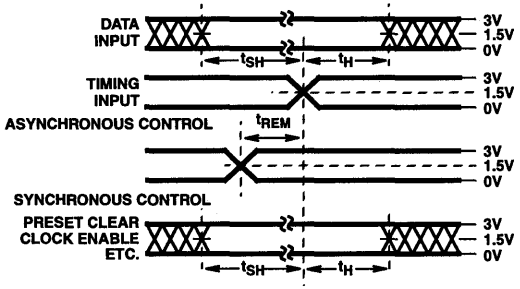


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

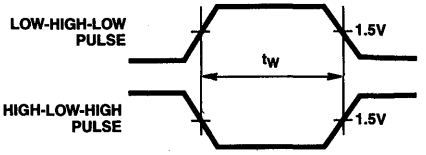


FIGURE 3. PULSE WIDTH

Test Circuits and Waveforms (Continued)

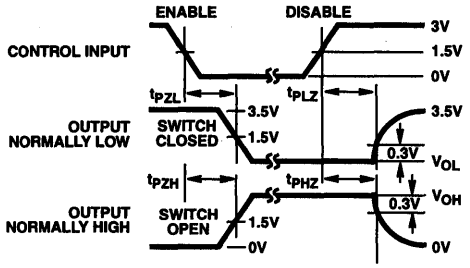


FIGURE 4. ENABLE AND DISABLE TIMING

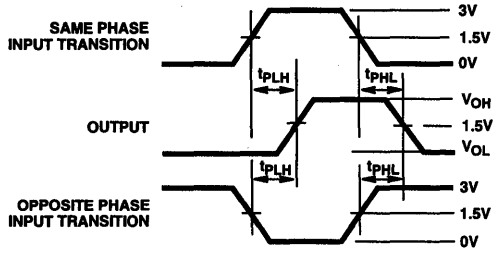
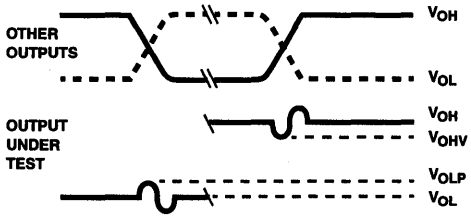


FIGURE 5. PROPAGATION DELAY



NOTES:

11. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
12. Input pulses have the following characteristics:
    $P_{RR} \leq 1MHz$, $t_r = 2.5ns$, $t_f = 2.5ns$, skew 1ns.
13. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT821A, CD74FCT822A

BiCMOS FCT Interface Logic, 10- Bit D-Type Flip-Flops, Three-State

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 7.5ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- CD74FCT821A
  - Noninverting
- CD74FCT822A
  - Inverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Description

The CD74FCT821A and CD74FCT822A ten bit, D-Type, three-state, positive edge triggered flip-flops use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

The ten flip-flops enter data into their registers on the LOW to HIGH transition of the clock(CP). The Output Enable ($\overline{OE}$) controls the three state outputs and is independent of the register operation. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The CD74FCT821A and CD74FCT822A share the same configurations, but the CD74FCT821A outputs are noninverted while the CD74FCT822A devices have inverted outputs.

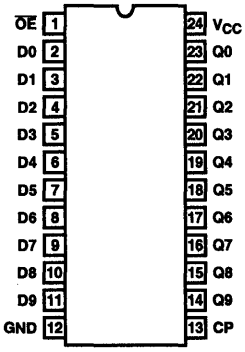
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT821AEN	0 to 70	24 Ld PDIP	E24.3
CD74FCT822AEN	0 to 70	24 Ld PDIP	E24.3
CD74FCT821AM	0 to 70	24 Ld SOIC	M24.3

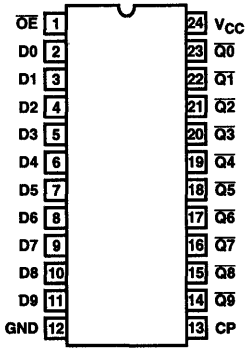
NOTE: When ordering the suffix M packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinouts

CD74FCT821A
(PDIP, SOIC)
TOP VIEW



CD74FCT822A
(PDIP, SOIC)
TOP VIEW



8 BiCMOS FCT PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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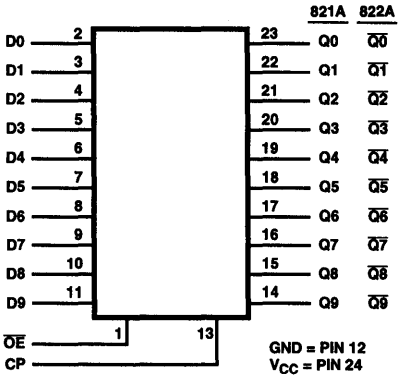
File Number 2390.2

Functional Diagram



TRUTH TABLE

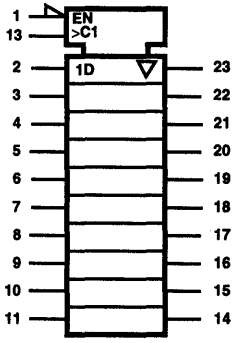
INPUTS			OUTPUTS	
			CD74FCT821A	CD74FCT822A
$\overline{OE}$	CP	DN	QN	$\overline{QN}$
L	↑	H	H	L
L	↑	L	L	H
L	L	X	NC	NC
H	X	X	Z	Z

NOTE:

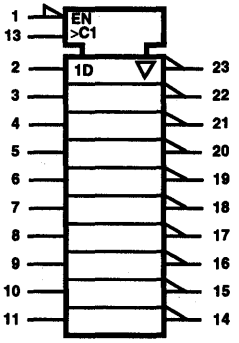
1. H = HIGH level (steady state)
   L = LOW level (steady state)
   X = Immaterial
   ↑ = Transition from LOW to HIGH level
   Z = HIGH impedance
   NC = No change

IEC Logic Symbol

CD74FCT821A



CD74FCT822A



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) ..... -0.5V to 6V
DC Diode Current, I_{IK} (For V_I < -0.5V) ..... -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) ..... -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO ..... -30mA
DC V_{CC} Current (I_{CC}) 260mA
DC Ground Current (I_{GND}) 500mA

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	75
SOIC Package	75

Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC-Lead Tips Only)

Operating Conditions

Operating Temperature Range, T_A ..... 0°C to 70°C
Supply Voltage Range, V_{CC} ..... 4.75V to 5.25V
DC Input Voltage, V_I ..... 0 to V_{CC}
DC Output Voltage, V_O ..... 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv ..... 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC}, Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-75	-	-75	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70°C.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (See Figures)

PARAMETER		SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays (Note 6)							
Clock to Q	CD74FCT821A	t_{PLH}, t_{PHL}	5	7.5	1.5	10	ns
Clock to $\overline{Q}$	CD74FCT822A	t_{PLH}, t_{PHL}	5	7.5	1.5	10	ns
Output Enable to Q	CD74FCT821A	t_{PZL}, t_{PZH}	5	9	1.5	12	ns
Output Disable to Q	CD74FCT821A	t_{PLZ}, t_{PHZ}	5	6	1.5	8	ns
Output Enable to $\overline{Q}$	CD74FCT822A	t_{PZL}, t_{PZH}	5	9	1.5	12	ns
Output Disable to $\overline{Q}$	CD74FCT822A	t_{PLZ}, t_{PHZ}	5	6	1.5	8	ns
Power Dissipation Capacitance (Note 7)		C_{PD}	–				pF
Minimum (Valley) V_{OH} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV}	5	0.5 Typical at 25°C			V
Maximum (Peak) V_{OL} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP}	5	1 Typical at 25°C			V
Input Capacitance		C_I	-	-	-	10	pF
Three-State Output Capacitance		C_O	-	-	-	15	pF

NOTES:

6. 5V: Minimum is at 5.25V for 0°C to 70°C, Maximum is at 4.75 for 0°c t0 70°C, Typical is at 5V.
7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + Σ (V_{CC}^2 f_I C_{PD} + V_O^2 $f_O C_L$ + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

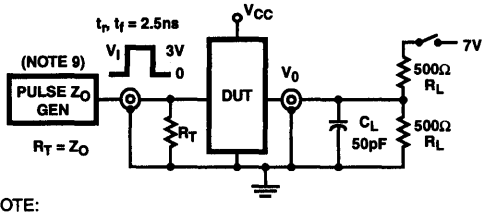
Prerequisite for Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Maximum Frequency (Note 8)	f_{MAX}	5	-	70	-	MHz
Data to Clock Setup Time	t_{SU}	5	-	4	-	ns
Data to Clock Hold Time	t_H	5	-	2	-	ns
Clock Pulse Width	t_W	5	-	7	-	ns

NOTE:

8. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

9. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

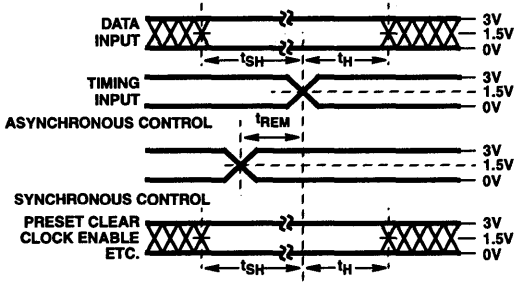


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

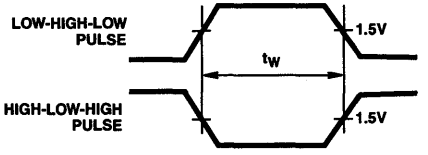


FIGURE 3. PULSE WIRTH

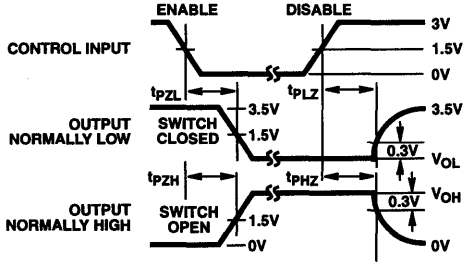


FIGURE 4. ENABLE AND DISABLE TIMING

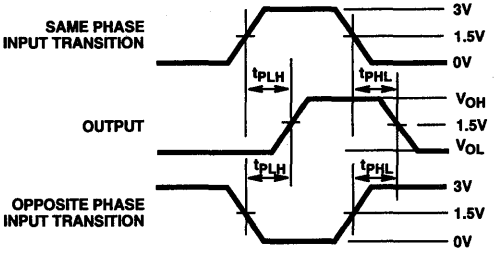
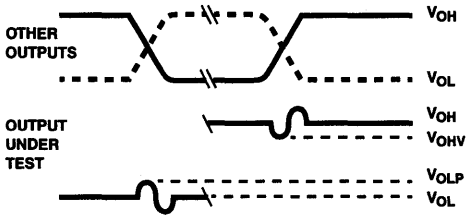


FIGURE 5. PROPAGATION DELAY



NOTES:

10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
11. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT823A, CD74FCT824A

BiCMOS FCT Interface Logic, 9-Bit D-Type Flip-Flops, Three-State

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 7.5ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- Positive Edge Triggered
- CD74FCT824A
  - Inverting
- CD74FCT823A
  - Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Description

The CD74FCT823A and CD74FCT824A nine bit, D-Type, three-state, positive edge triggered flip-flops use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

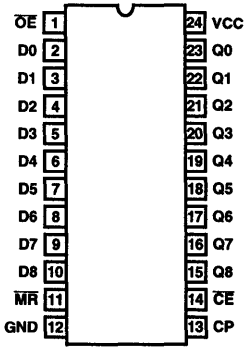
The nine flip-flops enter data into their registers on the LOW to HIGH transition of the clock (CP). The Output Enable (OE) controls the three-state outputs and is independent of the register operation. These nine bit wide buffered registers with clock Enable (CE) and Master Reset (MR) inputs are ideal for parity bus interfacing in high performance microprogrammed systems.

Ordering Information

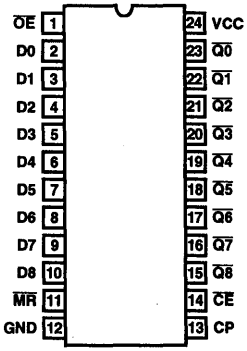
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT823AEN	0 to 70	24 Ld PDIP	E24.3
CD74FCT824AEN	0 to 70	24 Ld PDIP	E24.3

Pinout

CD74FCT823A
(PDIP)
TOP VIEW



CD74FCT824A
(PDIP)
TOP VIEW

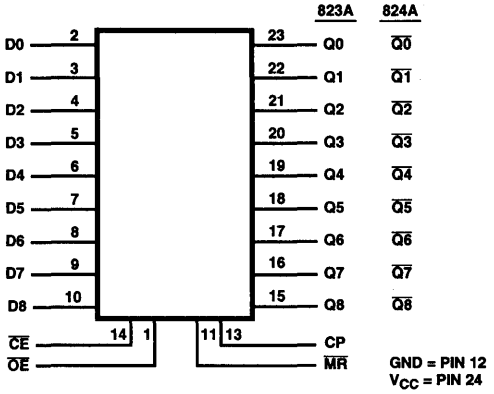


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **2389.2**

Functional Diagram



TRUTH TABLE (Note 1)

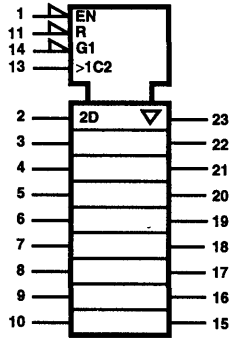
INPUTS					Q OUTPUTS		
$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	D	CP	CD74FCT823A	CD74FCT824A	FUNCTION
H	X	L	L	↑	Z	Z	High Z
H	X	L	H	↑	Z	Z	
H	L	X	X	X	Z	Z	Reset
L	L	X	X	X	L	L	
H	H	H	X	X	Z	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	↑	Z	Z	Load
H	H	L	H	↑	Z	Z	
L	H	L	L	↑	L	H	
L	H	L	H	↑	H	L	

NOTE:

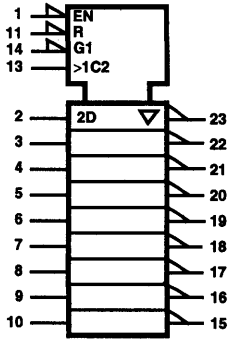
1. H= HIGH Voltage Level
   L = LOW Voltage Level
   NC = No Change
   ↑ = LOW to HIGH Transition
   X = Don't Care
   Z = HIGH Impedance

IEC Logic Symbol

CD74FCT823A



CD74FCT824A



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) ..... -0.5V to 6V
DC Diode Current, I_{IK} (For V_I < -0.5V) ..... -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) ..... -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO ..... -30mA
DC V_{CC} Current (I_{CC}) 234mA
DC Ground Current (I_{GND}) 453mA

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
PDIP Package 75
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C

Operating Conditions

Operating Temperature Range, T_A ..... 0°C to 70°C
Supply Voltage Range, V_{CC} ..... 4.75V to 5.25V
DC Input Voltage, V_I ..... 0 to V_{CC}
DC Output Voltage, V_O ..... 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv ..... 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-75	-	-75	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70°C.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 1)

PARAMETER		SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays			(Note 6)				
Clock to Q	CD74FCT823A	t_{PLH}, t_{PHL}	5	7.5	1.5	10	ns
Clock to $\overline{Q}$	CD74FCT824A	t_{PLH}, t_{PHL}	5	7.5	1.5	10	ns
$\overline{MR}$ to Q		t_{PHL}	5	10.5	1.5	14	ns
Output Enable to Q	CD74FCT823A	t_{PZL}, t_{PZH}	5	9	1.5	12	ns
Output Disable to Q	CD74FCT823A	t_{PLZ}, t_{PHZ}	5	6	1.5	8	ns
Output Enable to $\overline{Q}$	CD74FCT824A	t_{PZL}, t_{PZH}	5	9	1.5	12	ns
Output Disable to $\overline{Q}$	CD74FCT824A	t_{PLZ}, t_{PHZ}	5	6	1.5	8	ns
Power Dissipation Capacitance		C_{PD} (Note 7)	-	-	-	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV}	5	**0.5**	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP}	5	1	-	-	V
Input Capacitance		C_I	-	-	-	10	pF
Three-State Output Capacitance		C_O	-	-	-	15	pF

NOTES:

6. 5V: Minimum is at 5.25V for 0°C to 70°C, Maximum is at 4.75V for 0°C to 70°C, Typical is at 5V.
7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$ where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

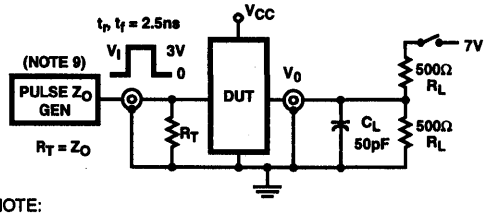
Prerequisite for Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Maximum Clock Frequency	f_{MAX}	5 (Note 8)	-	70	-	MHz
Master Reset Recovery Time	t_{REC}	5	-	7	-	ns
Setup Time, Data to Clock, $\overline{CE}$ to Clock	t_{SU}	5	-	4	-	ns
Hold Time - Data, $\overline{CE}$	t_H	5	-	2	-	ns
Pulse Width - Clock, $\overline{MR}$	t_W	5	-	7	-	ns

NOTE:

8. 5V: Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

9. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

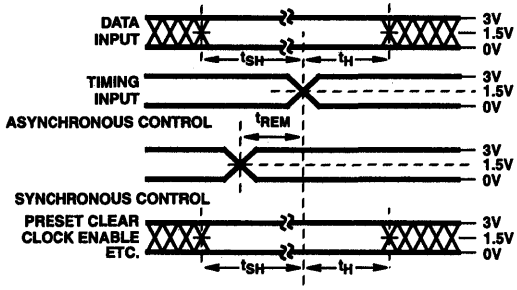


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

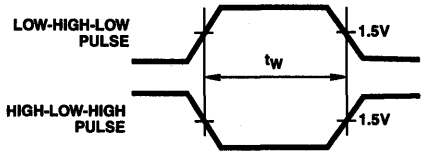


FIGURE 3. PULSE WIDTH

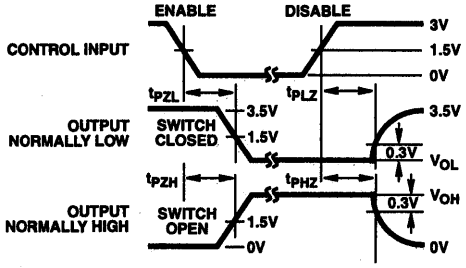


FIGURE 4. ENABLE AND DISABLE TIMING

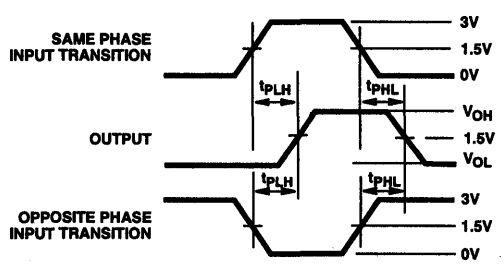
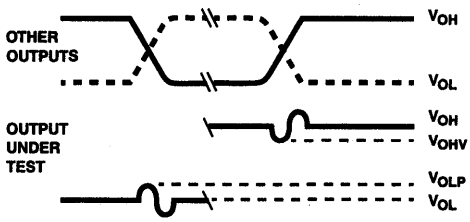


FIGURE 5. PROPAGATION DELAY



NOTES:

10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
11. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT841A, CD74FCT842A

BiCMOS FCT Interface Logic, 10-Bit Transparent Latches, Three-State

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 6.8ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF (CD74FCT841A)
- CD74FCT841A
  - Noninverting
- CD74FCT842A
  - Inverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT841AEN	0 to 70	24 Ld PDIP	E24.3
CD74FCT841AM	0 to 70	24 Ld SOIC	M24.3
CD74FCT842AM	0 to 70	24 Ld SOIC	M24.3

NOTE: When ordering the suffix M packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

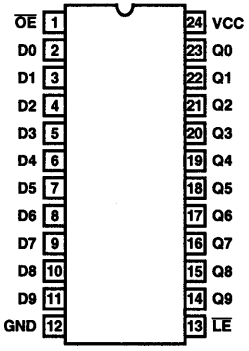
Description

The CD74FCT841A and CD74FCT842A ten bit transparent latches use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

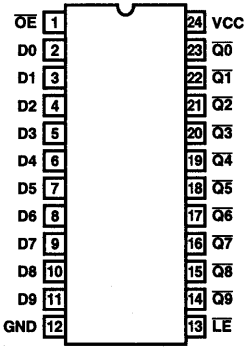
The CD74FCT841A and CD74FCT842A outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the three state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The latch operation is independent of the state of the Output Enable. These devices provide extra data width for wider address/data paths or buses carrying parity.

Pinouts

CD74FCT841A
(PDIP, SOIC)
TOP VIEW



CD74FCT842A
(PDIP, SOIC)
TOP VIEW



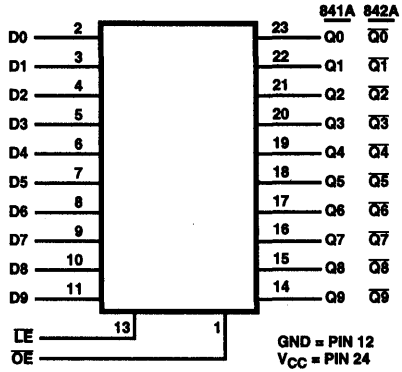
8 BiCMOS FCT PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **2397.2**

Functional Diagram



TRUTH TABLE (Note 1)

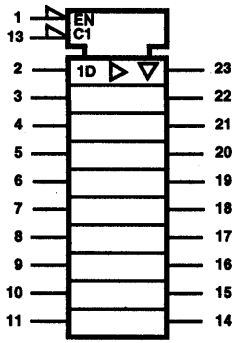
OUTPUT ENABLE	LATCH ENABLE	DATA	CD74FCT841A OUTPUT	CD74FCT842A OUTPUT
L	H	H	H	L
L	H	L	L	H
L	L	l	L	H
L	L	h	H	L
H	X	X	Z	Z

NOTE:

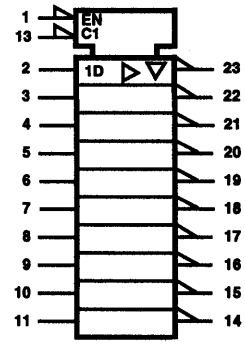
1. H= HIGH Voltage Level
   L = LOW Voltage Level
   l = LOW Voltage Level one set up time prior to the high-to-low latch enable transition.
   h = HIGH Voltage Level one set up time prior to the high-to-low latch enable transition.
   X = Immaterial
   Z = HIGH Impedance

IEC Logic Symbol

CD74FCT841A



CD74FCT842A



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) ..... -0.5V to 6V
DC Diode Current, I_{IK} (For V_I < -0.5V) ..... -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) ..... -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO ..... -30mA
DC V_{CC} Current (I_{CC}) 260mA
DC Ground Current (I_{GND}) 500mA

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} ($^oC/W$)
PDIP Package 75
SOIC Package 75
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC-Lead Tips Only)

Operating Conditions

Operating Temperature Range, T_A ..... 0°C to 70°C
Supply Voltage Range, V_{CC} ..... 4.75V to 5.25V
DC Input Voltage, V_I ..... 0 to V_{CC}
DC Output Voltage, V_O ..... 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv ..... 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS			AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}	-	-	4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}	-	-	4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}	-	Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND	-	Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}	-	Max	-	0.5	-	10	µA
	I_{OZL}	GND	-	Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND	-	Max	-75	-	-75	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)	-	Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at VCC or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Electrical Specifications table, e.g., 1.6mA Max. at 70°C.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 1)

PARAMETER		SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays							
Data to Outputs	CD74FCT841A	t_{PLH}, t_{PHL}	5 (Note 6)	6.8	1.5	9	ns
	CD74FCT842A	t_{PLH}, t_{PHL}	5	7.5	1.5	10	ns
$\overline{LE}$ to Outputs	CD74FCT841A	t_{PLH}, t_{PHL}	5	9	2	12	ns
	CD74FCT842A	t_{PLH}, t_{PHL}	5	9	2	12	ns
Output Enable Times	CD74FCT841A	t_{PZL}, t_{PZH}	5	8.6	1.5	11.5	ns
	CD74FCT842A	t_{PZL}, t_{PZH}	5	8.6	1.5	11.5	ns
Output Disable Times	CD74FCT841A	t_{PLZ}, t_{PHZ}	5	6	1.5	8	ns
	CD74FCT842A	t_{PLZ}, t_{PHZ}	5	6	1.5	8	ns
Power Dissipation Capacitance		C_{PD} (Note 7)	-	-	-	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV}	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP}	5	1	-	-	V
Input Capacitance		C_I	-	-	-	10	pF
Three State Output Capacitance		C_O	-	-	-	15	pF

NOTES:

6. 5V: Minimum is at 5.25V for 0°C to 70°C, Maximum is at 4.75V for 0°C to 70°C, Typical is at 5V.
7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$ where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

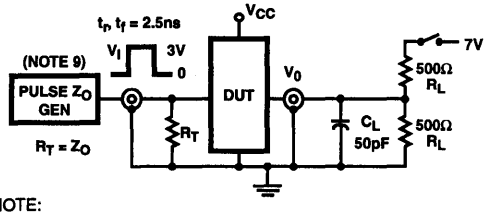
Prerequisite for Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Setup Time, Data to $\overline{LE}$	t_{SU}	5 (Note 8)	-	2.5	-	ns
Hold Time, Data to $\overline{LE}$	t_H	5	-	2.5	-	ns
$\overline{LE}$ Pulse Width	t_W	5	-	4	-	ns

NOTE:

8. 5V: Minimum is at 4.5V, Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

9. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

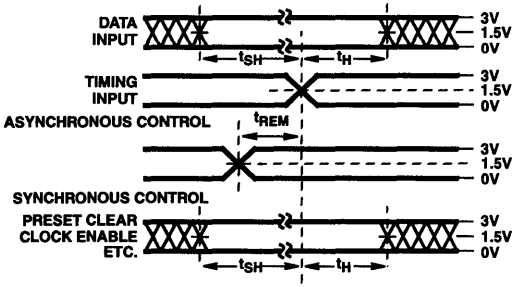


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

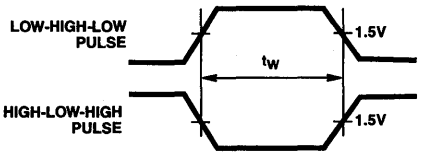


FIGURE 3. PULSE WIDTH

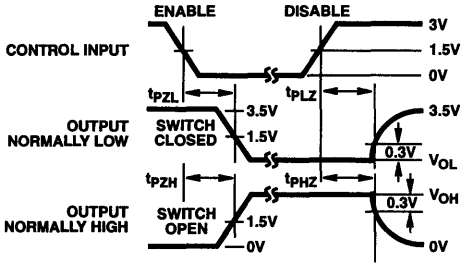


FIGURE 4. ENABLE AND DISABLE TIMING

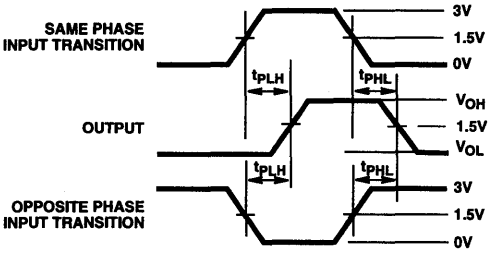
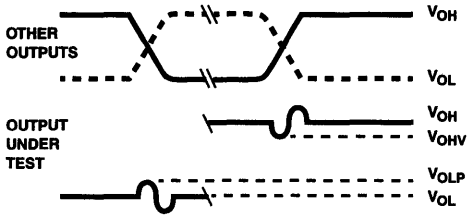


FIGURE 5. PROPAGATION DELAY



NOTES:

10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
11. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT843A, CD74FCT844A

BiCMOS FCT Interface Logic, 9-Bit Transparent Latches, Three-State

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 6.8ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF (FCT843A)
- CD74FCT843A
  - Noninverting
- CD74FCT844A
  - Inverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT844AEN	0 to 70	24 Ld PDIP	E24.3
CD74FCT843AM	0 to 70	24 Ld SOIC	M24.3

NOTE: When ordering the suffix M package, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

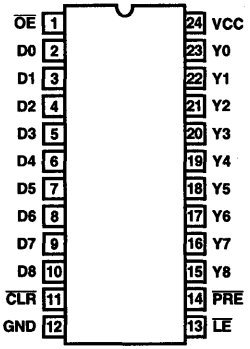
Description

The CD74FCT843A and CD74FCT844A nine bit transparent latches use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

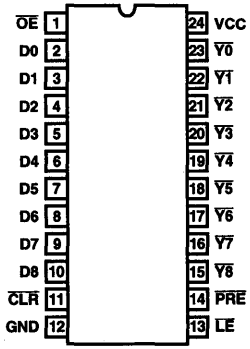
The CD74FCT843A and CD74FCT844A outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the three state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The latch operation is independent of the state of the Output Enable. These devices, having Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$), are ideal for parity bus interfacing. When $\overline{PRE}$ is low, the outputs are HIGH if $\overline{OE}$ is LOW. $\overline{PRE}$ overrides $\overline{CLR}$. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.

Pinouts

CD74FCT843A
(SOIC)
TOP VIEW



CD74FCT844A
(PDIP)
TOP VIEW

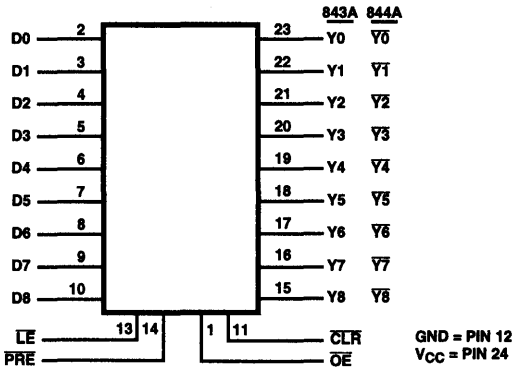


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number 2396.2

Functional Diagram



TRUTH TABLE (Note 1)

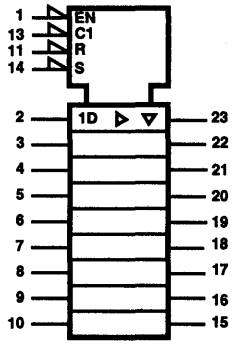
INPUTS						OUTPUTS	
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	$\overline{LE}$	843A Dn	844A Dn	Yn	FUNCTION
H	H	H	X	X	X	Z	High Z
H	H	H	L	X	X	Z	Latched (High Z)
H	H	L	H	L	H	L	Transparent
H	H	L	H	H	L	H	Transparent
H	H	L	L	X	X	NC	Latched
H	L	L	X	X	X	H	Preset
L	H	L	X	X	X	L	Clear
L	L	L	X	X	X	H	Preset
L	H	H	L	X	X	Z	Latched (High Z)
H	L	H	L	X	X	Z	Latched (High Z)

NOTE:

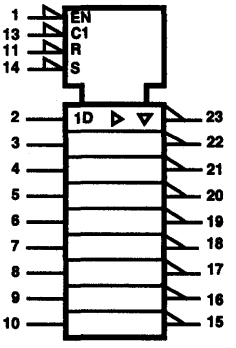
1. H= HIGH Voltage Level
   L = LOW Voltage Level
   X = Immaterial
   NC = No Change
   Z = High Impedance

IEC Logic Symbol

CD74FCT843A



CD74FCT844A



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) ..... -0.5V to 6V
DC Diode Current, I_{IK} (For V_I < -0.5V) ..... -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) ..... -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO ..... -30mA
DC V_{CC} Current (I_{CC}) 237mA
DC Ground Current (I_{GND}) 453mA

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
PDIP Package 75
SOIC Package 75
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(SOIC-Lead Tips Only)

Operating Conditions

Operating Temperature Range, T_A ..... 0°C to 70°C
Supply Voltage Range, V_{CC} ..... 4.75V to 5.25V
DC Input Voltage, V_I ..... 0 to V_{CC}
DC Output Voltage, V_O ..... 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv ..... 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS			AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-75	-	-75	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at VCC or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max. @ 70°C.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 1)

PARAMETER		SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Propagation Delays							
Data to Outputs	CD74FCT843A	t_{PLH}, t_{PHL}	5 (Note 6)	6.8	1.5	9	ns
	CD74FCT844A	t_{PLH}, t_{PHL}	5	7.5	1.5	10	ns
$\overline{LE}$ to Outputs		t_{PLH}, t_{PHL}	5	9	1.5	12	ns
$\overline{PRE}$ to Outputs		t_{PLH}	5	9	1.5	12	ns
$\overline{CLR}$ to Outputs		t_{PHL}	5	9.8	1.5	13	ns
Output Enable Times		t_{PZL}, t_{PZH}	-	10.5	1.5	14	ns
Output Disable Times		t_{PLZ}, t_{PHZ}	-	6	1.5	8	ns
Power Dissipation Capacitance		C_{PD} (Note 7)	-	-	-	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OHV}	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)		V_{OLP}	5	1	-	-	V
Input Capacitance		C_I	-	-	-	10	pF
Three-State Output Capacitance		C_O	-	-	-	15	pF

NOTES:

6. 5V: Minimum is at 5.25V for 0°C to 70°C, Maximum is at 4.75V for 0°C to 70°C, Typical is at 5V.
7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2$ f_I C_{PD} + V_O^2 $f_O C_L$ + V_{CC} ΔI_{CC} D) where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

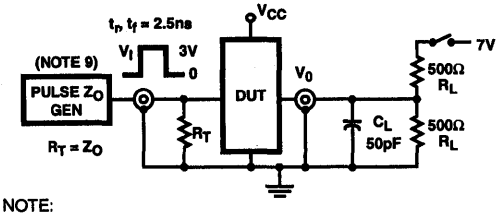
Prerequisite for Switching

PARAMETER	SYMBOL	V_{CC} (V)	25°C TYP	0°C TO 70°C MIN	0°C TO 70°C MAX	UNITS
Setup Time, Data to $\overline{LE}$	t_{SU}	5 (Note 8)	-	2.5	-	ns
Hold Time, Data to $\overline{LE}$	t_H	5	-	2.5	-	ns
$\overline{LE}$ Pulse Width	t_W	5	-	4	-	ns
$\overline{PRE}$, $\overline{CLR}$ Pulse Width	t_W	5	-	8	-	ns
$\overline{PRE}$, $\overline{CLR}$ Recovery Time	t_{REC}	5	-	14	-	ns

NOTE:

8. Minimum is at 4.75V for 0°C to 70°C, Typical is at 5V.

Test Circuits and Waveforms



NOTE:

9. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

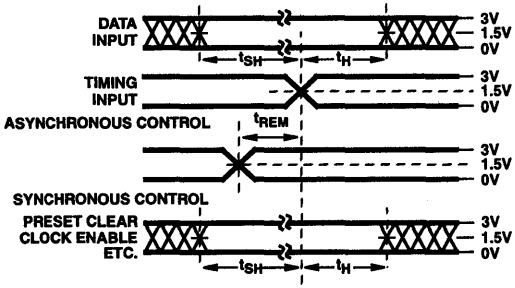


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

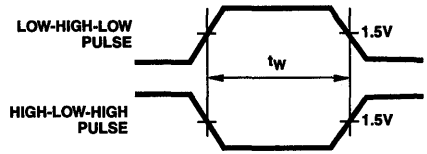


FIGURE 3. PULSE WIDTH

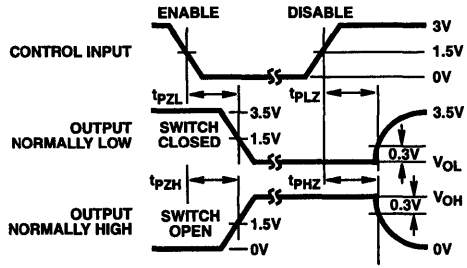


FIGURE 4. ENABLE AND DISABLE TIMING

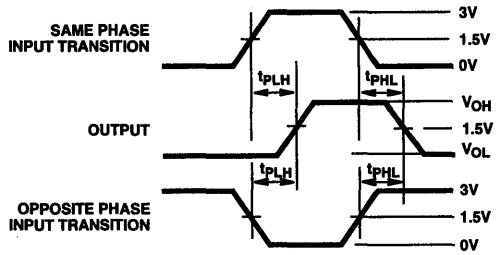
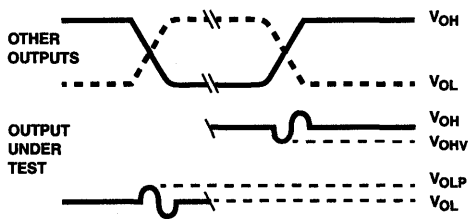


FIGURE 5. PROPAGATION DELAY



NOTES:

10. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
11. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
12. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT861A

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

BiCMOS FCT Interface Logic, 10-Bit Bus Transceiver, Three-State

Features

- Buffered Inputs
- Typical Propagation Delay: 6.0ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- CD74FCT861A
  - Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT861AM	0 to 70	24 Ld SOIC	M24.3

NOTE: When ordering the suffix M package, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

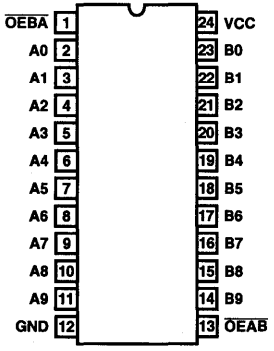
Description

The CD74FCT861A ten bit bus transceiver uses a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

This device provides extra data width for wider address/data paths or buses carrying parity. The dual Output Enable provision gives this device the capability to store data by simultaneously enabling $\overline{OEAB}$ and $\overline{OEBA}$. Each output reinforces its input under these conditions and, when all other data sources to the bus line are at high impedance, both sets of bus lines will remain in their last states.

Pinout

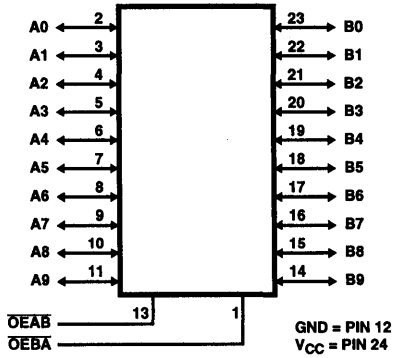
CD74FCT861A
(SOIC)
TOP VIEW



8 BiCMOS FCT PRODUCTS

File Number 2392.2

Functional Diagram



TRUTH TABLE (Note 1)

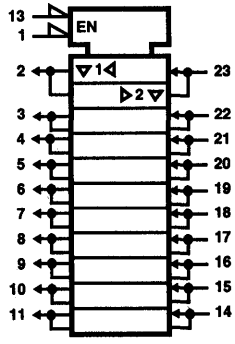
INPUTS				OUTPUTS		
$\overline{OEBA}$	$\overline{OEAB}$	B	A	B	A	FUNCTION
L	H	L	N/A	N/A	L	B Data to A Bus
L	H	H	N/A	N/A	H	B Data to A Bus
H	L	N/A	L	L	N/A	A Data to B Bus
H	L	N/A	H	H	N/A	A Data to B Bus
H	H	X	X	Z	Z	High Z
L	L	-	-	-	-	A Data to B Bus, B Data to A Bus

NOTE:

1. H= HIGH Voltage Level
   L = LOW Voltage Level
   N/A = Not Applicable
   X = Immaterial
   Z = HIGH Impedance

IEC Logic Symbol

CD74FCT861A



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) ..... -0.5V to 6V
DC Diode Current, I_{IK} (For V_I < -0.5V) ..... -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) ..... -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO ..... -30mA
DC V_{CC} Current (I_{CC}) 264mA
DC Ground Current (I_{GND}) 500mA

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
SOIC Package 75
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

Operating Conditions

Operating Temperature Range, T_A ..... 0°C to 70°C
Supply Voltage Range, V_{CC} ..... 4.75V to 5.25V
DC Input Voltage, V_I ..... 0 to V_{CC}
DC Output Voltage, V_O ..... 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv ..... 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-75	-	-75	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max at 70°C.

Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 1)

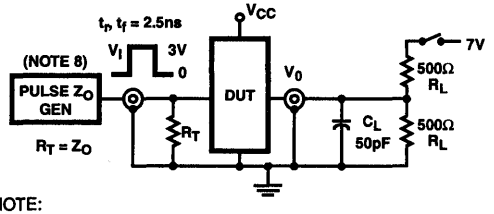
PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Propagation Delays Data to Outputs	t_{PLH}, t_{PHL}	5 (Note 6)	6	1.5	8	ns
Output Enable to Output	t_{PZL}, t_{PZH}	5	9	1.5	12	ns
Output Disable to Output	t_{PLZ}, t_{PHZ}	5	7.5	1.5	10	ns
Power Dissipation Capacitance	C_{PD} (Note 7)	-	-	-	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1	-	-	V
Input Capacitance	C_I	-	-	-	10	pF
Three-State Output Capacitance	C_O	-	-	-	15	pF

NOTES:

6. 5V: Minimum is at 5.25V for 0°C to 70°C, Maximum is at 4.75V for 0°C to 70°C, Typical is at 5V.

7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = V_{CC} I_{CC} + $\Sigma(V_{CC}^2 f_i C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$ where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_i = input frequency

Test Circuits and Waveforms



NOTE:

8. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

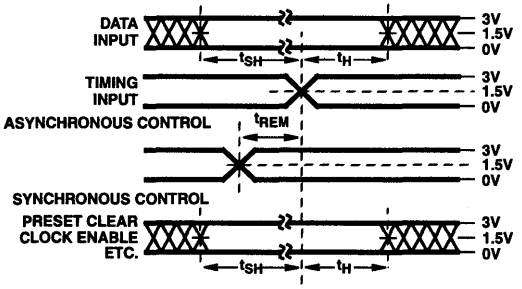


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

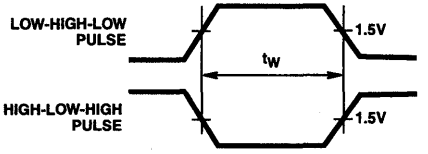


FIGURE 3. PULSE WIDTH

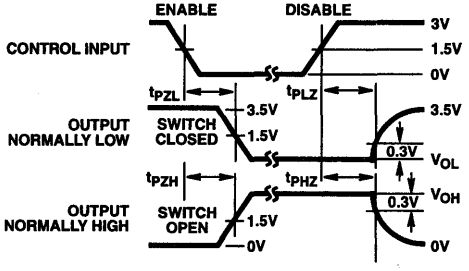


FIGURE 4. ENABLE AND DISABLE TIMING

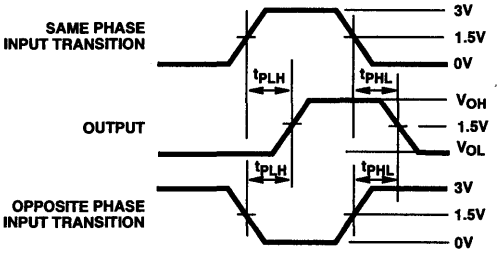
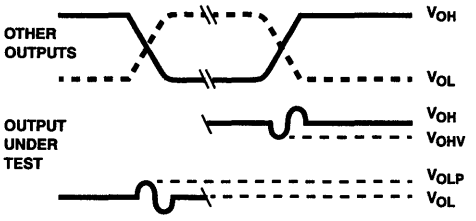


FIGURE 5. PROPAGATION DELAY



NOTES:

9. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
10. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
11. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

HARRIS SEMICONDUCTOR

CD74FCT863A

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

BiCMOS FCT Interface Logic, 9-Bit Bus Transceiver, Three-State

Features

- Buffered Inputs
- Typical Propagation Delay: 6.0ns at V_{CC} = 5V, T_A = 25°C, C_L = 50pF
- CD74FCT863A
  - Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S
- 48mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT863AM	0 to 70	24 Ld SOIC	M24.3

NOTE: When ordering the suffix M package, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

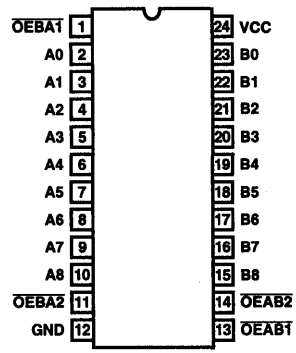
Description

The CD74FCT863A nine bit bus transceiver uses a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 milliamperes.

This device provides extra data width for wider address/data paths or buses carrying parity. The dual Output Enable provision gives this device the capability to store data by simultaneously enabling $\overline{OEAB}$ and $\overline{OEBA}$. Each output reinforces its input under these conditions and, when all other data sources to the bus line are at high impedance, both sets of bus lines will remain in their last states.

Pinout

CD74FCT863A
(SOIC)
TOP VIEW

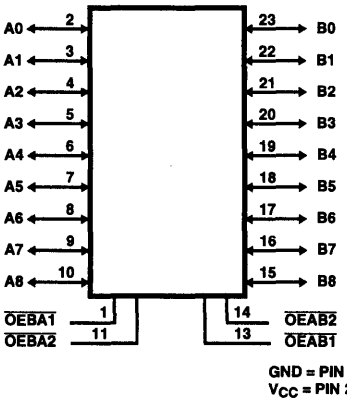


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

FAST™ is a trademark of Fairchild Semiconductor.

File Number **2391.2**

Functional Diagram



TRUTH TABLE (Note 1)

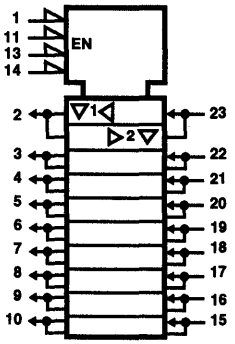
INPUTS				OUTPUTS		
$\overline{OEBA}$	$\overline{OEAB}$	B	A	B	A	FUNCTION
L	H	L	N/A	N/A	L	B Data to A Bus
L	H	H	N/A	N/A	H	B Data to A Bus
H	L	N/A	L	L	N/A	A Data to B Bus
H	L	N/A	H	H	N/A	A Data to B Bus
H	H	X	X	Z	Z	High Z
L	L	-	-	-	-	A Data to B Bus, B Data to A Bus

NOTE:

1. H= HIGH Voltage Level
   L = LOW Voltage Level
   N/A = Not Applicable
   X = Immaterial
   Z = HIGH Impedance

IEC Logic Symbol

CD74FCT863A



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) ..... -0.5V to 6V
DC Diode Current, I_{IK} (For V_I < -0.5V) ..... -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) ..... -50mA
DC Output Sink Current per Output Pin, IO 70mA
DC Output Source Current per Output Pin, IO ..... -30mA
DC V_{CC} Current (I_{CC}) 234mA
DC Ground Current (I_{GND}) 455mA

Thermal Information

Thermal Resistance (Typical, Note 2) θ_{JA} (°C/W)
SOIC Package 75
Maximum Junction Temperature ..... 150°C
Maximum Storage Temperature Range ..... -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) ..... 300°C
(Lead Tips Only)

Operating Conditions

Operating Temperature Range, T_A ..... 0°C to 70°C
Supply Voltage Range, V_{CC} ..... 4.75V to 5.25V
DC Input Voltage, V_I ..... 0 to V_{CC}
DC Output Voltage, V_O ..... 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv ..... 0 to 10ns/V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Commercial Temperature Range 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS			AMBIENT TEMPERATURE (T_A)				UNITS
					25°C		0°C TO 70°C		
		V_I (V)	I_O (mA)	V_{CC} (V)	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.75 to 5.25	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.75 to 5.25	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	48	Min	-	0.55	-	0.55	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	µA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	V
Short Circuit Output Current (Note 3)	I_{OS}	V_O = 0 V_{CC} or GND		Max	-75	-	-75	-	mA
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA Max. at 70°C.

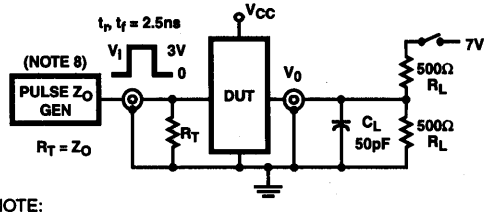
Switching Specifications Over Operating Range FCT Series t_r, t_f = 2.5ns, C_L = 50pF, R_L (Figure 1)

PARAMETER	SYMBOL	V_{CC} (V)	25°C	0°C TO 70°C		UNITS
			TYP	MIN	MAX	
Propagation Delays Data to Outputs	t_{PLH}, t_{PHL}	5 (Note 6)	6	1.5	8	ns
Output Enable to Output	t_{PZL}, t_{PZH}	5	9	1.5	12	ns
Output Disable to Output	t_{PLZ}, t_{PHZ}	5	7.5	1.5	10	ns
Power Dissipation Capacitance	C_{PD} (Note 7)	-	-	-	-	pF
Minimum (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV}	5	0.5	-	-	V
Maximum (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP}	5	1	-	-	V
Input Capacitance	C_I	-	-	-	10	pF
Three-State Output Capacitance	C_O	-	-	-	15	pF

NOTES:

6. 5V: Minimum is at 5.25V for 0°C to 70°C, Maximum is at 4.75V for 0°C to 70°C, Typical is at 5V.
7. C_{PD}, measured per flip-flop, is used to determine the dynamic power consumption.
   P_D (per package) = $V_{CC} I_{CC} + \Sigma(V_{CC}^2 f_I C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$ where:
   V_{CC} = supply voltage
   ΔI_{CC} = flow through current x unit load
   C_L = output load capacitance
   D = duty cycle of input high
   f_O = output frequency
   f_I = input frequency

Test Circuits and Waveforms



NOTE:

8. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

V_{IN} = 0V to 3V.

Input: $t_r = t_f$ = 2.5ns (10% to 90%), unless otherwise specified

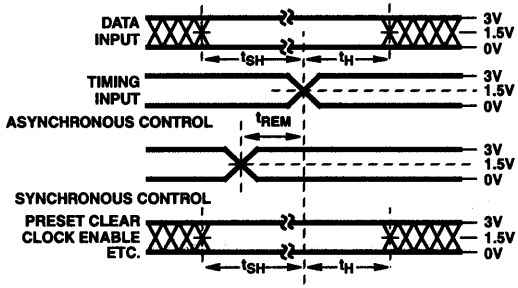


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

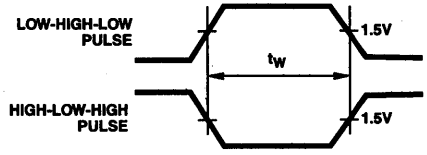


FIGURE 3. PULSE WIDTH

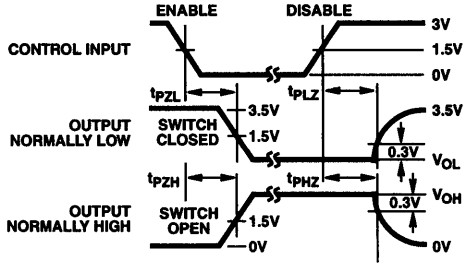


FIGURE 4. ENABLE AND DISABLE TIMING

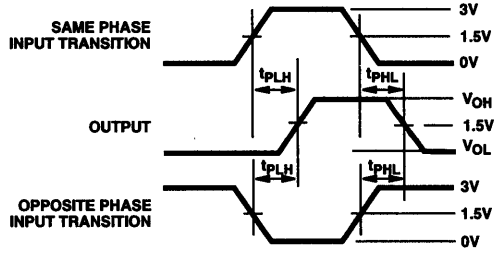
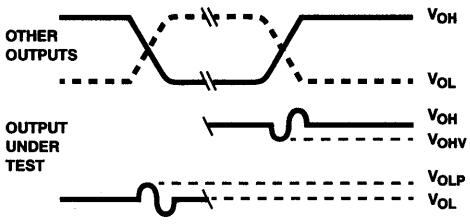


FIGURE 5. PROPAGATION DELAY



NOTES:

9. V_{OLP} is measured with respect to a ground reference near the output under test. V_{OHV} is measured with respect to V_{OH}.
10. Input pulses have the following characteristics: P_{RR} ≤ 1MHz, t_r = 2.5ns, t_f = 2.5ns, skew 1ns.
11. R.F. fixture with 700MHz design rules required. IC should be soldered into test board and bypassed with 0.1μF capacitor. Scope and probes require 700MHz bandwidth.

FIGURE 6. SIMULTANEOUS SWITCHING TRANSIENT WAVEFORMS

CMOS LOGIC 9

APPLICATION NOTES AND TECH BRIEFS

		PAGE
Application Notes		
AN9645	8-Bit FCT Characterization and Qualification Data	9-3
AN9646	Ground Bounce in 8-Bit High Speed Logic	9-8
AN9662	FCT Logic for Hot Plug Applications	9-11
Tech Briefs		
TB341	Low Power Technology (LPT) 3.3V Logic	9-14
TB342	Quiet FCT Logic Advantages	9-15
TB343	FCT vs ABT Logic Comparison - Double Density Types	9-18
TB344	CD74FCT162344T For Heavy Load/High Fan Out Applications	9-21
TB347	Tape and Reel Specification for Integrated Circuits	9-23

APPNOTE

No. AN9645 December 1996

Harris Logic

8-Bit FCT Characterization and Qualification Data

Introduciton

Harris Semiconductor's bus interface logic products are fabricated in an advanced CMOS technology to achieve industry leading speed grades and high reliability. It should be noted that this data is for octal FCT only. Double density 16-bit FCT data can be obtained by contacting the factory.

Process Features

- **0.8 micron CMOS Process**
- **NMOS and PMOS LDD Devices For Reliability and Low Leakage**
- **High Speed, High Drive Transistors Which Can Work Down to 0.55μm Effective Channel Length**
- **Low Capacitance and Low Resistance Interconnect For High Performance**
- **Fully Planarized Metal Technology**
- **Barrier Metal Technology**

Process Outline

- **N Well**
- **Field/Ilsand**
- **Field Implant**
- **N-Channel Punchthrough Suppression**
- **Poly Gate**
- **LDD Mask**
- **N+ Source/Drain**
- **P+ Source/Drain**
- **Contact**
- **Metal 1**
- **Metal Via**
- **Metal 2**
- **Passivation**

CD74FCT245T Product Features

- Very High Speed (Up to D Speed)
- Output Delay Has Low Sensitivity to Temperature and Power Supply Voltage
- Lower Ground Bounce Compared to Other FCT's (Except Pericom) at the Same Speed

Electrical Specifications

PARAMETER	TEST CONDITIONS (SEE CD74FCT245T D/S)	D SPEED SPEC	DATA			UNITS
			25°C	90°C	125°C	
DC ELECTRICAL SPECIFICATIONS, (NOTE 1)						
V_{OH}	I_{OH} = -8mA	2.4	3.4	-	-	V
	I_{OH} = -15mA	2.0	3.1	-	-	V
V_{OL}	I_{OL} = 48mA	-	0.22	-	-	V
	I_{OL} = 64mA	0.55	0.28	-	-	V
V_{IH}		2.0	1.55	-	-	V
V_{IL}		0.8	1.15	-	-	V
I_{IH}	V_{IN} = 2.7V	1	0	-	-	µA
I_{IL}	V_{IN} = 0.5V	-1	0	-	-	µA
V_{IK}	I_{IN} = 18mA	-1.2	-0.7	-	-	V
I_{OS}	V_{OUT} = GND	-60	-220	-	-	mA
POWER SUPPLY SPECIFICATIONS, (NOTE 1)						
I_{CC}	V_{IN} = GND/V_{CC}	1.5	0	-	-	µA
ΔI_{CC}	V_{IN} = 3.4V	2.5	0.948	-	-	mA
I_{CCD}	One Bit Toggle	0.25	0.197	-	-	mA/ MHz
SWITCHING SPECIFICATIONS, V_{CC} = 4.5V (NOTE 2)						
t_{PLH}	50pF, 500Ω	3.8	3.44	3.68	3.80	ns
t_{PHL}	50pF, 500Ω	3.8	3.28	3.56	3.72	ns
t_{PZH}	$\overline{OE}$ to A/B	5.0	3.40	3.80	3.86	ns
t_{PZL}	$\overline{OE}$ to A/B	5.0	3.88	4.16	4.32	ns
t_{PHZ}	$\overline{OE}$ to A/B	4.3	3.66	4.08	4.12	ns
t_{PLZ}	$\overline{OE}$ to A/B	4.3	2.54	2.74	2.90	ns

NOTES:

1. All DC Electrical Parameter and Power Supply Performance is similar for types:
   CD74FCT240T CD74FCT241T CD74FCT244T CD74FCT245T CD74FCT540T
   CD74FCT541T CD74FCT640T CD74FCT645T CD74FCT273T CD74FCT373T
   CD74FCT533T CD74FCT573T CD74FCT374T CD74FCT534T CD74FCT574T
   CD74FCT377T CD74FCT543T CD74FCT544T CD74FCT623T CD74FCT646T
   CD74FCT648T CD74FCT651T CD74FCT652T
   Figures 6 and 7 apply to preceding types.
   For the following types, DC Performance and Power Supply Performance is similar except for the V_{OL} specifications.
   These are the I_{OL} = 48mA specified types: CD74FCT399T, CD74FCT521T, and all CD74FCT8XXT.
2. Switching specification parameter performance is shown in Figures 1, 2, 3, 4, 5, 8, and 9 are similar for all types listed in note 1.

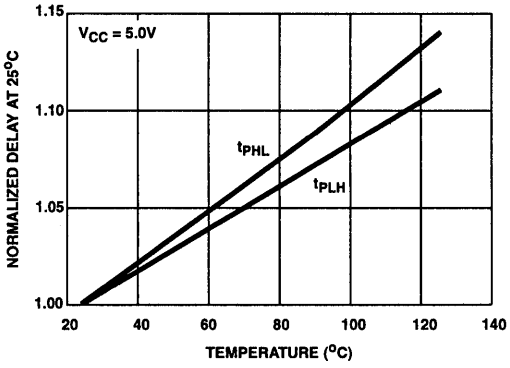


FIGURE 1. OUTPUT DELAY vs TEMPERATURE (t_{PLH}/t_{PHL})

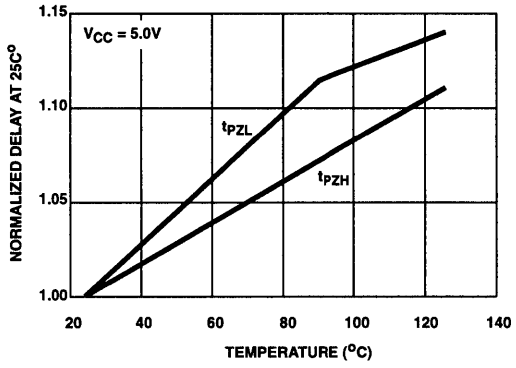


FIGURE 2. OUTPUT DELAY vs TEMPERATURE (t_{PZH}/t_{PZL})

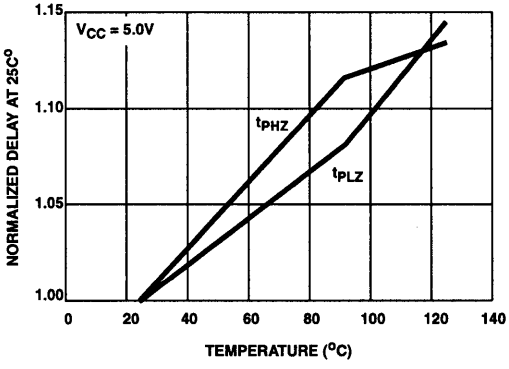


FIGURE 3. THREE-STATE DELAY vs TEMPERATURE (t_{PHZ}/t_{PLZ})

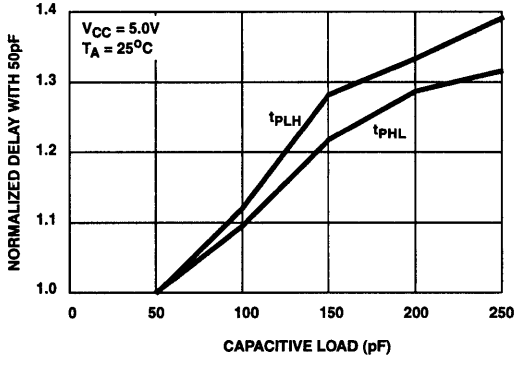


FIGURE 4. OUTPUT DELAY vs OUTPUT CAPACITANCE (t_{PLH}/t_{PHL})

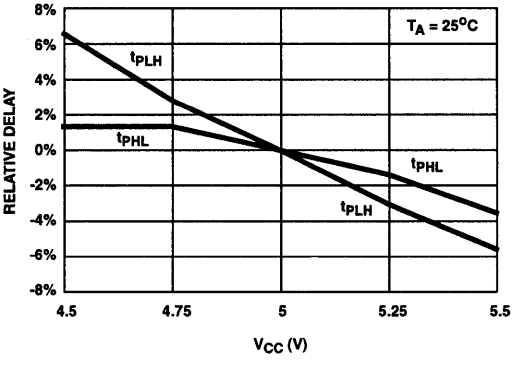


FIGURE 5. OUTPUT DELAY vs POWER SUPPLY VOLTAGE (t_{PLH}/t_{PHL})

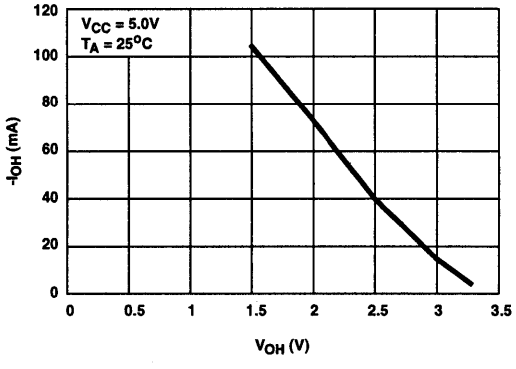


FIGURE 6. I_{OH} vs V_{OH}

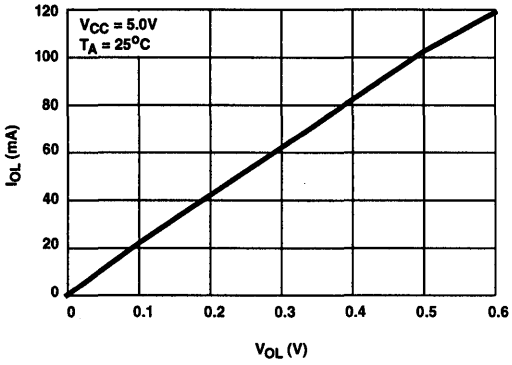


FIGURE 7. I_{OL} vs V_{OL}

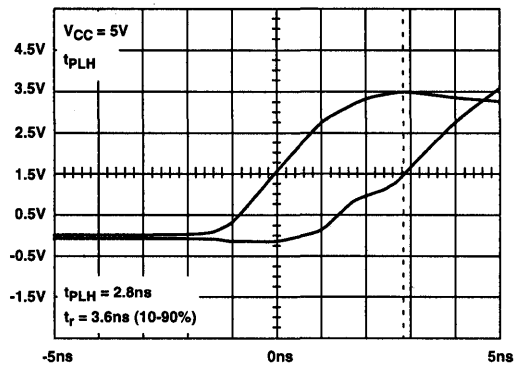


FIGURE 8. OUTPUT RISE TIME CHARACTERISTICS (25°C)

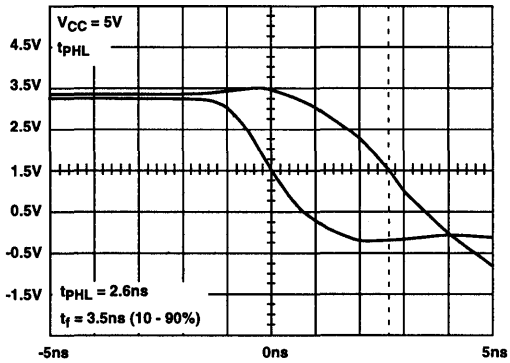


FIGURE 9. OUTPUT FALL TIME CHARACTERISTICS (25°C)

High Performance Bus Interface Logic

Low Skew

- Actual Device Performance is Derated With Skew Due to Imbalanced Switching
  - Pull Up/Pull Down
  - Pin-to-Pin
- Skew Is Minimized With:
  - Careful Design of Pull Up/Pull Down Ratio
  - Large Output Drive Capability
  - Careful Matching of Propagation Delay Between Different Paths
- Superior Performance in Skew Reduction Achieved
  - Pull Up/Pull Down Skew Less Than 300ps
  - Pin-to-Pin Skew Less Than 300ps

PULL UP/PULL DOWN SKEW (NOTE 3)

DEVICE	t_{PHL}	t_{PLH}	DELTA	UNITS
CD74FCT244	2.84	2.88	0.04	ns
CD74FCT245	2.76	2.86	0.10	ns
CD74FCT373	3.16	3.04	0.12	ns
CD74FCT374	4.0	4.0	0.0	ns
CD74FCT377	4.0	4.16	0.16	ns
CD74FCT273	4.0	3.96	0.04	ns
CD74FCT573	2.7	2.74	0.04	ns
CD74FCT574	3.34	3.08	0.26	ns
CD74FCT534	2.9	2.92	0.02	ns
CD74FCT623	3.3	3.38	0.08	ns

NOTE:

3. Measurement done with 1GHz HP Sampling Scope, at 25°C, V_{CC} = 5.0V.

PIN TO PIN SKEW (NOTE 4)

PIN	t_{PHL}	t_{PLH}	DELTA	UNITS	PIN	t_{PHL}	t_{PLH}	DELTA	UNITS
A_0	2.6	2.80	0.2	ns	B_0	2.76	2.82	0.06	ns
A_1	2.58	2.86	0.28	ns	B_1	2.66	2.76	0.10	ns
A_2	2.59	2.82	0.23	ns	B_2	2.70	2.86	0.16	ns
A_3	2.6	2.82	0.22	ns	B_3	2.68	2.85	0.17	ns
A_4	2.55	2.77	0.22	ns	B_4	2.65	2.82	0.17	ns
A_5	2.63	2.82	0.19	ns	B_5	2.61	2.71	0.10	ns
A_6	2.63	2.83	0.20	ns	B_6	2.61	2.76	0.15	ns
A_7	2.69	2.85	0.16	ns	B_7	2.63	2.72	0.09	ns
Range	0.14	0.09	-	ns	Range	0.15	0.15	-	ns

NOTE:

4. Measurement done with HP-54100 scope at 25°C, 5.0V on FCT-DTP 245.

APPNOTE

No. AN9646 December 1996

Harris Logic

Ground Bounce in 8-Bit High Speed Logic

Today's demand for higher speed systems is for increased performance, but with strong consideration for power usage. Traditionally, high-drive bus interface logic have been implemented in Bipolar technology, but recent years have witnessed strong demand for a CMOS counterpart series called FCT. In fact, FCT has evolved to deliver far greater performance (shorter propagation delays) than is available in Bipolar technology, thus becoming the only available avenue for very high-speed system designers. Maintaining the same high output drive capabilities as the Bipolar products (64mA sink), FCT circuits from Harris Semiconductor are now available with propagation delay down to 3.6ns (maximum) for some functions. However, speed improvements and power reduction has not come without some penalties in the form of a noise phenomena called "Ground Bounce."

Ground Bounce is the simultaneous switching noise of outputs during the logic HIGH to LOW transition and the resultant potential difference between the chip ground and the external ground plane. When several outputs switch simultaneously, the total build up of current in the common ground or V_{CC} lead inductance can be substantial. The noise becomes more pronounced as the output edge rate and the drive capability increase or as more current is switched through the ground lead.

Harris Semiconductor's FCT products are designed to have low ground bounce. The FCT family is TTL compatible and the output swing is limited to 3.4V TTL output swings instead of 5V. This reduces the discharge current through the ground lead and reduces maximum noise by 30% to 40%. Specially optimized control circuits are designed to gradually turn on the output driver to reduce ground bounce while achieving high speed. Optimized layout of the power and ground lines in the chip further reduces ground bounce.

Ground bounce and speed characterization were done on a special bench setup as shown in Figure 1. Ground bounce measurement was done with seven bits simultaneously driven from logic HIGH to logic LOW and the remaining bit tied to ground. The noise voltage waveform generated at the undriven bit (quiet bit) is measured and represents the worst case ground bounce noise. This is the standard setup and measurement in characterizing ground bounce. On system boards, the noise characteristics are usually much lower with proper board design.

A CD74FCT244T device in a plastic DIP package from Harris Semiconductor and two other suppliers were characterized with the setup as shown in Figure 1. Figures 2 and 3 compare the waveforms of the output voltage transitions and

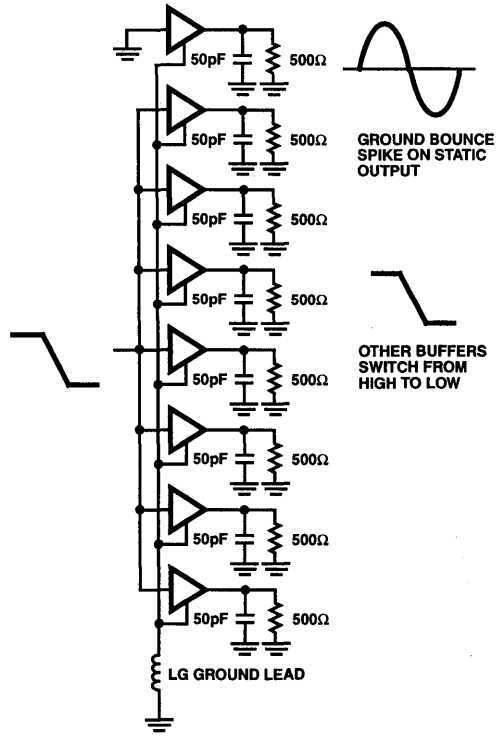


FIGURE 1. TYPICAL GROUND BOUNCE EVALUATION SETUP

the corresponding ground bounce as observed at the undriven LOW output. Table 1 summarizes the results. The results show that Harris Semiconductor's FCT device has significantly lower ground bounce compared to the other suppliers. Other Harris FCT octal types with similar ground bounce performances include:

CD74FCT240T	CD74FCT241T	CD74FCT245T
CD74FCT273T	CD74FCT373T	CD74FCT374T
CD74FCT377T	CD74FCT533T	CD74FCT534T
CD74FCT540T	CD74FCT541T	CD74FCT543T
CD74FCT544T	CD74FCT573T	CD74FCT574T
CD74FCT623T	CD74FCT640T	CD74FCT645T
CD74FCT646T	CD74FCT648T	CD74FCT651T
CD74FCT652T	CD74FCT825T	

Key to High Speed Low Noise Design

Ground bounce can only be minimized or circumvented, but rarely eliminated since the parasitic inductance cannot be totally removed from the package. Figure 4 shows a simplified circuit model to help explore several key factors which are critical for good ground bounce control design.

During the output HIGH to LOW transition, the sum of output load current and all switching current through the device flows through the ground lead and generates noise voltage. Several factors affect the amplitude of this voltage:

- Number of outputs switching simultaneously. The more outputs switching simultaneously, the more ground bounce.
- Magnitude of lead inductance. Higher lead inductance results in greater ground bounce. Thus, a package with less parasitic ground lead inductance would result in better noise performance.
- Output voltage swing. Higher output voltage swing would result in higher ground bounce. Thus, a CMOS compatible output with 5V V_{OH} would inherently result in higher noise than a TTL compatible output with lower V_{OH} voltage.

Output edge rate. The output edge rate determines how fast the current discharges through the ground lead inductor. Since the transient voltage across an inductor increases with the rate of change of the current, the faster the rate, the higher the noise. Thus it is very critical to control this output edge rate to get low noise performance.

Harris Semiconductor addresses these issues directly at the outset of the design. First, we design our FCT products to be TTL compatible. This limits the output swing to 3.4V instead of 5V. This reduces the maximum noise as the maximum output swing is lowered. To control the output edge rate without compromising speed, a proprietary control circuit is designed to gradually turn on the output driver to optimize the speed performance and ground bounce characteristics. Also, alternative package choices complement the high-speed low-noise design. Plastic DIP packages have the highest lead inductance and hence, the worst ground bounce characteristics. Packages like SOIC and QSOP have much lower lead inductance and hence, much lower ground bounce.

TABLE 1. GROUND BOUNCE COMPARISON AT ROOM TEMPERATURE: HARRIS vs COMPETITORS 1 AND 2

UNIT	SPEED (ns)		GROUND BOUNCE (V)	
	t_{PHL}	t_{PLH}	POSITIVE	NEGATIVE
Harris, D Speed	2.84	2.88	1.52	1.28
Competitor 1, D Speed	2.92	3.08	2.04	1.88
Harris, C Speed	3.2	3.4	1.32	1.00
Competitor 2, C Speed	3.24	3.84	1.52	1.34

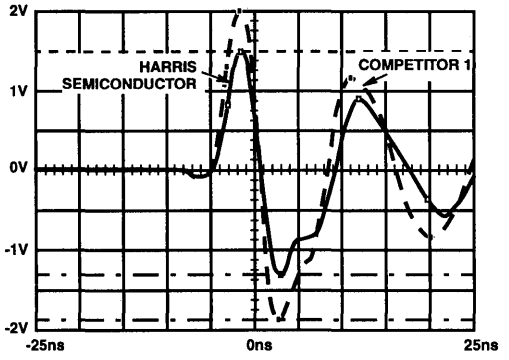


FIGURE 2. GROUND BOUNCE WAVEFORMS: HARRIS SEMICONDUCTOR vs COMPETITOR 1

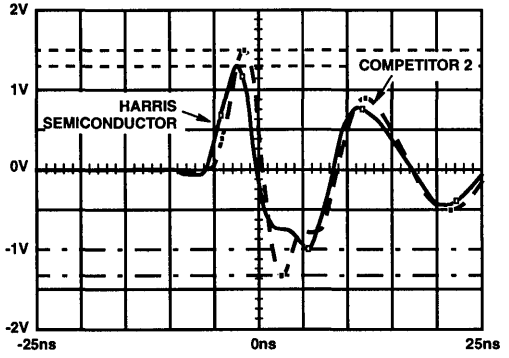


FIGURE 3. GROUND BOUNCE WAVEFORMS: HARRIS SEMICONDUCTOR vs COMPETITOR 2

Table 2 shows a comparison of package inductance and estimated ground bounce. It is evident that the surface mount packages (SOIC, QSOP) offer system designers the advantages of reduced board space, higher speed performance and lower ground bounce.

TABLE 2. GROUND BOUNCE PACKAGE COMPARISON

PACKAGE	GROUND LEAD INDUCTANCE	RELATIVE GROUND BOUNCE
PDIP	13.7nH	100%
SOIC	8.5nH	80%
QSOP	3.6nH	50%

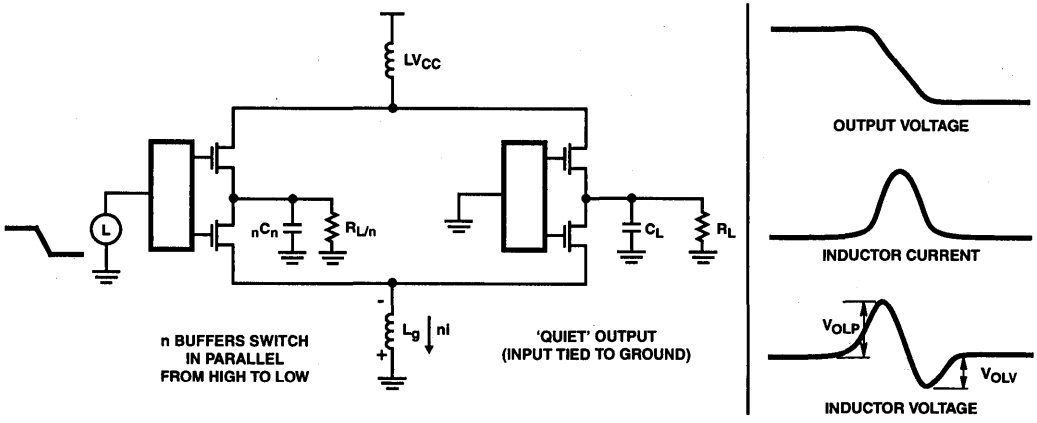


FIGURE 4. SIMPLIFIED CIRCUIT MODEL

Harris Semiconductor

APPNOTE

No. AN9662 December 1996

Harris Logic

FCT Logic for Hot Plug Applications

Introduction

"Hot Plug" and "Live Insertion" are both terms that apply to the technique of adding or removing modular components from a system while power is applied and the system is fully or partially operational.

These systems might typically be a complex computer system used for airline ticket reservations or for a large department store, where even short periods of down-time can result in thousands or even millions of dollars of lost business and good will. Another typical "Hot Plug" system might easily be found in a hospital where, although not used directly for life-support, a badly timed (or lengthy) computer failure can seriously delay the movement of critical information necessary for both health maintenance as well as for billing and insurance management.

One growing application that needs hot plug capability is portable computers, where deck insertion and removal from a docking station and the insertion and removal of PCMCIA cards often occur while power is applied.

When Harris Semiconductor's growing family of octal and double density FCT and fast TTL compatible CMOS logic are used in conjunction with good design practices can allow dynamic removal and insertion of subsystem modules. While the power is on and the system is operating; system power can be either 5V or 3.3V depending on device type.

The Working Environment

Typically, hot plug modules or cards are connected to a system through a live backplane. In some instances, a disabled or powered-down section of an existing board may be activated and subsequently enabled onto an internal system bus. Both of these instances require similar design considerations.

When designing a system with hot plug capabilities two main issues come to light:

- Uninterrupted System Operation
- Protection of All Devices During the Insertion or Removal Operation

The management of system operation begins with the impact of the module that is being added or removed. Adding new functionality to an existing system (expanding communications, adding additional processors or memory, etc.) usually depends on the ability of the system to integrate the new devices on-the-fly, assuming that the process of adding the new module is clean. In this application, (as well as during re-insertion of a repaired or replaced module) the key issue is how to ensure that the addition of the module does not create any undesirable electrical conditions that may upset the operation of the operating bus. Transient isolation and suppression during the insertion process, as well as during the power-up of the new module is critical.

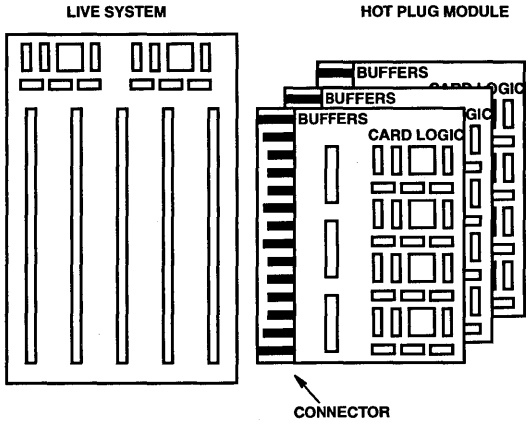


FIGURE 1. A BUS-BASED SYSTEM WITH HOT PLUG MODULES

The second issue concerns protection of both the new circuit components as they power up as well as existing live components. In this situation, the design of the plug-in module, the target host and the connectors plays a very important role. Although power sequencing has traditionally been the main concern, power-on reset, power-on preset to known conditions, controlled output enables, controlled PCB trace length, device input and output structure design, per pin and total capacitive load, host power supply characteristics, module power consumption and bypass design, low power detection and valid power detection as well as ESD protection (and more) all play a vital role in the overall design.

The following paragraphs will discuss how Harris FCT devices can be successfully used as an interface between a host system and a hot plug module as well as some important related design considerations.

Basic Design Considerations in Hot-Plug Systems

The Connector

When adding a module into a running system, the connecting mechanism must be designed to provide quick and solid electrical connection for the ground, power and signal lines. It is mandatory that the ground lines be connected as early as possible followed by the signal lines. It is a well understood phenomena that connecting signal lines or V_{CC} lines to a circuit with an unstable ground can result in device damage as well as unpredictable system level current surges. These current surges may adversely affect system operation. The ground and then the signal lines must be solidly connected before applying V_{CC}. Staggered connector pins and spring loaded insertion devices are two ways of providing predictable connections.

When using staggered card edge connector pins, it is important to keep in mind that even with good card guides, it is possible to insert one side of the connector before the other side. This can defeat a card edge connector sequencing that presumes that the insertion is going to be flat and uniform. To minimize the effects of this situation, use extended ground pins on both edges, slightly shorter pins with the output enables and other control signals, and the shortest pins for the power in the middle of the connector.

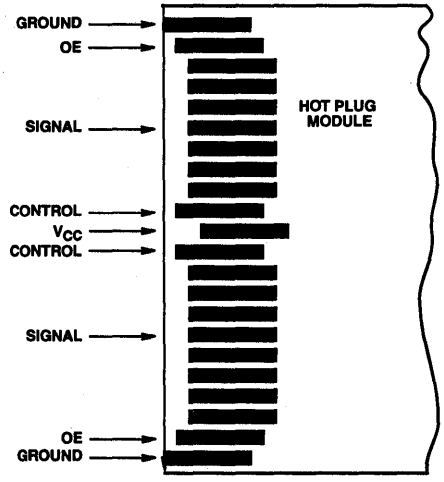


FIGURE 2. STAGGERED FINGER ARRANGEMENT FOR HOT PLUG APPLICATIONS

The Capacitance

When a hot plug card is connected to a bus structure, an additional load is applied to the system signal lines. One major effect of this additional load on the target bus is caused by the instantaneous charge redistribution between the system's bus capacitance and the capacitance of the added load. In general, a card used for a hot plug application should have a minimum number of loads connected to the bus signal lines, preferably only one device pin per signal. In addition, the device placement and trace layout of such a board must be designed to minimize trace length between the card edge or the card's connector to the board's components. This will help to minimize the capacitive load connected to the bus. Additional capacitive loads of 5pF up to 20pF will typically have no discernible effect on active signal levels of a bus driven by FCT devices. In the case of an internal bus with weak drivers, close attention will need to be paid to the drive characteristics of the devices used and their susceptibility to the addition of capacitive loads while operational. In some cases, experimentation may be required.

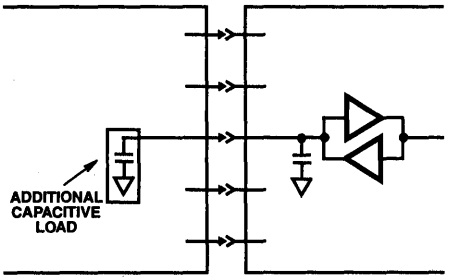


FIGURE 3. ADDING CAPACITIVE LOAD TO THE SYSTEM

The Enables

The logic on the hot plug card must be designed to disable all output signals going off board while power up is taking place. Once the card has stable power, the card logic or the host system may then enable the I/Os onto the system bus. Often, pull-up (or pull-down) resistors are added to these lines to force them to known states during uncontrolled conditions. This solution has some problems associated with it which are addressed later in this paper.

FCT Input and Output Structures

Signal pins connected to the host bus at the card edge may be inputs, outputs, three-state I/Os. The Input structure of a typical FCT device will be reviewed first.

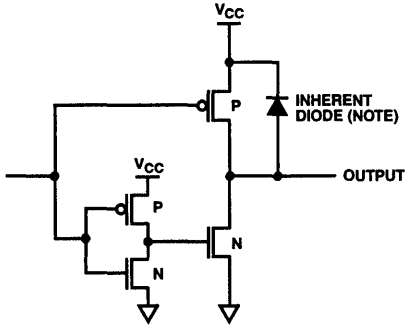
The Input Structures

All FCT logic input (and output) structures have industry standard (2000V) ESD protection circuits. All devices have input clamp diodes to ground, and most have hysteresis circuitry. Unlike many TTL devices, Harris FCT does not have a clamp diode to V_{CC}.

This lack of a V_{CC} clamp diode is very important for hot plug applications. A V_{CC} clamp diode will limit the input voltage to the V_{CC} level existing on the device's V_{CC} pin. If the V_{CC} pin is at ground, then the V_{CC} clamp diode shunts the input pin to ground. This is a real problem for an active system! With Harris's FCT logic, the inputs (and outputs and control lines as well) can tolerate levels up to 7V regardless of the V_{CC} level.

The Output Structures: Traditional CMOS Logic

Some CMOS logic families have an output structure consisting of an N-Channel between the output ground and a P-Channel transistor from V_{CC} to the output pin. The P-Channel transistor creates an inherent diode from the output pin to V_{CC}. As a result, when the output is not driven by the device (disabled) or when the V_{CC} pin at any level below the level seen on the pin, the signal is effectively "clamped" to V_{CC}. Again, this means that in hot plug operation such devices will temporarily short some system signals to ground.



NOTE: Not present in Harris 5V FCT family.

FIGURE 4. OUTPUT STAGE WITH N-P STRUCTURE USED IN LPT LOGIC FAMILY

The Output Structures: 5V FCT TTL Compatible CMOS Logic

Harris's FCT output stage is made up of only N-Channel transistors between the output and V_{CC} and ground (Figure 5). This structure isolates the output pin when disabled so that the host system can drive normal logic swings regardless of the V_{CC} supply to the output stage. This allows designers to connect the I/Os of an unpowered FCT device to an active bus without worrying about the integrity of the FCT devices or impacting the active logic state of the bus. Harris FCT Logic typically has about 5pF or 6pF of capacitance per pin, so the insertion is accomplished with a minimum of trauma.

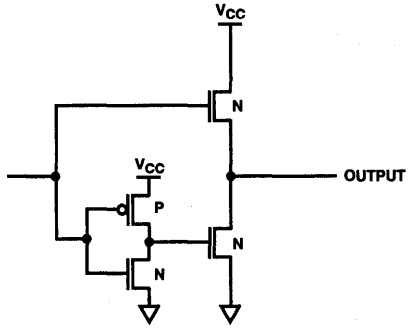


FIGURE 5. N-N OUTPUT STAGE STRUCTURE

Hot Plug Implementation Scenarios

Figure 6 depicts a simple circuit that can be used to disable the hot plug card I/Os during power-up as well as allow the hot plug card's logic to enable/disable the buffers during normal operation. The use of a pull-up resistor guarantees that the /OE line will follow V_{CC}, thus keeping the FCT I/Os disabled. Once the system has power, a logic low on the /OE signal will enable the I/Os onto the bus. The enable signal can also be sourced from the host system, allowing the module to be enabled when the system desires.

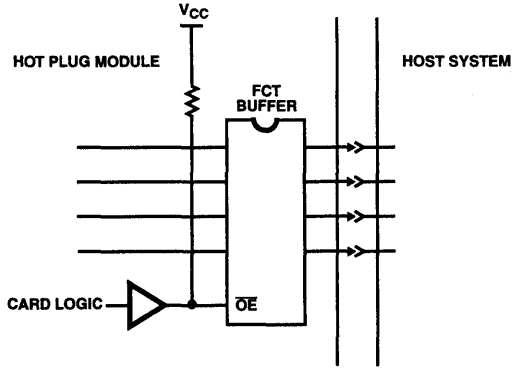


FIGURE 6. SIMPLE EXAMPLE OF OUTPUT ENABLE CONTROL FOR HOT-PLUG APPLICATIONS

Special care must be exercised in choosing the value of the pull-up resistor. A resistor with a value of a few hundred ohms will provide a solid disable function even if V_{CC} ramps up in less than 100ns. The disadvantage of a small resistor value is the power dissipation through it when the /OE is driven low.

The main item of concern with high resistor value is that the /OE will "lag" in time behind V_{CC}, especially if the V_{CC} ramps up quickly. In this case, the outputs may be partially or fully enabled accidentally when power is ramping up. This is obviously unacceptable for a hot plug system.

Related Techbrief: TB343, *FCT vs ABT Logic Comparison*

Harris Semiconductor

TechBrief

No. TB341 December 1996

Harris Logic

Low Power Technology (LPT) 3.3V Logic

Introduction

The Low Power Technology (LPT) Logic product line is comprised of both 8-bit octals and 16-bit double density products. The LPT series is an improved version of the LCX logic family. LPT offers a balanced drive ±24mA output. The output impedance is approximately 20Ω for both pullup and pulldown. Basically the edges are slow (3ns to 4ns) which result in minimal overshoot and undershoot. In other words, the LPT family is quiet...low noise, exhibiting low ground bounce. The 16 bit products also feature <500ns output skew. This brief will describe bus contention, live insertion, I/O tolerance and a comparison to LCX , ALVC and LVT.

LPT vs LVT

LVT is a BiCMOS logic family that has a bipolar output stage which is generally considered more robust. Even though LPT does not have bipolar technology it does have a very robust output stage as shown in Figure 1 during bus contention.

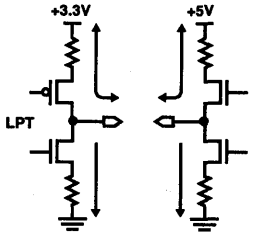


FIGURE 1. LPT BUS CONTENTION

When LPT drives the bus, a specification called Output High Current (I_{ODH}) allows the instantaneous or transition current to go as high as 110mA. Also, when LPT goes low the sink current, which is called I_{ODL} or Output Low Current, can sink up to 200mA of transition current. I_{ODH} and I_{ODL} are not generally specified in other type logic. Outputs can withstand 1s duration when grounded or at +5V. A worst case condition exists when both devices on the bus try to drive at the same time. This is referred to as bus contention. If LPT is connected to a 5V bus (no problem because LPT is I/O tolerant), as in Figure 1, the 5V logic device will try and push current into the active high LPT device. Generally this current is about 50mA and is not a problem.

Live Insertion

When inserting a logic device in a live circuit the most important rule is power sequencing. For instance ground, disable, and power should be connected in this sequence through a staggered edge PCB. Another hint is to make sure the disable RC time is about 10 times less than the power RC time, as shown in Figure 2. This insures that the part will be disabled and won't disrupt bus data during insertion. Actually all logic families should follow these hints.

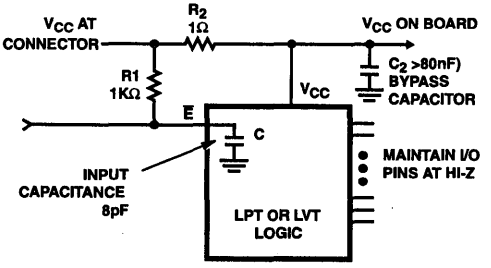


FIGURE 2. LIVE INSERTION

What Does I/O Tolerance Mean?

A special advantage was designed into LPT products: 5V I/O tolerance. This means that all input and output pins can be connected to 5V logic or bus even when power to the LPT device is 3.3V. No damage to the LPT device will occur. Contact the Harris application group if there is an interest in adapting LPT to 5V or 3V V_{CC}.

Competition

Table 1 exhibits the advantages of LPT. It should be noted that all technologies shown are CMOS except for LVT which is BiCMOS.

TABLE 1. COMPETITIVE COMPARISONS

COMPARISON	LPT	LCX	LVT	ALVC
I/O Tolerance	X	X	X	
Propagation Delay	4ns	4.5ns	2.5ns	3ns
Low Noise	X	X	X	
Robust Outputs	X	X	X	
Low Power	X	X		X
2.5V Low Voltage Operation	X (Note 1)			

NOTE:

1. Contact Factory.

Harris Semiconductor

TechBrief

No. TB342 December 1996

Harris Logic

Quiet FCT Logic Advantages

Introduction

With logic applications requiring faster clock speeds, which result in faster edge rates, the need for fast glue logic has become apparent. The problem is that the general result of a fast edge is excessive overshoot and undershoot that leads to ringing. Harris's new Quiet Series devices are described in this brief. A quiet part is a part that has minimal overshoot, undershoot, ringback and ground bounce which mean low noise. The CD74FCT162QXXX series is a family of Quiet Double Density (16-bit wide) logic devices. This family not only offers these almost noiseless parts, but also includes a bus hold feature. The following brief will describe noise, bus hold, operation, typical applications and a comparison to competition.

What is noise?

The Quiet Series was designed for light capacitance load applications of less than 50pF. For instance, clock buffering and low bank count memory are ideal uses for this product line. Figure 1 shows several sources of noise that should be averted to insure proper operation.

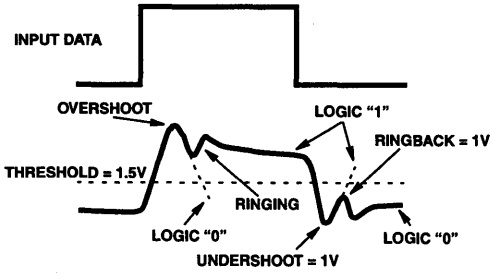


FIGURE 1. TYPICAL NOISE WAVEFORM

Most noise problems are a direct result of improper drive or termination. The Quiet series has series resistance (shown in Figure 3) that when added to the active pullup/pulldown is about 40Ω. Fast edges cause overshoot and undershoot which are virtually eliminated by this technique. Figure 2 exhibits another form of noise called ground bounce. By switching all bits simultaneously (B1 - B15) and checking one output (B16), whose input is grounded, ground bounce is viewed and recorded (Figure 2). Current, which is injected into the ground plane, is directly proportional to inductance L and d_I/d_T. Ground bounce is a form of noise and directly relates to undershoot and ringback. Trace length is critical because trace capacitance (and inductance) change with trace length.

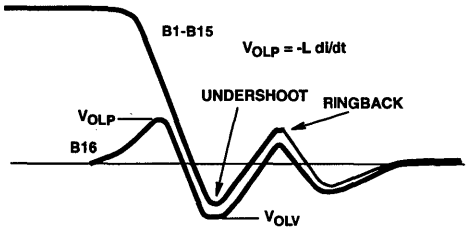


FIGURE 2. GROUND BOUNCE DESCRIPTION

The example shown here assumes a 60Ω trace impedance and 20pF per foot trace capacitance. The loaded impedance is 40Ω. Since the output impedance of the CD74FCT162Q244 is typically 40Ω, there should be minimal refection because the loaded trace is matched to the driver output Z. Of course as trace lengths change and the characteristic trace impedance changes, the loaded Z will change. Figure 3 shows this calculation. C_D is the load capacitance and C is the intrinsic line capacitance.

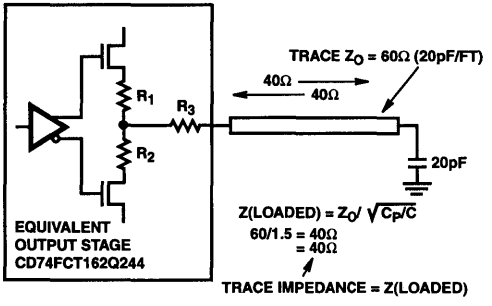


FIGURE 3. DESCRIPTION OF MATCHED LINE IMPEDANCE

Bus Hold Operation

Bus hold basically is a circuit that holds the last known state (Figure 4). Floating inputs do not need pullup/down resistors. All Quiet series devices have this feature. The bus hold sustaining current or hold current is 100μA. The effective bus hold capacitance is 8pF. It should be noted that if floating

inputs are left unterminated, oscillations may occur resulting in damage to devices not having the bus hold feature.

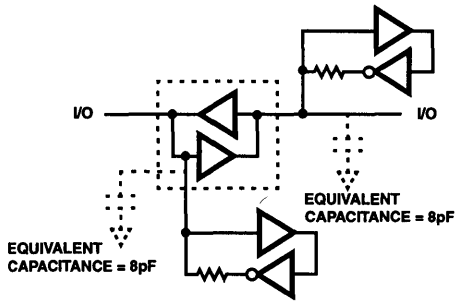


FIGURE 4. BUS HOLD

Figure 5 shows the time it takes to acquire and hold data. The bus hold circuit consists of 2 inverters with propagation delays of 300ps each. The typical hold time is 600ps with a max of 1ns; thus, noise pulses of <1ns are not responded to.

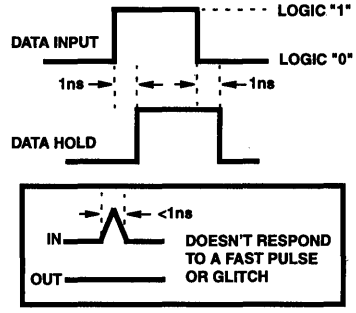


FIGURE 5. QUIET SERIES COMPARISON TO COMPETITION

Quiet Series Competition Comparison

Harris evaluated its "C" speed part to competitor B's "E" speed device. Figures 6, 7, 8 show waveforms (V_{CC} = 5V and C_L = 20pF) under light load conditions. This resulted in the Harris CD74FCT162Q244 showing much less noise than competition "B" part and similar noise performance to the competition "A" logic device. It should be noted here that all products have the bus hold feature. It should also be noted that the Q Series sub micron CMOS parts exhibit about half the dynamic power consumption compared to ABT's BiCMOS parts.

TABLE 1. COMPETITIVE COMPARISON

PARAMETER / PART	HARRIS CD74FCT 162Q244	COMP. A 74ABT 162244	COMP. B 74FCT 162H244E
Undershoot	0V	-0.2V	-1.5V
Ringback	0V	0V	0.7V
Ground Bounce	0.1V	0.1V	0.5V
I_C at 2.5MHz	16.5mA	30mA	16.5mA

Typical Application Hints

The Q Series parts are especially useful for PCI bus interface because this bus doesn't tolerate noisy logic. When buffering DRAM or SRAM and memory size is relatively low, it is very important to have a buffer with low overshoot and undershoot. Logic that doesn't have noise compensation will cause unwanted transition caused by ringing and ringback (Figure 1). Chip sets do not have enough drive for even light load (20pF to 50pF) applications. So quiet buffering is extremely important.

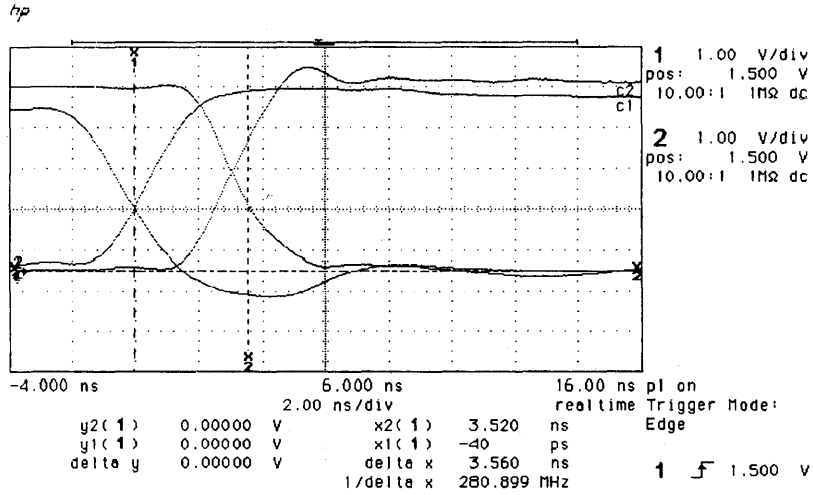


FIGURE 6. HARRIS 74FCT162Q244CTV

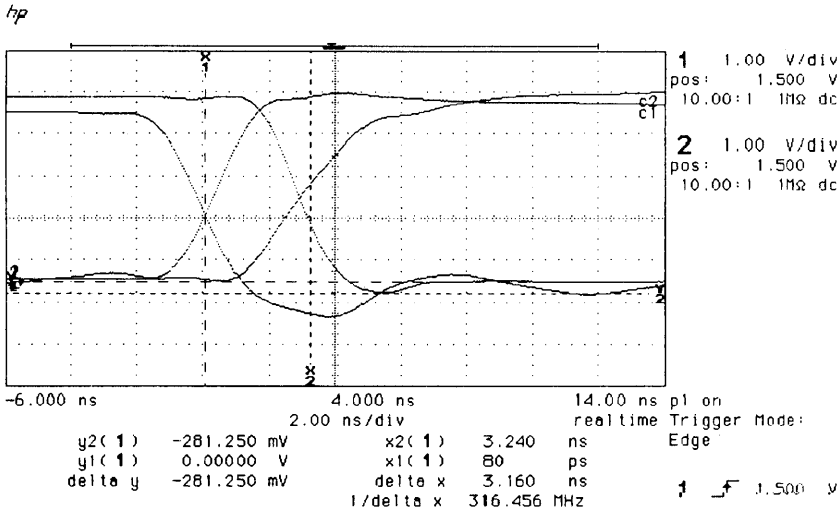


FIGURE 7. COMPETITION A: 74ABT162244DL

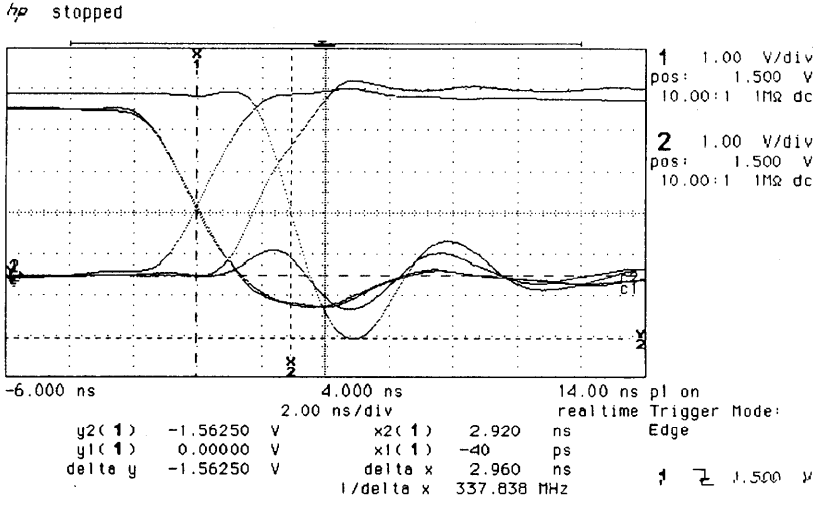


FIGURE 8. COMPETITION B: 74FCT162H244EPV

Harris Semiconductor

TechBrief

No. TB343 December 1996

Harris Logic

FCT vs ABT Logic Comparison - Double Density Types

Delays-Noise-Power

This brief shows that Harris FCT is faster and less noisy than ABT logic. With recent improvements in Harris FCT, propagation delays have reached 3.2ns maximum, which is substantially faster than ABT. For example, Harris FCT has excellent performance under heavy loads whereas the competing ABT part is almost 1ns slower. The ABT undershoot and power consumption (shown in the table as I_{CC} current drain) are twice that of the Harris part. The following table shows a direct comparison.

SWITCHING AND POWER CONSUMPTION COMPARISON

PARAMETER AND CONDITIONS	FCT162244	ABT16244A
t_P (typ) 120pF All Bits Switching	3.6ns (Figure 2)	4.4ns
t_P (typ) 50pF 1 Bit Switching	3.0ns (Figure 3)	3.6ns
t_P (typ) 50pF All Bits Switching	3.3ns (Figure 4)	4.0ns
Undershoot 120pF All Bits Switching	-0.75V (Figure 2)	-1.7V
Undershoot 50pF 1 Bit Switching	-0.85V (Figure 3)	-1.3V
Undershoot 50pF All Bits Switching	-1.2V (Figure 4)	-1.6V
I_{CC} (max)	17mA	32mA

Figure 2 shows FCT heavy load switching waveform comparison to ABT logic. Figures 3 and 4 show light load comparisons.

Type Applicability

The Harris Double Density Octal types that apply to this comparison with the ABT counterpart are:

CD74FCT16240T CD74FCT16244T CD74FCT16245T
CD74FCT16373T CD74FCT16374T CD74FCT16500T
CD74FCT16540T CD74FCT16541T CD74FCT16543T
CD74FCT16646T CD74FCT16652T CD74FCT16823T
CD74FCT16952T

Bus Contention

When a bus driver is in three-state, bus contention is not a problem. But when two or more drivers want control of the bus at the same time, data can be disrupted and damage to a driver is possible. Normally the Harris FCT can handle a contending device in the following worst-case scenarios:

- When FCT device is low and contending device is high, FCT will sink approximately 120mA through the active pull-down. See the data sheet parameter I_{ODL}.
- When the FCT device is high and a contending driver is low, drive current is approximately 100mA. See data sheet parameters I_{ODH} and I_{OS}.

With all of the outputs switching simultaneously, maximum current must be observed. Based on the above, Harris FCT will not be damaged, yet ABT would typically exhibit damage to the part.

Live Insertion

FCT like ABT must have all enables pulled up to ensure the outputs are in three-state during a live board insertion.

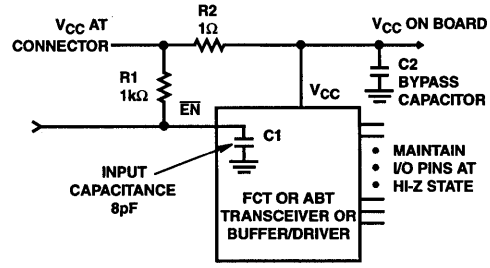


FIGURE 1. LIVE INSERTION CONFIGURATION

It should be noted that in Figure 1, R1xC1 should be >10 times faster than R2xC2. Where C2 is the total capacitance between on-board V_{CC} and ground, including all by-pass capacitors. This allows the voltage at /EN pin to reach logic "1" level much earlier.

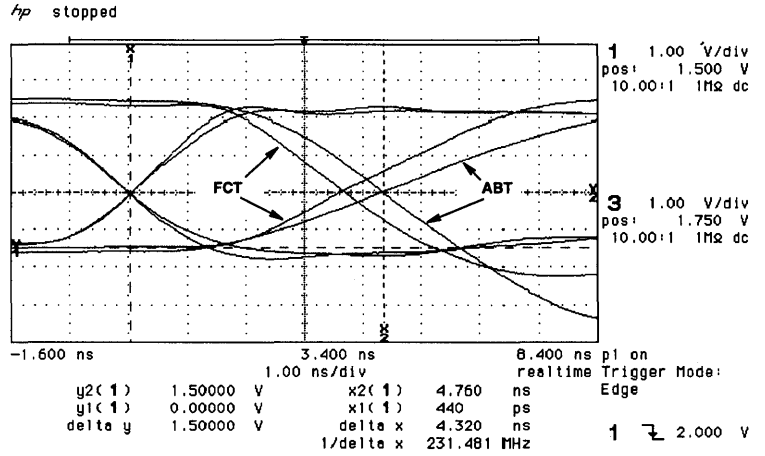


FIGURE 2. CD74FCT162244E COMPARISON TO ABT16244A, 120pF LOAD, ALL BITS SWITCHING

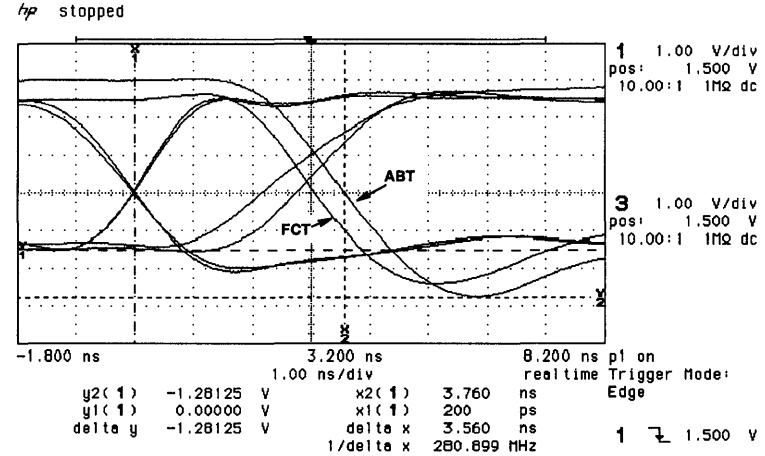


FIGURE 3. CD74FCT162244E COMPARISON TO ABT16244A, 50pF, 1-BIT SWITCHING

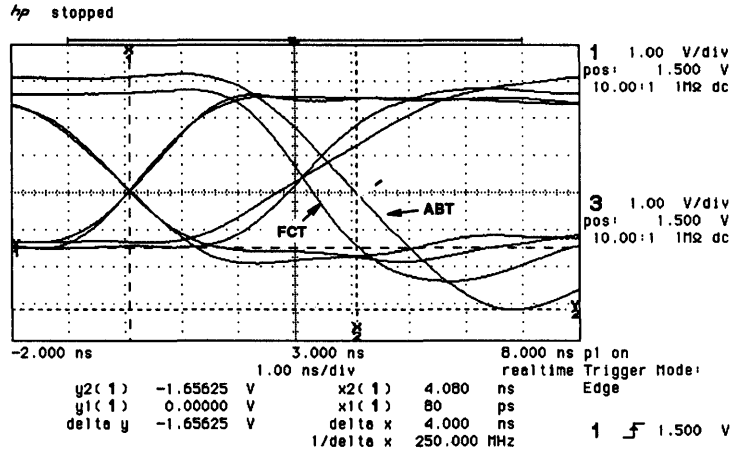


FIGURE 4. CD74FCT162244E COMPARISON TO ABT16244A, 50pF, ALL BITS SWITCHING

Harris Semiconductor

TechBrief

No. TB344 December 1996

Harris Logic

CD74FCT162344T For Heavy Load/High Fan Out Applications

Introduction

Complex memory modules and high-end motherboards require a driver to buffer and drive many loads. In some cases, the total capacitive load for each driver may exceed 150pF. As a result, the driver propagation delay significantly increases and the signal waveform deteriorates as it travels down the trace. This brief describes the CD74FCT162344T advantages in heavy load applications.

Enhanced Driving of Transmission Lines

On a high performance motherboard the signal rise/fall times are extremely fast, undermining signal integrity. Figure 1 shows a typical CD74FCT16244T buffer driving 12 logic devices. Since most traces on the board must be treated as transmission lines, this loading condition causes the signal integrity to deteriorate even more.

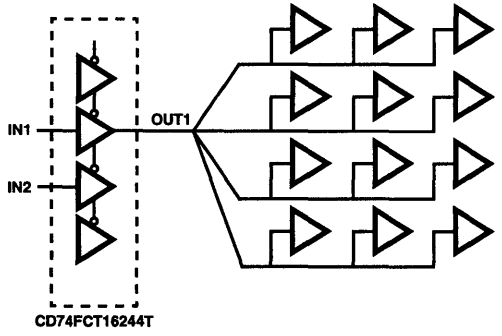


FIGURE 1. DRIVER WITH HEAVY LOADS

On the other hand, the CD74FCT162344T has far greater fanout. Its output stage was designed for balanced drive (both rise and fall directions). The I/V curve indicates ±24mA static current. Actually the available instantaneous current is 150mA which allows for driving high capacitance loads. Figure 2 exhibits each of the 4 outputs driving only 3 loads instead of all 12. This is a major advantage. Thus the Address/Clock Driver devices offer a solution for converting heavy loads to light loads.

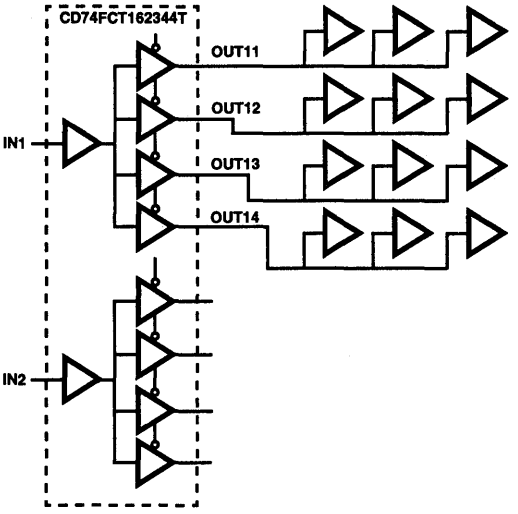


FIGURE 2. IMPROVED SOLUTION - DRIVER WITH NOMINAL LOADS

Maintaining Low Skew

Because there are twice as many output drivers on the CD74FCT162344T, 32 to 16 on the CD74FCT16244T; skew between drivers become very important. Skew is typically 0.25ns (see data sheet for exact specification method). Figure 2 shows very low skew between outputs provided by equalization of on-chip (with no delay stages) input to output delay and interconnect paths. It should be noted that trace length matching is also extremely important. Typically, propagation delay is 0.2ns per inch of trace. If traces are mismatched by 1 inch this would result in a skew error of 200ps.

Product Features

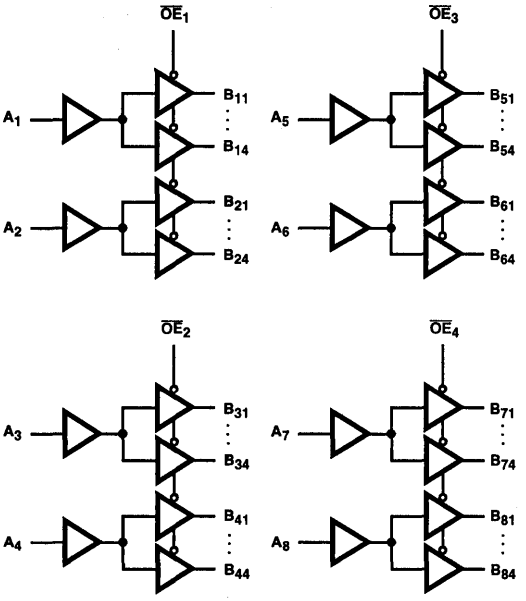
- **Ideal for Address Line Driving and Clock Distribution**
- **Eight Banks with 1:4 Fanout with Three-State Control**
- **Maximum $t_{SK(O)}$ Output Skew**
  - **Suffix AT ..... <500ps**
  - **Suffix CT ..... <500ps**
  - **Suffix T ..... <250ps**
- **Maximum Propagation Delay**
  - **Suffix AT 4.8ns**
  - **Suffix CT 4.3ns**
  - **Suffix ET 3.8ns**
- **Balanced Output Drivers: ±24mA**
- **Hysteresis On All Inputs**

Product Description

The CD74FCT162344T is an address/clock driver designed to provide the ability to fanout to memory arrays. Eight banks, each with a fanout of four, and three-state control, provide efficient address distribution. One or more banks may be used for clock distribution.

The CD74FCT162344T has balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Functional Block Diagram



Tape and Reel Specification for Integrated Circuits

Author: Laszlo Nemeth

Introduction

Many surface mounted devices (SMD) are being packaged for shipment in embossed tape and wound onto reels. The Harris Tape and Reel specifications are in compliance with Electronics Industries Association Standards for "Embossed Carrier Taping of Surface Mount Components for Automatic Handling".

- EIA-481-1-A..... for the 8mm and 12mm Wide Tape
- EIA-481-2..... for the 16mm and 24mm Wide Tape
- EIA-481-3... for the 32mm, 44mm and 56mm Wide Tape

Harris now supplies many different SMD's in Tape and Reel, as shown in Table 1.

General Information

The Harris Tape and Reel packing system protects the product from mechanical and electrical damage and is designed for automatic pick-and-place equipment.

The Tape and Reel packing system consists of a Pocket Carrier Tape sealed with a protective Cover Tape to hold the devices in place.

The devices are loaded with leads down, into the carrier pockets.

The tape is wound onto a plastic reel for Labeling and Packing for shipment.

All tape sizes are supplied on 13in diameter reels.

The conductive Carrier Tape, and antistatic coated Transparent Cover Tape and Reel provide ESD protection.

Information Labels, ESD Labels and Barcode Labels (if required) are placed on each reel.

Transparent Cover Tape allows device verification and brand inspection without having to remove or handle components.

No more than 2 date codes will be combined on any one reel.

TABLE 1. PACKAGE AND TAPE SPECIFICATIONS

PKG TYPE	NO. OF LEADS	PKG WIDTH	TAPE WIDTH mm	POCKET PITCH mm	UNITS/ REEL	TRAILER "A" LENGTH		LEADER "B" POCKETS	LEADER "B" LENGTH
SOPN	8	0.155	12	8	2,500	77	616mm	77	616mm
SOPN	14	0.155	16	8	2,500	77	616mm	77	616mm
SOPN	16	0.155	16	8	2,500	77	616mm	77	616mm
SOPW	16	0.296	16	12	1,000	34	420mm	45	552mm
SOPW	20	0.296	24	12	1,000	34	420mm	45	552mm
SOPW	24	0.296	24	12	1,000	34	420mm	45	552mm
SOPW	28	0.296	24	12	1,000	34	420mm	45	552mm
SSOP	16	0.209	16	12	1,000	24	420mm	45	552mm
SSOP	20	0.209	16	12	1,000	34	420mm	45	552mm
SSOP	24	0.209	16	12	1,000	34	420mm	45	552mm
SSOP	28	0.155	16	8	2,500	77	616mm	77	616mm
SSOP	28	0.209	24	12	1,000	34	420mm	45	552mm
PSOP2	20	0.296	24	12	1,000	34	420mm	45	552mm
PSOP3	20	0.433	24	24	650	15	360mm	25	600mm
PSOP3	24	0.433	24	24	650	15	360mm	25	600mm
PLCC	20	0.350 SQ	16	12	1,000	53	660mm	64	792mm
PLCC	28	0.450 SQ	24	16	750	15	256mm	25	416mm
PLCC	44	0.650 SQ	32	24	500	15	384mm	25	624mm
PLCC	68	0.950 SQ	44	32	250	25	832mm	25	832mm

TABLE 1. PACKAGE AND TAPE SPECIFICATIONS (Continued)

PKG TYPE	NO. OF LEADS	PKG WIDTH	TAPE WIDTH mm	POCKET PITCH mm	UNITS/ REEL	TRAILER "A" LENGTH		LEADER "B" POCKETS	LEADER "B" LENGTH
PLCC	84	1.150 SQ	44	36	200	25	936mm	25	936mm
MO-169	3,5,7	0.395	24	16	800	50	800mm	50	800mm
MQFP	44	10mm SQ	24	24	500	25	624mm	25	624mm
TQFP	48	7mm SQ	16	12	1,000	34	420mm	45	552mm
TQFP	80	14mm SQ	24	20	600	21	420mm	28	552mm

NOTES:

1. Package size is in inches unless otherwise indicated.
2. SSOP (0.155) also known as QSOP.
3. Pocket count and trailer/leader lengths are typical.

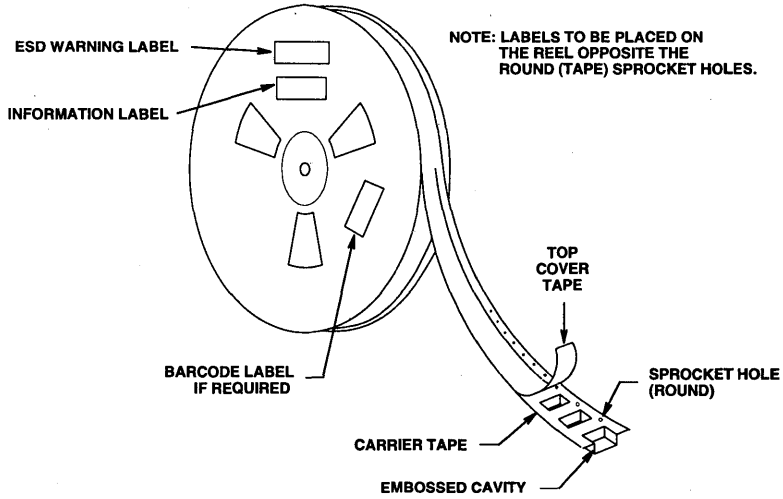


FIGURE 1. TAPE/REEL AND LABEL INFORMATION

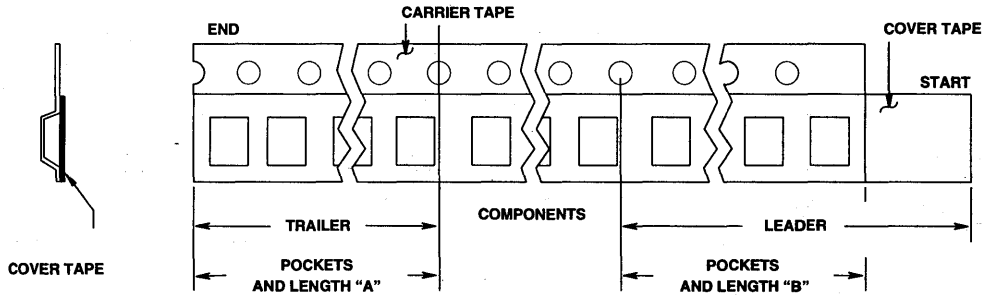


FIGURE 2. TAPE LEADER AND TRAILER

Materials and Design

Carrier Tape

The Pocketed Carrier Tape is made of Conductive Polystyrene + Carbon material (or equivalent). The surface resistivity is $10^6\Omega$/Sq. Maximum.

Pocket Tapes are designed in such a manner that the components remain in position for automatic handling after the removal of the cover tape.

Each pocket has a hole in the center for automated sensing of whether or not the pocket is occupied, thus facilitating device removal.

Sprocket holes along the edge of the carrier tape enable direct feeding into automated board assembly equipment.

See Figures 3 and 4 for Carrier Tape dimensions.

Cover Tape

The Cover Tape is made of Antistatic Transparent Polyester Film.

The surface resistivity is $10^7\Omega$/Sq. minimum to $10^{11}\Omega$/Sq. Maximum.

The Cover Tape is heat-sealed to the edges of the Carrier Tape to encase the devices in the pockets.

The force to peel back the Cover Tape from the Carrier Tape shall be a MEAN value of 30 to 80gm (0.3N to 0.8N).

Reel

The device loading orientation is in compliance with EIA-481-1-A, EIA-481-2, EIA-481-3. (See Figure 5).

The loaded Carrier Tape is wound onto a reel that is uniformly sized for all packages. (See Figure 6).

The Reel is made of Antistatic High Impact Polystyrene. The surface resistivity $10^7\Omega$/Sq. minimum to $10^{11}\Omega$/Sq. Maximum.

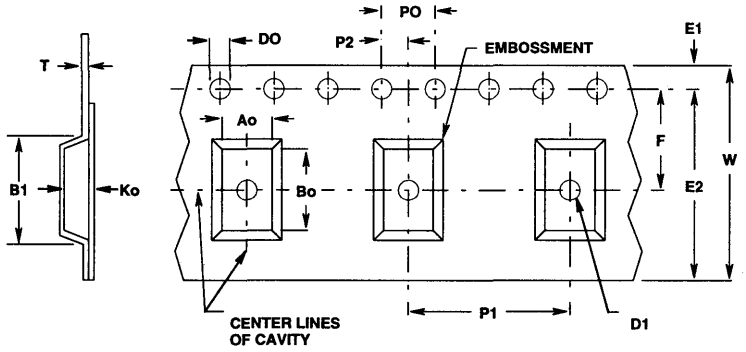


FIGURE 3. CONFIGURATION DWG FOR 12MM, 16MM, 24MM POCKET TAPE

W (NOMINAL) TAPE WIDTH	(NOTE 9) B1(MAXIMUM)	F (NOMINAL)	E2 (MINIMUM)
12mm (0.472)	8.2 (0.323)	5.5 (0.217)	10.25 (0.404)
16mm (0.629)	12.1 (0.476)	7.5 (0.295)	14.25 (0.561)
24mm (0.945)	20.1 (0.791)	11.5 (0.453)	22.25 (0.876)

NOTES:

4. Dimensions are in MM and are nominal unless otherwise indicated (inches are in brackets for reference only).
5. "T" dimension, nominal 0.30 or 0.35
6. "P1" cavity pitch is 8.0 MM min. and increases in 4.0 MM increments depending on package size. (See Table 1)
7. "P0" dimension is 4.0 MM
8. "P2" dimension is 2.0 MM
9. "B1" actual dimension is determined by package size.
10. "D1" diameter is 1.5 MM min.
11. "Do" diameter is 1.5 MM
12. "E1" dimension is 1.75 MM
13. "Ao", "Bo", "Ko" dimensions determined by component size

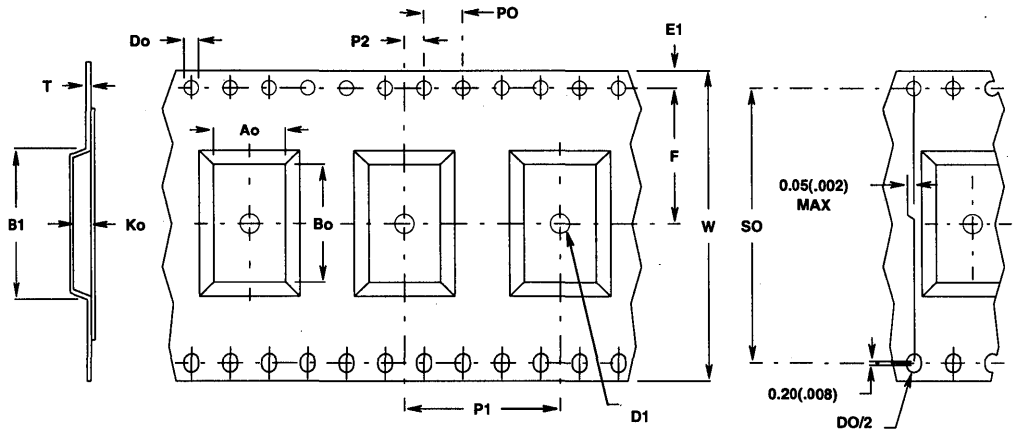


FIGURE 4. CONFIGURATION DWG FOR 32mm AND 44mm POCKET TAPE

W (NOMINAL) TAPE WIDTH	(NOTE 19) B1 (MAXIMUM)	F (NOMINAL)	S (NOMINAL)
32mm (1.260)	23.0 (0.906)	14.2 (0.559)	28.4 (1.118)
44mm (1.732)	35.0 (1.378)	20.2 (0.795)	40.4 (1.591)

NOTES:

14. Dimensions are in millimeters and are nominal unless otherwise indicated (inches are in brackets for reference only).
15. "T" dimension, nominal 0.30 or 0.35
16. "P1" cavity pitch is 8.0mm min. and increases in 4.0 MM increments depending on package size. (See Table 1)
17. "P0" dimension is 4.0mm
18. "P2" dimension is 2.0mm
19. "B1" actual dimension is determined by package size.
20. "D1" diameter is 2.0mm min.
21. "Do" diameter is 1.5mm
22. "E1" dimension is 1.75mm
23. "Ao", "Bo", "Ko" dimensions determined by component size

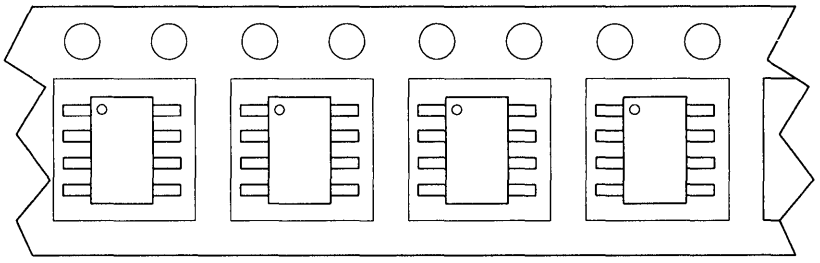


FIGURE 5A. SOP, SSOP AND PSOP (SSOP ALSO KNOWN AS QSOP)

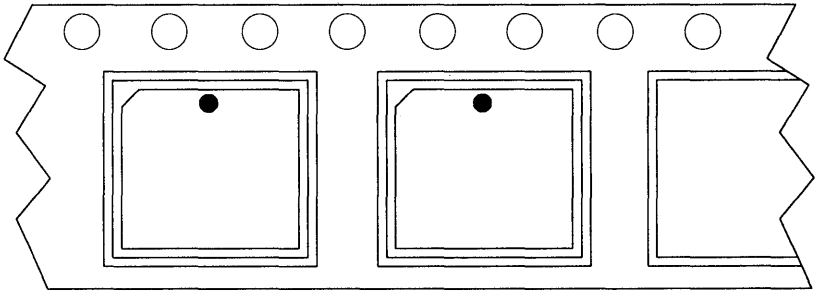


FIGURE 5B. PLCC

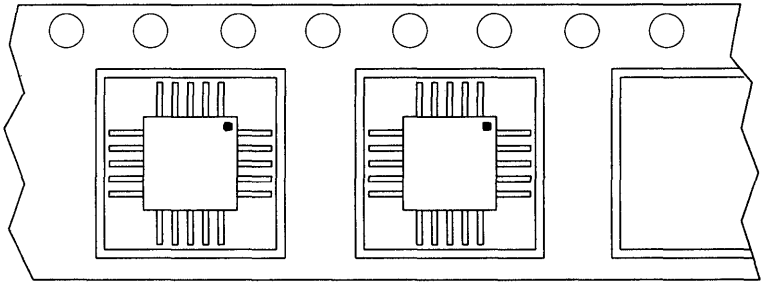


FIGURE 5C. MQFP AND TQFP

FIGURE 5. MECHANICAL POLARIZATION DIAGRAMS

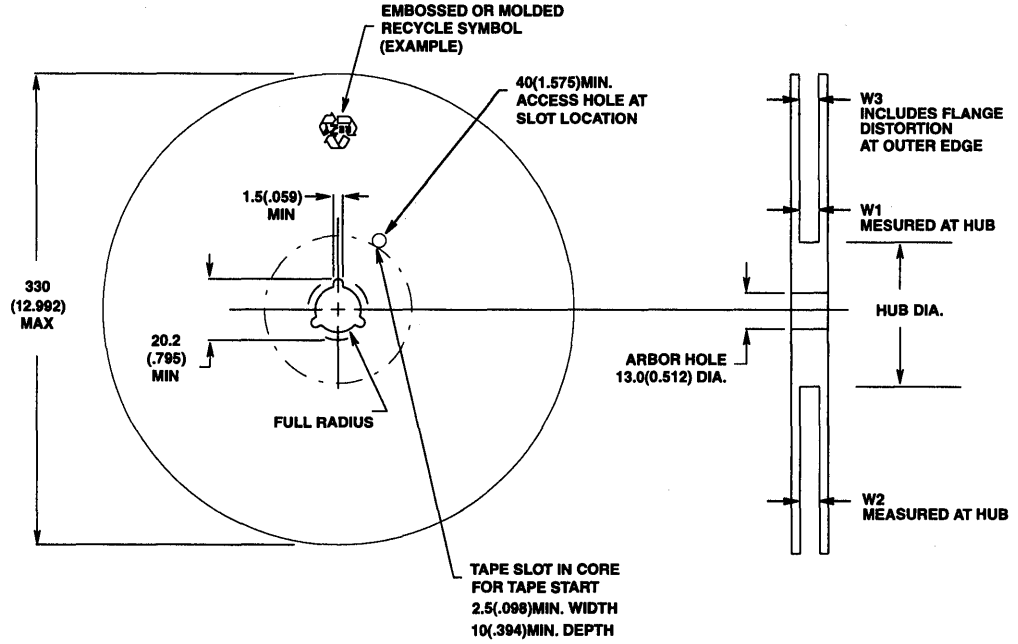


FIGURE 6. REEL DIMENSIONS

TAPE WIDTH	HUB (MINIMUM)	W1 (NOMINAL)	W2 (MAXIMUM)	W3 (MAXIMUM)
12mm (0.472)	100 (4.0)	12.4 (0.488)	18.4 (0.724)	15.4 (0.606)
16mm (0.629)	100 (4.0)	16.4 (0.646)	22.4 (0.882)	19.4 (0.764)
24mm (0.945)	100 (4.0)	24.4 (0.961)	30.4 (1.197)	27.4 (1.079)
32mm (1.260)	100 (4.0)	32.4 (1.276)	38.4 (1.512)	35.4 (1.394)
44mm (1.732)	152 (6.0)	44.4 (1.748)	50.4 (1.984)	47.4 (1.866)
24mm (0.945) (Note 25)	152 (6.0)	24.4 (0.961)	30.4 (1.197)	27.4 (1.079)

NOTES:

24. Dimensions are in millimeters (inches are in brackets for reference only).
25. Used for 44 lead MQFP on 24mm wide tape.

CMOS LOGIC 10

HARRIS QUALITY AND RELIABILITY

PAGE

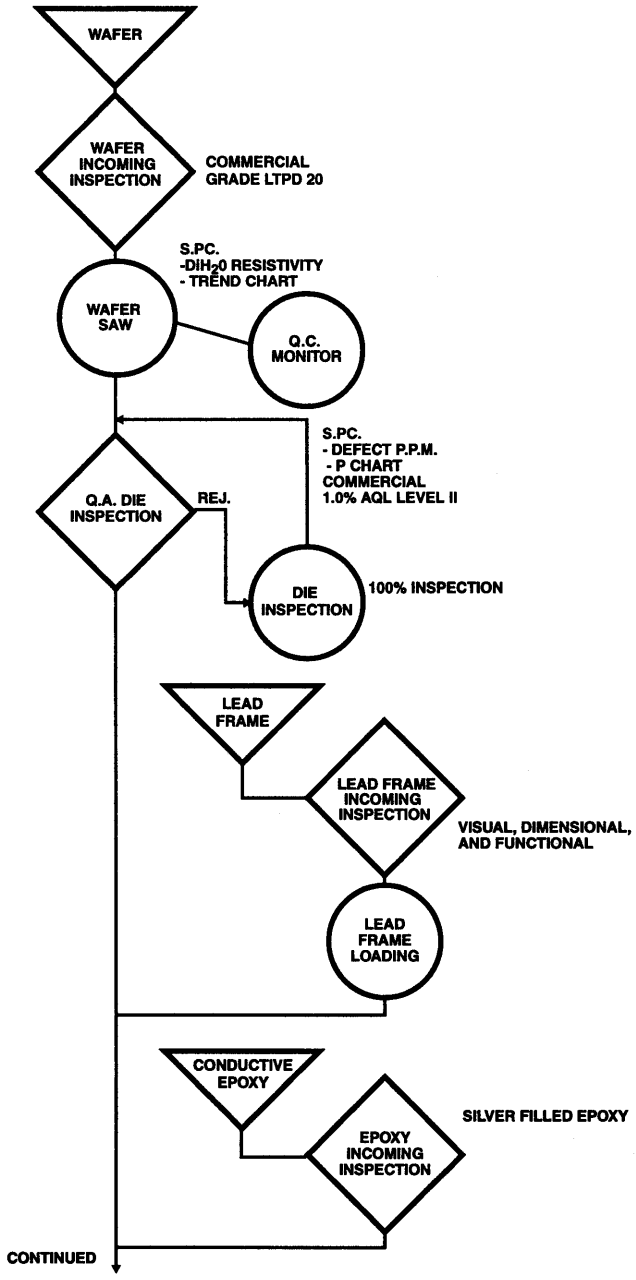
Quality and Reliability 10-3

Assembly Process Flow 10-3

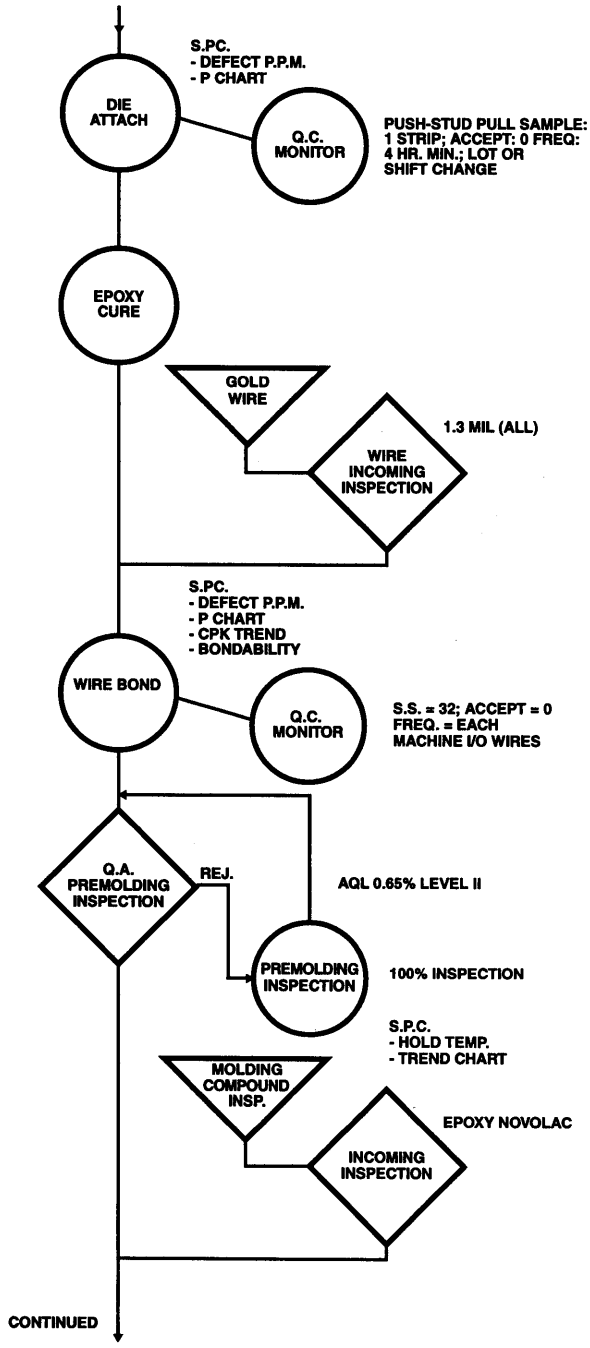
EXAMPLE: Assembly In-Process Quality and Reliability Control 10-8

Assembly Process Flow

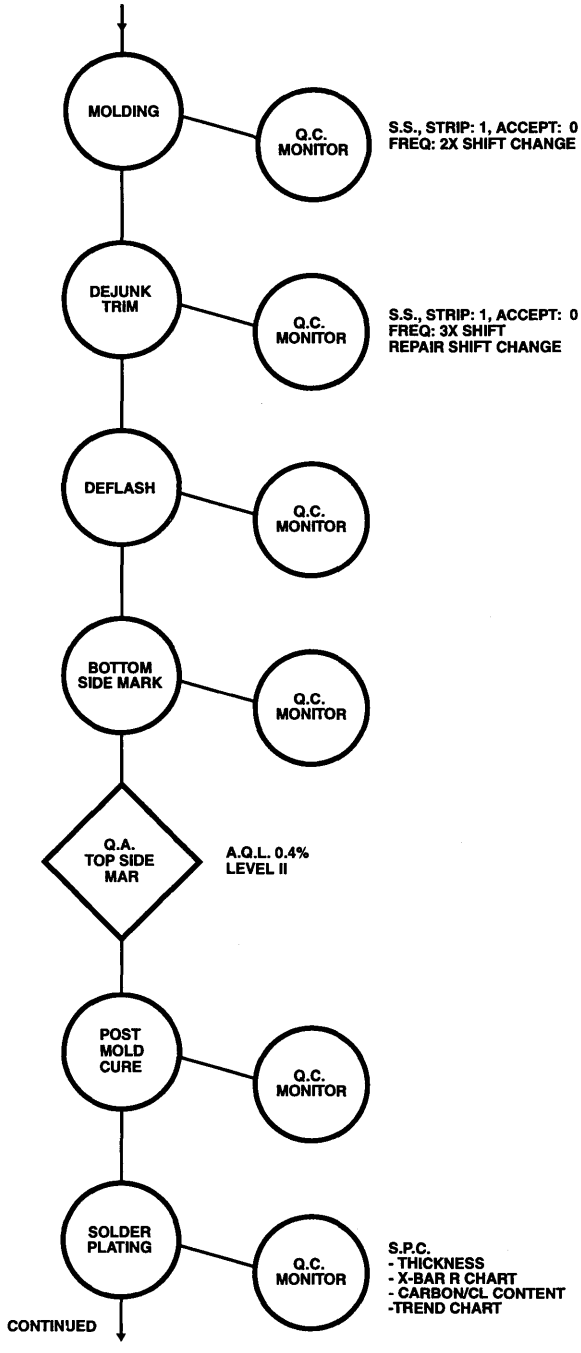
PRODUCT FLOW FOR SOIC, QSOP, SSOP



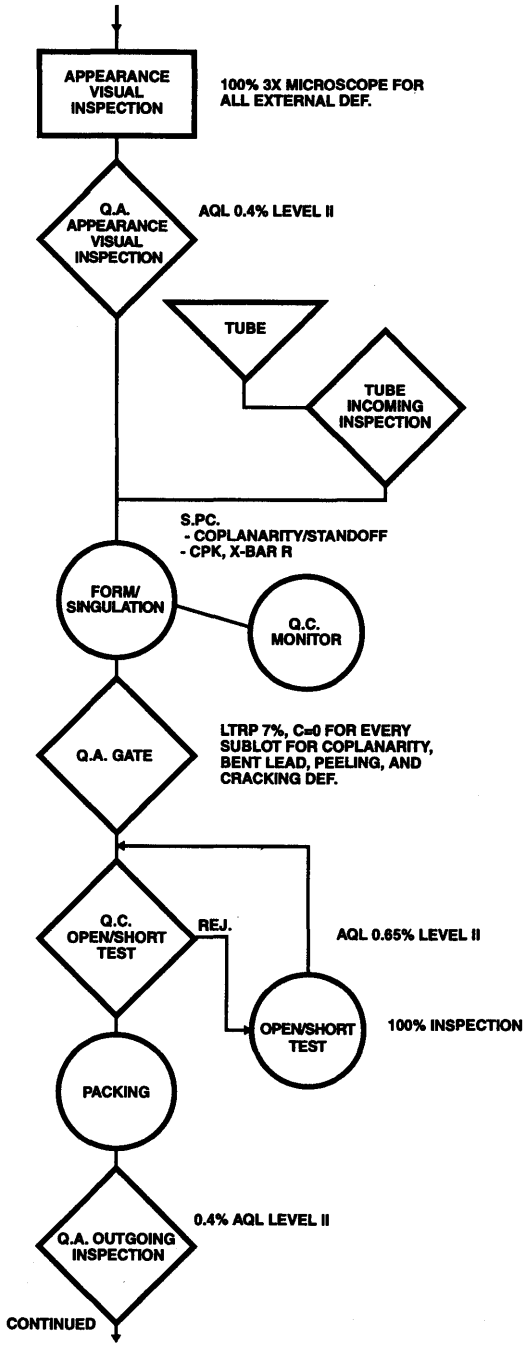
Assembly Process Flow (Continued)



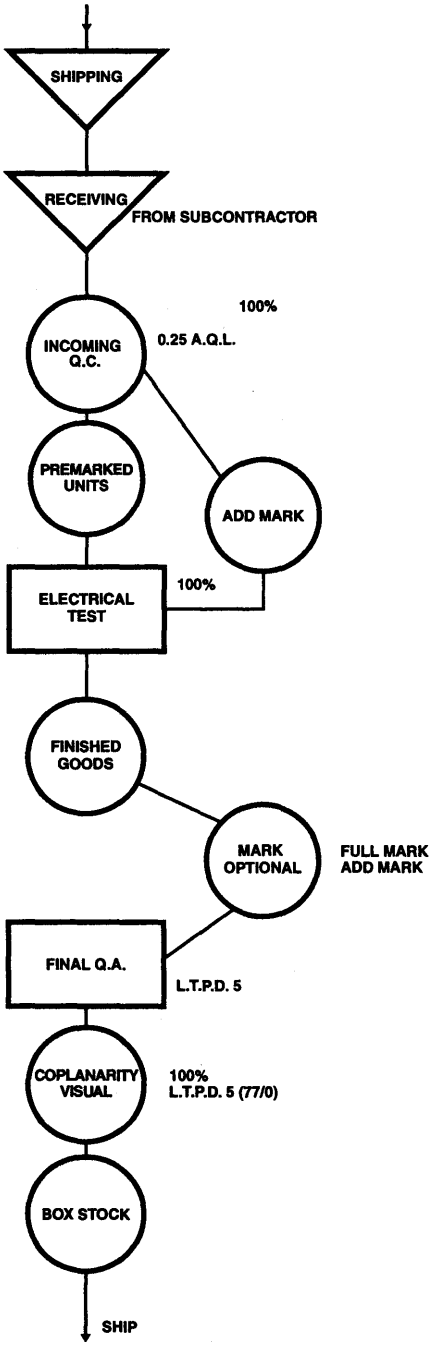
Assembly Process Flow (Continued)



Assembly Process Flow (Continued)



Assembly Process Flow (Continued)



EXAMPLE: Assembly In-Process Quality and Reliability Control

ITEM			CONTROL METHOD (FREQUENCY)
INCOMING MATERIAL QC			Functional test visual inspection and dimensions check; each shipment lot.
IN-PROCESS QC			Operating conditions and product quality monitors for all operations (see product flow).
RELIABILITY/QC MONITORS	Die Shear Test		5 each/epoxy curing cycle/machine. Criteria: MIL-STD-883C, METHOD 2019
	Bond Pull Test		4 times/shift/machine. Criteria: MIL-STD-883C, METHOD 2011
	Ball Shear Test		2 times/shift/machine. Criteria: ASTM STP 850
	BONDING PAD		
		Cratering Monitor	2 times/shift/machine.
		Solderability Test	3 devices/lot/shift -- S/D -- Plastic IC. Criteria: MIL-STD-883C, METHOD 2003
	TIN THICKNESS		
		Measurement	5 devices/sub-lot. Criteria: MIL-M-38510H, ITEM 3.5.6.2.1
		Marking Permanency	11 devices/lot.
		Test	Criteria: MIL-STD-883C, METHOD 2015
STORAGE			All wafers, frames, and wire stored in cabinets purged with dry nitrogen. Cold storage for epoxy, coating material, compound and ink pen manufacturer's specification.
ESD PROTECTION			All operators wear earth straps. All equipment and work tables are grounded. KATS UL-288 wax for clean room. Ionizer in use when units are singulated.
QA ENGINEERING INSPECTION	D.I. WATER		
		Bacteria Incubation	Weekly (100 COL/100 CC).
	D.I. WATER		
		Impurity Analysis	2 time/year.
	EPOXY THICKNESS		
		Measurement	3 devices/machine/weekly.
		Carbon Content Analysis	1 time/tin bath and solder bath/two weeks.
		Rinse Efficiency Test	1 time/tin bath (solder dipping machine)/week.
		Impurity Content Analysis of Raw Material	Conductive Epoxy: Quarterly Solder Bar: 1 Time/4 Shipment Lots Solder: 1 Time/Two Weeks Molding Compound: 2 Times/Year
	PROCESS/EQUIPMENT		
		Capability (CPK) Measurement	Once per month.
RELIABILITY TEST	Pressure Cooker Test		once per month by package type. (sample size: 32 pcs., 168 hours)
	Temperature Cycle		Once per month. (sample size: 32 pcs., 100/200 cycles)
DOCUMENT CONTROL SYSTEM			All inspection criteria and operation procedures/conditions instructions are specified in documents
CALIBRATION SYSTEM EQUIPMENT AND INSTRUMENTS			To calibrate all tools, equipment, and instruments periodically in accordance with the requirement of MIL-STD-45662.
ENVIRONMENTAL MONITOR SYSTEM			Cleanliness/atmosphere/temperature/relative humidity monitor to meet the requirement of FED-STD-209D.
CERTIFICATION AND DISQUALIFIED	Qualification		Q.A. inspector, twice per year.production inspector and operator, once per year.
	Disqualified		According to production inspector's monthly performance (Def PPM) to implement disqualification, retraining, and recertification system.
TRACEABILITY SYSTEM	Materials Tracking		All production lots can be traced to supplier's lot of material used and IQC inspection results.
	Assembly Conditions Tracking		All production lots can be traced to assembly conditions.
CONTINUOUS QUALITY AND YIELD IMPROVE MENT	Attendant		Production/process engineer and QA staff.
	Purpose		To review and improve the quality and assembly yield.
	Frequency		Weekly.

LPT/FCT LOGIC 11

PACKAGING INFORMATION

PAGE

Package Selection Guide 11-3

Plastic Packages for Integrated Circuits 11-9

E20.3 (JEDEC MS-001-AD ISSUE D) 11-9

E24.3 (JEDEC MS-001-AF ISSUE D) 11-10

M14.15-P 11-11

M16.15-P 11-12

M16.15A-P 11-13

M16.3-P 11-14

M20.15-P 11-15

M20.209 (JEDEC MO-150-AE ISSUE B) 11-16

M20.3 (JEDEC MS-013-AC ISSUE C) 11-17

M20.3-P 11-18

M24.15-P 11-19

M24.209 (JEDEC MO-150-AG ISSUE B) 11-20

M24.3 (JEDEC MS-013-AD ISSUE C) 11-21

M24.3-P 11-22

M48.240-P 11-23

M48.300-P 11-24

M56.240-P 11-25

M56.300-P 11-26

NOTES:

1. For information on Tape and Reel see Tech Brief 347 in Section 9.
2. Additional packages may be available upon request. Contact Sales and Marketing.

Package Selection Guide

LOGIC PACKAGE SELECTION GUIDE

PART NUMBER	PDIP	SOIC	SSOP	QSOP	TSSOP	FILE NUMBER
CD29FCT520T	-	M24.3-P	-	M24.15-P	-	4164
CD29FCT52T	-	M24.3-P	-	M24.15-P	-	4163
CD54FCT245	E20.3	M20.3	M20.209	-	-	2301
CD74FCT138T	-	M16.3-P, M16.15-P	-	M16.15A-P	-	4158
CD74FCT139T	-	M16.3-P, M16.15-P	-	M16.15A-P	-	4159
CD74FCT151T	-	M16.3-P, M16.15-P	-	M16.15A-P	-	4160
CD74FCT153T	-	M16.3-P, M16.15-P	-	M16.15A-P	-	4161
CD74FCT157T	-	M16.3-P	-	M16.15A-P	-	4166
CD74FCT162240T	-	-	M48.300-P	-	M48.240-P	4180
CD74FCT162244T	-	-	M48.300-P	-	M48.240-P	4181
CD74FCT162245T	-	-	M48.300-P	-	M48.240-P	4217
CD74FCT162373T	-	-	M48.300-P	-	M48.240-P	4182
CD74FCT162374T	-	-	M48.300-P	-	M48.240-P	4183
CD74FCT16240T	-	-	M48.300-P	-	M48.240-P	4180
CD74FCT16244T	-	-	M48.300-P	-	M48.240-P	4181
CD74FCT16245T	-	-	M48.300-P	-	M48.240-P	4217
CD74FCT162500T	-	-	M56.300-P	-	M56.240-P	4202
CD74FCT162501T	-	-	M56.300-P	-	M56.240-P	4184
CD74FCT162511T	-	-	M56.300-P	-	M56.240-P	4218
CD74FCT162540T	-	-	M48.300-P	-	M48.240-P	4185
CD74FCT162541T	-	-	M48.300-P	-	M48.240-P	4186
CD74FCT162543T	-	-	M56.300-P	-	M56.240-P	4187
CD74FCT162646T	-	-	M56.300-P	-	M56.240-P	4188
CD74FCT162652T	-	-	M56.300-P	-	M56.240-P	4203
CD74FCT162823T	-	-	M56.300-P	-	M56.240-P	4189
CD74FCT162827T	-	-	M56.300-P	-	M56.240-P	4190
CD74FCT162841T	-	-	M56.300-P	-	M56.240-P	4204
CD74FCT162952T	-	-	M56.300-P	-	M56.240-P	4191
CD74FCT162Q244T	-	-	M48.300-P	-	M48.240-P	4280
CD74FCT162Q245T	-	-	M48.300-P	-	M48.240-P	4277
CD74FCT162Q373T	-	-	M48.300-P	-	M48.240-P	4278
CD74FCT162Q374T	-	-	M48.300-P	-	M48.240-P	4279

LOGIC PACKAGE SELECTION GUIDE (Continued)

PART NUMBER	PDIP	SOIC	SSOP	QSOP	TSSOP	FILE NUMBER
CD74FCT163240	-	-	M48.300-P	-	M48.240-P	4255
CD74FCT163244	-	-	M48.300-P	-	M48.240-P	4192
CD74FCT163245	-	-	M48.300-P	-	M48.240-P	4193
CD74FCT163373	-	-	M48.300-P	-	M48.240-P	4194
CD74FCT163374	-	-	M48.300-P	-	M48.240-P	4195
CD74FCT16373T	-	-	M48.300-P	-	M48.240-P	4182
CD74FCT16374T	-	-	M48.300-P	-	M48.240-P	4183
CD74FCT16500T	-	-	M56.300-P	-	M56.240-P	4202
CD74FCT16501T	-	-	M56.300-P	-	M56.240-P	4184
CD74FCT16511T	-	-	M56.300-P	-	M56.240-P	4218
CD74FCT16540T	-	-	M48.300-P	-	M48.240-P	4185
CD74FCT16541T	-	-	M48.300-P	-	M48.240-P	4186
CD74FCT16543T	-	-	M56.300-P	-	M56.240-P	4187
CD74FCT16646T	-	-	M56.300-P	-	M56.240-P	4188
CD74FCT16652T	-	-	M56.300-P	-	M56.240-P	4203
CD74FCT16823T	-	-	M56.300-P	-	M56.240-P	4189
CD74FCT16827T	-	-	M56.300-P	-	M56.240-P	4190
CD74FCT16841T	-	-	M56.300-P	-	M56.240-P	4204
CD74FCT16952T	-	-	M56.300-P	-	M56.240-P	4191
CD74FCT2151T	-	M16.3-P, M16.15-P	-	M16.15A-P	-	4160
CD74FCT2153T	-	M16.3-P, M16.15-P	-	M16.15A-P	-	4161
CD74FCT2157T	-	M16.3-P	-	M16.15A-P	-	4166
CD74FCT2240T	-	M20.3-P	-	M20.15-P	-	4167
CD74FCT2241T	-	M20.3-P	-	M20.15-P	-	4167
CD74FCT2244T	-	M20.3-P	-	M20.15-P	-	4167
CD74FCT2245T	-	M20.3-P	-	M20.15-P	-	4168
CD74FCT2253T	-	M16.15-P	-	M16.15A-P	-	4161
CD74FCT2257T	-	M16.3-P, M16.15-P	-	M16.15A-P	-	4166
CD74FCT2273T	-	M20.3-P	-	M20.15-P	-	4169
CD74FCT2373T	-	M20.3-P,	-	M20.15-P	-	4170
CD74FCT2374T	-	M20.3-P	-	M20.15-P	-	4171
CD74FCT238T	-	M16.3-P, M16.15-P	-	M16.15A-P	-	4158

LOGIC PACKAGE SELECTION GUIDE (Continued)

PART NUMBER	PDIP	SOIC	SSOP	QSOP	TSSOP	FILE NUMBER
CD74FCT239T	-	M16.3-P, M16.15-P	-	M16.15A-P	-	4159
CD74FCT240	E20.3	M20.3	M20.209	-	-	2227
CD74FCT240AT	E20.3	-	-	-	-	2227
CD74FCT240T	-	M20.3-P	-	M20.15-P	-	4167
CD74FCT241T	-	M20.3-P	-	M20.15-P	-	4167
CD74FCT244	E20.3	M20.3	M20.209	-	-	2227
CD74FCT244AT	E20.3	-	-	-	-	2227
CD74FCT244T	-	M20.3-P	-	M20.15-P	-	4167
CD74FCT245	E20.3	M20.3	M20.209		-	2301
CD74FCT245T	-	M20.3-P	-	M20.15-P	-	4168
CD74FCT251T	-	M16.3-P, M16.15-P	-	M16.15A-P	-	4160
CD74FCT253T	-	M16.3-P, M16.15-P	-	M16.15A-P	-	4161
CD74FCT2541T	-	M20.3-P	-	M20.15-P	-	4167
CD74FCT2543T	-	M24.3-P	-	M24.15-P	-	4173
CD74FCT2573T	-	M20.3-P	-	M20.15-P	-	4170
CD74FCT2574T	-	M20.3-P	-	M20.15-P	-	4171
CD74FCT257T	-	M16.3-P	-	M16.15A-P	-	4166
CD74FCT2646T	-	M24.3-P	-	M24.15-P	-	4175
CD74FCT2652T	-	M24.3-P	-	M24.15-P	-	4175
CD74FCT273	E20.3	M20.3	-	-	-	2303
CD74FCT273T	-	M20.3-P	-	M20.15-P	-	4169
CD74FCT2821T	-	M24.3-P	-	M24.15-P	-	4176
CD74FCT2823T	-	M24.3-P	-	M24.15-P	-	4176
CD74FCT2827T	-	M24.3-P	-	M24.15-P	-	4179
CD74FCT2828T	-	M24.3-P	-	M24.15-P	-	4179
CD74FCT2841T	-	M24.3-P	-	M24.15-P	-	4177
CD74FCT373	E20.3	M20.3	M20.209	-	-	2230
CD74FCT373AT	E20.3	-	-	-	-	2230
CD74FCT373T	-	M20.3-P	-	M20.15-P	-	4170
CD74FCT374	E20.3	M20.3	M20.209	-	-	2305
CD74FCT374T	-	M20.3-P	-	M20.15-P	-	4171
CD74FCT377T	-	M20.3-P	-	M20.15-P	-	4172
CD74FCT399T	-	M16.3-P, M16.15-P	-	M16.15A-P	-	4252

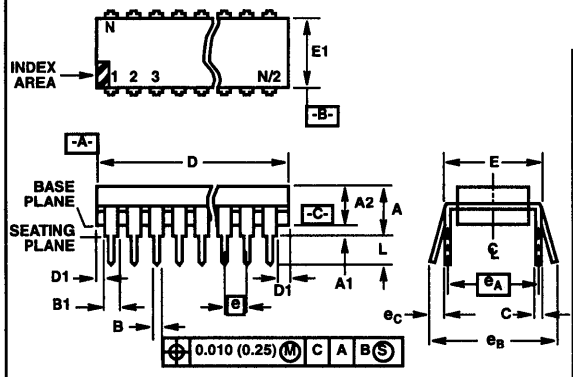
LOGIC PACKAGE SELECTION GUIDE (Continued)

PART NUMBER	PDIP	SOIC	SSOP	QSOP	TSSOP	FILE NUMBER
CD74FCT521T	-	M20.3-P	-	M20.15-P	-	4214
CD74FCT533T	-	M20.3-P	-	M20.15-P	-	4170
CD74FCT534T	-	M20.3-P	-	M20.15-P	-	4171
CD74FCT540	E20.3	M20.3	-	-	-	2283
CD74FCT540T	-	M20.3-P	-	M20.15-P	-	4167
CD74FCT541	E20.3	M20.3	M20.209	-	-	2283
CD74FCT541T	-	M20.3-P	-	M20.15-P	-	4167
CD74FCT543	E24.3	M24.3	M24.209	-	-	2399
CD74FCT543T	-	M24.3-P	-	M24.15-P	-	4173
CD74FCT544T	-	M24.3-P	-	M24.15-P	-	4173
CD74FCT564	E20.3	M20.3	M20.209	-	-	2295
CD74FCT573	-	M20.3	M20.209	-	-	2304
CD74FCT573AT	E20.3	-	-	-	-	2304
CD74FCT573T	-	M20.3-P	-	M20.15-P	-	4170
CD74FCT574	E20.3	M20.3	M20.209	-	-	2295
CD74FCT574T	-	M20.3-P	-	M20.15-P	-	4171
CD74FCT623T	-	M20.3-P	-	M20.15-P	-	4174
CD74FCT640T	-	M20.3-P	-	M20.15-P	-	4168
CD74FCT646	E24.3	M24.3	M24.209	-	-	2393
CD74FCT646T	-	M24.3-P	-	M24.15-P	-	4175
CD74FCT648T	-	M24.3-P	-	M24.15-P	-	4175
CD74FCT651	E24.3	M24.3	-	-	-	2394
CD74FCT651T	-	M24.3-P	-	M24.15-P	-	4175
CD74FCT652	E24.3	M24.3	-	-	-	2394
CD74FCT652T	-	M24.3-P	-	M24.15-P	-	4175
CD74FCT653	E24.3	M24.3	-	-	-	2403
CD74FCT654	E24.3	M24.3	-	-	-	2403
CD74FCT821A	E24.3	M24.3	-	-	-	2390
CD74FCT821T	-	M24.3-P	-	M24.15-P	-	4176
CD74FCT822A	E24.3	-	-	-	-	2390
CD74FCT823A	E24.3	-	-	-	-	2389
CD74FCT823T	-	M24.3-P	-	M24.15-P	-	4176
CD74FCT824A	E24.3	-	-	-	-	2389
CD74FCT825T	-	M24.3-P	-	M24.15-P	-	4176
CD74FCT827T	-	M24.3-P	-	M24.15-P	-	4179

LOGIC PACKAGE SELECTION GUIDE (Continued)

PART NUMBER	PDIP	SOIC	SSOP	QSOP	TSSOP	FILE NUMBER
CD74FCT828T	-	M24.3-P	-	M24.15-P	-	4179
CD74FCT841A	E24.3	M24.3	-	-	-	2397
CD74FCT841T	-	M24.3-P	-	M24.15-P	-	4177
CD74FCT842A	-	M24.3	-	-	-	2397
CD74FCT843A	-	M24.3	-	-	-	2396
CD74FCT843T	-	M24.3-P	-	M24.15-P	-	4177
CD74FCT844A	E24.3	-	-	-	-	2396
CD74FCT845T	-	M24.3-P	-	M24.15-P	-	4177
CD74FCT861A	-	M24.3	-	-	-	2392
CD74FCT861T	-	M24.3-P	-	M24.15-P	-	4178
CD74FCT863A	-	M24.3-P	-	M24.15-P	-	4178
CD74FCT863T	-	M24.3-P	-	M24.15-P	-	4178
CD74FCT864T	-	M24.3-P	-	M24.15-P	-	4178
CD74LPT16240	-	-	M48.300-P	-	M48.240-P	4215
CD74LPT16244	-	-	M48.300-P	-	M48.240-P	4216
CD74LPT16245	-	-	M48.300-P	-	M48.240-P	4205
CD74LPT16373	-	-	M48.300-P	-	M48.240-P	4206
CD74LPT16374	-	-	M48.300-P	-	M48.240-P	4207
CD74LPT16501	-	-	M56.300-P	-	M56.240-P	4208
CD74LPT16543	-	-	M56.300-P	-	M56.240-P	4209
CD74LPT16646	-	-	M56.300-P	-	M56.240-P	4210
CD74LPT16652	-	-	M56.300-P	-	M56.240-P	4211
CD74LPT16827	-	-	M56.300-P	-	M56.240-P	4212
CD74LPT16952	-	-	M56.300-P	-	M56.240-P	4213
CD74LPT241	-	M20.3-P	-	M20.15-P	-	4196
CD74LPT244	-	M20.3-P	-	M20.15-P	-	4197
CD74LPT245	-	M20.3-P	-	M20.15-P	-	4198
CD74LPT373	-	M20.3-P	-	M20.15-P	-	4199
CD74LPT541	-	M20.3-P	-	M20.15-P	-	4200
CD74LPT543	-	M24.3-P	-	M24.15-P	-	4256
CD74LPT573	-	M20.3-P	-	M20.15-P	-	4201
CD74LPT646	-	M24.3-P	-	M24.15-P	-	4257
CD74LPT652	-	M24.3-P	-	M24.15-P	-	4257
CD74LPT827	-	M24.3-P	-	M24.15-P	-	4258

Dual-In-Line Plastic Packages (PDIP)



E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

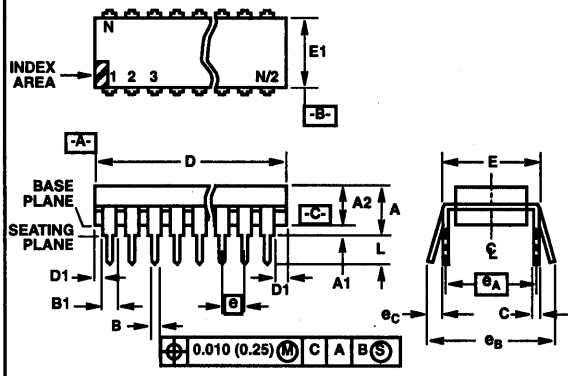
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E24.3 (JEDEC MS-001-AF ISSUE D)
24 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

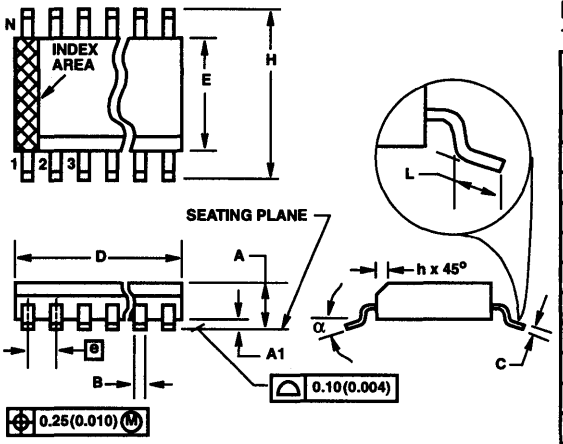
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	1.230	1.280	31.24	32.51	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	24		24		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Small Outline Plastic Packages (SOIC)



M14.15-P

14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

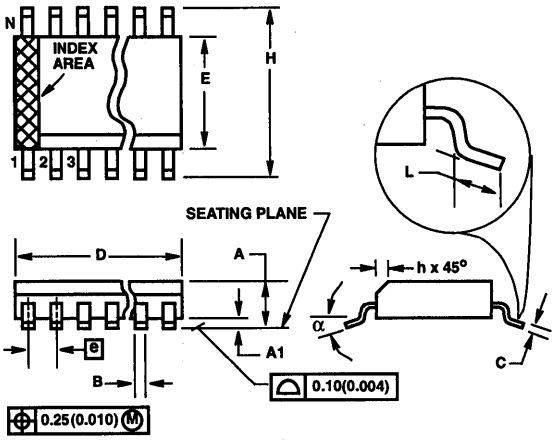
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.0040	0.0098	0.102	0.249	-
B	0.013	0.020	0.330	0.508	-
C	0.007	0.010	0.178	0.254	-
D	0.336	0.345	8.53	8.76	1
E	0.149	0.157	3.78	3.99	2
e	0.050 BSC		1.27 BSC		-
H	0.231	0.241	5.86	6.12	-
h	0.0099	0.0196	0.25	0.50	-
L	0.016	0.050	0.41	1.27	3
N	14		14		4
α	0^o	8^o	0^o	8^o	-

Rev. 0 6/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M16.15-P

16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

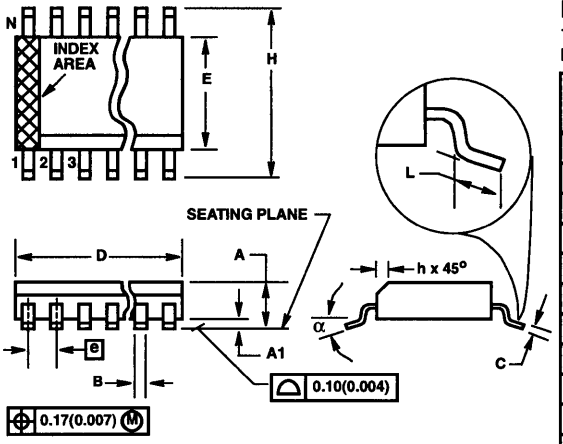
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.0040	0.0098	0.102	0.249	-
B	0.013	0.020	0.330	0.508	-
C	0.007	0.010	0.178	0.254	-
D	0.385	0.394	9.78	10.01	1
E	0.149	0.157	3.78	3.99	2
e	0.050 BSC		1.27 BSC		-
H	0.231	0.241	5.86	6.12	-
h	0.0099	0.0196	0.25	0.50	-
L	0.016	0.050	0.41	1.27	3
N	16		16		4
α	0^o	8^o	0^o	8^o	-

Rev. 0 6/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP/QSOP)



M16.15A-P

16 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

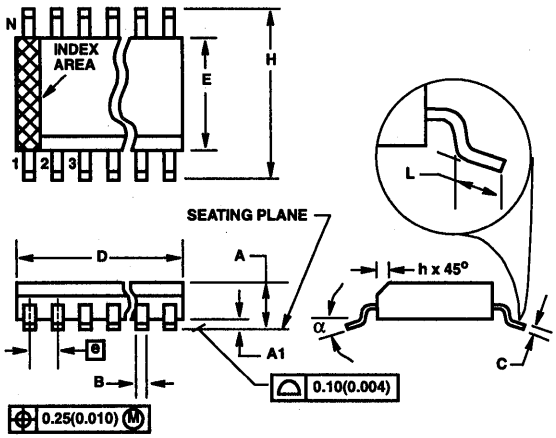
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.007	0.011	0.178	0.279	-
B	0.008	0.012	0.203	0.305	-
C	0.007	0.010	0.178	0.254	-
D	0.189	0.197	4.80	5.00	1
E	0.149	0.157	3.78	3.99	2
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.79	6.20	-
h	0.015		0.38		-
L	0.016	0.050	0.41	1.27	3
N	16		16		4
α	0^o	8^o	0^o	8^o	-

Rev. 2 7/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M16.3-P

16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

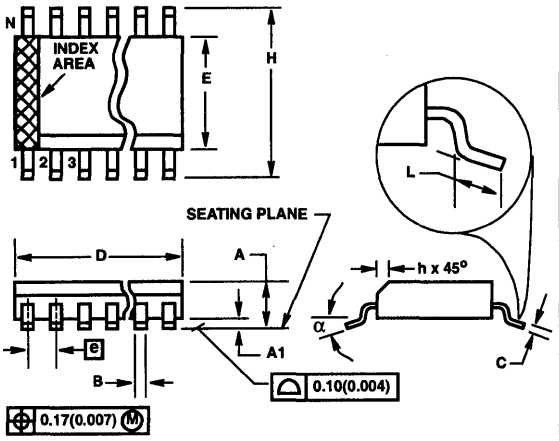
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.092	0.105	2.34	2.67	-
A1	0.004	0.012	0.102	0.302	-
B	0.013	0.020	0.330	0.508	-
C	0.009	0.011	0.229	0.279	-
D	0.397	0.413	10.08	10.49	1
E	0.291	0.299	7.39	7.59	2
e	0.050 BSC		1.27 BSC		-
H	0.401	0.411	10.18	10.44	-
h	0.010	0.029	0.254	0.737	-
L	0.016	0.050	0.41	1.27	3
N	16		16		4
α	0°	8°	0°	8°	-

Rev. 0 5/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP/QSOP)



M20.15-P

20 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

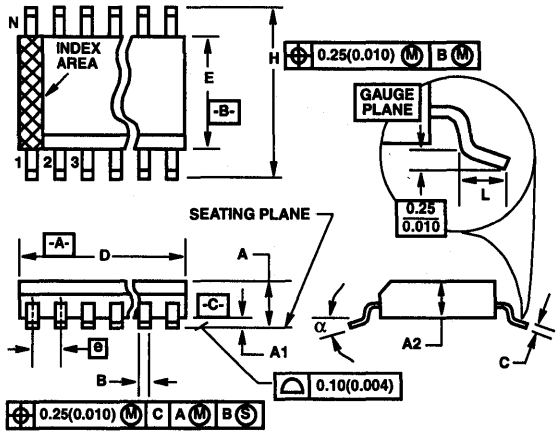
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.007	0.011	0.178	0.279	-
B	0.008	0.012	0.203	0.305	-
C	0.007	0.010	0.178	0.254	-
D	0.337	0.344	8.56	8.74	1
E	0.149	0.157	3.78	3.99	2
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.79	6.20	-
h	0.015		0.38		-
L	0.016	0.050	0.41	1.27	3
N	20		20		4
α	0°	8°	0°	8°	-

Rev. 1 7/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)



M20.209 (JEDEC MO-150-AE ISSUE B)
20 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

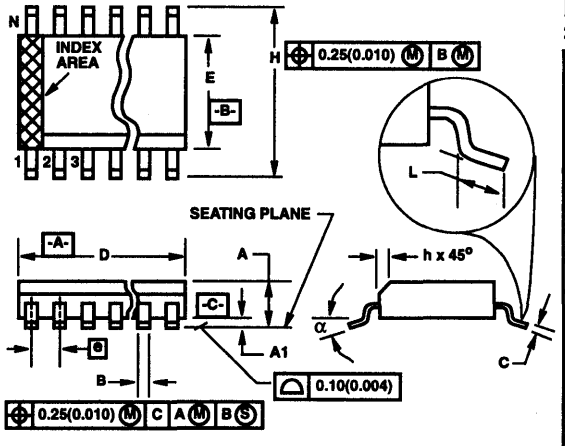
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.272	0.295	6.90	7.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 2 4/95

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

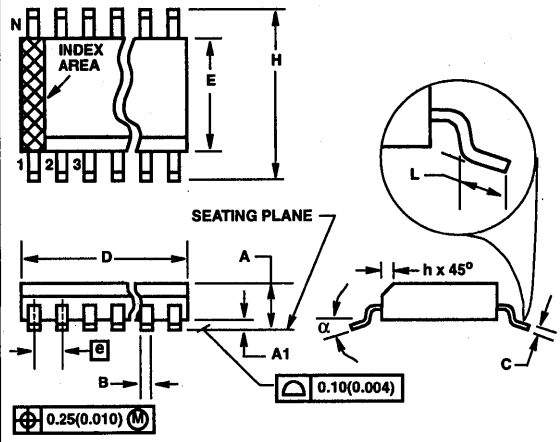
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M20.3-P

20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

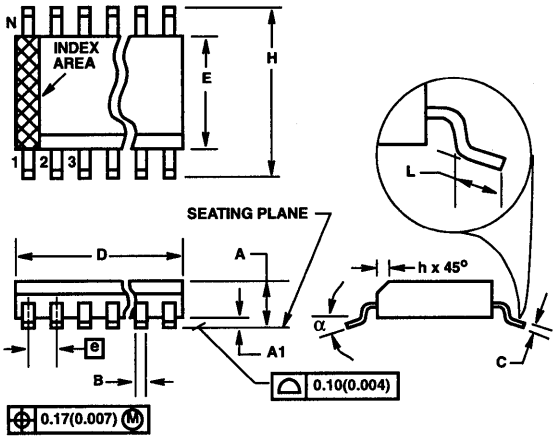
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.092	0.105	2.34	2.67	-
A1	0.004	0.012	0.102	0.302	-
B	0.013	0.020	0.330	0.508	-
C	0.009	0.011	0.229	0.279	-
D	0.496	0.512	12.60	13.00	1
E	0.291	0.299	7.39	7.59	2
e	0.050 BSC		1.27 BSC		-
H	0.401	0.411	10.18	10.44	-
h	0.010	0.029	0.254	0.737	-
L	0.016	0.050	0.41	1.27	3
N	20		20		4
α	0°	8°	0°	8°	-

Rev. 0 5/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP/QSOP)



M24.15-P

24 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

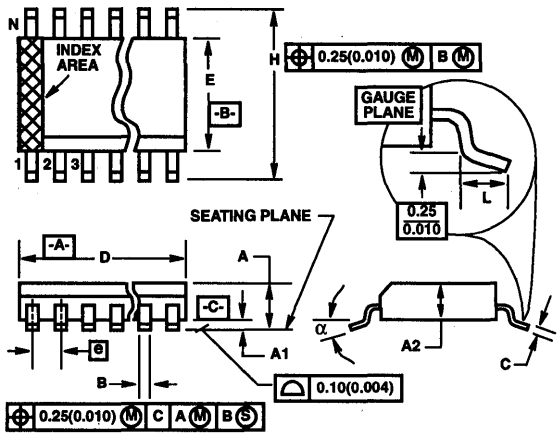
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.007	0.011	0.178	0.279	-
B	0.008	0.012	0.203	0.305	-
C	0.007	0.010	0.178	0.254	-
D	0.337	0.344	8.56	8.74	1
E	0.149	0.157	3.78	3.99	2
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.79	6.20	-
h	0.015		0.38		-
L	0.016	0.050	0.41	1.27	3
N	24		24		4
α	0°	8°	0°	8°	-

Rev. 1 7/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)



M24.209 (JEDEC MO-150-AG ISSUE B)
24 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

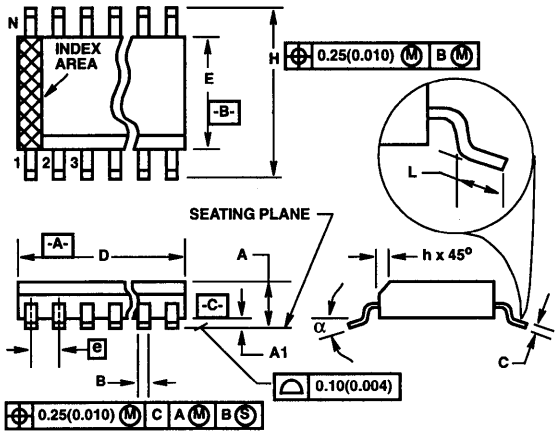
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.312	0.334	7.90	8.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	24		24		7
α	0°	8°	0°	8°	-

Rev. 1 3/95

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

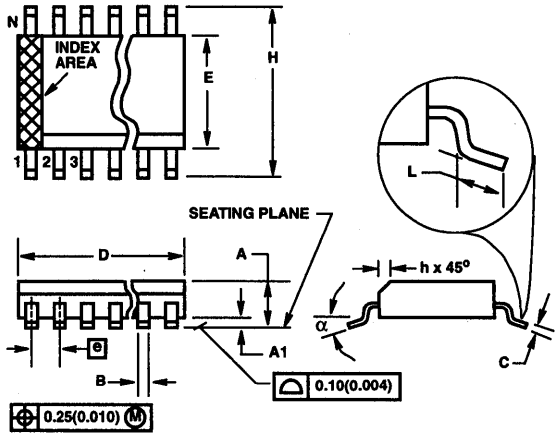
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M24.3-P

24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

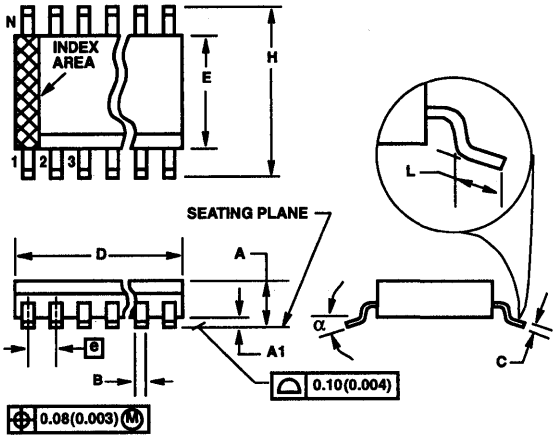
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.092	0.105	2.34	2.67	-
A1	0.004	0.012	0.102	0.302	-
B	0.013	0.020	0.330	0.508	-
C	0.009	0.011	0.229	0.279	-
D	0.598	0.614	15.19	15.60	1
E	0.291	0.299	7.39	7.59	2
e	0.050 BSC		1.27 BSC		-
H	0.401	0.411	10.18	10.44	-
h	0.010	0.029	0.254	0.737	-
L	0.016	0.050	0.41	1.27	3
N	24		24		4
α	0°	8°	0°	8°	-

Rev. 0 5/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Thin Shrink Small Outline Plastic Packages (TSSOP)



M48.240-P

48 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

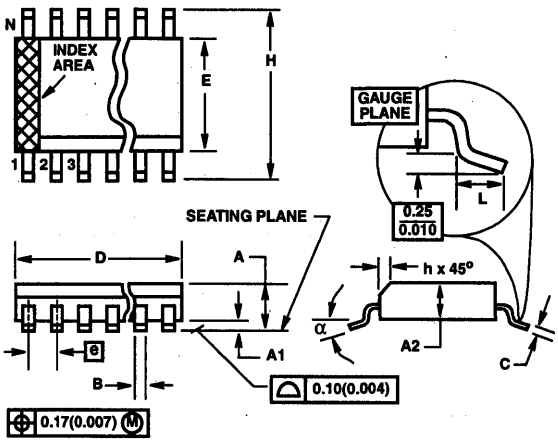
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.041	0.047	1.05	1.20	-
A1	0.002	0.006	0.05	0.15	-
B	0.007	0.010	0.178	0.254	-
C	0.004	0.008	0.102	0.203	-
D	0.488	0.496	12.40	12.59	1
E	0.236	0.244	6.00	6.19	2
e	0.0197 BSC		0.50 BSC		-
H	0.307	0.330	7.80	8.38	-
L	0.020	0.030	0.51	0.76	3
N	48		48		4
α	0°	8°	0°	8°	-

Rev. 0 6/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)



M48.300-P

48 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

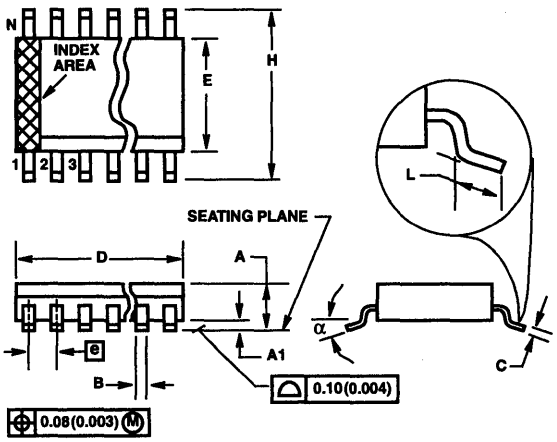
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.096	0.108	2.44	2.74	-
A1	0.008	0.016	0.20	0.41	-
A2	0.088	0.092	2.24	2.34	-
B	0.008	0.0135	0.20	0.34	-
C	0.005	0.010	0.13	0.25	-
D	0.620	0.630	15.75	16.00	2
E	0.291	0.299	7.39	7.59	3
e	0.025 BSC		0.635 BSC		-
H	0.395	0.415	10.03	10.54	-
h	0.015	0.025	0.381	0.635	-
L	0.020	0.040	0.51	1.01	4
N	48		48		5
α	0°	8°	0°	8°	-

Rev. 0 5/96

NOTES:

1. These package dimensions are within allowable dimensions of JECEC MO-118-AA, Issue B.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
3. Dimension "E" does not include interlead flash or protrusions.
4. "L" is the length of terminal for soldering to a substrate.
5. "N" is the number of terminal positions.
6. Terminal numbers are shown for reference only.
7. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Thin Shrink Small Outline Plastic Packages (TSSOP)



M56.240-P

56 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

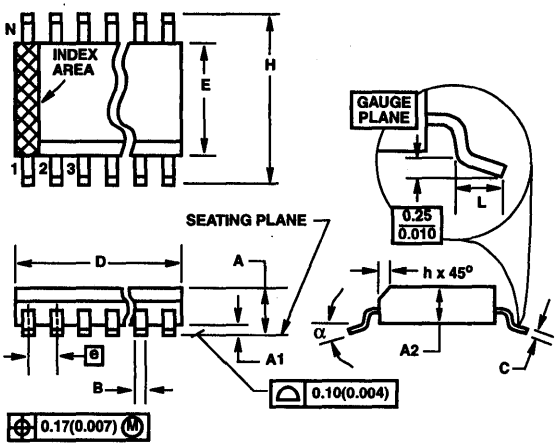
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.041	0.047	1.05	1.20	-
A1	0.002	0.006	0.05	0.15	-
B	0.007	0.010	0.178	0.254	-
C	0.004	0.008	0.102	0.203	-
D	0.547	0.555	13.90	14.09	1
E	0.236	0.244	6.00	6.19	2
e	0.0197 BSC		0.50 BSC		-
H	0.307	0.330	7.80	8.38	-
L	0.020	0.030	0.51	0.76	3
N	56		56		4
α	0°	8°	0°	8°	-

Rev. 0 6/96

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)



M56.300-P

56 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.096	0.108	2.44	2.74	-
A1	0.008	0.016	0.20	0.41	-
A2	0.088	0.092	2.24	2.34	-
B	0.008	0.0135	0.20	0.34	-
C	0.005	0.010	0.13	0.25	-
D	0.720	0.730	18.29	18.54	2
E	0.291	0.299	7.39	7.59	3
e	0.025 BSC		0.635 BSC		-
H	0.395	0.415	10.03	10.54	-
h	0.015	0.025	0.381	0.635	-
L	0.020	0.040	0.51	1.01	4
N	56		56		5
α	0°	8°	0°	8°	-

Rev. 0 5/96

NOTES:

1. These package dimensions are within allowable dimensions of JECEC MO-118-AB, Issue B.
2. Dimension "D" does not include mold flash, protrusions or gate burrs.
3. Dimension "E" does not include interlead flash or protrusions.
4. "L" is the length of terminal for soldering to a substrate.
5. "N" is the number of terminal positions.
6. Terminal numbers are shown for reference only.
7. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

CMOS LOGIC 12

HARRIS' ON-LINE SERVICES

PAGE

See Us on the Net 12-3

How to Use Harris AnswerFAX 12-4

Your Map to Harris AnswerFAX 12-5

Harris AnswerFAX Data Book Request Form - Document #199 12-6

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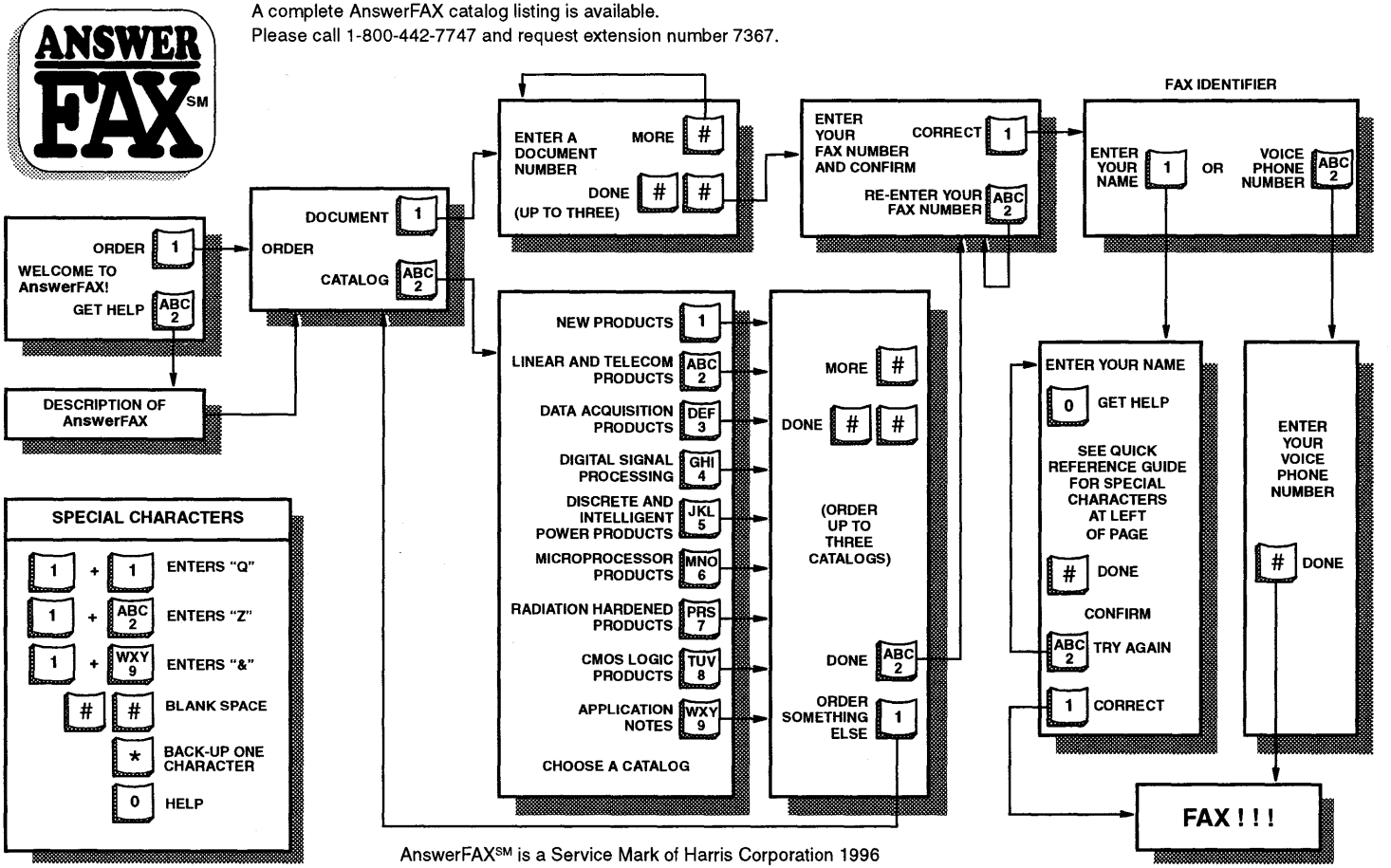

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FAX: (407) 290-0164

Elmo Semiconductor Corp.
7590 North Glenoaks Blvd.
Burbank, CA 91504-1052
TEL: (818) 768-7400
FAX: (818) 767-7038

Minco Technology Labs, Inc.
1805 Rutherford Lane
Austin, TX 78754
TEL: (512) 834-2022
FAX: (512) 837-6285

Puerto Rican Authorized Distributor

Hamilton Hallmark
Suite 318
S1 Mariolga Luis Munoz-Marin
Caguas, Puerto Rico 00725
TEL: (800) 327-8950

South American Authorized Distributor

Graftec Electronic Sales Inc.
One Boca Place, Suite 305 East
2255 Glades Road
Boca Raton, Florida 33431
TEL: (407) 994-0933
FAX: 407 994-5518

BRASIL

Graftec Brasil Ltda.
Rua Baronesa de Itu,
336 cj. 51/52 Sao Paulo - SP
CEP: 01231-000
TEL: 55-11-826-1666
FAX: 55-11-826-6526

North American Authorized Distributors and Corporate Offices

Hamilton Hallmark and Zeus are the only authorized North American distributors for stocking and sale of Harris Rad Hard Space products.

Alliance Electronics
(SAB Status)
7550 E. Redfield Rd.
Scottsdale, AZ 85260
TEL: (602) 483-9400
(800) 608-9494
FAX: (602) 443 3898

Allied Electronics
7410 Pebble Dr.
Ft. Worth, TX 76118
TEL: (800) 433-5700

Arrow/Schweber Electronics
25 Hub Dr.
Melville, NY 11747
TEL: (800) 777-2776

Bell Microproducts
1941 Ringwood Avenue
San Jose, CA 95131
TEL: (408)451-9400
FAX: (408)451-1600

Electronics Marketing Corporation (EMC)
1150 West Third Avenue
Columbus, OH 43212
TEL: (614) 299-4161
FAX: 614 299 4121

Farnell Electronic Services
300 North Rivermede Rd.
Concord, Ontario
Canada L4K 3N6
TEL: (416) 798-4884
FAX: 416 798 4889

Gerber Electronics
128 Carnegie Row
Norwood, MA 02062
TEL: (617) 769-6000, x156
FAX: 617 762 8931

Hamilton Hallmark
10950 W. Washington Blvd.
Culver City, CA 90230
TEL: (800) 332-8638

Newark Electronics
4801 N. Ravenswood
Chicago, IL 60640
TEL: (312) 784-5100
(800) 367-3673
FAX: 312 275-9596

Wyle Electronics
(Commercial Products)
3000 Bowers Avenue
Santa Clara, CA 95051
TEL: (800) 414-4144
FAX: 801 226-0210

Zeus Electronics, An Arrow Company
2900 Westchester Avenue
Purchase, NY 10577
TEL: (800) 524-4735

Obsolete/Discontinued Products:

Rochester Electronics
10 Malcom Hoyt Drive
Newburyport, MA 01950
TEL: (508) 462-9332
FAX: 508 462 9512

* Field Application Assistance Available

European Sales Offices, Representatives and Authorized Distributors

European Sales Headquarters

Harris Semiconductor
Mercure Center
Rue de la Fusee 100
B-1130 Brussels, Belgium
TEL: 32 2 724 21 11
FAX: 32 2 724 2205/...09

AUSTRIA

Avnet E2000
Waidhausenstrasse 19
A - 1140 Vienna
TEL: 43 1 911 28 47
FAX: 43 1 911 38 53

EBV Elektronik
* Diefenbachgasse 35
A - 1150 Vienna
TEL: 43 1 89 41 774
FAX: 43 1 89 41 775

Spoerle Electronic
Heiligenstädter 52
A - 1190 Vienna
TEL: 43 1 318 7270-0
FAX: 43 1 369 22 73

BELGIUM

EBV Spoerle Electronic
* Keiberg II
Minervastraat, 14/B2
B-1930 Zaventem
TEL: 32 2 725 46 60
FAX: 32 2 725 45 11

EBV Elektronik
* Excelsiorlaan 35B
B - 1930 Zaventem
TEL: 32 2 716 00 10
FAX: 32 2 720 81 52

DENMARK

Arrow-Exatec A/S
Mileparken 20E
DK-2740 Skovlunde
TEL: 45 4492 7000
FAX: 45 4492 6020

Avnet Nortec A/S
Transformervej, 17
DK - 2730 Herlev
TEL: 45 4488 0800
FAX: 45 4488 0888

EBV Elektronik
Ved Lunden 9
DK - 8230 Abyhoj
TEL: 45 86 25 04 66
FAX: 45 86 25 06 60

EBV Elecktronik
Gladsaxevej 370
DK - 2860 Soborg
TEL: 45 39 69 05 11
FAX: 45 39 69 05 04

Independent Electronic Components
Poppelskellet 2
DK-2000 Frederiksberg
TEL: 45 3645 1206
FAX: 45 3645 1205

EASTERN COUNTRIES

GRADER Friedhelm
Richard-Reitzner-Allee 4
G-85540 Haar
TEL: 49 89 46263-0

Spoerle Electronic
Charkovska 24
CZ-10100 Praha 10
Czechoslovakia
TEL: 42 2 73 13 54
FAX: 42 2 73 13 55

Spoerle Elektronik
ul. Domaniewska 41
PL-02672 Warszawa
Poland
TEL: 48 22 64 00 447
FAX: 48 22 64 00 348

FINLAND

Arrow Field OY
Niittylantie 5
FIN-00620 Helsinki
TEL: 358 9 777 571
FAX: 358 9 798 853

Avnet Nortec OY
Italahdenkatu, 18
FIN-00210 Helsinki
TEL: 358 9 61 31 81
FAX: 358 9 69 22 32 6

EBV Electronics
Pihatorma 1A
SF - 02240 Espoo
TEL: 358 9 855 77 30
358 9 855 77 90
FAX: 358 9 855 04 50

Harcomp Electronics OY
Syvalahdentie 79
SF - 51200 Kangasniemi
TEL: 358 59 432031
FAX: 358 59 432367

FRANCE

Harris Semiconducteurs
* 2-4, Avenue de l'Europe
F - 78941 Velizy Cedex
TEL: 33 1 34 65 40 80 (Dist)
TEL: 33 1 34 65 40 00(Sales)
FAX: 33 1 39 46 40 54

Arrow Electronique
73 - 79, Rue des Solets
Silic 585
F - 94663 Rungis Cedex
TEL: 33 1 49 78 49 78
FAX: 33 1 49 78 06 99

Avnet EMG
* 79, Rue Pierre Semard
P.B. 90
F-92322 Chatillon Sous Bagneux
TEL: 33 1 49 65 27 00
FAX: 33 1 49 65 25 39

CCI Electronique
* 12, Allee de la Vierge
Silic 577
F - 94653 Rungis
TEL: 33 1 41 80 70 00
FAX: 33 1 46 75 32 07

EBV Elektronik
3 rue del la Renaissance
92184 Antony cedex
TEL: (33) 1 40 96 30 00
FAX: (33) 1 40 96 30 30

SEI/3D
Z.I. des Glaises
6/8 Rue Ambroise Croizat
F - 91127 Palaiseau
TEL: 33 1 64 47 29 29
FAX: 33 1 64 47 00 84

GERMANY

Harris Semiconductor
* Richard-Reitzner-Allee 4
D-85540 Haar
TEL: 49 89 462 63 0
FAX: 49 89 462 63 133

Harris Semiconductor
Kieler Strasse 55-59
D-25451 Quickborn
TEL: 49 4106 50 02-04
FAX: 49 4106 6 88 50

Harris Semiconductor
Kolumbusstrasse 35/1
D - 71063 Sindelfingen
TEL: 49 7031 8 69 40
FAX: 49 7031 87 38 49

Ecker Michelstadt
In den Dorfwiesen 2A
Postfach 33 44
D - 64720 Michelstadt
TEL: 49 6061 22 33
FAX: 49 6061 50 39

Erwin W. Hildebrandt
Nieresch 32
D - 48301 Nottuln-Darup
TEL: 49 2502 2300 30
FAX: 49 2502 2300 18

FINK Handelsvertretung
Laurinweg, 1
D - 85521 Ottobrunn
TEL: 49 89 609 7004
FAX: 49 89 609 8170

Hans Flogel
Kielerstrasse 31b
D-25451 Quickborn
TEL: 49 4106 50502 07
FAX: 49 4106 68850

Hartmut Welte
* Traubenweg 7
D - 88048 Friedrichshafen
TEL: 49 7544 72555
FAX: 49 7544 72559

Avnet/E2000
* Stahlgruberring, 12
D - 81829 München
TEL: 49 89 4511001
FAX: 49 89 45110129

EBV Elektronik
* Ammerthalstrasse 28
D-85551 Kirchheim-Heimstetten
TEL: 49 89 99 11 40
FAX: 49 89 99 11 44 22

Indeg Industrie Elektronik
Emil Kömmerling Strasse 5
D - 66954 Pirmasens
Postfach 1563
D - 66924 Pirmasens
TEL: 49 6331 51700
FAX: 49 6331 9 40 64

Sasco Semiconductor GmbH
* Hermann-Oberth Strasse 16
D - 85640 Putzbrunn
TEL: 49 89 46 11-0
FAX: 49 89 46 11-270

Spoerle Electronic
* Max-Planck Strasse 1-3
D - 63303 Dreieich-bei-Frankfurt
TEL: 49 6103 304-8
FAX: 49 6103 304 201

GREECE

EBV Electronik
Anaxagora Street 1
GR-17778 Travros (Athens)
TEL: 30 1 34 14 300
FAX: 30 1 34 14 304

Semicon
104 Aeolou Street
GR - 10564 Athens
TEL: 30 1 32 53 626
FAX: 30 1 32 16 063

ISRAEL

Aviv Electronics
Hayetzira Street, 4 Ind. Zone
IS - 43651 Ra'anana
PO Box 2433
IS - 43100 Ra'anana
TEL: 972 9 748 3232
FAX: 972 9 741 6510

ITALY

Harris Semiconductor
* Viale Fulvio Testi, 126
I-20092 Cinisello Balsamo, (Milan)
TEL: 39 2 262 22 21 31 (Italy)
TEL: 39 2 262 07 61 (Rose)
FAX: 39 2 262 22 158 (Rose)

Claitron
Via Enrico Fermi, 8
I - 20090 Assago (MI)
TEL: 39 2 457 841
FAX: 39 2 488 02 75

HARRIS SEMICONDUCTOR

* Field Application Assistance Available

European Sales Offices, Representatives and Authorized Distributors (Continued)

Avnet EMG
Centro Direzionale
Via Novara, 570
I - 20153 Milano
TEL: 39 2 38 19 01
FAX: 39 2 38 00 29 88

EBV Elektronik
* Via C. Frova, 34
I - 20092 Cinisello Balsamo
TEL: 39 2 660 96 290
FAX: 39 2 660 170 20

FG Microdesign
Via A. Simoni 5
I-4001 Anzola Dell'Emilia
TEL: 39 51 73 20 95
FAX: 39 51 73 24 91

Lasi Elettronica
Viale Fulvio Testi 280
I - 20126 Milano
TEL: 39 2 661 431
FAX: 39 2 661 01385

Silverstar
Viale Fulvio Testi 280
I - 20126 Milano
TEL: 39 2 66 12 51
FAX: 39 2 66 10 13 59

NETHERLANDS

Acal
* Beatrix de Rijkweg, 8
NL - 5657 EG Eindhoven
TEL: 31 40 250 2602
FAX: 31 40 251 0255

Spoerle Electronic
* Coltbaan 17
NL - 3439 NG Nieuwegein
(Utrecht)
TEL: 31 30 609 1234
FAX: 31 30 603 5924

Spoerle Electronic
Postbus 7139
De Run 1120
NL - 5605 JC Eindhoven
TEL: 31 40 254 5430
FAX: 31 40 253 5540

EBV Elektronik
* Planetenbaan, 2
NL - 3606 AK Maarssenbroek
TEL: 31 346 58 30 10
FAX: 31 346 58 30 25

NORWAY

Arrow-Tahonic
Sagveien 17
P.O. Box 4554, Torshov
N-0404 Oslo
TEL: 47 22 37 84 40
FAX: 47 22 37 07 20

Avnet Nortec A/S
Box 123
N - 1364 Hvalstad
TEL: 47 66 84 62 10
FAX: 47 66 84 65 45

PORTUGAL

Amitron-Arrow
Quinta Grande, Lote 20
Alfragide
P - 2700 Amadora
TEL: 351.1.471 48 06
FAX: 351.1.471 08 02

SOUTH AFRICA

Allied Electronic Components
10, Skietlood Street
Isando, Ext. 3, 1600
P.O. Box 69
Isando, 1600
Transvaal
TEL: 27 11 392 3804/. . .19
FAX: 27 11 974 9625
FAX: 27 11 974 9683

SPAIN

Elcos
c/Avda Europa, 30 1 B-A
SP 28224 Pozuelo de
Alarcon/Madrid
TEL: 34 1 352 3052
FAX: 34 1 352 1147

Amitron-Arrow
Albasanz, 75
SP - 28037 Madrid
TEL: 34 1 304 30 40
FAX:34 1 327 24 72

EBV Elektronik
* Centro Empresarial Euronova
Ronda de Poniente,
4 Ala Derecha
1A Planta, Officina A
SP - 28760 Tres Cantos
Madrid
TEL: 34 1 8 04 32 56
FAX: 34 1 8 04 41 03

SWEDEN

Harris Semiconductor
Centralvagen, 12
S - 171 44 Solna
TEL: 46 8 270 660
FAX: 46 8 270 656

Arrow TH:s
Box 3027
Arrendevagen 36
S - 16303 Spanga
TEL: 46 8 36 29 70
FAX: 46 8 761 30 65

Avnet Nortec AB
Englundavagen 7
P.O. Box 1830
S - 171 27 Solna
TEL: 46 8 629 1400
FAX: 46 8 627 0280

SWITZERLAND

Avnet E2000
Boehirainstrasse 11
CH - 8801 Thalwil
TEL: 41 1 7221330
FAX: 41 1 7221340

Basix
Hardturmstrasse 181
CH - 8010 Zürich
TEL: 41 1 2 76 11 11
FAX: 41 1 2761234

EBV Elektronik
* Vorstadtstrasse 37
CH - 8953 Dietikon
TEL: 41 1 740 10 90
FAX: 41 1 741 51 10

Guidici Mauro O&T GmbH
Florastr 34
CH-8610 Uster
TEL: 41 1 9943290
FAX: 41 1 9943291

Spoerle Electronic
Cherstrasse 4
CH-8152 Opfikon-Glattbrugg
TEL: 41 1 874 6262
FAX: 41 1 874 6200

TURKEY

EBV Electronik
Bayar Cad. Gulbahar Sok No 17
Perdemsac Plaza D:131-132
TK-81090 Kazyatagl/Istanbul
TEL: 90 216 463 1352/3
FAX: 90 216 463 1355

EMPA
Besyol Londra Asfalti
TK - 34630 Sefakoy/Istanbul
TEL: 90 212 599 3050
FAX: 90 212 599 3059

UNITED KINGDOM

Harris Semiconductor
* Riverside Way
Watchmoor Park
Camberley
Surrey GU15 3YQ
TEL: 44 1276 686 886
FAX: 44 1276 682 323

Laser Electronics
Ballynamoney
Greenore
Co. Louth, Ireland
TEL: 353 4273165
FAX: 353 4273518

Complementary Technologies
Redgate Road
South Lancashire, Ind. Estate
Ashton-In-Makerfield
Wigan, Lancs WN4 8DT
TEL: 44 1942 274 731
FAX: 44 1942 274 732

Stuart Electronics
Phoenix House
Bothwell Road
Castlehill, Carluke
Lanarkshire ML8 5UF
TEL: 44 1555 751572
FAX: 44 1555 750028

Arrow Jermyn
St Martins Business Centre
Cambridge Road
Bedford MK42 0LF
TEL: 44 1234 270027
FAX: 44 1234 214674

Avnet Access
Jubilee House
Jubilee Road
Letchworth
Hertfordshire SG6 1QH
TEL: 44 1462 480888
FAX: 44 1462 488567

EBV Elektroik
EBV House
7 Frascati Way
Maidenhead
Berkshire SL6 4UY
TEL: 44 1628 783 688
FAX: 44 1628 783 811

Farnell Components
Sales, Mktg & Admin Center
Canal Road, Armley
Leeds LS12 2TU
TEL: 44 1132 790101
FAX: 44 1132 633404

Farnell Electronic Services
Edinburgh Way.
Harlow
Essex CM20 2DF
TEL: 44 1279 626777
FAX: 44 1279 441687

IEC Micromark Electronics
Boyn Valley Road
Maidenhead
Berkshire SL6 4DT
TEL: 44 1628 76176
FAX: 44 1628 783799

Harris Semiconductor Chip Distributors

Die Technology
Corbrook Rd., Chadderton
Lancashire OL9 9SD
TEL: 44 61 626 3827
FAX: 44 61 627 4321
TWX: 668570

Rood Technology
Test House Mill Lane, Alton
Hampshire GU34 2QG
TEL: 44 420 88022
FAX: 44 420 87259
TWX: 21137

* Field Application Assistance Available

Asian Pacific Sales Offices, Representatives and Authorized Distributors

AUSTRALIA

Avnet VSI Electronics Pty Ltd.
Unit C 6-8 Lyon Park Road
North Ryde NSW 2113
TEL: (612) 878-1299
FAX: (612) 878-1266

BBS Electronics Australia
Unit 24, 5-7 Anella Avenue,
Castle Hill, NSW, 2154
PO Box 6686
Baulkham Hills, NSW, 2153
TEL: 612-8945244
FAX:612-8945266

CHINA/HONG KONG

Harris Semiconductor China Ltd
* Room 3005 88 Tong Ren Road
Shanghai, 20040 China
TEL: 86-21-6247-7923
FAX: 86-21-6247-7926

Harris Semiconductor China Ltd.
* Unit 1801-2, 18th Floor
83 Austin Road
Tsimshatsui, Kowloon
TEL: (852) 2723-6339
FAX: (852) 2724-4369

Edal Electronics Co., Ltd.
Room 911-913, Chevalier
Commercial Centre,
8, Wang Hoi Road,
Kowloon Bay, Kowloon
TEL: (852) 2305-3863
FAX: (852) 2759-8225

Lucas Trading
Unit A, 8F
88 Hung To Road, Kwun Tong
Kowloon, Hong Kong
TEL: 852-3044023
FAX: 852-3040065

Means Come Ltd.
Room 1007, Harbour Centre
8 Hok Cheung Street
Hung Hom, Kowloon
TEL: (852) 2334-8188
FAX: (852) 2334-8649

Sunnice Electronics Co., Ltd.
Flat F, 5/F, Everest Ind. Cir.
396 Kwun Tong Road
Kowloon
TEL: (852) 2790-8073
FAX: (852) 2763-5477

Array Electronics Limited
24/F Wyler Centre, Phase 2
200 Tai Lin Pai Road
Kwai Chung
New Territories, Hong Kong
TEL: (852) 2418-3700
FAX: (852) 2481-5872

Inchcape Industrial
10/F, Tower 2, Metroplaza
223 Hing Fong Road,
Kwai Fong
New Territories, Hong Kong
TEL: 852-2410-6555
FAX: 852-2401-2497

Kingly International Co., Ltd.
Flat 03, 16/F, Block A,
Hi-Tech Ind. Centre
5-21 Pak Tin Par St.,
Tsuen Wan, New Territories, H.K.
TEL: (852) 2499-3109
FAX: (852) 2417-0961

INDIA

Intersil Private Limited
Plot 54, SEEPZ
Marol Industrial Area
Andheri (E) Bombay 400 096
TEL: (91) 22-832-3097
FAX: (91) 22-836-6682

Graftec Elec
49 J.C. Road
Bangalore 560002
TEL: (91) 80 223 3346
FAX: (91) 80 222 6490

Graftec India
No 143 Lakshmi Building
R.V. Road, V.V. Puram
Bangalore 560004
Karnataka
TEL: (91) 80-661 1095
FAX: (91) 80-222 6490

BBS Electronics (India) Pvt Ltd
309 Richmond Tower
No 12, Richmond Road
Bangalore 560025
TEL: (91) 80-221-7912
FAX: (91) 80-227 8043

S M Creative Electronics Ltd
10 Electronic City
Sector 18, Gurgaon 122015
Haryana
TEL: 91 124 342 137/237/1551
FAX: 91 124 236 or
91 11 622 8474

INDONESIA

P.T. Silicontama Jaya
Jalan A.M. Sangaji No 15 B4
Jakarta Pusat
TEL: (62) 21-345 4050
FAX: (62) 21-345 4427

SELC Sumber Elektronic
JL Jend A Yani #298,
Bandung 40271
TEL: (62) 22-706-056
FAX: (62) 22-703-622

JAPAN

Harris K.K.
* Kojimachi-Nakata Bldg. 4F
5-3-5 Kojimachi
Chiyoda-ku, Tokyo, 102 Japan
TEL: (81) 3-3265-7571
FAX: (81) 3-3265-7575

Hakuto Co., Ltd.
1-1-13 Shinjuku Shinjuku-ku
Tokyo 160
TEL: 81-3-3355-7615
FAX: 81-3-3355-7680

Jepico Corp.
Shinjuku Daiichi Seimei Bldg.
2-7-1, Nishi-Shinjuku
Shinjuku-ku, Tokyo 163
TEL: 81 3-3348-0611
FAX: 81 3-3348-0623

Macnica Inc.
Hakusan High Tech Park
1-22-2, Hakusan
Midori-ku, Yokohama-shi,
Kanagawa 226
TEL: 81 45-939-6116
FAX: 81 45-939-6117

Micron, Inc.
DJK Kouenji Bldg. 5F
4-26-16, Kouenji-Minami
Suginami-Ku, Tokyo 166
TEL: 81-3-3317-9911
FAX: 81-3-3317-9917

Okura Electronics Co., Ltd.
Okura Shoji Bldg.
2-3-6, Ginza Chuo-ku,
Tokyo 104
TEL: 81 3-3564-6822
FAX: 81 3-3564-6870

Takumi Shoji Co
3 Maruzen Bld, 6F
6-16-6 Nishi Shinjuku,
Shinjuku-Ku, Tokyo 160
TEL: 813-3343-9605
FAX: 813-3343-9624

AUTOMOTIVE REP/DISTRI

Continental Far East Inc.
3-1-5 Azabudai
Minatoki, Tokyo 106
TEL: 81-3-3584-0339
FAX: 81-3-3588-0930

Mitsuiwa Shoji Co., Ltd.
Namikibashi Bldg.
3-15-8 Shibuya
Shibuya-Ku, Toyko 150
TEL: 81 3-3407-2181
FAX: 81 3-3407-1472

Nissei Electronics Ltd.
Hitachi Atago Bldg.
2-15-12 Nishi-Shimbashi
Minato-Ku, Tokyo 105
TEL: 81 3-3504-7921
FAX: 81 3-3504-7900

KOREA

Harris Semiconductor YH
* RM #419-1
Korea Air Terminal Bldg.
159-6, Sam Sung-Dong,
Kang Nam-ku, Seoul
135-728, Korea
TEL: 82-2-551-0931
FAX: 82-2-551-0930

H.B. Corporation
Rm #1409,
Seocho World Officetel,
1355-3, Seocho-Dong,
Seocho-Ku, Seoul 137-020
TEL: 82-2-3472-3450
FAX: 82-2-3472-3458

Graftec Korea
Room #611, Yongsan
Electronic Offetel, 16-548
3-Ga Hankang-Ro,
Youngsan-Gu, Seoul
TEL: 822-715-8857
FAX: 822-715-8859

Inhwa Company, Ltd.
Room #305, Daegyo Bldg., 56-4,
Wonhyoro 3GA,
Young San-Ku, Seoul 140-113
TEL: 822-703-7231
FAX: 822-703-8711

Kumoh Electric Co., Ltd.
203-1, Yoido-Dong,
Young Duing Po-Ku, Seoul
TEL: 822-782-9393
FAX: 822-782-9388

Segyung Techcell Co., Ltd.
Dansan Nonhyun Bldg., 270-45
Nonhyun-Dong,
Kangnam-Ku, Seoul 135-010
TEL: 822-515-7477
FAX: 822-515-8889

MALAYSIA

BBS Electronics (M) Sdn Bhd
Lot 2-01, Wisma Denko
41, Lorong Adu Siti
10400 Penang
TEL: (604) 228 0433
FAX: (604) 228 1710

NEW ZEALAND

Arrow Components (NZ) Limited
19 Pretoria Street
PO Box 31186
Lower Hut
TEL: (64) 4 570 2260
FAX: (64) 4 566 2111

HARRIS SEMICONDUCTOR

* Field Application Assistance Available

Asian Pacific Sales Offices, Representatives and Authorized Distributors (Continued)

PHILIPPINES
Uraco Technologies Philippines Inc.
Unit 12A/310 Project J.P. Rizal St. Project 4
Quezon City, 1109
TEL: (632) 922 2250
FAX: (632) 922 8709

SINGAPORE
Harris Semiconductor Pte Ltd.
* #1, Tannery Road 09-01
Cencon 1, Singapore 347719
TEL: 65-748-4200
FAX: 65-748-0400

BBS Electronics Pte, Ltd.
1 Genting Link
#05-03 Perfect Indust. Bldg.
Singapore 1334
TEL: (65) 748-8400
FAX: (65) 748-8466

TAIWAN
Harris Semiconductor
* Room 823, N. 144, Sec. 3
Ming Chuan East Road
Taipei 10464, Taiwan, R.O.C.
TEL: (886) 2-716-9310
FAX: (886) 2-715-3029

Applied Component Tech. Corp.
8F No. 233-1, Pao-Chia Road
Hsin Tien City, Taipei Hsien,
Taiwan, R.O.C.
TEL: (886) 2 9170858
FAX: (886) 2 9171895

Galaxy Far East Corporation
8F-6, No. 390, Sec. 1
Fu Hsing South Road
Taipei, Taiwan
TEL: (886) 2-705-7266
FAX: (886) 2-708-7901

TECO Enterprise Co., Ltd.
10FL., No. 292, Min-Sheng W. Rd.
Taipei, Taiwan
TEL: (886) 2-555-9676
FAX: (886) 2-558-6006

THAILAND
Electronics Source Co., Ltd.
138 Banmoh Rd.
Pranakorn, Bankok 10200
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