1995

Signal Processing New Releases

OP-AMPS
A/D CONVERTERS
D/A CONVERTERS
INTERFACE
SWITCHES/MUXES
DSP PRODUCTS
TELECOM
SPECIAL CIRCUITS

HARRIS

DB
314

Linear, Telecom, Data Acquisition, DSP

Signal Processing New Releases

1995

OP-AMPS
A/D CONVERTERS
D/A CONVERTERS
INTERFACE
SWITCHES/MUXES
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HARRIS
SEMICONDUCTOR

$5.00

HARRIS
SEMICONDUCTOR

HARRIS SEMICONDUCTOR

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See Section 15 for Datasheets Available on AnswerFAX
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HARRIS SEMICONDUCTOR

SIGNAL PROCESSING NEW RELEASES

FOR COMMERCIAL APPLICATIONS

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SIGNAL PROCESSING NEW RELEASES

1

GENERAL INFORMATION

Alpha Numeric Product Index

NOTE: Bold Type Designates a New Product from Harris.

Alpha Numeric Product Index (Continued)

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Alpha Numeric Product Index (Continued)

		95 NEW RELEASES DB314	94 DAQ DB301B	94 DSP DB302B	93 LIN DB500B
HI-507A	16 Channel, 8 Channel, Differential 8 and Differential 4 Channel CMOS Analog MUXs with Active Overvoltage Protection	-	10-95	-	-
HI-508	Single 16 and 8/Differential 8 and 4 Channel CMOS Analog Multiplexers	-	10-78	-	-
HI-508A	16 Channel, 8 Channel, Differential 8 and Differential 4 Channel CMOS Analog MUXs with Active Overvoltage Protection	-	10-95	-	-
HI-509	Single 16 and 8/Differential 8 and 4 Channel CMOS Analog Multiplexers	-	10-78	-	-
HI-509A	16 Channel, 8 Channel, Differential 8 and Differential 4 Channel CMOS Analog MUXs with Active Overvoltage Protection	-	10-95	-	-
HI-516	16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer	-	10-109	-	-
HI-518	8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer	-	10-116	-	-
HI-524	4 Channel Wideband and Video Multiplexer.................	-	10-123	-	-
HI-539	Monolithic, 4 Channel, Low Level, Differential Multiplexer.......	-	10-129	-	-
HI-546	Single 16 and 8, Differential 8 and 4 Channel CMOS Analog MUXs with Active Overvoltage Protection	-	10-140	-	-
HI-547	Single 16 and 8, Differential 8 and 4 Channel CMOS Analog MUXs with Active Overvoltage Protection	-	10-140	-	-
HI-548	Single 16 and 8, Differential 8 and 4 Channel CMOS Analog MUXs with Active Overvoltage Protection	-	10-140	-	-
HI-549	Single 16 and 8, Differential 8 and 4 Channel CMOS Analog MUXs with Active Overvoltage Protection	-	10-140	-	-
HI-562A	12-Bit High Speed Monolithic D/A Converter	(AnswerFAX Only) Document # 3580			
HI-565A	High Speed Monolithic D/A Converter with Reference..........	-	8-42	-	-
HI-574A	Complete 12-Bit A/D Converter with Microprocessor Interface ...	-	5-34	-	-
HI-674A	Complete 12-Bit A/D Converter with Microprocessor Interface ...	-	5-34	-	-
HI-774	Complete 12-Bit A/D Converter with Microprocessor Interface ...	-	5-34	-	-
HI-1818A	Low Resistance, Single 8 Channel and Differential 4 Channel CMOS Analog Multiplexers.............................	-	10-70	-	-
HI-1828A	Low Resistance, Single 8 Channel and Differential 4 Channel CMOS Analog Multiplexers.............................	-	10-70	-	-
HI1166	8-Bit, 250 MSPS Flash A/D Converter	-	6-43	-	-
HI1171	8-Bit, 40 MSPS High Speed D/A Converter	-	8-57	-	-
HI1175	8-Bit, 20 MSPS Flash A/D Converter	-	7-3	-	-
HI1176	8-Bit, 20 MSPS Flash A/D Converter	-	7-12	-	-
HI1179	**8-Bit, 35 MSPS Video A/D Converter**......................	4-3	-	-	-
HI1276	8-Bit, 500 MSPS Flash A/D Converter	-	6-54	-	-
HI1386	8-Bit, 75 MSPS Flash A/D Converter	-	6-64	-	-
HI1396	8-Bit, 125 MSPS Flash A/D Converter	-	6-72	-	-
HI3050	**10-Bit, 50 MSPS High Speed 3-Channel D/A Converter**	5-3	-	-	-
HI-5040	CMOS Analog Switches	-	9-110	-	-
HI-5041	CMOS Analog Switches	-	9-110	-	-
HI-5042	CMOS Analog Switches	-	9-110	-	-

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Alpha Numeric Product Index (Continued)

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Product Index by Family

A/D CONVERTERS

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Product Index by Family (Continued)

A/D CONVERTERS (Continued)

		95 NEW RELEASES DB314	94 DAQ DB301B	94 DSP DB302B	93 LIN DB500B
HI7188	**8-Channel, 16-Bit High Precision Sigma-Delta A/D Converter**	4-103	-	-	-
HI7190	**24-Bit High Precision Sigma Delta A/D Converter**	4-110	-	-	-
ICL7106, ICL7107	31/2 Digit LCD/LED Display A/D Converter	-	2-33	-	-
ICL7109	12-Bit Microprocessor Compatible A/D Converter	-	3-17	-	-
ICL7112	12-Bit High-Speed CMOS µP-Compatible A/D Converter	(AnswerFAX Only) Document # 3639			
ICL7115	14-Bit High Speed CMOS µP-Compatible A/D Converter	(AnswerFAX Only) Document # 3101			
ICL7116, ICL7117	31/2 Digit LCD/LED Display A/D Converter with Display Hold	-	2-46	-	-
ICL7126	31/2 Digit Low Power Single-Chip A/D Converter	(AnswerFAX Only) Document # 3084			
ICL7129	41/2 Digit LCD Single-Chip A/D Converter	-	2-58	-	-
ICL7135	41/2 Digit BCD Output A/D Converter	-	3-40	-	-
ICL7136, ICL7137	31/2 Digit LCD/LED Low Power Display A/D Converter with Overrange Recovery	-	2-68	-	-
ICL7139, ICL7149	33/4 Digit Autoranging Multimeter	-	2-83	-	-
ICL8052/ ICL71C03, ICL8068/ ICL71C03	Precision 4 1/2 Digit A/D Converter	(AnswerFAX Only) Document # 3081			
ICL8052/ ICL7104, ICL8068/ ICL7104	14/16-Bit µP-Compatible, 2-Chip A/D Converter	(AnswerFAX Only) Document # 3091			

COMPARATORS

		95 NEW RELEASES DB314	94 DAQ DB301B	94 DSP DB302B	93 LIN DB500B
CA139, CA239, CA339, LM339	Quad Voltage Comparators for Industrial, Commercial and Military Applications	-	-	-	3-3
CA3098	Programmable Schmitt Trigger - with Memory Dual Input Precision Level Detectors	-	-	-	3-7
CA3290	BiMOS Dual Voltage Comparator with MOSFET Input, Bipolar Output	-	-	-	3-17
HA-4900, HA-4902, HA-4905	Precision Quad Comparator	-	-	-	3-25
HFA-0003, HFA-0003L	Ultra High Speed Comparator	-	-	-	3-33

NOTE: Bold Type Designates a New Product from Harris.

Product Index by Family (Continued)

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Product Index by Family (Continued)

		95 NEW RELEASES DB314	94 DAQ DB301B	94 DSP DB302B	93 LIN DB500B
DEVELOPMENT TOOLS					
DECI•MATE™	Harris HSP43220 Decimating Digital Filter Development Software	-	-	8-3	-
HSP-EVAL	DSP Evaluation Platform	-	-	8-7	-
HSP45116-DB	HSP45116 Daughter Board	-	-	8-8	-
HSP50016-EV	DDC Evaluation Platform	-	-	8-10	-
DIFFERENTIAL AMPLIFIERS					
CA3028, CA3053	Differential/Cascode Amplifiers for Commercial and Industrial Equipment from DC to 120MHz	-	-	-	5-3
CA3049, CA3102	Dual High Frequency Differential Amplifiers For Low Power Applications Up 500MHz	-	-	-	5-15
CA3054	Transistor Array - Dual Independent Differential Amp for Low Power Applications from DC to 120MHz	-	-	-	5-24
DIGITAL VIDEO CAPTURE					
HMP8100	**NTSC and PAL Video Decoder with 2 Dimensional Up/Down Scaler**	11-3	-	-	-
DISPLAY DRIVERS					
CA3161	BCD to Seven Segment Decoder/Driver	-	12-3	-	-
ICM7211, ICM7212	4-Digit ICM7211 (LCD) and ICM7212 (LED) Display Drivers	-	12-6	-	-
ICM7228	8-Digit μP Compatible LED Display Decoder Driver	-	12-19	-	-
ICM7231, ICM7232	Numeric/Alphanumeric Triplexed LCD Display Driver	-	12-37	-	-
ICM7243	8-Character μP-Compatible LED Display Decoder Driver	-	12-52	-	-
DOWN CONVERSION AND DEMODULATION					
HSP50016	Digital Down Converter	-	-	6-3	-
HSP50110	Digital Quadrature Tuner	-	-	6-25	-
DSP FILTERS					
HSP43124	**Serial I/O Filter**	10-3	-	-	-
HSP43168	**Dual FIR Filter**	10-17	-	-	-
HSP43168/883	Dual FIR Filter	-	-	3-35	-
HSP43216	Halfband Filter	-	-	3-43	-
HSP43220	Decimating Digital Filter	-	-	3-60	-
HSP43220/883	Decimating Digital Filter	-	-	3-83	-
HSP43481	Digital Filter	-	-	3-90	-
HSP43481/883	Digital Filter	-	-	3-105	-

NOTE: Bold Type Designates a New Product from Harris.

Product Index by Family (Continued)

DSP FILTERS (Continued)

		95 NEW RELEASES DB314	94 DAQ DB301B	94 DSP DB302B	93 LIN DB500B
HSP43881	Digital Filter	-	-	3-110	-
HSP43881/883	Digital Filter	-	-	3-125	-
HSP43891	Digital Filter	-	-	3-131	-
HSP43891/883	Digital Filter	-	-	3-147	-

MULTIPLEXERS

		95 NEW RELEASES DB314	94 DAQ DB301B	94 DSP DB302B	93 LIN DB500B
DG406, DG407	Single 16-Channel/Differential 8-Channel CMOS Analog Multiplexers	-	10-15	-	-
DG408, DG409	Single 8-Channel/Differential 4-Channel CMOS Analog Multiplexers	-	10-17	-	-
DG458, DG459	Single 8-Channel/Differential 4-Channel Fault Protected Analog Multiplexers	-	10-31	-	-
DG506A, DG507A, DG508A, DG509A	CMOS Analog Multiplexers	-	10-41	-	-
DG526, DG527, DG528, DG529	Analog CMOS Latchable Multiplexers	-	10-54	-	-
HI-1818A, HI-1828A	Low Resistance, Single 8 Channel and Differential 4 Channel CMOS Analog Multiplexers	-	10-70	-	-
HI-506, HI-507, HI-508, HI-509	Single 16 and 8/Differential 8 and 4 Channel CMOS Analog Multiplexers	-	10-78	-	-
HI-506A, HI-507A, HI-508A, HI-509A	16 Channel, 8 Channel, Differential 8 and Differential 4 Channel CMOS Analog MUXs with Active Overvoltage Protection	-	10-95	-	-
HI-516	16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer	-	10-109	-	-
HI-518	8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer	-	10-116	-	-
HI-524	4 Channel Wideband and Video Multiplexer	-	10-123	-	-
HI-539	Monolithic, 4 Channel, Low Level, Differential Multiplexer	-	10-129	-	-
HI-546, HI-547, HI-548, HI-549	Single 16 and 8, Differential 8 and 4 Channel CMOS Analog MUXs with Active Overvoltage Protection	-	10-140	-	-
IH6108	8-Channel CMOS Analog Multiplexer	(AnswerFAX Only) Document # 3156			
IH6208	4-Channel Differential CMOS Analog Multiplexer	(AnswerFAX Only) Document # 3157			

MULTIPLIERS

		95 NEW RELEASES DB314	94 DAQ DB301B	94 DSP DB302B	93 LIN DB500B
HMA510	16 x 16-Bit CMOS Parallel Multiplier Accumulator	-	-	2-3	-
HMA510/883	16 x 16-Bit CMOS Parallel Multiplier Accumulator	-	-	2-10	-

NOTE: Bold Type Designates a New Product from Harris.

Product Index by Family (Continued)

MULTIPLIERS (Continued)

		95 NEW RELEASES DB314	94 DAQ DB301B	94 DSP DB302B	93 LIN DB500B
HMU16, HMU17	16 x 16-Bit CMOS Parallel Multipliers	-	-	2-15	-
HMU16/883	16 x 16-Bit CMOS Parallel Multiplier	-	-	2-25	-
HMU17/883	16 x 16-Bit CMOS Parallel Multiplier	-	-	2-31	-

OPERATIONAL AMPLIFIERS

		95 NEW RELEASES DB314	94 DAQ DB301B	94 DSP DB302B	93 LIN DB500B
CA124, CA224, CA324, LM324, LM2902	Quad Operational Amplifiers for Commercial, Industrial, and Military Applications	-	-	-	2-19
CA158, CA258, CA358, CA2904, LM358, LM2904	Dual Operational Amplifiers for Commercial Industrial, and Military Applications	-	-	-	2-26
CA741, CA1458, CA1558, LM741, LM1458, LM1558	High Gain Single and Dual Operational Amplifiers for Military, Industrial and Commercial Applications	-	-	-	2-37
CA3020	Multipurpose Wide-Band Power Amps Military, Industrial and Commercial Equipment at Frequency Up to 8MHz	-	-	-	2-43
CA3060	Operational Transconductance Amplifier Arrays	-	-	-	2-52
CA3078	Micropower Operational Amplifier	-	-	-	2-64
CA3080	Operational Transconductance Amplifier (OTA)	-	-	-	2-73
CA3094	Programmable Power Switch/Amplifier for Control and General Purpose Applications	-	-	-	2-86
CA3100	Wideband Operational Amplifier	-	-	-	2-101
CA3130	BiMOS Operational Amplifier with MOSFET Input/CMOS Output	-	-	-	2-108
CA3140	BiMOS Operational Amplifier with MOSFET Input/Bipolar Output	-	-	-	2-123
CA3160	BiMOS Operational Amplifiers with MOSFET Input/CMOS Output	-	-	-	2-143
CA3193	BiCMOS Precision Operational Amplifiers	-	-	-	2-160
CA3240	Dual BiMOS Operational Amplifier with MOSFET Input/Bipolar Output	-	-	-	2-171
CA3260	BiMOS Operational Amplifier with MOSFET Input/CMOS Output	-	-	-	2-187
CA3280	Dual Variable Operational Amplifier	-	-	-	2-191
CA3420	Low Supply Voltage, Low Input Current BiMOS Operational Amplifiers	-	-	-	2-202
CA3440	Nanopower BiMOS Operational Amplifier	-	-	-	2-207
CA3450	Video Line Driver, High Speed Operational Amplifier	-	-	-	2-213

NOTE: Bold Type Designates a New Product from Harris.

Product Index by Family (Continued)

OPERATIONAL AMPLIFIERS (Continued)

NOTE: Bold Type Designates a New Product from Harris.

Product Index by Family (Continued)

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Product Index by Family (Continued)

OPERATIONAL AMPLIFIERS (Continued)

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Product Index by Family (Continued)

1 GENERAL INFORMATION

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Product Index by Family (Continued)

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Product Index by Family (Continued)

SWITCHES (Continued)

		95 NEW RELEASES DB314	94 DAQ DB301B	94 DSP DB302B	93 LIN DB500B
DG401, DG403, DG405	**Monolithic CMOS Analog Switches**	7-3	-	-	-
DG411, DG412, DG413	Monolithic Quad SPST CMOS Analog Switches	-	9-44	-	-
DG441, DG442	Monolithic Quad SPST CMOS Analog Switches	-	9-53	-	-
DG444, DG445	Monolithic Quad SPST CMOS Analog Switches	-	9-63	-	-
HI-200, HI-201	Dual/Quad SPST CMOS Analog Switches	-	9-73	-	-
HI-201HS	High Speed Quad SPST CMOS Analog Switch	-	9-82	-	-
HI-222	High Frequency/Video Switch	(AnswerFAX Only) Document # 3124			
HI-300 thru HI-307	CMOS Analog Switches	-	9-93	-	-
HI-381 thru HI-390	CMOS Analog Switches	-	9-103	-	-
HI-5040 thru HI-5051, HI-5046A and HI-5047A	CMOS Analog Switches	-	9-110	-	-
IH401A	QUAD Varafet Analog Switch	(AnswerFAX Only) Document # 3128			
IH5009 thru IH5012, IH5014, IH5016 thru IH5020, IH5022, IH5024	Virtual Ground Analog Switch	(AnswerFAX Only) Document # 3129			
IH5043	Dual SPDT CMOS Analog Switch	-	9-121	-	-
IH5052, IH5053	Quad CMOS Analog Switch	-	9-128	-	-
IH5140 thru IH5145	High-Level CMOS Analog Switch	-	9-134	-	-
IH5151	Dual SPDT CMOS Analog Switch	-	9-147	-	-
IH5341, IH5352	Dual SPST, Quad SPST CMOS RF/Video Switches	-	9-155	-	-
IH6201	Dual CMOS Driver/Voltage Translator	(AnswerFAX Only) Document # 3136			

TELECOMMUNICATIONS

		95 NEW RELEASES DB314	94 DAQ DB301B	94 DSP DB302B	93 LIN DB500B
CD22100	CMOS 4 x 4 Crosspoint Switch with Control Memory High-Voltage Type (20V Rating)	-	-	-	8-3
CD22101, CD22102	CMOS 4 x 4 x 2 Crosspoint Switch with Control Memory	-	-	-	8-12
CD22103A	CMOS HDB3 (High Density Bipolar 3) Transcoder for 2.048/8.448 Mb/s Transmission Applications	-	-	-	8-24
CD22202, CD22203	5V Low Power DTMF Receiver	-	-	-	8-30
CD22204	5V Low Power Subscriber DTMF Receiver	-	-	-	8-36
CD22301	Monolithic Pan Repeater	-	-	-	8-41

1

GENERAL INFORMATION

NOTE: Bold Type Designates a New Product from Harris.

Product Index by Family (Continued)

TELECOMMUNICATONS (Continued)

		95 NEW RELEASES DB314	94 DAQ DB301B	94 DSP DB302B	93 LIN DB500B
CD22354A, CD22357A	CMOS Single-Chip, Full-Feature PCM CODEC	-	-	-	8-46
CD22M3493	12 x 8 x 1 BiMOS-E Crosspoint Switch	-	-	-	8-56
CD22M3494	16 x 8 x 1 BiMOS-E Crosspoint Switch	-	-	-	8-61
CD22859	Monolithic Silicon COS/MOS Dual-Tone Multifrequency Tone Generator	-	-	-	8-67
CD74HC22106, CD74HCT22106	QMOS 8 x 8 x 1 Crosspoint Switch with Memory Control	-	-	-	8-72
HC-5502B	SLIC Subscriber Line Interface Circuit	-	-	-	8-81
HC-5504B	SLIC Subscriber Line Interface Circuit	-	-	-	8-90
HC-5504DLC	SLIC Subscriber Line Interface Circuit	-	-	-	8-98
HC-5509A1	SLIC Subscriber Line Interface Circuit	-	-	-	8-106
HC-5509B	SLIC Subscriber Line Interface Circuit	-	-	-	8-116
HC-5513	**Subscriber Line Interface Circuit**	12-3	-	-	-
HC-5524	SLIC Subscriber Line Interface Circuit	-	-	-	8-126
HC-5560	PCM Transcoder	-	-	-	8-135
HC-55536	Continuous Variable Slope Delta-Demodulator (CVSD)	-	-	-	8-144
HC-55564	Continuously Variable Slope Delta-Modulator (CVSD)	-	-	-	8-147

TRANSISTOR ARRAYS

		95 NEW RELEASES DB314	94 DAQ DB301B	94 DSP DB302B	93 LIN DB500B
CA3018	General Purpose Transistor Arrays	-	-	-	6-5
CA3039	Diode Array	-	-	-	6-11
CA3045, CA3046	General Purpose N-P-N Transistor Arrays	-	-	-	6-15
CA3081, CA3082	General Purpose High Current N-P-N Transistor Arrays	-	-	-	6-21
CA3083	General Purpose High Current N-P-N Transistor Array	-	-	-	6-24
CA3086	General Purpose N-P-N Transistor Array	-	-	-	6-28
CA3096	N-P-N/P-N-P Transistor Array	-	-	-	6-33
CA3127	High Frequency N-P-N Transistor Array	-	-	-	6-46
CA3141	High-Voltage Diode Array For Commercial, Industrial & Military Applications	-	-	-	6-52
CA3146, CA3183	High-Voltage Transistor Arrays	-	-	-	6-55
CA3227, CA3246	High-Frequency N-P-N Transistor Arrays For Low-Power Applications at Frequencies Up to 1.5GHz	-	-	-	6-65

NOTE: Bold Type Designates a New Product from Harris.

Product Index by Family (Continued)

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SIGNAL PROCESSING NEW RELEASES 2

OPERATIONAL AMPLIFIERS

HARRIS SEMICONDUCTOR

HA5013

July 1995

Triple 125MHz Video Amplifier

Features

- **Wide Unity Gain Bandwidth 125MHz**
- **Slew Rate 475V/μs**
- **Input Offset Voltage. 800μV**
- **Differential Gain 0.03%**
- **Differential Phase. . . . . 0.03 Deg.**
- **Supply Current (per Amplifier) 7.5mA**
- **ESD Protection. 4000V**
- **Guaranteed Specifications at ±5V Supplies**
- **Low Cost**

Applications

- **PC Add-On Multimedia Boards**
- **Flash A/D Driver**
- **Color Image Scanners**
- **CCD Cameras and Systems**
- **RGB Cable Driver**
- **RGB Video Preamp**
- **PC Video Conferencing**

Description

The HA5013 is a low cost triple amplifier optimized for RGB video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor.

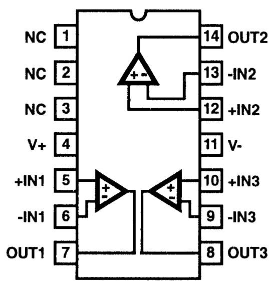
The performadnce of the HA5013 is very similar to the popular Harris HA-5020 single video amplifier.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA5013IP	-40°C to +85°C	14 Lead Plastic DIP
HA5013IB	-40°C to +85°C	14 Lead Plastic SOIC (N)

Pinout

HA5013
(PDIP, SOIC)
TOP VIEW



File Number **3654.2**

Absolute Maximum Ratings (Note 1)

ESD Protection (Note 15) 2000V
Voltage Between V+ and V- Terminals 36V
DC Input Voltage . . . . . $\pm V_{SUPPLY}$
Differential Input Voltage 10V
Output Current (Note 2) . . . . . Short Circuit Protected
Junction Temperature (Note 12) . . . . . +175°C
Junction Temperature (Plastic Package) (Note 12) . . . . . +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HA5013I . . . . . $-40^oC \le T_A \le +85^oC$
Supply Voltage Range . . . . . ±4.5V to ±15V
Storage Temperature Range . . . . . $-65^oC \le T_A \le +150^oC$
Thermal Package Resistance (°C/W) θ_{JA}
Plastic DIP 100
SOIC 120

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \le 10pF$, Unless Otherwise Specified

PARAMETER	(NOTE 16) TEST LEVEL	TEMPERATURE	HA5013I MIN	HA5013I TYP	HA5013I MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage (V_{IO})	A	+25°C	-	0.8	3	mV
	A	Full	-	-	5	mV
Delta V_{IO} Between Channels	A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift	B	Full	-	5	-	μV/°C
V_{IO} Common Mode Rejection Ratio (Note 3)	A	+25°C	53	-	-	dB
	A	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio (Note 4)	A	+25°C	60	-	-	dB
	A	Full	55	-	-	dB
Input Common Mode Range (Note 3)	A	Full	±2.5	-	-	V
Non-Inverting Input (+IN) Current	A	+25°C	-	3	8	μA
	A	Full	-	-	20	μA
+IN Common Mode Rejection (Note 3) $\left(+I_{BCMR} = \frac{1}{+R_{IN}}\right)$	A	+25°C	-	-	0.15	μA/V
	A	Full	-	-	0.5	μA/V
+IN Power Supply Rejection (Note 4)	A	+25°C	-	-	0.1	μA/V
	A	Full	-	-	0.3	μA/V
Inverting Input (-IN) Current	A	+25°C, +85°C	-	4	12	μA
	A	-40°C	-	10	30	μA
Delta - IN BIAS Current Between Channels	A	+25°C, +85°C	-	6	15	μA
	A	-40°C	-	10	30	μA
-IN Common Mode Rejection (Note 3)	A	+25°C	-	-	0.4	μA/V
	A	Full	-	-	1.0	μA/V
-IN Power Supply Rejection (Note 4)	A	+25°C	-	-	0.2	μA/V
	A	Full	-	-	0.5	μA/V
Input Noise Voltage (f = 1kHz)	B	+25°C	-	4.5	-	$nV/\sqrt{Hz}$
+Input Noise Current (f = 1kHz)	B	+25°C	-	2.5	-	$pA/\sqrt{Hz}$
-Input Noise Current (f = 1kHz)	B	+25°C	-	25.0	-	$pA/\sqrt{Hz}$

Electrical Specifications V+ = +5V, V- = -5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 16) TEST LEVEL	TEMPERATURE	HA5013I MIN	TYP	MAX	UNITS
TRANSFER CHARACTERISTICS						
Transimpedence (Note 14)	A	+25°C	1.0	-	-	MΩ
	A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain, R_L = 400Ω, V_{OUT} = ±2.5V	A	+25°C	70	-	-	dB
	A	Full	65	-	-	dB
Open Loop DC Voltage Gain, R_L = 100Ω, V_{OUT} = ±2.5V	A	+25°C	50	-	-	dB
	A	Full	45	-	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 13)	A	+25°C	±2.5	±3.0	-	V
	A	Full	±2.5	±3.0	-	V
Output Current (Note 13)	B	Full	±16.6	±20.0	-	mA
Output Current (Short Circuit, Note 10)	A	Full	±40	±60	-	mA
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range	A	+25°C	5	-	15	V
Quiescent Supply Current	A	Full	-	7.5	10	mA/Op Amp
AC CHARACTERISTICS (A_V = +1)						
Slew Rate (Note 5)	B	+25°C	275	350	-	V/µs
Full Power Bandwidth (Note 6)	B	+25°C	22	28	-	MHz
Rise Time (Note 7)	B	+25°C	-	6	-	ns
Fall Time (Note 7)	B	+25°C	-	6	-	ns
Propagation Delay (Note 7)	B	+25°C	-	6	-	ns
Overshoot	B	+25°C	-	4.5	-	%
-3dB Bandwidth (Note 8)	B	+25°C	-	125	-	MHz
Settling Time to 1%, 2V Output Step	B	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step	B	+25°C	-	75	-	ns
AC CHARACTERISTICS (A_V = +2, R_F = 681Ω)						
Slew Rate (Note 5)	B	+25°C	-	475	-	V/µs
Full Power Bandwidth (Note 6)	B	+25°C	-	26	-	MHz
Rise Time (Note 7)	B	+25°C	-	6	-	ns
Fall Time (Note 7)	B	+25°C	-	6	-	ns
Propagation Delay (Note 7)	B	+25°C	-	6	-	ns
Overshoot	B	+25°C	-	12	-	%

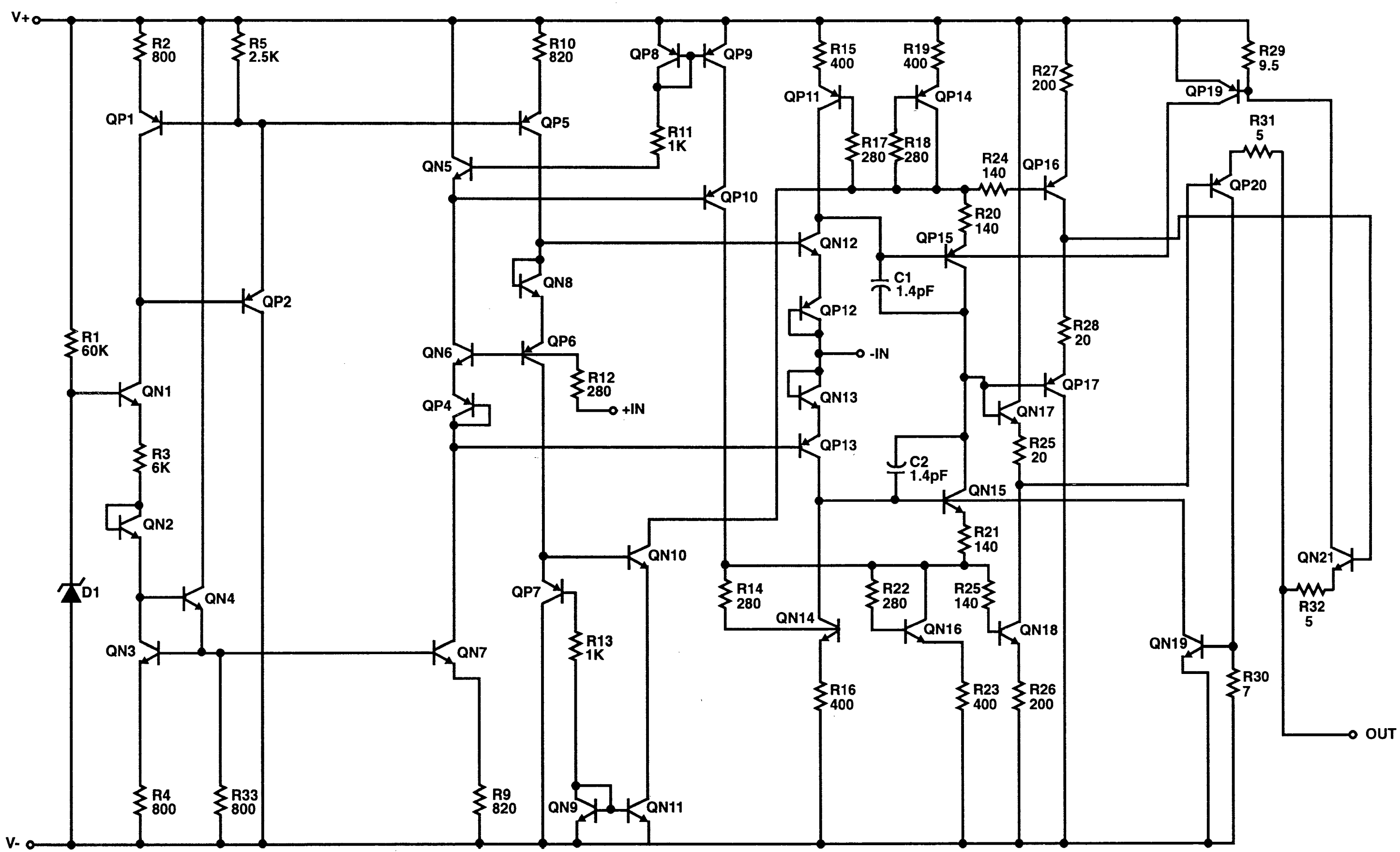
Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$. $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 16) TEST LEVEL	TEMPERATURE	HA5013I MIN	TYP	MAX	UNITS
-3dB Bandwidth (Note 8)		B	+25°C	-	95	-	MHz
Settling Time to 1%, 2V Output Step		B	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step		B	+25°C	-	100	-	ns
Gain Flatness	5MHz	B	+25°C	-	0.02	-	dB
	20MHz	B	+25°C	-	0.07	-	dB
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)							
Slew Rate (Note 5)		B	+25°C	350	475	-	V/µs
Full Power Bandwidth (Note 6)		B	+25°C	28	38	-	MHz
Rise Time (Note 7)		B	+25°C	-	8	-	ns
Fall Time (Note 7)		B	+25°C	-	9	-	ns
Propagation Delay (Note 7)		B	+25°C	-	9	-	ns
Overshoot		B	+25°C	-	1.8	-	%
-3dB Bandwidth (Note 8)		B	+25°C	-	65	-	MHz
Settling Time to 1%, 2V Output Step		B	+25°C	-	75	-	ns
Settling Time to 0.1%, 2V Output Step		B	+25°C	-	130	-	ns
VIDEO CHARACTERISTICS							
Differential Gain (Notes 11, 13)		B	+25°C	-	0.03	-	%
Differential Phase (Notes 11, 13)		B	+25°C	-	0.03	-	Degrees

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.
3. $V_{CM} = \pm 2.5V$. At -40°C Product is tested at $V_{CM} = \pm 2.25V$ because Short Test Duration does not allow self heating.
4. $\pm 3.5V \leq V_S \leq \pm 6.5V$
5. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
6. $2\left(FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}; V_{PEAK} = 2V\right)$
7. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
8. $R_L = 400\Omega$, $V_{OUT} = 100mV$.
9. A. Production Tested; B. Guaranteed Limit or Typical based on characterization; C. Design Typical for information only.
10. $V_{IN} = \pm 2.5V$, $V_{OUT} = 0V$.
11. Measured with a VM700A video tester using an NTC-7 composite VITS.
12. Maximum power dissipation, including output load, must be designed to maintain junction temperature below +175°C for die, and below +150°C for plastic packages. See Applications Information section for safe operating area information.
13. $R_L = 150\Omega$.
14. $V_{OUT} = \pm 2.5V$. At -40°C Product is tested at $V_{OUT} = \pm 2.25V$ because Short Test Duration does not allow self heating.
15. ESD protection is for human body model tested per MIL-STD - 883, Method 3015.7.
16. A. Production Tested; B. Guaranteed limit or Typical based on characterization; C. Design Typical for information only.

Schematic



V+
V-
R2 800
R5 2.5K
R10 820
QP8
QP9
R15 400
R19 400
R27 200
R29 9.5
QP19
QP11
QP14
QP1
QP5
R11 1K
R17 280
R18 280
R31 5
R24 140
QP16
QN5
QP10
QP20
R20 140
QN12
QP15
QN8
C1 1.4pF
QP2
QP12
-IN
R28 20
R1 60K
QN6
QP6
R12 280
+IN
QN1
QN13
QP17
QP4
QN17
QP13
R25 20
R3 6K
C2 1.4pF
QN15
QN2
R21 140
QN10
QN21
R14 280
R22 280
R25 140
D1
QN4
QP7
QN14
QN16
QN18
R32 5
QN3
QN7
R13 1K
QN19
R30 7
R16 400
R23 400
R26 200
OUT
R4 800
R33 800
R9 820
QN9
QN11

Test Circuits

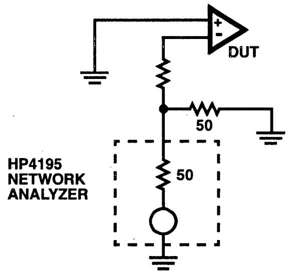


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

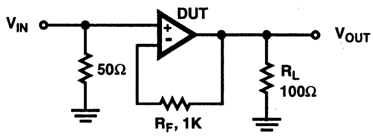


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

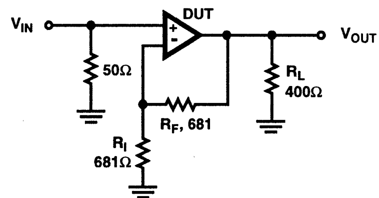


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT

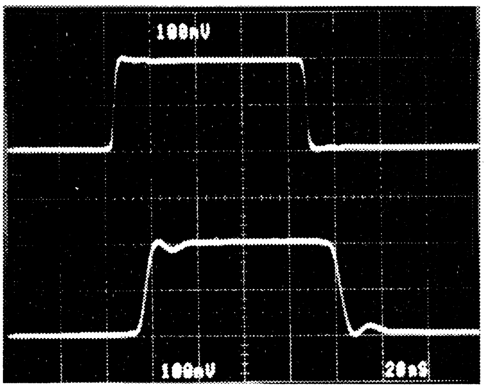


FIGURE 4. SMALL SIGNAL RESPONSE
Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

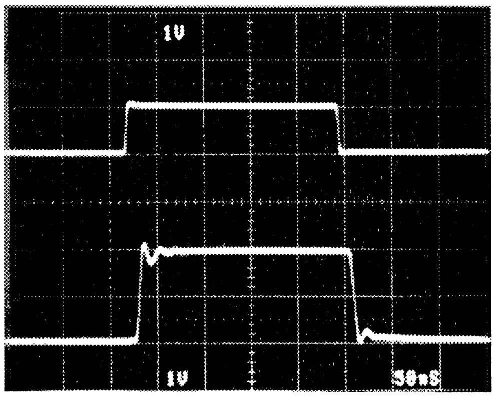


FIGURE 5. LARGE SIGNAL RESPONSE
Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 8 and Figure 9 in the typical performance section, illustrate the performance of the HA5013 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA5013 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10µF) tantalum or electrolytic capacitor in parallel with a small value (0.1µF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

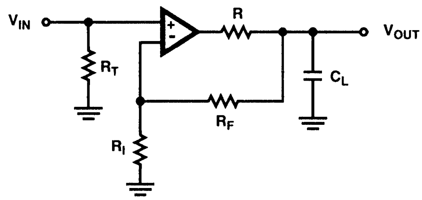


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Power Dissipation Considerations

Due to the high supply current inherent in quad amplifiers, care must be taken to insure that the maximum junction temperature (T_J, see Absolute Maximum Ratings) is not exceeded. Figure 7 shows the maximum ambient temperature versus supply voltage for the available package styles (Plastic DIP, SOIC). At ±5V_{DC} quiescent operation both package styles may be operated over the full industrial range of -40°C to +85°C. It is recommended that thermal calculations, which take into account output power, be performed by the designer.

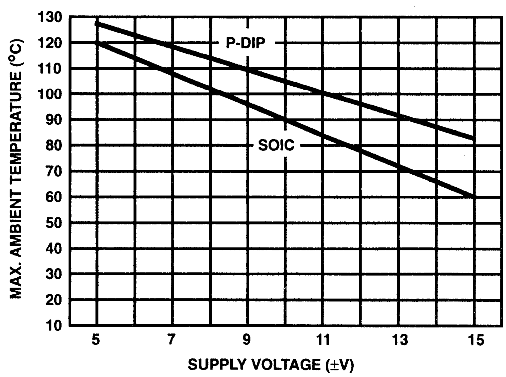


FIGURE 7. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified

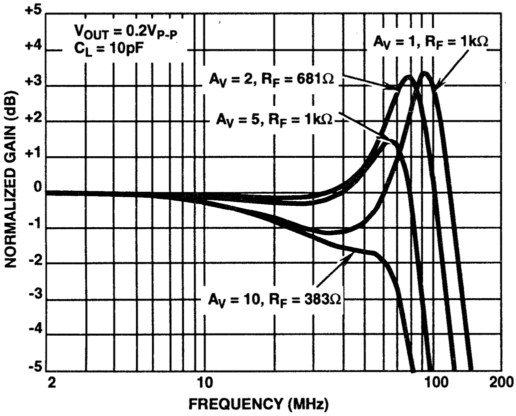


FIGURE 8. NON-INVERTING FREQUENCY RESPONSE

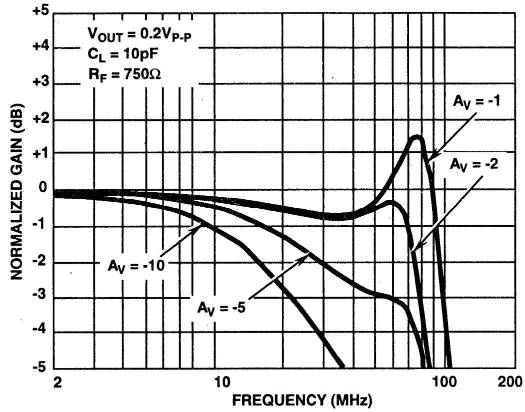


FIGURE 9. INVERTING FREQUENCY RESPONSE

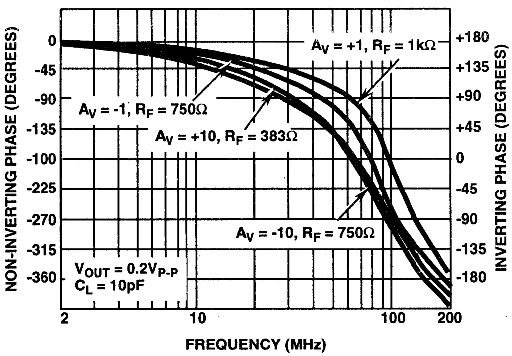


FIGURE 10. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

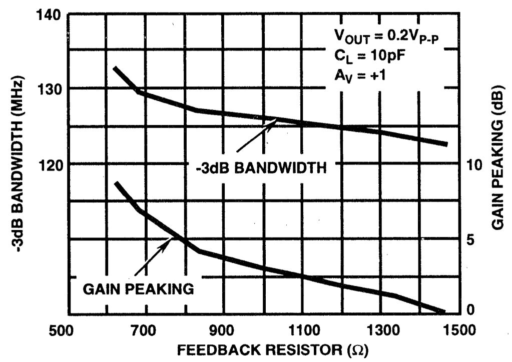


FIGURE 11. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

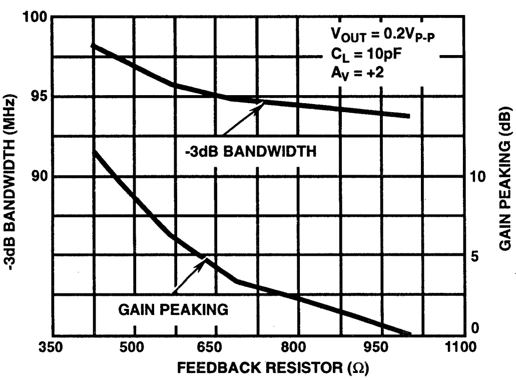


FIGURE 12. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

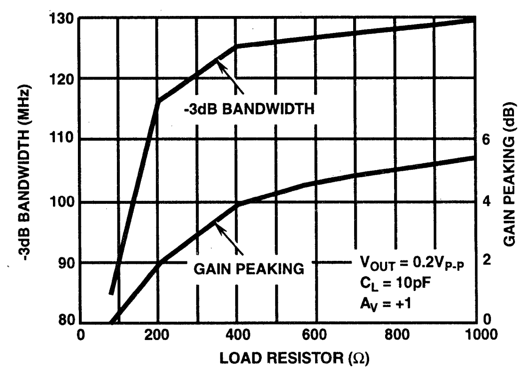


FIGURE 13. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

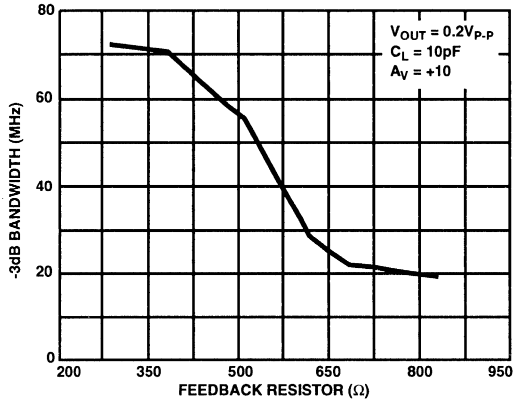


FIGURE 14. BANDWIDTH vs FEEDBACK RESISTANCE

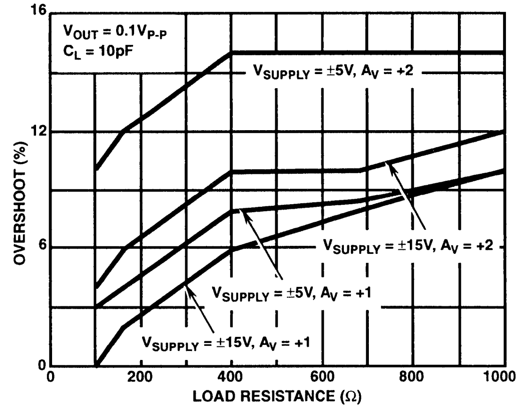


FIGURE 15. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

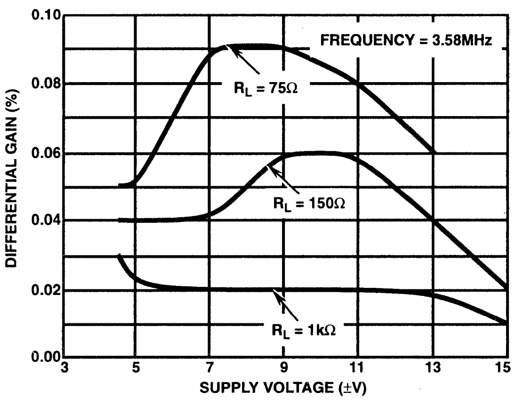


FIGURE 16. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

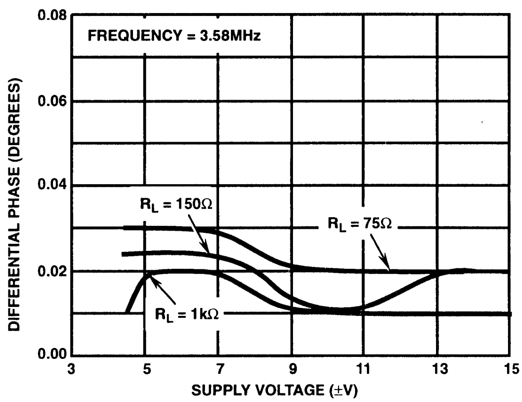


FIGURE 17. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

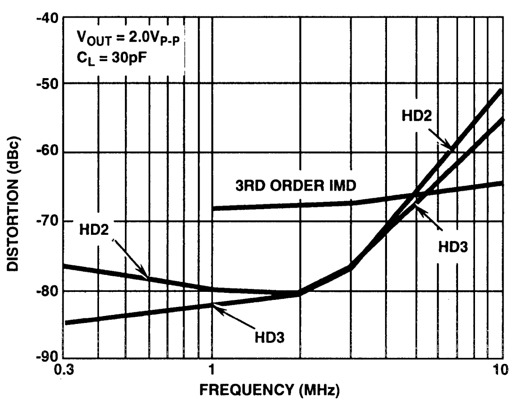


FIGURE 18. DISTORTION vs FREQUENCY

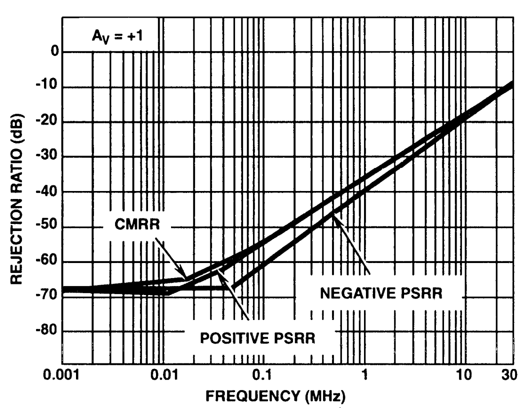


FIGURE 19. REJECTION RATIOS vs FREQUENCY

2

OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

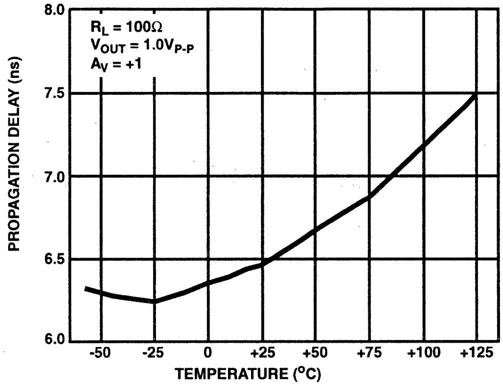


FIGURE 20. PROPAGATION DELAY vs TEMPERATURE

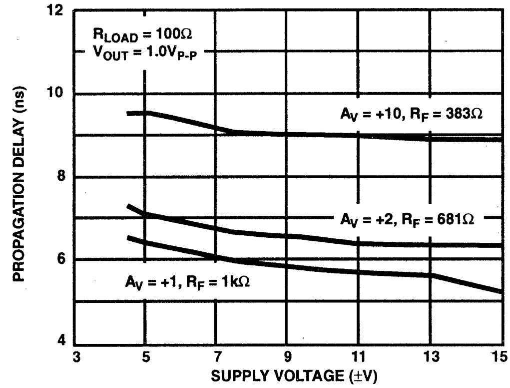


FIGURE 21. PROPAGATION DELAY vs SUPPLY VOLTAGE

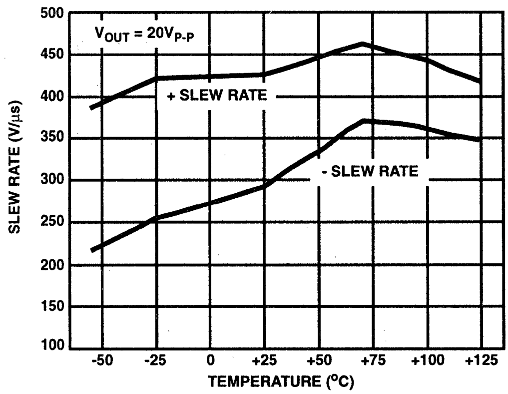


FIGURE 22. SLEW RATE vs TEMPERATURE

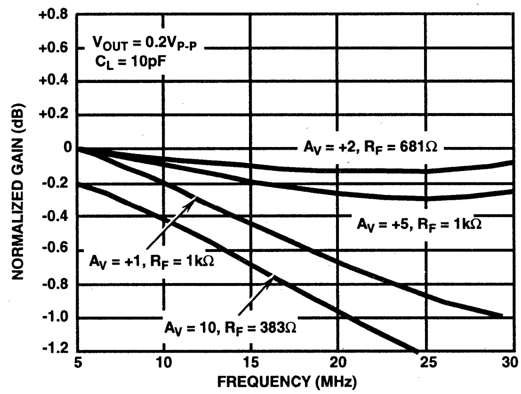


FIGURE 23. NON-INVERTING GAIN FLATNESS vs FREQUENCY

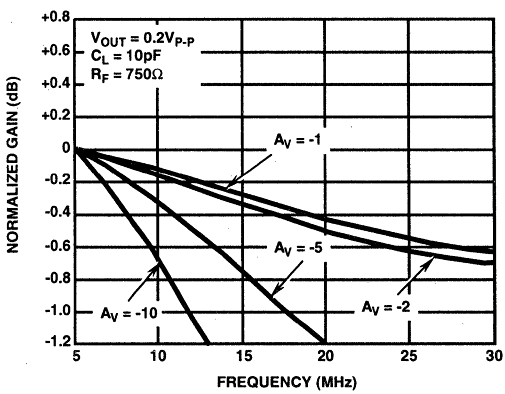


FIGURE 24. INVERTING GAIN FLATNESS vs FREQUENCY

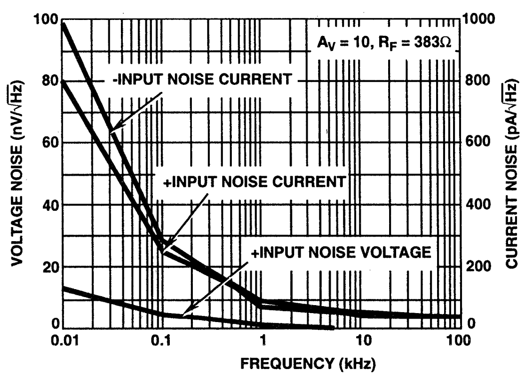


FIGURE 25. INPUT NOISE CHARACTERISTICS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

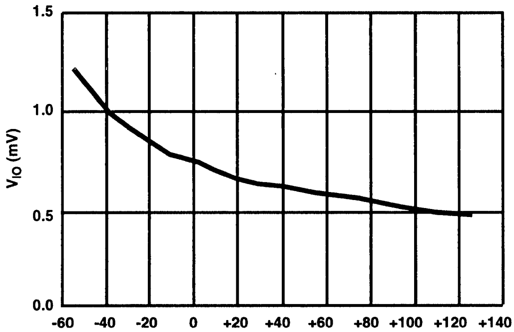


FIGURE 26. INPUT OFFSET VOLTAGE vs TEMPERATURE

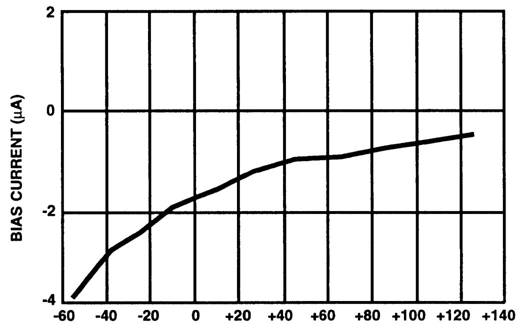


FIGURE 27. +INPUT BIAS CURRENT vs TEMPERATURE

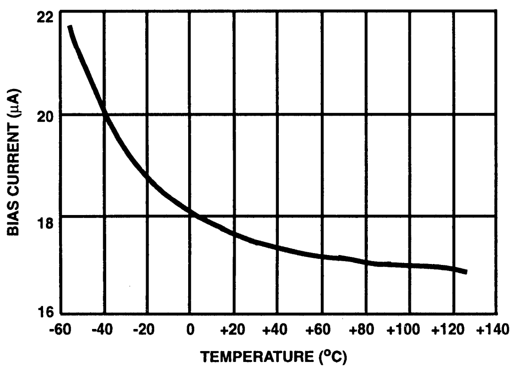


FIGURE 28. -INPUT BIAS CURRENT vs TEMPERATURE

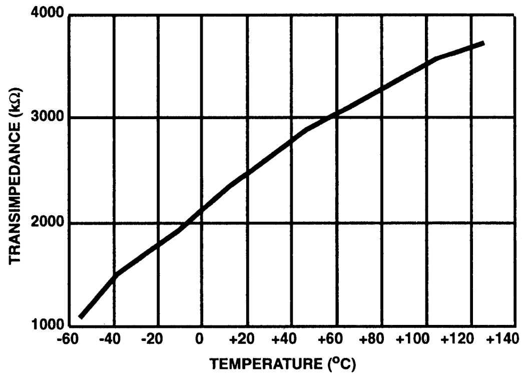


FIGURE 29. TRANSIMPEDANCE vs TEMPERATURE

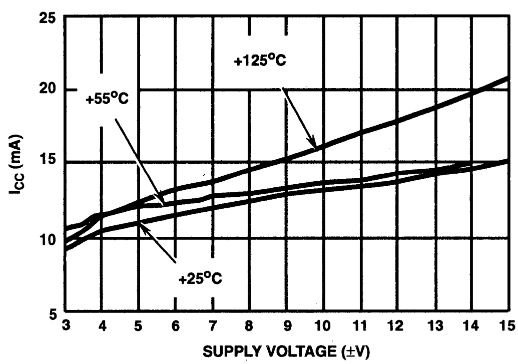


FIGURE 30. SUPPLY CURRENT vs SUPPLY VOLTAGE

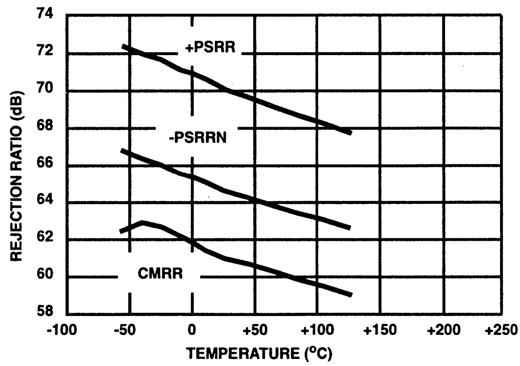


FIGURE 31. REJECTION RATIO vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

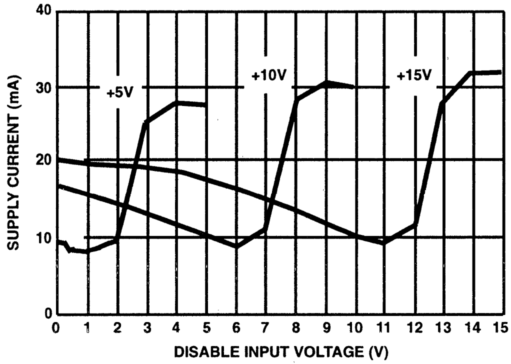


FIGURE 32. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

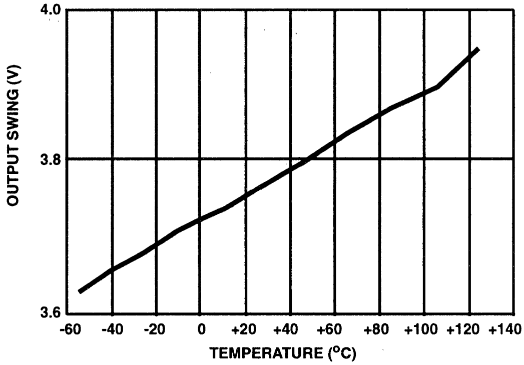


FIGURE 33. OUTPUT SWING vs TEMPERATURE

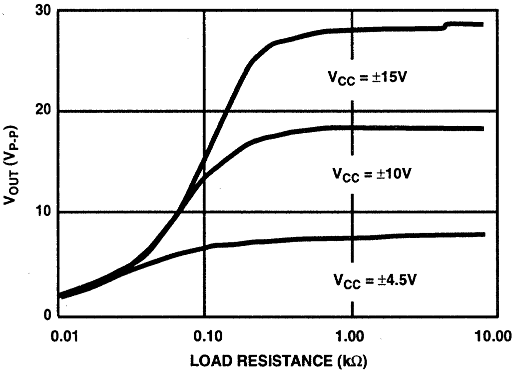


FIGURE 34. OUTPUT SWING vs LOAD RESISTANCE

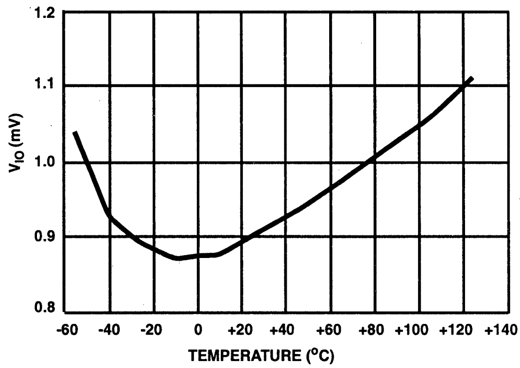


FIGURE 35. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

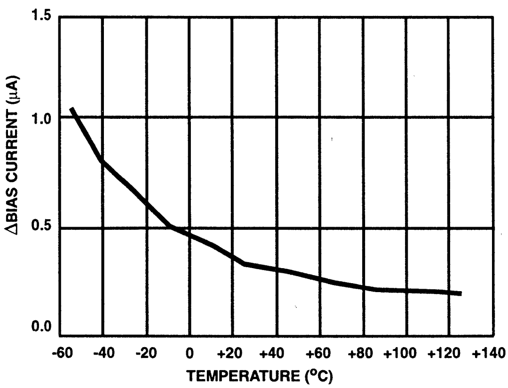


FIGURE 36. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

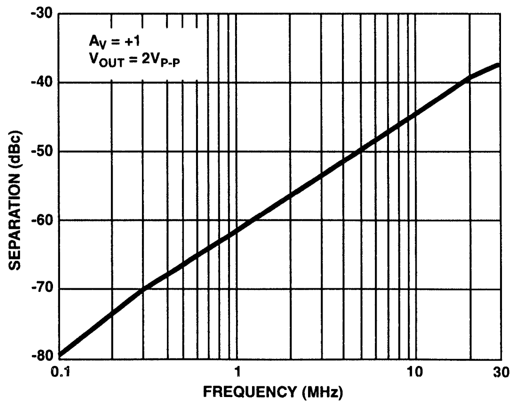


FIGURE 37. CHANNEL SEPARATION vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

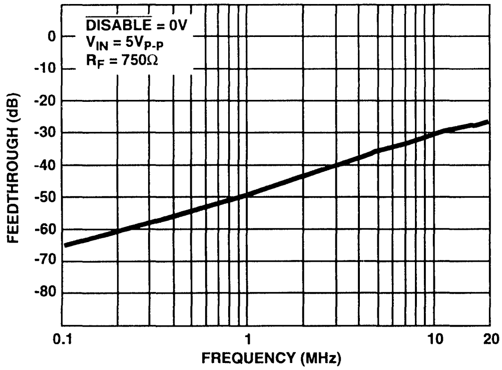


FIGURE 38. DISABLE FEEDTHROUGH vs FREQUENCY

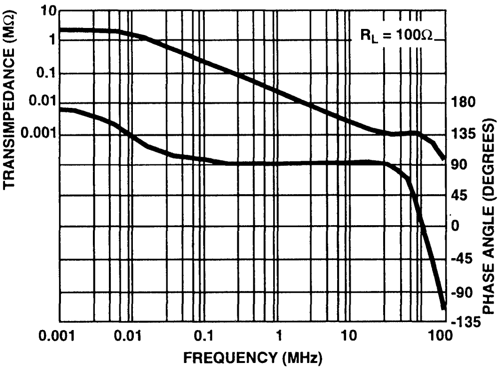


FIGURE 39. TRANSIMPEDANCE vs FREQUENCY

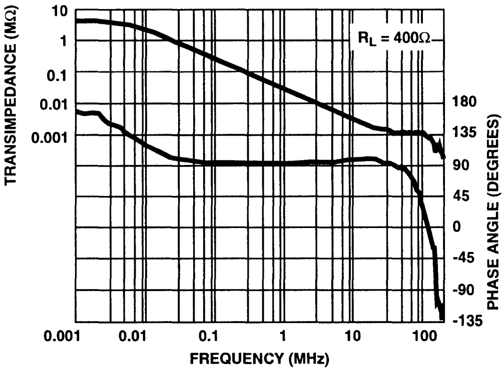


FIGURE 40. TRANSIMPEDENCE vs FREQUENCY

2

OPERATIONAL AMPLIFIERS

Die Characteristics

DIE DIMENSIONS:
2680μm x 2600μm x 483μm ±25.4μm

METALLIZATION:
Type: Metal 1: AlCu (1%), Metal 2: AlCu (1%)
Thickness: Metal 1: 8kÅ ± 0.4kÅ, Metal 2: 16kÅ ± 0.8kÅ

WORST CASE CURRENT DENSITY:
2.0 x 10^5 A/cm^2 at 50mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.4kÅ

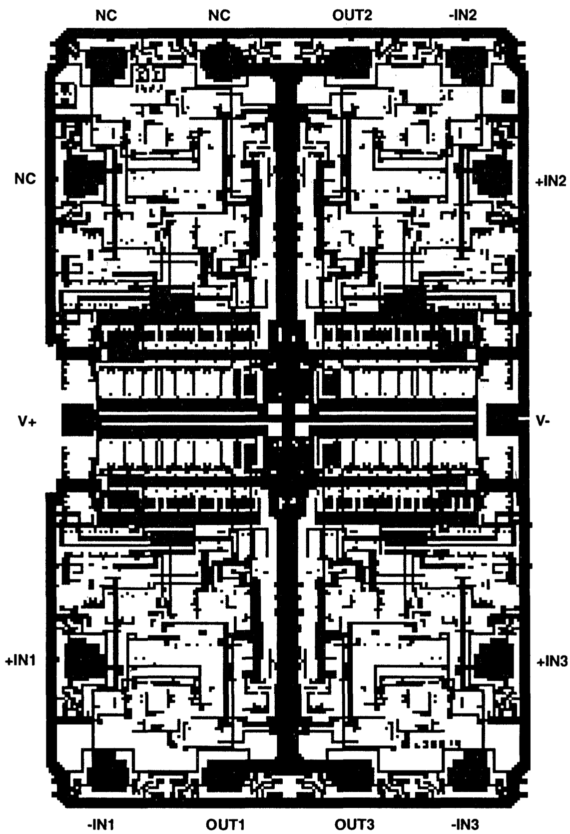
TRANSISTOR COUNT: 248

PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:
Material:Epoxy - Plastic DIP and SOIC

Metallization Mask Layout

HA5013



HARRIS SEMICONDUCTOR

HA-5020

100MHz Current Feedback Video Amplifier With Disable

July 1995

Features

- Wide Unity Gain Bandwidth 100MHz
- Slew Rate 800V/µs
- Output Current . . . . ±30mA (Min)
- Drives 3.5V into 75Ω
- Differential Gain 0.03%
- Differential Phase . . . . 0.03 Degrees
- Low Input Voltage Noise . . . . 4.5nV/√Hz
- Low Supply Current . . . . 10mA (Max)
- Wide Supply Range . . . . ±5V to ±15V
- Output Enable/Disable
- High Performance Replacement for EL2020

Applications

- Unity Gain Video/Wideband Buffer
- Video Gain Block
- Video Distribution Amp/Coax Cable Driver
- Flash A/D Driver
- Waveform Generator Output Driver
- Current to Voltage Converter; D/A Output Buffer
- Radar Systems
- Imaging Systems

Description

The HA-5020 is a wide bandwidth, high slew rate amplifier optimized for video applications and gains between 1 and 10. Manufactured on Harris' Reduced Feature Complementary Bipolar DI process, this amplifier uses current mode feedback to maintain higher bandwidth at a given gain than conventional voltage feedback amplifiers. Since it is a closed loop device, the HA-5020 offers better gain accuracy and lower distortion than open loop buffers.

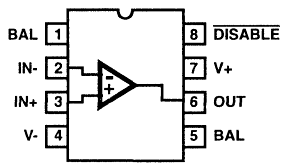
The HA-5020 features low differential gain and phase and will drive two double terminated 75Ω coax cables to video levels with low distortion. Adding a gain flatness performance of 0.1dB makes this amplifier ideal for demanding video applications. The bandwidth and slew rate of the HA-5020 are relatively independent of closed loop gain. The 100MHz unity gain bandwidth only decreases to 60MHz at a gain of 10. The HA-5020 used in place of a conventional op amp will yield a significant improvement in the speed power product. To further reduce power, the HA-5020 has a disable function which significantly reduces supply current, while forcing the output to a true high impedance state. This allows the outputs of multiple amplifiers to be wire-OR'd into multiplexer configurations. The device also includes output short circuit protection and output offset voltage adjustment.

The HA-5020 is available in commercial and industrial temperature ranges, and a choice of packages. See the "Ordering Information" section below for more information. For military grade product, please refer to the HA-5020/ 883 data sheet.

For multi channel versions of the HA-5020 see the HA5022 dual with disable, HA5023 dual, HA5013 triple, HA5024 quad with disable or HA5025 quad op amp data sheets.

Pinout

HA-5020
(PDIP, CERDIP, SOIC)
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA3-5020-5	0°C to +75°C	8 Lead Plastic DIP
HA7-5020-5	0°C to +75°C	8 Lead CerDIP
HA9P5020-5	0°C to +75°C	8 Lead Plastic SOIC (N)
HA3-5020-9	-40°C to +85°C	8 Lead Plastic DIP
HA7-5020-9	-40°C to +85°C	8 Lead CerDIP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **2845.6**

Absolute Maximum Ratings (Note 1)

Voltage Between V+ and V- Terminals 36V
DC Input Voltage . . . . . $\pm V_{SUPPLY}$
Differential Input Voltage 10V
Output Current . . . . . Short Circuit Protected
Junction Temperature (Note 19) . . . . . +175°C
Junction Temperature (Plastic Package) (Note 19) . . . . . +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C
(SOIC - Lead Tips Only)

Operating Temperature Range

HA-5020-5 . . . . . $0^oC \le T_A \le +75^oC$
HA-5020-9 . . . . . $-40^oC \le T_A \le +85^oC$
Storage Temperature Range . . . . . $-65^oC \le T_A \le +150^oC$

Thermal Package Resistance (°C/W)	θ_{JA}	θ_{JC}
Plastic DIP	130	N/A
CerDIP	115	35
SOIC	170	N/A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = +15V$, $V- = -15V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \le 10pF$, Unless Otherwise Specified

PARAMETER	TEMPERATURE	HA-5020-5, -9 MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Input Offset Voltage (Notes 2, 20)	+25°C	-	2	8	mV
	Full	-	-	10	mV
Average Input Offset Voltage Drift	Full	-	10	-	µV/°C
V_{IO} Common Mode Rejection Ratio (Notes 3, 20)	+25°C	60	-	-	dB
	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio (Notes 4, 20)	+25°C	64	-	-	dB
	Full	60	-	-	dB
Non-Inverting Input (+IN) Current (Note 20)	+25°C	-	3	8	µA
	Full	-	-	20	µA
+IN Common Mode Rejection (Note 3)	+25°C	-	-	0.1	µA/V
	Full	-	-	0.5	µA/V
+IN Power Supply Rejection (Note 4)	+25°C	-	-	0.06	µA/V
	Full	-	-	0.2	µA/V
Inverting Input (-IN) Current (Note 20)	+25°C	-	12	20	µA
	Full	-	25	50	µA
-IN Common Mode Rejection (Note 3)	+25°C	-	-	0.4	µA/V
	Full	-	-	0.5	µA/V
-IN Power Supply Rejection (Note 4)	+25°C	-	-	0.2	µA/V
	Full	-	-	0.5	µA/V
TRANSFER CHARACTERISTICS					
Transimpedance (Note 20)	+25°C	3500	-	-	V/mA
	Full	1000	-	-	V/mA
Open Loop DC Voltage Gain (Note 12)	+25°C	70	-	-	dB
$R_L = 400\Omega$, $V_{OUT} = \pm 10V$	Full	65	-	-	dB
Open Loop DC Voltage Gain	+25°C	60	-	-	dB
$R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$	Full	55	-	-	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Notes 20, 21)	+25°C to +85°C	±12	±12.7	-	V
	-40°C to 0°C	±11	±11.8	-	V
Output Current	+25°C	±30	±31.7	-	mA
(Guaranteed by Output Voltage Test)	Full	±27.5	-	-	mA
POWER SUPPLY CHARACTERISTICS					
Quiescent Supply Current (Note 20)	Full	-	7.5	10	mA
Supply Current, Disabled (Notes 5, 20)	Full	-	5	7.5	mA

Electrical Specifications V+ = +15V, V- = -15V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤ 10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMPERATURE	HA-5020-5, -9			UNITS
		MIN	TYP	MAX	
$\overline{\text{Disable}}$ Pin Input Current (Note 5)	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable (Note 6)	Full	350	-	-	μA
Maximum Pin 8 Current to Enable (Note 7)	Full	-	-	20	μA
AC CHARACTERISTICS (A_V = +1)					
Slew Rate (Note 8)	+25°C	600	800	-	V/μs
	Full	500	700	-	V/μs
Full Power Bandwidth (Note 9)	+25°C	9.6	12.7	-	MHz
(Guaranteed by Slew Rate Test)	Full	8.0	11.1	-	MHz
Rise Time (Note 10)	+25°C	-	5	-	ns
Fall Time (Note 10)	+25°C	-	5	-	ns
Propagation Delay (Notes 10, 20)	+25°C	-	6	-	ns
-3dB Bandwidth (Notes 11, 20)	+25°C	-	100	-	MHz
Settling Time to 1%, 10V Output Step	+25°C	-	45	-	ns
Settling Time to 0.25%, 10V Output Step	+25°C	-	100	-	ns
AC CHARACTERISTICS (A_V = +10, R_F = 383Ω)					
Slew Rate (Notes 8, 12)	+25°C	900	1100	-	V/μs
	Full	700	-	-	V/μs
Full Power Bandwidth (Note 9)	+25°C	14.3	17.5	-	MHz
(Guaranteed by Slew Rate Test)	Full	11.1	-	-	MHz
Rise Time (Note 10)	+25°C	-	8	-	ns
Fall Time (Note 10)	+25°C	-	8	-	ns
Propagation Delay (Notes 10, 20)	+25°C	-	9	-	ns
-3dB Bandwidth (Note 11)	+25°C	-	60	-	MHz
Settling Time to 1%, 10V Output Step	+25°C	-	55	-	ns
Settling Time to 0.1%, 10V Output Step	+25°C	-	90	-	ns
HARRIS VALUE ADDED SPECIFICATIONS					
Input Noise Voltage (f = 1kHz) (Note 20)	+25°C	-	4.5	-	nV/√Hz
+Input Noise Current (f = 1kHz) (Note 20)	+25°C	-	2.5	-	pA/√Hz
-Input Noise Current (f = 1kHz) (Note 20)	+25°C	-	25	-	pA/√Hz
Input Common Mode Range	Full	±10	±12	-	V
-Ibias Adjust Range (Note 2)	Full	±25	±40	-	μA
Overshoot (Note 20)	+25°C	-	7	-	%
Output Current (Short Circuit, Notes 13, 20)	Full	±50	±65	-	mA
Output Current (Disabled, Notes 5, 14, 20)	Full	-	-	1	μA
Output Disable Time (Notes 15, 20)	+25°C	-	10	-	μs
Output Enable Time (Notes 16, 20)	+25°C	-	200	-	ns
Supply Voltage Range	+25°C	5	-	15	V
Output Capacitance (Disabled, Notes 5, 29)	+25°C	-	15	-	pF
VIDEO CHARACTERISTICS					
Differential Gain (Notes 18, 20, 21)	+25°C	-	0.03	-	%
Differential Phase (Notes 18, 20, 21)	+25°C	-	0.03	-	Degrees
Gain Flatness to 5MHz	+25°C	-	0.1	-	dB

Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified. Parameters are not tested. The limits are guaranteed based on lab characterizations, and reflect lot-to-lot variation.

PARAMETER	TEMPERATURE	HA-5020-5, -9			UNITS
		MIN	TYP	MAX	
INPUT CHARACTERISTICS					
Input Offset Voltage (Notes 2, 20)	+25°C	-	2	8	mV
	Full	-	-	10	mV
Average Input Offset Voltage Drift	Full	-	10	-	µV/°C
V_{IO} Common Mode Rejection Ratio (Notes 20, 22)	+25°C	50	-	-	dB
	Full	35	-	-	dB
V_{IO} Power Supply Rejection Ratio (Notes 20, 23)	+25°C	55	-	-	dB
	Full	50	-	-	dB
Non-Inverting Input (+IN) Current (Note 20)	+25°C	-	3	8	µA
	Full	-	-	20	µA
+IN Common Mode Rejection (Note 22)	+25°C	-	-	0.1	µA/V
	Full	-	-	0.5	µA/V
+IN Power Supply Rejection (Note 23)	+25°C	-	-	0.06	µA/V
	Full	-	-	0.2	µA/V
Inverting Input (-IN) Current (Note 20)	+25°C	-	12	20	µA
	Full	-	25	50	µA
-IN Common Mode Rejection (Note 22)	+25°C	-	-	0.4	µA/V
	Full	-	-	0.5	µA/V
-IN Power Supply Rejection (Note 23)	+25°C	-	-	0.2	µA/V
	Full	-	-	0.5	µA/V
TRANSFER CHARACTERISTICS					
Transimpedance (Note 20)	+25°C	1000	-	-	V/mA
	Full	850	-	-	V/mA
Open Loop DC Voltage Gain	+25°C	65	-	-	dB
$R_L = 400\Omega$, $V_{OUT} = \pm 2.5V$	Full	60	-	-	dB
Open Loop DC Voltage Gain	+25°C	50	-	-	dB
$R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$	Full	45	-	-	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing (Note 20)	+25°C to +85°C	±2.5	±3.0	-	V
	-40°C to 0°C	±2.5	±3.0	-	V
Output Current (Note 21)	+25°C	±16.6	±20	-	mA
(Guaranteed by Output Voltage Test)	Full	±16.6	±20	-	mA
POWER SUPPLY CHARACTERISTICS					
Quiescent Supply Current (Note 20)	Full	-	7.5	10	mA
Supply Current, Disabled (Notes 5, 20)	Full	-	5	7.5	mA
$\overline{\text{Disable}}$ Pin Input Current (Note 5)	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable (Note 25)	Full	350	-	-	µA
Maximum Pin 8 Current to Enable (Note 7)	Full	-	-	20	µA

Electrical Specifications V+ = +5V, V- = -5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤10pF, Unless Otherwise Specified. Parameters are not tested. The limits are guaranteed based on lab characterizations, and reflect lot-to-lot variation. **(Continued)**

PARAMETER	TEMPERATURE	HA-5020-5, -9			UNITS
		MIN	TYP	MAX	
AC CHARACTERISTICS (A_V = +1)					
Slew Rate (Note 26)	+25°C	215	400	-	V/µs
Full Power Bandwidth (Note 27)	+25°C	22	28	-	MHz
Rise Time (Note 10)	+25°C	-	6	-	ns
Fall Time (Note 10)	+25°C	-	6	-	ns
Propagation Delay (Note 10)	+25°C	-	6	-	ns
Overshoot	+25°C	-	4.5	-	%
-3dB Bandwidth (Notes 11, 20)	+25°C	-	125	-	MHz
Settling Time to 1%, 2V Output Step	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step	+25°C	-	75	-	ns
AC CHARACTERISTICS (A_V = +2, R_F = 681Ω)					
Slew Rate (Note 26)	+25°C	-	475	-	V/µs
Full Power Bandwidth (Note 27)	+25°C	-	26	-	MHz
Rise Time (Note 10)	+25°C	-	6	-	ns
Fall Time (Note 10)	+25°C	-	6	-	ns
Propagation Delay (Note 10)	+25°C	-	6	-	ns
Overshoot	+25°C	-	12	-	%
-3dB Bandwidth (Note 11)	+25°C	-	95	-	MHz
Settling Time to 1%, 2V Output Step	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step	+25°C	-	100	-	ns
AC CHARACTERISTICS (A_V = +10, R_F = 383Ω)					
Slew Rate (Note 26)	+25°C	350	475	-	V/µs
Full Power Bandwidth (Note 27)	+25°C	28	38	-	MHz
Rise Time (Note 10)	+25°C	-	8	-	ns
Fall Time (Note 10)	+25°C	-	9	-	ns
Propagation Delay (Note 10)	+25°C	-	9	-	ns
Overshoot	+25°C	-	1.8	-	%
-3dB Bandwidth (Notes 11, 20)	+25°C	-	65	-	MHz
Settling Time to 1%, 2V Output Step	+25°C	-	75	-	ns
Settling Time to 0.1%, 2V Output Step	+25°C	-	130	-	ns
HARRIS VALUE ADDED SPECIFICATIONS					
Input Noise Voltage (f = 1kHz) (Note 20)	+25°C	-	4.5	-	nV/√Hz
+Input Noise Current (f = 1kHz) (Note 20)	+25°C	-	2.5	-	pA/√Hz
-Input Noise Current (f = 1kHz) (Note 20)	+25°C	-	25	-	pA/√Hz
Input Common Mode Range	Full	±2.5V	–	-	V
Output Current (Short Circuit, Note 24)	Full	±40	±60	-	mA
Output Current (Disabled, Notes 5, 20, 24)	Full	-	-	2	µA
Output Disable Time (Notes 20, 29)	+25°C	-	40	-	µs

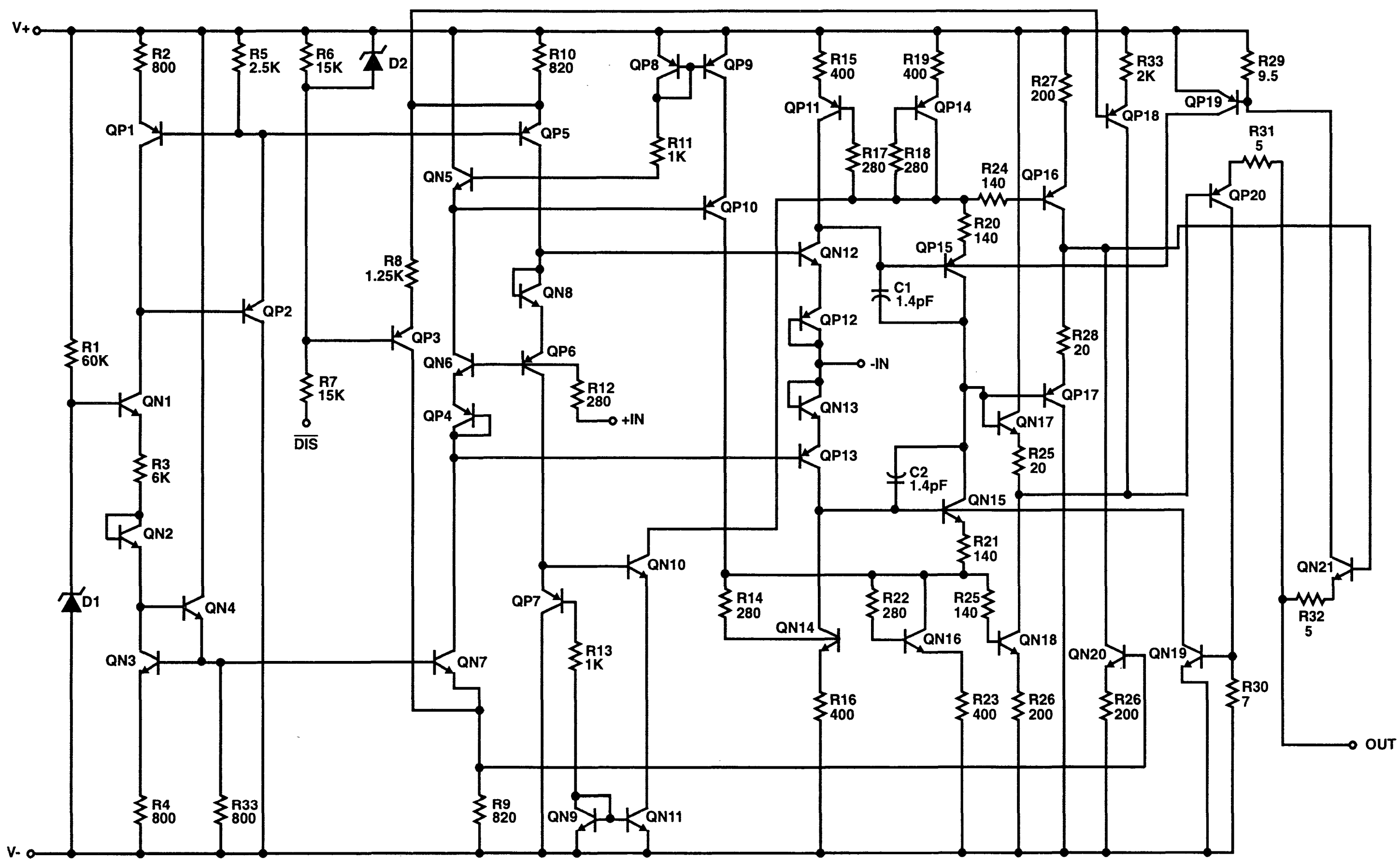
Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \le 10pF$, Unless Otherwise Specified. Parameters are not tested. The limits are guaranteed based on lab characterizations, and reflect lot-to-lot variation. **(Continued)**

PARAMETER	TEMPERATURE	HA-5020-5, -9			UNITS
		MIN	TYP	MAX	
Output Enable Time (Notes 20, 30)	+25°C	-	40	-	ns
Supply Voltage Range	+25°C	5	-	15	V
Output Capacitance (Disabled, Notes 5, 17)	+25°C	-	15	-	pF
VIDEO CHARACTERISTICS					
Differential Gain (Notes 18, 20, 21)	+25°C	-	0.03	-	%
Differential Phase (Notes 18, 20, 21)	+25°C	-	0.03	-	Degrees
Gain Flatness to 5MHz	+25°C	-	0.1	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Suggested V_{OS} Adjust Circuit: The inverting input current (-Ibias) can be adjusted with an external 10kΩ pot between pins 1 and 5, wiper connected to V+. Since -Ibias flows through the feedback resistor (R_F), the result is an adjustment in offset voltage. The amount of offset voltage adjustment is determined by the value of R_F ($\Delta V_{OS} = \Delta\text{-Ibias}^*R_F$).
3. $V_{CM} = \pm 10V$.
4. $\pm 4.5V \le V_S \le \pm 18V$.
5. $\overline{\text{Disable}} = 0V$.
6. $R_L = 100\Omega$, $V_{IN} = 10V$. This is the minimum current which must be pulled out of the $\overline{\text{Disable}}$ pin in order to disable the output. The output is considered disabled when $-10mV \le V_{OUT} \le +10mV$.
7. $V_{IN} = 0V$. This is the maximum current that can be pulled out of the $\overline{\text{Disable}}$ pin with the HA-5020 remaining enabled. The HA-5020 is considered disabled when the supply current has decreased by at least 0.5mA.
8. V_{OUT} switches from -10V to +10V, or from +10V to -10V. Specification is from the 25% to 75% points.
9. $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $V_{PEAK} = 10V$.
10. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
11. $R_L = 400\Omega$, $V_{OUT} = 100mV$.
12. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
13. $V_{IN} = \pm 10V$, $V_{OUT} = 0V$.
14. $V_{OUT} = \pm 10V$.
15. $V_{IN} = +10V$, $\overline{\text{Disable}} = +15V$ to 0V. Measured from the 50% point of $\overline{\text{Disable}}$ to $V_{OUT} = 0V$.
16. $V_{IN} = +10V$, $\overline{\text{Disable}} = 0V$ to +15V. Measured from the 50% point of $\overline{\text{Disable}}$ to $V_{OUT} = 10V$.
17. $V_{IN} = 0V$, Force V_{OUT} from 0V to ±10V, $t_R = t_F = 50ns$.
18. Measured with a VM700A video tester using a NTC-7 composite VITS.
19. Maximum power dissipation, including output load, must be designed to maintain junction temperature below +175°C for ceramic packages, and below +150°C for plastic packages.
20. See "Typical Performance Curves" for more information.
21. $R_L = 150\Omega$
22. $V_{CM} = \pm 2.5V$. At -40°C product is tested at $V_{CM} = \pm 2.25V$ because short test duration does not allow self heating.
23. $\pm 3.5V \le V_S \le \pm 6.5V$.
24. $V_{OUT} = \pm 2.5V$, $V_{IN} = 0$.
25. $R_L = 100\Omega$. $V_{IN} = 2.5V$. This is the minimum current which must be pulled out of the $\overline{\text{Disable}}$ pin in order to disable the output. The output is considered disabled when $-10mV \le V_{OUT} \le +10mV$.
26. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
27. $FPBW = \frac{\text{SlewRate}}{2\pi V_{PEAK}}$; $V_{PEAK} = 2V$
28. $V_{IN} = 0V$, Force V_{OUT} from 0V to ±2.5V, $t_R = t_F = 50ns$.
29. $V_{IN} = +2V$, $\overline{\text{Disable}} = +5V$ to 0V. Measured from the 50% point of $\overline{\text{Disable}}$ to $V_{OUT} = 0V$.
30. $V_{IN} = +2V$, $\overline{\text{Disable}} = 0V$ to +5V. Measured from the 50% point of $\overline{\text{Disable}}$ to $V_{OUT} = 2V$.

Schematic


V+
V-
R1 60K
R2 800
R3 6K
R4 800
R5 2.5K
R6 15K
R7 15K
R8 1.25K
R9 820
R10 820
R11 1K
R12 280
R13 1K
R14 280
R15 400
R16 400
R17 280
R18 280
R19 400
R20 140
R21 140
R22 280
R23 400
R24 140
R25 140
R25 20
R26 200
R26 200
R27 200
R28 20
R29 9.5
R30 7
R31 5
R32 5
R33 2K
R33 800
D1
D2
C1 1.4pF
C2 1.4pF
QP1
QP2
QP3
QP4
QP5
QP6
QP7
QP8
QP9
QP10
QP11
QP12
QP13
QP14
QP15
QP16
QP17
QP18
QP19
QP20
QN1
QN2
QN3
QN4
QN5
QN6
QN7
QN8
QN9
QN10
QN11
QN12
QN13
QN14
QN15
QN16
QN17
QN18
QN19
QN20
QN21
DIS
+IN
-IN
OUT

Die Characteristics

DIE DIMENSIONS:
1640μm x 1520μm x 483μm ±25.4μm

METALLIZATION:
Type: Aluminum, 1% Copper
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
5.77×10^4 A/cm^2 at 30mA

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Nitride over Silox
Silox Thickness: 12kÅ ± 2kÅ
Nitride Thickness: 3.5kÅ ± 1kÅ

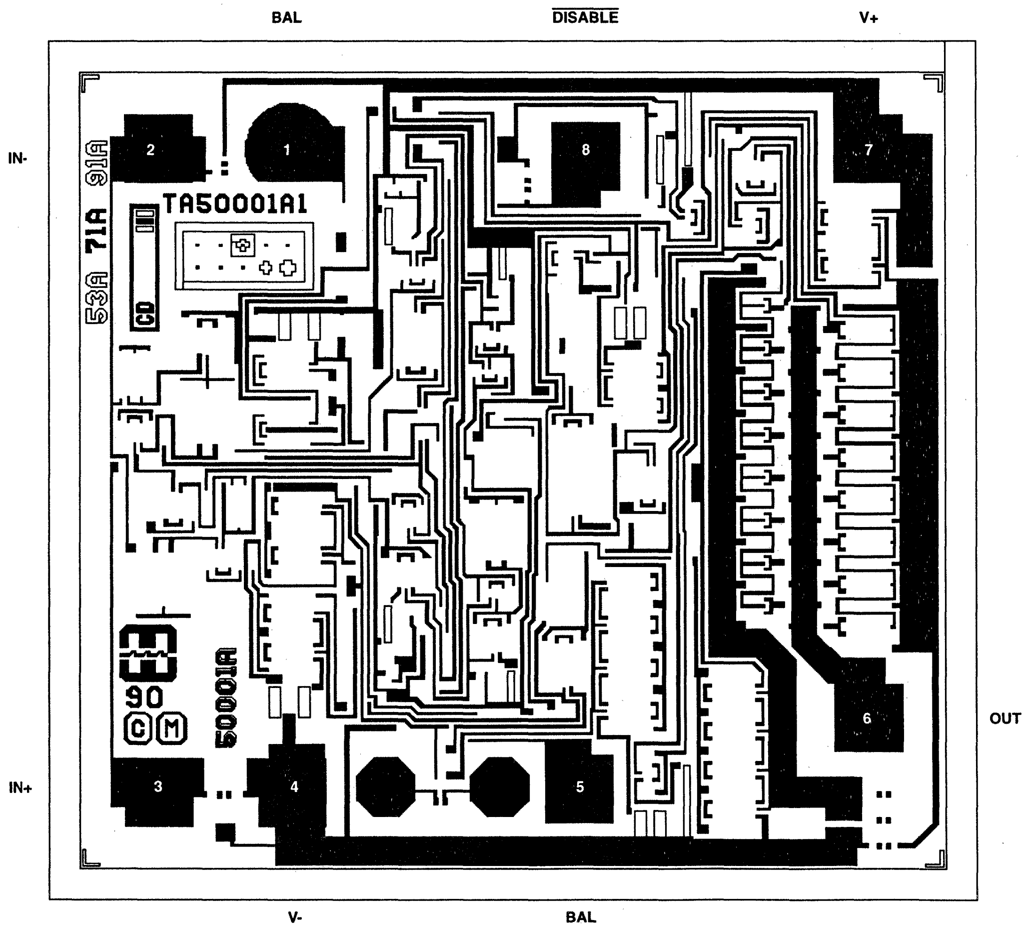
TRANSISTOR COUNT: 62

PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC

Metallization Mask Layout

HA-5020



Test Circuits

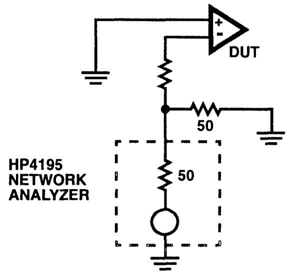


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

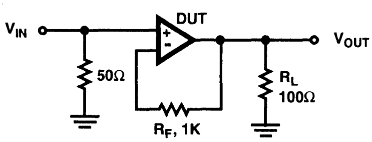


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

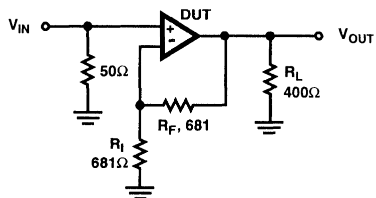


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT

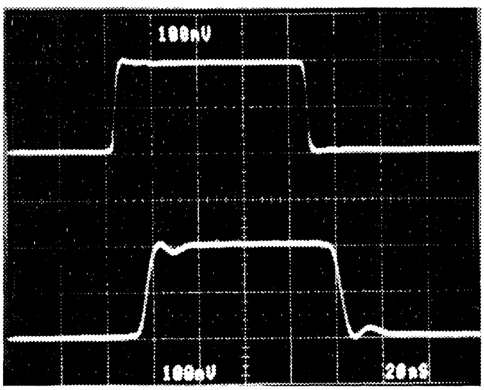


FIGURE 4. SMALL SIGNAL RESPONSE
Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

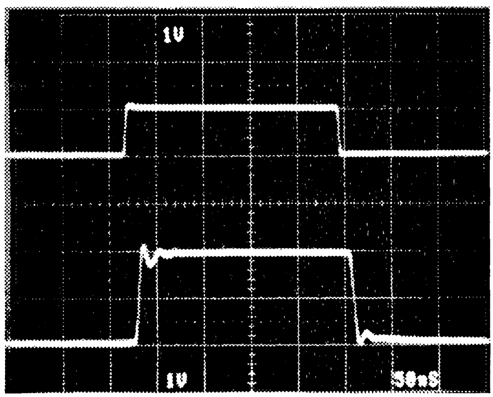


FIGURE 5. LARGE SIGNAL RESPONSE
Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25^oC$, Unless Otherwise Specified

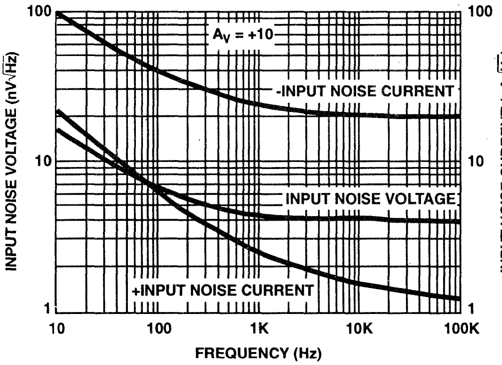


FIGURE 6. INPUT NOISE vs FREQUENCY
(Average of 18 Units from 3 Lots)

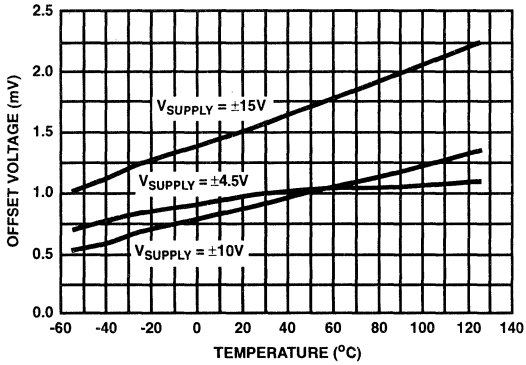


FIGURE 7. INPUT OFFSET VOLTAGE vs TEMPERATURE
(Absolute Value Average of 30 Units from 3 Lots)

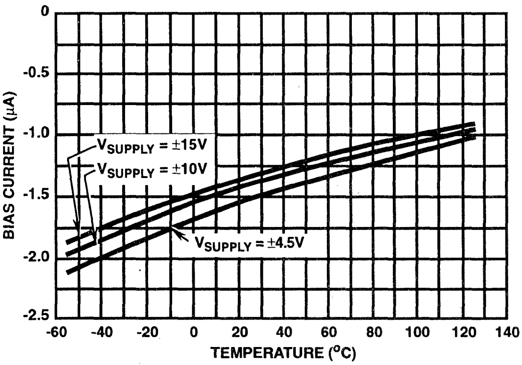


FIGURE 8. +INPUT BIAS CURRENT vs TEMPERATURE
Average of 30 Units from 3 Lots

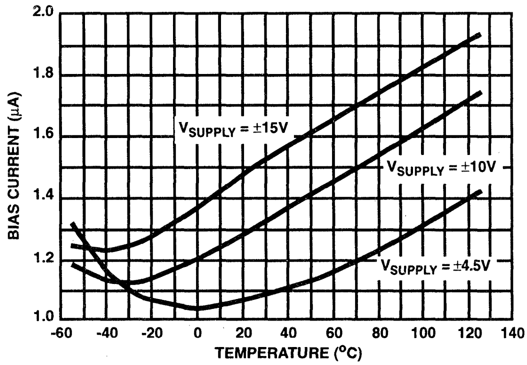


FIGURE 9. -INPUT BIAS CURRENT vs TEMPERATURE
Absolute Value Average of 30 Units from 3 Lots

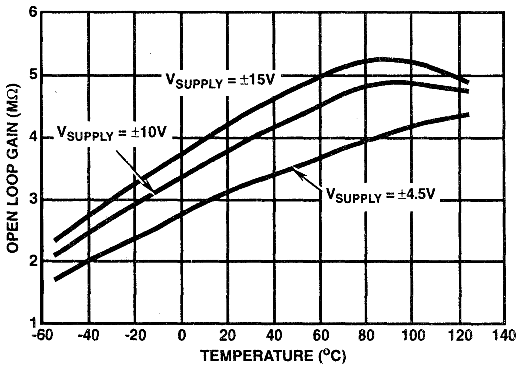


FIGURE 10. TRANSIMPEDANCE vs TEMPERATURE
Average of 30 Units from 3 Lots

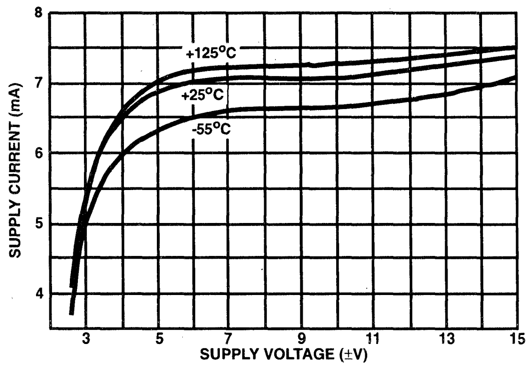


FIGURE 11. SUPPLY CURRENT vs SUPPLY VOLTAGE
Average of 30 Units from 3 Lots

Typical Performance Curves V_{SUPPLY} = ±15V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = +25°C, Unless Otherwise Specified **(Continued)**

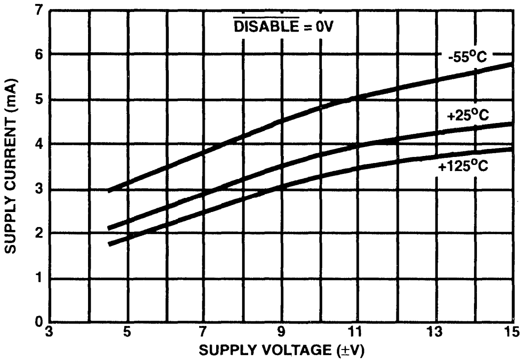


FIGURE 12. DISABLE SUPPLY CURRENT vs SUPPLY VOLTAGE
Average of 30 Units from 3 Lots

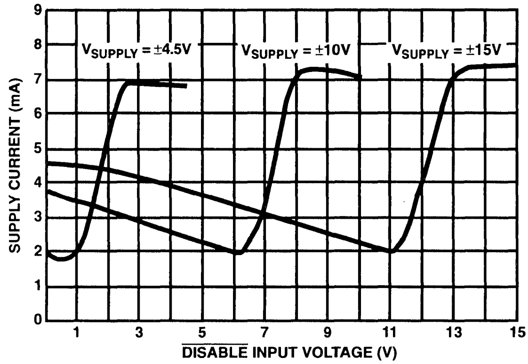


FIGURE 13. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

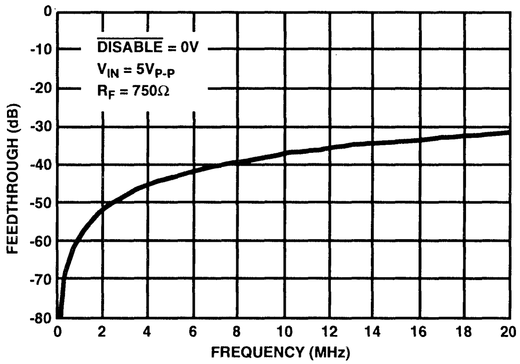


FIGURE 14. DISABLE MODE FEEDTHROUGH vs FREQUENCY

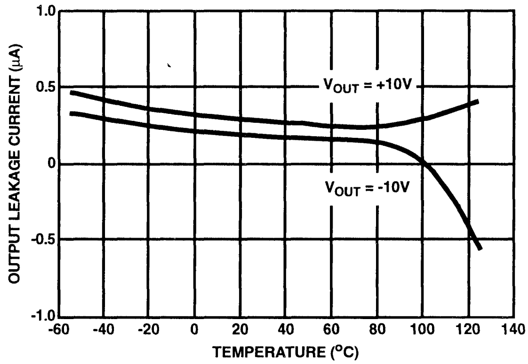


FIGURE 15. DISABLED OUTPUT LEAKAGE vs TEMPERATURE
Average of 30 Units from 3 Lots

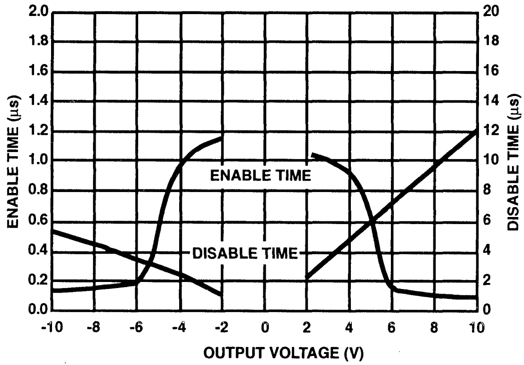


FIGURE 16. ENABLE/DISABLE TIME vs OUTPUT VOLTAGE
Average of 9 Units from 3 Lots

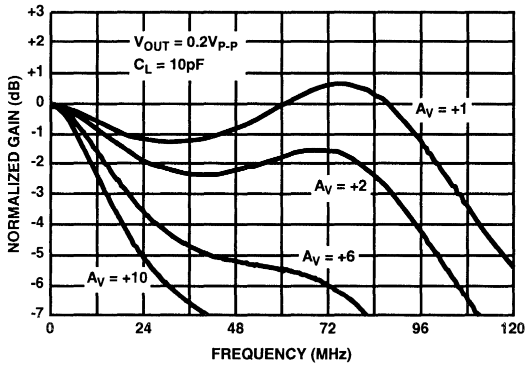


FIGURE 17. NON-INVERTING GAIN vs FREQUENCY

2
OPERATIONAL AMPLIFIERS

Typical Performance Curves V_{SUPPLY} = ±15V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = +25°C, Unless Otherwise Specified **(Continued)**

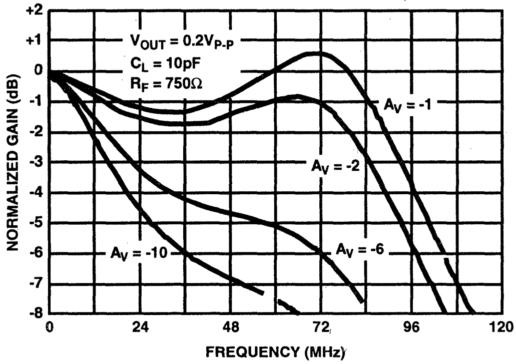


FIGURE 18. INVERTING FREQUENCY RESPONSE

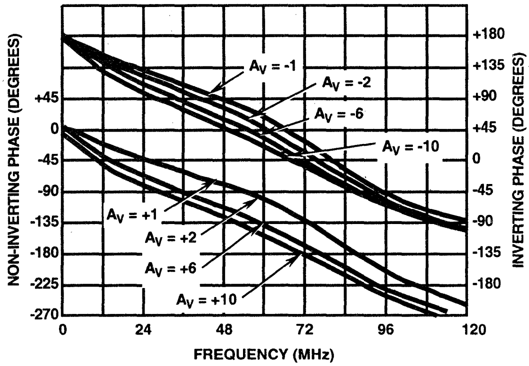


FIGURE 19. PHASE vs FREQUENCY

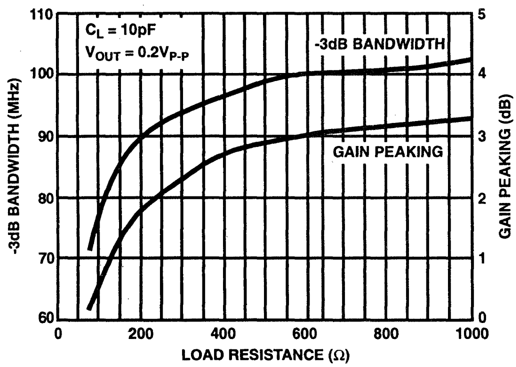


FIGURE 20. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

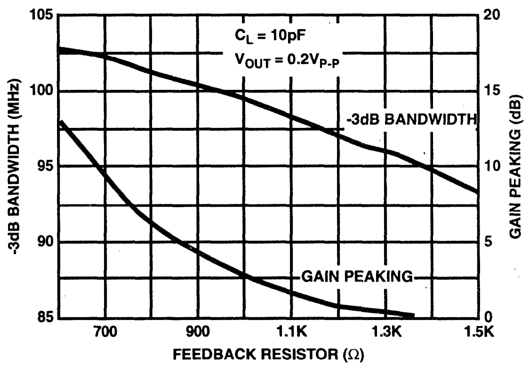


FIGURE 21. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

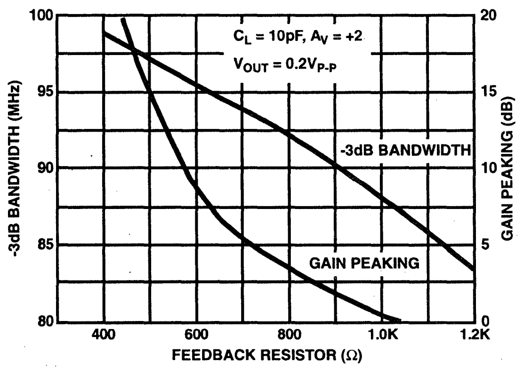


FIGURE 22. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

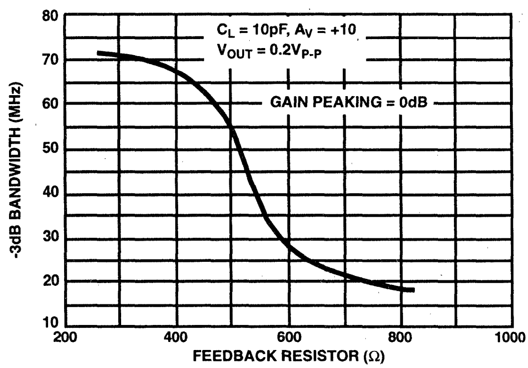


FIGURE 23. BANDWIDTH vs FEEDBACK RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25^oC$, Unless Otherwise Specified **(Continued)**

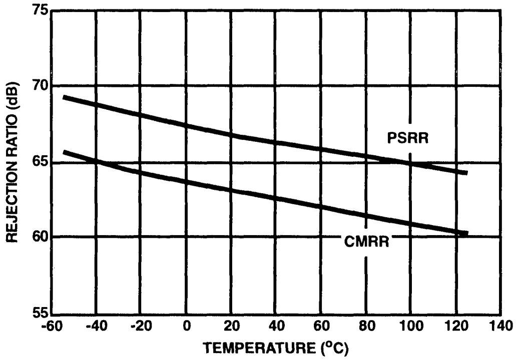


FIGURE 24. REJECTION RATIOS vs TEMPERATURE
Average of 30 Units from 3 Lots

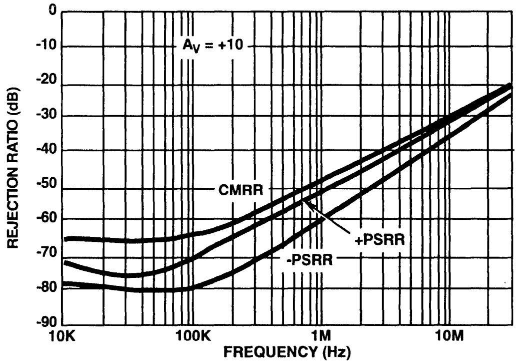


FIGURE 25. REJECTION RATIOS vs FREQUENCY

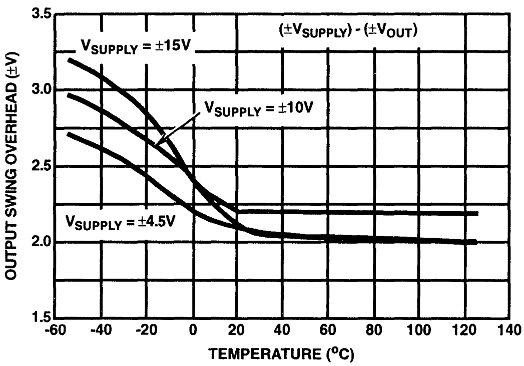


FIGURE 26. OUTPUT SWING OVERHEAD vs TEMPERATURE
Average of 30 Units from 3 Lots

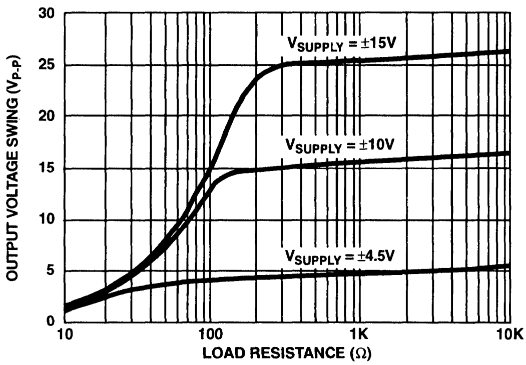


FIGURE 27. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

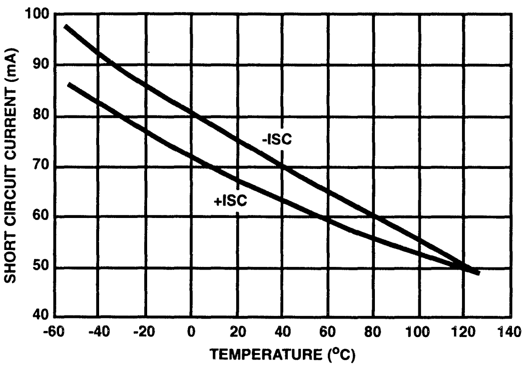


FIGURE 28. SHORT CIRCUIT CURRENT LIMIT vs TEMPERATURE

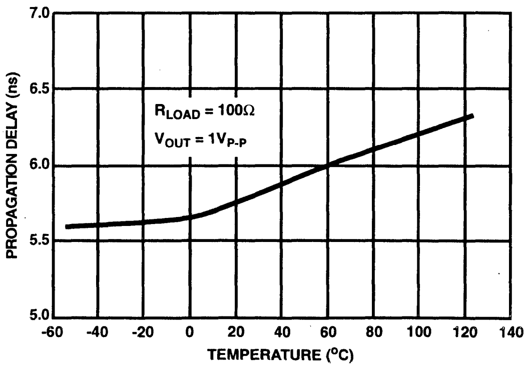


FIGURE 29. PROPAGATION DELAY vs TEMPERATURE
Average of 18 Units from 3 Lots

Typical Performance Curves $V_{SUPPLY} = \pm 15V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25^oC$, Unless Otherwise Specified **(Continued)**

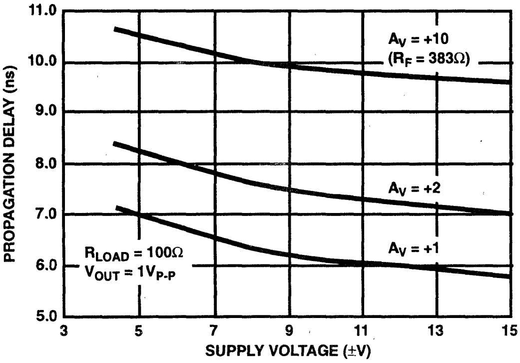


FIGURE 30. PROPAGATION DELAY vs SUPPLY VOLTAGE
Average of 18 Units From 3 Lots

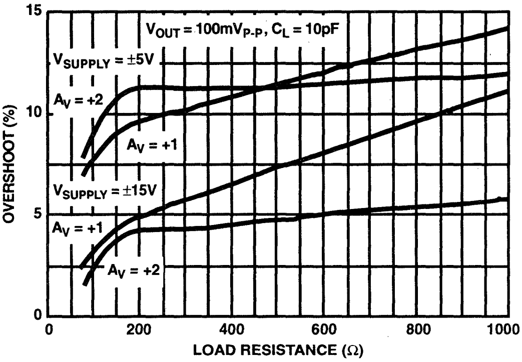


FIGURE 31. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

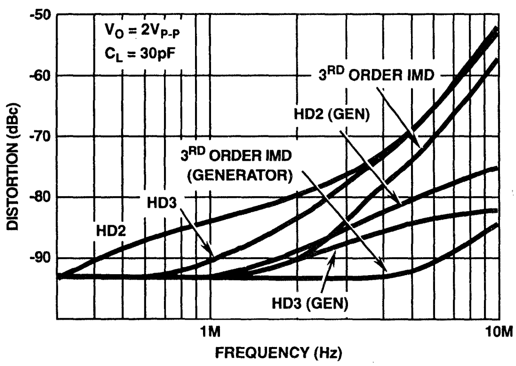


FIGURE 32. DISTORTION vs FREQUENCY

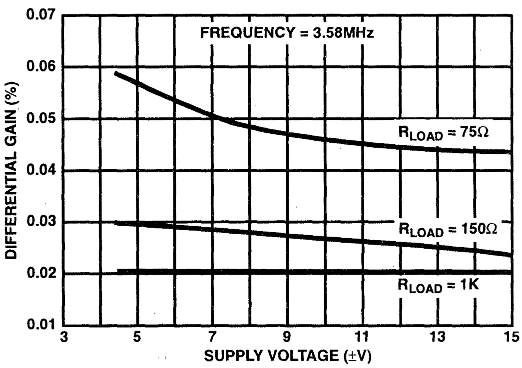


FIGURE 33. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE
Average of 18 Units from 3 Lots

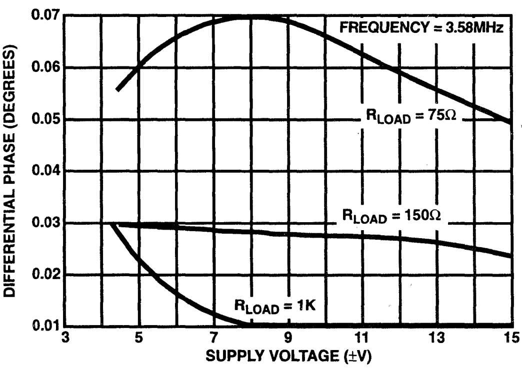


FIGURE 34. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE
Average of 18 Units from 3 Lots

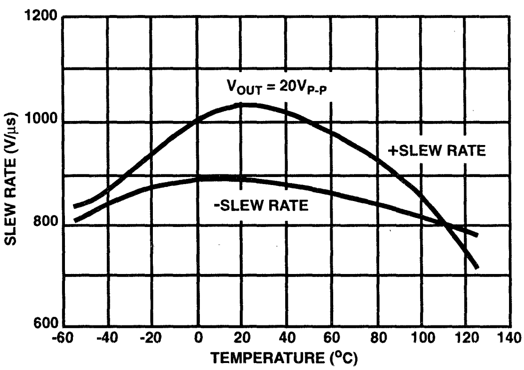


FIGURE 35. SLEW RATE vs TEMPERATURE
Average of 30 Units from 3 Lots

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25^oC$, Unless Otherwise Specified

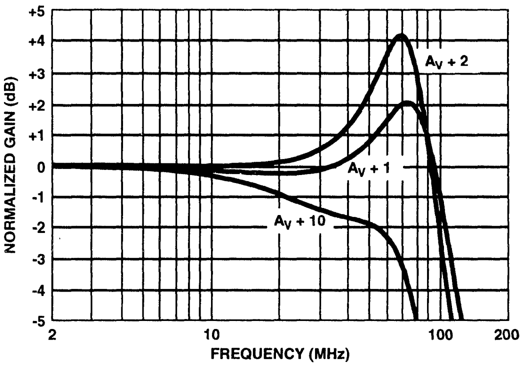


FIGURE 36. NON-INVERTING FREQUENCY RESPONSE

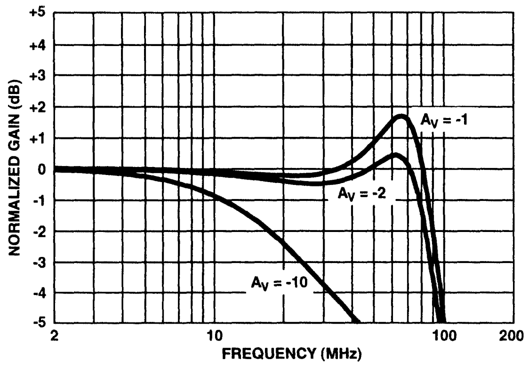


FIGURE 37. INVERTING FREQUENCY RESPONSE

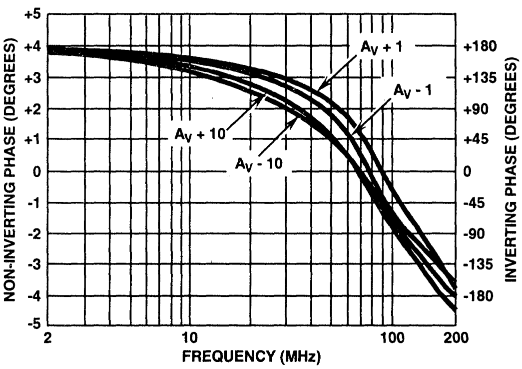


FIGURE 38. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

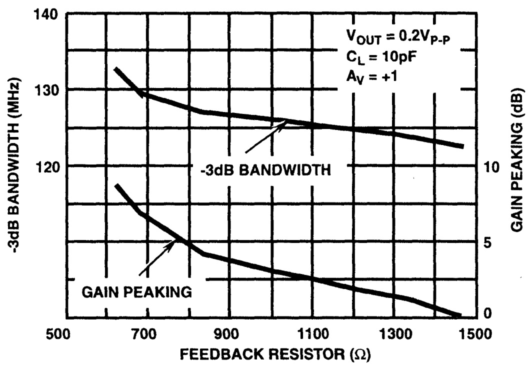


FIGURE 39. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

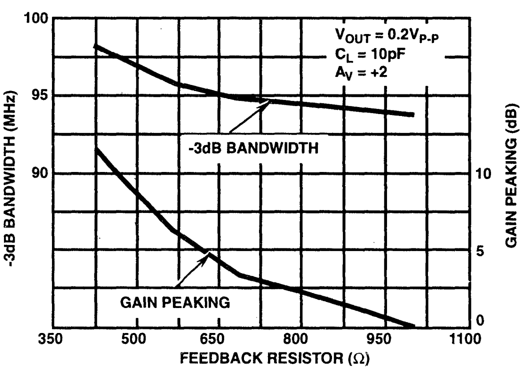


FIGURE 40. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

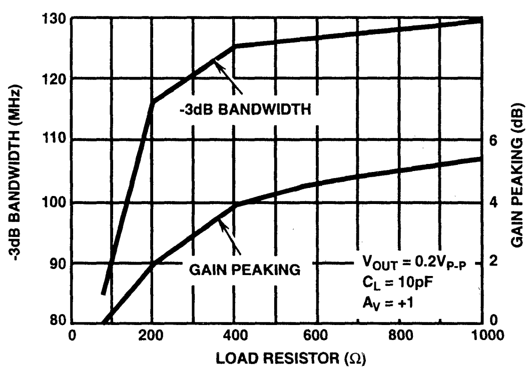


FIGURE 41. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25^oC$, Unless Otherwise Specified **(Continued)**

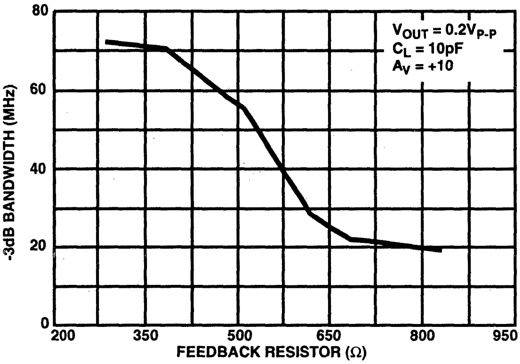


FIGURE 42. BANDWIDTH vs FEEDBACK RESISTANCE

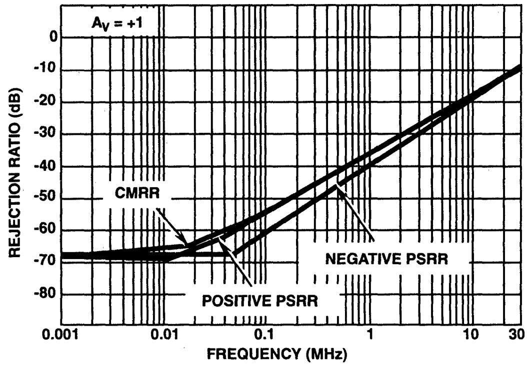


FIGURE 43. REJECTION RATIOS vs FREQUENCY

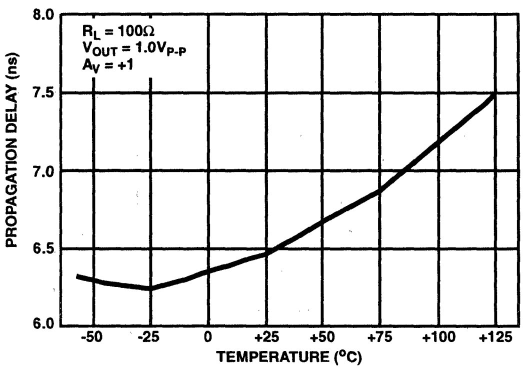


FIGURE 44. PROPAGATION DELAY vs TEMPERATURE

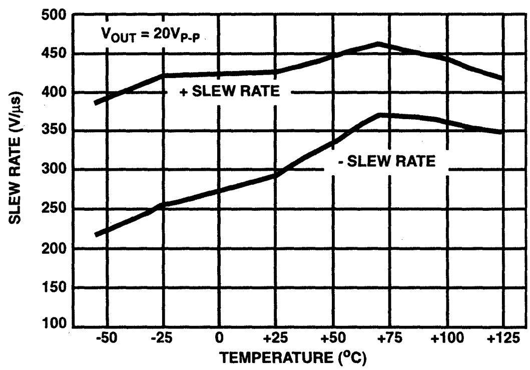


FIGURE 45. SLEW RATE vs TEMPERATURE

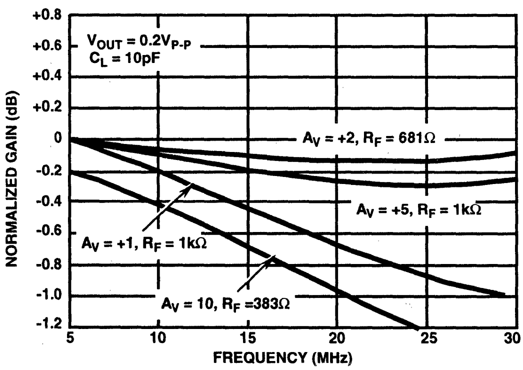


FIGURE 46. NON-INVERTING GAIN FLATNESS vs FREQUENCY

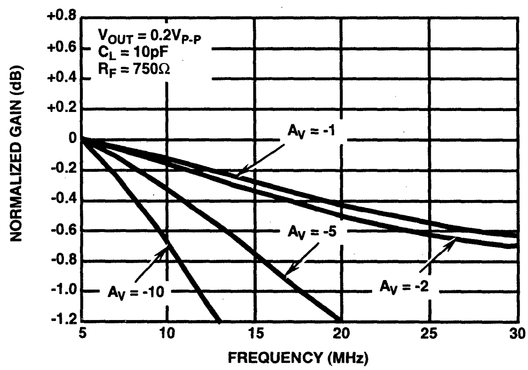


FIGURE 47. INVERTING GAIN FLATNESS vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = +25^oC$, Unless Otherwise Specified **(Continued)**

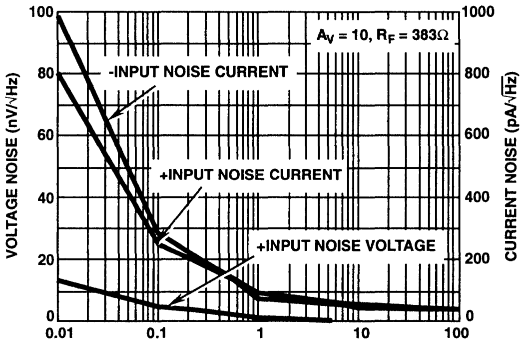


FIGURE 48. INPUT NOISE CHARACTERISTICS

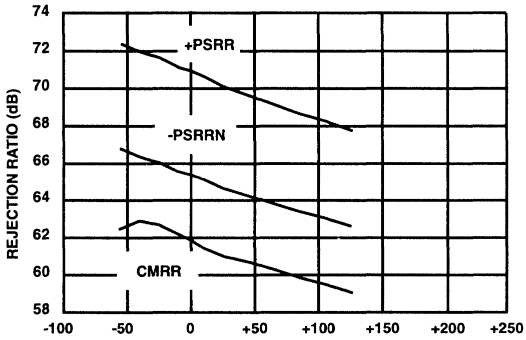


FIGURE 49. REJECTION RATIO vs TEMPERATURE

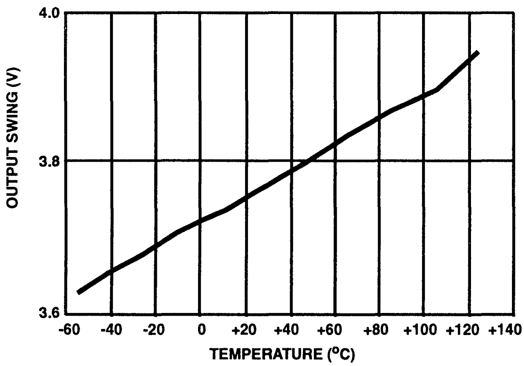


FIGURE 50. OUTPUT SWING vs TEMPERATURE

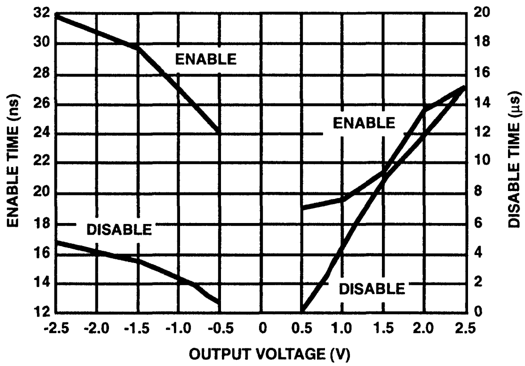


FIGURE 51. ENABLE/DISABLE TIME vs OUTPUT VOLTAGE

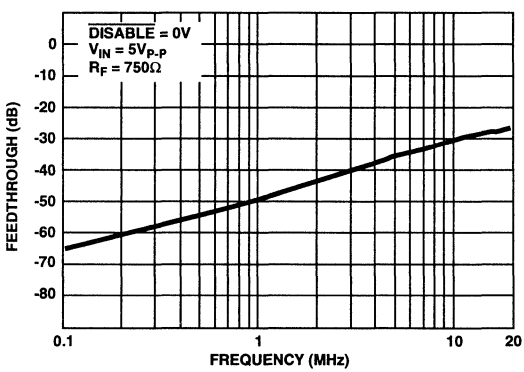


FIGURE 52. DISABLE FEEDTHROUGH vs FREQUENCY

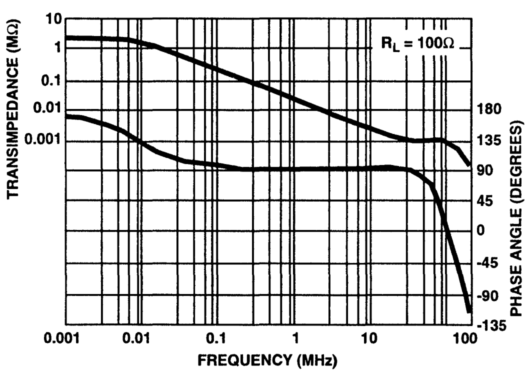


FIGURE 53. TRANSIMPEDANCE vs FREQUENCY

Typical Performance Curves V_{SUPPLY} = ±5V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = +25°C, Unless Otherwise Specified **(Continued)**

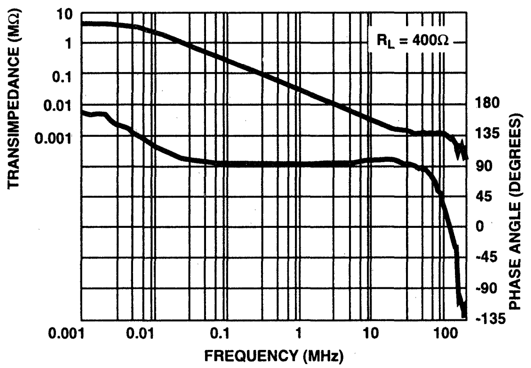


FIGURE 54. TRANSIMPEDENCE vs FREQUENCY

Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response illustrate the performance of the HA-5020 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA-5020 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10µF) tantalum or electrolytic capacitor in parallel with a small value (0.1µF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 55.

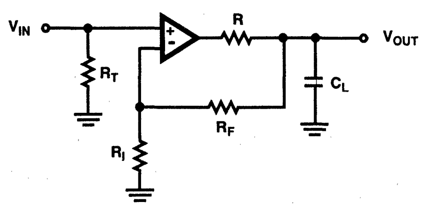


FIGURE 55. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Enable/Disable Function

When enabled the amplifier functions as a normal current feedback amplifier with all of the data in the electrical specifications table being valid and applicable. When disabled the amplifier output assumes a true high impedance state and the supply current is reduced significantly.

The circuit shown in Figure 56 is a simplified schematic of the enable/disable function. The large value resistors in series with the DISABLE pin makes it appear as a current source to the driver. When the driver pulls this pin low current flows out of the pin and into the driver. This current, which may be as large as 350µA when external circuit and process variables are at their extremes, is required to insure that point "A" achieves the proper potential to disable the output. The driver must have the compliance and capability of sinking all of this current.

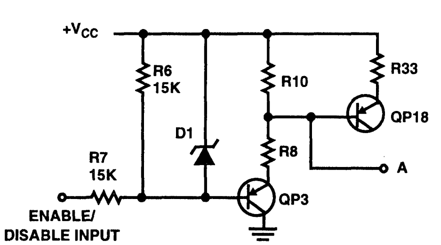


FIGURE 56. SIMPLIFIED SCHEMATIC OF ENABLE/DISABLE FUNCTION

When V_{CC} is +5V the DISABLE pin may be driven with a dedicated TTL gate. The maximum low level output voltage of the TTL gate, 0.4V, has enough compliance to insure that the amplifier will always be disabled even though D1 will not turn on, and the TTL gate will sink enough current to keep point "A" at its proper voltage. When V_{CC} is greater than +5 volts the DISABLE pin should be driven with an open collector device that has a breakdown rating greater than V_{CC}.

Referring to Figure 56, it can be seen that R6 will act as a pull-up resistor to $+V_{CC}$ if the DISABLE pin is left open. In those cases where the enable/disable function is not required on all circuits some circuits can be permanently enabled by letting the DISABLE pin float. If a driver is used to set the enable/disable level, be sure that the driver does not sink more than 20µA when the DISABLE pin is at a high level. TTL gates, especially CMOS versions, do not violate this criteria so it is permissible to control the enable/disable function with TTL.

Two Channel Video Multiplexer

Referring to the amplifier U1A in Figure 57, R1 terminates the cable in its characteristic impedance of 75Ω, and R4 back terminates the cable in its characteristic impedance. The amplifier is set up in a gain configuration of +2 to yield an overall network gain of +1 when driving a double terminated cable. The value of R3 can be changed if a different network gain is desired. R5 holds the disable pin at ground thus inhibiting the amplifier until the switch, S1, is thrown to position 1. At position 1 the switch pulls the disable pin up to the plus supply rail thereby enabling the amplifier. Since all of the actual signal switching takes place within the amplifier, it's differential gain and phase parameters, which are 0.03% and 0.03 degrees respectively, determine the circuit's performance. The other circuit, U1b, operates in a similar manner.

When the plus supply rail is 5V the disable pin can be driven by a dedicated TTL gate as discussed earlier. If a multiplexer IC or its equivalent is used to select channels its logic must be break before make. When these conditions are satisfied the HA-5020 is often used as a remote video multiplexer, and the multiplexer may be extended by adding more amplifier ICs.

Low Impedance Multiplexer

Two common problems surface when you try to multiplex multiple high speed signals into a low impedance source such as an A/D converter. The first problem is the low source impedance which tends to make amplifiers oscillate and causes gain errors. The second problem is the multiplexer which supplies no gain, introduces all kinds of distortion and limits the frequency response. Using op amps which have an enable/disable function, such as the HA-5020, eliminates the multiplexer problems because the external mux chip is not needed, and the HA-5020 can drive low impedance (large capacitance) loads if a series isolation resistor is used.

Referring to Figure 58, both inputs are terminated in their characteristic impedance; 75Ω is typical for video applications. Since the drivers usually are terminated in their characteristic impedance the input gain is 0.5, thus the amplifiers, U2, are configured in a gain of +2 to set the circuit gain equal to one. Resistors R2 and R3 determine the amplifier gain, and if a different gain is desired R2 should be changed according to the equation G = (1 + R3/R2). R3 sets the frequency response of the amplifier so you should refer to the manufacturers data sheet before changing it's value. R5, C1 and D1 are an asymmetrical charge/discharge time circuit which configures U1 as a break before make switch to prevent both amplifiers from being active simultaneously. If this design is extended to more channels the drive logic must be designed to be break before make. R4 is enclosed in the feedback loop of the amplifier so that the large open loop amplifier gain of U2 will present the load with a small closed loop output impedance while keeping the amplifier stable for all values of load capacitance.

The circuit shown in Figure 58 was tested for the full range of capacitor values with no oscillations being observed; thus, problem one has been solved. The frequency and gain characteristics of the circuit are now those of the amplifier and independent of any multiplexing action; thus, problem two has been solved. The multiplexer transition time is approximately 15µs with the component values shown.

2

OPERATIONAL AMPLIFIERS

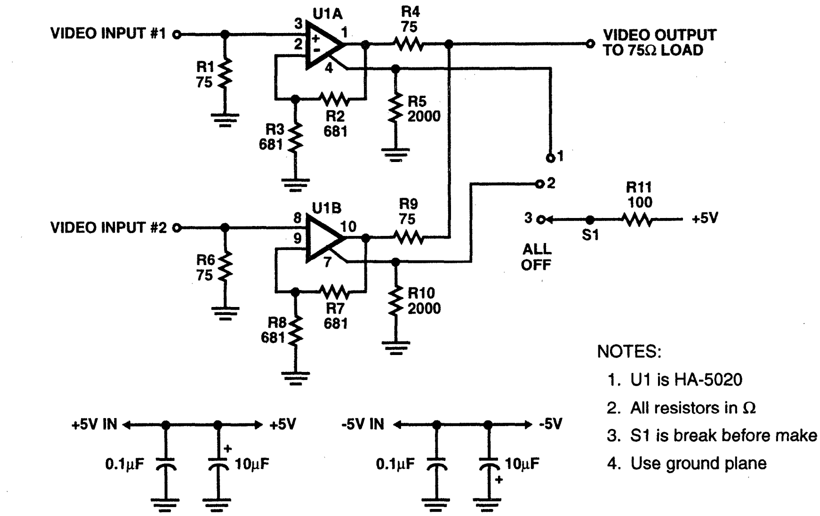


FIGURE 57. TWO CHANNEL HIGH IMPEDANCE MULTIPLEXER

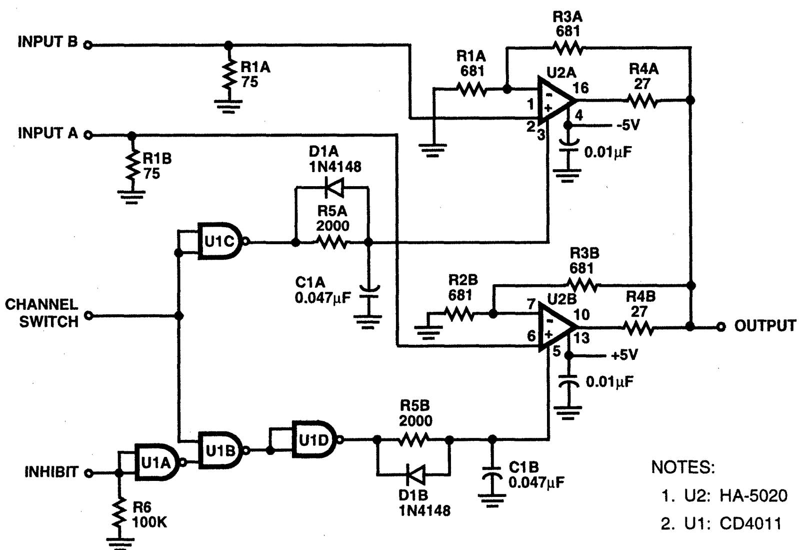


FIGURE 58. LOW IMPEDANCE MULTIPLEXER

HARRIS
SEMICONDUCTOR

HA5022

Dual 125MHz Video Current Feedback Amplifier with Disable

July 1995

Features

- **Dual Version of HA-5020**
- **Individual Output Enable/Disable**
- **Input Offset Voltage 800μV**
- **Wide Unity Gain Bandwidth 125MHz**
- **Slew Rate 475V/μs**
- **Differential Gain 0.03%**
- **Differential Phase. . . . . 0.03 Deg.**
- **Supply Current (per Amplifier) 7.5mA**
- **ESD Protection. 4000V**
- **Guaranteed Specifications at ±5V Supplies**

Applications

- **Video Multiplexers; Video Switching and Routing**
- **Video Gain Block**
- **Video Distribution Amplifier/RGB Amplifier**
- **Flash A/D Driver**
- **Current to Voltage Converter**
- **Medical Imaging**
- **Radar and Imaging Systems**

Description

The HA5022 is a dual version of the popular Harris HA-5020. It features wide bandwidth and high slew rate, and is optimized for video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The HA5022 also features a disable function that significantly reduces supply current while forcing the output to a true high impedance state. This functionality allows 2:1 video multiplexers to be implemented with a single IC.

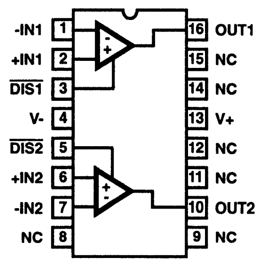
The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor. By reducing R_F, the bandwidth can be increased to compensate for decreases at higher closed loop gains or heavy output loads.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA5022IP	-40°C to +85°C	16 Lead Plastic DIP
HA5022IB	-40°C to +85°C	16 Lead Plastic SOIC (N)

Pinout

HA5022
(PDIP, 150 MIL SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3392.3**

Absolute Maximum Ratings (Note 1)

ESD Protection (Note 15) 2000V
Voltage Between V+ and V- Terminals 36V
DC Input Voltage .... $\pm V_{SUPPLY}$
Differential Input Voltage 10V
Output Current (Note 2) .... Short Circuit Protected
Junction Temperature (Note 19) .... +175°C
Junction Temperature (Plastic Package) (Note 19) .... +150°C
Lead Temperature (Soldering 10s) .... +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HA5022I .... $-40^oC \leq T_A \leq +85^oC$
Supply Voltage Range .... ±4.5V to ±15V
Storage Temperature Range .... $-65^oC \leq T_A \leq +150^oC$
Thermal Package Characteristics (°C/W) θ_{JA}
Plastic DIP 90
SOIC 115

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	(NOTE 12) TEST LEVEL	TEMPERATURE	HA5022I MIN	HA5022I TYP	HA5022I MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage (V_{IO})	A	+25°C	-	0.8	3	mV
	A	Full	-	-	5	mV
Delta V_{IO} Between Channels	A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift	B	Full	-	5	-	µV/°C
V_{IO} Common Mode Rejection Ratio (Note 3)	A	+25°C	53	-	-	dB
	A	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio (Note 4)	A	+25°C	60	-	-	dB
	A	Full	55	-	-	dB
Input Common Mode Range (Note 3)	A	Full	±2.5	-	-	V
Non-Inverting Input (+IN) Current	A	+25°C	-	3	8	µA
	A	Full	-	-	20	µA
+IN Common Mode Rejection (Note 3)	A	+25°C	-	-	0.15	µA/V
($+ I_{BCMR} = \frac{1}{R_{IN}}$)	A	Full	-	-	0.5	µA/V
+IN Power Supply Rejection (Note 4)	A	+25°C	-	-	0.1	µA/V
	A	Full	-	-	0.3	µA/V
Inverting Input (-IN) Current	A	+25°C, +85°C	-	4	12	µA
	A	-40°C	-	10	30	µA
Delta -IN BIAS Current Between Channels	A	+25°C, +85°C	-	6	15	µA
	A	-40°C	-	10	30	µA
-IN Common Mode Rejection (Note 3)	A	+25°C	-	-	0.4	µA/V
	A	Full	-	-	1.0	µA/V
-IN Power Supply Rejection (Note 4)	A	+25°C	-	-	0.2	µA/V
	A	Full	-	-	0.5	µA/V
Input Noise Voltage (f = 1kHz)	B	+25°C	-	4.5	-	$nV/\sqrt{Hz}$
+Input Noise Current (f = 1kHz)	B	+25°C	-	2.5	-	$pA/\sqrt{Hz}$
-Input Noise Current (f = 1kHz)	B	+25°C	-	25.0	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Transimpedance (Note 21)	A	+25°C	1.0	-	-	MΩ
	A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain	A	+25°C	70	-	-	dB
$R_L = 400\Omega$, $V_{OUT} = \pm 2.5V$	A	Full	65	-	-	dB

Electrical Specifications V+ = +5V, V- = -5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, $C_L \leq$ 10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 12) TEST LEVEL	TEMPERATURE	HA5022I MIN	TYP	MAX	UNITS
Open Loop DC Voltage Gain R_L = 100Ω, V_{OUT} = ±2.5V	A	+25°C	50	-	-	dB
	A	Full	45	-	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 20)	A	+25°C	±2.5	±3.0	-	V
	A	Full	±2.5	±3.0	-	V
Output Current (Note 20)	B	Full	±16.6	±20.0	-	mA
Output Current (Short Circuit, Note 13)	A	Full	±40	±60	-	mA
Output Current (Disabled, Notes 5, 14)	A	Full	-	-	2	μA
Output Disable Time (Note 15)	B	+25°C	-	40	-	μs
Output Enable Time (Note 16)	B	+25°C	-	40	-	ns
Output Capacitance (Disabled, Notes 5, 17)	B	+25°C	-	15	-	pF
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range	A	+25°C	5	-	15	V
Quiescent Supply Current	A	Full	-	7.5	10	mA/Op Amp
Supply Current, Disabled (Note 5)	A	Full	-	5	7.5	mA/Op Amp
$\overline{\text{Disable}}$ Pin Input Current (Note 5)	A	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable (Note 6)	A	Full	350	-	-	μA
Maximum Pin 8 Current to Enable (Note 7)	A	Full	-	-	20	μA
AC CHARACTERISTICS (A_V = +1)						
Slew Rate (Note 8)	B	+25°C	275	400	-	V/μs
Full Power Bandwidth (Note 9)	B	+25°C	22	28	-	MHz
Rise Time (Note 10)	B	+25°C	-	6	-	ns
Fall Time (Note 10)	B	+25°C	-	6	-	ns
Propagation Delay (Note 10)	B	+25°C	-	6	-	ns
Overshoot	B	+25°C	-	4.5	-	%
-3dB Bandwidth (Note 11)	B	+25°C	-	125	-	MHz
Settling Time to 1%, 2V Output Step	B	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step	B	+25°C	-	75	-	ns
AC CHARACTERISTICS (A_V = +2, R_F = 681Ω)						
Slew Rate (Note 8)	B	+25°C	-	475	-	V/μs
Full Power Bandwidth (Note 9)	B	+25°C	-	26	-	MHz
Rise Time (Note 10)	B	+25°C	-	6	-	ns
Fall Time (Note 10)	B	+25°C	-	6	-	ns
Propagation Delay (Note 10)	B	+25°C	-	6	-	ns
Overshoot	B	+25°C	-	12	-	%
-3dB Bandwidth (Note 11)	B	+25°C	-	95	-	MHz
Settling Time to 1%, 2V Output Step	B	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step	B	+25°C	-	100	-	ns
Gain Flatness 5MHz	B	+25°C	-	0.02	-	dB
20MHz	B	+25°C	-	0.07	-	dB

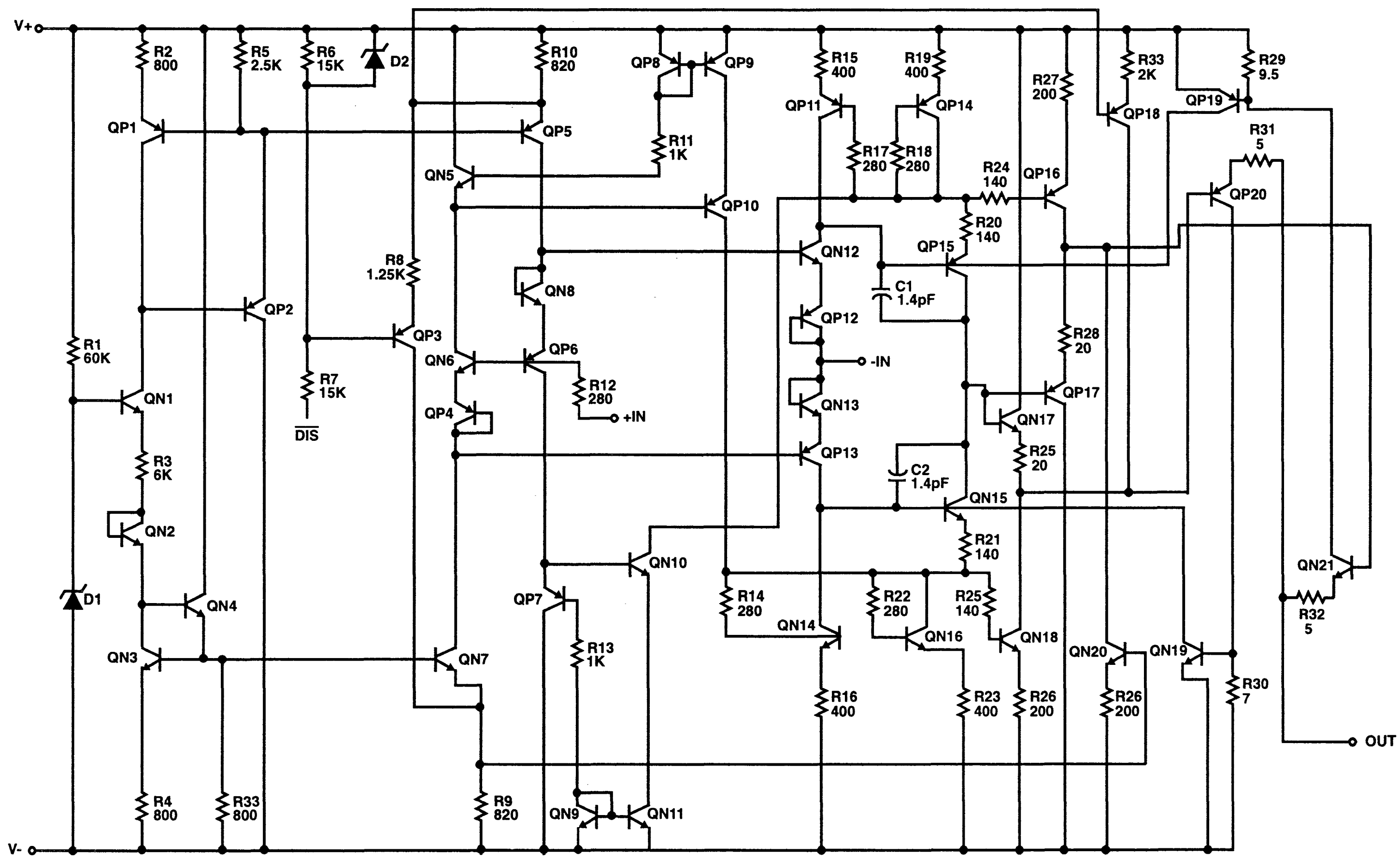
Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \le 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 12) TEST LEVEL	TEMPERATURE	HA5022I MIN	HA5022I TYP	HA5022I MAX	UNITS
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)						
Slew Rate (Note 8)	B	+25°C	350	475	-	V/µs
Full Power Bandwidth (Note 9)	B	+25°C	28	38	-	MHz
Rise Time (Note 10)	B	+25°C	-	8	-	ns
Fall Time (Note 10)	B	+25°C	-	9	-	ns
Propagation Delay (Note 10)	B	+25°C	-	9	-	ns
Overshoot	B	+25°C	-	1.8	-	%
-3dB Bandwidth (Note 11)	B	+25°C	-	65	-	MHz
Settling Time to 1%, 2V Output Step	B	+25°C	-	75	-	ns
Settling Time to 0.1%, 2V Output Step	B	+25°C	-	130	-	ns
VIDEO CHARACTERISTICS						
Differential Gain (Notes 18, 20)	B	+25°C	-	0.03	-	%
Differential Phase (Notes 18, 20)	B	+25°C	-	0.03	-	Degrees

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.
3. $V_{CM} = \pm 2.5V$. At -40°C Product is tested at $V_{CM} = \pm 2.25V$ because short test duration does not allow self heating.
4. $\pm 3.5V \le V_S \le \pm 6.5V$.
5. $\overline{\text{Disable}} = 0V$.
6. $R_L = 100\Omega$, $V_{IN} = 2.5V$. This is the minimum current which must be pulled out of the $\overline{\text{Disable}}$ pin in order to disable the output. The output is considered disabled when $-10mV \le V_{OUT} \le +10mV$.
7. $V_{IN} = 0V$. This is the maximum current that can be pulled out of the $\overline{\text{Disable}}$ pin with the HA5024 remaining enabled. The HA5024 is considered disabled when the supply current has decreased by at least 0.5mA.
8. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
9. $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}; V_{PEAK} = 2V$
10. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
11. $R_L = 400\Omega$, $V_{OUT} = 100mV$.
12. A. Production Tested; B. Guaranteed Limit or Typical based on characterization; C. Design Typical for information only.
13. $V_{IN} = \pm 2.5V$, $V_{OUT} = 0V$.
14. $V_{OUT} = \pm 2.5V$, $V_{IN} = 0V$.
15. $V_{IN} = +2V$, $\overline{\text{Disable}} = +5V$ to 0V. Measured from the 50% point of $\overline{\text{Disable}}$ to $V_{OUT} = 0V$.
16. $V_{IN} = +2V$, $\overline{\text{Disable}} = 0V$ to +5V. Measured from the 50% point of $\overline{\text{Disable}}$ to $V_{OUT} = 2V$.
17. $V_{IN} = 0V$, Force V_{OUT} from 0V to $\pm 2.5V$, $t_R = t_F = 50ns$.
18. Measured with a VM700A video tester using an NTC-7 composite VITS.
19. Maximum power dissipation, including output load, must be designed to maintain junction temperature below +175°C for die, and below +150°C for plastic packages. See Applications Information section for safe operating area information.
20. $R_L = 150\Omega$.
21. $V_{OUT} = \pm 2.5V$. At -40°C Product is tested at $V_{OUT} = \pm 2.25V$ because short test duration does not allow self heating.
22. ESD Protection is for human body model tested per MIL-STD-883, Method 3015.7.

Schematic


V+
V-
R1
60K
R2
800
R3
6K
R4
800
R5
2.5K
R6
15K
R7
15K
R8
1.25K
R9
820
R10
820
R11
1K
R12
280
R13
1K
R14
280
R15
400
R16
400
R17
280
R18
280
R19
400
R20
140
R21
140
R22
280
R23
400
R24
140
R25
20
R25
140
R26
200
R26
200
R27
200
R28
20
R29
9.5
R30
7
R31
5
R32
5
R33
2K
R33
800
C1
1.4pF
C2
1.4pF
D1
D2
QP1
QP2
QP3
QP4
QP5
QP6
QP7
QP8
QP9
QP10
QP11
QP12
QP13
QP14
QP15
QP16
QP17
QP18
QP19
QP20
QN1
QN2
QN3
QN4
QN5
QN6
QN7
QN8
QN9
QN10
QN11
QN12
QN13
QN14
QN15
QN16
QN17
QN18
QN19
QN20
QN21
DIS
+IN
-IN
OUT

Test Circuits

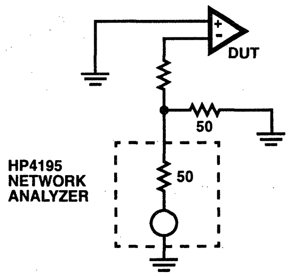


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

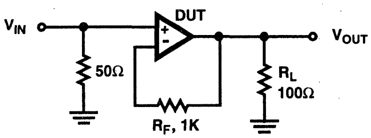


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

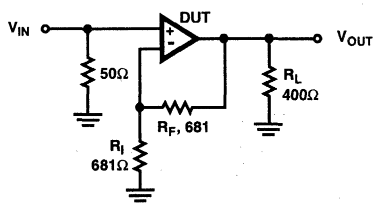


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT

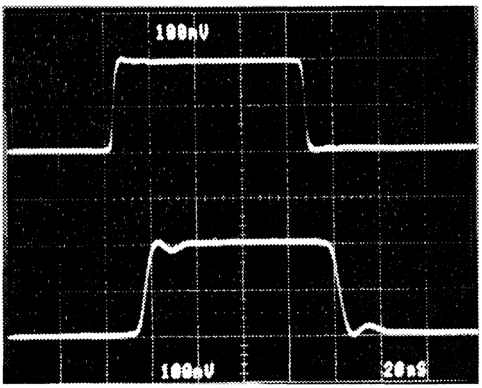


FIGURE 4. SMALL SIGNAL RESPONSE
Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

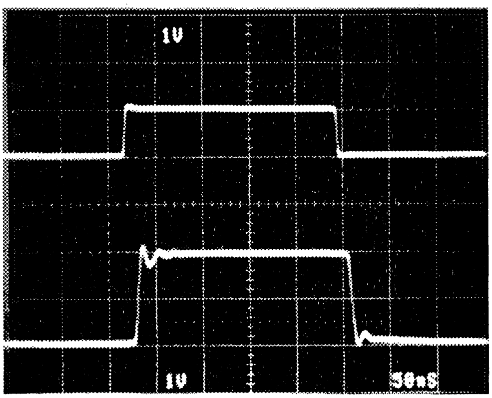


FIGURE 5. LARGE SIGNAL RESPONSE
Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 11 and Figure 12 in the Typical Performance Curves section, illustrate the performance of the HA5022 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA5022 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10μF) tantalum or electrolytic capacitor in parallel with a small value (0.1μF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

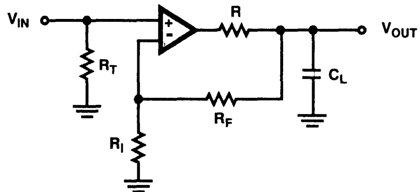


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Power Dissipation Considerations

Due to the high supply current inherent in quad amplifiers, care must be taken to insure that the maximum junction temperature (T_J, see Absolute Maximum Ratings) is not exceeded. Figure 7 shows the maximum ambient temperature versus supply voltage for the available package styles (Plastic DIP, SOIC). At $\pm 5V_{DC}$ quiescent operation both package styles may be operated over the full industrial range of -40°C to +85°C. It is recommended that thermal calculations, which take into account output power, be performed by the designer.

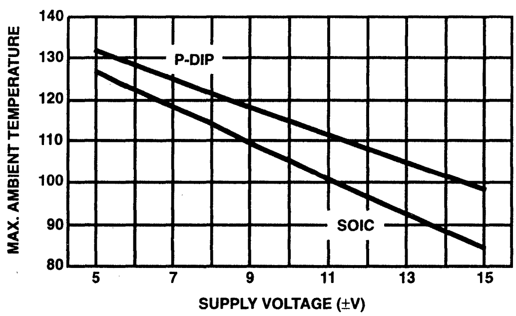


FIGURE 7. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

Enable/Disable Function

When enabled the amplifier functions as a normal current feedback amplifier with all of the data in the electrical specifications table being valid and applicable. When disabled the amplifier output assumes a true high impedance state and the supply current is reduced significantly.

The circuit shown in Figure 8 is a simplified schematic of the enable/disable function. The large value resistors in series with the DISABLE pin makes it appear as a current source to the driver. When the driver pulls this pin low current flows out of the pin and into the driver. This current, which may be as large as 350μA when external circuit and process variables are at their extremes, is required to insure that point "A" achieves the proper potential to disable the output. The driver must have the compliance and capability of sinking all of this current.

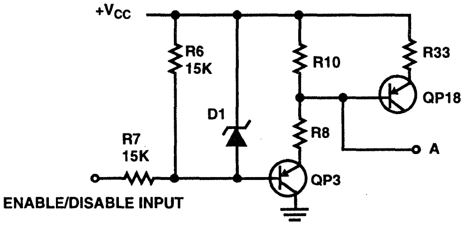


FIGURE 8. SIMPLIFIED SCHEMATIC OF ENABLE/DISABLE FUNCTION

When V_{CC} is +5V the DISABLE pin may be driven with a dedicated TTL gate. The maximum low level output voltage of the TTL gate, 0.4V, has enough compliance to insure that the amplifier will always be disabled even though D1 will not turn on, and the TTL gate will sink enough current to keep point "A" at its proper voltage. When V_{CC} is greater than +5 volts the DISABLE pin should be driven with an open collector device that has a breakdown rating greater than V_{CC}.

Referring to Figure 8, it can be seen that R6 will act as a pull-up resistor to $+V_{CC}$ if the DISABLE pin is left open. In those cases where the enable/disable function is not required on all circuits some circuits can be permanently enabled by letting the DISABLE pin float. If a driver is used to set the enable/disable level, be sure that the driver does not sink more than 20μA when the DISABLE pin is at a high level. TTL gates, especially CMOS versions, do not violate this criteria so it is permissible to control the enable/disable function with TTL.

Two Channel Video Multiplexer

Referring to the amplifier U1A in Figure 9, R1 terminates the cable in its characteristic impedance of 75Ω, and R4 back terminates the cable in its characteristic impedance. The amplifier is set up in a gain configuration of +2 to yield an overall network gain of +1 when driving a double terminated cable. The value of R3 can be changed if a different network gain is desired. R5 holds the disable pin at ground thus inhibiting the amplifier until the switch, S1, is thrown to position 1. At position 1 the switch pulls the disable pin up to the plus supply rail thereby enabling the amplifier. Since all of the actual signal switching takes place within the amplifier, it's differential gain and phase parameters, which are 0.03% and 0.03 degrees respectively, determine the circuit's performance. The other circuit, U1b, operates in a similar manner.

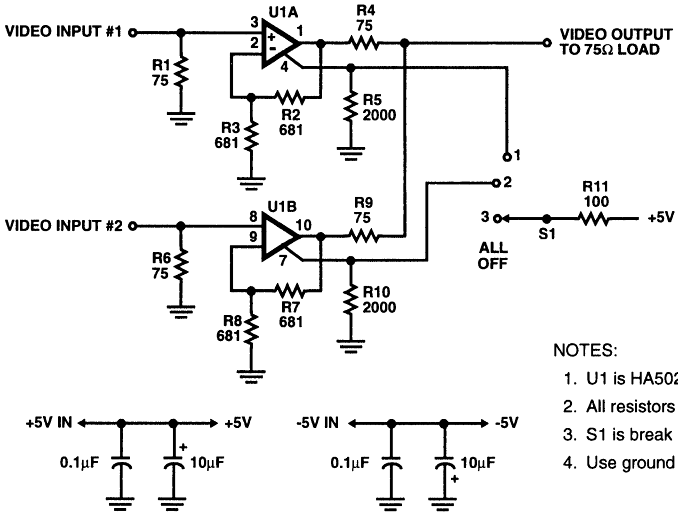
When the plus supply rail is 5V the disable pin can be driven by a dedicated TTL gate as discussed earlier. If a multiplexer IC or its equivalent is used to select channels its logic must be break before make. When these conditions are satisfied the HA5022 is often used as a remote video multiplexer, and the multiplexer may be extended by adding more amplifier ICs.

Low Impedance Multiplexer

Two common problems surface when you try to multiplex multiple high speed signals into a low impedance source such as an A/D converter. The first problem is the low source impedance which tends to make amplifiers oscillate and causes gain errors. The second problem is the multiplexer which supplies no gain, introduces all kinds of distortion and limits the frequency response. Using op amps which have an enable/disable function, such as the HA5022, eliminates the multiplexer problems because the external mux chip is not needed, and the HA5022 can drive low impedance (large capacitance) loads if a series isolation resistor is used.

Referring to Figure 10, both inputs are terminated in their characteristic impedance; 75Ω is typical for video applications. Since the drivers usually are terminated in their characteristic impedance the input gain is 0.5, thus the amplifiers, U2, are configured in a gain of +2 to set the circuit gain equal to one. Resistors R2 and R3 determine the amplifier gain, and if a different gain is desired R2 should be changed according to the equation G = (1 + R3/R2). R3 sets the frequency response of the amplifier so you should refer to the manufacturers data sheet before changing it's value. R5, C1 and D1 are an asymmetrical charge/discharge time circuit which configures U1 as a break before make switch to prevent both amplifiers from being active simultaneously. If this design is extended to more channels the drive logic must be designed to be break before make. R4 is enclosed in the feedback loop of the amplifier so that the large open loop amplifier gain of U2 will present the load with a small closed loop output impedance while keeping the amplifier stable for all values of load capacitance.

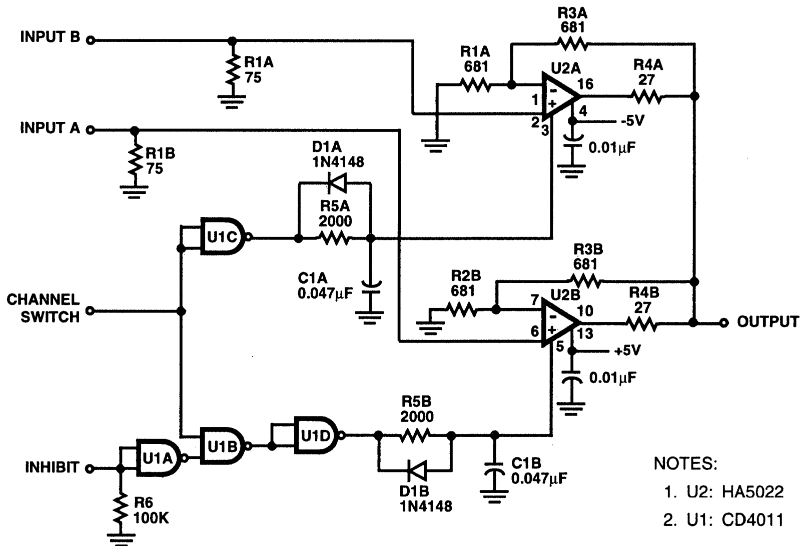
The circuit shown in Figure 10 was tested for the full range of capacitor values with no oscillations being observed; thus, problem one has been solved.The frequency and gain characteristics of the circuit are now those of the amplifier independent of any multiplexing action; thus, problem two has been solved. The multiplexer transition time is approximately 15μs with the component values shown.



NOTES:

1. U1 is HA5022
2. All resistors in Ω
3. S1 is break before make
4. Use ground plane

FIGURE 9. TWO CHANNEL HIGH IMPEDANCE MULTIPLEXER



NOTES:

1. U2: HA5022
2. U1: CD4011

FIGURE 10. LOW IMPEDANCE MULTIPLEXER

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified

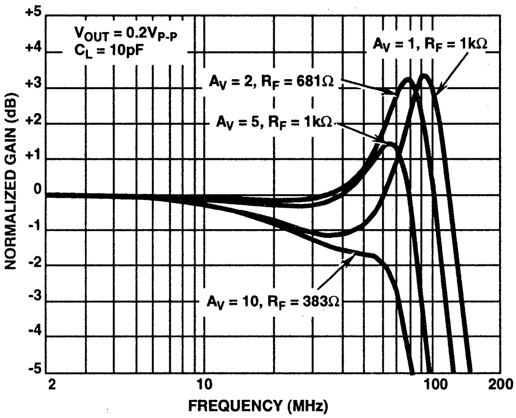


FIGURE 11. NON-INVERTING FREQENCY RESPONSE

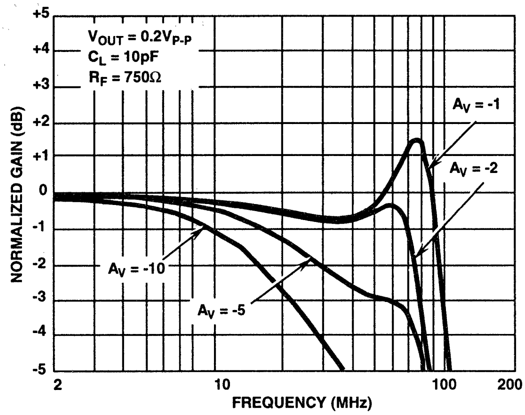


FIGURE 12. INVERTING FREQUENCY RESPONSE

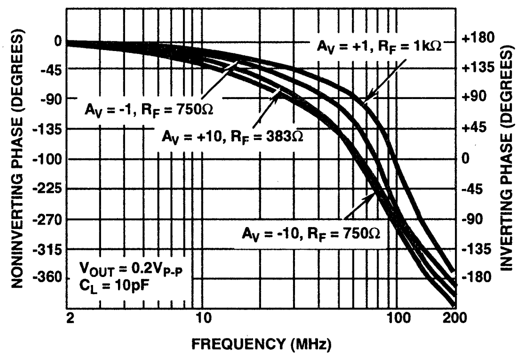


FIGURE 13. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

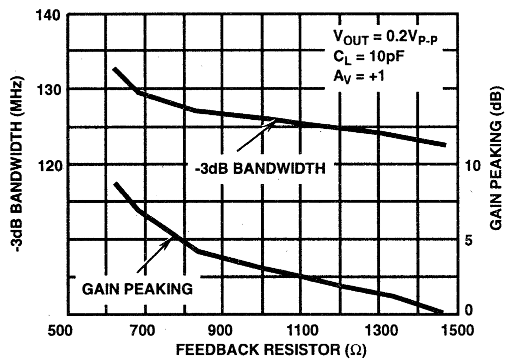


FIGURE 14. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

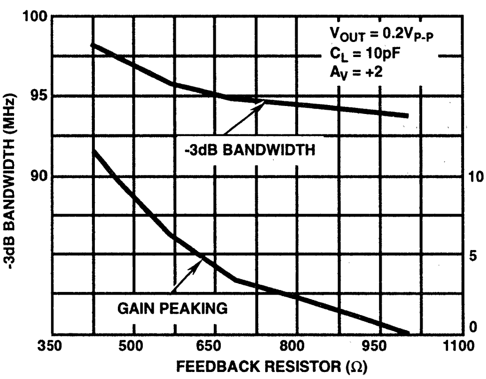


FIGURE 15. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

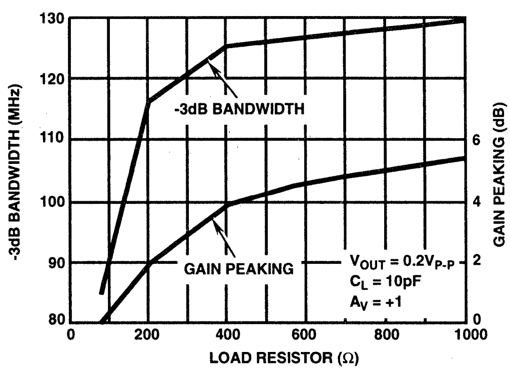


FIGURE 16. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

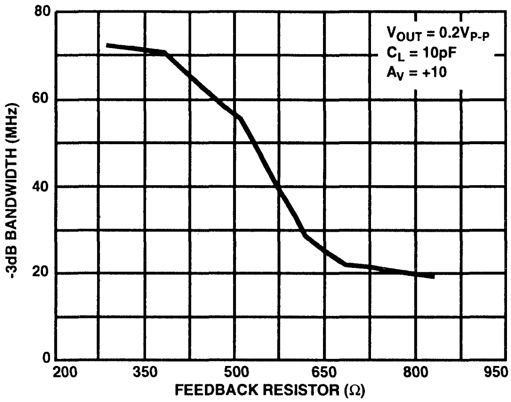


FIGURE 17. BANDWIDTH vs FEEDBACK RESISTANCE

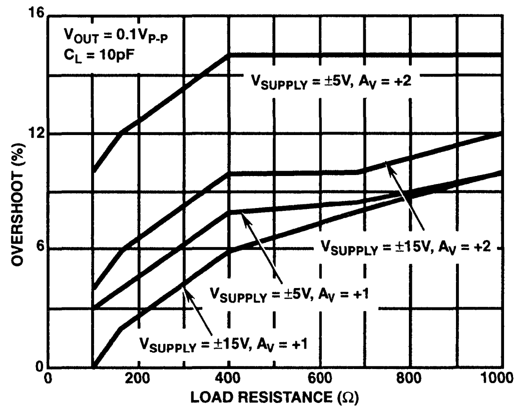


FIGURE 18. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

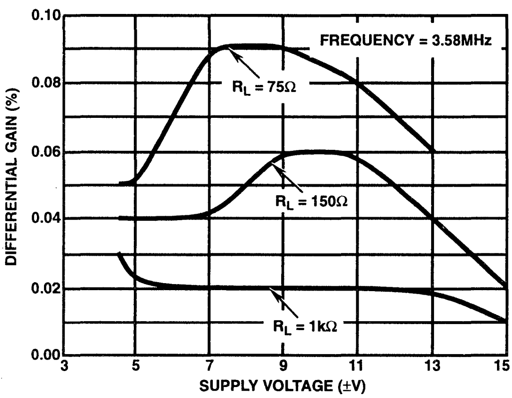


FIGURE 19. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

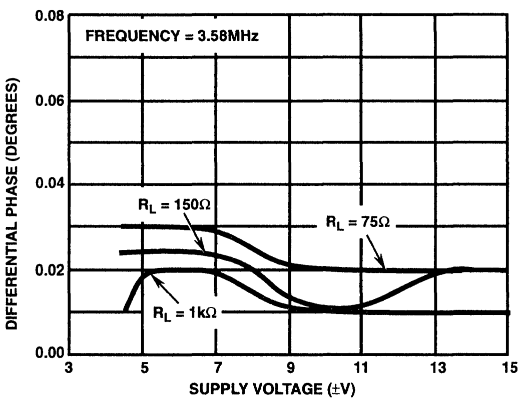


FIGURE 20. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

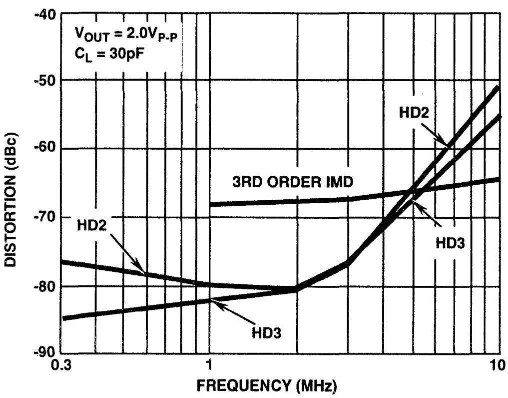


FIGURE 21. DISTORTION vs FREQUENCY

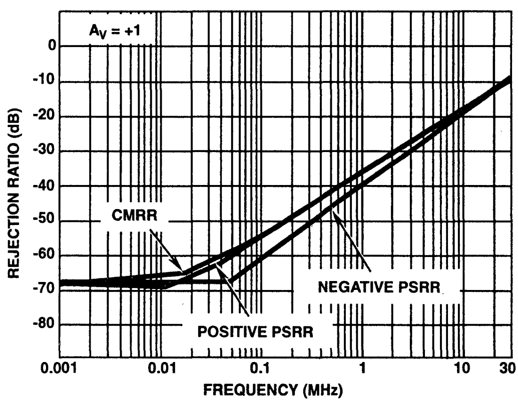


FIGURE 22. REJECTION RATIOS vs FREQUENCY

2

OPERATIONAL AMPLIFIERS

Typical Performance Curves

V_{SUPPLY} = ±5V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = 25°C, Unless Otherwise Specified **(Continued)**

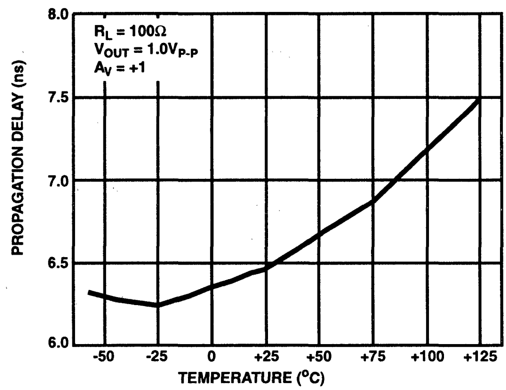


FIGURE 23. PROPAGATION DELAY vs TEMPERATURE

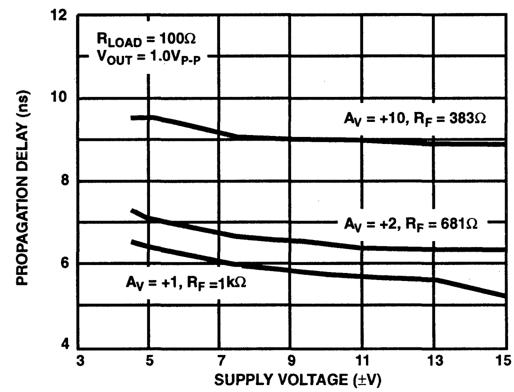


FIGURE 24. PROPAGATION DELAY vs SUPPLY VOLTAGE

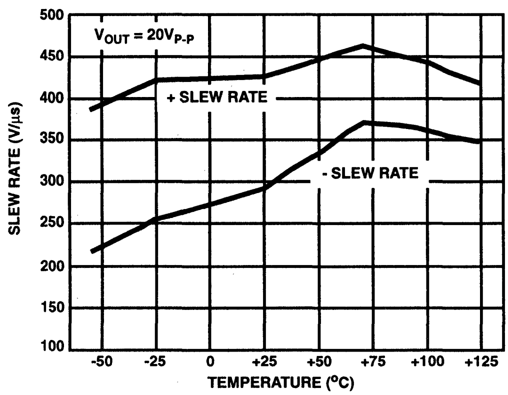


FIGURE 25. SLEW RATE vs TEMPERATURE

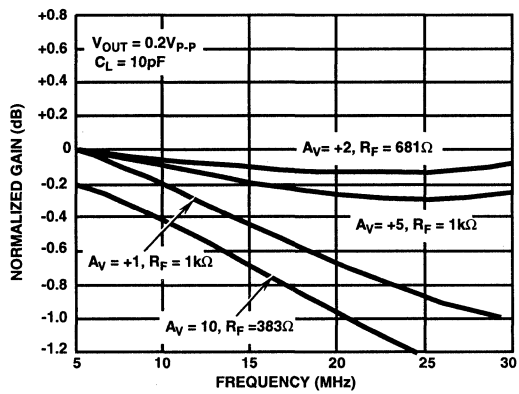


FIGURE 26. NON-INVERTING GAIN FLATNESS vs FREQUENCY

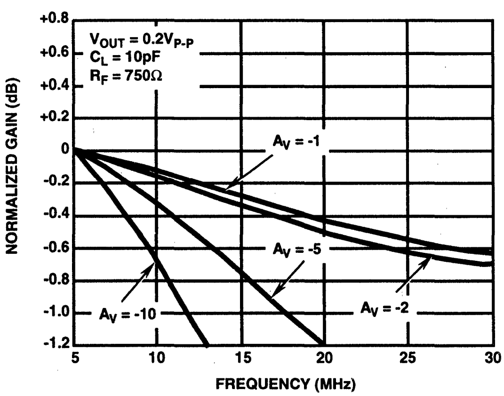


FIGURE 27. INVERTING GAIN FLATNESS vs FREQUENCY

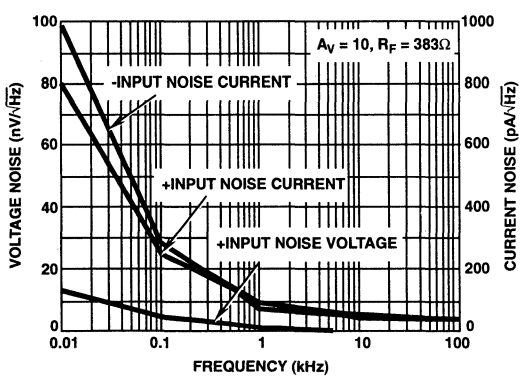


FIGURE 28. INPUT NOISE CHARACTERISTICS

Typical Performance Curves

$V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

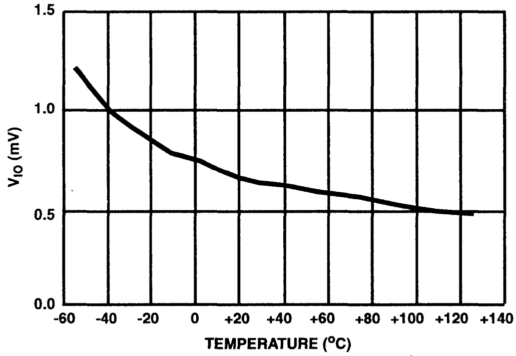


FIGURE 29. INPUT OFFSET VOLTAGE vs TEMPERATURE

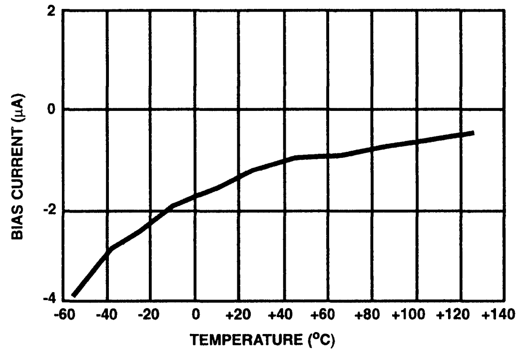


FIGURE 30. +INPUT BIAS CURRENT vs TEMPERATURE

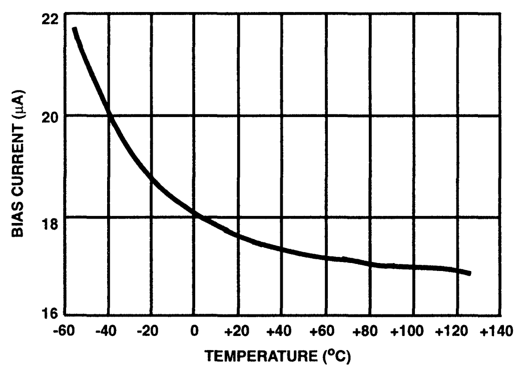


FIGURE 31. -INPUT BIAS CURRENT vs TEMPERATURE

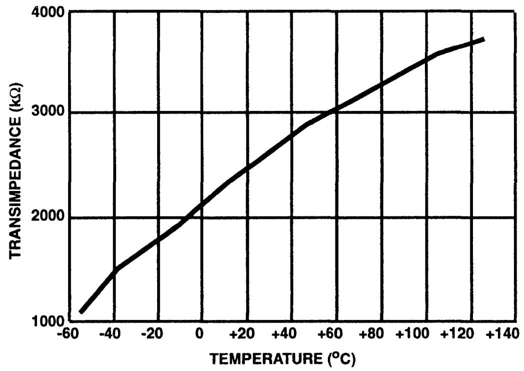


FIGURE 32. TRANSIMPEDANCE vs TEMPERATURE

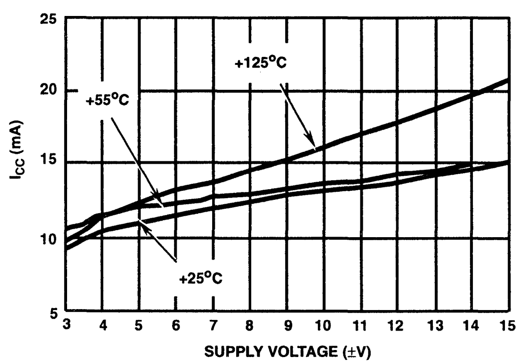


FIGURE 33. SUPPLY CURRENT vs SUPPLY VOLTAGE

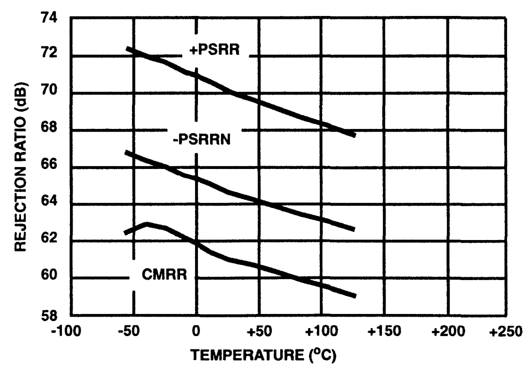


FIGURE 34. REJECTION RATIO vs TEMPERATURE

2

OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

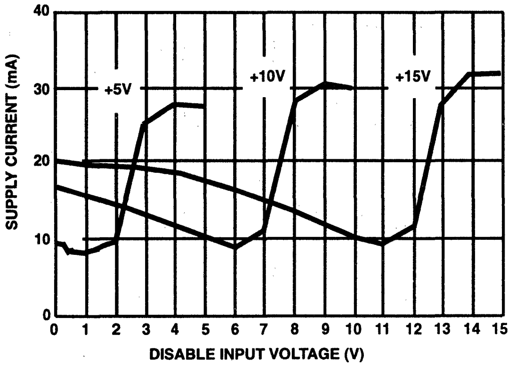


FIGURE 35. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

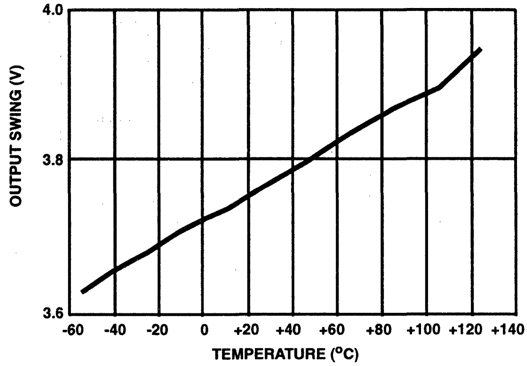


FIGURE 36. OUTPUT SWING vs TEMPERATURE

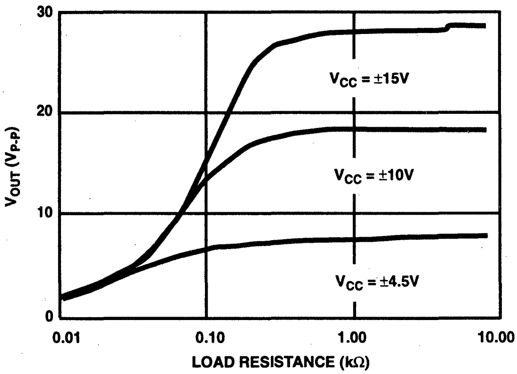


FIGURE 37. OUTPUT SWING vs LOAD RESISTANCE

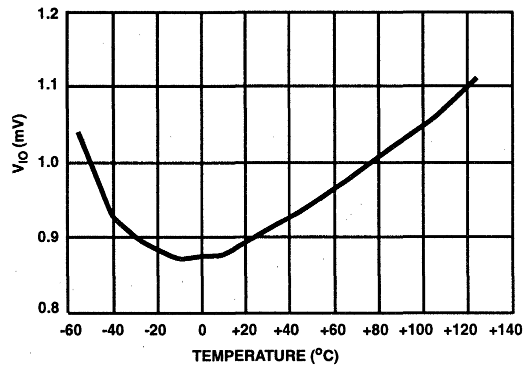


FIGURE 38. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

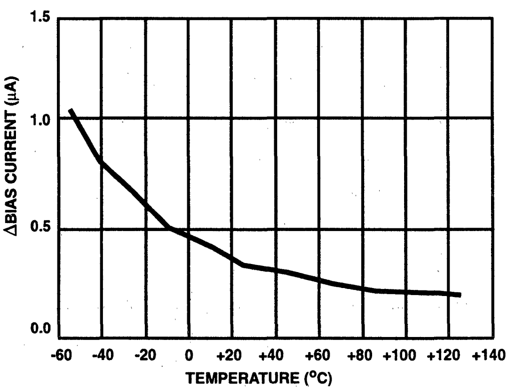


FIGURE 39. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

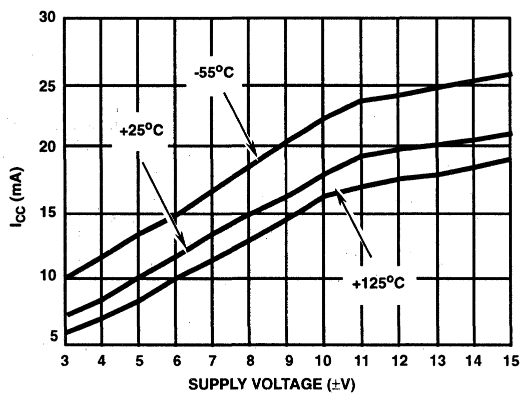


FIGURE 40. DISABLE SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

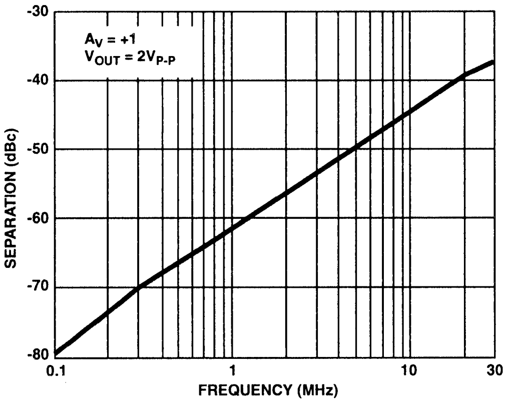


FIGURE 41. CHANNEL SEPARATION vs FREQUENCY

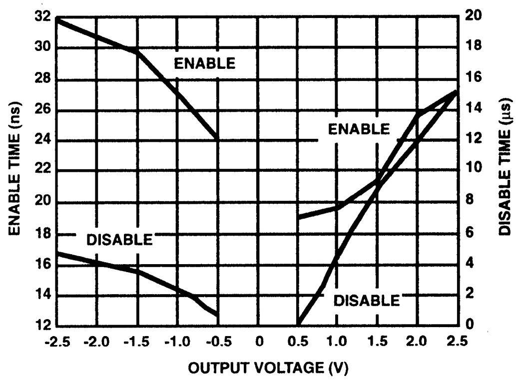


FIGURE 42. ENABLE/DISABLE TIME vs OUTPUT VOLTAGE

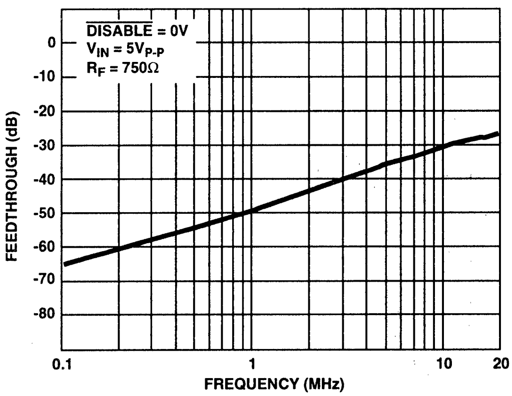


FIGURE 43. DISABLE FEEDTHROUGH vs FREQUENCY

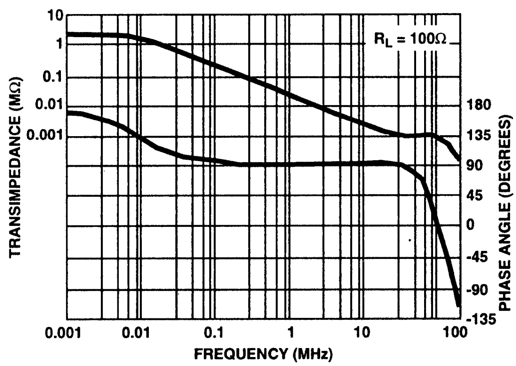


FIGURE 44. TRANSIMPEDANCE vs FREQUENCY

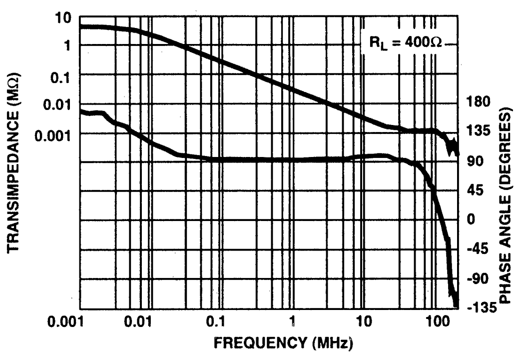


FIGURE 45. TRANSIMPEDENCE vs FREQUENCY

2

OPERATIONAL AMPLIFIERS

Die Characteristics

DIE DIMENSIONS:
1650µm x 2540µm x 483µm ±25.4µm

METALLIZATION:
Type: Metal 1: AlCu (1%), Metal 2: AlCu (1%)
Thickness: Metal 1: 8kÅ ± 0.4kÅ, Metal 2: 16kÅ ± 0.8kÅ

WORST CASE CURRENT DENSITY:
1.62×10^5 A/cm^2 at 35mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.4kÅ

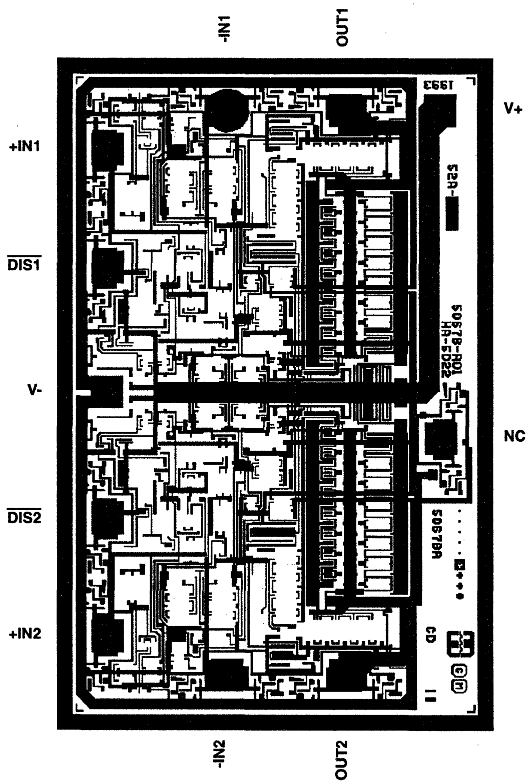
TRANSISTOR COUNT: 124

PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC

Metallization Mask Layout

HA5022



HA5023

Dual 125MHz Video Current Feedback Amplifier

July 1995

Features

- **Wide Unity Gain Bandwidth 125MHz**
- **Slew Rate 475V/µs**
- **Input Offset Voltage 800µV**
- **Differential Gain 0.03%**
- **Differential Phase . . . . 0.03 Deg.**
- **Supply Current (per Amplifier) 7.5mA**
- **ESD Protection 4000V**
- **Guaranteed Specifications at ±5V Supplies**

Applications

- **Video Gain Block**
- **Video Distribution Amplifier/ RGB Amplifier**
- **Flash A/D Driver**
- **Current to Voltage Converter**
- **Medical Imaging**
- **Radar and Imaging Systems**
- **Video Switching and Routing**

Description

The HA5023 is a wide bandwidth high slew rate dual amplifier optimized for video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor. By reducing R_F, the bandwidth can be increased to compensate for decreases at higher closed loop gains or heavy output loads.

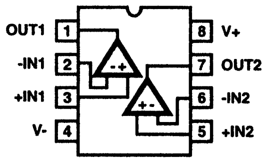
The performance of the HA5023 is very similar to the popular Harris HA-5020.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA5023IP	-40°C to +85°C	8 Lead Plastic DIP
HA5023IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

Pinout

HA5023
(PDIP, SOIC)
TOP VIEWV



File Number **3393.4**

Absolute Maximum Ratings (Note 1)

ESD Protection (Note 15) 2000V
Voltage Between V+ and V- Terminals 36V
DC Input Voltage . . . . $\pm V_{SUPPLY}$
Differential Input Voltage 10V
Output Current (Note 2) . . . . Short Circuit Protected
Junction Temperature (Note 12) . . . . +175°C
Junction Temperature (Plastic Package) (Note 12) . . . . +150°C
Lead Temperature (Soldering 10s) . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HA5023I . . . . $-40^oC \le T_A \le +85^oC$
Supply Voltage Range . . . . ±4.5V to ±15V
Storage Temperature Range . . . . $-65^oC \le T_A \le +150^oC$
Thermal Package Characteristics (°C/W) θ_{JA}
Plastic DIP 130
SOIC 160

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \le 10pF$, Unless Otherwise Specified

PARAMETER	(NOTE 16) TEST LEVEL	TEMPERATURE	HA5023I MIN	HA5023I TYP	HA5023I MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage (V_{IO})	A	+25°C	-	0.8	3	mV
	A	Full	-	-	5	mV
Delta V_{IO} Between Channels	A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift	B	Full	-	5	-	µV/°C
V_{IO} Common Mode Rejection Ratio (Note 3)	A	+25°C	53	-	-	dB
	A	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio (Note 4)	A	+25°C	60	-	-	dB
	A	Full	55	-	-	dB
Input Common Mode Range (Note 3)	A	Full	±2.5	-	-	V
Non-Inverting Input (+IN) Current	A	+25°C	-	3	8	µA
	A	Full	-	-	20	µA
+IN Common Mode Rejection (Note 3) ($+I_{BCMR} = \frac{1}{+R_{IN}}$)	A	+25°C	-	-	0.15	µA/V
	A	Full	-	-	0.5	µA/V
+IN Power Supply Rejection (Note 4)	A	+25°C	-	-	0.1	µA/V
	A	Full	-	-	0.3	µA/V
Inverting Input (-IN) Current	A	+25°C, +85°C	-	4	12	µA
	A	-40°C	-	10	30	µA
Delta - IN BIAS Current Between Channels	A	+25°C, +85°C	-	6	15	µA
	A	-40°C	-	10	30	µA
-IN Common Mode Rejection (Note 3)	A	+25°C	-	-	0.4	µA/V
	A	Full	-	-	1.0	µA/V
-IN Power Supply Rejection (Note 4)	A	+25°C	-	-	0.2	µA/V
	A	Full	-	-	0.5	µA/V
Input Noise Voltage (f = 1kHz)	B	+25°C	-	4.5	-	$nV/\sqrt{Hz}$
+Input Noise Current (f = 1kHz)	B	+25°C	-	2.5	-	$pA/\sqrt{Hz}$
-Input Noise Current (f = 1kHz)	B	+25°C	-	25.0	-	$pA/\sqrt{Hz}$

Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 16) TEST LEVEL	TEMPERATURE	HA5023I MIN	HA5023I TYP	HA5023I MAX	UNITS
TRANSFER CHARACTERISTICS						
Transimpedence (Note 14)	A	+25°C	1.0	-	-	MΩ
	A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain, $R_L = 400\Omega$, $V_{OUT} = \pm2.5V$	A	+25°C	70	-	-	dB
	A	Full	65	-	-	dB
Open Loop DC Voltage Gain, $R_L = 100\Omega$, $V_{OUT} = \pm2.5V$	A	+25°C	50	-	-	dB
	A	Full	45	-	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 13)	A	+25°C	±2.5	±3.0	-	V
	A	Full	±2.5	±3.0	-	V
Output Current (Note 13)	B	Full	±16.6	±20.0	-	mA
Output Current (Short Circuit, Note 10)	A	Full	±40	±60	-	mA
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range	A	+25°C	5	-	15	V
Quiescent Supply Current	A	Full	-	7.5	10	mA/Op Amp
AC CHARACTERISTICS ($A_V = +1$)						
Slew Rate (Note 5)	B	+25°C	275	350	-	V/µs
Full Power Bandwidth (Note 6)	B	+25°C	22	28	-	MHz
Rise Time (Note 7)	B	+25°C	-	6	-	ns
Fall Time (Note 7)	B	+25°C	-	6	-	ns
Propagation Delay (Note 7)	B	+25°C	-	6	-	ns
Overshoot	B	+25°C	-	4.5	-	%
-3dB Bandwidth (Note 8)	B	+25°C	-	125	-	MHz
Settling Time to 1%, 2V Output Step	B	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step	B	+25°C	-	75	-	ns
AC CHARACTERISTICS ($A_V = +2$, $R_F = 681\Omega$)						
Slew Rate (Note 5)	B	+25°C	-	475	-	V/µs
Full Power Bandwidth (Note 6)	B	+25°C	-	26	-	MHz
Rise Time (Note 7)	B	+25°C	-	6	-	ns
Fall Time (Note 7)	B	+25°C	-	6	-	ns
Propagation Delay (Note 7)	B	+25°C	-	6	-	ns
Overshoot	B	+25°C	-	12	-	%

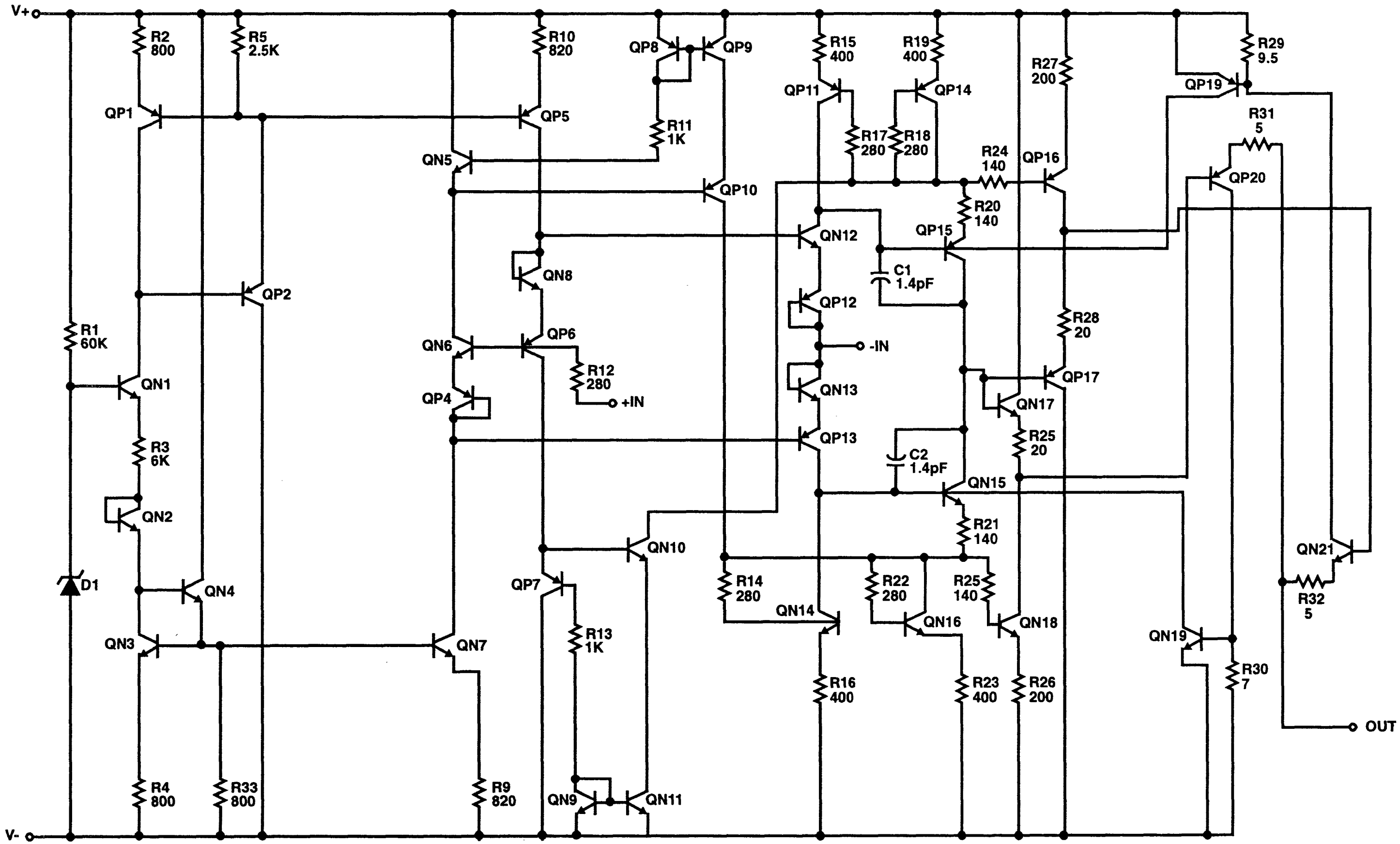
Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 16) TEST LEVEL	TEMPERATURE	HA5023I			UNITS
				MIN	TYP	MAX	
-3dB Bandwidth (Note 8)		B	+25°C	-	95	-	MHz
Settling Time to 1%, 2V Output Step		B	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step		B	+25°C	-	100	-	ns
Gain Flatness	5MHz	B	+25°C	-	0.02	-	dB
	20MHz	B	+25°C	-	0.07	-	dB
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)							
Slew Rate (Note 5)		B	+25°C	350	475	-	V/µs
Full Power Bandwidth (Note 6)		B	+25°C	28	38	-	MHz
Rise Time (Note 7)		B	+25°C	-	8	-	ns
Fall Time (Note 7)		B	+25°C	-	9	-	ns
Propagation Delay (Note 7)		B	+25°C	-	9	-	ns
Overshoot		B	+25°C	-	1.8	-	%
-3dB Bandwidth (Note 8)		B	+25°C	-	65	-	MHz
Settling Time to 1%, 2V Output Step		B	+25°C	-	75	-	ns
Settling Time to 0.1%, 2V Output Step		B	+25°C	-	130	-	ns
VIDEO CHARACTERISTICS							
Differential Gain (Notes 11, 13)		B	+25°C	-	0.03	-	%
Differential Phase (Notes 11, 13)		B	+25°C	-	0.03	-	Degrees

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.
3. $V_{CM} = \pm 2.5V$. At -40°C Product is tested at $V_{CM} = \pm 2.25V$ because Short Test Duration does not allow self heating.
4. $\pm 3.5V \leq V_S \leq \pm 6.5V$
5. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
6. $2\left(FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}};\ V_{PEAK} = 2V\right)$
7. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
8. $R_L = 400\Omega$, $V_{OUT} = 100mV$.
9. A. Production Tested; B. Guaranteed Limit or Typical based on characterization; C. Design Typical for information only.
10. $V_{IN} = \pm 2.5V$, $V_{OUT} = 0V$.
11. Measured with a VM700A video tester using an NTC-7 composite VITS.
12. Maximum power dissipation, including output load, must be designed to maintain junction temperature below +175°C for die, and below +150°C for plastic packages. See Applications Information section for safe operating area information.
13. $R_L = 150\Omega$.
14. $V_{OUT} = \pm 2.5V$. At -40°C Product is tested at $V_{OUT} = \pm 2.25V$ because Short Test Duration does not allow self heating.
15. ESD protection is for human body model tested per MIL-STD-883, Method 3015.7.
16. A. Production Tested; B. Guaranteed limit or Typical based on characterization; C. Design Typical for information only.

Schematic


V+
V-
R1 60K
R2 800
R3 6K
R4 800
R5 2.5K
R9 820
R10 820
R11 1K
R12 280
R13 1K
R14 280
R15 400
R16 400
R17 280
R18 280
R19 400
R20 140
R21 140
R22 280
R23 400
R24 140
R25 20
R25 140
R26 200
R27 200
R28 20
R29 9.5
R30 7
R31 5
R32 5
R33 800
C1 1.4pF
C2 1.4pF
D1
QP1
QP2
QP4
QP5
QP6
QP7
QP8
QP9
QP10
QP11
QP12
QP13
QP14
QP15
QP16
QP17
QP19
QP20
QN1
QN2
QN3
QN4
QN5
QN6
QN7
QN8
QN9
QN10
QN11
QN12
QN13
QN14
QN15
QN16
QN17
QN18
QN19
QN21
+IN
-IN
OUT

Test Circuits

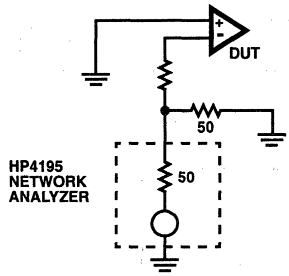


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

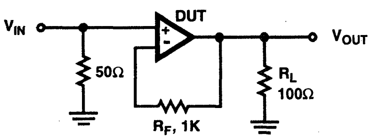


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

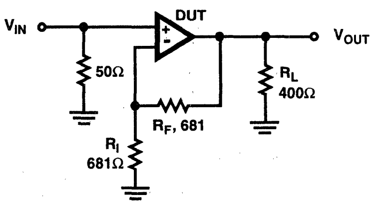


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT

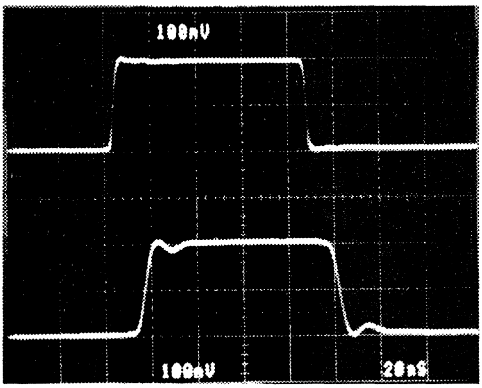


FIGURE 4. SMALL SIGNAL RESPONSE
Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

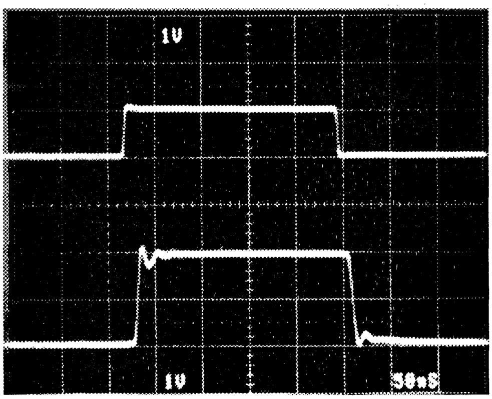


FIGURE 5. LARGE SIGNAL RESPONSE
Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 8 and Figure 9 in the typical performance section, illustrate the performance of the HA5023 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA5023 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10µF) tantalum or electrolytic capacitor in parallel with a small value (0.1µF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

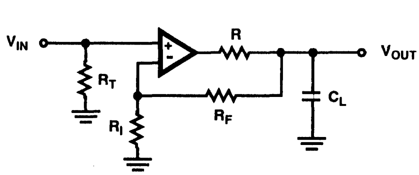


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Power Dissipation Considerations

Due to the high supply current inherent in quad amplifiers, care must be taken to insure that the maximum junction temperature (T_J, see Absolute Maximum Ratings) is not exceeded. Figure 7 shows the maximum ambient temperature versus supply voltage for the available package styles (Plastic DIP, SOIC). At ±5V_{DC} quiescent operation both package styles may be operated over the full industrial range of -40°C to +85°C. It is recommended that thermal calculations, which take into account output power, be performed by the designer.

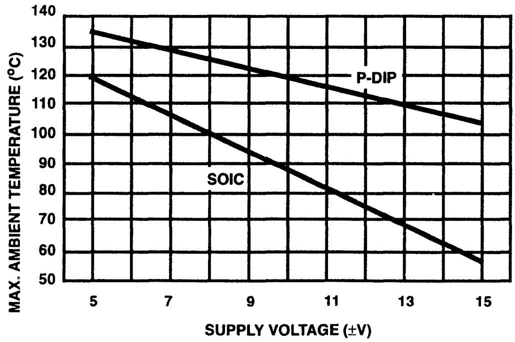


FIGURE 7. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

OPERATIONAL AMPLIFIERS 2

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified

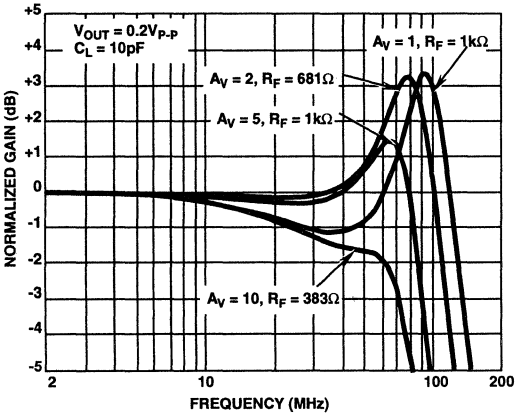


FIGURE 8. NON-INVERTING FREQENCY RESPONSE

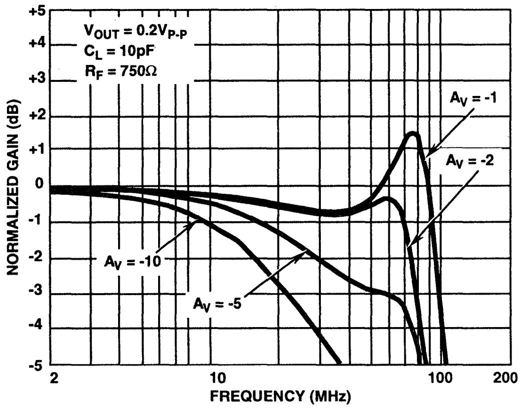


FIGURE 9. INVERTING FREQUENCY RESPONSE

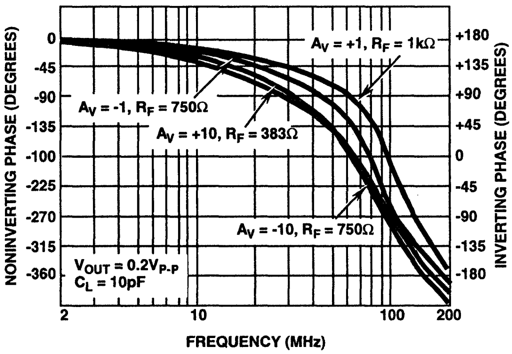


FIGURE 10. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

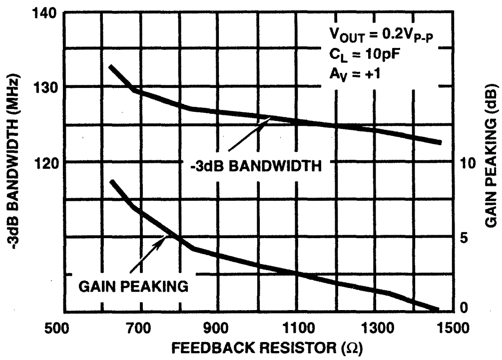


FIGURE 11. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

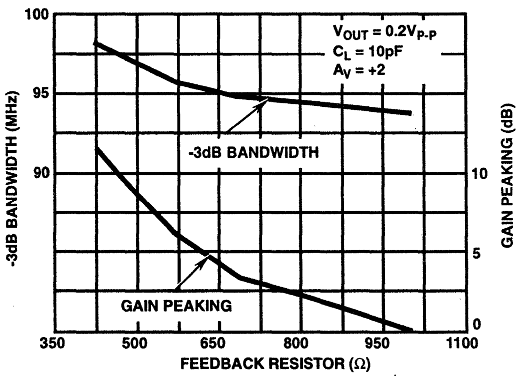


FIGURE 12. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

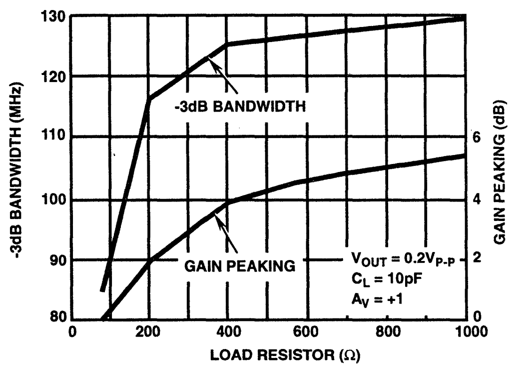


FIGURE 13. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

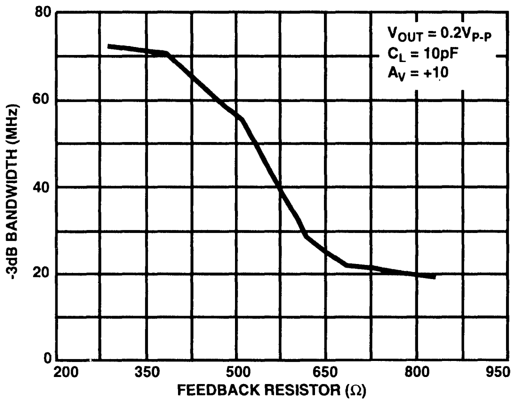


FIGURE 14. BANDWIDTH vs FEEDBACK RESISTANCE

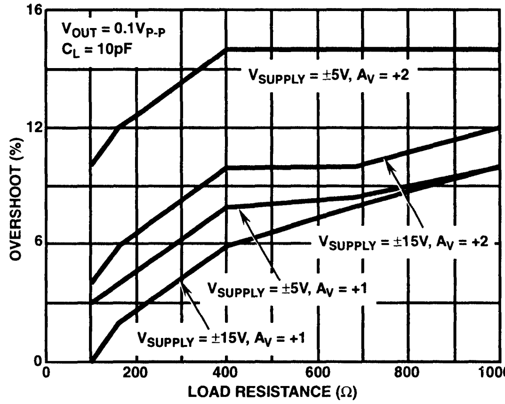


FIGURE 15. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

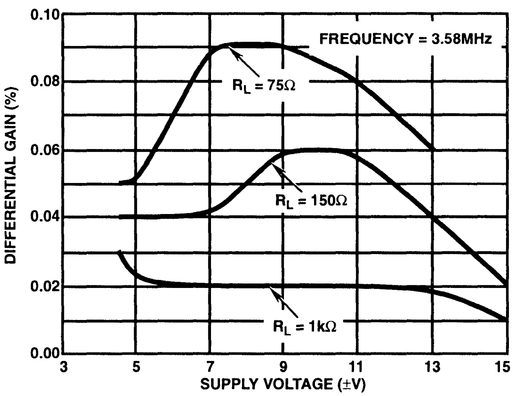


FIGURE 16. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

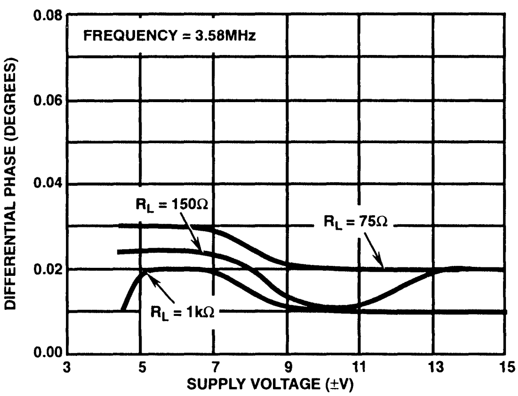


FIGURE 17. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

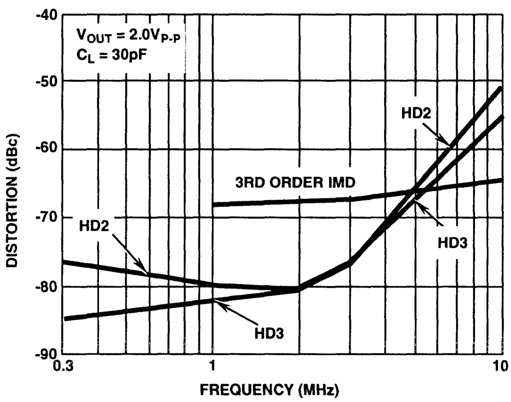


FIGURE 18. DISTORTION vs FREQUENCY

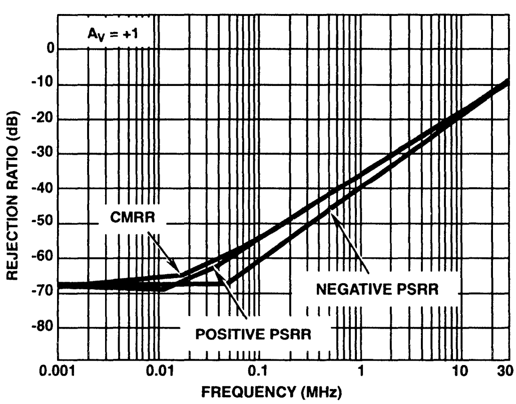


FIGURE 19. REJECTION RATIOS vs FREQUENCY

Typical Performance Curves V_{SUPPLY} = ±5V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = 25°C, Unless Otherwise Specified **(Continued)**

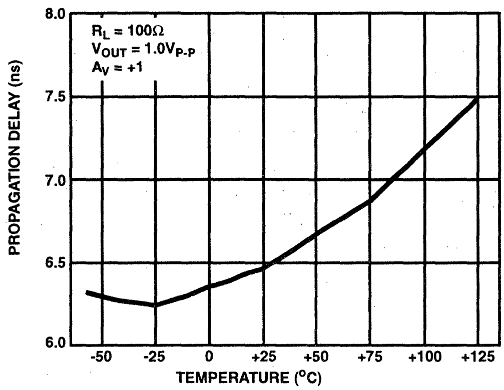


FIGURE 20. PROPAGATION DELAY vs TEMPERATURE

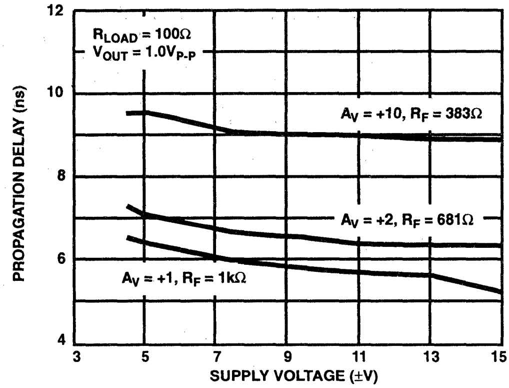


FIGURE 21. PROPAGATION DELAY vs SUPPLY VOLTAGE

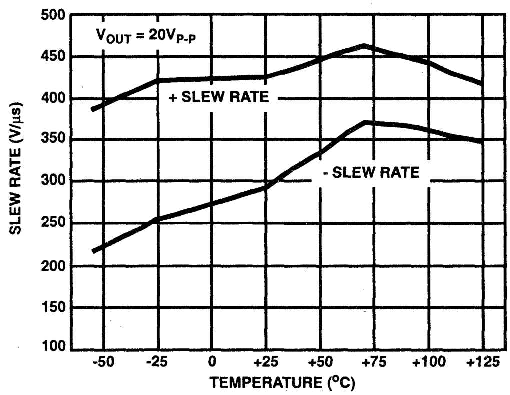


FIGURE 22. SLEW RATE vs TEMPERATURE

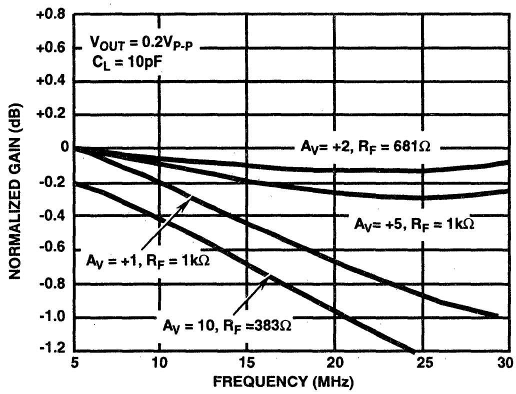


FIGURE 23. NON-INVERTING GAIN FLATNESS vs FREQUENCY

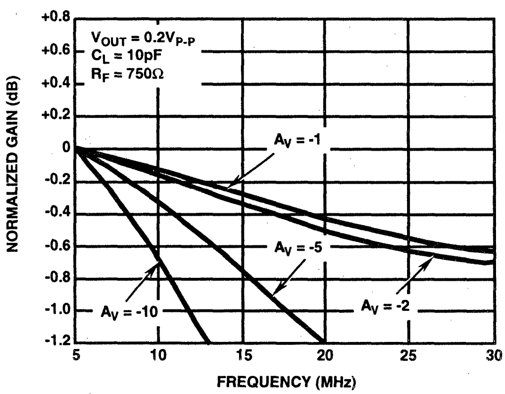


FIGURE 24. INVERTING GAIN FLATNESS vs FREQUENCY

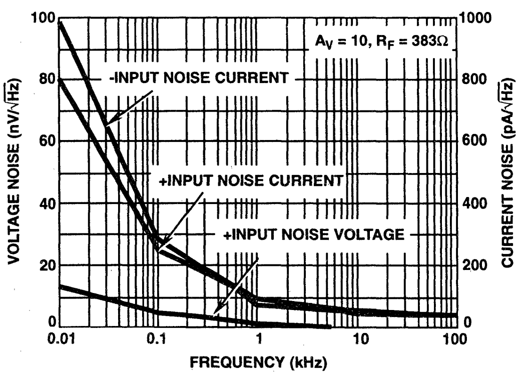


FIGURE 25. INPUT NOISE CHARACTERISTICS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

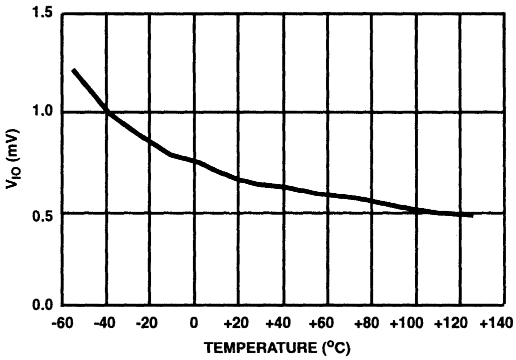


FIGURE 26. INPUT OFFSET VOLTAGE vs TEMPERATURE

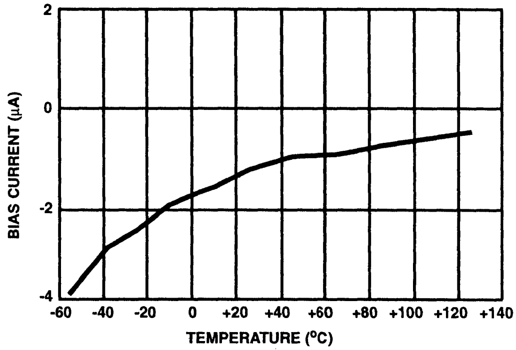


FIGURE 27. +INPUT BIAS CURRENT vs TEMPERATURE

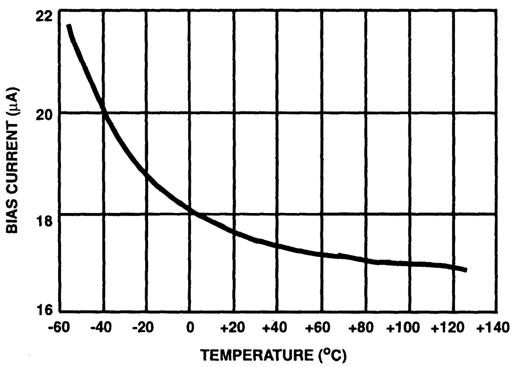


FIGURE 28. -INPUT BIAS CURRENT vs TEMPERATURE

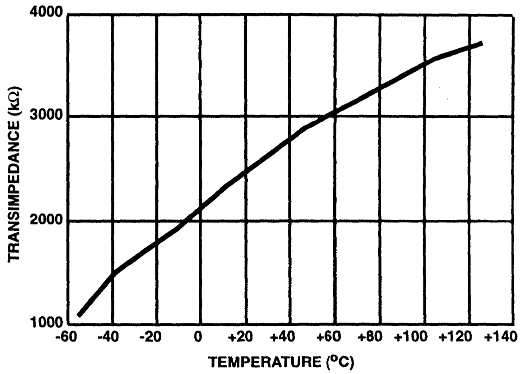


FIGURE 29. TRANSIMPEDANCE vs TEMPERATURE

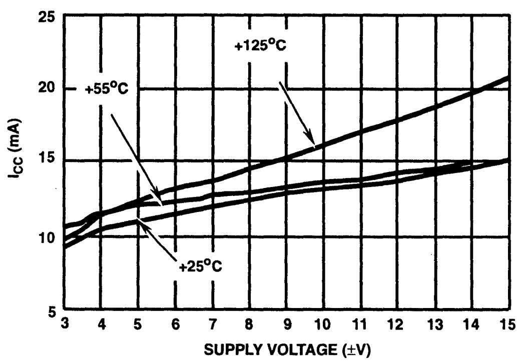


FIGURE 30. SUPPLY CURRENT vs SUPPLY VOLTAGE

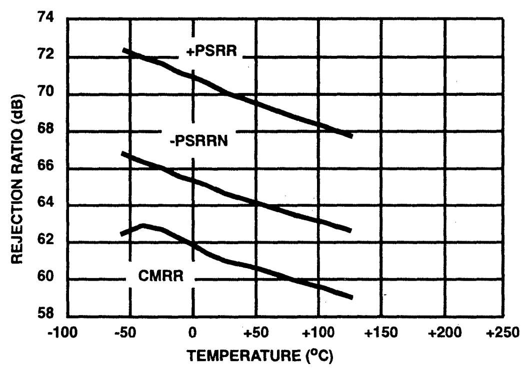


FIGURE 31. REJECTION RATIO vs TEMPERATURE

2

OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

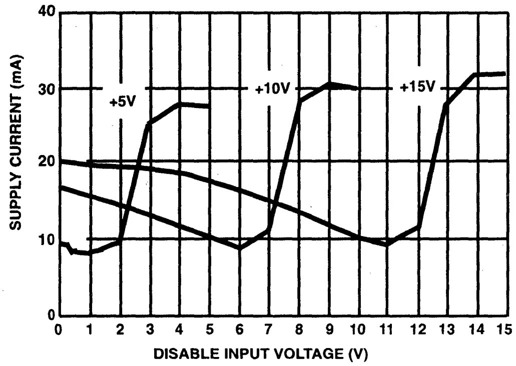


FIGURE 32. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

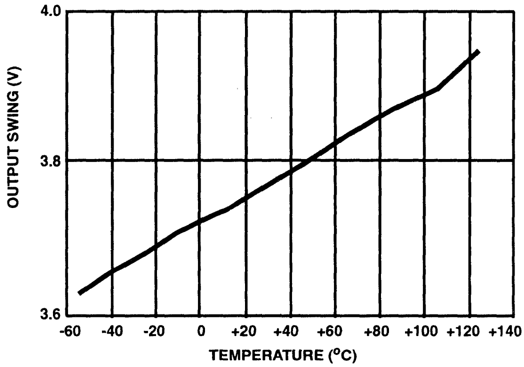


FIGURE 33. OUTPUT SWING vs TEMPERATURE

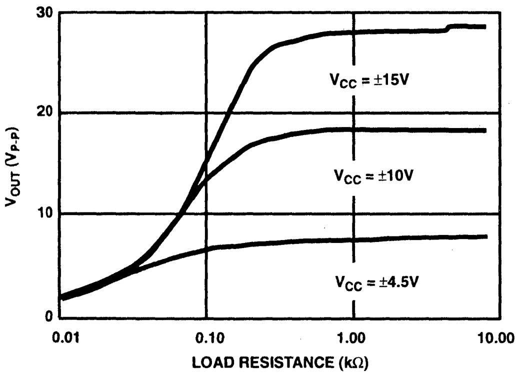


FIGURE 34. OUTPUT SWING vs LOAD RESISTANCE

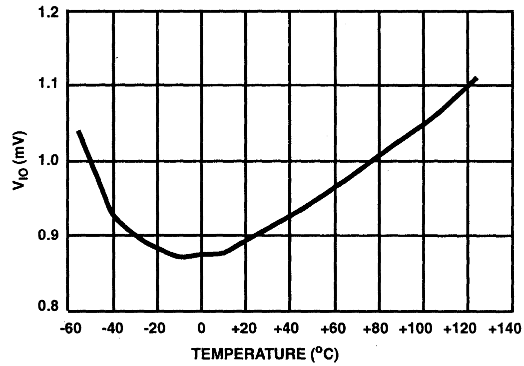


FIGURE 35. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

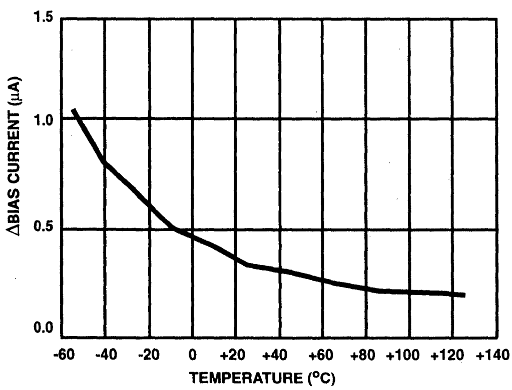


FIGURE 36. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

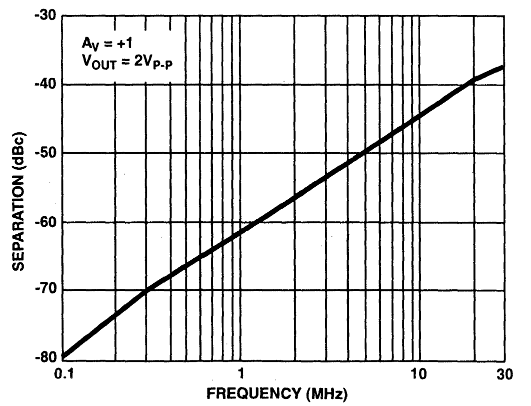


FIGURE 37. CHANNEL SEPARATION vs FREQUENCY

Typical Performance Curves V_{SUPPLY} = ±5V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = 25°C, Unless Otherwise Specified **(Continued)**

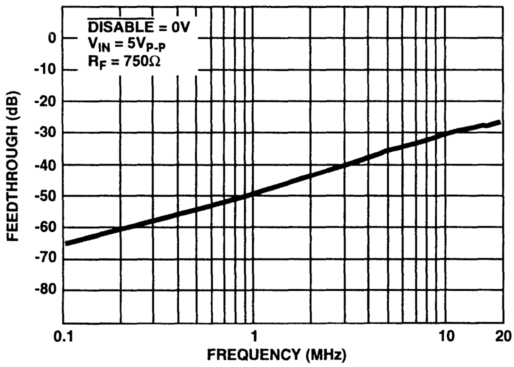


FIGURE 38. DISABLE FEEDTHROUGH vs FREQUENCY

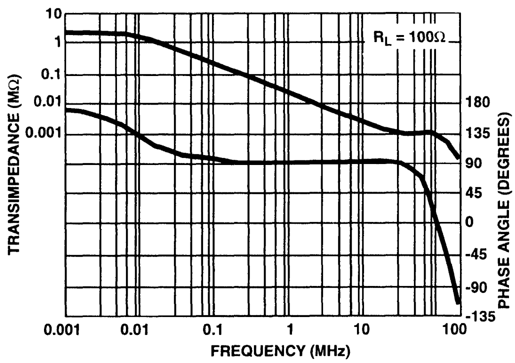


FIGURE 39. TRANSIMPEDANCE vs FREQUENCY

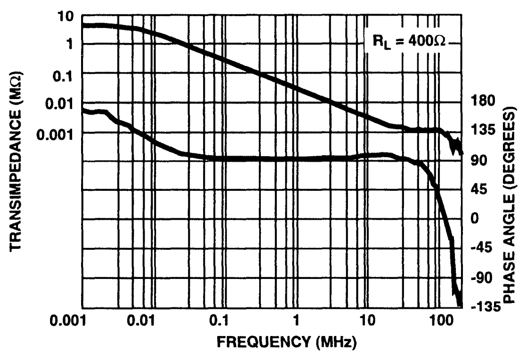


FIGURE 40. TRANSIMPEDENCE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:
1650μm x 2540μm x 483μm ±25.4μm

METALLIZATION:
Type: Metal 1: AlCu (1%), Metal 2: AlCu (1%)
Thickness: Metal 1: 8kÅ ± 0.4kÅ, Metal 2: 16kÅ ± 0.8kÅ

WORST CASE CURRENT DENSITY:
1.9×10^5 A/cm^2 at 15mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.4kÅ

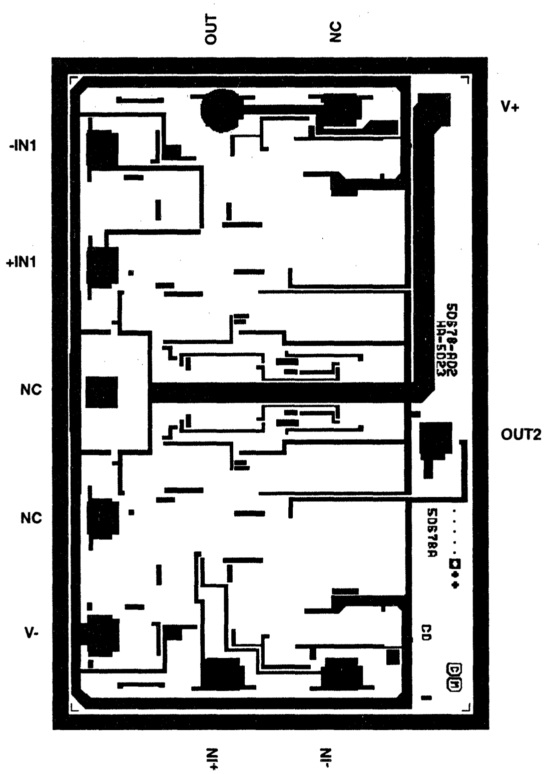
TRANSISTOR COUNT: 124

PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC

Metallization Mask Layout

HA5023



HARRIS SEMICONDUCTOR

HA5024

Quad 125MHz Video Current Feedback Amplifier with Disable

July 1995

Features

- Quad Version of HA-5020
- Individual Output Enable/Disable
- Input Offset Voltage 800μV
- Wide Unity Gain Bandwidth 125MHz
- Slew Rate 475V/μs
- Differential Gain 0.03%
- Differential Phase . . . . 0.03 Deg.
- Supply Current (per Amplifier) 7.5mA
- ESD Protection 4000V
- Guaranteed Specifications at ±5V Supplies

Applications

- Video Multiplexers; Video Switching and Routing
- Video Gain Block
- Video Distribution Amplifier/RGB Amplifier
- Flash A/D Driver
- Current to Voltage Converter
- Medical Imaging
- Radar and Imaging Systems

Description

The HA5024 is a quad version of the popular Harris HA5020. It features wide bandwidth and high slew rate, and is optimized for video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The HA5024 also features a disable function that significantly reduces supply current while forcing the output to a true high impedance state. This functionality allows 2:1 and 4:1 video multiplexers to be implemented with a single IC.

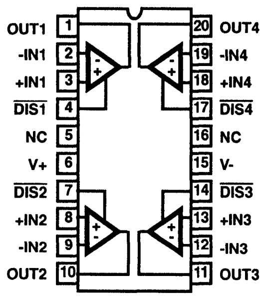
The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor. By reducing R_F, the bandwidth can be increased to compensate for decreases at higher closed loop gains or heavy output loads.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA5024IP	-40°C to +85°C	20 Lead Plastic DIP
HA5024IB	-40°C to +85°C	20 Lead Plastic SOIC (W)

Pinout

HA5024
(PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings (Note 1)

ESD Protection (Note 22) 2000V
Voltage Between V+ and V- Terminals 36V
DC Input Voltage . . . . . $\pm V_{SUPPLY}$
Differential Input Voltage 10V
Output Current (Note 2) . . . . . Short Circuit Protected
Junction Temperature (Note 19) . . . . . +175°C
Junction Temperature (Plastic Package) (Note 19) . . . . . +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HA5024I . . . . . $-40^oC \le T_A \le +85^oC$
Supply Voltage Range . . . . . ±4.5V to ±15V
Storage Temperature Range . . . . . $-65^oC \le T_A \le +150^oC$
Thermal Package Characteristics (°C/W) θ_{JA}
Plastic DIP 75
SOIC 90

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \le 10pF$, Unless Otherwise Specified

PARAMETER	(NOTE 12) TEST LEVEL	TEMPERATURE	HA5024I MIN	HA5024I TYP	HA5024I MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage (V_{IO})	A	+25°C	-	0.8	3	mV
	A	Full	-	-	5	mV
Delta V_{IO} Between Channels	A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift	B	Full	-	5	-	µV/°C
V_{IO} Common Mode Rejection Ratio (Note 3)	A	+25°C	53	-	-	dB
	A	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio (Note 4)	A	+25°C	60	-	-	dB
	A	Full	55	-	-	dB
Input Common Mode Range (Note 3)	A	Full	±2.5	-	-	V
Non-Inverting Input (+IN) Current	A	+25°C	-	3	8	µA
	A	Full	-	-	20	µA
+IN Common Mode Rejection (Note 3)	A	+25°C	-	-	0.15	µA/V
$(+I_{BCMR} = \frac{1}{R_{IN}})$	A	Full	-	-	0.5	µA/V
+IN Power Supply Rejection (Note 4)	A	+25°C	-	-	0.1	µA/V
	A	Full	-	-	0.3	µA/V
Inverting Input (-IN) Current	A	+25°C,+85°C	-	4	12	µA
	A	-40°C	-	10	30	µA
Delta -IN BIAS Current Between Channels	A	+25°C,+85°C	-	6	15	µA
	A	-40°C	-	10	30	µA
-IN Common Mode Rejection (Note 3)	A	+25°C	-	-	0.4	µA/V
	A	Full	-	-	1.0	µA/V
-IN Power Supply Rejection (Note 4)	A	+25°C	-	-	0.2	µA/V
	A	Full	-	-	0.5	µA/V
Input Noise Voltage (f = 1kHz)	B	+25°C	-	4.5	-	$nV/\sqrt{Hz}$
+Input Noise Current (f = 1kHz)	B	+25°C	-	2.5	-	$pA/\sqrt{Hz}$
-Input Noise Current (f = 1kHz)	B	+25°C	-	25.0	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Transimpedence (Note 21)	A	+25°C	1.0	-	-	MΩ
	A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain, $R_L = 400\Omega$, $V_{OUT} = \pm 2.5V$	25A	+25°C	70	-	-	dB
	A	Full	65	-	-	dB
Open Loop DC Voltage Gain, $R_L = 100\Omega$, $V_{OUT} = \pm 2.5V$	A	+25°C	50	-	-	dB
	A	Full	45	-	-	dB

Electrical Specifications V+ = +5V, V- = -5V, R_F = 1kΩ, A_V = +1, R_L = 400Ω, C_L ≤ 10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 12) TEST LEVEL	TEMPERATURE	HA5024I MIN	HA5024I TYP	HA5024I MAX	UNITS
OUTPUT CHARACTERISTICS						
Output Voltage Swing, (Note 20)	A	+25°C	±2.5	±3.0	-	V
	A	Full	±2.5	±3.0	-	V
Output Current (Note 20)	B	Full	±16.6	±20.0	-	mA
Output Current (Short Circuit, Note13)	A	Full	±40	±60	-	mA
Output Current (Disabled, Notes 5, 14)	A	Full	-	-	2	µA
Output Disable Time (Note15)	B	+25°C	-	40	-	µs
Output Enable Time (Note 16)	B	+25°C	-	40	-	ns
Output Capacitance (Disabled, Notes 5, 17)	B	+25°C	-	15	-	pF
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range	A	+25°C	5	-	15	V
Quiescent Supply Current	A	Full	-	7.5	10	mA/Op Amp
Supply Current, Disabled (Note 5)	A	Full	-	5	7.5	mA/Op Amp
$\overline{\text{Disable}}$ Pin Input Current (Note 5)	A	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable (Note 6)	A	Full	350	-	-	µA
Maximum Pin 8 Current to Enable (Note 7)	A	Full	-	-	20	µA
AC CHARACTERISTICS (A_V = +1)						
Slew Rate (Note 8)	B	+25°C	275	350	-	V/µs
Full Power Bandwidth (Note 9)	B	+25°C	22	28	-	MHz
Rise Time (Note 10)	B	+25°C	-	6	-	ns
Fall Time (Note 10)	B	+25°C	-	6	-	ns
Propagation Delay (Note 10)	B	+25°C	-	6	-	ns
Overshoot	B	+25°C	-	4.5	-	%
-3dB Bandwidth (Note 11)	B	+25°C	-	125	-	MHz
Settling Time to 1%, 2V Output Step	B	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step	B	+25°C	-	75	-	ns
AC CHARACTERISTICS (A_V = +2, R_F = 681Ω)						
Slew Rate (Note 8)	B	+25°C	-	475	-	V/µs
Full Power Bandwidth (Note 9)	B	+25°C	-	26	-	MHz
Rise Time (Note 10)	B	+25°C	-	6	-	ns
Fall Time (Note 10)	B	+25°C	-	6	-	ns
Propagation Delay (Note 10)	B	+25°C	-	6	-	ns
Overshoot	B	+25°C	-	12	-	%
-3dB Bandwidth (Note 11)	B	+25°C	-	95	-	MHz
Settling Time to 1%, 2V Output Step	B	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step	B	+25°C	-	100	-	ns
Gain Flatness 5MHz	B	+25°C	-	0.02	-	dB
20MHz	B	+25°C	-	0.07	-	dB
AC CHARACTERISTICS (A_V = +10, R_F = 383Ω)						
Slew Rate (Note 8)	B	+25°C	350	475	-	V/µs
Full Power Bandwidth (Note 9)	B	+25°C	28	38	-	MHz
Rise Time (Note 10)	B	+25°C	-	8	-	ns

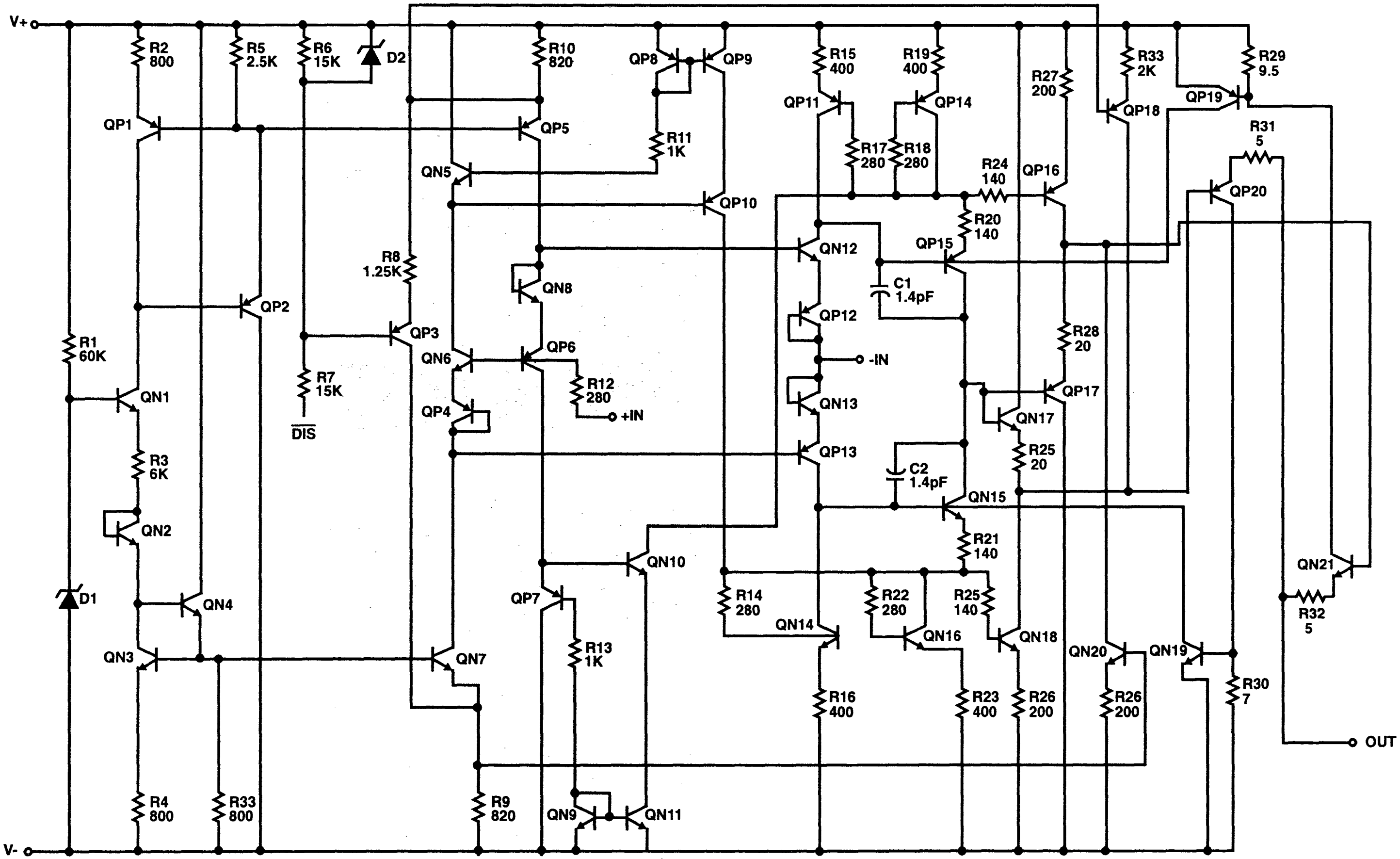
Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 12) TEST LEVEL	TEMPERATURE	HA5024I			UNITS
			MIN	TYP	MAX	
Fall Time (Note 10)	B	+25°C	-	9	-	ns
Propagation Delay (Note 10)	B	+25°C	-	9	-	ns
Overshoot	B	+25°C	-	1.8	-	%
-3dB Bandwidth (Note 11)	B	+25°C	-	65	-	MHz
Settling Time to 1%, 2V Output Step	B	+25°C	-	75	-	ns
Settling Time to 0.1%, 2V Output Step	B	+25°C	-	130	-	ns
VIDEO CHARACTERISTICS						
Differential Gain (Notes 18, 20)	B	+25°C	-	0.03	-	%
Differential Phase (Notes 18, 20)	B	+25°C	-	0.03	-	Degrees

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.
3. $V_{CM} = \pm 2.5V$. At -40°C Product is tested at $V_{CM} = \pm 2.25V$ because short test duration does not allow self heating.
4. $\pm 3.5V \leq V_S \leq \pm 6.5V$.
5. $\overline{\text{Disable}} = 0V$.
6. $R_L = 100\Omega$, $V_{IN} = 2.5V$. This is the minimum current which must be pulled out of the $\overline{\text{Disable}}$ pin in order to disable the output. The output is considered disabled when $-10mV \leq V_{OUT} \leq +10mV$.
7. $V_{IN} = 0V$. This is the maximum current that can be pulled out of the $\overline{\text{Disable}}$ pin with the HA5024 remaining enabled. The HA5024 is considered disabled when the supply current has decreased by at least 0.5mA.
8. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
9. $FPBW = \dfrac{\text{Slew Rate}}{2\pi V_{PEAK}}; V_{PEAK} = 2V$
10. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
11. $R_L = 400\Omega$, $V_{OUT} = 100mV$.
12. A. Production Tested; B. Guaranteed Limit or Typical based on characterization; C. Design Typical for information only.
13. $V_{IN} = \pm 2.5V$, $V_{OUT} = 0V$.
14. $V_{OUT} = \pm 2.5V$, $V_{IN} = 0V$.
15. $V_{IN} = +2V$, $\overline{\text{Disable}} = +5V$ to 0V. Measured from the 50% point of $\overline{\text{Disable}}$ to $V_{OUT} = 0V$.
16. $V_{IN} = +2V$, $\overline{\text{Disable}} = 0V$ to +5V. Measured from the 50% point of $\overline{\text{Disable}}$ to $V_{OUT} = 2V$.
17. $V_{IN} = 0V$, Force V_{OUT} from 0V to $\pm 2.5V$, $t_R = t_F = 50ns$.
18. Measured with a VM700A video tester using an NTC-7 composite VITS.
19. Maximum power dissipation, including output load, must be designed to maintain junction temperature below +175°C for die, and below +150°C for plastic packages. See Applications Information section for safe operating area information.
20. $R_L = 150\Omega$.
21. $V_{OUT} = \pm 2.5V$. At -40°C Product is tested at $V_{OUT} = \pm 2.25V$ because short test duration does not allow self heating.
22. ESD Protection is for human body model tested per MIL-STD-883, Method 3015.7.

Schematic



HA5024

Test Circuits

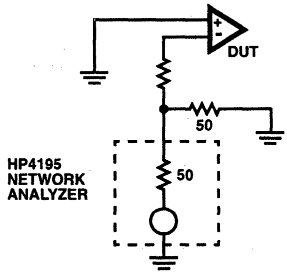


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

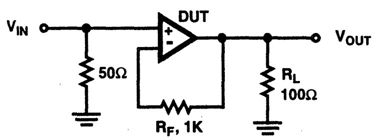


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

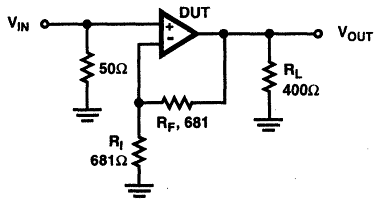


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT

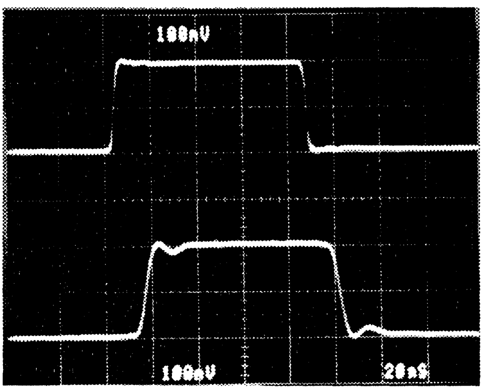


FIGURE 4. SMALL SIGNAL RESPONSE
Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

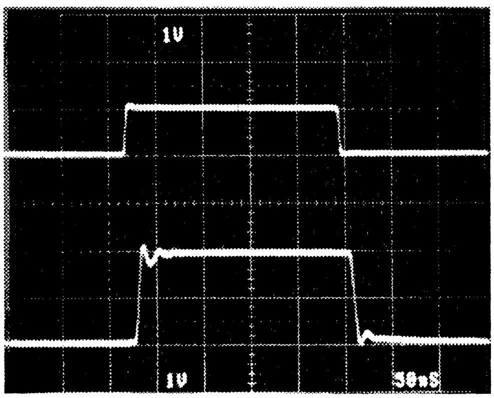


FIGURE 5. LARGE SIGNAL RESPONSE
Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 11 and Figure 12 in the Typical Performance Curves section, illustrate the performance of the HA5024 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA5024 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10µF) tantalum or electrolytic capacitor in parallel with a small value (0.1µF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

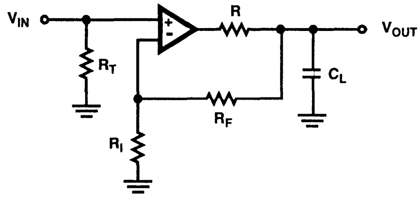


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resister is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Power Dissipation Considerations

Due to the high supply current inherent in quad amplifiers, care must be taken to insure that the maximum junction temperature (T_J, see Absolute Maximum Ratings) is not exceeded. Figure 7 shows the maximum ambient temperature versus supply voltage for the available package styles (Plastic DIP, SOIC). At $\pm 5V_{DC}$ quiescent operation both package styles may be operated over the full industrial range of -40°C to +85°C. It is recommended that thermal calculations, which take into account output power, be performed by the designer.

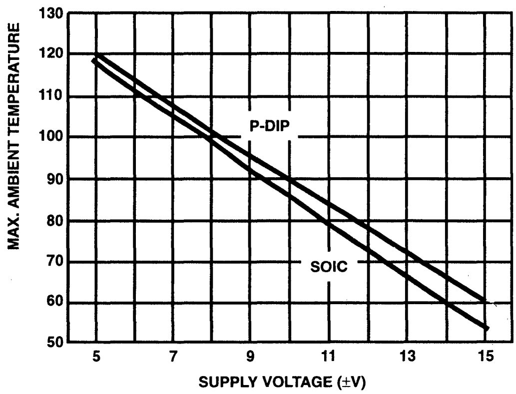


FIGURE 7. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

Enable/Disable Function

When enabled the amplifier functions as a normal current feedback amplifier with all of the data in the electrical specifications table being valid and applicable. When disabled the amplifier output assumes a true high impedance state and the supply current is reduced significantly.

The circuit shown in Figure 8 is a simplified schematic of the enable/disable function. The large value resistors in series with the DISABLE pin makes it appear as a current source to the driver. When the driver pulls this pin low current flows out of the pin and into the driver. This current, which may be as large as 350µA when external circuit and process variables are at their extremes, is required to insure that point "A" achieves the proper potential to disable the output.The driver must have the compliance and capability of sinking all of this current.

When V_{CC} is +5V the DISABLE pin may be driven with a dedicated TTL gate. The maximum low level output voltage of the TTL gate, 0.4V, has enough compliance to insure that the amplifier will always be disabled even though D1 will not turn on, and the TTL gate will sink enough current to keep point "A" at its proper voltage. When V_{CC} is greater than +5V the DISABLE pin should be driven with an open collector device that has a breakdown rating greater than V_{CC}.

Referring to Figure 8, it can be seen that R6 will act as a pull-up resistor to $+V_{CC}$ if the DISABLE pin is left open. In those cases where the enable/disable function is not required on all circuits some circuits can be permanently enabled by letting the DISABLE pin float. If a driver is used to set the enable/disable level, be sure that the driver does not sink more than 20µA when the DISABLE pin is at a high level. TTL gates, especially CMOS versions, do not violate this criteria so it is permissible to control the enable/disable function with TTL.

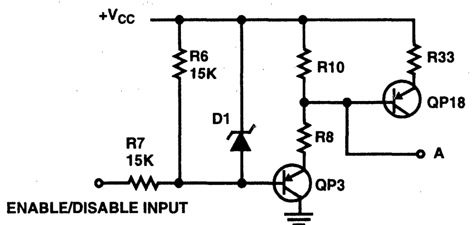


FIGURE 8. SIMPLIFIED SCHEMATIC OF ENABLE/DISABLE FUNCTION

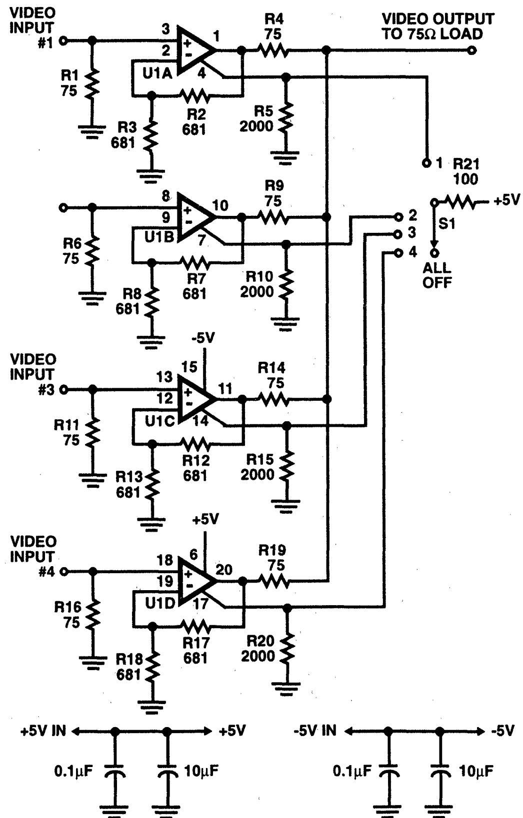
Four Channel Video Multiplexer

Referring to the amplifier U1A in Figure 9, R1 terminates the cable in its characteristic impedance of 75Ω, and R4 back terminates the cable in its characteristic impedance. The amplifier is set up in a gain configuration of +2 to yield an overall network gain of +1 when driving a double terminated cable. The value of R3 can be changed if a different network gain is desired. R5 holds the disable pin at ground thus inhibiting the amplifier until the switch, S1, is thrown to position 1. At position 1 the switch pulls the disable pin up to the plus supply rail thereby enabling the amplifier. Since all of the actual signal switching takes place within the amplifier, it's differential gain and phase parameters, which are 0.03% and 0.03 degrees respectively, determine the circuit's performance. The other three circuits, U1B through U1D, operate in a similar manner.

When the plus supply rail is 5V the disable pin can be driven by a dedicated TTL gate as discussed earlier. If a multiplexer IC or its equivalent is used to select channels its logic must be break before make. When these conditions are satisfied the HA5024IP is often used as a remote video multiplexer, and the multiplexer may be extended by adding more amplifier ICs.

Low Impedance Multiplexer

Two common problems surface when you try to multiplex multiple high speed signals into a low impedance source such as an A/D converter. The first problem is the low source impedance which tends to make amplifiers oscillate and causes gain errors. The second problem is the multiplexer which supplies no gain, introduces all kinds of distortion and limits the frequency response. Using op amps which have an enable/disable function, such as the HA5024, eliminates the multiplexer problems because the external mux chip is not needed, and the HA5024 can drive low impedance (large capacitance) loads if a series isolation resistor is used.



NOTES:

1. U1 is HA5024IP
2. All resistors in Ω
3. S1 is break before make
4. Use ground plane

FIGURE 9. FOUR CHANNEL VIDEO MULTIPLEXER

Referring to Figure 10, both inputs are terminated in their characteristic impedance; 75Ω is typical for video applications. Since the drivers usually are terminated in their characteristic impedance the input gain is 0.5, thus the amplifiers, U2, are configured in a gain of +2 to set the circuit gain equal to one. Resistors R2 and R3 determine the amplifier gain, and if a different gain is desired R2 should be changed according to the equation G = (1 + R3/R2). R3 sets the frequency response of the amplifier so you should refer to the manufacturers data sheet before changing it's value. R5, C1 and D1 are an asymmetrical charge/discharge time circuit which configures U1 as a break before make switch to prevent both amplifiers from being active simultaneously. If this design is extended to more channels the drive logic must be designed to be break before make. R4 is enclosed in the feedback loop of the amplifier so that the large open loop amplifier gain of U2 will present the load with a small closed loop output impedance while keeping the amplifier stable for all values of load capacitance.

The circuit shown in Figure 10 was tested for the full range of capacitor values with no oscillations being observed; thus, problem one has been solved.The frequency and gain characteristics of the circuit are now those of the amplifier independent of any multiplexing action; thus, problem two has been solved. The multiplexer transition time is approximately 15μs with the component values shown.

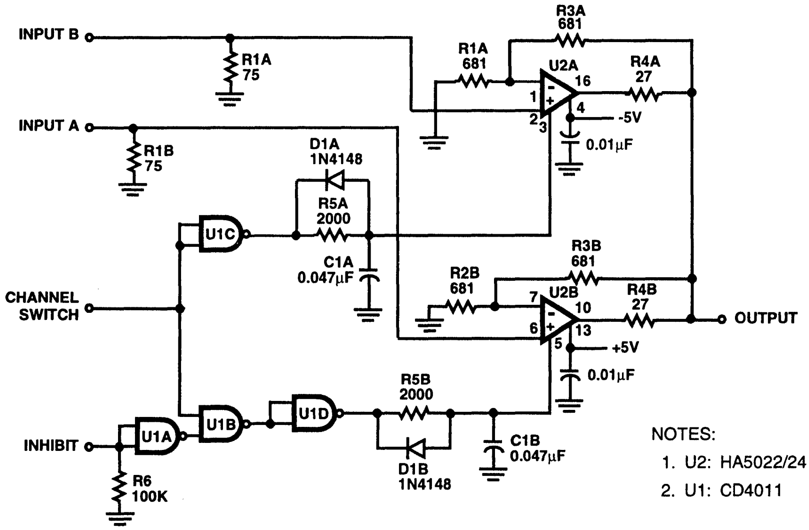


FIGURE 10. LOW IMPEDANCE MULTIPLEXER

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified

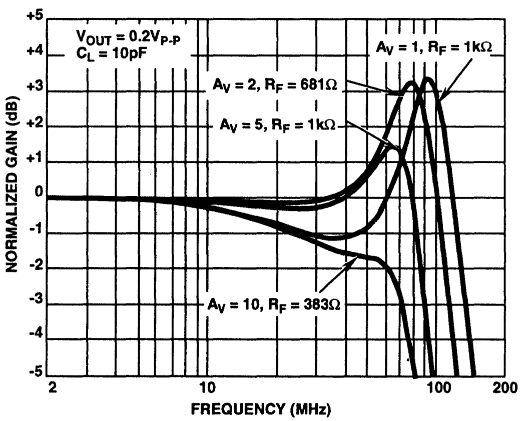


FIGURE 11. NON-INVERTING FREQENCY RESPONSE

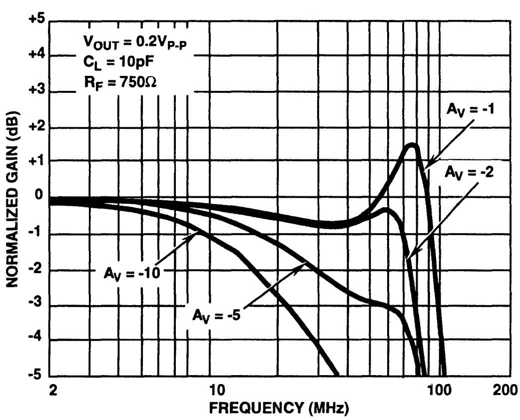


FIGURE 12. INVERTING FREQUENCY RESPONSE

Typical Performance Curves V_{SUPPLY} = ±5V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = 25°C, Unless Otherwise Specified **(Continued)**

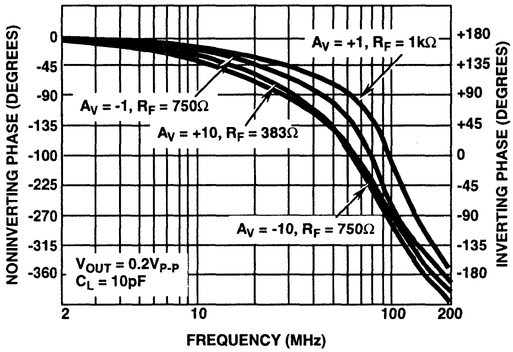


FIGURE 13. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

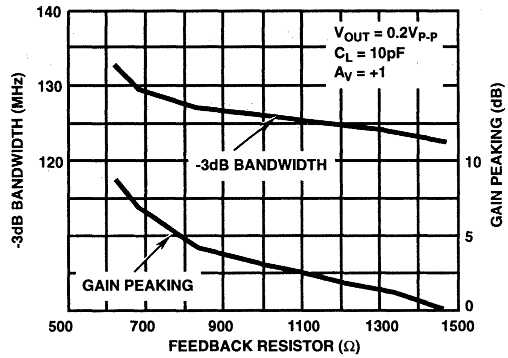


FIGURE 14. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

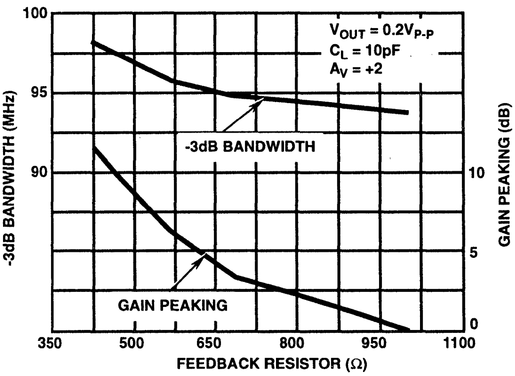


FIGURE 15. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

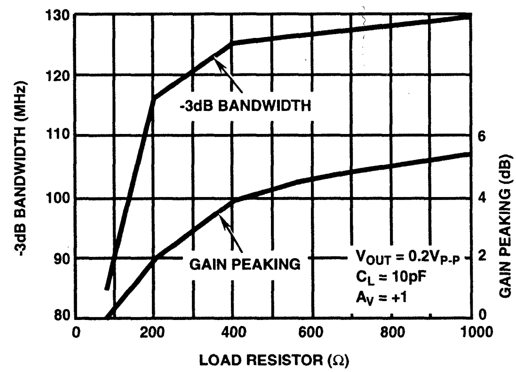


FIGURE 16. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

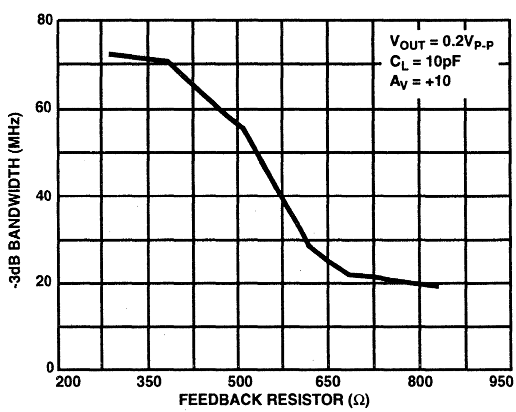


FIGURE 17. BANDWIDTH vs FEEDBACK RESISTANCE

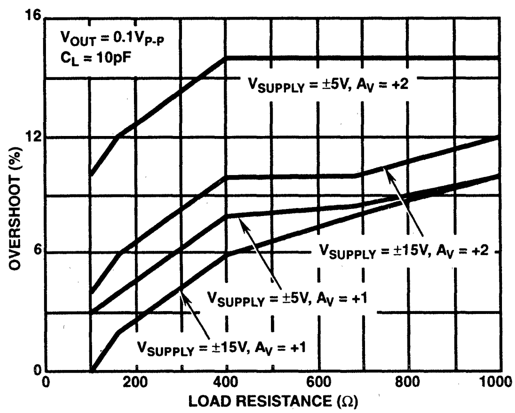


FIGURE 18. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

Typical Performance Curves V_{SUPPLY} = ±5V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = 25°C, Unless Otherwise Specified **(Continued)**

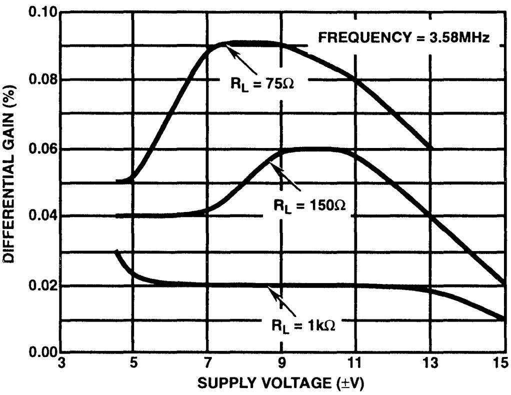


FIGURE 19. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

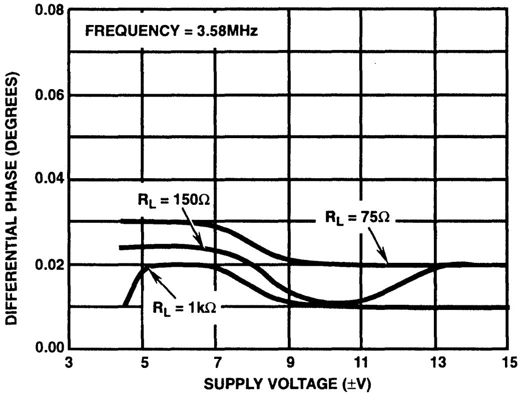


FIGURE 20. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

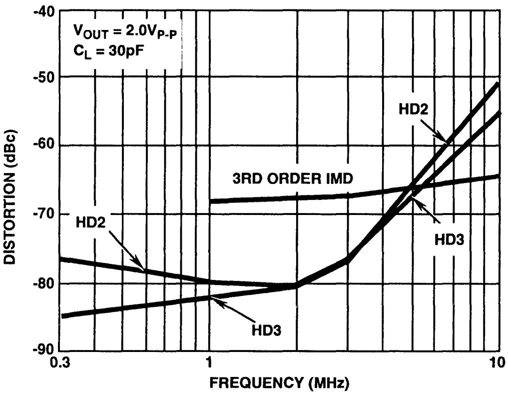


FIGURE 21. DISTORTION vs FREQUENCY

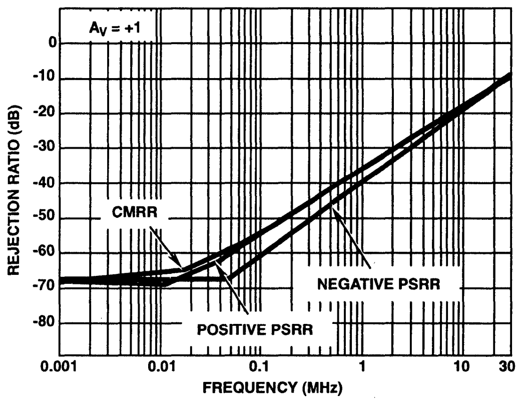


FIGURE 22. REJECTION RATIOS vs FREQUENCY

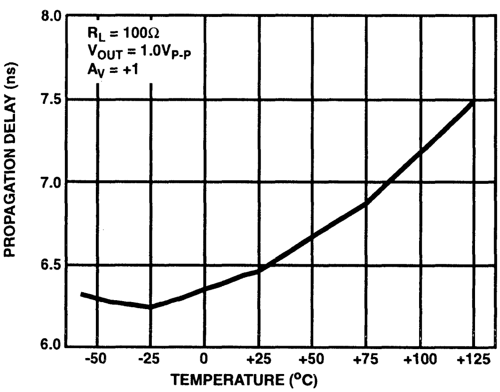


FIGURE 23. PROPAGATION DELAY vs TEMPERATURE

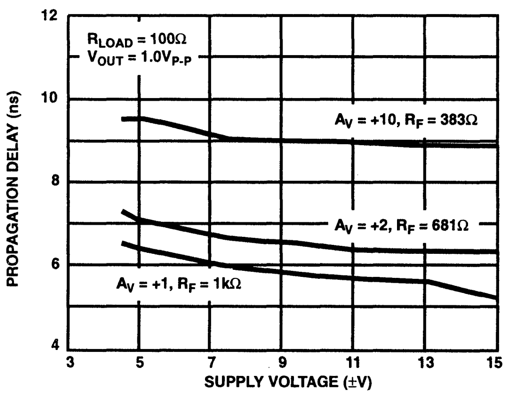


FIGURE 24. PROPAGATION DELAY vs SUPPLY VOLTAGE

2

OPERATIONAL AMPLIFIERS

Typical Performance Curves V_{SUPPLY} = ±5V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = 25°C, Unless Otherwise Specified **(Continued)**

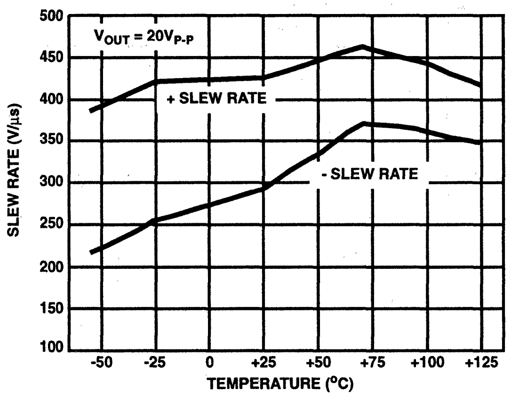


FIGURE 25. SLEW RATE vs TEMPERATURE

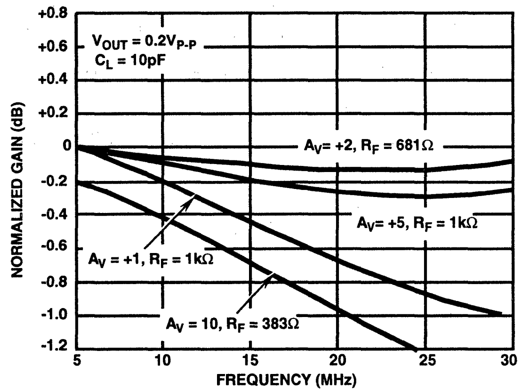


FIGURE 26. NON-INVERTING GAIN FLATNESS vs FREQUENCY

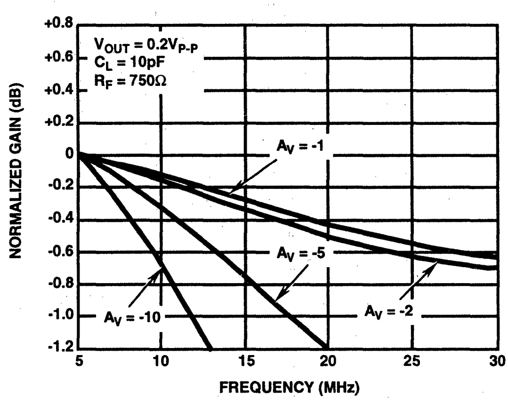


FIGURE 27. INVERTING GAIN FLATNESS vs FREQUENCY

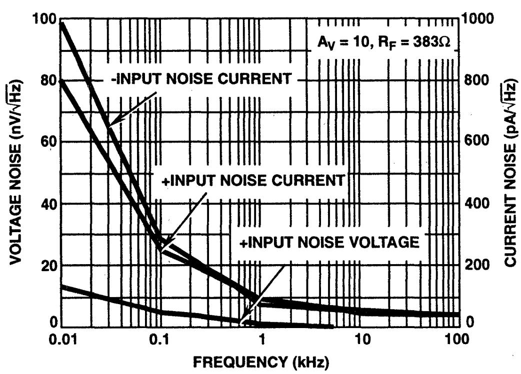


FIGURE 28. INPUT NOISE CHARACTERISTICS

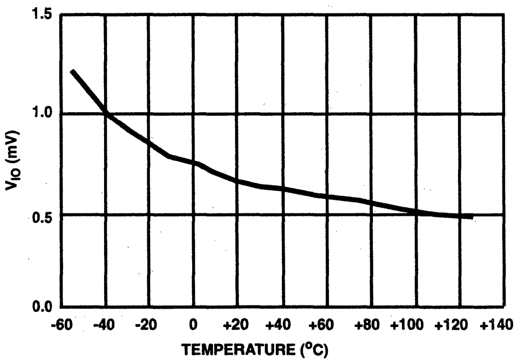


FIGURE 29. INPUT OFFSET VOLTAGE vs TEMPERATURE

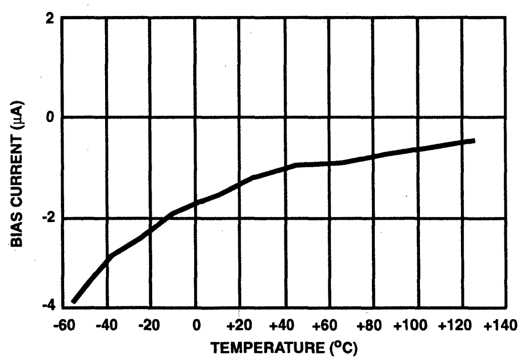


FIGURE 30. +INPUT BIAS CURRENT vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

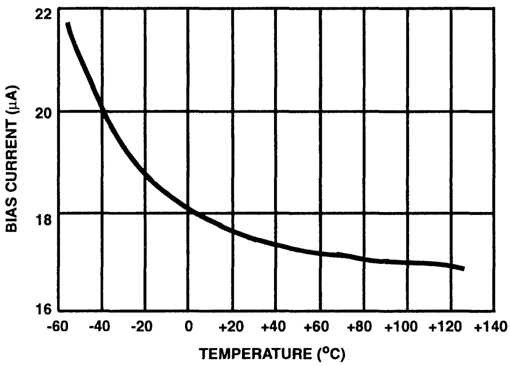


FIGURE 31. -INPUT BIAS CURRENT vs TEMPERATURE

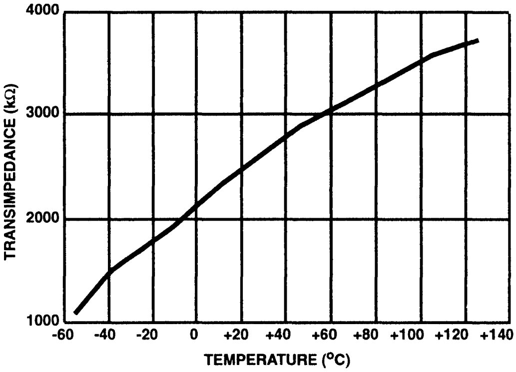


FIGURE 32. TRANSIMPEDANCE vs TEMPERATURE

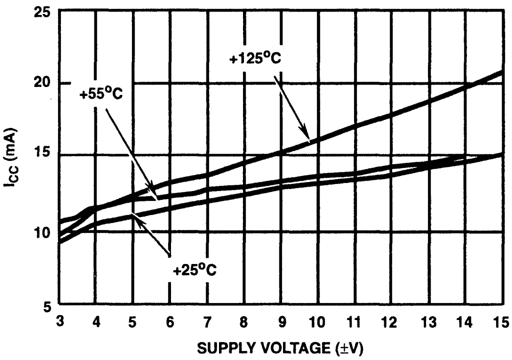


FIGURE 33. SUPPLY CURRENT vs SUPPLY VOLTAGE

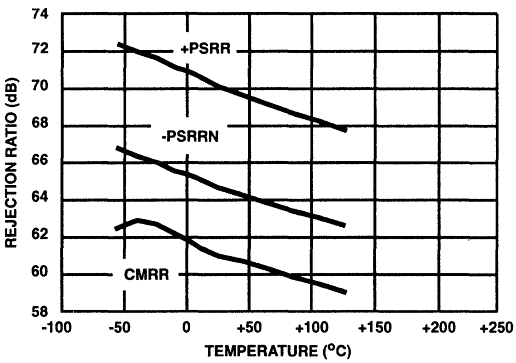


FIGURE 34. REJECTION RATIO vs TEMPERATURE

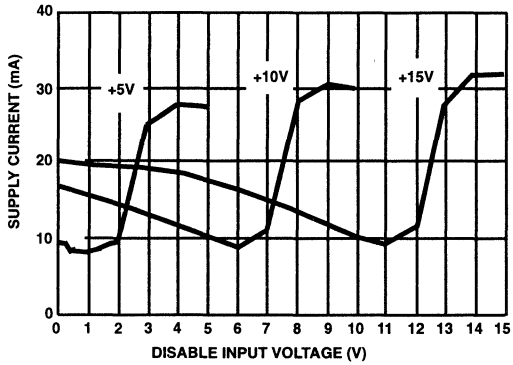


FIGURE 35. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

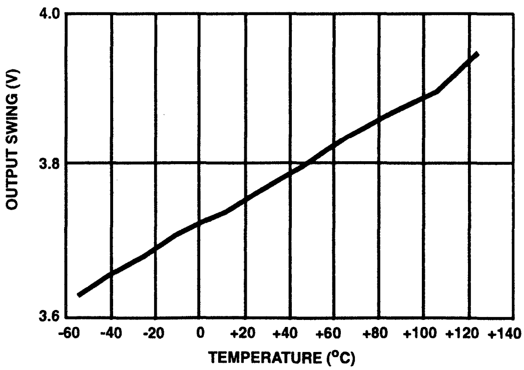


FIGURE 36. OUTPUT SWING vs TEMPERATURE

2

OPERATIONAL AMPLIFIERS

Typical Performance Curves V_{SUPPLY} = ±5V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = 25°C, Unless Otherwise Specified **(Continued)**

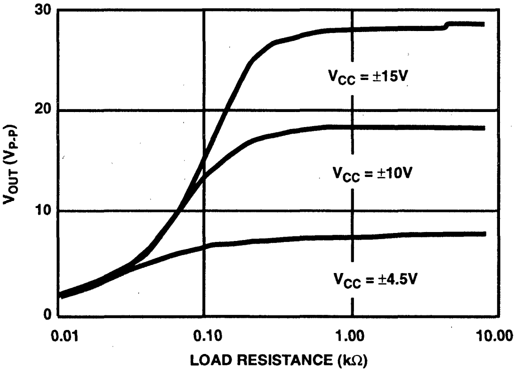


FIGURE 37. OUTPUT SWING vs LOAD RESISTANCE

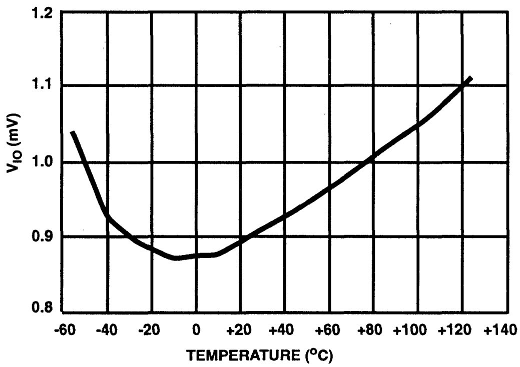


FIGURE 38. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

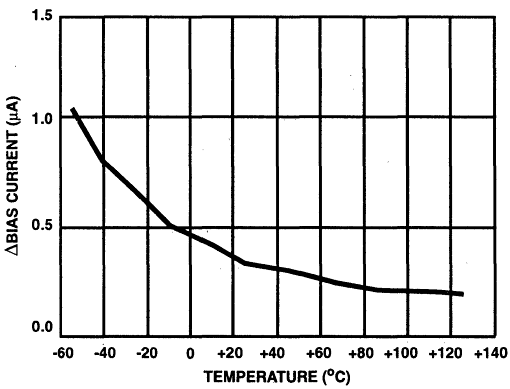


FIGURE 39. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

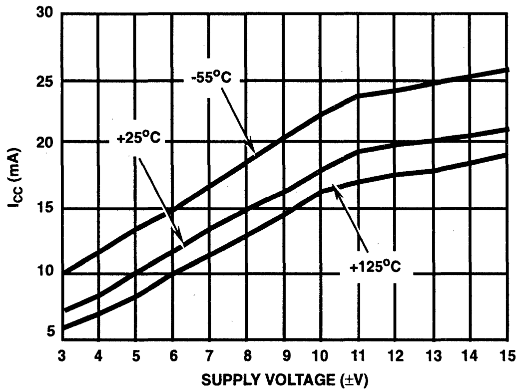


FIGURE 40. DISABLE SUPPLY CURRENT vs SUPPLY VOLTAGE

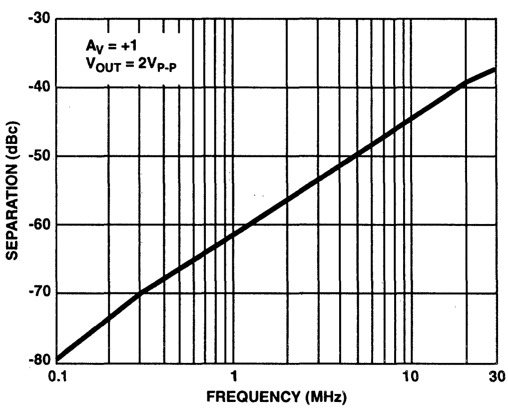


FIGURE 41. CHANNEL SEPARATION vs FREQUENCY

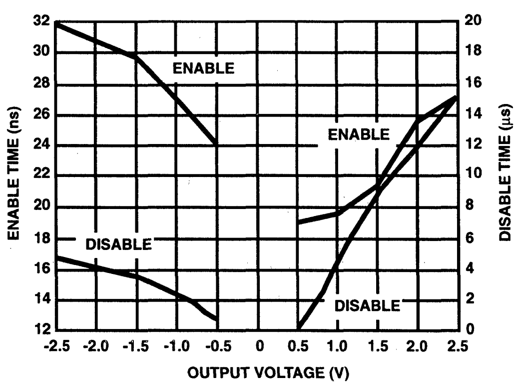


FIGURE 42. ENABLE/DISABLE TIME vs OUTPUT VOLTAGE

Typical Performance Curves V_{SUPPLY} = ±5V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = 25°C, Unless Otherwise Specified **(Continued)**

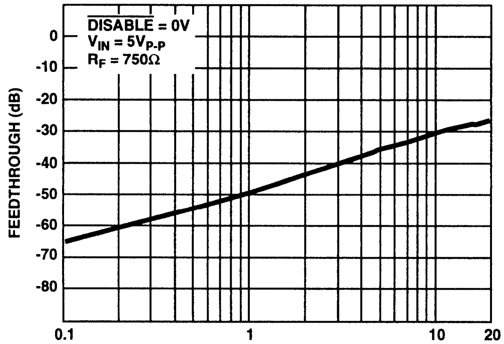


FIGURE 43. DISABLE FEEDTHROUGH vs FREQUENCY

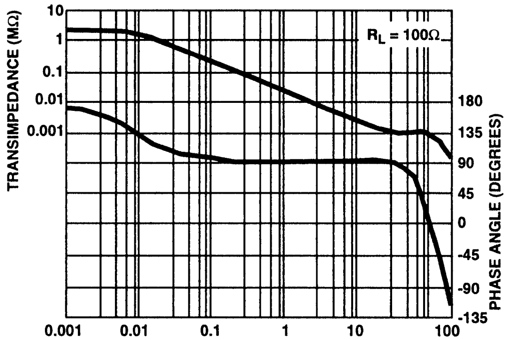


FIGURE 44. TRANSIMPEDANCE vs FREQUENCY

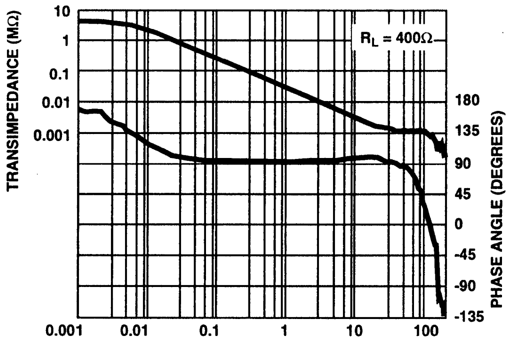


FIGURE 45. TRANSIMPEDENCE vs FREQUENCY

2

OPERATIONAL AMPLIFIERS

Die Characteristics

DIE DIMENSIONS:
2680µm x 2600µm x 483µm ±25.4µm

METALLIZATION:
Type: Metal 1: AlCu (1%), Metal 2: AlCu (1%)
Thickness: Metal 1: 8kÅ ± 0.4kÅ, Metal 2: 16kÅ ± 0.8kÅ

WORST CASE CURRENT DENSITY:
2.0×10^5 A/cm^2 at 50mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.4kÅ

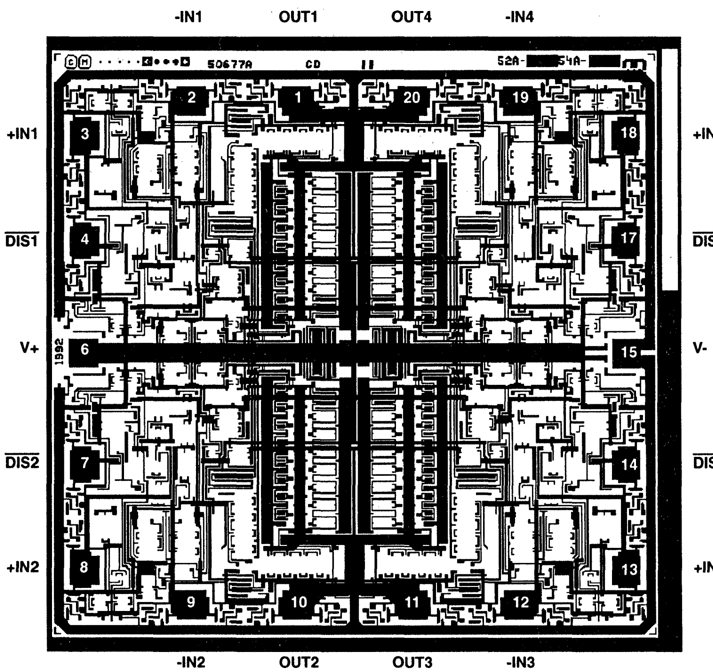
TRANSISTOR COUNT: 248

PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC

Metallization Mask Layout

HA5024



HARRIS SEMICONDUCTOR

HA5025

Quad 125MHz Video Current Feedback Amplifier

July 1995

Features

- Wide Unity Gain Bandwidth 125MHz
- Slew Rate 475V/µs
- Input Offset Voltage 800µV
- Differential Gain 0.03%
- Differential Phase .... 0.03 Deg
- Supply Current (per Amplifier) 7.5mA
- ESD Protection 4000V
- Guaranteed Specifications at ±5V Supplies

Applications

- Video Gain Block
- Video Distribution Amplifier/ RGB Amplifier
- Flash A/D Driver
- Current to Voltage Converter
- Medical Imaging
- Radar and Imaging Systems
- Video Switching and Routing

Description

The HA5025 is a wide bandwidth high slew rate quad amplifier optimized for video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor.

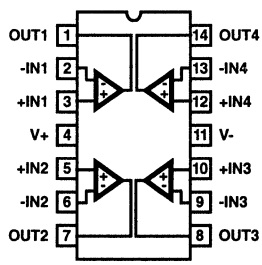
The performance of the HA5025 is very similar to the popular Harris HA-5020.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA5025IP	-40°C to +85°C	14 Lead Plastic DIP
HA5025IB	-40°C to +85°C	14 Lead Plastic SOIC (N)

Pinout

HA5025
(PDIP, SOIC)
TOP VIEW



File Number 3591.2

Absolute Maximum Ratings (Note 1)

ESD Protection (Note 15) 2000V
Voltage Between V+ and V- Terminals 36V
DC Input Voltage .... $\pm V_{SUPPLY}$
Differential Input Voltage 10V
Output Current (Note 2) .... Short Circuit Protected
Junction Temperature (Note 12) .... +175°C
Junction Temperature (Plastic Package) (Note 12) .... +150°C
Lead Temperature (Soldering 10s) .... +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HA5025I .... $-40^oC \leq T_A \leq +85^oC$
Supply Voltage Range .... ±4.5V to ±15V
Storage Temperature Range .... $-65^oC \leq T_A \leq +150^oC$
Thermal Package Characteristics (°C/W) θ_{JA}
Plastic DIP 100
SOIC 120

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	(NOTE 16) TEST LEVEL	TEMPERATURE	HA5025I MIN	HA5025I TYP	HA5025I MAX	UNITS
INPUT CHARACTERISTICS						
Input Offset Voltage (V_{IO})	A	+25°C	-	0.8	3	mV
	A	Full	-	-	5	mV
Delta V_{IO} Between Channels	A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift	B	Full	-	5	-	μV/°C
V_{IO} Common Mode Rejection Ratio (Note 3)	A	+25°C	53	-	-	dB
	A	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio (Note 4)	A	+25°C	60	-	-	dB
	A	Full	55	-	-	dB
Input Common Mode Range (Note 3)	A	Full	±2.5	-	-	V
Non-Inverting Input (+IN) Current	A	+25°C	-	3	8	μA
	A	Full	-	-	20	μA
+IN Common Mode Rejection (Note 3) ($+I_{BCMR} = \frac{1}{+R_{IN}}$)	A	+25°C	-	-	0.15	μA/V
	A	Full	-	-	0.5	μA/V
+IN Power Supply Rejection (Note 4)	A	+25°C	-	-	0.1	μA/V
	A	Full	-	-	0.3	μA/V
Inverting Input (-IN) Current	A	+25°C, +85°C	-	4	12	μA
	A	-40°C	-	10	30	μA
Delta - IN BIAS Current Between Channels	A	+25°C, +85°C	-	6	15	μA
	A	-40°C	-	10	30	μA
-IN Common Mode Rejection (Note 3)	A	+25°C	-	-	0.4	μA/V
	A	Full	-	-	1.0	μA/V
-IN Power Supply Rejection (Note 4)	A	+25°C	-	-	0.2	μA/V
	A	Full	-	-	0.5	μA/V
Input Noise Voltage (f = 1kHz)	B	+25°C	-	4.5	-	$nV/\sqrt{Hz}$
+Input Noise Current (f = 1kHz)	B	+25°C	-	2.5	-	$pA/\sqrt{Hz}$
-Input Noise Current (f = 1kHz)	B	+25°C	-	25.0	-	$pA/\sqrt{Hz}$

Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 16) TEST LEVEL	TEMPERATURE	HA5025I MIN	HA5025I TYP	HA5025I MAX	UNITS
TRANSFER CHARACTERISTICS						
Transimpedance (Note 14)	A	+25°C	1.0	-	-	MΩ
	A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain, $R_L = 400\Omega$, $V_{OUT} = \pm2.5V$	A	+25°C	70	-	-	dB
	A	Full	65	-	-	dB
Open Loop DC Voltage Gain, $R_L = 100\Omega$, $V_{OUT} = \pm2.5V$	A	+25°C	50	-	-	dB
	A	Full	45	-	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing (Note 13)	A	+25°C	±2.5	±3.0	-	V
	A	Full	±2.5	±3.0	-	V
Output Current (Note 13)	B	Full	±16.6	±20.0	-	mA
Output Current (Short Circuit, Note 10)	A	Full	±40	±60	-	mA
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range	A	+25°C	5	-	15	V
Quiescent Supply Current	A	Full	-	7.5	10	mA/Op Amp
AC CHARACTERISTICS ($A_V = +1$)						
Slew Rate (Note 5)	B	+25°C	275	350	-	V/µs
Full Power Bandwidth (Note 6)	B	+25°C	22	28	-	MHz
Rise Time (Note 7)	B	+25°C	-	6	-	ns
Fall Time (Note 7)	B	+25°C	-	6	-	ns
Propagation Delay (Note 7)	B	+25°C	-	6	-	ns
Overshoot	B	+25°C	-	4.5	-	%
-3dB Bandwidth (Note 8)	B	+25°C	-	125	-	MHz
Settling Time to 1%, 2V Output Step	B	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step	B	+25°C	-	75	-	ns
AC CHARACTERISTICS ($A_V = +2$, $R_F = 681\Omega$)						
Slew Rate (Note 5)	B	+25°C	-	475	-	V/µs
Full Power Bandwidth (Note 6)	B	+25°C	-	26	-	MHz
Rise Time (Note 7)	B	+25°C	-	6	-	ns
Fall Time (Note 7)	B	+25°C	-	6	-	ns
Propagation Delay (Note 7)	B	+25°C	-	6	-	ns
Overshoot	B	+25°C	-	12	-	%

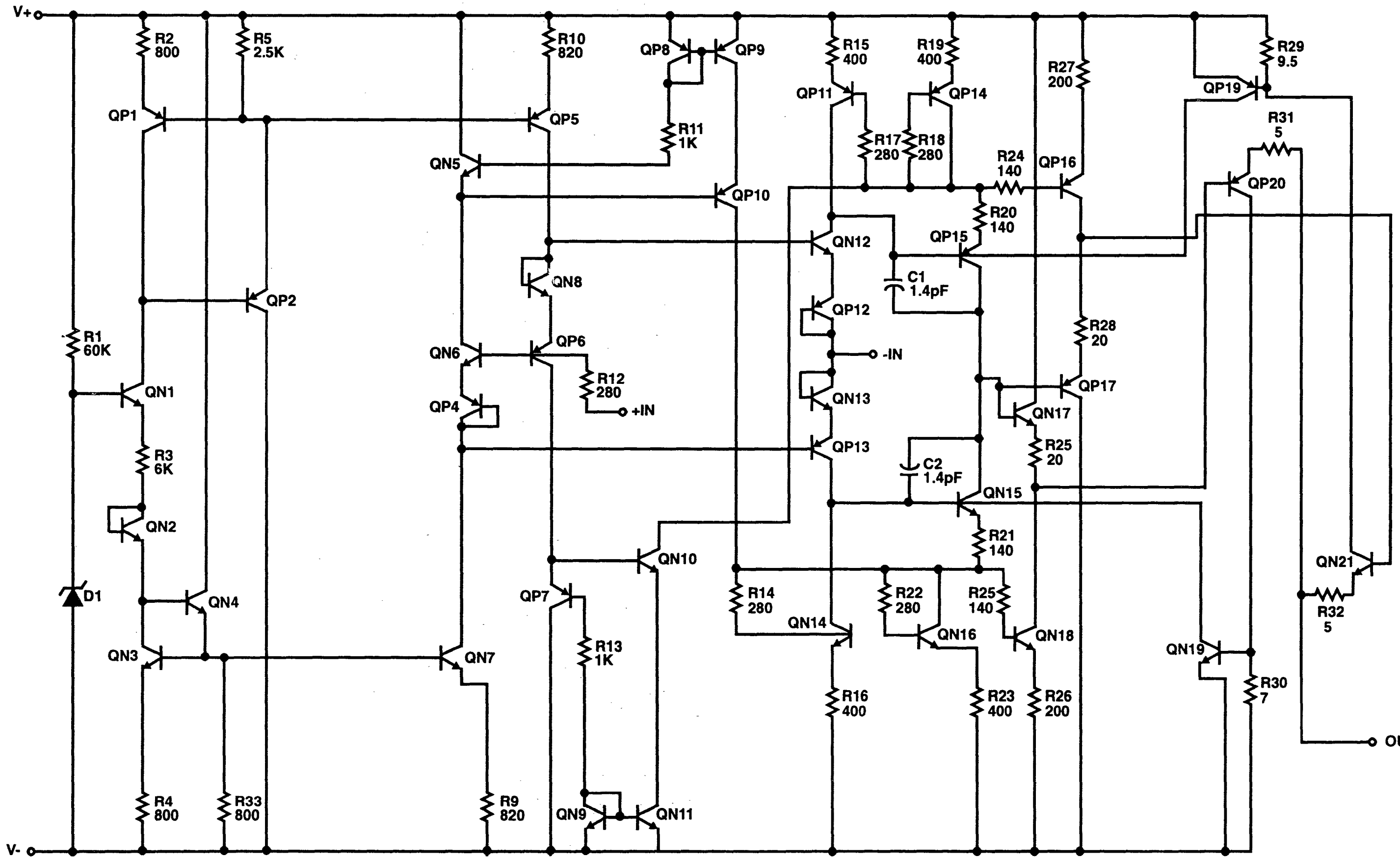
Electrical Specifications $V+ = +5V$, $V- = -5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 16) TEST LEVEL	TEMPERATURE	HA5025I			UNITS
				MIN	TYP	MAX	
-3dB Bandwidth (Note 8)		B	+25°C	-	95	-	MHz
Settling Time to 1%, 2V Output Step		B	+25°C	-	50	-	ns
Settling Time to 0.25%, 2V Output Step		B	+25°C	-	100	-	ns
Gain Flatness	5MHz	B	+25°C	-	0.02	-	dB
	20MHz	B	+25°C	-	0.07	-	dB
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)							
Slew Rate (Note 5)		B	+25°C	350	475	-	V/µs
Full Power Bandwidth (Note 6)		B	+25°C	28	38	-	MHz
Rise Time (Note 7)		B	+25°C	-	8	-	ns
Fall Time (Note 7)		B	+25°C	-	9	-	ns
Propagation Delay (Note 7)		B	+25°C	-	9	-	ns
Overshoot		B	+25°C	-	1.8	-	%
-3dB Bandwidth (Note 8)		B	+25°C	-	65	-	MHz
Settling Time to 1%, 2V Output Step		B	+25°C	-	75	-	ns
Settling Time to 0.1%, 2V Output Step		B	+25°C	-	130	-	ns
VIDEO CHARACTERISTICS							
Differential Gain (Notes 11, 13)		B	+25°C	-	0.03	-	%
Differential Phase (Notes 11, 13)		B	+25°C	-	0.03	-	Degrees

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.
3. $V_{CM} = \pm 2.5V$. At -40°C Product is tested at $V_{CM} = \pm 2.25V$ because Short Test Duration does not allow self heating.
4. $\pm 3.5V \leq V_S \leq \pm 6.5V$
5. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
6. $2\left(FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}};\ V_{PEAK} = 2V\right)$
7. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
8. $R_L = 400\Omega$, $V_{OUT} = 100mV$.
9. A. Production Tested; B. Guaranteed Limit or Typical based on characterization; C. Design Typical for information only.
10. $V_{IN} = \pm 2.5V$, $V_{OUT} = 0V$.
11. Measured with a VM700A video tester using an NTC-7 composite VITS.
12. Maximum power dissipation, including output load, must be designed to maintain junction temperature below +175°C for die, and below +150°C for plastic packages. See Applications Information section for safe operating area information.
13. $R_L = 150\Omega$.
14. $V_{OUT} = \pm 2.5V$. At -40°C Product is tested at $V_{OUT} = \pm 2.25V$ because Short Test Duration does not allow self heating.
15. ESD protection is for human body model tested per MIL-STD-883, Method 3015.7.
16. A. Production Tested; B. Guaranteed limit or Typical based on characterization; C. Design Typical for information only.

Schematic



V+
V-
R1 60K
R2 800
R3 6K
R4 800
R5 2.5K
R9 820
R10 820
R11 1K
R12 280
R13 1K
R14 280
R15 400
R16 400
R17 280
R18 280
R19 400
R20 140
R21 140
R22 280
R23 400
R24 140
R25 20
R25 140
R26 200
R27 200
R28 20
R29 9.5
R30 7
R31 5
R32 5
R33 800
C1 1.4pF
C2 1.4pF
D1
QP1
QP2
QP4
QP5
QP6
QP7
QP8
QP9
QP10
QP11
QP12
QP13
QP14
QP15
QP16
QP17
QP19
QP20
QN1
QN2
QN3
QN4
QN5
QN6
QN7
QN8
QN9
QN10
QN11
QN12
QN13
QN14
QN15
QN16
QN17
QN18
QN19
QN21
+IN
-IN
OUT

Test Circuits

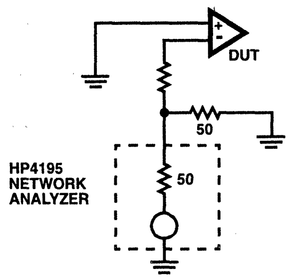


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

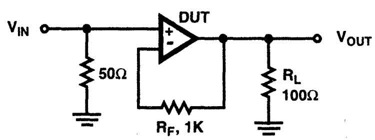


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

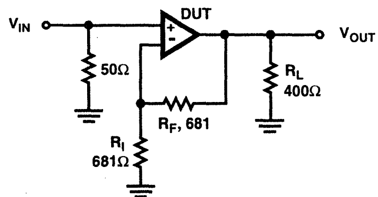


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT

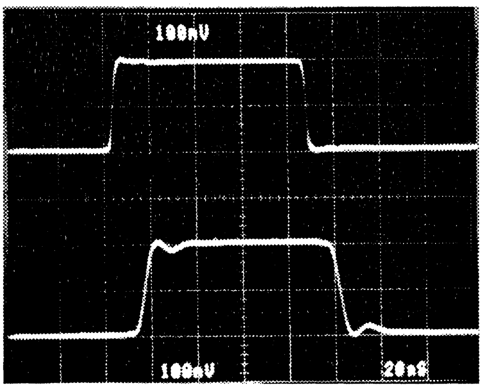


FIGURE 4. SMALL SIGNAL RESPONSE
Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.
Horizontal Scale: 20ns/Div.

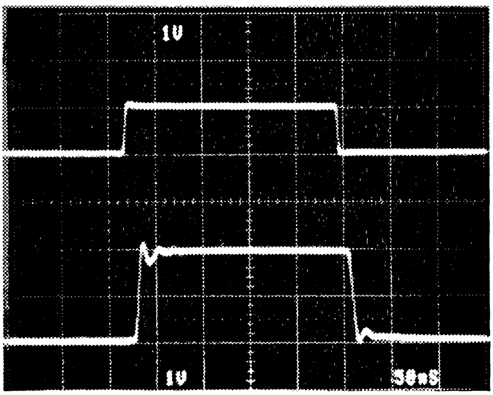


FIGURE 5. LARGE SIGNAL RESPONSE
Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 8 and Figure 9 in the typical performance section, illustrate the performance of the HA5025 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA5025 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10µF) tantalum or electrolytic capacitor in parallel with a small value (0.1µF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

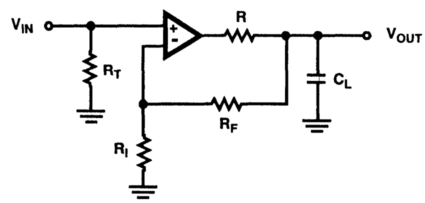


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resistor is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Power Dissipation Considerations

Due to the high supply current inherent in quad amplifiers, care must be taken to insure that the maximum junction temperature (T_J, see Absolute Maximum Ratings) is not exceeded. Figure 7 shows the maximum ambient temperature versus supply voltage for the available package styles (Plastic DIP, SOIC). At $\pm5V_{DC}$ quiescent operation both package styles may be operated over the full industrial range of -40°C to +85°C. It is recommended that thermal calculations, which take into account output power, be performed by the designer.

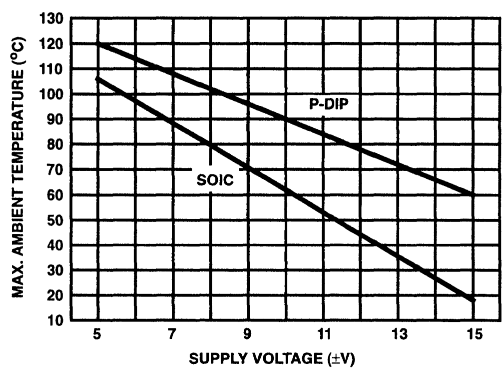


FIGURE 7. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified

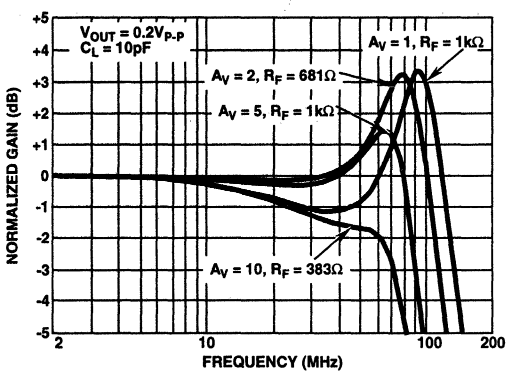


FIGURE 8. NON-INVERTING FREQUENCY RESPONSE

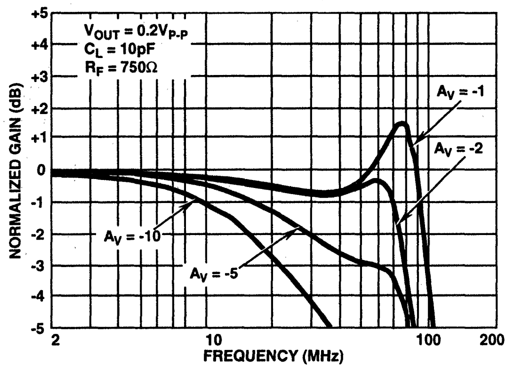


FIGURE 9. INVERTING FREQUENCY RESPONSE

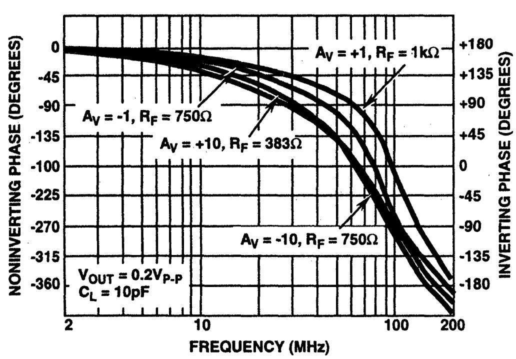


FIGURE 10. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

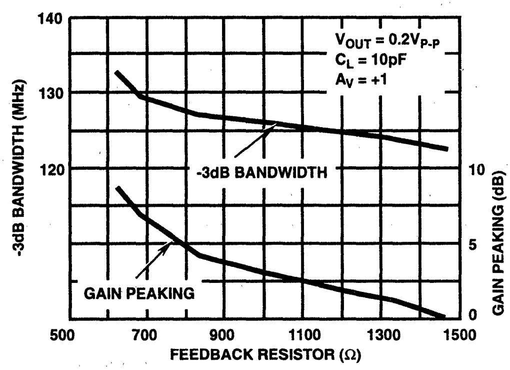


FIGURE 11. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

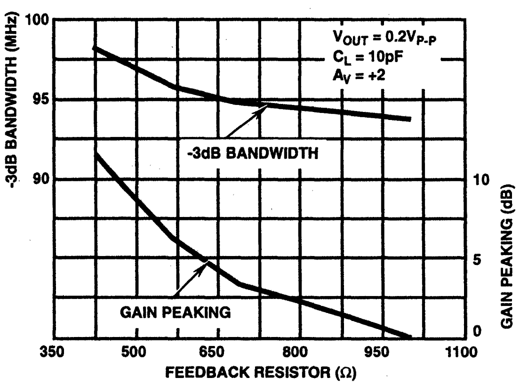


FIGURE 12. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

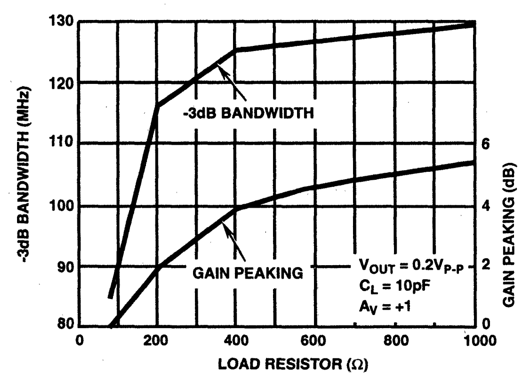


FIGURE 13. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

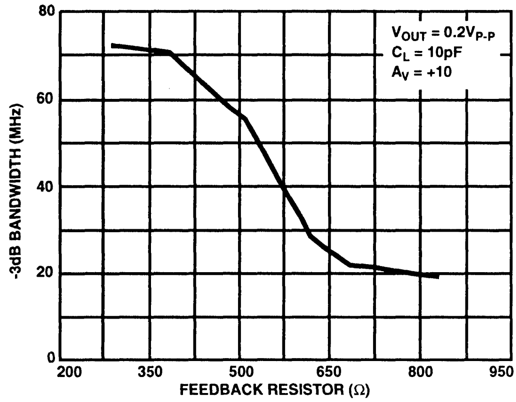


FIGURE 14. BANDWIDTH vs FEEDBACK RESISTANCE

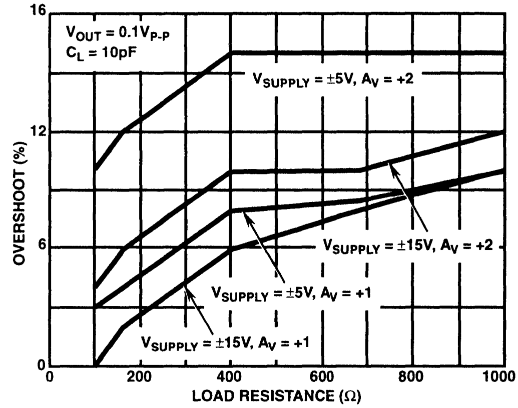


FIGURE 15. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

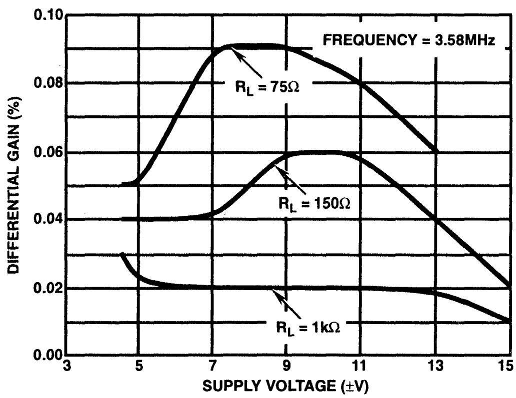


FIGURE 16. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

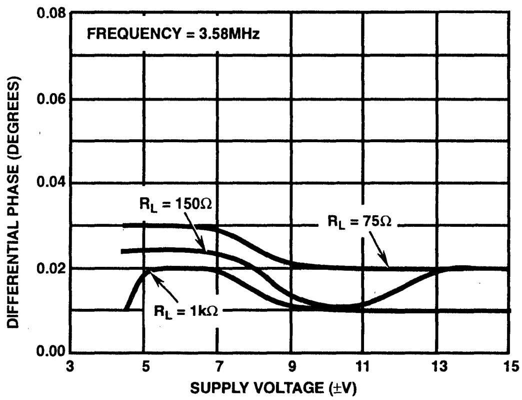


FIGURE 17. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

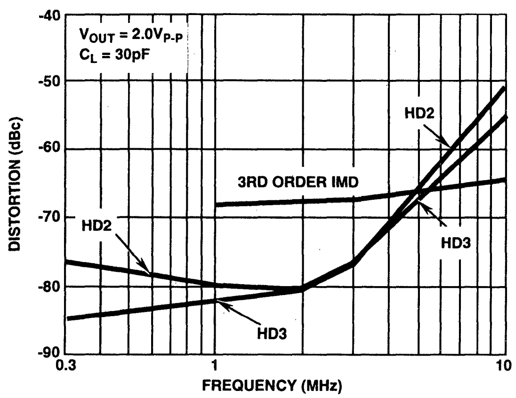


FIGURE 18. DISTORTION vs FREQUENCY

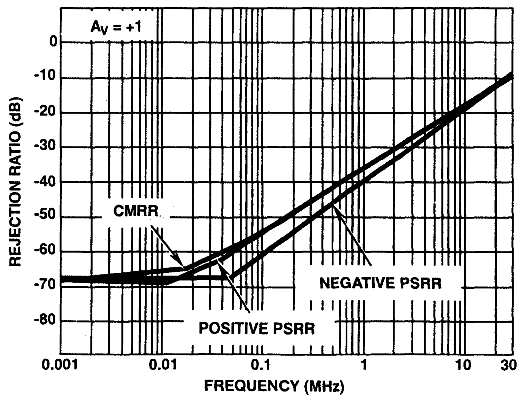


FIGURE 19. REJECTION RATIOS vs FREQUENCY

2

OPERATIONAL AMPLIFIERS

Typical Performance Curves V_{SUPPLY} = ±5V, A_V = +1, R_F = 1kΩ, R_L = 400Ω, T_A = 25°C, Unless Otherwise Specified **(Continued)**

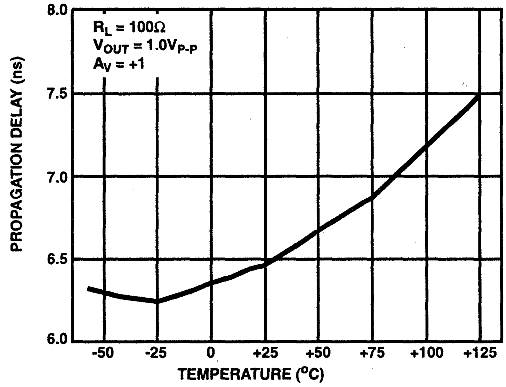


FIGURE 20. PROPAGATION DELAY vs TEMPERATURE

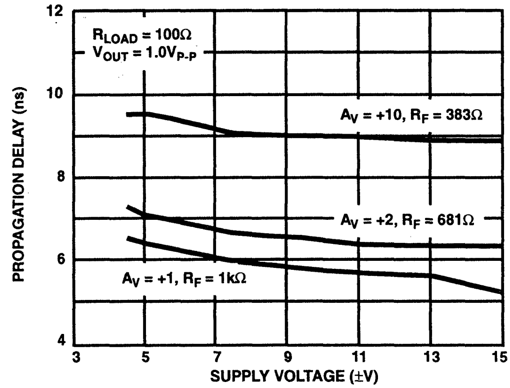


FIGURE 21. PROPAGATION DELAY vs SUPPLY VOLTAGE

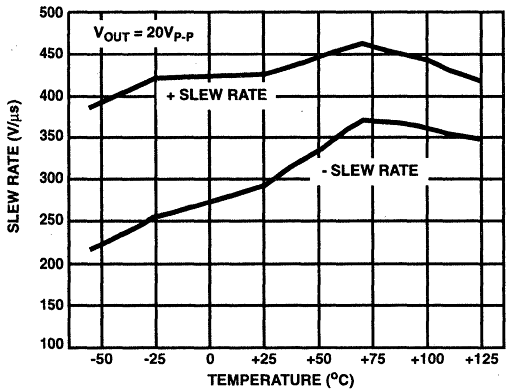


FIGURE 22. SLEW RATE vs TEMPERATURE

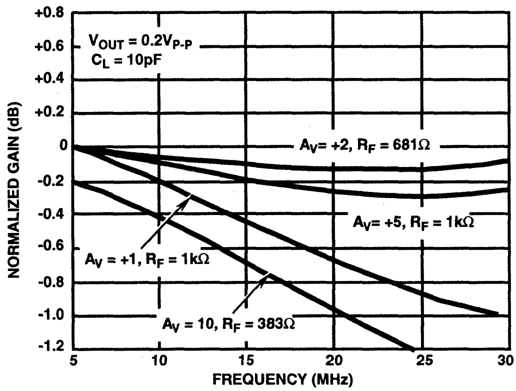


FIGURE 23. NON-INVERTING GAIN FLATNESS vs FREQUENCY

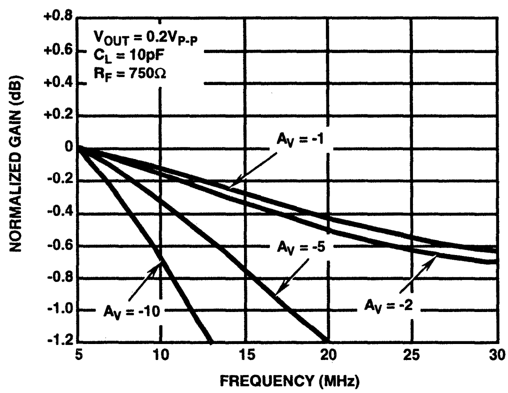


FIGURE 24. INVERTING GAIN FLATNESS vs FREQUENCY

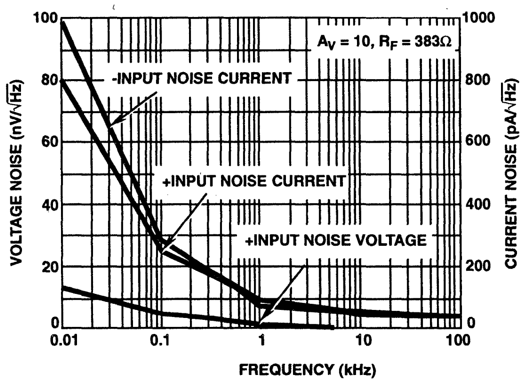


FIGURE 25. INPUT NOISE CHARACTERISTICS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

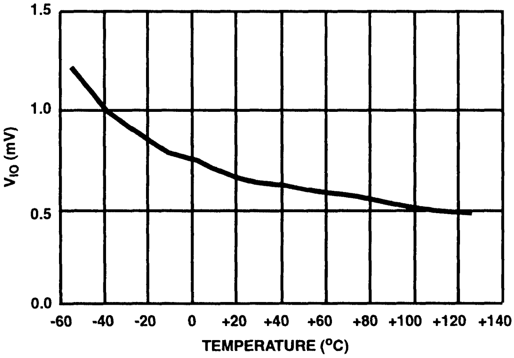


FIGURE 26. INPUT OFFSET VOLTAGE vs TEMPERATURE

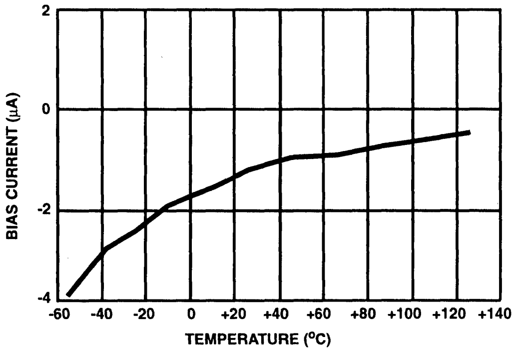


FIGURE 27. +INPUT BIAS CURRENT vs TEMPERATURE

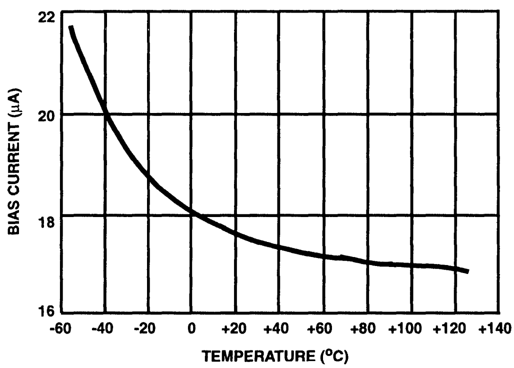


FIGURE 28. -INPUT BIAS CURRENT vs TEMPERATURE

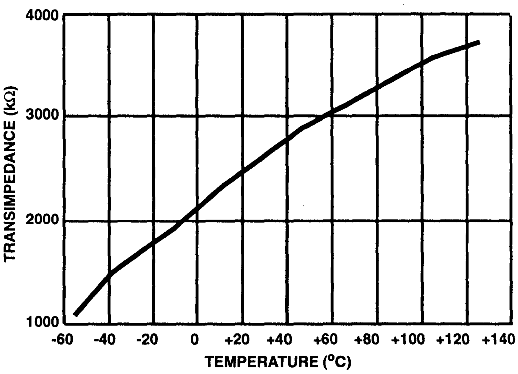


FIGURE 29. TRANSIMPEDANCE vs TEMPERATURE

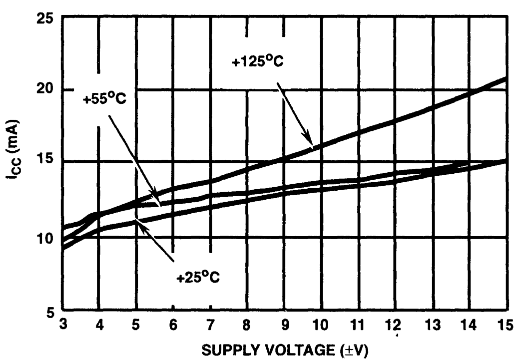


FIGURE 30. SUPPLY CURRENT vs SUPPLY VOLTAGE

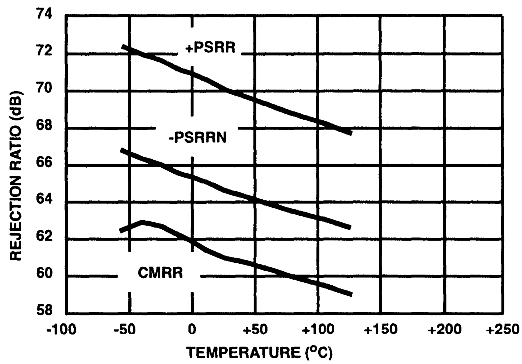


FIGURE 31. REJECTION RATIO vs TEMPERATURE

2 OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

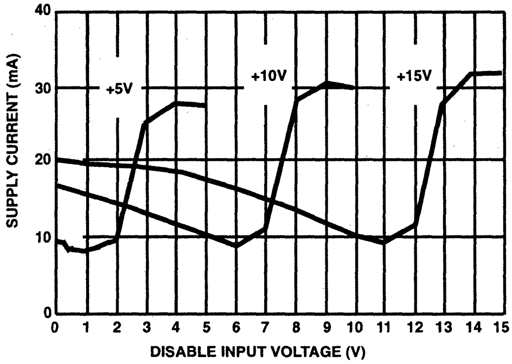


FIGURE 32. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

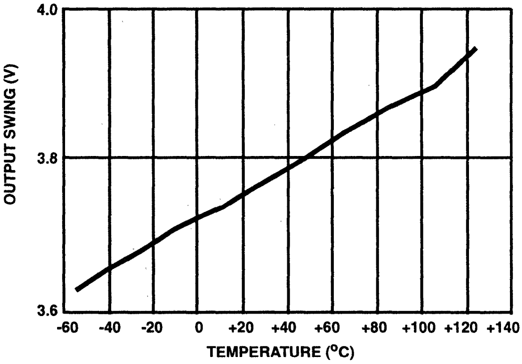


FIGURE 33. OUTPUT SWING vs TEMPERATURE

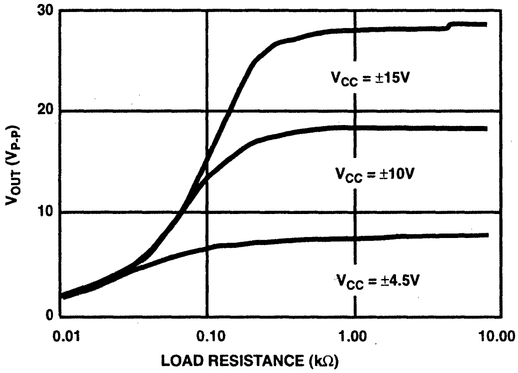


FIGURE 34. OUTPUT SWING vs LOAD RESISTANCE

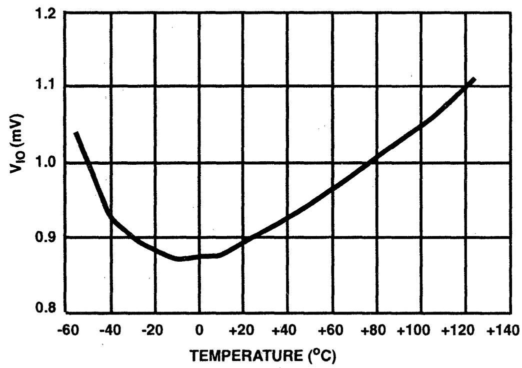


FIGURE 35. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

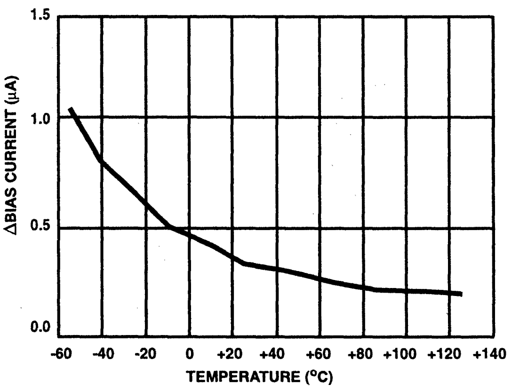


FIGURE 36. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

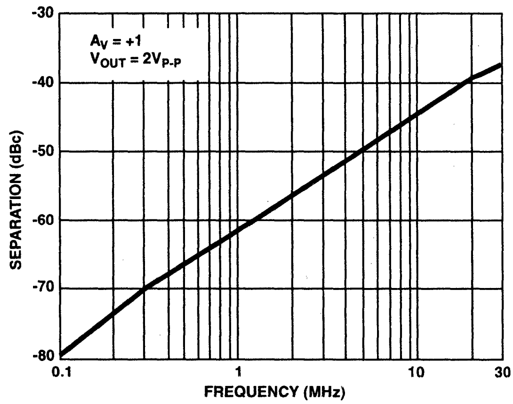


FIGURE 37. CHANNEL SEPARATION vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

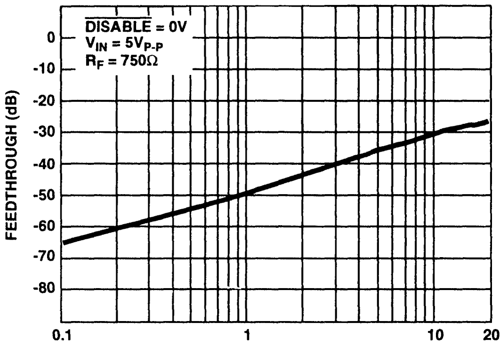


FIGURE 38. DISABLE FEEDTHROUGH vs FREQUENCY

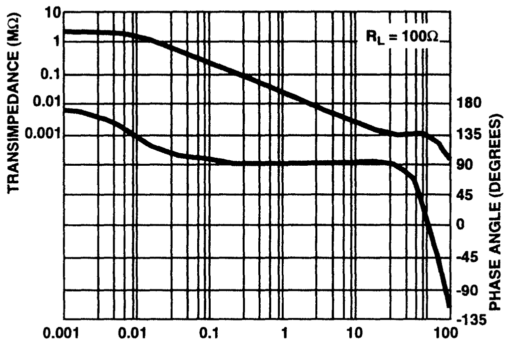


FIGURE 39. TRANSIMPEDANCE vs FREQUENCY

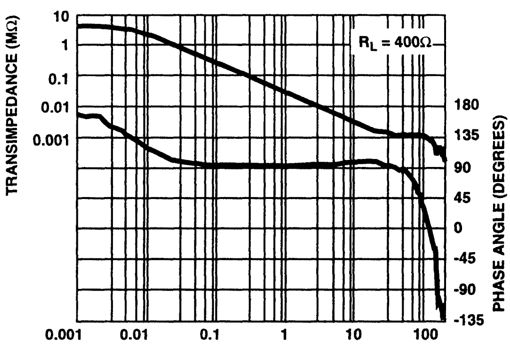


FIGURE 40. TRANSIMPEDANCE vs FREQUENCY

2

OPERATIONAL AMPLIFIERS

Die Characteristics

DIE DIMENSIONS:
2680µm x 2600µm x 483µm ±25.4µm

METALLIZATION:
Type: Metal 1: AlCu (1%), Metal 2: AlCu (1%)
Thickness: Metal 1: 8kÅ ±0.4kÅ, Metal 2: 16kÅ ±0.8kÅ

WORST CASE CURRENT DENSITY:
2.0×10^5 A/cm^2 at 50mA

SUBSTRATE POTENTIAL (POWERED UP): V-

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ±0.4kÅ

TRANSISTOR COUNT: 248

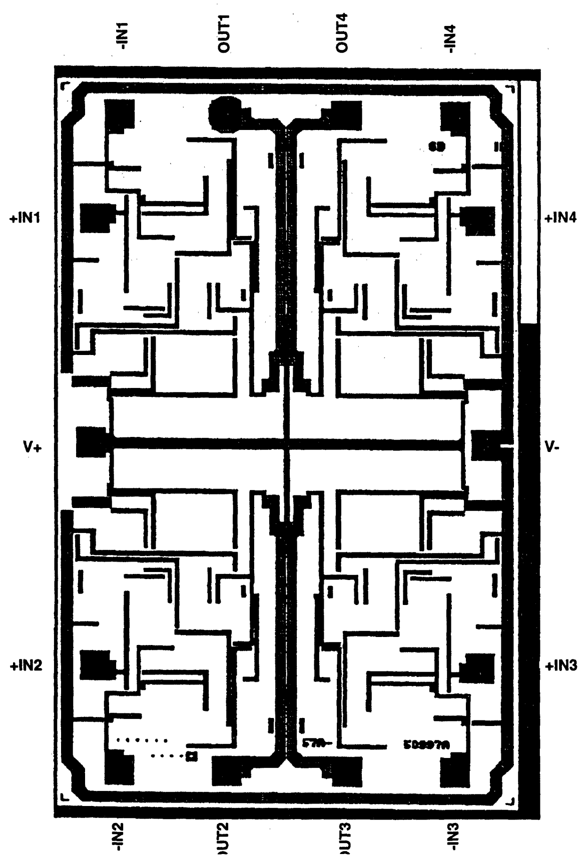
PROCESS: High Frequency Bipolar Dielectric Isolation

DIE ATTACH:

Material: Epoxy - Plastic DIP and SOIC

Metallization Mask Layout

HA5025



HFA1102

Ultra High-Speed Current Feedback Amplifier with Compensation Pin

July 1995

Features

- Compensation Pin for Bandwidth Limiting
- Low Distortion (30MHz) .... -56dBc
- -3dB Bandwidth 600MHz
- Very Fast Slew Rate 2000V/µs
- Fast Settling Time (0.1%) 11ns
- Excellent Gain Flatness
  - (100MHz) .... ±0.05dB
  - (50MHz) .... ±0.02dB
  - (30MHz) .... ±0.01dB
- High Output Current 60mA
- Overdrive Recovery .... <10ns

Applications

- Video Switching and Routing
- Pulse and Video Amplifiers
- Wideband Amplifiers
- RF/IF Signal Processing
- Flash A/D Driver
- Medical Imaging Systems

Description

The HFA1102 is a high speed wideband current feedback amplifier featuring a compensation pin for bandwidth limiting. Built with Harris' proprietary complementary bipolar UHF-1 process, it has excellent AC performance and low distortion.

Because the HFA1102 is already unity gain stable, the primary purpose for limiting the bandwidth is to reduce the total noise (broadband) of the circuit. The bandwidth of the HFA1102 may be limited by connecting a capacitor and series damping resistor from pin 8 to ground. Typical bandwidths for various values of compensation capacitors are shown in the Electrical Specifications section of this datasheet.

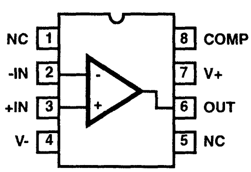
A variety of packages and temperature grades are available. See the ordering information below for details.

Ordering Information

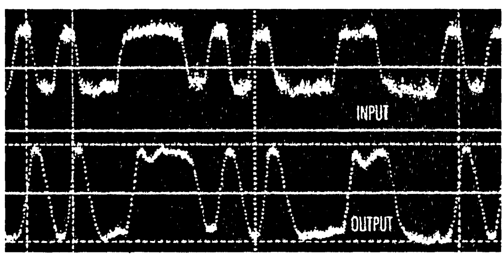
PART NUMBER	OPERATING TEMP RANGE	PRODUCT DESCRIPTION
HFA1102IJ	-40°C to +85°C	8 Lead CerDIP
HFA1102IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1102IB	-40°C to +85°C	8 Lead Plastic SOIC (N)
HFA1102Y	-40°C to +85°C	Die

Pinout

HFA1102
(PDIP, CERDIP, SOIC)
TOP VIEW



The Op Amps with Fastest Edges



INPUT 220MHz SIGNAL

OUTPUT (A_V = 2) HFA1102 OP AMP

0ns 25ns

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage .... V_{SUPPLY}
Differential Input Voltage 5V
Output Current (50% Duty Cycle) 60mA
Junction Temperature (Ceramic and Die) .... +175°C
Junction Temperature (Plastic Package) .... +150°C
Lead Temperature (Soldering 10s) .... +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HFA1102I .... $-40^oC \le T_A \le +85^oC$
Storage Temperature Range .... $-65^oC \le T_A \le +150^oC$

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
CerDIP Package	116	36
Plastic DIP Package	130	N/A
SOIC Package	170	N/A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, C_{COMP} = 0pF, Unless Otherwise Specified

PARAMETER	TEMP	HFA1102I MIN	HFA1102I TYP	HFA1102I MAX	UNITS
INPUT CHARACTERISTICS					
Input Offset Voltage	+25°C	-	2	6	mV
	Full	-	-	10	mV
Input Offset Voltage Drift	Full	-	10	-	µV/°C
V_{IO} CMRR (ΔV_{CM} = ±2V)	+25°C	40	46	-	dB
	Full	38	-	-	dB
V_{IO} PSRR (ΔV_S = ±1.25V)	+25°C	45	50	-	dB
	Full	42	-	-	dB
Non-Inv. Input Bias Current (+IN = 0V)	+25°C	-	25	40	µA
	Full	-	-	65	µA
$+I_{BIAS}$ Drift	Full	-	40	-	nA/°C
$+I_{BIAS}$ CMS (ΔV_{CM} = ±2V)	+25°C	-	20	40	µA/V
	Full	-	-	50	µA/V
Inv. Input Bias Current (-IN = 0V)	+25°C	-	12	50	µA
	Full	-	-	60	µA
$-I_{BIAS}$ Drift	Full	-	40	-	nA/°C
$-I_{BIAS}$ CMS (ΔV_{CM} = ±2V)	+25°C	-	1	7	µA/V
	Full	-	-	10	µA/V
$-I_{BIAS}$ PSS (ΔV_S = ±1.25V)	+25°C	-	6	15	µA/V
	Full	-	-	27	µA/V
Non-Inv. Input Resistance	+25°C	25	50	-	kΩ
Inv. Input Resistance	+25°C	-	16	30	Ω
Input Capacitance (either input)	+25°C	-	2	-	pF
Input Common Mode Range	Full	±2.5	±3.0	-	V
Input Noise Voltage (100kHz)	+25°C	-	4	-	nV/√Hz
+Input Noise Current (100kHz)	+25°C	-	18	-	pA/√Hz
-Input Noise Current (100kHz)	+25°C	-	21	-	pA/√Hz
TRANSFER CHARACTERISTICS A_V = +1, R_F = 150Ω, R_{DAMP} = 120Ω, Unless Otherwise Specified					
Open Loop Transimpedance	+25°C	-	500	-	kΩ

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, C_{COMP} = 0pF, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMP	HFA1102I MIN	TYP	MAX	UNITS
Linear Phase Deviation (DC to 100MHz)		+25°C	-	0.6	-	Degrees
Differential Gain (NTSC, R_L = 75Ω)		+25°C	-	0.03	-	%
Differential Phase (NTSC, R_L = 75Ω)		+25°C	-	0.03	-	Degrees
Minimum Stable Gain		Full	1	-	-	V/V
Bandwidth Limiting Characteristics -3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, A_V = +1)	C_{COMP} = 0pF	+25°C	-	600	-	MHz
	C_{COMP} = 1pF	+25°C	-	350	-	MHz
	C_{COMP} = 3pF	+25°C	-	190	-	MHz
	C_{COMP} = 7pF	+25°C	-	55	-	MHz
Gain Flatness (to 30MHz)	C_{COMP} = 0pF	+25°C	-	±0.01	-	dB
	C_{COMP} = 1pF	+25°C	-	±0.05	-	dB
	C_{COMP} = 3pF	+25°C	-	±0.10	-	dB
Gain Flatness (to 100MHz)		+25°C	-	±0.05	-	dB
Gain Flatness (to 50MHz)		+25°C	-	±0.02	-	dB
OUTPUT CHARACTERISTICS A_V = +2, Unless Otherwise Specified						
Output Voltage (A_V = -1)		+25°C	±3.0	±3.3	-	V
		Full	±2.5	±3.0	-	V
Output Current (R_L = 50Ω, A_V = -1)		+25°C	50	65	-	mA
		Full	40	60	-	mA
DC Closed Loop Output Impedance		+25°C	-	0.1	-	Ω
2nd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P})		+25°C	-	-56	-	dBc
3rd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P})		+25°C	-	-80	-	dBc
3rd Order Intercept (100MHz)		+25°C	-	30	-	dBm
1dB Compression (100MHz)		+25°C	-	20	-	dBm
TRANSIENT RESPONSE A_V = +1, R_F = 150Ω, R_{DAMP} = 120Ω, Unless Otherwise Specified						
Rise Time (V_{OUT} = 2.0V Step)		+25°C	-	600	-	ps
Overshoot (V_{OUT} = 2.0V Step)		+25°C	-	10	-	%
Slew Rate (A_V = +1, V_{OUT} = 5V_{P-P})		+25°C	-	1200	-	V/μs
Slew Rate (A_V = +2, V_{OUT} = 5V_{P-P})		+25°C	-	2000	-	V/μs
0.1% Settling (V_{OUT} = 2V to 0V)		+25°C	-	11	-	ns
0.2% Settling (V_{OUT} = 2V to 0V)		+25°C	-	7	-	ns
POWER SUPPLY CHARACTERISTICS						
Supply Voltage Range		Full	±4.5	-	±5.5	V
Supply Current		+25°C	-	21	26	mA
		Full	-	-	33	mA

Applications Information

Optimum Feedback Resistor (R_F)

All current feedback amplifiers require a feedback resistor, even for unity gain applications. The R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1102 design is optimized for a 150Ω R_F, at a gain of +1. Decreasing R_F in a unity gain application decreases stability, leading to excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a tradeoff of bandwidth vs. stability.

Bandwidth Limiting

The bandwidth of the HFA1102 may be limited by connecting a resistor (R_{DAMP}) and capacitor in series from pin 8 to GND. The series resister is required to damp the interaction between the package parasitics and C_{COMP}. Typical bandwidths for various values of compensation capacitor are shown in the specification tables. Because the HFA1102 is already unity gain stable, the main reason for limiting the bandwidth is to reduce the total noise (broadband) of the circuit. Additionally, compensating the HFA1102 allows the use of a lower value R_F for a given gain. The decreased bandwidth due to C_{COMP} offsets the bandwidth increase from the lower R_F, keeping the amplifier stable. Reducing R_F provides the double benefits of reduced DC errors ($-I_B \times R_F$) and reduced total noise (ini $\times R_F$ and $4KTR_F$).

PC Board Layout

The frequency performance of this amplifier depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value chip (0.1μF) capacitor works well in most cases.

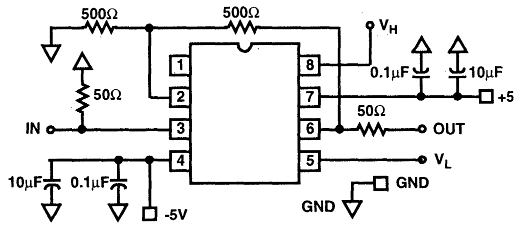
Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

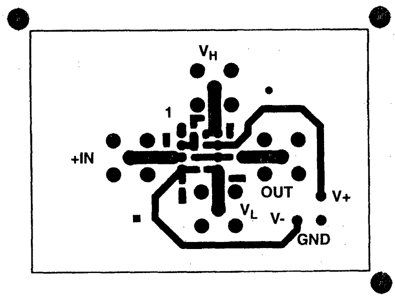
An example of a good high frequency layout is the Evaluation Board shown.

Evaluation Board

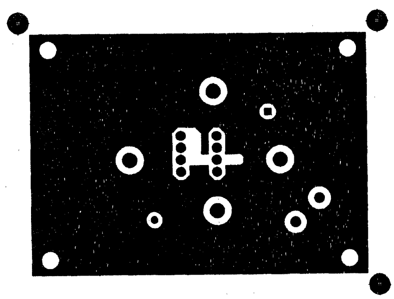
The HFA1102 may be evaluated using the HFA1130 Evaluation Board which is available from your local sales office. R_{DAMP} and C_{COMP} should be connected in series from the socket pin to the GND plane. The trace from pin 8 to the V_H connector should be cut near the socket to remove this parallel capacitance. The layout and schematic of the board are shown below:



TOP LAYOUT



BOTTOM LAYOUT



Die Characteristics

DIE DIMENSIONS:
63 mils x 44 mils x 19 mils ±1mil
1600μm x 1130μm ±25.4μm

METALLIZATION:
Type: Metal 1: AlCu (2%)/TiWType: Metal 2: AlCu (2%)
Thickness: Metal 1: 8kÅ ±0.4kÅThickness: Metal 2: 16kÅ ±0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC

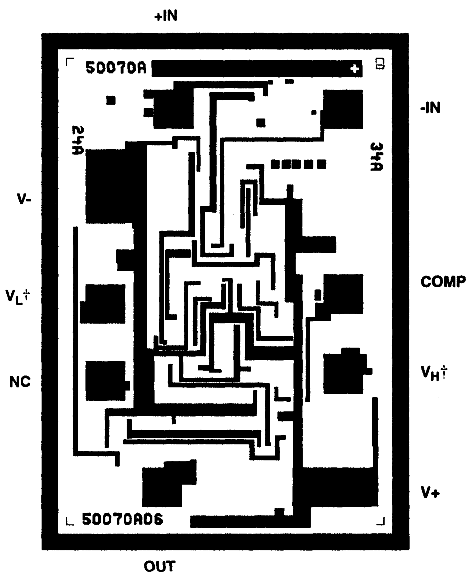
WORST CASE CURRENT DENSITY:
$0.909 \times 10^5 A/cm^2$

TRANSISTOR COUNT: 52

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1102



† Output Clamping Function (V_H, V_L) is available to users of the HFA1102 in die form. Please refer to the HFA1130 data sheet for infomation regarding the operation and use of this function.

HARRIS SEMICONDUCTOR

HFA1103

Video Op Amp with High Speed Sync Stripper

July 1995

Features

- Removes Sync Signal From Component Video
- Low Residual Sync .... 8mV (Typ)
- -3dB Bandwidth 200MHz
- Very Fast Slew Rate 600V/μs
- Fast Settling Time (0.1%) 9ns
- Excellent Gain Flatness, 32MHz .... ±0.1dB
- Overdrive Recovery .... <12ns

Applications

- RGB Video Sync Stripping
- RGB Video Distribution Amplifier for Workstations and PC Networks
- Video Conferencing Systems
- RGB Video Monitor Preamp
- Fiberoptic Receivers
- HDTV

Description

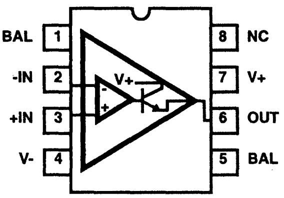
The HFA1103 is a high-speed, wideband, fast settling current feedback op amp with a sync stripping function. The HFA1103 is a basic op amp with a modified output stage that enables it to strip the sync from a component video signal. The output stage has an open emitter NPN transistor that prevents the output from going low during the sync pulse. Removing the sync signal benefits digitizing systems because only the active video information is applied to the A/D converter. This enables the full dynamic range of the A/D converter to be used to process the video signal. The HFA1103 includes inverting input bias current adjust pins (pins 1 and 5) for adjusting the output offset voltage.

Ordering Information

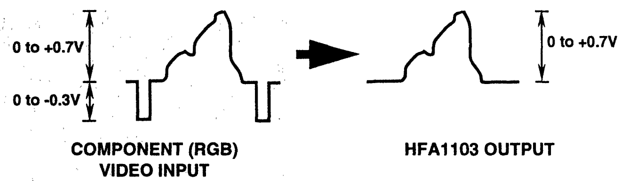
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1103IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1103IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

Pinout

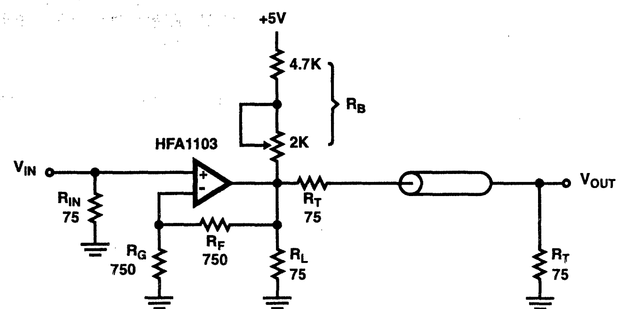
HFA1103
(PDIP, SOIC)
TOP VIEW



Sync Stripper Waveforms



Application Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3957.1

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage . . . . V_{SUPPLY}
Differential Input Voltage 5V
Output Current (50% Duty Cycle) 60mA
Junction Temperature (Plastic Package) . . . . +150°C
Lead Temperature (Soldering 10s) . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Thermal Resistance θ_{JA}
Plastic DIP Package . . . . 130°C/W
SOIC Package . . . . 170°C/W
HFA1103I . . . . $-40°C \le T_A \le +85°C$
Storage Temperature Range . . . . $-65°C \le T_A \le +150°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm 5V$, $A_V = +2$, $R_F = 750\Omega$, $R_L = 50\Omega$, Unless Otherwise Specified

PARAMETER	TEMP	HFA1103I MIN	HFA1103I TYP	HFA1103I MAX	UNITS
DC CHARACTERISTICS					
Residual Sync (V_{IN} = -300mV, A_V = +1, Note 2)	+25°C	-	8	10	mV
	Full	-	-	12	mV
Output Offset Voltage (Notes 3, 5)	+25°C	-	10	30	mV
	Full	-	-	40	mV
Output Offset Voltage Drift (Note 3)	Full	-	10	-	µV/°C
V_{OS} PSRR ($\Delta V_S = \pm 1.25V$)	+25°C	39	45	-	dB
	Full	35	-	-	dB
Non-Inverting Input Bias Current (+IN = 0V)	+25°C	-	5	40	µA
	Full	-	-	65	µA
Inverting Input Bias Current (-IN = 0V)	+25°C	-	5	50	µA
	Full	-	-	60	µA
$-I_{BIAS}$ Adjust Range (Notes 1, 4)	+25°C	100	200	-	µA
Non-Inverting Input Resistance	+25°C	25	50	-	kΩ
Inverting Input Resistance	+25°C	-	16	30	Ω
Input Capacitance (Either Input)	+25°C	-	2	-	pF
Input Common Mode Range	Full	±2.5	±3.0	-	V
Input Noise Voltage (100kHz)	+25°C	-	4	-	$nV/\sqrt{Hz}$
+Input Noise Current (100kHz)	+25°C	-	18	-	$pA/\sqrt{Hz}$
-Input Noise Current (100kHz)	+25°C	-	21	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS A_V = +2, Unless Otherwise Specified					
Open Loop Transimpedance	+25°C	-	500	-	kΩ
-3dB Bandwidth ($V_{OUT} = 1.0V_{P-P}$, A_V = +2)	+25°C	-	200	-	MHz
Gain Flatness (To ±0.1dB)	+25°C	-	32	-	MHz
Minimum Stable Gain	Full	1	-	-	V/V

Electrical Specifications $V_{SUPPLY} = \pm 5V$, $A_V = +2$, $R_F = 750\Omega$, $R_L = 50\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMP	HFA1103I MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS $A_V = +2$, Unless Otherwise Specified					
Output Voltage	+25°C, +85°C	2.5	3.0	-	V
	-40°C	1.75	2.5	-	V
Output Current	+25°C, +85°C	50	60	-	mA
	-40°C	35	50	-	mA
Linearity Near Zero	+25°C	-	0.01	-	%
TRANSIENT RESPONSE $A_V = +2$, Unless Otherwise Specified					
Rise Time (V_{OUT} = 2.0V Step)	+25°C	-	2	-	ns
Overshoot (V_{OUT} = 2.0V Step)	+25°C	-	10	-	%
Slew Rate (A_V = +2, V_{OUT} = 0 to 2V, +2V to 0)	+25°C	-	600	-	V/µs
0.1% Settling (V_{OUT} = 2V to 0V)	+25°C	-	9	-	ns
Overdrive Recovery Time (2X Overdrive)	+25°C	-	12	-	ns
POWER SUPPLY CHARACTERISTICS					
Supply Voltage Range	Full	±4.5	-	±5.5	V
Supply Current (No Load)	+25°C	-	11	16	mA
	Full	-	-	23	mA

NOTES:

1. This is the minimum change in inverting input bias current when a BAL pin is connected to V- through a 50Ω resistor.
2. The residual sync is specified at the output of a doubly terminated circuit (see page 1 of this data sheet).
3. Since the HFA1103 has an open emitter NPN output stage, this measurement is only valid for positive values.
4. The $-I_{BIAS}$ current can be used to adjust the offset voltage to zero, but $-I_{BIAS}$ does not flow bidirectionally because the HFA1103 output stage is an open emitter NPN transistor.
5. V_{OS} includes the error contribution of I_{BSN} at $R_F = 750\Omega$.

Test Circuit

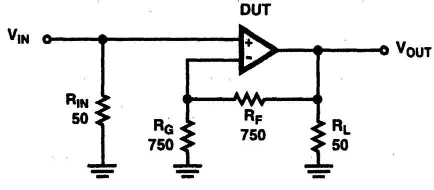


FIGURE 1. TEST CIRCUIT

Application Information

Offset Adjustment

The HFA1103 allows for adjustment of the inverting input bias current to null the output offset voltage. $-I_{BIAS}$ flows through R_F, so any change in bias current forces a corresponding change in output voltage. The amount of adjustment is a function of R_F. With $R_F = 750\Omega$, the typical adjust range is 150mV. For offset adjustment connect a 10kΩ potentiometer between pins 1 and 5 with the wiper connected to V-.

PC Board Layout

The frequency performance of these amplifiers depends a great deal on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance, such as that resulting from an improperly terminated transmission line will degrade the frequency response of the amplifier and may cause oscillations. In most cases, the oscillation can be avoided by placing a resistor in series with the output.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to pin 2, and connections to pin 2 should be kept as short as possible.

An example of a good high frequency layout is the Evaluation Board shown.

Evaluation Board

The HFA1100 series evaluation board may be used for the HFA1103 with minor modifications. The evaluation board may be ordered using part number HFA11XXEVAL. Please note that an HFA1103 sample is not included with the evaluation board and must be ordered separately.

The layout and schematic of the board are shown below:

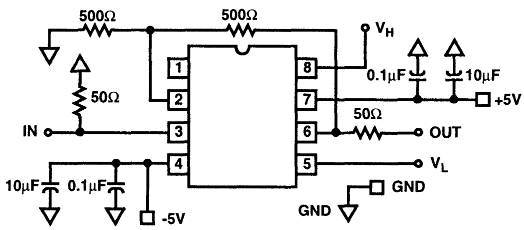
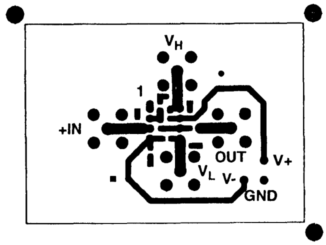


FIGURE 2. EVALUATION BOARD SCHEMATIC

TOP LAYOUT



BOTTOM LAYOUT

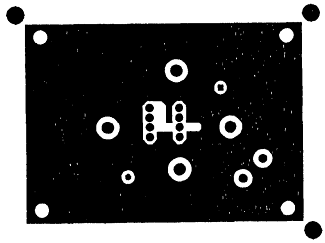


FIGURE 3. EVALUATION BOARD ARTWORK

Applications Circuits

A circuit which performs the sync stripper and DC restore functions is shown on the next page in Figure 4. Please reference Harris Application Note AN9514, titled "Video Amplifier with Sync Stripper and DC Restore", for details on this circuit.

The standard output of a VM700 video measurement set is shown in Figure 5. The output, after passing through the Applications Schematic shown on the first page of this data sheet, is shown in Figure 6.

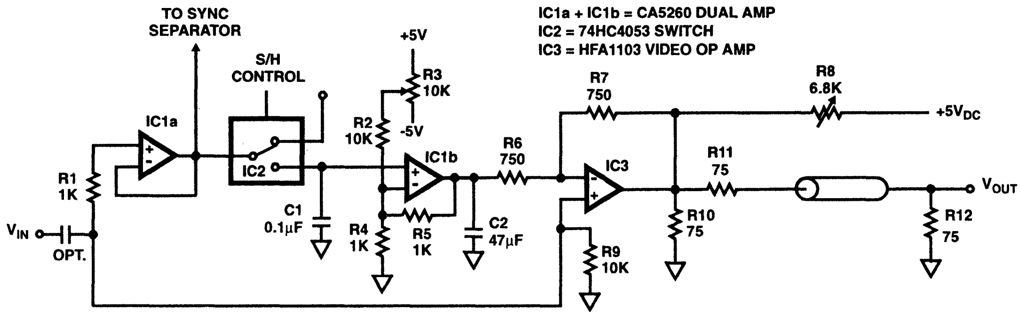


FIGURE 4. VIDEO AMPLIFIER WITH SYNC STRIPPER AND DC RESTORE

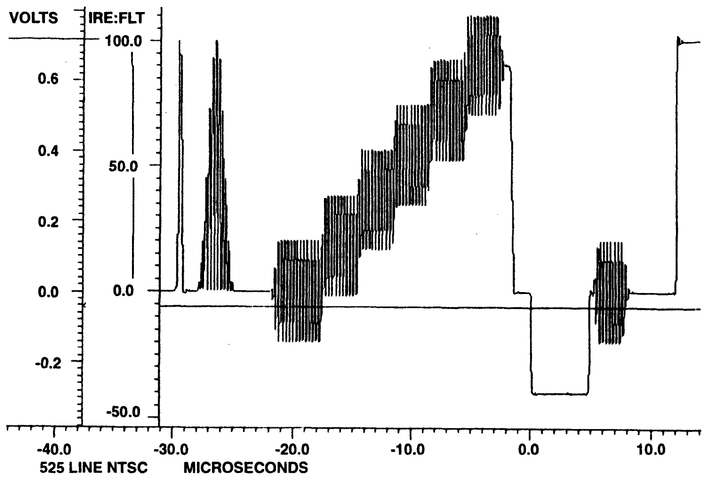


FIGURE 5. OUTPUT OF VM700 VIDEO MEASUREMENT SET

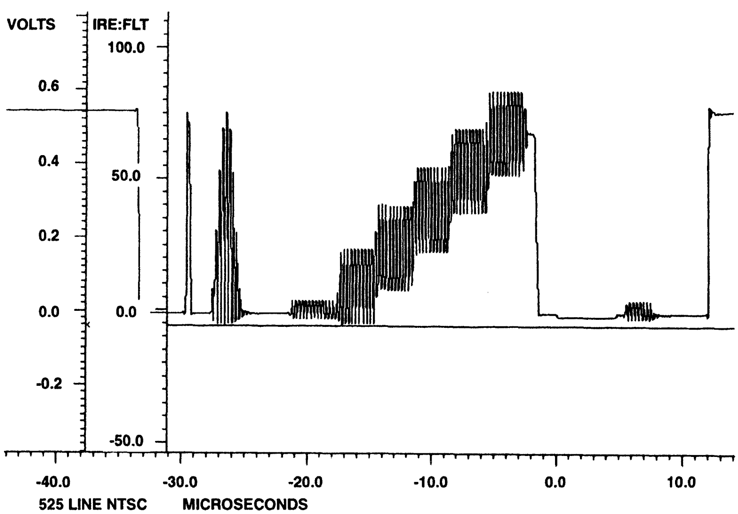


FIGURE 6. OUTPUT OF HFA1103 SYNC STRIPPER CONFIGURED AS ON THE FIRST PAGE OF THIS DATA SHEET

Metallization Topology

DIE DIMENSIONS:

63 mils x 44 mils x 19 mils ±1 mil
1600μm x 1130μm ±25.4μm

METALLIZATION:

Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu (2%)
Thickness: 16kÅ ±0.8kÅ

GLASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.5kÅ

WORST CASE CURRENT DENSITY:

2.12×10^5 A/cm^2 at 50mA

TRANSISTOR COUNT: 50

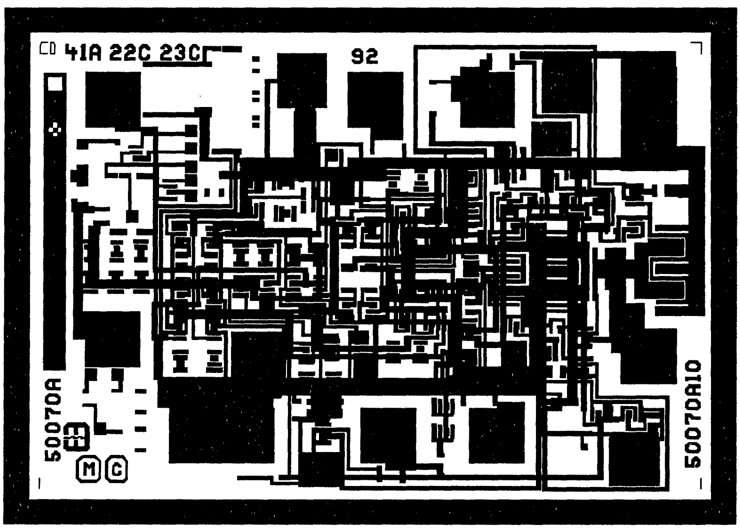
SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1103

BAL NC

-IN V+



+IN OUT

V- NC BAL

HARRIS SEMICONDUCTOR

HFA1105

High-Speed, Low Power, Current Feedback Video Operational Amplifier

July 1995

Features

- Low Supply Current 5.8mA
- High Input Impedance 1MΩ
- Wide -3dB Bandwidth 330MHz
- Very Fast Slew Rate 1000V/μs
- Gain Flatness (to 75MHz) 0.1dB
- Differential Gain 0.02%
- Differential Phase . . . . 0.03 Degrees
- Pin Compatible Upgrade for CLC406

Applications

- Flash A/D Drivers
- Video Switching and Routing
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications

Description

The HFA1105 is a high speed, low power current feedback amplifier built with Harris' proprietary complementary bipolar UHF-1 process.

This amplifier features an excellent combination of low power dissipation (58mW) and high performance. The slew rate, bandwidth, and low output impedance (0.08Ω) make this amplifier a good choice for driving Flash ADCs. Component and composite video systems also benefit from this op amp's excellent gain flatness, and good differential gain and phase specifications. The HFA1105 is ideal for interfacing to Harris' line of video crosspoint switches (HA4201, HA4600, HA4314, HA4404, HA4344), to create high performance, low power switchers and routers.

The HFA1105 is a low power, high performance upgrade for the CLC406. For a comparable amplifier with output disable or output limiting functions, please see the data sheets for the HFA1145 and HFA1135 respectively.

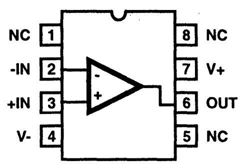
For Military grade product, please refer to the HFA1145/883 data sheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1105IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1105IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

Pinout

HFA1105
(PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage .... V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 2) .... Short Circuit Protected
.... 30mA Continuous
.... 60mA ≤ 50% Duty Cycle
Junction Temperature (Die Only) .... +175°C
Junction Temperature (Plastic Package) .... +150°C
ESD Rating .... >2000V
Lead Temperature (Soldering, 10s) .... +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range .... $-40^oC \le T_A \le +85^oC$
Storage Temperature Range .... $-65^oC \le T_A \le +150^oC$
Thermal Package Characteristics (°C/W) θ_{JA}
Plastic DIP Package 130
SOIC Package 170

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER		(NOTE 1) TEST LEVEL	TEMPERATURE	ALL GRADES MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	+25°C	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	+25°C	47	50	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	45	48	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	45	48	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	+25°C	50	54	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	+85°C	47	50	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40°C	47	50	-	dB
Non-Inverting Input Bias Current		A	+25°C	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	+25°C	-	0.5	1	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	+85°C	-	0.8	3	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40°C	-	0.8	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	+25°C	0.8	1.2	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	0.5	0.8	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	0.5	0.8	-	MΩ
Inverting Input Bias Current		A	+25°C	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/°C
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm1.8V$	A	+25°C	-	3	6	µA/V
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	-	4	8	µA/V
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	-	4	8	µA/V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 1) TEST LEVEL	TEMPERATURE	ALL GRADES MIN	TYP	MAX	UNITS
Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	+25°C	-	2	5	µA/V
	ΔV_{PS} = ±1.8V	A	+85°C	-	4	8	µA/V
	ΔV_{PS} = ±1.2V	A	-40°C	-	4	8	µA/V
Inverting Input Resistance		C	+25°C	-	60	-	Ω
Input Capacitance (either input)		C	+25°C	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	+25°C, +85°C	±1.8	±2.4	-	V
		A	-40°C	±1.2	±1.7	-	V
Input Noise Voltage Density (f = 100kHz)		B	+25°C	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density (f = 100kHz)		B	+25°C	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density (f = 100kHz)		B	+25°C	-	20	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain (A_V = -1)		C	+25°C	-	500	-	kΩ
AC CHARACTERISTICS R_F = 510Ω, Unless Otherwise Specified							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Note 5)	A_V = +1, $+R_S$ = 510Ω	B	+25°C	-	270	-	MHz
		B	Full	-	240	-	MHz
	A_V = -1, R_F = 425Ω	B	+25°C	-	300	-	MHz
	A_V = +2	B	+25°C	-	330	-	MHz
		B	Full	-	260	-	MHz
	A_V = +10, R_F = 180Ω	B	+25°C	-	130	-	MHz
		B	Full	-	90	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2/-1, 4V_{P-P} at A_V = +1, Note 5)	A_V = +1, $+R_S$ = 510Ω	B	+25°C	-	135	-	MHz
	A_V = -1	B	+25°C	-	140	-	MHz
	A_V = +2	B	+25°C	-	115	-	MHz
Gain Flatness (A_V = +2, V_{OUT} = 0.2V_{P-P}, Note 5)	to 25MHz	B	+25°C	-	±0.03	-	dB
		B	Full	-	±0.04	-	dB
	to 75MHz	B	+25°C	-	±0.11	-	dB
		B	Full	-	±0.22	-	dB
Gain Flatness (A_V = +1, $+R_S$ = 510Ω, V_{OUT} = 0.2V_{P-P}, Note 5)	to 25MHz	B	+25°C	-	±0.03	-	dB
	to 75MHz	B	+25°C	-	±0.09	-	dB
Minimum Stable gain		A	Full	-	1	-	V/V
OUTPUT CHARACTERISTICS A_V = +2, R_F = 510Ω Unless Otherwise Specified							
Output Voltage Swing (A_V = -1, R_L = 100Ω, Note 5)		A	+25°C	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 1) TEST LEVEL	TEMPERATURE	ALL GRADES MIN	TYP	MAX	UNITS
Output Current ($A_V = -1$, $R_L = 50\Omega$, Note 5)		A	+25°C, +85°C	50	60	-	mA
		A	-40°C	28	42	-	mA
Output Short Circuit Current		B	+25°C	-	90	-	mA
DC Closed Loop Output Impedance (Note 5)		B	+25°C	-	0.08	-	Ω
Second Harmonic Distortion ($V_{OUT} = 2V_{P-P}$, Note 5)	10MHz	B	+25°C	-	-48	-	dBc
	20MHz	B	+25°C	-	-44	-	dBc
Third Harmonic Distortion ($V_{OUT} = 2V_{P-P}$, Note 5)	10MHz	B	+25°C	-	-50	-	dBc
	20MHz	B	+25°C	-	-45	-	dBc
Reverse Isolation (30MHz, Note 5)		B	+25°C	-	-55	-	dB
TRANSIENT CHARACTERISTICS $A_V = +2$, $R_F = 510\Omega$, Unless Otherwise Specified							
Rise and Fall Times ($V_{OUT} = 0.5V_{P-P}$)		B	+25°C	-	1.1	-	ns
		B	Full	-	1.4	-	ns
Overshoot (Note 3) (V_{OUT} = 0 to 0.5V, V_{IN} t_{RISE} = 1ns)	+OS	B	+25°C	-	3	-	%
	-OS	B	+25°C	-	5	-	%
Overshoot (Note 3) ($V_{OUT} = 0.5V_{P-P}$, V_{IN} t_{RISE} = 1ns)	+OS	B	+25°C	-	3	-	%
	-OS	B	+25°C	-	11	-	%
Slew Rate ($V_{OUT} = 4V_{P-P}$, $A_V = +1$, $+R_S = 510\Omega$)	+SR	B	+25°C	-	1000	-	V/µs
		B	Full	-	975	-	V/µs
	-SR (Note 4)	B	+25°C	-	650	-	V/µs
		B	Full	-	580	-	V/µs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = +2$)	+SR	B	+25°C	-	1400	-	V/µs
		B	Full	-	1200	-	V/µs
	-SR (Note 4)	B	+25°C	-	800	-	V/µs
		B	Full	-	700	-	V/µs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = -1$)	+SR	B	+25°C	-	2100	-	V/µs
		B	Full	-	1900	-	V/µs
	-SR (Note 4)	B	+25°C	-	1000	-	V/µs
		B	Full	-	900	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step, Note 5)	To 0.1%	B	+25°C	-	15	-	ns
	To 0.05%	B	+25°C	-	23	-	ns
	To 0.02%	B	+25°C	-	30	-	ns
Overdrive Recovery Time ($V_{IN} = \pm2V$)		B	+25°C	-	8.5	-	ns
VIDEO CHARACTERISTICS $A_V = +2$, $R_F = 510\Omega$, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	$R_L = 150\Omega$	B	+25°C	-	0.02	-	%
	$R_L = 75\Omega$	B	+25°C	-	0.03	-	%

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 1) TEST LEVEL	TEMPERATURE	ALL GRADES MIN	TYP	MAX	UNITS
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	+25°C	-	0.03	-	Degrees
	R_L = 75Ω	B	+25°C	-	0.05	-	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	+25°C	±4.5	-	±5.5	V
Power Supply Current		A	+25°C	-	5.8	6.1	mA
		A	Full	-	5.9	6.3	mA

NOTE:

1. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.
3. Undershoot dominates for output signal swings below GND (e.g. $0.5V_{P-P}$), yielding a higher overshoot limit compared to the V_{OUT} = 0 to 0.5V condition. See the "Application Information" section for details.
4. Slew rates are asymmetrical if the output swings below GND (e.g. a bipolar signal). Positive unipolar output signals have symmetric positive and negative slew rates comparable to the +SR specification. See the "Application Information" section, and the pulse response graphs for details.
5. See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1105 design is optimized for R_F = 510Ω at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains, however, the amplifier is more stable so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For a gain of +1, a resistor (+R_S) in series with +IN is required to reduce gain peaking and increase stability.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	425	300
+1	510 (+R_S = 510Ω)	270
+2	510	330
+5	200	300
+10	180	130

Non-inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

Pulse Undershoot and Asymmetrical Slew Rates

The HFA1105 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (See Figures 5, 8, and 11). This undershoot isn't present for small bipolar signals, or large positive signals. Another artifact of the composite device is asymmetrical slew rates for output signals with a negative voltage component. The slew rate degrades as the output signal crosses through 0V (See Figures 5, 8, and 11), resulting in a slower overall negative slew rate. Positive only signals have symmetrical slew rates as illustrated in the large signal positive pulse response graphs (See Figures 4, 7, and 10).

PC Board Layout

The amplifier's frequency response depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the device's input and output connections. Capacitance, parasitic or planned, connected to the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground at the amplifier's inverting input (-IN), as this capacitance causes gain peaking, pulse overshoot, and if large enough, instability. To reduce this capacitance, the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 270MHz (for $A_V = +1$). By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, the bandwidth decreases as the load capacitance increases. For example, at $A_V = +1$, $R_S = 62\Omega$, $C_L = 40pF$, the overall bandwidth is limited to 180MHz, and bandwidth drops to 75MHz at $A_V = +1$, $R_S = 8\Omega$, $C_L = 400pF$.

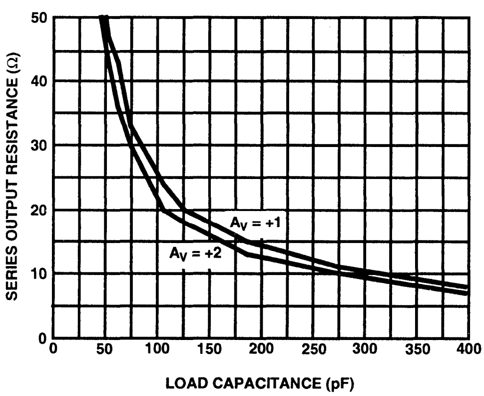


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1105 may be evaluated using the HFA11XX Evaluation Board.

The layout and schematic of the board are shown in Figure 2. To order evaluation boards (part number HFA11XXEVAL), please contact your local sales office.

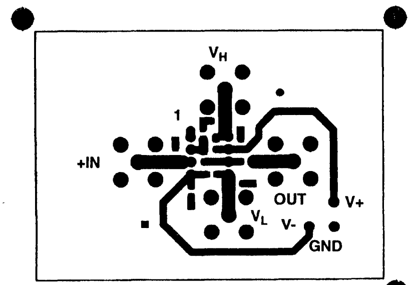


FIGURE 2A. TOP LAYOUT

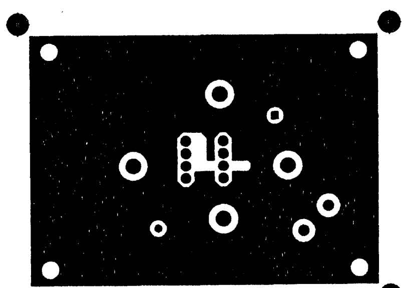


FIGURE 2B. BOTTOM LAYOUT

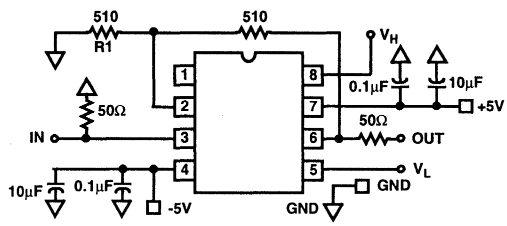


FIGURE 2C. SCHEMATIC

FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Die Characteristics

DIE DIMENSIONS:
59 x 59 x 19 ± 1mils
1500μm x 1500μm x 483μm ± 25.4μm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

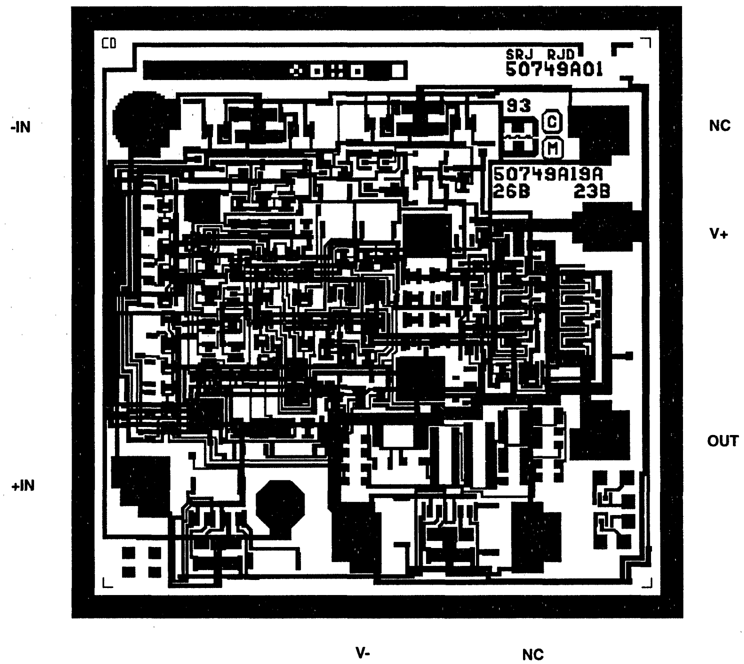
GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

TRANSISTOR COUNT: 75

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1105



Typical Performance Curves V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified

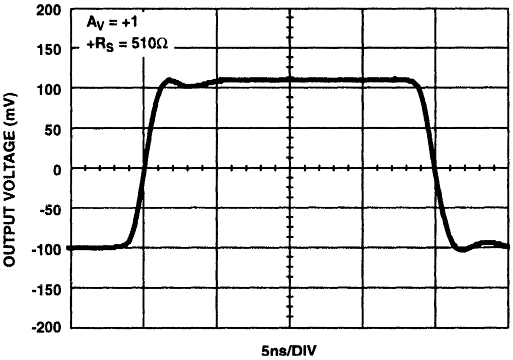


FIGURE 3. SMALL SIGNAL PULSE RESPONSE

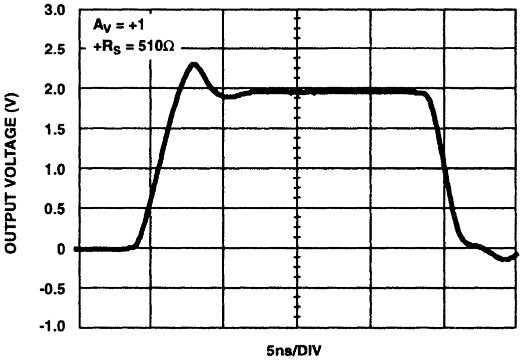


FIGURE 4. LARGE SIGNAL POSITIVE PULSE RESPONSE

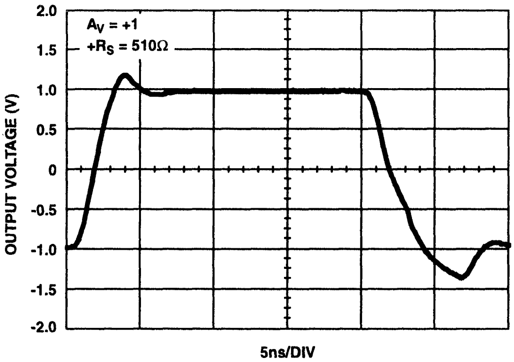


FIGURE 5. LARGE SIGNAL BIPOLAR PULSE RESPONSE

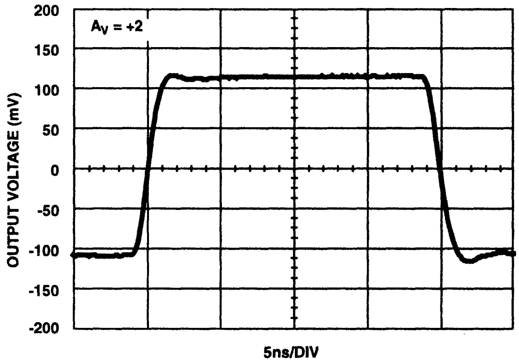


FIGURE 6. SMALL SIGNAL PULSE RESPONSE

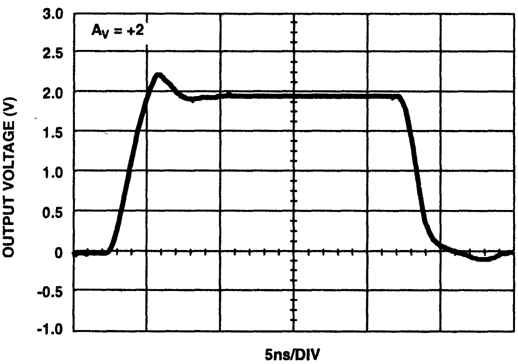


FIGURE 7. LARGE SIGNAL POSITIVE PULSE RESPONSE

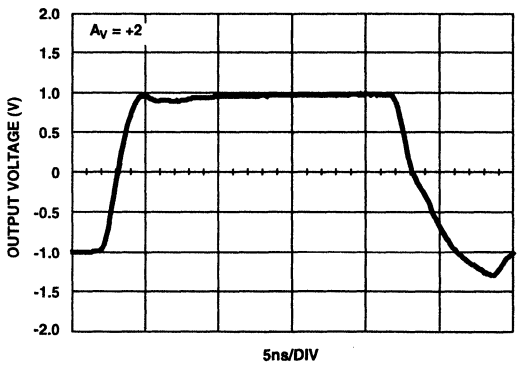


FIGURE 8. LARGE SIGNAL BIPOLAR PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

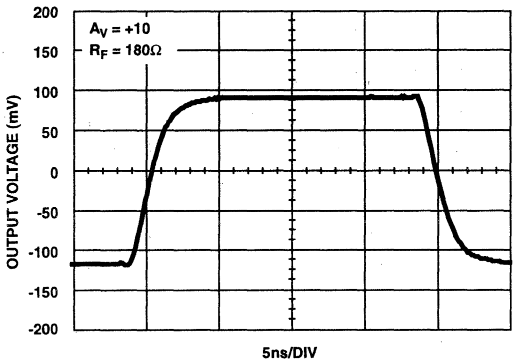


FIGURE 9. SMALL SIGNAL PULSE RESPONSE

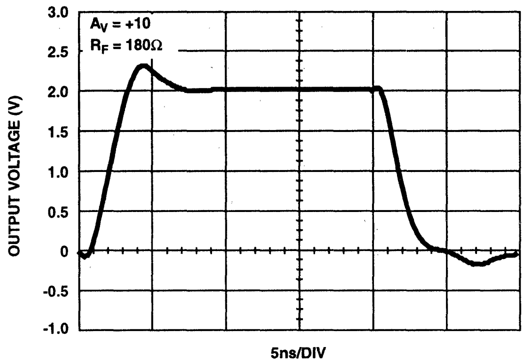


FIGURE 10. LARGE SIGNAL POSITIVE PULSE RESPONSE

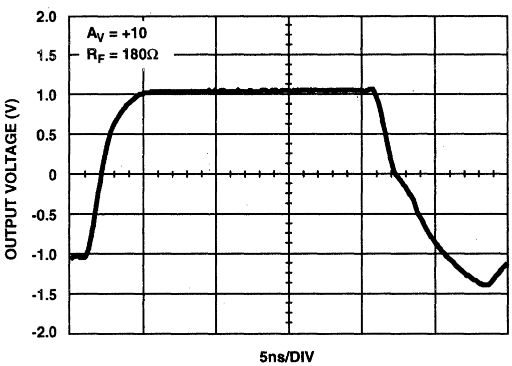


FIGURE 11. LARGE SIGNAL BIPOLAR PULSE RESPONSE

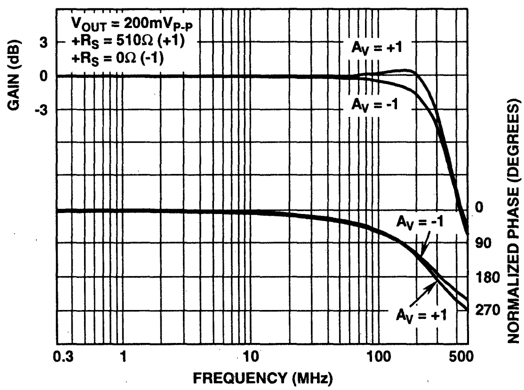


FIGURE 12. FREQUENCY RESPONSE

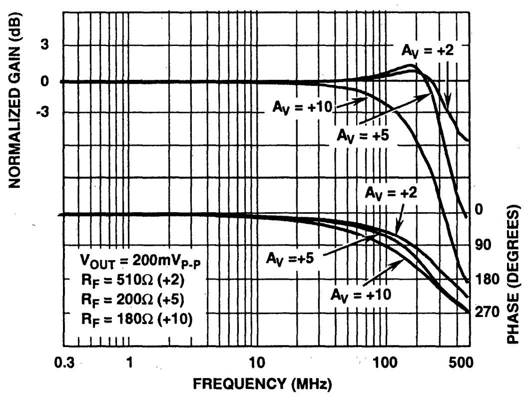


FIGURE 13. FREQUENCY RESPONSE

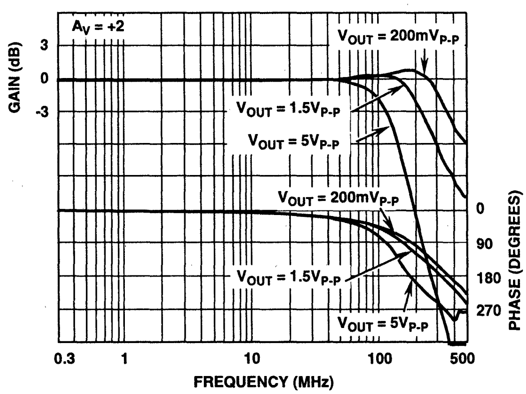


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

Typical Performance Curves V_{SUPPLY} = ±5V, R_F = 510Ω, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

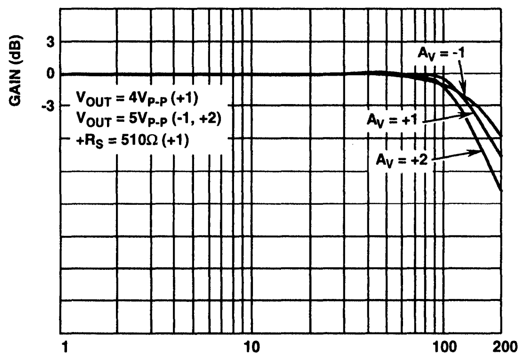


FIGURE 15. FULL POWER BANDWIDTH

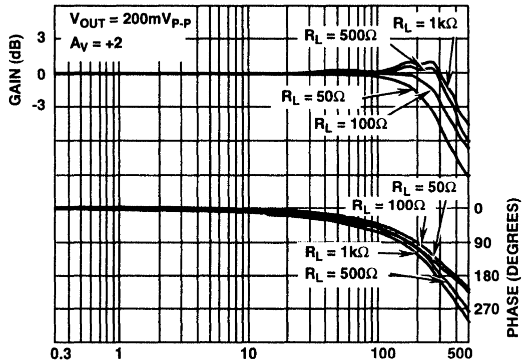


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

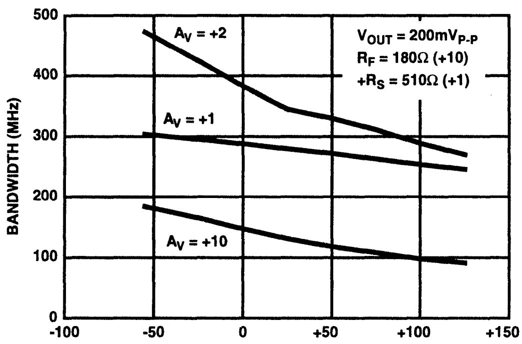


FIGURE 17. -3dB BANDWIDTH vs TEMPERATURE

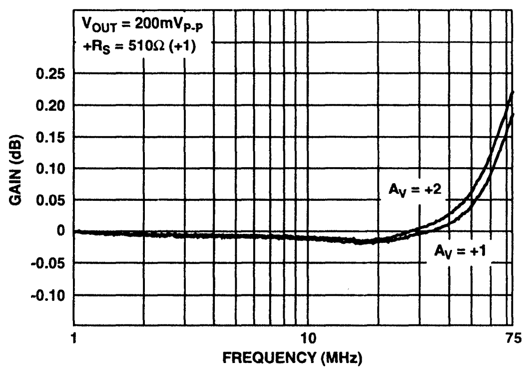


FIGURE 18. GAIN FLATNESS

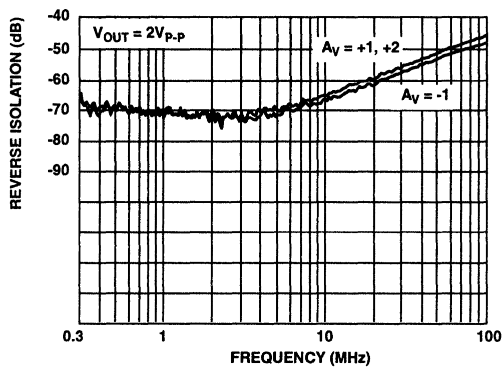


FIGURE 19. REVERSE ISOLATION

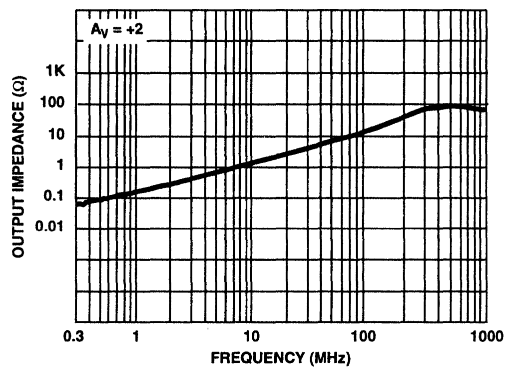


FIGURE 20. OUTPUT IMPEDANCE

2
OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $R_F = 510\Omega$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

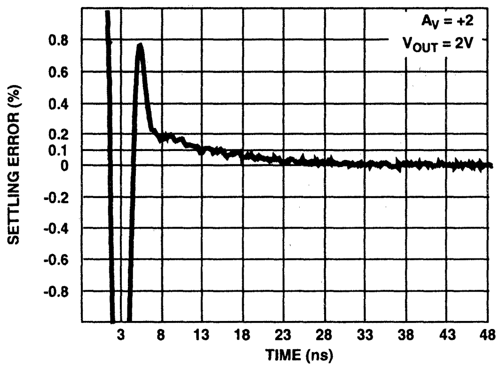


FIGURE 21. SETTLING RESPONSE

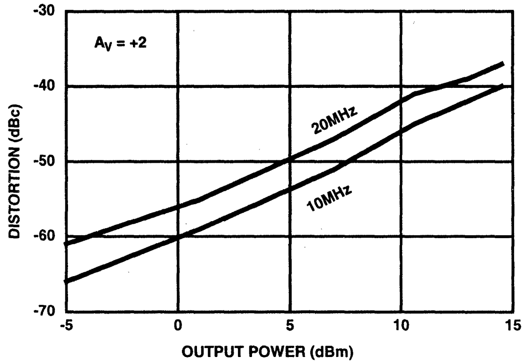


FIGURE 22. 2nd HARMONIC DISTORTION vs P_{OUT}

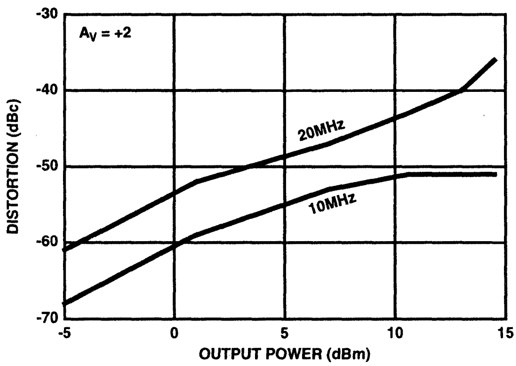


FIGURE 23. 3rd HARMONIC DISTORTION vs P_{OUT}

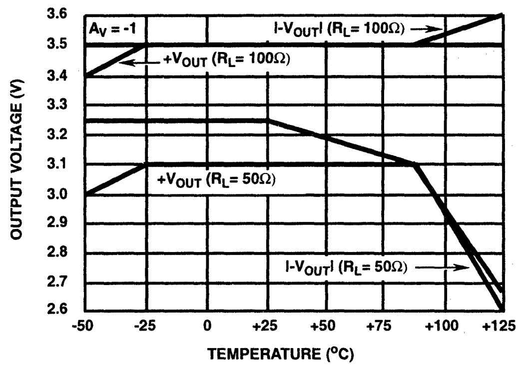


FIGURE 24. OUTPUT VOLTAGE vs TEMPERATURE

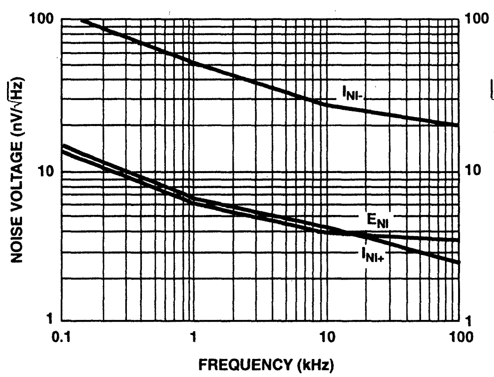


FIGURE 25. INPUT NOISE CHARACTERISTICS

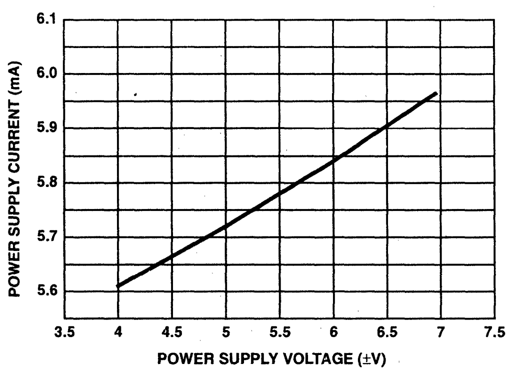


FIGURE 26. SUPPLY CURRENT vs SUPPLY VOLTAGE

HARRIS SEMICONDUCTOR

HFA1106

High Speed, Low Power, Video Operational Amplifier with Compensation Pin

June 1995

Features

- Compensation Pin for Bandwidth Limiting
- Lower Lot-to-Lot Variability With External Compensation
- High Input Impedance 1MΩ
- Differential Gain 0.02%
- Differential Phase. . . . . 0.05 Deg.
- Wide -3dB Bandwidth 315MHz
- Very Fast Slew Rate. 700V/µs
- Low Supply Current. 5.8mA
- Gain Flatness (to 100MHz) . . . . ±0.1dB

Applications

- Noise Critical Applications
- Professional Video Processing
- Medical Imaging
- Video Digitizing Boards/Systems
- Radar/IF Processing
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications
- Flash A/D Drivers
- Oscilloscopes and Analyzers

Description

The HFA1106 is a high speed, low power current feedback operational amplifier built with Harris' proprietary complementary bipolar UHF-1 process. This amplifier features a compensation pin connected to the internal high impedance node, which allows for implementation of external clamping or bandwidth limiting.

Bandwidth limiting is accomplished by connecting a capacitor (C_{COMP}) and series damping resistor (R_{COMP}) from pin 8 to ground. Amplifier performance for various values of C_{COMP} is documented in the Electrical Specifications.

The HFA1106 is ideal for noise critical wideband applications. Not only can the bandwidth be limited to minimize broadband noise, the HFA1106 is optimized for lower feedback resistors (R_F = 100Ω for A_V = +2) than most current feedback amplifiers. The low feedback resistor reduces the inverting input noise current contribution to total output noise, while reducing DC errors as well. Please see the "Application Information" section for details.

Ordering Information

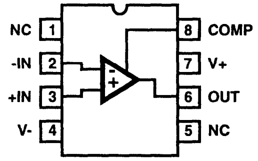
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1106IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1106IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

2

OPERATIONAL AMPLIFIERS

Pinout

HFA1106
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3922

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 2) . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
Junction Temperature. . . . . +175°C
Junction Temperature (Plastic Package) . . . . +150°C
ESD Rating. . . . . >2000V
Lead Temperature (Soldering 10s). +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range . . . . -40°C ≤ T_A ≤ +85°C
Storage Temperature Range. . . . . -65°C ≤ T_A ≤ +150°C
Package Thermal Characteristics θ_{JA}
Plastic DIP Package . . . . 130°C/W
SOIC Package. . . . . 170°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, C_{COMP} = 0pF, R_L = 100Ω Unless Otherwise Specified

PARAMETER		(NOTE 1) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	+25°C	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	ΔV_{CM} = ±1.8V	A	+25°C	47	50	-	dB
	ΔV_{CM} = ±1.8V	A	+85°C	45	48	-	dB
	ΔV_{CM} = ±1.2V	A	-40°C	45	48	-	dB
Input Offset Voltage Power Supply Rejection Ratio	ΔV_{PS} = ±1.8V	A	+25°C	50	54	-	dB
	ΔV_{PS} = ±1.8V	A	+85°C	47	50	-	dB
	ΔV_{PS} = ±1.2V	A	-40°C	47	50	-	dB
Non-Inverting Input Bias Current		A	+25°C	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	+25°C	-	0.5	1	µA/V
	ΔV_{PS} = ±1.8V	A	+85°C	-	0.8	3	µA/V
	ΔV_{PS} = ±1.2V	A	-40°°C	-	0.8	3	µA/V
Non-Inverting Input Resistance	ΔV_{CM} = ±1.8V	A	+25°C	0.8	1.2	-	MΩ
	ΔV_{CM} = ±1.8V	A	+85°C	0.5	0.8	-	MΩ
	ΔV_{CM} = ±1.2V	A	-40°C	0.5	0.8	-	MΩ
Inverting Input Bias Current		A	+25°C	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/°C
Inverting Input Bias Current Common-Mode Sensitivity	ΔV_{CM} = ±1.8V	A	+25°C	-	3	6	µA/V
	ΔV_{CM} = ±1.8V	A	+85°C	-	4	8	µA/V
	ΔV_{CM} = ±1.2V	A	-40°C	-	4	8	µA/V
Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	+25°C	-	2	5	µA/V
	ΔV_{PS} = ±1.8V	A	+85°C	-	4	8	µA/V
	ΔV_{PS} = ±1.2V	A	-40°C	-	4	8	µA/V
Inverting Input Resistance		C	+25°C	-	60	-	Ω
Input Capacitance (Either Input)		C	+25°C	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS Tests)		A	+25°C, +85°C	±1.8	±2.4	-	V
		A	-40°C	±1.2	±1.7	-	V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $C_{COMP} = 0pF$, $R_L = 100\Omega$ Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 1) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
Input Noise Voltage Density (f = 100kHz)		B	+25°C	-	3.5	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current Density (f = 100kHz)		B	+25°C	-	2.5	-	$pA/\sqrt{Hz}$
Inverting Input Noise Current Density (f = 100kHz)		B	+25°C	-	20	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain (A_V = -1)		C	+25°C	-	500	-	kΩ
AC CHARACTERISTICS $A_V = +2$, $R_F = 100\Omega$, $R_{COMP} = 51\Omega$, Unless Otherwise Specified							
-3dB Bandwidth ($A_V = +1$, $R_F = 150\Omega$, $V_{OUT} = 0.2V_{P-P}$)	C_C = 0pF	B	+25°C	250	315	-	MHz
	C_C = 2pF	B	+25°C	140	170	-	MHz
	C_C = 5pF	B	+25°C	65	80	-	MHz
-3dB Bandwidth ($A_V = +2$, $V_{OUT} = 0.2V_{P-P}$)	C_C = 0pF	B	+25°C	185	245	-	MHz
	C_C = 2pF	B	+25°C	110	140	-	MHz
	C_C = 5pF	B	+25°C	55	70	-	MHz
±0.1dB Flat Bandwidth ($A_V = +1$, $R_F = 150\Omega$, $V_{OUT} = 0.2V_{P-P}$)	C_C = 0pF	B	+25°C	45	65	-	MHz
	C_C = 2pF	B	+25°C	25	40	-	MHz
	C_C = 5pF	B	+25°C	13	17	-	MHz
±0.1dB Flat Bandwidth ($A_V = +2$, $V_{OUT} = 0.2V_{P-P}$)	C_C = 0pF	B	+25°C	60	100	-	MHz
	C_C = 2pF	B	+25°C	15	30	-	MHz
	C_C = 5pF	B	+25°C	11	14	-	MHz
Minimum Stable Gain		A	Full	1	-	-	V/V
OUTPUT CHARACTERISTICS $A_V = +2$, $R_F = 100\Omega$, $R_{COMP} = 51\Omega$, Unless Otherwise Specified							
Output Voltage Swing ($A_V = -1$, $R_F = 510\Omega$)		A	+25°C	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current ($A_V = -1$, $R_L = 50\Omega$, $R_F = 510\Omega$)		A	+25°C, +85°C	50	60	-	mA
		A	-40°C	28	42	-	mA
DC Closed Loop Output Impedance		B	+25°C	-	0.07	-	Ω
Output Short Circuit Current (A_V = -1)		B	+25°C	-	90	-	mA
Second Harmonic Distortion (10MHz, $V_{OUT} = 2V_{P-P}$)	C_C = 0pF	B	+25°C	-45	-53	-	dBc
	C_C = 2pF	B	+25°C	-42	-48	-	dBc
	C_C = 5pF	B	+25°C	-38	-44	-	dBc
Third Harmonic Distortion (10MHz, $V_{OUT} = 2V_{P-P}$)	C_C = 0pF	B	+25°C	-50	-57	-	dBc
	C_C = 2pF	B	+25°C	-48	-56	-	dBc
	C_C = 5pF	B	+25°C	-48	-56	-	dBc
Second Harmonic Distortion (20MHz, $V_{OUT} = 2V_{P-P}$)	C_C = 0pF	B	+25°C	-42	-46	-	dBc
	C_C = 2pF	B	+25°C	-38	-42	-	dBc
	C_C = 5pF	B	+25°C	-34	-38	-	dBc
Third Harmonic Distortion (20MHz, $V_{OUT} = 2V_{P-P}$)	C_C = 0pF	B	+25°C	-46	-57	-	dBc
	C_C = 2pF	B	+25°C	-52	-57	-	dBc
	C_C = 5pF	B	+25°C	-50	-57	-	dBc

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, C_{COMP} = 0pF, R_L = 100Ω Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 1) TEST LEVEL	TEMP	ALL GRADES			UNITS
				MIN	TYP	MAX	
TRANSIENT CHARACTERISTICS A_V = +2, R_F = 100Ω, R_{COMP} = 51Ω, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = 0.5V_{P-P}, A_V = +1, R_F = 150Ω)	C_C = 0pF	B	+25°C	-	2.6	2.9	ns
	C_C = 2pF	B	+25°C	-	3.7	4.2	ns
	C_C = 5pF	B	+25°C	-	5.2	6.2	ns
Rise and Fall Times (V_{OUT} = 0.5V_{P-P}, A_V = +2)	C_C = 0pF	B	+25°C	-	2.7	3.2	ns
	C_C = 2pF	B	+25°C	-	3.9	4.4	ns
	C_C = 5pF	B	+25°C	-	5.9	6.9	ns
Overshoot (Note 3) (A_V = +1, R_F = 150Ω, V_{IN} t_{RISE} = 2.5ns)	V_{OUT} = 250mV_{P-P}	B	+25°C	-	1.5	4	%
	V_{OUT} = 2V_{P-P}	B	+25°C	-	6	10	%
	V_{OUT} = 0 to 2V	B	+25°C	-	4	7.5	%
Overshoot (Note 3) (A_V = +2, V_{IN} t_{RISE} = 2.5ns)	V_{OUT} = 250mV_{P-P}	B	+25°C	-	2	5	%
	V_{OUT} = 2V_{P-P}	B	+25°C	-	6.5	12	%
	V_{OUT} = 0 to 2V	B	+25°C	-	2.5	7.5	%
Slew Rate (V_{OUT} = 4V_{P-P}, A_V = +1, R_F = 150Ω)	+SR, C_C = 0pF	B	+25°C	580	680	-	V/µs
	-SR, C_C = 0pF	B	+25°C	400	545	-	V/µs
	+SR, C_C = 2pF	B	+25°C	470	530	-	V/µs
	-SR, C_C = 2pF	B	+25°C	300	410	-	V/µs
	+SR, C_C = 5pF	B	+25°C	320	365	-	V/µs
	-SR, C_C = 5pF	B	+25°C	200	300	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = +2)	+SR, C_C = 0pF	B	+25°C	750	910	-	V/µs
	-SR, C_C = 0pF	B	+25°C	500	720	-	V/µs
	+SR, C_C = 2pF	B	+25°C	550	730	-	V/µs
	-SR, C_C = 2pF	B	+25°C	350	520	-	V/µs
	+SR, C_C = 5pF	B	+25°C	380	485	-	V/µs
	-SR, C_C = 5pF	B	+25°C	250	375	-	V/µs
Settling Time (V_{OUT} = +2V to 0V Step, C_C = 0pF to 5pF)	To 0.1%	B	+25°C	-	26	35	ns
	To 0.05%	B	+25°C	-	33	43	ns
	To 0.02%	B	+25°C	-	49	75	ns
Overload Recovery Time (V_{IN} = ±2V)		B	+25°C	-	8.5	-	ns
VIDEO CHARACTERISTICS A_V = +2, R_F = 100Ω, R_{COMP} = 51Ω, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz, R_L = 150Ω)	C_C = 0pF	B	+25°C	-	0.02	-	%
	C_C = 5pF	B	+25°C	-	0.02	-	%
Differential Phase (f = 3.58MHz, R_L = 150Ω)	C_C = 0pF	B	+25°C	-	0.05	-	Degrees
	C_C = 5pF	B	+25°C	-	0.07	-	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	+25°C	±4.5	-	±5.5	V
Power Supply Current		A	+25°C	-	5.8	6.1	mA
		A	Full	-	5.9	6.3	mA

NOTES:

1. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability; however, continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.
3. Undershoot dominates for output signal swings below GND (e.g. 2V_{P-P}) yielding a higher overshoot limit compared to the V_{OUT} = 0 to 2V condition.

Application Information

Optimum Feedback Resistor

All current feedback amplifiers (CFAs) require a feedback resistor (R_F) even for unity gain applications, and R_F in conjunction with the internal compensation capacitor sets the dominant pole of the frequency response. Thus the amplifier's bandwidth is inversely proportional to R_F. The HFA1106 design is optimized for $R_F = 150\Omega$ at a gain of +1. Decreasing R_F decreases stability resulting in excessive peaking and overshoot - Note: Capacitive feedback causes the same problems due to the feedback impedance decrease at higher frequencies. At higher gains, however, the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth (e.g. $R_F = 100\Omega$ for $A_V = +2$).

Why Use Externally Compensated Amplifiers?

Externally compensated op amps were originally developed to allow operation at gains below the amplifier's minimum stable gain. This enabled development of non-unity gain stable op amps with very high bandwidth and slew rates. Users needing lower closed loop gains could stabilize the amplifier with external compensation if the associated performance decrease was tolerable.

With the advent of CFAs, unity gain stability and high performance are no longer mutually exclusive, so why offer unity gain stable op amps with compensation pins?

The main reason for external compensation is to allow users to tailor the amplifier's performance to their specific system needs. Bandwidth can be limited to the exact value required, thereby eliminating excess bandwidth and its associated noise. A compensated op amp is also more predictable; lower lot-to-lot variation requires less system overdesign to cover process variability. Finally, access to the internal high impedance node allows users to implement external output limiting or allows for stabilizing the amplifier when driving large capacitive loads.

Noise Advantages - Uncompensated

The HFA1106 delivers lower broadband noise even without an external compensation capacitor. Package capacitance present at the Comp pin stabilizes the op amp, so lower value feedback resistors can be used. A smaller value R_F minimizes the noise voltage contribution of the amplifier's inverting input noise current - $I_{NI} \times R_F$, usually a large contributor on CFAs - and minimizes the resistor's thermal noise contribution ($4KTR_F$). Figure 1 details the HFA1105 broadband noise performance in its recommended configuration of $A_V = +2$, and $R_F = 510\Omega$. Adding a Comp pin to the HFA1105 (thereby creating the HFA1106) yields the 23% noise reduction shown in Figure 2. In both cases, the scope bandwidth, 100MHz, limits the measurement range to prevent amplifier bandwidth differences from affecting the results.

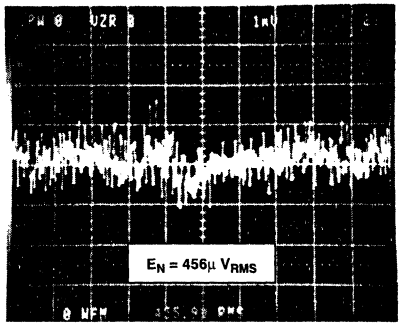


FIGURE 1. HFA1105 NOISE PERFORMANCE, $A_V = +2$, $R_F = 510\Omega$

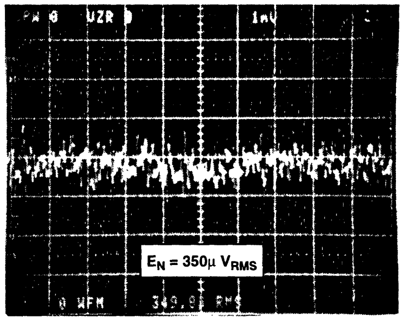


FIGURE 2. HFA1106 NOISE PERFORMANCE, UNCOMPENSATED, $A_V = +2$, $R_F = 100\Omega$

Offset Advantage

An added advantage of the lower value R_F is a smaller DC output offset. The op amp's inverting input bias current (I_{BI}) flows through the feedback resistor and generates an offset voltage error defined by:

$$V_E = I_{BI} \times R_F;\ \text{and}\ V_{OS} = A_V\left(\pm V_{IO}\right) \pm V_E$$

Reducing R_F reduces these errors.

Bandwidth Limiting

The HFA1106 bandwidth may be limited by connecting a resistor, R_{COMP} (required to damp the interaction between the compensation capacitor and the package parasitics), and capacitor, C_{COMP}, in series from pin 8 to GND. Typical performance characteristics for various C_{COMP} values are listed in the specification table. The HFA1106 is already unity gain stable, so the main reason for limiting the bandwidth is to reduce the broadband noise.

Noise Advantages - Compensated

System noise reduction is maximized by limiting the op amp to the bandwidth required for the application. Noise increases as the square root of the bandwidth increase (4x bandwidth increase yields 2x noise increase), so eliminating excess bandwidth significantly reduces system noise. Figure 3 illustrates the noise performance of the HFA1106 with its bandwidth limited to 40MHz by a 10pF C_{COMP}. As expected the noise decreases by approximately 37% (100% x (1-$\sqrt{40MHz/100MHz}$)) compared with Figure 2. The decrease is an even more dramatic 48% versus the HFA1105 noise level in Figure 1.

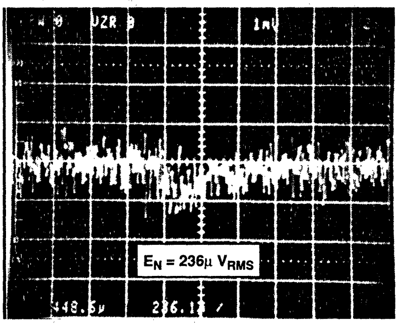


FIGURE 3. HFA1106 NOISE PERFORMANCE, COMPENSATED, $A_V = +2$, $R_F = 100\Omega$, $C_C = 10pF$

Additionally, compensating the HFA1106 allows the use of a lower value R_F for a given gain. The decreased bandwidth due to C_{COMP} keeps the amplifier stable by offsetting the increased bandwidth from the lower R_F. As noted previously, a lower value R_F provides the double benefit of reduced DC errors and lower total noise.

Less Lot-to-Lot Variability

External compensation provides another advantage by allowing designers to set the op amp's performance with a precision external component. On-chip compensation capacitors can vary by 10-20% over the process extremes. A precise external capacitor dominates the on-chip compensation for consistent lot-to-lot performance and more robust designs. Compensating high frequency amplifiers to lower bandwidths can simplify design tasks and ensure long term manufacturability.

PC Board Layout

This amplifier's frequency response depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the device's input and output connections. Capacitance, parasitic or planned, connected to the output must be minimized, compensated for by increasing C_{COMP}, or isolated by a series output resistor.

Care must also be taken to minimize the capacitance to ground at the amplifier's inverting input (-IN), as this capacitance causes gain peaking, pulse overshoot, and if large enough, instability. To reduce this capacitance, the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 4.

Evaluation Board

The performance of the HFA1106 may be evaluated using the HFA11XX Evaluation Board.

Figure 4 details the evaluation board layout and schematic. Connecting R_{COMP} and C_{COMP} in series from socket pin 8 to the GND plane compensates the op amp. Cutting the trace from pin 8 to the V_H connector removes the stray parallel capacitance, which would otherwise affect the evaluation. Additionally, the 500Ω feedback and gain setting resistors should be changed to the proper value for the gain being evaluated.

To order evaluation boards (part number HFA11XXEVAL), please contact your local sales office.

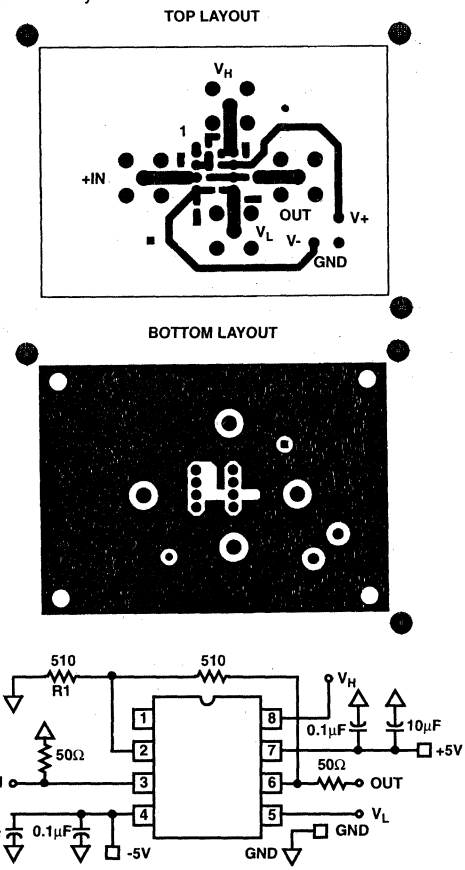


FIGURE 4. EVALUATION BOARD SCHEMATIC AND LAYOUT

Die Characteristics

DIE DIMENSIONS:

59mils x 58.2mils x 19mils ± 1mils
1500μm x 1480μm x 483μm ± 25.4μm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:

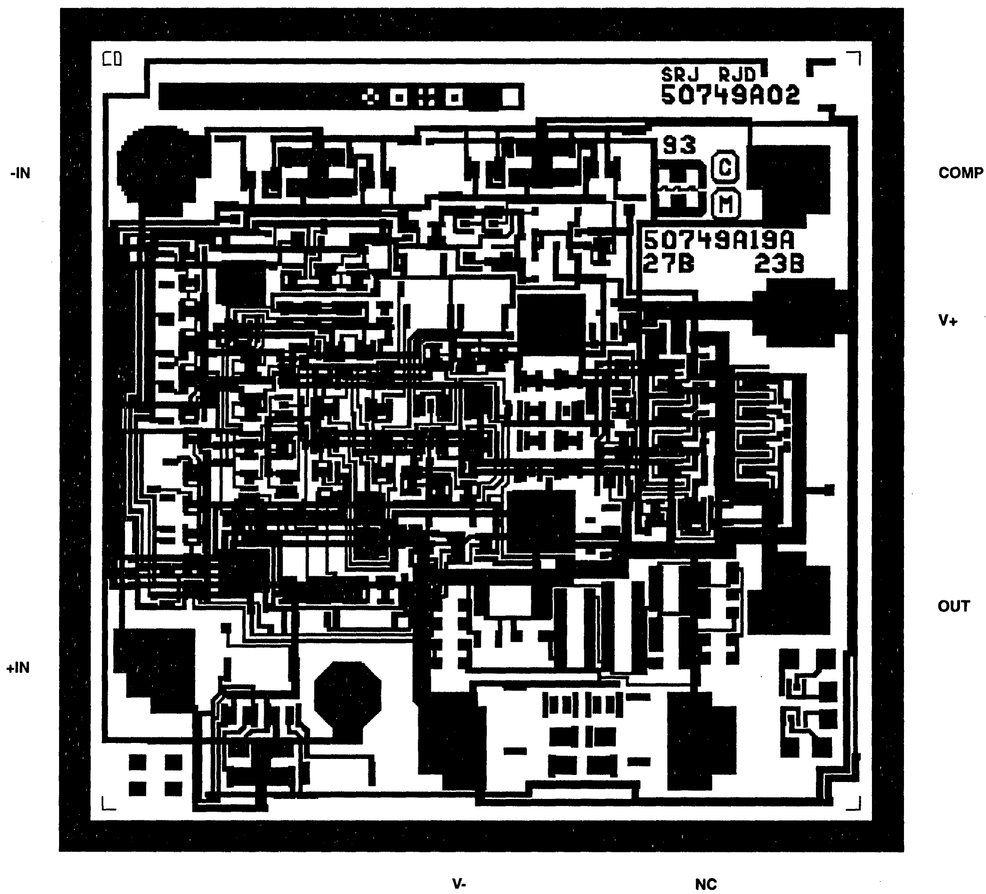
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

TRANSISTOR COUNT: 75

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1106



Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

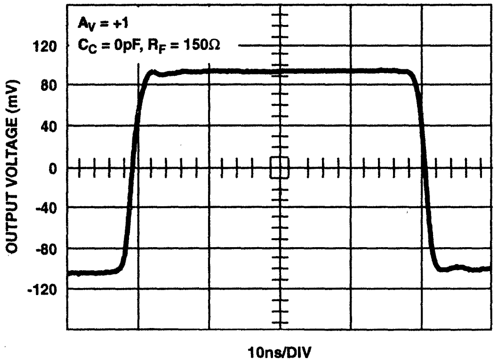


FIGURE 5. SMALL SIGNAL PULSE RESPONSE

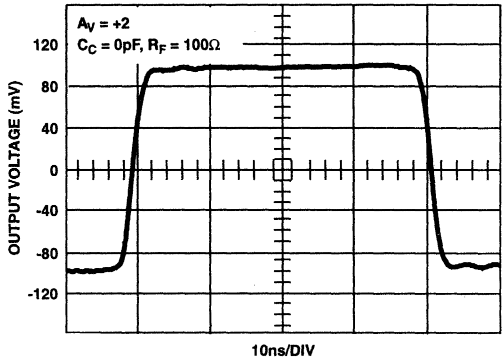


FIGURE 6. SMALL SIGNAL PULSE RESPONSE

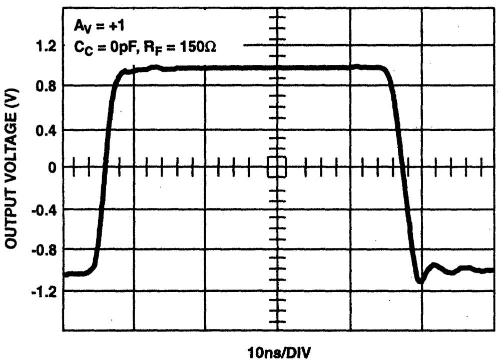


FIGURE 7. LARGE SIGNAL PULSE RESPONSE

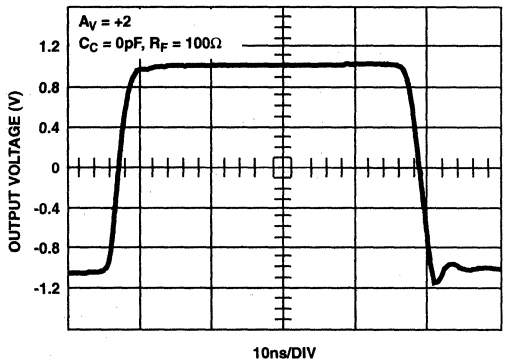


FIGURE 8. LARGE SIGNAL PULSE RESPONSE

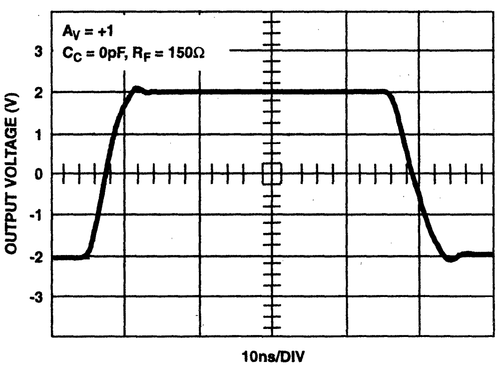


FIGURE 9. LARGE SIGNAL PULSE RESPONSE

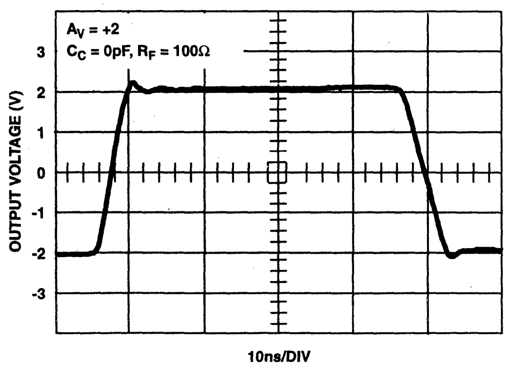


FIGURE 10. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

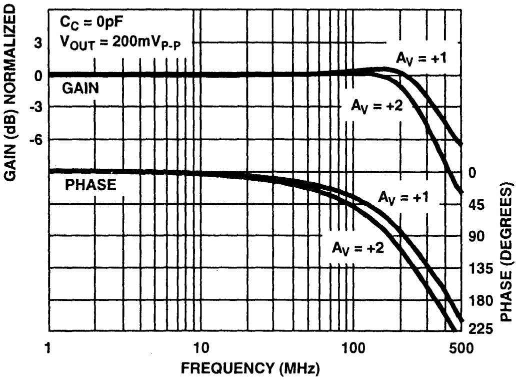


FIGURE 11. FREQUENCY RESPONSE

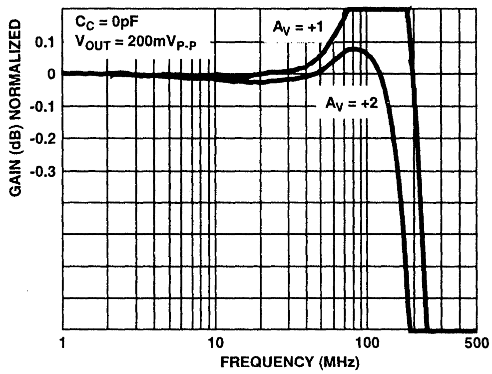


FIGURE 12. GAIN FLATNESS

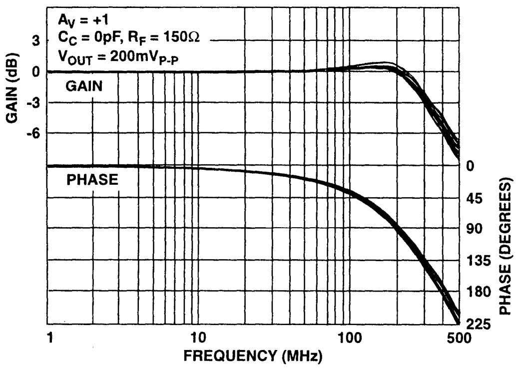


FIGURE 13. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

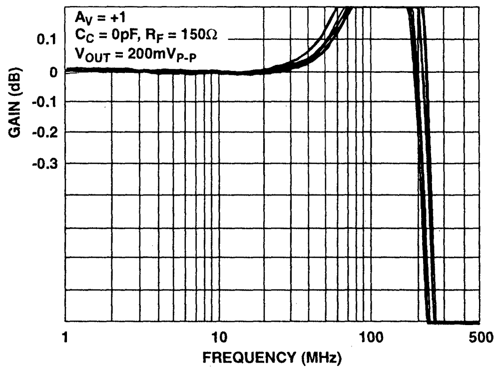


FIGURE 14. GAIN FLATNESS (12 UNITS, 4 RUNS)

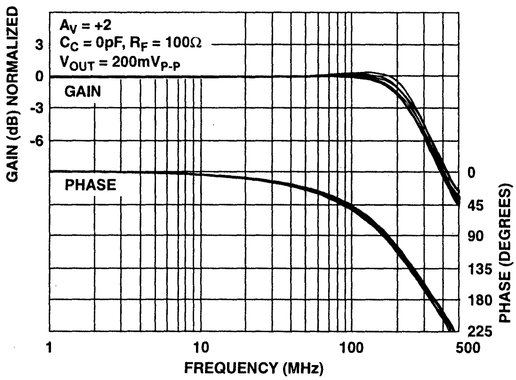


FIGURE 15. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

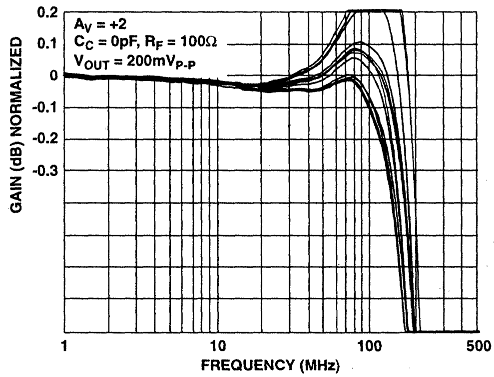


FIGURE 16. GAIN FLATNESS (12 UNITS, 4 RUNS)

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

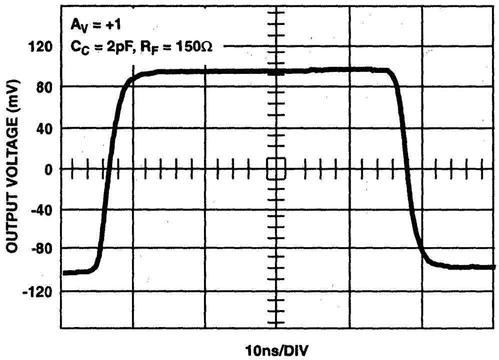


FIGURE 17. SMALL SIGNAL PULSE RESPONSE

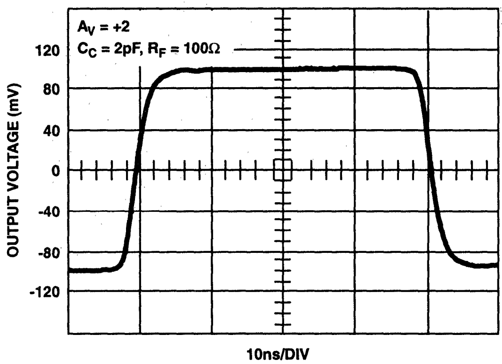


FIGURE 18. SMALL SIGNAL PULSE RESPONSE

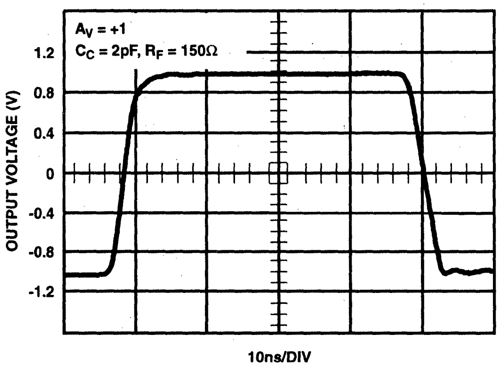


FIGURE 19. LARGE SIGNAL PULSE RESPONSE

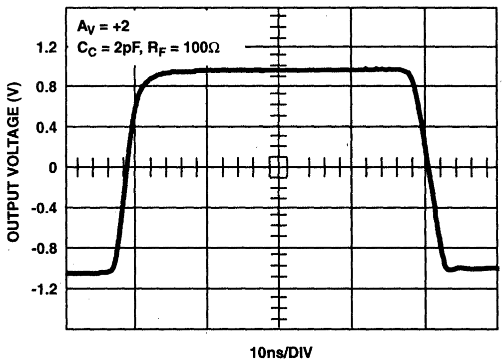


FIGURE 20. LARGE SIGNAL OUTPUT VOLTAGE

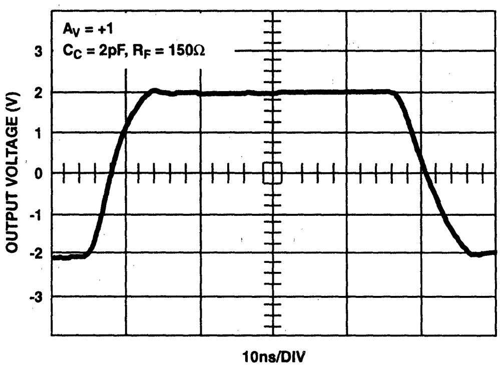


FIGURE 21. LARGE SIGNAL PULSE RESPONSE

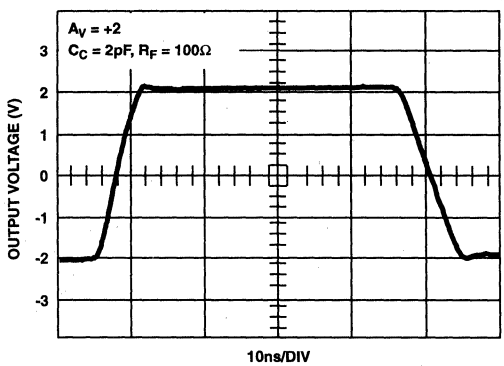


FIGURE 22. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

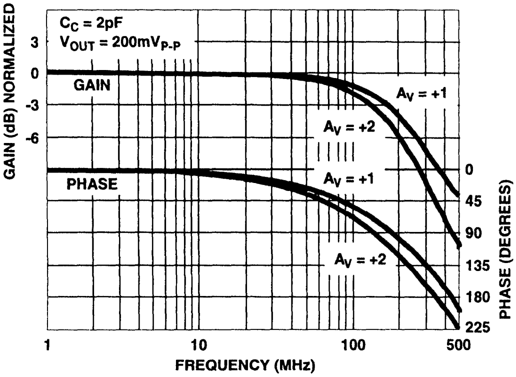


FIGURE 23. FREQUENCY RESPONSE

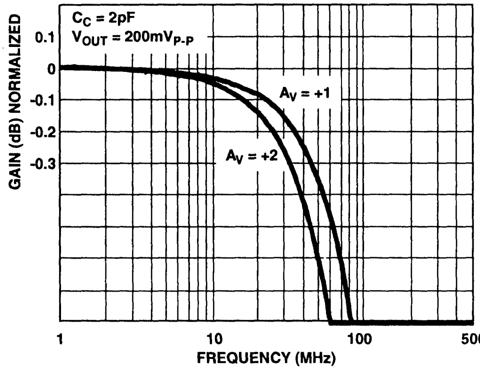


FIGURE 24. GAIN FLATNESS

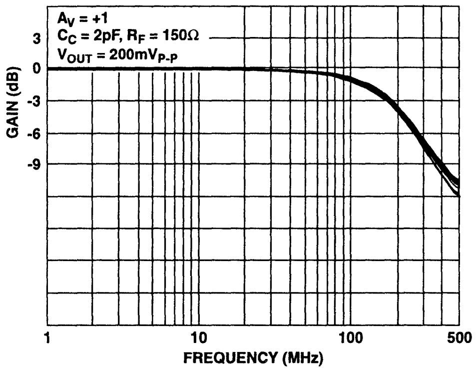


FIGURE 25. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

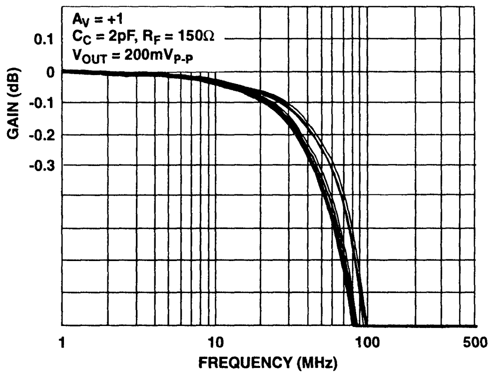


FIGURE 26. GAIN FLATNESS (12 UNITS, 4 RUNS)

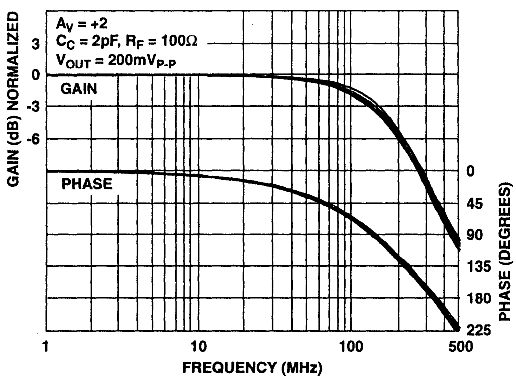


FIGURE 27. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

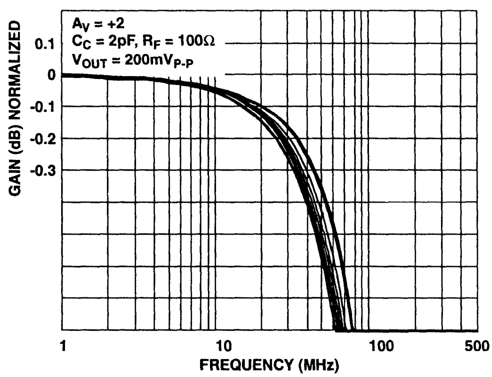


FIGURE 28. GAIN FLATNESS (12 UNITS, 4 RUNS)

2

OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

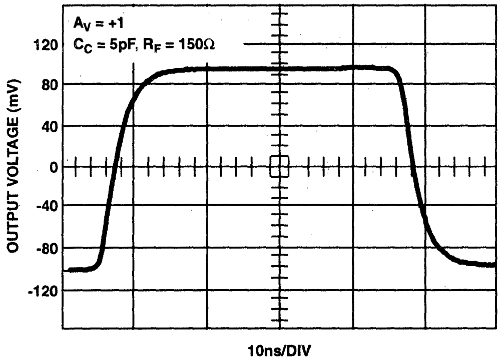


FIGURE 29. SMALL SIGNAL PULSE RESPONSE

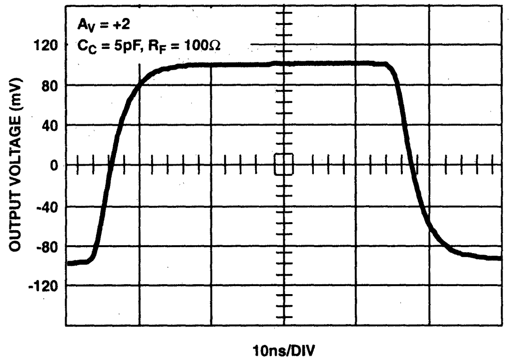


FIGURE 30. SMALL SIGNAL PULSE RESPONSE

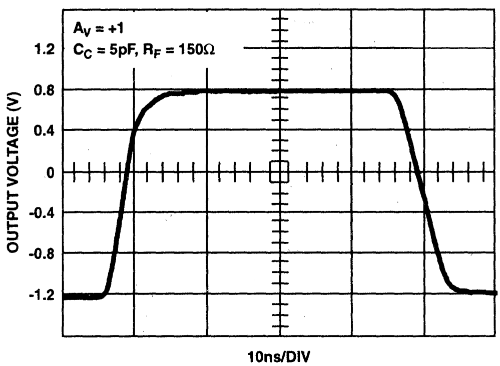


FIGURE 31. LARGE SIGNAL PULSE RESPONSE

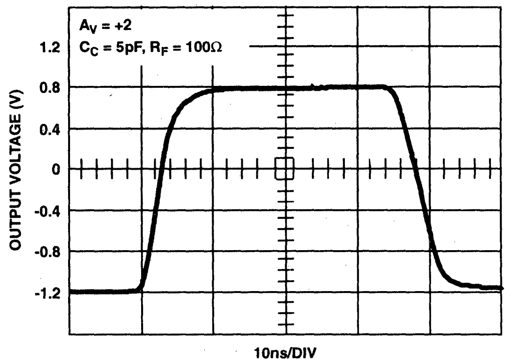


FIGURE 32. LARGE SIGNAL PULSE RESPONSE

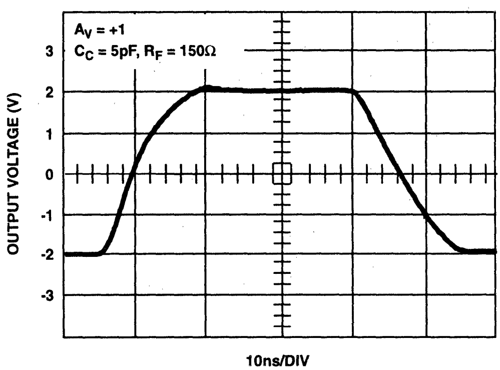


FIGURE 33. LARGE SIGNAL PULSE RESPONSE

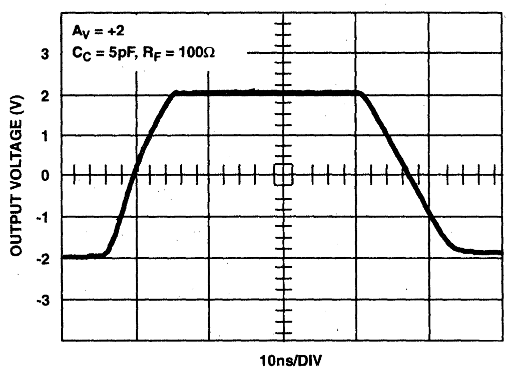


FIGURE 34. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

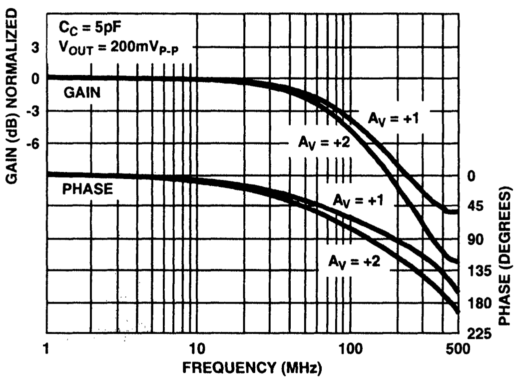


FIGURE 35. FREQUENCY RESPONSE

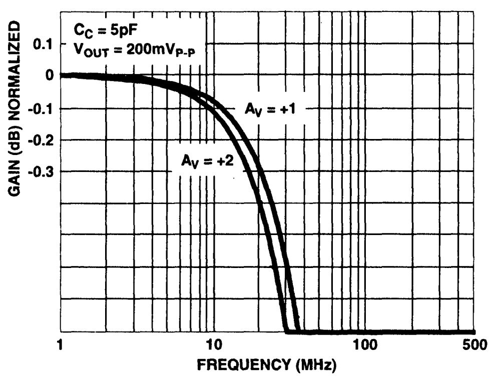


FIGURE 36. GAIN FLATNESS

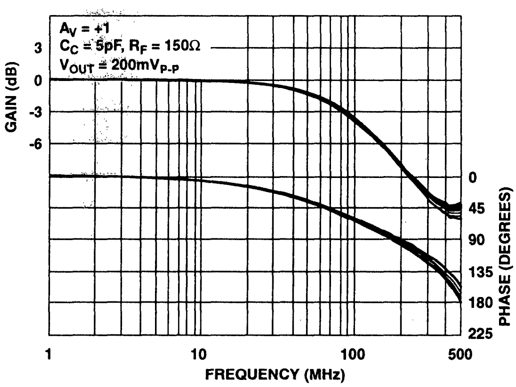


FIGURE 37. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

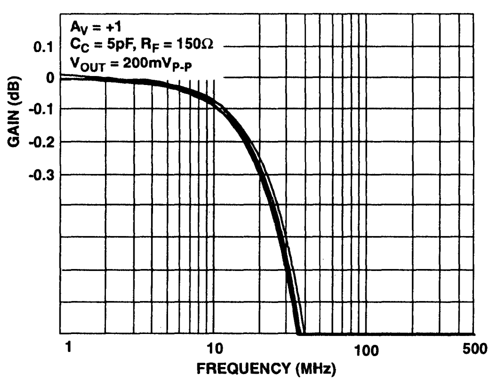


FIGURE 38. GAIN FLATNESS (12 UNITS, 4 RUNS)

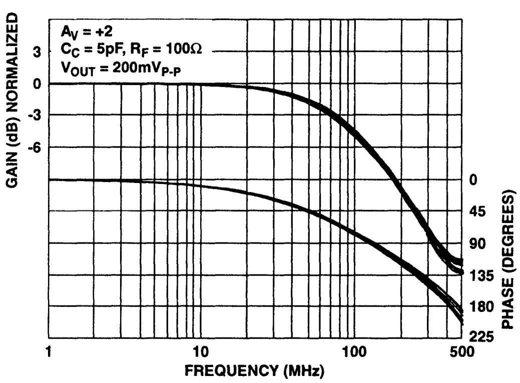


FIGURE 39. FREQUENCY RESPONSE (12 UNITS, 4 RUNS)

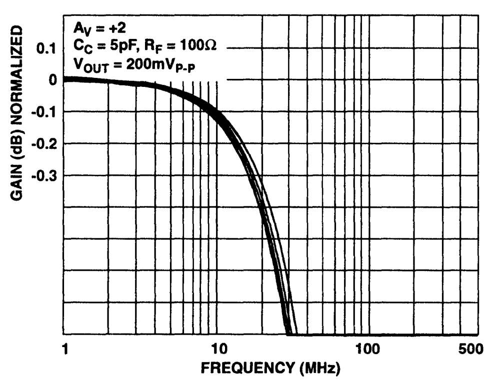


FIGURE 40. GAIN FLATNESS (12 UNITS, 4 RUNS)

2
OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

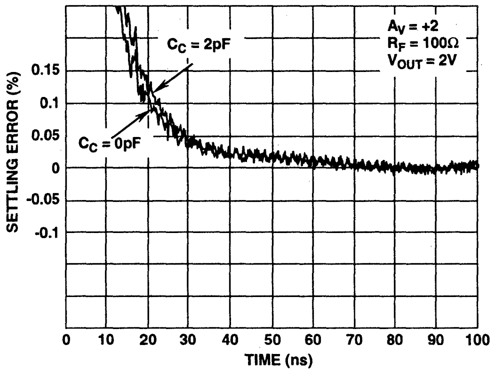


FIGURE 41. SETTLING RESPONSE

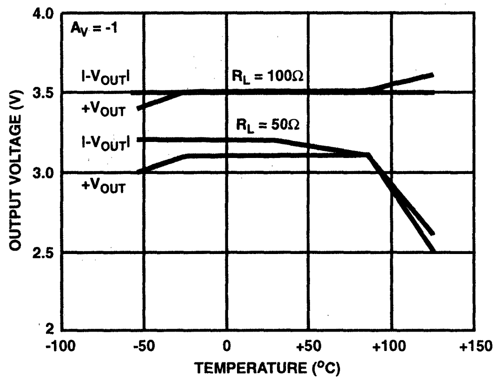


FIGURE 42. OUTPUT VOLTAGE vs TEMPERATURE

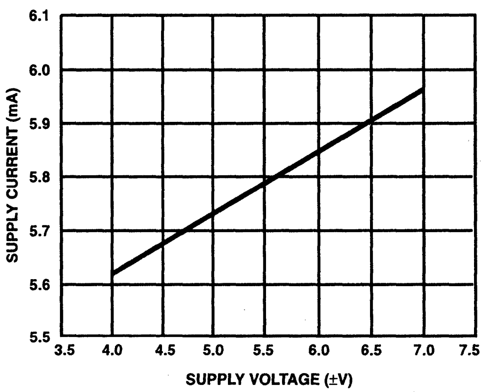


FIGURE 43. SUPPLY CURRENT vs SUPPLY VOLTAGE

HARRIS SEMICONDUCTOR

HFA1109, HFA1149

ADVANCE INFORMATION

June 1995

High-Speed, Low Power, Current Feedback Operational Amplifiers

Features

- Wide - 3dB Bandwidth (A_V = +2) 500MHz
- Gain Flatness (to 250MHz) 0.5dB
- Very Fast Slew Rate (A_V = +2) 1200V/µs
- High Input Impedance 1.7MΩ
- Differential Gain/Phase .... 0.02%/0.02 Deg
- Low Supply Current 10mA
- Fast Output Enable/Disable (HFA1149)

Applications

- Professional Video Processing
- Video Switchers and Routers
- Medical Imaging
- PC Multimedia Systems
- Video Pixel Switching (HFA1149)
- Video Distribution Amplifiers
- Flash Converter Drivers
- Radar/IF Processing

Description

The HFA1109, and HFA1149 are high speed, low power, current feedback amplifiers built with Harris' proprietary complementary bipolar UHF-1 process. These amplifiers feature a unique combination of power and performance specifically tailored for video applications.

The HFA1109 is a standard pinout op amp. It is a higher performance, drop-in replacement (no feedback resistor change required) for the CLC409.

The HFA1149 incorporates an output disable pin which is TTL/CMOS compatible, and user programmable for polarity (active high or low). This feature eliminates the inverter required between amplifiers in multiplexer configurations. The ultra-fast (10ns) enable and disable times make the HFA1149 the obvious choice for pixel switching and other high speed multiplexing applications. The HFA1149 is a high performance, pin compatible upgrade for the popular HA-5020 and HFA1145, as well as the CLC410.

2

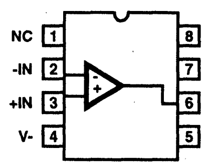
OPERATIONAL AMPLIFIERS

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1109IP, HFA1149IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1109IB, HFA1149IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

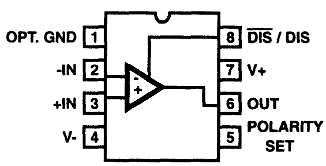
Pinouts

HFA1109
(PDIP, SOIC)
TOP VIEW



OP AMP

HFA1149
(PDIP, SOIC)
TOP VIEW



OP AMP WITH DISABLE

HFA1149 PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
Opt. Gnd	Optional Gnd. Maintains Disable Pin TTL Compatibility with Asymmetrical Supplies (e.g. +10V, 0V).
Polarity Set	Defines Polarity of Disable Input. High or Floating Selects Active Low Disable (i.e. $\overline{DIS}$).
$\overline{DIS}$/DIS	TTL Compatible Disable Input. Output is Driven to a True Hi-Z State When Active. Polarity depends on state of Polarity Set Pin.

HFA1149 DISABLE FUNCTIONALITY

POLARITY SET (PIN 5)	DISABLE (PIN 8)	OUTPUT (PIN 6)
High or Float	High or Float	Enabled
High or Float	Low	Disabled
Low	High or Float	Disabled
Low	Low	Enabled

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 4019

HARRIS SEMICONDUCTOR

HFA1112

July 1995

Ultra High-Speed Programmable Gain Buffer Amplifier

Features

- User Programmable for Closed-Loop Gains of +1, -1 or +2 without Use of External Resistors
- Wide -3dB Bandwidth 850MHz
- Very Fast Slew Rate..................... 2400V/µs
- Fast Settling Time (0.1%) 11ns
- High Output Current 60mA
- Excellent Gain Accuracy.................. 0.99V/V
- Overdrive Recovery....................... <10ns
- Standard Operational Amplifier Pinout

Applications

- RF/IF Processors
- Driving Flash A/D Converters
- High-Speed Communications
- Impedance Transformation
- Line Driving
- Video Switching and Routing
- Radar Systems
- Medical Imaging Systems

Description

The HFA1112 is a closed loop Buffer featuring user programmable gain and ultra high speed performance. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, the HFA1112 offers a wide -3dB bandwidth of 850MHz, very fast slew rate, excellent gain flatness, low distortion and high output current.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" section. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

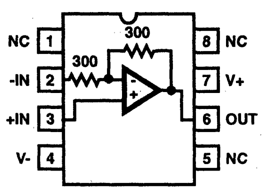
This amplifier is available with programmable output clamps as the HFA1113. For applications requiring a standard buffer pinout, please refer to the HFA1110 datasheet. For Military product, refer to the HFA1112/883 data sheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1112MJ/883	-55°C to +125°C	8 Lead CerDIP
HFA1112IJ	-40°C to +85°C	8 Lead CerDIP
HFA1112IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1112IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

Pinout

HFA1112
(PDIP, CERDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1, 5, 8	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
OUT	6	Output
V+	7	Positive Supply

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 2992.3

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage.................................... V_{SUPPLY}
Differential Input Voltage 5V
Output Current 60mA
Junction Temperature (Ceramic and Die)............... +175°C
Junction Temperature (Plastic Package) .... +150°C
Lead Temperature (Soldering 10s).................... +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HFA1112I............................ -40°C ≤ T_A ≤ +85°C
Storage Temperature ....-65°C ≤ T_A ≤ +150°C

Thermal Package Characteristics (°C/W)	θ_{JA}	θ_{JC}
CerDIP Package	116	36
Plastic DIP Package	98	N/A
SOIC Package	170	N/A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEMPERATURE	HFA1112I MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Output Offset Voltage	+25°C	-	8	25	mV
	Full	-	-	35	mV
Output Offset Voltage Drift	Full	-	10	-	μV/°C
PSRR	+25°C	39	45	-	dB
	Full	35	-	-	dB
Input Noise Voltage (100kHz, Note 2)	+25°C	-	9	-	nV/√Hz
Non-Inverting Input Noise Current (100kHz, Note 2)	+25°C	-	37	-	pA/√Hz
Non-Inverting Input Bias Current	+25°C	-	25	40	μA
	Full	-	-	65	μA
Non-Inverting Input Resistance	+25°C	25	50	-	kΩ
Inverting Input Resistance (Note 1)	+25°C	240	300	360	Ω
Input Capacitance (Either Input)	+25°C	-	2	-	pF
Input Common Mode Range	Full	±2.5	±2.8	-	V
TRANSFER CHARACTERISTICS					
Gain (A_V = +1, V_{IN} = +2V)	+25°C	0.980	0.990	1.020	V/V
	Full	0.975	-	1.025	V/V
Gain (A_V = +2, V_{IN} = +1V)	+25°C	1.96	1.98	2.04	V/V
	Full	1.95	-	2.05	V/V
DC Non-Linearity (A_V = +2, ±2V Full Scale, Note 2)	+25°C	-	0.02	-	%
OUTPUT CHARACTERISTICS					
Output Voltage (A_V = -1, Note 2)	+25°C	±3.0	±3.3	-	V
	Full	±2.5	±3.0	-	V
Output Current (R_L = 50Ω, Note 2)	+25°C, +85°C	50	60	-	mA
	-40°C	35	50	-	mA
DC Closed Loop Output Impedance (A_V = +2)	+25°C	-	0.3	-	Ω
POWER SUPPLY CHARACTERISTICS					
Supply Voltage Range	Full	±4.5	-	±5.5	V
Supply Current (Note 2)	+25°C	-	21	26	mA
	Full	-	-	33	mA

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMPERATURE	HFA1112I MIN	TYP	MAX	UNITS
AC CHARACTERISTICS						
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	450	800	-	MHz
	A_V = +1	+25°C	500	850	-	MHz
	A_V = +2	+25°C	350	550	-	MHz
Slew Rate (V_{OUT} = 5V_{P-P}, Note 1)	A_V = -1	+25°C	1500	2400	-	V/µs
	A_V = +1	+25°C	800	1500	-	V/µs
	A_V = +2	+25°C	1100	1900	-	V/µs
Full Power Bandwidth (V_{OUT} = 5V_{P-P}, Note 2)	A_V = -1	+25°C	-	300	-	MHz
	A_V = +1	+25°C	-	150	-	MHz
	A_V = +2	+25°C	-	220	-	MHz
Gain Flatness (to 30MHz, Notes 1, 2)	A_V = -1	+25°C	-	±0.02	-	dB
	A_V = +1	+25°C	-	±0.1	-	dB
	A_V = +2	+25°C	-	±0.015	±0.04	dB
Gain Flatness (to 50MHz, Notes 1, 2)	A_V = -1	+25°C	-	±0.05	-	dB
	A_V = +1	+25°C	-	±0.2	-	dB
	A_V = +2	+25°C	-	±0.036	±0.08	dB
Gain Flatness (to 100MHz, Notes 1, 2)	A_V = -1	+25°C	-	±0.10	-	dB
	A_V = +2	+25°C	-	±0.07	±0.22	dB
Linear Phase Deviation (to 100MHz, Note 2)	A_V = -1	+25°C	-	±0.13	-	Degrees
	A_V = +1	+25°C	-	±0.83	-	Degrees
	A_V = +2	+25°C	-	±0.05	-	Degrees
2nd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	-	-52	-	dBc
	A_V = +1	+25°C	-	-57	-	dBc
	A_V = +2	+25°C	-	-52	-45	dBc
3rd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	-	-71	-	dBc
	A_V = +1	+25°C	-	-73	-	dBc
	A_V = +2	+25°C	-	-72	-65	dBc
2nd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	-	-47	-	dBc
	A_V = +1	+25°C	-	-53	-	dBc
	A_V = +2	+25°C	-	-47	-40	dBc
3rd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	-	-63	-	dBc
	A_V = +1	+25°C	-	-68	-	dBc
	A_V = +2	+25°C	-	-65	-55	dBc
2nd Harmonic Distortion (100MHz, V_{OUT} = 2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	-	-41	-	dBc
	A_V = +1	+25°C	-	-50	-	dBc
	A_V = +2	+25°C	-	-42	-35	dBc
3rd Harmonic Distortion (100MHz, V_{OUT} = 2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	-	-55	-	dBc
	A_V = +1	+25°C	-	-49	-	dBc
	A_V = +2	+25°C	-	-62	-45	dBc

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMPERATURE	HFA1112I MIN	HFA1112I TYP	HFA1112I MAX	UNITS
3rd Order Intercept (A_V = +2, Note 2)	100MHz	+25°C	-	28	-	dBm
	300MHz	+25°C	-	13	-	dBm
1dB Compression (A_V = +2, Note 2)	100MHz	+25°C	-	19	-	dBm
	300MHz	+25°C	-	12	-	dBm
Reverse Isolation (S_{12}, Note 2)	40MHz	+25°C	-	-70	-	dB
	100MHz	+25°C	-	-60	-	dB
	600MHz	+25°C	-	-32	-	dB
TRANSIENT CHARACTERISTICS						
Rise Time (V_{OUT} = 0.5V Step, Note 1)	A_V = -1	+25°C	-	500	800	ps
	A_V = +1	+25°C	-	480	750	ps
	A_V = +2	+25°C	-	700	1000	ps
Rise Time (V_{OUT} = 2V Step)	A_V = -1	+25°C	-	0.82	-	ns
	A_V = +1	+25°C	-	1.06	-	ns
	A_V = +2	+25°C	-	1.00	-	ns
Overshoot (V_{OUT} = 0.5V Step, Input t_R/t_F = 200ps, Notes 1, 2, 3)	A_V = -1	+25°C	-	12	30	%
	A_V = +1	+25°C	-	45	65	%
	A_V = +2	+25°C	-	6	20	%
0.1% Settling (V_{OUT} = 2V to 0V, Note 2)		+25°C	-	11	-	ns
0.05% Settling (V_{OUT} = 2V to 0V)		+25°C	-	15	-	ns
Overdrive Recovery Time (V_{IN} = $5V_{P-P}$)		+25°C	-	8.5	-	ns
Differential Gain	A_V = +1, 3.58MHz, R_L = 150Ω	+25°C	-	0.03	-	%
	A_V = +2, 3.58MHz, R_L = 150Ω	+25°C	-	0.02	-	%
Differential Phase	A_V = +1, 3.58MHz, R_L = 150Ω	+25°C	-	0.05	-	Degrees
	A_V = +2, 3.58MHz, R_L = 150Ω	+25°C	-	0.04	-	Degrees

NOTES:

1. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
2. See Typical Performance Curves for more information.
3. Overshoot decreases as input transition times increase, especially for A_V = +1. Please refer to Performance Curves.

Die Characteristics

DIE DIMENSIONS:
63 x 44 x 19 ± 1mils
1600µm x 1130µm ±25.4µm

METALLIZATION:
Type: Metal 1: AlCu (2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu (2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC

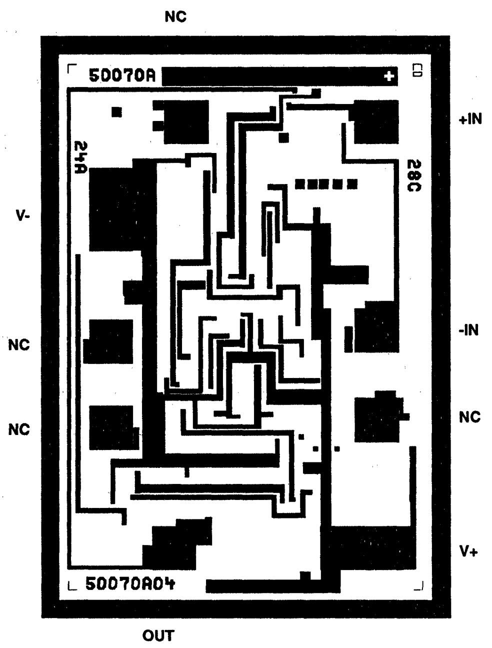
WORST CASE CURRENT DENSITY:
2.12 x 10^5 A/cm^2 at 50mA

TRANSISTOR COUNT: 52

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1112



Application Information

Closed Loop Gain Selection

The HFA1112 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1, while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT (PIN 3)	-INPUT (PIN 2)
-1	GND	Input
+1	Input	NC (Floating)
+2	Input	GND

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

For unity gain applications, care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. At higher frequencies this capacitance will tend to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This will cause excessive high frequency peaking and potentially other problems as well.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at $A_V = +1$, $R_S = 50\Omega$, $C_L = 30pF$, the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at $A_V = +1$, $R_S = 5\Omega$, $C_L = 340pF$.

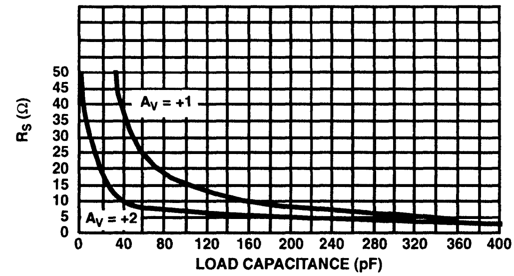


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1112 may be evaluated using the HFA11XX Evaluation Board, slightly modified as follows:

1. Remove the 500Ω feedback resistor (R2), and leave the connection open.
2. a. For $A_V = +1$ evaluation, remove the 500Ω gain setting resistor (R1), and leave pin 2 floating.
   b. For $A_V = +2$, replace the 500Ω gain setting resistor with a 0Ω resistor to GND.

The layout and modified schematic of the board are shown in Figure 2.

To order evaluation boards, please contact your local sales office.

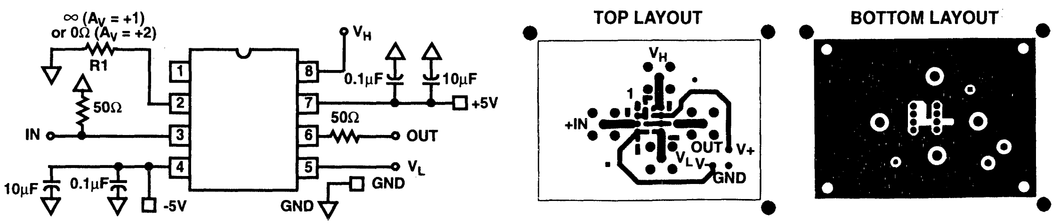


FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

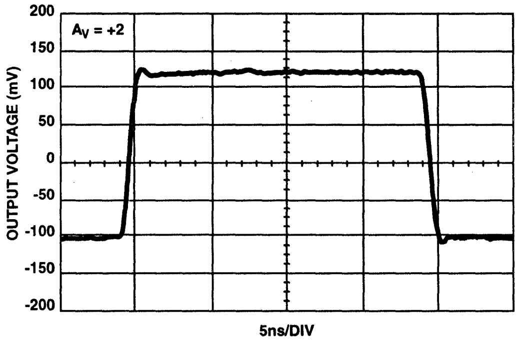


FIGURE 3. SMALL SIGNAL PULSE RESPONSE

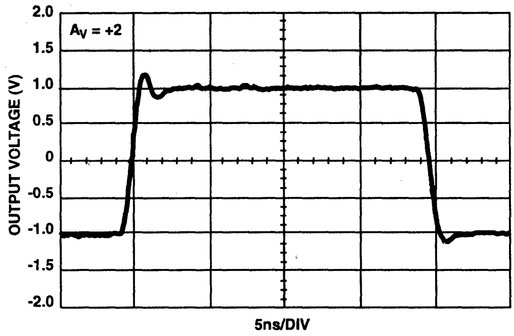


FIGURE 4. LARGE SIGNAL PULSE RESPONSE

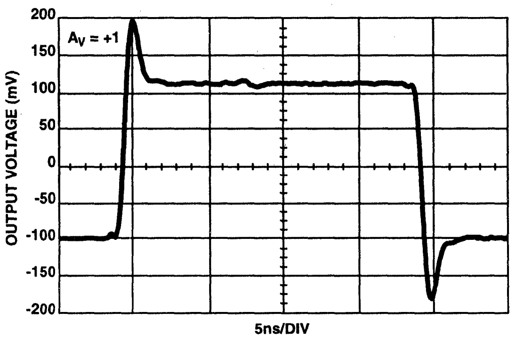


FIGURE 5. SMALL SIGNAL PULSE RESPONSE

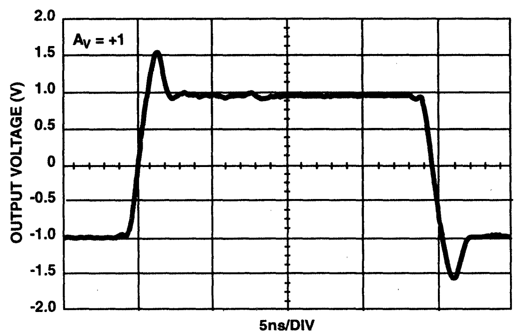


FIGURE 6. LARGE SIGNAL PULSE RESPONSE

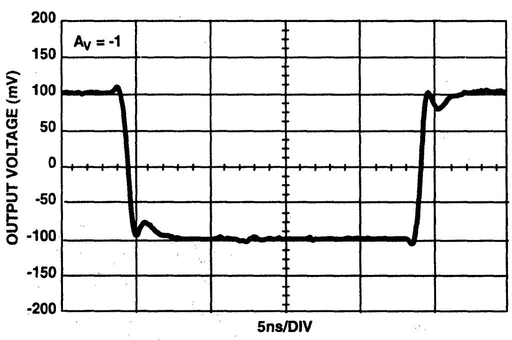


FIGURE 7. SMALL SIGNAL PULSE RESPONSE

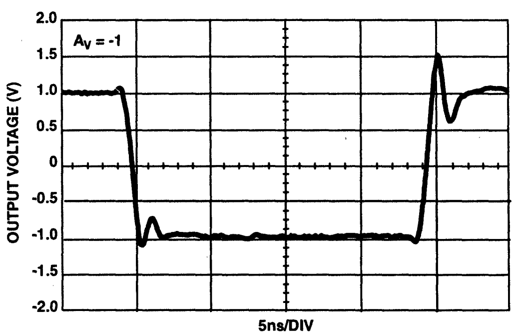


FIGURE 8. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

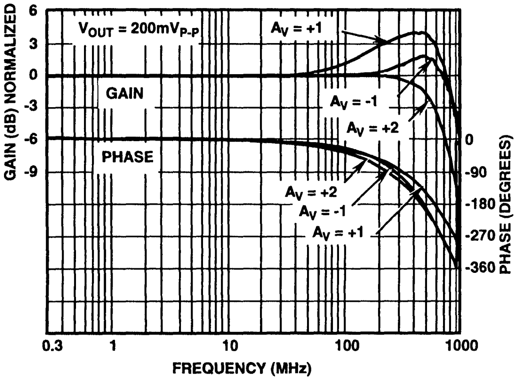


FIGURE 9. FREQUENCY RESPONSE

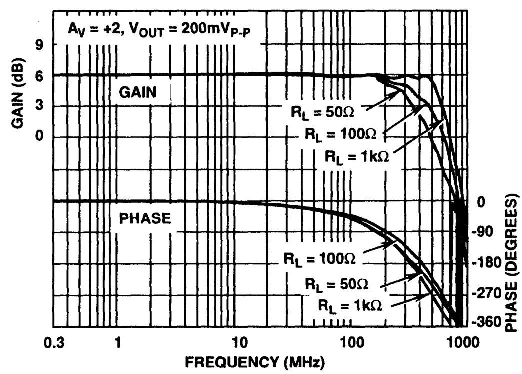


FIGURE 10. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

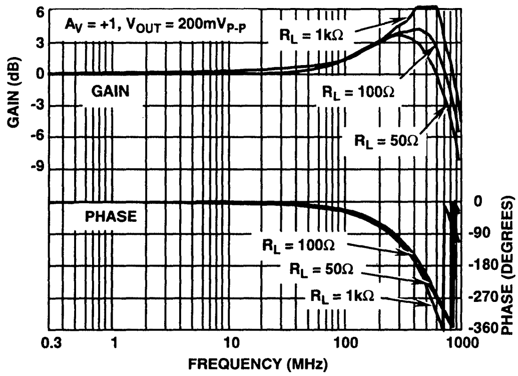


FIGURE 11. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

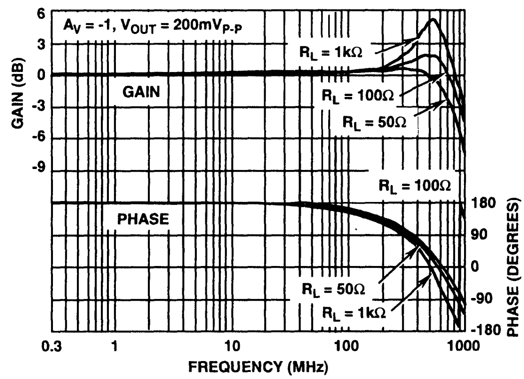


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

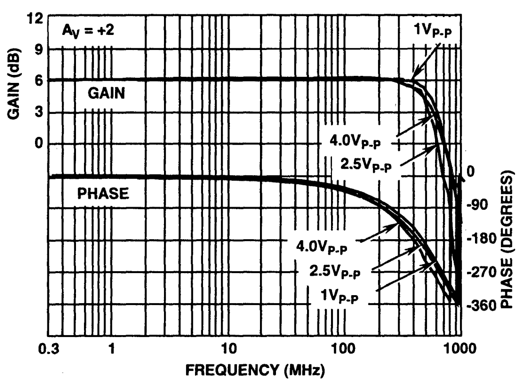


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

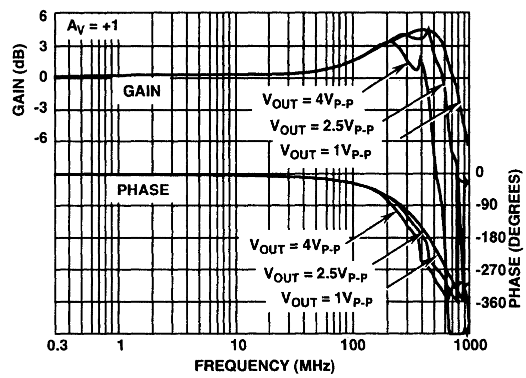


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

2

OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

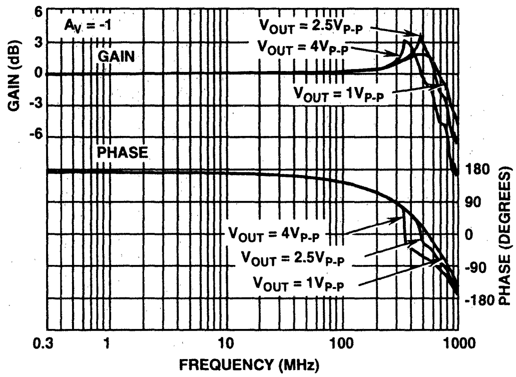


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

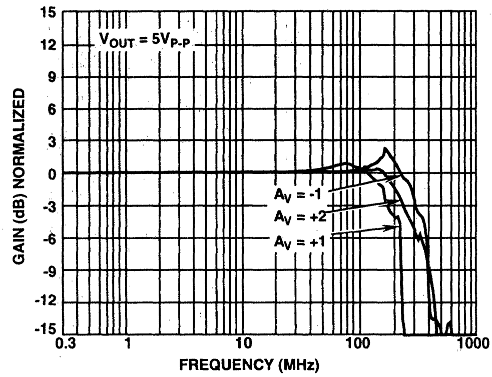


FIGURE 16. FULL POWER BANDWIDTH

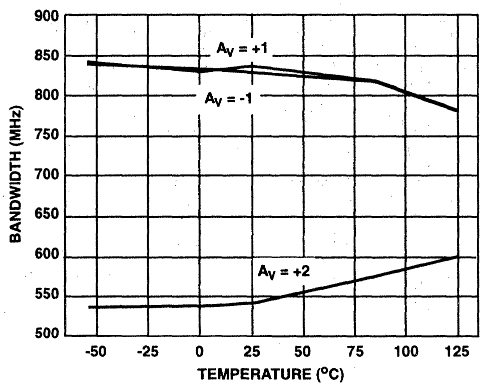


FIGURE 17. -3dB BANDWIDTH vs TEMPERATURE

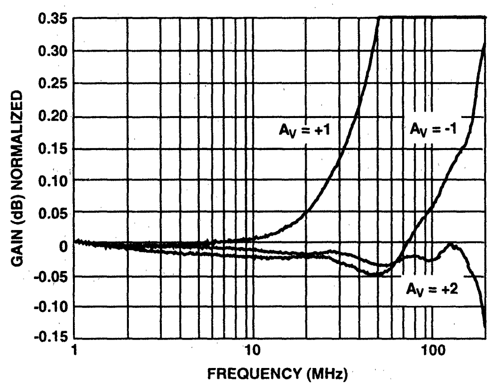


FIGURE 18. GAIN FLATNESS

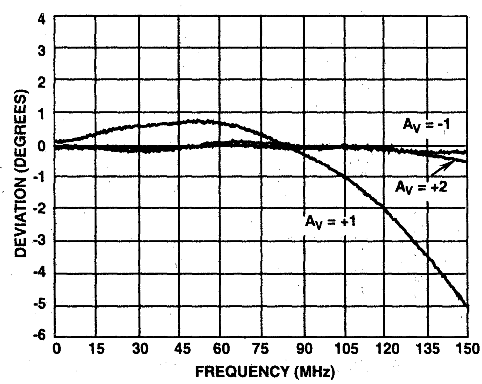


FIGURE 19. DEVIATION FROM LINEAR PHASE

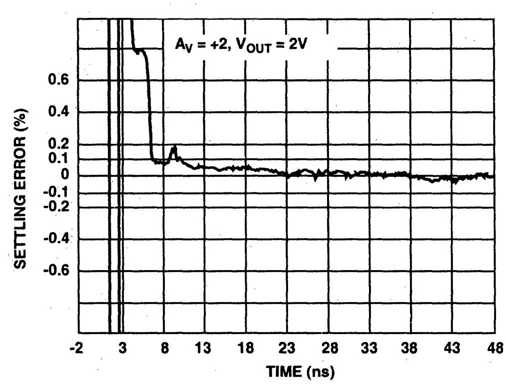


FIGURE 20. SETTLING RESPONSE

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

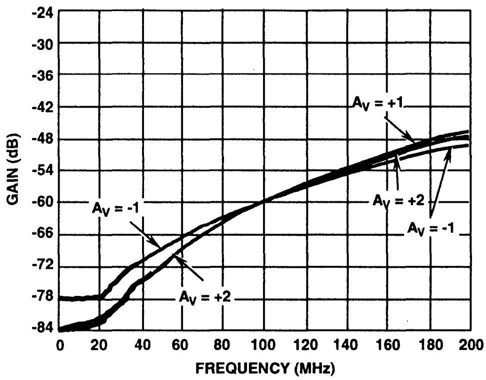


FIGURE 21. LOW FREQUENCY REVERSE ISOLATION (S_{12})

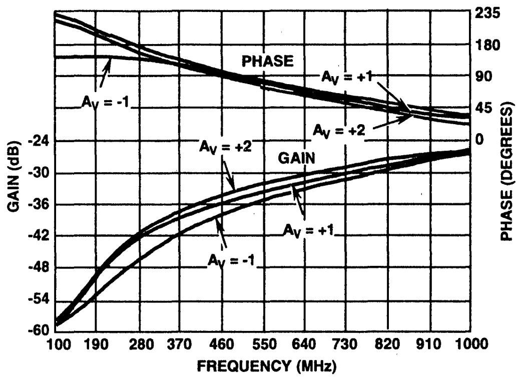


FIGURE 22. HIGH FREQUENCY REVERSE ISOLATION (S_{12})

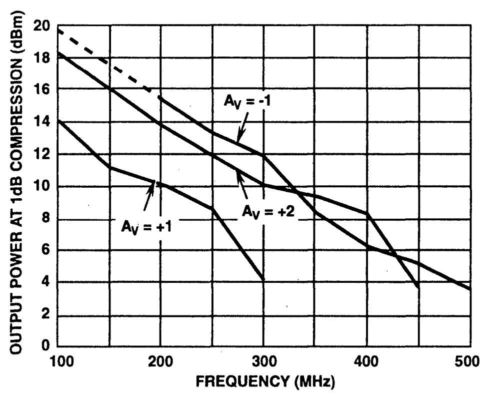


FIGURE 23. 1dB GAIN COMPRESSION vs FREQUENCY

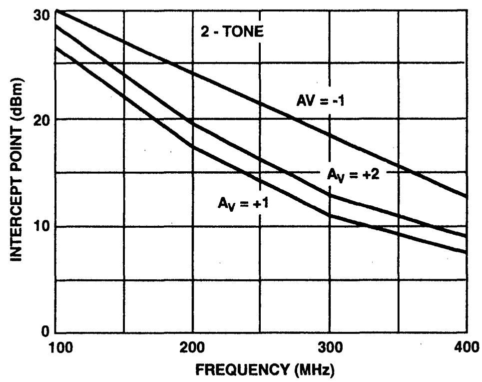


FIGURE 24. 3rd ORDER INTERMODULATION INTERCEPT vs FREQUENCY

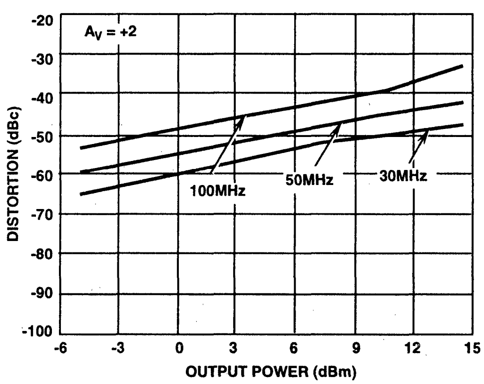


FIGURE 25. 2nd HARMONIC DISTORTION vs P_{OUT}

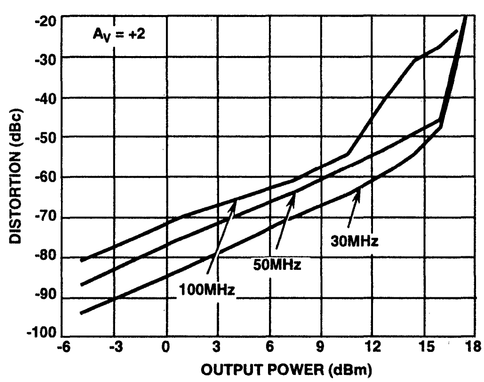


FIGURE 26. 3rd HARMONIC DISTORTION vs P_{OUT}

2
OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

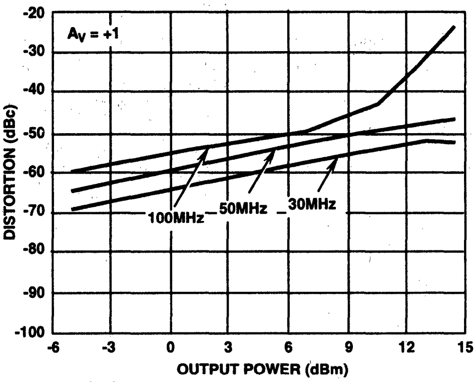


FIGURE 27. 2nd HARMONIC DISTORTION vs P_{OUT}

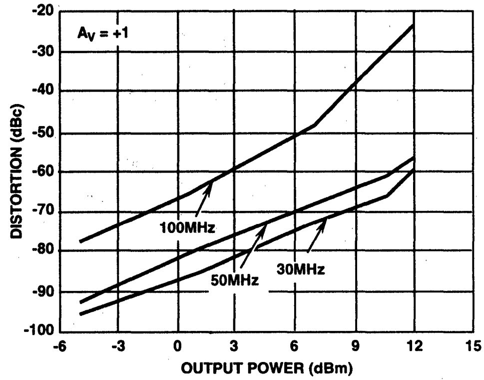


FIGURE 28. 3rd HARMONIC DISTORTION vs P_{OUT}

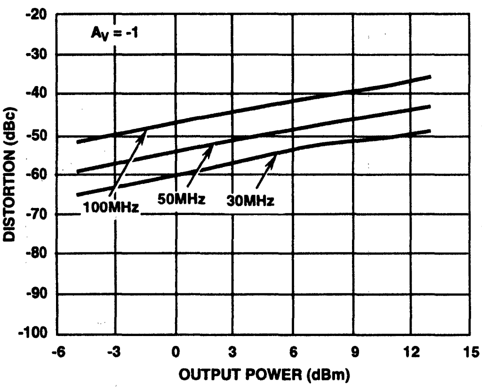


FIGURE 29. 2nd HARMONIC DISTORTION vs P_{OUT}

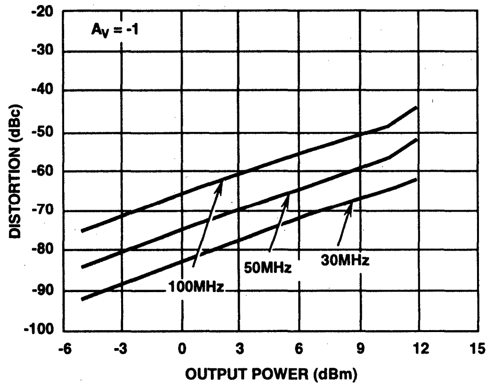


FIGURE 30. 3rd HARMONIC DISTORTION vs P_{OUT}

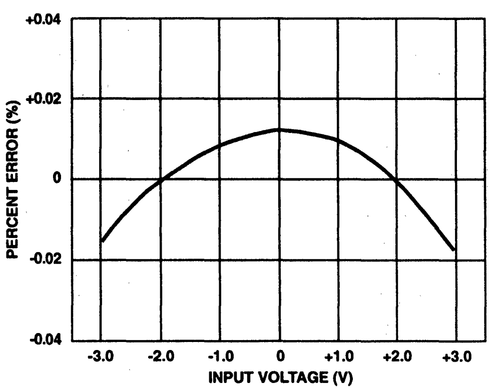


FIGURE 31. INTEGRAL LINEARITY ERROR

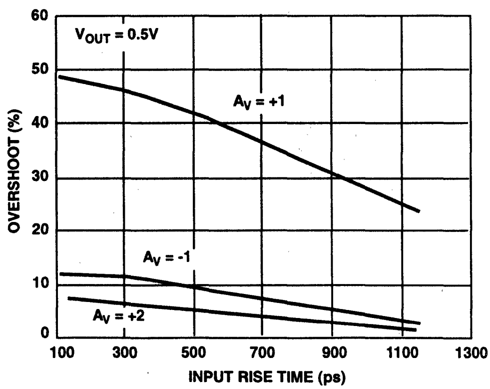


FIGURE 32. OVERSHOOT vs INPUT RISE TIME

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

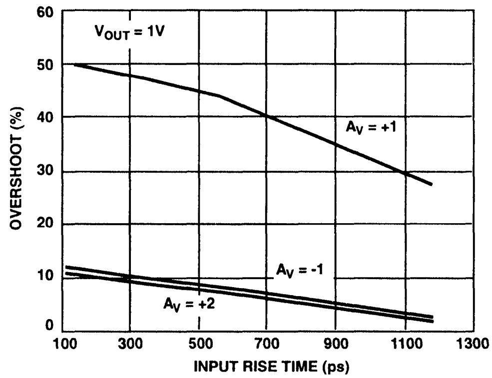


FIGURE 33. OVERSHOOT vs INPUT RISE TIME

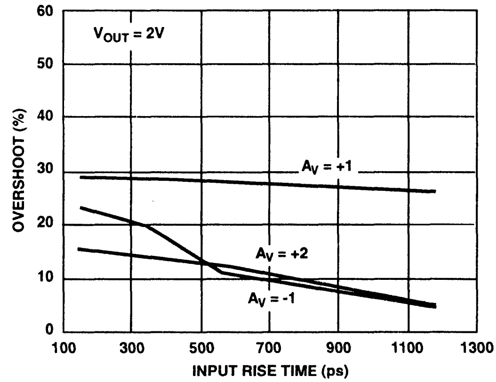


FIGURE 34. OVERSHOOT vs INPUT RISE TIME

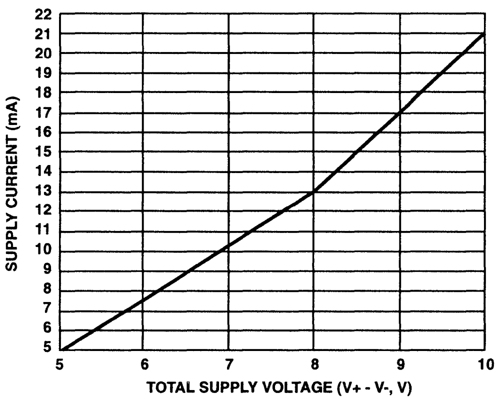


FIGURE 35. SUPPLY CURRENT vs SUPPLY VOLTAGE

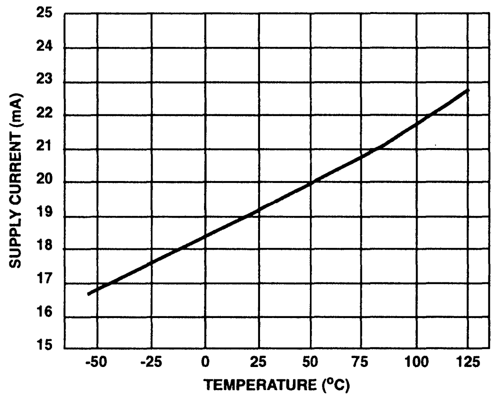


FIGURE 36. SUPPLY CURRENT vs TEMPERATURE

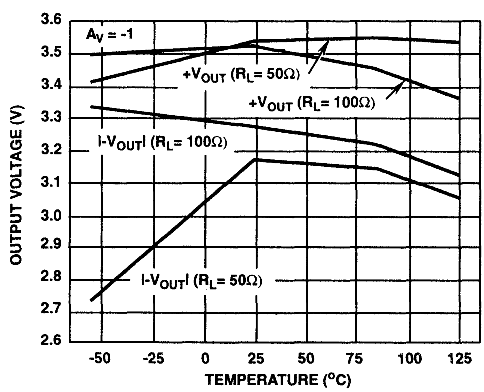


FIGURE 37. OUTPUT VOLTAGE vs TEMPERATURE

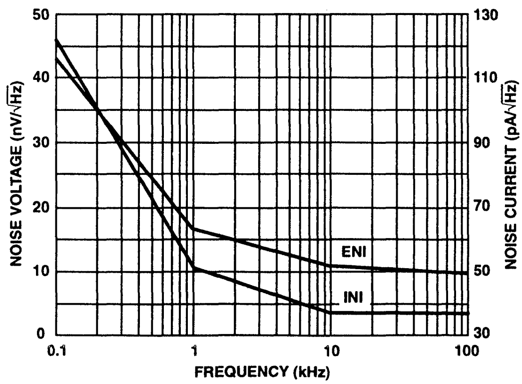


FIGURE 38. INPUT NOISE CHARACTERISTICS

HARRIS SEMICONDUCTOR

HFA1113

Output Limiting, Ultra High Speed, Programmable Gain, Buffer Amplifier

July 1995

Features

- User Programmable Output Voltage Limiting
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Wide -3dB Bandwidth 850MHz
- Excellent Gain Flatness (to 100MHz) .... ±0.07dB
- Low Differential Gain and Phase .... 0.02%/0.04 Deg.
- Low Distortion (HD3, 30MHz) .... -73dBc
- Very Fast Slew Rate 2400V/µs
- Fast Settling Time (0.1%) 13ns
- High Output Current 60mA
- Excellent Gain Accuracy................... 0.99V/V
- Overdrive Recovery......................... <1ns
- Standard Operational Amplifier Pinout

Applications

- RF/IF Processors
- Driving Flash A/D Converters
- High-Speed Communications
- Impedance Transformation
- Line Driving
- Video Switching and Routing
- Radar Systems
- Medical Imaging Systems

Description

The HFA1113 is a high speed Buffer featuring user programmable gain and output limiting coupled with ultra high speed performance. This buffer is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overload recovery times. The output limiting function allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The sub-nanosecond overdrive recovery time quickly returns the amplifier to linear operation following an overdrive condition.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components, as described in the "Application Information" section. Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

Component and composite video systems will also benefit from this buffer's performance, as indicated by the excellent gain flatness, and 0.02%/0.04 Deg. Differential Gain/Phase specifications ($R_L = 150\Omega$).

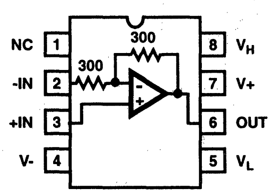
For Military product, refer to the HFA1113/883 data sheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1113MJ/883	-55°C to +125°C	8 Lead CerDIP
HFA1113IJ	-40°C to +85°C	8 Lead CerDIP
HFA1113IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1113IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

Pinout

HFA1113
(PDIP, CERDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
V_L	5	Lower Output Limit
OUT	6	Output
V+	7	Positive Supply
V_H	8	Upper Output Limit

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage .... V_{SUPPLY}
Differential Input Voltage 5V
Voltage at V_H or V_L Terminal .... (V+) + 2V to (V-) - 2V
Output Current (50% Duty Cycle) 60mA
Junction Temperature (Ceramic and Die) .... +175°C
Junction Temperature (Plastic Package) .... +150°C
Lead Temperature (Soldering 10s) .... +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HFA1113I .... $-40^oC \le T_A \le +85^oC$
Storage Temperature .... $-65^oC \le T_A \le +150^oC$

Thermal Resistance (°C/W)	θ_{JA}	θ_{JC}
CerDIP	116	36
Plastic DIP	130	N/A
SOIC	170	N/A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEMPERATURE	HFA1113I MIN	HFA1113I TYP	HFA1113I MAX	UNITS
INPUT CHARACTERISTICS					
Output Offset Voltage	+25°C	-	8	25	mV
	Full	-	-	35	mV
Output Offset Voltage Drift	Full	-	10	-	µV/°C
PSRR	+25°C	39	45	-	dB
	Full	35	-	-	dB
Input Voltage Noise (100kHz, Note 2)	+25°C	-	9	-	nV/√Hz
+Input Current Noise (100kHz, Note 2)	+25°C	-	37	-	pA/√Hz
Non-Inverting Input Bias Current	+25°C	-	25	40	µA
	Full	-	-	65	µA
Non-Inverting Input Resistance	+25°C	25	50	-	kΩ
Inverting Input Resistance (Note 1)	+25°C	240	300	360	Ω
Input Capacitance (Either Input)	+25°C	-	2	-	pF
Input Common Mode Range	Full	±2.5	±2.8	-	V
TRANSFER CHARACTERISTICS					
Gain ($A_V = +1$, $V_{IN} = +2V$)	+25°C	0.980	0.990	1.020	V/V
	Full	0.975	-	1.025	V/V
Gain ($A_V = +2$, $V_{IN} = +1V$)	+25°C	1.96	1.98	2.04	V/V
	Full	1.95	-	2.05	V/V
DC Non-Linearity ($A_V = +2$, ±2V Full Scale, Note 2)	+25°C	-	0.02	-	%
OUTPUT CHARACTERISTICS					
Output Voltage ($A_V = -1$, Note 2)	+25°C	±3.0	±3.3	-	V
	Full	±2.5	±3.0	-	V
Output Current ($R_L = 50\Omega$, Note 2)	+25°C, 85°C	50	60	-	mA
	-40°C	35	50	-	mA
DC Closed Loop Output Impedance	+25°C	-	0.3	-	Ω
POWER SUPPLY CHARACTERISTICS					
Supply Voltage Range	Full	±4.5	-	±5.5	V
Supply Current (Note 2)	+25°C	-	21	26	mA
	Full	-	-	33	mA

2

OPERATIONAL AMPLIFIERS

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMPERATURE	HFA1113I MIN	TYP	MAX	UNITS
AC CHARACTERISTICS						
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	450	800	-	MHz
	A_V = +1	+25°C	500	850	-	MHz
	A_V = +2	+25°C	350	550	-	MHz
Slew Rate (V_{OUT} = 5V_{P-P}, Note 1)	A_V = -1	+25°C	1500	2400	-	V/μs
	A_V = +1	+25°C	800	1500	-	V/μs
	A_V = +2	+25°C	1100	1900	-	V/μs
Full Power Bandwidth (V_{OUT} = 5V_{P-P}, Note 2)	A_V = -1	+25°C	-	300	-	MHz
	A_V = +1	+25°C	-	150	-	MHz
	A_V = +2	+25°C	-	220	-	MHz
Gain Flatness (to 30MHz, Notes 1, 2)	A_V = -1	+25°C	-	±0.02	-	dB
	A_V = +1	+25°C	-	±0.1	-	dB
	A_V = +2	+25°C	-	±0.015	±0.04	dB
Gain Flatness (to 50MHz, Notes 1, 2)	A_V = -1	+25°C	-	±0.05	-	dB
	A_V = +1	+25°C	-	±0.2	-	dB
	A_V = +2	+25°C	-	±0.036	±0.08	dB
Gain Flatness (to 100MHz, Notes 1, 2)	A_V = -1	+25°C	-	±0.10	-	dB
	A_V = +2	+25°C	-	±0.07	±0.22	dB
Linear Phase Deviation (to 100MHz, Note 2)	A_V = -1	+25°C	-	±0.13	-	Degrees
	A_V = +1	+25°C	-	±0.83	-	Degrees
	A_V = +2	+25°C	-	±0.05	-	Degrees
2nd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	-	-52	-	dBc
	A_V = +1	+25°C	-	-57	-	dBc
	A_V = +2	+25°C	-	-52	-45	dBc
3rd Harmonic Distortion (30MHz, V_{OUT} = 2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	-	-71	-	dBc
	A_V = +1	+25°C	-	-73	-	dBc
	A_V = +2	+25°C	-	-72	-65	dBc
2nd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	-	-47	-	dBc
	A_V = +1	+25°C	-	-53	-	dBc
	A_V = +2	+25°C	-	-47	-40	dBc
3rd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	-	-63	-	dBc
	A_V = +1	+25°C	-	-68	-	dBc
	A_V = +2	+25°C	-	-65	-55	dBc
2nd Harmonic Distortion (100MHz, V_{OUT} = 2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	-	-41	-	dBc
	A_V = +1	+25°C	-	-50	-	dBc
	A_V = +2	+25°C	-	-42	-35	dBc
3rd Harmonic Distortion (100MHz, V_{OUT} = 2V_{P-P}, Notes 1, 2)	A_V = -1	+25°C	-	-55	-	dBc
	A_V = +1	+25°C	-	-49	-	dBc
	A_V = +2	+25°C	-	-62	-45	dBc

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMPERATURE	HFA1113I MIN	HFA1113I TYP	HFA1113I MAX	UNITS
3rd Order Intercept (A_V = +2, Note 2)	100MHz	+25°C	-	28	-	dBm
	300MHz	+25°C	-	13	-	dBm
1dB Compression (A_V = +2, Note 2)	100MHz	+25°C	-	19	-	dBm
	300MHz	+25°C	-	12	-	dBm
Reverse Isolation (S_{12}, Note 2)	40MHz	+25°C	-	-70	-	dB
	100MHz	+25°C	-	-60	-	dB
	600MHz	+25°C	-	-32	-	dB
TRANSIENT CHARACTERISTICS						
Rise Time (V_{OUT} = 0.5V Step, Note 1)	A_V = -1	+25°C	-	500	800	ps
	A_V = +1	+25°C	-	480	750	ps
	A_V = +2	+25°C	-	700	1000	ps
Rise Time (V_{OUT} = 2V Step)	A_V = -1	+25°C	-	0.82	-	ns
	A_V = +1	+25°C	-	1.06	-	ns
	A_V = +2	+25°C	-	1.00	-	ns
Overshoot (V_{OUT} = 0.5V Step, Input t_R/t_F = 200ps, Notes 1, 2, 3)	A_V = -1	+25°C	-	12	30	%
	A_V = +1	+25°C	-	45	65	%
	A_V = +2	+25°C	-	6	20	%
0.1% Settling (V_{OUT} = 2V to 0V, Note 2)		+25°C	-	13	20	ns
0.05% Settling (V_{OUT} = 2V to 0V)		+25°C	-	20	33	ns
Differential Gain	A_V = +1, 3.58MHz, R_L = 150Ω	+25°C	-	0.03	-	%
	A_V = +2, 3.58MHz, R_L = 150Ω	+25°C	-	0.02	-	%
Differential Phase	A_V = +1, 3.58MHz, R_L = 150Ω	+25°C	-	0.05	-	Degrees
	A_V = +2, 3.58MHz, R_L = 150Ω	+25°C	-	0.04	-	Degrees
OUTPUT LIMITING CHARACTERISTICS A_V = +2, V_H = +1V, V_L = -1V, Unless Otherwise Specified.						
Clamp Accuracy (V_{IN} = ±1.6V, A_V = -1, Note 2)		+25°C	-	±100	±150	mV
		Full	-	-	±200	mV
Clamp Overshoot (V_{IN} = ±1V, Input t_R/t_F = 500ps)		+25°C	-	7	-	%
Overdrive Recovery Time (V_{IN} = ±1V, Note 2)		+25°C	-	0.75	1.5	ns
Negative Clamp Range		+25°C	-	-5.0 to +2.0	-	V
Positive Clamp Range		+25°C	-	-2.0 to +5.0	-	V
Clamp Input Bias Current (Note 2)		+25°C	-	50	200	μA
		Full	-	-	300	μA
Clamp Input Bandwidth (V_H or V_L = 100mV_{P-P}, Note 2)		+25°C	-	500	-	MHz

NOTES:

1. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
2. See Typical Performance Curves for more information.
3. Overshoot decreases as input transition times increase, especially for A_V = +1. Please refer to Typical Performance Curves.

Die Characteristics

DIE DIMENSIONS:
63 x 44 x 19 ± 1mils
1600μm x 1130μm ± 25.4μm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

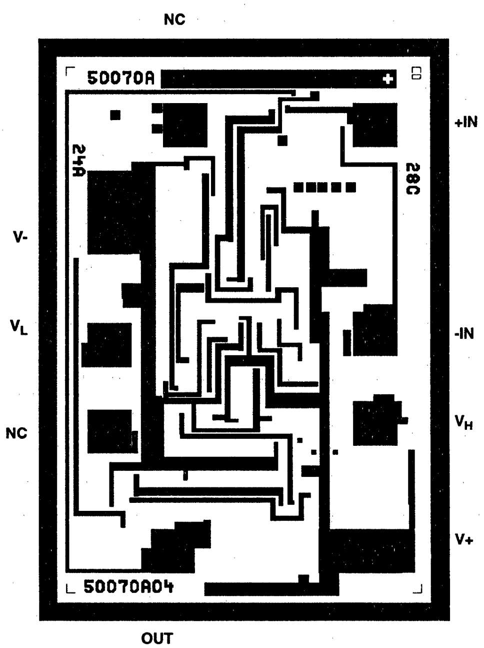
WORST CASE CURRENT DENSITY:
0.909×10^5 A/cm^2

TRANSISTOR COUNT: 52

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1113



Application Information

Closed Loop Gain Selection

The HFA1113 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±Inputs. Applying the input signal to +IN and floating -IN selects a gain of +1, while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT (PIN 3)	-INPUT (PIN 2)
-1	GND	Input
+1	Input	NC (Floating)
+2	Input	GND

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

For unity gain applications, care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. At higher frequencies this capacitance will tend to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This will cause excessive high frequency peaking and potentially other problems as well.

An example of a good high frequency layout is the Evaluation Board shown in Figure 3.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at $A_V = +1$, $R_S = 50\Omega$, $C_L = 30pF$, the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at $A_V = +1$, $R_S = 5\Omega$, $C_L = 340pF$.

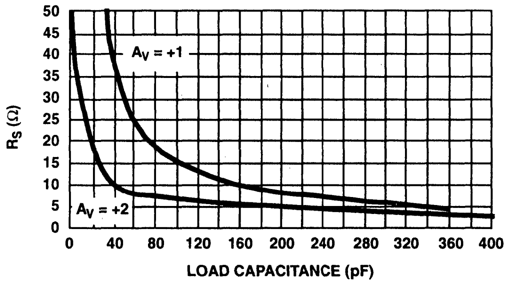


FIGURE 1. RECOMMENDED SERIES RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1113 may be evaluated using the HFA11XX Evaluation Board, slightly modified as follows:

1. Remove the 500Ω feedback resistor (R2), and leave the connection open.
2. a. For $A_V = +1$ evaluation, remove the 500Ω gain setting resistor (R1), and leave pin 2 floating.
   b. For $A_V = +2$, replace the 500Ω gain setting resistor with a 0Ω resistor to GND.

The modified schematic and layout of the board are shown in Figures 2 and 3.

To order evaluation boards, please contact your local sales office.

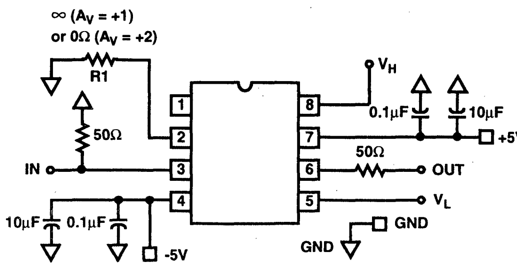


FIGURE 2. MODIFIED EVALUATION BOARD SCHEMATIC

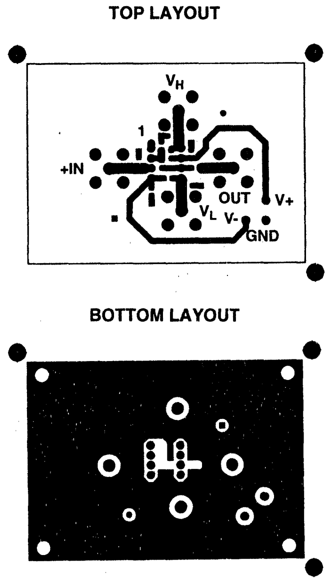


FIGURE 3. EVALUATION BOARD LAYOUT

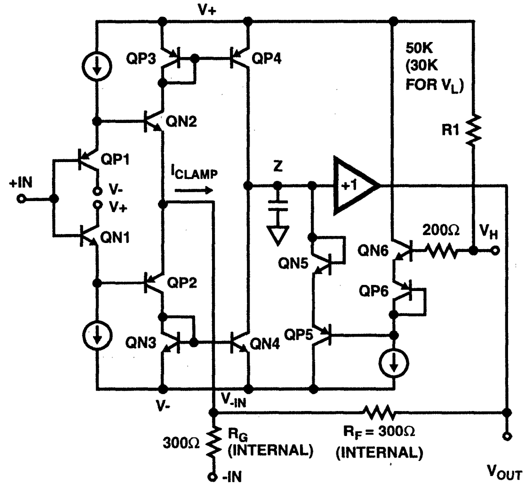


FIGURE 4. HFA1113 SIMPLIFIED V_H CLAMP CIRCUITRY

Clamp Operation

General

The HFA1113 features user programmable output clamps to limit output voltage excursions. Clamping action is obtained by applying voltages to the V_H and V_L terminals (pins 8 and 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower clamp level. If the amplifier tries to drive the output above V_H, or below V_L, the clamp circuitry limits the output voltage at V_H or V_L (± the clamp accuracy), respectively. The low input bias currents of the clamp pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or DACs.

Clamp Circuitry

Figure 4 shows a simplified schematic of the HFA1113 input stage, and the high clamp (V_H) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (QX1 - QX2) between the positive and negative inputs. This buffer forces -IN to track +IN, and sets up a slewing current of:

$(V_{-IN} - V_{OUT})/R_F + V_{-IN}/R_G$

This current is mirrored onto the high impedance node (Z) by QX3-QX4, where it is converted to a voltage and fed to the output via another unity gain buffer. If no clamping is utilized, the high impedance node may swing within the limits defined by QP4 and QN4. Note that when the output reaches it's quiescent value, the current flowing through -IN is reduced to only that small current ($-I_{BIAS}$) required to keep the output at the final voltage.

Tracing the path from V_H to Z illustrates the effect of the clamp voltage on the high impedance node. V_H decreases by $2V_{BE}$ (QN6 and QP6) to set up the base voltage on QP5.

QP5 begins to conduct whenever the high impedance node reaches a voltage equal to QP5's base voltage + $2V_{BE}$ (QP5 and QN5). Thus, QP5 clamps node Z whenever Z reaches V_H. R1 provides a pull-up network to ensure functionality with the clamp inputs floating. A similar description applies to the symmetrical low clamp circuitry controlled by V_L.

When the output is clamped, the negative input continues to source a slewing current (I_{CLAMP}) in an attempt to force the output to the quiescent voltage defined by the input. QP5 must sink this current while clamping, because the -IN current is always mirrored onto the high impedance node. The clamping current is calculated as:

$I_{CLAMP} = (V_{-IN} - V_{OUT\ CLAMPED})/300\Omega + V_{-IN}/R_G$.

As an example, a unity gain circuit with $V_{IN} = 2V$, and $V_H = 1V$, would have $I_{CLAMP} = (2V - 1V)/300\Omega + 2V/\infty = 3.33mA$ ($R_G = \infty$ because -IN is floated for unity gain applications). Note that I_{CC} will increase by I_{CLAMP} when the output is clamp limited.

Clamp Accuracy

The clamped output voltage will not be exactly equal to the voltage applied to V_H or V_L. Offset errors, mostly due to V_{BE} mismatches, necessitate a clamp accuracy parameter which is found in the device specifications. Clamp accuracy is a function of the clamping conditions. Referring again to Figure 4, it can be seen that one component of clamp accuracy is the V_{BE} mismatch between the QX6 transistors, and the QX5 transistors. If the transistors always ran at the same current level there would be no V_{BE} mismatch, and no contribution to the inaccuracy. The QX6 transistors are biased at a constant current, but as described earlier, the current through QX5 is equivalent to I_{CLAMP}. V_{BE} increases as I_{CLAMP} increases, causing the clamped output voltage to increase as well. I_{CLAMP} is a function of the overdrive level (A_{VCL} x V_{IN} - $V_{OUT\ CLAMPED}$), so clamp accuracy degrades as the overdrive increases. As an example, the specified accuracy of ±100mV ($A_V = -1$, $V_H = 1V$) for a 1.6X overdrive degrades to ±240mV for a 3X (200%) overdrive, as shown in Figure 43.

Consideration must also be given to the fact that the clamp voltages have an affect on amplifier linearity. The "Nonlinearity Near Clamp Voltage" curve, Figure 48, illustrates the impact of several clamp levels on linearity.

Clamp Range

Unlike some competitor devices, both V_H and V_L have usable ranges that cross 0V. While V_H must be more positive than V_L, both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HFA1113 could be limited to ECL output levels by setting V_H = -0.8V and V_L = -1.8V. V_H and V_L may be connected to the same voltage (GND for instance) but the result won't be in a DC output voltage from an AC input signal. A 150mV - 200mV AC signal will still be present at the output.

Recovery from Overdrive

The output voltage remains at the clamp level as long as the overdrive condition remains. When the input voltage drops below the overdrive level (V_{CLAMP}/A_{VCL}) the amplifier will return to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. The plots of "Unclamped Performance" and "Clamped Performance" (Figures 41 and 42) highlight the HFA1113's subnanosecond recovery time. The difference between the unclamped and clamped propagation delays is the overdrive recovery time. The appropriate propagation delays are 8.0ns for the unclamped pulse, and 8.8ns for the clamped (2X overdrive) pulse yielding an overdrive recovery time of 800ps. The measurement uses the 90% point of the output transition to ensure that linear operation has resumed. Note: The propagation delay illustrated is dominated by the fixturing. The delta shown is accurate, but the true HFA1113 propagation delay is 500ps.

Overdrive recovery time is also a function of the overdrive level. Figure 47 details the overdrive recovery time for various clamp and overdrive levels.

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

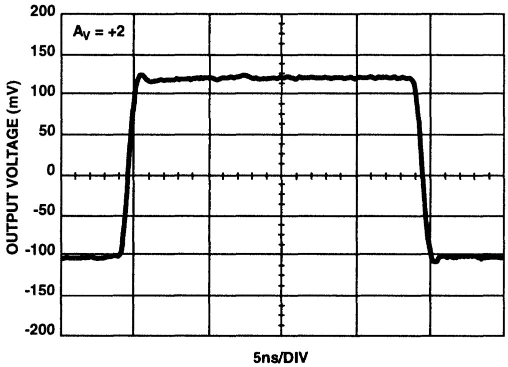


FIGURE 5. SMALL SIGNAL PULSE RESPONSE

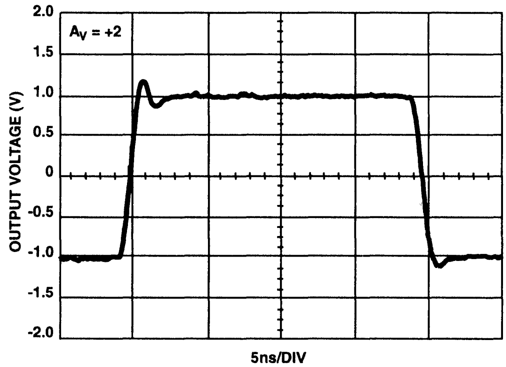


FIGURE 6. LARGE SIGNAL PULSE RESPONSE

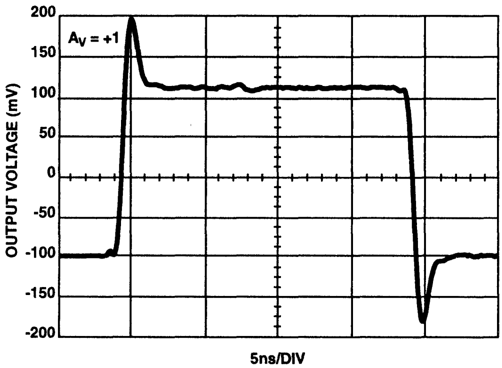


FIGURE 7. SMALL SIGNAL PULSE RESPONSE

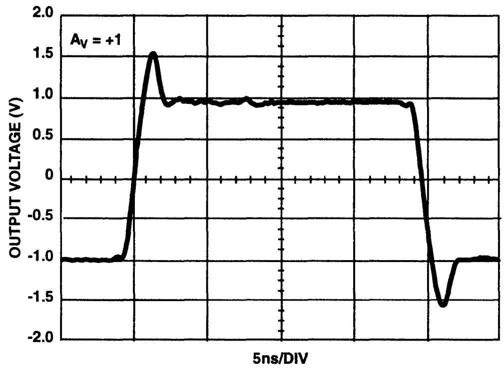


FIGURE 8. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

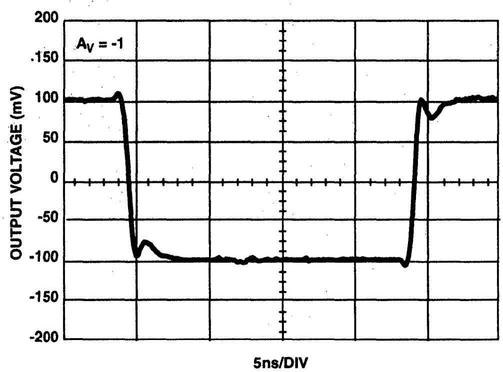


FIGURE 9. SMALL SIGNAL PULSE RESPONSE

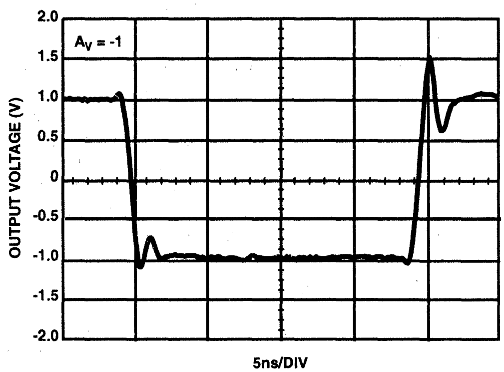


FIGURE 10. LARGE SIGNAL PULSE RESPONSE

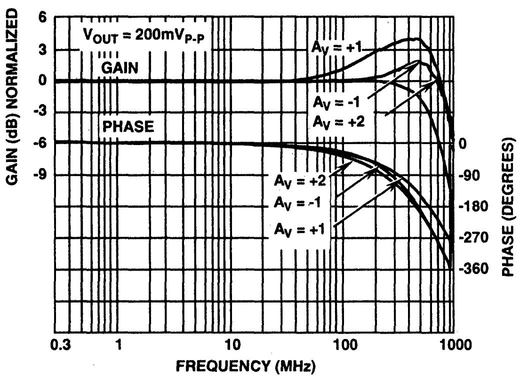


FIGURE 11. FREQUENCY RESPONSE

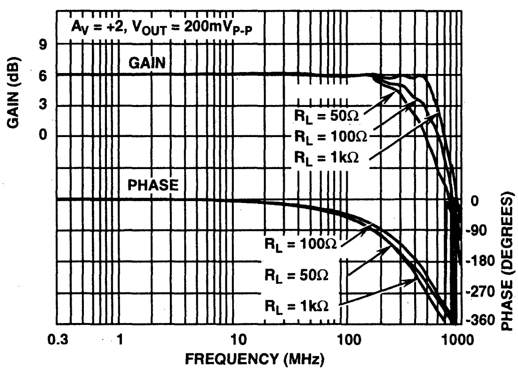


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

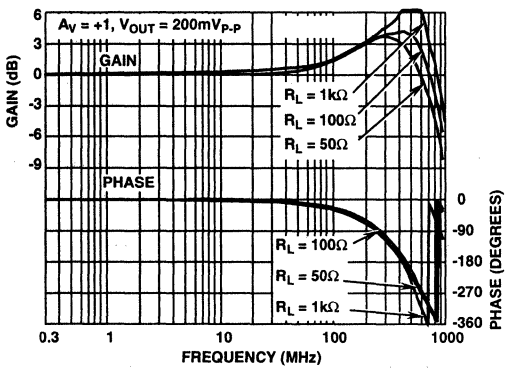


FIGURE 13. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

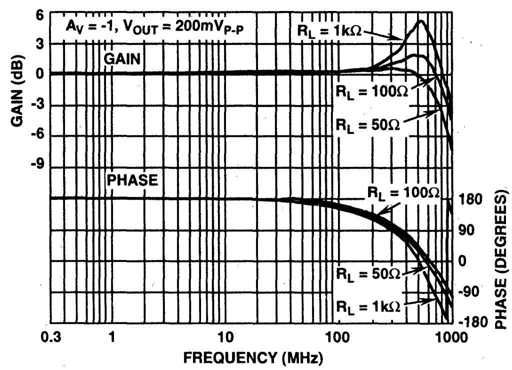


FIGURE 14. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

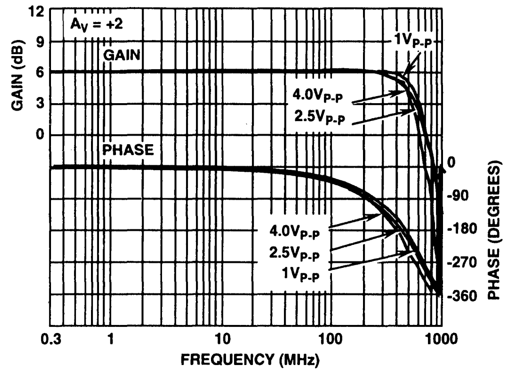


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

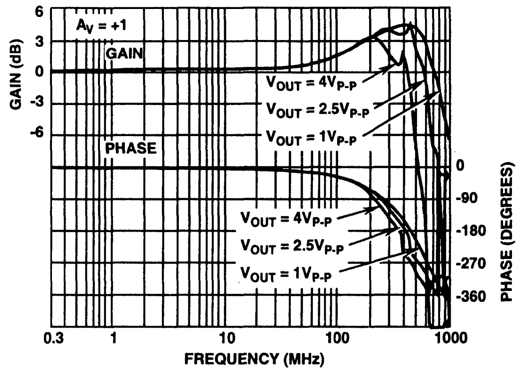


FIGURE 16. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

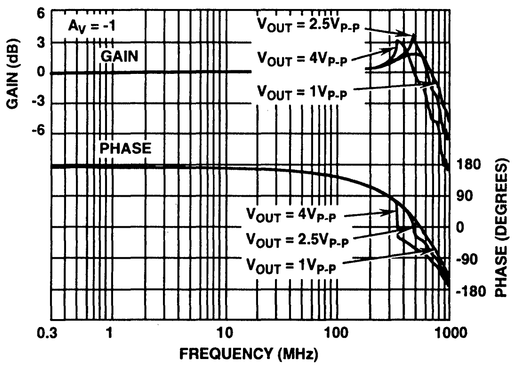


FIGURE 17. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

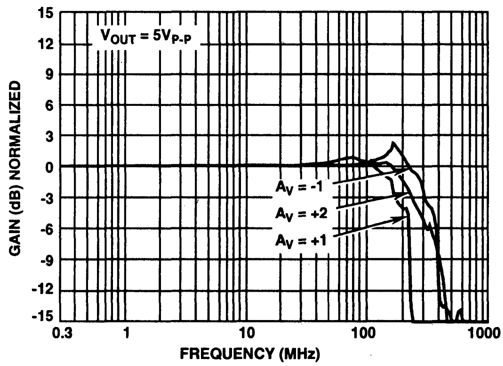


FIGURE 18. FULL POWER BANDWIDTH

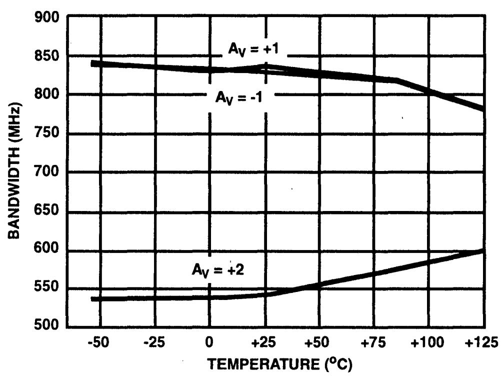


FIGURE 19. -3dB BANDWIDTH vs TEMPERATURE

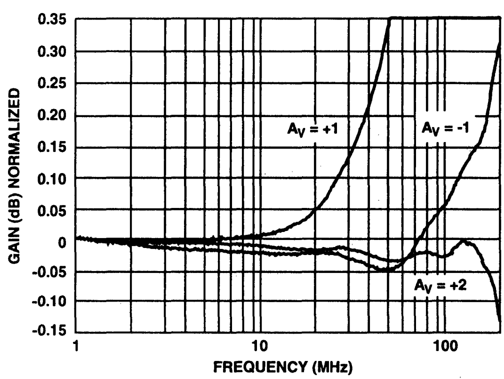


FIGURE 20. GAIN FLATNESS

2

OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

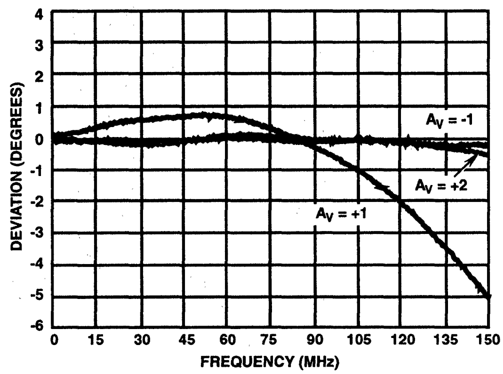


FIGURE 21. DEVIATION FROM LINEAR PHASE

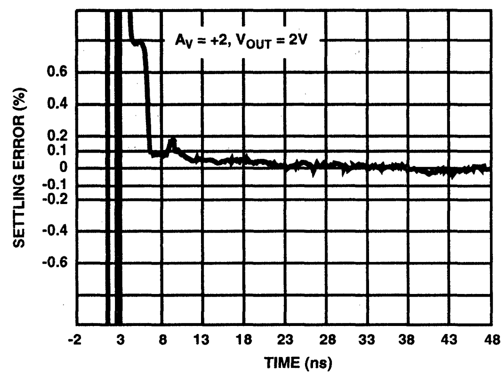


FIGURE 22. SETTLING RESPONSE

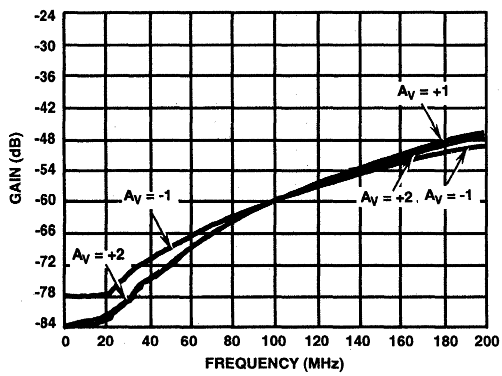


FIGURE 23. LOW FREQUENCY REVERSE ISOLATION (S_{12})

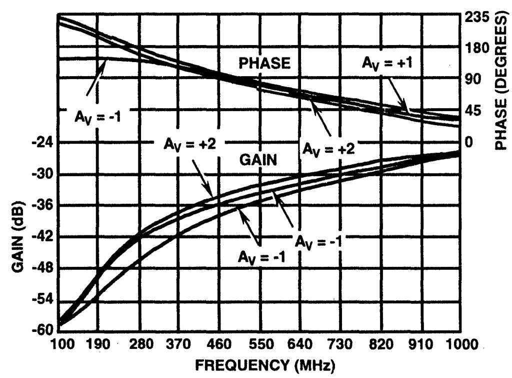


FIGURE 24. HIGH FREQUENCY REVERSE ISOLATION (S_{12})

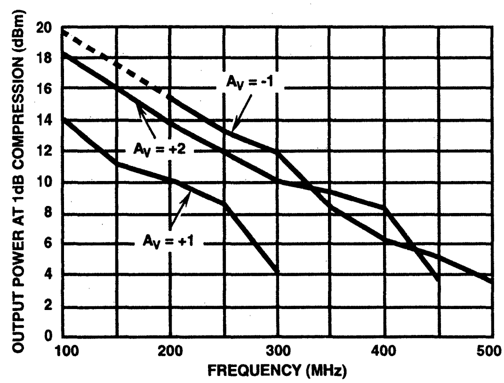


FIGURE 25. 1dB GAIN COMPRESSION vs FREQUENCY

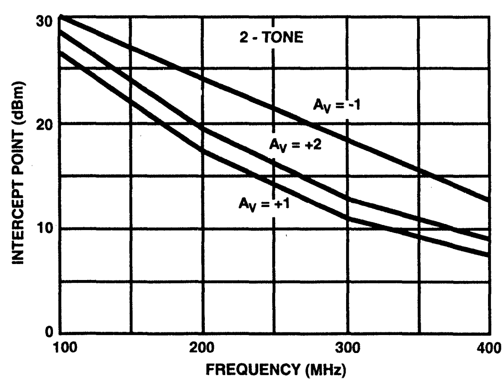


FIGURE 26. 3rd ORDER INTERMODULATION INTERCEPT vs FREQUENCY

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

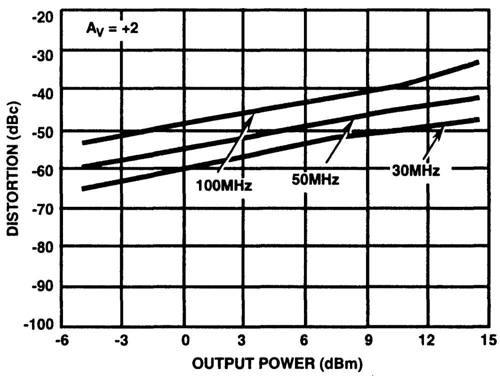


FIGURE 27. 2nd HARMONIC DISTORTION vs P_{OUT}

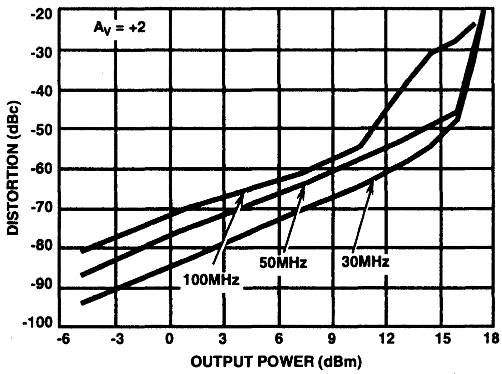


FIGURE 28. 3rd HARMONIC DISTORTION vs P_{OUT}

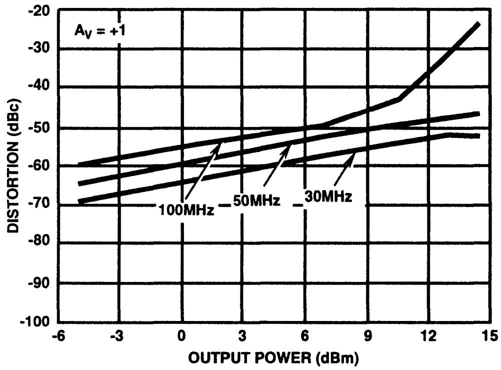


FIGURE 29. 2nd HARMONIC DISTORTION vs P_{OUT}

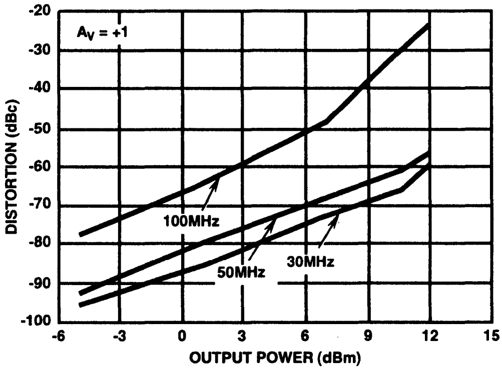


FIGURE 30. 3rd HARMONIC DISTORTION vs P_{OUT}

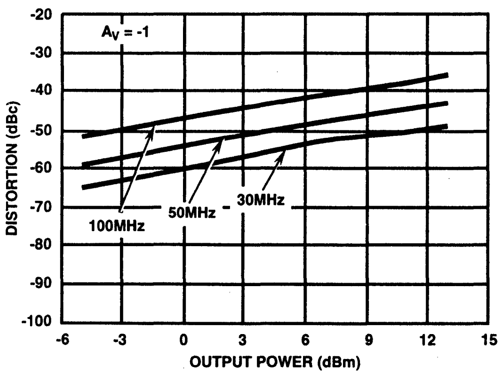


FIGURE 31. 2nd HARMONIC DISTORTION vs P_{OUT}

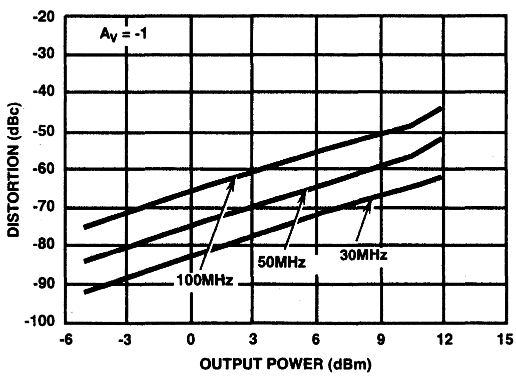


FIGURE 32. 3rd HARMONIC DISTORTION vs P_{OUT}

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

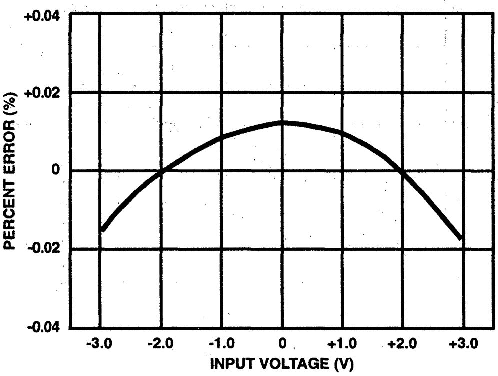


FIGURE 33. INTEGRAL LINEARITY ERROR

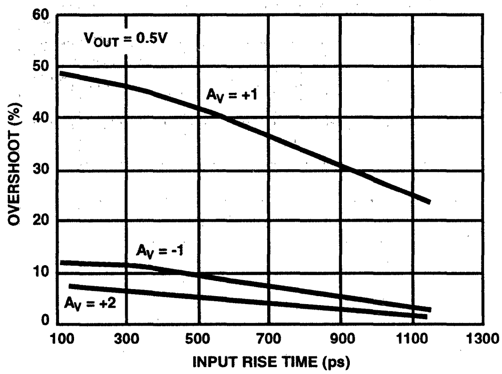


FIGURE 34. OVERSHOOT vs INPUT RISE TIME

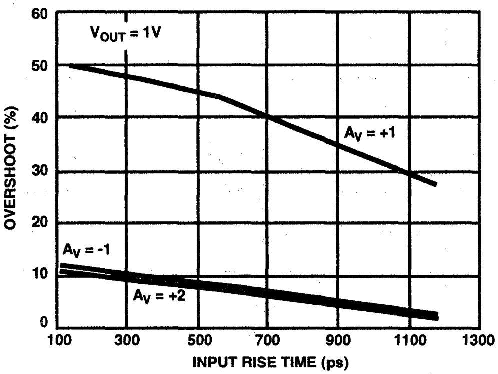


FIGURE 35. OVERSHOOT vs INPUT RISE TIME

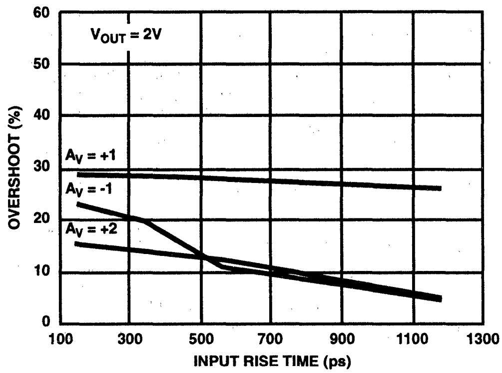


FIGURE 36. OVERSHOOT vs INPUT RISE TIME

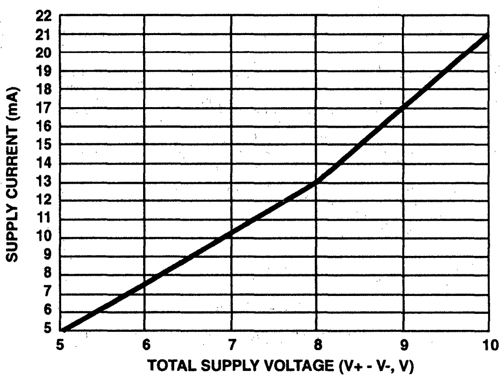


FIGURE 37. SUPPLY CURRENT vs SUPPLY VOLTAGE

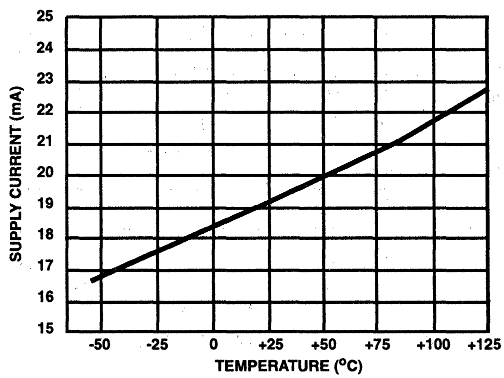


FIGURE 38. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

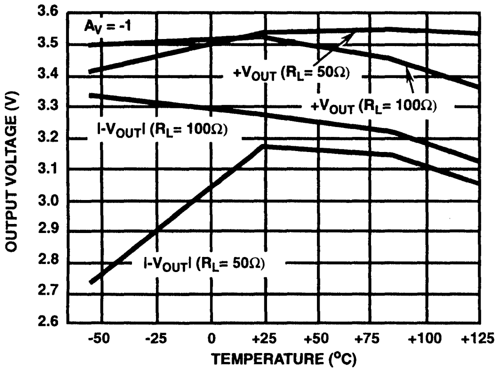


FIGURE 39. OUTPUT VOLTAGE vs TEMPERATURE

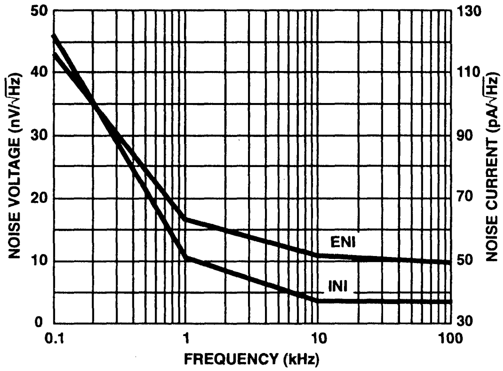


FIGURE 40. INPUT NOISE CHARACTERISTICS

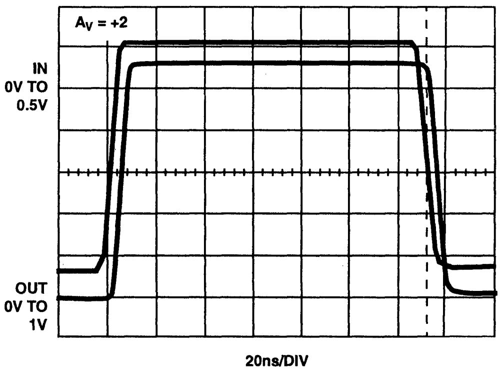


FIGURE 41. UNCLAMPED PERFORMANCE

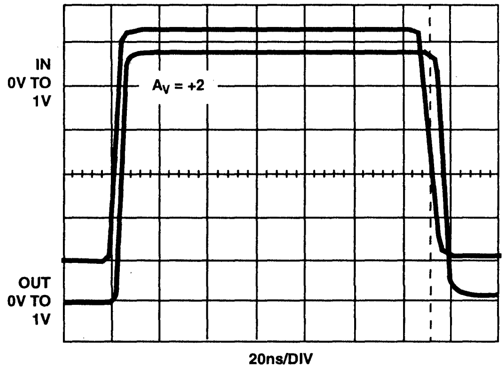


FIGURE 42. CLAMPED PERFORMANCE

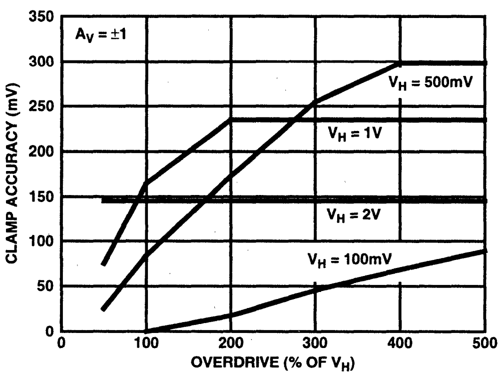


FIGURE 43. V_H CLAMP ACCURACY vs OVERDRIVE

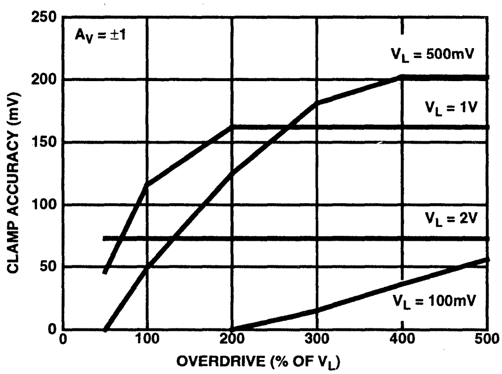


FIGURE 44. V_L CLAMP ACCURACY vs OVERDRIVE

2

OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

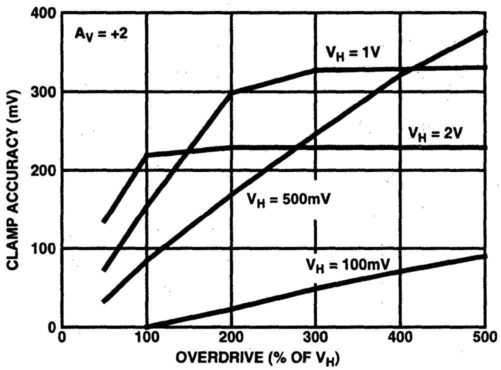


FIGURE 45. V_H CLAMP ACCURACY vs OVERDRIVE

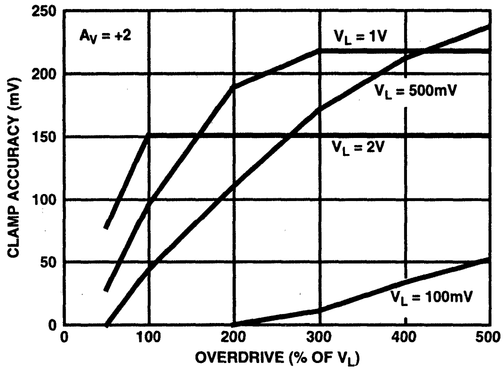


FIGURE 46. V_L CLAMP ACCURACY vs OVERDRIVE

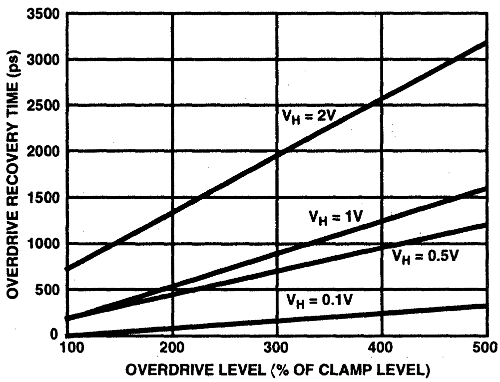


FIGURE 47. OVERDRIVE RECOVERY vs OVERDRIVE

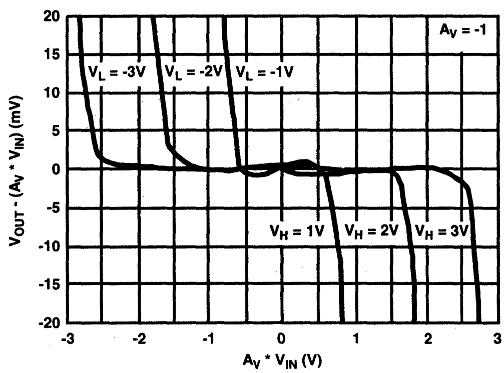


FIGURE 48. NON-LINEARITY NEAR CLAMP VOLTAGE

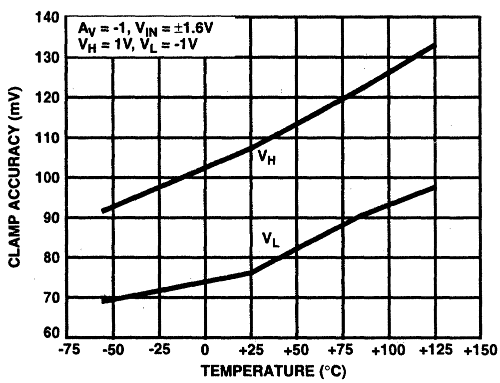


FIGURE 49. CLAMP ACCURACY vs TEMPERATURE

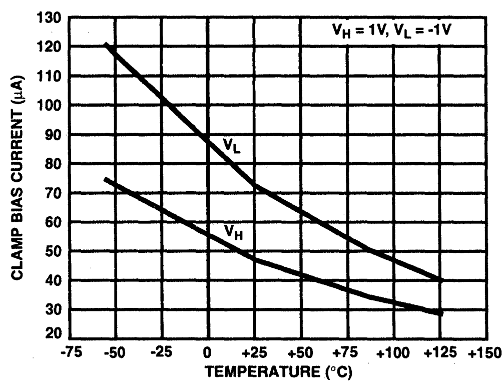


FIGURE 50. CLAMP BIAS CURRENT vs TEMPERATURE

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = +25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

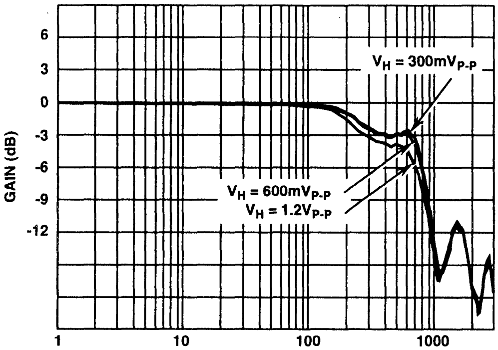


FIGURE 51. V_H CLAMP INPUT BANDWIDTH

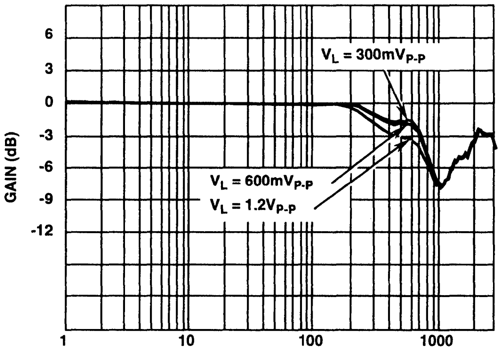


FIGURE 52. V_L CLAMP INPUT BANDWIDTH

HARRIS SEMICONDUCTOR

HFA1114

Ultra High Speed Programmable Gain Buffer Amplifier

July 1995

Features

- **Access to Summing Node Allows Circuit Customization**
- **User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors**
- **Wide -3dB Bandwidth 850MHz**
- **Very Fast Slew Rate 2400V/μs**
- **Fast Settling Time (0.1%) 11ns**
- **High Output Current 60mA**
- **Excellent Gain Accuracy.................. 0.99V/V**
- **Overdrive Recovery......................... <10ns**
- **Standard Operational Amplifier Pinout**

Applications

- **RF/IF Processors**
- **Driving Flash A/D Converters**
- **High Speed Communications**
- **Impedance Transformation**
- **Line Driving**
- **Video Switching and Routing**
- **Radar Systems**
- **Medical Imaging Systems**

Description

The HFA1114 is a closed loop Buffer featuring user programmable gain and ultra high speed performance. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, the HFA1114 offers a wide -3dB bandwidth of 850MHz, very fast slew rate, excellent gain flatness, low distortion and high output current.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" section. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date.

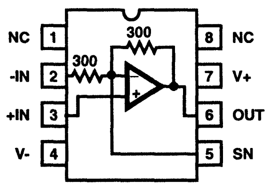
For applications requiring a standard buffer pinout, please refer to the HFA1110 datasheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1114IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1114IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

Pinout

HFA1114
(PDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1, 8	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
SN	5	Summing Node
OUT	6	Output
V+	7	Positive Supply

File Number **3151.2**

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
DC Input Voltage .... V_{SUPPLY}
Differential Input Voltage 5V
Output Current 60mA
Junction Temperature (Die Only) .... +175°C
Junction Temperature (Plastic Package) .... +150°C
Lead Temperature (Soldering 10s) .... +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HFA1114I .... $-40^oC \le T_A \le +85^oC$
Storage Temperature .... $-65^oC \le T_A \le +150^oC$
Thermal Resistance (°C/W) θ_{JA}
Plastic DIP Package 130
SOIC Package 170

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	TEMP.	HFA1114I MIN	HFA1114I TYP	HFA1114I MAX	UNITS
INPUT CHARACTERISTICS					
Output Offset Voltage	+25°C	-	8	25	mV
	Full	-	-	35	mV
Output Offset Voltage Drift	Full	-	10	-	µV/°C
PSRR	+25°C	39	45	-	dB
	Full	35	-	-	dB
Input Noise Voltage (100kHz)	+25°C	-	9	-	nV/√Hz
Non-Inverting Input Noise Current (100kHz)	+25°C	-	37	-	pA/√Hz
Non-Inverting Input Bias Current	+25°C	-	25	40	µA
	Full	-	-	65	µA
Non-Inverting Input Resistance	+25°C	25	50	-	kΩ
Inverting Input Resistance	+25°C	240	300	360	Ω
Input Capacitance (Either Input)	+25°C	-	2	-	pF
Input Common Mode Range	Full	±2.5	±2.8	-	V
TRANSFER CHARACTERISTICS					
Gain ($A_V = +1$, $V_{IN} = +2V$)	+25°C	0.980	0.990	1.02	V/V
	Full	0.975	-	1.025	V/V
Gain ($A_V = +2$, $V_{IN} = +1V$)	+25°C	1.96	1.98	2.04	V/V
	Full	1.95	-	2.05	V/V
DC Non-Linearity ($A_V = +2$, ±2V Full Scale)	+25°C	-	0.02	-	%
OUTPUT CHARACTERISTICS					
Output Voltage ($A_V = -1$)	+25°C	±3.0	±3.3	-	V
	Full	±2.5	±3.0	-	V
Output Current ($A_V = -1$, $R_L = 50\Omega$)	+25°C, +85°C	50	60	-	mA
	-40°C	35	50	-	mA
DC Closed Loop Output Impedance ($A_V = +2$)	+25°C	-	0.3	-	Ω
POWER SUPPLY CHARACTERISTICS					
Supply Voltage Range	Full	±4.5	-	±5.5	V
Supply Current	+25°C	-	21	26	mA
	Full	-	-	33	mA

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMP.	HFA1114I MIN	HFA1114I TYP	HFA1114I MAX	UNITS
AC CHARACTERISTICS						
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P})	A_V = -1	+25°C	-	800	-	MHz
	A_V = +1	+25°C	-	850	-	MHz
	A_V = +2	+25°C	-	550	-	MHz
Slew Rate (V_{OUT} = 5V_{P-P})	A_V = -1	+25°C	-	2400	-	V/µs
	A_V = +1	+25°C	-	1500	-	V/µs
	A_V = +2	+25°C	-	1900	-	V/µs
Full Power BW (5V_{P-P}, A_V = +2)		+25°C	-	220	-	MHz
Gain Flatness (to 30MHz, A_V = +2)		+25°C	-	±0.015	-	dB
Gain Flatness (to 100MHz, A_V = +2)		+25°C	-	±0.07	-	dB
2nd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P})		+25°C	-	-53	-	dBc
3rd Harmonic Distortion (50MHz, V_{OUT} = 2V_{P-P})		+25°C	-	-68	-	dBc
3rd Order Intercept (100MHz, A_V = +2)		+25°C	-	28	-	dBm
1dB Compression (100MHz, A_V = +2)		+25°C	-	19	-	dBm
Rise Time (V_{OUT} = 0.5V Step)	A_V = +2	+25°C	-	700	-	ps
	A_V = +1	+25°C	-	480	-	ps
Overshoot (V_{OUT} = 0.5V Step, A_V = +2)		+25°C	-	6	-	%
0.1% Settling (V_{OUT} = 2V to 0V)		+25°C	-	11	-	ns
0.05% Settling (V_{OUT} = 2V to 0V)		+25°C	-	15	-	ns
Overdrive Recovery Time		+25°C	-	8.5	-	ns
Differential Gain	A_V = +1, 3.58MHz, R_L = 150Ω	+25°C	-	0.03	-	%
	A_V = +2, 3.58MHz, R_L = 150Ω	+25°C	-	0.02	-	%
Differential Phase	A_V = +1, 3.58MHz, R_L = 150Ω	+25°C	-	0.05	-	Degrees
	A_V = +2, 3.58MHz, R_L = 150Ω	+25°C	-	0.04	-	Degrees

Application Information

Closed Loop Gain Selection

The HFA1114 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1, while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT (PIN 3)	-INPUT (PIN 2)
-1	GND	Input
+1	Input	NC (Floating)
+2	Input	GND

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

For unity gain applications, care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. At higher frequencies this capacitance will tend to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This will cause excessive high frequency peaking and potentially other problems as well.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 850MHz. By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at A_V = +1, R_S = 50Ω, C_L = 30pF, the overall bandwidth is limited to 300MHz, and bandwidth drops to 100MHz at A_V = +1, R_S = 5Ω, C_L = 340pF.

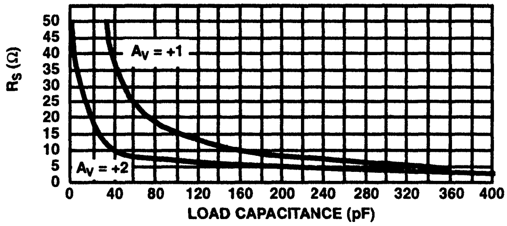


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs. LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1114 may be evaluated using the HFA11XX Evaluation Board, slightly modified as follows:

1. Remove the 500Ω feedback resistor (R2), and leave the connection open.
2. a. For A_V = +1 evaluation, remove the 500Ω gain setting resistor (R1), and leave pin 2 floating.
   b. For A_V = +2, replace the 500Ω gain setting resistor with a 0Ω resistor to GND.
3. Isolate Pin 5 from the stray board capacitance to minimize peaking and overshoot.

The layout and modified schematic of the board are shown in Figure 2.

To order evaluation boards, please contact your local sales office.

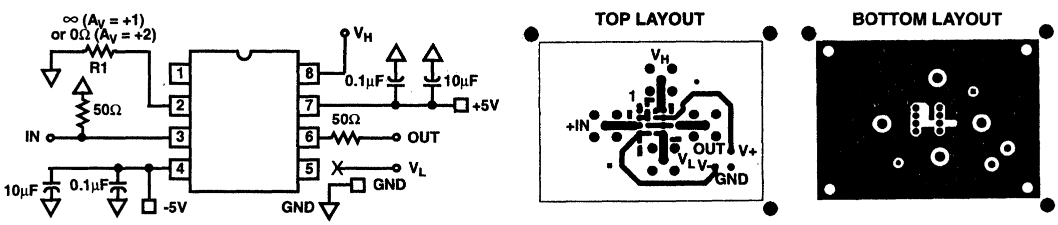


FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Die Characteristics

DIE DIMENSIONS:

63 x 44 x 19 ± 1mils
1600μm x 1130μm x 483μm ± 25.4μm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:

Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

DIE ATTACH:

Material: Epoxy - Plastic DIP and SOIC
Gold Eutectic - Ceramic DIP

WORST CASE CURRENT DENSITY:

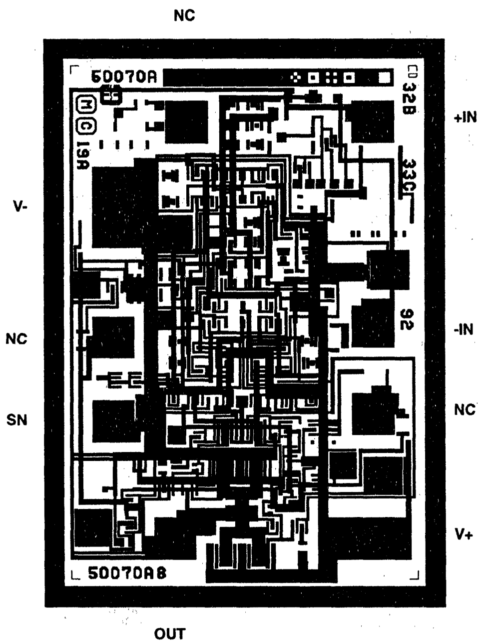
2.12×10^5 A/cm^2 at 50mA

TRANSISTOR COUNT: 52

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1114



HFA1115

High-Speed, Low Power, Output Limiting, Closed Loop Buffer Amplifier

July 1995

Features

- User Programmable Output Voltage Limiting
- High Input Impedance 1MΩ
- Differential Gain 0.02%
- Differential Phase. . . . . 0.03Deg.
- Wide -3dB Bandwidth (A_V = +2) 225MHz
- Very Fast Slew Rate (A_V = -1) 1135V/µs
- Low Supply Current. 7.1mA
- High Output Current 60mA
- Excellent Gain Accuracy. 0.99V/V
- User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors
- Fast Overdrive Recovery. . . . . <1ns
- Standard Operational Amplifier Pinout

Applications

- Flash A/D Drivers
- Video Cable Drivers
- High Resolution Monitors
- Professional Video Processing
- Medical Imaging
- Video Digitizing Boards/Systems
- Battery Powered Communications

Description

The HFA1115 is a high speed closed loop Buffer featuring both user programmable gain and output limiting. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, the HFA1115 also offers a wide -3dB bandwidth of 225MHz, very fast slew rate, excellent gain flatness and high output current.

This buffer is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overload recovery times. The limiting function allows the designer to set the maximum positive and negative output levels, thereby protecting later stages from damage or input saturation. The HFA1115 also allows for voltage gains of +2, +1, and -1, without the use of external resistors. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" text. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

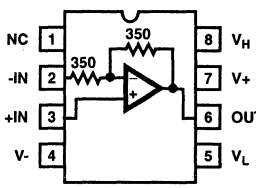
Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path, should a higher closed loop gain be needed at a future date. For Military product, refer to the HFA1115/883 data sheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1115IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1115IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

Pinout

HFA1115
(PDIP, SOIC)
TOP VIEW



Pin Descriptions

NAME	PIN NUMBER	DESCRIPTION
NC	1	No Connection
-IN	2	Inverting Input
+IN	3	Non-Inverting Input
V-	4	Negative Supply
V_L	5	Lower Output Limit
OUT	6	Output
V+	7	Positive Supply
V_H	8	Upper Output Limit

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . V_{SUPPLY}
Output Current (Note 1) . . . . Short Circuit Protected
Junction Temperature (Die Only) . . . . +175°C
Junction Temperature (Plastic Package) . . . . +150°C
ESD Rating. . . . . TBD
Lead Temperature (Soldering 10s). . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range . . . . $-40°C \leq T_A \leq +85°C$
Storage Temperature Range. . . . . $-65°C \leq T_A \leq +150°C$
Thermal Package Characteristics (°C/W) θ_{JA}
Plastic DIP. 130
SOIC 170

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER		(NOTE 2) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Output Offset Voltage		A	+25°C	-	2	10	mV
		A	Full	-	3	15	mV
Average Output Offset Voltage Drift		B	Full	-	22	70	µV/°C
Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	+25°C	42	45	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	40	44	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	40	45	-	dB
Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	+25°C	45	49	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	+85°C	43	48	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40°C	43	48	-	dB
Non-Inverting Input Bias Current		A	+25°C	-	1	15	µA
		A	Full	-	3	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	30	80	nA/°C
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	+25°C	0.8	1.1	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	0.5	1.4	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	0.5	1.3	-	MΩ
Inverting Input Resistance		C	+25°C	280	350	420	Ω
Input Capacitance (Either Input)		C	+25°C	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR and $+R_{IN}$ Tests)		A	+25°C, +85°C	±1.8	±2.4	-	V
		A	-40°C	±1.2	±1.7	-	V
Input Noise Voltage Density (f = 100kHz)		B	+25°C	-	7	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current Density (f = 100kHz)		B	+25°C	-	3.6	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS							
Gain	$A_V = -1$	A	+25°C	-0.98	-0.996	-1.02	V/V
		A	Full	-0.975	-1.000	-1.025	V/V
	$A_V = +1$	A	+25°C	0.98	0.992	1.02	V/V
		A	Full	0.975	0.993	1.025	V/V
	$A_V = +2$	A	+25°C	1.96	1.988	2.04	V/V
		A	Full	1.95	1.990	2.05	V/V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 2) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
AC CHARACTERISTICS							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P})	A_V = -1	B	+25°C	-	225	-	MHz
	A_V = +1, +R_S = 620Ω	B	+25°C	-	170	-	MHz
	A_V = +2	B	+25°C	-	225	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2/-1, 4V_{P-P} at A_V = +1)	A_V = -1	B	+25°C	-	157	-	MHz
	A_V = +1, +R_S = 620Ω	B	+25°C	-	140	-	MHz
	A_V = +2	B	+25°C	-	125	-	MHz
Gain Flatness (to 25MHz, V_{OUT} = 0.2V_{P-P})	A_V = +1, +R_S = 620Ω	B	+25°C	-	±0.1	-	dB
	A_V = +2	B	+25°C	-	±0.04	-	dB
Gain Flatness (to 50MHz, V_{OUT} = 0.2V_{P-P})	A_V = +1, +R_S = 620Ω	B	+25°C	-	±0.25	-	dB
	A_V = +2	B	+25°C	-	±0.1	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing (A_V = -1)		A	+25°C	±3.0	±3.2	-	V
		A	Full	±2.8	±3.0	-	V
Output Current (A_V = -1, R_L = 50Ω)		A	+25°C, +85°C	50	55	-	mA
		A	-40°C	28	42	-	mA
Output Short Circuit Current		B	+25°C	-	90	-	mA
DC Closed Loop Output Impedance (A_V = +2)		B	+25°C	-	0.07	-	Ω
Second Harmonic Distortion (A_V = +2, V_{OUT} = 2V_{P-P})	10MHz	B	+25°C	-	-50	-	dBc
	20MHz	B	+25°C	-	-45	-	dBc
Third Harmonic Distortion (A_V = +2, V_{OUT} = 2V_{P-P})	10MHz	B	+25°C	-	-50	-	dBc
	20MHz	B	+25°C	-	-45	-	dBc
TRANSIENT RESPONSE A_V = +2, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = 0.5V_{P-P})	Rise Time	B	+25°C	-	1.7	-	ns
	Fall Time	B	+25°C	-	1.9	-	ns
Overshoot (V_{OUT} = 0.5V_{P-P}, V_{IN} t_{RISE} = 2.5ns)	+OS	B	+25°C	-	0	-	%
	-OS	B	+25°C	-	0	-	%
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = -1)	+SR	B	+25°C	-	1660	-	V/µs
	-SR	B	+25°C	-	1135	-	V/µs
Slew Rate (V_{OUT} = 4V_{P-P}, A_V = +1, +R_S = 620Ω)	+SR	B	+25°C	-	1125	-	V/µs
	-SR	B	+25°C	-	800	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = +2)	+SR	B	+25°C	-	1265	-	V/µs
	-SR	B	+25°C	-	870	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step)	To 0.1%	B	+25°C	-	15	-	ns
	To 0.05%	B	+25°C	-	20	-	ns
	To 0.02%	B	+25°C	-	30	-	ns

Electrical Specifications $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 2) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
VIDEO CHARACTERISTICS						
Differential Gain (f = 3.58MHz, $A_V = +2$, $R_L = 150\Omega$)	B	+25°C	-	0.02	-	%
Differential Phase (f = 3.58MHz, $A_V = +2$, $R_L = 150\Omega$)	B	+25°C	-	0.03	-	Degrees
POWER SUPPLY CHARACTERISTICS						
Power Supply Range	C	+25°C	4.5	-	5.5	±V
Power Supply Current	A	+25°C	6.6	6.9	7.1	mA
	A	Full	-	7.1	7.3	mA
Non-Inverting Input Bias Current Power Supply Sensitivity ($\Delta V_{PS} = \pm 1.25V$)	A	+25°C	-	0.5	1	µA/V
	A	Full	-	-	3	µA/V
OUTPUT LIMITING CHARACTERISTICS $A_V = +2$, $V_H = +1V$, $V_L = -1V$, Unless Otherwise Specified						
Clamp Accuracy ($V_{IN} = \pm 1.6V$, $A_V = -1$)	A	Full	-125	-70	125	mV
Overdrive Recovery Time ($V_{IN} = \pm 1V$)	B	+25°C	-	0.8	-	ns
Negative Clamp Range	B	+25°C		-5.0 to +2.0		V
Positive Clamp Range	B	+25°C		-2.0 to +5.0		V
Clamp Input Bias Current	A	Full	-	85	200	µA
Clamp Input Bandwidth	C	+25°C	-	100	-	MHz

NOTES:
1. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 30mA for maximum reliability.
2. Test Level: A. Production Tested.; B. Guaranteed Limit or Typical Based on Characterization.; C. Design Typical for Information Only.

Die Characteristics

DIE DIMENSIONS:
59 x 58.2 x 19 ± 1mils
1500μm x 1480μm ± 25.4μm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

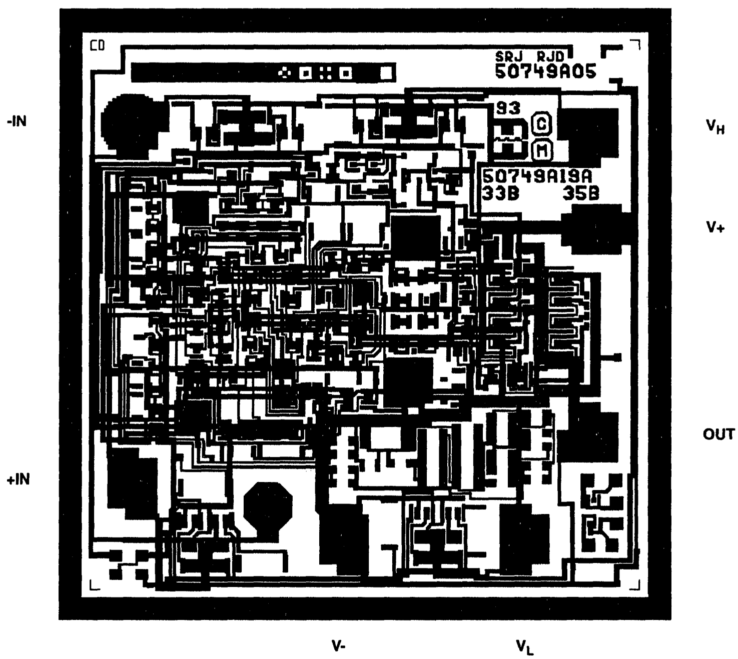
DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC

TRANSISTOR COUNT: 89

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1115



Application Information

Closed Loop Gain Selection

The HFA1115 features a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1 (see next section for layout caveats), while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT (PIN 3)	-INPUT (PIN 2)
-1	GND	Input
+1	Input	NC (Floating)
+2	Input	GND

Unity Gain Considerations

Unity gain selection is accomplished by floating the -Input of the HFA1115. Anything that tends to short the -Input to GND, such as stray capacitance at high frequencies, will cause the amplifier gain to increase toward a gain of +2. The result is excessive high frequency peaking, and possible instability. Even the minimal amount of capacitance associated with attaching the -Input lead to the PCB results in approximately 3dB of gain peaking. At a minimum this requires due care to ensure the minimum capacitance at the -Input connection.

Table 1 lists five alternate methods for configuring the HFA1115 as a unity gain buffer, and the corresponding performance. The implementations vary in complexity and involve performance trade-offs. The easiest approach to implement is simply shorting the two input pins together, and applying the input signal to this common node. The amplifier bandwidth drops from 400MHz to 200MHz, but excellent gain flatness is the benefit. Another drawback to this approach is that the amplifier input noise voltage and input offset voltage terms see a gain of +2, resulting in higher noise and output offset voltages. Alternately, a 100pF capacitor between the inputs shorts them only at high frequencies, which prevents the increased output offset voltage but delivers less gain flatness.

Another straightforward approach is to add a 620Ω resistor in series with the positive input. This resistor and the HFA1115 input capacitance form a low pass filter which rolls off the signal bandwidth before gain peaking occurs. This configuration was employed to obtain the datasheet AC and transient parameters for a gain of +1.

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

For unity gain applications, care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input. At higher frequencies this capacitance will tend to short the -INPUT to GND, resulting in a closed loop gain which increases with frequency. This will cause excessive high frequency peaking and potentially other problems as well.

An example of a good high frequency layout is the Evaluation Board shown in Figure 1.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 225MHz. By decreasing R_S as C_L increases the maximum bandwidth is obtained without sacrificing stability.

TABLE 1. UNITY GAIN PERFORMANCE FOR VARIOUS IMPLEMENTATIONS

APPROACH	PEAKING (dB)	BW (MHz)	+SR/-SR (V/µs)	±0.1dB GAIN FLATNESS (MHz)
Remove Pin 2	2.5	400	1200/850	20
$+R_S = 620\Omega$	0.6	170	1125/800	25
$+R_S = 620\Omega$ and Remove Pin 2	0	165	1050/775	65
Short Pins 2, 3	0	200	875/550	45
100pF cap. between pins 2, 3	0.2	190	900/550	19

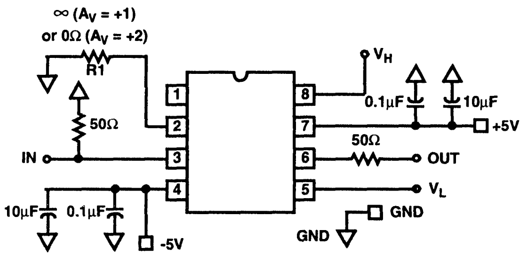
Evaluation Board

The performance of the HFA1115 may be evaluated using the HFA11XX Evaluation Board, slightly modified as follows:

1. Remove the 500Ω feedback resistor (R2), and leave the connection open.
2. a. For $A_V = +1$ evaluation, remove the 500Ω gain setting resistor (R1), and leave pin 2 floating.
   b. For $A_V = +2$, replace the 500Ω gain setting resistor with a 0Ω resistor to GND.

The layout and modified schematic of the board are shown in Figure 1.

To order evaluation boards, please contact your local sales office.



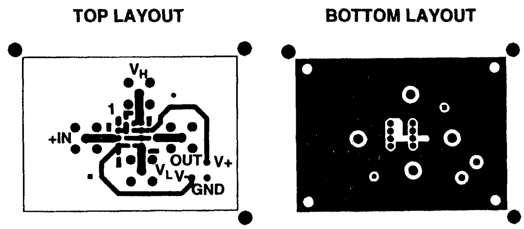


FIGURE 1. EVALUATION BOARD SCHEMATIC AND LAYOUT

HARRIS SEMICONDUCTOR

HFA1118, HFA1119

ADVANCE INFORMATION Programmable Gain Video Buffers with Output Limiting and Output Disable

June 1995

Features

- User Programmable For Closed Loop Gains of ±1, or +2 Without Use of External Resistors
- User Programmable Output Limiting (HFA1119)
- Standard Operational Amplifier Pinout
- Excellent Gain Accuracy .... ±0.5%
- Wide -3dB Bandwidth (A_V = +2) 500MHz
- Gain Flatness (to 250MHz) .... ±0.5dB
- Very Fast Slew Rate (A_V = +2) 1200V/µs
- Differential Gain/Phase .... 0.02%/0.02 Deg
- Fast Output Enable/Disable 10ns

Applications

- Flash A/D Drivers
- Video Cable Drivers
- Professional Video Processing
- Medical Imaging
- PC Multimedia Systems
- Video Pixel Switching
- Oscilloscopes and Analyzers

Description

The HFA1118, and HFA1119 are high speed, low power, closed loop buffers built with Harris' proprietary complementary bipolar UHF-1 process. Both buffers allow for selection of voltage gains of +2 and ±1, without the use of external gain setting resistors.

The HFA1119 is the ideal choice for high frequency applications requiring output limiting, especially those needing ultra fast overload recovery times. For added flexibility, the HFA1119 also features an active low, TTL/CMOS compatible disable input, which when activated forces the output to a high impedance state, and reduces supply current.

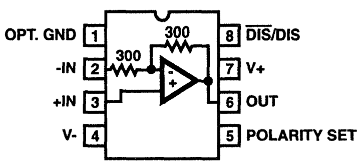
The HFA1118 features a TTL/CMOS compatible output disable pin which is user programmable for polarity (active high or low). This feature eliminates the inverter required between amplifiers in multiplexer configurations. The ultra-fast (10ns) enable and disable times make the HFA1118 and HFA1119 the obvious choices for pixel switching and other high speed multiplexing applications.

Ordering Information

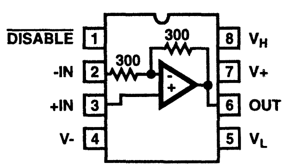
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1118IP, HFA1119IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1118IB, HFA1119IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

Pinouts

HFA1118
(PDIP, SOIC)
TOP VIEW



HFA1119
(PDIP, SOIC)
TOP VIEW



HFA1118 PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
Opt. Gnd	Optional GND. Maintains Disable Pin TTL Compatibility with Asymmetrical Supplies (e.g. +10V, 0V)
Polarity Set	Defines Polarity of Disable Input. High or Floating Selects Active Low Disable (i.e. $\overline{DIS}$).
$\overline{DIS}$/DIS	TTL Compatible Disable Input. Output is Driven to a True Hi-Z State When Active. Polarity depends on state of Polarity Set Pin.

HFA1118 DISABLE FUNCTIONALITY

POLARITY SET (PIN 5)	DISABLE (PIN 8)	OUTPUT (PIN 6)
High or Float	High or Float	Enabled
High or Float	Low	Disabled
Low	High or Float	Disabled
Low	Low	Enabled

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 4020

HARRIS SEMICONDUCTOR

HFA1135

High-Speed, Low Power, Video Operational Amplifier with Output Limiting

July 1995

Features

- User Programmable Output Voltage Limiting
- Fast Overdrive Recovery . . . . <1ns
- Low Supply Current 6.8mA
- High Input Impedance 2MΩ
- Wide -3dB Bandwidth 360MHz
- Very Fast Slew Rate 1200V/μs
- Gain Flatness (to 50MHz) . . . . ±0.07dB
- Differential Gain 0.02%
- Differential Phase . . . . 0.04 Deg.
- Pin Compatible Upgrade to CLC501 and CLC502

Applications

- Flash A/D Drivers
- High Resolution Monitors
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications

Description

The HFA1135 is a high speed, low power current feedback amplifier build with Harris' proprietary complementary bipolar UHF-1 process. This amplifier features user programmable output limiting, via the V_H and V_L pins.

The HFA1135 is the ideal choice for high speed, low power applications requiring output limiting (e.g. flash A/D drivers), especially those requiring fast overdrive recovery times. The limiting function allows the designer to set the maximum and minimum output levels to protect downstream stages from damage or input saturation. The sub-nanosecond overdrive recovery time ensures a quick return to linear operation following an overdrive condition.

Component and composite video systems also benefit from this operational amplifier's performance, as indicated by the gain flatness, and differential gain and phase specifications.

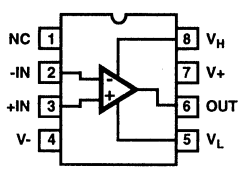
The HFA1135 is a low power, high performance upgrade for the CLC501 and CLC502.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1135IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1135IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

Pinout

HFA1135
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3653.1

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 2) . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
Junction Temperature (Die Only) . . . . +175°C
Junction Temperature (Plastic Package) . . . . +150°C
ESD Rating. . . . . >2000V
Lead Temperature (Soldering 10s). . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range . . . . $-40^oC \le T_A \le +85^oC$
Storage Temperature Range. . . . . $-65^oC \le T_A \le +150^oC$
Package Thermal Characteristics θ_{JA}
Plastic DIP . . . . 130°C/W
SOIC . . . . 170°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_F = 510\Omega$ (Note 3), $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER		(NOTE1) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	+25°C	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm 1.8V$	A	+25°C	47	50	-	dB
	$\Delta V_{CM} = \pm 1.8V$	A	+85°C	45	48	-	dB
	$\Delta V_{CM} = \pm 1.2V$	A	-40°C	45	48	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm 1.8V$	A	+25°C	50	54	-	dB
	$\Delta V_{PS} = \pm 1.8V$	A	+85°C	47	50	-	dB
	$\Delta V_{PS} = \pm 1.2V$	A	-40°C	47	50	-	dB
Non-Inverting Input Bias Current		A	+25°C	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm 1.8V$	A	+25°C	-	0.5	1	µA/V
	$\Delta V_{PS} = \pm 1.8V$	A	+85°C	-	0.8	3	µA/V
	$\Delta V_{PS} = \pm 1.2V$	A	-40°C	-	0.8	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm 1.8V$	A	+25°C	0.8	2	-	MΩ
	$\Delta V_{CM} = \pm 1.8V$	A	+85°C	0.5	1.3	-	MΩ
	$\Delta V_{CM} = \pm 1.2V$	A	-40°C	0.5	1.3	-	MΩ
Inverting Input Bias Current		A	+25°C	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/°C
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm 1.8V$	A	+25°C	-	3	6	µA/V
	$\Delta V_{CM} = \pm 1.8V$	A	+85°C	-	4	8	µA/V
	$\Delta V_{CM} = \pm 1.2V$	A	-40°C	-	4	8	µA/V
Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm 1.8V$	A	+25°C	-	2	5	µA/V
	$\Delta V_{PS} = \pm 1.8V$	A	+85°C	-	4	8	µA/V
	$\Delta V_{PS} = \pm 1.2V$	A	-40°C	-	4	8	µA/V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$ (Note 3), $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE1) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
Inverting Input Resistance		C	+25°C	-	40	-	Ω
Input Capacitance (Either Input)		C	+25°C	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	+25°C, +85°C	±1.8	±2.4	-	V
		A	-40°C	±1.2	±1.7	-	V
Input Noise Voltage Density (f = 100kHz)		B	+25°C	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density (f = 100kHz)		B	+25°C	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density (f = 100kHz)		B	+25°C	-	20	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain (A_V = -1)		C	+25°C	-	500	-	kΩ
A.C. CHARACTERISTICS $A_V = +2$, $R_F = 250\Omega$, Unless Otherwise Specified							
-3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$)	$A_V = +1$, $R_F = 1.5k\Omega$	B	+25°C	-	660	-	MHz
	$A_V = +2$, $R_F = 250\Omega$	B	+25°C	-	360	-	MHz
	$A_V = +2$, $R_F = 330\Omega$	B	+25°C	-	315	-	MHz
	$A_V = -1$, $R_F = 330\Omega$	B	+25°C	-	290	-	MHz
Full Power Bandwidth ($V_{OUT} = 5V_{P-P}$ at $A_V = +2/-1$, $4V_{P-P}$ at $A_V = +1$)	$A_V = +1$, $R_F = 1.5k\Omega$	B	+25°C	-	90	-	MHz
	$A_V = +2$, $R_F = 250\Omega$	B	+25°C	-	130	-	MHz
	$A_V = -1$, $R_F = 330\Omega$	B	+25°C	-	170	-	MHz
Gain Flatness (to 25MHz, $V_{OUT} = 0.2V_{P-P}$)	$A_V = +1$, $R_F = 1.5k\Omega$	B	+25°C	-	±0.10	-	dB
	$A_V = +2$, $R_F = 250\Omega$	B	+25°C	-	±0.02	-	dB
	$A_V = +2$, $R_F = 330\Omega$	B	+25°C	-	±0.02	-	dB
Gain Flatness (to 50MHz, $V_{OUT} = 0.2V_{P-P}$)	$A_V = +1$, $R_F = 1.5k\Omega$	B	+25°C	-	±0.22	-	dB
	$A_V = +2$, $R_F = 250\Omega$	B	+25°C	-	±0.07	-	dB
	$A_V = +2$, $R_F = 330\Omega$	B	+25°C	-	±0.03	-	dB
Minimum Stable Gain		A	Full	-	1	-	V/V
OUTPUT CHARACTERISTICS $R_F = 510\Omega$, Unless Otherwise Specified							
Output Voltage Swing ($A_V = -1$, $R_L = 100\Omega$)		A	+25°C	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current ($A_V = -1$, $R_L = 50\Omega$)		A	+25°C, +85°C	50	60	-	mA
		A	-40°C	28	42	-	mA
Output Short Circuit Current		B	+25°C	-	90	-	mA
DC Closed Loop Output Impedance ($A_V = +2$, $R_F = 250\Omega$)		B	+25°C	-	0.07	-	Ω
Second Harmonic Distortion ($A_V = +2$, $R_F = 250\Omega$, $V_{OUT} = 2V_{P-P}$)	10MHz	B	+25°C	-	-50	-	dBc
	20MHz	B	+25°C	-	-45	-	dBc
Third Harmonic Distortion ($A_V = +2$, $R_F = 250\Omega$, $V_{OUT} = 2V_{P-P}$)	10MHz	B	+25°C	-	-50	-	dBc
	20MHz	B	+25°C	-	-45	-	dBc

2

OPERATIONAL AMPLIFIERS

Electrical Specifications $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_F = 510\Omega$ (Note 3), $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE1) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
TRANSIENT CHARACTERISTICS $A_V = +2$, $R_F = 250\Omega$, Unless Otherwise Specified							
Rise and Fall Times ($V_{OUT} = 0.5V_{P-P}$)	Rise Time	B	+25°C	-	0.81	-	ns
	Fall Time	B	+25°C	-	1.25	-	ns
Overshoot (Note 4) (V_{OUT} = 0 to 0.5V, V_{IN} t_{RISE} = 2.5ns)	+OS	B	+25°C	-	3	-	%
	-OS	B	+25°C	-	5	-	%
Overshoot (Note 4) ($V_{OUT} = 0.5V_{P-P}$, V_{IN} t_{RISE} = 2.5ns)	+OS	B	+25°C	-	2	-	%
	-OS	B	+25°C	-	10	-	%
Slew Rate ($V_{OUT} = 4V_{P-P}$, $A_V = +1$, $R_F = 1.5k\Omega$)	+SR	B	+25°C	-	875	-	V/µs
	-SR	B	+25°C	-	510	-	V/µs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = +2$, $R_F = 250\Omega$)	+SR	B	+25°C	-	1530	-	V/µs
	-SR	B	+25°C	-	850	-	V/µs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = -1$, $R_F = 330\Omega$)	+SR	B	+25°C	-	2300	-	V/µs
	-SR	B	+25°C	-	1200	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step)	To 0.1%	B	+25°C	-	15	-	ns
	To 0.05%	B	+25°C	-	20	-	ns
	To 0.02%	B	+25°C	-	30	-	ns
VIDEO CHARACTERISTICS $A_V = +2$, $R_F = 250\Omega$, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	$R_L = 150\Omega$	B	+25°C	-	0.02	-	%
	$R_L = 75\Omega$	B	+25°C	-	0.03	-	%
Differential Phase (f = 3.58MHz)	$R_L = 150\Omega$	B	+25°C	-	0.04	-	Degrees
	$R_L = 75\Omega$	B	+25°C	-	0.06	-	Degrees
OUTPUT LIMITING CHARACTERISTICS $A_V = +2$, $R_F = 250\Omega$, $V_H = +1V$, $V_L = -1V$, Unless Otherwise Specified.							
Clamp Accuracy ($V_{IN} = \pm 2V$, $A_V = -1$, $R_F = 510\Omega$)		A	Full	-125	25	125	mV
Overdrive Recovery Time ($V_{IN} = \pm 1V$)		B	+25°C	-	0.8	-	ns
Negative Clamp Range		B	+25°C	-5.0 to +2.0			V
Positive Clamp Range		B	+25°C	-2.0 to +5.0			V
Clamp Input Bias Current		A	+25°C	-	50	200	µA
		A	Full	-	80	200	µA
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	+25°C	±4.5	-	±5.5	V
Power Supply Current		A	+25°C	6.6	6.8	7.1	mA
		A	Full	6.4	6.9	7.3	mA

NOTES:

1. Test Level: A. Production Tested.; B. Guaranteed Limit or Typical Based on Characterization.; C. Design Typical for Information Only.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.
3. The optimum feedback resistor for the HFA1135 at $A_V = +1$ is $1.5k\Omega$. The Production Tested parameters are tested with $R_F = 510\Omega$ because the HFA1135 shares test hardware with the HFA1105 amplifier.
4. Undershoot dominates for output signal swings below GND (e.g. $0.5V_{P-P}$), yielding a higher overshoot limit compared to the V_{OUT} = 0V to 0.5V condition.

Die Characteristics

DIE DIMENSIONS:
59 x 58.2 x 19 ± 1mils
1500μm x 1480μm ± 25.4μm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

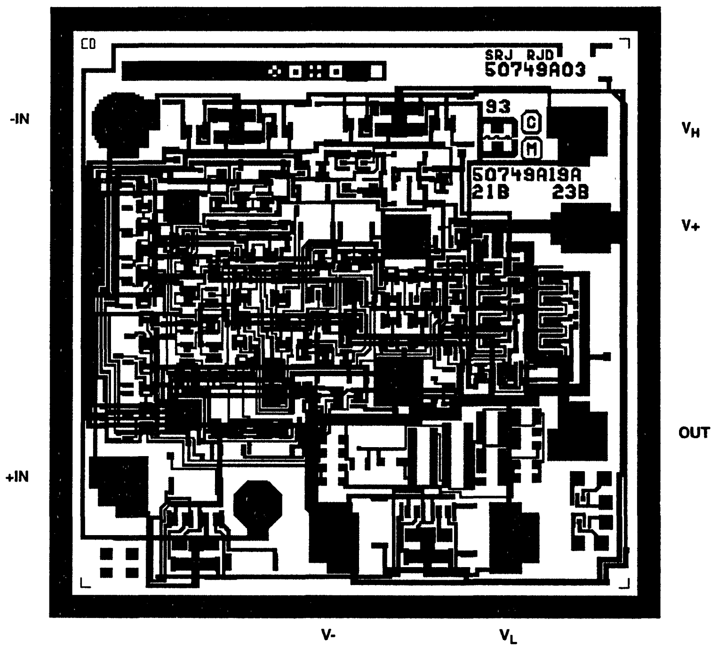
DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC

TRANSISTOR COUNT: 89

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1135



HARRIS SEMICONDUCTOR

HFA1145

High-Speed, Low Power, Current Feedback Video Operational Amplifier with Output Disable

July 1995

Features

- Low Supply Current 5.8mA
- High Input Impedance 1MΩ
- Wide -3dB Bandwidth 330MHz
- Very Fast Slew Rate 1000V/μs
- Gain Flatness (to 75MHz) . . . . ±0.1dB
- Differential Gain 0.02%
- Differential Phase 0.03Degrees
- Output Enable/Disable Time 180ns/35ns
- Pin Compatible Upgrade for CLC410

Applications

- Flash A/D Drivers
- Video Switching and Routing
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications

Description

The HFA1145 is a high speed, low power current feedback amplifier built with Harris' proprietary complementary bipolar UHF-1 process.

This amplifier features a TTL/CMOS compatible disable control, pin 8, which when pulled low reduces the supply current and forces the output into a high impedance state. This allows easy implementation of simple, low power video switching and routing systems. Component and composite video systems also benefit from this op amp's excellent gain flatness, and good differential gain and phase specifications.

Multiplexed A/D applications will also find the HFA1145 useful as the A/D driver/multiplexer.

The HFA1145 is a low power, high performance upgrade for the CLC410.

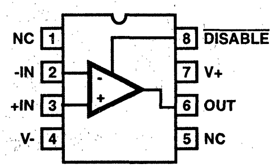
For Military grade product, please refer to the HFA1145/883 data sheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1145IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1145IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

Pinout

HFA1145
(PDIP, SOIC)
TOP VIEW



File Number 3955.1

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 2) . . . . Short Circuit Protected
. . . . 30mA Continuous
. . . . 60mA ≤ 50% Duty Cycle
Junction Temperature (Die Only) . . . . +175°C
Junction Temperature (Plastic Package) . . . . +150°C
ESD Rating . . . . >2000V
Lead Temperature (Soldering, 10s) . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range . . . . $-40^oC \le T_A \le +85^oC$
Storage Temperature Range . . . . $-65^oC \le T_A \le +150^oC$
Thermal Package Characteristics (°C/W) θ_{JA}
Plastic DIP Package 130
SOIC Package 170

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER		(NOTE1) TEST LEVEL	TEMPERATURE	ALL GRADES MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	+25°C	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	+25°C	47	50	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	45	48	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	45	48	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	+25°C	50	54	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	+85°C	47	50	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40°C	47	50	-	dB
Non-Inverting Input Bias Current		A	+25°C	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	+25°C	-	0.5	1	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	+85°C	-	0.8	3	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40°C	-	0.8	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	+25°C	0.8	1.2	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	0.5	0.8	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	0.5	0.8	-	MΩ
Inverting Input Bias Current		A	+25°C	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/°C
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm1.8V$	A	+25°C	-	3	6	µA/V
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	-	4	8	µA/V
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	-	4	8	µA/V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 510\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE1) TEST LEVEL	TEMPERATURE	ALL GRADES MIN	TYP	MAX	UNITS
Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	+25°C	-	2	5	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	+85°C	-	4	8	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40°C	-	4	8	µA/V
Inverting Input Resistance		C	+25°C	-	60	-	Ω
Input Capacitance (either input)		C	+25°C	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	+25°C, +85°C	±1.8	±2.4	-	V
		A	-40°C	±1.2	±1.7	-	V
Input Noise Voltage Density (f = 100kHz, Note 5)		B	+25°C	-	3.5	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current Density (f = 100kHz, Note 5)		B	+25°C	-	2.5	-	$pA/\sqrt{Hz}$
Inverting Input Noise Current Density (f = 100kHz, Note 5)		B	+25°C	-	20	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain ($A_V = -1$)		C	+25°C	-	500	-	kΩ
AC CHARACTERISTICS $R_F = 510\Omega$, Unless Otherwise Specified							
-3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$, Note 5)	$A_V = +1$, $+R_S = 510\Omega$	B	+25°C	-	270	-	MHz
		B	Full	-	240	-	MHz
	$A_V = -1$, $R_F = 425\Omega$	B	+25°C	-	300	-	MHz
	$A_V = +2$	B	+25°C	-	330	-	MHz
		B	Full	-	260	-	MHz
	$A_V = +10$, $R_F = 180\Omega$	B	+25°C	-	130	-	MHz
		B	Full	-	90	-	MHz
Full Power Bandwidth ($V_{OUT} = 5V_{P-P}$ at $A_V = +2/-1$, $4V_{P-P}$ at $A_V = +1$, Note 5)	$A_V = +1$, $+R_S = 510\Omega$	B	+25°C	-	135	-	MHz
	$A_V = -1$	B	+25°C	-	140	-	MHz
	$A_V = +2$	B	+25°C	-	115	-	MHz
Gain Flatness ($A_V = +2$, $V_{OUT} = 0.2V_{P-P}$, Note 5)	to 25MHz	B	+25°C	-	±0.03	-	dB
		B	Full	-	±0.04	-	dB
	to 75MHz	B	+25°C	-	±0.11	-	dB
		B	Full	-	±0.22	-	dB
Gain Flatness ($A_V = +1$, $+R_S = 510\Omega$, $V_{OUT} = 0.2V_{P-P}$, Note 5)	to 25MHz	B	+25°C	-	±0.03	-	dB
	to 75MHz	B	+25°C	-	±0.09	-	dB
Minimum Stable gain		A	Full	-	1	-	V/V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE1) TEST LEVEL	TEMPERATURE	ALL GRADES MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS A_V = +2, R_F = 510Ω, Unless Otherwise Specified							
Output Voltage Swing (A_V = -1, R_L = 100Ω, Note 5)		A	+25°C	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current (A_V = -1, R_L = 50Ω, Note 5)		A	+25°C, +85°C	50	60	-	mA
		A	-40°C	28	42	-	mA
Output Short Circuit Current		B	+25°C	-	90	-	mA
DC Closed Loop Output Impedance (Note 5)		B	+25°C	-	0.08	-	Ω
Second Harmonic Distortion (V_{OUT} = 2V_{P-P}, Note 5)	10MHz	B	+25°C	-	-48	-	dBc
	20MHz	B	+25°C	-	-44	-	dBc
Third Harmonic Distortion (V_{OUT} = 2V_{P-P}, Note 5)	10MHz	B	+25°C	-	-50	-	dBc
	20MHz	B	+25°C	-	-45	-	dBc
Reverse Isolation (30MHz, Note 5)		B	+25°C	-	-55	-	dB
TRANSIENT CHARACTERISTICS A_V = +2, R_F = 510Ω, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = 0.5V_{P-P})		B	+25°C	-	1.1	-	ns
		B	Full	-	1.4	-	ns
Overshoot (Note 3) (V_{OUT} = 0 to 0.5V, V_{IN} t_{RISE} = 1ns)	+OS	B	+25°C	-	3	-	%
	-OS	B	+25°C	-	5	-	%
Overshoot (Note 3) (V_{OUT} = 0.5V_{P-P}, V_{IN} t_{RISE} = 1ns)	+OS	B	+25°C	-	3	-	%
	-OS	B	+25°C	-	11	-	%
Slew Rate (V_{OUT} = 4V_{P-P}, A_V = +1, +R_S = 510Ω)	+SR	B	+25°C	-	1000	-	V/µs
		B	Full	-	975	-	V/µs
	-SR (Note 4)	B	+25°C	-	650	-	V/µs
		B	Full	-	580	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = +2)	+SR	B	+25°C	-	1400	-	V/µs
		B	Full	-	1200	-	V/µs
	-SR (Note 4)	B	+25°C	-	800	-	V/µs
		B	Full	-	700	-	V/µs
Slew Rate (V_{OUT} = 5V_{P-P}, A_V = -1)	+SR	B	+25°C	-	2100	-	V/µs
		B	Full	-	1900	-	V/µs
	-SR (Note 4)	B	+25°C	-	1000	-	V/µs
		B	Full	-	900	-	V/µs

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE1) TEST LEVEL	TEMPERATURE	ALL GRADES MIN	TYP	MAX	UNITS
Settling Time (V_{OUT} = +2V to 0V step, Note 5)	To 0.1%	B	+25°C	-	15	-	ns
	To 0.05%	B	+25°C	-	23	-	ns
	To 0.02%	B	+25°C	-	30	-	ns
Overdrive Recovery Time (V_{IN} = ±2V)		B	+25°C	-	8.5	-	ns
VIDEO CHARACTERISTICS A_V = +2, R_F = 510Ω, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	+25°C	-	0.02	-	%
	R_L = 75Ω	B	+25°C	-	0.03	-	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	+25°C	-	0.03	-	Degrees
	R_L = 75Ω	B	+25°C	-	0.05	-	Degrees
DISABLE CHARACTERISTICS							
Disabled Supply Current ($V_{\overline{DISABLE}}$ = 0V)		A	Full	-	3	4	mA
$\overline{\text{DISABLE}}$ Input Logic Low		A	Full	-	-	0.8	V
$\overline{\text{DISABLE}}$ Input Logic High		A	+25°C, +85°C	2.0	-	-	V
		A	-40°C	2.4	-	-	V
$\overline{\text{DISABLE}}$ Input Logic Low Current ($V_{\overline{DISABLE}}$ = 0V)		A	Full	-	100	200	µA
$\overline{\text{DISABLE}}$ Input Logic High Current ($V_{\overline{DISABLE}}$ = 5V)		A	Full	-	1	15	µA
Output Disable Time (V_{IN} = ±1V, $V_{\overline{DISABLE}}$ = 2.4V to 0V, Note 5)		B	+25°C	-	35	-	ns
Output Enable Time (V_{IN} = ±1V, $V_{\overline{DISABLE}}$ = 0V to 2.4V, Note 5)		B	+25°C	-	180	-	ns
Disabled Output Capacitance ($V_{\overline{DISABLE}}$ = 0V)		B	+25°C	-	2.5	-	pF
Disabled Output Leakage ($V_{\overline{DISABLE}}$ = 0V, V_{IN} = ∓2V, V_{OUT} = ±3V)		A	Full	-	3	10	µA
Off Isolation ($V_{\overline{DISABLE}}$ = 0V, V_{IN} = $1V_{P-P}$, Note 5)	at 5MHz	B	+25°C	-	-75	-	dB
	at 25MHz	B	+25°C	-	-60	-	dB
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	+25°C	±4.5	-	±5.5	V
Power Supply Current		A	+25°C	-	5.8	6.1	mA
		A	Full	-	5.9	6.3	mA

NOTES:

1. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.
3. Undershoot dominates for output signal swings below GND (e.g. $0.5V_{P-P}$), yielding a higher overshoot limit compared to the V_{OUT} = 0 to 0.5V condition. See the "Application Information" section for details.
4. Slew rates are asymmetrical if the output swings below GND (e.g. a bipolar signal). Positive unipolar output signals have symmetric positive and negative slew rates comparable to the +SR specification. See the "Application Information" section, and the pulse response graphs for details.
5. See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1145 design is optimized for $R_F = 510\Omega$ at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains, however, the amplifier is more stable so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For a gain of +1, a resistor (+R_S) in series with +IN is required to reduce gain peaking and increase stability.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	425	300
+1	510 (+R_S = 510Ω)	270
+2	510	330
+5	200	300
+10	180	130

Non-inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be $\geq 50\Omega$. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

$\overline{\text{DISABLE}}$ Input TTL Compatibility

The HFA1145 derives an internal GND reference for the digital circuitry as long as the power supplies are symmetrical about GND. With symmetrical supplies the digital switching threshold ($V_{TH} = (V_{IH} + V_{IL}) / 2 = (2.0 + 0.8) / 2)$ is 1.4V, which ensures the TTL compatibility of the $\overline{\text{DISABLE}}$ input. If asymmetrical supplies (e.g. +10V, 0V) are utilized, the switching threshold becomes:

$$V_{TH} = \frac{V+ + V-}{2} + 1.4V$$

and the V_{IH} and V_{IL} levels will be $V_{TH} \pm 0.6V$, respectively.

Optional GND Pad (Die Use Only) for TTL Compatibility

The die version of the HFA1145 provides the user with a GND pad for setting the disable circuitry GND reference. With symmetrical supplies the GND pad may be left unconnected, or tied directly to GND. If asymmetrical supplies (e.g. +10V, 0V) are utilized, and TTL compatibility is desired, die users must connect the GND pad to GND. With an external GND, the $\overline{\text{DISABLE}}$ input is TTL compatible regardless of supply voltage utilized.

Pulse Undershoot and Asymmetrical Slew Rates

The HFA1145 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (See Figures 5, 8, and 11). This undershoot isn't present for small bipolar signals, or large positive signals. Another artifact of the composite device is asymmetrical slew rates for output signals with a negative voltage component. The slew rate degrades as the output signal crosses through 0V (See Figures 5, 8, and 11), resulting in a slower overall negative slew rate. Positive only signals have symmetrical slew rates as illustrated in the large signal positive pulse response graphs (See Figures 4, 7, and 10).

PC Board Layout

This amplifier's frequency response depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the device's input and output connections. Capacitance, parasitic or planned, connected to the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground at the amplifier's inverting input (-IN), as this capacitance causes gain peaking, pulse overshoot, and if large enough, instability. To reduce this capacitance, the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

An example of a good high frequency layout is the Evaluation Board shown in Figure 2.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 270MHz (for $A_V = +1$). By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, the bandwidth decreases as the load capacitance increases. For example, at $A_V = +1$, $R_S = 62\Omega$, $C_L = 40pF$, the overall bandwidth is limited to 180MHz, and bandwidth drops to 75MHz at $A_V = +1$, $R_S = 8\Omega$, $C_L = 400pF$.

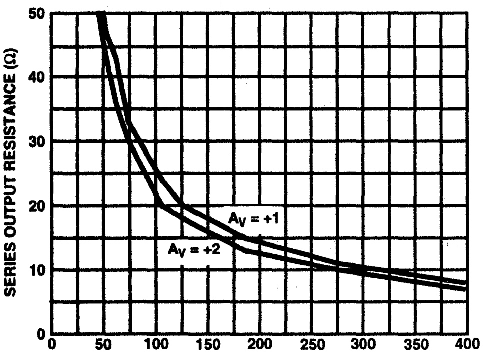


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1145 may be evaluated using the HFA11XX Evaluation Board.

The layout and schematic of the board are shown in Figure 2. The V_H connection may be used to exercise the DISABLE pin, but note that this connection has no 50Ω termination. To order evaluation boards (part number HFA11XXEVAL), please contact your local sales office.

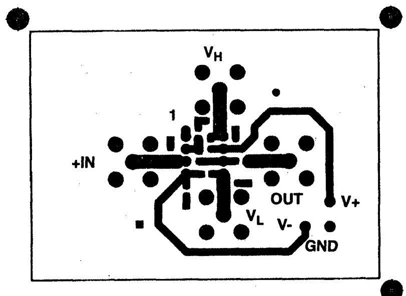


FIGURE 2A. TOP LAYOUT

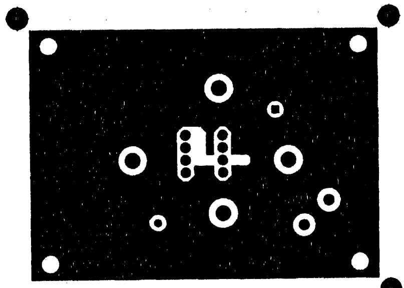


FIGURE 2B. BOTTOM LAYOUT

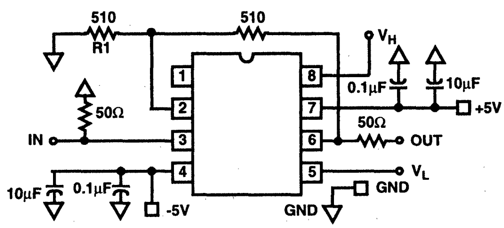


FIGURE 2C. SCHEMATIC

FIGURE 2. EVALUATION BOARD SCHEMATIC AND LAYOUT

Die Characteristics

DIE DIMENSIONS:
59 x 59 x 19 ± 1mils
1500µm x 1500µm x 483µm ± 25.4µm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

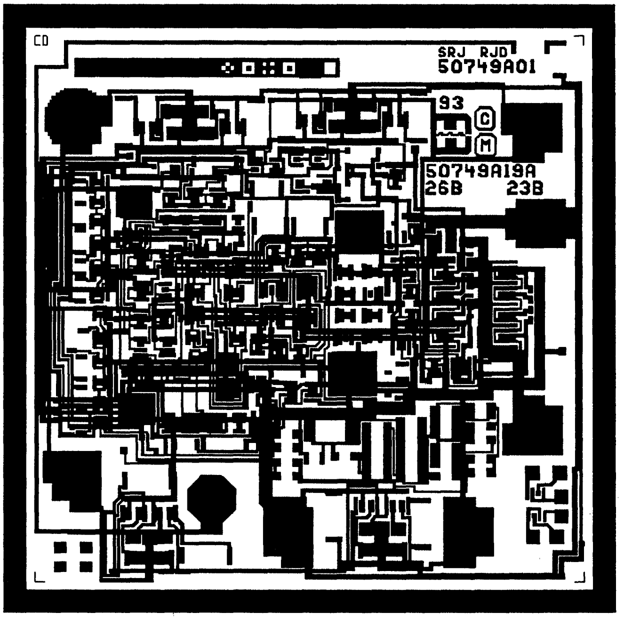
GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

TRANSISTOR COUNT: 75

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1145



† This pad is not bonded out on packaged units. Die users may set a GND reference, via this pad, to ensure the TTL compatibility of the $\overline{\text{DIS}}$ input when using asymmetrical supplies (e.g. V+ = 10V, V- = 0V). See the "Application Information" section for details.

2

OPERATIONAL AMPLIFIERS

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

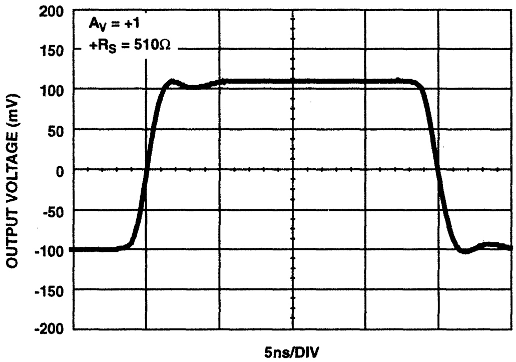


FIGURE 3. SMALL SIGNAL PULSE RESPONSE

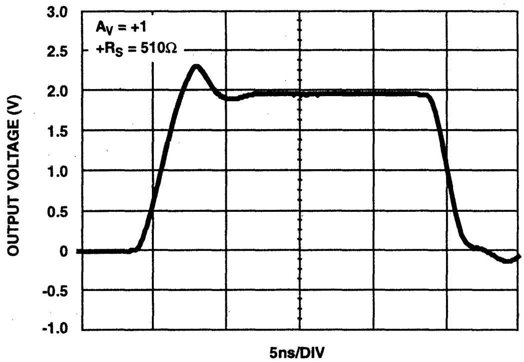


FIGURE 4. LARGE SIGNAL POSITIVE PULSE RESPONSE

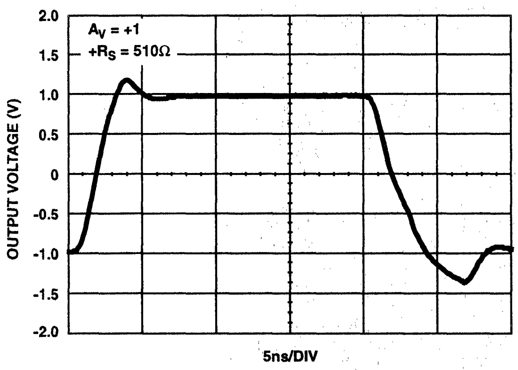


FIGURE 5. LARGE SIGNAL BIPOLAR PULSE RESPONSE

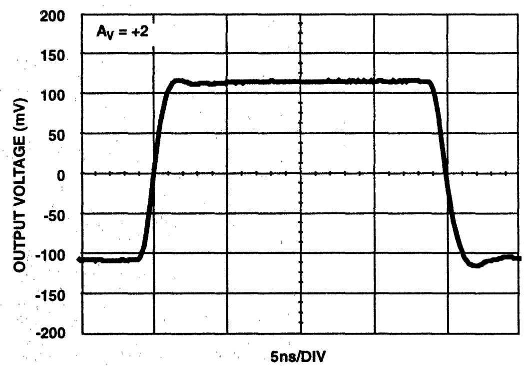


FIGURE 6. SMALL SIGNAL PULSE RESPONSE

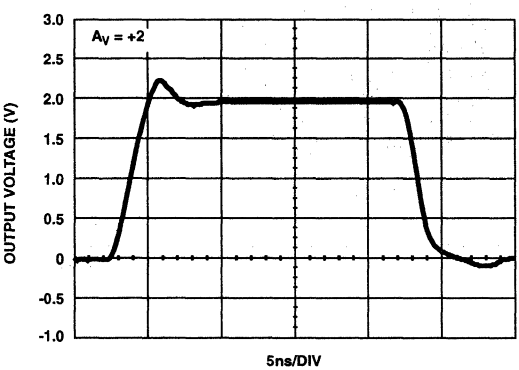


FIGURE 7. LARGE SIGNAL POSITIVE PULSE RESPONSE

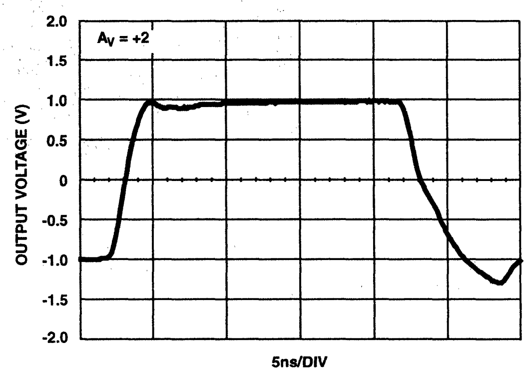


FIGURE 8. LARGE SIGNAL BIPOLAR PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

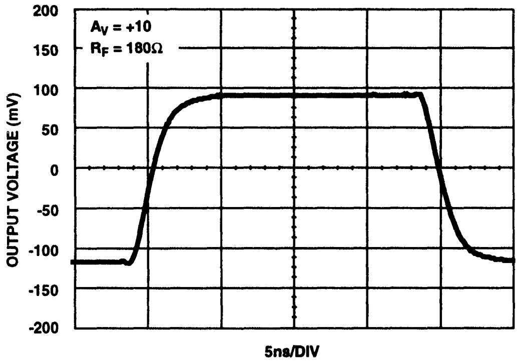


FIGURE 9. SMALL SIGNAL PULSE RESPONSE

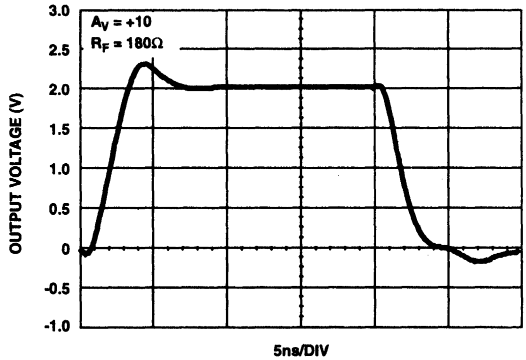


FIGURE 10. LARGE SIGNAL POSITIVE PULSE RESPONSE

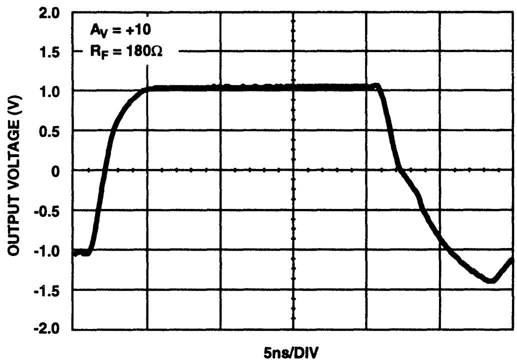


FIGURE 11. LARGE SIGNAL BIPOLAR PULSE RESPONSE

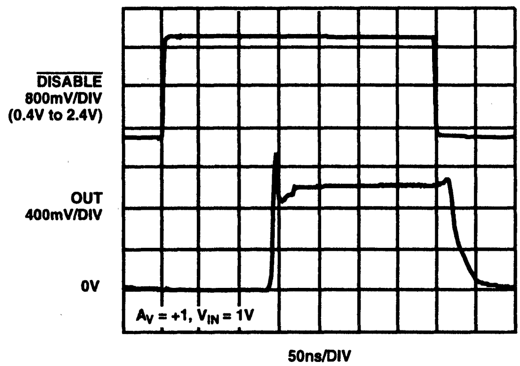


FIGURE 12. OUTPUT ENABLE AND DISABLE RESPONSE

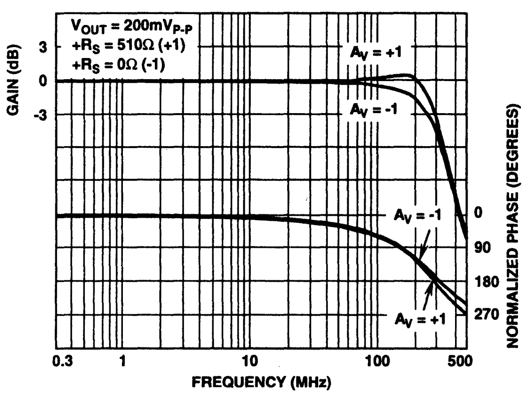


FIGURE 13. FREQUENCY RESPONSE

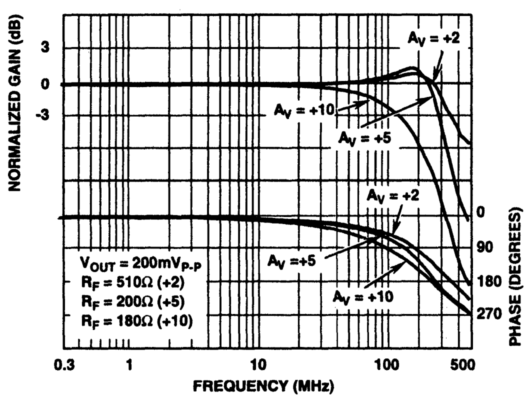


FIGURE 14. FREQUENCY RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $R_F = 510\Omega$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

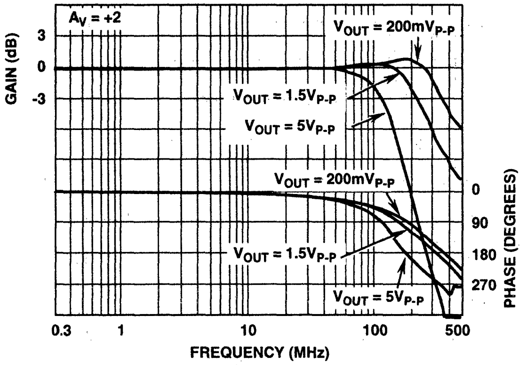


FIGURE 15. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

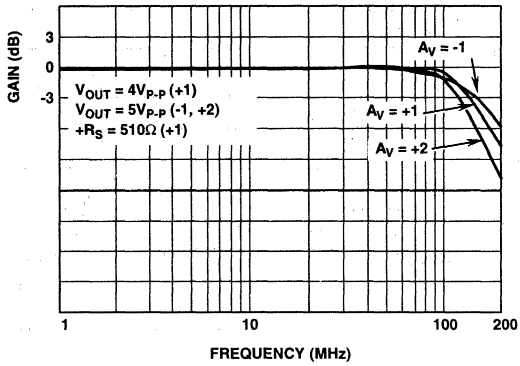


FIGURE 16. FULL POWER BANDWIDTH

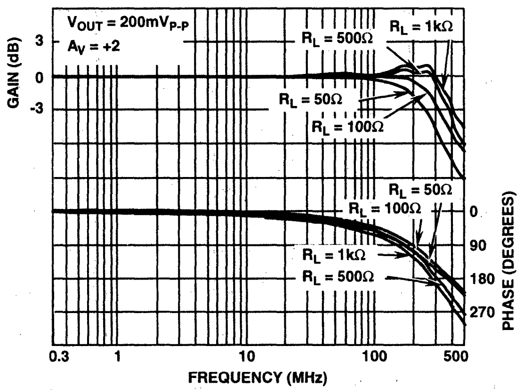


FIGURE 17. FREQUENCY RESPONSE FOR VARIOUS LOAD RESISTORS

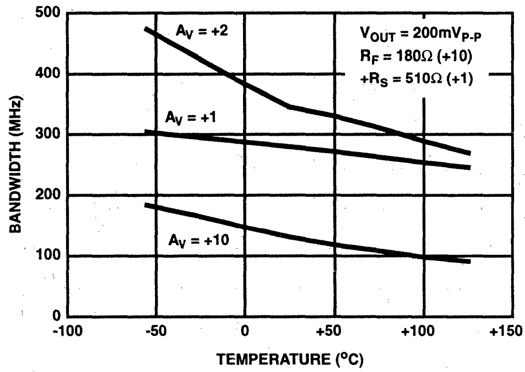


FIGURE 18. -3dB BANDWIDTH vs TEMPERATURE

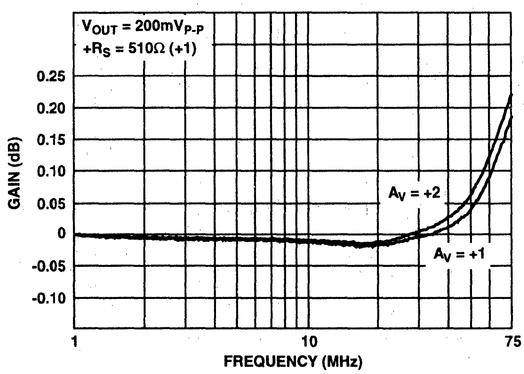


FIGURE 19. GAIN FLATNESS

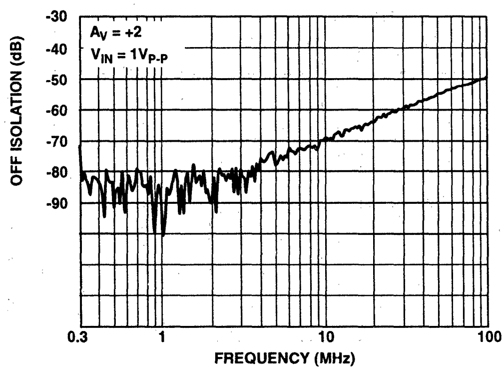


FIGURE 20. OFF ISOLATION

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $R_F = 510\Omega$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

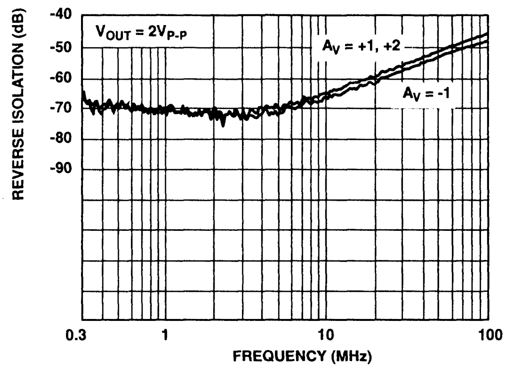


FIGURE 21. REVERSE ISOLATION

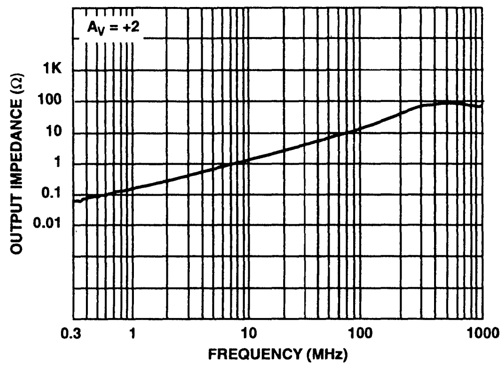


FIGURE 22. ENABLED OUTPUT IMPEDANCE

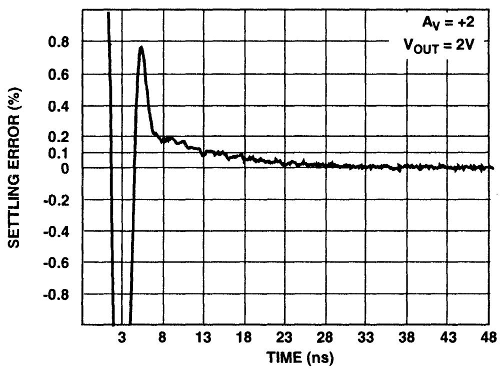


FIGURE 23. SETTLING RESPONSE

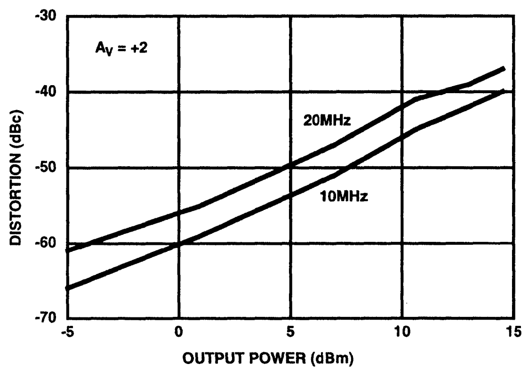


FIGURE 24. 2nd HARMONIC DISTORTION vs P_{OUT}

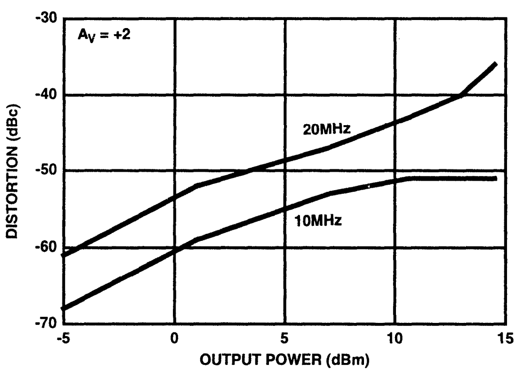


FIGURE 25. 3rd HARMONIC DISTORTION vs P_{OUT}

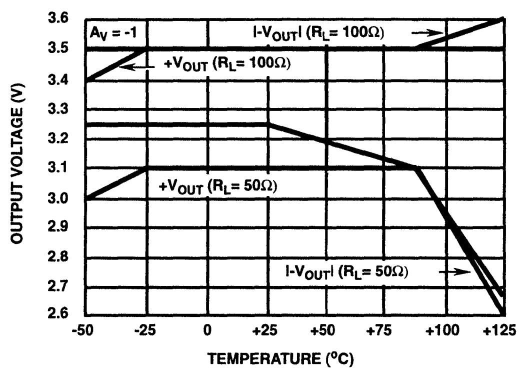


FIGURE 26. OUTPUT VOLTAGE vs TEMPERATURE

Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $R_F = 510\Omega$, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

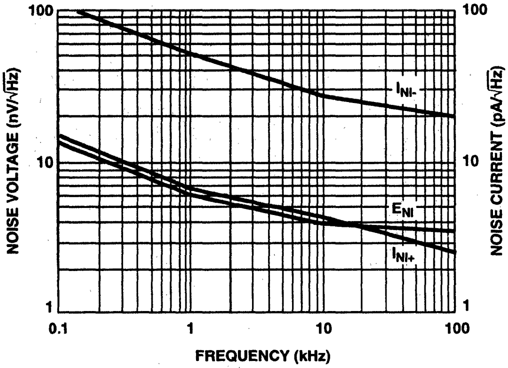


FIGURE 27. INPUT NOISE CHARACTERISTICS

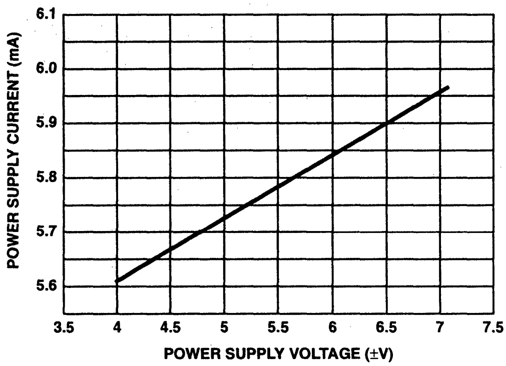


FIGURE 28. SUPPLY CURRENT vs SUPPLY VOLTAGE

HARRIS SEMICONDUCTOR

HFA1205

Dual High-Speed, Low Power, Video Operational Amplifier

July 1995

Features

- **Low Supply Current . . . . 5.8mA/Op Amp**
- **High Input Impedance 2MΩ**
- **Wide -3dB Bandwidth (A_V = +2) 400MHz**
- **Very Fast Slew Rate 1275V/µs**
- **Gain Flatness (to 50MHz) . . . . ±0.03dB**
- **Differential Gain 0.03%**
- **Differential Phase. . . . . .0.03Deg.**
- **Pin Compatible Upgrade to HA5023**

Applications

- **Flash A/D Drivers**
- **High Resolution Monitors**
- **Video Switching and Routing**
- **Professional Video Processing**
- **Video Digitizing Boards/Systems**
- **Multimedia Systems**
- **RGB Preamps**
- **Medical Imaging**
- **Hand Held and Miniaturized RF Equipment**
- **Battery Powered Communications**
- **High Speed Oscilloscopes and Analyzers**

Description

The HFA1205 is a dual, high speed, low power current feedback amplifier built with Harris' proprietary complementary bipolar UHF-1 process.

These amplifiers deliver 400MHz bandwidth and 1275V/µs slew rate, on only 60mW of quiescent power. They are specifically designed to meet the performance, power, and cost requirements of high volume video applications. The excellent gain flatness and differential gain/phase performance make these amplifiers well suited for component or composite video applications. Video performance is maintained even when driving a back terminated cable (R_L = 150Ω), and degrades only slightly when driving two back terminated cables (R_L = 75Ω). RGB applications will benefit from the high slew rates, and high full power bandwidth.

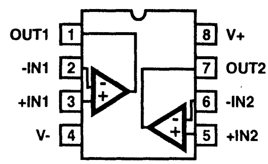
The HFA1205 is a pin compatible, low power, high performance upgrade for the popular Harris HA5023. For a dual amplifier with output disable capability, please see the HFA1245 datasheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1205IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1205IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

Pinout

HFA1205
(PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 2) . . . . Short Circuit Protected
30mA Continuous
60mA ≤ 50% Duty Cycle
Junction Temperature (Die Only) . . . . +175°C
Junction Temperature (Plastic Package) . . . . +150°C
ESD Rating. . . . . >2000V
Lead Temperature (Soldering 10s). . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range . . . . $-40^oC \le T_A \le +85^oC$
Storage Temperature Range. . . . . $-65^oC \le T_A \le +150^oC$
Thermal Package Characteristics θ_{JA}
Plastic DIP. . . . . 130°C/W
SOIC . . . . 160°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 560\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER		(NOTE 1) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	+25°C	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	+25°C	45	48	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	43	46	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	43	46	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	+25°C	48	52	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	+85°C	46	50	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40°C	46	50	-	dB
Non-Inverting Input Bias Current		A	+25°C	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	+25°C	-	0.5	1	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	+85°C	-	0.8	3	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40°C	-	0.8	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	+25°C	0.8	2	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	0.5	1.3	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	0.5	1.3	-	MΩ
Inverting Input Bias Current		A	+25°C	-	2	8.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/°C
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm1.8V$	A	+25°C	-	3	6	µA/V
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	-	4	8	µA/V
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	-	4	8	µA/V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 560\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 1) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	+25°C	-	2	5	μA/V
	$\Delta V_{PS} = \pm1.8V$	A	+85°C	-	4	8	μA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40°C	-	4	8	μA/V
Inverting Input Resistance		C	+25°C	-	60	-	Ω
Input Capacitance (either input)		C	+25°C	-	1.6	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	+25°C, +85°C	±1.8	±2.4	-	V
		A	-40°C	±1.2	±1.7	-	V
Input Noise Voltage Density (f = 100kHz)		B	+25°C	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density (f = 100kHz)		B	+25°C	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density (f = 100kHz)		B	+25°C	-	20	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain (A_V = -1)		C	+25°C	-	500	-	kΩ
AC CHARACTERISTICS $A_V = +2$, $R_F = 464\Omega$, Unless Otherwise Specified							
-3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$)	$A_V = +1$, $+R_S = 432\Omega$	B	+25°C	-	280	-	MHz
	$A_V = +2$	B	+25°C	-	400	-	MHz
	$A_V = -1$, $R_F = 332\Omega$	B	+25°C	-	360	-	MHz
Full Power Bandwidth ($V_{OUT} = 5V_{P-P}$ at $A_V = +2/-1$, $4V_{P-P}$ at $A_V = +1$)	$A_V = +1$, $R_S = 432\Omega$	B	+25°C	-	140	-	MHz
	$A_V = +2$	B	+25°C	-	125	-	MHz
	$A_V = -1$, $R_F = 332\Omega$	B	+25°C	-	180	-	MHz
Gain Flatness ($A_V = +2$, $V_{OUT} = 0.2V_{P-P}$)	To 25MHz	B	+25°C	-	±0.02	-	dB
	To 50MHz	B	+25°C	-	±0.03	-	dB
Minimum Stable Gain		A	Full	-	1	-	V/V
Crosstalk	5MHz	B	+25°C	-	-60	-	dB
	10MHz	B	+25°C	-	-54	-	dB
OUTPUT CHARACTERISTICS $R_F = 560\Omega$, Unless Otherwise Specified							
Output Voltage Swing ($A_V = -1$, $R_L = 100\Omega$)		A	+25°C	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current ($A_V = -1$, $R_L = 50\Omega$)		A	+25°C, +85°C	50	60	-	mA
		A	-40°C	28	42	-	mA
Output Short Circuit Current		B	+25°C	-	90	-	mA
DC Closed Loop Output Impedance ($A_V = +2$, $R_F = 464\Omega$)		B	+25°C	-	0.07	-	Ω
Second Harmonic Distortion ($A_V = +2$, $R_F = 464\Omega$, $V_{OUT} = 2V_{P-P}$)	10MHz	B	+25°C	-	-50	-	dBc
	20MHz	B	+25°C	-	-45	-	dBc
Third Harmonic Distortion ($A_V = +2$, $R_F = 464\Omega$, $V_{OUT} = 2V_{P-P}$)	10MHz	B	+25°C	-	-55	-	dBc
	20MHz	B	+25°C	-	-50	-	dBc

Electrical Specifications $V_{SUPPLY} = \pm 5V$, $A_V = +1$, $R_F = 560\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 1) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
TRANSIENT CHARACTERISTICS $A_V = +2$, $R_F = 464\Omega$, Unless Otherwise Specified							
Rise and Fall Times ($V_{OUT} = 0.5V_{P-P}$)	Rise Time	B	+25°C	-	0.8	-	ns
	Fall Time	B	+25°C	-	1.25	-	ns
Overshoot ($V_{OUT} = 0.5V_{P-P}$, V_{IN} $t_{RISE} = 2.5ns$)		B	+25°C	-	5	-	%
Slew Rate ($V_{OUT} = 4V_{P-P}$, $A_V = +1$, $+R_S = 432\Omega$)	+SR	B	+25°C	-	1050	-	V/µs
	-SR	B	+25°C	-	750	-	V/µs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = +2$)	+SR	B	+25°C	-	1375	-	V/µs
	-SR	B	+25°C	-	875	-	V/µs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = -1$, $R_F = 332\Omega$)	+SR	B	+25°C	-	2250	-	V/µs
	-SR	B	+25°C	-	1275	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step)	To 0.1%	B	+25°C	-	15	-	ns
	To 0.05%	B	+25°C	-	20	-	ns
	To 0.02%	B	+25°C	-	30	-	ns
Overdrive Recovery Time ($V_{IN} = \pm 2V$)		B	+25°C	-	10	-	ns
VIDEO CHARACTERISTICS $A_V = +2$, $R_F = 464\Omega$, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	$R_L = 150\Omega$	B	+25°C	-	0.03	-	%
	$R_L = 75\Omega$	B	+25°C	-	0.03	-	%
Differential Phase (f = 3.58MHz)	$R_L = 150\Omega$	B	+25°C	-	0.03	-	Degrees
	$R_L = 75\Omega$	B	+25°C	-	0.05	-	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	+25°C	±4.5	-	±5.5	V
Power Supply Current		A	+25°C	5.6	5.8	6.1	mA/ Op Amp
		A	Full	5.4	5.9	6.3	mA/ Op Amp

NOTES:

1. Test Level: A. Production Tested.; B. Guaranteed Limit or Typical Based on Characterization.; C. Design Typical for Information Only.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.

Die Characteristics

DIE DIMENSIONS:
69 x 92 x 19 ± 1mils
1750μm x 2330μm ± 25.4μm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

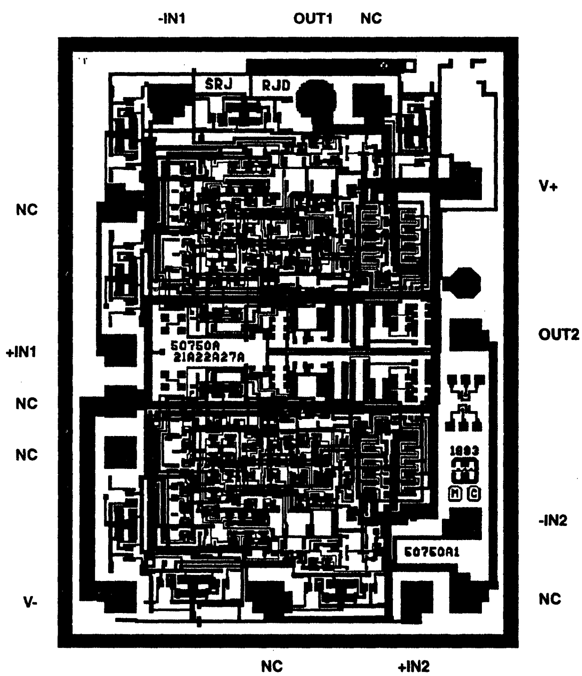
DIE ATTACH:
Material: Epoxy - Plastic DIP and SOIC

TRANSISTOR COUNT: 180

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1205



Application Information

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F , in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1205 design is optimized for a 464Ω R_F at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For good channel-to-channel gain matching, it is recommended that all resistors (termination as well as gain setting) be ±1% tolerance or better. Note that a series input resistor, on +IN, is required for a gain of +1, to reduce gain peaking and increase stability.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	332	360
+1	464 (+R_S = 432Ω)	280
+2	464	400

Non-inverting Input Source Impedance

For best operation, the D.C. source impedance seen by the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to -IN, and connections to -IN should be kept as short as possible.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 280MHz (for $A_V = +1$). By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth decreases as the load capacitance increases. For example, at $A_V = +1$, $R_S = 62Ω$, $C_L = 40pF$, the overall bandwidth is limited to 180MHz, and bandwidth drops to 70MHz at $A_V = +1$, $R_S = 8Ω$, $C_L = 400pF$.

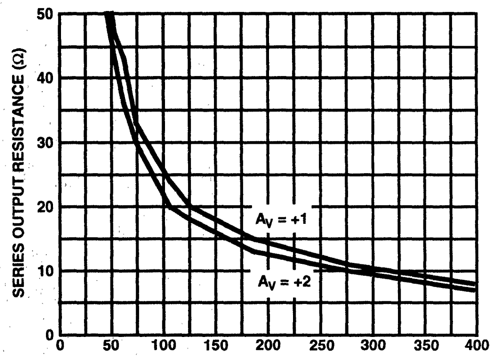


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1205 may be evaluated using the HA5023 Evaluation Board. The feedback and gain setting resistors must be replaced with the appropriate value (see "Optimum Feedback Resistor" section) for the gain being evaluated.

To order evaluation boards, please contact your local sales office.

Typical Performance Curves
$V_{SUPPLY} = \pm5V$, R_F = Optimum Value From "Apps Info" Table, $T_A = +25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

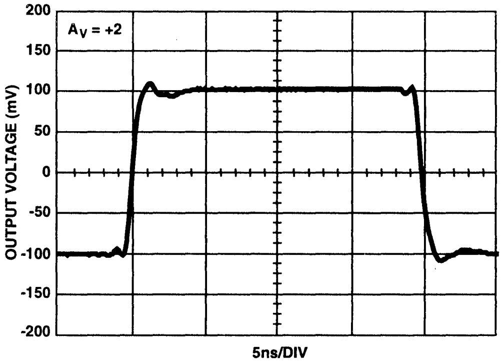


FIGURE 2. SMALL SIGNAL PULSE RESPONSE

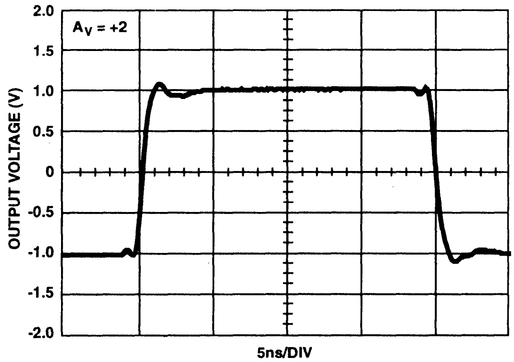


FIGURE 3. LARGE SIGNAL PULSE RESPONSE

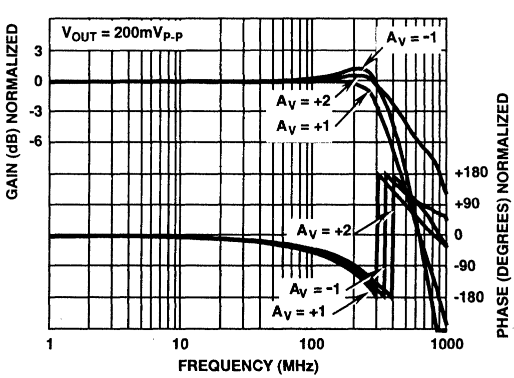


FIGURE 4. FREQUENCY RESPONSE

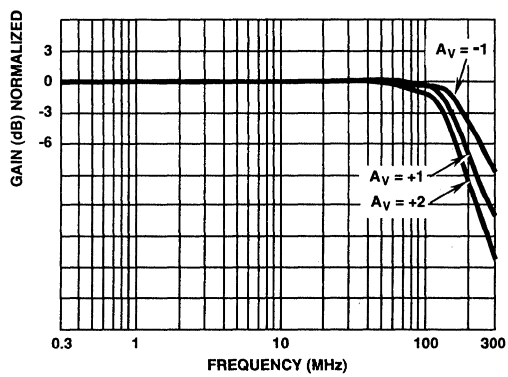


FIGURE 5. FULL POWER BANDWIDTH

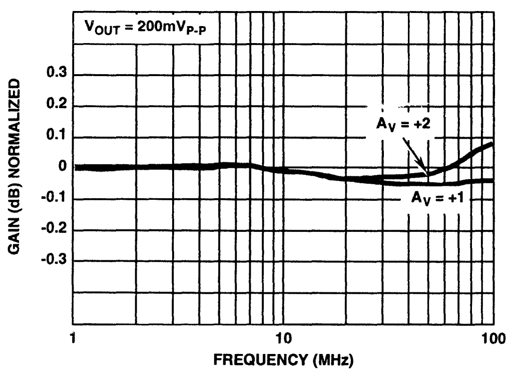


FIGURE 6. GAIN FLATNESS

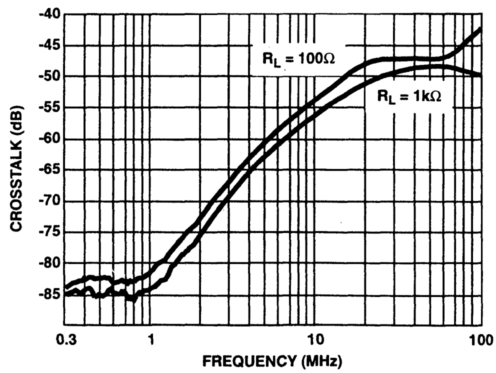


FIGURE 7. CROSSTALK vs FREQUENCY

HARRIS SEMICONDUCTOR HFA1212, HFA1412

July 1995

Dual/Quad High Speed, Low Power Closed Loop Buffer Amplifiers

Features

- **Differential Gain 0.025%**
- **Differential Phase .... 0.02 Deg.**
- **Wide -3dB Bandwidth (A_V = +2) 350MHz**
- **Very Fast Slew Rate (A_V = -1) 1100V/µs**
- **Low Supply Current 6mA/Buffer**
- **High Output Current 60mA**
- **Excellent Gain Accuracy 0.99V/V**
- **User Programmable For Closed-Loop Gains of +1, -1 or +2 Without Use of External Resistors**
- **Overdrive Recovery 8ns**
- **Standard Operational Amplifier Pinout**

Applications

- **High Resolution Monitors**
- **Professional Video Processing**
- **Medical Imaging**
- **Video Digitizing Boards/Systems**
- **RF/IF Processors**
- **Battery Powered Communications**
- **Flash Converter Drivers**
- **High Speed Pulse Amplifiers**

Description

The HFA1212 and HFA1412 are closed loop Buffers featuring user programmable gain and high speed performance. Manufactured on Harris' proprietary complementary bipolar UHF-1 process, these devices offer wide -3dB bandwidth of 350MHz, very fast slew rate, excellent gain flatness and high output current.

A unique feature of the pinout allows the user to select a voltage gain of +1, -1, or +2, without the use of any external components. Gain selection is accomplished via connections to the inputs, as described in the "Application Information" section. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

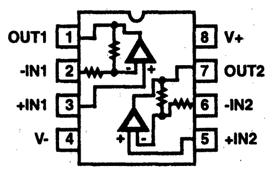
Compatibility with existing op amp pinouts provides flexibility to upgrade low gain amplifiers, while decreasing component count. Unlike most buffers, the standard pinout provides an upgrade path should a higher closed loop gain be needed at a future date. For Military product, refer to the HFA1212/883 or HFA1412/883 data sheets.

Ordering Information

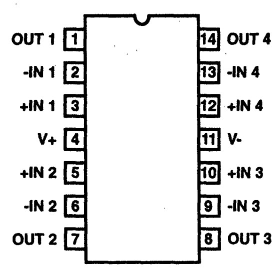
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1212IP	-40°C to +85°C	8 Lead Plastic DIP
HFA1212IB	-40°C to +85°C	8 Lead Plastic SOIC (N)
HFA1412IP	-40°C to +85°C	14 Lead Plastic DIP
HFA1412IB	-40°C to +85°C	14 Lead Plastic SOIC (N)

Pinouts

HFA1212
(PDIP, SOIC)
TOP VIEW



HFA1412
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3607.2**

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . . V_{SUPPLY}
Differential Input Voltage 5V
Output Current (Note 1) . . . . . Short Circuit Protected
Junction Temperature (Die Only) . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . +150°C
ESD Rating. . . . . >2000V
Lead Temperature (Soldering 10s). . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range . . . . . $-40^oC \le T_A \le +85^oC$
Storage Temperature Range. . . . . $-65^oC \le T_A \le +150^oC$
Thermal Package Characteristics θ_{JA}
8 Lead Plastic DIP. . . . . 130°C/W
8 Lead SOIC . . . . . 160°C/W
14 Lead Plastic DIP. . . . . 100°C/W
14 Lead SOIC . . . . . 120°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER	(NOTE 2) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Output Offset Voltage	A	+25°C	-	2	10	mV
	A	Full	-	3	15	mV
Average Output Offset Voltage Drift	B	Full	-	22	70	µV/°C
Non-Inverting Input Bias Current	A	+25°C	-	6	15	µA
	A	Full	-	-	25	µA
Non-Inverting Input Bias Current Drift	B	Full	-	30	-	nA/°C
Non-Inverting Input Resistance ($\Delta V_{CM} = \pm1.2V$)	A	+25°C	0.8	1.1	-	MΩ
Input Capacitance (either input)	C	+25°C	-	2	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMRR tests)	A	+25°C	±1.8	±2.4	-	V
	A	Full	±1.2	±1.7	-	V
Input Noise Voltage Density (f = 10kHz)	B	+25°C	-	7	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current Density (f = 10kHz)	B	+25°C	-	3.6	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS						
Gain ($A_V = +2$)	B	+25°C	1.96	1.98	2.04	V/V
	B	Full	1.95	1.99	2.05	V/V
Input Offset Voltage Common-Mode Rejection Ratio ($\Delta V_{CM} = \pm1.2V$)	A	+25°C	42	45	-	dB
	A	Full	40	-	-	dB
-3dB Bandwidth ($A_V = +1$, $+R_S = 620\Omega$, $V_{OUT} = 0.2V_{P-P}$)	B	+25°C	-	240	-	MHz
-3dB Bandwidth ($A_V = +2$, $V_{OUT} = 0.2V_{P-P}$)	B	+25°C	-	350	-	MHz
-3dB Bandwidth ($A_V = -1$, $V_{OUT} = 0.2V_{P-P}$)	B	+25°C	-	300	-	MHz
Gain Flatness (to 25MHz, $V_{OUT} = 0.2V_{P-P}$, $A_V = +2$)	B	+25°C	-	±0.03	-	dB
Gain Flatness (to 50MHz, $V_{OUT} = 0.2V_{P-P}$, $A_V = +2$)	B	+25°C	-	±0.04	-	dB
OUTPUT CHARACTERISTICS						
Output Voltage Swing ($A_V = -1$)	A	+25°C	±3.0	±3.2	-	V
	A	Full	±2.8	-	-	V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 2) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
Output Current - implied by output voltage swing into 50Ω ($A_V = -1$, $R_L = 50\Omega$)	A	+25°C, +85°C	50	55	-	mA
	A	-40°C	28	-	-	mA
Output Short Circuit Current ($A_V = -1$)	B	+25°C	-	90	-	mA
Second Harmonic Distortion (20MHz, $V_{OUT} = 2V_{P-P}$, $A_V = +2$)	B	+25°C	-	50	-	dBc
Third Harmonic Distortion (20MHz, $V_{OUT} = 2V_{P-P}$, $A_V = +2$)	B	+25°C	-	50	-	dBc
TRANSIENT RESPONSE						
Rise Time ($V_{OUT} = 0.5V_{P-P}$, $A_V = +2$)	B	+25°C	-	1.1	-	ns
Overshoot (V_{OUT} = 0V to 0.5V, $A_V = +2$, V_{IN} $t_{RISE} = 1.0ns$)	B	+25°C	-	5	-	%
Slew Rate ($V_{OUT} = 4V_{P-P}$, $A_V = +1$, $+R_S = 620\Omega$)	B	+25°C	-	850	-	V/μs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = +2$)	B	+25°C	-	900	-	V/μs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = -1$)	B	+25°C	-	1100	-	V/μs
0.1% Settling Time (V_{OUT} = +2V to 0V step, $A_V = +2$)	B	+25°C	-	15	-	ns
Overload Recovery Time ($A_V = +2$, V_{IN} = ±2V to 0V step)	B	+25°C	-	8	-	ns
VIDEO CHARACTERISTICS						
Differential Gain (f = 3.58MHz, $A_V = +2$, $R_L = 150\Omega$)	B	+25°C	-	0.025	-	%
Differential Phase (f = 3.58MHz, $A_V = +2$, $R_L = 150\Omega$)	B	+25°C	-	0.02	-	Degrees
POWER SUPPLY CHARACTERISTICS						
Power Supply Range	C	+25°C	±4.5	-	±5.5	V
Power Supply Current	A	+25°C	5.4	5.9	6.1	mA/ Op Amp
	A	Full	-	-	6.3	mA/ Op Amp
Non-Inverting Input Bias Current Power Supply Sensitivity ($\Delta V_{PS} = \pm1.25V$)	A	+25°C	-	0.5	1	μA/V
	A	Full	-	-	3	μA/V
Input Offset Voltage Power Supply Rejection Ratio ($\Delta V_{PS} = \pm1.25V$)	A	+25°C	45	49	-	dB
	A	Full	43	-	-	dB

NOTES:

1. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 30mA for maximum reliability.
2. Test Level: A. Production Tested.; B. Guaranteed Limit or Typical Based on Characterization.; C. Design Typical for Information Only.

Application Information

Closed Loop Gain Selection

The HFA1X12 feature a novel design which allows the user to select from three closed loop gains, without any external components. The result is a more flexible product, fewer part types in inventory, and more efficient use of board space.

This "buffer" operates in closed loop gains of -1, +1, or +2, and gain selection is accomplished via connections to the ±inputs. Applying the input signal to +IN and floating -IN selects a gain of +1 (see next section for layout caveats), while grounding -IN selects a gain of +2. A gain of -1 is obtained by applying the input signal to -IN with +IN grounded through a 50Ω resistor.

The table below summarizes these connections:

GAIN (A_{CL})	CONNECTIONS	
	+INPUT	-INPUT
-1	50Ω to GND	Input
+1	Input	NC (Floating)
+2	Input	GND

Unity Gain Considerations

Unity gain selection is accomplished by floating the -Input of the buffer. Anything that tends to short the -Input to GND, such as stray capacitance at high frequencies, will cause the amplifier gain to increase toward a gain of +2. The result is excessive high frequency peaking, and possible instability. Even the minimal amount of capacitance associated with attaching the -Input lead to the PCB results in approximately 3dB of gain peaking. At a minimum this requires due care to ensure the minimum capacitance at the -Input connection.

There are at least three alternate methods for configuring the HFA1X12 as a unity gain buffer. The implementations vary in complexity and involve performance trade-offs. The easiest approach to implement is simply shorting the two input pins together, and applying the input signal to this common node. The amplifier bandwidth decreases, but excellent gain flatness is the benefit. Another drawback to this approach is that the amplifier input noise voltage and input offset voltage terms see a gain of +2, resulting in higher noise and output offset voltages. Alternately, a 100pF capacitor between the inputs shorts them only at high frequencies, which prevents the increased output offset voltage but delivers less gain flatness.

Another straightforward approach is to add a 620Ω resistor in series with the positive input. This resistor and the buffer's input capacitance form a low pass filter which rolls off the signal bandwidth before gain peaking occurs. This configuration was employed to obtain the datasheet AC and transient parameters for a gain of +1.

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value chip (0.1µF) capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Output capacitance must be minimized, or isolated as discussed in the "Driving Capacitive Loads" section.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 350MHz. By decreasing R_S as C_L increases the maximum bandwidth is obtained without sacrificing stability.

HARRIS SEMICONDUCTOR

HFA1245

Dual, High-Speed, Low Power, Video Operational Amplifier with Disable

July 1995

Features

- Low Supply Current . . . . 5.8mA/Op Amp
- High Input Impedance 2MΩ
- Low Crosstalk (5MHz) . . . . -73dB
- High Off Isolation (5MHz) . . . . -61dB
- Wide -3dB Bandwidth (A_V = +2) 530MHz
- Very Fast Slew Rate 1050V/µs
- Gain Flatness (to 50MHz) . . . . ±0.11dB
- Differential Gain 0.02%
- Differential Phase . . . . 0.03Deg.
- Individual Output Enable/Disable
- Output Enable/Disable Time 160ns/20ns
- Pin Compatible Upgrade to HA5022

Applications

- Flash A/D Drivers
- High Resolution Monitors
- Video Multiplexers
- Video Switching and Routing
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications
- High Speed Oscilloscopes and Analyzers

Description

The HFA1245 is a dual, high speed, low power current feedback amplifier built with Harris' proprietary complementary bipolar UHF-1 process.

The HFA1245 features individual TTL/CMOS compatible disable controls. When pulled low they disable the corresponding amplifier, which reduces the supply current and forces the output into a high impedance state. This feature allows easy implementation of simple, low power video switching and routing systems. Component and composite video systems also benefit from this op amp's excellent gain flatness, and good differential gain and phase specifications.

Multiplexed A/D applications will also find the HFA1245 useful as the A/D driver/multiplexer.

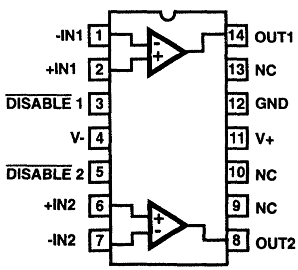
The HFA1245 is a low power, high performance upgrade for the popular Harris HA5022. For a dual amplifier without disable, in a standard 8 lead pinout, please see the HFA1205 data sheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1245IP	-40°C to +85°C	14 Lead Plastic DIP
HFA1245IB	-40°C to +85°C	14 Lead Plastic SOIC (N)

Pinout

HFA1245
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3682.1

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 2) . . . . Short Circuit Protected
. . . . 30mA Continuous
. . . . 60mA ≤ 50% Duty Cycle
Junction Temperature (Die Only) . . . . +175°C
Junction Temperature (Plastic Package) . . . . +150°C
ESD Rating. . . . . >2000V
Lead Temperature (Soldering 10s). +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range . . . . $-40^oC \le T_A \le +85^oC$
Storage Temperature Range. . . . . $-65^oC \le T_A \le +150^oC$
Thermal Package Characteristics θ_{JA}
Plastic DIP. . . . . 100°C/W
SOIC . . . . 120°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 560\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified

PARAMETER		(NOTE 1) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	+25°C	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	$\Delta V_{CM} = \pm1.8V$	A	+25°C	45	48	-	dB
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	43	46	-	dB
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	43	46	-	dB
Input Offset Voltage Power Supply Rejection Ratio	$\Delta V_{PS} = \pm1.8V$	A	+25°C	48	52	-	dB
	$\Delta V_{PS} = \pm1.8V$	A	+85°C	46	50	-	dB
	$\Delta V_{PS} = \pm1.2V$	A	-40°C	46	50	-	dB
Non-Inverting Input Bias Current		A	+25°C	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	+25°C	-	0.5	1	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	+85°C	-	0.8	3	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40°C	-	0.8	3	µA/V
Non-Inverting Input Resistance	$\Delta V_{CM} = \pm1.8V$	A	+25°C	0.8	2	-	MΩ
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	0.5	1.3	-	MΩ
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	0.5	1.3	-	MΩ
Inverting Input Bias Current		A	+25°C	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/°C
Inverting Input Bias Current Common-Mode Sensitivity	$\Delta V_{CM} = \pm1.8V$	A	+25°C	-	3	6	µA/V
	$\Delta V_{CM} = \pm1.8V$	A	+85°C	-	4	8	µA/V
	$\Delta V_{CM} = \pm1.2V$	A	-40°C	-	4	8	µA/V
Inverting Input Bias Current Power Supply Sensitivity	$\Delta V_{PS} = \pm1.8V$	A	+25°C	-	2	5	µA/V
	$\Delta V_{PS} = \pm1.8V$	A	+85°C	-	4	8	µA/V
	$\Delta V_{PS} = \pm1.2V$	A	-40°C	-	4	8	µA/V
Inverting Input Resistance		C	+25°C	-	40	-	Ω

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 560\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 1) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
Input Capacitance (either input)		C	+25°C	-	2.5	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	+25°C, +85°C	±1.8	±2.4	-	V
		A	-40°C	±1.2	±1.7	-	V
Input Noise Voltage Density (f = 100kHz)		B	+25°C	-	3.5	-	$nV/\sqrt{Hz}$
Non-Inverting Input Noise Current Density (f = 100kHz)		B	+25°C	-	2.5	-	$pA/\sqrt{Hz}$
Inverting Input Noise Current Density (f = 100kHz)		B	+25°C	-	20	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain (A_V = -1)		C	+25°C	-	500	-	kΩ
AC CHARACTERISTICS $A_V = +2$, $R_F = 560\Omega$, Unless Otherwise Specified							
-3dB Bandwidth ($V_{OUT} = 0.2V_{P-P}$)	$A_V = +1$, $+R_S = 560\Omega$	B	+25°C	-	290	-	MHz
	$A_V = +2$	B	+25°C	-	530	-	MHz
	$A_V = -1$, $R_F = 510\Omega$	B	+25°C	-	230	-	MHz
Full Power Bandwidth ($V_{OUT} = 5V_{P-P}$ at $A_V = +2/-1$, $4V_{P-P}$ at $A_V = +1$)	$A_V = +1$, $+R_S = 560\Omega$	B	+25°C	-	150	-	MHz
	$A_V = +2$	B	+25°C	-	130	-	MHz
	$A_V = -1$, $R_F = 510\Omega$	B	+25°C	-	120	-	MHz
Gain Flatness ($A_V = +2$, $V_{OUT} = 0.2V_{P-P}$)	To 25MHz	B	+25°C	-	±0.04	-	dB
	To 50MHz	B	+25°C	-	±0.11	-	dB
Minimum Stable Gain		A	Full	-	1	-	V/V
Crosstalk (Note 3)	5MHz	B	+25°C	-	-73	-	dB
	10MHz	B	+25°C	-	-64	-	dB
OUTPUT CHARACTERISTICS $R_F = 560\Omega$, Unless Otherwise Specified							
Output Voltage Swing ($A_V = -1$, $R_L = 100\Omega$)		A	+25°C	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current ($A_V = -1$, $R_L = 50\Omega$)		A	+25°C, +85°C	50	60	-	mA
		A	-40°C	28	42	-	mA
Output Short Circuit Current		B	+25°C	-	90	-	mA
DC Closed Loop Output Impedance ($A_V = +2$, $R_F = 560\Omega$)		B	+25°C	-	0.07	-	Ω
Second Harmonic Distortion ($A_V = +2$, $R_F = 560\Omega$, $V_{OUT} = 2V_{P-P}$)	10MHz	B	+25°C	-	-50	-	dBc
	20MHz	B	+25°C	-	-45	-	dBc
Third Harmonic Distortion ($A_V = +2$, $R_F = 560\Omega$, $V_{OUT} = 2V_{P-P}$,)	10MHz	B	+25°C	-	-55	-	dBc
	20MHz	B	+25°C	-	-50	-	dBc
TRANSIENT CHARACTERISTICS $A_V = +2$, $R_F = 560\Omega$, Unless Otherwise Specified							
Rise and Fall Times ($V_{OUT} = 0.5V_{P-P}$)	Rise Time	B	+25°C	-	0.65	-	ns
	Fall Time	B	+25°C	-	1.20	-	ns
Overshoot ($V_{OUT} = 0.5V_{P-P}$, V_{IN} t_{RISE} = 1.0ns)		B	+25°C	-	7	-	%
Slew Rate ($V_{OUT} = 4V_{P-P}$, $A_V = +1$, $+R_S = 560\Omega$)	+SR	B	+25°C	-	1050	-	V/µs
	-SR	B	+25°C	-	800	-	V/µs
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = +2$)	+SR	B	+25°C	-	1400	-	V/µs
	-SR	B	+25°C	-	900	-	V/µs

Electrical Specifications $V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 560\Omega$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 1) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
Slew Rate ($V_{OUT} = 5V_{P-P}$, $A_V = -1$, $R_F = 510\Omega$)	+SR	B	+25°C	-	1950	-	V/µs
	-SR	B	+25°C	-	1050	-	V/µs
Settling Time ($V_{OUT} = +2V$ to 0V step)	To 0.1%	B	+25°C	-	15	-	ns
	To 0.05%	B	+25°C	-	20	-	ns
	To 0.02%	B	+25°C	-	30	-	ns
Overdrive Recovery Time ($V_{IN} = \pm2V$)		B	+25°C	-	8.5	-	ns
VIDEO CHARACTERISTICS $A_V = +2$, $R_F = 560\Omega$, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	$R_L = 150\Omega$	B	+25°C	-	0.02	-	%
	$R_L = 75\Omega$	B	+25°C	-	0.03	-	%
Differential Phase (f = 3.58MHz)	$R_L = 150\Omega$	B	+25°C	-	0.03	-	Degrees
	$R_L = 75\Omega$	B	+25°C	-	0.05	-	Degrees
DISABLE CHARACTERISTICS							
Disabled Supply Current ($V_{\overline{DISABLE}} = 0V$)		A	Full	-	3	4	mA/ Op Amp
$\overline{\text{DISABLE}}$ Input Logic Low Voltage		A	Full	-	-	0.8	V
$\overline{\text{DISABLE}}$ Input Logic High Voltage		A	+25°C, +85°C	2.0	-	-	V
		A	-40°C	2.4	-	-	V
$\overline{\text{DISABLE}}$ Input Logic Low Current ($V_{\overline{DISABLE}} = 0V$)		A	Full	-	100	200	µA
$\overline{\text{DISABLE}}$ Input Logic High Current ($V_{\overline{DISABLE}} = 5V$)		A	Full	-	1	15	µA
Output Disable Time ($V_{IN} = \pm1V$, $V_{\overline{DISABLE}} = 2.4V$ to 0V)		B	+25°C	-	20	-	ns
Output Enable Time ($V_{IN} = \pm1V$, $V_{\overline{DISABLE}} = 0V$ to 2.4V)		B	+25°C	-	160	-	ns
Disabled Output Capacitance ($V_{\overline{DISABLE}} = 0V$)		B	+25°C	-	3.8	-	pF
Disabled Output Leakage ($V_{\overline{DISABLE}} = 0V$, $V_{IN} = \mp2V$, $V_{OUT} = \pm3V$)		A	Full	-	2	10	µA
Off Isolation ($V_{\overline{DISABLE}} = 0V$, $V_{IN} = 1V_{P-P}$, $A_V = +2$)	at 5MHz	B	+25°C	-	-61	-	dB
	at 10MHz	B	+25°C	-	-55	-	dB
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	+25°C	±4.5	-	±5.5	V
Power Supply Current		A	+25°C	5.6	5.8	6.1	mA/ Op Amp
		A	Full	5.4	5.9	6.3	mA/ Op Amp

NOTES:

1. Test Level: A. Production Tested.; B. Guaranteed Limit or Typical Based on Characterization.; C. Design Typical for Information Only.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.
3. The typical use for these amplifiers is in multiplexed configurations, where one amplifier (hostile channel) is enabled, and the passive channel is disabled. The crosstalk data specified is tested in this manner, with the input signal applied to the hostile channel, while monitoring the output of the passive channel. Crosstalk performance with both the hostile and passive channels enabled is typically: -63dB at 5MHz, and -50dB at 10MHz.

Die Characteristics

DIE DIMENSIONS:

69 x 92 x 19 ± 1mils

1750µm x 2330µm ± 25.4µm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

GLASSIVATION:

Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

DIE ATTACH:

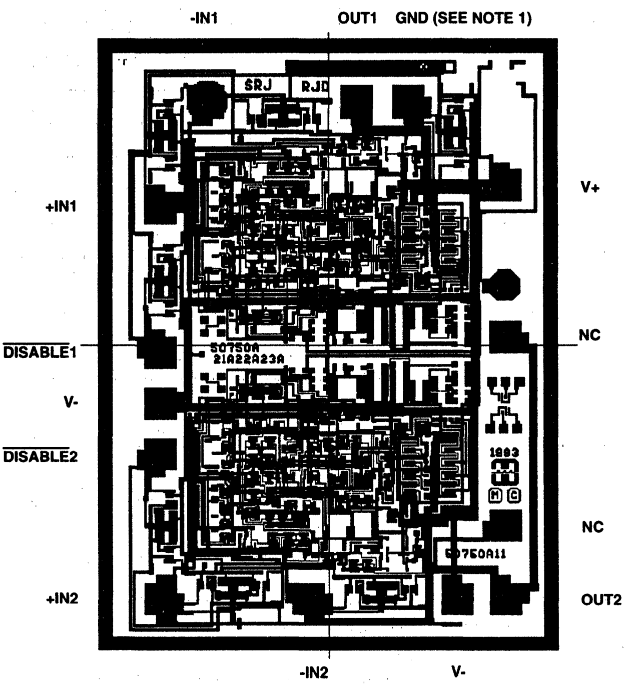
Material: Epoxy - Plastic DIP and SOIC

TRANSISTOR COUNT: 180

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1245



NOTE:

1. This is an optional GND pad. Users may set a GND reference, via this pad, to ensure the TTL compatibility of the DISABLE inputs when using asymmetrical supplies (e.g. V+ = 10V, V- = 0V). See the "Application Information" section for details.

Application Information

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1245 design is optimized for a 560Ω R_F at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For good channel-to-channel gain matching, it is recommended that all resistors (termination as well as gain setting) be ±1% tolerance or better. Note that a series input resistor, on +IN, is required for a gain of +1, to reduce gain peaking and increase stability.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	510	230
+1	560 (+R_S = 560Ω)	290
+2	560	530

Non-inverting Input Source Impedance

For best operation, the D.C. source impedance looking out of the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

Optional GND Pin for TTL Compatibility

The HFA1245 derives an internal GND reference for the digital circuitry as long as the power supplies are symmetrical about GND. The GND reference is used to ensure the TTL compatibility of the $\overline{\text{DISABLE}}$ inputs. With symmetrical supplies the GND pin (Pin 12) may be floated, or connected directly to GND. If asymmetrical supplies (e.g. +10V, 0V) are utilized, and TTL compatibility is desired, the GND pin must be connected to GND.

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. To this end, it is recommended that the ground plane be removed under traces connected to -IN, and connections to -IN should be kept as short as possible.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 290MHz (for A_V = +1). By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve. For example, at A_V = +1, R_S = 62Ω, C_L = 40pF, the overall bandwidth is limited to 180MHz, and bandwidth drops to 70MHz at A_V = +1, R_S = 8Ω, C_L = 400pF.

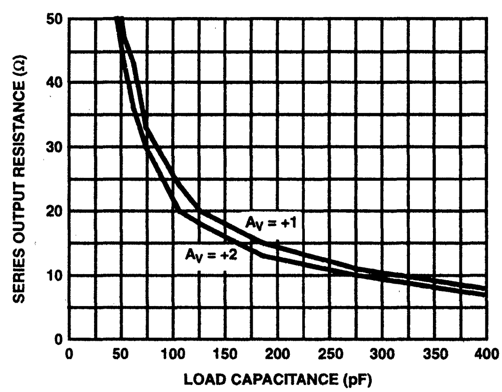


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

2 OPERATIONAL AMPLIFIERS

HARRIS SEMICONDUCTOR

HFA1405

Quad, High-Speed, Low Power, Video Operational Amplifier

July 1995

Features

- **Low Supply Current . . . . 5.8mA/Op Amp**
- **High Input Impedance 1MΩ**
- **Wide -3dB Bandwidth (A_V = +2) 560MHz**
- **Very Fast Slew Rate 1700V/µs**
- **Gain Flatness (to 50MHz) . . . . ±0.03dB**
- **Differential Gain 0.02%**
- **Differential Phase . . . . 0.03 Degrees**
- **All Hostile Crosstalk (5MHz) . . . . -60dB**
- **Pin Compatible Upgrade to HA5025 and CLC414**

Applications

- **Flash A/D Drivers**
- **Professional Video Processing**
- **Video Digitizing Boards/Systems**
- **Multimedia Systems**
- **RGB Preamps**
- **Medical Imaging**
- **Hand Held and Miniaturized RF Equipment**
- **Battery Powered Communications**
- **High Speed Oscilloscopes and Analyzers**

Description

The HFA1405 is a quad, high speed, low power current feedback amplifier built with Harris' proprietary complementary bipolar UHF-1 process.

These amplifiers deliver 560MHz bandwidth and 1700V/µs slew rate, on only 58mW of quiescent power. They are specifically designed to meet the performance, power, and cost requirements of high volume video applications. The excellent gain flatness and differential gain/phase performance make these amplifiers well suited for component or composite video applications. Video performance is maintained even when driving a back terminated cable (R_L = 150Ω), and degrades only slightly when driving two back terminated cables (R_L = 75Ω). RGB applications will benefit from the high slew rates, and high full power bandwidth.

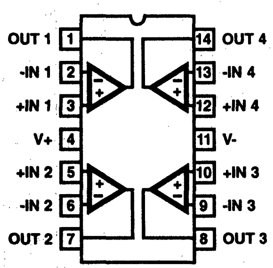
The HFA1405 is a pin compatible, low power, high performance upgrade for the popular Harris HA5025, and for the CLC414.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA1405IB	-40°C to +85°C	14 Lead Plastic SOIC (N)

Pinout

HFA1405
(SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3604.2**

Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . V_{SUPPLY}
Differential Input Voltage 5V
Output Current (Note 2) . . . . Short Circuit Protected
. . . . 30mA Continuous
. . . . .60mA ≤ 50% Duty Cycle
Junction Temperature (Die Only) . . . . +175°C
Junction Temperature (Plastic Package) . . . . +150°C
ESD Rating. . . . . >2000V
Lead Temperature (Soldering 10s). +300°C
(Lead Tips Only)

Operating Conditions

Operating Temperature Range . . . . -40°C ≤ T_A ≤ +85°C
Storage Temperature Range. . . . .-65°C ≤ T_A ≤ +150°C
Thermal Package Characteristics θ_{JA}
SOIC Package. . . . . 120°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified

PARAMETER		(NOTE 1) TEST LEVEL	TEMPERATURE	HFA1405IB			UNITS
				MIN	TYP	MAX	
INPUT CHARACTERISTICS							
Input Offset Voltage		A	+25°C	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/°C
Input Offset Voltage Common-Mode Rejection Ratio	ΔV_{CM} = ±1.8V	A	+25°C	45	48	-	dB
	ΔV_{CM} = ±1.8V	A	+85°C	43	46	-	dB
	ΔV_{CM} = ±1.2V	A	-40°C	43	46	-	dB
Input Offset Voltage Power Supply Rejection Ratio	ΔV_{PS} = ±1.8V	A	+25°C	48	52	-	dB
	ΔV_{PS} = ±1.8V	A	+85°C	46	48	-	dB
	ΔV_{PS} = ±1.2V	A	-40°C	46	48	-	dB
Non-Inverting Input Bias Current		A	+25°C	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/°C
Non-Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	+25°C	-	0.5	1	µA/V
	ΔV_{PS} = ±1.8V	A	+85°C	-	0.8	3	µA/V
	ΔV_{PS} = ±1.2V	A	-40°C	-	0.8	3	µA/V
Non-Inverting Input Resistance	ΔV_{CM} = ±1.8V	A	+25°C	0.8	1.2	-	MΩ
	ΔV_{CM} = ±1.8V	A	+85°C	0.5	0.8	-	MΩ
	ΔV_{CM} = ±1.2V	A	-40°C	0.5	0.8	-	MΩ
Inverting Input Bias Current		A	+25°C	-	2	7.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/°C
Inverting Input Bias Current Common-Mode Sensitivity	ΔV_{CM} = ±1.8V	A	+25°C	-	3	6	µA/V
	ΔV_{CM} = ±1.8V	A	+85°C	-	4	8	µA/V
	ΔV_{CM} = ±1.2V	A	-40°C	-	4	8	µA/V
Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	+25°C	-	2	5	µA/V
	ΔV_{PS} = ±1.8V	A	+85°C	-	4	8	µA/V
	ΔV_{PS} = ±1.2V	A	-40°C	-	4	8	µA/V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 1) TEST LEVEL	TEMPERATURE	HFA1405IB MIN	TYP	MAX	UNITS
Inverting Input Resistance		C	+25°C	-	60	-	Ω
Input Capacitance (any input)		B	+25°C	-	1.4	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	+25°C, +85°C	±1.8	±2.4	-	V
		A	-40°C	±1.2	±1.7	-	V
Input Noise Voltage Density (f = 100kHz)		B	+25°C	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density (f = 100kHz)		B	+25°C	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density (f = 100kHz)		B	+25°C	-	20	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain (A_V = -1)		C	+25°C	-	500	-	kΩ
AC CHARACTERISTICS R_F = 510Ω, Unless Otherwise Specified							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P})	A_V = -1, R_F = 360Ω	B	+25°C	-	420	-	MHz
	A_V = +2	B	+25°C	-	560	-	MHz
	A_V = +6, R_F = 500Ω	B	+25°C	-	140	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P})	A_V = -1, R_F = 360Ω	B	+25°C	-	260	-	MHz
	A_V = +2	B	+25°C	-	165	-	MHz
	A_V = +6, R_F = 500Ω	B	+25°C	-	150	-	MHz
Gain Flatness (A_V = -1, R_F = 360Ω, V_{OUT} = 0.2V_{P-P})	to 25MHz	B	+25°C	-	±0.03	-	dB
	to 50MHz	B	+25°C	-	±0.04	-	dB
Gain Flatness (A_V = +2, V_{OUT} = 0.2V_{P-P})	to 25MHz	B	+25°C	-	±0.03	-	dB
	to 50MHz	B	+25°C	-	±0.03	-	dB
Gain Flatness (A_V = +6, R_F = 500Ω, V_{OUT} = 0.2V_{P-P})	to 15MHz	B	+25°C	-	±0.08	-	dB
	to 30MHz	B	+25°C	-	±0.19	-	dB
Minimum Stable Gain		A	Full	-	1	-	V/V
Crosstalk (All Channels Hostile)	5MHz	B	+25°C	-	-60	-	dB
	10MHz	B	+25°C	-	-56	-	dB
OUTPUT CHARACTERISTICS A_V = +2, R_F = 510Ω, Unless Otherwise Specified							
Output Voltage Swing (A_V = -1, R_L = 100Ω)		A	+25°C	±3	±3.4	-	V
		A	Full	±2.8	±3	-	V
Output Current (A_V = -1, R_L = 50Ω)		A	+25°C, +85°C	50	60	-	mA
		A	-40°C	28	42	-	mA
Output Short Circuit Current		B	+25°C	-	90	-	mA
DC Closed Loop Output Impedance		B	+25°C	-	0.2	-	Ω
Second Harmonic Distortion (V_{OUT} = 2V_{P-P})	10MHz	B	+25°C	-	-51	-	dBc
	20MHz	B	+25°C	-	-46	-	dBc

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 510Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 1) TEST LEVEL	TEMPERATURE	HFA1405IB MIN	TYP	MAX	UNITS
Third Harmonic Distortion (V_{OUT} = $2V_{P-P}$)	10MHz	B	+25°C	-	-63	-	dBc
	20MHz	B	+25°C	-	-56	-	dBc
TRANSIENT CHARACTERISTICS A_V = +2, R_F = 510Ω, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = $0.5V_{P-P}$)	A_V = +2	B	+25°C	-	0.8	-	ns
	A_V = +6, R_F = 500Ω	B	+25°C	-	2.9	-	ns
Overshoot (Note 3) (A_V = -1, R_F = 360Ω, V_{OUT} = $2V_{P-P}$, V_{IN} t_{RISE} = 1ns)	+OS	B	+25°C	-	13	-	%
	-OS	B	+25°C	-	21	-	%
Overshoot (Note 3) (A_V = +2, V_{OUT} = $2V_{P-P}$, V_{IN} t_{RISE} = 1ns)	+OS	B	+25°C	-	13	-	%
	-OS	B	+25°C	-	16	-	%
Overshoot (A_V = +6, R_F = 500Ω, V_{OUT} = $2V_{P-P}$, V_{IN} t_{RISE} = 1ns)	+OS	B	+25°C	-	0	-	%
	-OS	B	+25°C	-	2	-	%
Slew Rate (V_{OUT} = $5V_{P-P}$, A_V = -1, R_F = 360Ω)	+SR	B	+25°C	-	2500	-	V/µs
	-SR	B	+25°C	-	1900	-	V/µs
Slew Rate (V_{OUT} = $5V_{P-P}$, A_V = +2)	+SR	B	+25°C	-	1700	-	V/µs
	-SR	B	+25°C	-	1700	-	V/µs
Slew Rate (V_{OUT} = $5V_{P-P}$, A_V = +6, R_F = 500Ω)	+SR	B	+25°C	-	1500	-	V/µs
	-SR	B	+25°C	-	1100	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step)	To 0.1%	B	+25°C	-	23	-	ns
	To 0.05%	B	+25°C	-	30	-	ns
	To 0.025%	B	+25°C	-	37	-	ns
Overdrive Recovery Time (V_{IN} = ±2V)		B	+25°C	-	8.5	-	ns
VIDEO CHARACTERISTICS A_V = +2, R_F = 510Ω, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	+25°C	-	0.02	-	%
	R_L = 75Ω	B	+25°C	-	0.03	-	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	+25°C	-	0.03	-	Degrees
	R_L = 75Ω	B	+25°C	-	0.06	-	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	+25°C	±4.5	-	±5.5	V
Power Supply Current		A	+25°C	-	5.8	6.1	mA/Op Amp
		A	Full	-	5.9	6.3	mA/Op Amp

NOTES:

1. Test Level: A. Production Tested; B. Typical or Guaranteed Limit Based on Characterization; C. Design Typical for Information Only.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.
3. Undershoot dominates for output signal swings below GND (e.g. $2V_{P-P}$), yielding a higher overshoot limit compared to the V_{OUT} = 0V to 2V condition. See the "Application Information" section for details.

Application Information

Optimum Feedback Resistor

Although a current feedback amplifier's bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HFA1405 design is optimized for $R_F = 510\Omega$ at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback causes the same problems due to the feedback impedance decrease at higher frequencies). However, at higher gains the amplifier is more stable so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth. For good channel-to-channel gain matching, it is recommended that all resistors (termination as well as gain setting) be ±1% tolerance or better.

OPTIMUM FEEDBACK RESISTOR

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	360	420
+2	510	560
+6	500 (Note)	140

NOTE: $R_F = 500\Omega$ is not the optimum value. It was chosen to match the R_F of the CLC412, for performance comparison purposes. Performance at $A_V = +6$ may be increased by reducing R_F below 500Ω.

Non-inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be $\geq 50\Omega$. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

Pulse Undershoot

The HFA1405 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (see Figure 4 and Figure 7). This undershoot isn't present for small bipolar signals, or large positive signals (see Figure 3 and Figure 6).

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance, parasitic or planned, connected to the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and eventual instability. To reduce this capacitance the designer should remove the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 560MHz. By decreasing R_S as C_L increases (as illustrated in the curve), the maximum bandwidth is obtained without sacrificing stability. Even so, bandwidth does decrease as you move to the right along the curve.

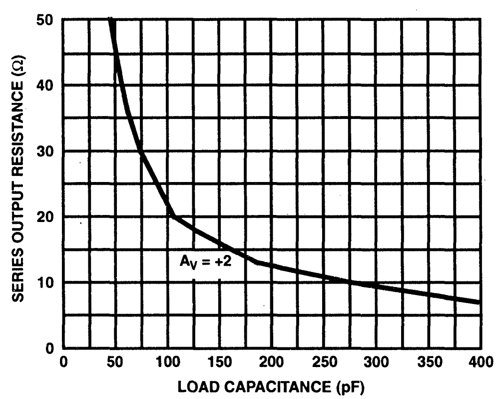


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Die Characteristics

DIE DIMENSIONS:

79 mils x 118 mils x 19 mils ±1mil
2000μm x 3000μm x 483μm ±25.4μm

METALLIZATION:

Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

GLASSIVATION:

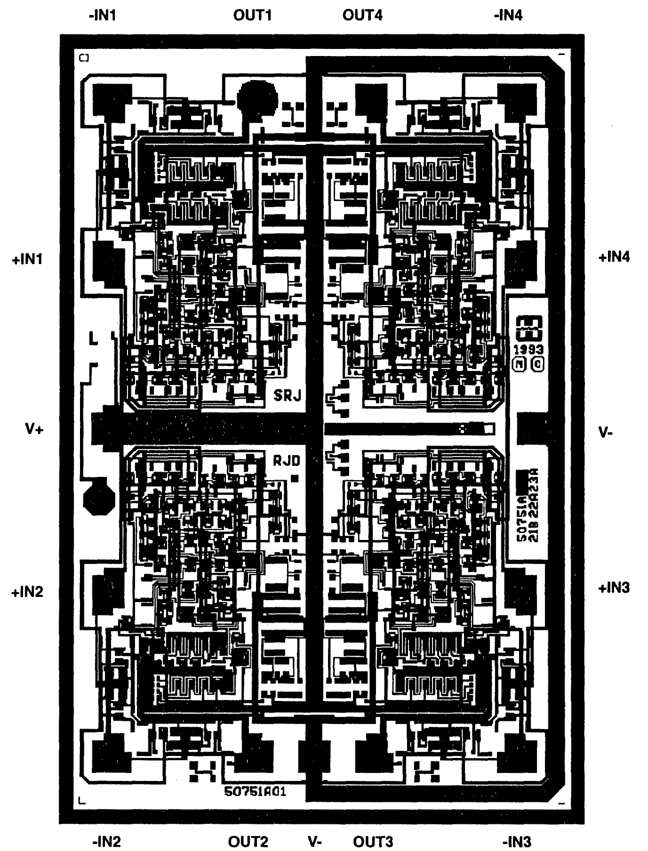
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT: 320

SUBSTRATE POTENTIAL (Powered Up): Floating (Recommend Connection to V-)

Metallization Mask Layout

HFA1405



Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified

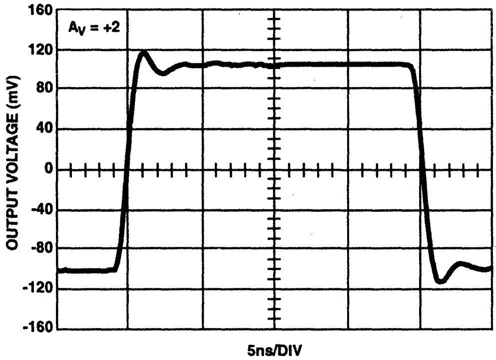


FIGURE 2. SMALL SIGNAL PULSE RESPONSE

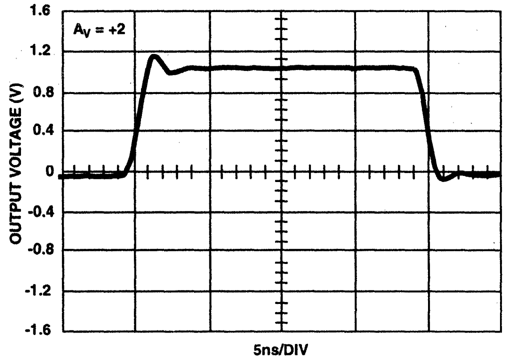


FIGURE 3. LARGE SIGNAL PULSE RESPONSE

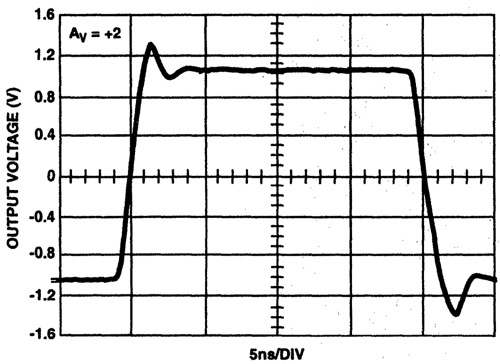


FIGURE 4. LARGE SIGNAL PULSE RESPONSE

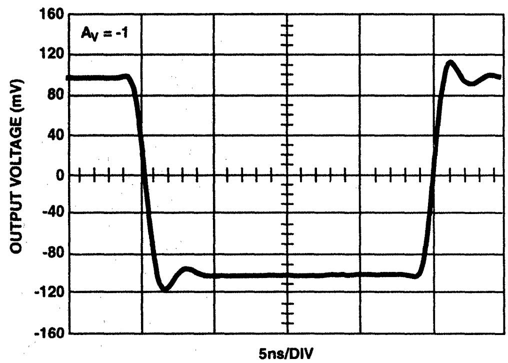


FIGURE 5. SMALL SIGNAL PULSE RESPONSE

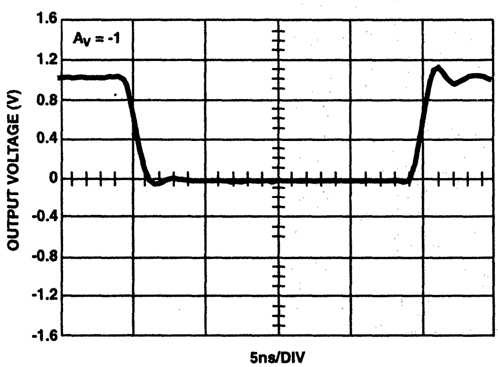


FIGURE 6. LARGE SIGNAL PULSE RESPONSE

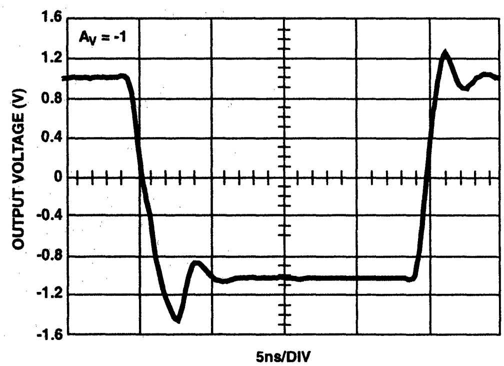


FIGURE 7. LARGE SIGNAL PULSE RESPONSE

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, R_F = Value From the Optimum Feedback Resistor Table, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

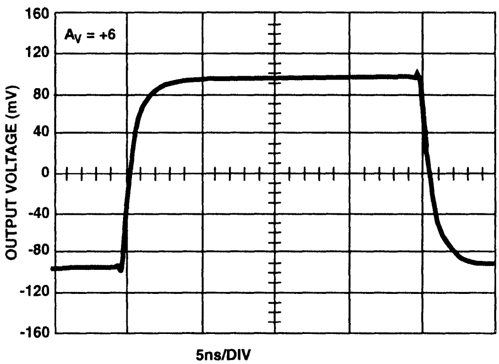


FIGURE 8. SMALL SIGNAL PULSE RESPONSE

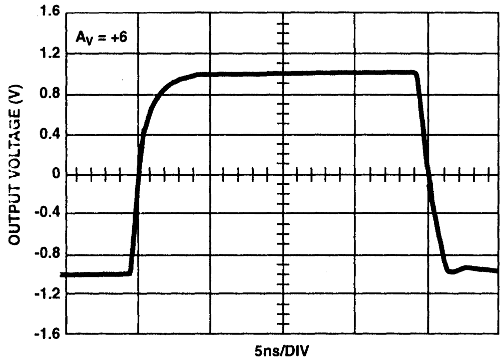


FIGURE 9. LARGE SIGNAL PULSE RESPONSE

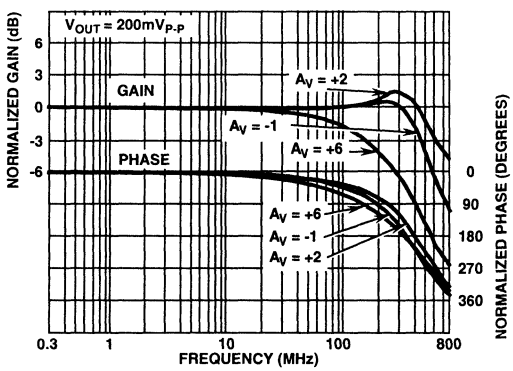


FIGURE 10. FREQUENCY RESPONSE

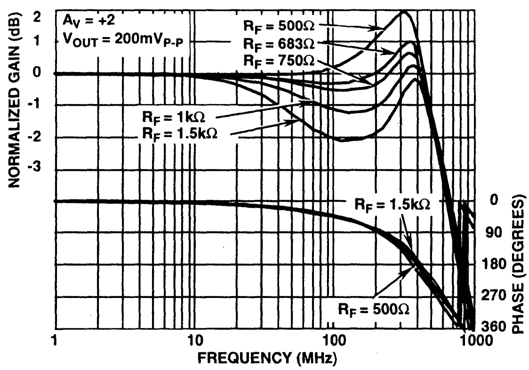


FIGURE 11. FREQUENCY RESPONSE vs FEEDBACK RESISTOR

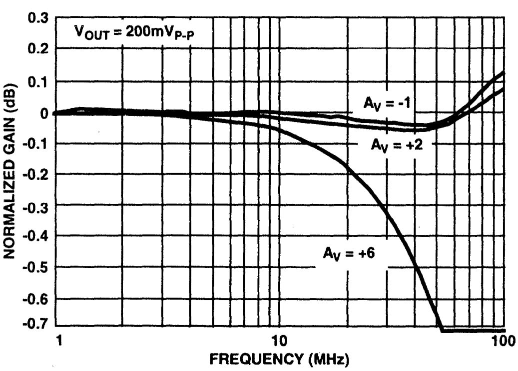


FIGURE 12. GAIN FLATNESS

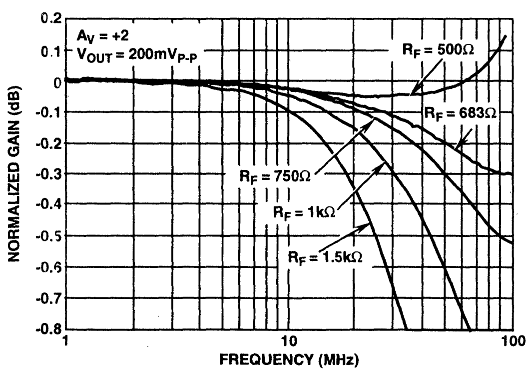


FIGURE 13. GAIN FLATNESS vs FEEDBACK RESISTOR

Typical Performance Curves V_{SUPPLY} = ±5V, T_A = +25°C, R_F = Value From the Optimum Feedback Resistor Table, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

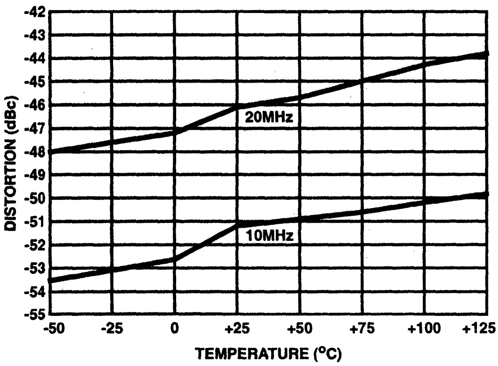


FIGURE 14. 2nd HARMONIC DISTORTION vs TEMPERATURE

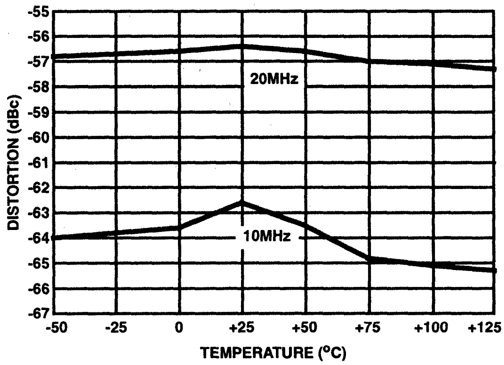


FIGURE 15. 3rd HARMONIC DISTORTION vs TEMPERATURE

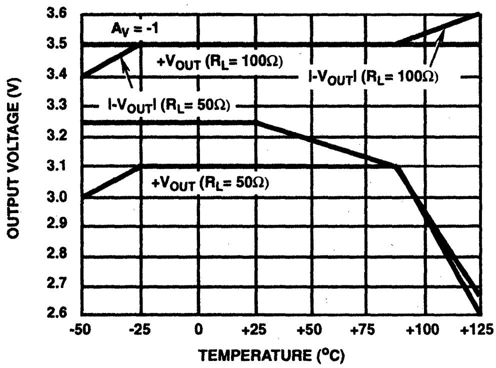


FIGURE 16. OUTPUT VOLTAGE vs TEMPERATURE

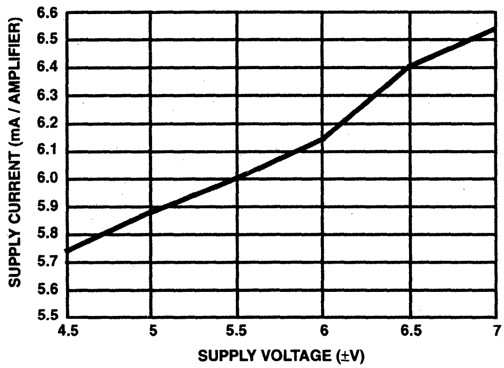


FIGURE 17. SUPPLY CURRENT vs SUPPLY VOLTAGE

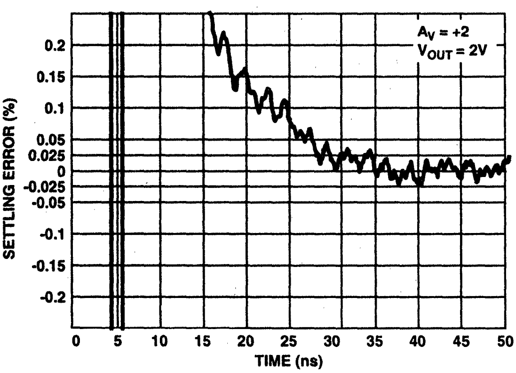


FIGURE 18. SETTLING RESPONSE

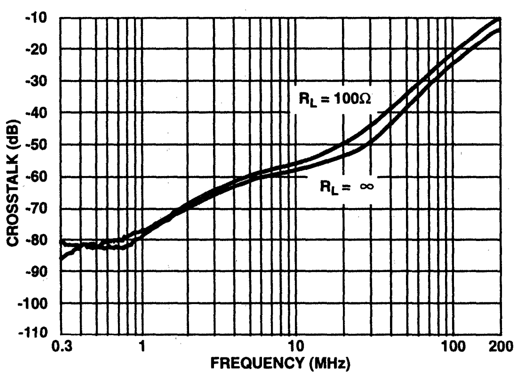


FIGURE 19. ALL HOSTILE CROSSTALK

SIGNAL PROCESSING NEW RELEASES 3

SAMPLE AND HOLD AMPLIFIERS

HARRIS SEMICONDUCTOR

HA5351

July 1995

Fast Acquisition Sample and Hold Amplifier

Features

- Fast Acquisition to 0.01% . . . . 70ns (Max)
- Low Offset Error. . . . . ±2mV (Max)
- Low Pedestal Error . . . . ±10mV (Max)
- Low Droop Rate . . . . 2μV/μs (Max)
- Wide Unity Gain Bandwidth 40MHz
- Low Power Dissipation . . . . 220mW (Max)
- Total Harmonic Distortion (Hold Mode) . . . . -72dBc (V_{IN} = $5V_{P-P}$ at 1MHz)
- Fully Differential Inputs
- On Chip Hold Capacitor

Applications

- Synchronous Sampling
- Wide Bandwidth A/D Conversion
- Deglitching
- Peak Detection
- High Speed DC Restore

Description

The HA5351 is a fast acquisition, wide bandwidth sample and hold amplifier, built with the Harris HBC-10 BiCMOS process. This sample and hold amplifier offers a combination of desirable features; fast acquisition time (70ns to 0.01% maximum), excellent DC precision and extremely low power dissipation, making it ideal for use in systems that sample multiple signals and require low power. For systems with multiple channels, consider the Dual HA5352 sample and hold amplifier.

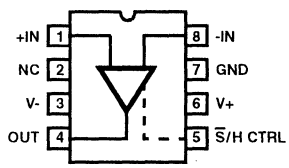
The HA5351 is in an open loop configuration with fully differential inputs providing flexibility for user defined feedback. In unity gain the HA5351 is completely self-contained and requires no external components. The on-chip 15pF hold capacitor is completely isolated to minimizing droop rate and reduce sensitivity to pedestal error. The HA5351 is available in 8 lead PDIP and SOIC packages for minimizing board space and ease of layout.

Ordering Information

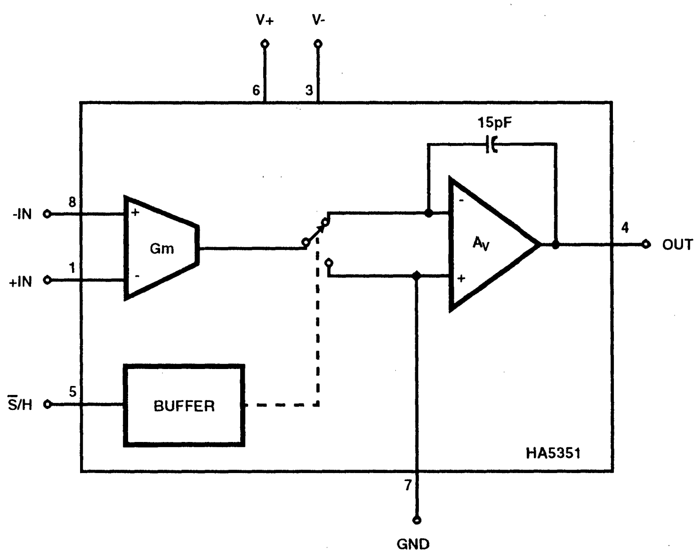
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA5351IP	-40°C to +85°C	8 Lead Plastic DIP
HA5351IB	-40°C to +85°C	8 Lead SOIC (N)

Pinout

HA5351 (PDIP, SOIC) TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals . . . . +11V
Differential Input Voltage . . . . +6V
Voltage Between Sample and Hold Control and Ground . . . . . +5.5V
Output Current, Continuous . . . . ±37mA
Junction Temperature (Plastic Packages) . . . . +150°C
Lead Soldering Temperature (Soldering 10s). . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HA5351I. . . . . $-40^oC \le T_A \le +85^oC$
Storage Temperature Range. . . . . $-65^oC \le T_A \le +150^oC$

Thermal Resistance	θ_{JA}
Plastic DIP	120°C/W
SOIC	160°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions: V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), C_L = 5pF, Unless Otherwise Specified

PARAMETERS		TEMP	HA5351I MIN	HA5351I TYP	HA5351I MAX	UNITS
INPUT CHARACTERISTICS						
Input Voltage Range		Full	-2.5	-	+2.5	V
Input Resistance (Note 2)		+25°C	100	500	-	kΩ
Input Capacitance		+25°C	-	-	5	pF
Input Offset Voltage		+25°C	-2	-	2	mV
		Full	-3.0	-	3.0	mV
Offset Voltage Temperature Coefficient		Full	-	15	-	μV/°C
Bias Current		Full	-	2.5	5	μA
Offset Current		Full	-1.5	-	+1.5	μA
Common Mode Range		Full	-2.5	-	+2.5	V
Common Mode Rejection (±2.5V_{DC}) (Note 3)		Full	60	80	-	dB
TRANSFER CHARACTERISTICS						
Large Signal Voltage Gain (±2.5V_{OUT})		+25°C	95	108	-	dB
		Full	85	-	-	dB
Unity Gain -3dB Bandwidth		+25°C	-	40	-	MHz
TRANSIENT RESPONSE						
Rise Time (200mV Step)		+25°C	-	8.5	-	ns
Overshoot (200mV Step)		+25°C	0	-	30	%
Slew Rate (5V Step)		Full	88	105	-	V/μs
DIGITAL INPUT CHARACTERISTICS						
Input Voltage (High)	V_{IH}	+25°C, +85°C	2.1	-	5.0	V
		-40°C	2.4	-	5.0	V
Input Voltage (Low)	V_{IL}	Full	0	-	0.8	V
Input Current (V_{IL} = 0V)	I_{IL}	Full	-1.0	-	1.0	μA
Input Current (V_{IH} = 5V)	I_{IH}	Full	-1.0	-	1.0	μA
OUTPUT CHARACTERISTICS						
Output Voltage (R_L = 510Ω)		Full	-3.0	-	+3.0	V
Output Current (R_L = 100Ω)		25, 85	20	25	-	mA
		-40°C	15	-	-	mA

Electrical Specifications Test Conditions: $V_{SUPPLY} = \pm 5V$; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), C_L = 5pF, Unless Otherwise Specified **(Continued)**

PARAMETERS		TEMP	HA5351I MIN	HA5351I TYP	HA5351I MAX	UNITS
Full Power Bandwidth ($5V_{P-P}$, A_V = +1, -3dB)		Full	-	13	-	MHz
Output Resistance - Hold Mode		+25°C	-	0.02	-	Ω
TOTAL OUTPUT NOISE, DC TO 10MHz						
Sample Mode		+25°C	-	325	-	μV_{RMS}
Hold Mode		+25°C	-	325	-	μV_{RMS}
DISTORTION CHARACTERISTICS						
SAMPLE MODE						
Total Harmonic Distortion	$V_{IN} = 4.5V_{P-P}$, F_{IN} = 100kHz	+25°C	-	-80	-76	dBc
	$V_{IN} = 5V_{P-P}$, F_{IN} = 1MHz	+25°C	-	-74	-69	dBc
	$V_{IN} = 1V_{P-P}$, F_{IN} = 10MHz	+25°C	-	-57	-52	dBc
Signal to Noise Ratio (RMS Signal to RMS Noise)	$V_{IN} = 4.5V_{P-P}$, F_{IN} = 100kHz	+25°C	-	73	-	dB
HOLD MODE (50% Duty Cycle S/H)						
Total Harmonic Distortion	$V_{IN} = 4.5V_{P-P}$, F_{IN} = 100kHz, $F_S \cong$ 100kHz	+25°C	-	-78	-74	dBc
	$V_{IN} = 5V_{P-P}$, F_{IN} = 1MHz, $F_S \cong$ 1MHz	+25°C	-	-72	-67	dBc
	$V_{IN} = 1V_{P-P}$, F_{IN} = 10MHz, $F_S \cong$ 1MHz	+25°C	-	-51	-47	dBc
Signal to Noise Ratio (RMS Signal to RMS Noise)	$V_{IN} = 4.5V_{P-P}$, F_{IN} = 100kHz, $F_S \cong$ 100kHz	+25°C	-	70	-	dB
SAMPLE AND HOLD CHARACTERISTICS						
Acquisition Time	0V to 2.0V Step to ±1mV	+25°C	-	53	-	ns
	0V to 2.0V Step to 0.01% (±200μV)	+25°C	-	64	70	ns
	-2.5V to +2.5V Step to 0.01% (±500μV)	+25°C	-	90	100	ns
Droop Rate		+25°C	-	0.3	-	μV/μs
		Full	-2	-	2	μV/μs
Hold Step Error (V_{IL} = 0V, V_{IH} = 4.0V, t_R = 5ns)		Full	-10	-	+10	mV
Hold Mode Settling Time (to ±1mV)		+25°C	-	50	-	ns
Hold Mode Feedthrough ($5V_{P-P}$, 500kHz, Sine)		+25°C	-	72	-	dB
EADT (Effective Aperture Delay Time)		+25°C	-	+1	-	ns
Aperture Time (Note 2)		+25°C	-	10	-	ns
Aperture Uncertainty		+25°C	-	10	20	ps
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current		Full	-	20	22	mA
Negative Supply Current		Full	-	20	22	mA
PSRR (+V or -V, 10% Delta)		Full	60	74	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Derived from Computer Simulation only, not tested.
3. +CMRR is measured from 0V to +2.5V, -CMRR is measured from 0V to -2.5V.

Typical Performance Curves

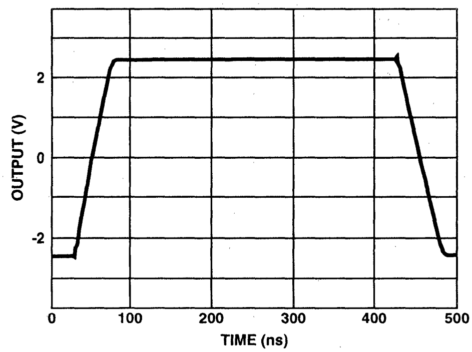


FIGURE 1. LARGE SIGNAL RESPONSE

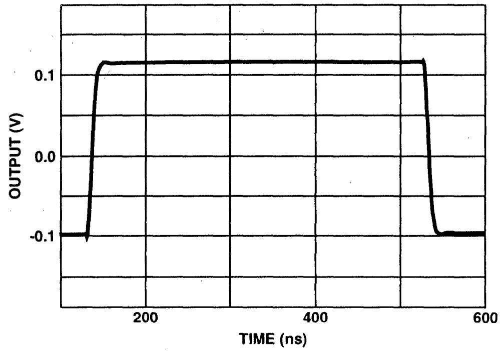


FIGURE 2. SMALL SIGNAL RESPONSE

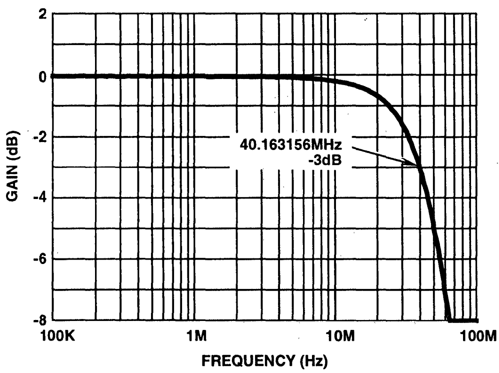


FIGURE 3. UNITY GAIN FREQUENCY RESPONSE

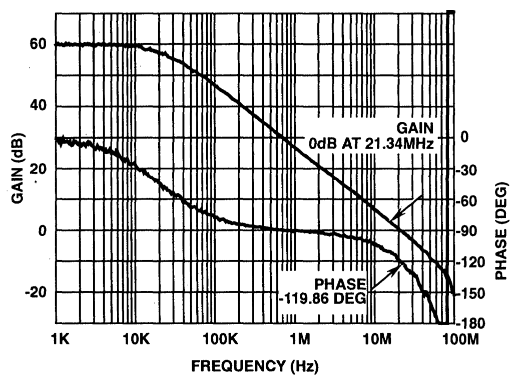


FIGURE 4. CLOSED LOOP GAIN/PHASE A_V = +1000

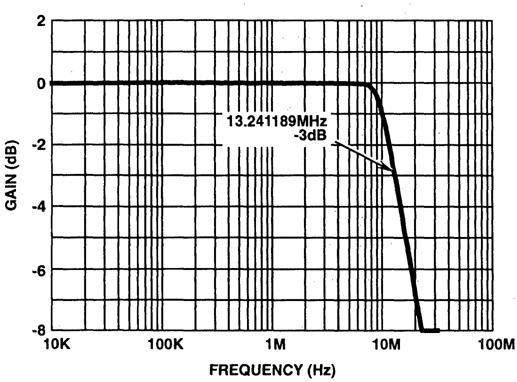


FIGURE 5. $5V_{P-P}$ FULL POWER FREQUENCY RESPONSE

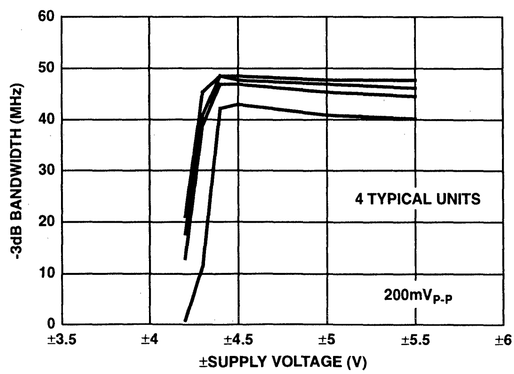


FIGURE 6. -3dB BANDWIDTH vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

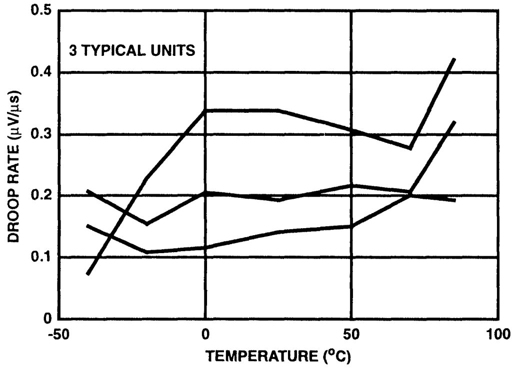


FIGURE 7. DROOP RATE vs TEMPERATURE

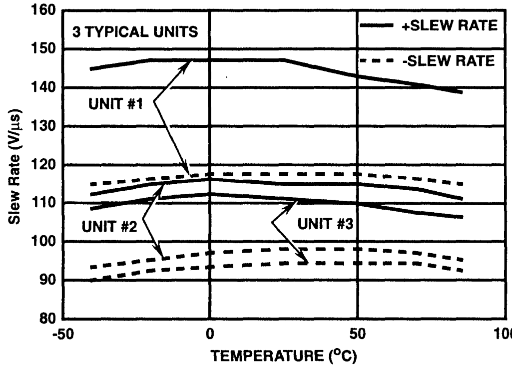


FIGURE 8. SLEW RATE vs TEMPERATURE

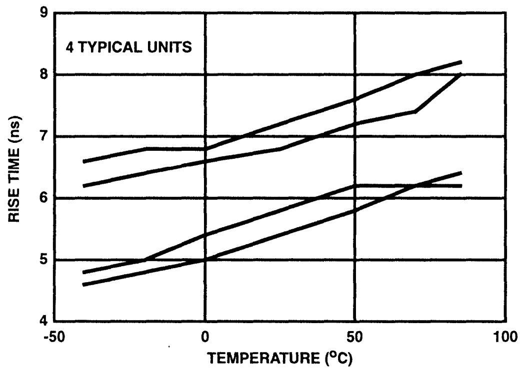


FIGURE 9. RISE TIME vs TEMPERATURE

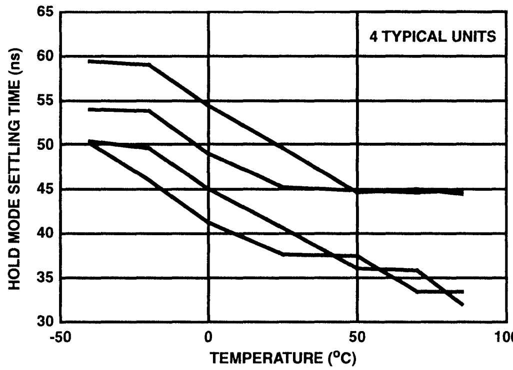


FIGURE 10. HOLD MODE SETTLING vs TEMPERATURE

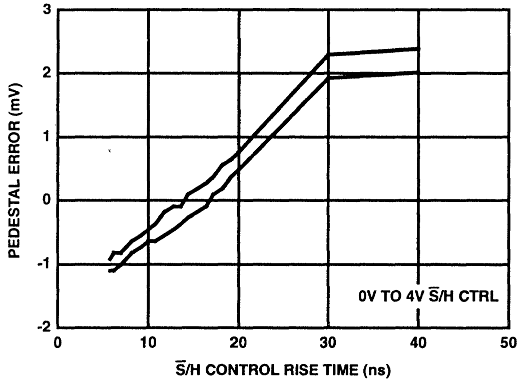


FIGURE 11. PEDESTAL vs S̅/H CONTROL RISE TIME

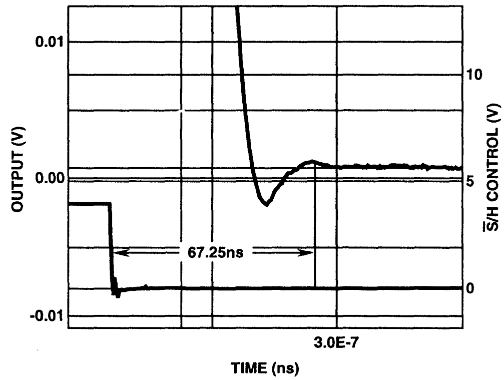


FIGURE 12. ACQUISITION TIME 0.01% 0V TO 2V STEP

3

SAMPLE AND HOLD AMPLIFIERS

Typical Performance Curves (Continued)

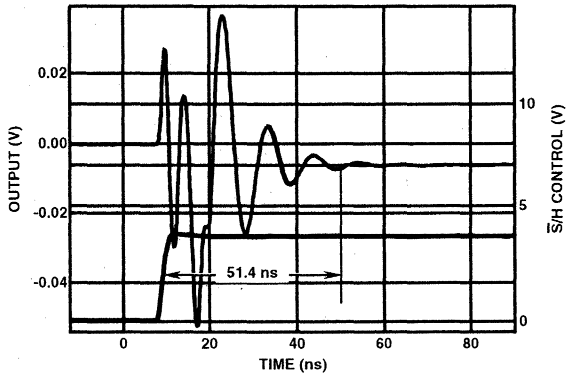


FIGURE 13. HOLD MODE SETTLING TIME (±200μV)

Die Characteristics

DIE DIMENSIONS:
2530 x 1760 x 525 ±25.4μm
100 x 69 x 19 ±1mils

METALLIZATION:
Type: Metal 1: AlSiCu/TiW
Thickness: Metal 1: 6kÅ ± 750Å

Type: Metal 2: AlSiCu
Thickness: Metal 2: 16kÅ ± 1.1kÅ

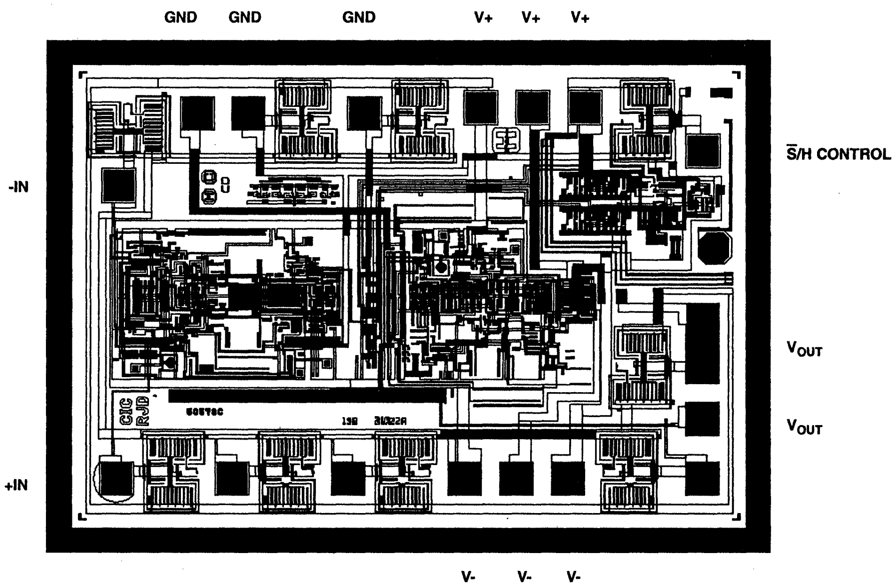
GLASSIVATION:
Type: Sandwich Passivation
Nitride - 4kÅ, Undoped Si Glass(USG) - 8kÅ, Total - 12kÅ ±2kÅ

SUBSTRATE POTENTIAL: V-

TRANSISTOR COUNT: 156

Metallization Mask Layout

HA5351



3
SAMPLE AND HOLD AMPLIFIERS

HARRIS SEMICONDUCTOR

HA5352

Fast Acquisition Dual Sample and Hold Amplifier

July 1995

Features

- **Fast Acquisition to 0.01% . . . . 70ns (Max)**
- **Low Offset Error . . . . ±2mV (Max)**
- **Low Pedestal Error . . . . ±10mV (Max)**
- **Low Droop Rate . . . . 2μV/μs (Max)**
- **Wide Unity Gain Bandwidth 40MHz**
- **Low Power Dissipation per Amp . . . . . . 220mW (Max)**
- **Total Harmonic Distortion (Hold Mode) . . . . -72dBc (V_{IN} = $5V_{P-P}$ at 1MHz)**
- **Fully Differential Inputs**
- **On Chip Hold Capacitor**

Applications

- **Synchronous Sampling**
- **Wide Bandwidth A/D Conversion**
- **Deglitching**
- **Peak Detection**
- **High Speed DC Restore**

Description

The HA5352 is a fast acquisition, wide bandwidth Dual Sample and Hold amplifier built with the Harris HBC-10 BiCMOS process. This Sample and Hold amplifier offers the combination of features; fast acquisition time (70ns to 0.01%), excellent DC precision and extremely low power dissipation, making it ideal for use in multi-channel systems that require low power.

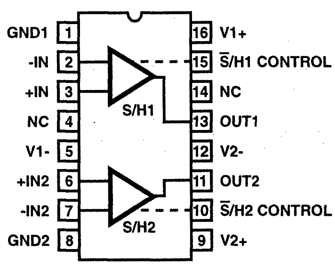
The HA5352 comes in an open loop configuration with fully differential inputs providing flexibility for user defined feedback. In unity gain the HA5352 is completely self-contained and requires no external components. The on-chip 15pF hold capacitors are completely isolated to minimize droop rate and reduce the sensitivity of pedestal error. The HA5352 Dual Sample and Hold is available in a 14 lead PDIP and 16 lead SOIC packages saving board space while its pinout is designed to simplify layout.

Ordering Information

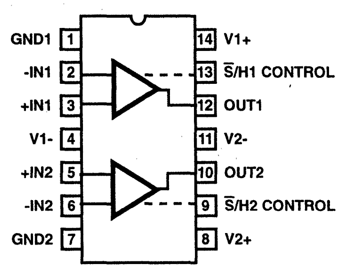
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA5352IP	-40°C to +85°C	14 Lead Plastic DIP
HA5352IB	-40°C to +85°C	16 Lead Plastic SOIC (W)

Pinouts

HA5352 (300 mil SOIC)
TOP VIEW



HA5352 (PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Absolute Maximum Ratings

Voltage Between V+ and V- Terminals .... +11V
Differential Input Voltage .... +6V
Voltage between S/H control and ground .... +5.5V
Output Current, Continuous .... ±37mA
Junction Temperature (Plastic Packages) .... +150°C
Lead Temperature (Soldering, 10s) .... +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HA5352I .... $-40^oC \le T_A \le +85^oC$
Storage Temperature Range .... $-65^oC \le T_A \le +150^oC$
Thermal Package Characteristics θ_{JA}
Plastic DIP .... 90°C/W
SOIC .... 95°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions: V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), C_L = 5pF, Unless Otherwise Specified

PARAMETERS	TEMP	HA5352I			UNITS
		MIN	TYP	MAX	
INPUT CHARACTERISTICS					
Input Voltage Range	Full	-2.5	-	+2.5	V
Input Resistance (Note 2)	+25°C	100	500	-	kΩ
Input Capacitance	+25°C	-	-	5	pF
Input Offset Voltage	+25°C	-2	-	2	mV
	Full	-3.0	-	3.0	mV
Offset Voltage Temperature Coefficient	Full	-	15	-	µV/°C
Bias Current	Full	-	2.5	5	µA
Offset Current	Full	-1.5	-	+1.5	µA
Common Mode Range	Full	-2.5	-	+2.5	V
Common Mode Rejection (±2.5V_{DC}, Note 3)	Full	60	80	-	dB
TRANSFER CHARACTERISTICS					
Large Signal Voltage Gain (±2.5V_{OUT})	+25°C	95	108	-	dB
	Full	85	-	-	dB
Unity Gain -3dB Bandwidth	+25°C	-	40	-	MHz
TRANSIENT RESPONSE					
Rise Time (200mV Step)	+25°C	-	8.5	-	ns
Overshoot (200mV Step)	+25°C	0	-	30	%
Slew Rate (5V Step)	Full	88	105	-	V/µs
DIGITAL INPUT CHARACTERISTICS					
Input Voltage (High) V_{IH}	+25°C, +85°C	2.1	-	5.0	V
	-40°C	2.4	-	5.0	V
Input Voltage (Low) V_{IL}	Full	0	-	0.8	V

Electrical Specifications Test Conditions: V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), C_L = 5pF, Unless Otherwise Specified **(Continued)**

PARAMETERS		TEMP	HA5352I MIN	TYP	MAX	UNITS
Input Current (V_{IL} = 0V)	I_{IL}	Full	-1	-	+1	µA
Input Current (V_{IH} = 5V)	I_{IH}	Full	-1	-	+1	µA
OUTPUT CHARACTERISTICS						
Output Voltage (R_L = 510Ω)		Full	-3	-	+3	V
Output Current (R_L = 100Ω)		+25°C, +85°C	20	25	-	mA
		-40°C	15	-	-	mA
Full Power Bandwidth (5V_{P-P}, A_V = +1, -3dB)		Full	-	13	-	MHz
Output Resistance - Hold Mode		+25°C	-	0.02	-	Ω
TOTAL OUTPUT NOISE, D.C. TO 10MHz						
Sample Mode		+25°C	-	325	-	µVrms
Hold Mode		+25°C	-	325	-	µVrms
SAMPLE MODE DISTORTION CHARACTERISTICS						
Total Harmonic Distortion	V_{IN} = 4.5V_{P-P}, F_{IN} = 100kHz	+25°C	-	-80	-76	dBc
	V_{IN} = 5V_{P-P}, F_{IN} = 1MHz	+25°C	-	-74	-69	dBc
	V_{IN} = 1V_{P-P}, F_{IN} = 10MHz	+25°C	-	-57	-52	dBc
Signal to Noise Ratio (RMS Signal to RMS Noise)	V_{IN} = 4.5V_{P-P}, F_{IN} = 100kHz	+25°C	-	73	-	dB
Crosstalk	V_{IN} = 5V_{P-P}, F_{IN} = 10MHz	+25°C	-	75	-	dB
HOLD MODE DISTORTION CHARACTERISTICS (50% Duty Cycle S/H)						
Total Harmonic Distortion	V_{IN} = 4.5V_{P-P}, F_{IN} = 100kHz, F_S ≅ 100kHz	+25°C	-	-78	-74	dBc
	V_{IN} = 5V_{P-P}, F_{IN} = 1MHz, F_S ≅ 1MHz	+25°C	-	-72	-67	dBc
	V_{IN} = 1V_{P-P}, F_{IN} = 10MHz, F_S ≅ 1MHz	+25°C	-	-51	-47	dBc
Signal to Noise Ratio (RMS Signal to RMS Noise)	V_{IN} = 4.5V_{P-P}, F_{IN} =100kHz, F_S ≅ 100kHz	+25°C	-	70	-	dB
SAMPLE AND HOLD CHARACTERISTICS						
Acquisition Time	0V to 2.0V Step to ±1mV	+25°C	-	53	-	ns
	0V to 2.0V Step to 0.01% (±200µV)	+25°C	-	64	70	ns
	-2.5V to +2.5V Step to 0.01% (±500µV)	+25°C	-	90	100	ns

Electrical Specifications Test Conditions: V_{SUPPLY} = ±5V; C_H = Internal = 15pF, Digital Input: V_{IL} = +0.0V (Sample), V_{IH} = 4.0V (Hold). Non-Inverting Unity Gain Configuration (Output Tied to -Input), C_L = 5pF, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEMP	HA5352I			UNITS
		MIN	TYP	MAX	
Droop Rate	+25°C	-	0.3	-	µV/µs
	Full	-2	-	2	µV/µs
Hold Step Error (V_{IL} = 0V, V_{IH} = 4.0V, t_R = 5ns)	Full	-10	-	+10	mV
Hold Mode Settling Time (to ±1mV)	25°C	-	50	-	ns
Hold Mode Feedthrough ($5V_{P-P}$, 500kHz, Sine)	25°C	-	72	-	dB
EADT (Effective Aperture Delay Time)	+25°C	-	+1	-	ns
Aperture Time (Note 2)	+25°C	-	10	-	ns
Aperture Uncertainty	+25°C	-	10	20	ps
Aperture Match	+25°C	-	30	-	ps
POWER SUPPLY CHARACTERISTICS					
Supply Current (per Amp)	Full	-	20	22	mA
Total Supply Current	Full	-	40	44	mA
PSRR (+V or -V, 10% Delta)	Full	60	74	-	dB

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Derived from Computer Simulation only, not tested.
3. +CMRR is measured from 0V to +2.5V, -CMRR is measured from 0V to -2.5V.

Die Characteristics

DIE DIMENSIONS:

2530 x 3110 x 525 ±25.4µm
100 x 122 x 19 ±1mil

METALLIZATION:

Type: Metal 1: AlSiCu/TiW
Thickness: Metal 1: 6kÅ ± 750Å

Type: Metal 2: AlSiCu
Thickness: Metal 2: 16kÅ ± 1.1kÅ

GLASSIVATION:

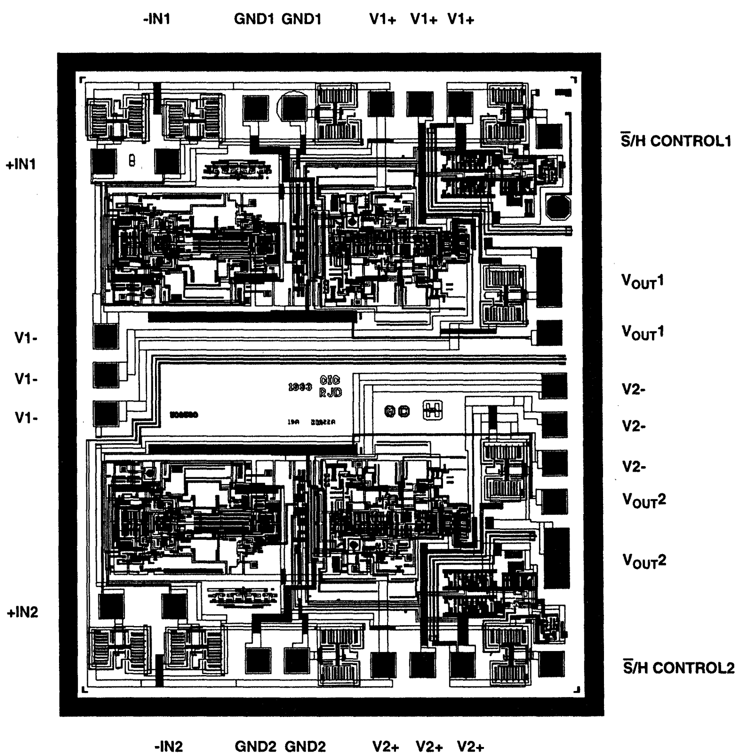
Type: Sandwich Passivation
Nitride - 4kÅ, Undoped Si Glass(USG) - 8kÅ, Total - 12kÅ ±2kÅ

SUBSTRATE POTENTIAL: V-

TRANSISTOR COUNT: 312

Metallization Mask Layout

HA5352



SIGNAL PROCESSING NEW RELEASES 4

A/D CONVERTERS

A/D CONVERTERS

RELATED APPLICATION NOTES AND TECH BRIEFS AVAILABLE ON AnswerFAX		PAGE AnswerFAX DOCUMENT NO.
AN9336	Multi-Meter Display Converter Eases DMM Design	99336
AN9407	Using the HI1176/HI1179 Evaluation Board	99407
AN9410	Using the HI5721 Evaluation Module	99410
AN9411	Using the HI1171 Evaluation Kit	99411
AN9412	Using the HI5702 Evaluation Board	99412
AN9413	Driving the Analog Input of the HI5702	99413
AN9419	Using the DAC Reconstruct Board	99419
AN9501	Understanding the HI5721 D/A Converter Spectral Specifications	99501
AN9504	A Brief Introduction to Sigma Delta Conversion	99504
AN9511	Using the HI5710 Evaluation Board	99511
TB322	Replacing an MP7684/MP7684A with an HI5700	82322
TB323	Replacing An MP7682 With An HI5701	82323
TB324	Clamping the Analog Input of the HI5800	82324
TB329	Harris Sigma-Delta Calibration Technique	82329
TB331	Using the HI7190 Serial Interface	82331

June 1995

8-Bit, 35 MSPS Video A/D Converter

Features

- Resolution 8-Bit ±0.5 LSB (DNL)
- ENOB, 7.6 Bits
- Maximum Sampling Frequency 35 MSPS
- Low Power Consumption 80mW (at 35 MSPS Typ) (Reference Current Excluded)
- Built-In Input Clamp Function (DC Restore)
- No Sample/Hold Required
- Internal Voltage Reference
- Input CMOS Compatible
- Three-State TTL Compatible Output
- Single +5V Power Supply
- Low Input Capacitance 8pF (Typical)
- Reference Impedance 330Ω (Typical)
- Evaluation Board Available: HI1179-EV

Applications

- Desktop Video
- Multimedia
- Video Digitizing
- Image Scanners
- Low Cost High Speed Data Acquisition Systems

Description

The HI1179 is an 8-bit CMOS analog-to-digital converter for video use that features a sync clamp function. The adoption of a 2-step parallel method realizes low power consumption and a maximum conversion speed of 35 MSPS, allowing up to 8x over sampling of NTSC and PAL signals.

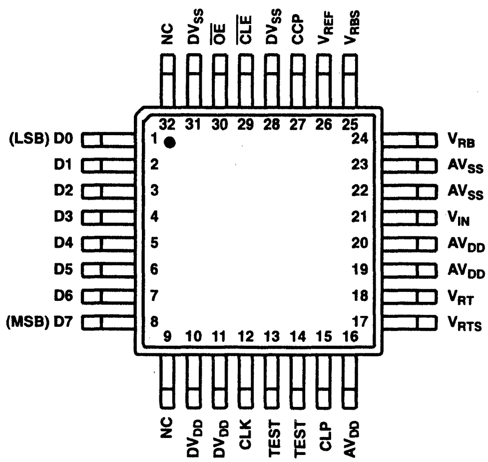
The HI1179 is available in the Commercial temperature range and is supplied in 32 lead Plastic Metric Quad Flatpack (MQFP) package. For lower sampling rates, refer to the HI1176 data sheet.

Ordering Information

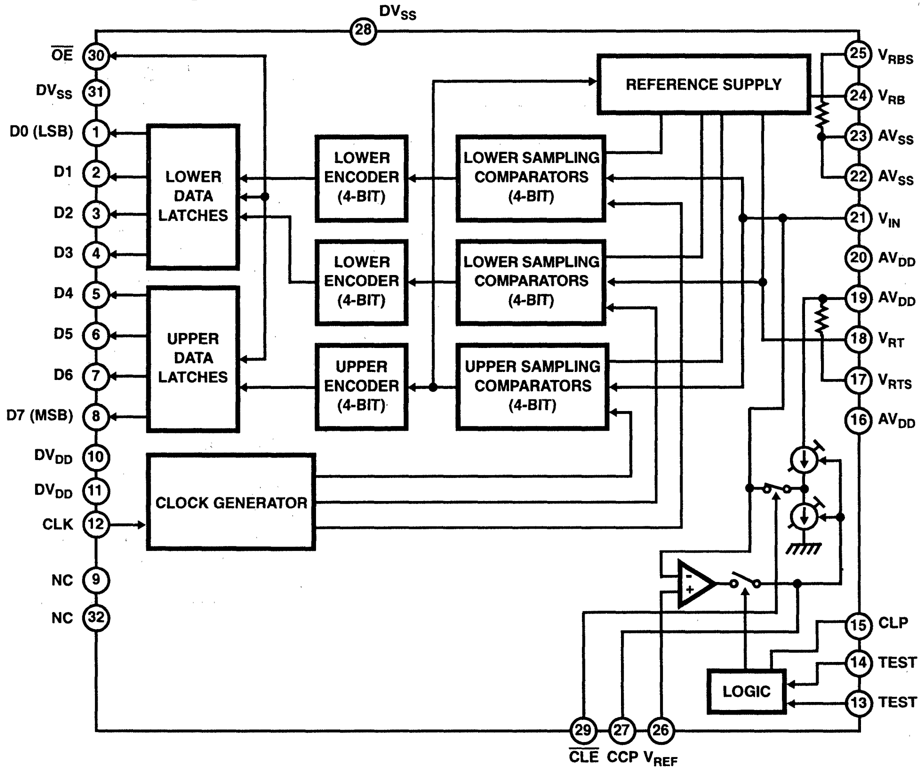
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1179JCQ	0°C to +75°C	32 Lead Plastic Metric Quad Flatpack

Pinout

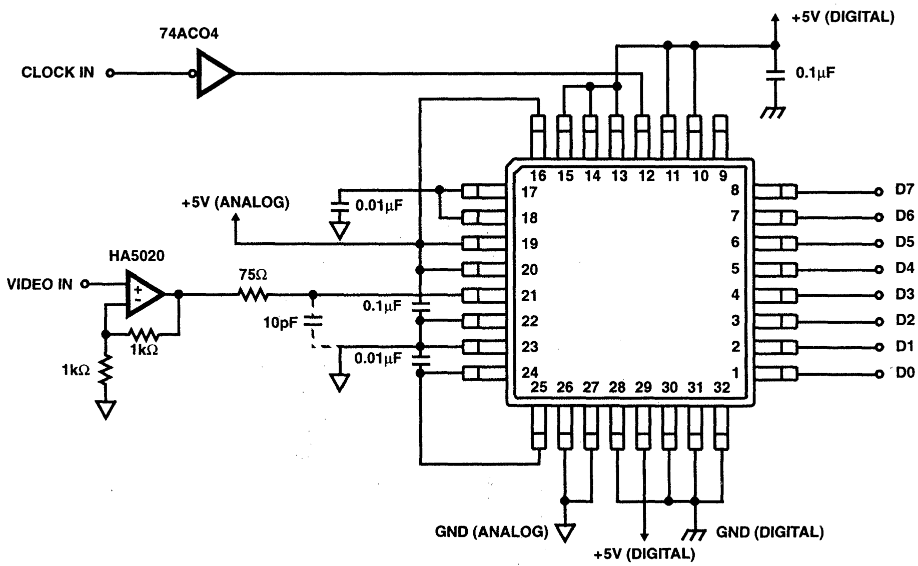
HI1179 (MQFP)
TOP VIEW



Functional Block Diagram



Typical Application Schematic



NON-CLAMP APPLICATION (INTERNAL REFERENCE USED)

Absolute Maximum Ratings

Supply Voltage, V_{DD} 7V
Reference Voltage, V_{RT}, V_{RB} .... V_{DD} to V_{SS}
Analog Input Voltage, V_{IN} .... V_{DD} to V_{SS}
Digital Input Voltage .... V_{DD} to V_{SS}
Digital Output Voltage, V_{OH}, V_{OL} .... V_{DD} to V_{SS}
Storage Temperature, T_{STG} .... -55°C to +150°C

Thermal Information

Thermal Resistance θ_{JA}
HI1179JCQ .... 122°C/W
Operating Temperature, T_A .... 0°C to +75°C
Maximum Junction Temperature .... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions (Note 1)

Supply Voltage
AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS} .... +4.75V to +5.25V
|DGND-AGND| .... 0mV to 100mV
Reference Input Voltage
V_{RB} .... 0V and Above
V_{RT} .... 2.7V and Below

Analog Input Voltage, V_{IN} .... V_{RB} to V_{RT} ($1.8V_{P-P}$ to AV_{DD})
Clock Pulse Width
T_{PW1} .... 14ns (Min)
T_{PW0} .... 14ns (Min)

Electrical Specifications F_C = 35 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = +25°C (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Offset Voltage					
E_{OT}		-60	-40	-20	mV
E_{OB}		+55	+75	+95	mV
Integral Non-Linearity, (INL)	F_C = 35 MSPS, V_{IN} = 0.5V to 2.5V	-1.0	±0.5	+1.3	LSB
Differential Non-Linearity, (DNL)	F_C = 35 MSPS, V_{IN} = 0.5V to 2.5V	-0.5	±0.3	+0.5	LSB
DYNAMIC CHARACTERISTICS					
ENOB	F_{IN} = 1MHz	-	7.6	-	Bits
	F_{IN} = 5MHz	-	7.3	-	Bits
Maximum Conversion Speed, F_C	V_{IN} = 0.5V to 2.5V, F_{IN} = 1kHz Ramp	35	40	-	MSPS
Minimum Conversion Speed, F_C	V_{IN} = 0.5V to 2.5V, F_{IN} = 1kHz Ramp	-	-	0.5	MSPS
Differential Gain Error, DG	NTSC 40 IRE Mod Ramp, F_C = 14.3 MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Aperture Jitter, t_{AJ}		-	30	-	ps
Sampling Delay, t_{SD}		-	2	-	ns
ANALOG INPUTS					
Analog Input Bandwidth, BW	-1dB	-	25	-	MHz
	-3dB	-	60	-	MHz
Analog Input Capacitance, C_{IN}	V_{IN} = 1.5V + $0.07V_{RMS}$	-	8	-	pF
REFERENCE INPUT					
Reference Pin Current, I_{REF}		4.5	6.1	8.7	mA
Reference Resistance (V_{RT} to V_{RB}), R_{REF}		230	330	440	Ω
INTERNAL VOLTAGE REFERENCES					
Self Bias					
V_{RB}	Short V_{RB} to V_{RBS}, Short V_{RT} to V_{RTS}	0.52	0.56	0.60	V
V_{RT} - V_{RB}		1.96	2.10	2.24	V
V_{RT} - V_{RB}	Short V_{RT} to V_{RTS}, Short V_{RB} to AV_{SS}	2.13	2.33	2.53	V

Electrical Specifications F_C = 35 MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = +25°C (Note 1) **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DIGITAL INPUTS						
Digital Input Voltage						
V_{IH}			3.5	-	-	V
V_{IL}			-	-	0.5	V
Digital Input Current						
I_{IH}	V_{DD} = Max	$V_{IH} = V_{DD}$	-	-	5	μA
I_{IL}		V_{IL} = 0V	-	-	5	μA
DIGITAL OUTPUTS						
Digital Output Current						
I_{OH}	$\overline{OE} = V_{SS}$, V_{DD} = Min	$V_{OH} = V_{DD}$ -0.5V	-1.1	-2.5	-	mA
I_{OL}		V_{OL} = 0.4V	3.7	6.5	-	mA
Digital Output Leakage Current						
I_{OZH}	$\overline{OE} = V_{DD}$, V_{DD} = Max	$V_{OH} = V_{DD}$	-	-	16	μA
I_{OZL}		V_{OL} = 0V	-	-	16	μA
TIMING CHARACTERISTICS						
Output Data Delay, t_D	Load is One TTL Gate		7	13	18	ns
Output Enable/Disable Delay	t_{PZL}		-	6.8	-	ns
	t_{PLZ}		-	7.2	-	ns
	t_{PHZ}		-	6.6	-	ns
	t_{PZH}		-	7.8	-	ns
POWER SUPPLY CHARACTERISTIC						
Supply Current, I_{DD}	F_C = 35 MSPS, NTSC Ramp Wave Input		-	16	22	mA
CLAMP CHARACTERISTICS						
Clamp Offset Voltage, E_{OC}	V_{IN} = DC, PWS = 3μs	V_{REF} = 0.5V	-20	0	+20	mV
		V_{REF} = 2.5V	-30	-10	+10	mV
Clamp Pulse Delay, t_{CPD}			-	25	-	ns

NOTE:

1. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagrams

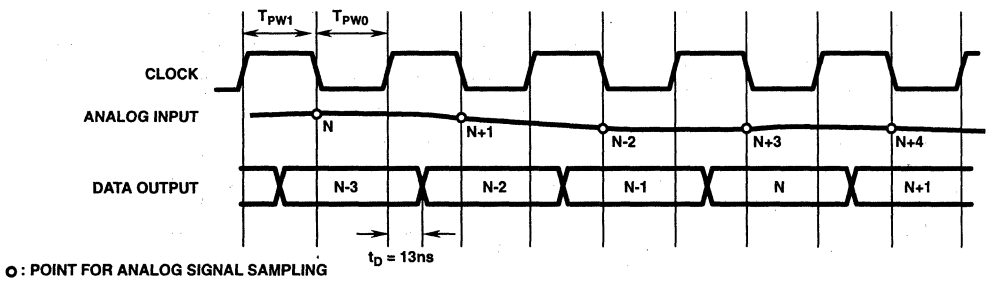


FIGURE 1.

Timing Diagrams (Continued)

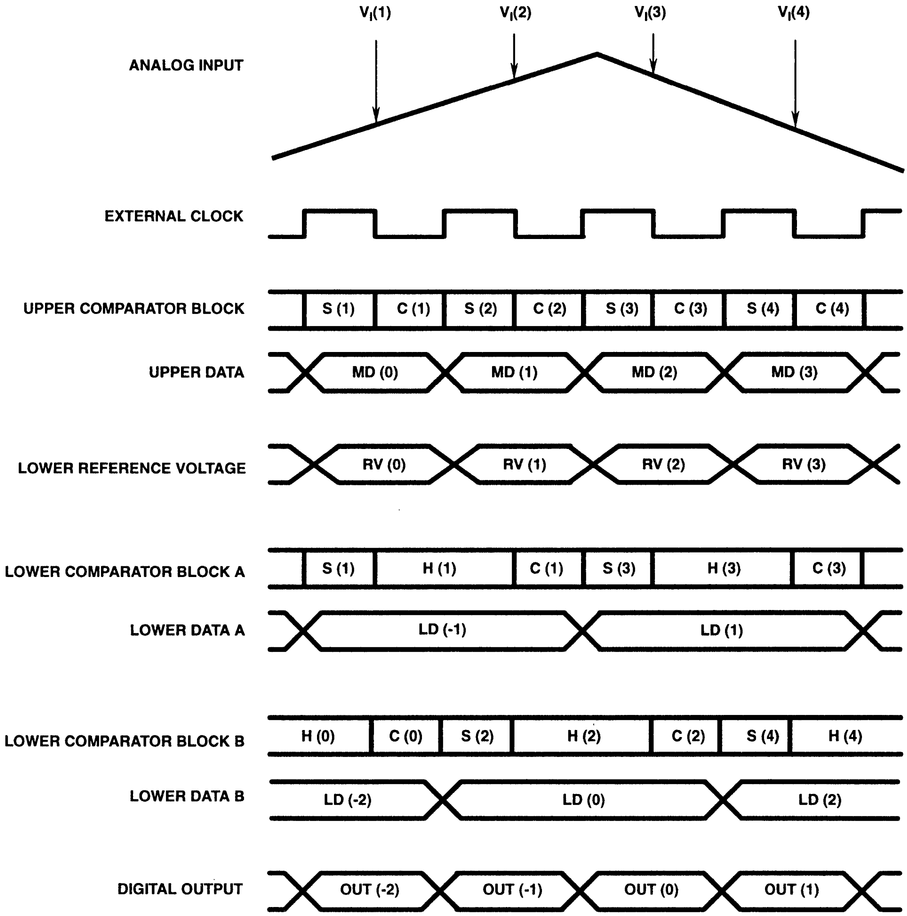


FIGURE 2.

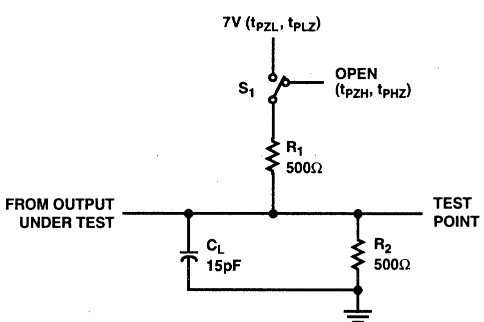


FIGURE 3A. THREE-STATE LOAD CIRCUIT

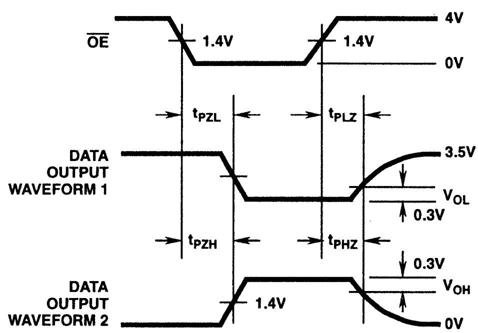


FIGURE 3B. THREE-STATE OUTPUT ENABLE/DISABLE TIMES

FIGURE 3.

Typical Performance Curves F_C = 35 MSPS, T_A = +25°C, Unless Otherwise Specified

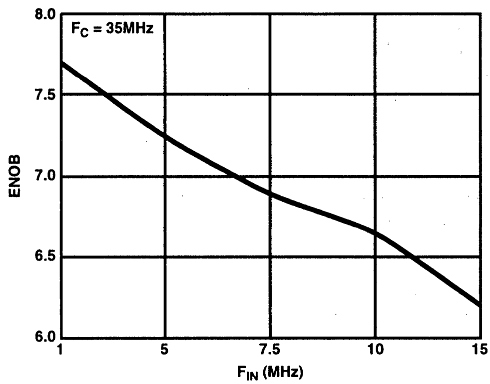


FIGURE 4. ENOB vs INPUT FREQUENCY

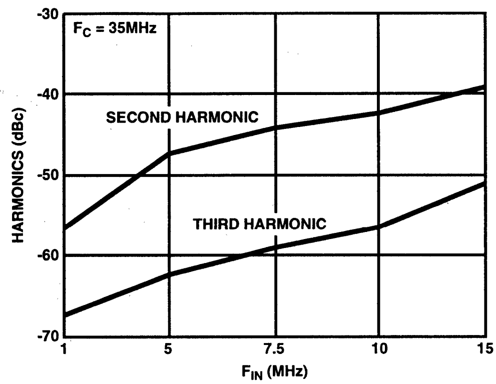


FIGURE 5. HARMONICS vs INPUT FREQUENCY

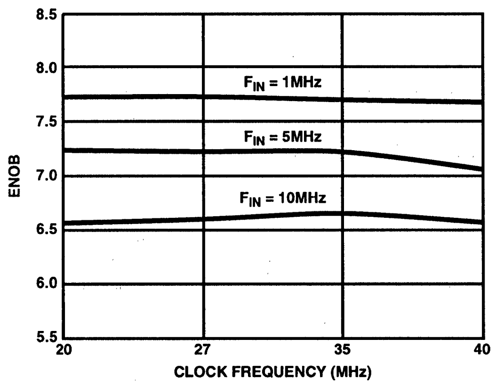


FIGURE 6. ENOB vs CLOCK FREQUENCY

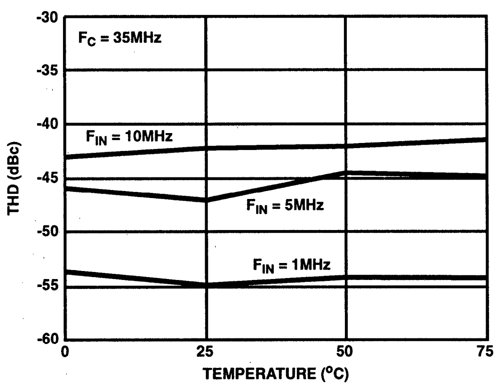


FIGURE 7. THD vs TEMPERATURE

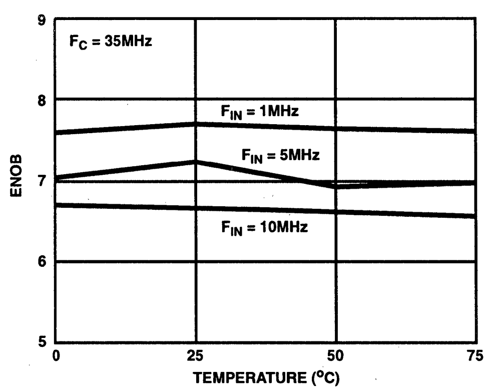


FIGURE 8. ENOB vs TEMPERATURE

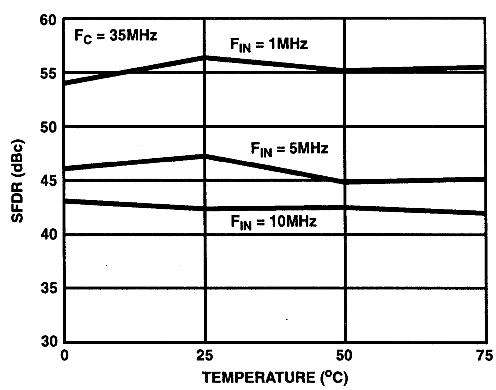


FIGURE 9. SFDR vs TEMPERATURE

Typical Performance Curves F_C = 35 MSPS, T_A = +25°C, Unless Otherwise Specified **(Continued)**

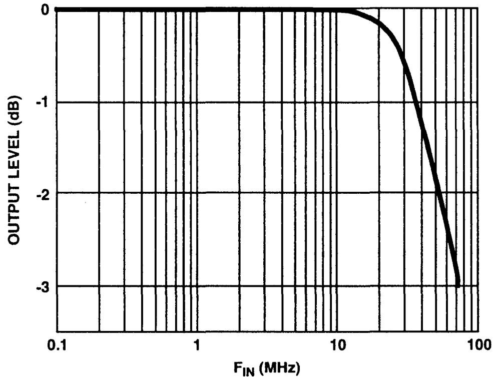


FIGURE 10. OUTPUT LEVEL vs INPUT FREQUENCY

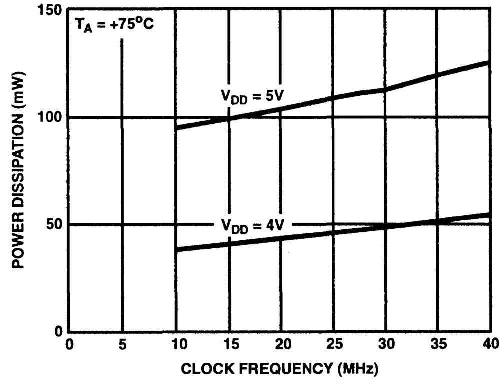
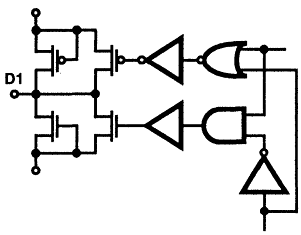
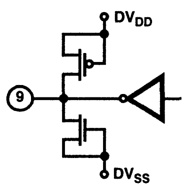
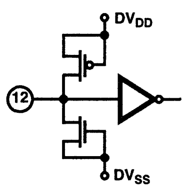
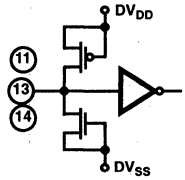
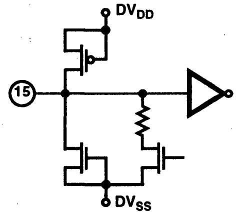
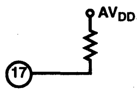
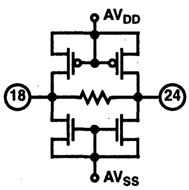
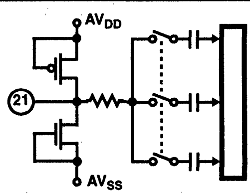
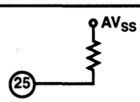


FIGURE 11. POWER DISSIPATION vs CLOCK FREQUENCY

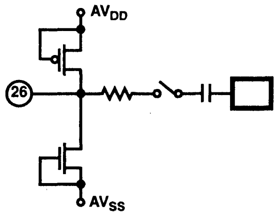
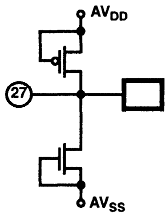
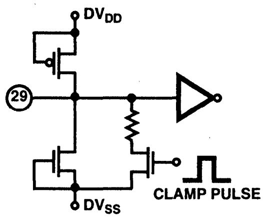
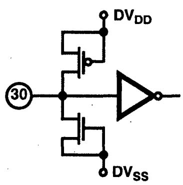
Pin Number Description

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1-8	D0 to D7		D0 (LSB) to D7 (MSB) output.
9	NC		This pin must be left open. Used for test purposes only.
10	DV_{DD}		Digital +5V.
12	CLK		Clock input.

Pin Number Description (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
11, 13, 14	TEST		Pin 11 must be connected to DV_{DD}. Pin 13, and Pin 14 must be connected to DV_{DD} or DV_{SS}. Used for test purposes only.
15	CLP		Clamp pulse input. The input signal voltage is clamped to V_{REF} while the clamp pulse is low.
16, 19, 20	AV_{DD}		Analog +5V.
17	V_{RTS}		When shorted with V_{RT}, generates approximately +2.6V.
18	V_{RT}		Reference voltage (top).
24	V_{RB}		Reference voltage (bottom).
21	V_{IN}		Analog input.
22, 23	AV_{SS}		Analog ground.
25	V_{RBS}		When shorted with V_{RB}, generates approximately +0.5V.

Pin Number Description (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
26	V_{REF}		Clamp reference voltage input.
27	CCP		Integrates the voltage for clamp control. CCP and V_{IN} voltage changes are in phase.
28, 31	DV_{SS}		Digital ground.
29	$\overline{CLE}$		When $\overline{CLE}$ is low, clamp function is activated. When $\overline{CLE}$ is high, clamp function is OFF and only the usual A/D converter function is active. By connecting $\overline{CLE}$ pin to DV_{DD} via a several hundred Ω resistance, the clamp pulse can be tested.
30	$\overline{OE}$		When $\overline{OE}$ is low, data is valid. When $\overline{OE}$ is high, D0 to D7 pins are high impedance.

A/D OUTPUT CODE TABLE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE MSB							LSB
V_{RT}	255	1	1	1	1	1	1	1	1
⋮	⋮					⋮			
⋮	128	1	0	0	0	0	0	0	0
⋮	127	0	1	1	1	1	1	1	1
⋮	⋮					⋮			
V_{RB}	0	0	0	0	0	0	0	0	0

Detailed Description

The HI1179 is a 2-step A/D converter featuring a 4-bit upper comparator group and two lower comparator groups of 4 bits each. The reference voltage can be obtained from the onboard bias generator or be supplied externally. This IC uses an offset canceling type comparator that operates synchronously with an external clock. The operating modes of the part are input sampling/autozero (S), hold (H), and compare (C).

The operation of the part is illustrated in Figure 2. A reference voltage that is between V_{RT}-V_{RB} is constantly applied to the upper 4-bit comparator group. $V_I(1)$ is sampled with the falling edge of the first clock by the upper comparator block. The lower block A also samples $V_I(1)$ on the same edge. The upper comparator block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates a reference voltage RV(1) that corresponds to the upper results and applies it to the lower comparator block A. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as OUT(1) with the rising edge of the third clock. There is a 2.5 clock cycle delay from the analog input sampling point to the corresponding digital output data. Notice how the lower comparator blocks A and B alternate generating the lower data in order to increase the overall A/D sampling rate.

Power, Grounding, and Decoupling

Separate analog and digital grounds to reduce noise effects, connecting them at a single point near the HI1179. Analog and digital power should also be separated for optimum performance. If a single 5V supply is used, isolate the analog and digital power with an inductor or ferrite bead to minimize the digital noise on the analog supply.

Bypass both the digital and analog V_{DD} pins to their respective grounds with a ceramic 0.1µF capacitor close to the pin.

Analog Input

The analog input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with a low impedance source with sufficient bandwidth and drive capability.

Op amps such as the HA-2544, the HA5020 and the HFA1100 family should make excellent input amplifiers depending on the applications requirements. In order to prevent parasitic oscillation, it may be necessary to insert a resistor between the output of the amplifier and the A/D input.

The input can be AC or DC coupled. If AC coupled the input will float to about $1/2(V_{RT} + V_{RB})$. The other option is to use the internal clamp, which will be discussed later. When DC coupling the input be sure to disable the clamp function ($\overline{CLE}$, pin 29).

Reference Input

The HI1179 has an internal reference with the option to use an external reference if more accuracy is desired.

The analog input range of the A/D is set by the voltage between V_{RT} and V_{RB}. The internal reference can be used by shorting V_{RT} to V_{RTS} and V_{RB} to V_{RBS}. The internal bias generator will set V_{RT} to about 2.6V and V_{RB} to about 0.6V. The analog input range of the A/D will now be from 0.6V to 2.6V. The internal reference may be subjected to power supply variations since the internal reference resistor ladder is connected directly to V_{DD} and V_{SS}. Any supply variations can be minimized by good decoupling of V_{RT} and V_{RB}.

An external reference can be used for increased accuracy, by connecting the reference voltage to V_{RT} and V_{RB}. If an external reference is used, V_{RT} should be keep below 2.8V and $(V_{RT} - V_{RB})$ should be less than 2.8V and greater than 1.8V. If a V_{RB} below +0.6V is used the linearity of the part may degrade. An ICL8069 reference and a dual op amp, with outputs connect to V_{RT} and V_{RB}, makes a good, low cost external reference.

Bypass V_{RT} and V_{RB} to analog ground with a 0.1µF capacitor when using either internal or external references.

Clamp Operation

The HI1179 provides a clamp (DC restore) option that allows the user to clamp a portion of the analog input to a voltage set by the V_{REF} pin before the signal is digitized. The clamp function is enabled by tying $\overline{CLE}$ low. In this case a negative going pulse is sent to the CLP pin. V_{IN} will now be clamped during the low period of the clamp pulse to the voltage on the V_{REF} pin. Figure 15 shows the HI1179 configured for this mode of operation.The clamp pulse is latched by the ADC sampling clock through an external latch. This is not necessary to the operation of the clamp function but in video applications, if this is not done, then a slight beat might be generated as vertical sag according to the relation between the sampling frequency and the clamp frequency. The pulse width of the input clamp pulse will depend on the input signal. For example, a 1µs pulse width will allow the user to clamp the back porch of an NTSC input signal to the reference voltage, V_{REF}.

The clamp can be disabled by tying $\overline{CLE}$ high and then the HI1179 acts like a normal A/D converter, accepting a DC coupled input. The Typical Application Schematic illustrates the operation of HI1179 when the clamp function is not used.

Additional information on the HI1179 is available in Application Note #9407, "Using the HI1176/HI1179 Evaluation Board".

Test Circuits

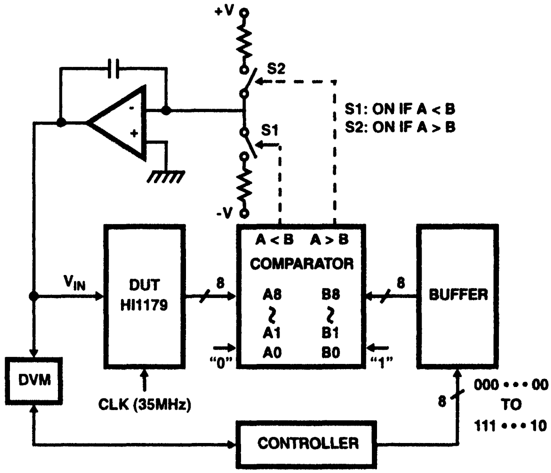


FIGURE 12. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

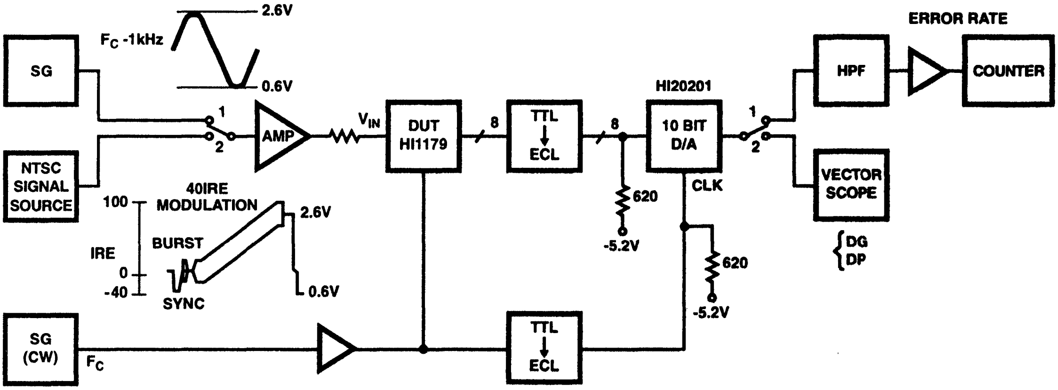


FIGURE 13. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

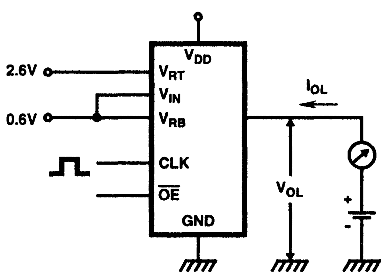


FIGURE 14A.

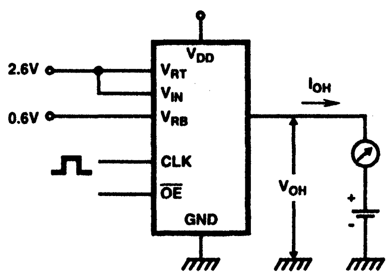


FIGURE 14B.

FIGURE 14. DIGITAL OUTPUT CURRENT TEST CIRCUIT

Typical Application Circuits

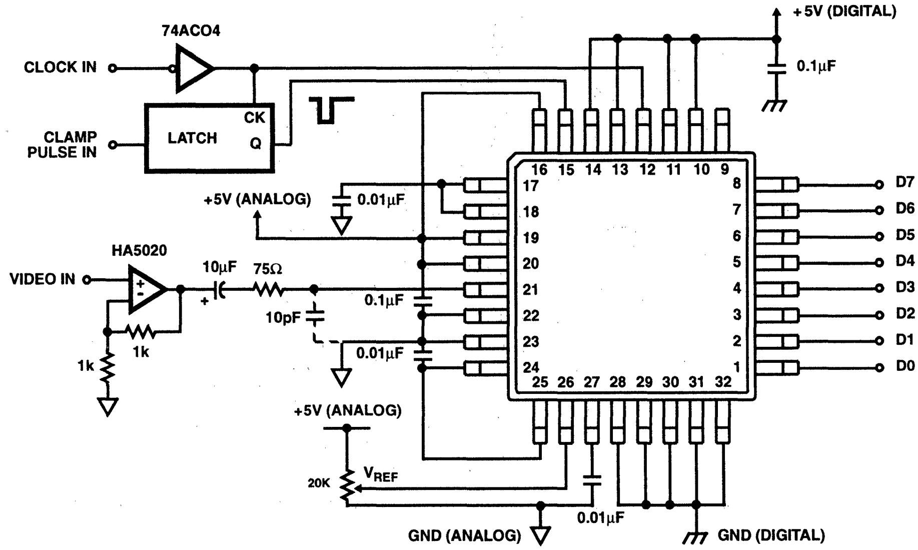
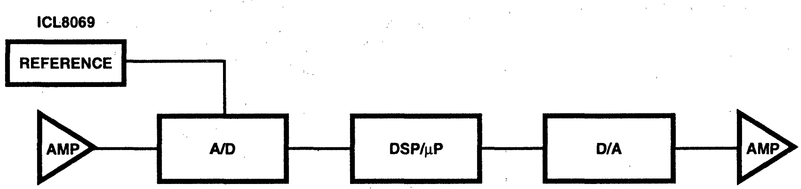


FIGURE 15. INPUT CLAMP APPLICATION (INTERNAL REFERENCE USED)



HA5020 (Single)	HI1179 (8-Bit)	HSP9501	HI1171 (8-Bit)	HA5020 (Single)
HA5022(Dual)		HSP48410	CA3338 (8-Bit)	HA2842 (Single)
HA5024 (Quad)		HSP48908		HFA1115 (Single)
HA5013 (Triple)		HSP48901		HFA1212 (Dual)
HFA1105(Single)		HSP48212		HFA1412 (Quad)
HFA1205(Dual)		HSP43881		
HFA1405(Quad)		HSP43168		

HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution, 4K x 4K Frame Size
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48901: 3 x 3 Image Filter, 30MHz, 8-Bit
HSP48212: Video Mixer
HSP43881: Digital Filter, 30MHz, 1-D and 2-D FIR Filters
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz

CMOS Logic Available in HC, HCT, AC, ACT and FCT.

FIGURE 16. 8-BIT VIDEO COMPONENTS

Static Performance Definitions

Offset, full-scale, and gain all use a measured value of the internal voltage reference to determine the ideal plus and minus full-scale values. The results are all displayed in LSB's.

Offset Error (VOS)

The first code transition should occur at a level 1/2 LSB above the negative full-scale. Offset is defined as the deviation of the actual code transition from this point. Note that this is adjustable to zero.

Full-Scale Error (FSE)

The last code transition should occur for a analog input that is 1 and 1/2 LSB's below positive full-scale. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1LSB. The converter is guaranteed to have no missing codes.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI1179. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 1024 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from fullscale for all these tests. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to fullscale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$$

where: $V_{CORR} = 0.5dB$

Total Harmonic Distortion

This is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the 2nd and 3rd harmonic component respectively to the RMS value of the measured input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

Full Power Input Bandwidth

Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Timing Definitions

Sampling Delay (t_{SD})

Sampling delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

This is the RMS variation in the sampling delay due to variation of internal clock path delays.

Data Latency (t_{LAT})

After the analog sample is taken, the data on the bus is available after 2.5 cycles of the clock. This is due to the architecture of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 2.5 cycles.

Output Data Delay (t_D)

Output Data Delay is the delay time from when the data is valid (rising clock edge) to when it shows up at the output bus. This is due to internal delays at the digital output.

December 1993

8-Bit, 20 MSPS Flash A/D Converter

Features

- 20MSPS with No Missing Codes
- 18MHz Full Power Input Bandwidth
- No Missing Codes Over Temperature
- Sample and Hold Not Required
- Single +5V Supply Voltage
- CMOS/TTL
- Overflow Bit
- Improved Replacement for MP7684
- Evaluation Board Available
- /883 Version Available

Applications

- Video Digitizing
- Radar Systems
- Medical Imaging
- Communication Systems
- High Speed Data Acquisition Systems

Description

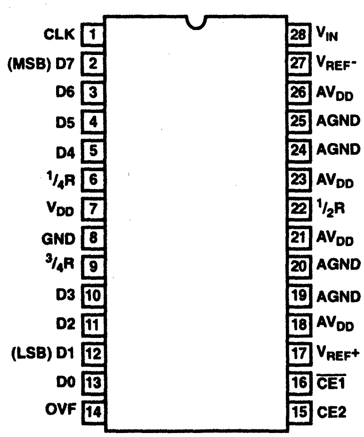
The HI-5700 is a monolithic, 8-bit, CMOS Flash Analog-to-Digital Converter. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 20 MSPS speed is made possible by a parallel architecture which also eliminates the need for an external sample and hold circuit. The HI-5700 delivers ±0.5 LSB differential nonlinearity while consuming only 725mW (typical) at 20 MSPS. Microprocessor compatible data output latches are provided which present valid data to the output bus 1.5 clock cycles after the convert command is received. An overflow bit is provided to allow the series connection of two converters to achieve 9-bit resolution.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-5700J-5	0°C to +70°C	28 Lead Plastic DIP
HI9P5700J-5	0°C to +70°C	28 Lead Plastic SOIC (W)
HI3-5700A-9	-40°C to +85°C	28 Lead Plastic DIP
HI9P5700A-9	-40°C to +85°C	28 Lead Plastic SOIC (W)

Pinout

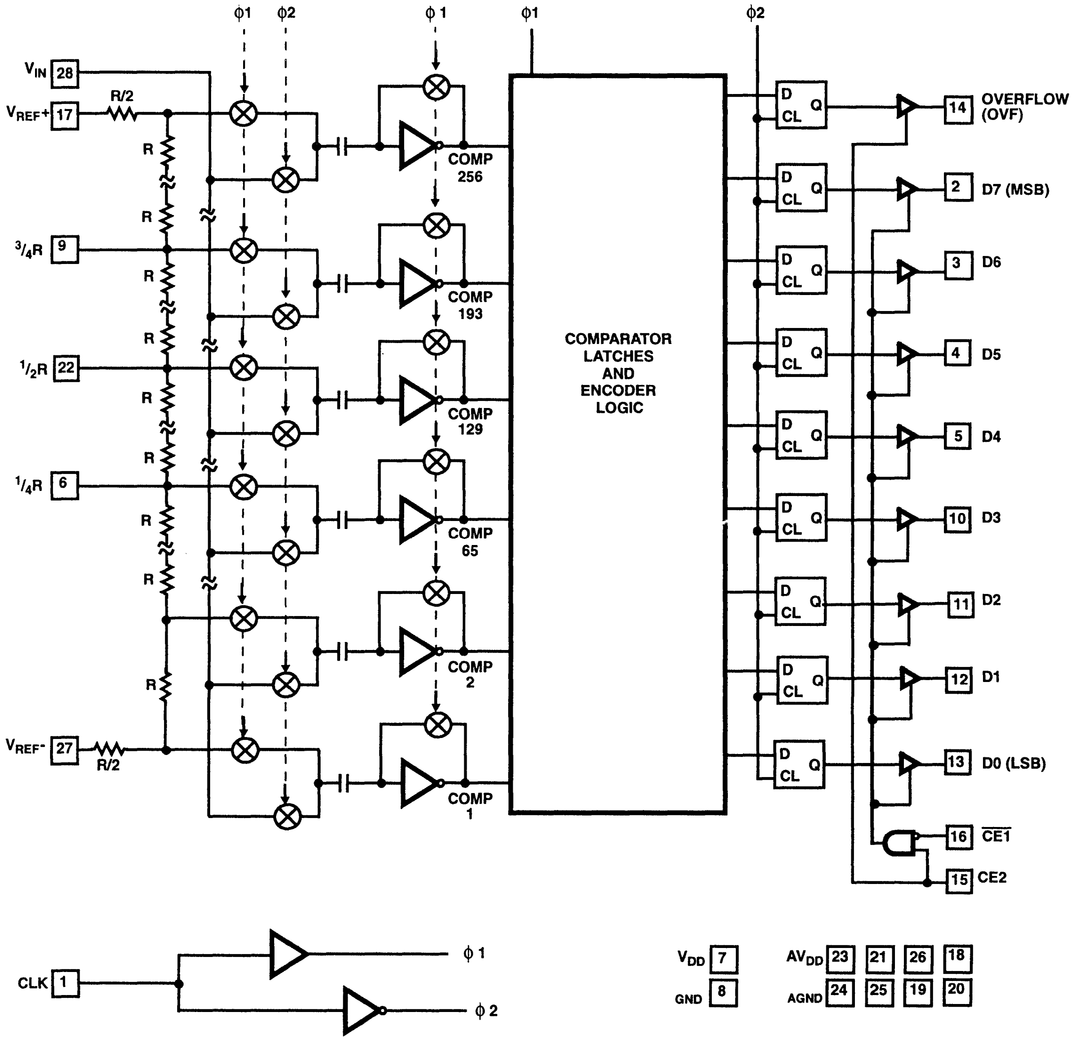
HI-5700
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3174.3

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{DD} to GND . . . . (GND - 0.5) < V_{DD} < +7.0V
Analog and Reference Input Pins. . . .(V_{SS} - 0.5) < V_{INA} < (V_{DD} +0.5V)
Digital I/O Pins . . . . (GND - 0.5) < $V_{I/O}$ < (V_{DD} +0.5V)
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . 300°C
(SOIC - Lead Tips Only)

Thermal Information

Thermal Resistance θ_{JA}
HI3-5700J-5, HI3-5700A-9 . . . . 55°C/W
HI9P5700J-5, HI9P5700A-9 . . . . 75°C/W
Maximum Power Dissipation +70°C 1.05W
Operating Temperature Range
HI3-5700J-5, HI9P5700J-5 . . . . 0°C to +70°C
HI3-5700A-9, HI9P5700A-9 . . . . -40°C to +85°C
Junction Temperature . . . . +150°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Electrical Specifications

$AV_{DD} = V_{DD} = +5.0V$; $V_{REF+} = +4.0V$; V_{REF-} = GND = AGND = 0V; F_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified

PARAMETER	TEST CONDITION	+25°C MIN	+25°C TYP	+25°C MAX	(NOTE 2) 0°C TO +70°C -40°C TO +85°C MIN	(NOTE 2) 0°C TO +70°C -40°C TO +85°C MAX	UNITS
SYSTEM PERFORMANCE							
Resolution		8	-	-	8	-	Bits
Integral Linearity Error (INL) (Best Fit Method)	F_S = 15MHz, f_{IN} = DC	-	±0.9	±2.0	-	±2.25	LSB
	F_S = 20MHz, f_{IN} = DC	-	±1.0	±2.25	-	±3.25	LSB
Differential Linearity Error (DNL) (Guaranteed No Missing Codes)	F_S = 15MHz, f_{IN} = DC	-	±0.4	±0.9	-	±1.0	LSB
	F_S = 20MHz, f_{IN} = DC	-	±0.5	±0.9	-	±1.0	LSB
Offset Error (VOS)	F_S = 15MHz, f_{IN} = DC	-	±5.0	±8.0	-	±9.5	LSB
	F_S = 20MHz, f_{IN} = DC	-	±5.0	±8.0	-	±9.5	LSB
Full Scale Error (FSE)	F_S = 15MHz, f_{IN} = DC	-	±0.5	±4.5	-	±8.0	LSB
	F_S = 20MHz, f_{IN} = DC	-	±0.6	±4.5	-	±8.0	LSB
DYNAMIC CHARACTERISTICS							
Maximum Conversion Rate	No Missing Codes	20	25	-	20	-	MSPS
Minimum Conversion Rate	No Missing Codes (Note 2)	-	-	0.125	-	0.125	MSPS
Full Power Input Bandwidth	F_S = 20MHz	-	18	-	-	-	MHz
Signal to Noise Ratio (SNR) $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	F_S = 15MHz, f_{IN} = 100kHz	-	46.5	-	-	-	dB
	F_S = 15MHz, f_{IN} = 3.58MHz	-	44.0	-	-	-	dB
	F_S = 15MHz, f_{IN} = 4.43MHz	-	43.4	-	-	-	dB
	F_S = 20MHz, f_{IN} = 100kHz	-	45.9	-	-	-	dB
	F_S = 20MHz, f_{IN} = 3.58MHz	-	42.0	-	-	-	dB
	F_S = 20MHz, f_{IN} = 4.43MHz	-	41.6	-	-	-	dB
Signal to Noise and Distortion Ratio (SINAD) $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	F_S = 15MHz, f_{IN} = 100kHz	-	43.4	-	-	-	dB
	F_S = 15MHz, f_{IN} = 3.58MHz	-	34.3	-	-	-	dB
	F_S = 15MHz, f_{IN} = 4.43MHz	-	32.3	-	-	-	dB
	F_S = 20MHz, f_{IN} = 100kHz	-	42.3	-	-	-	dB
	F_S = 20MHz, f_{IN} = 3.58MHz	-	35.2	-	-	-	dB
	F_S = 20MHz, f_{IN} = 4.43MHz	-	32.8	-	-	-	dB
Total Harmonic Distortion (THD)	F_S = 15MHz, f_{IN} = 100kHz	-	-46.9	-	-	-	dBc
	F_S = 15MHz, f_{IN} = 3.58MHz	-	-34.8	-	-	-	dBc
	F_S = 15MHz, f_{IN} = 4.43MHz	-	-32.8	-	-	-	dBc
	F_S = 20MHz, f_{IN} = 100kHz	-	-46.6	-	-	-	dBc
	F_S = 20MHz, f_{IN} = 3.58MHz	-	-36.6	-	-	-	dBc
	F_S = 20MHz, f_{IN} = 4.43MHz	-	-33.5	-	-	-	dBc
Differential Gain	F_S = 14MHz, f_{IN} = 3.58MHz	-	3.5	-	-	-	%
Differential Phase Error	F_S = 14MHz, f_{IN} = 3.58MHz	-	0.9	-	-	-	Degree

Electrical Specifications $AV_{DD} = V_{DD} = +5.0V$; $V_{REF+} = +4.0V$; V_{REF-} = GND = AGND = 0V; F_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	+25°C			(NOTE 2) 0°C TO +70°C -40°C TO +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
ANALOG INPUTS							
Analog Input Resistance, R_{IN}	V_{IN} = 4V	4	10	-	-	-	MΩ
Analog Input Capacitance, C_{IN}	V_{IN} = 0V	-	60	-	-	-	pF
Analog Input Bias Current, IB	V_{IN} = 0V, 4V	-	±0.01	±1.0	-	±1.0	µA
REFERENCE INPUTS							
Total Reference Resistance, R_L		250	330	-	235	-	Ω
Reference Resistance Tempco, T_C		-	+0.31	-	-	-	Ω/°C
DIGITAL INPUTS							
Input Logic High Voltage, V_{IH}		2.0	-	-	2.0	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	-	0.8	V
Input Logic High Current, I_{IH}	V_{IN} = 5V	-	-	1.0	-	1.0	µA
Input Logic Low Current, I_{IL}	V_{IN} = 0V	-	-	1.0	-	1.0	µA
Input Capacitance, C_{IN}		-	7	-	-	-	pF
DIGITAL OUTPUTS							
Output Logic Sink Current, I_{OL}	V_O = 0.4V	3.2	-	-	3.2	-	mA
Output Logic Source Current, I_{OH}	V_O = 4.5V	-3.2	-	-	-3.2	-	mA
Output Leakage, I_{OZ}	CE2 = 0V, V_O = 0V, 5V	-	-	±1.0	-	±1.0	µA
Output Capacitance, C_{OUT}	CE2 = 0V	-	5.0	-	-	-	pF
TIMING CHARACTERISTICS							
Aperture Delay, t_{AP}		-	6	-	-	-	ns
Aperture Jitter, t_{AJ}		-	30	-	-	-	ps
Data Output Enable Time, t_{EN}		-	18	25	-	30	ns
Data Output Disable Time, t_{DIS}		-	15	20	-	25	ns
Data Output Delay, t_{OD}		-	20	25	-	30	ns
Data Output Hold, t_H		10	20	-	5	-	ns
POWER SUPPLY REJECTION							
Offset Error PSRR, ΔVOS	V_{DD} = 5V ±10%	-	±0.1	±2.75	-	±5.0	LSB
Gain Error PSRR, ΔFSE	V_{DD} = 5V ±10%	-	±0.1	±2.75	-	±5.0	LSB
POWER SUPPLY CURRENT							
Supply Current, I_{DD}	F_S = 20MHz	-	145	180	-	190	mA

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Parameter guaranteed by design or characterization and not production tested.

Timing Waveforms

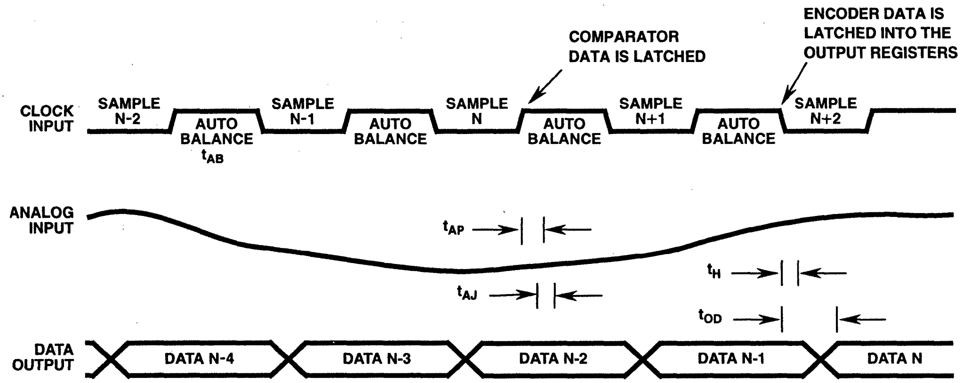


FIGURE 1. INPUT-TO-OUTPUT TIMING

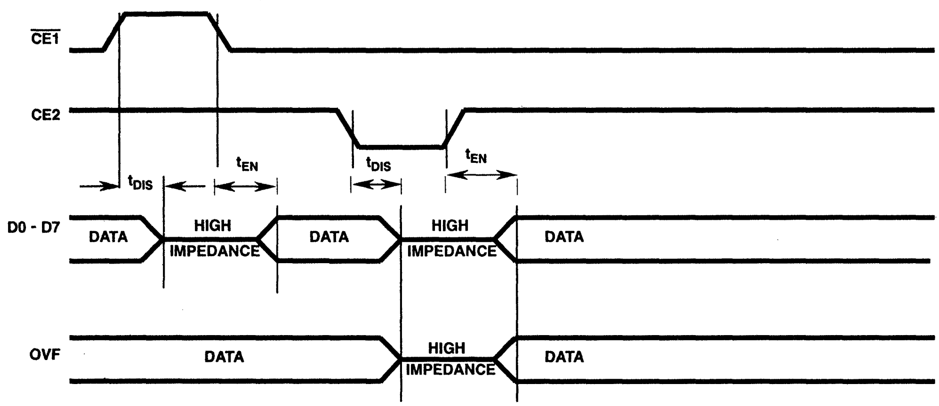


FIGURE 2. OUTPUT ENABLE TIMING

Typical Performance Curves

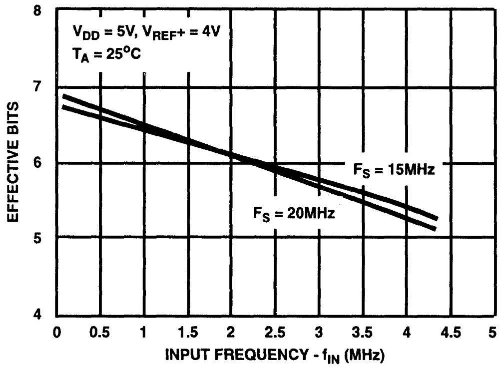


FIGURE 3. EFFECTIVE NUMBER OF BITS vs f_{IN}

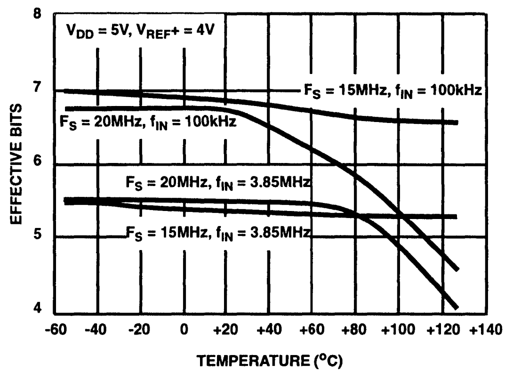


FIGURE 4. EFFECTIVE NUMBER OF BITS vs TEMPERATURE

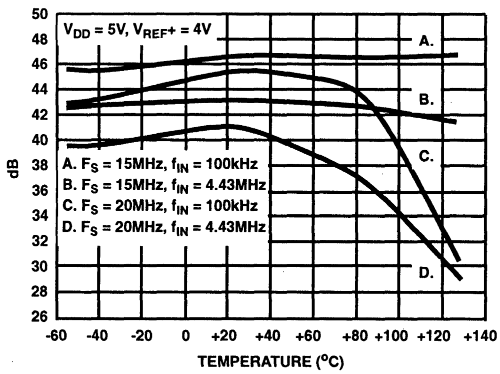


FIGURE 5. SNR vs TEMPERATURE

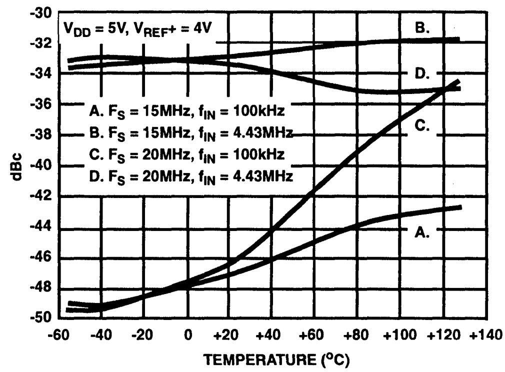


FIGURE 6. TOTAL HARMONIC DISTORTION vs TEMPERATURE

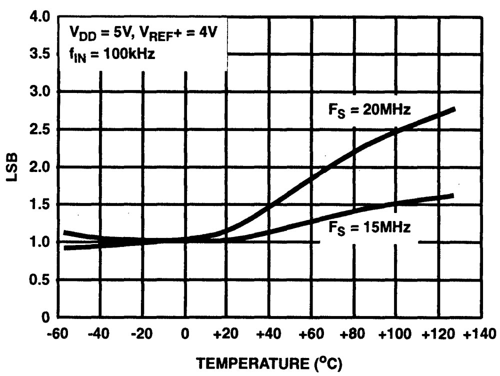


FIGURE 7. INL vs TEMPERATURE

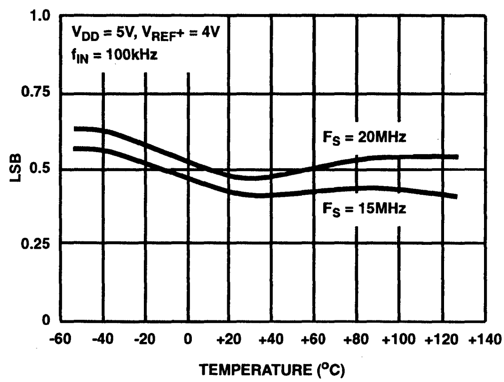


FIGURE 8. DNL vs TEMPERATURE

4

A/D CONVERTERS

Typical Performance Curves (Continued)

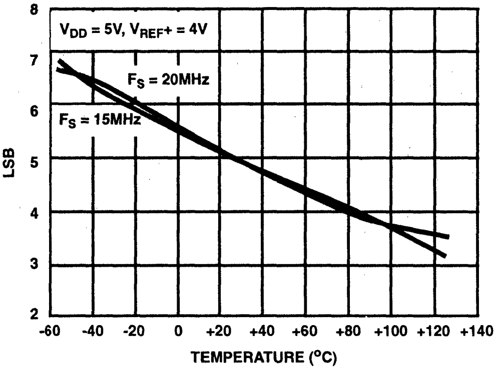


FIGURE 9. OFFSET VOLTAGE vs TEMPERATURE

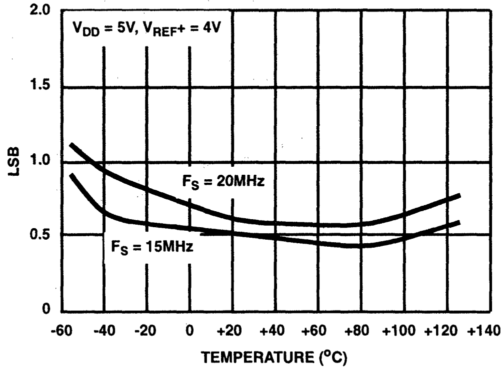


FIGURE 10. FULL SCALE ERROR vs TEMPERATURE

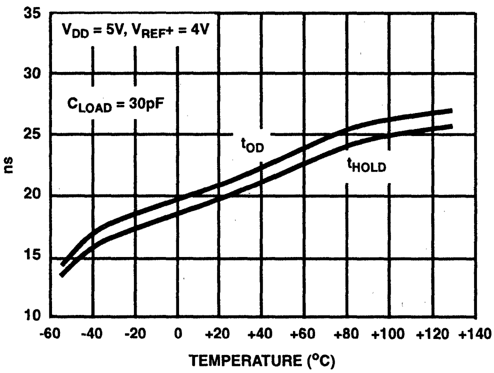


FIGURE 11. OUTPUT DELAY vs TEMPERATURE

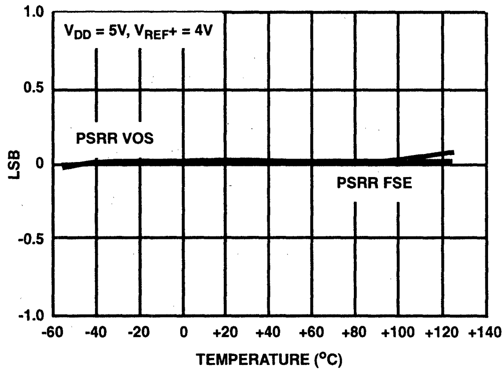


FIGURE 12. POWER SUPPLY REJECTION vs TEMPERATURE

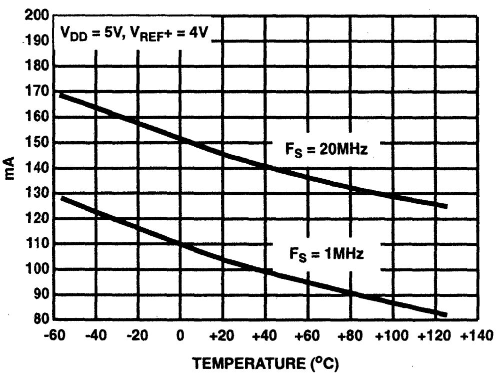


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE

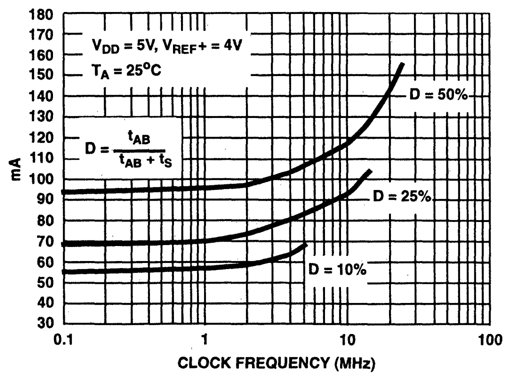


FIGURE 14. SUPPLY CURRENT vs CLOCK DUTY CYCLE

TABLE 1. PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	CLK	Clock Input
2	D7	Bit 7, Output (MSB)
3	D6	Bit 6, Output
4	D5	Bit 5, Output
5	D4	Bit 4, Output
6	$^1/_4$R	$^1/_4$th Point of Reference Ladder
7	V_{DD}	Digital Power Supply
8	GND	Digital Ground
9	$^3/_4$R	$^3/_4$th Point of Reference Ladder
10	D3	Bit 3, Output
11	D2	Bit 2, Output
12	D1	Bit 1, Output
13	D0	Bit 0, Output (LSB)
14	OVF	Overflow, Output
15	CE2	Three-State Output Enable Input, Active High. (See Table 2)
16	$\overline{CE1}$	Three-State Output Enable Input, Active Low. (See Table 2)
17	$V_{REF}+$	Reference Voltage Positive Input
18	AV_{DD}	Analog Power Supply, +5V
19	AGND	Analog Ground
20	AGND	Analog Ground
21	AV_{DD}	Analog Power Supply, +5V
22	$^1/_2$R	$^1/_2$ Point of Reference Ladder
23	AV_{DD}	Analog Power Supply, +5V
24	AGND	Analog Ground
25	AGND	Analog Ground
26	AV_{DD}	Analog Power Supply, +5V
27	$V_{REF}-$	Reference Voltage Negative Input
28	V_{IN}	Analog Input

TABLE 2. CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	D0 - D7	OVF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X's = Don't Care.

Theory of Operation

The HI-5700 is an 8-bit analog-to-digital converter based on a parallel CMOS "flash" architecture. This flash technique is an extremely fast method of A/D conversion because all bit decisions are made simultaneously. In all, 256 comparators are used in the HI-5700: (2^8-1) comparators to encode the output word, plus an additional comparator to detect an overflow condition.

The CMOS HI-5700 works by alternately switching between a "Sample" mode and an "Auto Balance" mode. Splitting up the comparison process in this CMOS technique offers a number of significant advantages. The offset voltage of each CMOS comparator is dynamically canceled with each conversion cycle such that offset voltage drift is virtually eliminated during operation. The block diagram and timing diagram illustrate how the HI-5700 CMOS flash converter operates.

The input clock which controls the operation of the HI-5700 is first split into a non-inverting $\phi 1$ clock and an inverting $\phi 2$ clock. These two clocks, in turn, synchronize all internal timing of analog switches and control logic within the converter.

In the "Auto Balance" mode ($\phi 1$), all $\phi 1$ switches close and $\phi 2$ switches open. The output of each comparator is momentarily tied to its own input, self-biasing the comparator midway between GND and V_{DD} and presenting a low impedance to a small input capacitor. Each capacitor, in turn, is connected to a reference voltage tap from the resistor ladder. The Auto Balance mode quickly precharges all 256 input capacitors between the self-bias voltage and each respective tap voltage.

In the "Sample" mode ($\phi 2$), all $\phi 1$ switches open and $\phi 2$ switches close. This places each comparator in a sensitive high gain amplifier configuration. In this open loop state, the input impedance is very high and any small voltage shift at the input will drive the output either high or low. The $\phi 2$ state also switches each input capacitor from its reference tap to the input signal. This instantly transfers any voltage difference between the reference tap and input voltage to the comparator input. All 256 comparators are thus driven simultaneously to a defined logic state. For example, if the input voltage is at mid-scale, capacitors precharged near zero during $\phi 1$ will push comparator inputs higher than the self bias voltage at $\phi 2$; capacitors precharged near the reference voltage push the respective comparator inputs lower than the bias point. In general, all capacitors precharged by taps above the input voltage force a "low" voltage at comparator inputs; those precharged below the input voltage force "high" inputs at the comparators.

During the next $\phi 1$ Auto-Balancing state, comparator output data is latched into the encoder logic block and the first stage of encoding takes place. The following $\phi 2$ state completes the encoding process. The 8 data bits (plus overflow bit) are latched into the output flip-flops at the next falling clock edge. The Overflow bit is set if the input voltage exceeds $V_{REF}+$ - 0.5 LSB. The output bus may be either enabled or disabled according to the state of $\overline{CE1}$ and CE2 (See Table 2). When disabled, output bits assume a high impedance state.

As shown in the timing diagram, the digital output word becomes valid after the second $\phi 1$ state. There is thus a one and a half cycle pipeline delay between input sample and digital output. "Data Output Delay" time indicates the slight time delay for data to become valid at the end of the $\phi 1$ state.

4

A/D CONVERTERS

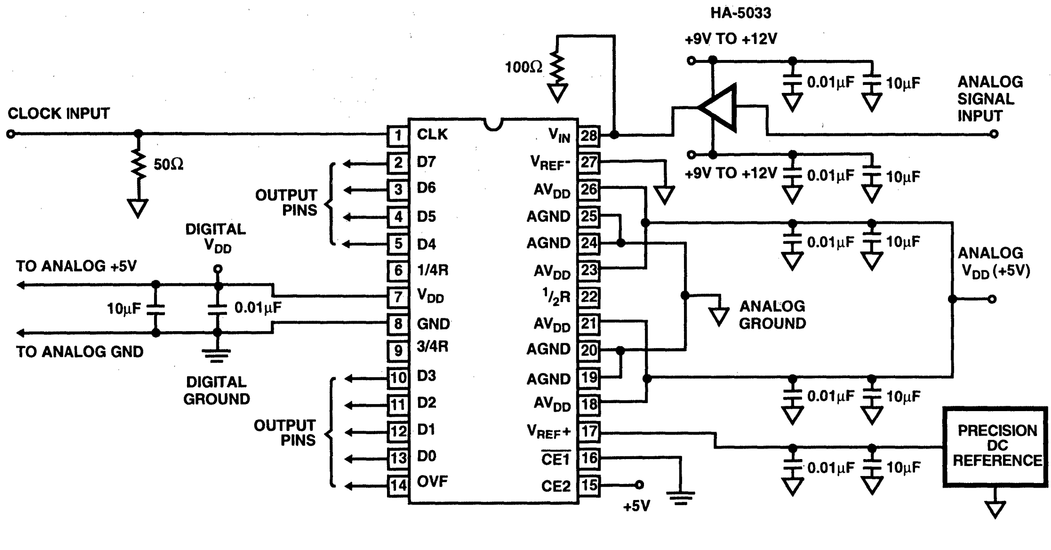


FIGURE 15. TEST CIRCUIT

Applications Information

Voltage Reference

The reference voltage is applied across the resistor ladder between V_{REF}+ and V_{REF}-. In most applications, V_{REF}- is simply tied to analog ground such that the reference source drives V_{REF}+. The reference must be capable of supplying enough current to drive the minimum ladder resistance of 235Ω over temperature.

The HI-5700 is specified for a reference voltage of 4.0V, but will operate with voltages as high as the V_{DD} supply. In the case of 4.0V reference operation, the converter encodes the analog input into a binary output in LSB increments of (V_{REF}+ - V_{REF}-)/256, or 15.6mV. Reducing the reference voltage reduces the LSB size proportionately and thus increases linearity errors. The minimum practical reference voltage is about 2.5V. Because the reference voltage terminals are subjected to internal transient currents during conversion, it is important to drive the reference pins from a low impedance source and to decouple thoroughly. Again, ceramic and tantalum (0.01µF and 10µF) capacitors near the package pin are recommended. It is not necessary to decouple the $^1/_4$R, $^1/_2$R, and $^3/_4$R tap point pins for most applications.

It is possible to elevate V_{REF}- from ground if necessary. In this case, the V_{REF}- pin must be driven from a low impedance reference capable of sinking the current through the resistor ladder. Careful decoupling is again recommended.

Digital Control and Interface

The HI-5700 provides a standard high speed interface to external CMOS and TTL logic families. Two chip enable inputs control the three-state outputs of output bits D0 through D7 and the Overflow (OVF) bit. As indicated in the Truth Table, all output bits are high impedance when CE2 is low, and output bits D0 through D7 are independently controlled by $\overline{CE1}$.

Although the Digital Outputs are capable of handling typical data bus loading, the bus capacitance charge/discharge currents will produce supply and local group disturbances. Therefore, an external bus driver is recommended.

Clock

The clock should be properly terminated to digital ground near the clock input pin. Clock frequency defines the conversion frequency and controls the converter as described in the "Theory of Operation" section. The Auto Balance $\phi1$ half cycle of the clock may be reduced to approximately 20ns; the Sample $\phi2$ half cycle may be varied from a minimum of 25ns to a maximum of 5µs.

Signal Source

A current pulse is present at the analog input (V_{IN}) at the beginning of every sample and auto balance period. The transient current is due to comparator charging and switch feedthrough in the capacitor array. It varies with the amplitude of the analog input and the converter's sampling rate.

The signal source must absorb these transients prior to the end of the sample period to ensure a valid signal for conversion. Suitable broad band amplifiers or buffers which exhibit low output impedance and high output drive include the HA-5004, HA-5002, and HA-5003.

The signal source may drive above or below the power supply rails, but should not exceed 0.5V beyond the rails or damage may occur. Input voltages of -0.5V to +0.5 LSB are converted to all zeroes; input voltages of V_{REF}+ -0.5 LSB to V_{DD} +0.5V are converted to all ones with the Overflow bit set.

Full Scale Offset Error Adjustment

In applications where accuracy is of utmost importance, three adjustments can be made; i.e., offset, gain, and reference tap point trims. In general, offset and gain correction can be done in the preamp circuitry.

Offset Adjustment

Offset correction can be done in the preamp driving the converter by introducing a DC component to the input signal. An alternate method is to adjust V_{REF}- to produce the desired offset. It is adjusted such that the 0 to 1 code transition occurs at 0.5 LSB.

Gain Adjustment

In general, full scale error correction can be done in the preamp circuitry by adjusting the gain of the op amp. An alternate method is to adjust the V_{REF}+ voltage. The reference voltage is the ideal location.

Quarter Point Adjustment

The reference tap points are brought out for linearity adjustment or creating a nonlinear transfer function if desired. It is not necessary to decouple the $^1/_4$R, $^1/_2$R, and $^3/_4$R tap points in most applications.

Power Supplies

The HI-5700 operates nominally from 5V supplies but will work from 3V to 6V. Power to the device is split such that analog and digital circuits within the HI-5700 are powered separately. The analog supply should be well regulated and "clean" from significant noise, especially high frequency noise. The digital supply should match the analog supply within about 0.5V and should be referenced externally to the analog supply at a single point. Analog and digital grounds should not be separated by more that 0.5V. It is recommended that power supply decoupling capacitors be placed as close to the supply pins as possible. A combination of 0.01μF ceramic and 10μF tantalum capacitors is recommended for this purpose as shown in the test circuit.

Reducing Power Consumption

Power dissipation in the HI-5700 is related to clock frequency and clock duty cycle. For a fixed 50% clock duty cycle, power may be reduced by lowering the clock frequency. For a given conversion frequency, power may be reduced by decreasing the Auto-Balance (ϕ1) portion of the clock duty cycle. This relationship is illustrated in the performance curves.

TABLE 3. CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE † V_{REF}+ = 4.0V V_{REF}- = 0.0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE								
				MSB							LSB
			OVF	D7	D6	D5	D4	D3	D2	D1	D0
Overflow (OVF)	4.000	511	1	1	1	1	1	1	1	1	1
Full Scale (FS)	3.9766	255	0	1	1	1	1	1	1	1	1
FS - 1 LSB	3.961	254	0	1	1	1	1	1	1	1	0
3/4 FS	2.992	192	0	1	1	0	0	0	0	0	0
1/2 FS	1.992	128	0	1	0	0	0	0	0	0	0
1/4 FS	0.992	64	0	0	1	0	0	0	0	0	0
1 LSB	0.0078	1	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0

† The voltages listed above represent the ideal transition of each output code shown as a function of the reference voltage.

Glossary of Terms

Aperture Delay: Aperture delay is the time delay between the external sample command (the rising edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter: This is the RMS variation in the aperture delay due to variation of internal $\phi 1$ and $\phi 2$ clock path delays and variation between the individual comparator switching times.

Differential Linearity Error (DNL): The differential linearity error is the difference in LSBs between the spacing of the measured midpoint of adjacent codes and the spacing of ideal midpoints of adjacent codes. The ideal spacing of each midpoint is 1.0 LSB. The range of values possible is from -1.0 LSB (which implies a missing code) to greater than +1.0 LSB.

Full Power Input Bandwidth: Full power input bandwidth is the frequency at which the amplitude of the fundamental of the digital output word has decreased 3dB below the amplitude of an input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Full Scale Error (FSE): Full Scale Error is the difference between the actual input voltage of the 254 to 255 code transition and the ideal value of $V_{REF}+$ - 1.5 LSB. This error is expressed in LSBs.

Integral Linearity Error (INL): The integral linearity error is the difference in LSBs between the measured code centers and the ideal code centers. The ideal code centers are calculated using a best fit line through the converter's transfer function.

LSB: Least Significant Bit = ($V_{REF}+$ - $V_{REF}-$)/256. All HI-5700 specifications are given for a 15.6mV LSB size $V_{REF}+$ = 4.0V, $V_{REF}-$ = 0.0V.

Offset Error (VOS): Offset error is the difference between the actual input voltage of the 0 to 1 code transition and the ideal value of $V_{REF}-$ + 0.5 LSB, V_{OS} Error is expressed in LSBs.

Power Supply Rejection Ratio (PSRR): PSRR is expressed in LSBs and is the maximum shift in code transition points due to a power supply voltage shift. This is measured at the 0 to 1 code transition point and the 254 to 255 code transition point with a power supply voltage shift from the nominal value of 5.0V.

Signal to Noise Ratio (SNR): SNR is the ratio in dB of the RMS signal to RMS noise at specified input and sampling frequencies.

Signal to Noise and Distortion Ratio (SINAD): SINAD is the ratio in dB of the RMS signal to the RMS sum of the noise and harmonic distortion at specified input and sampling frequencies.

Total Harmonic Distortion (THD): THD is the ratio in dBc of the RMS sum of the first five harmonic components to the RMS signal for a specified input and sampling frequency.

Die Characteristics

DIE DIMENSIONS:
154.3 x 173.2 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

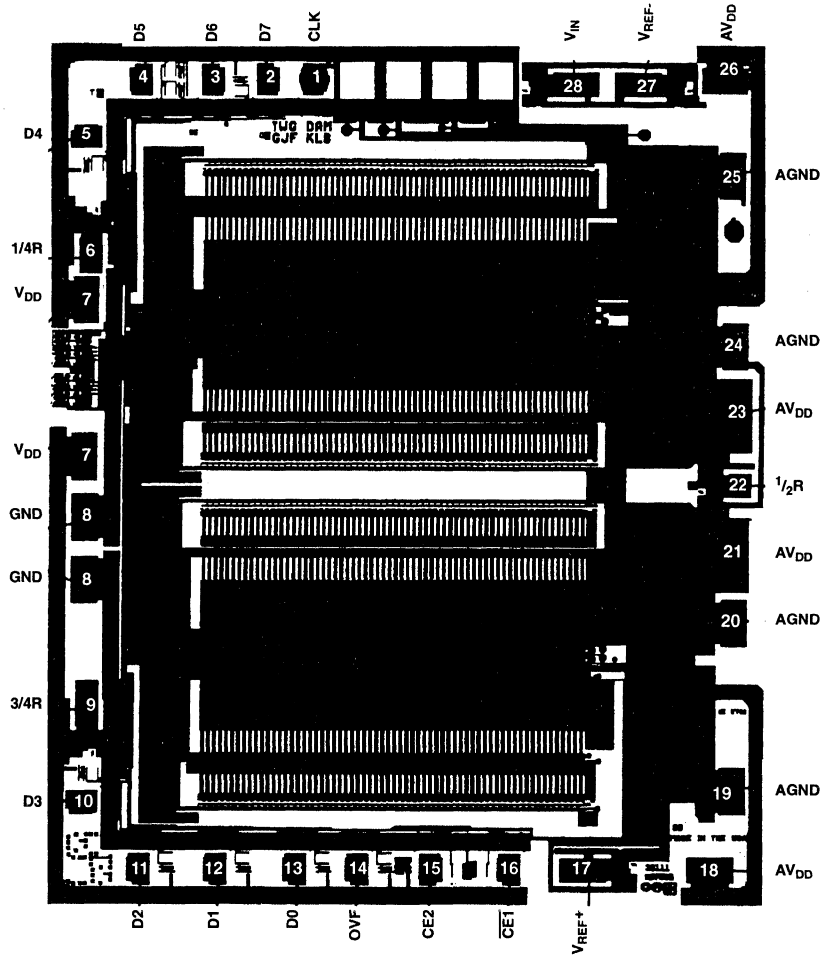
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

TRANSISTOR COUNT: 8000

SUBSTRATE POTENTIAL (Powered Up): V+

Metallization Mask Layout

HI-5700



February 1995

10-Bit, 40 MSPS A/D Converter

Features

- 40 MSPS Sampling Rate
- 8.3 Bits Guaranteed at f_{IN} = 10MHz
- Low Power
- Wide 250MHz Full Power Input Bandwidth
- Sample and Hold Not Required
- Single-Ended or Differential Input
- 1.25V Input Signal Range
- Single +5V Supply Voltage
- TTL Compatible Interface
- Evaluation Boards Available (HI5702-EV, HI5702-EV2)

Applications

- Professional Video Digitizing
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition

Description

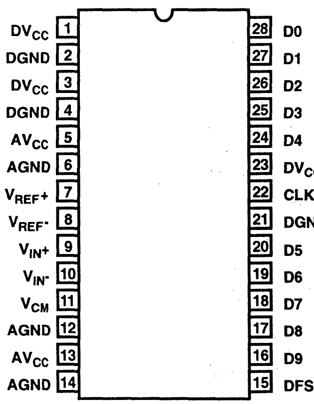
The HI5702 is a monolithic, 10-bit, analog-to-digital converter fabricated in Harris's HBC10 BiCMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 40 MSPS speed is made possible by a fully differential pipeline architecture which also eliminates the need for an external sample and hold circuit. The HI5702 has excellent dynamic performance while consuming <650mW power at 40 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles.

Ordering Information

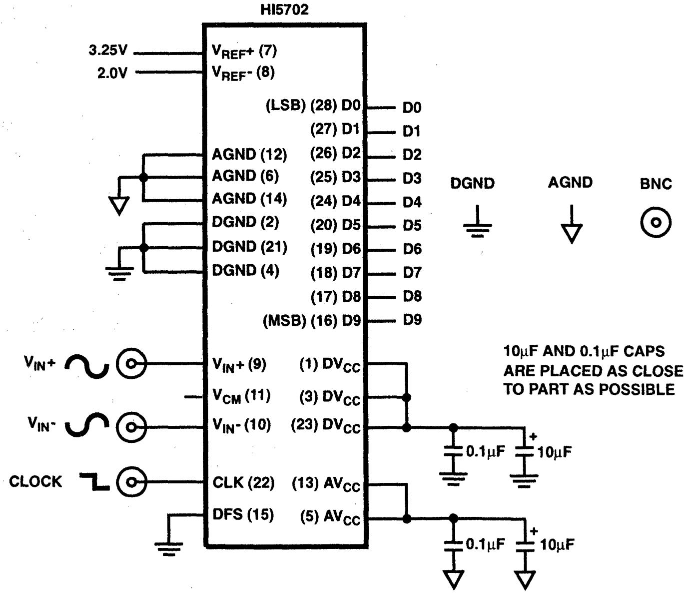
PART NUMBER	SAMPLE RATE	TEMPERATURE RANGE	PACKAGE
HI5702KCB	40 MSPS	0^oC to $+70^oC$	28 Lead Plastic SOIC (W)
HI5702JCB	36 MSPS	0^oC to $+70^oC$	28 Lead Plastic SOIC (W)

Pinout

HI5702 (SOIC)
TOP VIEW

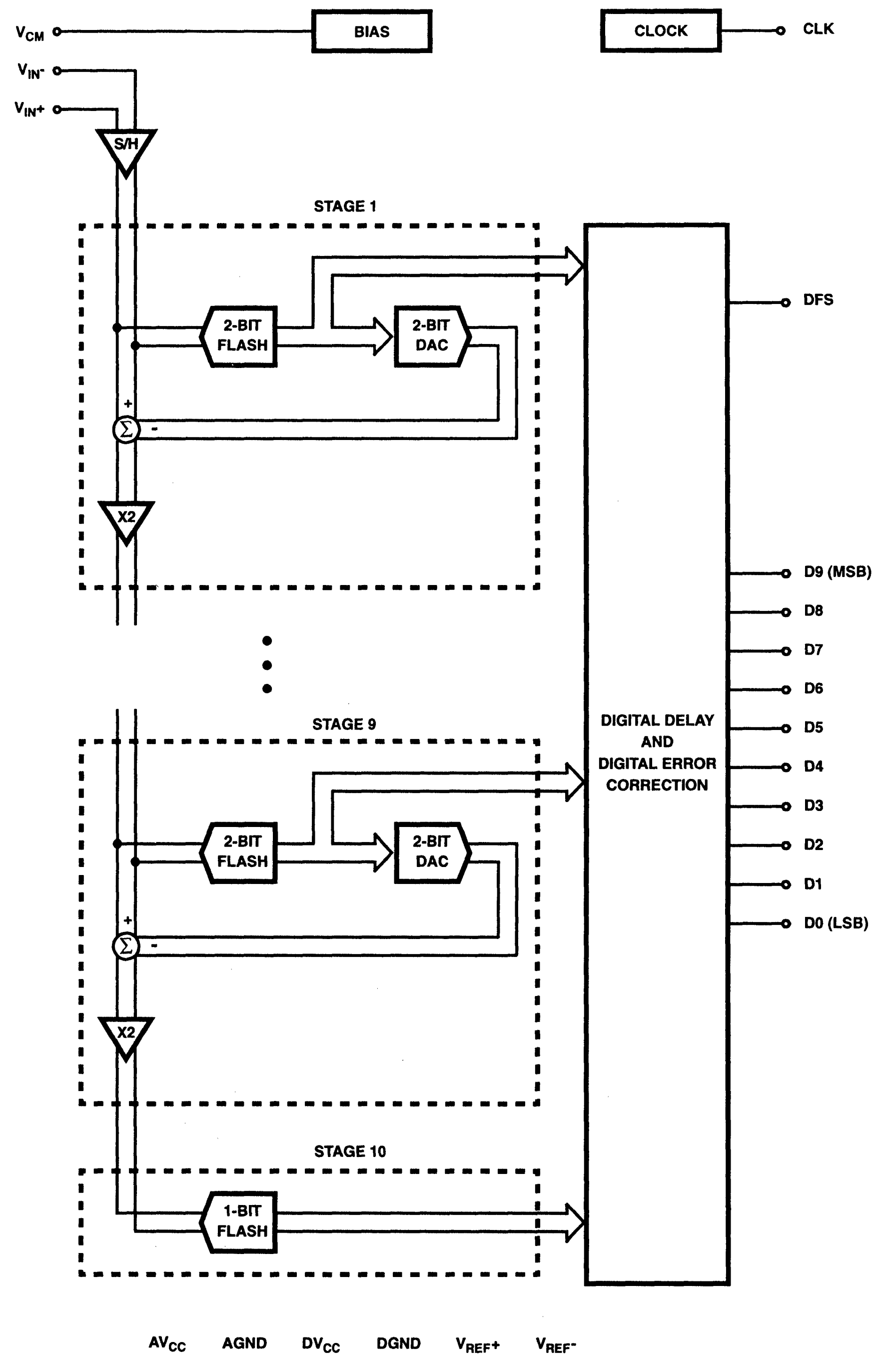


Typical Application Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND . . . . +6V
DGND to AGND 0.3V
Digital I/O Pins . . . . DGND to DV_{CC}
Analog I/O Pins. . . . . AGND to AV_{CC}
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . +300°C
(Lead Tips Only)

Thermal Information

Thermal Resistance θ_{JA}
HI5702KCB/JCB . . . . 75°C/W
Maximum Junction Temperature. . . . . +150°C
Operating Temperature Range
HI5702KCB/JCB . . . . 0°C to +70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

AV_{CC} = DV_{CC} = +5.0V; $V_{REF}+$ = 3.25V; $V_{REF}-$ = 2.0V; F_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 20pF; T_A = +25°C; Unless Otherwise Specified

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		10	-	-	Bits
Integral Linearity Error (INL)	f_{IN} = DC	-	±1	±2.0	LSB
Differential Linearity Error (DNL) (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1	LSB
Offset Error (V_{OS})	f_{IN} = DC	-	3	-	LSB
Full Scale Error (FSE)	f_{IN} = DC	-	2	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	-	MSPS
Maximum Conversion Rate	No Missing Codes HI5702KCB	40	-	-	MSPS
	HI5702JCB	36	-	-	MSPS
Effective Number of Bits (ENOB)	f_{IN} = 1MHz	-	9.0	-	Bits
	f_{IN} = 5MHz	-	9.0	-	Bits
	f_{IN} = 10MHz	8.3	8.8	-	Bits
Signal to Noise Ratio (SNR) $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 1MHz	-	57	-	dB
	f_{IN} = 5MHz	-	57	-	dB
	f_{IN} = 10MHz	51	56	-	dB
Signal to Noise and Distribution Ratio (SINAD) $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	-	56	-	dB
	f_{IN} = 5MHz	-	56	-	dB
	f_{IN} = 10MHz	51	55	-	dB
Total Harmonic Distortion (THD)	f_{IN} = 1MHz	-	-64	-	dBc
	f_{IN} = 5MHz	-	-63	-	dBc
	f_{IN} = 10MHz	-	-60	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	-75	-	dBc
	f_{IN} = 5MHz	-	-75	-	dBc
	f_{IN} = 10MHz	-	-73	-	dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	-66	-	dBc
	f_{IN} = 5MHz	-	-64	-	dBc
	f_{IN} = 10MHz	-	-63	-	dBc
Spurious Free Dynamic Range (SFDR)	f_{IN} = 1MHz	-	66	-	dBc
	f_{IN} = 5MHz	-	64	-	dBc
	f_{IN} = 10MHz	54	63	-	dBc
Intermodulation Distortion (IMD)	f1 = 1MHz, f2 = 1.02MHz	-	-59	-	dBc
Differential Gain Error	F_S = 17.72MHz, 6 Step, Mod Ramp	-	0.5	1	%
Differential Phase Error	F_S = 17.72MHz, 6 Step, Mod Ramp	-	0.25	0.5	Degree

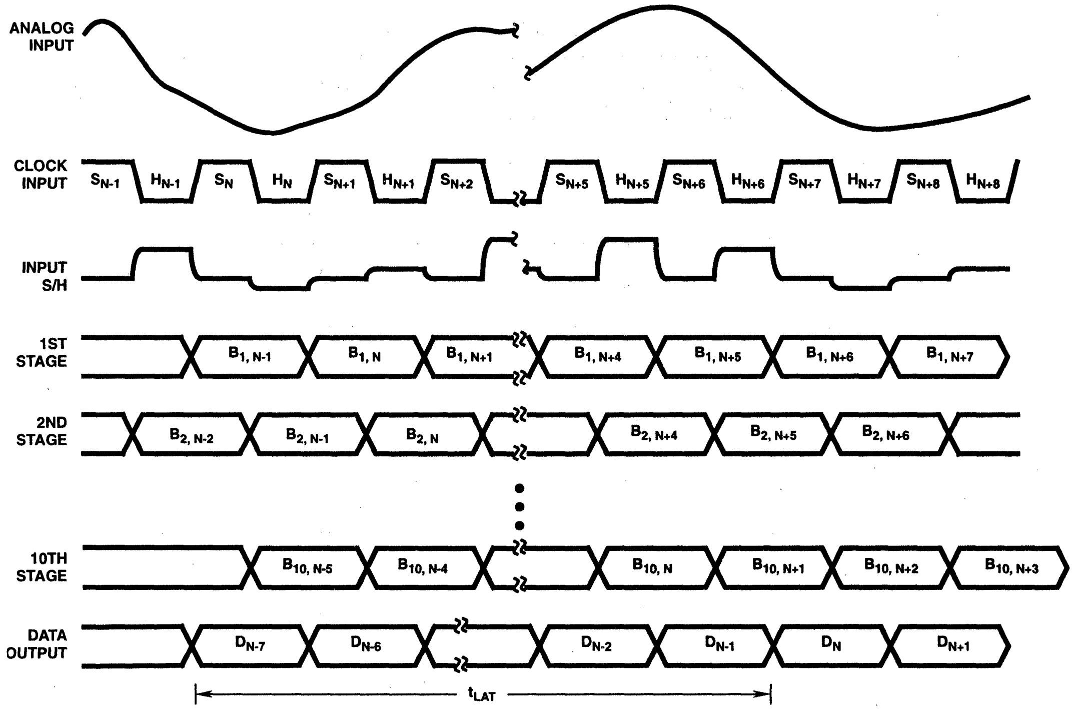
Electrical Specifications $AV_{CC} = DV_{CC} = +5.0V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2.0V$; F_S = Specified Clock Frequency at 50% Duty Cycle; $C_L = 20pF$; $T_A = +25^oC$; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Transient Response		-	1	-	Cycle
Overvoltage Recovery	0.2V Overdrive	-	1	-	Cycle
ANALOG INPUT					
Analog Input Resistance, R_{IN}	(Note 2)	-	1	-	MΩ
Analog Input Capacitance, C_{IN}		-	7	-	pF
Analog Input Bias Current, I_B	(Note 2)	-50	-	+50	µA
Full Power Input Bandwidth		-	250	-	MHz
Analog Input Common Mode Range ($V_{IN}+ + V_{IN}-$) / 2	Differential Mode (Note 1)	0.625	-	4.375	V
REFERENCE INPUT					
Total Reference Resistance, R_L		200	400	-	Ω
Reference Current		-	3	6	mA
Positive Reference Input, $V_{REF}+$	(Note 1)	-	3.25	3.3	V
Negative Reference Input, $V_{REF}-$	(Note 1)	1.95	2.0	-	V
Reference Common Mode Voltage ($V_{REF}+ + V_{REF}-$) / 2	(Note 1)	2.575	2.625	2.675	V
COMMOM MODE VOLTAGE					
Common Mode Voltage Output, V_{CM}		-	2.8	-	V
Max Output Current		-	-	1	mA
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Current, I_{IH}	$V_{IN} = 5V$	-	-	10.0	µA
Input Logic Low Current, I_{IL}	$V_{IN} = 0V$	-	-	10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS					
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$	3.2	-	-	mA
Output Logic Source Current, I_{OH}	$V_O = 2.4V$	-0.2	-	-	mA
Output Capacitance, C_{OUT}		-	5	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps
Data Output Delay, t_{OD}		-	6	-	ns
Data Output Hold, t_H		-	5	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 1)	-	-	7	Cycles
Power-Up Initialization	Data Invalid Time (Note 1)	-	-	20	Cycles
POWER SUPPLY CHARACTERISTICS					
Supply Current, I_{CC}	$V_{IN} = 0V$	-	120	130	mA
Power Dissipation	$V_{IN} = 0V$	-	600	650	mW
Offset Error PSRR, ΔV_{OS}	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	0.2	-	LSB
Gain Error PSRR, ΔFSE	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	1	-	LSB

NOTES:

1. Parameter guaranteed by design or characterization and not production tested.
2. With the clock off.

Timing Waveforms



NOTES:

1. S_N: N-th sampling period.
2. H_N: N-th holding period.
3. $B_{M, N}$: M-th stage digital output corresponding to N-th sampled input.
4. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5702 INTERNAL CIRCUIT TIMING

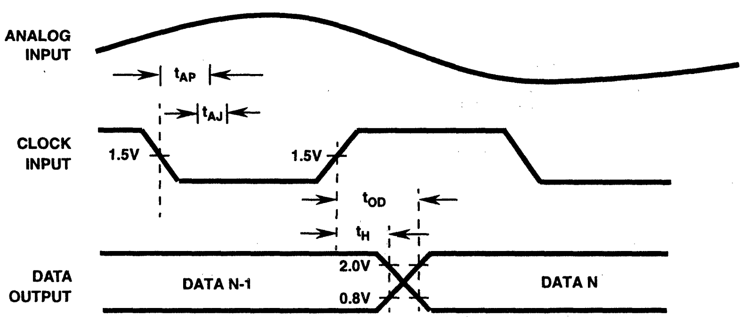


FIGURE 2. INPUT-TO-OUTPUT TIMING

Typical Performance Curves

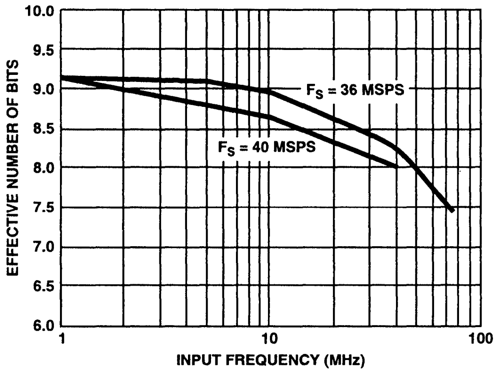


FIGURE 3. ENOB vs INPUT FREQUENCY

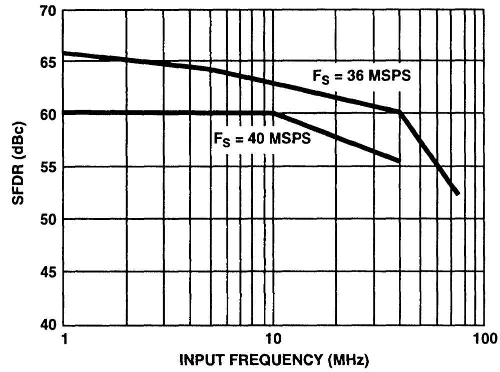


FIGURE 4. SFDR vs INPUT FREQUENCY

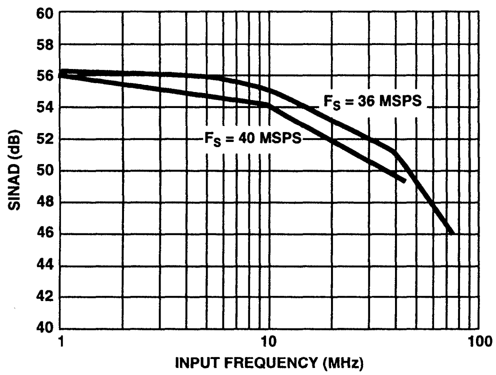


FIGURE 5. SINAD vs INPUT FREQUENCY

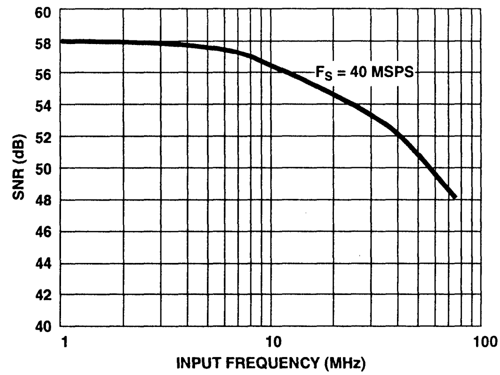


FIGURE 6. SNR vs INPUT FREQUENCY

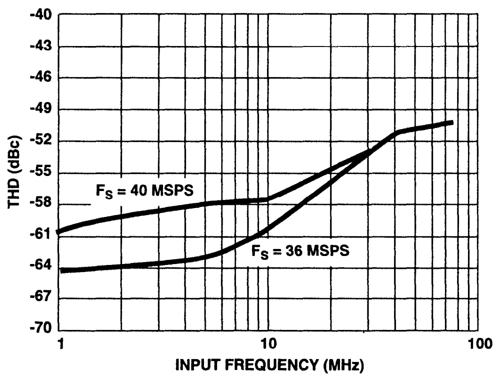


FIGURE 7. THD vs INPUT FREQUENCY

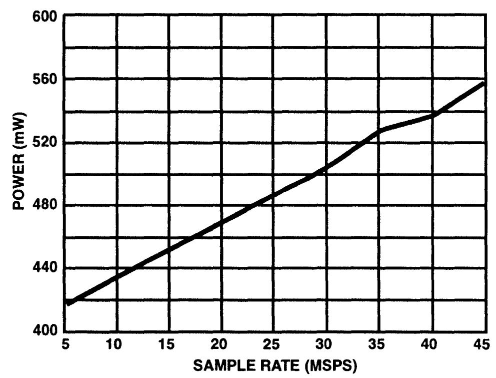


FIGURE 8. POWER DISSIPATION vs SAMPLE RATE

Typical Performance Curves (Continued)

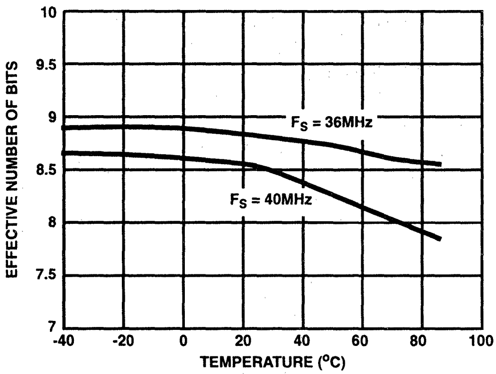


FIGURE 9. ENOB vs TEMPERATURE

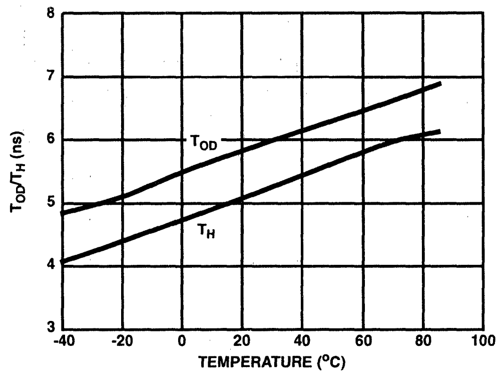


FIGURE 10. T_{OH}/T_D vs TEMPERATURE

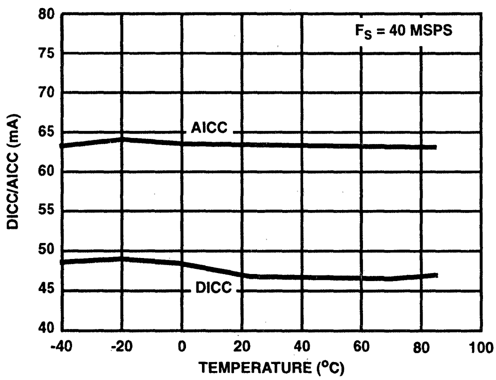


FIGURE 11. SUPPLY CURRENT vs TEMPERATURE

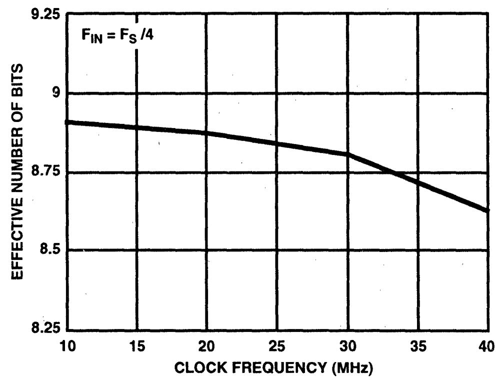


FIGURE 12. ENOB vs SAMPLE RATE WITH FIXED 12.5ns CLOCK PULSE WIDTH

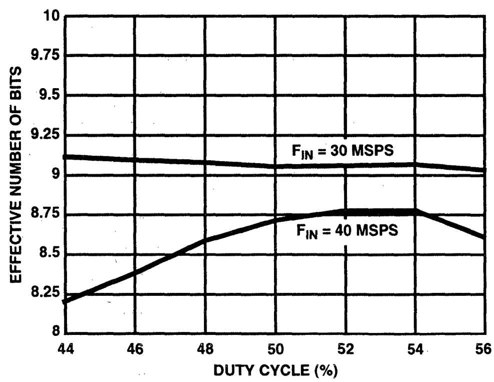


FIGURE 13. ENOB vs DUTY CYCLE

TABLE 1. PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	DV_{CC}	Digital Supply
2	DGND	Digital Ground
3	DV_{CC}	Digital Supply
4	DGND	Digital Ground
5	AV_{CC}	Analog Supply
6	AGND	Analog Ground
7	$V_{REF}+$	Positive Reference
8	$V_{REF}-$	Negative Reference
9	$V_{IN}+$	Positive Analog Input
10	$V_{IN}-$	Negative Analog Input
11	V_{CM}	DC Output Voltage Source
12	AGND	Analog Ground
13	AV_{CC}	Analog Supply
14	AGND	Analog Ground
15	DFS	Data Format Select
16	D9	Data Bit 9 Output (MSB)
17	D8	Data Bit 8 Output
18	D7	Data Bit 7 Output
19	D6	Data Bit 6 Output
20	D5	Data Bit 5 Output
21	DGND	Digital Ground
22	CLK	Input Clock
23	DV_{CC}	Digital Supply
24	D4	Data Bit 4 Output
25	D3	Data Bit 3 Output
26	D2	Data Bit 2 Output
27	D1	Data Bit 1 Output
28	D0	Data Bit 0 Output (LSB)

Detailed Description

Theory of Operation

The HI5702 is a 10-bit fully differential sampling pipeline A/D converter with digital error correction. Figure 13 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The small values of these components result in a typical full power bandwidth of 250MHz.

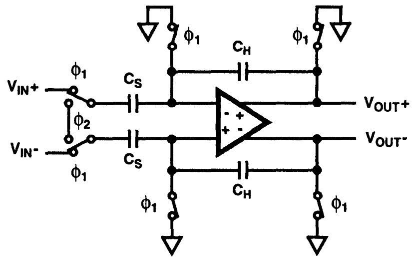


FIGURE 14. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the Functional Block Diagram and the Timing Diagram in Figure 1, nine identical pipeline subconverter stages, each containing a two-bit flash and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the tenth stage being a one bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual sub-converter clock signal is offset by 180 degrees from the previous stage clock signal with the result that alternate stages in the pipeline will perform the same operation.

The two-bit digital output of each stage is fed to a digital delay line controlled by the internal clock. The purpose of the delay line is to align the digital output data to the corresponding sampled analog input signal. This delayed data is fed to the digital error correction circuit which corrects the error in the output data with the information contained in the redundant bits to form the final 10-bit output for the converter.

Because of the pipeline nature of this converter, the data on the bus is output at the 7th cycle of the clock after the analog sample is taken. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The output data is synchronized to the external clock by a double buffered latching technique.

The output of the digital correction circuit is available in two's complement or binary format depending on the condition of the Data Format Select (DFS) input.

Analog Input, Differential Connection

The analog input to the HI5702 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 15) will give the best performance for the converter.

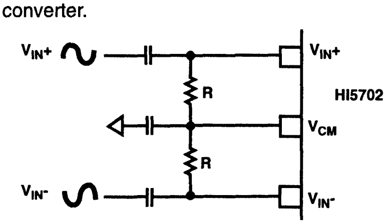


FIGURE 15. AC COUPLED DIFFERENTIAL INPUT

4

A/D CONVERTERS

Since the HI5702 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V, which implies the common mode voltage can range of 0.625V to 4.375V. The performance of the ADC does not change significantly with the value of the common mode voltage.

A DC voltage source, V_{CM}, about half way between the top and bottom reference voltages, is made available to the user to help simplify circuit design when using a differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent bias source and stays within the common mode range over temperature. It has a temperature coefficient of about 200ppm.

Assume the difference between $V_{REF}+$, typically 3.25V, and $V_{REF}-$, typically 2V, is 1.25V in Figure 15. Fullscale is achieved when $V_{IN}+$ and $V_{IN}-$ inputs are $1.25V_{P-P}$, with $V_{IN}-$ being 180 degrees out of phase with $V_{IN}+$. The converter will be at positive fullscale when the $V_{IN}+$ input is at V_{CM} + 0.625V and $V_{IN}-$ is at V_{CM} - 0.625V ($V_{IN}+ - V_{IN}- = 1.25V$). Conversely, the ADC will be at negative fullscale when the $V_{IN}+$ input is equal to V_{CM} - 0.625V and $V_{IN}-$ is at V_{CM} + 0.625V ($V_{IN}+ - V_{IN}- = -1.25V$).

The analog input can be DC coupled as long as the inputs are within the common mode range, Figure 16.

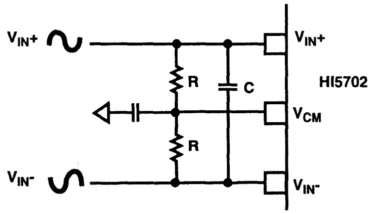


FIGURE 16. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 16 are not absolutely necessary but will improve performance. Values of 100Ω or less are typical. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help common mode any noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well.

Analog Input, Single-Ended Connection

The configuration shown in Figure 17 may be used with a single ended AC coupled input.

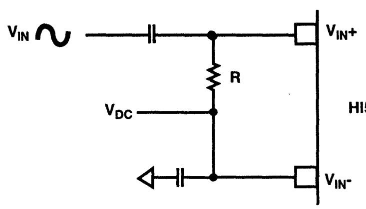


FIGURE 17. AC COUPLED SINGLE ENDED INPUT

Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND.

Again, assume the difference between $V_{REF}+$, typically 3.25V, and $V_{REF}-$, typically 2V, is 1.25V. If V_{IN} is a $2.5V_{P-P}$ sinewave riding on a positive voltage equal to V_{DC}, the converter will be at positive fullscale when $V_{IN}+$ is at V_{DC} + 1.25V and will be at negative fullscale when V_{IN} is equal to V_{DC} - 1.25V. In this case, V_{DC} could range between 1.25V and 3.75V without a significant change in ADC performance. The simplest way to produce V_{DC} is to use the V_{CM} output of the HI5702.

The analog input can be DC coupled as long as the input is within the common mode range, Figure 18.

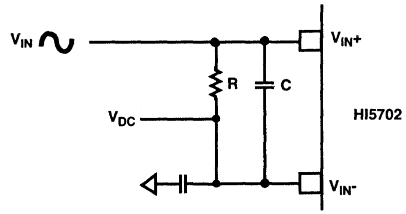


FIGURE 18. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 18 is not absolutely necessary but will improve performance. Values of 100Ω or less are typical. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help common mode any noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well.

A single ended source may give better overall system performance if it is first converted to differential before driving the HI5702. Also refer to the application note AN9413, "Driving the Analog Input of the HI5702". This application note describes several different ways of driving the analog differential inputs.

Reference Input, $V_{REF}-$ $V_{REF}+$

The converter requires two reference voltages connected to the V_{REF} pins. The voltage range of the part with a differential input will be $V_{REF}+$ - $V_{REF}-$. The HI5702 is tested with $V_{REF}-$ equal to 2V and $V_{REF}+$ equal to 3.25V for an input range of 1.25V. $V_{REF}+$ and $V_{REF}-$ can differ from the above voltages as long as the common mode voltage between the reference pins (($V_{REF}+$ + $V_{REF}-$) / 2) does not exceed 2.65V ±50mV and the limits on $V_{REF}+$ and $V_{REF}-$ are not exceeded.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference input pin.

Digital Control and Clock Requirements

The HI5702 provides a standard high-speed interface to external TTL logic families.

In order to ensure rated performance of the HI5702, the duty cycle of the clock should be held at 50%. It must also have low jitter and operate at standard TTL levels.

A Data Format Select (DFS) pin is provided which will determine the format of the digital data. When at logic low the data will be output in offset binary format. When at a logic high the data will be output in a two's complement format. Refer to Table 2 for further information.

Performance of the HI5702 will only be guaranteed at conversion rates above 1 MSPS. This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1 MSPS will have to be performed before valid data is available.

Supply and Ground Considerations

The HI5702 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5702 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the Application Note "Using Harris High Speed A/D Converters" (AN9214) for additional considerations when using high speed converters.

Increased Accuracy

The V_{OS} and FSE errors as reported on the data sheet can be decreased by further calibration of the ADC. It will be assumed that the converter has offset binary coding. See the A/D code table (Table 2) for the ideal code transitions.

The first step would be to center the analog input to the desired midscale voltage. This voltage would then be adjusted up or down in the circuitry driving one side of the input to the HI5702 until the 511 to 512 transition occurs on the digital output.

Next, set the analog input to the HI5702 to the desired positive fullscale voltage. Adjust one side of the reference circuit up or down until the 1022 to 1023 transition occurs on the digital output of the converter.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level 1/4 LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for a analog input that is 1 and 3/4 LSB's below positive full-scale with the offset error removed. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection Ratio (PSRR)

Each of the power supplies are moved plus and minus 5% and the shift in the offset and gain error (in LSB's) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5702. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full-scale for all these tests.

SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

TABLE 2. A/D CODE TABLE

CODE DESCRIPTION	(NOTE 1) DIFFERENTIAL INPUT VOLTAGE $V_{REF}+ = 3.25V$ $V_{REF}- = 2.0V$ (V)	OFFSET BINARY OUTPUT CODE (DFS LOW)										TWO'S COMPLEMENT OUTPUT CODE (DFS HIGH)									
		MSB									LSB	MSB									LSB
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full Scale (FS)	1.25V	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
FS - 1 3/4 LSB	1.2479V	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
1/2 FS + 1/4 LSB	0.3mV	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1/2 FS - 3/4 LSB	2.1mV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1 1/4 LSB	-1.2485V	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
Zero	-1.25V	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

NOTE:

1. The voltages listed above represent the ideal transition of each output code shown as a function of the reference voltage.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$$

where: $V_{CORR} = 0.5dB$

V_{CORR} adjusts the ENOB for the amount the input is below fullscale.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present on the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are $(f_1 + f_2)$, $(f_1 - f_2)$, $(2f_1)$, $(2f_2)$, $(2f_1 + f_2)$, $(2f_1 - f_2)$, $(f_1 + 2f_2)$, $(f_1 - 2f_2)$. The ADC is tested with each tone 6dB below fullscale.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component in the spectrum below fs/2.

Transient Response

Transient response is measured by providing a fullscale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Overvoltage Recovery

Overvoltage Recovery is measured by providing a fullscale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Video Definitions

Differential gain and Differential Phase are two commonly found video specifications for characterizing the distortion of a chrominance (3.58MHz) signal as it is offset through the input voltage range of an ADC.

Differential Gain (DG)

Differential Gain is the peak difference in chrominance amplitude (in percent) at two different DC levels.

Differential Phase (DP)

Differential Phase is the peak difference in chrominance phase (in degrees) at two different DC levels.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AD})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

This is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the data on the bus is output at 7th cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 7 cycles.

Power-Up Initialization

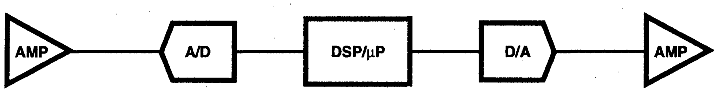
This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize the dynamic circuits within the converter.

HFA1135	HI5702	HSP9501	HI5780	HA5020
HFA1245	HI5705	HSP48410	HI1171	HA2842
		HSP48908	CA3338	HFA1115
		HSP48212		
		HSP43891		
		HSP43168		
		HSP43216		

HFA1135: 350MHz Op Amp with Output Limiting
HFA1245: Dual 350MHz Op Amp with Disable/Enable
HI5702: 10-Bit 40 MSPS A/D Converter
HI5705: Low Cost 10-Bit 40 MSPS A/D Converter
HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48212: Digital Video Mixer
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HI5780: 10-Bit 80MHz Video D/A Converter
HI1171: 8-Bit 40MHz Video D/A Converter
CA3338: 8-Bit 50MHz Video D/A Converter
HFA5020: 100MHz Video Op Amp
HA2842: High Output Current, Video Op Amp
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 16. 10-BIT VIDEO IMAGING COMPONENTS



HFA3600	HI5702	HSP43168	HI5721	HFA1115
HFA3102	HI5703	HSP43216	HI5780	
HFA3101		HSP43891	HI20201	
HFA1100		HSP50016	HI20203	
		HSP50110		
		HSP50210		

HFA3600: Low Noise Amplifier/Mixer
HFA3102: Dual Long-Tailed Pair Transistor Array
HFA3101: Gilbert Cell Transistor Array
HFA1100: 850MHz Op Amp
HI5702: 10-Bit 40 MSPS A/D Converter
HI5703: 10-Bit 40 MSPS A/D Converter
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP50016: Digital Down Converter
HSP50110: Digital Quadrature Tuner
HSP50210: Digital Costas Loop
HI5721: 10-Bit 100MHz Communications D/A Converter
HI5780: 10-Bit 80MHz D/A Converter
HI20201: 10-Bit 160MHz High Speed D/A Converter
HI20203: 8-Bit 160MHz High Speed D/A Converter
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 17. 10-BIT COMMUNICATIONS COMPONENTS

Die Characteristics

DIE DIMENSIONS: 159.4 x 175.2 x 19 ± 1mils

METALLIZATION:
Type: Al Si Cu
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: Sandwich Passivation
Nitride + Undoped Silicon Glass (USG)
Thickness: Nitride 4.2kÅ, USG 8kÅ
Total 12.2kÅ ± 2kÅ

DIE ATTACH: Silver Filled Epoxy

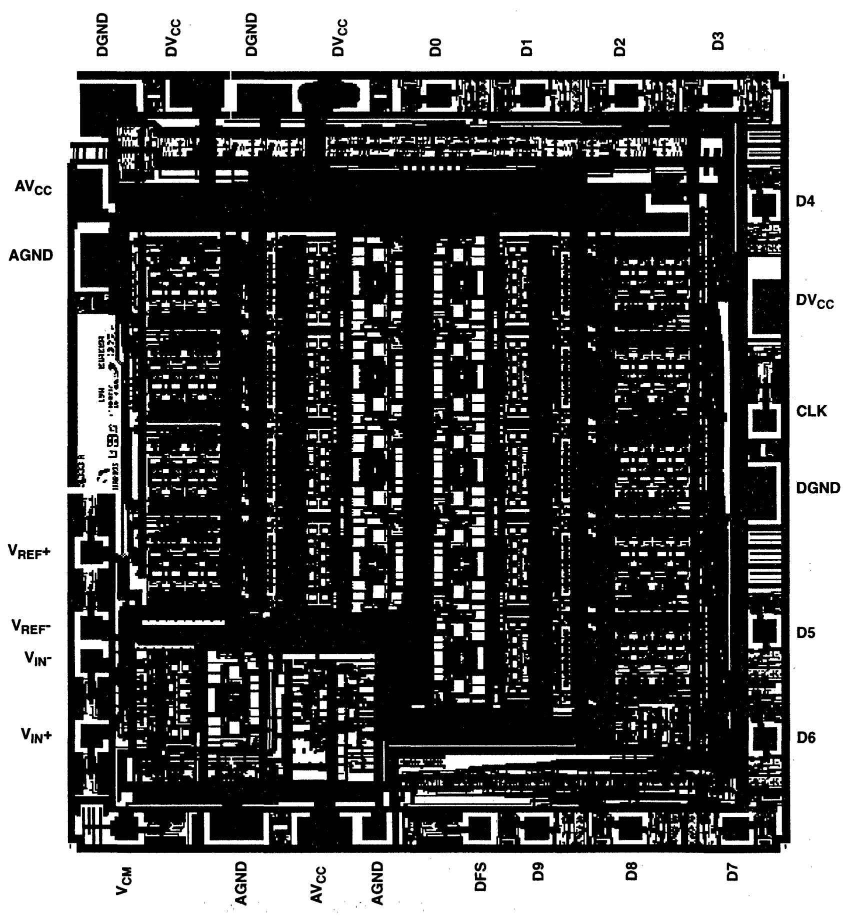
WORST CASE CURRENT DENSITY: 1.6×10^4 A/cm^2

TRANSISTOR COUNT: 4514

SUBSTRATE POTENTIAL (Powered Up): GND (0.0V)

Metallization Mask Layout

HI5702



HARRIS SEMICONDUCTOR

HI5703

July 1995

10-Bit, 40 MSPS A/D Converter

Features

- 40 MSPS Sampling Rate
- 8.3 Bits Guaranteed at f_{IN} = 10MHz
- Low Power
- Wide 250MHz Full Power Input Bandwidth
- On Chip Sample and Hold
- Single-Ended or Differential Input
- 1.25V Input Signal Range
- Single +5V Supply Voltage
- TTL Compatible Interface
- Evaluation Board Available (HI5703EVAL)
- 3.3V Digital Outputs Available

Applications

- Professional Video Digitizing
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition

Description

The HI5703 is a monolithic, 10-bit, analog-to-digital converter fabricated in Harris's HBC10 BiCMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 40 MSPS speed is made possible by a fully differential pipeline architecture with an internal sample and hold.

The HI5703 has excellent dynamic performance while consuming only 400mW power at 40 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles.

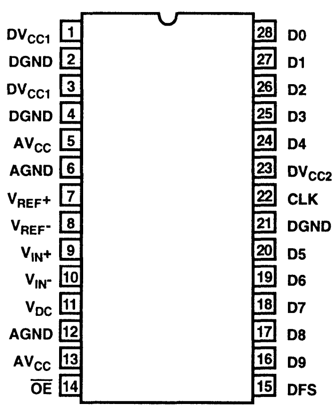
The HI5703 is available in the commercial temperature range and is supplied in a 28 lead wide body SOIC package. It is pin-to-pin compatible with the HI5702.

Ordering Information

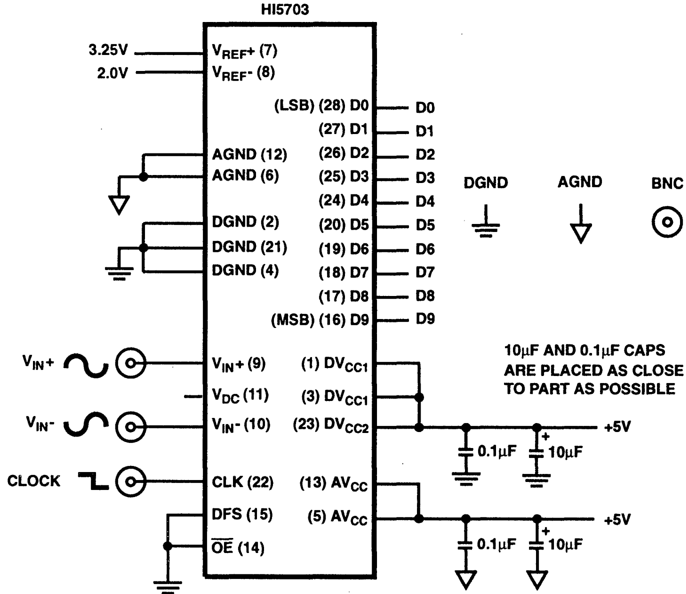
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI5703KCB	0°C to +70°C	28 Lead Plastic SOIC (W)

Pinout

HI5703 (SOIC)
TOP VIEW



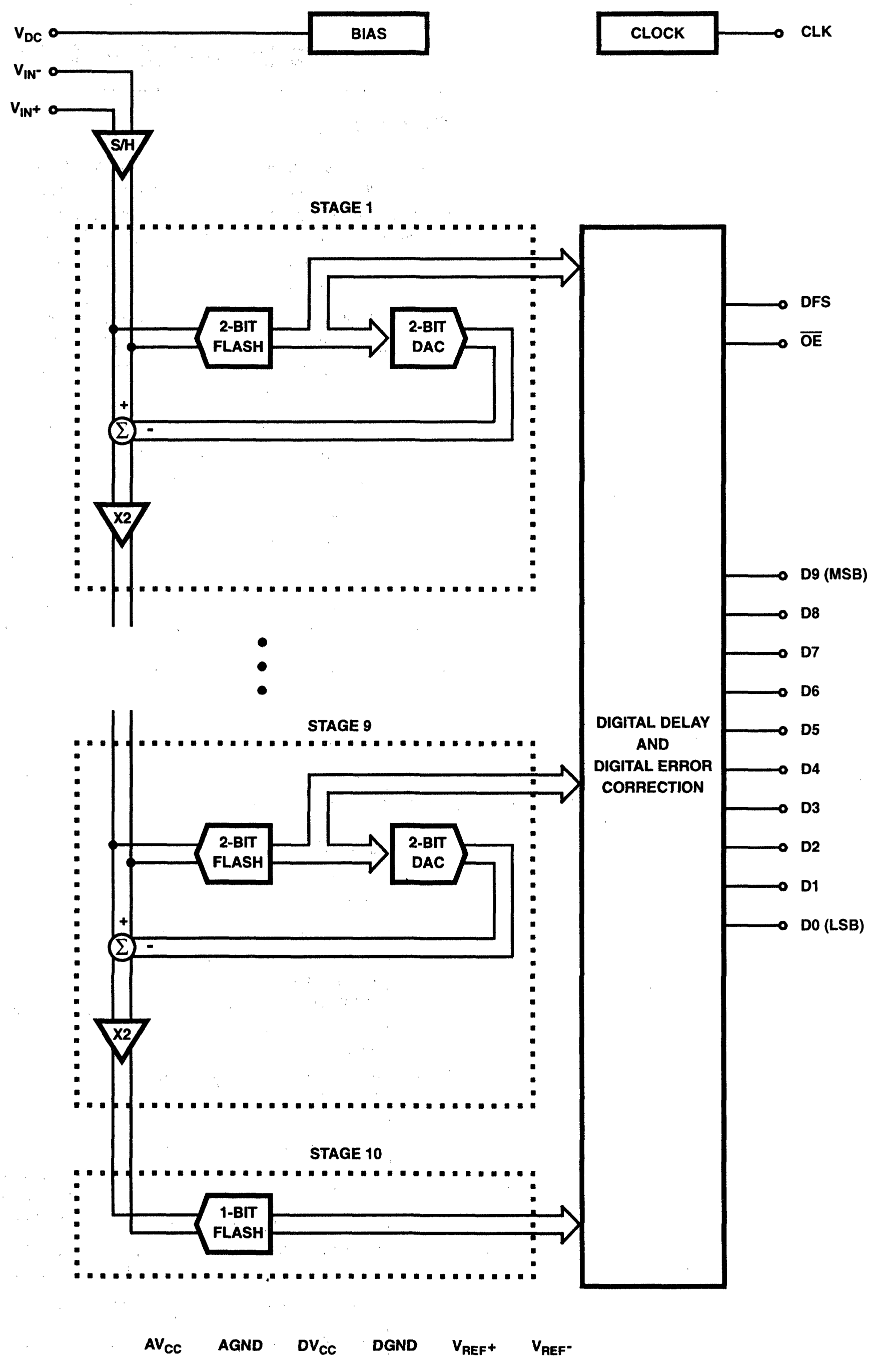
Typical Application Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3950.1

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND . . . . +6V
DGND to AGND 0.3V
Digital I/O Pins . . . . DGND to DV_{CC}
Analog I/O Pins. . . . . AGND to AV_{CC}
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering 10s). . . . . +300°C
(Lead Tips Only)

Thermal Information

Thermal Resistance θ_{JA}
HI5703KCB . . . . 75°C/W
Maximum Junction Temperature. . . . . +150°C
Operating Temperature Range
HI5703KCB . . . . 0°C to +70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2.0V$; F_S = 40 MSPS at 50% Duty Cycle; C_L = 20pF; T_A = +25°C; Unless Otherwise Specified

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		10	-	-	Bits
Integral Linearity Error (INL)	f_{IN} = DC	-	±1	±2.0	LSB
Differential Linearity Error (DNL) (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1	LSB
Offset Error (V_{OS})	f_{IN} = DC	-	4	-	LSB
Full Scale Error (FSE)	f_{IN} = DC	-	1	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	1	MSPS
Maximum Conversion Rate	No Missing Codes	40	-	-	MSPS
Effective Number of Bits (ENOB)	f_{IN} = 1MHz	-	9.2	-	Bits
	f_{IN} = 5MHz	-	9.2	-	Bits
	f_{IN} = 10MHz	8.3	9.0	-	Bits
Signal to Noise Ratio (SNR) $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 1MHz	-	58	-	dB
	f_{IN} = 5MHz	-	58	-	dB
	f_{IN} = 10MHz	51	57	-	dB
Signal to Noise and Distortion Ratio (SINAD) $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 1MHz	-	57	-	dB
	f_{IN} = 5MHz	-	57	-	dB
	f_{IN} = 10MHz	51	56	-	dB
Total Harmonic Distortion (THD)	f_{IN} = 1MHz	-	-64	-	dBc
	f_{IN} = 5MHz	-	-63	-	dBc
	f_{IN} = 10MHz	-	-60	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	-75	-	dBc
	f_{IN} = 5MHz	-	-75	-	dBc
	f_{IN} = 10MHz	-	-73	-	dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	-66	-	dBc
	f_{IN} = 5MHz	-	-64	-	dBc
	f_{IN} = 10MHz	-	-63	-	dBc
Spurious Free Dynamic Range (SFDR)	f_{IN} = 1MHz	-	66	-	dBc
	f_{IN} = 5MHz	-	64	-	dBc
	f_{IN} = 10MHz	54	63	-	dBc
Intermodulation Distortion (IMD)	f1 = 1MHz, f2 = 1.02MHz	-	-59	-	dBc
Differential Gain Error	F_S = 17.72MHz, 6 Step, Mod Ramp	-	0.5	-	%
Differential Phase Error	F_S = 17.72MHz, 6 Step, Mod Ramp	-	0.1	-	Degree
Transient Response		-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive	-	1	-	Cycle

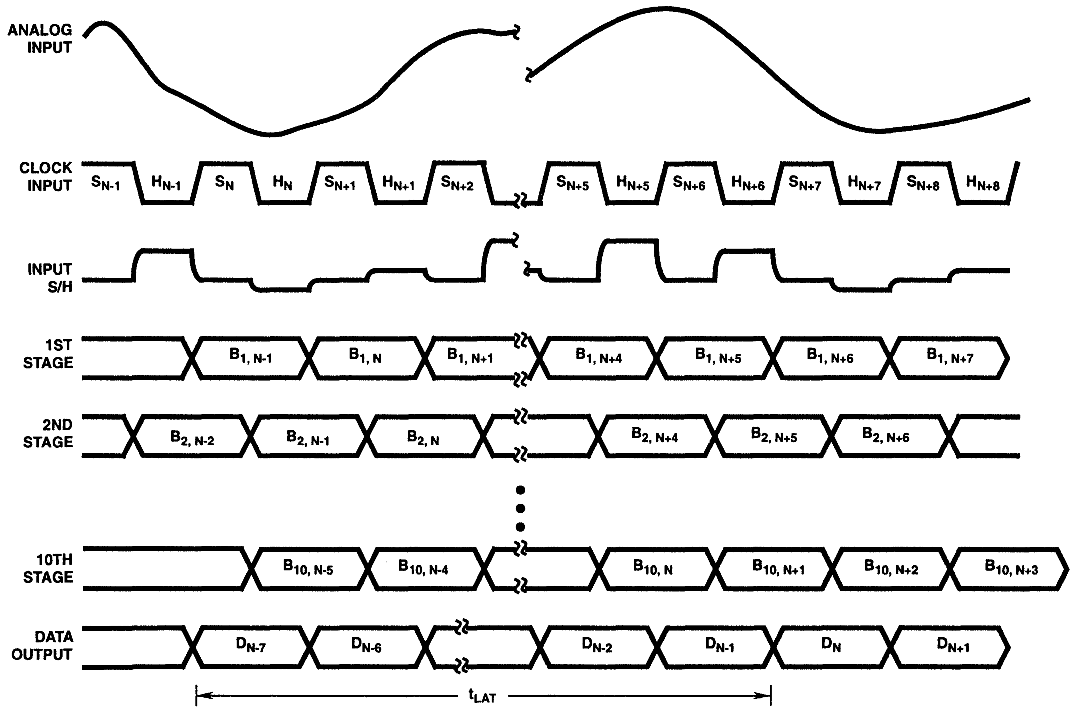
Electrical Specifications $AV_{CC} = DV_{CC1} = DV_{CC2} = +5.0V$; $V_{REF}+ = 3.25V$; $V_{REF}- = 2.0V$; F_S = 40 MSPS at 50% Duty Cycle; C_L = 20pF; $T_A = +25^oC$; Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
ANALOG INPUT					
Analog Input Resistance, R_{IN}	(Note 2)	-	1	-	MΩ
Analog Input Capacitance, C_{IN}		-	7	-	pF
Analog Input Bias Current, I_B	(Note 2)	-50	-	+50	µA
Full Power Input Bandwidth		-	250	-	MHz
Analog Input Common Mode Range ($V_{IN}+ + V_{IN}-$) / 2	Differential Mode (Note 1)	0.625	-	4.375	V
REFERENCE INPUT					
Total Reference Resistance, R_L		300	400	500	Ω
Reference Current		2.5	3.125	4.2	mA
Positive Reference Input, $V_{REF}+$	(Note 1)	-	3.25	3.3	V
Negative Reference Input, $V_{REF}-$	(Note 1)	1.95	2.0	-	V
Reference Common Mode Voltage ($V_{REF}+ + V_{REF}-$) / 2	(Note 1)	2.575	2.625	2.675	V
COMMOM MODE VOLTAGE					
Common Mode Voltage Output, V_{CM}		-	2.8	-	V
Max Output Current		-	-	1	mA
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Current, I_{IH}	V_{IH} = 5V	-	-	10.0	µA
Input Logic Low Current, I_{IL}	V_{IL} = 0V	-	-	10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS					
Output Logic Sink Current, I_{OL}	V_O = 0.4V; DV_{CC2} = 5V	1.6	-	-	mA
Output Logic Source Current, I_{OH}	V_O = 2.4V; DV_{CC2} = 5V	-0.2	-	-	mA
Output Three-State Leakage Current, I_{OZ}	V_O = 0/5V; DV_{CC2} = 5V	-	±1	±10	µA
Output Logic Sink Current, I_{OL}	V_O = 0.4V; DV_{CC2} = 3.3V	1.6	-	-	mA
Output Logic Source Current, I_{OH}	V_O = 2.4V; DV_{CC2} = 3.3V	-0.2	-	-	mA
Output Three-State Leakage Current, I_{OZ}	V_O = 0/5V; DV_{CC2} = 3.3V	-	±1	±10	µA
Output Capacitance, C_{OUT}		-	5	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps
Data Output Delay, t_{OD}		-	7	-	ns
Data Output Hold, t_H		-	4	-	ns
Data Output Enable Time, t_{EN}		-	7	-	ns
Data Output Enable Time, t_{DIS}		-	7	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 1)	-	-	7	Cycles
Power-Up Initialization	Data Invalid Time (Note 1)	-	-	20	Cycles
POWER SUPPLY CHARACTERISTICS					
Supply Current, I_{CC}	$V_{IN}+ - V_{IN}-$ = 1.25V and DFS = "0"	-	80	-	mA
Power Dissipation	$V_{IN}+ - V_{IN}-$ = 1.25V and DFS = "0"	-	400	-	mW
Offset Error Sensitivity, ΔV_{OS}	AV_{CC} or DV_{CC} = 5V ± 5%	-	±1.5	-	LSB
Gain Error Sensitivity, ΔFSE	AV_{CC} or DV_{CC} = 5V ± 5%	-	±0.2	-	LSB

NOTES:

1. Parameter guaranteed by design or characterization and not production tested.
2. With the clock low and DC input.

Timing Waveforms



NOTES:

1. S_N: N-th sampling period.
2. H_N: N-th holding period.
3. $B_{M, N}$: M-th stage digital output corresponding to N-th sampled input.
4. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5703 INTERNAL CIRCUIT TIMING

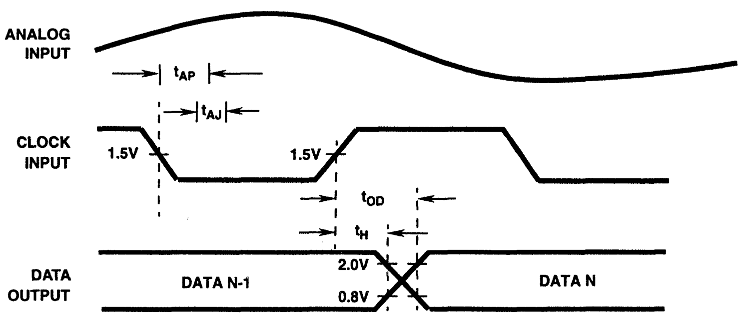


FIGURE 2. INPUT-TO-OUTPUT TIMING

TABLE 1. PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	DV_{CC1}	Digital Supply
2	DGND	Digital Ground
3	DV_{CC1}	Digital Supply
4	DGND	Digital Ground
5	AV_{CC}	Analog Supply
6	AGND	Analog Ground
7	$V_{REF}+$	Positive Reference
8	$V_{REF}-$	Negative Reference
9	$V_{IN}+$	Positive Analog Input
10	$V_{IN}-$	Negative Analog Input
11	V_{CM}	Input Common Mode Voltage
12	AGND	Analog Ground
13	AV_{CC}	Analog Supply
14	$\overline{OE}$	Output Enable
15	DFS	Data Format Select
16	D9	Data Bit 9 Output (MSB)
17	D8	Data Bit 8 Output
18	D7	Data Bit 7 Output
19	D6	Data Bit 6 Output
20	D5	Data Bit 5 Output
21	DGND	Digital Ground
22	CLK	Input Clock
23	DV_{CC2}	Digital Output Supply (+5V or +3.3V)
24	D4	Data Bit 4 Output
25	D3	Data Bit 3 Output
26	D2	Data Bit 2 Output
27	D1	Data Bit 1 Output
28	D0	Data Bit 0 Output (LSB)

Detailed Description

Theory of Operation

The HI5703 is a 10-bit fully differential sampling pipeline A/D converter with digital error correction. Figure 3 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, Φ_1 and Φ_2, derived from the master clock. During the sampling phase, Φ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of Φ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, Φ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The small values of these components result in a typical full power input bandwidth of 250MHz.

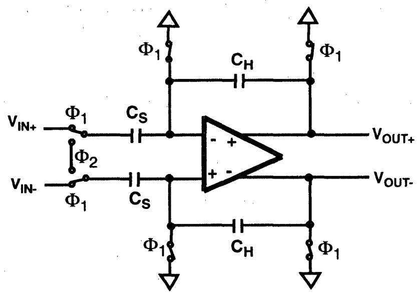


FIGURE 3. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figure 1, nine identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the tenth stage being only a one bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual sub-converter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The two-bit digital output of each stage is fed to a digital delay line controlled by the internal clock. The purpose of the delay line is to align the digital output data to the corresponding sampled analog input signal. This delayed data is fed to the digital error correction circuit which corrects the error in the output data with the information contained in the redundant bits to form the final ten bit output for the converter.

Because of the pipeline nature of this converter, the data on the bus is output at the 7th cycle of the clock after the analog sample is taken. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The output data is synchronized to the external clock by a double buffered latching technique.

The digital output bits are available in offset binary or two's complement format, set by the Data Format Select (DFS) input.

Reference Input, $V_{REF}-$ $V_{REF}+$

The HI5703 requires two reference voltages connected to the V_{REF} pins. The HI5703 is tested with $V_{REF}-$ equal to 2V and $V_{REF}+$ equal to 3.25V for a fully differential input range of ±1.25V. $V_{REF}+$ and $V_{REF}-$ can differ from the above voltages as long as the common mode voltage between the reference pins $((V_{REF}+ + V_{REF}-)/2)$ does not exceed 2.625V ±50mV and the limits on $V_{REF}+$ and $V_{REF}-$ are not exceeded.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference input pins, $V_{REF}+$ and $V_{REF}-$.

Analog Input, Differential Connection

The analog input to the HI5703 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figures 4 and 5) will give the best performance for the converter.

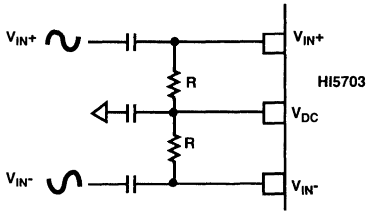


FIGURE 4. AC COUPLED DIFFERENTIAL INPUT

Since the HI5703 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V. For the differential input connection this implies the analog input common mode voltage can range from 0.625V to 4.375V. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

A DC voltage source, V_{DC}, equal to 2.8V (typical), is made available to the user to help simplify circuit design when using an AC coupled differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent bias source and stays within the analog input common mode range over temperature. It has a temperature coefficient of approximately 200ppm/°C.

For the AC coupled differential input (Figure 4) assume the difference between $V_{REF}+$, typically 3.25V, and $V_{REF}-$, typically 2V, is 1.25V. Fullscale is achieved when $V_{IN}+$ and $V_{IN}-$ inputs are $1.25V_{P-P}$, with $V_{IN}-$ being 180 degrees out of phase with $V_{IN}+$. The converter will be at positive fullscale when the $V_{IN}+$ input is at V_{DC} + 0.625V and $V_{IN}-$ is at V_{DC} - 0.625V ($V_{IN}+$ - $V_{IN}-$ = 1.25V). Conversely, the converter will be at negative fullscale when the $V_{IN}+$ input is equal to V_{DC} - 0.625V and $V_{IN}-$ is at V_{DC} + 0.625V ($V_{IN}+$ - $V_{IN}-$ = -1.25V).

The analog input can be DC coupled (Figure 5) as long as the inputs are within the analog input common mode voltage range.

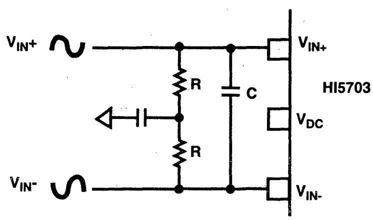


FIGURE 5. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 5 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well.

Analog Input, Single-Ended Connection

The configuration shown in Figure 6 may be used with a single ended AC coupled input.

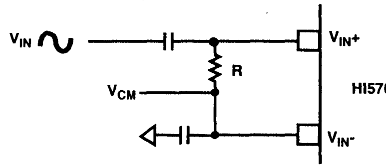


FIGURE 6. AC COUPLED SINGLE ENDED INPUT

Again, assume the difference between $V_{REF}+$, typically 3.25V, and $V_{REF}-$, typically 2V, is 1.25V. If V_{IN} is a 2.5 V_{P-P} sinewave, then $V_{IN}+$ is a $2.5V_{P-P}$ sinewave riding on a positive voltage equal to V_{CM}. The converter will be at positive fullscale when $V_{IN}+$ is at V_{CM} + 1.25V and will be at negative fullscale when $V_{IN}+$ is equal to V_{CM} - 1.25V. Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND. In this case, V_{CM} could range between 1.25V and 3.75V without a significant change in ADC performance. The simplest way to produce V_{CM} is to use the V_{DC} output of the HI5703.

The single ended analog input can be DC coupled (Figure 7) as long as the input is within the analog input common mode voltage range.

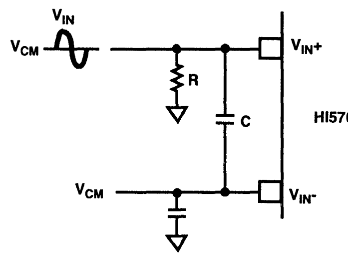


FIGURE 7. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 7 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well.

A single ended source may give better overall system performance if it is first converted to differential before driving the HI5703. Refer to the application note AN9413, "Driving the Analog Input of the HI5702". This application note applies to the HI5703 as well as the HI5702 and describes several different ways of driving the analog differential inputs.

Digital Output Control and Clock Requirements

The HI5703 provides a standard high-speed interface to external TTL logic families.

In order to ensure rated performance of the HI5703, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5703 will only be guaranteed at conversion rates above 1 MSPS. This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1 MSPS will have to be performed before valid data is available.

A Data Format Select (DFS) pin is provided which will determine the format of the digital data. When at logic low, the data will be output in offset binary format. When at logic high, the data will be output in two's complement format. Refer to Table 2 for further information.

The output enable pin, $\overline{OE}$, when pulled high will three-state the digital outputs to a high impedance state. Set the $\overline{OE}$ input to logic low for normal operation.

$\overline{OE}$ INPUT	DIGITAL OUTPUTS
0	Active
1	High Impedance

Supply and Ground Considerations

The HI5703 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The digital data outputs also have a separate supply pin, DV_{CC2}, which can be powered from a 3.3V to 5.0V supply. This allows the outputs to interface with 3.3V logic if so desired.

The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5703 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the application notes "Using Harris High Speed A/D Converters" (AN9214) for additional considerations when using high speed converters.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level 1/4 LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for a analog input that is 3/4 LSB's below positive full-scale (+FS) with the offset error removed. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Sensitivity

Each of the power supplies are moved plus and minus 5% and the shift in the offset and gain error (in LSB's) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5703. A low distortion sine wave is applied to the input, it is coherently sampled, and the

TABLE 2. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE ($V_{IN}+ - V_{IN}-$)	OFFSET BINARY OUTPUT CODE (DFS LOW)										TWO'S COMPLEMENT OUTPUT CODE (DFS HIGH)									
		MSB									LSB	MSB									LSB
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) 1/4 LSB	1.24939V	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
+FS - 1 1/4 LSB	1.24695V	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
+3/4 LSB	1.83mV	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-1/4 LSB	-0.610mV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-FS + 1 3/4 LSB	-1.24573V	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + 3/4 LSB	-1.24817V	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

NOTE:

1. The voltages listed above represent the ideal center of each output code shown as a function of the reference voltage.
2. $V_{REF}+ = 3.25V$ and $V_{REF}- = 2.0V$.

output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full-scale for all these tests.

SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by

$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$

where: $V_{CORR} = 0.5$ dB

V_{CORR} adjusts the ENOB for the amount the input is below fullscale.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present on the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are (f_1+f_2), (f_1-f_2), $(2f_1)$, $(2f_2)$, $(2f_1+f_2)$, $(2f_1-f_2)$, (f_1+2f_2), (f_1-2f_2). The ADC is tested with each tone 6dB below fullscale.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component in the spectrum below fs/2.

Transient Response

Transient response is measured by providing a fullscale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Over-Voltage Recovery

Over-Voltage Recovery is measured by providing a fullscale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Video Definitions

Differential Gain and Differential Phase are two commonly found video specifications for characterizing the distortion of a chrominance signal as it is offset through the input voltage range of an ADC.

Differential Gain (DG)

Differential Gain is the peak difference in chrominance amplitude (in percent) relative to the reference burst.

Differential Phase (DP)

Differential Phase is the peak difference in chrominance phase (in degrees) relative to the reference burst.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AD})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

This is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

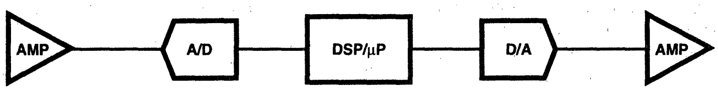
Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the data on the bus is output at 7th cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 7 cycles.

Power-Up initialization

This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize the dynamic circuits within the converter.



HFA1135	HI5702	HSP9501	HI5780	HA5020
HFA1245	HI5705	HSP48410	HI1171	HA2842
		HSP48908	CA3338	HFA1115
		HSP48212		
		HSP43891		
		HSP43168		
		HSP43216		

HFA1135: 350MHz Op Amp with Output Limiting
HFA1245: Dual 350MHz Op Amp with Disable/Enable
HI5702: 10-Bit 40 MSPS A/D Converter
HI5705: Low Cost 10-Bit 40 MSPS A/D Converter
HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48212: Digital Video Mixer
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HI5780: 10-Bit 80MHz Video D/A Converter
HI1171: 8-Bit 40MHz Video D/A Converter
CA3338: 8-Bit 50MHz Video D/A Converter
HFA5020: 100MHz Video Op Amp
HA2842: High Output Current, Video Op Amp
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 16. 10-BIT VIDEO IMAGING COMPONENTS

HFA3600	HI5702	HSP43168	HI5721	HFA1115
HFA3102	HI5703	HSP43216	HI5780	
HFA3101		HSP43891	HI20201	
HFA1100		HSP50016	HI20203	
		HSP50110		
		HSP50210		

HFA3600: Low Noise Amplifier/Mixer
HFA3102: Dual Long-Tailed Pair Transistor Array
HFA3101: Gilbert Cell Transistor Array
HFA1100: 850MHz Op Amp
HI5702: 10-Bit 40 MSPS A/D Converter
HI5703: 10-Bit 40 MSPS A/D Converter
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP50016: Digital Down Converter
HSP50110: Digital Quadrature Tuner
HSP50210: Digital Costas Loop
HI5721: 10-Bit 100MHz Communications D/A Converter
HI5780: 10-Bit 80MHz D/A Converter
HI20201: 10-Bit 160MHz High Speed D/A Converter
HI20203: 8-Bit 160MHz High Speed D/A Converter
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 17. 10-BIT COMMUNICATIONS COMPONENTS

HI5705

PRELIMINARY

May 1995

Low Cost 10-Bit, 40 MSPS A/D Converter

Features

- 10-Bit Resolution
- 40 MSPS Sampling Rate
- Low Power: 400mW
- On-Chip Sample and Hold
- Single-Ended Analog Input
- Single +5V Supply Voltage
- 3.0V Digital Outputs Available
- TTL Compatible Interface
- Evaluation Board Available

Applications

- Professional Video Digitizing
- QAM Demodulation
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition
- Instrumentation

Description

The HI5705 is a monolithic, 10-bit, analog-to-digital converter fabricated in Harris's HBC10 BiCMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 40 MSPS speed is made possible by a fully differential pipeline architecture with an internal sample and hold.

The HI5705 has excellent dynamic performance while consuming only 400mW power at 40 MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles.

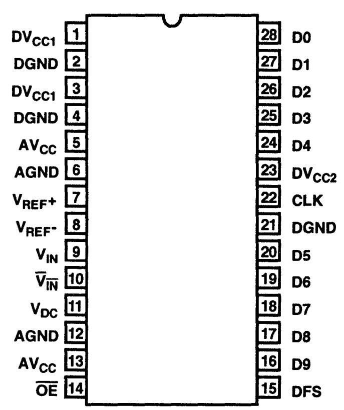
The HI5705 is available in the commercial temperature range and is supplied in a 28 lead wide body SOIC package. For increased performance, the HI5703 is available.

Ordering Information

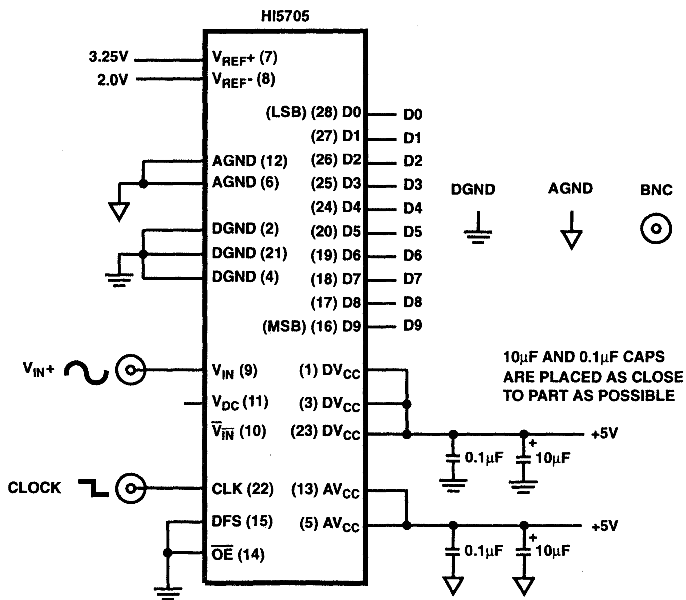
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI5705KCB	0^oC to $+70^oC$	28 Lead Plastic SOIC (W)

4 A/D CONVERTERS

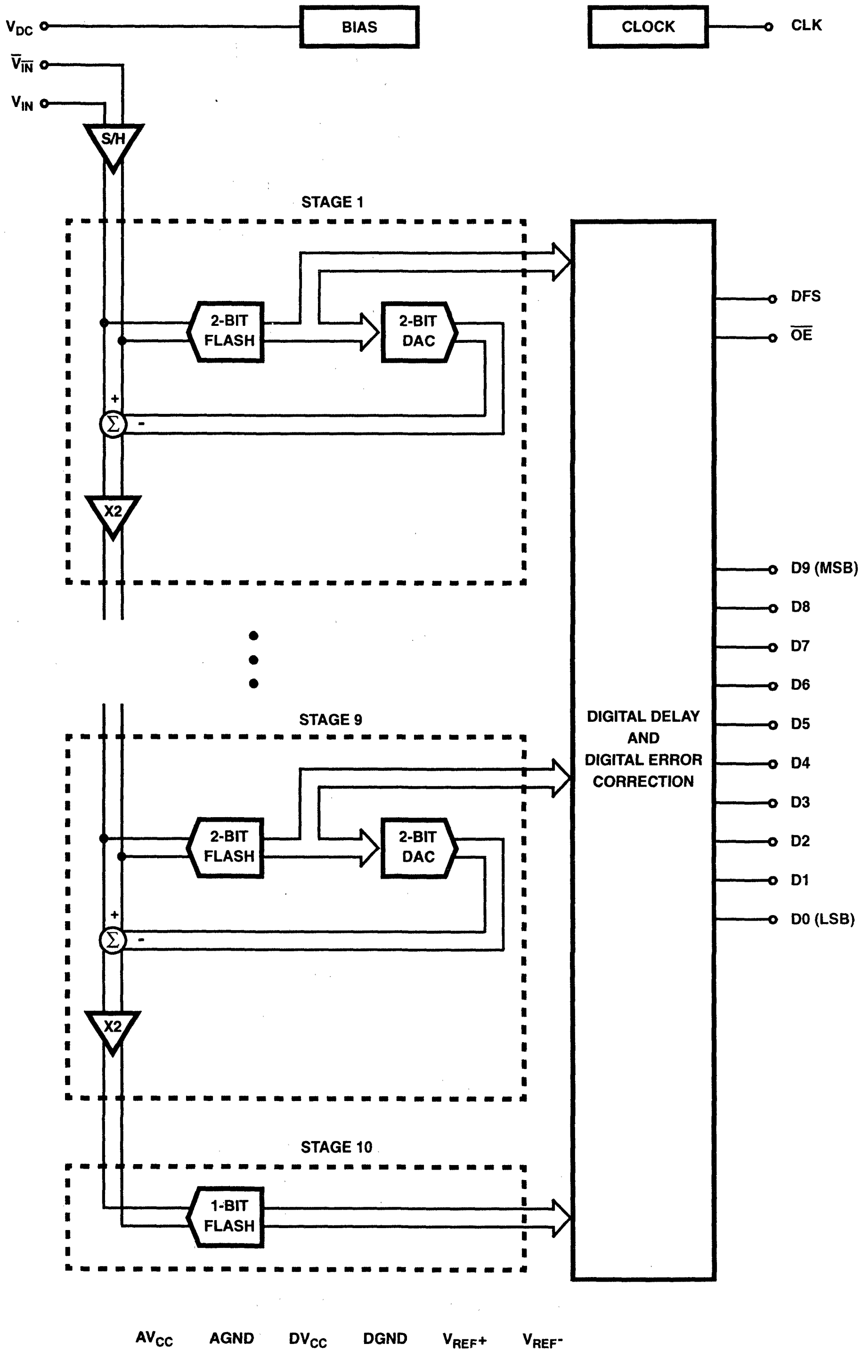
Pinout



Typical Application Schematic



Functional Block Diagram



HI5710

February 1995

10-Bit, 20 MSPS A/D Converter

Features

- Resolution 10-Bit ±0.5 LSB (DNL)
- Maximum Sampling Frequency 20 MSPS
- Low Power Consumption 140mW (Reference Current Excluded)
- Standby Mode Power 5mW
- No Sample and Hold Required
- TTL/CMOS Compatible I/O
- Three-State Outputs
- Single +5V Analog Power Supply
- Single +3.3V or +5V Digital Power Supply
- Evaluation Board Available: HI5710EVAL

Applications

- Video Digitizing - Multimedia
- Data Communications
- Image Scanners
- Medical Imaging
- Video Recording Equipment
- Camcorders
- QAM Demodulation

Description

The HI5710 is a low power, 10-bit, CMOS analog-to-digital converter. The use of a 2-step architecture realizes low power consumption, 140mW, and a maximum conversion speed of 20MHz with only a 3 clock cycle data latency. The HI5710 can be powered down, disabling the chip and the digital outputs, reducing power to less than 5mW. A built-in, user controlled, calibration circuit is used to provide low linearity error, 1 LSB. The low power, high speed and small package outline make the HI5710 an ideal choice for CCD, battery, and high channel count applications.

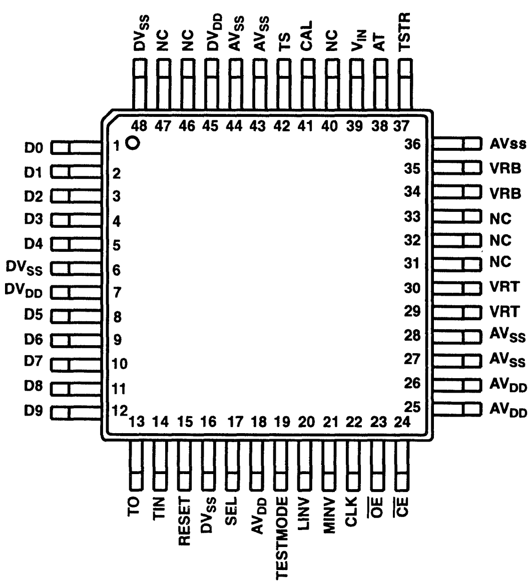
The HI5710 does not require an external sample and hold but requires an external reference and includes force and sense reference pins for increased accuracy. The digital outputs can be inverted, with the MSB controlled separately, allowing for various digital output formats. The HI5710 includes a test mode where the digital outputs can be set to a fixed state to ease in-circuit testing.

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HI5710JCQ	0^oC to $+75^oC$	48 Lead Plastic Metric Quad Flatpack

Pinout

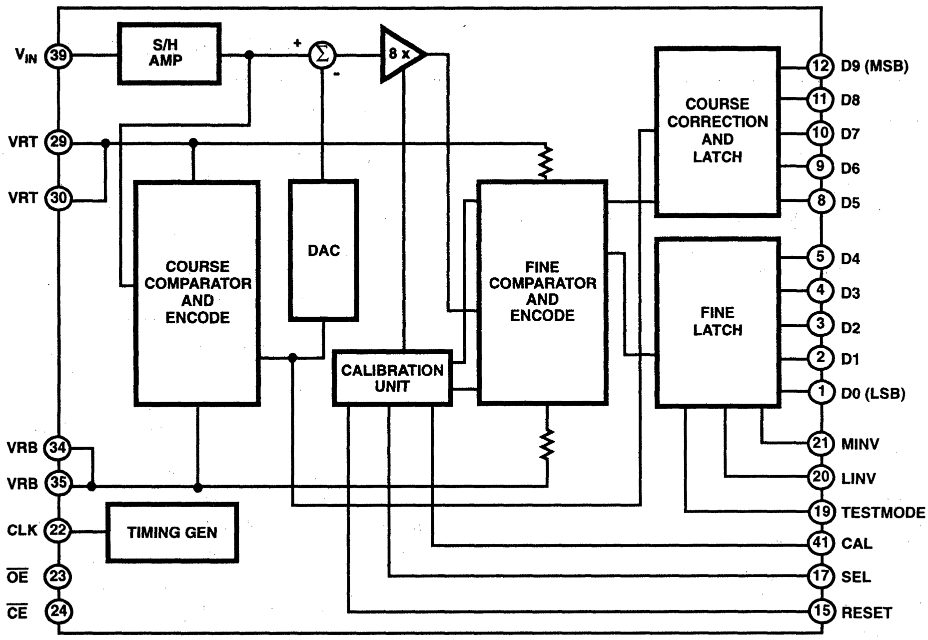
HI5710 (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3921.2**

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{DD} 7V
Reference Voltage, V_{RT}, V_{RB} . . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Analog Input Voltage, V_{IN} . . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Digital Input Voltage, V_{IH}, V_{IL} . . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Digital Output Voltage, V_{OH}, V_{OL} . . . . . . V_{DD} + 0.5V to V_{SS} - 0.5V
Storage Temperature, T_{STG} . . . . . . -55°C to +150°C
Lead Temperature (Soldering 10s) . . . . . . +300°C
(Lead Tips Only)

Thermal Information

Thermal Resistance θ_{JA}
HI5710JCQ . . . . . . 111°C/W
Operating Temperature, T_A . . . . . . 0°C to +75°C
Maximum Junction Temperature . . . . . . +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions (Note 1)

Supply Voltage
AV_{DD}, AV_{SS} . . . . . . +5V ± 0.25V
DV_{DD}, DV_{SS} . . . . . . +3.3V ± 0.25V
IDGND-AGNDI . . . . . . 0mV to 100mV
Reference Input Voltage
V_{RB} . . . . . . 1.8V to 2.8V
V_{RT} . . . . . . 3.6V to 4.6V

Analog Input Range, V_{IN} . . . . . . (V_{RT} - V_{RB}) (1.8V_{P-P} to 2.8V_{P-P})
Clock Pulse Width
T_{PW1} . . . . . . 25ns (Min)
T_{PW0} . . . . . . 25ns (Min)

Electrical Specifications F_C = 20 MSPS, AV_{DD} = +5V, DV_{DD} = +3.3V, V_{RB} = 2.0V, V_{RT} = 4.0V, T_A = +25°C (Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE						
Offset Voltage	E_{OT}		47	67	87	mV
	E_{OB}		-68	-48	-28	mV
Integral Non-Linearity, INL		V_{IN} = 2.0V to 4.0V	-	±1.3	±2.0	LSB
Differential Non-Linearity, DNL			-	±0.5	±1.0	LSB
DYNAMIC CHARACTERISTICS						
Maximum Conversion Speed, F_C		F_{IN} = 1kHz Ramp	20	-	-	MSPS
Minimum Conversion Speed, F_C			-	-	0.5	MSPS
Effective Number of Bits, ENOB		F_{IN} = 3MHz	-	8.7	-	Bits
Signal to Noise and Distortion, SINAD		F_{IN} = 100kHz	-	53	-	dB
		F_{IN} = 500kHz	-	52	-	dB
		F_{IN} = 1MHz	-	53	-	dB
		F_{IN} = 3MHz	-	54	-	dB
		F_{IN} = 7MHz	-	47	-	dB
		F_{IN} = 10MHz	-	45	-	dB
Spurious Free Dynamic Range, SFDR		F_{IN} = 100kHz	-	60	-	dB
		F_{IN} = 500kHz	-	59	-	dB
		F_{IN} = 1MHz	-	60	-	dB
		F_{IN} = 3MHz	-	65	-	dB
		F_{IN} = 7MHz	-	50	-	dB
		F_{IN} = 10MHz	-	49	-	dB
Differential Gain Error, DG		NTSC 40 IRE Mod Ramp, F_C = 14.3 MSPS	-	1.0	-	%
Differential Phase Error, DP			-	0.3	-	Degree

Electrical Specifications F_C = 20 MSPS, AV_{DD} = +5V, DV_{DD} = +3.3V, V_{RB} = 2.0V, V_{RT} = 4.0V, T_A = +25°C (Note 1) **(Continued)**

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG INPUTS							
Analog Input Bandwidth (-3dB), BW				-	100	-	MHz
Analog Input Current		V_{IN} = 4V		-	-	50	µA
		V_{IN} = 2V		-50	-	-	µA
Analog Input Capacitance, C_{IN}		V_{IN} = 2.5V + 0.07V_{RMS}		-	9	-	pF
REFERENCE INPUT							
Reference Pin Current, I_{RT}		RESET = Low		7.2	8.2	9.2	mA
Reference Pin Current, I_{RB}		RESET = Low		4.2	5.2	6.2	mA
Reference Resistance (V_{RT} to V_{RB}), R_{REF}				210	300	390	Ω
DIGITAL INPUTS							
Digital Input Voltage	V_{IH1}	AV_{DD} = 4.75V to 5.25V, $\overline{OE}$ Excluded		2.3	-	-	V
	V_{IL1}			-	-	0.80	V
Digital Input Voltage	V_{IH2}	$\overline{OE}$ Only		0.7 x DV_{DD}	-	-	V
	V_{IL2}			-	-	0.3 x DV_{DD}	V
Digital Input Current	I_{IH}	DV_{DD} = Max	V_{IH} = DV_{DD}	-	-	5	µA
	I_{IL}		V_{IL} = 0V	-	-	5	µA
DIGITAL OUTPUTS							
Digital Output Current	I_{OH}	$\overline{OE}$ = DV_{SS}, DV_{DD} = Min	V_{OH} = DV_{DD} -0.5V	4.0	-	-	mA
	I_{OL}		V_{OL} = 0.4V	3.5	-	-	mA
Digital Output Leakage Current	I_{OZH}	$\overline{OE}$ = DV_{DD}, DV_{DD} = Max	V_{OH} = DV_{DD}	-	-	1	µA
	I_{OZL}		V_{OL} = 0V	-	-	1	µA
TIMING CHARACTERISTICS							
Output Data Delay, T_{DL}		Load is One TTL Gate		8	13	18	ns
Output Enable/Disable Delay	t_{PZL}			10	15	20	ns
	t_{PLZ}			20	25	30	ns
	t_{PZH}			10	15	20	ns
	t_{PHZ}			20	25	30	ns
Sampling Delay, t_{SD}				-	4	6	ns
POWER SUPPLY CHARACTERISTIC							
Analog Supply Current, IA_{DD}		F_{IN} = 1kHz Ramp Wave Input		23	26	29	mA
Digital Supply Current, ID_{DD}				1.6	1.7	1.8	mA
Analog Standby Current		$\overline{CE}$ = High		-	-	1.0	mA
Digital Standby Current				-	-	1.0	µA

NOTE:

1. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagrams

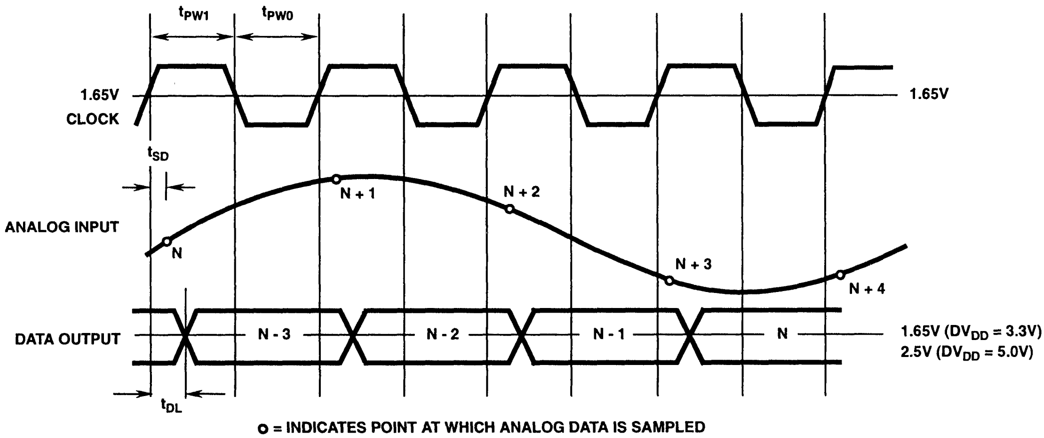


FIGURE 1.

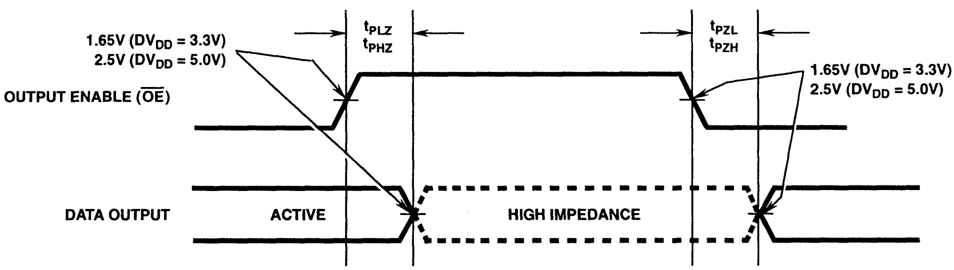


FIGURE 2.

Calibration Timing Diagrams

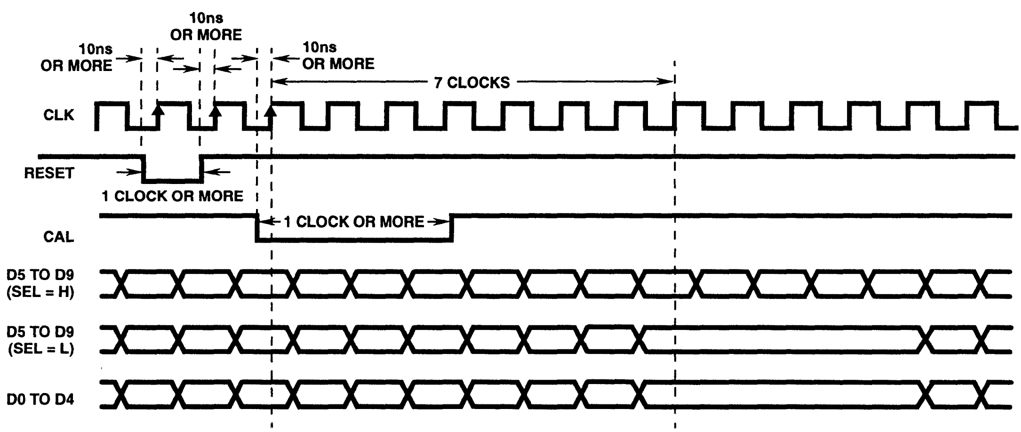


FIGURE 3.

Calibration Timing Diagrams (Continued)

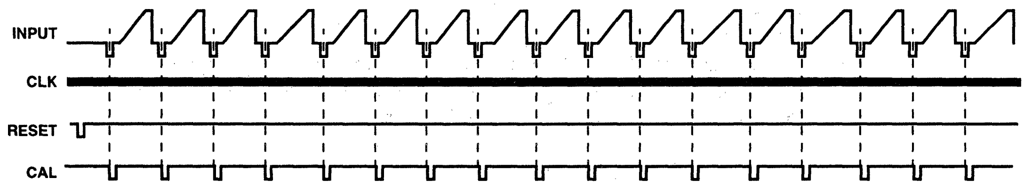


FIGURE 4A. CALIBRATION DURING H SYNC

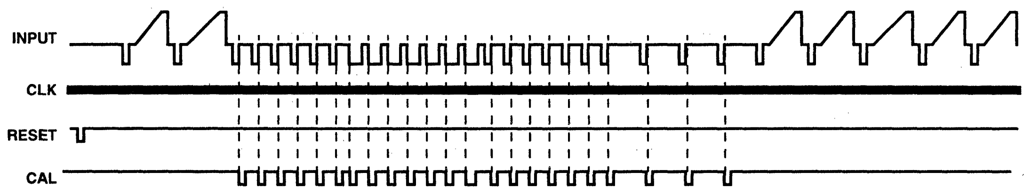


FIGURE 4B. CALIBRATION DURING V SYNC

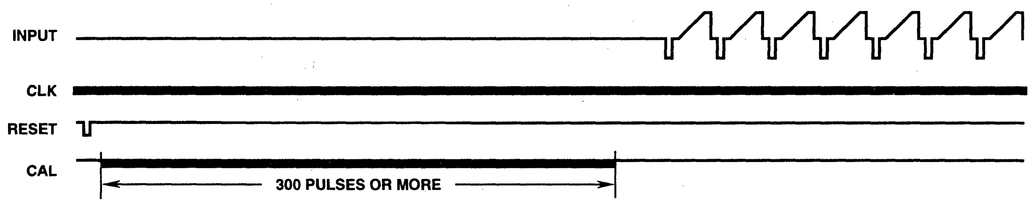


FIGURE 4C. CALIBRATION UPON POWER ON

FIGURE 4. VARIOUS CALIBRATION TIMINGS

Typical Performance Curves

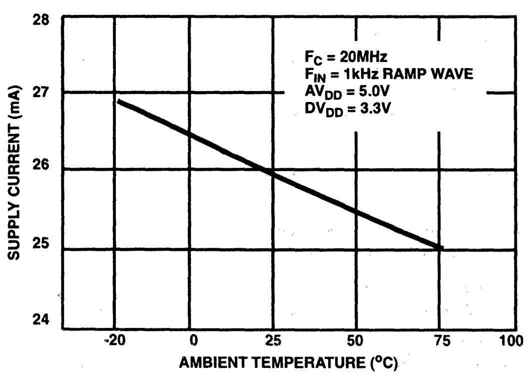


FIGURE 5. SUPPLY CURRENT vs AMBIENT TEMPERATURE

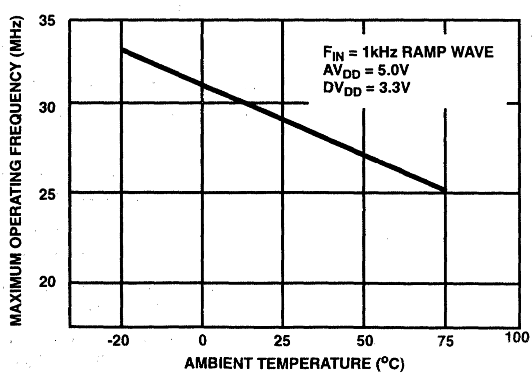


FIGURE 6. MAXIMUM OPERATING FREQUENCY vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

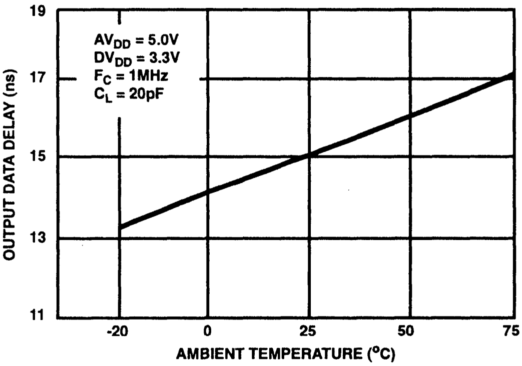


FIGURE 7. OUTPUT DATA DELAY vs AMBIENT TEMPERATURE

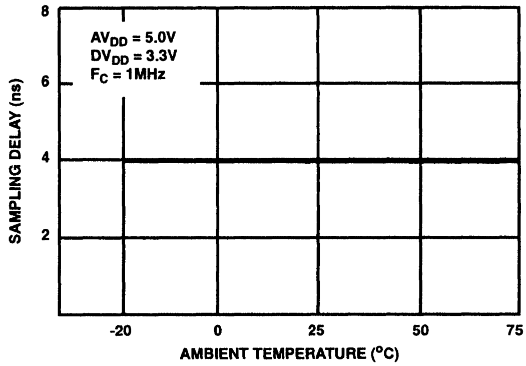


FIGURE 8. SAMPLING DELAY vs AMBIENT TEMPERATURE

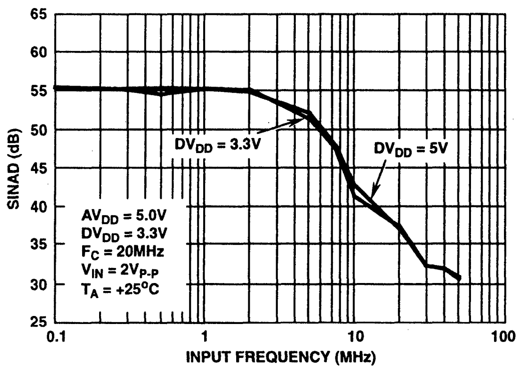


FIGURE 9. SINAD vs INPUT FREQUENCY

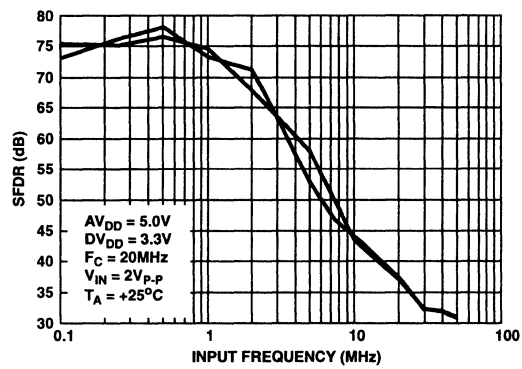


FIGURE 10. SFDR vs INPUT FREQUENCY

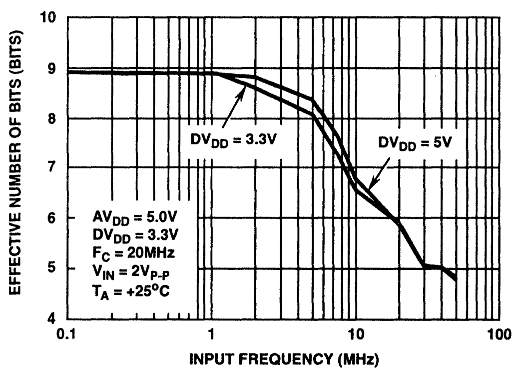


FIGURE 11. EFFECTIVE BITS vs INPUT FREQUENCY

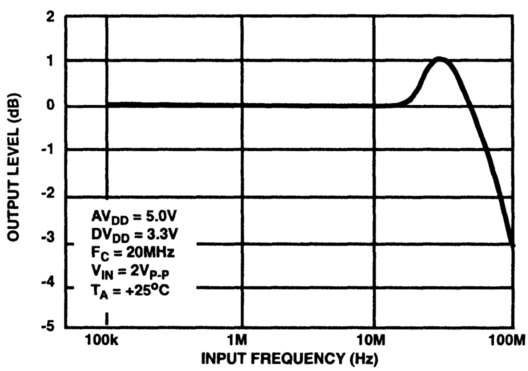


FIGURE 12. INPUT BANDWIDTH

Typical Performance Curves (Continued)

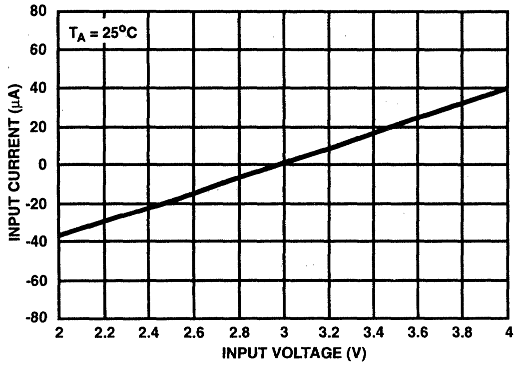


FIGURE 13. ANALOG INPUT CURRENT vs INPUT VOLTAGE

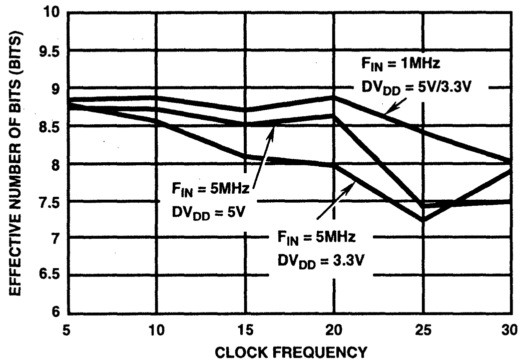


FIGURE 14. ENOB vs CLOCK FREQUENCY

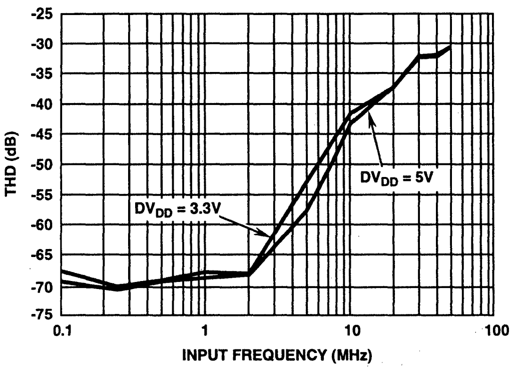


FIGURE 15. THD vs INPUT FREQUENCY

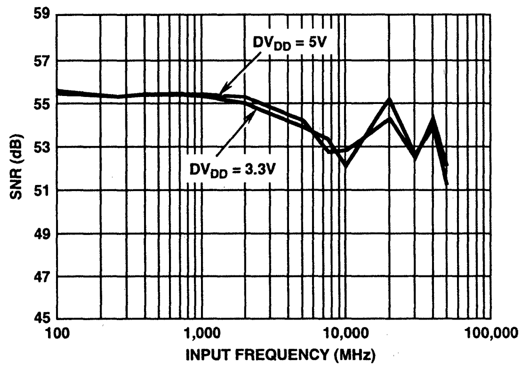
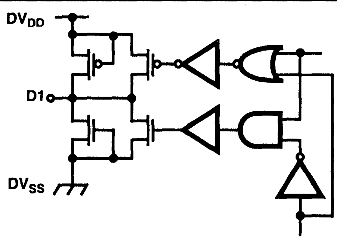
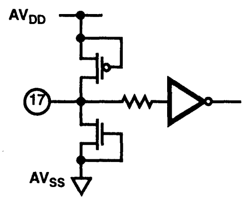
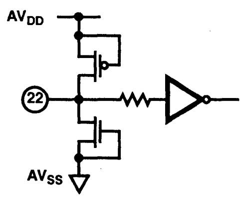
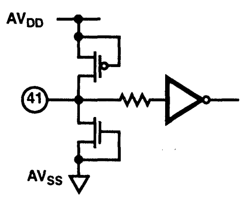
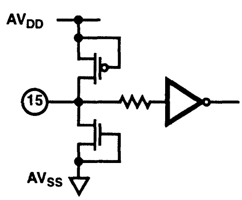
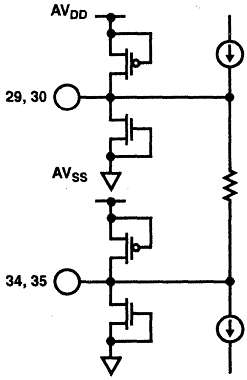
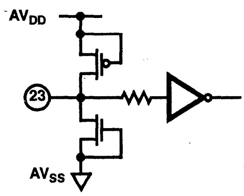
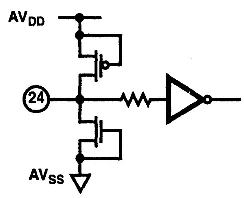
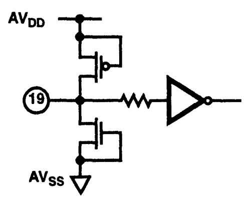


FIGURE 16. SNR vs INPUT FREQUENCY

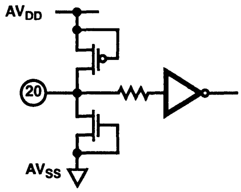
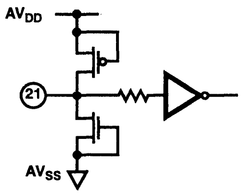
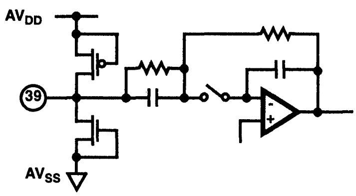
Pin Description and I/O Pin Equivalent Circuit

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 5, 8 to 12	D0 to D9		Digital Outputs: D0 (LSB) to D9 (MSB).
13	TO		Test Pin, Leave Pin Open
7, 45	DV_{DD}		Digital V_{DD}
6, 16, 48	DV_{SS}		Digital V_{SS}
27, 28, 36, 43, 44	AV_{SS}		Analog V_{SS}
17	SEL		D5 to D9 Output Data Select for Calibration (4 CLK) High: Through Output Low: Data Fixed as With D0 to D4
22	CLK		Clock Pin
41	CAL		Calibration Pulse Input, Calibration Starts On a Falling Edge, Normally High
15	RESET		Calibration Circuit Reset, Resets With a Negative Pulse, Normally High

Pin Description and I/O Pin Equivalent Circuit (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
14	TIN		Factory Test Signal Input, Normally Tied to AV_{SS} or AV_{DD}
29, 30	VRT		Reference Top, Normally 4.0V
34, 35	VRB		Reference Bottom, Normally 2.0V
38	AT		Factory Test Signal Output, Leave Pin Open
42	TS		Factory Test Signal Input, Tie to AV_{DD}
37	TSTR		Factory Test Signal Input, Tie to AV_{SS} or AV_{DD}
23	$\overline{OE}$		D0 to D9 Output Enable Low: Output's Enabled High: High Impedance State
24	$\overline{CE}$		Chip Enable Low: Active State High: Standby State
19	TESTMODE		Test Mode High: Normal Output State Low: Output fixed

Pin Description and I/O Pin Equivalent Circuit (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
20	LINV		Output Inversion High: D0 to D8 are Inverted Low: D0 to D8 are Normal
21	MINV		Output Inversion High: D9 is Inverted Low: D9 is Normal
18, 25, 26	AV_{DD}		Analog V_{DD}
39	V_{IN}		Analog Input

A/D OUTPUT CODE TABLE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE										
		MSB										LSB
V_{RT}	1023	1	1	1	1	1	1	1	1	1	1	1
•	•					•						
•	•					•						
•	•					•						
•	512	1	0	0	0	0	0	0	0	0	0	0
•	511	0	1	1	1	1	1	1	1	1	1	1
•	•					•						
•	•					•						
•	•					•						
V_{RB}	0	0	0	0	0	0	0	0	0	0	0	0

NOTE:

1. This table shows the correlation between the analog input voltage and the digital output code. (TESTMODE = 1, MINV and LINV= 0)

OUTPUT DATA FORMAT TABLE

TESTMODE	LINV	MINV	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
1	0	0	N	N	N	N	N	N	N	N	N	N
1	1	0	I	I	I	I	I	I	I	I	I	N
1	0	1	N	N	N	N	N	N	N	N	N	I
1	1	1	I	I	I	I	I	I	I	I	I	I
0	1	1	1	0	1	0	1	0	1	0	1	0
0	0	1	0	1	0	1	0	1	0	1	0	0
0	1	0	1	0	1	0	1	0	1	0	1	1
0	0	0	0	1	0	1	0	1	0	1	0	1

NOTE:

1. This table shows the output state for the combination of TESTMODE, LINV, and MINV states.
2. N: Non-Inverted Output.
3. I: Inverted Output.

Detailed Description

The HI5710 is a two step A/D converter featuring a 5-bit upper comparator group and a 5-bit lower comparator group. An internal calibration mode is used to improve linearity which is user controlled.

The reference voltage must be supplied externally, with V_{RB} and V_{RT} typically set to 2.0V and 4.0V respectively.

Both chip enable and output enable pins are provided for flexibility and to reduce power consumption. The digital outputs can be inverted by inputs LINV and MINV, where LINV controls outputs D0 through D8 and MINV controls output D9 (MSB). This allows for outputs of various digital formats, such as straight binary, inverted binary, offset two's complement or inverted offset two's complement.

Analog Input

The analog input typically requires a $2V_{P-P}$ full scale input signal. The full scale input can range from 1.8V to 2.8V depending on the reference voltages.

The input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with an amplifier with sufficient bandwidth and drive capability. Op amps such as the HA5020 should make an excellent input amplifier depending on the applications requirements. In order to prevent parasitic oscillation, it may be necessary to insert a resistor between the output of the amplifier and the A/D input. Be sure to consider the amplifiers settling time in CCD applications or where step inputs are expected.

Reference Input

The input range of the A/D is set by the voltage difference of V_{RT} and V_{RB}. The HI5710 is designed to use an external reference from 2.0V to 4.0V on V_{RB} and V_{RT}, respectively. The analog input range of the A/D will now be from 2.0V to 4.0V. The V_{RB} range is 1.8V to 2.8V, the V_{RT} range is 3.6V to 4.6V, and (V_{RT} - V_{RB}) range is 1.8V to 2.8V.

V_{RT} and V_{RB} must be decoupled to analog ground to minimize noise on the reference. A 0.1μF capacitor is usually adequate.

Clock Input

The HI5710 samples the input signal on the rising edge of the clock with the digital data latched at the output after 3 clock cycles. The HI5710 is designed to use a 50% duty cycle square wave, but a 10% variation should not affect performance.

The clock input can be driven from +3.3V or +5V TTL or CMOS logic. Be sure not to use +5V logic if the HI5710 digital supply is +3.3V, unless you are sure the input will not exceed the supply voltage. When using a +3.3V digital supply, HC or AC CMOS logic will work well.

Digital Inputs

The digital inputs can be driven from +3.3V or +5V TTL or CMOS logic, except for the $\overline{OE}$ input. The $\overline{OE}$ input should be driven by CMOS logic when using a +5V digital supply though TTL logic may work if not heavily loaded. Be sure not to use 5V logic if the HI5710 digital supply is +3.3V, unless you are sure the input will not exceed the supply voltage. When using a +3.3V digital supply, HC or AC CMOS logic will work well.

Digital Outputs

The digital outputs are CMOS outputs. The LINV input will invert outputs D0 through D8 and MINV will invert output D9 (MSB). This allows the user to set the output for a number of different digital formats. The outputs can also be three-stated by pulling the $\overline{OE}$ input high.

The digital supply can run from +3.3V to +5V. The digital outputs will generate less radiated noise using +3.3V, but the outputs will have less drive capability. The digital outputs will only swing to DV_{DD}, therefore exercise care if interfacing to +5V logic when using a +3.3V supply.

The outputs can also be set to a fixed, defined state, see Output Data Format table. By setting the TESTMODE pin low, the outputs go to a defined digital pattern. This pattern is varied by the MINV and LINV inputs. This feature can be used for in-circuit testing of the digital bus.

Calibration Function

The HI5710 has a built-in calibration circuit to minimize linearity error. The RESET and CAL inputs should be timed as shown in Figure 4. A setup time of 10ns or longer is required for both the RESET and CAL inputs and they must stay low for at least one clock period.

A negative pulse on the RESET input should occur before the CAL input sees a falling edge. This sets up the initial calibration value. The calibration starts on the rising edge of the clock after the falling edge of the CAL pulse and requires 300 pulses to complete the calibration. The RESET input serves to minimize the calibration time, but it is not mandatory that it be used. The RESET input must remain at a high state when not in use. The calibration, when executed without the RESET pulse, requires 600 calibration pulses.

One calibration cycle is completed in 11 clock cycles. Seven clock cycles after the calibration pulse, the calibration circuit takes exclusive possession of the lower comparators, D0 through D4, for four clock cycles. During this time, the outputs are latched with the previous data (cycle seven data).

The upper 5 bits, D5 through D9, will operate as usual during the calibration if the SEL input is held high, making the HI5710 a 5 bit A/D converter during the last four clock cycles of the calibration. If the SEL input is low, the upper 5 bits are latched with the previous data (cycle seven data) during the last four cycles of the calibration as are the lower 5 bits.

The calibration must be done when the part is first powered up, when the supplies vary more that 100mV or when (V_{RT} - V_{RB}) changes more than 200mV. When first powered up, a minimum of 300 calibration pulses are required after the reset pulse. If no reset pulse is given, then a minimum of 600 calibration pulses are needed. Figure 4 shows several possible calibration timing schemes. It is not necessary to calibrate as often as these figures show, these are only design ideas. The HI5710 application note AN9511 shows a simple circuit for controlling the calibration function.

Power, Grounding, and Decoupling

To reduce noise effects, separate the analog and digital grounds. Bypass both the digital and analog V_{DD} pins to their respective grounds with a ceramic 0.1μF capacitor close to the pin. A larger capacitor (1μF to 10μF) should be placed somewhere on the PC board for low frequency decoupling of both analog and digital supplies.

The analog supply should be present before the digital supply to reduce the risk of latch-up. The digital supply can run from +3.3V to +5V. +3.3V generates less radiated noise at the digital outputs, but they have less drive capability. The specifications do not change with digital supply levels. Remember, the digital outs will only swing to DV_{DD}.

Typical Application Circuit

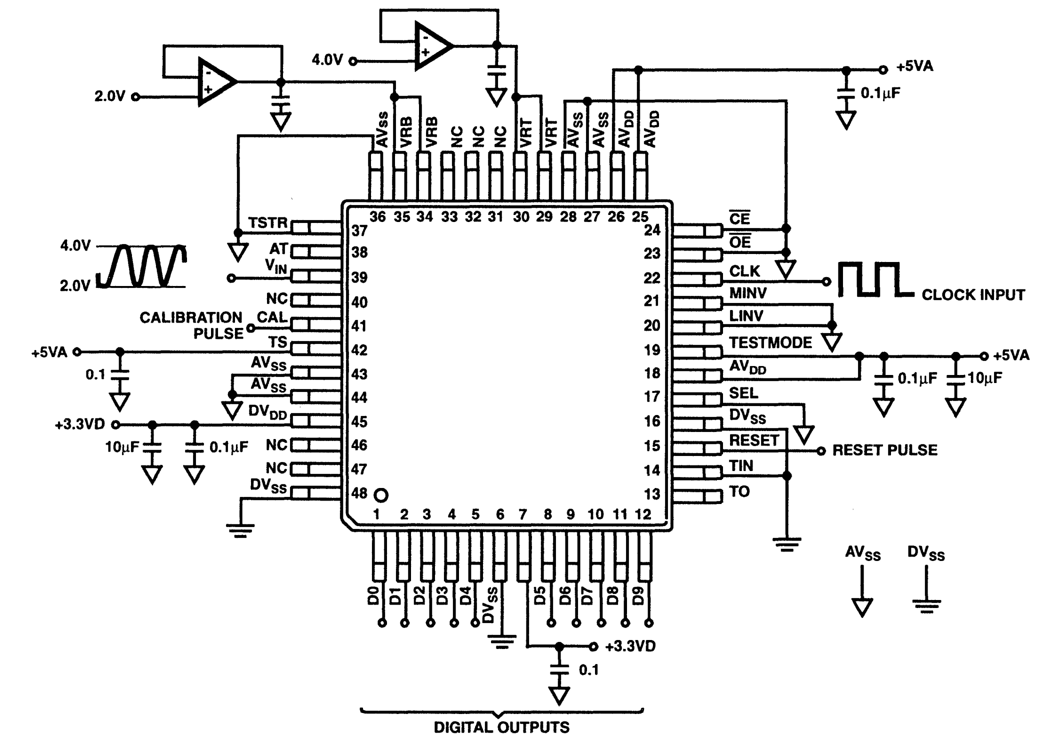


FIGURE 13.

Test Circuits

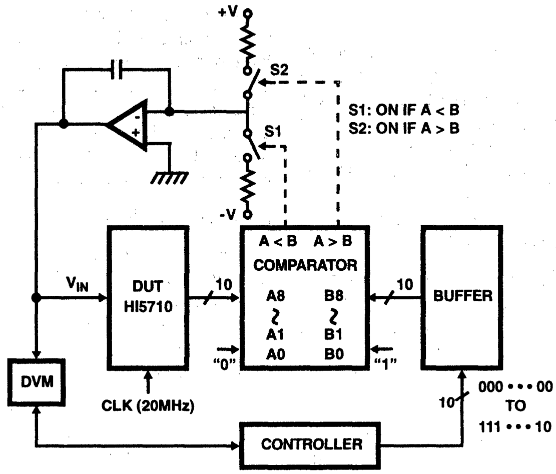


FIGURE 14. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

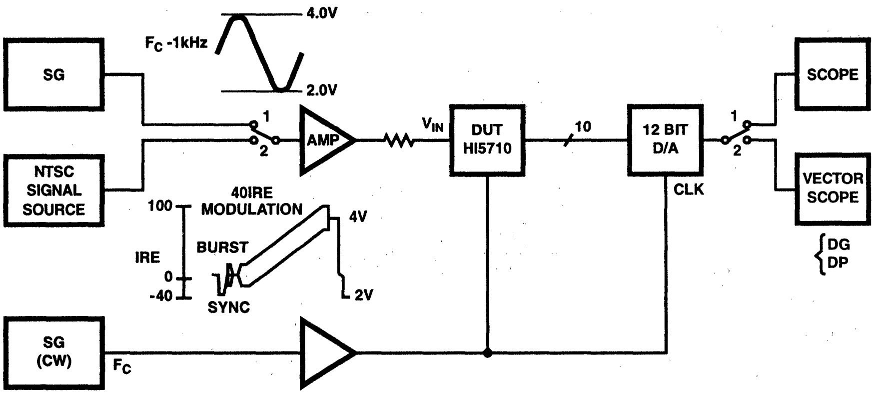


FIGURE 15. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

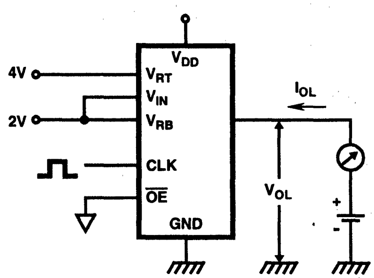


FIGURE 16A.

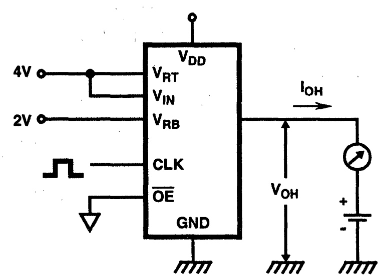


FIGURE 16B.

FIGURE 16. DIGITAL OUTPUT CURRENT TEST CIRCUIT

Timing Definitions

Aperture Delay - Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter - This is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Latency - After the analog sample is taken, the data on the bus is output at 3rd cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 3 cycles.

Power-up initialization - This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize some dynamic circuits within the converter.

Static Performance Definitions

Offset, full-scale, and gain all use a measured value of the external voltage reference to determine the ideal plus and minus full-scale values. The results are all displayed in LSBs.

Offset Error (V_{OS}) - The first code transition should occur at a level 1/2 LSB above the negative full-scale. Offset is defined as the deviation of the actual code transition from this point. Note that this is adjustable to zero.

Full-Scale Error (FSE) - The last code transition should occur for a analog input that is 1 and 1/2 LSBs below positive full-scale. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL) - DNL is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed for no missing codes over all temperature ranges.

Integral Linearity Error (INL) - INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection (PSRR) - Each of the power supplies are moved plus and minus 5% and the shift in the offset and gain error is noted. The number reported is the percent change in these parameters versus full-scale divided by the percent change in the supply.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5710. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 2048 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full-scale for all these tests. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR) - SNR is the measured rms signal to rms noise at a specified input and sampling frequency. The noise is the rms sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD) - SINAD is the measured rms signal to rms sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB) - The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$$

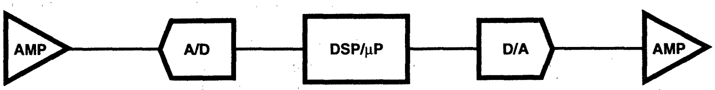
where: $V_{CORR} = 0.5dB$

2nd and 3rd Harmonic Distortion - This is the ratio of the rms value of the 2nd and 3rd harmonic component respectively to the rms value of the measured input signal.

Transient Response - Transient response is measured by inputting a step to the input to the part and measuring the number of cycles it takes for the output code to settle within a defined accuracy.

Overvoltage Recovery - Overvoltage Recovery is measured by inputting a step, which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within a defined accuracy.

Full Power Input Bandwidth - Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.



HFA1135	HI5710	HSP9501	HI1171	HA5020
HFA1245	HI5702	HSP48410	CA3338	HA2842
HA5020		HSP48908	HI3050	HFA1115
		HSP48212		
		HSP43891		
		HSP43168		
		HSP43216		

HFA1135: 350MHz Op Amp with Output Limiting
HFA1245: Dual 350MHz Op Amp with Disable/Enable
HA5020: 100MHz Video Op Amp
HI5710: 10-Bit 20 MSPS A/D Converter
HI5702: 10-Bit 40 MSPS A/D Converter
HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/Accumulating Buffer, 10-Bit Pixel Resolution
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48212: Digital Video Mixer
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HI1171: 8-Bit 40MHz Video D/A Converter
CA3338: 8-Bit 50MHz Video D/A Converter
HI3050: Triple 10-Bit 50MHz Video DAC
HA2842: High Output Current, Video Op Amp
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 16. 10-BIT VIDEO IMAGING COMPONENTS

HFA3600	HI5710	HSP43168	HI5721	HFA1115
HFA3102	HI5702	HSP43216	HI20201	
HFA3101		HSP43891	HI20203	
HFA1100		HSP50016		
		HSP50110		
		HSP50210		

HFA3600: Low Noise Amplifier/Mixer
HFA3102: Dual Long-Tailed Pair Transistor Array
HFA3101: Gilbert Cell Transistor Array
HFA1100: 850MHz Op Amp
HI5710: 10-Bit 20 MSPS A/D Converter
HI5702: 10-Bit 40 MSPS A/D Converter
HSP43168: Dual FIR Filter, 10-Bit, 33MHz/45MHz
HSP43216: Digital Half Band Filter
HSP43891: Digital Filter, 30MHz, 9-Bit
HSP50016: Digital Down Converter
HSP50110: Digital Quadrature Tuner
HSP50210: Digital Costas Loop
HI5721: 10-Bit 100MHz Communications D/A Converter
HI20201: 10-Bit 160MHz High Speed D/A Converter
HI20203: 8-Bit 160MHz High Speed D/A Converter
HFA1115: 350MHz Programmable Gain Buffer with Output Limiting

CMOS Logic Available in HC, HCT, AC, ACT, and FCT.

FIGURE 17. 10-BIT COMMUNICATIONS COMPONENTS

HARRIS SEMICONDUCTOR

HI5714

PRELIMINARY

May 1995

8-Bit, 75 MSPS A/D Converter

Features

- **75 MSPS Sampling Rate**
- **Low Power (325mW)**
- **7.7 ENOB at 4.43MHz**
- **Overflow/Underflow Three-State TTL Output**
- **Operates with Low Level AC Clock**
- **Very Low Analog Input Capacitance**
- **No Buffer Amplifier Required**
- **No Sample and Hold Required**
- **TTL Compatible I/O**
- **Evaluation Board Available, HI5714EVAL**

Applications

- **Video Digitizing**
- **Direct Broadcast Satellite (DBS) Receivers**
- **Tape Drive/Mass Storage**
- **Medical Ultrasound Imaging**
- **Communication Systems**
- **Wireless LAN Systems**

Description

The HI5714 is a high precision, monolithic, 8-bit, Analog-to-Digital Converter fabricated in Harris's advanced HBC10 BiCMOS process.

The HI5714 is optimized for a wide range of applications such as ultrasound imaging, mass storage, instrumentation, and video digitizing, where wide bandwidth and low power consumption are essential. The HI5714 is offered in 40 MSPS, 60 MSPS, and 75 MSPS samples rates.

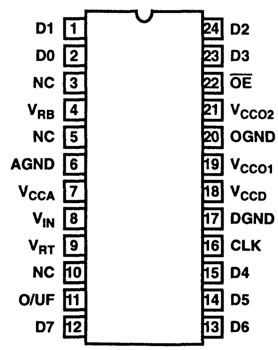
The HI5714 delivers ±0.5 LSB differential nonlinearity while consuming only 325mW power at 75 MSPS. The digital inputs and outputs are TTL compatible, as well as allowing for a low-level sine wave clock input. The HI5714 is a pin for pin replacement for the TDA8714.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE	SAMPLING FREQUENCY (MHz)
HI5714/4CB	0^oC to $+70^oC$	24 Lead Plastic SOIC (W)	40
HI5714/6CB	0^oC to $+70^oC$	24 Lead Plastic SOIC (W)	60
HI5714/7CB	0^oC to $+70^oC$	24 Lead Plastic SOIC (W)	75

Pinout

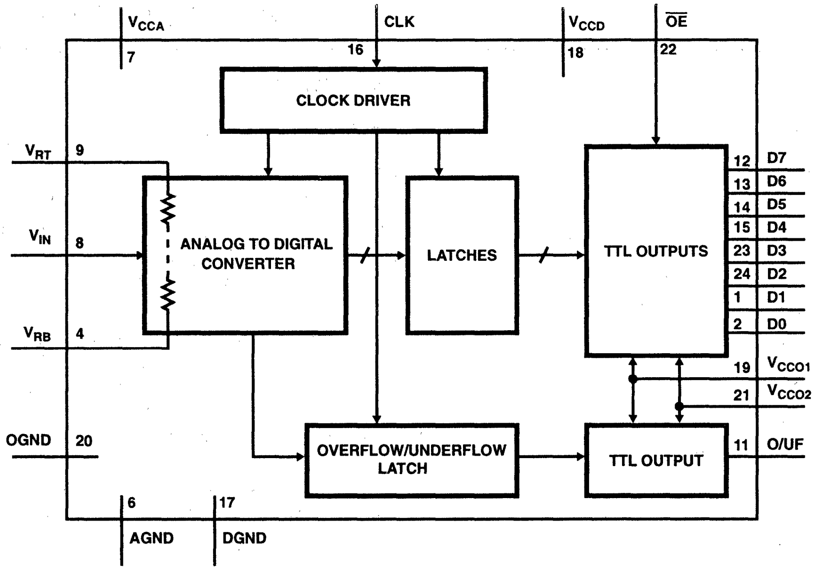
HI5714
SOIC (300 MIL)
TOP VIEW



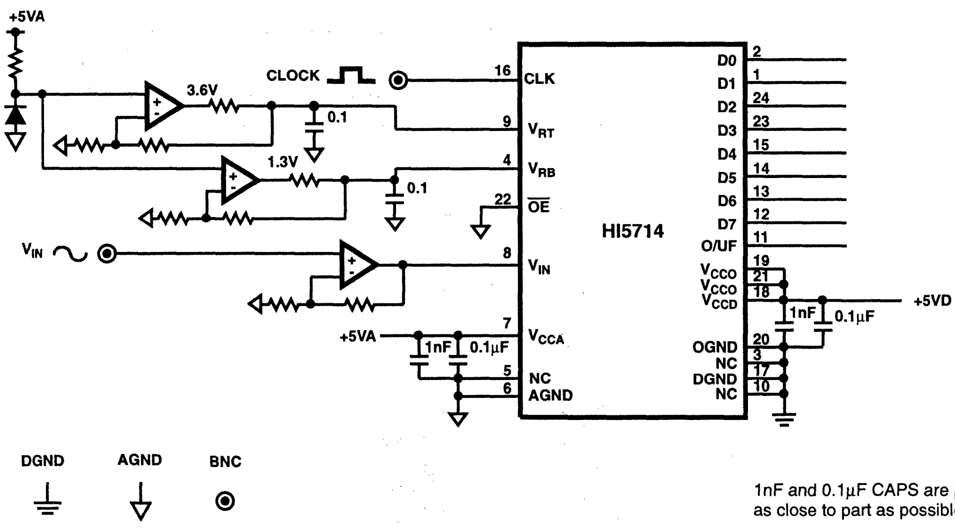
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3973**

Functional Block Diagram



Typical Application Schematic



1nF and 0.1µF CAPS are placed as close to part as possible.

NOTES:

1. Pin 5 should be connected to AGND and pins 3 and 10 to DGND to reduce noise coupling into the device.
2. Analog and Digital supplies should be separated and decoupled to reduce digital noise coupling into the analog supply.

Absolute Maximum Ratings

V_{CCA}, V_{CCD}, V_{CCO} . . . . . -0.3V to +6.0V
V_{CCA} - V_{CCD} 0.3V
V_{CCO} - V_{CCD} 0.3V
V_{CCA} - V_{CCO} 0.3V
V_{IN}, V_{CLK}, V_{RT}, V_{RB}, $\overline{OE}$ . . . . . -0.3V to +6.0V
I_{OUT}, Digital Pins. 10mA
Input Current, All Pins 1mA
Digital I/O Pins . . . . . OGND to V_{CCO}
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . . 300°C
(Lead Tips Only)

Thermal Information

Thermal Resistance θ_{JA}
HI5714CB . . . . . 75°C/W
Maximum Junction Temperature. . . . . +150°C
Operating Temperature Range
HI5714CB . . . . . 0°C to +70°C

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. The supply voltages V_{CCA} and V_{CCD} may have any value between -0.3V and +6V as long as the difference V_{CCA} - V_{CCD} lies between -0.3V and +0.3V.

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Electrical Specifications

$V_{CCA} = V_{CCD} = V_{CCO} = +5V$; $V_{RB} = 1.3V$; $V_{RT} = 3.6V$; $T_A = 25°C$, Unless Otherwise Specified

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
CLOCK (Referenced to DGND) (Note 1)					
Logic Input Voltage Low, V_{IL}		0	-	0.8	V
Logic Input Voltage High, V_{IH}		2.0	-	V_{CCD}	V
Logic Input Current Low, I_{IL}	$V_{CLK} = 0.4V$	-400	-	-	µA
Logic Input Current High, I_{IH}	$V_{CLK} = 2.7V$	-	-	300	µA
Input Impedance, Z_{IN}	$f_{CLK} = 75MHz$	-	2	-	kΩ
Input Capacitance, C_{IN}	$f_{CLK} = 75MHz$	-	4.5	-	pF
$\overline{OE}$ (Referenced to DGND)					
Logic Input Voltage Low, V_{IL}		0	-	0.8	V
Logic Input Voltage High, V_{IH}		2.0	-	V_{CCD}	V
Logic Input Current Low, I_{IL}	$V_{IL} = 0.4V$	-400	-	-	µA
Logic Input Current High, I_{IH}	$V_{IH} = 2.7V$	-	-	20	µA
V_{IN} (Referenced to AGND)					
Input Current Low, I_{IL}	$V_{IN} = 1.2V$	-	0	-	µA
Input Current High, I_{IH}	$V_{IN} = 3.5V$	80	130	180	µA
Input Impedance, Z_{IN}	$f_{IN} = 4.43MHz$	-	10	-	kΩ
Input Capacitance, C_{IN}	$f_{IN} = 4.43MHz$	-	14	-	pF
REFERENCE INPUT					
Bottom Reference Range, V_{RB}		1.2	1.3	1.6	V
Top Reference Range, V_{RT}		3.5	3.6	3.9	V
Reference Range, V_{REF} (V_{RT} - V_{RB})		1.9	2.3	2.7	V
Reference Current, I_{REF}		-	10	-	mA
Reference Ladder Resistance, R_{LAD}		-	230	-	Ω
R_{LADTC}		-	0.24	-	Ω/°C

Electrical Specifications $V_{CCA} = V_{CCD} = V_{CCO} = +5V$; $V_{RB} = 1.3V$; $V_{RT} = 3.6V$; $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Offset Error, V_{OB}	(Note 2)	-	255	-	mV
V_{OBTC}	(Note 2)	-	TBD	-	µV/°C
Full Scale Error, V_{OT}	(Note 2)	-	-300	-	mV
V_{OTTC}	(Note 2)	-	TBD	-	µV/°C
DIGITAL OUTPUTS (D0 to D7 and O/UF Referenced to OGND)					
Logic Output Voltage Low, V_{OL}	$I_O = 1mA$	0	-	0.4	V
Logic Output Voltage High, V_{OH}	$I_O = -0.4mA$	2.7	-	V_{CCO}	V
Output Leakage Current, I_D	$0.4V < V_{OUT} < V_{CCO}$	-20	-	+20	A
SWITCHING CHARACTERISTICS (Notes 1, 2) See Figure 3					
Sample Rate, f_{CLK} HI5714/7		75	-	-	MHz
HI5714/6		60	-	-	MHz
HI5714/4		40	-	-	MHz
Clock Pulse Width High, t_{CPH}		6	-	-	ns
Clock Pulse Width Low, t_{CPL}		6	-	-	ns
ANALOG SIGNAL PROCESSING ($f_{CLK} = 40MHz$)					
Differential Gain, DG	(Note 3)	-	0.3	-	%
Differential Phase, DP	(Note 3)	-	0.4	-	degree
HARMONICS ($f_{CLK} = 75MHz$)					
Second Harmonic, H2	$f_{IN} = 4.43MHz$	-	-65	-	dB
Third Harmonic, H3	$f_{IN} = 4.43MHz$	-	-62	-	dB
Total Harmonic Distortion, THD	$f_{IN} = 4.43MHz$	-	-60	-	dB
Spurious Free Dynamic Range, SFDR	$f_{IN} = 4.43MHz$	-	62	-	dB
Analog Input Bandwidth (-3dB)		-	18	-	MHz
TRANSFER FUNCTION					
Integral Linearity Error, INL		-	±0.5	-	LSB
Differential Linearity Error, DNL		-	±0.35	-	LSB
AC INL	(Note 4)	-	±1	-	LSB
EFFECTIVE NUMBER OF BITS					
ENOB HI5714/4 ($f_{CLK} = 40MHz$)	$f_{IN} = 4.43MHz$	-	7.8	-	Bits
	$f_{IN} = 7.5MHz$	-	7.6	-	Bits
HI5714/6 ($f_{CLK} = 60MHz$)	$f_{IN} = 4.43MHz$	-	7.75	-	Bits
	$f_{IN} = 7.5MHz$	-	7.55	-	Bits
HI5714/7 ($f_{CLK} = 75MHz$)	$f_{IN} = 4.43MHz$	-	7.7	-	Bits
	$f_{IN} = 10MHz$	-	7.3	-	Bits
	$f_{IN} = 15MHz$	-	6.3	-	Bits

Electrical Specifications $V_{CCA} = V_{CCD} = V_{CCO} = +5V$; $V_{RB} = 1.3V$; $V_{RT} = 3.6V$; $T_A = 25^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Bit Error Rate, BER	(Note 5)	-	10^{-11}	-	Times/ Sample
TIMING (f_{CLK} = 75MHz) See Figures 1, 2					
Sampling Delay, t_{SD}		-	-	2	ns
Output Hold Time, t_{HD}		5	-	-	ns
Output Delay Time, t_D		-	10	13	ns
Output Enable Delay, t_{PZH}	Enable to High	-	19	-	ns
Output Enable Delay, t_{PZL}	Enable to Low	-	16	-	ns
Output Disable Delay, t_{PHZ}	Disable from High	-	14	-	ns
Output Disable Delay, t_{PLZ}	Disable from Low	-	9	-	ns
Aperture Jitter, t_{AJ}		-	50	-	ps
POWER SUPPLY CHARACTERISTICS					
Analog Power Supply Range, V_{CCA}		4.75	5.0	5.25	V
Digital Power Supply Range, V_{CCD}		4.75	5.0	5.25	V
Output Power Supply Range, V_{CCO}		4.75	5.0	5.25	V
Total Supply Current			65	75	mA
Supply Current, I_{CCA}		-	31	-	mA
Supply Current, I_{CCD}		-	26	-	mA
Supply Current, I_{CCO}		-	7	-	mA
Power Dissipation		-	320	375	mW

NOTES:

1. In addition to a good layout of the digital and analog ground, it is recommended that the rise and fall times of the clock not be less than 1ns.
2. Analog input voltages producing code 00 up to and including FF.

   V_{OB} (Bottom Offset Voltage) is the difference between the analog input which produces data equal to 00 and the Bottom Reference Voltage (V_{RB}).

   V_{OBTC} (Bottom Offset Voltage Temperature Coefficient) is the variation of V_{OB} with temperature.

   V_{OT} (Top Offset Voltage) is the difference between the Top Reference Voltage (V_{RT}) and the analog input which produces data output equal to FF.

   V_{OTTC} (Top Offset Voltage Temperature Coefficient) is the variation of V_{OT} with temperature.
3. Input is standard 5 step video test signal. A 12-bit R reconstruct DAC and VM700 are used for measurement.
4. Full-scale sinewave, f_{IN} = 4.43MHz.
5. f_{CLK} = 75MHz, f_{IN} = 4.43MHz, V_{IN} = ±8 LSB at code 128, 50% Clock duty cycle.

Timing Waveforms

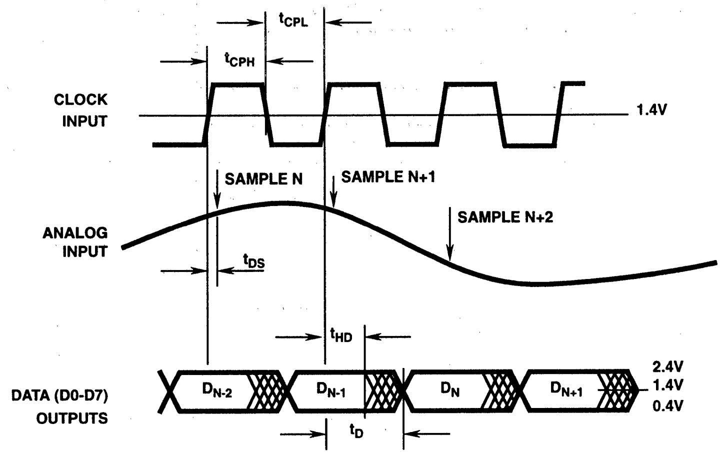


FIGURE 1. INPUT-TO-OUTPUT TIMING

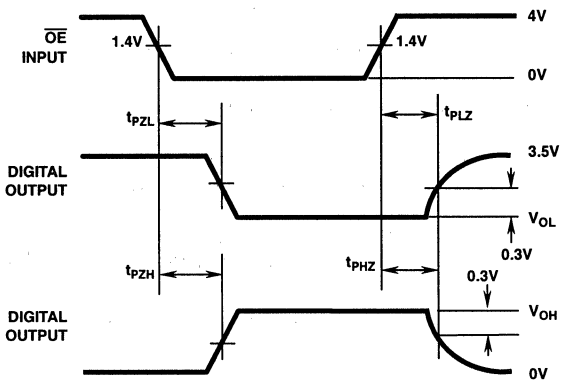


FIGURE 2. THREE-STATE TIMING CIRCUIT

Pin Description

PIN NUMBER	SYMBOL	DESCRIPTION
1, 2,12-15, 23, 24	D0 to D7	Digital outputs, D0 (LSB) to D7 (MSB)
4	V_{RB}	Bottom reference voltage input. Range: 1.2V to 1.6V
6	AGND	Analog ground
7	V_{CCA}	Analog +5V
8	V_{IN}	Analog input
9	V_{RT}	Top reference voltage input. Range: 3.5V to 3.9V
11	O/UF	Underflow/Overflow digital output. Goes high if the analog input goes above or below the reference (VRB, VRT) minus the offset
16	CLK	Clock input
17	DGND	Digital GND
18	V_{CCD}	Digital +5V
19, 21	V_{CCO1}, V_{CCO2}	Digital +5V for digital output stage
20	OGND	Digital ground for digital output stage
22	$\overline{OE}$	Output enable High: Digital outputs are three-stated Low: Digital outputs are active

TABLE 1. A/D CODE TABLE

CODE DESCRIPTION	(NOTE 1) INPUT VOLTAGE V_{RT} = 3.6V V_{RB} = 1.3V	O/UF	BINARY OUTPUT CODE							
			D7	D6	D5	D4	D3	D2	D1	D0
Underflow	<1.555V	1	0	0	0	0	0	0	0	0
0	1.555V	0	0	0	0	0	0	0	0	0
1	-	0	-	-	-	-	-	-	-	-
-	-	0	-	-	-	-	-	-	-	-
-	-	0	-	-	-	-	-	-	-	-
254	-	0	1	1	1	1	1	1	1	0
255	3.300V	0	1	1	1	1	1	1	1	1
Overflow	>3.300V	1	1	1	1	1	1	1	1	1

NOTE:

1. The voltages listed above represent the ideal transition of each output code shown as a function of the reference voltage, including the typical reference offset voltages.

TABLE 2. MODE SELECTION

$\overline{OE}$	D7 to D0	O/UF
1	High Impedance	High Impedance
0	Active: Binary	Active

4 A/D CONVERTERS

Detailed Description

Theory of Operation

The HI5714 design utilizes a folding and interpolating architecture. This architecture reduces the number of comparators, reference taps, and latches, thereby reducing power requirements, die size and cost.

A folding A/D converter operates basically like a 2 step subranging converter by using 2 lower resolution converters to do a course and subranged fine conversion. A more complete description is given in the application note "Using the HI5714 Evaluation Board" (ANXXXX).

Reference Input, V_{RT} and V_{RB}

The HI5714 requires an external reference to be connected to pins 4 and 9, V_{RB} and V_{RT}.

It is recommended that adequate high frequency decoupling be provided at the reference input pin in order to minimize overall converter noise. A 0.1μF and a 1nF capacitor as close as possible to the reference pins work well.

V_{RT} must be kept within the range of 3.5V to 3.9V and V_{RB} within 1.2V to 1.6V. If the reference voltages go outside their respective ranges, the input folding amplifiers may saturate giving erroneous digital data. The range for (V_{RT} - V_{RB}) is 1.9V to 2.7V, which defines the analog input range.

Digital Control and Clock Requirements

The HI5714 provides a standard high-speed interface to external TTL logic families.

The outputs can be three-stated by setting the $\overline{OE}$ input (pin 22) high.

The clock input operates at standard TTL levels as well as a low level sine wave around the threshold level. The HI5714 can operate with clock frequencies from DC to 75MHz. The clock duty cycle should be 50% ±10% to ensure rated performance. Duty cycle variation, within the specified range, has little effect on performance. Due to the clock speed it is important to remember that clock jitter will affect the quality of the digital output data.

The clock can be stopped at any time and restarted at a later time. Once restarted the digital data will be valid at the second rising edge of the clock plus the data delay time.

Digital Outputs and O/UF Output

The digital outputs are standard TTL type outputs. The HI5714 can drive 1 to 3 TTL inputs depending on the input current requirements.

Should the analog input exceed the top or bottom reference the over/underflow output (pin 11) will go high. Should the analog input exceed the top reference voltage, V_{RT}, the digital outputs will remain at all 1s until the analog input goes below V_{RT}. Also, should the analog input go below the bottom reference voltage, V_{RB}, the digital outputs will remain at all 0s until the analog input goes above V_{RT}.

Analog Input

The analog input will accept a voltage within the reference voltage levels, V_{RB} and V_{RT}, minus some offset. The offset is specified in the Electrical Specifications table.

The analog input is relatively high impedance (10kΩ) but should be driven from a low impedance source. The input capacitance is low (14pF) and there is little kickback from the input, so a series resistance is not necessary but it may help to prevent the driving amplifier from oscillating.

The input bandwidth is typically 18MHz. Exceeding 18MHz will result in sparkle at the digital outputs. The bandwidth remains constant at clock rates up to 75MHz.

Supply and Ground Considerations

In order to keep digital noise out of the analog signal path, the HI5714 has separate analog and digital supply and ground pins. The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds.

The analog and digital grounds should be tied together at one point near the HI5714. The grounds can be connected directly, through an inductor (ferrite bead), or a low valued resistor. DGND and AGND can be tied together. To help minimize noise, tie pin 5 (NC) to AGND and pins 3 (NC) and 10 (NC) to DGND.

For best performance, the supplies to the HI5714 should be driven by clean, linear regulated supplies. The board should also have good high frequency leaded decoupling capacitors mounted as close as possible to the converter. Capacitor leads must be kept as short as possible (less than 1/2 inch total length). A 0.1μF and a 1nF capacitor as close as possible to the pin works well. Chip capacitors will provide better high frequency decoupling but leaded capacitors appear to be adequate.

If the part is to be powered by a single supply, then the analog supply pins should be isolated by ferrite beads from the digital supply pins. This should help minimize noise on the analog power pins.

Refer to Application Note AN9214, "Using Harris High Speed A/D Converters", for additional considerations when using high speed converters.

Increased Accuracy

Further calibration of the ADC can be done to increase absolute level accuracy. First, a precision voltage equal to the ideal VIN_{-FS} + 0.5 LSB is applied at V_{IN}. Adjust V_{RB} until the 0 to 1 transition occurs on the digital output. Next, a voltage equal to the ideal VIN_{+FS} - 1.5 LSB is applied at V_{IN}. V_{RT} is then adjusted until the 254 to 255 transition occurs on the digital output.

Applications

Figures 3 and 4 show two possible circuit configurations, AC coupled with a DC restore circuit and DC coupled with a DC offset amplifier.

Due to the high clock rate, FCT (TTL/CMOS) or FAST (TTL) glue logic should be used. FCT logic will tend to have large overshoots if not loaded. Long traces (>2 or 3 inches) should be terminated to maintain signal integrity.

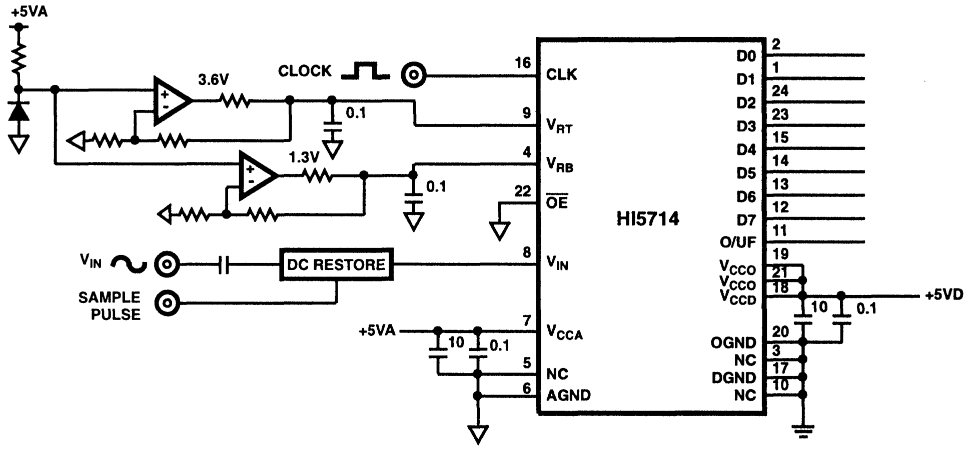


FIGURE 3. TYPICAL AC COUPLED INPUT WITH DC RESTORE

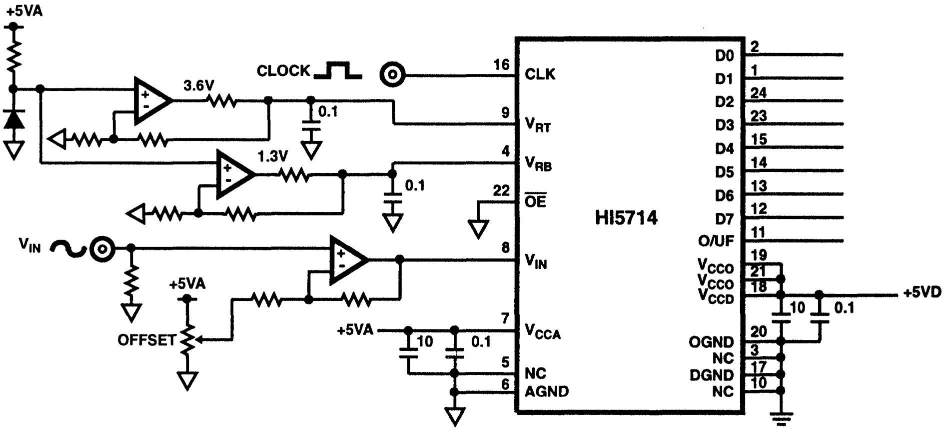
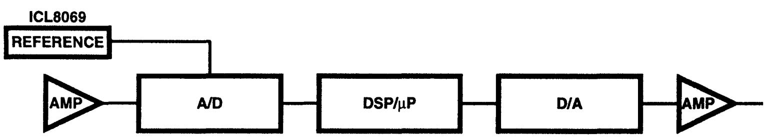


FIGURE 4. TYPICAL DC COUPLED INPUT



HA5020 (Single)	HI5714 (8-Bit)	HSP9501	HI1171 (8-Bit)	HA5020 (Single)
HA5022 (Dual)		HSP48410	CA3338 (8-Bit)	HA2842 (Single)
HA5024 (Quad)		HSP48908	HI5721 (10-Bit)	HFA1115 (Single)
HA5013 (Triple)		HSP48901	HI3050 (10-Bit)	HFA1212 (Dual)
HFA1105 (Single)		HSP48212		HFA1412 (Quad)
HFA1205 (Dual)		HSP43881		
HFA1405 (Quad)		HSP43168		

HSP9501: Programmable Data Buffer
HSP48410: Histogrammer/accumulating Buffer, 10-Bit Pixel Resolution, 4K x 4K Frame Size
HSP48908: 2-D Convolver, 3 x 3 Kernal Convolution, 8-Bit
HSP48901: 3 x 3 Image Filter, 30MHz, 8-Bit
HSP48212: Video Mixer
HSP43881: Digital Filter, 30MHz, 1-D and 2-D Fir Filters
HSP43168: Dual Fir Filter, 10-Bit, 33/45MHz

CMOS Logic Available in FCT

FIGURE 5. 8-BIT VIDEO COMPONENTS

Timing Definitions

Aperture Delay: Aperture delay is the time delay between the external sample command (the rising edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter: This is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Latency

After the analog sample is taken, the data on the bus is output at the next rising edge of the clock. This is due to the output latch of the converter. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 1 cycle.

Static Performance Definitions

Offset Error and Full-Scale Error use a measured value of the external voltage reference to determine the ideal plus and minus full-scale values. The results are all displayed in LSBs.

Offset Error (V_{OB})

The first code transition should occur at a level 0.5 LSB above the negative full-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (V_{OT})

The last code transition should occur for a analog input that is 1.5 LSBs below positive full-scale. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed to have no missing codes.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5714. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 2048 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is 0.5dB down from full-scale for these tests. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$$

where: $V_{CORR} = 0.5dB$.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the 2nd and 3rd harmonic component respectively to the RMS value of the measured input signal.

Full Power Input Bandwidth

Full power bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Die Characteristics

DIE DIMENSIONS:
134 x 134 x 19 ±1 mils

METALLIZATION:
Type: Al Si Cu
Thickness: M1 - 8kÅ, M2 - 17kÅ

GLASSIVATION:
Type: Sandwich Passivation
Undoped Silicon Glass (USG) + Nitride
Thickness: USG - 8kÅ, Nitride - 4.2kÅ
Total 12.2kÅ + 2kÅ

DIE ATTACH: Silver Filled Epoxy

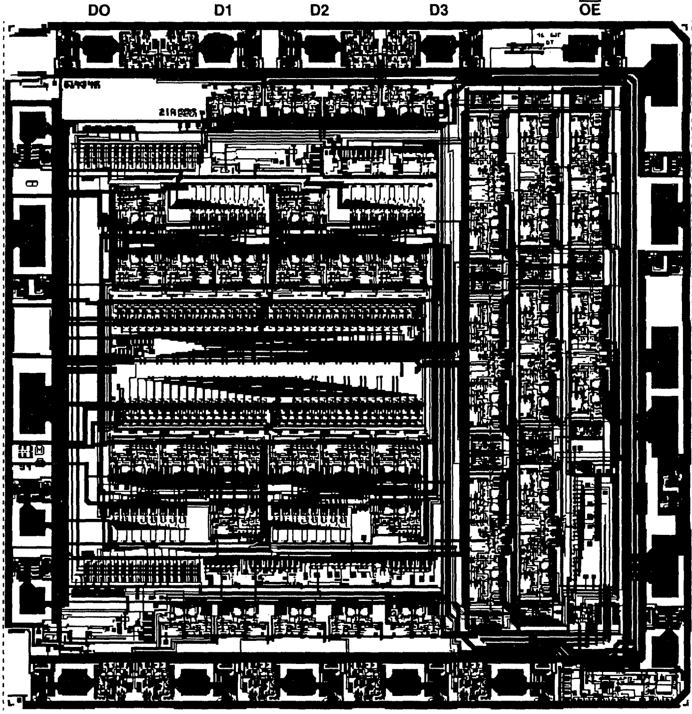
WORST CASE CURRENT DENSITY:
1.6×10^4 A/cm^2

TRANSISTOR COUNT: 3714

SUBSTRATE POTENTIAL (Powered UP): GND (0.0V)

Metallization Mask Layout

HI5714



July 1995

12-Bit, 3 MSPS Sampling A/D Converter

Features

- 3 MSPS Throughput Rate
- 12-Bit, No Missing Codes Over Temperature
- 1.0 LSB Integral Linearity Error
- Buffered Sample and Hold Amplifier
- Precision Voltage Reference
- ±2.5V Input Signal Range
- 20MHz Input BW Allows Sampling Beyond Nyquist
- Zero Latency/No Pipeline Delay
- Evaluation Board Available

Applications

- High Speed Data Acquisition Systems
- Medical Imaging
- Radar Signal Analysis
- Document and Film Scanners
- Vibration/Waveform Spectrum Analysis
- Digital Servo Control

Description

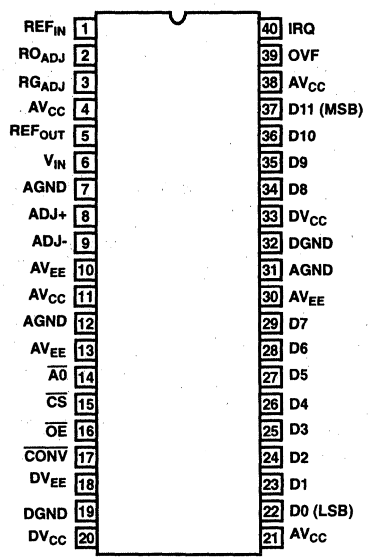
The HI5800 is a monolithic, 12-bit, sampling Analog-to-Digital Converter fabricated in the HBC10 BiCMOS process. It is a complete subsystem containing a sample and hold amplifier, voltage reference, two-step subranging A/D, error correction, control logic, and timing generator. The HI5800 is designed for high speed applications where wide bandwidth, accuracy and low distortion are essential.

Ordering Information

PART NUMBER	LINEARITY	TEMP. RANGE	PACKAGE
HI5800BID	±1 LSB	-40°C to +85°C	40 Lead Sidebraze
HI5800JCD HI5800KCD	±2 LSB ±1 LSB	0°C to +70°C	40 Lead Sidebraze

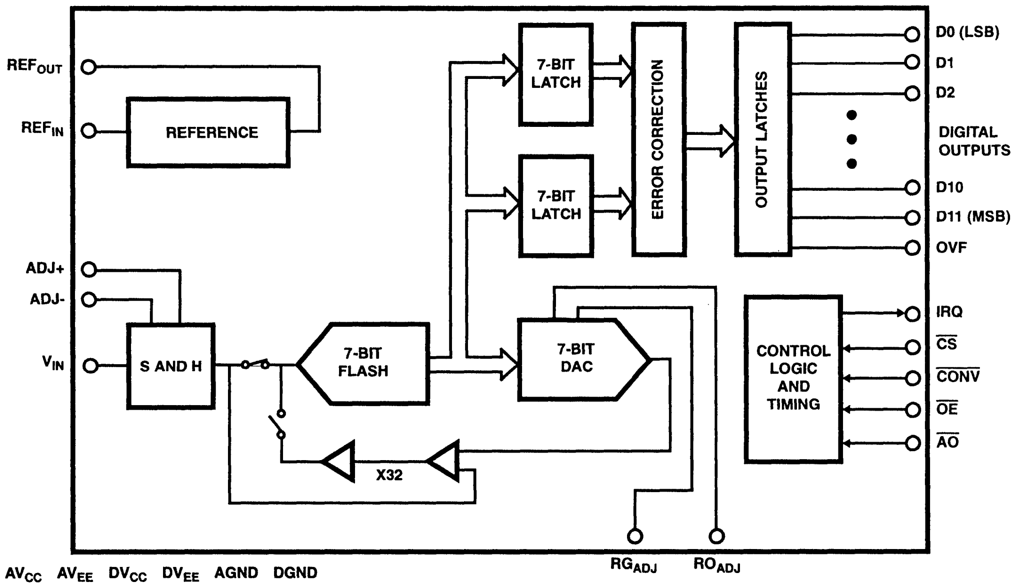
Pinout

40 LEAD SIDEBRAZE
TOP VIEW

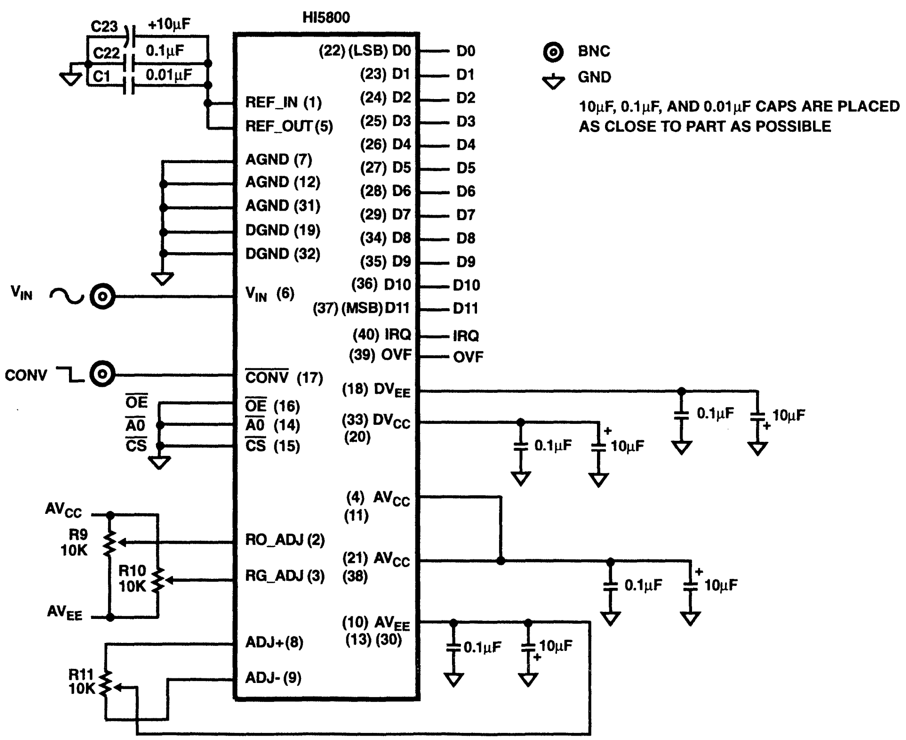


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Block Diagram



Typical Application Schematic



4

A/D CONVERTERS

Absolute Maximum Ratings

Supply Voltages
- AV_{CC} or DV_{CC} to GND . . . . . +5.5V
- AV_{EE} or DV_{EE} to GND. . . . . -5.5V
- DGND to AGND . . . . . ±0.3V

Analog Input Pins
- Reference Input REF_{IN} . . . . . +2.75V
- Signal Input V_{IN} . . . . . ±(REF_{IN} +0.2V)

RO_{ADJ}, RG_{ADJ}, ADJ+, ADJ- . . . . . V_{EE} to V_{CC}
Digital I/O Pins . . . . . GND to V_{CC}
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . . +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
HI5800BID/JCD/KCD	29°C/W	9°C/W

Maximum Power Dissipation +70°C 2.26W
Junction Temperature
- HI5800JCD/KCD . . . . . +175°C
- HI5800BID . . . . . +175°C

Operating Temperature
- HI5800JCD/KCD . . . . . 0°C to +70°C
- HI5800BID . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used Unless Otherwise Specified

PARAMETER	TEST CONDITION		HI5800JCD 0°C TO +70°C MIN	TYP	MAX	HI5800KCD, HI5800BID 0°C TO +70°C -40°C TO +85°C MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE									
Resolution			12	-	-	12	-	-	Bits
Integral Linearity Error, INL	F_S = 3MHz, f_{IN} = 45Hz Ramp		-	±0.7	±2	-	±0.5	±1	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	F_S = 3MHz, f_{IN} = 45Hz Ramp		-	±0.5	±1	-	±0.3	±1	LSB
Offset Error, VOS (Adjustable to Zero)	(Note 7)	JCD, KCD	-	±2	±15	-	±2	±10	LSB
		BID	-	-	-	-	±3	±15	LSB
Full Scale Error, FSE (Adjustable to Zero)	(Note 7)	JCD, KCD	-	±2	±15	-	±2	±10	LSB
		BID	-	-	-	-	±3	±15	LSB
DYNAMIC CHARACTERISTICS (Input Signal Level 0.5dB below full scale)									
Throughput Rate	No Missing Codes		3.0	-	-	3.0	-	-	MSPS
Signal to Noise Ratio (SNR) $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	F_S = 3MHz, f_{IN} = 20kHz		66	69	-	68	71	-	dB
	F_S = 3MHz, f_{IN} = 1MHz		65	67	-	67	69	-	dB
Signal to Noise Ratio (SINAD) $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	F_S = 3MHz, f_{IN} = 20kHz		66	68	-	68	71	-	dB
	F_S = 3MHz, f_{IN} = 1MHz		65	67	-	67	68	-	dB
Total Harmonic Distortion, THD	F_S = 3MHz, f_{IN} = 20kHz		-	-74	-70	-	-85	-74	dBc
	F_S = 3MHz, f_{IN} = 1MHz		-	-70	-68	-	-77	-70	dBc
Spurious Free Dynamic Range, SFDR	F_S = 3MHz, f_{IN} = 20kHz		71	76	-	76	86	-	dBc
	F_S = 3MHz, f_{IN} = 1MHz		68	72	-	71	77	-	dBc
Intermodulation Distortion, IMD	F_S = 3MHz, f1 = 49kHz, f_2 = 50kHz		-	-74	-66	-	-79	-70	dBc
Differential Gain	F_S = 1MHz		-	0.9	-	-	0.9	-	%
Differential Phase	F_S = 1MHz		-	0.05	-	-	0.05	-	Degrees

Electrical Specifications AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	HI5800JCD 0°C TO +70°C MIN	TYP	MAX	HI5800KCD, HI5800BID 0°C TO +70°C -40°C TO +85°C MIN	TYP	MAX	UNITS
Aperture Delay, t_{AD}		-	12	20	-	12	20	ns
Aperture Jitter, t_{AJ}		-	10	20	-	10	20	ps
ANALOG INPUT								
Input Voltage Range		-	±2.5	±2.7	-	±2.5	±2.7	V
Input Resistance		1	3	-	1	3	-	MΩ
Input Capacitance		-	5	-	-	5	-	pF
Input Current		-	±1	±10	-	±1	±10	μA
Input Bandwidth		-	20	-	-	20	-	MHz
INTERNAL VOLTAGE REFERENCE								
Reference Output Voltage, REF_{OUT} (Loaded)		2.450	2.500	2.550	2.470	2.500	2.530	V
Reference Output Current	Note 5	2	-	-	2	-	-	mA
Reference Temperature Coefficient		-	20	-	-	13	-	ppm/°C
REFERENCE INPUT								
Reference Input Range		-	2.5	2.6	-	2.5	2.6	V
Reference Input Resistance		-	200	-	-	200	-	Ω
DIGITAL INPUTS								
Input Logic High Voltage, V_{IH}	Note 6	2.0	-	-	2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	-	-	0.8	V
Input Logic Current, I_{IL}	V_{IN} = 0V, 5V	-	±1	±10	-	±1	±10	μA
Digital Input Capacitance, C_{IN}	V_{IN} = 0V	-	5	-	-	5	-	pF
DIGITAL OUTPUTS								
Output Logic High Voltage, V_{OH}	I_{OUT} = -160μA	2.4	4.3	-	2.4	4.3	-	V
Output Logic Low Voltage, V_{OL}	I_{OUT} = 3.2mA	-	0.22	0.4	-	0.22	0.4	V
Output Logic High Current, I_{OH}		-0.160	-6	-	-0.160	-6	-	mA
Output Logic Low Current, I_{OL}		3.2	6	-	3.2	6	-	mA
Output Three-State Leakage Current, I_{OZ}	V_{OUT} = 0V, 5V	-	±1	±10	-	±1	±10	μA
Digital Output Capacitance, C_{OUT}		-	10	-	-	10	-	pF
TIMING CHARACTERISTICS								
Minimum $\overline{CONV}$ Pulse, t1	(Notes 2, 3)	10	-	-	10	-	-	ns
$\overline{CS}$ to $\overline{CONV}$ Setup Time, t2	(Note 2)	10	-	-	10	-	-	ns

4

A/D CONVERTERS

Electrical Specifications AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	HI5800JCD 0°C TO +70°C			HI5800KCD, HI5800BID 0°C TO +70°C -40°C TO +85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CONV}$ to $\overline{CS}$ Setup Time, t3	(Note 2)	0	-	-	0	-	-	ns
Minimum $\overline{OE}$ Pulse, t4	(Notes 2, 4)	15	-	-	15	-	-	ns
$\overline{CS}$ to $\overline{OE}$ Setup Time, t5	(Note 2)	0	-	-	0	-	-	ns
$\overline{OE}$ to $\overline{CS}$ Setup Time, t6	(Note 2)	0	-	-	0	-	-	ns
IRQ Delay from Start Convert, t7	(Note 2)	10	20	25	10	20	25	ns
IRQ Pulse Width, t8	JCD, KCD	190	200	230	190	200	230	ns
	BID	-	-	-	180	195	230	ns
Minimum Cycle Time for Conversion, t9		-	325	333	-	325	333	ns
IRQ to Data Valid Delay, t10	(Note 2)	-5	0	+5	-5	0	+5	ns
Minimum $\overline{A0}$ Pulse, t11	(Notes 2, 4)	10	-	-	10	-	-	ns
Data Access from $\overline{OE}$ Low, t12	(Note 2)	10	18	25	10	18	25	ns
LSB, Nibble Delay from $\overline{A0}$ High, t13	(Note 2)	-	10	20	-	10	20	ns
MSB Delay from $\overline{A0}$ Low, t14	(Note 2)	-	14	20	-	14	20	ns
$\overline{CS}$ to Float Delay, t15	(Note 2)	10	18	25	10	18	25	ns
Minimum $\overline{CS}$ Pulse, t16	(Notes 2, 4)	15	-	-	15	-	-	ns
$\overline{CS}$ to Data Valid Delay, t17	(Note 2)	10	18	25	10	18	25	ns
Output Fall Time, tf	(Note 2)	-	5	20	-	5	20	ns
Output Rise Time, tr	(Note 2)	-	5	20	-	5	20	ns
POWER SUPPLY CHARACTERISTICS								
IV_{CC}		-	170	220	-	170	220	mA
IV_{EE}		-	150	190	-	150	190	mA
IDV_{CC}		-	24	40	-	24	40	mA
IDV_{EE}		-	2	5	-	2	5	mA
Power Dissipation		-	1.7	2.2	-	1.7	2.2	W
PSRR	V_{CC}, V_{EE} ±5%	-	0.01	0.05	-	0.01	0.05	%/%

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Parameter guaranteed by design or characterization and not production tested.
3. Recommended pulse width for $\overline{CONV}$ is 60ns.
4. Recommended minimum pulse width is 25ns.
5. This is the additional current available from the REF_{OUT} pin with the REF_{OUT} pin driving the REF_{IN} pin.
6. The $\overline{A0}$ pin V_{IH} at -40°C may exceed 2.0V by up to 0.4V at initial power up.
7. Excludes error due to internal reference temperature drift.

Timing Diagrams

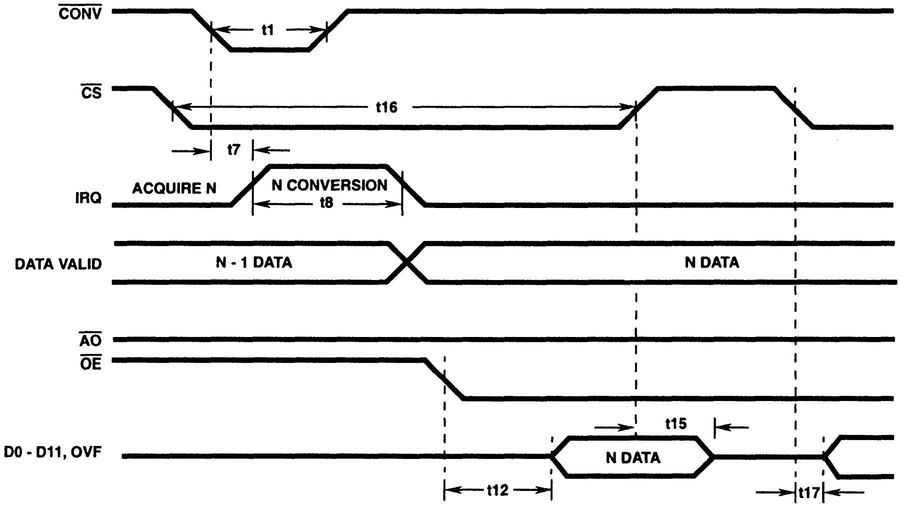


FIGURE 1. SINGLE SHOT TIMING

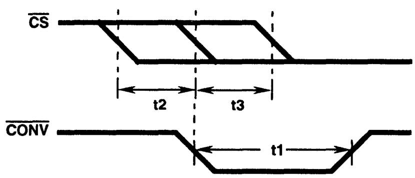


FIGURE 2A. START CONVERSION SETUP TIME

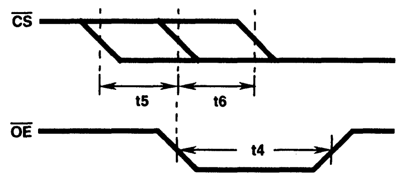


FIGURE 2B. OUTPUT ENABLE SETUP TIME

FIGURE 2.

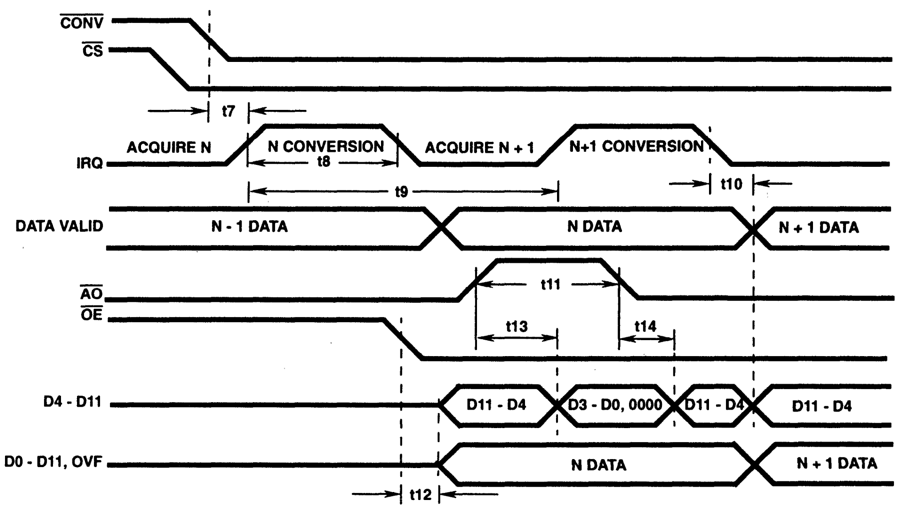


FIGURE 3. CONTINUOUS CONVERSION TIMING

Typical Performance Curves

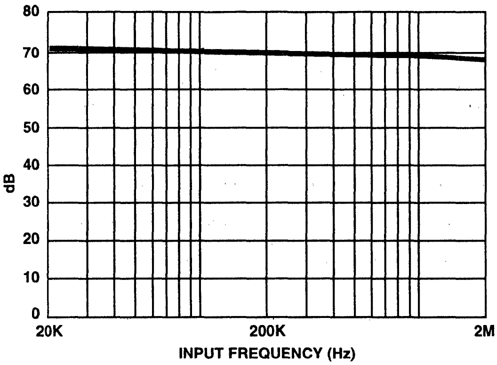


FIGURE 4. TYPICAL SNR vs INPUT FREQUENCY

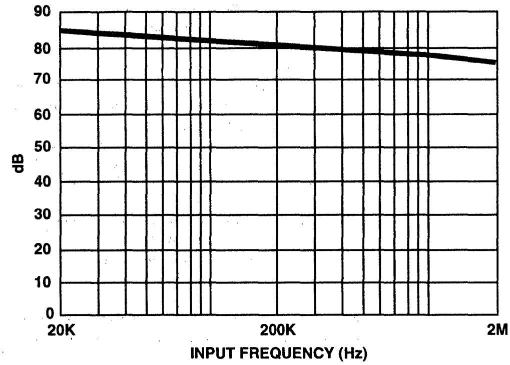


FIGURE 5. TYPICAL THD vs INPUT FREQUENCY

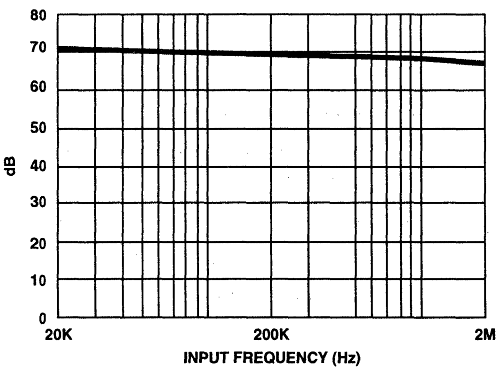


FIGURE 6. TYPICAL SINAD vs INPUT FREQUENCY

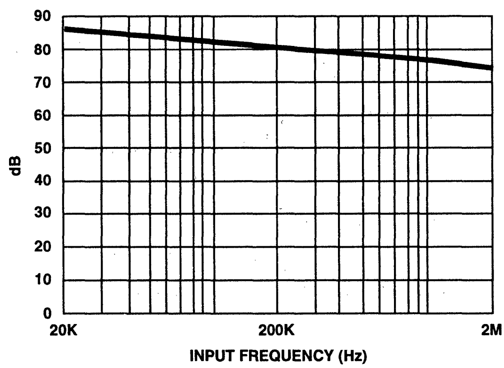


FIGURE 7. TYPICAL SFDR vs INPUT FREQUENCY

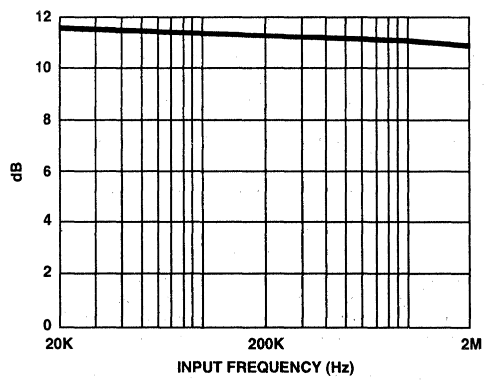


FIGURE 8. TYPICAL EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

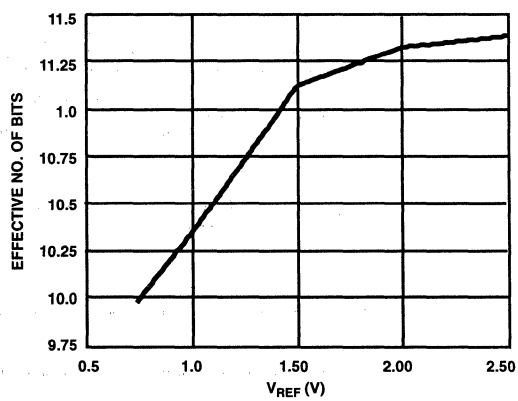


FIGURE 9. EFFECTIVE NUMBER OF BITS vs REFERENCE VOLTAGE (F_S = 3MHz, F_{IN} = 20kHz)

Typical Performance Curves (Continued)

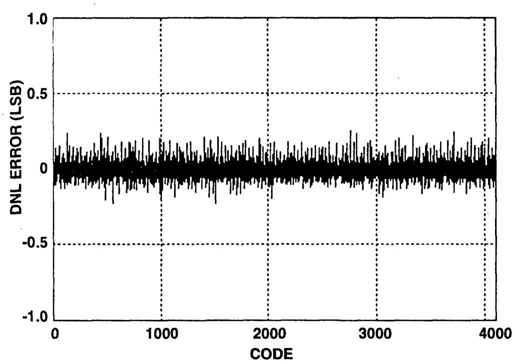


FIGURE 10. DIFFERENTIAL NON-LINEARITY

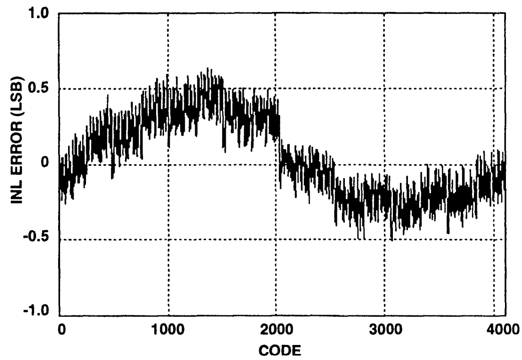


FIGURE 11. INTEGRAL NON-LINEARITY

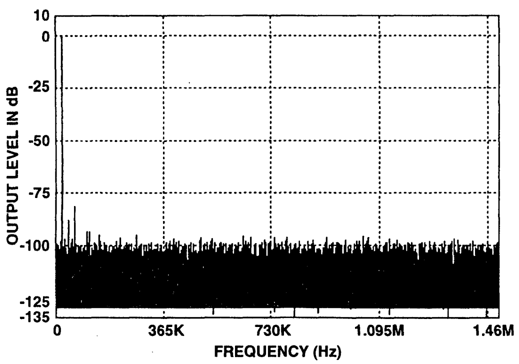


FIGURE 12. FFT SPECTRAL PLOT FOR F_{IN} = 20kHz, F_S = 3MHz

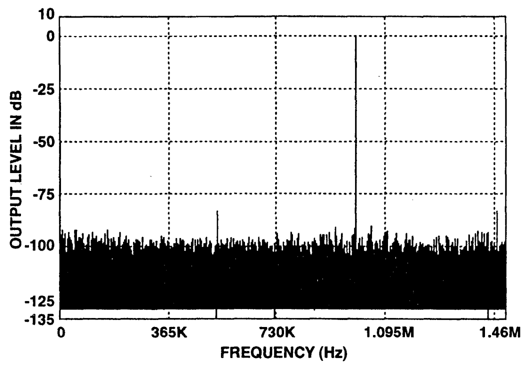


FIGURE 13. FFT SPECTRAL PLOT FOR F_{IN} = 1MHz, F_S = 3MHz

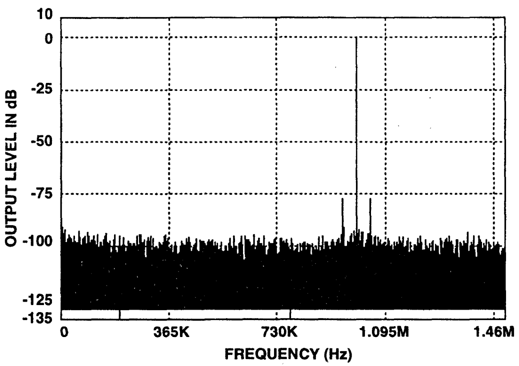


FIGURE 14. FFT SPECTRAL PLOT FOR F_{IN} = 2MHz, F_S = 3MHz

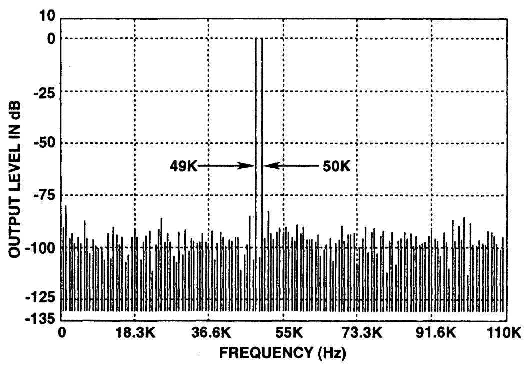


FIGURE 15. INTERMODULATION DISTORTION PLOT FOR F_{IN} = 49kHz, 50kHz at F_S = 3MHz

4

A/D CONVERTERS

Pin Description

PIN #	SYMBOL	PIN DESCRIPTION
1	REF_{IN}	External reference input.
2	RO_{ADJ}	DAC offset adjust (Connect to AGND if not used).
3	RG_{ADJ}	DAC gain adjust (Connect to AGND if not used).
4	AV_{CC}	Analog positive power supply, +5V.
5	REF_{OUT}	Internal reference output, +2.5V.
-	NC	No connection.
6	V_{IN}	Analog input voltage.
7	AGND	Analog ground.
8	ADJ+	Sample/hold offset adjust (Connect to AGND if not used).
9	ADJ-	Sample/hold offset adjust (Connect to AGND if not used).
10	AV_{EE}	Analog negative power supply, -5V.
11	AV_{CC}	Analog positive power supply, +5V.
12	AGND	Analog ground.
13	AV_{EE}	Analog negative power supply, -5V.
14	$\overline{A0}$	Output byte control input, active low. When low, data is presented as a 12-bit word or the upper byte (D11 - D4) in 8-bit mode. When high, the second byte contains the lower LSBs (D3 - D0) with 4 trailing zeroes. See Text.
15	$\overline{CS}$	Chip Select input, active low. Dominates all control inputs.
-	NC	No connection.
16	$\overline{OE}$	Output Enable input, active low.
17	$\overline{CONV}$	Convert start input. Initiates conversion on the falling edge. If held low, continuous conversion mode overrides and remains in effect until the input goes high.
18	DV_{EE}	Digital negative power supply, -5V.
19	DGND	Digital ground.
20	DV_{CC}	Digital positive power supply, +5V.
21	AV_{CC}	Analog positive power supply, +5V.
22	D0	Data bit 0, (LSB).
23	D1	Data bit 1.
24	D2	Data bit 2.
25	D3	Data bit 3.
-	NC	No connection
26	D4	Data bit 4.
27	D5	Data bit 5.
28	D6	Data bit 6.
29	D7	Data bit 7.
30	AV_{EE}	Analog negative power supply, -5V.
31	AGND	Analog ground.
32	DGND	Digital ground.
33	DV_{CC}	Digital positive power supply, +5V.
34	D8	Data bit 8.
35	D9	Data bit 9.
-	NC	No connection.
36	D10	Data bit 10.
37	D11	Data bit 11 (MSB).
38	AV_{CC}	Analog positive power supply, +5V.
39	OVF	Overflow output. Active high when either an overrange or underrange analog input condition is detected.
40	IRQ	Interrupt ReQuest output. Goes low when a conversion is complete.

Description

The HI5800 is a 12-bit two step sampling analog to digital converter which uses a subranging technique with digital error correction. As illustrated in the block diagram, it uses a sample and hold front end, 7-bit R-2R D/A converter which is laser trimmed to 14 bits accuracy, a 7-bit BiCMOS flash converter, precision bandgap reference, digital controller and timing generator, error correction logic, output latches and BiCMOS output drivers.

The falling edge of the convert command signal puts the sample and hold (S/H) in the hold mode and the conversion process begins. At this point the Interrupt Request (IRQ) line is set high indicating that a conversion is in progress. The output of the S/H circuit drives the input of the 7-bit flash converter through a switch. After allowing the flash to settle, the intermediate output of the flash is stored in the latches which feed the D/A and error correction logic. The D/A reconstructs the analog signal and feeds the gain amplifier whose summing node subtracts the held signal of the S/H and amplifies the residue by 32. This signal is then switched to the flash for a second pass using the input switch. The output of the second flash conversion is fed directly to the error correction which reconstructs the twelve bit word from the fourteen bit input. The logic also decodes the overflow bit and the polarity of the overflow. The output of the error correction is then gated through the read controller to the output drivers. The data is ready on the bus as soon as the IRQ line goes low.

I/O Control Inputs

The converter has four active low inputs ($\overline{CS}$, $\overline{CONV}$, $\overline{OE}$ and $\overline{A0}$) and fourteen outputs (D0 - D11, IRQ and OVF). All inputs and outputs are TTL compatible and will also interface to the newer TTL compatible families. All four inputs are CMOS high input impedance stages and all outputs are BiMOS drivers capable of driving 100pF loads.

In order to initiate a conversion or read the data bus, $\overline{CS}$ should be held low. The conversion is initiated by the falling edge of the $\overline{CONV}$ command. The $\overline{OE}$ input controls the output bus directly and is independent of the conversion process. The data on the bus changes just before the IRQ goes low. Therefore if the $\overline{OE}$ line is held low all the time, the data on the bus will change just before the IRQ line goes low. The byte control signal $\overline{A0}$ is also independent of the conversion process and the byte can be manipulated anytime. When $\overline{A0}$ is low the 12-bits and overflow word is read on the bus. The bus can also be hooked up such that the upper byte (D11 - D4) is read when $\overline{A0}$ is low. When $\overline{A0}$ is high, the lower byte (D3 - D0) is output on the same eight pins with trailing zeros.

In order to minimize switching noise during a conversion, byte manipulations done using the $\overline{A0}$ signal should be done in the single shot mode and $\overline{A0}$ should be changed during the acquisition phase. For accuracy, allow sufficient time for settling from any glitches before the next conversion.

Once a conversion is started, the converter will complete the conversion and acquisition periods irrespective of the input states. If during these cycles another convert command is issued, it will be ignored until the acquire phase is complete.

Stand Alone Operation

The converter can be operated in a stand alone configuration with bus inputs controlling the converter. The conversion will be started on the negative edge of the convert ($\overline{CONV}$) pulse as long as this pulse is less than the converter throughput rate. If the converter is given multiple convert commands, it will ignore all but the first command until such time when the acquisition period of the next cycle is complete. At this point it will start a new conversion on the first negative edge of the input command. This allows the converter to be synchronized to a multiple of a faster external clock. The new output data of the conversion is available on the same cycle at the negative edge of the IRQ pulse and is valid until the next negative edge of the IRQ pulse. Data may be accessed at any time during these cycles. It should be noted that if the data bus is kept enabled all the time ($\overline{OE}$ is low), then the data will be updating just before the IRQ goes low. During this time, the data may not be valid for a few nanoseconds.

Continuous Convert Mode

The converter can be operated at its maximum rate by taking the $\overline{CONV}$ line low (supplying the first negative edge) and holding it low. This enables the continuous convert mode. During this time, at the end of the internal acquisition period, the converter automatically starts a new conversion. The data will be valid between the IRQ negative edges.

Note that there is no pipeline delay on the data. The output data is available during the same cycle as the conversion and is valid until the next conversion ends. This allows data access to both previous and present conversions in the same cycle.

When initiating a conversion or a series of conversions, the last signal ($\overline{CS}$ and $\overline{CONV}$) to arrive dominates the function. The same condition holds true for enabling the bus to read the data ($\overline{CS}$ and $\overline{OE}$). To terminate the bus operations, the first signal ($\overline{CS}$ and $\overline{OE}$) to arrive dominates the function.

Interrupt Request Output

The interrupt request line (IRQ) goes high at the start of each conversion and goes low to indicate the start of the acquisition. During the time that IRQ is high, the internal sample and hold is in hold mode. At the termination of IRQ, the sample and hold switches to acquire mode which lasts approximately 100ns. If no convert command is issued for a period of time, the sample and hold simply remains in acquire mode tracking the analog input signal until the next conversion cycle is initiated. The IRQ line is the only output that is not three-stateable.

Analog Input, V_{IN}

The analog input of the HI5800 is coupled into the input stage of the Sample and Hold amplifier. The input is a high impedance bipolar differential pair complete with an ESD protection circuit. Typically it has >3MΩ input impedance. With this high input impedance circuit, the HI5800 is easily interfaced to any type of op amp without a requirement for a high drive capability. Adequate precautions should be taken while driving the input from high voltage output op amps to ensure that the analog input pin is not overdriven above the specified maximum limits. For a +2.5V reference, the analog input range is ±2.5V. This input range scales with the value of the external reference voltage if the internal reference is not used. For best performance, the analog ground pin next to the analog input should be utilized for signal return.

Figures 4 and 5 illustrate the use of an input buffer as a level shifter to convert a unipolar signal to the bipolar input used by the HI5800. Figure 4 is an example of a non-inverting buffer that takes a 0 to 2.5V input and shifts it to ±2.5V. The gain can be calculated from

$$V_{OUT} = \left[1 + \frac{R_2}{(R_1 \| R_3)}\right] \times V_{IN} - \left[\frac{R_1}{R_1 + R_3}\right] \times V_{OFFSET}$$

$$R_1 \| R_3 = \frac{R_1 R_3}{R_1 + R_3}$$

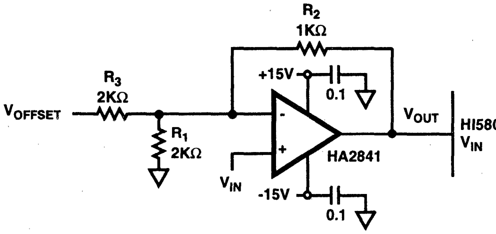


FIGURE 4. NON-INVERTING BUFFER

Figure 5 is an example of an inverting buffer that level shifts a 0V to 5V input to ±2.5V. Its gain can be calculated from

$$V_{OUT} = (-R_2/R_1) \times V_{IN} - (R_2/R_3) \times V_{OFFSET}$$

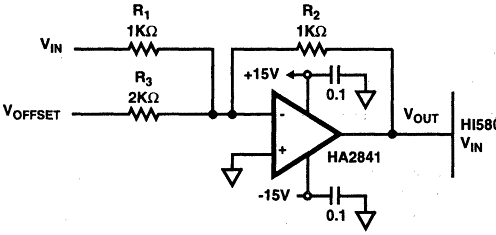


FIGURE 5. INVERTING BUFFER

Note that the correct op amp must be chosen in order to not degrade the overall dynamic performance of the circuit. Recommended op amps are called out in the figures.

Voltage Reference, REF_{OUT}

The HI5800 has a curvature corrected internal band-gap reference generator with a buffer amplifier capable of driving up to 15mA. The band-gap and amplifier are trimmed to give +2.50V. When connected to the reference input pin REF_{IN}, the reference is capable of driving up to 2mA externally. Further loading may degrade the performance of the output voltage. It is recommended that the output of the reference be decoupled with good quality capacitors to reduce the high-frequency noise.

Reference Input, REF_{IN}

The converter requires a voltage reference connected to the REF_{IN} pin. This can be the above internal reference or it can be an external reference. It is recommended that adequate high frequency decoupling is provided at the reference input pin in order to minimize overall converter noise.

A user trying to provide an external reference to a HI5800 is faced with two problems. First, the drift of the reference over temperature must be very low. Second, it must be capable of driving the 200Ω input impedance seen at the REF_{IN} pin of the HI5800. Figure 6 is a recommended circuit for doing this that is capable of 2ppm/°C drift over temperature.

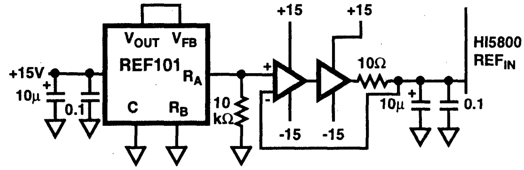


FIGURE 6. EXTERNAL REFERENCE

Supply and Ground Considerations

The HI5800 has separate analog and digital supply and ground pins to help keep digital noise out of the analog signal path. For the best performance, the part should be mounted on a board that provides separate low impedance planes for the analog and digital supplies and grounds. Only connect the two grounds together at one place preferably as close as possible to the part. The supplies should be driven by clean linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the HI5800.

If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the Application Note "Using Harris High Speed A/D Converters" (AN9214) for additional suggestions to consider when using the HI5800.

Error Adjustments

For most applications the accuracy of the HI5800 is sufficient without any adjustments. In applications where accuracy is of utmost importance three external adjustments are possible: S/H offset, D/A offset and D/A gain. Figure 7 illustrates the use of external potentiometers to reduce the HI5800 errors to zero.

The D/A offset (RO_{ADJ}) and S/H offset (ADJ+ and ADJ-) trims adjust the voltage offset of the transfer curve while the D/A gain trim (RG_{ADJ}) adjusts the tilt of the transfer curve around the curve midpoint (code 2048). The 10kΩ potentiometers can be installed to achieve the desired adjustment in the following manner.

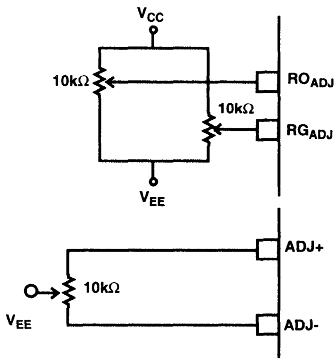


FIGURE 7. D/A OFFSET, D/A GAIN AND S/H OFFSET ADJUSTMENTS

Typically only one of the offset trimpots needs to be used. The offset should first be adjusted to get code 2048 centered at a desired DC input voltage such as zero volts. Next the gain trim can be adjusted by trimming the gain pot until the 4094 to 4095 code transition occurs at the desired voltage (2.500V - 1.5 LSBs for a 2.5V reference). The gain trim can also be done by adjusting the gain pot until the code 0 to 1 transition occurs at a particular voltage (-2.5V + 0.5 LSBs for a 2.5V reference). If a nonzero offset is needed, then the offset pot can be adjusted after the gain trim is finished. The gain trim is simplified if an offset trim to zero is done first with a nonzero offset trim done after the gain trim is finished. The D/A offset and S/H offset trimpots have an identical effect on the converter except that the S/H offset is a finer resolution trim. The D/A offset and D/A gain typically have an adjustment range of ±30 LSBs and the S/H offset typically has an adjustment range of ±20 LSBs.

TABLE 2. I/O TRUTH TABLE

INPUTS				OUTPUT	
CS	CONV	OE	A0	IRQ	FUNCTION
1	X	X	X	X	No operation.
0	0	X	X	X	Continuous convert mode.
0	X	0	0	X	Outputs all 12-bits and OVF or upper byte D11 - D4 in 8 bit mode.
0	X	0	1	X	In 8-bit mode, outputs lower LSBs D3 - D0 followed by 4 trailing zeroes and OVF, (See text).
0	1	X	X	0	Converter is in acquisition mode.
0	X	X	X	1	Converter is busy doing a conversion.
0	X	1	X	X	Data outputs and OVF in high impedance state.

X's = Don't Care

TABLE 3. A/D OUTPUT CODE TABLE

CODE DESCRIPTION $LSB = \frac{2\,(REF_{IN})}{4096}$	(NOTE 1) INPUT VOLTAGE $REF_{IN} = 2.5V$ (V)	OUTPUT DATA (OFFSET BINARY)	MSB											LSB
		OVF	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
≥+FS	≥ +2.5000	1	1	1	1	1	1	1	1	1	1	1	1	1
+FS - 1LSB	+2.49878	0	1	1	1	1	1	1	1	1	1	1	1	1
+3/4FS	+1.8750	0	1	1	1	0	0	0	0	0	0	0	0	0
+1/2FS	+1.2500	0	1	1	0	0	0	0	0	0	0	0	0	0
+1LSB	+0.00122	0	1	0	0	0	0	0	0	0	0	0	0	1
0	0.0000	0	1	0	0	0	0	0	0	0	0	0	0	0
-1 LSB	-0.00122	0	0	1	1	1	1	1	1	1	1	1	1	1
-1/2FS	-1.2500	0	0	1	0	0	0	0	0	0	0	0	0	0
-3/4FS	-1.8750	0	0	0	1	0	0	0	0	0	0	0	0	0
-FS + 1LSB	-2.49878	0	0	0	0	0	0	0	0	0	0	0	0	1
≤-FS	≤ -2.5000	1	0	0	0	0	0	0	0	0	0	0	0	0

NOTE:

1. The voltages listed above represent the ideal center of each output code shown as a function of the reference voltage.

If no external adjustments are required the following pins should be connected to analog ground (AGND) for optimum performance: RO_{ADJ}, RG_{ADJ}, ADJ+, and ADJ-.

Typical Application Schematic

A typical application schematic diagram for the HI5800 is shown with the block diagram. The adjust pins are shown with 10kΩ potentiometers used for gain and offset adjustments. These potentiometers may be left out and the respective pins should be connected to ground for best untrimmed performance.

Definitions

Static Performance Definitions

Offset, fullscale, and gain all use a measured value of the internal voltage reference to determine the ideal plus and minus fullscale values. The results are all displayed in LSB's.

Offset Error (VOS)

The first code transition should occur at a level $^1/_2$ LSB above the negative fullscale. Offset is defined as the deviation of the actual code transition from this point. Note that this is adjustable to zero.

Fullscale Error (FSE)

The last code transition should occur for a analog input that is $1^1/_2$ LSBs below positive fullscale. Fullscale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed for no missing codes over all temperature ranges.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection (PSRR)

Each of the power supplies are moved plus and minus 5% and the shift in the offset and fullscale error is noted. The number reported is the percent change in these parameters versus fullscale divided by the percent change in the supply.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5800. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from fullscale for all these tests. Distortion results are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$$

where: $V_{CORR} = 0.5dB$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f1 and f2, are present on the inputs. The ratio of the measured signal to the distortion terms is calculated. The IMD products used to calculate the total distortion are (f2-f1), (f2+f1), (2f1-f2), (2f1+f2), (2f2-f1), (2f2+f1), (3f1-f2), (3f1+f2), (3f2-f1), (3f2+f1), (2f2-2f1), (2f2+2f1), (2f1), (2f2), (2f1), (2f2), (4f1), (4f2). The data reflects the sum of all the IMD products.

Full Power Input Bandwidth

Full power input bandwidth is the frequency at which the amplitude of the fundamental of the digital output word has decreased 3dB below the amplitude of an input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Die Characteristics

DIE DIMENSIONS:
202 x 283 x 19 ± 1mils

METALLIZATION:
Metal 1: Type: AlSiCu, Thickness: 6KÅ +1500A/-750Å
Metal 1: Type: AlSiCu, Thickness: 16KÅ +2500A/-1100Å

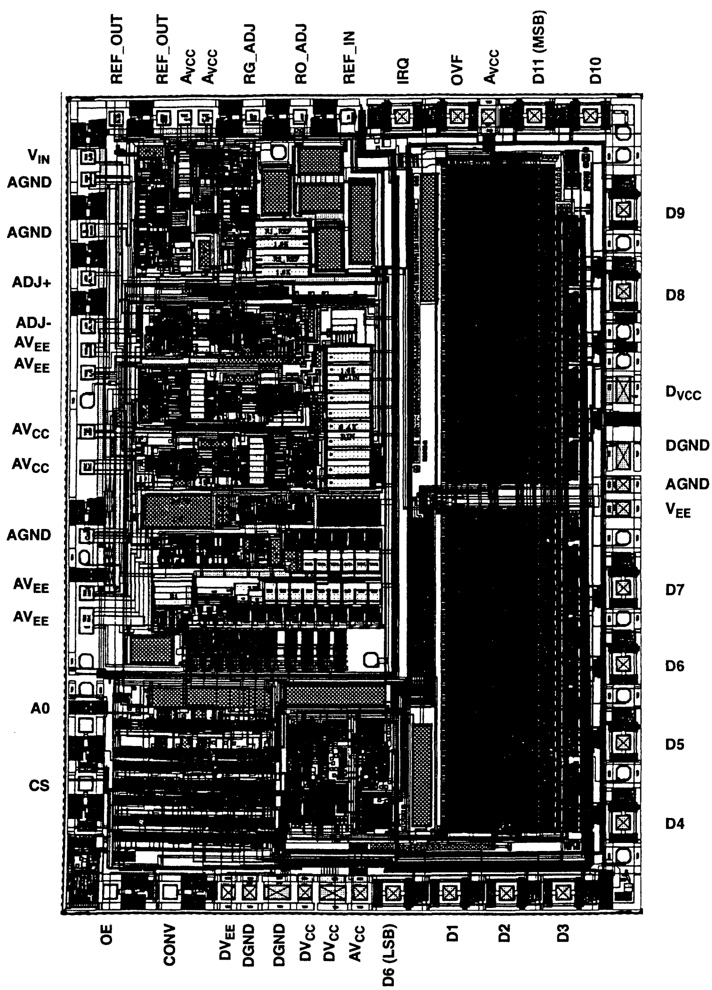
GLASSIVATION:
Type: Sandwich Passivation - Nitride + Undoped Si Glass (USG)
Thickness: Nitride - 4KÅ, USG - 8KÅ, Total - 12KÅ ±2KÅ

TRANSISTOR COUNT: 10K

SUBSTRATE POTENTIAL (Powered Up): V_{EE}

Metallization Mask Layout

HI5800



4 A/D CONVERTERS

HARRIS SEMICONDUCTOR

HI5805

PRELIMINARY

June 1995

12-Bit, 5 MSPS A/D Converter

Features

- 5 MSPS Sampling Rate
- Low Power
- Internal Sample and Hold
- Fully Differential Architecture
- 100MHz Full Power Input Bandwidth
- HI5805E Extends the FPIBW to >300MHz
- Low Distortion
- Internal Reference
- TTL/CMOS Compatible Digital I/O
- 5V or 3.0V Digital Outputs

Applications

- Digital Communication Systems
- Undersampling Digital IF
- Document Scanners

Description

The HI5805 is a monolithic, 12-bit, Analog-to-Digital Converter fabricated in Harris' HBC10 BiCMOS process. It is designed for high speed, high resolution applications where wide bandwidth and low power consumption are essential.

The HI5805 is designed in a fully differential pipelined architecture with a front end differential-in-differential-out sample-and-hold (S/H). The HI5805 has excellent dynamic performance while consuming 300mW power at 5 MSPS.

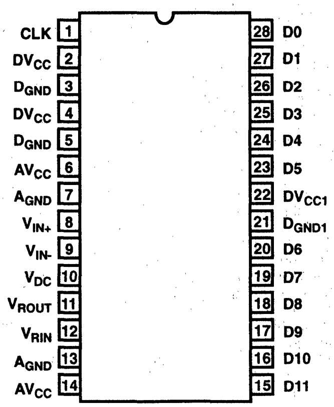
The 100MHz full power input bandwidth is ideal for communication systems and document scanner applications. Data output latches are provided which present valid data to the output bus with a latency of 3 clock cycles. The digital outputs have a separate supply pin which can be powered from a 3.0V to 5.0V supply.

Ordering Information

PART NUMBER	SAMPLE RATE	TEMPERATURE RANGE	PACKAGE
HI5805BIB	5 MSPS	-40°C to +85°C	28 Lead Plastic SOIC (W)

Pinout

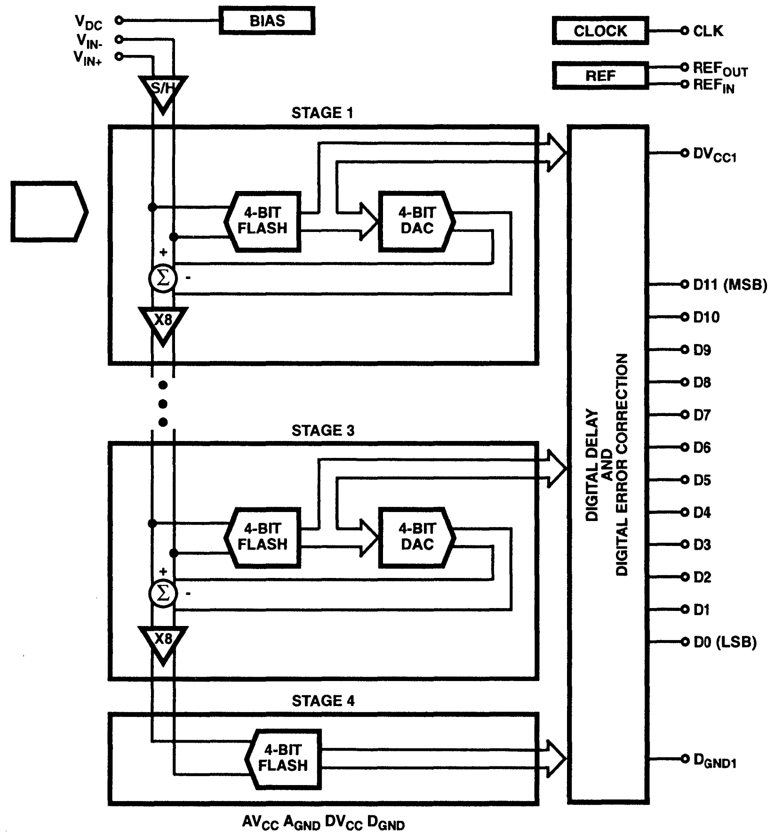
28 LEAD SOIC
TOP VIEW



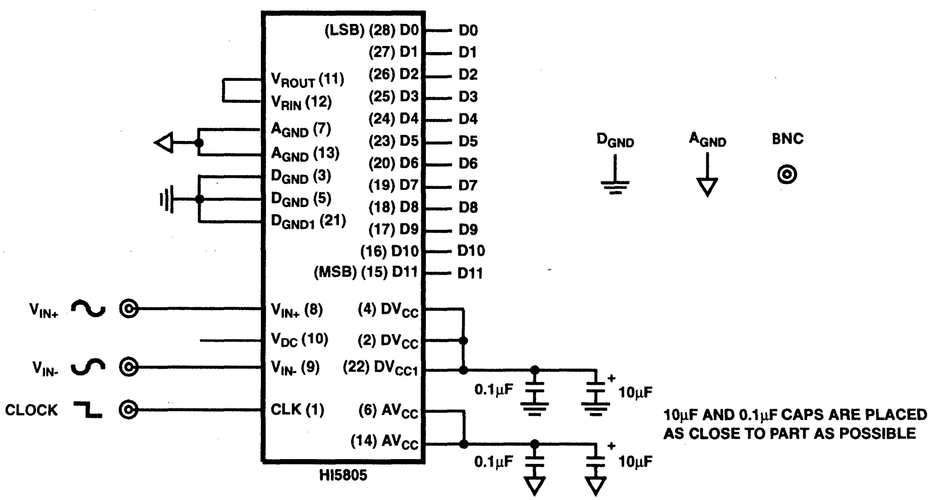
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3984**

Functional Block Diagram



Typical Applications Schematic



Absolute Maximum Ratings

Supply Voltage, AV_{CC} or DV_{CC} to A_{GND} or D_{GND} . . . . +6.0V
D_{GND} to A_{GND} 0.3V
Digital I/O Pins . . . . D_{GND} to DV_{CC}
Analog I/O Pins. . . . . A_{GND} to AV_{CC}
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . +300°C
(Lead Tips Only)

Thermal Information

Thermal Resistance θ_{JA}
HI5805BIB . . . . 75°C/W
Maximum Junction Temperature . . . . +150°C
Operating Temperature Range
HI5805BIB . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$AV_{CC} = DV_{CC} = DV_{CC1} = +5.0V$, $F_S = 5$ MSPS at 50% Duty Cycle, $V_{RIN} = 3.5V$, $C_L = 10pF$, $T_A = -40^oC$ to $+85^oC$, Unless Otherwise Specified

PARAMETER	TEST CONDITION	HI5805BIB -40°C to +85°C MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		12	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±1	±2	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1	LSB
Offset Error, V_{OS}	f_{IN} = DC	-	TBD	-	LSB
Full Scale Error, FSE	f_{IN} = DC	-	TBD	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	-	MSPS
Maximum Conversion Rate	No Missing Codes	5	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 1MHz	-	11	-	Bits
	f_{IN} = 2MHz	-	TBD	-	Bits
Signal to Noise Ratio, SNR	f_{IN} = 1MHz	-	TBD	-	dB
$= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 2MHz	-	TBD	-	dB
Signal to Noise Ratio, SINAD	f_{IN} = 1MHz	-	68	-	dB
$= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 2MHz	-	TBD	-	dB
Total Harmonic Distortion, THD	f_{IN} = 1MHz	-	TBD	-	dBc
	f_{IN} = 2MHz	-	TBD	-	dBc
2nd Harmonic Distortion	f_{IN} = 1MHz	-	TBD		dBc
	f_{IN} = 2MHz	-	TBD	-	dBc
3rd Harmonic Distortion	f_{IN} = 1MHz	-	TBD	-	dBc
	f_{IN} = 2MHz	-	TBD	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 1MHz	-	-69	-	dBc
	f_{IN} = 2MHz	-	-67	-	dBc
Intermodulation Distortion, IMD	f1 = 1MHz, f2 = 1.02MHz	-	-68	-	dBc
Transient Response		-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive	-	2	-	Cycle
ANALOG INPUT					
Analog Input Resistance, R_{IN}	(Notes 1, 2)	1	-	-	MΩ
Analog Input Capacitance, C_{IN}		1	10	-	pF
Analog Input Bias Current, I_B		-50	-	+50	µA
Full Power Input Bandwidth (FPIBW)		-	100	-	MHz
Analog Input Common Mode Range (V_{IN}+ + V_{IN}-)/2	Differential Mode (Note 1)	1	2.3	4	V

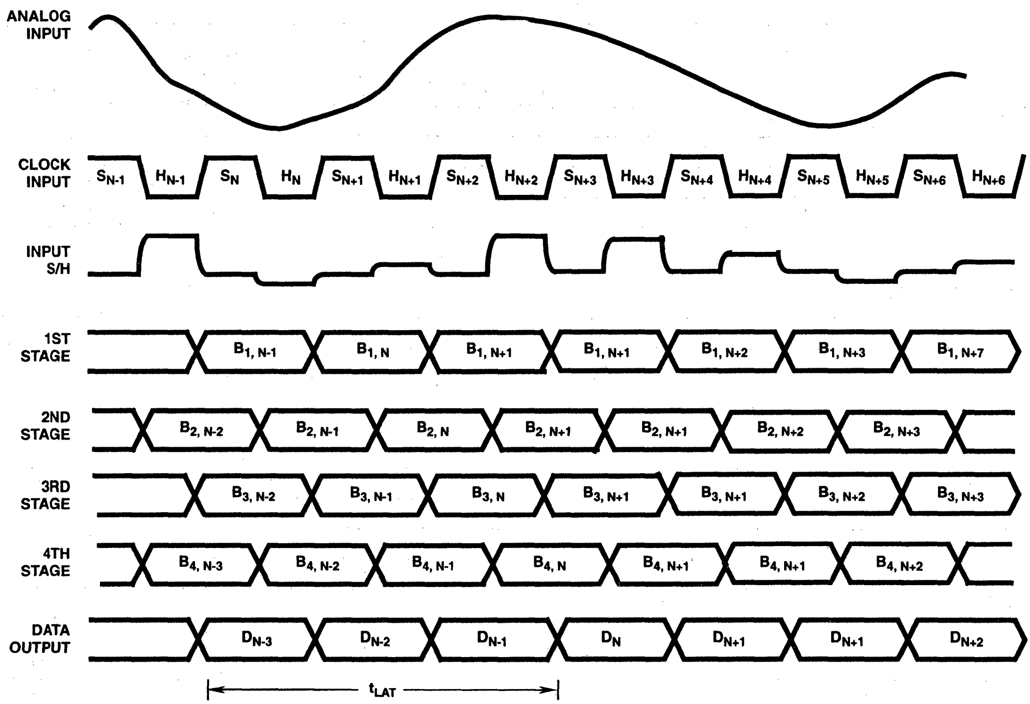
Electrical Specifications $AV_{CC} = DV_{CC} = DV_{CC1} = +5.0V$, $F_S = 5$ MSPS at 50% Duty Cycle, $V_{RIN} = 3.5V$, $C_L = 10pF$, $T_A = -40^oC$ to $+85^oC$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	HI5805BIB -40°C to +85°C MIN	TYP	MAX	UNITS
INTERNAL VOLTAGE REFERENCE					
Reference Output Voltage, REF_{OUT} (Loaded)		-	3.5	-	V
Reference Output Current		-	TBD	-	mA
Reference Temperature Coefficient		-	TBD	-	ppm/°C
REFERENCE INPUT					
Total Reference Resistance, R_L		-	7.8	-	kΩ
Reference Current		-	450	-	μA
DC OUTPUT VOLTAGE					
DC Voltage Output, V_{DC}		-	2.3	-	V
Max Output Current		-	-	1	mA
DIGITAL INPUTS (CLK)					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic High Current, I_{IH}	$V_{CLK} = 5V$	-	-	10.0	μA
Input Logic Low Current, I_{IL}	$V_{CLK} = 0V$	-	-	10.0	μA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS (D0-D11)					
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$	1.6	-	-	mA
	$DV_{CC1} = 3.0V$, $V_O = 0.4V$	-	1.6	-	mA
Output Logic Source Current, I_{OH}	$V_O = 2.4V$	-0.2	-	-	mA
	$DV_{CC1} = 3.0V$, $V_O = 2.4V$	-	-0.2	-	mA
Output Capacitance, C_{OUT}		-	5	-	pF
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps
Data Output Delay, t_{OD}		-	TBD	-	ns
Data Output Hold, t_H		-	TBD	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 1)	-	-	3	Cycles
Clock Pulse Width (Low)	5MHz Clock	95	100	105	ns
Clock Pulse Width (High)	5MHz Clock	95	100	105	ns
POWER SUPPLY CHARACTERISTICS					
Total Supply Current, I_{CC}	$V_{IN}+ = V_{IN}- = V_{DC}$	-	60	70	mA
Analog Supply Current, AI_{CC}	$V_{IN}+ = V_{IN}- = V_{DC}$	-	46	-	mA
Digital Supply Current, DI_{CC}	$V_{IN}+ = V_{IN}- = V_{DC}$	-	13	-	mA
Output Supply Current, DI_{CC1}	$V_{IN}+ = V_{IN}- = V_{DC}$	-	1	-	mA
Power Dissipation	$V_{IN}+ = V_{IN}- = V_{DC}$	-	300	350	mW
Offset Error PSRR, ΔV_{OS}	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	TBD	-	LSB
Gain Error PSRR, ΔFSE	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	TBD	-	LSB

NOTES:

1. Parameter guaranteed by design or characterization and not production tested.
2. With the clock off (clock low, hold mode).

Timing Waveforms



NOTES:
1. S_N: N-th sampling period.
2. H_N: N-th holding period.
3. $B_{M,N}$: M-th stage digital output corresponding to N-th sampled input.
4. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. INTERNAL CIRCUIT TIMING

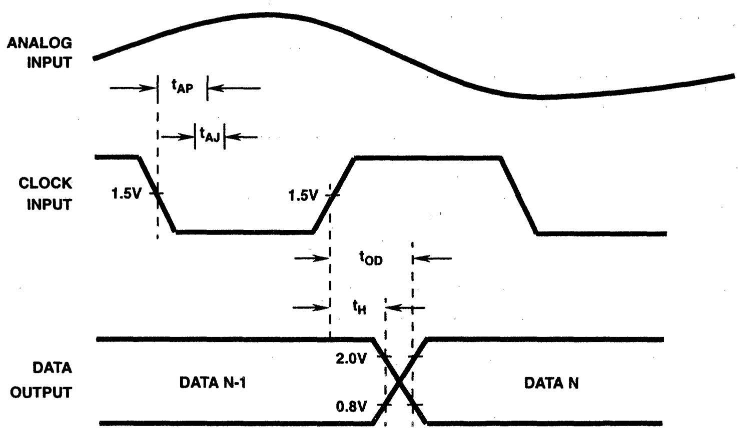


FIGURE 2. INPUT-TO-OUTPUT TIMING

Pin Description

PIN #	NAME	DESCRIPTION
1	CLK	Input Clock
2	DV_{CC}	Digital Supply
3	D_{GND}	Digital Ground
4	DV_{CC}	Digital Supply
5	D_{GND}	Digital Ground
6	AV_{CC}	Analog Supply
7	A_{GND}	Analog Ground
8	V_{IN+}	Positive Analog Input
9	V_{IN-}	Negative Analog Input
10	V_{DC}	DC Output
11	V_{ROUT}	Reference Output
12	V_{RIN}	Reference Input
13	A_{GND}	Analog Ground
14	AV_{CC}	Analog Supply
15	D11	Data Bit 11 Output (MSB)
16	D10	Data Bit 10 Output
17	D9	Data Bit 9 Output
18	D8	Data Bit 8 Output
19	D7	Data Bit 7 Output
20	D6	Data Bit 6 Output
21	D_{GND1}	Output Digital Ground
22	DV_{CC1}	Output Digital Supply
23	D5	Data Bit 5 Output
24	D4	Data Bit 4 Output
25	D3	Data Bit 3 Output
26	D2	Data Bit 2 Output
27	D1	Data Bit 1 Output
28	D0	Data Bit 0 Output (LSB)

Detailed Description

Theory of Operation

The HI5805 is a 12-bit fully differential sampling pipeline A/D converter with digital error correction. Figure 3 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The small values of these components result in a typical full power input bandwidth of 100MHz.

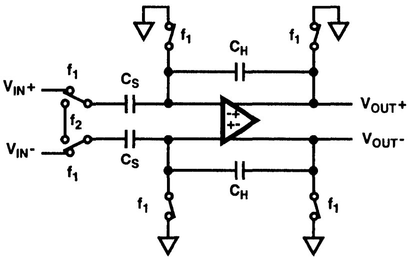


FIGURE 3. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figure 1, three identical pipeline subconverter stages, each containing a four-bit flash converter, a four-bit digital-to-analog converter and an amplifier with a voltage gain of 8, follow the S/H circuit with the fourth stage being only a 4-bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual sub-converter clock signal is offset by 180 degrees from the previous stage clock signal, with the result that alternate stages in the pipeline will perform the same operation.

The 4-bit digital output of each stage is fed to a digital delay line controlled by the internal clock. The purpose of the delay line is to align the digital output data to the corresponding sampled analog input signal. This delayed data is fed to the digital error correction circuit which corrects the error in the output data with the information contained in the redundant bits to form the final 12-bit output for the converter.

Because of the pipeline nature of this converter, the data on the bus is output at the 3rd cycle of the clock after the analog sample is taken. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The output data is synchronized to the external clock by a latch. The digital outputs are in offset binary format (See Table 1).

Reference Generator, V_{ROUT} and V_{RIN}

The HI5805 has an internal reference generator, therefore, no external reference voltage is required. V_{ROUT} must be connected to V_{RIN} when using the internal reference.

The HI5805 can be used with an external reference. The converter requires only one external reference voltage connected to the V_{RIN} pin with V_{ROUT} left open.

The HI5805 is tested with V_{RIN} equal to 3.5V. Internal to the converter, two reference voltages of 1.3V and 3.3V are generated for a fully differential input signal range of $\pm$2V.

In order to minimize overall converter noise, it is recommended that adequate high frequency decoupling be provided at the reference input pin, V_{RIN}.

TABLE 1. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE † (USING INTERNAL REFERENCE)	OFFSET BINARY OUTPUT CODE											
		MSB											LSB
		D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale(+FS) - 1/4 LSB	+1.99976V	1	1	1	1	1	1	1	1	1	1	1	1
+FS - 1 1/4 LSB	1.99878V	1	1	1	1	1	1	1	1	1	1	1	0
+ 3/4 LSB	732.4μV	1	0	0	0	0	0	0	0	0	0	0	0
- 1/4 LSB	-244.1μV	0	1	1	1	1	1	1	1	1	1	1	1
-FS + 1 3/4 LSB	-1.99829V	0	0	0	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + 3/4 LSB	-1.99927V	0	0	0	0	0	0	0	0	0	0	0	0

† The voltages listed above represent the ideal center of each offset binary output code shown as a function of the reference voltage.

Analog Input, Differential Connection

The analog input to the HI5805 can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 4) will give the best performance for the converter.

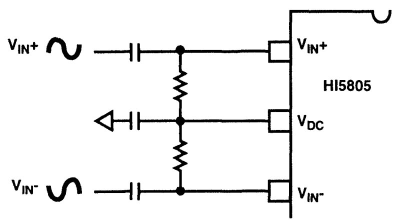


FIGURE 4. AC COUPLED DIFFERENTIAL INPUT

Since the HI5805 is powered off a single +5V supply, the analog input must be biased so it lies within the input common mode range of 1.0V to 4.0V. The performance of the ADC does not change significantly with the value of the common mode voltage.

A 2.3V DC voltage source, V_{DC}, half way between the top and bottom internal reference voltages, is made available to the user to help simplify circuit design when using a differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent bias source and stays within the common mode range over temperature. It has a temperature coefficient of about 200ppm.

The difference between the two internal voltage references is 2V. If V_{IN} is a $2V_{P-P}$ sinewave riding on a common mode voltage equal to V_{DC}, the converter will be at positive full scale when the $V_{IN}+$ input is at V_{DC} + 1V and $V_{IN}-$ is at V_{DC} - 1V ($V_{IN}+$ - $V_{IN}-$ = 2V). Conversely, the ADC will be at negative full scale when the $V_{IN}+$ input is equal to V_{DC} - 1V and $V_{IN}-$ is at V_{DC} + 1V ($V_{IN}+$ - $V_{IN}-$ = -2V).

Analog Input, Single-Ended Connection

The configuration shown in Figure 5 may be used with a single ended AC coupled input. Sufficient headroom must be provided such that the input voltage never goes above +5V or below A_{GND}.

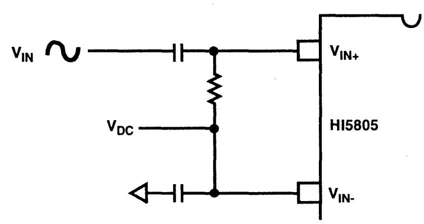


FIGURE 5. AC COUPLED SINGLE ENDED INPUT

Again, the difference between the two internal voltage references is 2V. If V_{IN} is a $4V_{P-P}$ sinewave riding on a positive voltage equal to V_{DC}, the converter will be at positive full scale when V_{IN} is at V_{DC} + 2V and will be at negative full scale when V_{IN} is equal to V_{DC} - 2V. In this case, V_{DC} could range between 2V and 3V without a significant change in ADC performance.

A single ended source will give better overall system performance if it is first converted to differential before driving the HI5805.

Digital I/O and Clock Requirements

The HI5805 provides a standard high-speed interface to external TTL/CMOS logic families. The digital CMOS clock input has TTL level thresholds. The low input bias current allows the HI5805 to be driven by CMOS logic.

The digital CMOS outputs have a separate digital supply. This allows the digital outputs to operate from a 3.0V to 5.0V supply. When driving CMOS logic, the digital outputs will swing to the rails. When driving standard TTL loads, the digital outputs will meet standard TTL level requirements even with a 3.0V supply.

In order to ensure rated performance of the HI5805, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5805 will only be guaranteed at conversion rates above 0.5 MSPS. This ensures proper performance of the internal dynamic circuits.

Supply and Ground Considerations

The HI5805 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5805 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the Application Note AN9214, "Using Harris High Speed A/D Converters" for additional considerations when using high speed converters.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level 1/4 LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is 3/4 LSB's below positive full-scale with the offset error removed. Full-scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection Ratio (PSRR)

Each of the power supplies are moved plus and minus 5% and the shift in the offset and gain error (in LSB's) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5805. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from full-scale for all these tests. SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency, excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by:

$$ENOB = (SINAD + V_{CORR} - 1.76)/6.02$$

where: V_{CORR} = 0.5dB

V_{CORR} adjusts the ENOB for the amount the input is below fullscale.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present on the inputs. The ratio of the measured distortion terms to the signal is calculated. The terms included in the calculation are $(f_1 + f_2)$, $(f_1 - f_2)$, $(2f_1)$, $(2f_2)$, $(2f_1 + f_2)$, $(2f_1 - f_2)$, $(f_1 + 2f_2)$, $(f_1 - 2f_2)$. The ADC is tested with each tone 6dB below full scale.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component in the spectrum below fs/2.

Transient Response

Transient response is measured by providing a fullscale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 12-bit accuracy.

Over-Voltage Recovery

Over-voltage Recovery is measured by providing a fullscale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 12-bit accuracy.

Full Power Input Bandwidth (FPIBW)

Full power input bandwidth is the frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has a peak-to-peak amplitude equal to the difference between the two internal voltage references. The bandwidth given is measured at the specified sampling frequency.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AD})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

This is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the data is output on the bus after the third cycle of the clock. This is due to the pipeline nature of the converter where the data has to ripple through the stages. This delay is specified as the data latency. After the data latency time, the data representing each succeeding sample is output at the following clock pulse. The digital data lags the analog input by 3 cycles.

HARRIS SEMICONDUCTOR

HI7188

PRELIMINARY

July 1995

8-Channel, 16-Bit High Precision Sigma-Delta A/D Converter Sub-System

Features

- 16-Bit Resolution with No Missing Codes
- 0.0015% Integral Non-Linearity
- On Chip 8 Channel Multiplexer
- 20mV to 2.5V Full Scale Input Ranges
- Low Power Dissipation; 40mW (Max)
- Internal PGIA with Gains of 1 to 8
- Serial Data I/O Interface, SPI Compatible
- Differential Analog and Reference Inputs
- System Calibration
- -120dB Rejection of 60/50Hz Line Noise

Applications

- Multi-Channel Process Controls
- Multi-Channel Industrial Controls
- Weight Scales
- Medical Patient Monitoring
- Laboratory Instrumentation

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI7188IP	-40°C to +85°C	40 Lead Plastic DIP
HI7188IN	-40°C to +85°C	44 Lead MQFP

Additional Reference Documents

- AN9504 “A Brief Introduction to Sigma Delta Conversion”
- TB329 “Harris Sigma-Delta Calibration Techniques”

Description

The Harris HI7188 is a monolithic 8-channel sigma-delta instrumentation A/D converter suitable for physical and electrical measurements in scientific, medical, and industrial applications where the input frequency is below 25Hz. The signal and reference inputs are fully differential for maximum flexibility and performance. An internal Programmable Gain Instrumentation Amplifier (PGIA) provides input gains of 1, 2, 4, and 8.

The output data rate of the HI7188 is 240 or 200 conversions per second per channel when used in the 60 or 50Hz line rejection modes respectively. While operating from 5V power supplies the digital filter provides over 120dB of 60/50Hz noise rejection. If line noise rejection is not required, the HI7188 can operate at higher speeds.

The HI7188 supports continuous conversion on any number of channels (up to 8) with both the number of channels to be converted and the order they are to be converted controlled by the user. System offset and gain calibration modes compensate for offset and gain errors due to drifts that may occur over time and temperature.

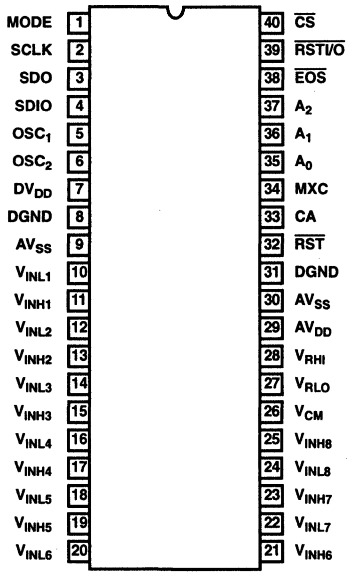
The HI7188 contains a serial I/O port, and is compatible with most synchronous transfer formats, including both the Motorola/Harris 6805/11 series SPI and Intel 8051 series SSR protocols. A sophisticated set of commands gives the user control over calibration, PGIA gain, and bipolar/unipolar modes on a per channel basis. Number of channels to convert, data coding, line noise rejection, etc. can be programmed at the chip level. The on-chip calibration registers allow the user to read and write calibration data.

4

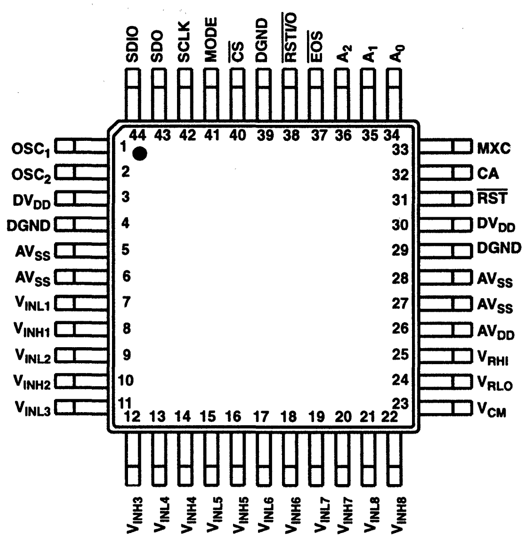
A/D CONVERTERS

Pinouts

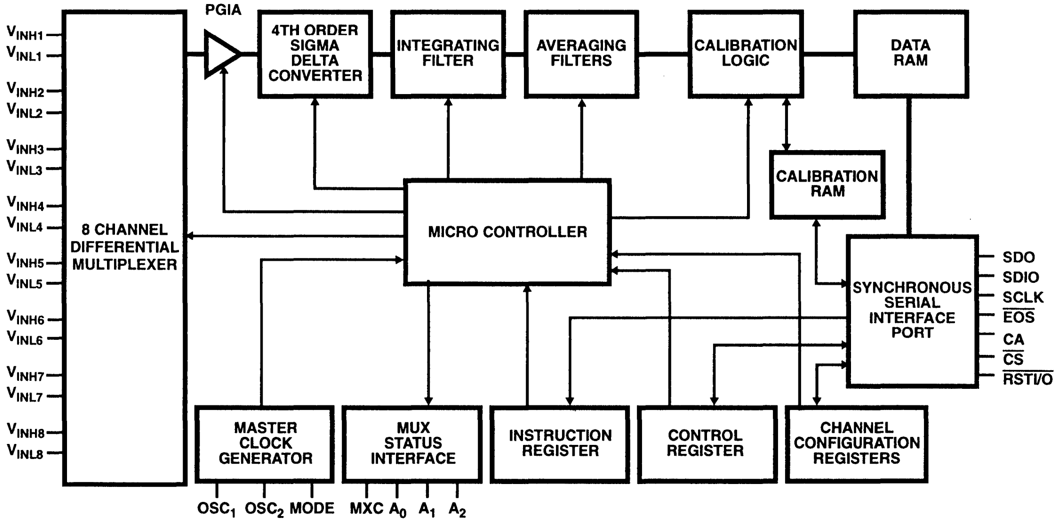
HI7188 (PDIP)
TOP VIEW



HI7188 (MQFP)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage
AV_{DD} to AGND . . . . . +5.5V
AV_{SS} to AGND . . . . . -5.5V
DV_{DD} to DGND . . . . . +5.5V
DGND to AGND . . . . . ±0.3V
Analog Input Pins . . . . . AV_{SS} to AV_{DD}
Digital Input, Output and I/O Pins . . . . . DGND to DV_{DD}
ESD Tolerance (No Damage) 2500V

Thermal Reliability Information

Thermal Resistance (Note 1) θ_{JA}
HI7188IP . . . . . 50°C/W
HI7188IN . . . . . 80°C/W
Maximum Power Dissipation
HI7188Ix 0.5W
Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +150°C
Lead Temperature (Soldering 10s) . . . . . +300°
(MQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{RHI} = +2.5V, V_{RLO} = AGND, V_{CM} = AGND, PGIA Gain = 1, OSC_{IN} = 3.6864MHz, Bipolar Input Range Selected

PARAMETER	TEST CONDITION	-40°C TO +85°C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution	Dependent on Gain (Note 2)	-	-	16	Bits
Integral Non-Linearity, INL	FS = 25Hz, +FS, +MS, 0, -MS, -FS End Point Line Method (Notes 3, 5, 6)	-	0.0007	0.0015	%FS
Differential Non-Linearity	(Note 2)	No Missing Codes to 16-Bits			-
Offset Error, V_{OS} (Can be Calibrated to Zero)	$V_{INHI} = V_{INLO}$ (Notes 3, 4)	-	0.0007	-	%FS
Full Scale Error, FSE (Can be Calibrated to Zero)	$V_{INHI} - V_{INLO}$ = +2.5V (Notes 3, 4)	-	0.0007	-	%FS
Gain Error (Can be Calibrated to Zero)	Slope = +Full Scale - (-Full Scale) (Notes 3, 4)	-	0.0007	-	%FS
Noise, e_N		-	TBD	-	V
Common Mode Rejection Ratio, CMRR	V_{CM} = 0V (Note 5) Delta V_{CM} = ±3V	-120	-	-	dB
Off Channel Isolation	(Note 2)	-100	-	-	dB
ANALOG INPUT					
Common Mode Input Range, V_{CM}	(Note 2)	AV_{SS}	-	AV_{DD}	-
Input Leakage Current, I_{IN}	$V_{IN} = AV_{DD}$ (Note 3)	-	-	1.0	nA
Input Capacitance, C_{IN}	(Note 2)	-	-	5.0	pF
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic Current, I_I	V_{IN} = 0V, +5V	-	1.0	10	A
Input Capacitance, C_{IN}	V_{IN} = 0V (Note 2)	-	5.0	-	pF

Electrical Specifications AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{RHI} = +2.5V, V_{RLO} = AGND, V_{CM} = AGND, PGIA Gain = 1, OSC_{IN} = 3.6864MHz, Bipolar Input Range Selected **(Continued)**

PARAMETER	TEST CONDITION	-40°C TO +85°C			UNITS
		MIN	TYP	MAX	
DIGITAL OUTPUTS					
Output Logic High Voltage, V_{OH}	I_{OUT} = -100µA (Note 7)	2.4	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OUT} = 3.0mA (Note 7)	-	-	0.4	V
Output Three-State Leakage Current, I_{OZ}	V_{OUT} = 0V, +5V (Note 7)	-	1	10	µA
Digital Output Capacitance, C_{OUT}	(Note 2)	-	10	-	pF
POWER SUPPLY CHARACTERISTICS					
IAV_{DD}	AV_{DD} = +5V, OSC_1 = 3.6864MHz (Note 3)	-	2.0	-	mA
IAV_{SS}	AV_{SS} = -5V, OSC_1 = 3.6864MHz (Note 3)	-	2.0	-	mA
IDV_{DD}	DV_{DD} = +5V, SCLK = 4MHz	-	2.0	-	mA
Power Dissipation, Active PD_A	AV_{DD} = +5V, AV_{SS} = -5V, SLP = '0' (Notes 3, 9)	-	30	-	mW
Power Dissipation, Sleep PD_S	AV_{DD} = +5V, AV_{SS} = -5V, SLP = '1' (Notes 3, 9)	-	20	-	mW
PSRR	AV_{DD} = +5V, AV_{SS} = -5V, (Note 3)	-	80	-	dB

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Parameter guaranteed by design or characterization, not production tested.
3. Applies to both Bipolar and Unipolar Input Ranges.
4. These errors can be removed by re-calibrating at the desired operating temperature.
5. Applies after calibration.
6. Fully differential input signal source is used.
7. See Load Test Circuit R1 = 10k, C_L= 50pF (Includes Stray and Jig Capacitance).
8. For Line Noise Rejection, 3.6864MHz is required to develope internal clocks to reject 50/60Hz.
9. SLP is the sleep mode enable bit defined in bit 3 of the Control Register (CR <3>).

Pin Description

40 PIN DIP	44 PIN QUAD FLAT PACK	PIN NAME	PIN DESCRIPTION
1	41	MODE	Mode input. Used to select between Synchronous Self Clocking (MODE = 1) or Synchronous External Clocking (MODE = 0) for the Serial Port.
2	42	SCLK	Serial clock input. Synchronizes serial data transfers.
3	43	SDO	Serial Data Out. Serial data is read from this line when using a 3 wire serial protocol such as the Motorola Serial Peripheral Interface.
4	44	SDIO	Serial Data In or Out. Serial data is written to this pin for loading the command register and instruction register, and for reading data. This line is bidirectional programmable and interfaces directly to the Intel Standard Serial Interface using a 2 wire serial protocol.
5	1	OSC_1	Oscillator clock input for the device. A crystal connected between OSC_1 and OSC_2 will provide a clock to the device, or an external oscillator can drive OSC_1. The oscillator frequency should be 3.6864MHz).
6	2	OSC_2	Used to connect a crystal source between OSC_1 and OSC_2. Leave open otherwise.
7	3, 30	DV_{DD}	Positive Digital supply (+5V).
8, 31	4, 29, 39	DGND	Digital supply ground
9, 30	5, 6, 27, 28	AV_{SS}	Negative analog power supply (-5V).
10	7	V_{INL1}	Analog input low for Channel 1.
11	8	V_{INH1}	Analog input high for Channel 1.
12	9	V_{INL2}	Analog input low for Channel 2.
13	10	V_{INH2}	Analog input high for Channel 2.
14	11	V_{INL3}	Analog input low for Channel 3.
15	12	V_{INH3}	Analog input high for Channel 3.
16	13	V_{INL4}	Analog input low for Channel 4.
17	14	V_{INH4}	Analog input high for Channel 4.
18	15	V_{INL5}	Analog input low for Channel 5.
19	16	V_{INH5}	Analog input high for Channel 5.
20	17	V_{INL6}	Analog input low for Channel 6.
21	18	V_{INH6}	Analog input high for Channel 6.
22	19	V_{INL7}	Analog input low for Channel 7.
23	20	V_{INH7}	Analog input high for Channel 7.
24	21	V_{INL8}	Analog input low for Channel 8.
25	22	V_{INH8}	Analog input high for Channel 8.
26	23	V_{CM}	Common mode voltage. Should be tied to the mid point of AV_{DD} and AV_{SS}.
27	24	V_{RLO}	External reference input. Should be negative referenced to V_{RHI}.

Pin Description (Continued)

40 PIN DIP	44 PIN QUAD FLAT PACK	PIN NAME	PIN DESCRIPTION
28	25	V_{RHI}	External reference input. Should be positive referenced to V_{RLO}.
29	26	AV_{DD}	Positive analog power supply (+5V).
32	31	$\overline{RST}$	Reset (active low) input. Resets registers, filter, and state machines.
33	32	CA	Calibration Active output. Indicates that at least one channel is in a calibration mode.
34	33	MXC	Multiplexer Control output. Indicates that the conversion for the active channel is complete.
35	34	A_0	Channel count output (LSB).
36	35	A_1	Channel count output.
37	36	A_2	Channel count output (MSB).
38	37	$\overline{EOS}$	End of Scan output. Signals the end of a channel scan (all programmed channels have been converted) and data is available to be read.
39	38	$\overline{RSTI/O}$	I/O Reset (active low) input. Resets serial interface state machine only.
40	40	$\overline{CS}$	Chip Select input. Used to select a serial data transfer cycle. This line can be tied to DGND.

HI7190

24-Bit High Precision Sigma Delta A/D Converter

June 1995

Features

- 22-Bit Resolution with No Missing Code
- 0.0007% Integral Non-Linearity (Typ)
- 20mV to ±2.5V Full Scale Input Ranges
- Internal PGIA with Gains of 1 to 128
- Serial Data I/O Interface, SPI Compatible
- Differential Analog and Reference Inputs
- Internal or System Calibration
- -120dB Rejection of 60/50Hz Line Noise
- Min. Settling Time of 3 Conversions for Step Input

Applications

- Process Control and Measurement
- Industrial Weight Scales
- Part Counting Scales
- Laboratory Instrumentation
- Motion Control
- Seismic Monitoring
- Magnetic Field Monitoring
- Intruder Detection
- Medical Patient Monitoring

Description

The Harris HI7190 is a monolithic instrumentation sigma delta A/D converter which operates from ±5V supplies. Both the signal and reference inputs are fully differential for maximum flexibility and performance. An internal Programmable Gain Instrumentation Amplifier (PGIA) provides input gains from 1 to 128 eliminating the need for external pre-amplifiers. The on-demand converter auto-calibrate function is capable of removing offset and gain errors existing in external and internal circuitry. The on-board user programmable digital filter provides over -120dB of 60/50Hz noise rejection and allows fine tuning of resolution and conversion speed over a wide dynamic range.

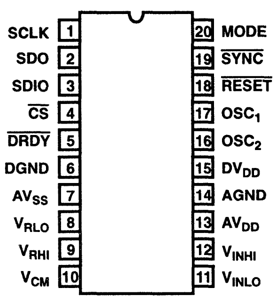
The HI7190 contains a serial I/O port and is compatible with most synchronous transfer formats including both the Motorola 6805/11 series SPI and Intel 8051 series SSR protocols. A sophisticated set of commands gives the user control over calibration, PGIA gain, device selection, standby mode, and several other features. The On-chip Calibration Registers allow the user to read and write calibration data.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI7190IP	-40°C to +85°C	20 Lead Plastic DIP
HI7190IB	-40°C to +85°C	20 Lead Plastic SOIC (W)

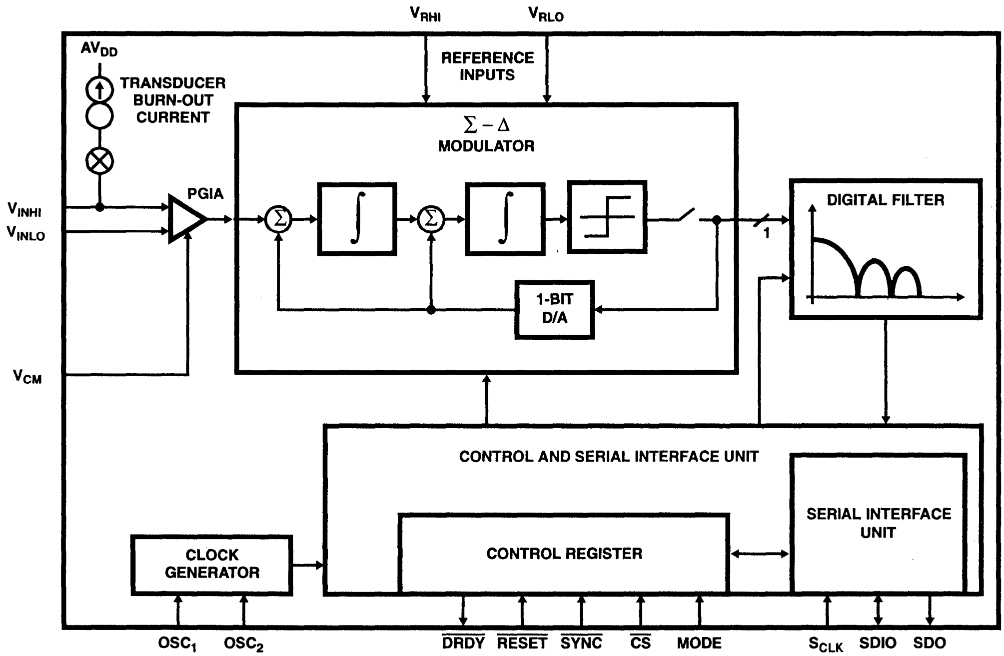
Pinout

HI7190
(PDIP, SOIC)
TOP VIEW

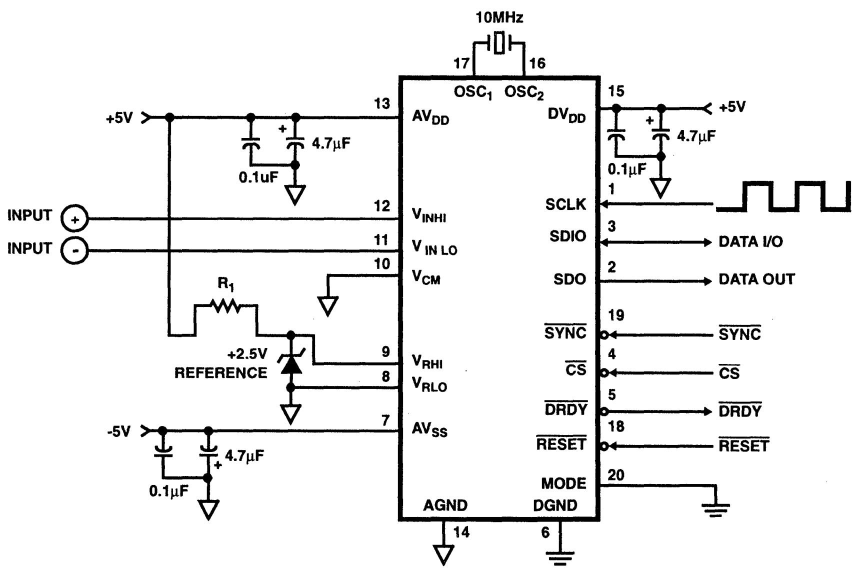


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltage
- AV_{DD} to AGND . . . . . +5.5V
- AV_{SS} to AGND . . . . . -5.5V
- DV_{DD} to DGND . . . . . +5.5V
- DGND to AGND . . . . . ±0.3V

Analog Input Pins . . . . . AV_{SS} to AV_{DD}

Digital Input, Output and I/O Pins . . . . . DGND to DV_{DD}

ESD Tolerance (No Damage)
- Human Body Model 500V
- Machine Model . . . . . +100V
- Charged Device Model 1000V

Thermal Information

Thermal Resistance (Note 1) θ_{JA}
- HI7190IP . . . . . 125°C/W
- HI7190IB . . . . . 100°C/W

Maximum Power Dissipation
- HI7190Ix 0.5W

Operating Temperature Range . . . . . -40°C to +85°C

Junction Temperature
- HI7190Ix . . . . . +150°C

Lead Temperature (Soldering, 10s) . . . . . +300°C
- For SOIC - Lead Tips Only

Storage Temperature Range . . . . . -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{RHI} = +2.5V, V_{RLO} = AGND = 0V, V_{CM} = AGND, PGIA Gain = 1, OSC_{IN} = 10MHz, Bipolar Input Range Selected, f_N = 10Hz

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Integral Non-Linearity, INL	End Point Line Method (Notes 3, 5, 6,)	-	±0.0007	±0.0015	%FS
Differential Non-Linearity	(Note 2)	No Missing codes to 22-Bits			LSB
Offset Error, V_{OS}	$V_{INHI} = V_{INLO}$ (Notes 3, 5, 8, 10)	-	-	-	-
Offset Error Drift	$V_{INHI} = V_{INLO}$ (Notes 3, 8)	-	1	-	µV/ °C
Full Scale Error, FSE	$V_{INHI} - V_{INLO}$ = +2.5V (Notes 3, 5, 8, 10)	-	-	-	-
Noise, e_N	See Table 1	-	-	-	-
Common Mode Rejection Ratio, CMRR	V_{CM} = 0V $V_{INHI} = V_{INLO}$ from -2V to +2V		-75	-	dB
Normal Mode 50Hz Rejection	Filter Notch = 10, 25, 50 Hz (Note 2)	-120	-	-	dB
Normal Mode 60Hz Rejection	Filter Notch = 10, 30, 60 Hz (Note 2)	-120	-	-	dB
Step Response Settling Time		3	-	4	Conversions
ANALOG INPUTS					
Input Voltage Range	Unipolar Mode (Note 9)	0	-	V_{REF}	V
Input Voltage Range	Bipolar Mode (Note 9)	$-V_{REF}$	-	V_{REF}	V
Common Mode Input Range	(Note 2)	AV_{SS}	-	AV_{DD}	V
Input Leakage Current, I_{IN}	$V_{IN} = AV_{DD}$ (Note 2)	-	-	1.0	nA
Input Capacitance, C_{IN}		-	5.0	-	pF
Reference Voltage Range, V_{REF} ($V_{REF} = V_{RHI} - V_{RLO}$)		2.5	-	5	V
Transducer Burn-Out Current, I_{BO}		100	500	-	nA
CALIBRATION LIMITS					
Positive Full Scale Calibration Limit		-	-	1.2(V_{REF}/ Gain)	-
Negative Full Scale Calibration Limit		-	-	1.2(V_{REF}/ Gain)	-
Offset Calibration Limit		-	-	1.2(V_{REF}/ Gain)	-

Electrical Specifications AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{RHI} = +2.5V, V_{RLO} = AGND = 0V, V_{CM} = AGND, PGIA Gain = 1, OSC_{IN} = 10MHz, Bipolar Input Range Selected, f_N = 10Hz **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
Input Span		0.2(V_{REF}/ Gain)	-	2.4(V_{REF}/ Gain)	-
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		3.5	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic Current, I_I	V_{IN} = 0V, +5V	-	1.0	10	µA
Input Capacitance, C_{IN}	V_{IN} = 0V	-	5.0	-	pF
DIGITAL OUTPUTS					
Output Logic High Voltage, V_{OH}	I_{OUT} = -100µA (Note 7)	2.4	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OUT} = 3.0mA (Note 7)	-	-	0.4	V
Output Three-State Leakage Current, I_{OZ}	V_{OUT} = 0V, +5V (Note 7)	-10	1	10	µA
Digital Output Capacitance, C_{OUT}		-	10	-	pF
TIMING CHARACTERISTICS					
SCLK Minimum Cycle Time, t_{SCLK}		200	-	-	ns
SCLK Minimum Pulse Width, t_{SCLKPW}		50	-	-	ns
$\overline{CS}$ to SCLK Precharge Time, t_{PRE}		50	-	-	ns
$\overline{DRDY}$ Minimum High Pulse Width	(Notes 2, 7)	500	-	-	ns
Data Setup to SCLK Rising Edge (Write), t_{DSU}		50	-	-	ns
Data Hold from SCLK Rising Edge (Write), t_{DHLD}		0	-	-	ns
Data Read Access from Instruction Byte Write, t_{ACC}	(Note 7)	-	-	40	ns
Read Bit Valid from SCLK Falling Edge, t_{DV}	(Note 7)	-	-	40	ns
Last Data Transfer to Data Ready Inactive, $t_{\overline{DRDY}}$	(Note 7)	-	35	-	ns
$\overline{RESET}$ Low Pulse Width	(Note 2)	100	-	-	ns
$\overline{SYNC}$ Low Pulse Width	(Note 2)	100	-	-	ns
Oscillator Clock Frequency	(Note 2)	0.1	-	10	MHz
Output Rise/Fall Time	(Note 2)	-	-	30	ns
Input Rise/Fall Time	(Note 2)	-	-	1	µs

Electrical Specifications AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{RHI} = +2.5V, V_{RLO} = AGND = 0V, V_{CM} = AGND, PGIA Gain = 1, OSC_{IN} = 10MHz, Bipolar Input Range Selected, f_N = 10Hz **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
POWER SUPPLY CHARACTERISTICS					
IAV_{DD}		-	-	1.5	mA
IAV_{SS}		-	-	1.5	mA
IDV_{DD}	SCLK = 4MHz	-	-	3.0	mA
Power Dissipation, Active PD_A	SB = '0'	-	15	30	mW
Power Dissipation, Standby PD_S	SB = '1'	-	5	-	mW
PSRR	(Note 3)	-	-70	-	dB

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Parameter guaranteed by design or characterization, not production tested.
3. Applies to both bipolar and unipolar input ranges.
4. These errors can be removed by re-calibrating at the desired operating temperature.
5. Applies after system calibration.
6. Fully differential input signal source is used.
7. See Load Test Circuit, Figure 10, R1 = 10kΩ, C_L = 50pF.
8. 1 LSB = 298nV at 24-bits for a Full Scale Range of 5V.
9. $V_{REF} = V_{RHI} - V_{RLO}$
10. These errors are on the order of the output noise shown in Table 1.

Timing Diagrams

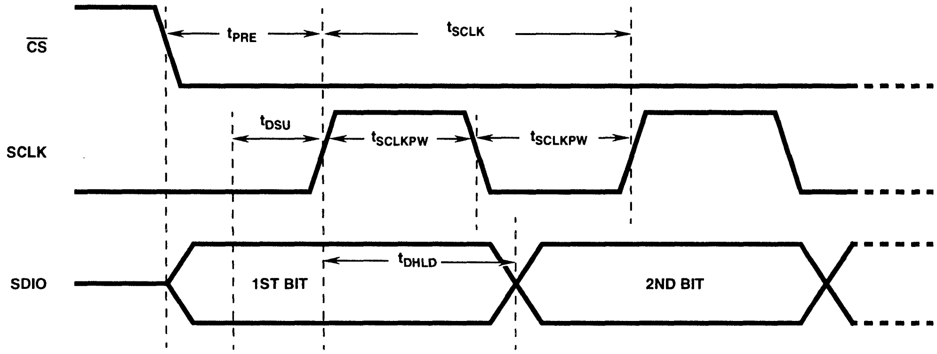


FIGURE 1. DATA WRITE TO HI7190

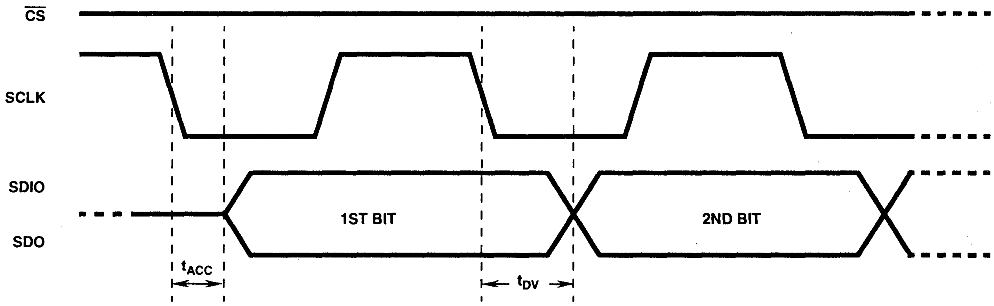


FIGURE 2. DATA READ FROM HI7190

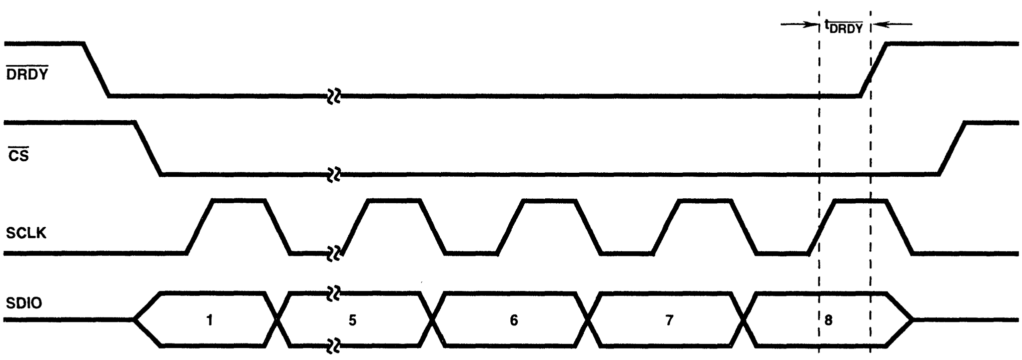


FIGURE 3. DATA READ FROM HI7190

4

A/D CONVERTERS

Pin Descriptions

20 LEAD DIP, SOIC	PIN NAME	PIN DESCRIPTION
1	SCLK	Serial interface clock. Synchronizes serial data transfers. Data is input on the rising edge and output on the falling edge.
2	SDO	Serial Data OUT. Serial data is read from this line when using a 3-wire serial protocol such as the Motorola Serial Peripheral Interface.
3	SDIO	Serial Data IN or OUT. This line is bidirectional programmable and interfaces directly to the Intel Standard Serial Interface using a 2-wire serial protocol.
4	CS	Chip Select input. Used to select the HI7190 for a serial data transfer cycle. This line can be tied to DGND.
5	DRDY	An active low interrupt indicating that a new data word is available for reading.
6	DGND	Digital supply ground.
7	AV_{SS}	Negative analog power supply (-5V).
8	V_{RLO}	External reference input. Should be negative referenced to V_{RHI}.
9	V_{RHI}	External reference input. Should be positive referenced to V_{RLO}.
10	V_{CM}	Common mode input. Should be set to halfway between AV_{DD} and AV_{SS}.
11	V_{INLO}	Analog Input LO. Negative input of the PGIA.
12	V_{INHI}	Analog Input HI. Positive input of the PGIA. The V_{INHI} input is connected to a current source that can be used to check the condition of an external transducer. This current source is controlled via the Control Register.
13	AV_{DD}	Positive analog power supply (+5V).
14	AGND	Analog supply ground.
15	DV_{DD}	Positive digital supply (+5V).
16	OSC_2	Used to connect a crystal source between OSC_1 and OSC_2. Leave open otherwise.
17	OSC_1	Oscillator clock input for the device. A crystal connected between OSC_1 and OSC_2 will provide a clock to the device, or an external oscillator can drive OSC_1. The oscillator frequency should be 10MHz (Typ).
18	RESET	Active low Reset pin. Used to initialize the HI7190 registers, filter and state machines.
19	SYNC	Active low Sync input. Used to control the synchronization of a number of HI7190s. A logic '0' initializes the converter.
20	MODE	Mode pin. Used to select between Synchronous Self Clocking (Mode = 1) or Synchronous External Clocking (Mode = 0) for the Serial Port.

Load Test Circuit

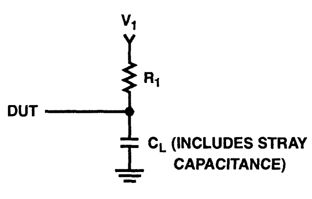


FIGURE 4.

ESD Test Circuit

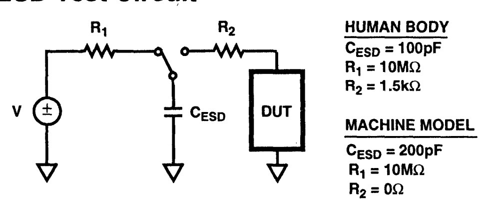


FIGURE 5A.

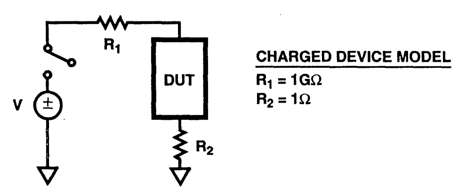


FIGURE 5B.

TABLE 1A. PEAK-TO-PEAK NOISE AND ENOB FOR VARIOUS GAINS AND CONVERSION FREQUENCIES

CONVERSION RATE (f_N)	INPUT CUTOFF FREQUENCY (-3dB, f_S)	GAIN = 1		GAIN = 2		GAIN = 4		GAIN = 8	
		P-P NOISE (μV)	NUMBER OF BITS	P-P NOISE (μV)	NUMBER OF BITS	P-P NOISE (μV)	NUMBER OF BITS	P-P NOISE (μV)	NUMBER OF BITS
10Hz	2.62Hz	2.87	23.5	3.24	23.3	3.54	23.2	6.63	22.2
25Hz	6.55Hz	3.99	23.0	4.43	22.8	5.95	22.4	13.0	21.3
30Hz	7.86Hz	4.54	22.8	10.5	21.6	14.7	21.1	17.3	20.9
50Hz	13.1Hz	5.96	22.4	8.30	22.3	9.02	21.8	27.9	20.2
60Hz	15.7Hz	6.89	22.2	7.26	22.1	10.0	21.7	18.5	20.8
100Hz	26.2Hz	16.5	20.9	13.8	21.2	16.6	20.9	41.5	19.6
250Hz	65.5Hz	44.4	19.5	33.0	19.9	33.8	19.9	66.8	18.9
500Hz	131Hz	128	18.0	101	18.3	388	18.4	134	17.9
1kHz	262Hz	638	15.7	431	16.2	486	16.1	583	15.8
2kHz	524Hz	3820	13.1	2610	13.6	2890	13.5	3310	13.3

TABLE 1A. PEAK-TO-PEAK NOISE AND ENOB FOR VARIOUS GAINS AND CONVERSION FREQUENCIES

CONVERSION RATE (f_N)	INPUT CUTOFF FREQUENCY (-3dB, f_S)	GAIN = 16		GAIN = 32		GAIN = 64		GAIN = 128	
		P-P NOISE (μV)	NUMBER OF BITS	P-P NOISE (μV)	NUMBER OF BITS	P-P NOISE (μV)	NUMBER OF BITS	P-P NOISE (μV)	NUMBER OF BITS
10Hz	2.62Hz	6.93	22.2	28.2	20.2	29.4	20.1	50.5	19.3
25Hz	6.55Hz	25.0	20.3	44.4	19.5	93.1	18.4	176	17.5
30Hz	7.86Hz	17.2	20.9	16.4	20.9	44.2	19.5	201	17.3
50Hz	13.1Hz	27.2	20.2	93.4	18.4	94.7	18.4	308	16.7
60Hz	15.7Hz	30.9	20.0	90.4	18.5	148	17.8	276	16.9
100Hz	26.2Hz	42.84	19.6	142	17.8	175	17.5	419	16.3
250	65.5Hz	70.6	18.8	232.8	17.1	1010	15	2030	14
500Hz	131Hz	148	17.8	468	16.1	1690	14.3	4050	13.0
1kHz	262Hz	544.6	15.9	2150	13.9	2030	13.9	4750	12.8
2kHz	524Hz	3570	13.2	22400	10.5	23300	10.5	20700	10.6

TABLE 1B. RMS INPUT REFERRED NOISE FOR VARIOUS GAINS AND CONVERSION FREQUENCIES

CONVERSION RATE (f_N)	INPUT CUTOFF FREQUENCY (-3dB, f_S)	GAIN = 1	GAIN = 2	GAIN = 4	GAIN = 8	GAIN = 16	GAIN = 32	GAIN = 64	GAIN = 128
		RMS NOISE (μV)	RMS NOISE (μV)	RMS NOISE (μV)	RMS NOISE (μV)	RMS NOISE (μV)	RMS NOISE (μV)	RMS NOISE (μV)	RMS NOISE (μV)
10Hz	2.62Hz	0.435	0.246	0.134	0.126	0.066	0.134	0.070	0.060
25Hz	6.55Hz	0.604	0.336	0.226	0.246	0.237	0.212	0.220	0.209
30Hz	7.86Hz	0.689	0.796	0.557	0.327	0.163	0.077	0.105	0.238
50Hz	13.1Hz	0.903	0.477	0.341	0.529	0.258	0.442	0.224	0.364
60Hz	15.7Hz	1.04	0.550	0.380	0.350	0.293	0.428	0.350	0.326
100Hz	26.2Hz	2.50	1.05	0.628	0.786	0.406	0.672	0.414	0.496
250Hz	65.5Hz	6.73	2.50	1.28	1.26	0.669	1.10	2.40	2.40
500Hz	131Hz	19.4	7.61	14.7	2.54	1.40	2.22	3.40	4.79
1kHz	262Hz	96.7	32.6	18.4	11.0	5.16	10.2	4.97	5.63
2kHz	524Hz	579	198	109	62.8	33.8	108	55.2	24.5

Definitions

Integral Non-Linearity (INL) - This is the maximum deviation of any digital code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (a point 0.5 LSB below the first code transition 000...000 and 000...001) and full scale (a point 0.5 LSB above the last code transition 111...110 to 111...111).

Differential Non-Linearity (DNL) - This is the deviation from the actual difference between midpoints and the ideal difference between midpoints (1 LSB) for adjacent codes. If this difference is equal to or more negative than 1 LSB, a code will be missed.

Offset Error (V_{OS}) - The offset error is the deviation of the first code transition from the ideal input voltage (V_{IN} - 0.5 LSB). This error can be calibrated to the order of the noise level shown in Table 1.

Full Scale Error (FSE) - The full scale error is the deviation of the last code transition from the ideal input full-scale voltage (V_{IN^-} + V_{REF}/Gain - 1.5 LSB). This error can be calibrated to the order of the noise level shown in Table 1.

Input Span - The input span defines the minimum and maximum input voltages the device can handle while still calibrating properly for gain.

Noise (e_N) - Table 1 shows the input referred peak-to-peak and RMS noise for some typical notch and -3dB frequencies. The numbers given are for the bipolar input ranges with a V_{REF} of +2.5V which means the input range is ±2.5V. Measurements are taken for 100 conversions with the peak-to-peak output noise being the difference between the maximum and minimum readings over the 100 conversions.

Table 1A and 1B show the output peak-to-peak noise of the device while table 1C shows the RMS output noise referred back to the input. The RMS input referred noise data is calculated by converting the peak-to-peak numbers to RMS values by dividing by a crest factor of 6.6, and then dividing that result by the gain of the HI7190. Finally, the Effective Number of Bits (ENOB) or effective resolution is calculated by taking the $\log_2$ (5V/RMS output noise).

The noise from the part comes from two sources, the quantization noise from the analog-to-digital conversion process and device noise. Device noise (or Wideband Noise) is independent of gain and essentially flat across the frequency spectrum. Quantization noise is ratiometric to input full-scale (and hence gain) and its frequency response is shaped by the modulator.

Looking at the table, as the cut-off frequency increases the output noise increases. This is due to more of the quantization noise of the part coming through to the output and, hence, the output noise increases with increasing -3dB frequencies. For the lower notch settings, the output noise is dominated by the device noise and, hence, altering the gain has little effect on the output noise. At higher notch frequencies, the quantization noise dominates the output noise and, in this case, the output noise tends to decrease with increasing gain.

Since the output noise comes from two sources, the effective resolution of the device (i.e. the ratio of the input full-scale to the output rms noise) does not remain constant with increasing gain or with increasing bandwidth. It is possible to do post-filtering (such as brick wall filtering) on the data to improve the overall resolution for a given -3dB frequency and also to further reduce the output noise.

Circuit Description

The HI7190 is a monolithic sigma delta A/D converter which operates from ±5V supplies and is intended for measurement of wide dynamic range, low frequency signals. It contains a Programmable Gain Instrumentation Amplifier (PGIA), sigma delta ADC, digital filter, bidirectional serial port (compatible with many industry standard protocols), clock oscillator, and an on chip controller.

The signal and reference inputs are fully differential for maximum flexibility and performance. Normally V_{RHI} and V_{RLO} are tied to +2.5V and AGND respectively. This allows for input ranges of 2.5V and 5V when operating in the unipolar and bipolar modes respectively (assuming the PGIA is configured for a gain of 1). The internal PGIA provides input gains from 1 to 128 and eliminates the need for external pre-amplifiers. This means the device will convert signals ranging from 0V to +20mV and 0V to +2.5V when operating in the unipolar mode or signals in the range of ±20mV to ±2.5V when operating in the bipolar mode.

The input signal is continuously sampled at the input to the HI7190 at a clock rate set by the oscillator frequency and the selected gain. This signal then passes through the sigma delta modulator (which includes the PGIA) and emerges as a pulse train whose code density contains the analog signal information. The output of the modulator is fed into the sinc^3 digital low pass filter. The filter output passes into the calibration block where offset and gain errors are removed. The calibrated data is then coded (2's complement, offset binary or binary) before being stored in the Data Output Register. The Data Output Register update rate is determined by the first notch frequency of the digital filter. This first notch frequency is programmed into HI7190 via the Control Register and has a range of 9.54Hz to 1.953kHz which corresponds to -3dB frequencies of 2.58Hz and 512Hz respectively.

Output data coding on the HI7190 is programmable via the Control Register. When operating in bipolar mode, data output can be either 2's complement or offset binary. In unipolar mode output is binary.

The DRDY signal is used to alert the user that new output data is available. Converted data is read via the HI7190 serial I/O port which is compatible with most synchronous transfer formats including both the Motorola 6805/11 series SPI and Intel 8051 series SSR protocols. Data Integrity is always maintained at the HI7190 output port. This means that if a data read of conversion N is begun but not finished before the next conversion (conversion N+1) is complete, the DRDY line remains active (low) and the data being read is not overwritten.

The HI7190 provides many calibration modes that can be initiated at any time by writing to the Control Register. The device can perform system calibration where external components are included with the HI7190 in the calibration loop or self-calibration where only the HI7190 itself is in the calibration loop. The On-chip Calibration Registers are read/write registers which allow the user to read calibration coefficients as well as write previously determined calibration coefficients.

Circuit Operation

The analog and digital supplies and grounds are separate on the HI7190 to minimize digital noise coupling into the analog circuitry. Nominal supply voltages are AV_{DD} = +5V, DV_{DD} = +5V, and AV_{SS} = -5V. If the same supply is used for AV_{DD} and DV_{DD} it is imperative that the supply is separately decoupled to the AV_{DD} and DV_{DD} pins on the HI7190. Separate analog and digital ground planes should be maintained on the system board and the grounds should be tied together back at the power supply.

When the HI7190 is powered up it needs to be reset by pulling the $\overline{RESET}$ line low. The reset sets the internal registers of the HI7190 as shown in Table 2 and puts the part in the bipolar mode with a gain of 1 and offset binary coding. The filter notch of the digital filter is set at 30Hz while the I/O is set up for bidirectional I/O (data is read and written on the SDIO line and SDO is three-stated), descending byte order, and MSB first data format. A self calibration is performed before the device begins converting. $\overline{DRDY}$ goes low when valid data is available at the output.

TABLE 2. REGISTER RESET VALUES

REGISTER	VALUE (HEX)
Data Output Register	XXXX (undefined)
Control Register	28B300
Offset Calibration Register	Self Calibration Value
Positive Full Scale Calibration Register	Self Calibration Value
Negative Full Scale Calibration Register	Self Calibration Value

The configuration of the HI7190 is changed by writing new setup data to the Control Register. Whenever data is written to byte 2 and/or byte 1 of the Control Register the part assumes that a critical setup parameter is being changed which means that $\overline{DRDY}$ goes high and the device is re-synchronized. If the configuration is changed such that the device is in any one of the calibration modes, a new calibration is performed before normal conversions continue. If the device is written to the conversion mode, a new calibration is NOT performed (A new calibration is recommended any time data is written to the Control Register.). In either case, $\overline{DRDY}$ goes low when valid data is available at the output.

If a single data byte is written to byte 0 of the Control Register, the device assumes the gain has NOT been changed. It is up to the user to re-calibrate the device if the gain is changed in this manner. For this reason it is recommended that the entire Control Register be written when changing the gain of the device. This ensures that the part is re-calibrated (if in a calibration mode) before the $\overline{DRDY}$ output goes low indicating that valid data is available.

The calibration registers can be read via the serial interface at any time. However, care must be taken when writing data to the calibration registers. If the HI7190 is internally updating any calibration register the user can not write to that calibration register. See the Operational Modes section for details on which calibration registers are updated for the various modes.

Since access to the calibration registers is asynchronous to the conversion process the user is cautioned that new calibration data may not be used on the very next set of "valid" data after a calibration register write. It is guaranteed that the new data will take effect on the second set of output data. Non-calibrated data can be obtained from the device by writing 000000 (h) to the Offset Calibration Register, 800000 (h) to the Positive Full Scale Calibration Register, and 800000 (h) to the Negative Full Scale Calibration Register. This sets the offset correction factor to 0 and the positive and negative gain slope factors to 1.

If several HI7190s share a system master clock the $\overline{SYNC}$ pin can be used to synchronize their operation. A common $\overline{SYNC}$ input to multiple devices will synchronize operation such that all output registers are updated simultaneously. Of course the $\overline{SYNC}$ pin would normally be activated only after each HI7190 has been calibrated or has had calibration coefficients written to it.

The $\overline{SYNC}$ pin can also be used to control the HI7190 when an external multiplexer is used with a single HI7190. The $\overline{SYNC}$ pin in this application can be used to guarantee a maximum settling time of 3 conversion periods when switching channels on the multiplexer.

Analog Section Description

Figure 6 shows a simplified block diagram of the analog modulator front end of a sigma delta A/D Converter. The input signal V_{IN} comes into a summing junction (the PGIA in this case) where the previous modulator output is subtracted from it. The resulting signal is then integrated and the output of the integrator goes into the comparator. The output of the comparator is then fed back via a one bit DAC to the summing junction. The feedback loop forces the average of the fed back signal to be equal to the input signal V_{IN}.

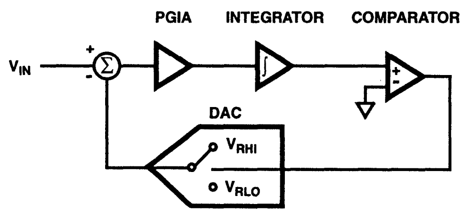


FIGURE 6. SIMPLE MODULATOR BLOCK DIAGRAM

Analog Inputs

The analog input on the HI7190 is a fully differential input with programmable gain capabilities. The input accepts both unipolar and bipolar input signals and gains range from 1 to 128. The common mode range of this input is from AV_{SS} to AV_{DD} provided that the absolute value of the analog input voltage lies within the power supplies. The input impedance of the HI7190 is dependent upon the modulator input sampling rate and the sampling rate varies with the selected PGIA gain. Table 3 below shows the sampling rates and input impedances for the different gain settings of the HI7190. Note that this table is valid only for a 10MHz master clock. If the input clock frequency is changed then the input impedance will change accordingly. The equation used to calculate the input impedance is

$Z_{IN} = 1/(C_{IN} \times f_S)$

where C_{in} is the nominal input capacitance (8pF) and f_s is the modulator sampling rate.

TABLE 3. EFFECTIVE INPUT IMPEDANCE VS GAIN

GAIN	SAMPLING RATE (kHz)	INPUT IMPEDANCE (MΩ)
1	78.125	1.6
2	156.25	0.8
4	312.5	0.4
8, 16, 32, 64, 128	625	0.2

Bipolar/Unipolar Input Ranges

The input on the HI7190 can accept either unipolar or bipolar input voltages. Bipolar or unipolar options are chosen by programming the B/$\overline{U}$ bit of the Control Register. Programming the part for either unipolar or bipolar operation does not change the input signal conditioning.

The inputs are differential, and as a result are referenced to the voltage on the V_{INLO} input. For example, if V_{INLO} is +1.25V and the HI7190 is configured for unipolar operation with a gain of 1 and a V_{REF} of +2.5 V, the input voltage range on the V_{INLO} input is +1.25V to +3.75V. If V_{INLO} is +1.25V and the HI7190 is configured for bipolar mode with gain of 1 and a V_{REF} of +2.5 V, the analog input range on the V_{INHI} input is -1.25V to +3.75V.

Programmable Gain Instrumentation Amplifier

The Programmable Gain Instrumentation Amplifier allows the user to directly interface low level sensors and bridges directly to the HI7190. The PGIA has 4 selectable gain options of 1, 2, 4, 8 which are implemented by multiple sampling of the input signal. Input signals can be gained up further to 16, 32, 64 or 128. These higher gains are implemented in the digital section of the design to maintain a high signal to noise ratio through the front end amplifiers. The gain is digitally programmable in the Control Register via the serial interface. For optimum PGIA performance the V_{CM} pin should be tied to the mid point of the analog supplies.

Differential Reference Input

The reference inputs of the of the HI7190,V_{RHI} and V_{RLO}, provide a differential reference input capability. The nominal differential voltage ($V_{REF} = V_{RHI} - V_{RLO}$) is +2.5V and the common mode voltage cab be anywhere between AV_{SS} and AV_{DD}. Larger values of V_{REF} can be used without degradation in performance with the maximum reference voltage being V_{REF} = +5V. Smaller values of V_{REF} can also be used but performance will be degraded since the LSB size is reduced.

The full scale range of the HI7190 is defined as

$FSR_{BIPOLAR} = 2 \times V_{REF}/GAIN$

$FSR_{UNIPOLAR} = V_{REF}/GAIN$

and V_{RHI} must always be greater than V_{RLO} for proper operation of the device.

The reference inputs provide a high impedance dynamic load similar to the analog inputs and the effective input impedance for the reference inputs can be calculated in the same manner as it is for the analog input impedance. The only difference in the calculation is that C_{IN} for the reference inputs is 10.67pF. Therefor, the input impedance range for the reference inputs is from 149kΩ in a gain of 8 or higher mode to 833kΩ in the gain of 1 mode.

V_{CM} Input

The voltage at the V_{CM} input is the voltage that the internal analog circuitry is referenced to and should always be tied to the midpoint of the AV_{DD} and AV_{SS} supplies. This point provides a common mode input voltage for the internal operational amplifiers and must be driven from a low noise, low impedance source if it is not tied to analog ground. Failure to do so will result in degraded HI7190 performance. It is recommended that V_{CM} be tied to analog ground when operating off of AV_{DD} = +5V and AV_{SS} = -5V supplies.

V_{CM} also determines the headroom at the upper and lower ends of the power supplies which is limited by the common mode input range where the internal operational amplifiers remain in the linear, high gain region of operation. The HI7190 is designed to have a range of $AV_{SS} + 1.8V < V_{CM} < AV_{DD} - 1.8V$. Exceeding this range on the V_{CM} pin will compromise the device performance.

Transducer Burn-Out Current Source

The V_{INHI} input of the HI7190 contains a 500nA (typical) current source which can be turned on/off via the Control Register. This current source can be used in checking whether a transducer has burnt-out or become open before attempting to take measurements on that channel. When the current source is turned on an additional offset will be created indicating the presence of a transducer. The current source is controlled by the BO bit (Bit 4) in the Control Register and is disabled on power up. See Figure 7 for an applications circuit.

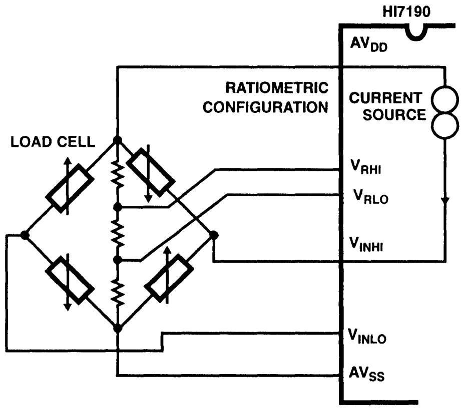


FIGURE 7. BURN-OUT CURRENT SOURCE CIRCUIT

Digital Section Description

A block diagram of the digital section of the HI7190 is shown in Figure 8. This section includes a low pass decimation filter, conversion controller, calibration logic, serial interface, and clock generator.

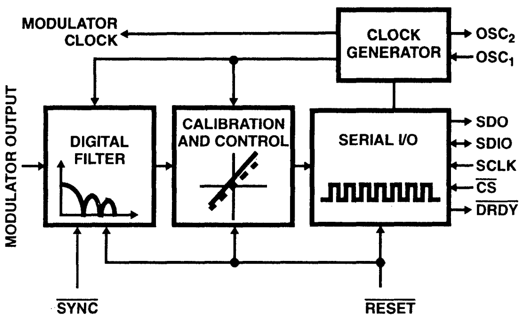


FIGURE 8. DIGITAL SECTION BLOCK DIAGRAM

Digital Filtering

One advantage of digital filtering is that it occurs after the conversion process and can remove noise introduced during the conversion. It can not, however, remove noise present on the analog signal prior to the ADC (which an analog filter can).

One problem with the modulator/digital filter combination is that excursions outside the full scale range of the device could cause the modulator and digital filter to saturate. This device has headroom built in to the modulator and digital filter which tolerates signal deviations up to 33% outside of the full scale range of the device. If noise spikes can drive the input signal outside of this extended range it is recommended that an input analog filter is used or the overall input signal level is reduced.

Low Pass Decimation Filter

The digital low pass filter is a Hogenauer (sinc^3) decimating filter. This filter was chosen because it is a cost effective low pass decimating filter that minimizes the need for internal multipliers and extensive storage and is most effective when used with high sampling or oversampling rates. Figure 9 shows the frequency characteristics of the filter where f_C is the -3dB frequency of the input signal and f_N is the programmed notch frequency. The analog modulator sends a one bit data stream to the filter at a rate of that is determined by:

$f_{MODULATOR} = f_{OSC}/128$

$f_{MODULATOR} = 78.125$ kHz for $f_{OSC} = 10$MHz.

The filter then converts the serial modulator data into 40-bit words for processing by the Hogenauer filter. The data is decimated in the filter at a rate determined by the CODE word FP10-FP0 (programed by the user into the Control Register) and the external clock rate. The equation is:

$f_{NOTCH} = f_{OSC}/(512 \times \text{CODE})$.

The Control Register has 11 bits that select the filter cut off frequency and the first notch of the filter. The output data update rate is equal to the notch frequency. The notch frequency sets the Nyquist sampling rate of the device while the -3dB point of the filter determines the frequency spectrum of interest (f_S). The FP bits have a usable range of 10 through 2047 where 10 yields a 1.953kHz Nyquist rate.

The Hogenauer filter contains alias components that reflect around the notch frequency. If the spectrum of the frequency of interest reaches the alias component, the data has been aliased and therefore undersampled.

Filter Characteristics

The FP10 to FP0 bits programmed into the Control Register determine the cutoff (or notch) frequency of the digital filter. The maximum and minimum cutoff frequencies of the filter are 1.953kHz and 9.54Hz respectively when operating at a clock frequency of 10MHz. If a 1MHz clock is used then the maximum and minimum cutoff frequencies become 0.1953kHz and 0.954Hz respectively. A plot of the $(\sin x/x)^3$ digital filter characteristics is shown in Figure 9. This filter provides greater than 120dB of 50Hz or 60Hz rejection. Changing the clock frequency or the programming of the FP bits does not change the shape of the filter characteristics, it merely shifts the notch frequency. This low pass digital filter at the output of the converter has an accompanying settling time for step inputs just as a low pass analog filter does. New data takes between 3 and 4 conversion periods to settle and update on the serial port with a conversion period T_{CONV} being equal to $1/f_N$.

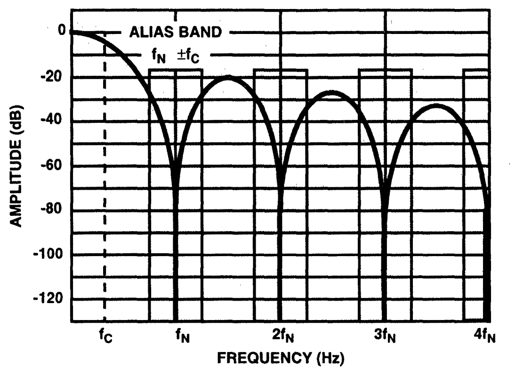


FIGURE 9. LOW PASS FILTER FREQUENCY CHARACTERISTICS

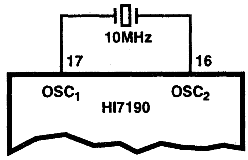


FIGURE 10A.

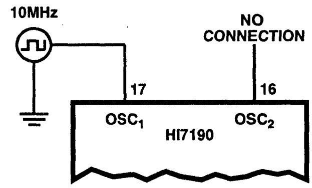


FIGURE 10B.

FIGURE 10. OSCILLATOR CONFIGURATIONS

Input Filtering

The digital filter does not provide rejection at integer multiples of the modulator sampling frequency. This implies that there are frequency bands where noise passes to the output without attenuation. For most cases this is not a problem because the high oversampling rate and noise shaping characteristics of the modulator cause this noise to become a small portion of the broadband noise which is filtered. However, if an anti-alias filter is necessary a single pole RC filter is usually sufficient.

If an input filter is used the user must be careful that the source impedance of the filter is low enough not to cause gain errors in the system. The DC input impedance at the inputs is > 1GΩ but it is a dynamic load that changes with clock frequency and selected gain. The input sample rate, also dependent upon clock frequency and gain, determines the allotted time for the input capacitor to charge. The addition of external components may cause the charge time of the capacitor to increase beyond the allotted time. The result of the input not settling to the proper value is a system gain error which can be eliminated by system calibration of the HI7190.

Clocking/Oscillators

The master clock into the HI7190 can be supplied by either a crystal connected between the OSC_1 and OSC_2 pins as shown in Figure 10A or a CMOS compatible clock signal connected to the OSC_1 pin as shown in Figure 10B. The input sampling frequency, modulator sampling frequency, filter -3dB frequency, output update rate, and calibration time are all directly related to the master clock frequency, f_{OSC}. For example, if a 1MHz clock is used instead of a 10MHz clock, what is normally a 10Hz conversion rate becomes a 1Hz conversion rate. Lowering the clock frequency will also lower the amount of current drawn from the power supplies. Please note that the HI7190 specifications are written for a 10MHz clock only.

Operational Modes

The HI7190 contains several operational modes including calibration modes for cancelling offset and gain errors of both internal and external circuitry. A calibration routine should be initiated whenever there is a change in the ambient operating temperature or supply voltage. Calibration should also be initiated if there is a change in the gain, filter notch, bipolar, or unipolar input range. Non-calibrated data can be obtained from the device by writing 000000 to the Offset Calibration Register, 800000 (h) to the Positive Full Scale Calibration Register, and 800000 (h) to the Negative Full Scale Calibration Register. This sets the offset correction factor to 0 and both the positive and negative gain slope factors to 1.

The HI7190 offers several different modes of Self-Calibration and System Calibration. For calibration to occur, the on-chip microcontroller must convert the modulator output for three different input conditions - "zero-scale," "positive full-scale," and "negative full-scale". With these readings, the HI7190 can null any offset errors and calculate the gain slope factor for the transfer function of the converter. It is imperative that the zero-scale calibration be performed before either of the gain calibrations. However, the order of the gain calibrations is not important.

The calibration modes are user selectable in the Control Register by using the MD bits (MD2-MD0) as shown in Table 3. $\overline{DRDY}$ will go low indicating that the calibration is complete and there is valid data at the output.

TABLE 4. HI7190 OPERATIONAL MODES

MD2	MD1	MD0	OPERATIONAL MODE
0	0	0	Conversion
0	0	1	Self Calibration
0	1	0	System Offset Calibration
0	1	1	System Positive Full Scale Calibration
1	0	0	System Negative Full Scale Calibration
1	0	1	System Offset/Internal Gain Calibration
1	1	0	System Gain Calibration
1	1	1	Reserved

Conversion Mode

For Conversion Mode operation the HI7190 converts the differential voltage between V_{INHI} and V_{INLO}. From switching into this mode it takes 3 conversion periods (3 x $1/f_N$) for $\overline{DRDY}$ to go low and new data to be valid. No calibration coefficients are generated when operating in Conversion Mode as data is calibrated using the existing calibration coefficients.

Self Calibration Mode

The Self Calibration Mode is a three step process that updates the Offset Calibration Register, the Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. In this mode an internal offset calibration is done by disconnecting the external inputs and shorting the inputs of the PGIA together. After 3 conversion periods the Offset Calibration Register is updated with the value that corrects any internal offset errors.

After the offset calibration is completed the Positive and Negative Full Scale Calibration Registers are updated. The inputs V_{INHI} and V_{INLO} are disconnected and the external reference is applied across the modulator inputs. The HI7190 then takes 3 conversion cycles to sample the data and update the Positive Full Scale Calibration Register. Next the polarity of the reference voltage across the modulator input terminals is reversed and after 3 conversion cycles the Negative Full Calibration Register is updated. The values stored in the Positive and Negative Full Scale Calibration Registers correct for any internal gain errors in the A/D transfer function. After 3 more conversion cycles the $\overline{DRDY}$ line will activate signaling that the calibration is complete and valid data is present in the Data Output Register.

Please note, self calibration is only valid when operating in a gain of one.

System Offset Calibration Mode

The System Offset Calibration Mode is a single step process that allows the user to lump offset errors of external circuitry and the internal errors of the HI7190 together and null them out. This mode will convert the external differential signal applied to the V_{IN} inputs and then store that value in the Offset Calibration Register. *The user must apply the zero point or offset voltage to the HI7190 analog inputs and allow the signal to settle* ***before*** *selecting this mode.* After 4 conversion periods the $\overline{DRDY}$ line will activate signaling that the calibration is complete and valid data is present in the Data Output Register.

System Positive Full Scale Calibration Mode

The System Positive Full Scale Calibration Mode is a single step process that allows the user to lump gain errors of external circuitry and the internal errors of the HI7190 together and null them out. This mode will convert the external differential signal applied to the V_{IN} inputs and stores the converted value in the Positive Full Scale Calibration Register. *The user must apply the +Full Scale voltage to the HI7190 analog inputs and allow the signal to settle* ***before*** *selecting this mode.* After 4 conversion periods the $\overline{DRDY}$ line will activate signaling the calibration is complete and valid data is present in the Data Output Register.

System Negative Full Scale Calibration Mode

The System Negative Full Scale Calibration Mode is a single step process that allows the user to lump gain errors of external circuitry and the internal errors of the HI7190 together and null them out. This mode will convert the external differential signal applied to the V_{IN} inputs and stores the converted value in the Negative Full Scale Calibration Register. *The user must apply the -Full Scale voltage to the HI7190 analog inputs and allow the signal to settle* ***before*** *selecting this mode.* After 4 conversion periods the $\overline{DRDY}$ line will activate signaling the calibration is complete and valid data is present in the Data Output Register.

System Offset/Internal Gain Calibration Mode

The System Offset/Internal Gain Calibration Mode is a single step process that updates the Offset Calibration Register, the Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. First the external differential signal applied to the V_{IN} inputs is converted and that value is stored in the Offset Calibration Register. *The user must apply the zero point or offset voltage to the HI7190 analog inputs and allow the signal to settle* ***before*** *selecting this mode.*

After this is completed the Positive and Negative Full Scale Calibration Registers are updated. The inputs V_{INHI} and V_{INLO} are disconnected and the external reference is switched in. The HI7190 then takes 3 conversion cycles to sample the data and update the Positive Full Scale Calibration Register. Next the polarity of the reference voltage across the V_{INHI} and V_{INLO} terminals is reversed and after 3 conversion cycles the Negative Full Calibration Register is updated. The values stored in the Positive and Negative Full Scale Calibration Registers correct for any internal gain errors in the A/D transfer function. After 3 more conversion cycles, the $\overline{DRDY}$ line will activate signaling that the calibration is complete and valid data is present in the Data Output Register.

System Gain Calibration Mode

The Gain Calibration Mode is a single step process that updates the Positive and Negative Full Scale Calibration Registers. This mode will convert the external differential signal applied to the V_{IN} inputs and then store that value in the Negative Full Scale Calibration Register. Then the polarity of the input is reversed internally and another conversion is performed. This conversion result is written to the Positive Full Scale Calibration Register. *The user must apply the +Full Scale voltage to the HI7190 analog inputs and allow the sig-*

*nal to settle **before** selecting this mode.* After 1 more conversion period the $\overline{DRDY}$ line will activate signaling the calibration is complete and valid data is present in the data output register.

Reserved

This mode is not used in the HI7190 and should not be selected. There is no internal detection logic to keep this condition from being selected and care should be taken not to assert this bit combination.

Offset and Span Limits

There are limits to the amount of offset and gain which can be adjusted out for the HI7190. For both bipolar and unipolar modes the minimum and maximum input spans are 0.2 x V_{REF} / GAIN and 1.2 x V_{REF} / GAIN respectively.

In the unipolar mode the offset plus the span cannot exceed the 1.2 x V_{REF} / GAIN limit. So, if the span is at its minimum value of 0.2 x V_{REF} / GAIN, the offset must be less than 1 x V_{REF} / GAIN. In bipolar mode the span is equidistant around the voltage used for the zero scale point. For tis mode the offset plus half the span cannot exceed 1.2 x V_{REF} / GAIN. If the span is at ±0.2 x V_{REF} / GAIN, then the offset can not be greater than ±2 x V_{REF} / GAIN.

Serial Interface

The HI7190 has a flexible, synchronous serial communication port to allow easy interfacing to many industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6805/11 SPI and Intel 8051 SSR protocols.The Serial Interface is a flexible 2 or 3-wire hardware interface where the HI7190 can be configured to read and write on a single bidirectional line (SDIO) or configured for writing on SDIO and reading on the SDO line.

The interface is byte organized with each register byte having a specific address and single or multiple byte transfers are supported. In addition, the interface allows flexibility as to the byte and bit access order. That is, the user can specify MSB/LSB first bit positioning and can access bytes in ascending/descending order from any byte position.

The serial interface allows the user to communicate with 5 registers that control the operation of the device.

Data Output Register - a 24-bit read only register containing the conversion results.

Control Register - a 24-bit read/write register containing the setup and operating modes of the device.

Offset Calibration Register - a 24-bit read/write register used for calibrating the zero point of the converter or system.

Positive Full Scale Calibration Register - a 24-bit read/write register used for calibrating the Positive Full Scale point of the converter or system.

Negative Full Scale Calibration Register - a 24-bit read/write register used for calibrating the Negative Full Scale point of the converter or system.

Two clock modes are supported. The HI7190 can accept the serial interface clock (SCLK) as an input from the system or generate the SCLK signal as an output. If the MODE pin is logic low the HI7190 is in external clocking mode and the SCLK pin is configured as an input. In this mode the user supplies the serial interface clock and all interface timing specifications are synchronous to this input. If the MODE pin is logic high the HI7190 is in self-clocking mode and the SCLK pin is configured as an output. In self-clocking mode, SCLK runs at $F_{SCLK} = OSC_1/8$ and stalls high at byte boundaries. SCLK does NOT have the capability to stall low in this mode. All interface timing specifications are synchronous to the SCLK output.

Normal operation in self-clocking mode is as follows (See Figure 12): $\overline{CS}$ is sampled low on falling OSC_1 edges. The first SCLK transition output is delayed 29 OSC_1 cycles from the next rising OSC_1. SCLK transitions eight times and then stalls high for 28 OSC_1 cycles. After this stall period is completed SCLK will again transition eight times and stall high. This sequence will repeat continuously while $\overline{CS}$ is active.

The extra OSC_1 cycle required when coming out of the $\overline{CS}$ inactive state is a one clock cycle latency required to properly sample the $\overline{CS}$ input. Note that the normal stall at byte boundaries is 28 OSC_1 cycles thus giving a SCLK rising to rising edge stall period of 32 OSC_1 cycles.

The affects of $\overline{CS}$ on the I/O are different for self-clocking mode (MODE = 1) than for external mode (MODE = 0). For external clocking mode $\overline{CS}$ inactive disables the I/O state machine, effectively freezing the state of the I/O cycle. That is, an I/O cycle can be interrupted using chip select and the HI7190 will continue with that I/O cycle when re-enabled via $\overline{CS}$. SCLK can continue toggling while $\overline{CS}$ is inactive. If $\overline{CS}$ goes inactive during an I/O cycle, it is up to the user to ensure that the state of SCLK is identical when reactivating $\overline{CS}$ as to what it was when $\overline{CS}$ went inactive. For read operations in external clocking mode, the output will go three-state immediately upon deactivation of $\overline{CS}$.

For self-clocking mode (MODE = 1), the affects of $\overline{CS}$ are different. If $\overline{CS}$ transitions high (inactive) during the period when data is being transferred (any non stall time) the HI7190 will complete the data transfer to the byte boundary. That is, once SCLK begins the eight transition sequence, it will always complete the eight cycles. If $\overline{CS}$ remains inactive after the byte has been transferred it will be sampled and SCLK will remain stalled high indefinitely. If $\overline{CS}$ has returned to active low before the data byte transfer period is completed the HI7190 acts as if $\overline{CS}$ was active during the entire transfer period.

It is important to realize that the user can interrupt a data transfer on byte boundaries. That is, if the Instruction Register calls for a 3 byte transfer and $\overline{CS}$ is inactive after only one byte has been transferred, the HI7190, when reactivated, will continue with the remaining two bytes before looking for the next Instruction Register write cycle.

Note that the outputs will NOT go three-state immediately upon $\overline{CS}$ inactive for read operations in self-clocking mode. In the case of $\overline{CS}$ going inactive during a read cycle the outputs remain driving until after the last data bit is transferred. In the case of $\overline{CS}$ inactive during the clock stall time it takes 1 OSC_1 cycle plus prop delay (maximum) for the outputs to be disabled.

I/O Port Pin Descriptions

The serial I/O port is a bidirectional port which is used to read the data register and read or write the control register and calibration registers. The port contains two data lines, a synchronous clock, and a status flag. Figure 11 shows a diagram of the serial interface lines.

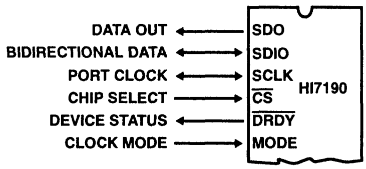


FIGURE 11. HI7190 SERIAL INTERFACE

SDO - Serial Data out. Data is read from this line using those protocols with separate lines for transmitting and receiving data. An example of such a standard is the Motorola Serial Peripheral Interface (SPI) using the 68HC05 and 68HC11 family of micro-controllers, or other similar processors. In the case of using bidirectional data transfer on SDIO, SDO does not output data and is set in a high impedance state.

SDIO - Serial Data in or out. Data is always written to the device on this line. However, this line can be used as a bidirectional data line. This is done by properly setting up the Control Register. Bidirectional data transfer on this line can be used with Intel standard serial interfaces (SSR, Mode 0) in MCS51 and MCS96 family of microcontrollers, or other similar processors.

SCLK - Serial clock. The serial clock pin is used to synchronize data to and from the HI7190 and to run the port state machines. In Synchronous External Clock Mode, SCLK is configured as an input, is supplied by the user, and can run up to a 5MHz rate. In Synchronous Self Clocking Mode, SCLK is configured as an output and runs at $OSC_1/8$.

$\overline{CS}$ - Chip select. This signal is an active low input that allows more than one device on the same serial communication lines. The SDO and SDIO will go to a high impedance state when this signal is high. If driven high during any communication cycle, that cycle will be suspended until $\overline{CS}$ reactivation. Chip select can be tied low in systems that maintain control of SCLK.

$\overline{DRDY}$ - Data Ready. This is an output status flag from the device to signal that the Data Output Register has been updated with the new conversion result. $\overline{DRDY}$ is useful as an edge or level sensitive interrupt signal to a microprocessor or microcontroller. $\overline{DRDY}$ low indicates that new data is available at the Data Output Register. $\overline{DRDY}$ will return high upon completion of a complete Data Output Register read cycle.

MODE - Mode. This input is used to select between Synchronous Self Clocking Mode ('1') or the Synchronous External Clocking Mode ('0'). When this pin is tied to V_{DD} the serial port is configured in the Synchronous Self Clocking mode where the synchronous shift clock (SCLK) for the serial port is generated by the HI7190 and has a frequency of $OSC_1/8$. When the pin is tied to DGND the serial port is configured for the Synchronous External Clocking Mode where the synchronous shift clock for the serial port is generated by an external device up to a maximum frequency of 5MHz.

Programming the Serial Interface

It is useful to think of the HI7190 interface in terms of communication cycles. Each communication cycle happens in 2 phases. The first phase of every communication cycle is the writing of an instruction byte. The second phase is the data transfer as described by the instruction byte. It is important to note that phase 2 of the communication cycle can be a single byte or a multi-byte transfer of data. For example, the 3 byte Data Output Register can be read using one multi-byte communication cycle rather than three single byte communication cycles. It is up to the user to maintain synchronism with respect to data transfers. If the system processor "gets lost" the only way to recover is to reset the HI7190. Figure 13 shows both a 2-wire and a 3-wire data transfer.

Several formats are available for reading from and writing to the HI7190 registers in both the 2-wire and 3-wire protocols. A portion of these formats is controlled by the CR<2:1> (BD and $\overline{MSB}$) bits which control the byte direction and bit order of a data transfer respectively. These two bits can be written in any combination but only the two most useful will be discussed here.

The first combination is to reset both the BD and $\overline{MSB}$ bits (BD = 0, $\overline{MSB}$ = 0). This sets up the interface for descending byte order and MSB first format. When this combination is used the user should always write the Instruction Register such that the starting byte is the most significant byte address. For example, read three bytes of DR starting with the most significant byte. The first byte read will be the most significant in MSB to LSB format. The next byte will be the next least significant (recall descending byte order) again in MSB to LSB order. The last byte will be the next lesser significant byte in MSB to LSB order. *The entire word was read MSB to LSB format.*

The second combination is to set both the BD and $\overline{MSB}$ bits to 1. This sets up the interface for ascending byte order and LSB first format. When this combination is used the user should always write the Instruction Register such that the starting byte is the least significant byte address. For example, read three bytes of DR starting with the least significant byte. The first byte read will be the least significant in LSB to MSB format. The next byte will be the next greater significant (recall

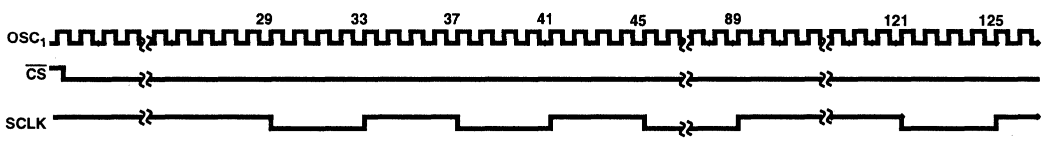


FIGURE 12. SCLK OUTPUT IN SELF CLOCKING MODE

ascending byte order) again in LSB to MSB order. The last byte will be the next greater significant byte in LSB to MSB order. *The entire word was read MSB to LSB format.*

After completion of each communication cycle, The HI7190 interface enters a standby mode while waiting to receive a new instruction byte.

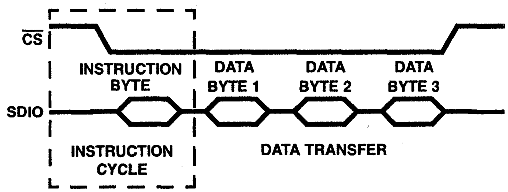


FIGURE 13A. 2-WIRE, 3 BYTE READ OR WRITE TRANSFER

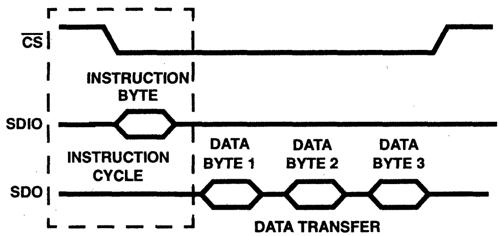


FIGURE 13B. 3-WIRE, 3 BYTE READ TRANSFER

Instruction Byte Phase

The instruction byte phase initiates a data transfer sequence. The processor writes an 8-bit byte (Instruction Byte) to the Instruction Register. The instruction byte informs the HI7190 about the Data transfer phase activities and includes the following information:

- Read or Write cycle
- Number of Bytes to be transferred
- Which register and starting byte to be accessed

Data Transfer Phase

In the data transfer phase, data transfer takes place as set by the Instruction Register contents. See Write Operation and Read Operation sections for detailed descriptions.

Instruction Register

The Instruction Register is an 8-bit register which is used during a communications cycle for setting up read/write operations.

INSTRUCTION REGISTER

MSB	6	5	4	3	2	1	LSB
$\overline{R}$/W	MB1	MB0	FSC	A3	A2	A1	A0

$\overline{R}$/W - Bit 7 of the Instruction Register determines whether a read or write operation will be done following the instruction byte load. 0 = READ, 1 = WRITE.

MB1, MB0 - Bits 6 and 5 of the Instruction Register determine the number of bytes that will be accessed following the instruction byte load. See Table 4 for the number of bytes to transfer in the transfer cycle.

TABLE 5. MULTIPLE BYTE ACCESS BITS

MB1	MB0	DESCRIPTION
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

FSC - Bit 4 is used to determine whether a Positive Full Scale Calibration Register I/O transfer (FSC = 0) or a Negative Full Scale Calibration Register I/O transfer (FSC = 1) is being performed (see Table 5).

A3, A2, A1, A0 - Bits 3 and 2 (A3 and A2) of the Instruction Register determine which internal register will be accessed while bits 1 and 0 (A1 and A0) determine which byte of that register will be accessed first. See Table 5 for the address decode.

TABLE 6. INTERNAL DATA ACCESS DECODE STARTING BYTE

FSC	A3	A2	A1	A0	DESCRPTION
X	0	0	0	0	Data Output Register Byte 0
X	0	0	0	1	Data Output Register Byte 1
X	0	0	1	0	Data Output Register Byte 2
X	0	1	0	0	Control Register Byte 0
X	0	1	0	1	Control Register Byte 1
X	0	1	1	0	Control Register Byte 2
X	1	0	0	0	Offset Cal Register Byte 0
X	1	0	0	1	Offset Cal Register Byte 1
X	1	0	1	0	Offset Cal Register Byte 2
0	1	1	0	0	Positive Full Scale Cal Register Byte 0
0	1	1	0	1	Positive Full Scale Cal Register Byte 1
0	1	1	1	0	Positive Full Scale Cal Register Byte 2
1	1	1	0	0	Negative Full Scale Cal Register Byte 0
1	1	1	0	1	Negative Full Scale Cal Register Byte 1
1	1	1	1	0	Negative Full Scale Cal Register Byte 2

Write Operation

Data can be written to the Control Register, Offset Calibration Register, Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. Write operations are done using the SDIO, $\overline{CS}$ and SCLK lines only, as all data is written into the HI7190 via the SDIO line even when using the 3-wire configuration. Figures 14 and 15 show typical write timing diagrams.

The communication cycle is started by asserting the $\overline{CS}$ line low and starting the clock from its idle state. To assert a write cycle, during the instruction phase of the communication cycle, the Instruction Byte should be set to a write transfer ($\overline{R}$/W = 1).

When writing to the serial port, data is latched into the HI7190 on the rising edge of SCLK. Data can then be changed on the falling edge of SCLK. Data can also be changed on the rising edge of SCLK due to the 0 ns hold time required on the data. This is useful in pipelined applications where the data is latched on the rising edge of the clock.

Read Operation - 3-Wire Transfer

Data can be read from the Data Output Register, Control Register, Offset Calibration Register, Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. When configured in 3-wire transfer mode, read operations are done using the SDIO, SDO, $\overline{CS}$ and SCLK lines. All data is read via the SDO line. Figures 16 and 17 show typical 3-wire read timing diagrams.

The communication cycle is started by asserting the $\overline{CS}$ line and starting the clock from it's idle state. To assert a read cycle, during the instruction phase of the communication cycle, the Instruction Byte should be set to a read transfer ($\overline{R}$/W = 0).

When reading the serial port, data is driven out of the HI7190 on the falling edge of SCLK. Data can be registered externally on the next rising edge of SCLK.

Read Operation - 2-Wire Transfer

Data can be read from the Data Output Register, Control Register, Offset Calibration Register, Positive Full Scale Calibration Register, and the Negative Full Scale Calibration Register. When configured in two wire transfer mode, read operations are done using the SDIO, $\overline{CS}$ and SCLK lines. All data is read via the SDIO line. Figures 18 and 19 show typical 2-wire read timing diagrams.

The communication cycle is started by asserting the $\overline{CS}$ line and starting the clock from it's idle state. To assert a read cycle, during the instruction phase of the communication cycle, the Instruction Byte should be set to a read transfer ($\overline{R}$/W = 0).

When reading the serial port, data is driven out of the HI7190 on the falling edge of SCLK. Data can be registered externally on the next rising edge of SCLK.

Detailed Register Descriptions

Data Output Register

The Data Output Register contains 24-bits of converted data. This register is a read only register.

BYTE 2

MSB	22	21	20	19	18	17	16
D23	D22	D21	D20	D19	D18	D17	D16

BYTE 1

15	14	13	12	11	10	9	8
D15	D14	D13	D12	D11	D10	D9	D8

BYTE 0

7	6	5	4	3	2	1	LSB
D7	D6	D5	D4	D3	D2	D1	D0

Control Register

The Control Register contains 24-bits to control the various sections of the HI7190. This register is a read/write register.

BYTE 2

MSB	22	21	20	19	18	17	16
DC	FP10	FP9	FP8	FP7	FP6	FP5	FP4

BYTE 1

15	14	13	12	11	10	9	8
FP3	FP2	FP1	FP0	MD2	MD1	MD0	B/U

BYTE 0

7	6	5	4	3	2	1	LSB
G2	G1	G0	BO	SB	BD	MSB	SDL

DC - Bit 23 is the Data Coding Bit used to select between two's complementary and offset binary data coding. When this bit is set (DC = 1) the data in the Data Output Register will be two's complement. When cleared (DC = 0) this data will be offset binary. When operating in the unipolar mode the output data is available in straight binary only (the DC bit is ignored). This bit is cleared after a $\overline{RESET}$ is applied to the part.

FP10 through FP0 - Bits 22 through 12 are the Filter programming bits that determine the frequency response of the digital filter. These bits determine the filter cutoff frequency, the position of the first notch and the data rate of the HI7190. The first notch of the filter is equal to the decimation rate and can be determined by the formula:

$f_{NOTCH} = f_{OSC}/(512 \times CODE)$

where CODE is the decimal equivalent of the value in FP10 through FP0. The values that can be programmed into these bits are 10 to 2047 decimal, which allows a conversion rate range of 9.54Hz to 1.953kHz when using a 10MHz clock.

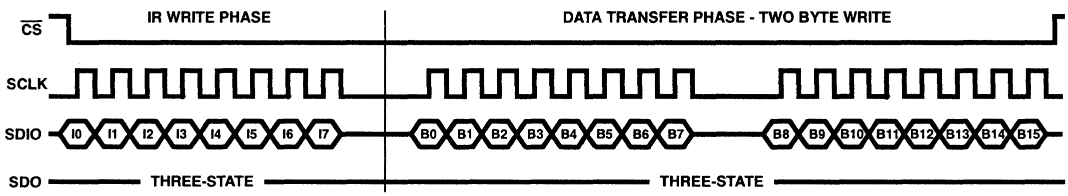


FIGURE 14. DATA WRITE CYCLE, SCLK IDLE LOW

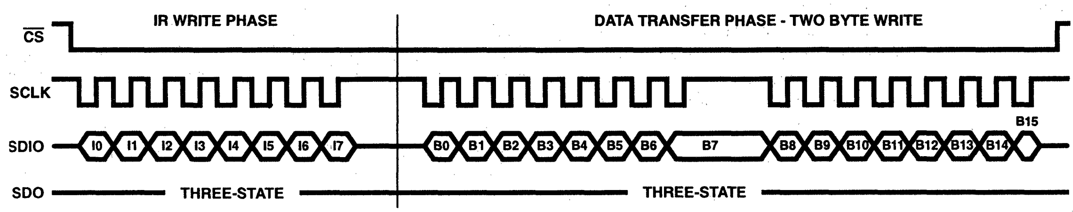


FIGURE 15. DATA WRITE CYCLE, SCLK IDLE HIGH

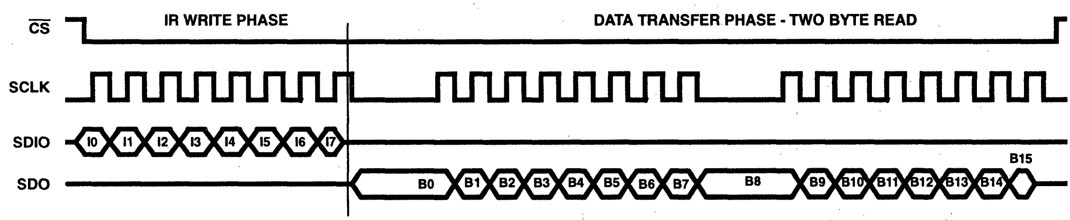


FIGURE 16. DATA READ CYCLE, 3-WIRE CONFIGURATION, SCLK IDLE LOW

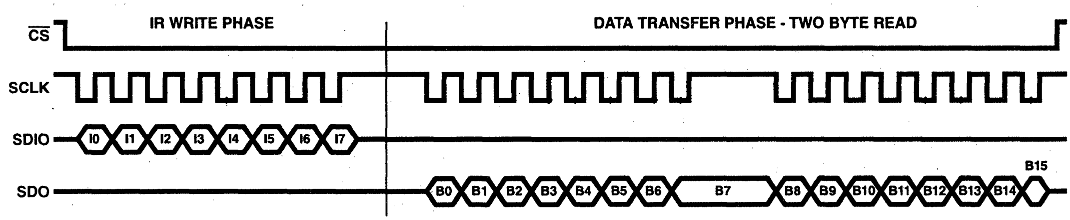


FIGURE 17. DATA READ CYCLE, 3-WIRE CONFIGURATION, SCLK IDLE HIGH

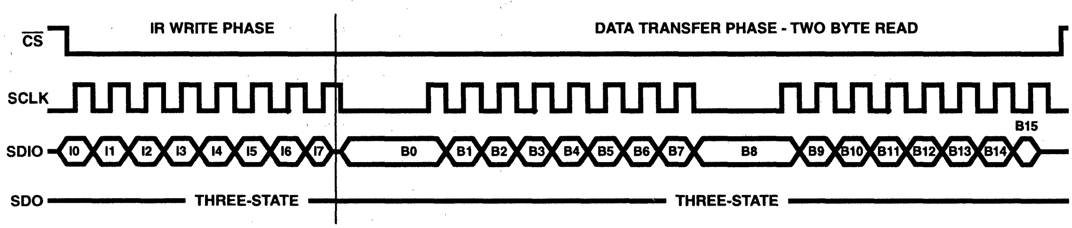


FIGURE 18. DATA READ CYCLE, 2-WIRE CONFIGURATION, SCLK IDLE LOW

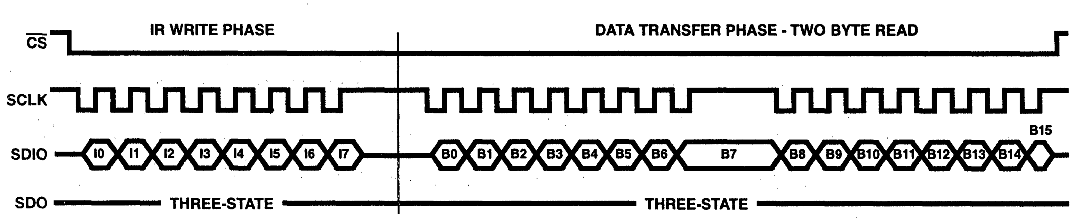


FIGURE 19. DATA READ CYCLE, 2-WIRE CONFIGURATION, SCLK IDLE HIGH

Changing the filter notch frequency, as well as the selected gain, impacts resolution. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch to the filter. For example, if the first notch of the filter is selected at 50Hz then a new word is available at a 50Hz rate or every 20ms. If the first notch is at 1kHz a new word is available every 1ms.

The settling-time of the converter to a full-scale step input change is between 3 and 4 times the data rate. For example, with the first filter notch at 50Hz, the worst case settling time to a full-scale step input change is 80ms. If the first notch is 1kHz, the settling time to a full-scale input step is 4ms maximum.

The -3dB frequency is determined by the programmed first notch frequency according to the relationship:

$f_{-3dB} = 0.262 \times f_{NOTCH}$.

MD2 through MD0 - Bits 11 through 9 are the Operational Modes of the converter. See Table 3 for the Operational Modes description. After a $\overline{\text{RESET}}$ is applied to the part these bits are set to the self calibration mode.

B/$\overline{\text{U}}$ - Bit 8 is the Bipolar/Unipolar select bit. When this bit is set the HI7190 is configured for bipolar operation. When this bit is reset the part is in unipolar mode. This bit is set after a $\overline{\text{RESET}}$ is applied to the part.

G2 through G0 - Bits 7 through 5 select the gain of the input analog signal. The gain is accomplished through a programmable gain instrumentation amplifier that gains up incoming signals from 1 to 8. This is achieved by using a switched capacitor voltage multiplier network preceding the modulator. The higher gains (i.e. 16 to 128) are achieved through a combination of a PGIA gain of 8 and a digital multiply after the digital filter (see Table 6). The gain will affect noise and Signal to Noise Ratio of the conversion. These bits are cleared to a gain of 1 (G2,G1,G0 = 000) after a $\overline{\text{RESET}}$ is applied to the part.

TABLE 7. GAIN SELECT BITS

G2	G1	G0	GAIN	GAIN ACHIEVED
0	0	0	1	PGIA = 1, Filter Multiply = 1
0	0	1	2	PGIA = 2, Filter Multiply = 1
0	1	0	4	PGIA = 4, Filter Multiply = 1
0	1	1	8	PGIA = 8, Filter Multiply = 1
1	0	0	16	PGIA = 8, Filter Multiply = 2
1	0	1	32	PGIA = 8, Filter Multiply = 4
1	1	0	64	PGIA = 8, Filter Multiply = 8
1	1	1	128	PGIA = 8, Filter Multiply = 16

BO - Bit 4 is the Transducer Burn-Out Current source enable bit. When this bit is set (BO = 1) the burn-out current source connected to V_{INHI} internally is enabled. This current source can be used to detect the presence of an external connection to V_{INHI}. This bit is cleared after a $\overline{\text{RESET}}$ is applied to the part.

SB - Bit 3 is the Standby Mode enable bit used to put the HI7190 in a lower power/standby mode. When this bit is set (SB = 1) the filter nodes are halted, the $\overline{\text{DRDY}}$ line is set high and the modulator clock is disabled. When this bit is cleared the HI7190 begins operation as described by the contents of the Control Register. For example, if the Control Register is programmed for Self Calibration Mode and a notch frequency to 10Hz, the HI7190 will perform the self calibration before providing the data at the 10Hz rate. This bit is cleared after a $\overline{\text{RESET}}$ is applied to the part.

BD - Bit 2 is the Byte Direction bit used to select the multi-byte access ordering. The bit determines the either ascending or descending order access for the multi-byte registers. When set (BD = 1) the user can access multi-byte registers in ascending byte order and when cleared (BD = 0) the multi-byte registers are accessed in descending byte order. This bit is cleared after a $\overline{\text{RESET}}$ is applied to the part.

$\overline{\text{MSB}}$ - Bit 1 is used to select whether a serial data transfer is MSB or LSB first. This bit allows the user to change the order that data can be transmitted or received by the HI7190. When this bit is cleared ($\overline{\text{MSB}}$ = 0) the MSB is the first bit in a serial data transfer. If set ($\overline{\text{MSB}}$ = 1), the LSB is the first bit transferred in the serial data stream. This bit is cleared after a $\overline{\text{RESET}}$ is applied to the part.

SDL - Bit 0 is the Serial Data Line control bit. This bit selects the transfer protocol of the serial interface. When this bit is cleared (SDL = 0), both read and write data transfers are done using the SDIO line. When set (SDL = 1), write transfers are done on the SDIO line and read transfers are done on the SDO line. This bit is cleared after a RESET is applied to the part.

Reading the Data Output Register

The HI7190 generates an active low interrupt ($\overline{\text{DRDY}}$) indicating valid conversion results are available for reading. At this time the Data Output Register contains the latest conversion result available from the HI7190. Data integrity is maintained at the serial output port but it is possible to miss a conversion result if the Data Output Register is not read within a given period of time. Maintaining data integrity means that if a Data Output Register read of conversion N is begun but not finished before the next conversion (conversion N+1) is complete, the $\overline{\text{DRDY}}$ line remains active low and the data being read is not overwritten.

In addition to the Data Output Register, the HI7190 has a one conversion result storage buffer. No conversion results will be lost if the following constraints are met.

1) A Data Output Register read cycle is started for a given conversion (conversion X) $1/f_N$ - $(128^*1/f_{OSC})$ after $\overline{\text{DRDY}}$ initially goes active low. Failure to start the read cycle may result in conversion X+1 data overwriting conversion X results. For example, with f_{OSC} = 10MHz, f_N = 2kHz, the read cycle must start within $1/2000 - 128(1/10^6) = 487\mu s$ after $\overline{\text{DRDY}}$ went low.

2) The Data Output Register read cycle for conversion X must be completed within $2(1/f_N)$-$1440(1/f_{OSC})$ after $\overline{\text{DRDY}}$ initially goes active low. If the read cycle for conversion X is not complete within this time the results of conversion X+1 are lost and results from conversion X+2 are now stored in the data output word buffer.

Completing the Data Output Register read cycle inactivates the $\overline{DRDY}$ interrupt. If the one word data output buffer is full when this read is complete this data will be immediately transferred to the Data Output Register and a new $\overline{DRDY}$ interrupt will be issued after the minimum $\overline{DRDY}$ pulse high time is met.

Writing the Control Register

If data is written to byte 2 and/or byte 1 of the Control Register the $\overline{DRDY}$ output is taken high and the device re-calibrates if written to a calibration mode. This action is taken because it is assumed that by writing byte 2 or byte 1 that the user either re-programmed the filter or changed modes of the part. However, if a single data byte is written to byte 0, it is assumed that the gain has NOT been changed. It is up to the user to re-calibrate the HI7190 after the gain has been changed by this method. It is recommended that the entire Control Register be written to when changing the selected gain. This ensures that the part is re-calibrated before the $\overline{DRDY}$ signal goes low indicating valid data is available.

Offset Calibration Register

The Offset Calibration Register is a 24-bit register containing the offset correction factor. This register is indeterminate on power-up but will contain a Self Calibration correction value after a $\overline{RESET}$ has been applied.

BYTE 2

MSB	22	21	20	19	18	17	16
O23	O22	O21	O20	O19	O18	O17	O16

BYTE 1

15	14	13	12	11	10	9	8
O15	O14	O13	O12	O11	O10	O9	O8

BYTE 0

7	6	5	4	3	2	1	LSB
O7	O6	O5	O4	O3	O2	O1	O0

The Offset Calibration Register holds the value that corrects the filter output data to all 0's when the analog input is zero volts.

Positive Full Scale Calibration Register

The Positive Full Scale Calibration Register is a 24-bit register containing the Positive Full Scale correction coefficient. This coefficient is used to determine the positive gain slope factor. This register is indeterminate on power- up but will contain a Self Calibration correction coefficient after a $\overline{RESET}$ has been applied.

BYTE 2

MSB	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16

BYTE 1

15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8

BYTE 0

7	6	5	4	3	2	1	LSB
P7	P6	P5	P4	P3	P2	P1	P0

Negative Full Scale Calibration Register

The Negative Full Scale Calibration Register is a 24-bit register containing the Negative Full Scale correction coefficient. This coefficient is used to determine the negative gain slope factor. This register is indeterminate on power- up but will contain a Self Calibration correction coefficient after a $\overline{RESET}$ has been applied.

BYTE 2

MSB	22	21	20	19	18	17	16
N23	N22	N21	N20	N19	N18	N17	N16

BYTE 1

15	14	13	12	11	10	9	8
N15	N14	N13	N12	N11	N10	N9	N8

BYTE 0

7	6	5	4	3	2	1	LSB
N7	N6	N5	N4	N3	N2	N1	N0

Die Characteristics

DIE DIMENSIONS:
3550μm x 6340μm

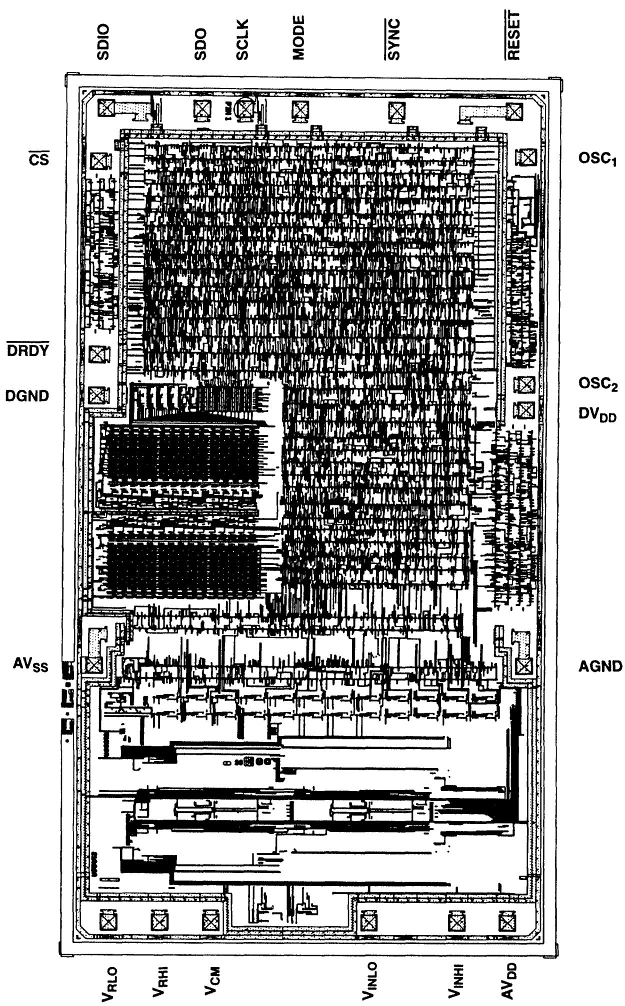
METALLIZATION:
Type: Al Si Cu
Thickness: Metal 2 16kÅ
Metal 1 6kÅ

GLASSIVATION:
Type: Sandwich
Thickness: Nitride 8kÅ
USG 1kÅ

SUBSTRATE POTENTIAL (Powered Up): AV_{SS}

Metallization Mask Layout

HI7190



SIGNAL PROCESSING NEW RELEASES 5

D/A CONVERTERS

HARRIS SEMICONDUCTOR

HI3050

10-Bit, 50 MSPS High Speed 3-Channel D/A Converter

April 1995

Features

- 10-Bit Resolution
- 50 MSPS Throughput Rate
- 3-Channel, RGB, I/O
- RS-343A/RS-170 Compatible Outputs
- Low Power Consumption 500mW (Typ)
- ±0.5 LSB Differential Linearity Error
- Low Glitch Energy
- CMOS Compatible Inputs

Applications

- NTSC, PAL, SECAM Displays
- High Definition Television (HDTV)
- Presentation and Broadcast Video
- Image Processing
- Graphics Displays

Description

The HI3050 is a triple, 10-bit D/A converter, fabricated in a silicon gate CMOS process, ideally suited for RGB video applications.

The converter incorporates three 10-bit input data registers with a common blanking capability, forcing all outputs to 0mA. The HI3050 features low glitch, high impedance current outputs and single 5V supply operation. Low current inputs accept standard TTL/CMOS levels. The architecture is a current cell arrangement providing low differential and integral linearity errors.

The HI3050 requires a 2V external reference and a set resistor to control the output current. The HI3050 also features a chip enable/disable pin for reducing power consumption(<5mW) when the part is not in use.

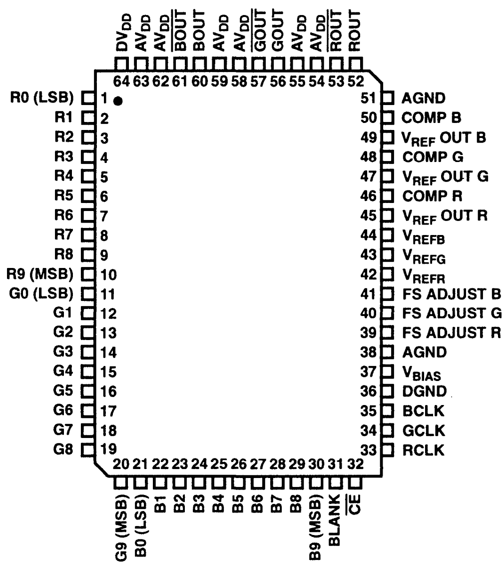
The HI3050 can generate RS-343A and RS-170 compatible video signals into doubly terminated and singly terminated 75Ω loads.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3050JCQ	0°C to +75°C	64 Lead Plastic MQFP

Pinout

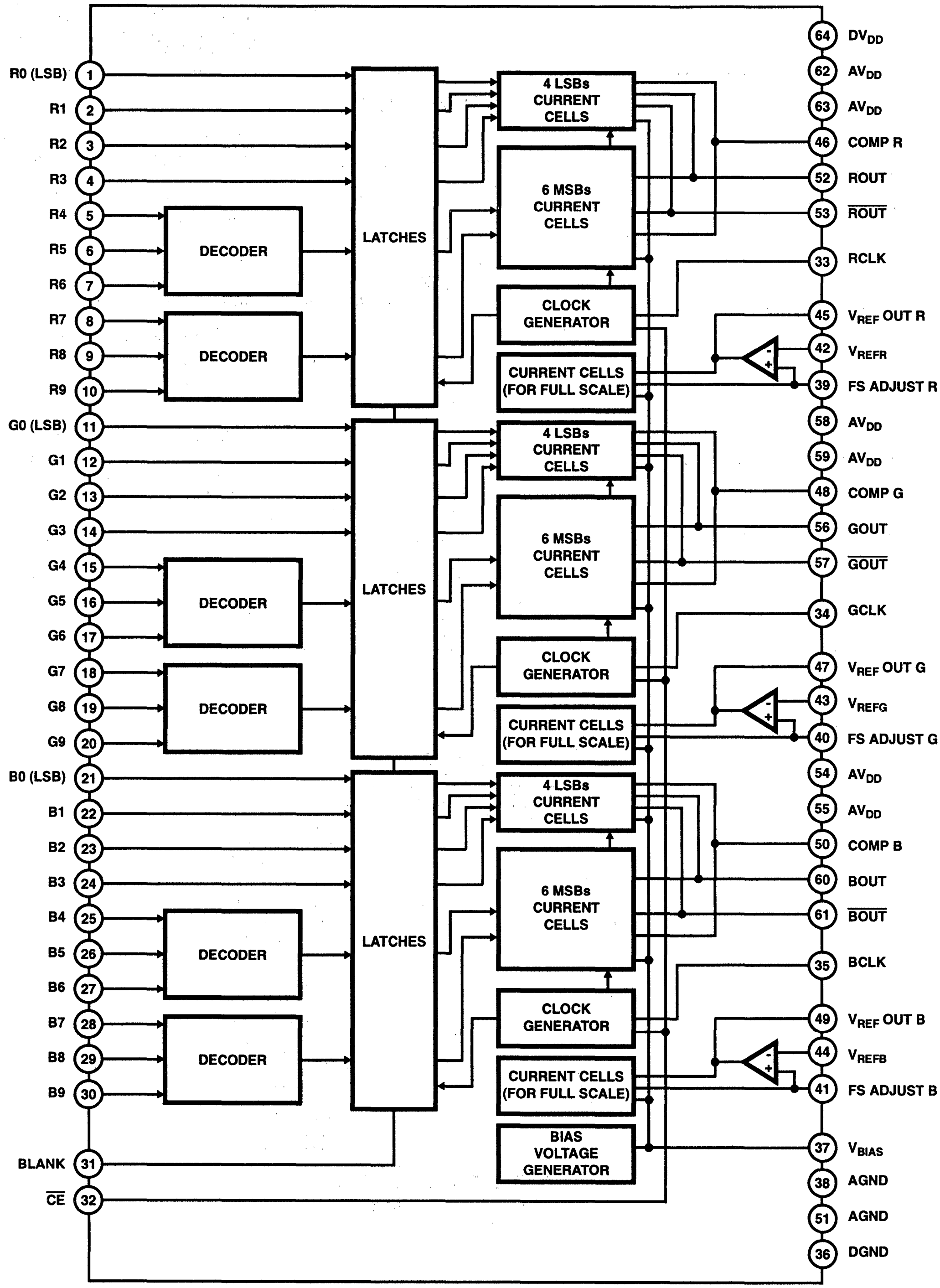
HI3050 (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3936**

Functional Block Diagram



Absolute Maximum Ratings

Digital Supply Voltage, DV_{DD} to DGND . . . . +7V
Analog Supply Voltage, AV_{DD} to AGND . . . . +7V
Digital Input Voltages . . . . DV_{DD} to DGND
Analog Output Current (I_{OUT}) 30mA
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) (Lead Tips Only) . . . . . . +300°C

Thermal Information

Thermal Resistance (See Note 1) θ_{JA}
HI3050JCQ . . . . 80°C/W
Operating Temperature Range
HI3050JCQ . . . . 0°C to +75°C
Maximum Junction Temperature
HI3050JCQ . . . . +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

AV_{DD} = +5V, DV_{DD} = +5V, F_{CLK} = 50MHz, R_L = 75, V_{REF} = 2V, R_{SET} = 1.2K, T_A = +25°C

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	"Best Fit" Straight Line	-2.0	-	2.0	LSB
Differential Linearity Error, DNL		-0.5	-	0.5	LSB
Output Offset Voltage, V_{OS}		-	-	1	mV
Output Full Scale Ratio Error, F_{SRE}	(Note 2)	0	1.5	3	%
Full Scale Output Current, I_{FS}		-	27	30	mA
Full Scale Output Voltage, V_{FS}	$R_L = 75\Omega$	1.8	1.9	2.0	V
Output Voltage Compliance Range		-	2.5	-	V
DYNAMIC CHARACTERISTICS					
Maximum Throughput Rate		50	-	-	MSPS
Glitch Energy, GE	$R_L = 75\Omega$	-	50	-	pV-s
Settling Time	$R_L = 75\Omega$, I_{OUT} = 13.5mA	-	40	-	ns
Crosstalk	10MHz Output Sine Wave	-	54	-	dB
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic Current, I_{IH}		-	-	5	µA
Input Logic Current, I_{IL}		-5	-	-	µA
Digital Input Capacitance, C_{IN}		-	10	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 1	-	5	7	ns
Data Hold Time, t_{HLD}	See Figure 1	-	1	3	ns
Propagation Delay Time, t_{PD}	See Figure 1	-	10	-	ns
Clock Pulse Width, T_{PW1}, T_{PW0}	See Figure 1	10	-	-	ns
POWER SUPPLY CHARACTERISITICS					
Total Supply Current, $AI_{DD} + DI_{DD}$		-	100	110	mA
Analog Supply Current, AI_{DD}		-	92	-	mA
Digital Supply Current, DI_{DD}		-	8	-	mA
Power Dissipation		-	500	550	mW

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Configured for Common Reference.

$$F_{SRE} = \left| \frac{\text{Full Scale Voltage of Channel}}{\text{Average Full Scale Voltage of All Channels}} - 1 \right| \times 100\%$$

5

D/A CONVERTERS

Timing Diagram

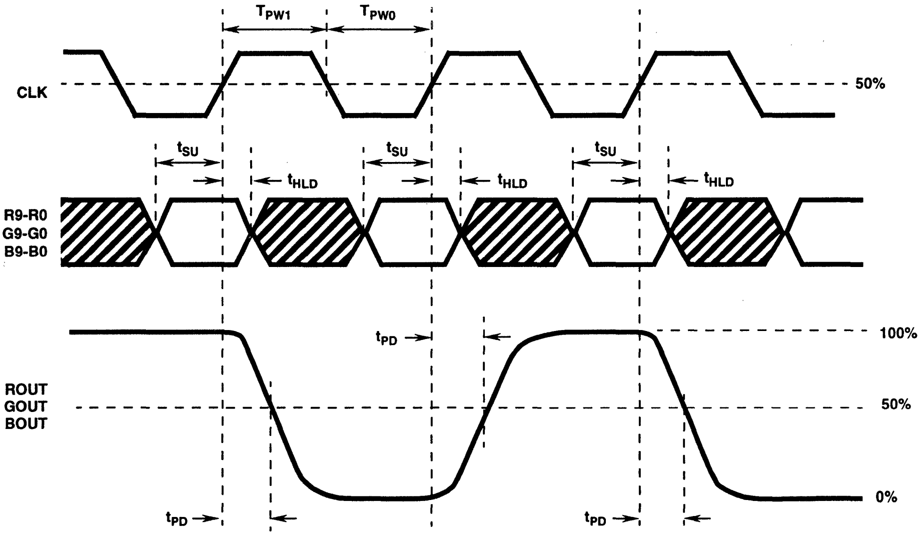


FIGURE 1. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Typical Performance Curves

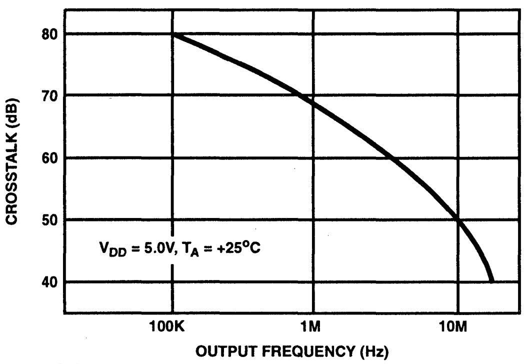


FIGURE 2. OUTPUT FREQUENCY vs CROSSTALK

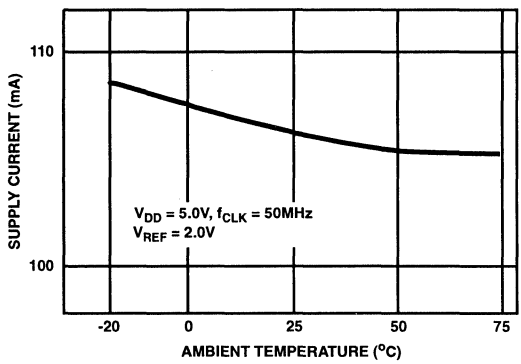


FIGURE 3. SUPPLY CURRENT vs AMBIENT TEMPERATURE

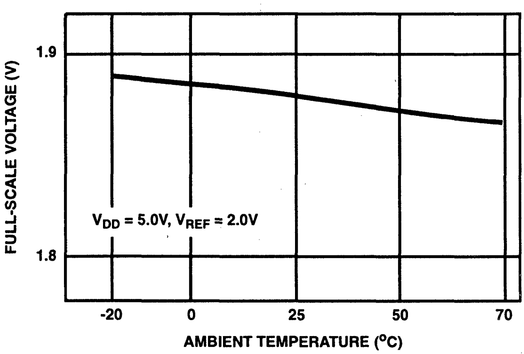


FIGURE 4. FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

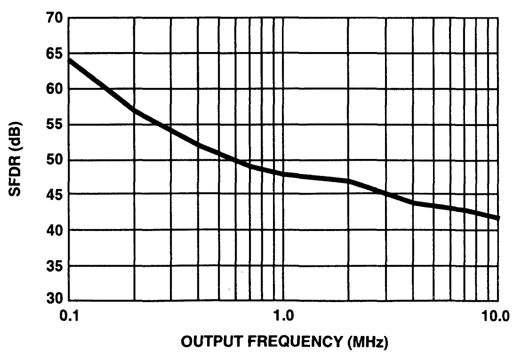
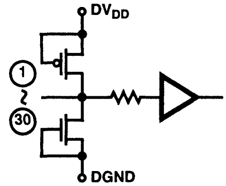
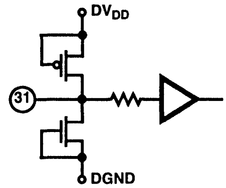
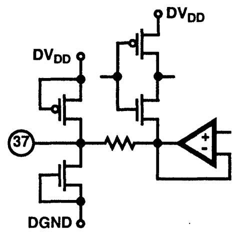
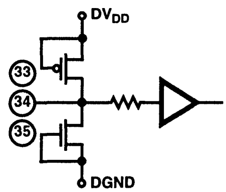
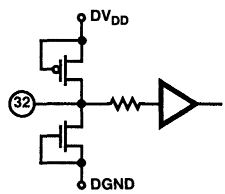
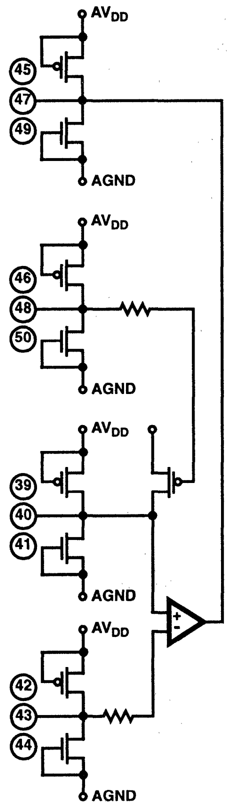
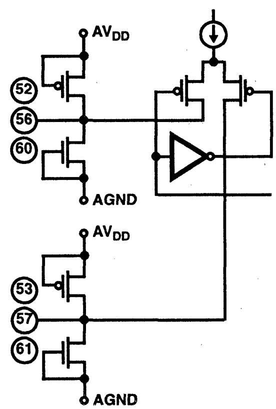


FIGURE 5. SFDR vs OUTPUT FREQUENCY

Pin Description and Equivalent Circuit

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 - 10	R0 - R9		Digital Inputs
11 - 20	G0 - G9		
21 - 30	B0 - B9		
31	BLANK		Output Blanking Input High: Outputs Set to 0mA. Low: Normal Output Operation.
37	V_{BIAS}		Internal Bias Decoupling Connect a 0.1μF decoupling capacitor to DGND.
33	RCLK		Clock Inputs All input pins are TTL/CMOS compatible.
34	GCLK		
35	BCLK		
36	DGND		Digital Ground
38, 51	AGND		Analog Ground
32	$\overline{CE}$		Chip Enable Pin High: Part Disabled Low: Part Enabled
54, 55, 58, 59, 62, 63	AV_{DD}		Analog Power Supply

Pin Description and Equivalent Circuit (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
45	V_{REF} OUT R		Reference Output Typically connected to the Reference Decoupling inputs (COMP R, COMP G, COMP B). See Figures 11 and 12 for various configurations.
47	V_{REF} OUT G		
49	V_{REF} OUT B		
46	COMP R		Reference Decoupling Connect a decoupling capacitor (0.1μF) to reduce noise on reference to AV_{DD}.
48	COMP G		
50	COMP B		
39	FS ADJUST R		Full Scale Adjust Typically connect a 1.2kΩ resistor, R_{SET}, to AGND. R_{SET} is used to determine full scale output current.
40	FS ADJUST G		
41	FS ADJUST B		
42	V_{REFR}		Voltage Reference Input Typically set to 2V and determines full scale output current. $I_{OUT}\text{ (Full Scale)} = \frac{V_{REF}}{R_{SET}} \times 16$
43	V_{REFG}		
44	V_{REFB}		
52	ROUT		Current Outputs
56	GOUT		
60	BOUT		
53	$\overline{ROUT}$		Inverted Current Outputs
57	$\overline{GOUT}$		
61	$\overline{BOUT}$		
64	DV_{DD}		Digital Power Supply

DAC INPUT/OUTPUT CODE TABLE (NOTE 1)

INPUT CODE										
MSB D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0	OUTPUT VOLTAGE
1	1	1	1	1	1	1	1	1	1	2.0V
				• • •						
1	0	0	0	0	0	0	0	0	0	1.0V
				• • •						
0	0	0	0	0	0	0	0	0	0	0V

NOTE:

1. V_{REF} = 2.0V, R_{SET} = 1.2K, R_{LOAD} = 75Ω

Detailed Description

The HI3050 contains three matched, individual, 10-bit current output digital-to-analog converters. The DACs can convert at 50 MSPS and run on +5V for both the analog and digital supplies. The architecture is a current cell arrangement. 10-bit linearity is obtained without laser trimming due to an internal calibration.

Digital Inputs

The digital inputs to the HI3050 have TTL level thresholds. Due to the low input currents CMOS logic can be used as well. The digital inputs are latched on the rising edge of the clock.

To reduce switching noise from the digital data inputs, a series termination resistor is the best solution. Using a 50Ω to 130Ω resistor in series with the data lines, the edge rates are slowed. Slower edge rates reduce the amount of overshoot and undershoot that directly couples through the lead frame of the device. TTL drivers such as the 74ALS or 74F series or CMOS logic series drivers, ACT, AC, or FCT, are excellent for driving the TTL/CMOS inputs of the converter.

Clocks and Termination

The HI3050 clock rate can run to 50MHz, therefore, to minimize reflections and clock noise into the part, proper termination should be considered. In PCB layout clock traces should be kept short and have a minimum of loads. To guarantee consistent results from board to board controlled impedance traces should be used with a characteristic line impedance.

To terminate the clock line, a shunt terminator to an AC ground is the most effective type at a 50MHz clock rate. Shunt termination is best used at the receiving end of the transmission line or as close to the HI3050 CLK pin as possible.

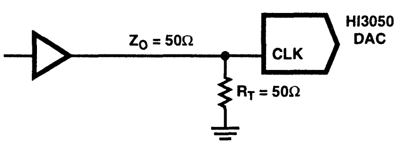


FIGURE 6. AC TERMINATION OF THE HI3050 CLOCK LINE

Rise and fall times and propagation delay of the line will be affected by the Shunt Terminator. The terminator can be connected to DGND.

Power Supplies

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1μF and 0.01μF ceramic capacitors placed as close to the body of the HI3050 as possible on the analog (AV_{DD}) and digital (DV_{DD}) supplies. The analog and digital ground returns should be connected together at the device to ensure proper operation on power up.

Reference

The HI3050 DACs have their own references and can be set individually, see Figure 13. The three references can also share a common reference voltage, see Figure 12. A shared reference gives DAC to DAC matching of 1.5%, typically.

The HI3050 requires an external reference voltage to set the full scale output current. The external reference voltage is connected to the V_{REF} inputs (V_{REFR}, V_{REFG}, and V_{REFB}). The Full Scale Adjust input (FS ADJUST R, FS ADJUST G, FS ADJUST B) should be connected to AGND through a 1.2kΩ resistor, R_{SET}. The reference outputs (V_{REF} OUT R, V_{REF} OUT G, V_{REF} OUT B) should be connected to the decoupling input (COMP R, COMP G, COMP B) and decoupled to AV_{DD} with a 0.1μF capacitor. This improves settling time by decoupling switching noise from the reference output of the HI3050.

The full scale output current is controlled by the voltage reference pin and the set resistor (R_{SET}). The ratio is:

$$I_{OUT} \text{ (Full Scale)} = (V_{REF}/R_{SET}) \times 16,\ I_{OUT} \text{ is in mA} \qquad \text{(EQ.1)}$$

Blanking Input

The BLANK input, when pulled high, will force the outputs of all three DACs to 0mA.

5

D/A CONVERTERS

Chip Enable

The chip enable input, $\overline{CE}$, will shut down the HI3050 causing the outputs to go to 0mA. The analog and digital supply current will decrease to less than 1mA, reducing power for low power applications.

Outputs

The HI3050 DAC outputs are complementary current outputs. Current is steered to either I_{OUT} or $\overline{I_{OUT}}$ in proportion to the digital input code. The current output can be converted to a voltage by using a resistor load or I/V converting op amp. If only one output of a converter is being used, the unused output can be connected to ground or to a load equal to the used output. The output voltage when using a resistor load is:

$$V_{OUT} = I_{OUT} \times R_{OUT} \qquad \text{(EQ. 2)}$$

The compliance range of the outputs is from 0V to +2.5V.

To convert the output current of the D/A converter to a voltage a load resistor followed by a buffer amplifier can be used as shown in Figure 5. The DAC needs a 75Ω termination resistor on the I_{OUT} pin to ensure proper settling.

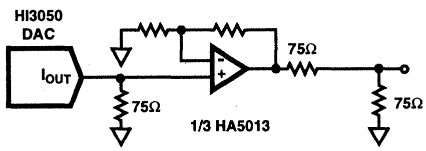


FIGURE 7. HIGH SPEED CURRENT TO VOLTAGE CONVERSION

Glitch

The output glitch of the HI3050 is measured by summing the area under the switching transients after an update of the DAC. Glitch is caused by the time skew between bits of the incoming digital data. Typically the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). Unequal delay paths through the device can also cause one current source to change before another. To minimize this the Harris HI3050 employes an internal register, just prior to the current sources, that is updated on the clock edge.

In measuring the output glitch of the HI3050 the output is terminated into a 75Ω load. The glitch is measured at the major carries throughout the DACs output range.

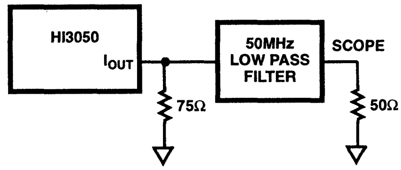
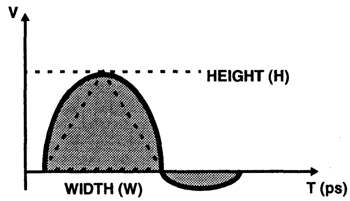


FIGURE 8. GLITCH TEST CIRCUIT

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 9 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt-seconds (pV-sec).



GLITCH AREA = 1/2 (H X W)

FIGURE 9. GLITCH ENERGY

Test Circuits

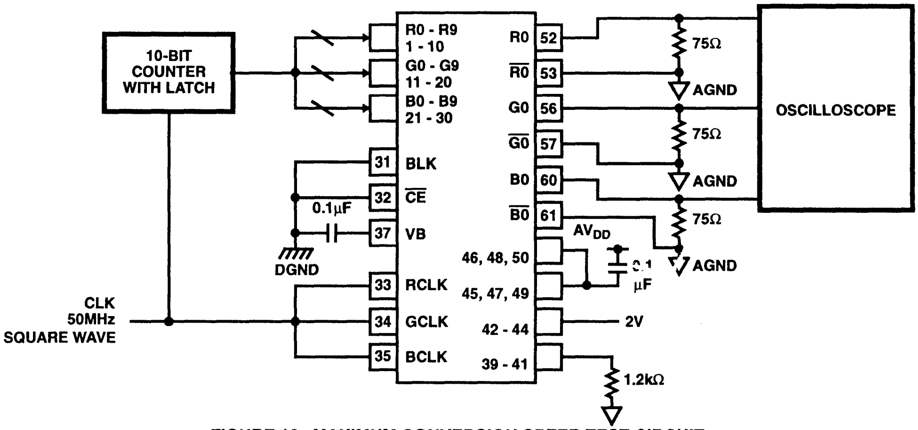


FIGURE 10. MAXIMUM CONVERSION SPEED TEST CIRCUIT

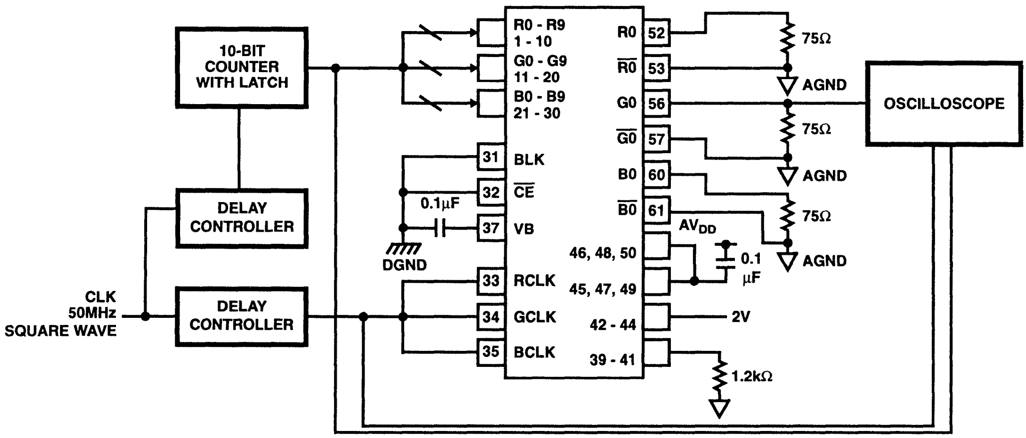


FIGURE 11. SETUP HOLD TIME AND GLITCH ENERGY TEST CIRCUIT

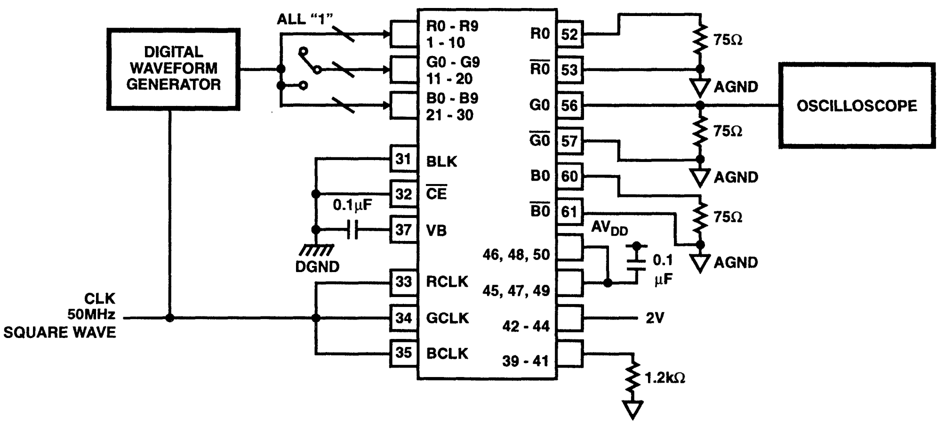


FIGURE 12. CROSSTALK TEST CIRCUIT

Applications Circuits

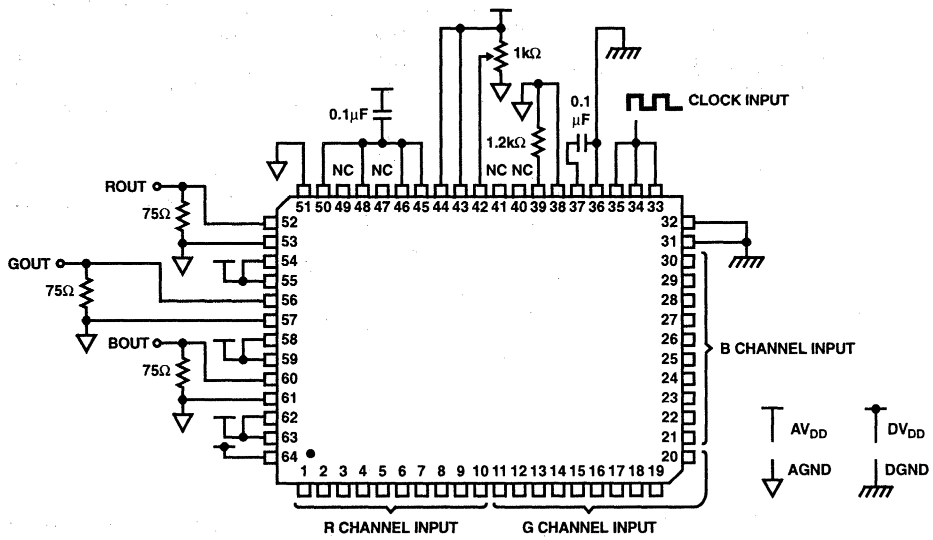


FIGURE 13. COMMON VOLTAGE REFERENCE

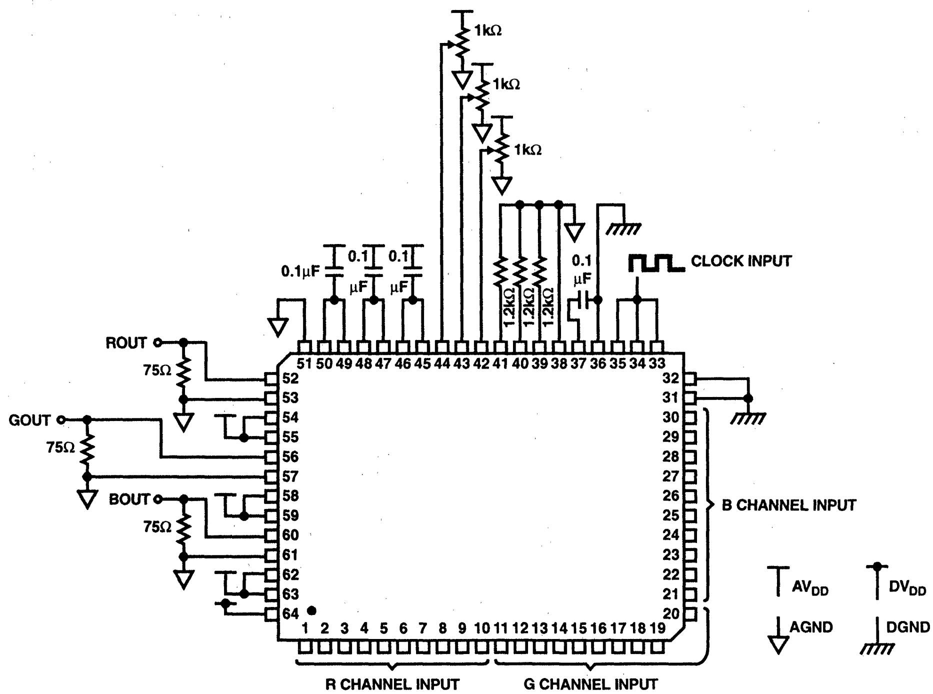


FIGURE 14. INDEPENDENT REFERENCES

Definition of Specifications

Integral Linearity Error (INL) - The measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error (DNL) - The measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Crosstalk - Is the undesirable signal coupling from one channel to another.

Feedthrough - The measure of the undesirable switching noise coupled to the output.

Output Voltage Full Scale Settling Time - The time required from the 50% point on the clock input for a full scale step to settle within an 1/2 LSB error band.

Output Voltage Small Scale Settling Time - The time required from the 50% point on the clock input for a 100mV step to settle within an 1/2 LSB error band. This is used by applications reconstructing highly correlated signals such as sine waves with more than 5 points per cycle.

Glitch Energy (GE) - The switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a Volt-Time specification.

Differential Gain (DG) - Differential Gain is the peak difference in chrominance amplitude (in percent) at two different DC levels.

Differential Phase (DP) - Differential Phase is the peak difference in chrominance phase (in degrees) at two different DC levels.

Signal to Noise Ratio (SNR) - The ratio of a fundamental to the noise floor of the analog output. The first 5 harmonics are ignored, and an output filter of 1/2 the clock frequency is used to eliminate alias products.

Total Harmonic Distortion (THD) - The ratio of the DAC output fundamental to the RMS sum of the harmonics. The first 5 harmonics are included, and an output filter of 1/2 the clock frequency is used to eliminate alias products.

Spurious Free Dynamic Range (SFDR) - The amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at 1/2 the clock frequency to eliminate noise from clocking alias terms.

Intermodulation Distortion (IMD) - The measure of the sum and difference products produced when a two tone input is driven into the D/A. The distortion products created will arise at sum and difference frequencies of the two tones. IMD is

$$IMD = \frac{20 \log (\text{RMS of sum and difference distortion products})}{(\text{RMS amplitude of the fundamental})}$$

HARRIS SEMICONDUCTOR

HI5721

July 1995

10-Bit, 125 MSPS High Speed D/A Converter

Features

- 125 MSPS Throughput Rate
- Low Power - 700mW
- 1.5 LSB Integral Linearity Error
- Low Glitch Energy - 1.5pV-s
- TTL/CMOS Compatible Inputs
- Improved Hold Time - 0.5ns
- Excellent Spurious Free Dynamic Range
- Improved Second Source for the AD9721

Applications

- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- HDTV
- Test Equipment
- High Resolution Imaging Systems
- Arbitrary Waveform Generators

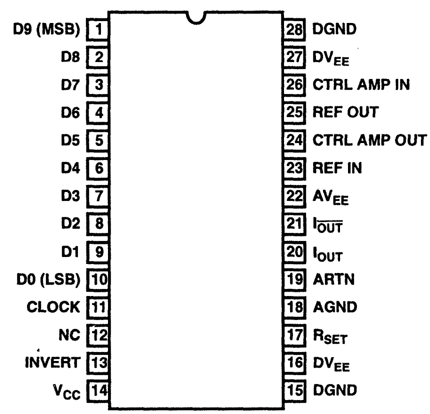
The HI5721 is a 10-bit 125MHz high speed D/A converter. The converter incorporates a 10-bit input data register with quadrature data logic capability, and current outputs. The HI5721 features low glitch energy and excellent frequency domain specifications.

Ordering Information

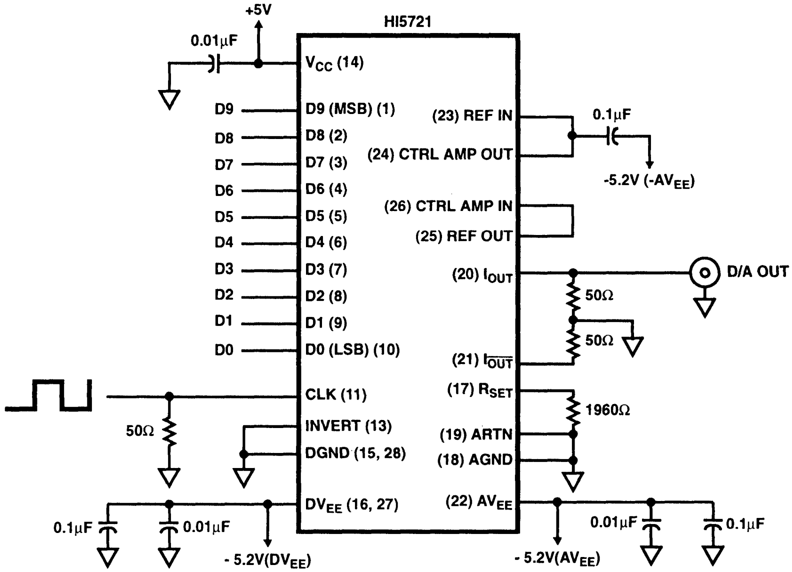
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI5721BIP	-40°C to +85°C	28 Lead PDIP (600 mil)
HI5721BIB	-40°C to +85°C	28 Lead Plastic SOIC (W)

Pinout

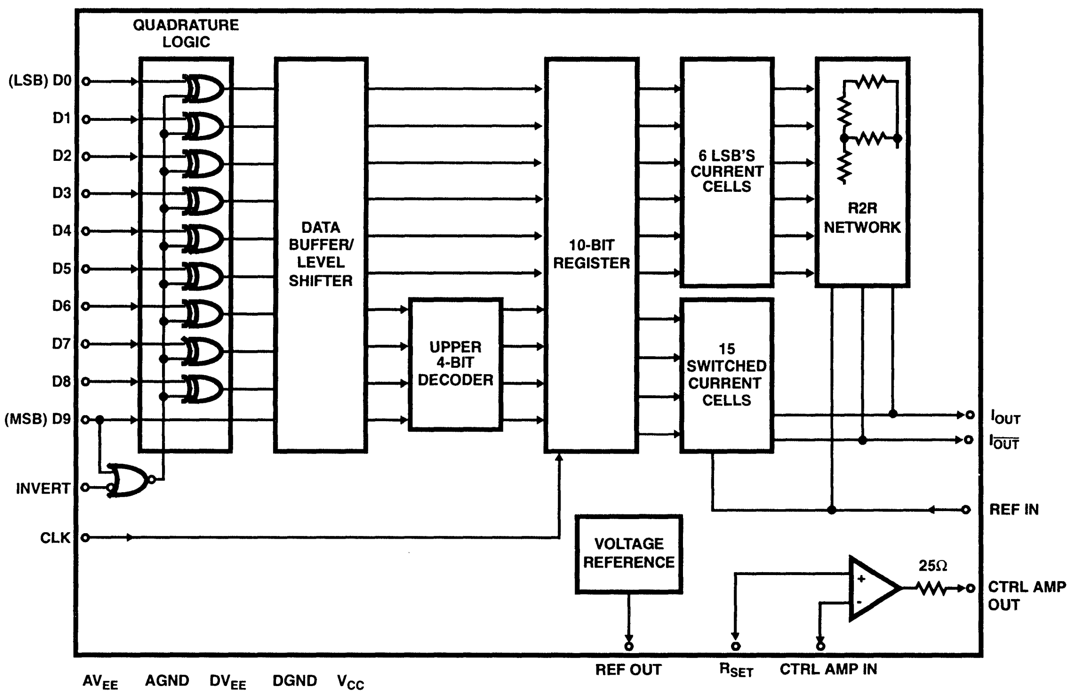
HI5721
(PDIP, SOIC)
TOP VIEW



Typical Applications Circuit



Functional Block Diagram



5

D/A CONVERTERS

Absolute Maximum Ratings

Digital Supply Voltage V_{CC} to DGND .... +5.5V
Negative Digital Supply Voltage DV_{EE} to DGND .... -5.5V
Negative Analog Supply Voltage AV_{EE} to AGND, ARTN ..... -5.5V
Digital Input Voltages (D9-D0, CLK, INVERT) .... V_{CC} to -0.5 V
Internal Reference Output Current 500μA
Control Amplifier Input Voltage Range .... AGND to -4.0V
Control Amplifier Output Current .... ±2.5mA
Reference Input Voltage Range .... -3.7 V to AV_{EE}
Analog Output Current (I_{OUT}) 30mA
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering 10s) .... +300°C
(SOIC - Lead Tips Only)

Thermal Information

Thermal Resistance (See Note 1) θ_{JA}
Plastic DIP Package .... 55°C/W
SOIC Package .... 70°C/W
Maximum Power Dissipation
HI5721BI 750mW
Operating Temperature Range
HI5721BIx .... -40°C to +85°C
Junction Temperature
HI5721BIx .... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, V_{REF} = -1.25V, T_A = see Spec Tables.

PARAMETER	TEST CONDITION	HI5721BI T_A = -40°C to +85°C MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	(Notes 4, 5) ("Best Fit" Straight Line)	-	±0.5	±1.5	LSB
Differential Linearity Error, DNL	(Notes 4, 5)	-	±0.5	±1.0	LSB
Offset Error, I_{OS}	(Notes 4, 5)	-	16	75	μA
Full Scale Gain Error, FSE	(Notes 2, 4, 5)	-	2	15	%
Offset Drift Coefficient	(Note 3)	-	0.1	-	μA/°C
Full Scale Output Current, I_{FS}	(Note 4)	-	-20.48	-	mA
Output Voltage Compliance Range	(Note 3)	-1.5	-	+3.0	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	(Note 3)	125.0	-	-	MSPS
Output Voltage Full Scale Step Settling Time, $t_{SETT\ FS}$	To ±0.5 LSB Error Band R_L = 50Ω (Note 3)	-	4.5	-	ns
Output Voltage Small Step Settling Time, $t_{SETT\ SM}$	100mV Step to ±0.5 LSB Error Band, R_L = 50Ω (Note 3)	-	3.5	-	ns
Singlet Glitch Area, GE (Peak Glitch)	R_L = 50Ω (Note 3)	-	3.5	-	pV-s
Doublet Glitch Area, (Net Glitch)		-	1.5	-	pV-s
Output Slew Rate	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	1,000	-	V/μs
Output Rise Time	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	675	-	ps
Output Fall Time	R_L = 50Ω, DAC Operating in Latched Mode (Note 3)	-	470	-	ps
Spurious Free Dynamic Range, SFDR to Nyquist	f_{CLK} = 125 MHz, f_{OUT} = 2.02MHz, 62.5MHz Span (Notes 3, 6)	-	-59	-	dBc
	f_{CLK} = 125MHz, f_{OUT} = 25MHz, 62.5MHz Span (Notes 3, 6)	-	-53	-	dBc

Electrical Specifications AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, V_{REF} = -1.25V, T_A = see Spec Tables. **(Continued)**

PARAMETER	TEST CONDITION	HI5721BI T_A = -40°C to +85°C MIN	TYP	MAX	UNITS
Spurious Free Dynamic Range, SFDR within a Window	f_{CLK} = 125 MHz, f_{OUT} = 2.02MHz, 2MHz Span (Notes 3, 6)	-	-75	-	dBc
	f_{CLK} = 125MHz, f_{OUT} = 25MHz, 2MHz Span (Notes 3, 6)	-	-70	-	dBc
Spurious Free Dynamic Range, SFDR to Nyquist	f_{CLK} = 100 MHz, f_{OUT} = 2.02MHz, 50MHz Span (Notes 3, 6)	-	-59	-	dBc
	f_{CLK} = 100MHz, f_{OUT} = 25MHz, 50MHz Span (Notes 3, 6)	-	-51	-	dBc
Spurious Free Dynamic Range, SFDR within a Window	f_{CLK} = 100 MHz, f_{OUT} = 2.02MHz, 2MHz Span (Notes 3, 6)	-	-75	-	dBc
	f_{CLK} = 100MHz, f_{OUT} = 25MHz, 2MHz Span (Notes 3, 6)	-	-72	-	dBc
Signal to Noise Ratio (SNR) to Nyquist (Ignoring the first 5 harmonics)	f_{CLK} = 125 MHz, f_{OUT} = 2.02MHz, (Notes 3, 6)	-	54	-	dB
	f_{CLK} = 125MHz, f_{OUT} = 25MHz (Notes 3, 6)	-	51.5	-	dB
Signal to Noise Ratio (SNR) to Nyquist (Ignoring the first 5 harmonics)	f_{CLK} = 100 MHz, f_{OUT} = 2.02MHz, (Notes 3, 6)	-	54.5	-	dB
	f_{CLK} = 100MHz, f_{OUT} = 25MHz (Notes 3, 6)	-	50.3	-	dB
Signal to Noise Ratio + Distortion (SINAD) to Nyquist	f_{CLK} = 125 MHz, f_{OUT} = 2.02MHz, (Notes 3, 6)	-	52.4	-	dB
	f_{CLK} = 125MHz, f_{OUT} = 25MHz (Notes 3, 6)	-	49.2	-	dB
Signal to Noise Ratio + Distortion (SINAD) to Nyquist	f_{CLK} = 100 MHz, f_{OUT} = 2.02MHz, (Notes 3, 6)	-	52.7	-	dB
	f_{CLK} = 100MHz, f_{OUT} = 25MHz (Notes 3, 6)	-	47.6	-	dB
Total Harmonic Distortion (THD) to Nyquist	f_{CLK} = 125 MHz, f_{OUT} = 2.02MHz, (Notes 3, 6)	-	-57.8	-	dBc
	f_{CLK} = 125MHz, f_{OUT} = 25MHz (Notes 3, 6)	-	-53.3	-	dBc
Total Harmonic Distortion (THD) to Nyquist	f_{CLK} = 100 MHz, f_{OUT} = 2.02MHz, (Notes 3, 6)	-	-57.9	-	dBc
	f_{CLK} = 100MHz, f_{OUT} = 25MHz (Notes 3, 6)	-	-51	-	dBc
Intermodulation Distortion (IMD) to Nyquist	f_{CLK} = 125 MHz, f_{OUT1} = 800kHz, f_{OUT2} = 900kHz (Notes 3, 6)	-	57.3	-	dB
Intermodulation Distortion (IMD) to Nyquist	f_{CLK} = 100 MHz, f_{OUT1} = 800kHz, f_{OUT2} = 900kHz (Notes 3, 6)	-	57.2	-	dB

Electrical Specifications AV_{EE}, DV_{EE} = -4.94 to -5.46V, V_{CC} = +4.75 to +5.25V, V_{REF} = -1.25V, T_A = see Spec Tables. **(Continued)**

PARAMETER	TEST CONDITION	HI5721BI T_A = -40°C to +85°C MIN	TYP	MAX	UNITS
REFERENCE/CONTROL AMPLIFIER					
Internal Reference Voltage, V_{REF}	(Notes 4, 5)	-1.15	-1.25	-1.35	V
Internal Reference Voltage Drift	(Note 3)	-	100	-	µV/°C
Internal Reference Output Current Sink/Source Capability	(Note 3)	-50	-	+500	µA
Amplifier Input Impedance	(Note 3)	-	10	-	MΩ
Amplifier Large Signal Bandwidth	4.0V_{P-P} Sine Wave Input, to Slew Rate Limited (Note 3)	-	1	-	MHz
Amplifier Small Signal Bandwidth	1.0V_{P-P} Sine Wave Input, to -3dB Loss (Note 3)	-	10	-	MHz
Reference Input Impedance	(Note 3)	-	4.6	-	kΩ
Reference Input Multiplying Bandwidth	R_L = 50Ω, 100mV Sine Wave, to -3dB Loss at I_{OUT} (Note 3)	-	75	-	MHz
DIGITAL INPUTS (D9-D0, CLK, INVERT)					
Input Logic High Voltage, V_{IH}	(Note 5)	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 5)	-	-	0.8	V
Input Logic Current, I_{IH}	(Note 5)	-	-	400	µA
Input Logic Current, I_{IL}	(Note 5)	-	-	700	µA
Digital Input Capacitance, C_{IN}	(Note 3)	-	3.0	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 3, (Note 3)	2.0	-	-	ns
Data Hold Time, t_{HLD}	See Figure 3, (Note 3)	0.5	-	-	ns
Propagation Delay Time, t_{PD}	See Figure 3, (Note 3)	-	4.5	-	ns
CLK Pulse Width, T_{PW1}, T_{PW2}	See Figure 3, (Note 3)	1.0	0.85	-	ns
POWER SUPPLY CHARACTERISITICS					
IAV_{EE}	(Notes 4, 5)	-	100	110	mA
IDV_{EE}	(Notes 4, 5)	-	-	15	mA
V_{CC}	(Notes 4, 5)	-	14	25	mA
Power Dissipation	(Note 5)	-	700	775	mW
Power Supply Rejection Ratio	V_{CC} ±5%, V_{EE} ±5% (Note 4)	-	50	-	µA/V

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 640µA). Ideally the ratio should be 32.
3. Parameter guaranteed by design or characterization and not production tested.
4. Typical values are test results at T_A = +25°C.
5. All devices are 100% tested at +25°C. 100% productions tested at temperature extremes for military temperature devices, sample tested for industrial temperature devices.
6. Spectral measurements made without external filtering.

Timing Diagrams

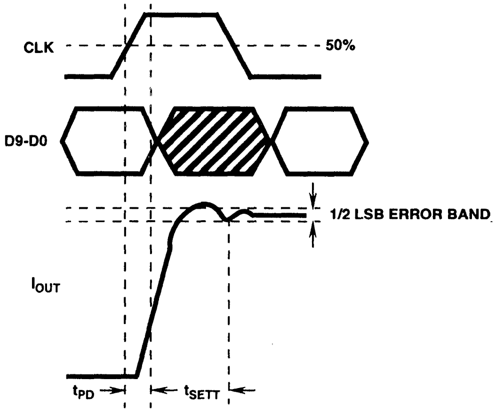


FIGURE 1. FULL SCALE SETTLING TIME DIAGRAM

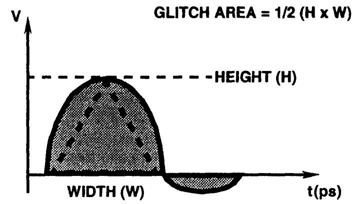


FIGURE 2. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

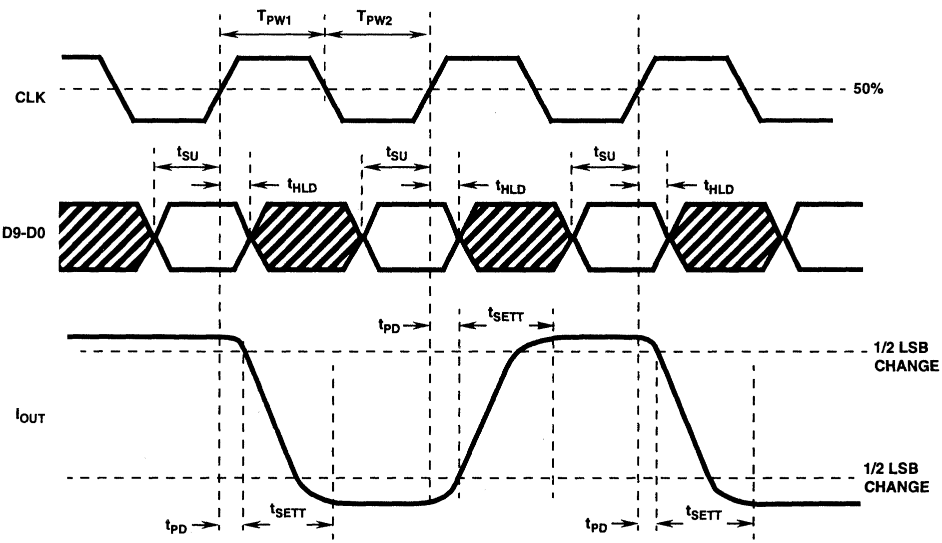


FIGURE 3. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Typical Performance Curves

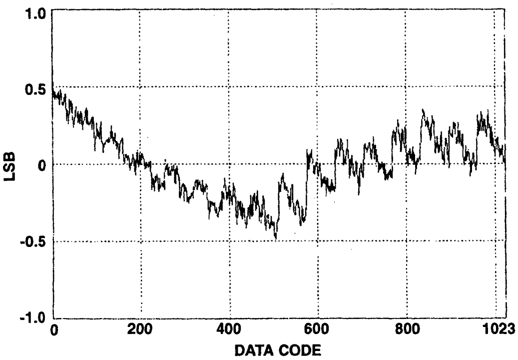


FIGURE 4. INTEGRAL NON-LINEARITY "BEST FIT" STRAIGHT LINE

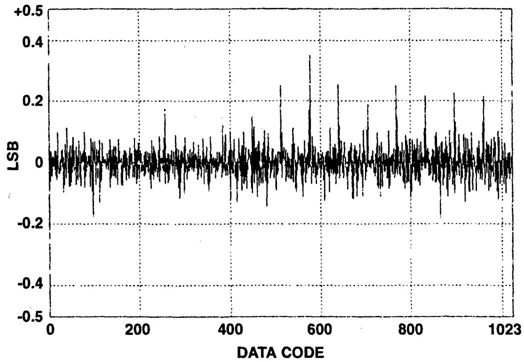


FIGURE 5. DIFFERENTIAL NON-LINEARITY

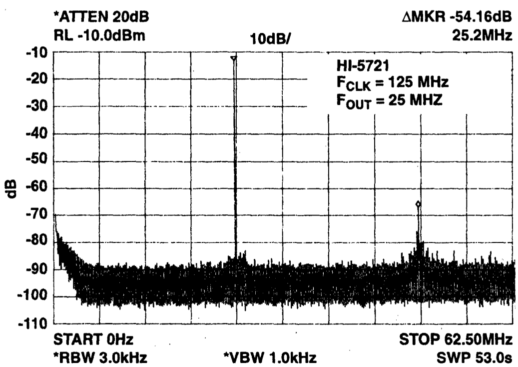


FIGURE 6. SPURIOUS FREE DYNAMIC RANGE TO NYQUIST 25MHz FUNDAMENTAL

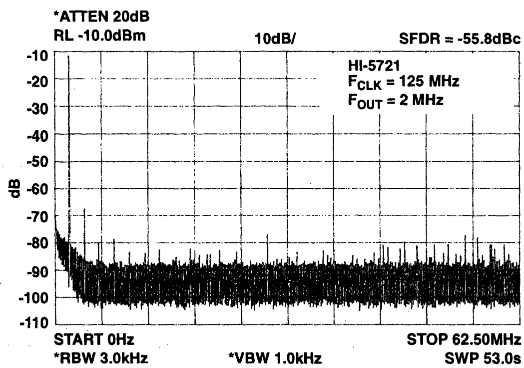


FIGURE 7. SPURIOUS FREE DYNAMIC RANGE TO NYQUIST 2MHz FUNDAMENTAL

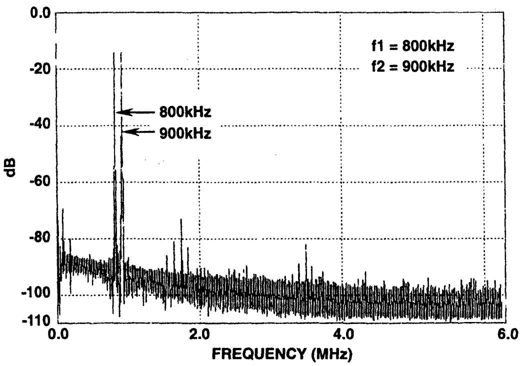


FIGURE 8. INTERMODULATION DISTORTION

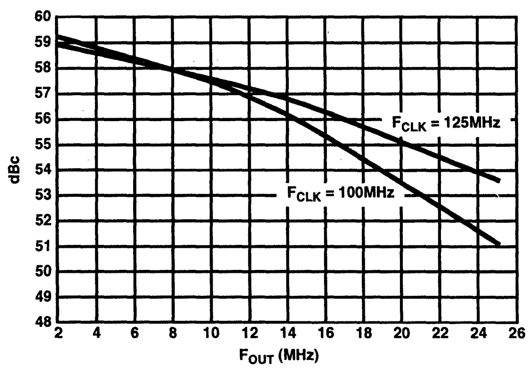


FIGURE 9. SPURIOUS FREE DYNAMIC RANGE (TO NYQUIST) vs OUTPUT FREQUENCY

Typical Performance Curves (Continued)

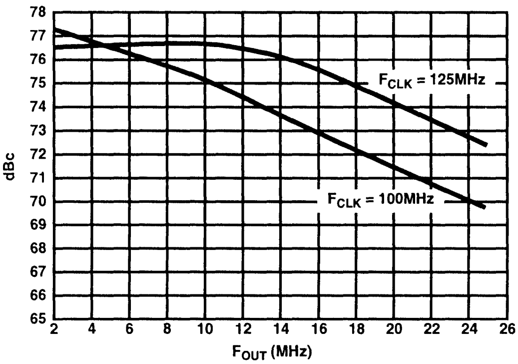


FIGURE 10. SPURIOUS FREE DYNAMIC RANGE (±1MHz WINDOW) vs FREQUENCY

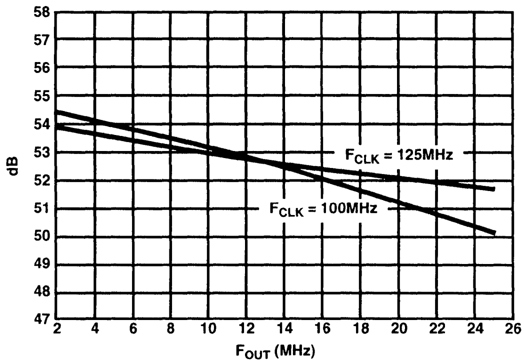


FIGURE 11. SIGNAL TO NOISE RATIO vs OUTPUT FREQUENCY

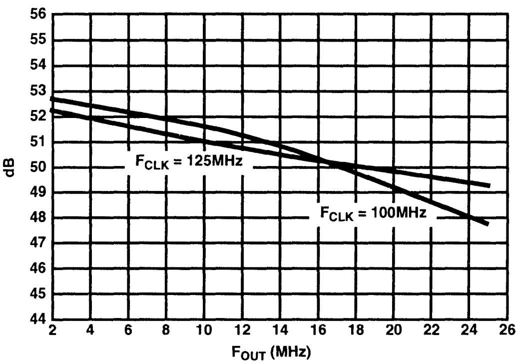


FIGURE 12. SIGNAL TO NOISE + DISTORTION vs OUTPUT FREQUENCY

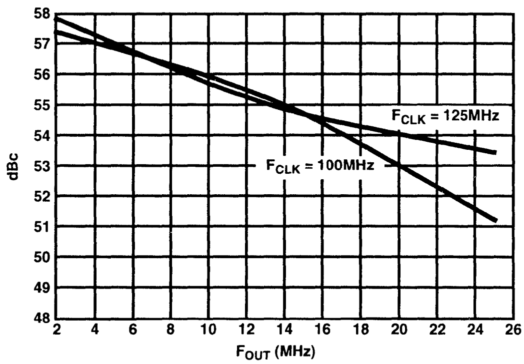


FIGURE 13. TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

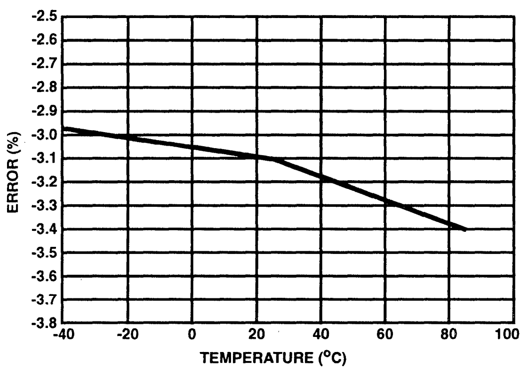


FIGURE 14. GAIN ERROR vs TEMPERATURE

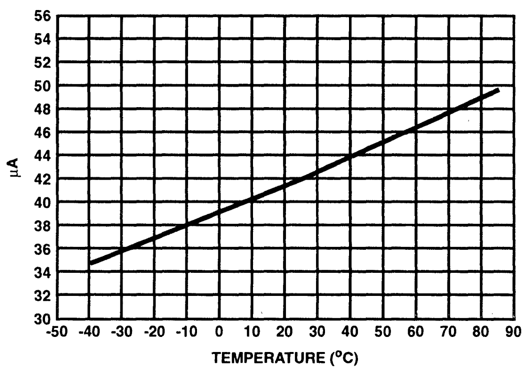


FIGURE 15. OFFSET ERROR vs TEMPERATURE

Typical Performance Curves (Continued)

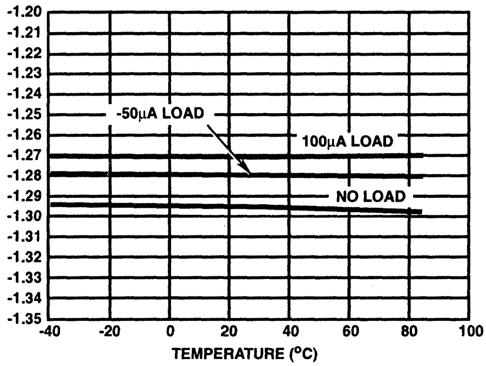
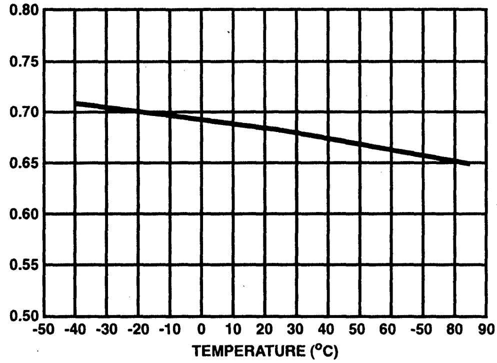


FIGURE 16. REFERENCE VOLTAGE vs TEMPERATURE



NOTE: Clock Frequency does not alter power dissipation.

FIGURE 17. POWER DISSIPATION vs TEMPERATURE

Pin Descriptions

PIN NO.	PIN NAME	PIN DESCRIPTION
1-10	D0 (LSB) through D9 (MSB)	Digital Data Bit 0, the Least Significant Bit through Digital Data Bit 9, the Most Significant Bit
11	CLK	Data Clock Pin 100kHz to 125MHz
12	NC	No Connect
13	INVERT	Data Invert control for bits D0 (LSB) through D8. D9 (MSB) is not affected.
14	V_{CC}	Digital Logic Supply +5V
15, 28	DGND	Digital Ground
16, 27	DV_{EE}	-5.2V Logic Supply
17	R_{SET}	External resistor to set the full scale output current. I_{FS} = 32 x (CTRL AMP IN/R_{SET}). Typically 1960Ω.
18	AGND	Analog Ground supply current return pin
19	ARTN	Analog Signal Return for the R/2R ladder
20	I_{OUT}	Current Output Pin
21	$I_{\overline{OUT}}$	Complementary Current Output Pin
22	AV_{EE}	-5.2V Analog Supply
23	REF IN	Reference Input pin. Typically connected to CTRL AMP OUT and a 0.1μF capacitor should be connected to AV_{EE} to bypass the reference voltage. Provides a reference for the current switching network.
24	CTRL AMP OUT	Control Amplifier Output. Used to convert the internal reference or an external signal to the precision reference current.
25	REF OUT	Internal Reference Output. Output of the internal -1.25V (typical) bandgap voltage reference.
26	CTRL AMP IN	Control Amplifier Input. High impedance, inverting input of the reference control/buffer amplifier.

Detailed Description

The HI5721 is a 10-bit, current out D/A converter. The DAC can convert at 125 MSPS and runs on +5V and -5.2V supplies. The architecture is an R/2R and segmented switching current cell arrangement to reduce glitch and maintain 10-bit linearity without laser trimming. The HI5721 achieves its low power and high speed performance from an advanced BiCMOS process. The HI5721 consumes 700mW (typical) and has an improved hold time of only 0.5ns (typical). The HI5721 is an excellent converter to be used for communications applications and high performance video systems.

Digital Inputs

The HI5721 is a TTL/CMOS compatible D/A. The inputs can be inverted using the INVERT pin. When INVERT is LOW ('0') the input quadrature logic simply passes the data through unchanged.

When INVERT is HIGH ('1') bits D0 (LSB) through D8 are inverted. D9 is not inverted and can be considered a sign bit when enabling this quadrature compatible mode. The INVERT function can simplify the requirements for large sine wave lookup tables in a Numerically Controlled Oscillator. The NCO used in a DDS application would only have to store or generate 90^o of information and then use the INVERT control to control the sign of the output waveform.

Data Buffer/Level Shifters

Data inputs D0 (LSB) through D9 (MSB) are internally translated from TTL to ECL. The internal latch and switching current source controls are implemented in ECL technology to maintain high switching speeds and low noise characteristics.

Decoder/Driver

The architecture employs a split R/2R and Segmented Current source arrangement. Bits D0 (LSB) through D5 directly drive a typical R/2R network to create the binary weighted current sources. Bits D6 through D9 (MSB) pass through a "thermometer" encoder that converters the incoming data into 15 individual segmented current source enables. The split architecture helps to improve glitch while maintaining 10-bit linearity without laser trimming. The worst case glitch is more constant across the entire output transfer function.

Clocks and Termination

The internal 10-bit register is updated on the rising edge of the clock. Since the HI5721 clock rate can run to 125MHz, to minimize reflections and clock noise into the part proper termination should be used. In PCB layout clock runs should be kept short and have a minimum of loads. To guarantee consistent results from board to board controlled impedance PCBs should be used with a characteristic line impedance Z_O of 50Ω.

To terminate the clock line a shunt terminator to ground is the most effective type at a 125MHz clock rate. A typical value for termination can be determined by the equation:

$R_T = Z_O$

for the termination resistor. For a controlled impedance board with a Z_O of 50Ω, the R_T = 50Ω. Shunt termination is best used at the receiving end of the transmission line or as close to the HI5721 CLK pin as possible.

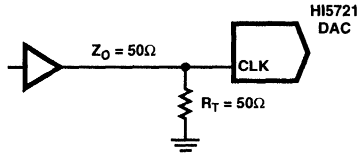


FIGURE 18. AC TERMINATION OF THE HI5721 CLOCK LINE

Rise and Fall times and propagation delay of the line will be affected by the Shunt Terminator. The terminator can be connected to DGND.

Noise Reduction

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1μF and 0.01μF ceramic capacitors placed as close to the body of the HI5721 as possible on the analog (AV_{EE}) and digital (DV_{EE}) supplies. The analog and digital ground returns should be connected together back at the device to ensure proper operation on power up. The V_{CC} power pin should be decoupled with a 0.1μF capacitor.

Reference

The internal reference in the HI5721 is a -1.25V (typical) bandgap voltage reference with a 100μV/°C temperature drift (typical). The internal reference should be buffered by the Control Amplifier to provide adequate drive for the segmented current cells and the R/2R resistor ladder. Reference Out (REF OUT) should be connected to the Control Amplifier Input (CTRL AMP IN). The Control Amplifier Output (CTRL AMP OUT) should be used to drive the Reference Input (REF IN) and a 0.1μF capacitor to analog V- (AV_{EE}). This improves settling time by decoupling switching noise from the analog output of the HI5721.

The Full Scale Output Current is controlled by the CTRL AMP IN pin and the set resistor (R_{SET}). The ratio is:

I_{OUT} (Full Scale) = ($V_{CTRL\ AMP\ IN}/R_{SET}$) x 32

Multiplying Capability

The HI5721 can operate in two different multiplying configurations. First, using the CTRL AMP IN input pin, a -0.6V to -1.2V signal can be applied with a bandwidth up to 1MHz. To increase the multiplying bandwidth, the 0.1μF capacitor connected from REF IN to AV_{EE} can be reduced.

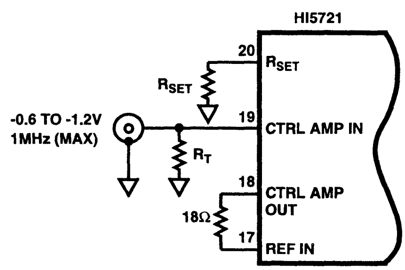


FIGURE 19. LOW FREQUENCY MULTIPLYING CIRCUIT

If higher multiplying frequencies are desired, the reference input can be directly driven. The analog signal range is -3.3V to -4.25V. The multiplying signal must be capacitively coupled into REF IN onto a DC bias between -3.3V to -4.25V (-3.8V typically).

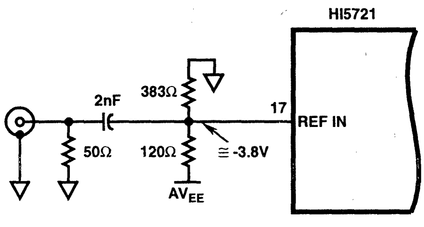


FIGURE 20. WIDEBAND MULTIPLYING CIRCUIT

Outputs

The outputs I_{OUT} and $I_{\overline{OUT}}$ are complementary current outputs. Current is steered to either I_{OUT} or $I_{\overline{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full scale current minus one LSB. The current output can be converted to a voltage by using a resistor load. Both current outputs should have the same load (50Ω typically). The output voltage is:

$$V_{OUT} = I_{OUT} \times R_{OUT}$$

The compliance range of the outputs is from -1.5V to +3.0V.

Glitch

TABLE 1. INPUT CODING vs CURRENT OUTPUT

INPUT CODE (D9-D0)	I_{OUT} (mA)	$I_{\overline{OUT}}$ (mA)
11 1111 1111	-20.48	0
10 0000 0000	-10.24	-10.24
00 0000 0000	0	-20.48

The output glitch of the HI5721 is measured by summing the area under the switching transients after an update of the DAC. Glitch is caused by the time skew between bits of the incoming digital data. Typically the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). Unequal delay paths through the device can also cause one current source to change before another. To minimize this the Harris HI5721 employes an internal register, just prior to the current sources, that is updated on the clock edge. Lastly the worst case glitch usually happens at the major transition i.e. 01 1111 1111 to 10 0000 0000. But in the HI5721 the glitch is moved to the 00 0001 1111 to 11 1110 0000 transition. This is achieved by the split R/2R segmented current source architecture. This decreases the amount of current switching at any one time and makes the glitch practically constant over the entire output range. By making the glitch a constant size over the entire output range this effectively integrates this error out of the end application.

In measuring the output glitch of the HI5721 the output is terminated into a 50Ω load. The glitch is measured at the major carry's throughout the DACs output range.

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 21 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt-seconds (pV-s).

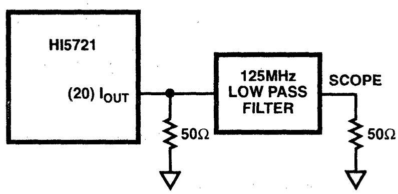


FIGURE 21. GLITCH TEST CIRCUIT

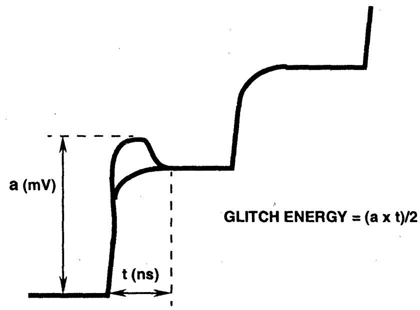


FIGURE 22. GLITCH ENERGY

Applications

Voltage Conversion of the Output

To convert the output current of the D/A converter, to a voltage an amplifier should be used as shown in Figure 23 below. The DAC needs a 50Ω termination resistor on the I_{OUT} pin to ensure proper settling. The HFA1110 has an internal feedback resistor to compensate for high frequency operation.

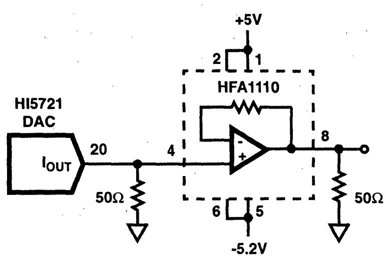


FIGURE 23. HIGH SPEED CURRENT TO VOLTAGE CONVERSION

Bipolar Applications

To convert the output to a bipolar 2.0V output swing the following applications circuit is recommended. The Reference can only provide 100μA of drive, so it must be buffered to create the bipolar offset current needed to generate -2.5V output with all bits 'off'. The output current must be converted to a voltage and then gained up and offset to produce the proper swing. Care must be taken to compensate for the output voltage swing and error.

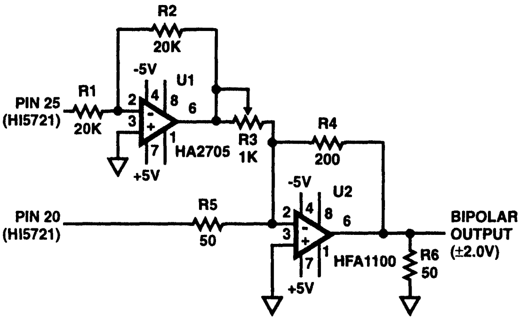


FIGURE 24. BIPOLAR OUTPUT CONFIGURATION

Interfacing to the HSP45106 NCO-16

The HSP45106 is a 16-bit output Numerically Controlled Oscillator (NCO). The HSP45106 can be used to generate various modulation schemes for Direct Digital Synthesis (DDS) applications. Figure 25 shows how to interface an HI5721 to the HSP45106.

Interfacing to the HSP45102 NCO-12

The HSP45102 is a 12-bit output Numerically Controlled Oscillator (NCO). The HSP45102 can be used to generate various modulation schemes for Direct Digital Synthesis (DDS) applications. Figure 26 shows how to interface an HI5721 to the HSP45102.

This high level block diagram is that of a basic PSK modulator. In this example the encoder generates the PSK waveform by driving the Phase Modulation Inputs (P1, P0) of the HSP45102. The P1-0 inputs impart a phase shift to the carrier wave as defined in Table 2.

TABLE 2. PHASE MODULATION INPUT CODING

P1	P0	PHASE SHIFT
0	0	0°
0	1	90°
1	0	270°
1	1	180°

The 10 MSB's of the HSP45102 drive the 10-bit HI5721 DAC which converts the NCO output into an analog waveform. The output filter connected to the DAC can be tailored to remove unwanted spurs for the desired carrier frequency. The controller is used to load the desired center frequency and control the HSP45102. The HI5721 coupled with the HSP45102 make an inexpensive PSK modulator with Spurious Free operation down to -76dBc.

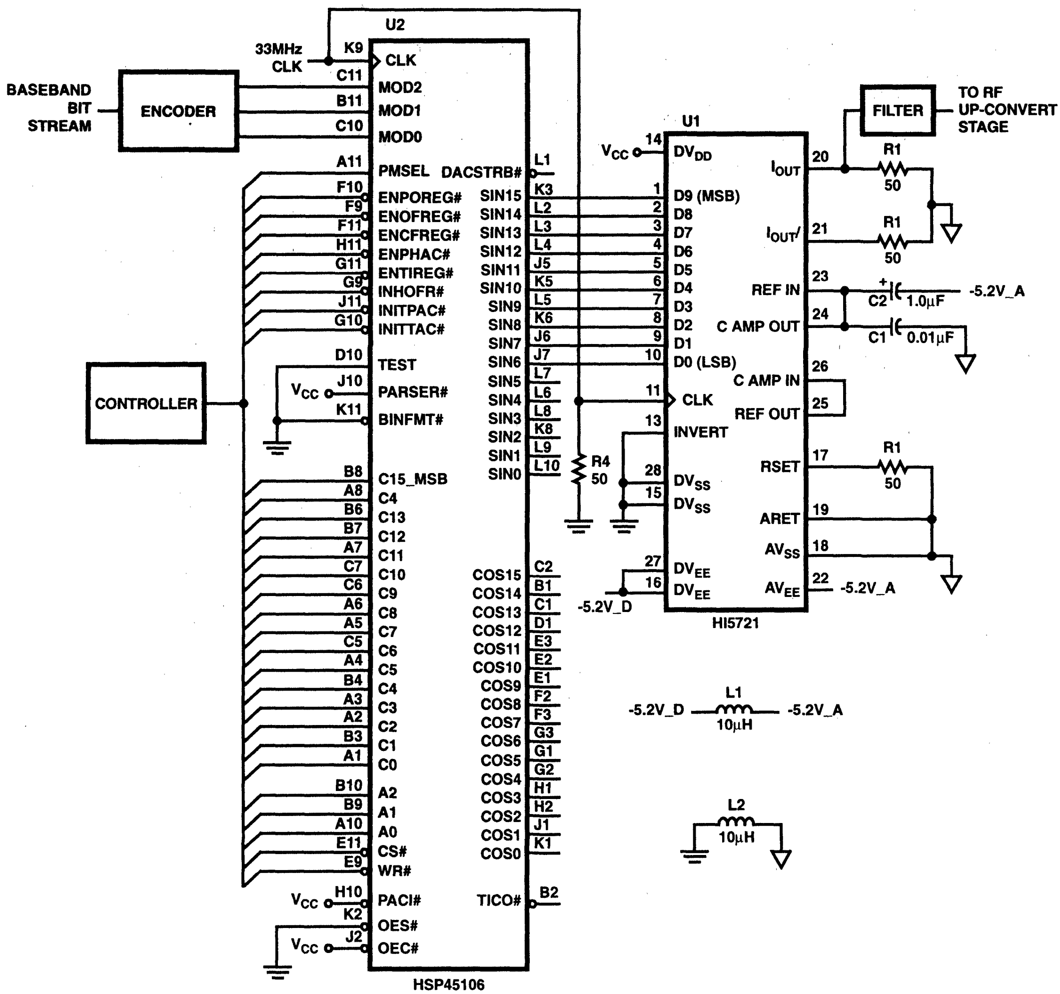


FIGURE 25. PSK MODULATOR USING THE HI5721 AND THE HSP45106 12-BIT NCO

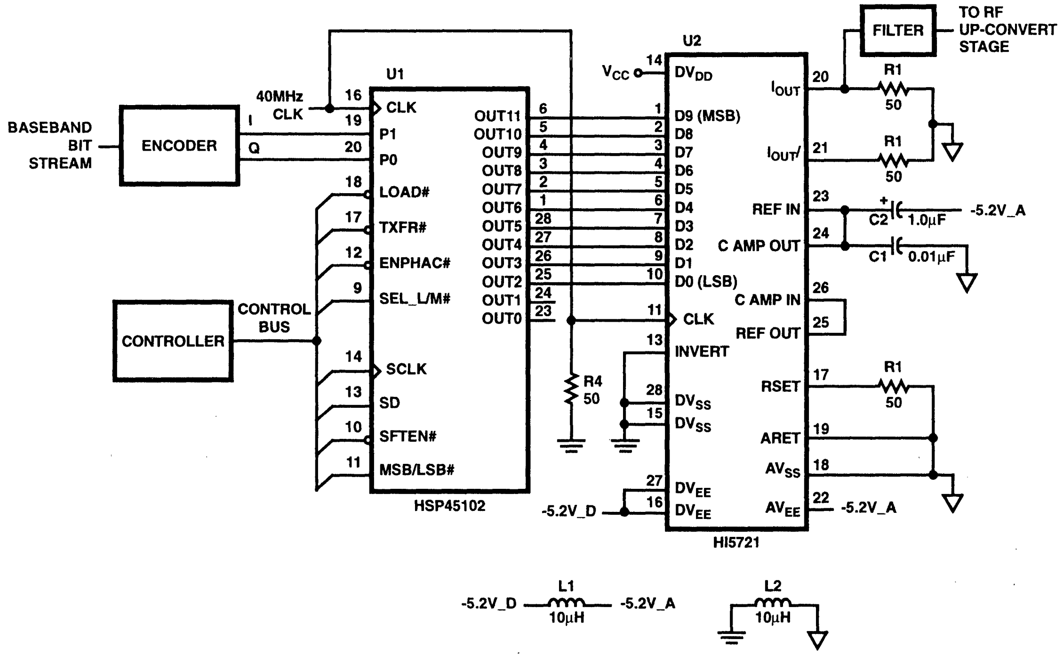


FIGURE 26. PSK MODULATOR USING THE HI5721 AND THE HSP45102 12-BIT NCO

Definition of Specifications

Integral Linearity Error, INL is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Feedthru, is the measure of the undesirable switching noise coupled to the output.

Output Voltage Full Scale Settling Time, is the time required from the 50% point on the clock input for a full scale step to settle within an 1/2 LSB error band.

Output Voltage Small Scale Settling Time, is the time required from the 50% point on the clock input for a 100mV step to settle within an 1/2 LSB error band. This is used by applications reconstructing highly correlated signals such as sine waves with more than 5 points per cycle.

Glitch Area, GE is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a Volt-Time specification.

Differential Gain, ΔA_V is the gain error from an ideal sine wave with a normalized amplitude.

Differential Phase, $\Delta\Phi$ is the phase error from and ideal sine wave.

Signal to Noise Ratio, SNR is the ratio of a fundamental to the noise floor of the analog output. The first 5 harmonics are ignored, and an output filter of 1/2 the clock frequency is used to eliminate alias products.

Total Harmonic Distortion, THD is the ratio of the DAC output fundamental to the RMS sum of the harmonics. The first 5 harmonics are included, and an output filter of 1/2 the clock frequency is used to eliminate alias products.

Spurious Free Dynamic Range, SFDR is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at 1/2 the clock frequency to eliminate noise from clocking alias terms.

Intermodulation Distortion, IMD is the measure of the sum and difference products produced when a two tone input is driven into the D/A. The distortion products created will arise at sum and difference frequencies of the two tones. IMD is

$$\text{IMD} = \frac{20\log\ (\text{RMS of sum and difference distortion products})}{(\text{RMS amplitude of the fundamental.})}$$

HARRIS SEMICONDUCTOR

HI5780

PRELIMINARY

June 1995

10-Bit, 80 MSPS High Speed, Low Power D/A Converter

Features

- 80 MSPS Throughput Rate
- Low Power - 150mW
- ±0.5 LSB Differential Linearity Error
- TTL/CMOS Compatible Inputs
- Built in Bandgap Voltage Reference
- Power Down and Blanking Control Pins

Applications

- Wireless Communications
- Direct Digital Frequency Synthesis
- Signal Reconstruction
- Test Equipment
- High Resolution Imaging and Graphics Systems
- Arbitrary Waveform Generators

Description

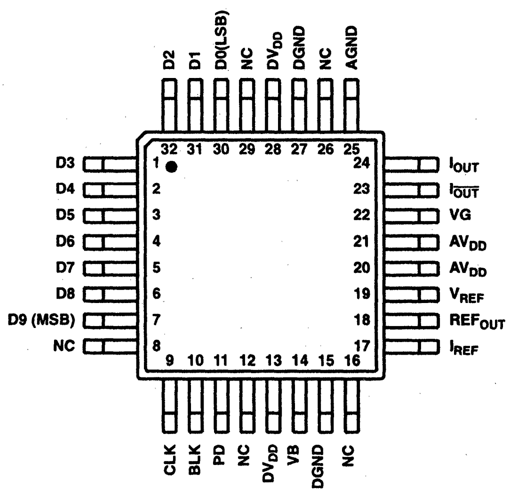
The HI5780 is a 10-bit 80MHz high speed, low power D/A converter. The converter incorporates a 10-bit input data register with current outputs. The HI5780 includes a power down feature that reduces power consumption and a blanking control. The on chip bandgap reference can be used to set the output current range of the D/A.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI5780JCQ	-20°C to +75°C	32 Lead Plastic MQFP

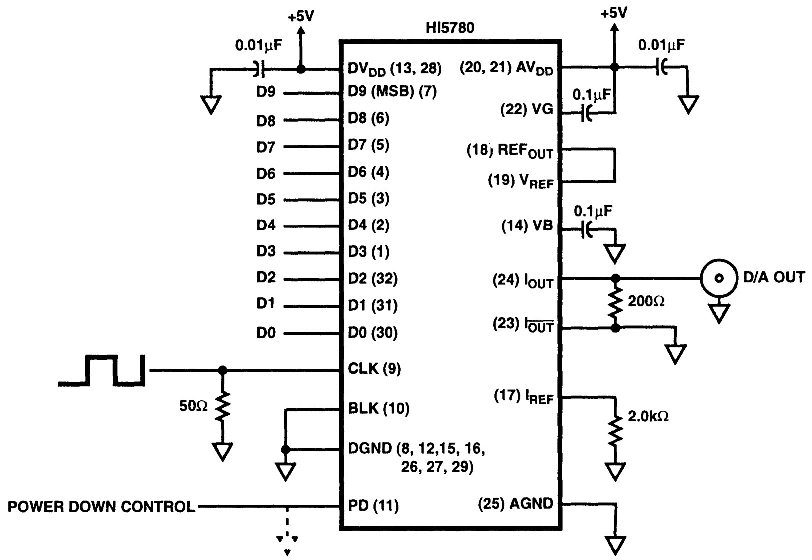
Pinout

HI5780
(MQFP)
TOP VIEW

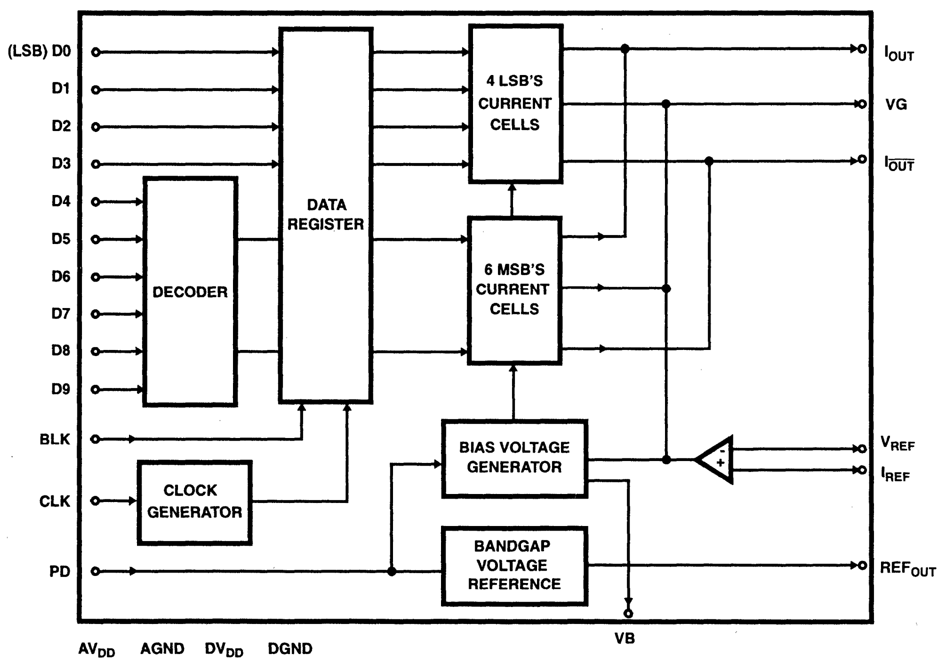


File Number **4024**

Typical Application Circuit



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage V_{DD} to DGND . . . . +7.0V
Digital Input Voltages (D9-D0, CLK, BLANK, PD) . . . . V_{DD} to -0.5V
Internal Reference Output Current . . . . ±2.5mA
Reference Input Voltage Range (V_{REF}) . . . . V_{DD} to -0.5 V
Analog Output Current (I_{OUT}) 15mA
Storage Temperature Range . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) (Lead Tips Only) . . . . . . +300°C

Thermal Information

Thermal Resistance (Note 1) θ_{JA}
Plastic Quad Flatpack Package. . . . . 122°C/W
Maximum Power Dissipation
HI5780BI 180mW
Operating Temperature Range
HI5780BIx . . . . -20°C to +75°C
Junction Temperature
HI5780BIx . . . . +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

AV_{DD}, DV_{DD} = 5.00V, V_{REF} = 2.00V, f_{CLK} = 80MHz, R_{LOAD} = 200Ω, R_{REF} = 3.3kΩ, T_A = 25°C

PARAMETER	TEST CONDITION	HI5780BI MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	(Notes 4, 5) ("Best Fit" Straight Line)	-	-	2.0	LSB
Differential Linearity Error, DNL	(Notes 4, 5)	-	-	0.5	LSB
Offset Error, I_{OS}	(Notes 4, 5)	-	-	5	µA
Full Scale Output Current, I_{FS}	(Note 4)	9.0	9.6	10	mA
Full Scale Drift Coefficient, I_{DRIFT}	(Note 2)	-	0.26	-	mV/°C
Output Voltage Compliance Range	(Note 3)	1.8	1.92	2.0	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	(Note 3)	80.0	-	-	MSPS
Output Voltage Full Scale Step Settling Time, $t_{SETT\ FS}$	To ±0.5 LSB Error Band R_L = 50Ω (Note 3)	-	TBD	-	ns
Singlet Glitch Area, GE (Peak)	R_{LOAD} = 100Ω, V_{OUT} = 1.0 V_{P-P} (Note 3)	-	50	-	pV-s
Differential Gain, DG	(Note 4)	-	2.5	-	%
Differential Phase, DP	(Note 4)	-	1.3	-	Degrees
Spurious Free Dynamic Range, SFDR to Nyquist	f_{CLK} = 80MHz, f_{OUT} = 2.02MHz, 40MHz Span (Note 3)	-	TBD	-	dBc
	f_{CLK} = 80MHz, f_{OUT} = 25MHz, 40MHz Span (Note 3)	-	TBD	-	dBc
Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 80MHz, f_{OUT} = 2.02MHz, 2MHz Span (Note 3)	-	TBD	-	dBc
	f_{CLK} = 80MHz, f_{OUT} = 25MHz, 2MHz Span (Note 3)	-	TBD	-	dBc
REFERENCE					
Internal Reference Voltage, REF_{OUT}	(Notes 4, 5)	1.0	-	1.3	V
Internal Reference Voltage Drift	(Note 3)	-	0.34	-	mV/°C
Reference Input Voltage Range, V_{REF}	(Note 3)	0.5	-	2.0	V
DIGITAL INPUTS (D9-D0, CLK, BLK, PD)					
Input Logic High Voltage, V_{IH}	(Note 5)	2.15	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 5)	-	-	0.85	V
Input Logic Current, I_{IH}	(Note 5)	-	-	5	µA
Input Logic Current, I_{IL}	(Note 5)	-5	-	-	µA
Digital Input Capacitance, C_{IN}	(Note 3)	-	3.0	-	pF

Electrical Specifications AV_{DD}, DV_{DD} = 5.00V, V_{REF} = 2.00V, f_{CLK} = 80MHz, R_{LOAD} = 200Ω, R_{REF} = 3.3kΩ, T_A = 25°C **(Continued)**

PARAMETER	TEST CONDITION	HI5780BI MIN	HI5780BI TYP	HI5780BI MAX	UNITS
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 1, (Note 3)	5.0	-	-	ns
Data Hold Time, t_{HLD}	See Figure 1, (Note 3)	1.0	-	-	ns
Propagation Delay Time, t_{PD}	See Figure 1, (Note 3)	-	10	-	ns
CLK Pulse Width, T_{PW1}, T_{PW2}	See Figure 1, (Note 3)	6.25	-	-	ns
POWER SUPPLY CHARACTERISTICS					
IAV_{DD}	(Notes 4, 5)	-	-	15	mA
IDV_{DD}	(Notes 4, 5)	-	-	15	mA
Power Dissipation	(Note 5)	-	-	150	mW
Sleep Mode Power Consumption	PD = 0 (Note 4)	-	TBD	TBD	mW

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. R_{LOAD} is connected to I_{OUT} (pin 24) and R_{REF} is connected to I_{REF} (pin 17).
3. Parameter guaranteed by design or characterization and not production tested.
4. Typical values are test results at T_A = +25°C.
5. All devices are 100% tested at +25°C.

Timing Diagrams

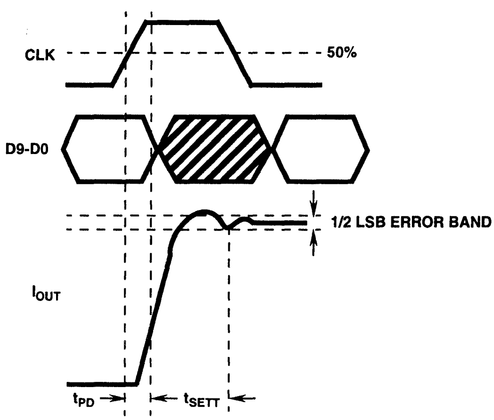


FIGURE 1. FULL SCALE SETTLING TIME DIAGRAM

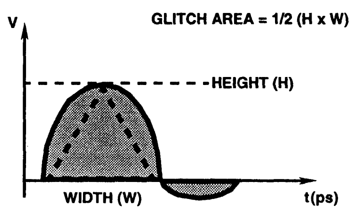


FIGURE 2. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

Timing Diagrams (Continued)

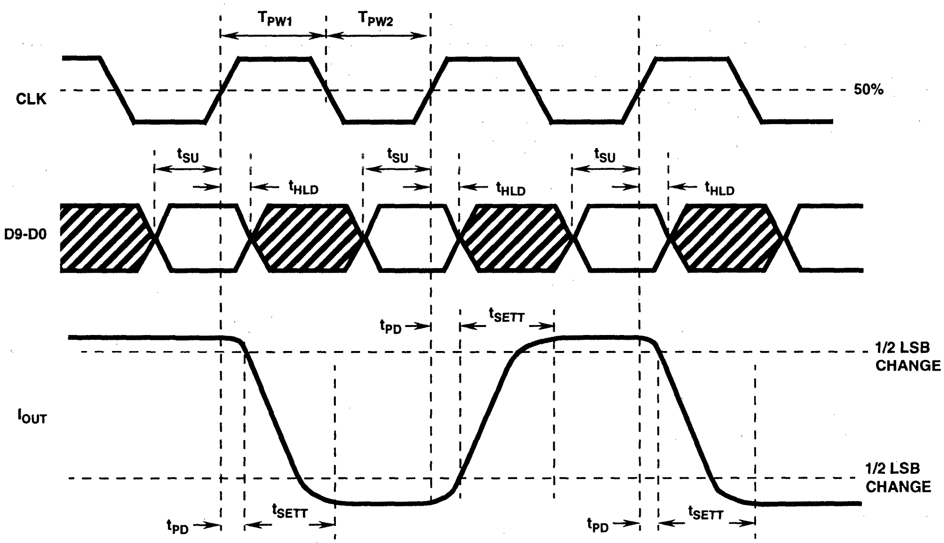


FIGURE 3. PROPAGATION DELAY, SETUP TIME AND MINIMUM PULSE WIDTH DIAGRAM

Pin Descriptions

PIN	PIN NAME	DESCRIPTION
1-7, 30-32	D0 (LSB) thru D9 (MSB)	Digital data bit 0, the least significant bit thru digital data Bit 9, the most significant bit.
9	CLK	Data clock pin 100kHz to 80MHz.
13, 28	DV_{DD}	Digital logic supply +5V.
15, 27	DGND	Digital ground.
20, 21	AV_{DD}	Analog supply +5V.
23	BLK	Output blanking pin. When set ('1') this pin zeros the I_{OUT} pin.
25	AGND	Analog ground supply current return pin.
11	PD	Power down mode pin. This pin when set ('1') places the HI5780 in lower power mode and zeros the output. Power consumption is reduced.
24	I_{OUT}	Current output pin.
23	$\overline{I_{OUT}}$	Complementary current output pin.
18	REF_{OUT}	Bandgap reference output.
17	I_{REF}	Reference resistor. Value is 16 times greater than the load resistor (R_{LOAD}).
19	V_{REF}	Voltage reference input.
14	VB	Bias voltage generator bypass capacitor.
22	VG	Reference amplifier bypass capacitor pin.

Detailed Description

The HI5780 is a 10-bit, current out D/A converter. The DAC can convert at 80 MSPS and runs on +5V supplies. The HI5780 achieves it's low power and high speed performance from an advanced CMOS process. The HI5780 consumes 150mW (maximum) and has a power down mode that only consumes TBD mW when in sleep mode. The HI5780 is an excellent converter to be used for communications applications and high performance video systems.

Digital Inputs

The HI5780 is a TTL/CMOS compatible D/A. Data is latched by a 10-bit latch. Once latched data inputs D0 (LSB) thru D9 (MSB) are decoded to the intnerl current cells; the internal latch and switching current source controls are implemented in CMOS technology to maintain high switching speeds and low power consumption.

Clocks and Termination

The internal 10-bit register is updated on the rising edge of the clock. Since the HI5780 clock rate can run to 80MHz, to minimize reflections and clock noise into the part, proper termination should be used. In PCB layout clock runs should be kept short and have a minimum of loads. To guarantee consistent results from board to board controlled impedance, PCBs should be used with a characteristic line impedance Z_O of 50Ω.

To terminate the clock line a shunt terminator to ground is the most effective type at a 80MHz clock rate. A typical value for termination can be determined by the equation:

$$R_T = Z_O$$

for the termination resistor. For a controlled impedance board with a Z_O of 50Ω, the R_T = 50Ω. Shunt termination is best used at the receiving end of the transmission line or as close to the HI5780 CLK pin as possible.

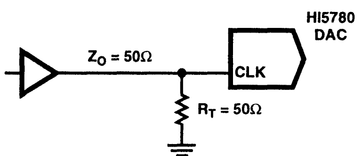


FIGURE 4. AC TERMINATION OF THE HI5780 CLOCK LINE

Rise and Fall times and propagation delay of the line will be affected by the Shunt Terminator. The terminator can be connected to DGND.

Noise Reduction

To reduce power supply noise, separate analog and digital power supplies should be used with 0.1μF and 0.01μF ceramic capacitors placed as close to the body of the HI5780 as possible on the analog (AV_{DD}) and digital (DV_{DD}) supplies. The analog and digital ground returns should be connected together back at the device to ensure proper operation on power up.

Reference

The internal reference in the HI5780 is a 1.25V (typical) bandgap voltage reference. The internal reference is buffered by an amplifier to provide adequate drive for the current cells and the R/2R resistor ladder. Reference Out (REF_{OUT}) is connected to the V_{REF} pin. The Full Scale Output Current is controlled by the resistor connected to I_{REF}. The full scale output voltage, is set by the following equation:

$$V_{OUT}(\text{Full Scale}) = V_{REF} \times 16\,(R_{LOAD}/R_{REF})$$

Applications

Voltage Conversion of the Output

To convert the output current of the D/A converter, to a voltage, an amplifier should be used as shown in Figure 5 below. The DAC needs a 50Ω termination resistor on the I_{OUT} pin to ensure proper settling. The HFA1110 has an internal feedback resistor to compensate for high frequency operation.

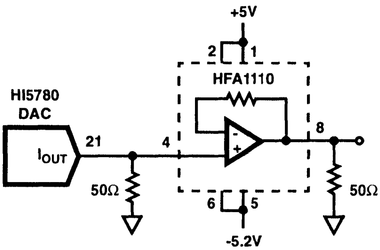


FIGURE 5. HIGH SPEED CURRENT TO VOLTAGE CONVERSION

Definition of Specifications

Integral Linearity Error, INL is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Output Voltage Full Scale Settling Time, is the time required from the 50% point on the clock input for a full scale step to settle within an 1/2 LSB error band.

Glitch Area, GE is the switching transient appearing on the output during a code transition. It is measured as the area under the curve and expressed as a Volt-Time specification.

Differential Gain, ΔA_V is the gain error from an ideal sine wave with a normalized amplitude.

Differential Phase, ΔΦ is the phase error from and ideal sine wave.

Spurious Free Dynamic Range, SFDR is the amplitude difference from a fundamental to the largest harmonically or non-harmonically related spur. A sine wave is loaded into the D/A and the output filtered at 1/2 the clock frequency to eliminate noise from clocking alias terms.

5

D/A CONVERTERS

SIGNAL PROCESSING NEW RELEASES 6

COMMUNICATION INTERFACE

HARRIS SEMICONDUCTOR

HIN200 thru HIN213

+5V Powered RS-232 Transmitters/Receivers with 0.1Microfarad External Capacitors

July 1995

Features

- Meets All RS-232E and V.28 Specifications
- Requires Only 0.1μF External Capacitors
- 120kbit/s Data Rate
- Two Receivers Active in Shutdown Mode (HIN213)
- Requires Only Single +5V Power Supply
  - (+5V and +12V - HIN201 and HIN209)
- Onboard Voltage Doubler/Inverter
- Low Power Consumption Typically 5mA
- Low Power Shutdown Function Typically 1μA
- Three-State TTL/CMOS Receiver Outputs
- Multiple Drivers
  - ±10V Output Swing for +5V Input
  - 300Ω Power-Off Source Impedance
  - Output Current Limiting
  - TTL/CMOS Compatible
  - 30V/μs Maximum Slew Rate
- Multiple Receivers
  - 30V Input V oltage Range
  - 3kΩ to 7kΩ Input Impedance
  - 0.5V Hysteresis to Improve Noise Rejection

Description

The HIN200-HIN213 family of RS-232 transmitters/receivers interface circuits meet all EIA RS-232E and V.28 specifications, and are particularly suited for those applications where ±12V is not available. They require a single +5V power supply (except HIN201 and HIN209) and feature onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply. The family of devices offers a wide variety of RS232 transmitter/receiver combinations to accommodate various applications (see Selection Table).

The HIN200, HIN206, HIN211 and HIN213 feature a low power shutdown mode to conserve energy in battery powered applications. In addition, the HIN213 provides two active receivers in shutdown mode allowing for easy "wakeup" capability.

The drivers feature true TTL/CMOS input compatibility, slewrate-limited output, and 300Ω power-off source impedance. The receivers can handle up to ±30V input, and have a 3kΩ to 7kΩ input impedance. The receivers also feature hysteresis to greatly improve noise rejection.

Applications

- Any System Requiring RS-232 Communications Port
  - Computer - Portable, Mainframe, Laptops
  - Peripheral - Printers and Terminals
  - Portable Instrumentation
  - Modems

6

COMMUNICATION INTERFACE

Selection Table

PART NUMBER	POWER SUPPLY VOLTAGE	NUMBER OF RS-232 DRIVERS	NUMBER OF RS-232 RECEIVERS	EXTERNAL COMPONENTS	LOW POWER SHUTDOWN/TTL THREE-STATE	NUMBER OF RECEIVERS ACTIVE IN SHUTDOWN
HIN200	+5V	5	0	4 Capacitors	Yes/No	0
HIN201	+5V and +7.5V to 13.2V	2	2	2 Capacitors	No/No	0
HIN202	+5V	2	2	4 Capacitors	No/No	0
HIN204	+5V	4	0	4 Capacitors	No/No	0
HIN206	+5V	4	3	4 Capacitors	Yes/Yes	0
HIN207	+5V	5	3	4 Capacitors	No/No	0
HIN208	5V	4	4	4 Capacitors	No/No	0
HIN209	+5V and +7.5V to 13.2V	3	5	2 Capacitors	No/Yes	0
HIN211	+5V	4	5	4 Capacitors	Yes/Yes	0
HIN213 (Note)	+5V	4	5	4 Capacitors	Yes/Yes	2

NOTE: Available in Q3, CY95

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3980.2

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIN200CB	0°C to +70°C	20 Lead Plastic SOIC (W)
HIN200IB	-40°C to +85°C	20 Lead Plastic SOIC (W)
HIN201CB	0°C to +70°C	16 Lead Plastic SOIC (W)
HIN201IB	-40°C to +85°C	16 Lead Plastic SOIC (W)
HIN202CP	0°C to +70°C	16 Lead Plastic DIP
HIN202CB	0°C to +70°C	16 Lead Plastic SOIC (W)
HIN202IP	-40°C to +85°C	16 Lead Plastic DIP
HIN202IB	-40°C to +85°C	16 Lead Plastic SOIC (W)
HIN204CB	0°C to +70°C	16 Lead Plastic SOIC (W)
HIN204IB	-40°C to +85°C	16 Lead Plastic SOIC (W)
HIN206CP	0°C to +70°C	24 Lead Plastic DIP (N)
HIN206CB	0°C to +70°C	24 Lead Plastic SOIC (W)
HIN206CA	0°C to +70°C	24 Lead Plastic SSOP
HIN206IP	-40°C to +85°C	24 Lead Plastic DIP (N)
HIN206IB	-40°C to +85°C	24 Lead Plastic SOIC (W)
HIN206IA	-40°C to +85°C	24 Lead Plastic SSOP
HIN207CP	0°C to +70°C	24 Lead Plastic DIP (N)
HIN207CB	0°C to +70°C	24 Lead Plastic SOIC (W)
HIN207CA	0°C to +70°C	24 Lead Plastic SSOP
HIN207IP	-40°C to +85°C	24 Lead Plastic DIP (N)

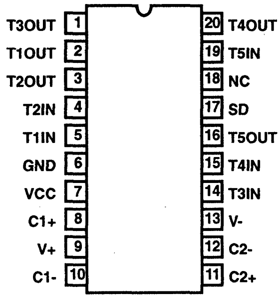
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIN207IB	-40°C to +85°C	24 Lead Plastic SOIC (W)
HIN207IA	-40°C to +85°C	24 Lead Plastic SSOP
HIN208CP	0°C to +70°C	24 Lead Plastic DIP (N)
HIN208CB	0°C to +70°C	24 Lead Plastic SOIC (W)
HIN208CA	0°C to +70°C	24 Lead Plastic SSOP
HIN208IP	-40°C to +85°C	24 Lead Plastic DIP (N)
HIN208IB	-40°C to +85°C	24 Lead Plastic SOIC (W)
HIN208IA	-40°C to +85°C	24 Lead Plastic SSOP
HIN209CP	0°C to +70°C	24 Lead Plastic DIP (N)
HIN209CB	0°C to +70°C	24 Lead Plastic SOIC (W)
HIN209IP	-40°C to +85°C	24 Lead Plastic DIP (N)
HIN209IB	-40°C to +85°C	24 Lead Plastic SOIC (W)
HIN211CB	0°C to +70°C	28 Lead Plastic SOIC (W)
HIN211CA	0°C to +70°C	28 Lead Plastic SSOP
HIN211IB	-40°C to +85°C	28 Lead Plastic SOIC (W)
HIN211IA	-40°C to +85°C	28 Lead Plastic SSOP
HIN213CB	0°C to +70°C	28 Lead Plastic SOIC (W)
HIN213CA	0°C to +70°C	28 Lead Plastic SSOP
HIN213IB	-40°C to +85°C	28 Lead Plastic SOIC (W)
HIN213IA	-40°C to +85°C	28 Lead Plastic SSOP

Pin Description

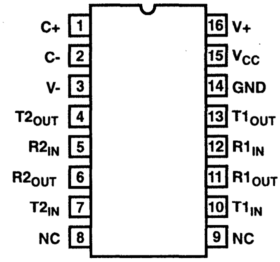
PIN	FUNCTION
V_{CC}	Power Supply Input 5V ±10%.
V+	Internally generated positive supply (+10V nominal), HIN201 and HIN209 requires +7.5V to +13.2V.
V-	Internally generated negative supply (-10V nominal).
GND	Ground lead. Connect to 0V.
C1+	External capacitor (+ terminal) is connected to this lead.
C1-	External capacitor (- terminal) is connected to this lead.
C2+	External capacitor (+ terminal) is connected to this lead.
C2-	External capacitor (- terminal) is connected to this lead.
T_{IN}	Transmitter Inputs. These leads accept TTL/CMOS levels. An internal 400kΩ pull-up resistor to V_{CC} is connected to each lead.
T_{OUT}	Transmitter Outputs. These are RS-232 levels (nominally ±10V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 input levels. An internal 5kΩ pull-down resistor to GND is connected to each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$, EN	Enable input. This is an active low input which enables the receiver outputs. With $\overline{EN}$ = 5V, (HIN213 EN = 0V), the outputs are placed in a high impedance state.
SD, $\overline{SD}$	Shutdown Input. With SD = 5V (HIN213 $\overline{SD}$ = 0V), the charge pump is disabled, the receiver outputs are in a high impedance state (except R4 and R5 of HIN213) and the transmitters are shut off.
NC	No Connect. No connections are made to these leads.

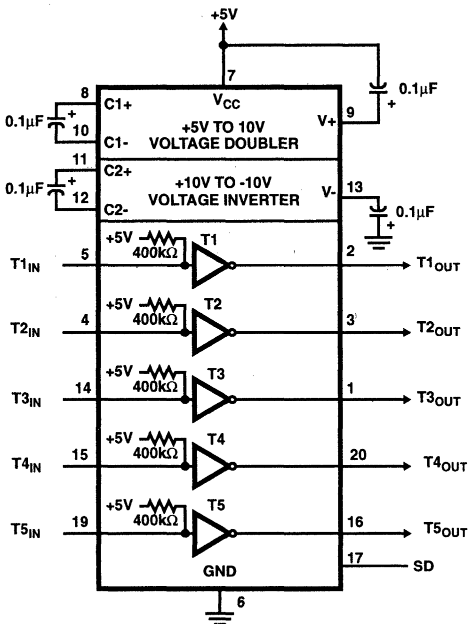
Pinouts

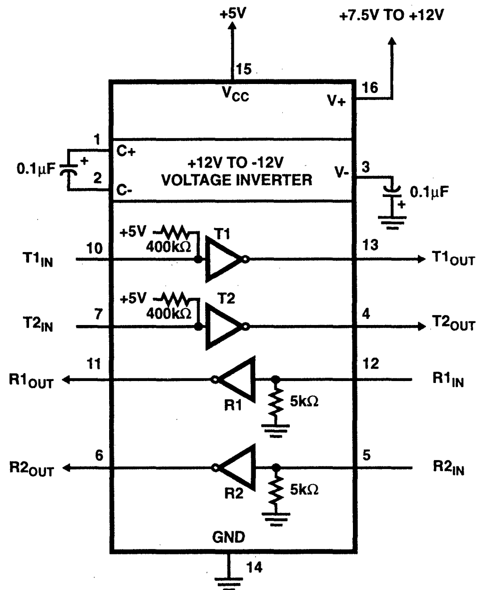
HIN200 (SOIC)
TOP VIEW



HIN201 (SOIC)
TOP VIEW

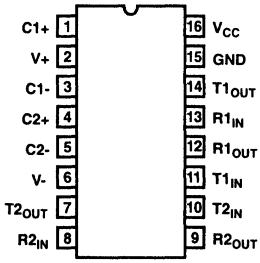




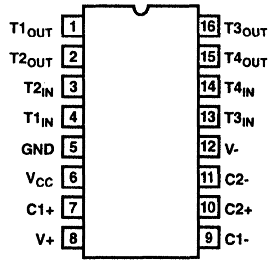


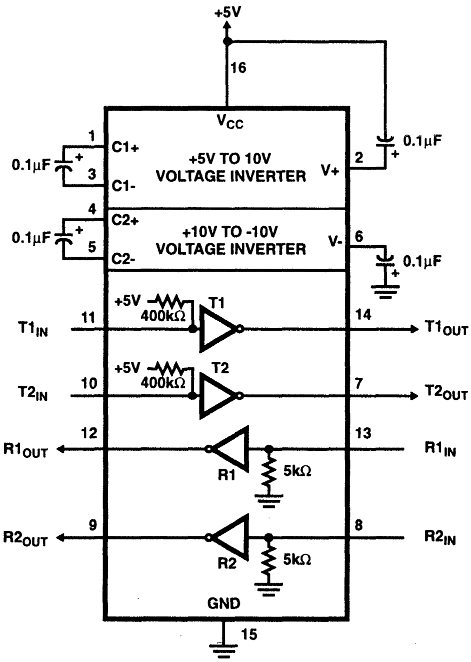
Pinouts (Continued)

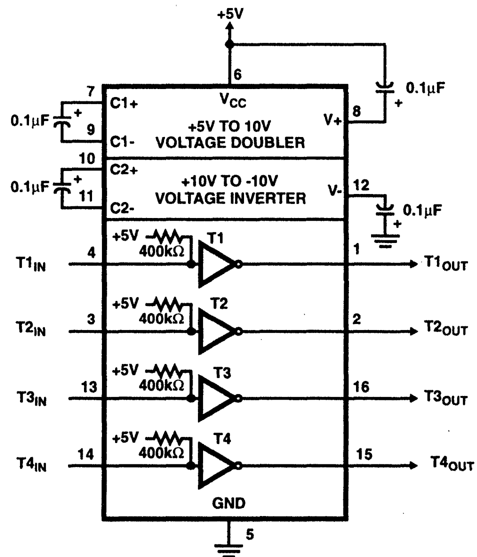
HIN202 (PDIP, SOIC)
TOP VIEW



HIN204 (SOIC)
TOP VIEW



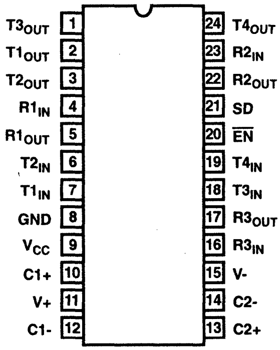




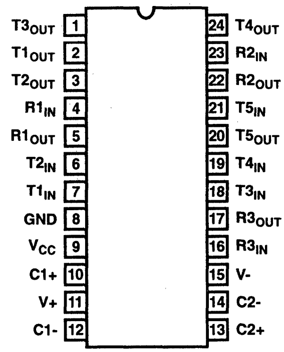
6
COMMUNICATION INTERFACE

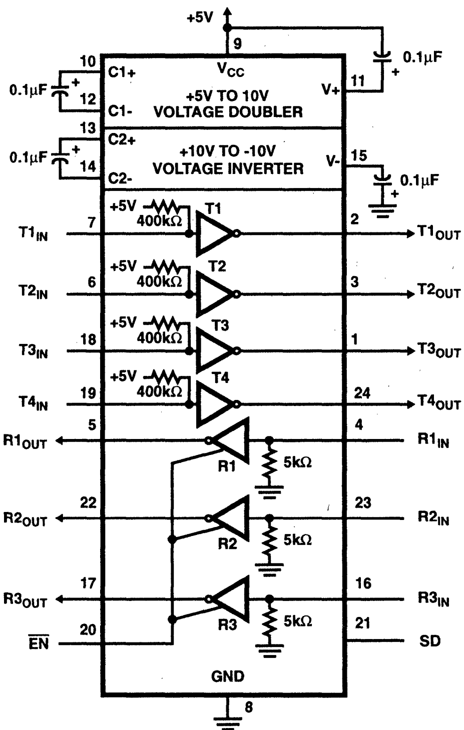
Pinouts (Continued)

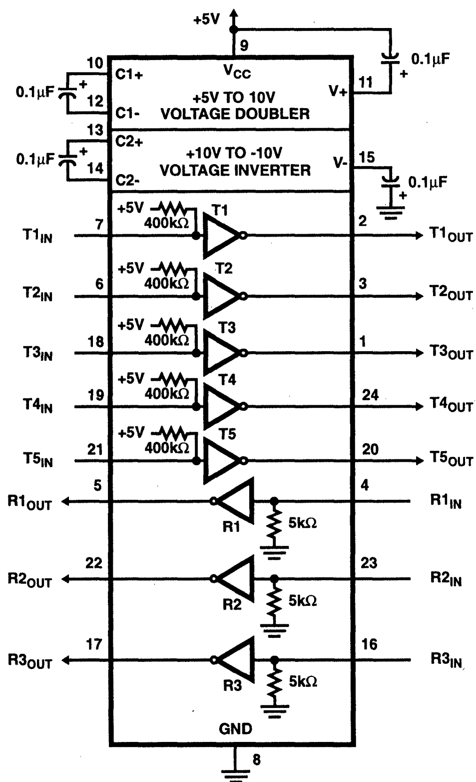
HIN206 (PDIP, SOIC, SSOP)
TOP VIEW



HIN207 (PDIP, SOIC, SSOP)
TOP VIEW

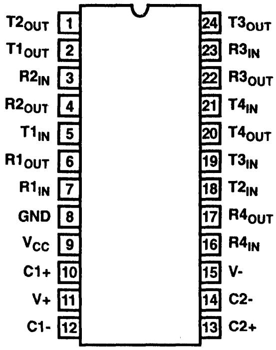




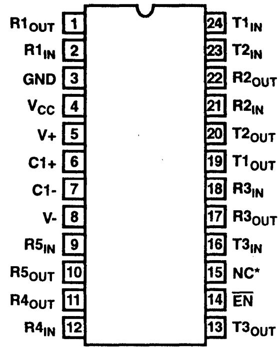


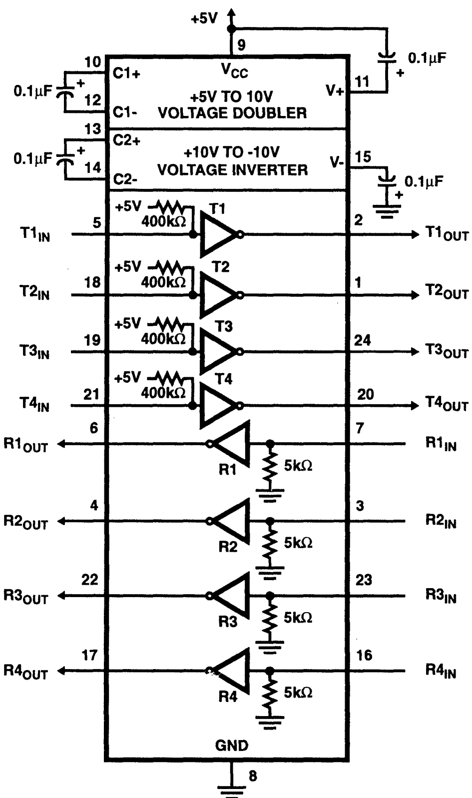
Pinouts (Continued)

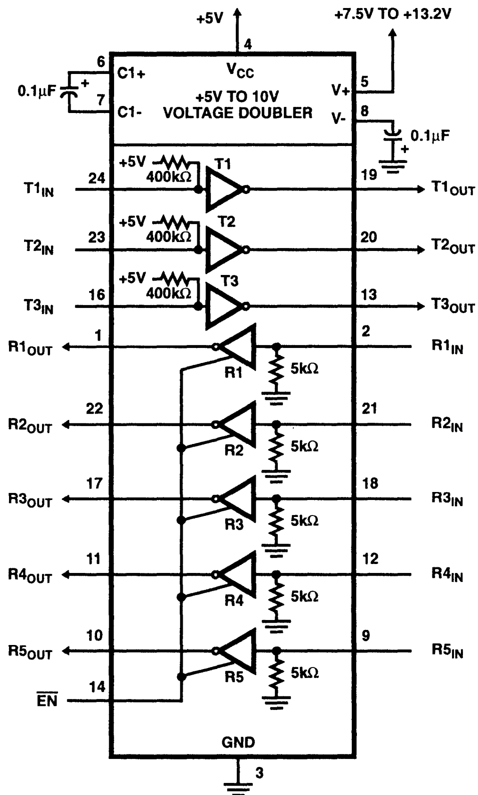
HIN208 (PDIP, SOIC, SSOP)
TOP VIEW



HIN209 (PDIP, SOIC, SSOP)
TOP VIEW

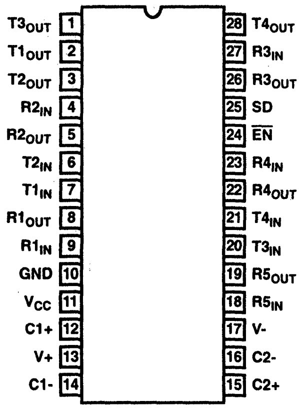




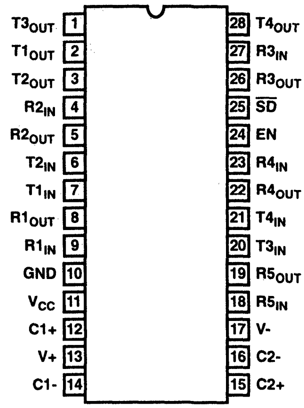


Pinouts (Continued)

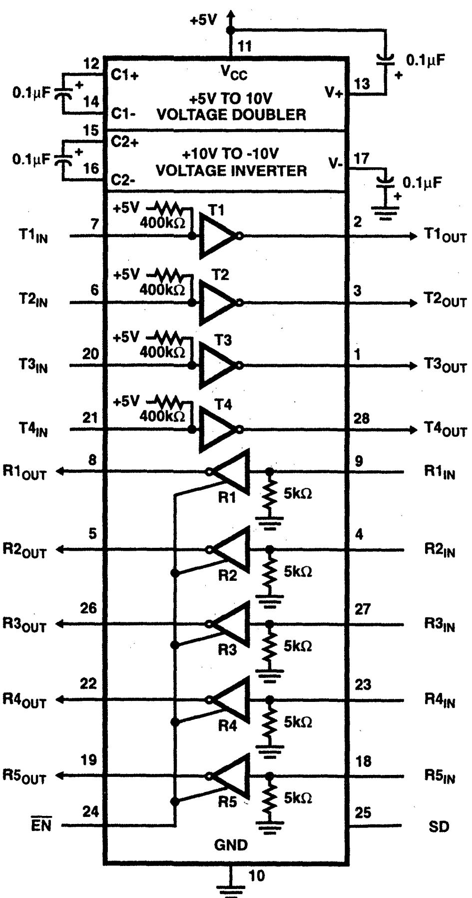
HIN211 (SOIC, SSOP)
TOP VIEW

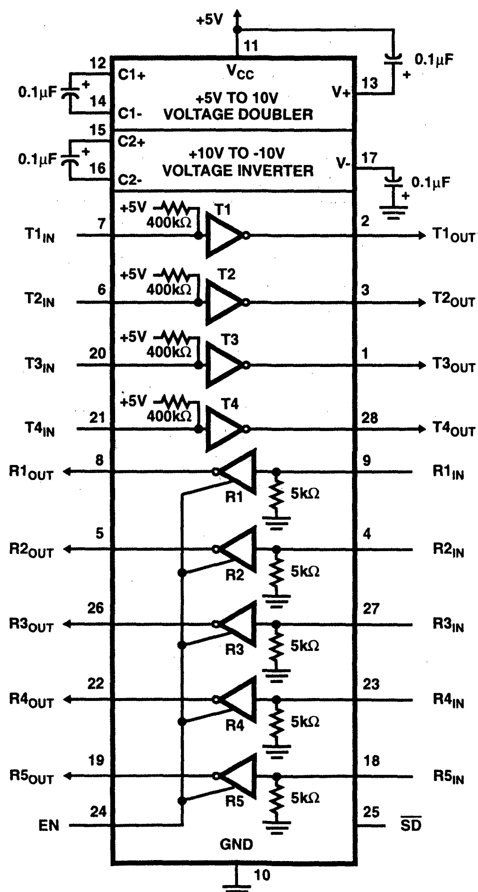


HIN213 (SOIC, SSOP)
TOP VIEW



NOTE: R4 AND R5 ACTIVE IN SHUTDOWN





Absolute Maximum Ratings

V_{CC} to Ground . . . . . . (GND -0.3V) <V_{CC} < 6V
V+ to Ground . . . . . . (V_{CC} -0.3V) <V+ < 12V
V- to Ground . . . . . . -12V < V- < (GND +0.3V)
Input Voltages
T_{IN} . . . . . . (V- -0.3V) < V_{IN} < (V+ +0.3V)
R_{IN} . . . . . . ±30V
Output Voltages
T_{OUT} . . . . . . (V- -0.3V) < V_{TXOUT} < (V+ +0.3V)
R_{OUT} . . . . . . (GND -0.3V) < V_{RXOUT} < (V+ +0.3V)
Short Circuit Duration
T_{OUT} . . . . . . Continuous
R_{OUT} . . . . . . Continuous
Lead Temperature (Soldering 10s) . . . . . . +300°C
(SOIC and SSOP - Lead Tips Only)
ESD Classification . . . . . . Class 1

Continuous Power Dissipation (T_A = 70°C)
16 Lead Plastic DIP
(Derate 11.1mW/°C above 70°C) 888mW
24 Lead Plastic DIP (N)
(Derate 13.3mW/°C above 70°C) 1067mW
16 Lead Plastic SOIC (W)
(Derate 10mW/°C above 70°C) 800mW
20 Lead Plastic SOIC (W)
(Derate 10mW/°C above 70°C) 800mW
24 Lead Plastic SOIC (W)
(Derate 12.5mW/°C above 70°C) 1000mW
28 Lead Plastic SOIC (W)
(Derate 13.3mW/°C above 70°C) 1067mW
24 Lead Plastic SSOP
(Derate 7.4mW/°C above 70°C) 592mW
28 Lead Plastic SSOP
(Derate 10mW/°C above 70°C) 800mW
Storage Temperature Range . . . . . . -40°C to +85°C
Maximum Die Junction Temperature
Plastic Package . . . . . . +150°C
Operating Temperature Range
HIN-XXXCX . . . . . . 0°C to +70°C
HIN-XXXIX . . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions: V_{CC} = +5V ±10%, (V_{CC} = +5V ±5% HIN200 and HIN207), T_A = Operating Temperature Range

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing, T_{OUT}	Transmitter Outputs, 3kΩ to Ground		±5	±9	±10	V
Power Supply Current, I_{CC}	No Load, T_A = +25°C	HIN202-203	-	8	15	mA
		HIN200, HIN204-208, HIN211-213	-	11	20	mA
		HIN201, HIN209	-	0.4	1	mA
V+ Power Supply Current, I_{CC}	No Load	HIN201	-	5.0	10	mA
		HIN209	-	7.0	15	mA
Shutdown Supply Current, I_{CC}(SD)	HIN200, HIN206, HIN211		-	1	10	µA
	HIN213		-	15	50	µA
Input Logic Low, T_{IN}, $\overline{EN}$, V_{IL}	T_{IN}, $\overline{EN}$, SD, EN, $\overline{SD}$		-	-	0.8	V
Input Logic High, V_{IH}	T_{IN}		2.0	-	-	V
	$\overline{EN}$, SD, EN, $\overline{SD}$		2.4	-	-	V
Logic Pullup Current, I_P	T_{IN} = 0V		-	15	200	µA
RS-232 Input Voltage Range, V_{IN}			-30	-	+30	V
Receiver Input Impedance, R_{IN}	V_{IN} = ±3V		3.0	5.0	7.0	kΩ
Receiver Input Low Threshold, V_{IN} (H-L)	V_{CC} = 5.0V, T_A = +25°C	Active Mode	0.8	1.2	-	V
		Shutdown Mode HIN213 R4 & R5	0.6	1.5	-	V

6

COMMUNICATION INTERFACE

Electrical Specifications Test Conditions: V_{CC} = +5V ±10%, (V_{CC} = +5V ±5% HIN200 and HIN207), T_A = Operating Temperature Range **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
Receiver Input High Threshold, V_{IN} (L-H)	V_{CC} = 5.0V, T_A = +25°C	Active Mode	-	1.7	2.4	V
		Shutdown Mode HIN213 R4 & R5	-	1.5	2.4	V
Receiver Input Hysteresis, V_{HYST}	No Hysteresis in Shutdown Mode		0.2	0.5	1.0	V
TTL/CMOS Receiver Output Voltage Low, V_{OL}	I_{OUT} = 1.6mA (HIN201-HIN203, I_{OUT} = 3.2mA)		-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, V_{OH}	I_{OUT} = -1.0mA (HIN213, I_{OUT} = -200μA)		3.5	4.6	-	V
Output Enable Time, t_{EN}	HIN206, HIN209, HIN211, HIN213		-	600	-	ns
Output Disable Time, t_{DIS}	HIN206, HIN209, HIN211, HIN213		-	200	-	ns
Propagation Delay, t_{PD}	HIN213 $\overline{SD}$ = 0V, R4, R5		-	4.0	40	μs
	HIN213 $\overline{SD}$ = VCC		-	0.5	10	μs
	HIN200 - HIN211		-	0.5	10	μs
Transition Region Slew Rate, SR_T	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or -3V to +3V (Note 1)	HIN200, HIN204 to HIN211, HIN213	-	3	30	V/μs
		HIN201, HIN202	-	4.0	30	V/μs
Output Resistance, R_{OUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	T_{OUT} shorted to GND		-	±10	-	mA

NOTE:

1. Guaranteed by design.

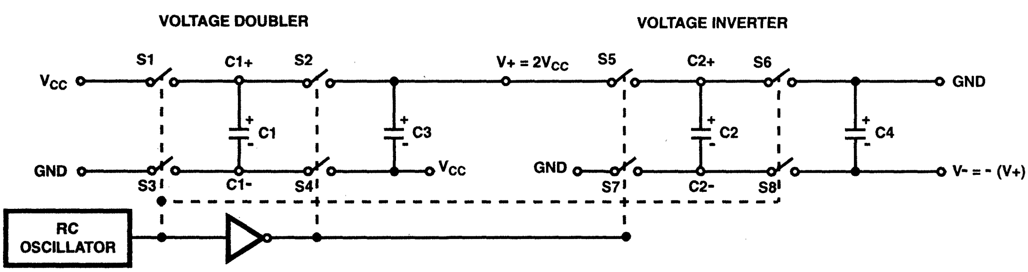


FIGURE 1. CHARGE PUMP

Detailed Description

The HIN200 thru HIN213 family of RS-232 transmitters/receivers are powered by a single +5V power supply (except HIN201 and HIN209), feature low power consumption, and meet all EIA RS232C and V.28 specifications. The circuit is divided into three sections: the charge pump, transmitter, and receiver.

Charge Pump

An equivalent circuit of the charge pump is illustrated in Figure 1. The charge pump contains two sections: the voltage doubler and the voltage inverter. Each section is driven by a two phase, internally generated clock to generate +10V and -10V. The nominal clock frequency is 125kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C3 equal to twice V_{CC}. During phase two, C2 is also charged to $2V_{CC}$, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The charge pump accepts input voltages up to 5.5V. The output impedance of the voltage doubler section (V+) is approximately 200Ω, and the output impedance of the voltage inverter section (V-) is approximately 450Ω. A typical application uses 0.1μF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.

During shutdown mode (HIN200, HIN206 and HIN211, SD = V_{CC}, HIN213, $\overline{SD}$ = 0V) the charge pump is turned off, V+ is pulled down to V_{CC}, V- is pulled up to GND, and the supply current is reduced to less than 10μA. The transmitter outputs are disabled and the receiver outputs (except for HIN213, R4 and R5) are placed in the high impedance state.

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ -0.6V). Each transmitter input has an internal 400kΩ pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specifications of ±5V minimum with the worst case conditions of: all transmitters driving 3kΩ minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/μs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with ±2V applied to the outputs and V_{CC} = 0V.

Receivers

The receiver inputs accept up to ±30V while presenting the required 3kΩ to 7kΩ input impedance even if the power is off (V_{CC} = 0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specifications. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis (except during shutdown) to improve noise rejection. The receiver Enable line ($\overline{EN}$, on HIN206, HIN209, and HIN211, EN on HIN213) when unasserted, disables the receiver outputs, placing them in the high impedance mode. The receiver outputs are also placed in the high impedance state when in shutdown mode (except HIN213 R4 and R5).

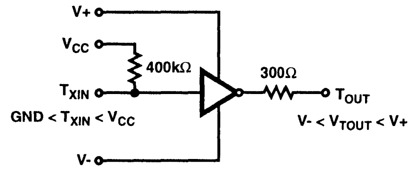


FIGURE 2. TRANSMITTER

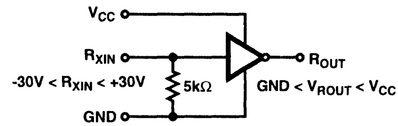
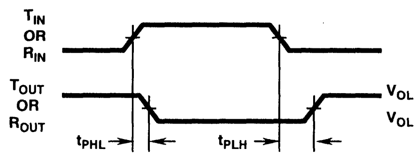


FIGURE 3. RECEIVER



AVERAGE PROPAGATION DELAY = $\frac{t_{PHL} + t_{PLH}}{2}$

FIGURE 4. PROPAGATION DELAY DEFINITION

HIN213 Operation in Shutdown

The HIN213 features two receivers, R4 and R5, which remain active in shutdown mode. During normal operation the receivers propagation delay is typically 0.5μs. This propagation delay increases to 4μs (typical) during shutdown. When entering shut down mode, receivers R4 and R5 are not valid for 80μs after $\overline{SD}$ = V_{IL}. When exiting shutdown mode, all receiver outputs will be invalid until the charge pump circuitry reaches normal operating voltage. This is typically less than 2ms when using 0.1μF capacitors.

Typical Performance Curves

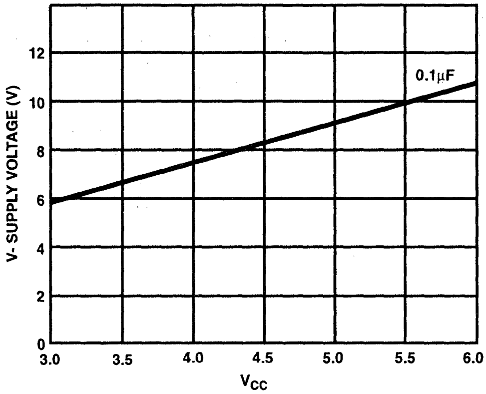


FIGURE 5. V- SUPPLY VOLTAGE vs V_{CC}

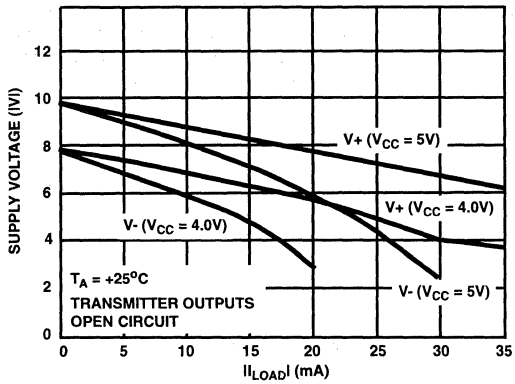


FIGURE 6. V+, V- OUTPUT VOLTAGE vs LOAD

Test Circuits (HIN-202)

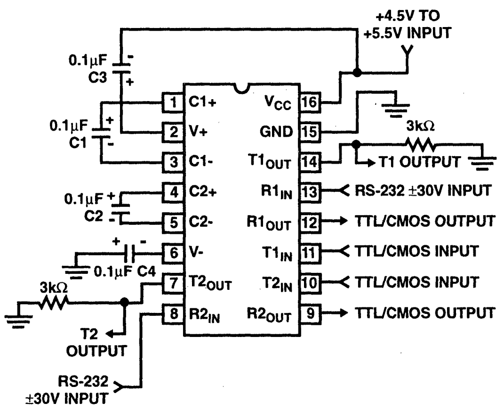


FIGURE 7. GENERAL TEST CIRCUIT

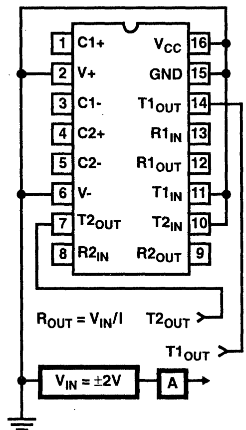


FIGURE 8. POWER-OFF SOURCE RESISTANCE CONFIGURATION

Applications

The HINXXX may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 9. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

In applications requiring four RS-232 inputs and outputs (Figure 10), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

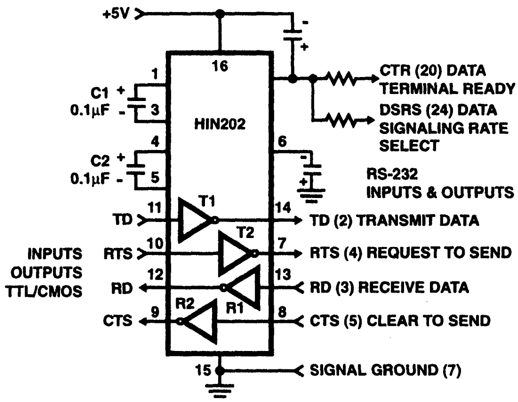


FIGURE 9. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

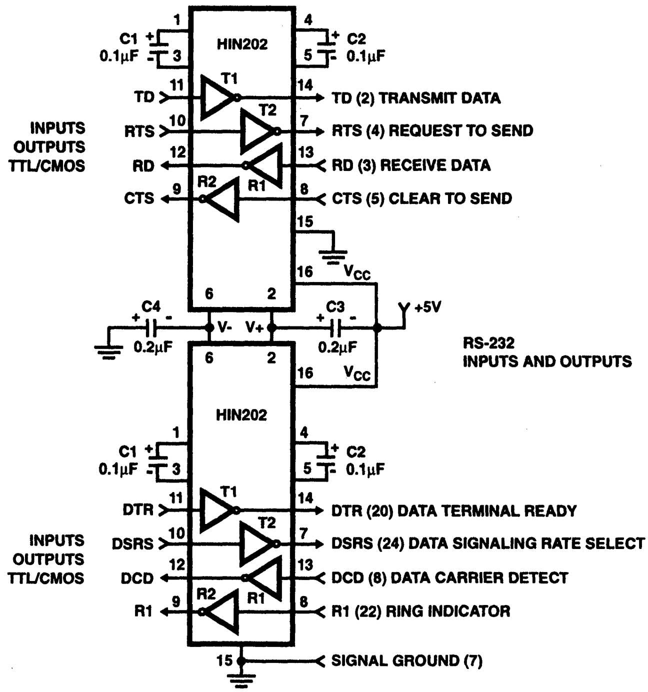


FIGURE 10. COMBINING TWO HIN202s FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

6 COMMUNICATION INTERFACE

Die Characteristics

DIE DIMENSIONS:
160 x 140 mils

METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

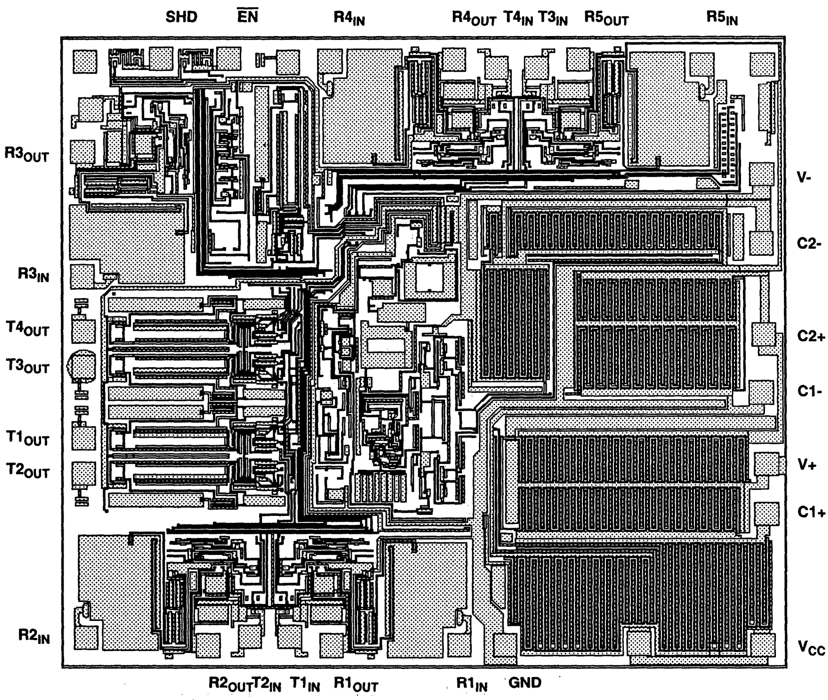
TRANSISTOR COUNT: 238

PROCESS: CMOS Metal Gate

SUBSTRATE POTENTIAL: V+

Metallization Mask Layout

HIN211



SIGNAL PROCESSING NEW RELEASES 7

SWITCHES

7 SWITCHES

HARRIS SEMICONDUCTOR

DG401, DG403, DG405

July 1995

Monolithic CMOS Analog Switches

Features

- **ON-Resistance <35Ω**
- **Low Power Consumption (P_D <35μW)**
- **Fast Switching Action**
  - t_{ON} **<150ns**
  - t_{OFF} **<100ns**
- **Low Charge Injection**
- **DG401 Dual SPST; Same Pinout as HI-5041**
- **DG403 Dual SPDT; DG190, IH5043, IH5151, HI-5051**
- **DG405 Dual DPST; DG184, HI-5045, IH5145**
- **TTL, CMOS Compatible**
- **Single or Split Supply Operation**

Applications

- **Audio Switching**
- **Battery Operated Systems**
- **Data Acquisition**
- **Hi-Rel Systems**
- **Sample and Hold Circuits**
- **Communication Systems**
- **Automatic Test Equipment**

Description

The DG401, DG403 and DG405 monolithic CMOS analog switches have TTL and CMOS compatible digital inputs.

These switches feature low analog ON resistance (<35Ω) and fast switch time (t_{ON} < 150ns). Low charge injection simplifies sample and hold applications.

The improvements in the DG401/403/405 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V peak-to-peak signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±17V.

The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±15V analog input range. The three different devices provide the equivalent of two SPST (DG401), two SPDT (DG403) or two DPST (DG405) relay switch contacts with CMOS or TTL level activation. The pinout is similar, permitting a standard layout to be used, choosing the switch function as needed.

Ordering Information

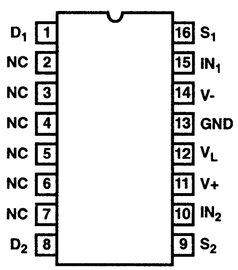
PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG401AK/883 (Note 2)	-55°C to +125°C	16 Lead CerDIP
DG401DJ	-40°C to +85°C	16 Lead Plastic DIP
DG401DY	-40°C to +85°C	16 Lead Plastic SOIC (N)
DG401EJ (Note 1)	-40°C to +85°C	16 Lead Plastic DIP
DG401EY (Note 1)	-40°C to +85°C	16 Lead Plastic SOIC (N)
DG403AK/883 (Note 2)	-55°C to +125°C	16 Lead CerDIP DIP
DG403DJ	-40°C to +85°C	16 Lead Plastic DIP
DG403DY	-40°C to +85°C	16 Lead Plastic SOIC (N)
DG403EJ (Note 1)	-40°C to +85°C	16 Lead Plastic DIP
DG403EY (Note 1)	-40°C to +85°C	16 Lead Plastic SOIC (N)
DG405AK/883 (Note 2)	-55°C to +125°C	16 Lead CerDIP
DG405DJ	-40°C to +85°C	16 Lead Plastic DIP
DG405DY	-40°C to +85°C	16 Lead Plastic SOIC (N)
DG405EJ (Note 1)	-40°C to +85°C	16 Lead Plastic DIP
DG405EY (Note 1)	-40°C to +85°C	16 Lead Plastic SOIC (N)

NOTES:

1. Extended Processing Flow.
2. Refer to Military data sheet for complete specifications.

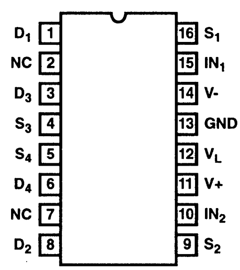
Pinouts

DG401 (CDIP, PDIP, SOIC)
TOP VIEW



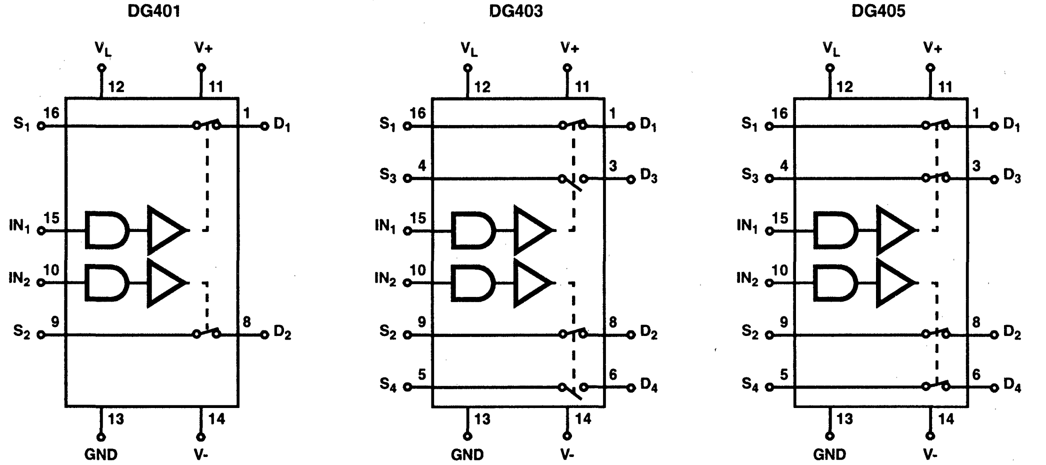
(NC) NO CONNECTION

DG403, DG405 (CDIP, PDIP, SOIC)
TOP VIEW

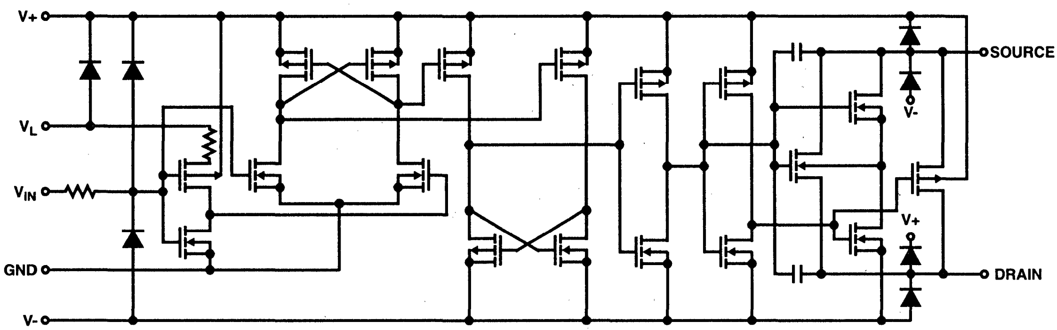


(NC) NO CONNECTION

Functional Diagram



Schematic Diagram



Truth Table

LOGIC	DG401	DG403		DG405
	SWITCH	SWITCH 1, 2	SWITCH 3, 4	SWITCH
0	OFF	OFF	ON	OFF
1	ON	ON	OFF	ON

NOTE: Logic "0" ≤0.8V. Logic "1" ≥2.4V.

Absolute Maximum Ratings

V+ to V- . . . +44.0V
GND to V- . . . 25V
VL . . . (GND - 0.3V) to (VC+) +0.3V
Digital Inputs (Note 1), V_S, V_D . . . (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous (Any Terminal) Current, (Note 1) . . . ±30mA
Peak Current, S or D (Note 1) . . . ±100mA
(Pulsed 1ms, 10% Duty Cycle)
Storage Temperature Range (D and E Suffix) . . . -65°C to +125°C

Thermal Information

Thermal Resistance (Note 2) θ_{JA}
Plastic DIP Package . . . 90°C/W
SOIC Package . . . 115°C/W
Lead Temperature (Soldering 10s) . . . +300°C
(SOIC - Lead Tips Only)
Operating Temperature (D and E Suffix) . . . -40°C to +85°C
Junction Temperature (PDIP, SOIC) . . . +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . ±20V Max
Operating Temperature Range . . . -55°C to +125°C
Input Low Voltage . . . 0.8V Max
Input High Voltage . . . 2.4V Min
Input Rise and Fall Time . . . 20ns

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, V_L = 5V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITION	(NOTE 4) TEMP	D SUFFIX -40°C TO +85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	R_L = 300Ω, C_L = 35pF	Room	-	100	150	ns
Turn-OFF Time, t_{OFF}		Room	-	60	100	ns
Break-Before-Make, Time Delay (DG403), t_D	R_L = 300Ω, C_L = 35pF	Room	5	12	-	ns
Charge Injection, Q	C_L = 10,000pF, V_{GEN} = 0V, R_{GEN} = 0Ω	Room	-	60	-	pC
OFF Isolation Reject Ratio, OIRR	R_L = 100Ω, C_L = 5pF, f = 1MHz	Room	-	72	-	dB
Crosstalk (Channel-to-Channel), CCRR	R_L = 100Ω, C_L = 5pF, f = 1MHz	Room	-	90	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz, V_S = 0V	Room	-	12	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	f = 1MHz, V_S = 0V	Room	-	12	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$	f = 1MHz, V_S = 0V	Room	-	39	-	pF
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, I_S = -10mA, V_D = ±10V	Room	-	20	45	Ω
		Full	-	-	55	Ω
Drain-Source ON Resistance, $\Delta r_{DS(ON)}$	V+ = 16.5V, V- = -16.5V, I_S = -10mA, V_D = 5, 0, -5V	Room	-	3	3	Ω
		Full	-	-	5	Ω
Switch OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5 V_D = ±15.5V, V_S = ∓15.5V	Room	-0.5	-0.01	0.5	nA
		Full	-5	-	5	nA
Switch OFF Leakage Current, $I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	Room	-0.5	-0.01	0.5	nA
		Full	-5	-	5	nA
Channel ON Leakage Current, $I_{D(ON)}$	V± = ±16.5V, V_D = V_S = ±15.5V	Room	-1	-0.04	1	nA
		Full	-10	-	10	nA

7

SWITCHES

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, V_L = 5V (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	(NOTE 4) TEMP	D SUFFIX -40°C TO +85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DIGITAL CONTROL						
Input Current with V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-1	0.005	1	µA
Input Current with V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-1	0.005	1	µA
POWER SUPPLIES						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	Room	-	0.01	1	µA
		Full	-	-	5	µA
Negative Supply Current, I-		Room	-1	-0.01	-	µA
		Full	-5	-	-	µA
Logic Supply Current, I_L		Room	-	0.01	1	µA
		Full	-	-	5	µA
Ground Current, I_{GND}		Room	-1	-0.01	-	µA
		Full	-5	-	-	µA

NOTES:

1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. All leads soldered to PC Board.
3. V_{IN} = input voltage to perform proper function.
4. Hot = as determined by the operating temperature suffix.
5. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
7. Guaranteed by design, not subject to production test.

Typical Performance Curves

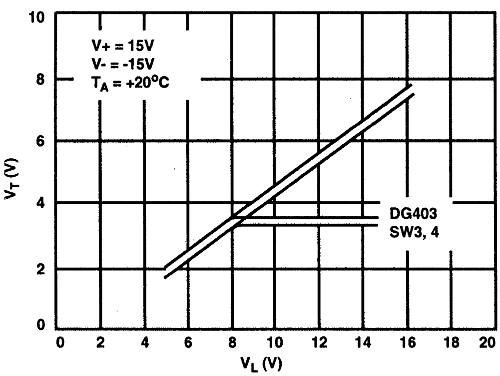


FIGURE 1. INPUT SWITCHING THRESHOLD vs LOGIC SUPPLY VOLTAGE

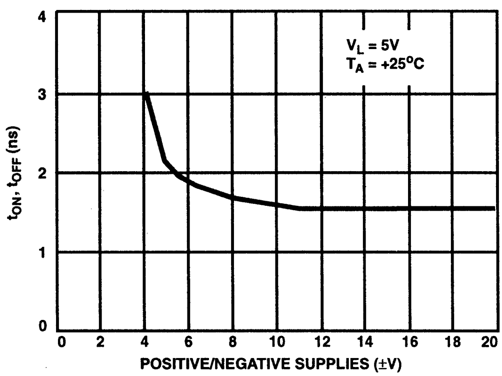


FIGURE 2. INPUT SWITCHING THRESHOLD vs POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

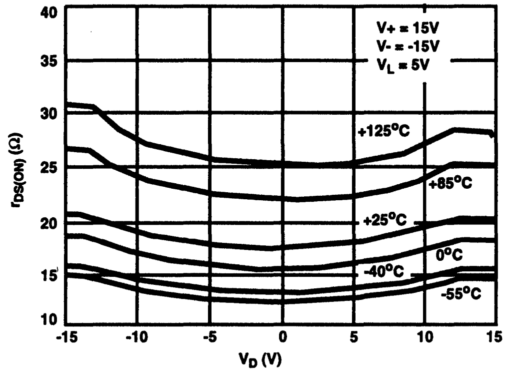


FIGURE 3. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

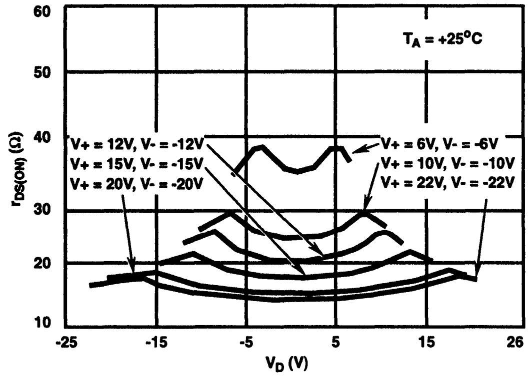


FIGURE 4. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

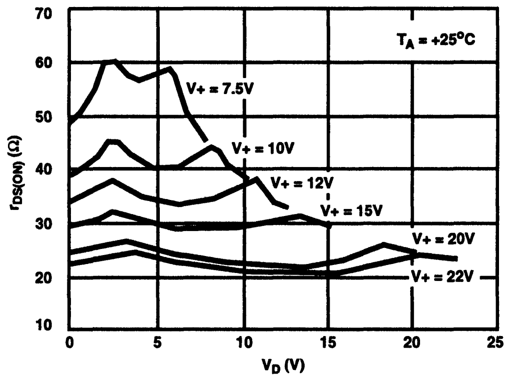


FIGURE 5. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE, V- = -0V

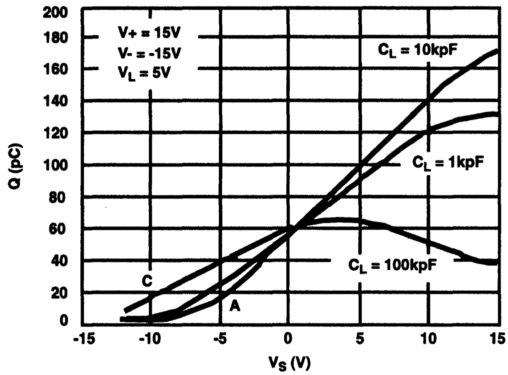


FIGURE 6. CHARGE INJECTION vs ANALOG VOLTAGE (V_S)

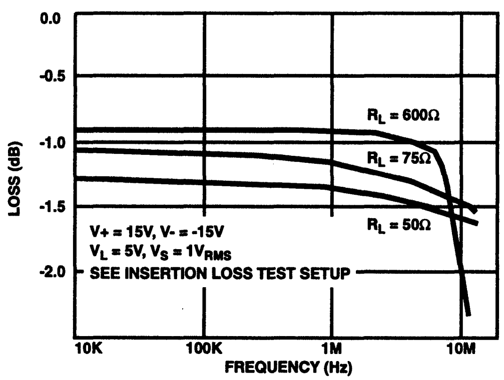


FIGURE 7. INSERTION LOSS vs FREQUENCY

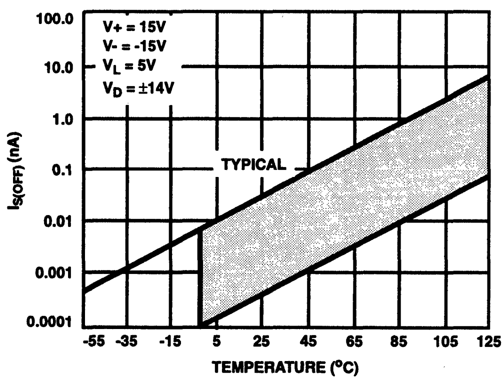


FIGURE 8. $I_{S(OFF)}$ vs TEMPERATURE

7

SWITCHES

Typical Performance Curves (Continued)

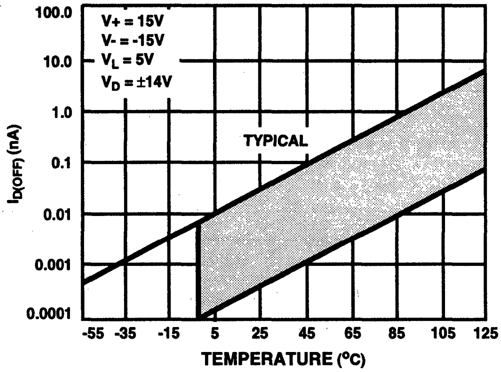


FIGURE 9. $I_{D(OFF)}$ vs TEMPERATURE

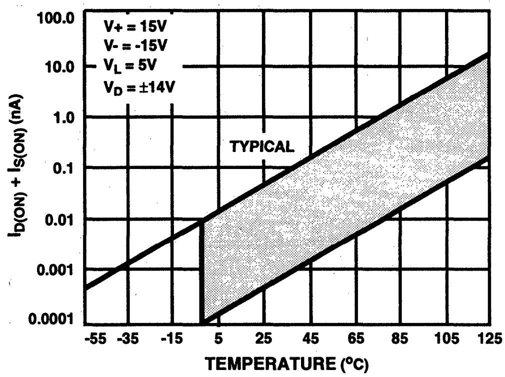


FIGURE 10. $I_{D(ON)} + I_{S(ON)}$ vs TEMPERATURE

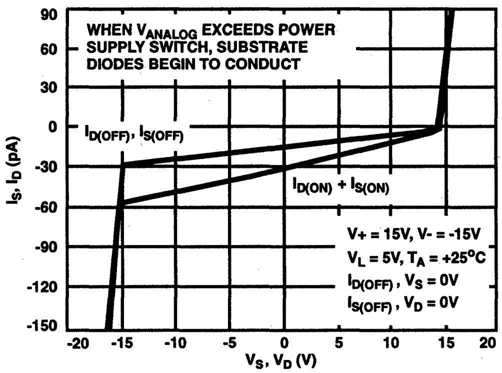


FIGURE 11. LEAKAGE CURRENT vs ANALOG VOLTAGE

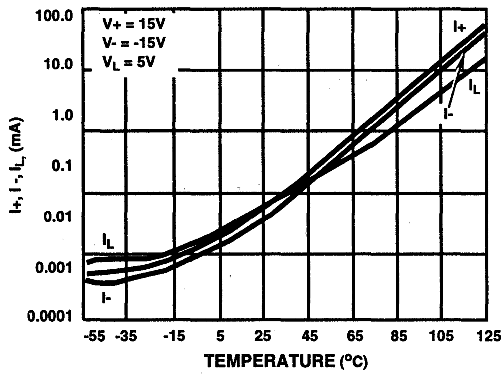


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE

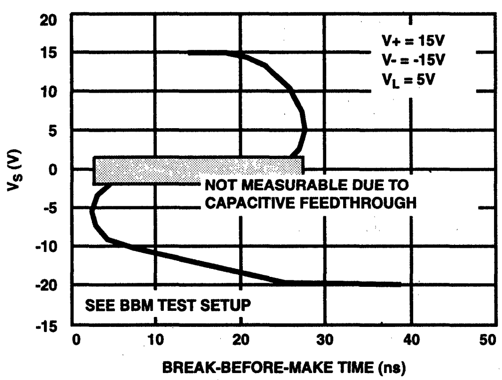


FIGURE 13. BREAK-BEFORE-MAKE vs ANALOG VOLTAGE

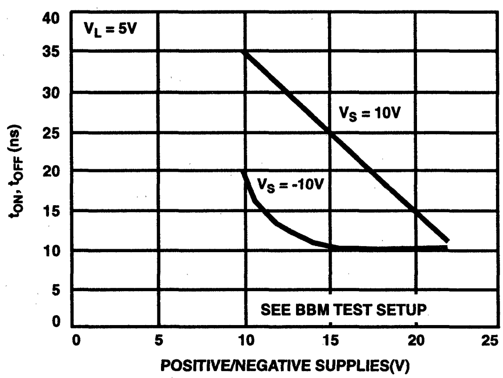


FIGURE 14. BREAK-BEFORE-MAKE vs POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

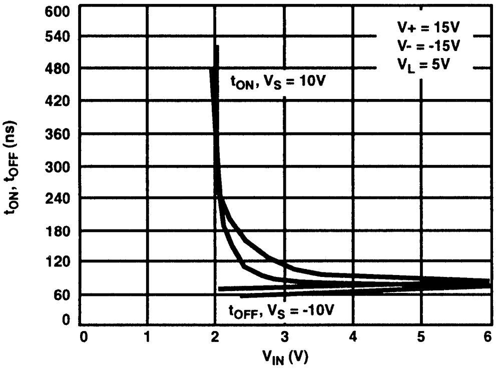


FIGURE 15. SWITCHING TIME vs INPUT LOGIC VOLTAGE (V_{IN}) (NOTE 1)

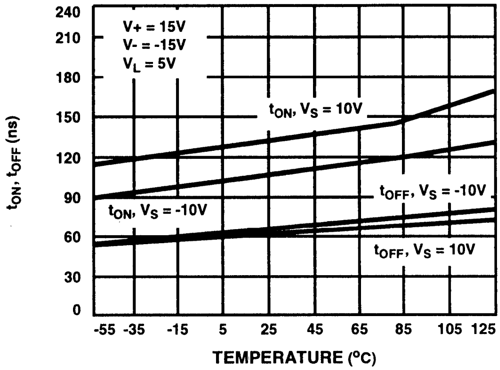


FIGURE 16. SWITCHING TIME vs TEMPERATURE (NOTE 1)

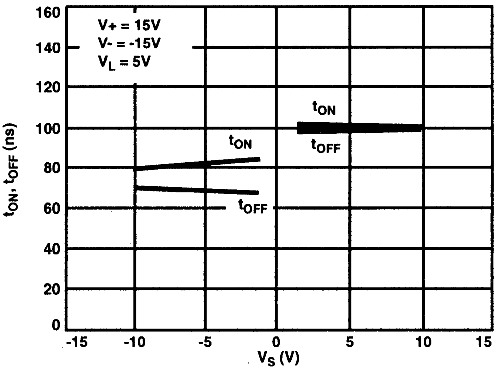


FIGURE 17. SWITCHING TIME vs ANALOG VOLTAGE (NOTE 1)

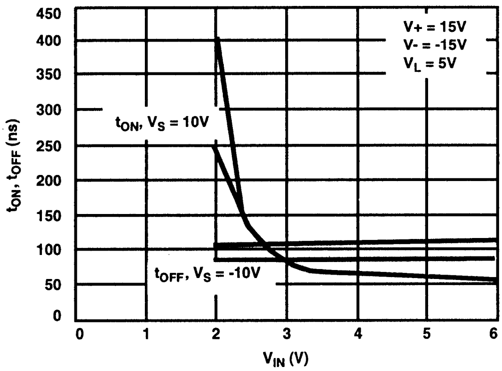


FIGURE 18. SWITCHING TIME vs INPUT LOGIC VOLTAGE (V_{IN}) (NOTE 1)

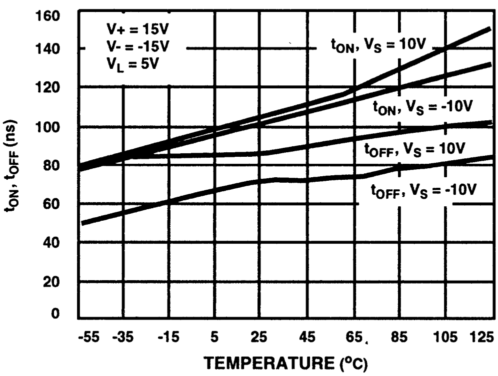


FIGURE 19. SWITCHING TIME vs TEMPERATURE (NOTE 1)

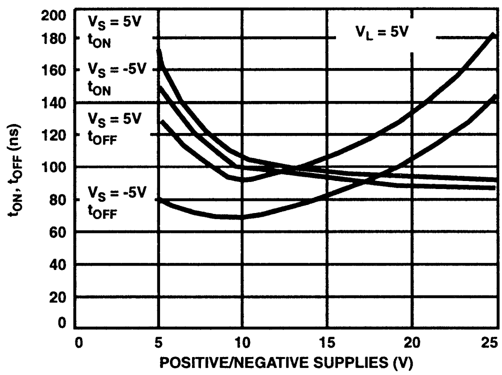


FIGURE 20. SWITCHING TIME vs POWER SUPPLY VOLTAGE (NOTE 1)

7

SWITCHES

Typical Performance Curves (Continued)

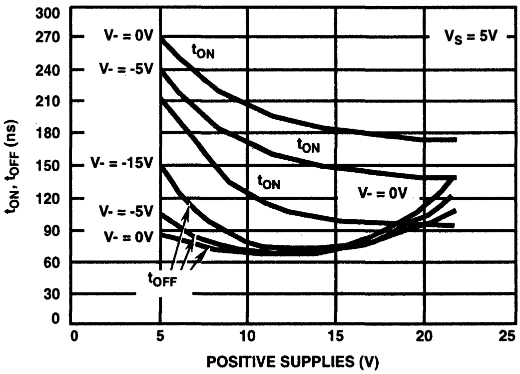


FIGURE 21. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

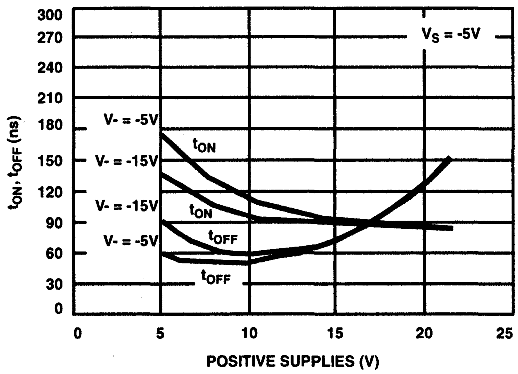


FIGURE 22. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

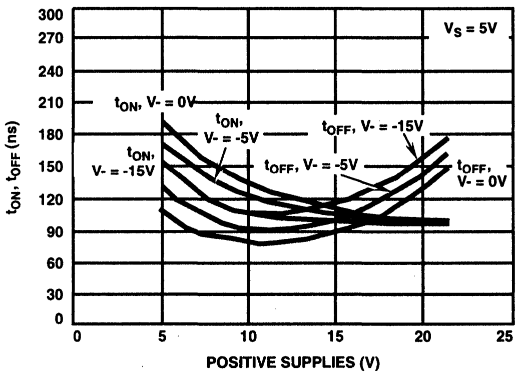


FIGURE 23. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

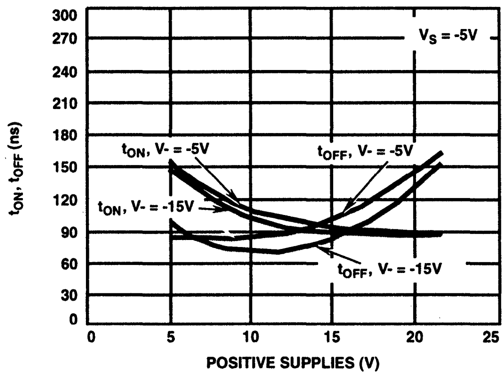
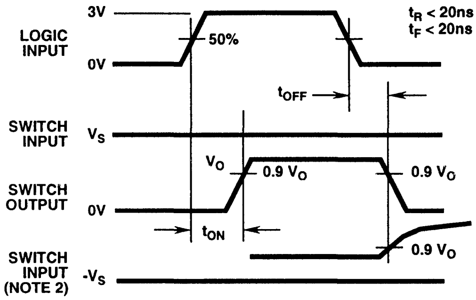


FIGURE 24. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE (NOTE 1)

NOTE:

1. Refer to Figure 1 for test conditions.

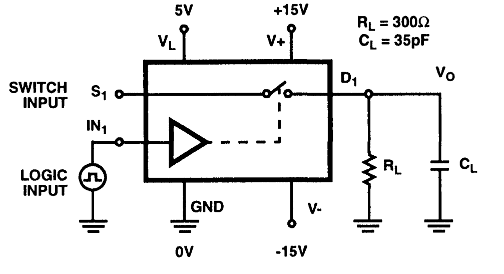
Test Circuits



NOTES:

1. Logic input waveform is inverted for switches that have the opposite logic sense.
2. V_S = 10V for t_{ON}, V_S = -10V for t_{OFF}.

FIGURE 25A.



Repeat test for IN_2 and S_2

For load conditions, see Specifications. C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 25B.

FIGURE 25. SWITCHING TIME

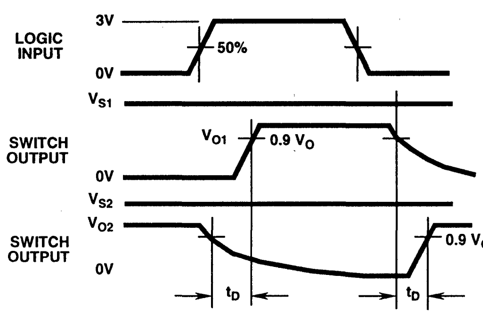
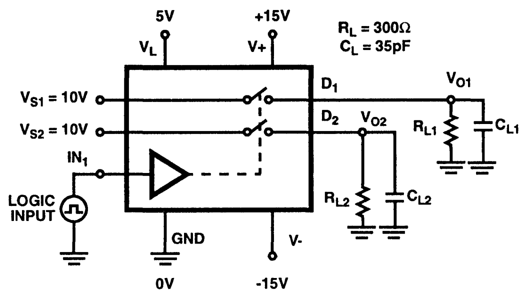


FIGURE 26A.



C_L (includes fixture and stray capacitance)

FIGURE 26B.

FIGURE 26. BREAK-BEFORE-MAKE

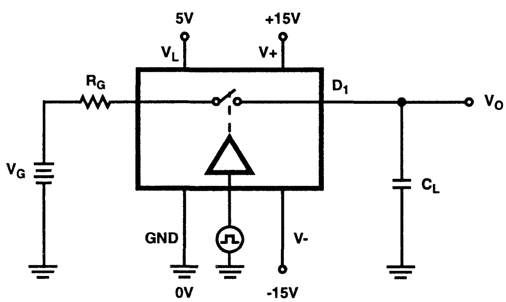
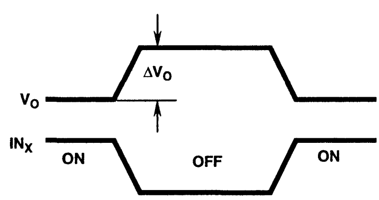


FIGURE 27A.



Q = ΔV_O x C_L

FIGURE 27B.

FIGURE 27. CHARGE INJECTION

Test Circuits (Continued)

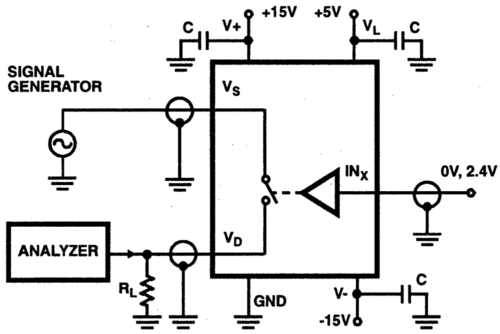


FIGURE 28. OFF ISOLATION

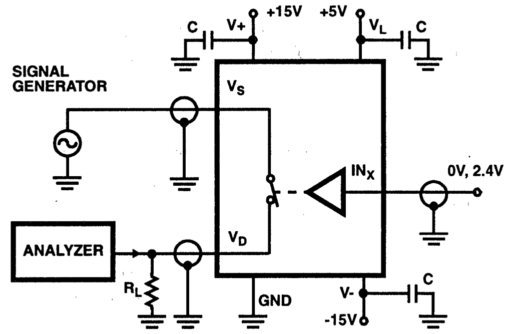


FIGURE 29. INSERTION LOSS

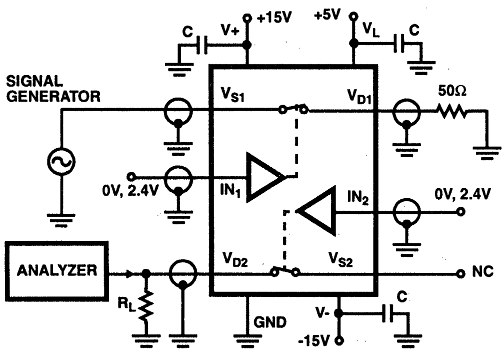


FIGURE 30. CROSSTALK

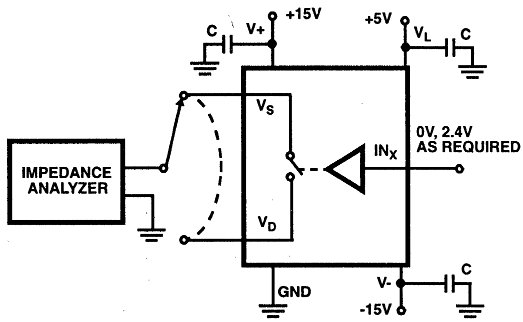


FIGURE 31. CAPACITANCES

Dual Slope Integrators

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor C_1 or C_2. Another one selects e_{IN} or discharges the capacitor in preparation for the next integration cycle.

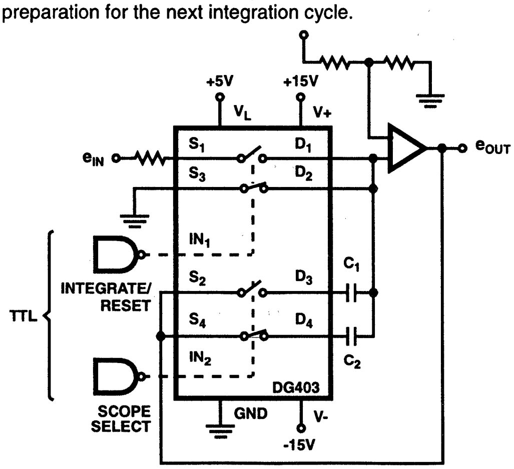


FIGURE 32. DUAL SLOPE INTEGRATOR

Peak Detector

A_3 acting as a comparator provides the logic drive for operating SW_1. the output of A_2 is fed back to A_3 and compared to the analog input e_{IN}. If $e_{IN} > e_{OUT}$ the output of A_3 is high keeping SW_1 closed. This allows C_1 to charge up to the analog input voltage. When e_{IN} goes below e_{OUT} of A_3 goes negative, turning SW_1 off. the system will therefore store the most positive analog input experienced.

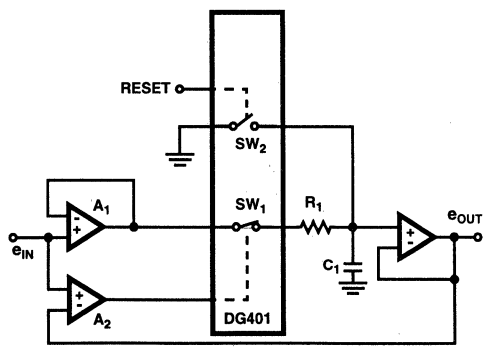


FIGURE 33. POSITIVE PEAK DETECTOR

SIGNAL PROCESSING NEW RELEASES 8

VIDEO SWITCHES

PAGE

VIDEO SWITCH DATA SHEETS

HARRIS SEMICONDUCTOR

HA4201

Wideband, 1 x 1 Video Crosspoint Switch with Tally Output

July 1995

Features

- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1700V/μs
- 0.1dB Gain Flatness 250MHz
- Off Isolation (100MHz) 85dB
- Differential Gain 0.01%
- Differential Phase .... 0.01 Degrees
- High ESD Rating .... >2000V
- TTL Compatible Enable Input
- Open Collector Tally Output
- Improved Replacement for GX4201

Applications

- Professional Video Switching and Routing
- Video Multiplexers
- HDTV
- Computer Graphics
- RF Switching and Routing
- PCM Data Routing

Description

The HA4201 is a very wide bandwidth 1 x 1 crosspoint switch ideal for professional video switching, HDTV, computer monitor routing, and other high performance applications. The circuit features very low power dissipation (105mW Enabled, 1mW Disabled), excellent differential gain and phase, and very high off isolation. When disabled, the output is switched to a high impedance state, making the HA4201 ideal for routing matrix equipment.

The HA4201 requires no external current source, and features fast switching and symmetric slew rates. The tally output is an open collector PNP transistor to V_{CC}, and is activated whenever EN = 1 to provide an indication of crosspoint selection.

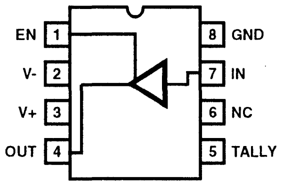
For applications which don't require a Tally output, please refer to the HA4600 data sheet.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA4201CP	0°C to +70°C	8 Lead Plastic DIP
HA4201CB	0°C to +70°C	8 Lead Plastic SOIC (N)

Pinout

HA4201
(PDIP, SOIC)
TOP VIEW



Truth Table

EN	OUT	TALLY
0	High Z	Off
1	Active	On

8 VIDEO SWITCHES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3680.2

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage. . . . . V_{SUPPLY}
Digital Input Current (Note 2) . . . . ±25mA
Analog Input Current (Note 2) . . . . ±5mA
Output Current 20mA
Junction Temperature (Die Only) . . . . +175°C
Junction Temperature (Plastic Package) . . . . +150°C
Lead Temperature (Soldering 10s). +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HA4201C. . . . . $0^oC \le T_A \le +70^oC$
Storage Temperature . . . . $-65^oC \le T_A \le +150^oC$
Thermal Package Characteristics θ_{JA}
Plastic DIP Package . . . . 130°C/W
SOIC Package. . . . . 170°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_L = 10k\Omega$, $V_{EN} = 2.0V$, Unless Otherwise Specified

PARAMETER		TEMPERATURE	HA4201C			UNITS
			MIN	TYP	MAX	
DC SUPPLY CHARACTERISTICS						
Supply Voltage		Full	±4.5	±5.0	±5.5	V
Supply Current (V_{OUT} = 0V)	V_{EN} = 2.0V	+25°C, +70°C	-	10.5	13	mA
	V_{EN} = 2.0V	0°C	-	-	14.5	mA
	V_{EN} = 0.8V	+25°C, +70°C	-	100	115	μA
	V_{EN} = 0.8V	0°C	-	100	125	μA
ANALOG DC CHARACTERISTICS						
Output Voltage Swing without Clipping ($V_{OUT} = V_{IN} \pm V_{IO} \pm 20mV$)		+25°C, +70°C	±2.7	±2.8	-	V
		0°C	±2.4	±2.5	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	μA
Output Offset Voltage		+25°C	-10	-	10	mV
Output Offset Voltage Drift (Note 1)		Full	-	25	50	μV/°C
SWITCHING CHARACTERISTICS						
Turn-On Time		+25°C	-	160	-	ns
Turn-Off Time		+25°C	-	320	-	ns
DIGITAL DC CHARACTERISTICS						
Input Logic High Voltage		Full	2	-	-	V
Input Logic Low Voltage		Full	-	-	0.8	V
EN Input Current (V_{EN} = 0 to 4V)		Full	-2	-	2	μA
Tally Output High Voltage (I_{OH} = 1mA)		Full	4.7	4.8	-	V
Tally Off Leakage Current (V_{TALLY} = 0V, -5V)		Full	-20	-	20	μA
AC CHARACTERISTICS						
Insertion Loss (±1V)		Full	-	0.04	0.05	dB
-3dB Bandwidth	$R_S = 82\Omega$, C_L = 10pF		-	480	-	MHz
	$R_S = 43\Omega$, C_L = 15pF	+25°C	-	380	-	MHz
	$R_S = 36\Omega$, C_L = 21pF	+25°C	-	370	-	MHz
±0.1dB Flat Bandwidth	$R_S = 82\Omega$, C_L = 10pF	+25°C	-	250	-	MHz
	$R_S = 43\Omega$, C_L = 15pF	+25°C	-	175	-	MHz
	$R_S = 36\Omega$, C_L = 21pF	+25°C	-	170	-	MHz
Input Resistance		Full	200	400	-	kΩ
Input Capacitance		Full	-	1.0	-	pF

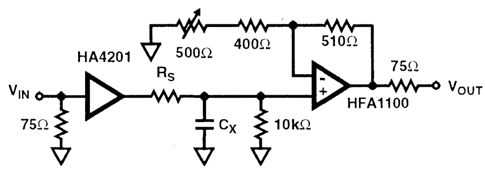
Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_L = 10k\Omega$, $V_{EN} = 2.0V$, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMPERATURE	HA4201C			UNITS
			MIN	TYP	MAX	
Enabled Output Resistance		Full	-	15	-	Ω
Disabled Output Capacitance (V_{EN} = 0.8V)		Full	-	2.0	-	pF
Differential Gain (4.43MHz, Note 1)		+25°C	-	0.01	0.02	%
Differential Phase (4.43MHz, Note 1)		+25°C	-	0.01	0.02	Degrees
Off Isolation ($1V_{P-P}$, 100MHz, V_{EN} = 0.8V, R_L = 10Ω)		Full	-	85	-	dB
Slew Rate ($1.5V_{P-P}$, +SR/-SR)	R_S = 82Ω, C_L = 10pF	+25°C	-	1750/1770	-	V/µs
	R_S = 43Ω, C_L = 15pF	+25°C	-	1460/1360	-	V/µs
	R_S = 36Ω, C_L = 21pF	+25°C	-	1410/1360	-	V/µs
Total Harmonic Distortion (Note 1)		Full	-	0.01	0.1	%
Disabled Output Resistance		Full	-	12	-	MΩ

NOTES:

1. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
2. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.

AC Test Circuit



NOTE: $C_L = C_X$ + Test Fixture Capacitance.

PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Keep input and output traces as short as possible, because trace inductance and capacitance can easily become the performance limiting items.

Application Information

General

The HA4201 is a 1 x 1 crosspoint switch that is ideal for the matrix element in small, high input-to-output isolation switchers and routers. It also excels as an input buffer for routers with a large number of outputs (i.e. each input must connect to a large number of outputs) and delivers performance superior to most video amplifiers at a fraction of the cost. As an input buffer, the HA4201's low input capacitance and high input resistance provide excellent video terminations when used with an external 75Ω resistor. This crosspoint contains no feedback or gain setting resistors, so the output is a true high impedance load when the IC is disabled (EN = 0).

Frequency Response

Most applications utilizing the HA4201 require a series output resistor, R_S, to tune the response for the specific load capacitance, C_L, driven. Bandwidth and slew rate degrade as C_L increases (as shown in the Electrical Specification table), so give careful consideration to component placement to minimize trace length. As an example, -3dB bandwidth decreases to 160MHz for C_L = 100pF, R_S = 0Ω. In big matrix configurations where C_L is large, better frequency response is obtained by cascading two levels of crosspoints in the case of multiplexed outputs (see Figure 2), or distributing the load between two drivers if C_L is due to bussing and subsequent stage input capacitance.

Control Signals

EN - The ENABLE input is a TTL/CMOS compatible, active high input. When driven low this input forces the output to a true high impedance state and reduces the power dissipation by two orders of magnitude. The EN input has no on-chip pull-up resistor, so it must be connected to a logic high (recommend V+) if the enable function isn't utilized.

Tally - The Tally output is an open collector PNP transistor connected to V+. When EN = 1, the PNP transistor is enabled and current is delivered to the load. When the crosspoint is disabled, the Tally output presents a very high impedance to the external circuitry. Several Tally outputs may be wire OR'd together to generate complex control signals, as shown with the HA4404 in the application circuits below. The Tally load may be terminated to GND or to V- as long as the continuous output current doesn't exceed 3mA (6mA at 50% duty cycle, etc.).

Switcher/Router Applications

Figure 1 illustrates one possible implementation of a wide-band, low power, 4 x 4 switcher/router. A 4 x 4 switcher/router allows any of the four outputs to be driven by any one of the four inputs (e.g. each of the four inputs may connect to a different output, or an input may connect to multiple outputs). This application utilizes the HA4201 for the input buffer, the HA4404 (4 x 1 crosspoint switch) as the switch matrix, and the HFA1112 (programmable gain buffer) as the gain of two output driver. Figure 2 details a 16 x 1 switcher (basically a 16:1 mux) which uses the HA4201 in a cascaded stage configuration to minimize capacitive loading at each output node, thus increasing system bandwidth.

Power Up Considerations

No signals should be applied to the analog or digital inputs before the power supplies are activated. Latch-up may occur if the inputs are driven at the time of power up. To prevent latch-up, the input currents during power up must not exceed the values listed in the Absolute Maximum Ratings.

Harris' Crosspoint Family

Harris offers a variety of 1 x 1 and 4 x 1 crosspoint switches. In addition to the HA4201, the 1 x 1 family includes the HA4600 which is an essentially similar device but without the Tally output. The 4 x 1 family is comprised of the HA4314, HA4404, and HA4344. The HA4314 is a 14 lead basic 4 x 1 crosspoint. The HA4404 is a 16 lead device with Tally outputs to indicate the selected channel. The HA4344 is a 16 lead crosspoint with synchronized control lines (A0, A1, $\overline{CS}$). With synchronization, the control information for the next channel switch can be loaded into the crosspoint without affecting the current state. On a subsequent clock edge the stored control state effects the desired channel switch.

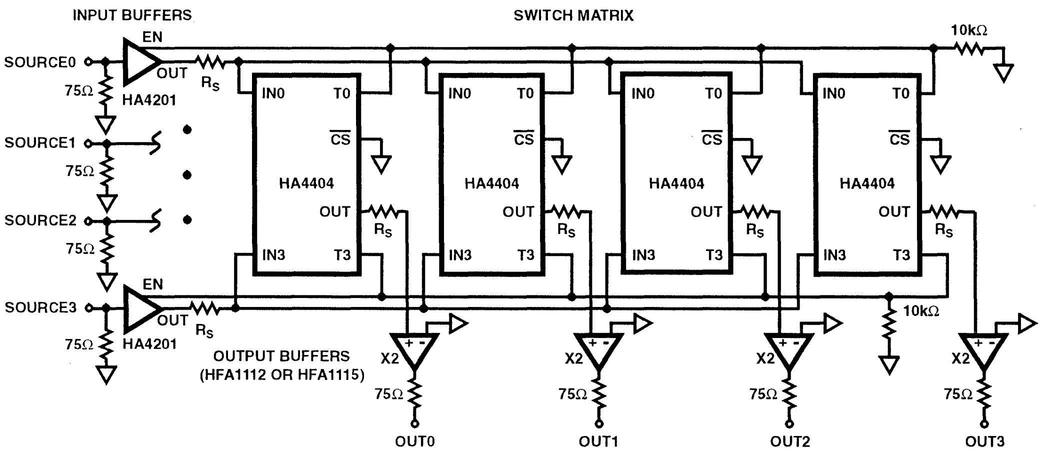


FIGURE 1. 4 x 4 SWITCHER/ROUTER APPLICATION

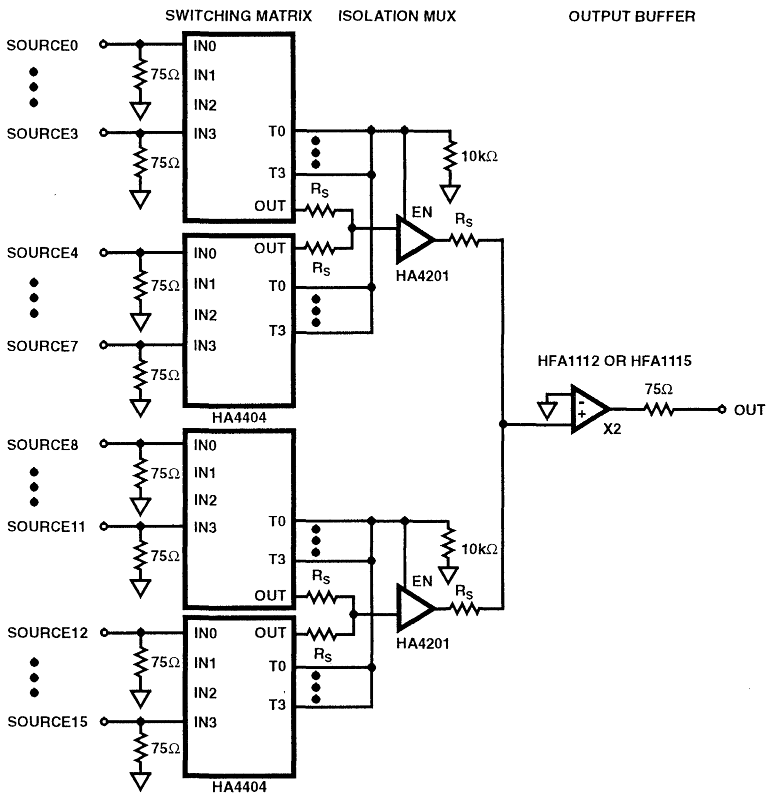


FIGURE 2. 16 x 1 SWITCHER APPLICATION

Die Characteristics

DIE DIMENSIONS:

54 x 39 x 19 ± 1mils

1380µm x 1000µm x 483µm ±25.4µm

METALLIZATION:

Type: Metal 1: AlCu (1%)/TiW
Thickness: Metal 1: 6kÅ ± 0.8kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ± 1.1kÅ

GLASSIVATION:

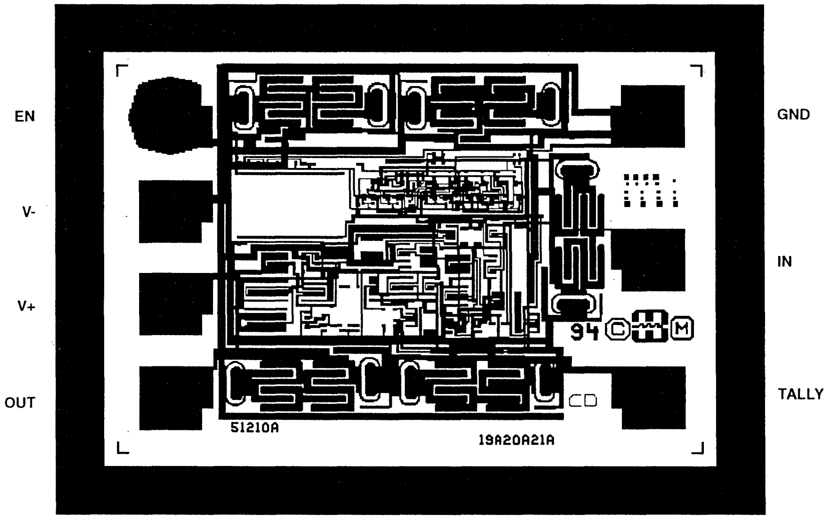
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

TRANSISTOR COUNT: 53

SUBSTRATE POTENTIAL (Powered Up): V-

Metallization Mask Layout

HA4201



Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 10k\Omega$, Unless Otherwise Specified

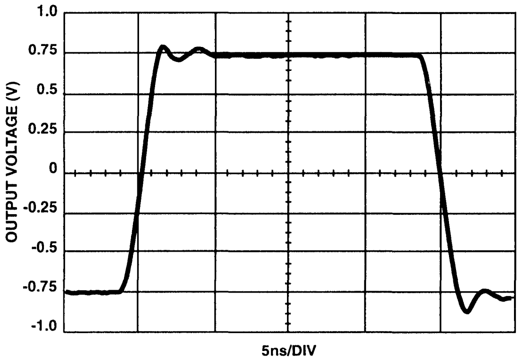


FIGURE 3. LARGE SIGNAL PULSE RESPONSE

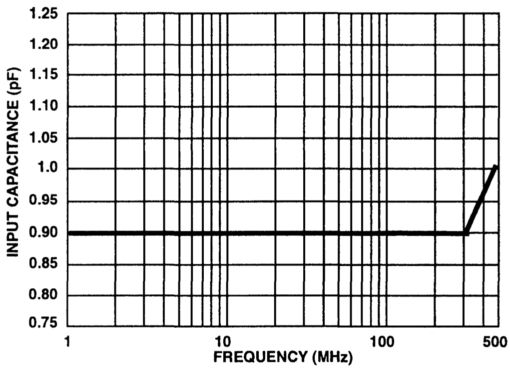


FIGURE 4. INPUT CAPACITANCE vs FREQUENCY

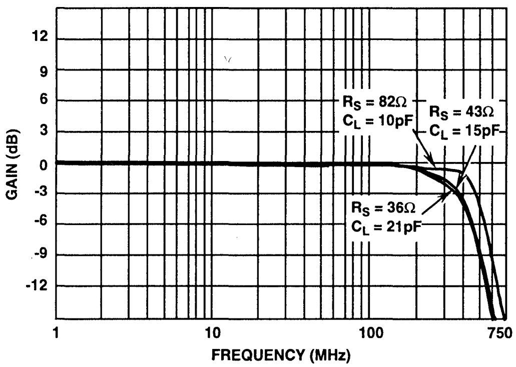


FIGURE 5. FREQUENCY RESPONSE

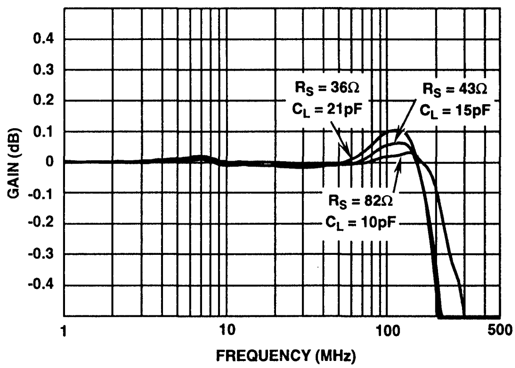


FIGURE 6. GAIN FLATNESS

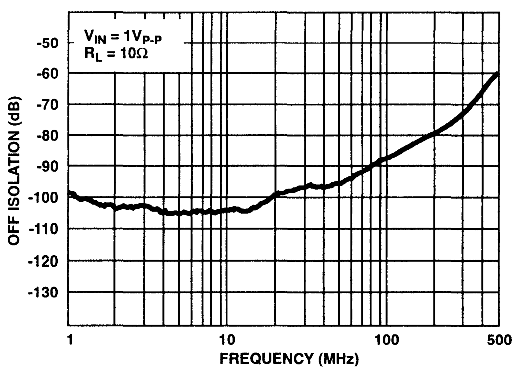


FIGURE 7. OFF ISOLATION

8

VIDEO SWITCHES

HARRIS SEMICONDUCTOR

HA4314, HA4314A

Wideband, 4 x 1 Video Crosspoint Switch

July 1995

Features

- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1400V/μs
- 0.1dB Gain Flatness...................... 100MHz
- -3dB Bandwidth 400MHz
- Off Isolation (100MHz)....................... 70dB
- Crosstalk Rejection (30MHz)................. 80dB
- Differential Gain and Phase ..... 0.01%/0.01 Degrees
- High ESD Rating .... >2000V
- TTL Compatible Control Inputs
- Improved Replacement for GX4314 and GX4314L

Applications

- Professional Video Switching and Routing
- HDTV
- Computer Graphics
- RF Switching and Routing
- PCM Data Routing

Description

The HA4314 is a very wide bandwidth 4 x 1 crosspoint switch ideal for professional video switching, HDTV, computer monitor routing, and other high performance applications. The circuit features very low power dissipation (105mW Enabled, 4mW Disabled), excellent differential gain and phase, and very high off isolation. When disabled, the output is switched to a high impedance state, making the HA4314 ideal for routing matrix equipment.

The HA4314 requires no external current source, and features fast switching and symmetric slew rates.

The only difference between the HA4314 and HA4314A is that the A grade part has lower disabled output capacitance.

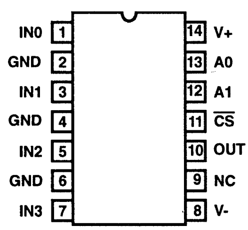
For a 4 x 1 crosspoint with Tally outputs (channel indicators) or with synchronous control signals, please refer to the HA4404A and HA4344A data sheets, respectively.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA4314CB	0°C to +70°C	14 Lead Plastic SOIC (N)
HA4314ACP	0°C to +70°C	14 Lead Plastic DIP
HA4314ACB	0°C to +70°C	14 Lead Plastic SOIC (N)

Pinout

HA4314, HA4314A
(PDIP, SOIC)
TOP VIEW



Truth Table

$\overline{CS}$	A1	A0	OUT
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3
1	X	X	HIGH - Z

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3679.2**

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage. . . . . V_{SUPPLY}
Digital Input Current (Note 2) . . . . ±25mA
Analog Input Current (Note 2) . . . . ±5mA
Output Current 20mA
Junction Temperature (Die Only) . . . . +175°C
Junction Temperature (Plastic Package) . . . . +150°C
Lead Temperature (Soldering 10s). . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HA4314C, HA4314AC. 0°C ≤ T_A ≤ +70°C
Storage Temperature . . . . -65°C ≤ T_A ≤ +150°C
Thermal Package Characteristics (°C/W) θ_{JA}
Plastic DIP Package 100
SOIC Package. 120

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, $V_{\overline{CS}}$ = 0.8V, Unless Otherwise Specified

PARAMETER		(NOTE 3) TEMPERATURE	HA4314C, HA4314AC MIN	TYP	MAX	UNITS
DC SUPPLY CHARACTERISTICS						
Supply Voltage		Full	±4.5	±5.0	±5.5	V
Supply Current (V_{OUT} = 0V)	$V_{\overline{CS}}$ = 0.8V	+25°C, +70°C	-	10.5	13	mA
	$V_{\overline{CS}}$ = 0.8V	0°C	-	-	15.5	mA
	$V_{\overline{CS}}$ = 2.0V	+25°C, +70°C	-	400	450	µA
	$V_{\overline{CS}}$ = 2.0V	0°C	-	400	580	µA
ANALOG DC CHARACTERISTICS						
Output Voltage Swing without Clipping (V_{OUT} = V_{IN} ± V_{IO} ± 20mV)		+25°C, +70°C	±2.7	±2.8	-	V
		0°C	±2.4	±2.5	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	µA
Output Offset Voltage		Full	-10	-	10	mV
Output Offset Voltage Drift (Note 1)		Full	-	25	50	µV/°C
SWITCHING CHARACTERISTICS						
Turn-On Time		+25°C	-	160	-	ns
Turn-Off Time		+25°C	-	320	-	ns
Output Glitch During Switching		+25°C	-	±10	-	mV
DIGITAL DC CHARACTERISTICS						
Input Logic High Voltage		Full	2	-	-	V
Input Logic Low Voltage		Full	-	-	0.8	V
Input Current (0V to 4V)		Full	-2	-	2	µA
AC CHARACTERISTICS						
Insertion Loss (±1V)		+25°C	-	0.055	0.063	dB
		Full	-	0.07	0.08	dB
Channel-to-Channel Insertion Loss Match		Full	-	±0.004	±0.006	dB
-3dB Bandwidth	R_S = 50Ω, C_L = 10pF	+25°C	-	400	-	MHz
	R_S = 20Ω, C_L = 20pF	+25°C	-	280	-	MHz
	R_S = 16Ω, C_L = 36pF	+25°C	-	140	-	MHz
	R_S = 13Ω, C_L = 49pF	+25°C	-	110	-	MHz

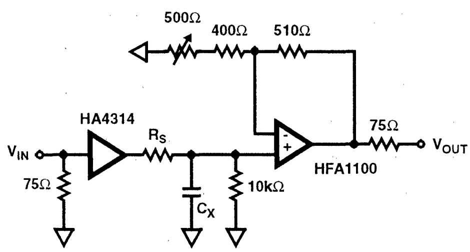
Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_L = 10k\Omega$, $V_{\overline{CS}} = 0.8V$, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 3) TEMPERATURE	HA4314C, HA4314AC MIN	TYP	MAX	UNITS
±0.1dB Flat Bandwidth	$R_S = 50\Omega$, $C_L = 10pF$	+25°C	-	100	-	MHz
	$R_S = 20\Omega$, $C_L = 20pF$	+25°C	-	100	-	MHz
	$R_S = 16\Omega$, $C_L = 36pF$	+25°C	-	85	-	MHz
	$R_S = 13\Omega$, $C_L = 49pF$	+25°C	-	75	-	MHz
Input Resistance		Full	200	400	-	kΩ
Input Capacitance		Full	-	1.5	-	pF
Enabled Output Resistance		Full	-	15	-	Ω
Disabled Output Capacitance ($V_{\overline{CS}} = 2.0V$)	HA4314	Full	-	6.5	-	pF
	HA4314A	Full	-	2.5	-	pF
Differential Gain (4.43MHz, Note 1)		+25°C	-	0.01	0.02	%
Differential Phase (4.43MHz, Note 1)		+25°C	-	0.01	0.02	Degrees
Off Isolation ($1V_{P-P}$, 100MHz, $V_{\overline{CS}} = 2.0V$, $R_L = 10\Omega$)		Full	-	70	-	dB
Crosstalk Rejection ($1V_{P-P}$, 30MHz)		Full	-	80	-	dB
Slew Rate ($1.5V_{P-P}$, +SR/-SR)	$R_S = 50\Omega$, $C_L = 10pF$	+25°C	-	1425/1450	-	V/µs
	$R_S = 20\Omega$, $C_L = 20pF$	+25°C	-	1010/1010	-	V/µs
	$R_S = 16\Omega$, $C_L = 36pF$	+25°C	-	725/750	-	V/µs
	$R_S = 13\Omega$, $C_L = 49pF$	+25°C	-	600/650	-	V/µs
Total Harmonic Distortion (10MHz, $R_L = 1k\Omega$, Note 1)		Full	-	0.01	0.1	%
Disabled Output Resistance ($V_{\overline{CS}} = 2.0V$)		Full	-	12	-	MΩ

NOTES:

1. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
2. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.
3. Units are 100% tested at +25°C, Sample tested at +70°C, Guaranteed but not tested at 0°C.

AC Test Circuit



NOTE:

1. $C_L = C_X$ + Test Fixture Capacitance.

PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Keep input and output traces as short as possible, because trace inductance and capacitance can easily become the performance limiting items.

Application Information

General

The HA4314 is a 4 x 1 crosspoint switch that is ideal for the matrix element of high performance switchers and routers. This crosspoint's low input capacitance and high input resistance provide excellent video terminations when used with an external 75Ω resistor. Nevertheless, if several HA4314 inputs are connected together, the use of an input buffer should be considered (see Figure 1). This crosspoint contains no feedback or gain setting resistors, so the output is a true high impedance load when the IC is disabled ($\overline{CS} = 1$).

Ground Connections

All GND pins are connected to a common point on the die, so any one of them will suffice as the functional GND connection. For the best isolation and crosstalk rejection, however, all GND pins must connect to the GND plane.

Frequency Response

Most applications utilizing the HA4314 require a series output resistor, R_S, to tune the response for the specific load capacitance, C_L, driven. Bandwidth and slew rate degrade as C_L increases (as shown in the Electrical Specification table), so give careful consideration to component placement to minimize trace length. In big matrix configurations where C_L is large, better frequency response is obtained by cascading two levels of crosspoints in the case of multiplexed outputs (see Figure 2), or distributing the load between two drivers if C_L is due to bussing and subsequent stage input capacitance.

Control Signals

$\overline{CS}$ - This is a TTL/CMOS compatible, active low Chip Select input. When driven high, $\overline{CS}$ forces the output to a true high impedance state and reduces the power dissipation by a factor of 25. The $\overline{CS}$ input has no on-chip pull-down resistor, so it must be connected to a logic low (recommend GND) if the enable function isn't utilized.

A0, A1 - These are binary coded, TTL/CMOS compatible address inputs that select which one of the four inputs connect to the crosspoint output.

Switcher/Router Applications

Figure 1 illustrates one possible implementation of a wideband, low power, 4 x 4 switcher/router utilizing the HA4314 for the switch matrix. A 4 x 4 switcher/router allows any of the four outputs to be driven by any one of the four inputs (e.g. each of the four inputs may connect to a different output, or an input may connect to multiple outputs). This application utilizes the HA4600 (video buffer with output disable) for the input buffer, the HA4314 as the switch matrix, and the HFA1112 (programmable gain buffer) as the gain of two output driver. Figure 2 details a 16 x 1 switcher (basically a 16:1 mux) which uses the HA4201 (1 x 1 crosspoint) and the HA4314 in a cascaded stage configuration to minimize capacitive loading at each output node, thus increasing system bandwidth.

Power Up Considerations

No signals should be applied to the analog or digital inputs before the power supplies are activated. Latch-up may occur if the inputs are driven at the time of power up. To prevent latch-up, the input currents during power up must not exceed the values listed in the Absolute Maximum Ratings.

Harris' Crosspoint Family

Harris offers a variety of 4 x 1 and 1 x 1 crosspoint switches. In addition to the HA4314, the 4 x 1 family includes the HA4404 and HA4344. The HA4404 is a 16 lead device with Tally outputs to indicate the selected channel. The HA4344 is a 16 lead crosspoint with synchronized control lines (A0,

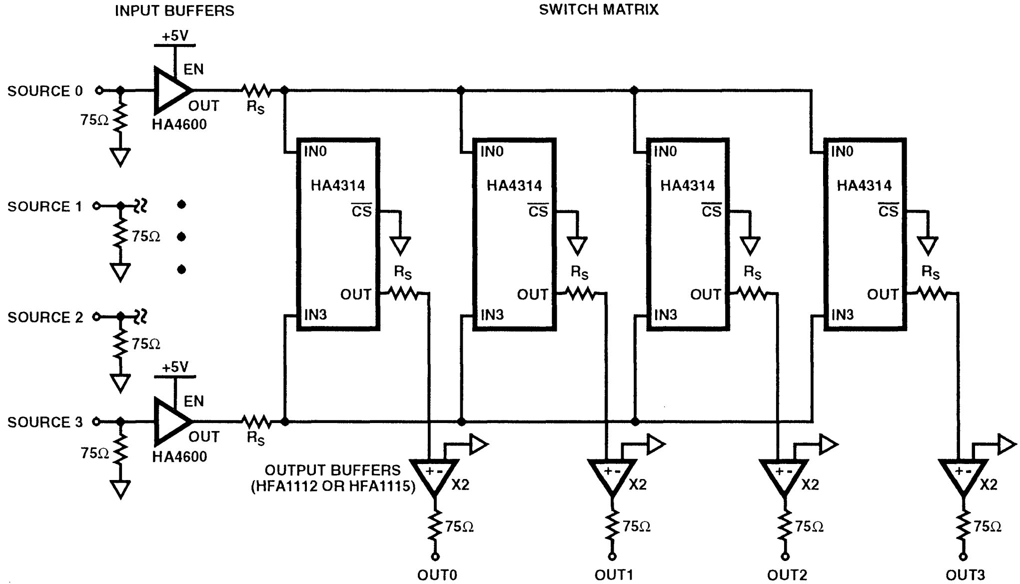


FIGURE 1. 4 x 4 SWITCHER/ROUTER APPLICATION

A1, $\overline{CS}$). With synchronization, the control information for the next channel switch can be loaded into the crosspoint without affecting the current state. On a subsequent clock edge the stored control state effects the desired channel switch.

The 1 x 1 family is comprised of the HA4201 and HA4600. They are essentially similar devices, but the HA4201 includes a Tally output (enable indicator). The 1 x 1s are useful as high performance video input buffers, or in a switch matrix requiring very high off isolation.

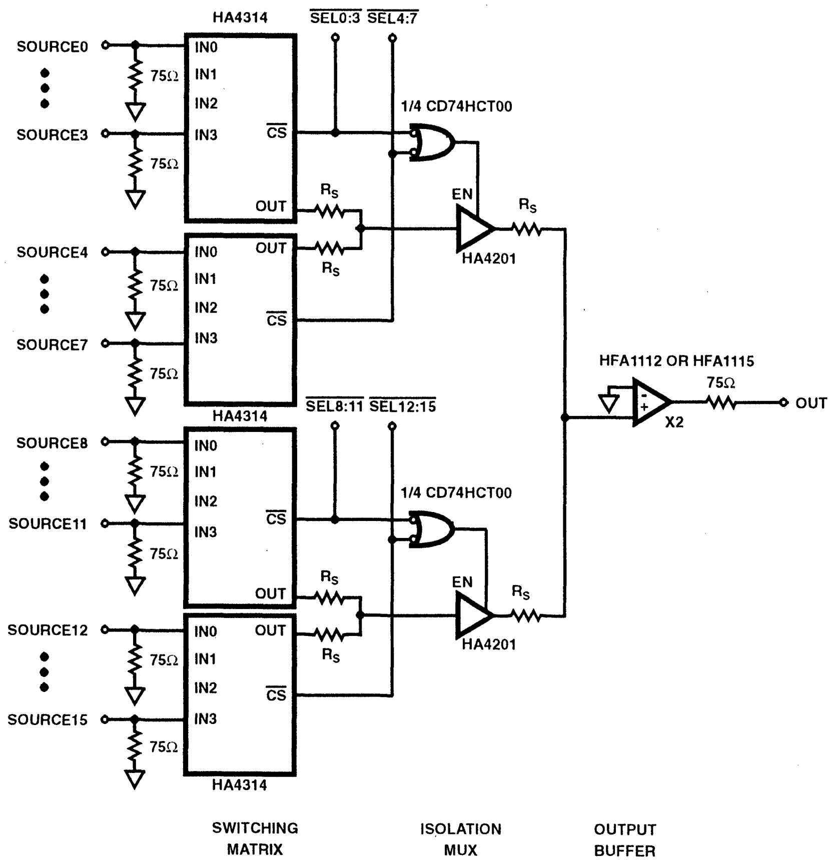


FIGURE 2. 16 x 1 SWITCHER APPLICATION

Die Characteristics

DIE DIMENSIONS:

65 x 118 x 19 ±1mil

1640μm x 3000μm x 483μm ±25.4μm

METALLIZATION:

Type: Metal 1: AlCu (1%)/TiW
Thickness: Metal 1: 6kÅ ±0.8kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±1.1kÅ

GLASSIVATION:

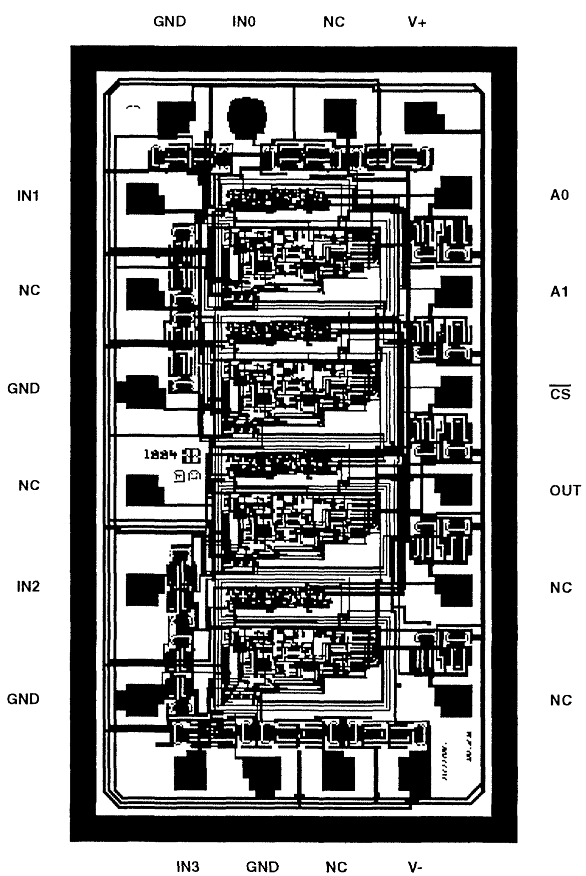
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT: 200

SUBSTRATE POTENTIAL (Powered Up): V-

Metallization Mask Layout

HA4314, HA4314A



Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 10k\Omega$, Unless Otherwise Specified

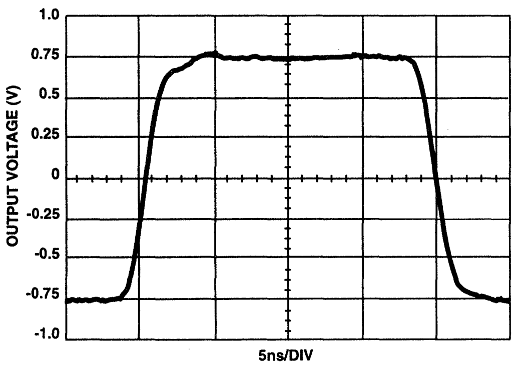


FIGURE 3. LARGE SIGNAL PULSE RESPONSE

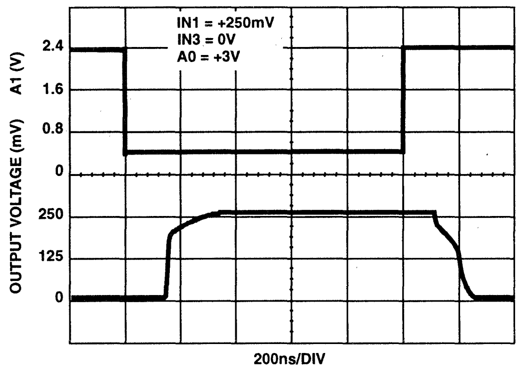


FIGURE 4. CHANNEL-TO-CHANNEL SWITCHING RESPONSE

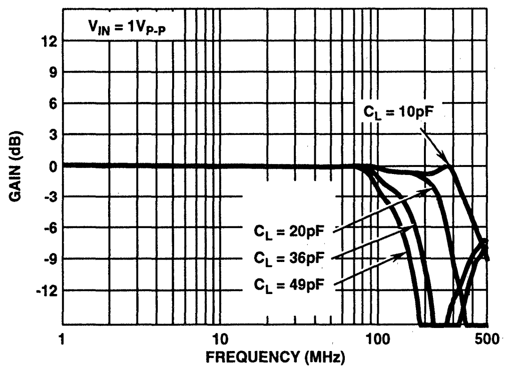


FIGURE 5. FREQUENCY RESPONSE

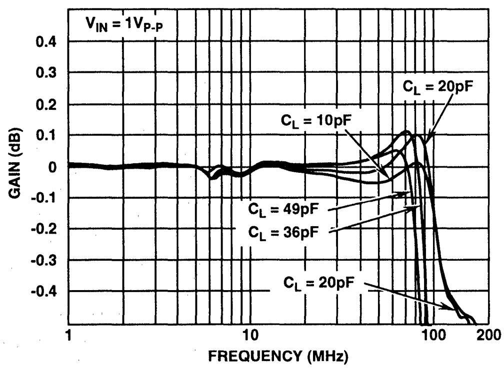


FIGURE 6. GAIN FLATNESS

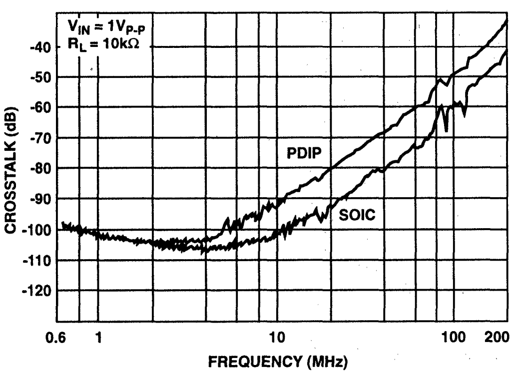


FIGURE 7. ALL HOSTILE CROSSTALK REJECTION

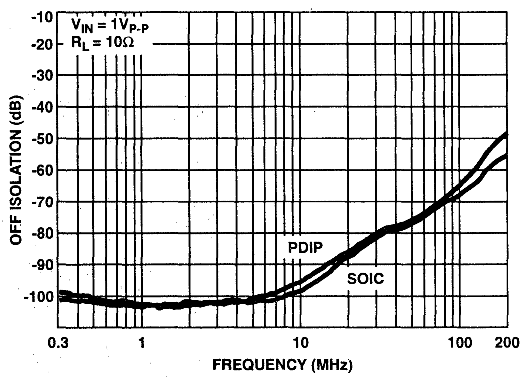


FIGURE 8. ALL HOSTILE OFF ISOLATION

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 10k\Omega$, Unless Otherwise Specified **(Continued)**

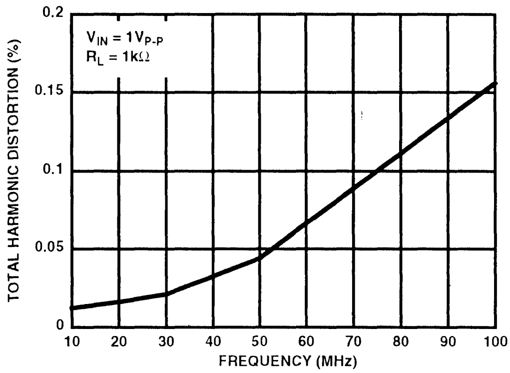


FIGURE 9. TOTAL HARMONIC DISTORTION vs FREQUENCY

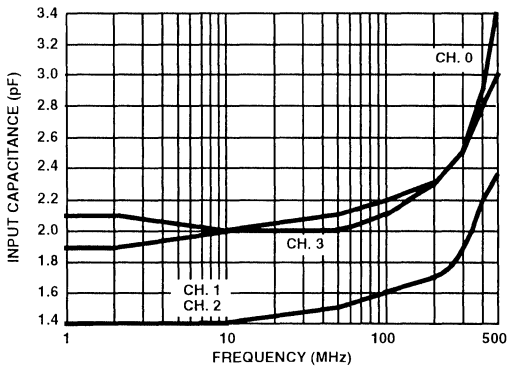


FIGURE 10. INPUT CAPACITANCE vs FREQUENCY

8

VIDEO SWITCHES

HARRIS SEMICONDUCTOR

HA4344B

PRELIMINARY

July 1995

Wideband, 4 x 1 Video Crosspoint Switch with Synchronous Controls

Features

- **Low Power Dissipation 105mW**
- **Symmetrical Slew Rates 1400V/µs**
- **0.1dB Gain Flatness. 100MHz**
- **-3dB Bandwidth 350MHz**
- **Off Isolation (100MHz). 70dB**
- **Crosstalk Rejection (30MHz). 80dB**
- **Differential Gain and Phase . . . . 0.01%/0.01Deg.**
- **High ESD Rating . . . . >2000V**
- **TTL Compatible Control Signals**
- **Latched Control Lines for Synchronous Switching**

Applications

- **Professional Video Switching and Routing**
- **RGB Video Distribution Systems**
- **Computer Graphics**
- **RF Switching and Routing**

Description

The HA4344B is a very wide bandwidth 4 x 1 crosspoint switch ideal for professional video switching, HDTV, computer display routing, and other high performance applications. This circuit features very low power dissipation, excellent differential gain and phase, high off isolation, symmetric slew rates, fast switching, and latched control signals. When disabled, the output is switched to a high impedance state, making the HA4344B ideal for matrix routers.

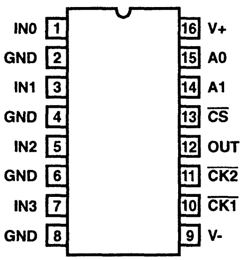
The latched control signals allow for synchronized channel switching. When $\overline{\text{CK1}}$ is low the master control latch loads the next switching address (A0, A1, $\overline{\text{CS}}$), while the closed (assuming $\overline{\text{CK2}}$ is the inverse of $\overline{\text{CK1}}$) slave control latch maintains the crosspoint in its current state. $\overline{\text{CK2}}$ switching low closes the master latch (with previous assumption), loads the now open slave latch, and switches the crosspoint to the newly selected channel. Channel selection is asynchronous (changes with any control signal change) if both $\overline{\text{CK1}}$ and $\overline{\text{CK2}}$ are low.

Ordering Information

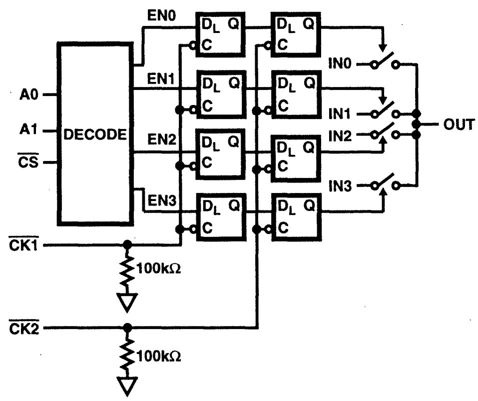
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA4344BCP	0°C to +70°C	16 Lead Plastic DIP
HA4344BCB	0°C to +70°C	16 Lead Plastic SOIC (N)

Pinout

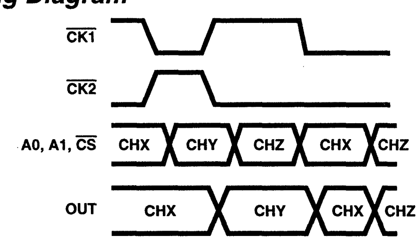
HA4344B
(PDIP, 150mil SOIC)
TOP VIEW



Functional Diagram



Timing Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage. . . . . . V_{SUPPLY}
Digital Input Current (Note 2) . . . . . . ±25mA
Analog Input Current (Note 2) . . . . . . ±5mA
Output Current 20mA
Junction Temperature (Die Only) . . . . . . +175°C
Junction Temperature (Plastic Package) . . . . . . +150°C
Lead Temperature (Soldering 10s) . . . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HA4344BC. . . . . . $0^oC \leq T_A \leq +70^oC$
Storage Temperature . . . . . . $-65^oC \leq T_A \leq +150^oC$
Thermal Package Characteristics . . . . . . θ_{JA}
Plastic DIP Package . . . . . . 90°C/W
SOIC Package . . . . . . 115°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, $V_{\overline{CS}}$ = 0.8V Unless Otherwise Specified

PARAMETER		(NOTE 3) TEMPERATURE	HA4344BC MIN	TYP	MAX	UNITS
DC SUPPLY CHARACTERISTICS						
Supply Voltage		Full	±4.5	±5.0	±5.5	V
Supply Current (V_{OUT} = 0V)	$V_{\overline{CS}}$ = 0.8V	+25°C, +70°C	-	10.5	13	mA
	$V_{\overline{CS}}$ = 0.8V	0°C	-	-	15.5	mA
	$V_{\overline{CS}}$ = 2.0V	+25°C, +70°C	-	400	450	μA
	$V_{\overline{CS}}$ = 2.0V	0°C	-	400	580	μA
ANALOG DC CHARACTERISTICS						
Output Voltage Swing Without Clipping ($V_{OUT} = V_{IN} \pm V_{IO} \pm 20mV$)		+25°C, +70°C	±2.7	±2.8	-	V
		0°C	±2.4	±2.5	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	μA
Output Offset Voltage		Full	-10	-	10	mV
Output Offset Voltage Drift (Note 1)		Full	-	25	50	μV/°C
SWITCHING CHARACTERISTICS						
Turn-On Time		+25°C	-	160	-	ns
Turn-Off Time		+25°C	-	320	-	ns
Output Glitch During Switching		+25°C	-	±10	-	mV
DIGITAL DC CHARACTERISTICS						
Input Logic High Voltage		Full	2	-	-	V
Input Logic Low Voltage		Full	-	-	0.8	V
$\overline{CLK1}$, $\overline{CLK2}$ Input Current (0 to 4V)		Full	-	40	50	μA
$\overline{CS}$, A0, A1 Input Current (0 to 4V)		Full	-2	-	2	μA
AC CHARACTERISTICS						
Insertion Loss (±1V)		+25°C	-	0.055	0.063	dB
		Full	-	0.07	0.08	dB
Channel-to-Channel Insertion Loss Match		Full	-	±0.004	±0.006	dB

8

VIDEO SWITCHES

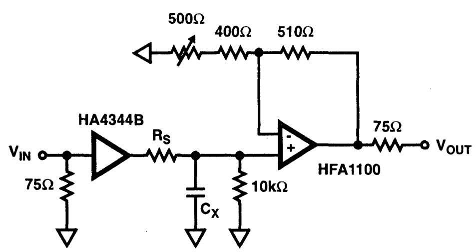
Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, $V_{\overline{CS}}$ = 0.8V Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 3) TEMPERATURE	HA4344BC MIN	TYP	MAX	UNITS
-3dB Bandwidth	R_S = 47Ω, C_L = 10pF	+25°C	-	350	-	MHz
	R_S = 29Ω, C_L = 20pF	+25°C	-	300	-	MHz
	R_S = 16Ω, C_L = 33pF	+25°C	-	220	-	MHz
	R_S = 9Ω, C_L = 52pF	+25°C	-	160	-	MHz
±0.1dB Flat Bandwidth	R_S = 47Ω, C_L = 10pF	+25°C	-	150	-	MHz
	R_S = 29Ω, C_L = 20pF	+25°C	-	110	-	MHz
	R_S = 16Ω, C_L = 33pF	+25°C	-	100	-	MHz
	R_S = 9Ω, C_L = 52pF	+25°C	-	70	-	MHz
Input Resistance		Full	200	400	-	kΩ
Input Capacitance		Full	-	1.5	-	pF
Enabled Output Resistance		Full	-	15	-	Ω
Disabled Output Capacitance ($V_{\overline{CS}}$ = 2.0V)		Full	-	2.5	-	pF
Differential Gain (4.43MHz, Note 1)		+25°C	-	0.01	0.02	%
Differential Phase (4.43MHz, Note 1)		+25°C	-	0.01	0.02	Degrees
Off Isolation (1V_{P-P}, 100MHz, $V_{\overline{CS}}$ = 2.0V)		Full	-	70	-	dB
Crosstalk Rejection (1V_{P-P}, 30MHz)		Full	-	80	-	dB
Slew Rate (1.5V_{P-P}, +SR/-SR)	R_S = 47Ω, C_L = 10pF	+25°C	-	1400/1490	-	V/μs
	R_S = 29Ω, C_L = 20pF	+25°C	-	1200/1260	-	V/μs
	R_S = 16Ω, C_L = 33pF	+25°C	-	870/940	-	V/μs
	R_S = 9Ω, C_L = 52pF	+25°C	-	750/710	-	V/μs
Total Harmonic Distortion (Note 1)		Full	-	0.01	0.1	%
Disabled Output Resistance ($V_{\overline{CS}}$ = 2.0V)		Full	-	12	-	MΩ

NOTES:

1. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
2. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.
3. Units are 100% tested at +25°C; sample tested at +70°C; guaranteed, but not tested at 0°C.

AC Test Circuit



NOTE:

1. C_L = C_X + Test Fixture Capacitance.

HA4404, HA4404A

Wideband, 4 x 1 Video Crosspoint Switch with Tally Outputs

July 1995

Features

- Low Power Dissipation 105mW
- Symmetrical Slew Rates 1250V/µs
- 0.1dB Gain Flatness..................... 165MHz
- -3dB Bandwidth......................... 330MHz
- Off Isolation (100MHz)....................... 70dB
- Crosstalk Rejection (30MHz).................. 80dB
- Differential Gain and Phase ..... 0.01%/0.01 Degrees
- High ESD Rating .... >2000V
- TTL Compatible Control Inputs
- Open Collector Tally Outputs
- Improved Replacement for GX4404

Applications

- Professional Video Switching and Routing
- HDTV
- Computer Graphics
- RF Switching and Routing

Description

The HA4404 is a very wide bandwidth 4 x 1 crosspoint switch ideal for professional video switching, HDTV, computer monitor routing, and other high performance applications. The circuit features very low power dissipation (105mW Enabled, 4mW Disabled), excellent differential gain and phase, and very high off isolation. When disabled, the output is switched to a high impedance state, making the HA4404 ideal for routing matrix equipment.

The HA4404 requires no external current source, and features fast switching and symmetric slew rates. The tally outputs are open collector PNP transistors to V_{CC} to provide an indication of crosspoint selection.

The only difference between the HA4404 and HA4404A is that the A grade part has lower disabled output capacitance.

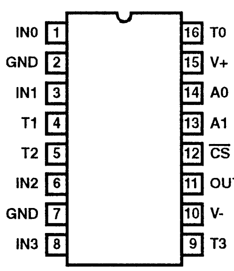
For a 4 x 1 crosspoint without Tally outputs or with synchronous control signals, please refer to the HA4314A and HA4344A Data Sheets, respectively.

Ordering Information

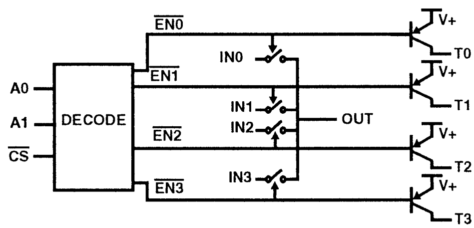
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA4404CB	0°C to +70°C	16 Lead Plastic SOIC (N)
HA4404ACP	0°C to +70°C	16 Lead Plastic DIP
HA4404ACB	0°C to +70°C	16 Lead Plastic SOIC (N)

Pinout

HA4404, HA4404A
(PDIP, SOIC)
TOP VIEW



Functional Diagram



Truth Table

$\overline{CS}$	A1	A0	OUT	ACTIVE TALLY OUTPUT
0	0	0	IN0	T0
0	0	1	IN1	T1
0	1	0	IN2	T2
0	1	1	IN3	T3
1	X	X	High - Z	None, All High - Z

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3678.2

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage. . . . . V_{SUPPLY}
Digital Input Current (Note 2) . . . . ±25mA
Analog Input Current (Note 2) . . . . ±5mA
Output Current 20mA
Junction Temperature (Die Only) . . . . +175°C
Junction Temperature (Plastic Package) . . . . +150°C
Lead Temperature (Soldering 10s). +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HA4404C, HA4404AC. $0^oC \leq T_A \leq +70^oC$
Storage Temperature . . . . $-65^oC \leq T_A \leq +150^oC$

Thermal Package Characteristics (°C/W) θ_{JA}
Plastic DIP Package 90
SOIC Package. 115

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, $V_{\overline{CS}}$ = 0.8V, Unless Otherwise Specified

PARAMETER		(NOTE 3) TEMPERATURE	HA4404C, HA4404AC MIN	TYP	MAX	UNITS
DC SUPPLY CHARACTERISTICS						
Supply Voltage		Full	±4.5	±5.0	±5.5	V
Supply Current (V_{OUT} = 0V)	$V_{\overline{CS}}$ = 0.8V	+25°C, +70°C	-	10.5	13	mA
	$V_{\overline{CS}}$ = 0.8V	0°C	-	-	15.5	mA
	$V_{\overline{CS}}$ = 2.0V	+25°C, +70°C	-	400	450	μA
	$V_{\overline{CS}}$ = 2.0V	0°C	-	400	580	μA
ANALOG DC CHARACTERISTICS						
Output Voltage Swing without Clipping ($V_{OUT} = V_{IN} \pm V_{IO} \pm 20mV$)		+25°C, +70°C	±2.7	±2.8	-	V
		0°C	±2.4	±2.5	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	μA
Output Offset Voltage		Full	-10	-	10	mV
Output Offset Voltage Drift (Note 1)		Full	-	25	50	μV/°C
SWITCHING CHARACTERISTICS						
Turn-On Time		+25°C	-	160	-	ns
Turn-Off Time		+25°C	-	320	-	ns
Output Glitch During Switching		+25°C	-	±10	-	mV
DIGITAL DC CHARACTERISTICS						
Input Logic High Voltage		Full	2	-	-	V
Input Logic Low Voltage		Full	-	-	0.8	V
Input Current (0V to 4V)		Full	-2	-	2	μA
Tally Output High Voltage (I_{OH} = 1mA)		Full	4.7	4.8	-	V
Tally Off Leakage Current (V_{TALLY} = 0V)		Full	-20	-	20	μA
AC CHARACTERISTICS						
Insertion Loss (±1V)		+25°C	-	0.055	0.063	dB
		Full	-	0.07	0.08	dB
Channel-to-Channel Insertion Loss Match		Full	-	±0.004	±0.006	dB

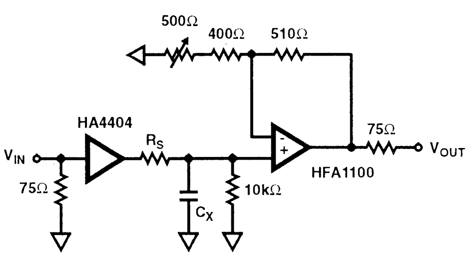
Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, $V_{\overline{CS}}$ = 0.8V, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 3) TEMPERATURE	HA4404C, HA4404AC			UNITS
			MIN	TYP	MAX	
-3dB Bandwidth	R_S = 50Ω, C_L = 11pF	+25°C	-	330	-	MHz
	R_S = 24Ω, C_L = 19pF	+25°C	-	290	-	MHz
	R_S = 15Ω, C_L = 34pF	+25°C	-	210	-	MHz
	R_S = 11Ω, C_L = 49pF	+25°C	-	170	-	MHz
±0.1dB Flat Bandwidth	R_S = 50Ω, C_L = 11pF	+25°C	-	165	-	MHz
	R_S = 24Ω, C_L = 19pF	+25°C	-	130	-	MHz
	R_S = 15Ω, C_L = 34pF	+25°C	-	137	-	MHz
	R_S = 11Ω, C_L = 49pF	+25°C	-	100	-	MHz
Input Resistance		Full	200	400	-	kΩ
Input Capacitance		Full	-	1.5	-	pF
Enabled Output Resistance		Full	-	15	-	Ω
Disabled Output Capacitance ($V_{\overline{CS}}$ = 2.0V)	HA4404	Full	-	6.5	-	pF
	HA4404A	Full	-	2.5	-	pF
Differential Gain (4.43MHz, Note 1)		+25°C	-	0.01	0.02	%
Differential Phase (4.43MHz, Note 1)		+25°C	-	0.01	0.02	Degrees
Off Isolation (1V_{P-P}, 100MHz, $V_{\overline{CS}}$ = 2.0V, R_L = 10Ω)		Full	-	70	-	dB
Crosstalk Rejection (1V_{P-P}, 30MHz)		Full	-	80	-	dB
Slew Rate (1.5V_{P-P}, +SR/-SR)	R_S = 50Ω, C_L = 11pF	+25°C	-	1280/1260	-	V/µs
	R_S = 24Ω, C_L = 19pF	+25°C	-	1190/1170	-	V/µs
	R_S = 15Ω, C_L = 34pF	+25°C	-	960/930	-	V/µs
	R_S = 11Ω, C_L = 49pF	+25°C	-	810/790	-	V/µs
Total Harmonic Distortion (10MHz, R_L = 1kΩ, Note 1)		Full	-	0.01	0.1	%
Disabled Output Resistance ($V_{\overline{CS}}$ = 2.0V)		Full	-	12	-	MΩ

NOTES:

1. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
2. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.
3. Units are 100% tested at +25°C, sample tested at 70°C, guaranteed, but not tested at 0°C.

AC Test Circuit



NOTE:

1. C_L = C_X + Test Fixture Capacitance.

PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Keep input and output traces as short as possible, because trace inductance and capacitance can easily become the performance limiting items.

8

VIDEO SWITCHES

Application Information

General

The HA4404 is a 4 x 1 crosspoint switch that is ideal for the matrix element of high performance switchers and routers. This crosspoint's low input capacitance and high input resistance provide excellent video terminations when used with an external 75Ω resistor. Nevertheless, if several HA4404 inputs are connected together, the use of an input buffer should be considered (see Figure 1). This crosspoint contains no feedback or gain setting resistors, so the output is a true high impedance load when the IC is disabled ($\overline{CS}$ = 1).

Ground Connections

All GND pins are connected to a common point on the die, so any one of them will suffice as the functional GND connection. For the best isolation and crosstalk rejection, however, all GND pins must connect to the GND plane.

Frequency Response

Most applications utilizing the HA4404 require a series output resistor, R_S, to tune the response for the specific load capacitance, C_L, driven. Bandwidth and slew rate degrade as C_L increases (as shown in the Electrical Specification table), so give careful consideration to component placement to minimize trace length. In big matrix configurations where C_L is large, better frequency response is obtained by cascading two levels of crosspoints in the case of multiplexed outputs (see Figure 2), or distributing the load between two drivers if C_L is due to bussing and subsequent stage input capacitance.

Control Signals

$\overline{CS}$ - This is a TTL/CMOS compatible, active low Chip Select input. When driven high, $\overline{CS}$ forces the output to a true high impedance state and reduces the power dissipation by a factor of 25. The $\overline{CS}$ input has no on-chip pull-down resistor, so it must be connected to a logic low (recommend GND) if the enable function isn't utilized.

A0, A1 - These are binary coded, TTL/CMOS compatible address inputs that select which one of the four inputs connect to the crosspoint output.

T0-T3 - The Tally outputs are open collector PNP transistors connected to V+. When $\overline{CS}$ = 0, the PNP transistor associated with the selected input is enabled and current is delivered to the load. When the crosspoint is disabled, or the channel is unselected, the Tally output(s) present a very high impedance to the external circuitry. Several Tally outputs may be wire OR'd together to generate complex control signals, as shown in the application circuits below. The Tally load may be terminated to GND or to V- as long as the continuous output current doesn't exceed 3mA (6mA at 50% duty cycle, etc.).

Switcher/Router Applications

Figure 1 illustrates one possible implementation of a wideband, low power, 4 x 4 switcher/router utilizing the HA4404 for the switch matrix. A 4 x 4 switcher/router allows any of the four outputs to be driven by any one of the four inputs (e.g. each of the four inputs may connect to a different output, or an input may connect to multiple outputs). This application utilizes the HA4600 (video buffer with output disable)

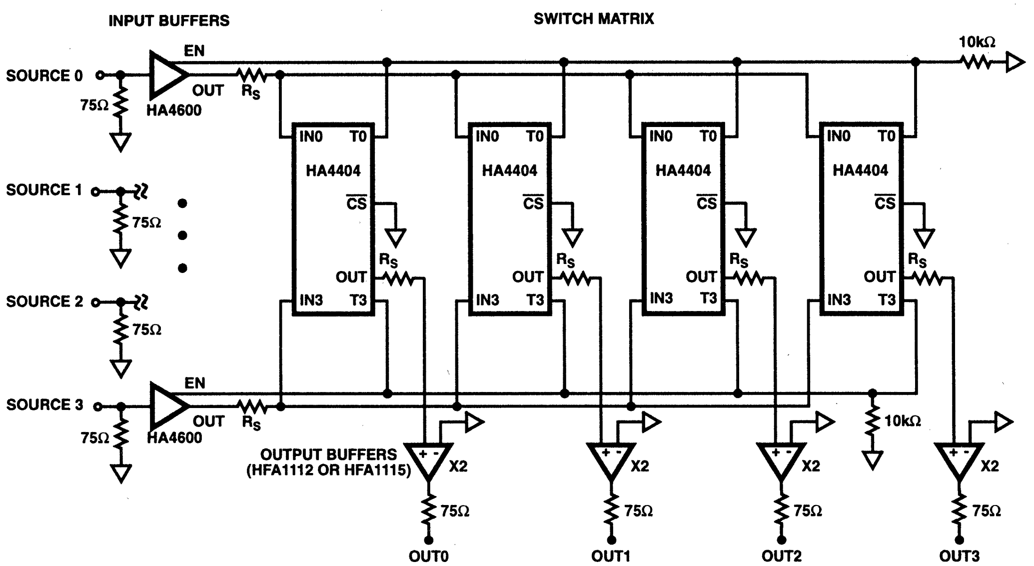


FIGURE 1. 4 X 4 SWITCHER/ROUTER APPLICATION

for the input buffer, the HA4404 as the switch matrix, and the HFA1112 (programmable gain buffer) as the gain of two output driver. Figure 2 details a 16 x 1 switcher (basically a 16:1 mux) which uses the HA4201 (1 x 1 crosspoint) and the HA4404 in a cascaded stage configuration to minimize capacitive loading at each output node, thus increasing system bandwidth.

Power Up Considerations

No signals should be applied to the analog or digital inputs before the power supplies are activated. Latch-up may occur if the inputs are driven at the time of power up. To prevent latch-up, the input currents during power up must not exceed the values listed in the Absolute Maximum Ratings.

Harris' Crosspoint Family

Harris offers a variety of 4 x 1 and 1 x 1 crosspoint switches. In addition to the HA4404, the 4 x 1 family includes the HA4314 and HA4344. The HA4314 is a basic 14 lead device without Tally outputs. The HA4344 is a 16 lead crosspoint with synchronized control lines (A0, A1, $\overline{CS}$). With synchronization, the control information for the next channel switch can be loaded into the crosspoint without affecting the current state. On a subsequent clock edge the stored control state effects the desired channel switch.

The 1 x 1 family is comprised of the HA4201 and HA4600. They are essentially similar devices, but the HA4201 includes a Tally output. The 1 x 1's are useful as high performance video input buffers, or in a switch matrix requiring very high off isolation.

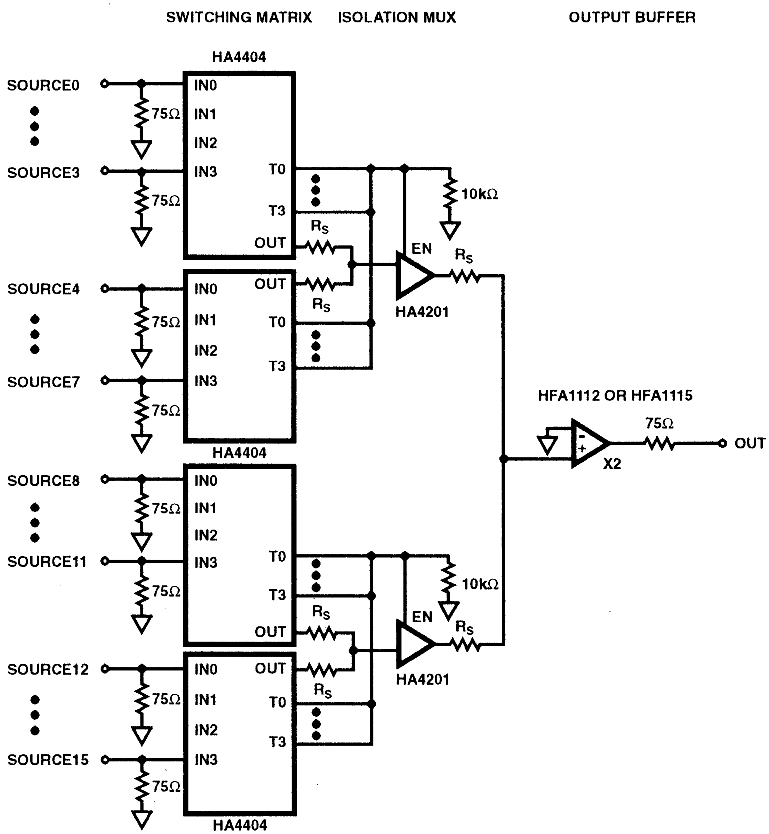


FIGURE 2. 16 X 1 SWITCHER APPLICATION

Die Characteristics

DIE DIMENSIONS:
65 x 118 x 19 ±1mil
1640μm x 3000μm x 483μm ±25.4μm

METALLIZATION:
Type: Metal 1: AlCu (1%)/TiW
Thickness: Metal 1: 6kÅ ±0.8kÅ
Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±1.1kÅ

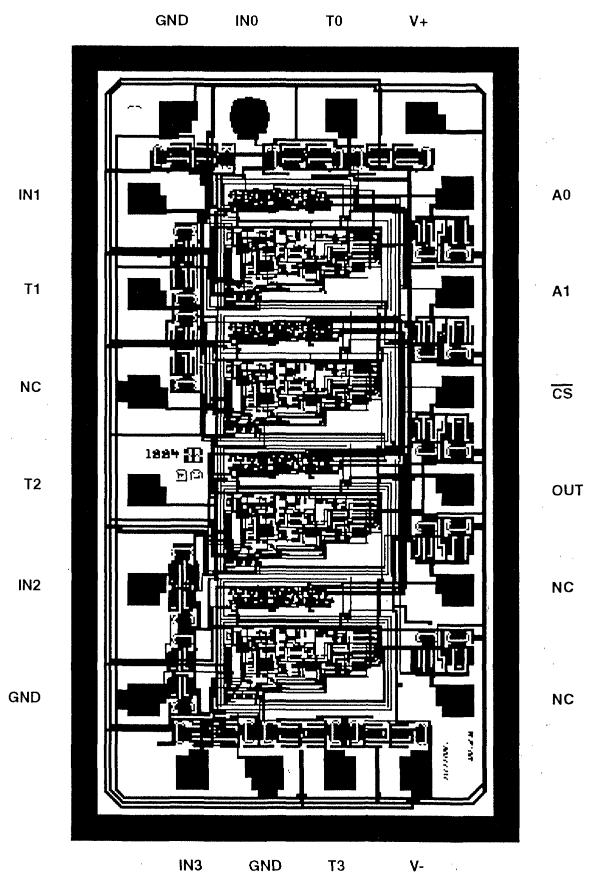
GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ±0.5kÅ

TRANSISTOR COUNT: 200

SUBSTRATE POTENTIAL (Powered Up): V-

Metallization Mask Layout

HA4404, HA4404A



Typical Performance Curves $V_{SUPPLY} = \pm 5V$, $T_A = +25^oC$, $R_L = 10k\Omega$, Unless Otherwise Specified

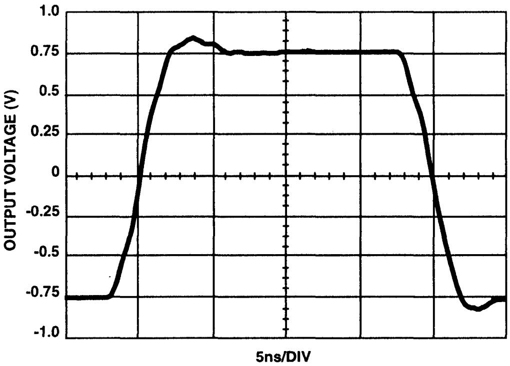


FIGURE 3. LARGE SIGNAL PULSE RESPONSE

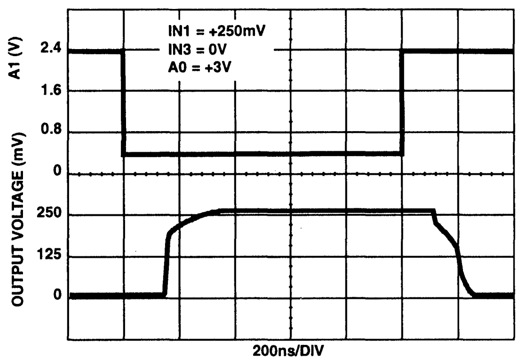


FIGURE 4. CHANNEL-TO-CHANNEL SWITCHING RESPONSE

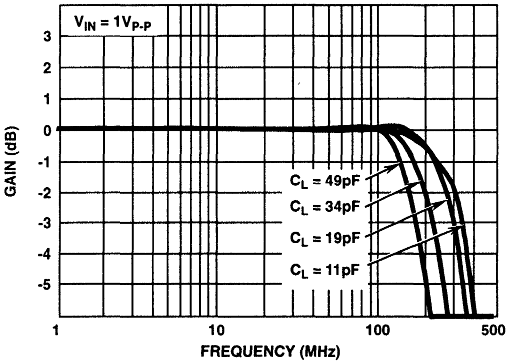


FIGURE 5. FREQUENCY RESPONSE

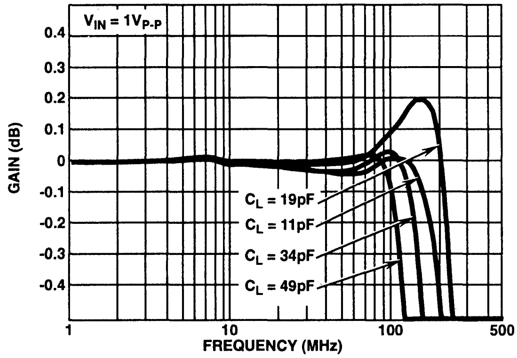


FIGURE 6. GAIN FLATNESS

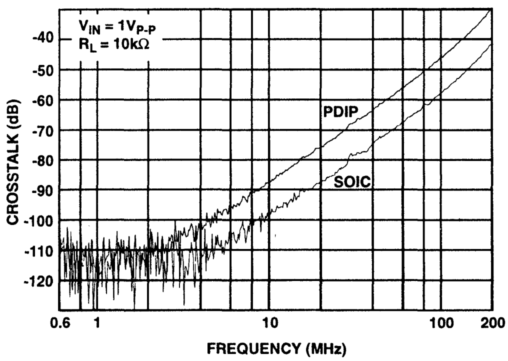


FIGURE 7. ALL HOSTILE CROSSTALK REJECTION

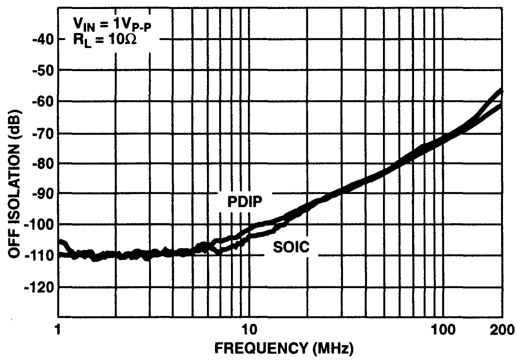


FIGURE 8. ALL HOSTILE OFF ISOLATION

8

VIDEO SWITCHES

Typical Performance Curves $V_{SUPPLY} = \pm5V$, $T_A = +25^oC$, $R_L = 10k\Omega$, Unless Otherwise Specified **(Continued)**

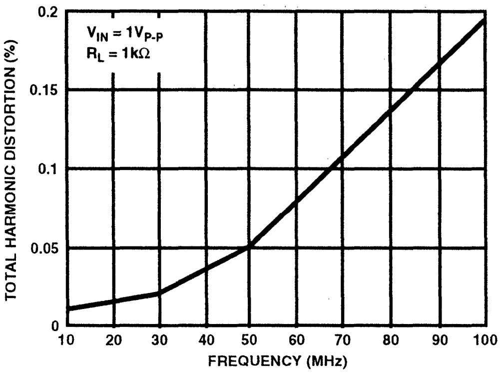


FIGURE 9. TOTAL HARMONIC DISTORTION vs FREQUENCY

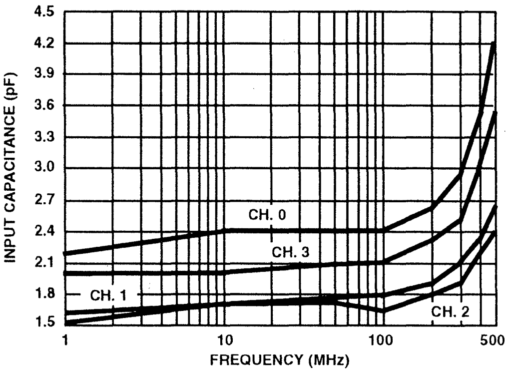


FIGURE 10. INPUT CAPACITANCE vs FREQUENCY

HARRIS SEMICONDUCTOR

HA4600

Wideband, Video Buffer with Output Disable

July 1995

Features

- Low Power Dissipation .105mW
- Symmetrical Slew Rates 1700V/μs
- 0.1dB Gain Flatness. 250MHz
- Off Isolation (100MHz). 85dB
- Differential Gain and Phase 0.01%/0.01Degrees
- High ESD Rating . . . . >2000V
- TTL Compatible Enable Input
- Improved Replacement for GB4600

Applications

- Professional Video Switching and Routing
- Video Multiplexers
- HDTV
- Computer Graphics
- RF Switching and Routing
- PCM Data Routing

Description

The HA4600 is a very wide bandwidth, unity gain buffer ideal for professional video switching, HDTV, computer monitor routing, and other high performance applications. The circuit features very low power dissipation (105mW Enabled, 1mW Disabled), excellent differential gain and phase, and very high off isolation. When disabled, the output is switched to a high impedance state, making the HA4600 ideal for routing matrix equipment and video multiplexers.

The HA4600 also features fast switching and symmetric slew rates. A typical application for the HA4600 is interfacing Harris' wide range of video crosspoint switches.

For applications requiring a tally output (enable indicator), please refer to the HA4201 data sheet.

Ordering Information

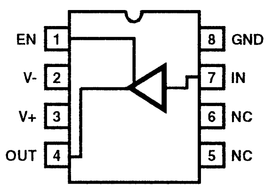
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA4600CP	0°C to +70°C	8 Lead Plastic DIP
HA4600CB	0°C to +70°C	8 Lead Plastic SOIC (N)

8

VIDEO SWITCHES

Pinout

HA4600
(PDIP, SOIC)
TOP VIEW



Truth Table

EN	OUT
0	High Z
1	Active

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3990.1

Absolute Maximum Ratings

Voltage Between V+ and V- 12V
Input Voltage. . . . . V_{SUPPLY}
Digital Input Current (Note 2) . . . . ±25mA
Analog Input Current (Note 2) . . . . ±5mA
Output Current 20mA
Junction Temperature (Die Only) . . . . +175°C
Junction Temperature (Plastic Package) . . . . . . +150°C
Lead Temperature (Soldering 10s). . . . . +300°C
(SOIC - Lead Tips Only)

Operating Conditions

Operating Temperature Range
HA4600C. . . . . $0^oC \le T_A \le +70^oC$
Storage Temperature . . . . $-65^oC \le T_A \le +150^oC$
Thermal Package Characteristics θ_{JA}
Plastic DIP Package . . . . 130°C/W
SOIC Package. . . . . 170°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications
V_{SUPPLY} = ±5V, R_L = 10kΩ, V_{EN} = 2.0V, Unless Otherwise Specified

PARAMETER		TEMPERATURE	HA4600C MIN	HA4600C TYP	HA4600C MAX	UNITS
DC SUPPLY CHARACTERISTICS						
Supply Voltage		Full	±4.5	±5.0	±5.5	V
Supply Current (V_{OUT} = 0V)	V_{EN} = 2.0V	+25°C, +70°C	-	10.5	13	mA
	V_{EN} = 2.0V	0°C	-	-	14.5	mA
	V_{EN} = 0.8V	+25°C, +70°C	-	100	115	μA
	V_{EN} = 0.8V	0°C	-	100	125	μA
ANALOG DC CHARACTERISTICS						
Output Voltage Swing without Clipping ($V_{OUT} = V_{IN} \pm V_{IO} \pm 20mV$)		+25°C, +70°C	±2.7	±2.8	-	V
		0°C	±2.4	±2.5	-	V
Output Current		Full	15	20	-	mA
Input Bias Current		Full	-	30	50	μA
Output Offset Voltage		+25°C	-10	-	10	mV
Output Offset Voltage Drift (Note 1)		Full	-	25	50	μV/°C
SWITCHING CHARACTERISTICS						
Turn-On Time		+25°C	-	160	-	ns
Turn-Off Time		+25°C	-	320	-	ns
DIGITAL DC CHARACTERISTICS						
Input Logic High Voltage		Full	2	-	-	V
Input Logic Low Voltage		Full	-	-	0.8	V
EN Input Current (0 to 4V)		Full	-2	-	2	μA
AC CHARACTERISTICS						
Insertion Loss (±1V)		Full	-	0.04	0.05	dB
-3dB Bandwidth	R_S = 82Ω, C_L = 10pF	+25°C	-	480	-	MHz
	R_S = 43Ω, C_L = 15pF	+25°C	-	380	-	MHz
	R_S = 36Ω, C_L = 21pF	+25°C	-	370	-	MHz
±0.1dB Flat Bandwidth	R_S = 82Ω, C_L = 10pF	+25°C	-	250	-	MHz
	R_S = 43Ω, C_L = 15pF	+25°C	-	175	-	MHz
	R_S = 36Ω, C_L = 21pF	+25°C	-	170	-	MHz
Input Resistance		Full	200	400	-	kΩ

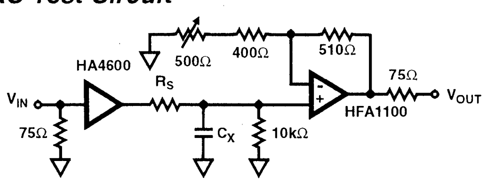
Electrical Specifications V_{SUPPLY} = ±5V, R_L = 10kΩ, V_{EN} = 2.0V, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMPERATURE	HA4600C MIN	HA4600C TYP	HA4600C MAX	UNITS
Input Capacitance		Full	-	1.0	-	pF
Enabled Output Resistance		Full	-	15	-	Ω
Disabled Output Capacitance (V_{EN} = 0.8V)		Full	-	2.0	-	pF
Differential Gain (4.43MHz, Note 1)		+25°C	-	0.01	0.02	%
Differential Phase (4.43MHz, Note 1)		+25°C	-	0.01	0.02	Degrees
Off Isolation (1V_{P-P}, 100MHz, V_{EN} = 0.8V, R_L = 10Ω)		Full	-	85	-	dB
Slew Rate (1.5V_{P-P}, +SR/-SR)	R_S = 82Ω, C_L = 10pF	+25°C	-	1750/1770	-	V/µs
	R_S = 43Ω, C_L = 15pF	+25°C	-	1460/1360	-	V/µs
	R_S = 36Ω, C_L = 21pF	+25°C	-	1410/1360	-	V/µs
Total Harmonic Distortion (Note 1)		Full	-	0.01	0.1	%
Disabled Output Resistance		Full	-	12	-	MΩ

NOTES:

1. This parameter is not tested. The limits are guaranteed based on lab characterization, and reflect lot-to-lot variation.
2. If an input signal is applied before the supplies are powered up, the input current must be limited to these maximum values.

AC Test Circuit



NOTE:

1. C_L = C_X + Test Fixture Capacitance.

PC Board Layout

The frequency response of this circuit depends greatly on the care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10µF) tantalum in parallel with a small value (0.1µF) chip capacitor works well in most cases.

Keep input and output traces as short as possible, because trace inductance and capacitance can easily become the performance limiting items.

Application Information

General

The HA4600 is a unity gain buffer that is optimized for high performance video applications. The output disable function makes it ideal for the matrix element in small, high input-to-output isolation switchers and routers. This buffer contains no feedback or gain setting resistors, so the output is a true high impedance load when the IC is disabled (EN = 0). The HA4600 also excels as an input buffer for routers with a large number of outputs (i.e. each input must connect to a large number of outputs) and delivers performance superior to most video amplifiers at a fraction of the cost. As an input buffer, the HA4600's low input capacitance and high input resistance provide excellent video terminations when used with an external 75Ω resistor.

Frequency Response

Most applications utilizing the HA4600 require a series output resistor, R_S, to tune the response for the specific load capacitance, C_L, driven. Bandwidth and slew rate degrade as C_L increases (as shown in the Electrical Specification table), so give careful consideration to component placement to minimize trace length. As an example, -3dB bandwidth decreases to 160MHz for C_L = 100pF, R_S = 0Ω. In big matrix configurations where C_L is large, better frequency response is obtained by cascading two levels of crosspoints in the case of multiplexed outputs (see Figure 2), or distributing the load between two drivers if C_L is due to bussing and subsequent stage input capacitance.

Control Signals

EN - The ENABLE input is a TTL/CMOS compatible, active high input. When driven low this input forces the output to a true high impedance state and reduces the power dissipation by two orders of magnitude. The EN input has no on-chip pull-up resistor, so it must be connected to a logic high (recommend V+) if the enable function isn't utilized.

Switcher/Router Applications

Figure 1 illustrates one possible implementation of a wideband, low power, 4 x 4 switcher/router. A 4 x 4 switcher/router allows any of the four outputs to be driven by any one of the four inputs (e.g. each of the four inputs may connect to a different output, or an input may connect to multiple outputs). This application utilizes the HA4600 for the input buffer, the HA4404 (4 x 1 crosspoint switch) as the switch matrix, and the HFA1112 (programmable gain buffer) as the gain of two output driver. Figure 2 details a 16 x 1 switcher (basically a 16:1 mux) which uses the HA4600 in a cascaded stage configuration to minimize capacitive loading at each output node, thus increasing system bandwidth.

Power Up Considerations

No signals should be applied to the analog or digital inputs before the power supplies are activated. Latch-up may occur if the inputs are driven at the time of power up. To prevent latch-up, the input currents during power up must not exceed the values listed in the Absolute Maximum Ratings.

Harris' Crosspoint Family

Harris offers a variety of 1 x 1 and 4 x 1 crosspoint switches. In addition to the HA4600, the 1 x 1 family includes the HA4201 which is an essentially similar device that includes a Tally output (enable indicator). The 4 x 1 family is comprised of the HA4314, HA4404, and HA4344. The HA4314 is a 14 lead basic 4 x 1 crosspoint. The HA4404 is a 16 lead device with Tally outputs to indicate the selected channel. The HA4344 is a 16 lead crosspoint with synchronized control lines (A0, A1, $\overline{CS}$). With synchronization, the control information for the next channel switch can be loaded into the crosspoint without affecting the current state. On a subsequent clock edge the stored control state effects the desired channel switch.

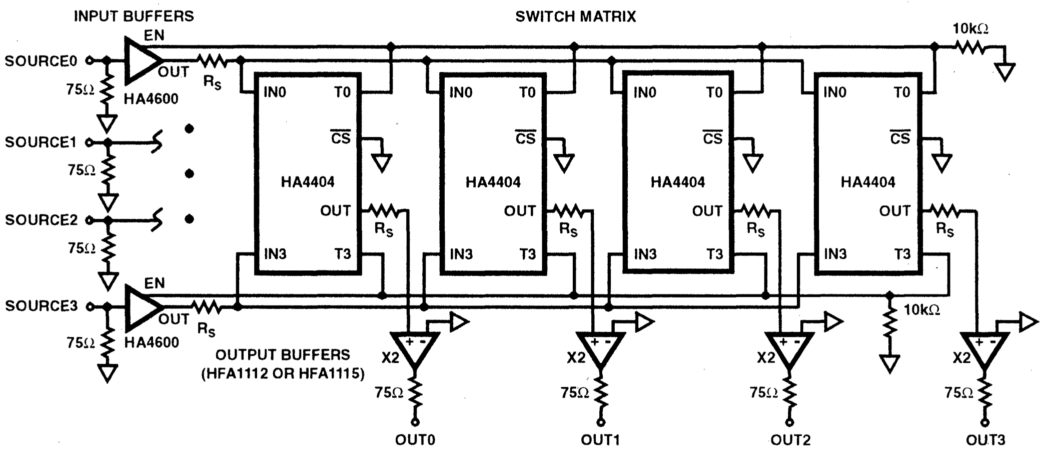


FIGURE 1. 4 x 4 SWITCHER/ROUTER APPLICATION

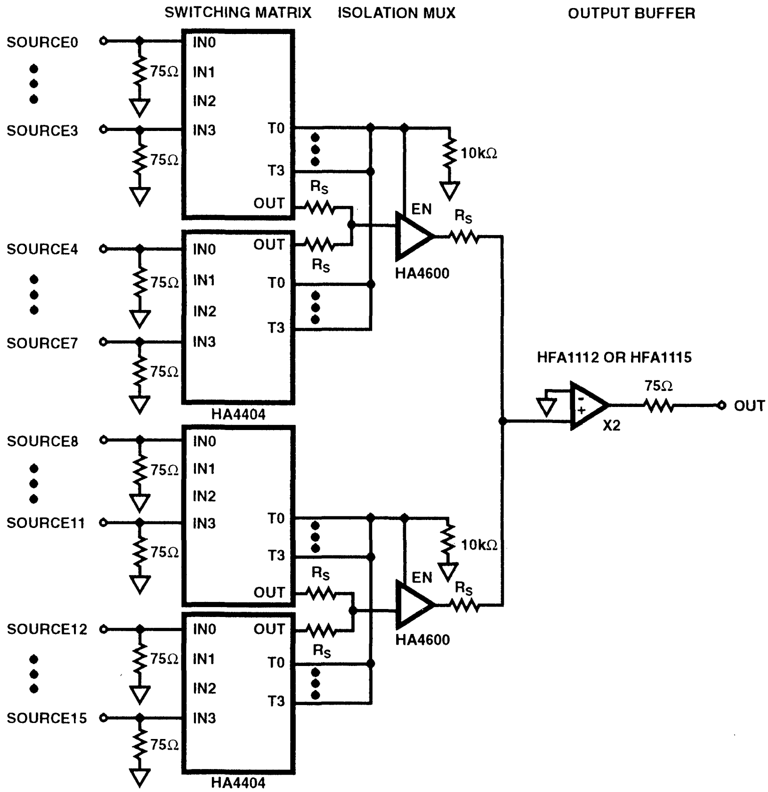


FIGURE 2. 16 x 1 SWITCHER APPLICATION

Die Characteristics

DIE DIMENSIONS:
54 x 39 x 19 ± 1mil
1380μm x 1000μm x 483μm ± 25.4μm

METALLIZATION:
Type: Metal 1: AlCu (1%)/TiW   Type: Metal 2: AlCu (1%)
Thickness: Metal 1: 6kÅ ± 0.8kÅ   Thickness: Metal 2: 16kÅ ± 1.1kÅ

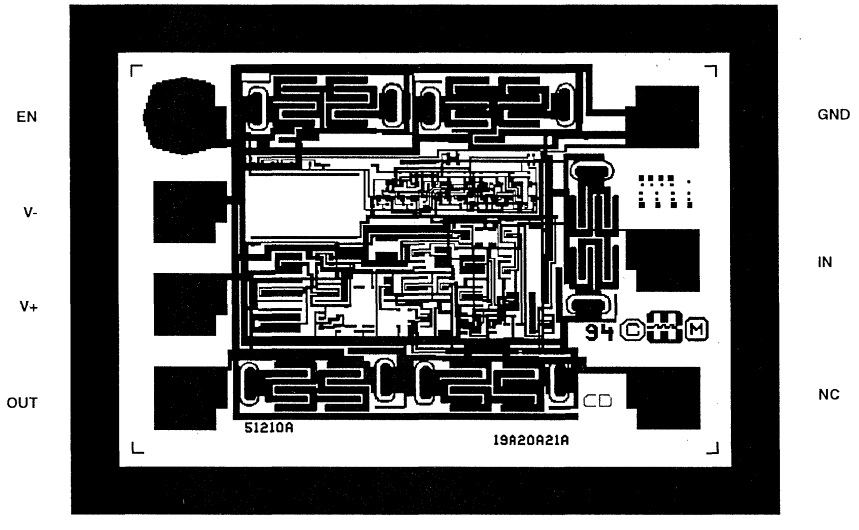
GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kA

TRANSISTOR COUNT: 53

SUBSTRATE POTENTIAL (Powered Up): V-

Metallization Mask Layout

HA4600



Typical Performance Curves V_{SUPPLY} = ±5V, T_A = +25°C, R_L = 10kΩ, Unless Otherwise Specified

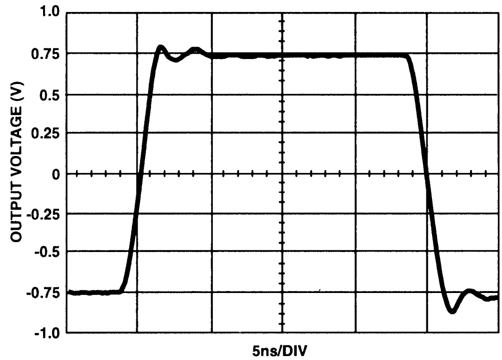


FIGURE 3. LARGE SIGNAL PULSE RESPONSE

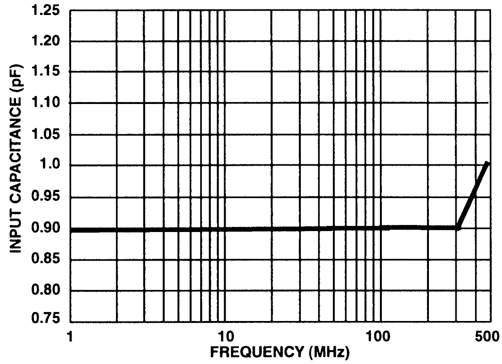


FIGURE 4. INPUT CAPACITANCE vs FREQUENCY

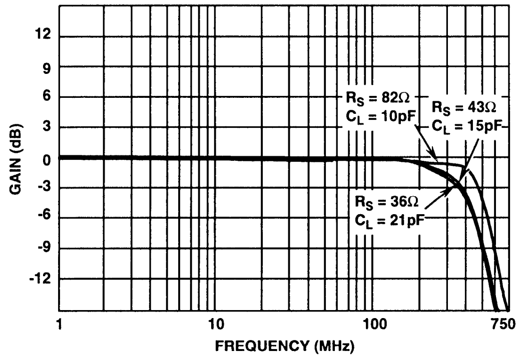


FIGURE 5. FREQUENCY REPONSE

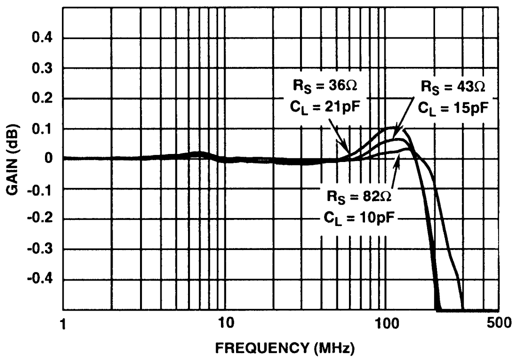


FIGURE 6. GAIN FLATNESS

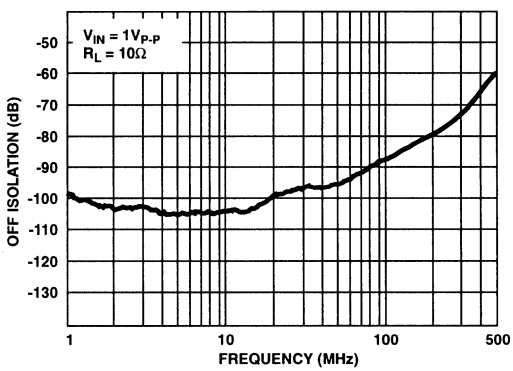


FIGURE 7. OFF ISOLATION

SIGNAL PROCESSING NEW RELEASES 9

SPECIAL ANALOG CIRCUITS

HARRIS SEMICONDUCTOR HA7210, HA7211

July 1995

Low Power Crystal Oscillator

Features

- Single Supply Operation at 32kHz . . . . 2.0V to 7.0V
- Operating Frequency Range. . . . . 10kHz to 10MHz
- Supply Current at 32kHz . . . . $5\mu A$
- Supply Current at 1MHz . . . . $130\mu A$
- Drives 2 CMOS Loads
- Only Requires an External Crystal for Operation
- Two Pinouts Available

Applications

- Battery Powered Circuits
- Remote Metering
- Embedded Microprocessors
- Palm Top/Notebook PC

Description

The HA7210 and HA7211 are very low power crystal-controlled oscillators that can be externally programmed to operate between 10kHz and 10MHz. For normal operation it requires only the addition of a crystal. The part exhibits very high stability over a wide operating voltage and temperature range.

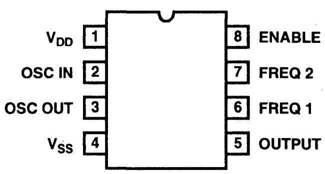
The HA7210 and HA7211 also feature a disable mode that switches the output to a high impedance state. This feature is useful for minimizing power dissipation during standby and when multiple oscillator circuits are employed.

Ordering Information

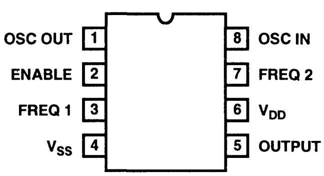
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA7210IP	-40°C to +85°C	8 Lead Plastic DIP
HA7210IB	-40°C to +85°C	8 Lead Plastic SOIC (N)
HA7210Y	-40°C to +85°C	DIE
HA7211IB	-40°C to +85°C	8 Lead Plastic SOIC (N)

Pinouts

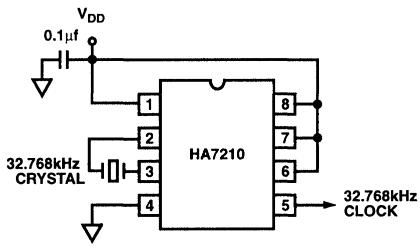
HA7210
TOP VIEW



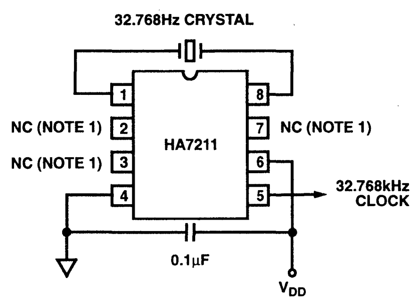
HA7211
TOP VIEW



Typical Application Circuits



32.768Hz MICROPOWER CLOCK OSCILLATOR

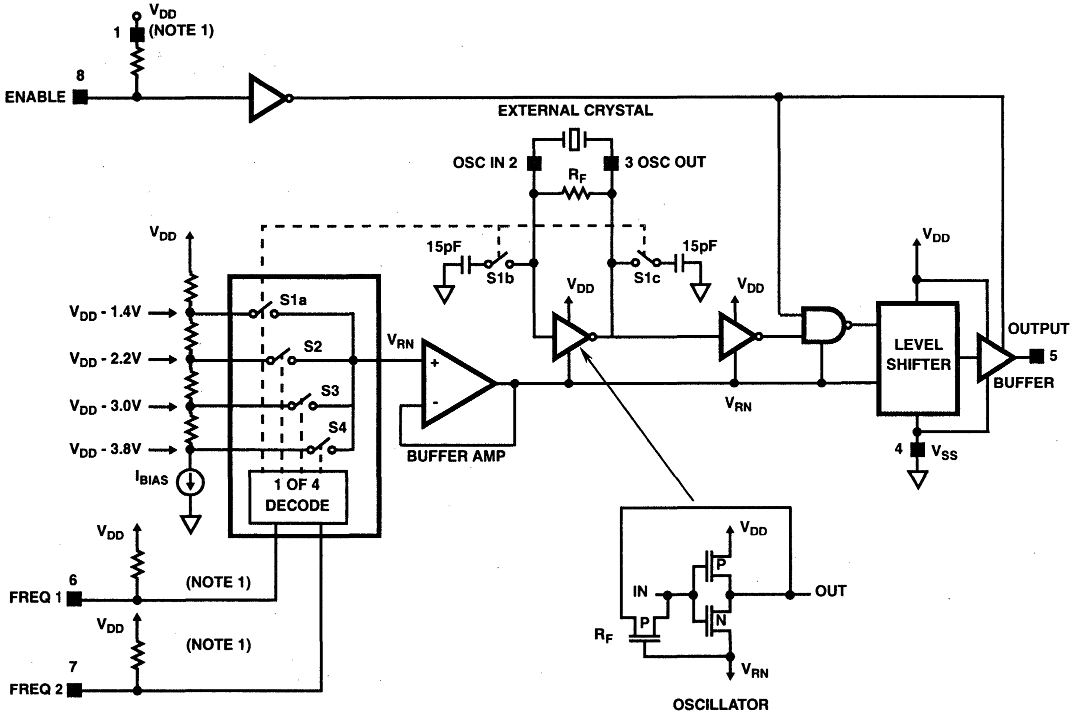


NOTE:

1. Internal pull-up resistors provided for both HA7210 and HA7211.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Simplified Block Diagram (HA7210)



FREQUENCY SELECTION TRUTH TABLE

ENABLE	FREQ 1	FREQ 2	SWITCH	OUTPUT RANGE
1	1	1	S1a, b, c	10kHz - 100kHz
1	1	0	S2	100kHz - 1MHz
1	0	1	S3	1MHz - 5MHz
1	0	0	S4	5MHz - 10MHz+
0	X	X	X	High Impedance

NOTE:

1. Logic input pull-up resistors are constant current source of 0.4μA.

Absolute Maximum Ratings

Supply Voltage 10.0V
Voltage (any pin). . . . . V_{SS}-0.3V to V_{DD}+0.3V
Junction Temperature (Plastic Package) . . . . . . +150°C
ESD Rating (Note 2). . . . . >4000V
Lead Temperature (Soldering 10s). . . . . +300°C
(SOIC - Lead Tip Only)

Operating Conditions

Operating Temperature (Note 3). . . . . -40°C to +85°C
Storage Temperature Range. . . . . -65°C to +150°C
Thermal Package Characteristics θ_{JA}
PDIP . . . . 125°C/W
SOIC . . . . 170°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{SS} = GND, T_A = +25°C, Unless Otherwise Specified

PARAMETER	V_{DD} = 5V MIN	V_{DD} = 5V TYP	V_{DD} = 5V MAX	V_{DD} = 3V MIN	V_{DD} = 3V TYP	V_{DD} = 3V MAX	UNITS
V_{DD} Supply Range (f_{OSC} = 32kHz)	2	5	7	-	-	-	V
I_{DD} Supply Current							
f_{OSC} = 32kHz, EN = 0 Standby	-	5.0	9.0	-	-	-	µA
f_{OSC} = 32kHz, C_L = 10pF (Note 1), EN = 1, Freq1 = 1, Freq2 = 1	-	5.2	10.2	-	3.6	6.1	µA
f_{OSC} = 32kHz, C_L = 40pF, EN = 1, Freq1 = 1, Freq2 = 1	-	10	15	-	6.5	9	µA
f_{OSC} = 1MHz, C_L = 10pF (Note 1), EN = 1, Freq1 = 0, Freq2 = 1	-	130	200	-	90	180	µA
f_{OSC} = 1MHz, C_L = 40pF, EN = 1, Freq1 = 0, Freq2 = 1	-	270	350	-	180	270	µA
V_{OH} Output High Voltage (I_{OUT} = -1mA)	4.0	4.9	-	-	2.8	-	V
V_{OL} Output Low Voltage (I_{OUT} = 1mA)	-	0.07	0.4	-	0.1	-	V
I_{OH} Output High Current ($V_{OUT} \geq$ 4V)	-	-10	-5	-	-	-	mA
I_{OL} Output Low Current ($V_{OUT} \leq$ 0.4V)	5.0	10.0	-	-	-	-	mA
Three-State Leakage Current							
(V_{OUT} = 0V, 5V, T_A = 25°C, -40°C)	-	0.1	-	-	-	-	nA
(V_{OUT} = 0V, 5V, T_A = 85°C)	-	10	-	-	-	-	nA
I_{IN} Enable, Freq1, Freq2 Input Current (V_{IN} = V_{SS} to V_{DD})	-	0.4	1.0	-	-	-	µA
V_{IH} Input High Voltage Enable, Freq1, Freq2	2.0	-	-	-	-	-	V
V_{IL} Input Low Voltage Enable, Freq1, Freq2	-	-	0.8	-	-	-	V
Enable Time (C_L = 18pF, R_L = 1kΩ)	-	800	-	-	-	-	ns
Disable Time (C_L = 18pF, R_L = 1kΩ)	-	90	-	-	-	-	ns
t_R Output Rise Time (10% - 90%, f_{OSC} = 32kHz, C_L = 40pF)	-	12	25	-	12	-	ns
t_F Output Fall Time (10% - 90%, f_{OSC} = 32kHz, C_L = 40pF)	-	12	25	-	14	-	ns
Duty Cycle (C_L = 40pF) f_{OSC} = 1MHz, Packaged Part Only (Note 4)	40	54	60	-	-	-	%
Duty Cycle (C_L = 40pF) f_{OSC} = 32kHz, (See Typical Curves)	-	41	-	-	44	-	%
Frequency Stability vs. Supply Voltage (f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF)	-	1	-	-	-	-	ppm/V
Frequency Stability vs. Temperature (f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF)	-	0.1	-	-	-	-	ppm/°C
Frequency Stability vs. Load (f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF)	-	0.01	-	-	-	-	ppm/pF

NOTES:

1. Calculated using the equation I_{DD} = I_{DD} (No Load) + (V_{DD}) (f_{OSC})(C_L)
2. Human body model.
3. This product is production tested at +25°C only.
4. Duty cycle will vary with supply voltage, oscillation frequency, and parasitic capacitance on the crystal pins.

Test Circuits

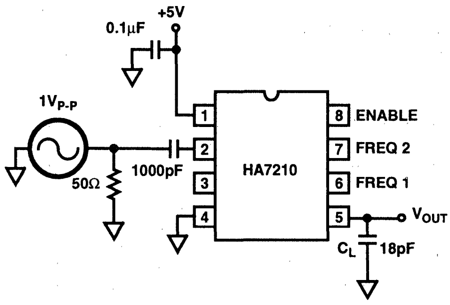


FIGURE 1.

In production the HA7210 is tested with a 32kHz and a 1MHz crystal. However for characterization purposes data was taken using a sinewave generator as the frequency determining element, as shown in Figure 1. The $1V_{P-P}$ input is a smaller amplitude than what a typical crystal would generate so the transitions are slower. In general the Generator data will show a "worst case" number for I_{DD}, duty cycle, and rise/fall time. The Generator test method is useful for testing a variety of frequencies quickly and provides curves which can be used for understanding performance trends. Data for the HA7210 using crystals has also been taken. This data has been overlaid onto the generator data to provide a reference for comparison.

Theory of Operation

The HA7210 and HA7211 are Pierce Oscillators optimized for low power consumption, requiring no external components except for a bypass capacitor and a Parallel Mode Crystal. The Simplified Block Diagram shows the Crystal attached to pins 2 and 3, (HA7210) the Oscillator input and output. The crystal drive circuitry is detailed showing the simple CMOS inverter stage and the P-channel device being used as biasing resistor R_F. The inverter will operate mostly in its linear region increasing the amplitude of the oscillation until limited by its transconductance and voltage rails, V_{DD} and V_{RN}. The inverter is self biasing using R_F to center the oscillating waveform at the input threshold. Do not interfere with this bias function with external loads or excessive leakage on pin 2 for HA7210, pin 8 for HA7211. Nominal value for R_F is 17MΩ in the lowest frequency range to 7MΩ in the highest frequency range.

The HA7210 and HA7211 optimizes its power for 4 frequency ranges selected by digital inputs Freq1 and Freq2 as shown in the Block Diagram. Internal pull up resistors (constant current 0.4µA) on Enable, Freq1 and Freq2 allow the user simply to leave one or all digital inputs not connected for a corresponding "1" state. All digital inputs may be left open for 10kHz to 100kHz operation.

A current source develops 4 selectable reference voltages through series resistors. The selected voltage, V_{RN}, is buffered and used as the negative supply rail for the oscillator section of the circuit. The use of a current source in the reference string allows for wide supply variation with minimal effect on performance. The reduced operating voltage of the oscillator section reduces power consumption and limits transconductance and bandwidth to the frequency range selected. For frequencies at the edge of a range, the higher range may provide better performance.

The OSC OUT waveform on pin 3 for HA7210 (pin 1 for HA7211) is squared up through a series of inverters to the output drive stage. The Enable function is implemented with a NAND gate in the inverter string, gating the signal to the level shifter and output stage. Also during Disable the output is set to a high impedance state useful for minimizing power during standby and when multiple oscillators are OR'd to a single node.

Design Considerations

The low power CMOS transistors are designed to consume power mostly during transitions. Keeping these transitions short requires a good decoupling capacitor as close as possible to the supply pins 1 and 4 for HA7210, pins 4 and 6 for HA7211. A ceramic 0.1µF is recommended. Additional supply decoupling on the circuit board with 1µF to 10µF will further reduce overshoot, ringing and power consumption. The HA7210, when compared to a crystal and inverter alone, will speed clock transition times, reducing power consumption of all CMOS circuitry run from that clock.

Power consumption may be further reduced by minimizing the capacitance on moving nodes. The majority of the power will be used in the output stage driving the load. Minimizing the load and parasitic capacitance on the output, pin 5, will play the major role in minimizing supply current. A secondary source of wasted supply current is parasitic or crystal load capacitance on pins 2 and 3 for HA7210, pins 1 and 8 for HA7211. The HA7210 is designed to work with most available crystals in its frequency range with no external components required. Two 15pF capacitors are internally switched onto crystal pins 2 and 3 on the HA7210 to compensate the oscillator in the 10kHz to 100kHz frequency range.

The supply current of the HA7210 and HA7211 may be approximately calculated from the equation:

$$I_{DD} = I_{DD}(\text{Disabled}) + V_{DD} \times F_{OSC} \times C_L$$

where: I_{DD} = Total supply current
V_{DD} = Total voltage from V_{DD} (pin1) to V_{SS} (pin4)
F_{OSC} = Frequency of Oscillation
C_L = Output (pin5) load capacitance

Example #1:

V_{DD} = 5V, F_{OSC} = 100kHz, C_L = 30pF
I_{DD}(Disabled) = 4.5µA (Figure 10)
I_{DD} = 4.5µA + (5V)(100kHz)(30pF) = 19.5µA
Measured I_{DD} = 20.3µA

Example #2:

V_{DD} = 5V, F_{OSC} = 5MHz, C_L = 30pF
I_{DD}(Disabled) = 75µA (Figure 9)
I_{DD} = 75µA + (5V)(5MHz)(30pF) = 825µA
Measured I_{DD} = 809µA

Crystal Selection

For general purpose applications, a Parallel Mode Crystal is a good choice for use with the HA7210 or HA7211. However for applications where a precision frequency is required, the designer needs to consider other factors.

Crystals are available in two types or modes of oscillation, Series and Parallel. Series Mode crystals are manufactured to operate at a specified frequency with zero load capacitance and appear as a near resistive impedance when oscillating. Parallel Mode crystals are manufactured to operate with a specific capacitive load in series, causing the crystal to operate at a more inductive impedance to cancel the load capacitor. Loading a crystal with a different capacitance will "pull" the frequency off its value.

The HA7210 and HA7211 has 4 operating frequency ranges. The higher three ranges do not add any loading capacitance to the oscillator circuit. The lowest range, 10kHz to 100kHz, automatically switches in two 15pF capacitors onto OSC IN and OSC OUT to eliminate potential start-up problems. These capacitors create an effective crystal loading capacitor equal to the series combination of these two capacitors. For the HA7210 and HA7211, in the lowest range, the effective loading capacitance is 7.5pF. Therefore the choice for a crystal, in this range, should be a Parallel Mode crystal that requires a 7.5pF load.

In the higher 3 frequency ranges, the capacitance on OSC IN and OSC OUT will be determined by package and layout parasitics, typically 4 to 5pF. Ideally the choice for crystal should be a Parallel Mode set for 2.5pF load. A crystal manufactured for a different load will be "pulled" from its nominal frequency (see Crystal Pullability).

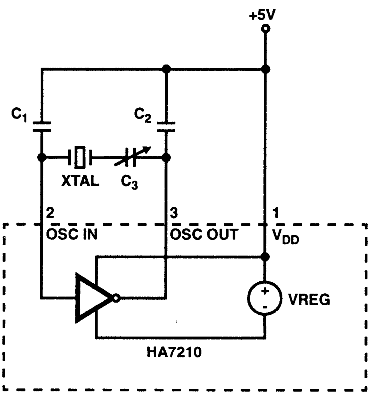


FIGURE 2.

Frequency Fine Tuning

Two Methods will be discussed for fine adjustment of the crystal frequency. The first and preferred method (Figure 2), provides better frequency accuracy and oscillator stability than method two (Figure 3). Method one also eliminates start-up problems sometimes encountered with 32kHz tuning fork crystals.

For best oscillator performance, two conditions must be met: the capacitive load must be matched to both the inverter and crystal to provide ideal conditions for oscillation, and the frequency of the oscillator must be adjustable to the desired frequency. In Method two these two goals can be at odds with each other; either the oscillator is trimmed to frequency by de-tuning the load circuit, or stability is increased at the expense of absolute frequency accuracy.

Method one allows these two conditions to be met independently. The two fixed capacitors, C_1 and C_2, provide the optimum load to the oscillator and crystal. C_3 adjusts the frequency at which the circuit oscillates without appreciably changing the load (and thus the stability) of the system. Once a value for C_3 has been determined for the particular type of crystal being used, it could be replaced with a fixed capacitor. For the most precise control over oscillator frequency, C_3 should remain adjustable.

This three capacitor tuning method will be more accurate and stable than method two and is recommended for 32kHz tuning fork crystals; without it they may leap into an overtone mode when power is initially applied.

Method two has been used for many years and may be preferred in applications where cost or space is critical. Note that in both cases the crystal loading capacitors are connected between the oscillator and V_{DD}; do not use V_{SS} as an AC ground. The Simplified Block Diagram shows that the oscillating inverter does not directly connect to V_{SS} but is referenced to V_{DD} and V_{RN}. Therefore V_{DD} is the best AC ground available.

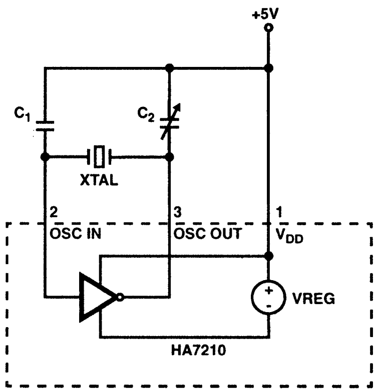


FIGURE 3.

Typical values of the capacitors in Figure 2 are shown below. Some trial and error may be required before the best combination is determined. The values listed are total capacitance including parasitic or other sources. Remember that in the 10kHz to 100kHz frequency range setting the HA7210 switches in two internal 15pF capacitors.

CRYSTAL FREQUENCY	LOAD CAPS C1, C2	TRIMMER CAP C3
32kHz	33pF	5-50pF
1MHz	33pF	5-50pF
2MHz	25pF	5-50pF
4MHz	22pF	5-100pF

Crystal Pullability

Figure 4 shows the basic equivalent circuit for a crystal and its loading circuit.

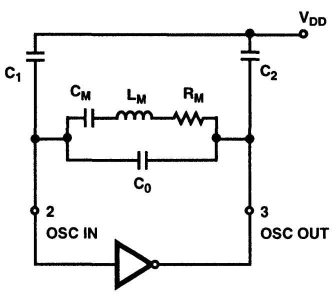


FIGURE 4.

Where: C_M = Motional Capacitance
L_M = Motional Inductance
R_M = Motional Resistance
C_0 = Shunt Capacitance

$$C_{CL} = \frac{1}{\left(\frac{1}{C_1} + \frac{1}{C_2}\right)} = \text{Equivalent Crystal Load}$$

If loading capacitance is connected to a Series Mode Crystal, the new Parallel Mode frequency of resonance may be calculated with the following equation:

$$F_P = F_S\left[1 + \frac{C_M}{2\left(C_0 + C_{CL}\right)}\right]$$

Where: F_P = Parallel Mode Resonant Frequency
F_S = Series Mode Resonant Frequency

In a similar way, the Series Mode resonant frequency may be calculated from a Parallel Mode crystal and then you may calculate how much the frequency will "pull" with a new load.

Layout Considerations

Due to the extremely low current (and therefore high impedance) the circuit board layout of the HA7210 or HA7211 must be given special attention. Stray capacitance should be minimized. Keep the oscillator traces on a single layer of the PCB. Avoid putting a ground plane above or below this layer. The traces between the crystal, the capacitors, and the OSC pins should be as short as possible. Completely surround the oscillator components with a thick trace of V_{DD} to minimize coupling with any digital signals. The final assembly must be free from contaminants such as solder flux, moisture, or any other potential source of leakage. A good solder mask will help keep the traces free of moisture and contamination over time.

Further Reading

Al Little "HA7210 Low Power Oscillator: Micropower Clock Oscillator and Op Amps Provide System Shutdown for Battery Circuits". Harris Semiconductor Application Note AN9317.

Robert Rood "Improving Start-Up Time at 32KHz for the HA7210 Low Power Crystal Oscillator". Harris Semiconductor Application Note AN9334.

S. S. Eaton "Timekeeping Advances Through COS/MOS Technology". Harris Semiconductor Application Note ICAN-6086.

E. A. Vittoz et. al. "High-Performance Crystal Oscillator circuits: Theory and Application". IEEE Journal of Solid-State Circuits, Vol. 23, No3, June 1988, pp774-783.

M. A. Unkrich et. al. "Conditions for Start-Up in Crystal Oscillators". IEEE Journal of Solid-State Circuits, Vol. 17, No1, Feb. 1982, pp87-90.

Marvin E. Frerking "Crystal Oscillator Design and Temperature Compensation". New York: Van Nostrand-Reinhold, 1978. Pierce Oscillators Discussed pp56-75.

Die Characteristics

DIE DIMENSIONS:
68 x 64 x 14 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 10kÅ ± 1kÅ

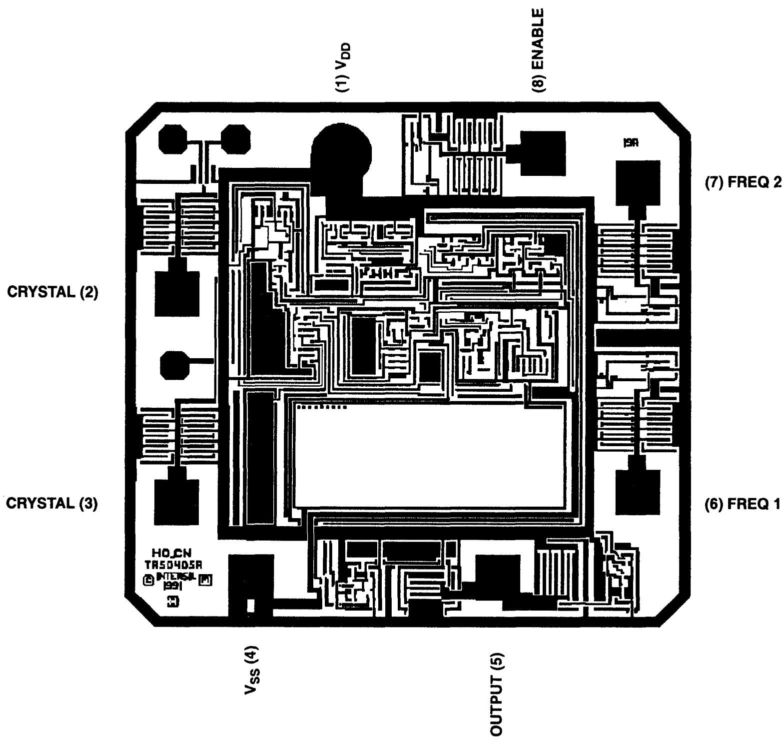
GLASSIVATION:
Type: Nitride (Si_3N_4) Over Silox (SiO_2, 3% Phos)
Silox Thickness: 7kÅ ± 1kÅ
Nitride Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Silver Epoxy - Plastic DIP and SOIC

SUBSTRATE POTENTIAL: V_{SS}

Metallization Mask Layout

HA7210



Typical Performance Curves

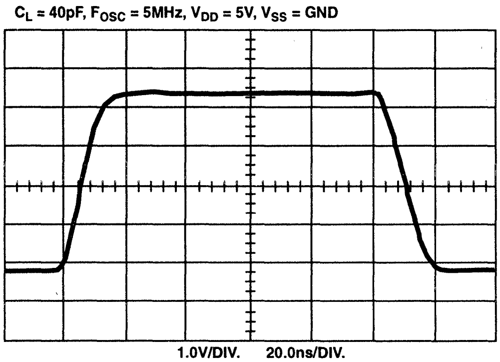


FIGURE 5. OUTPUT WAVEFORM (C_L = 40pF)

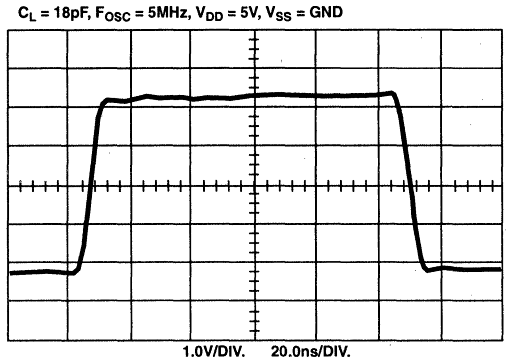


FIGURE 6. OUTPUT WAVEFORM (C_L = 18pF)

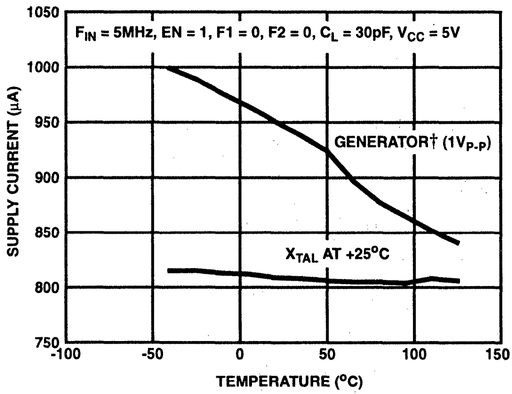


FIGURE 7. SUPPLY CURRENT vs TEMPERATURE

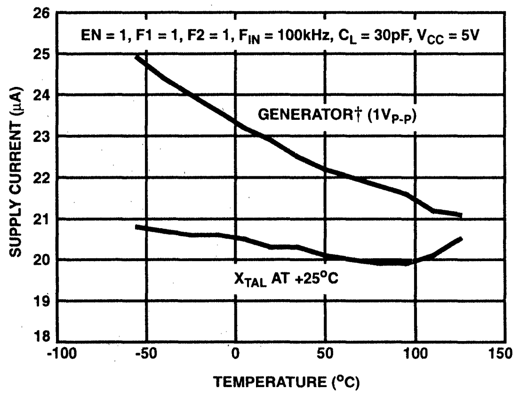


FIGURE 8. SUPPLY CURRENT vs TEMPERATURE

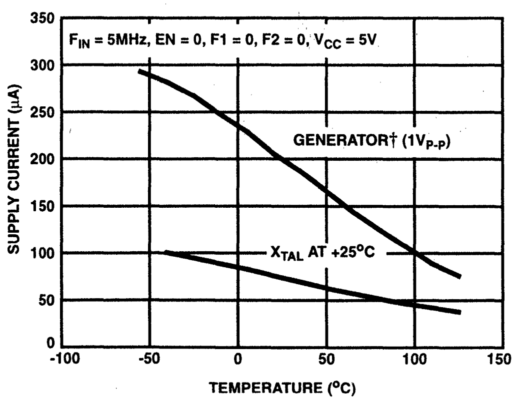


FIGURE 9. DISABLE SUPPLY CURRENT vs TEMPERATURE

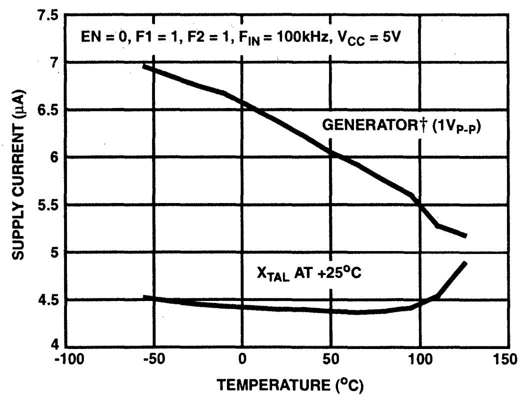


FIGURE 10. DISABLE SUPPLY CURRENT vs TEMPERATURE

†Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

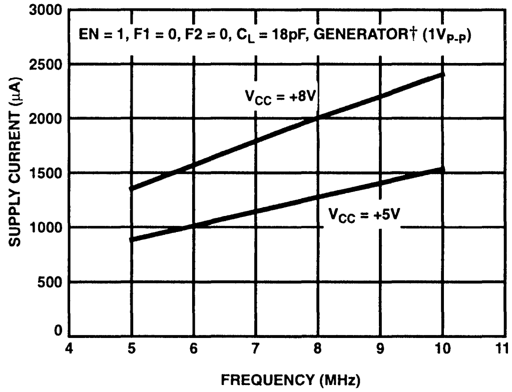


FIGURE 11. SUPPLY CURRENT vs FREQUENCY

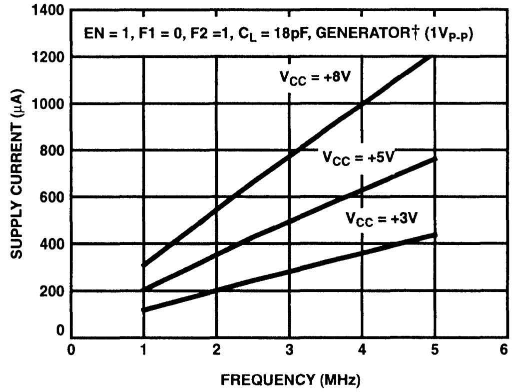


FIGURE 12. SUPPLY CURRENT vs FREQUENCY

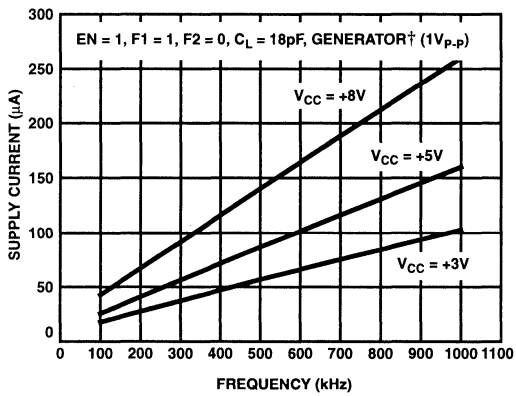


FIGURE 13. SUPPLY CURRENT vs FREQUENCY

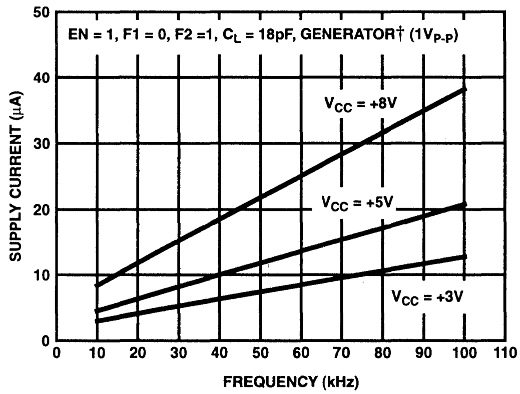


FIGURE 14. SUPPLY CURRENT vs FREQUENCY

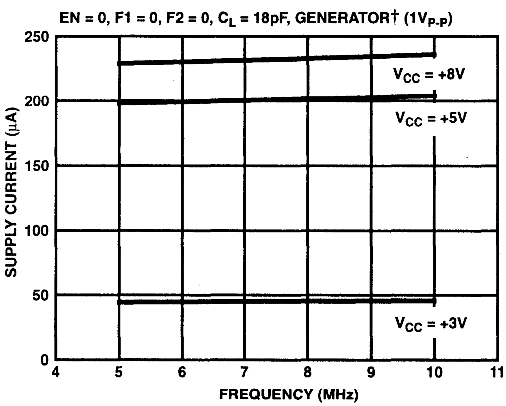


FIGURE 15. DISABLED SUPPLY CURRENT vs FREQUENCY

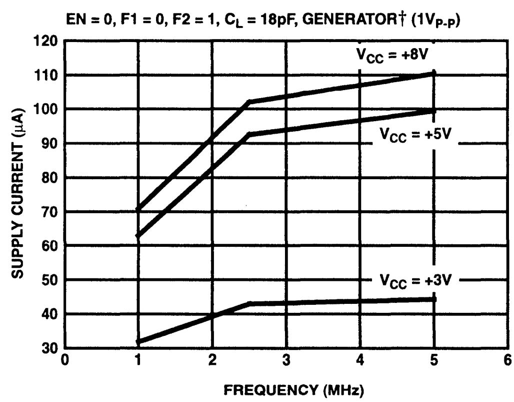


FIGURE 16. DISABLE SUPPLY CURRENT vs FREQUENCY

†Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

EN = 0, F1 = 1, F2 = 0, C_L = 18pF, GENERATOR† ($1V_{P-P}$)

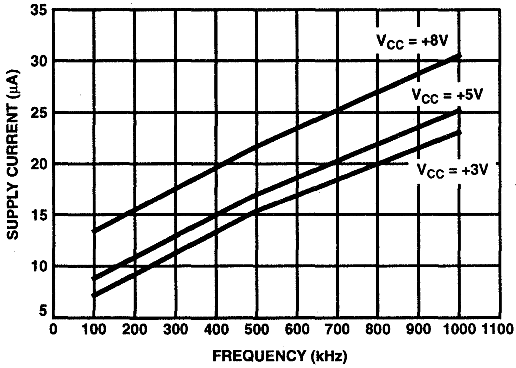


FIGURE 17. DISABLE SUPPLY CURRENT vs FREQUENCY

EN = 0, F1 = 1, F2 = 1, C_L = 18pF, GENERATOR† ($1V_{P-P}$)

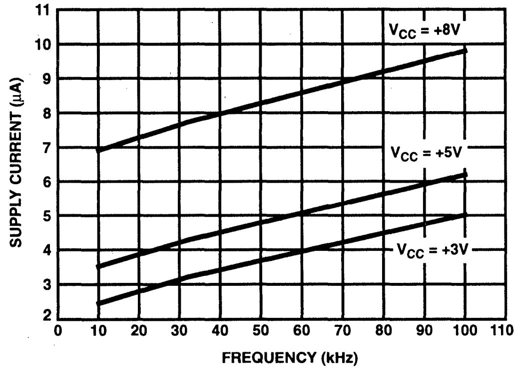


FIGURE 18. DISABLE SUPPLY CURRENT vs FREQUENCY

EN = 1, F1 = 0, F2 = 0, V_{CC} = +5V, GENERATOR† ($1V_{P-P}$)

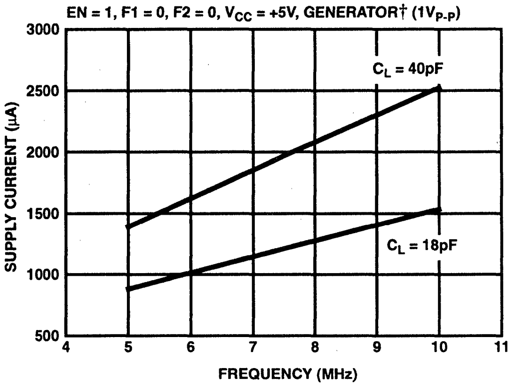


FIGURE 19. SUPPLY CURRENT vs FREQUENCY

EN = 1, F1 = 0, F2 = 1, V_{CC} = +5V, GENERATOR† ($1V_{P-P}$)

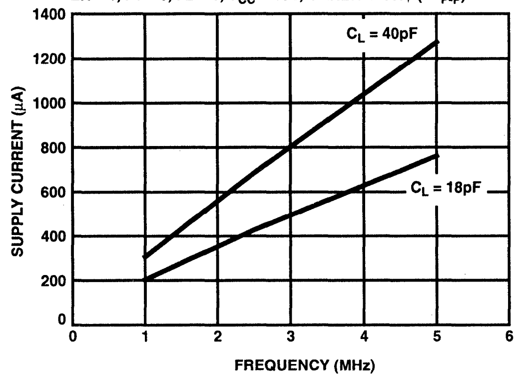


FIGURE 20. SUPPLY CURRENT vs FREQUENCY

EN = 1, F1 = 1, F2 = 0, V_{CC} = +5V, GENERATOR† ($1V_{P-P}$)

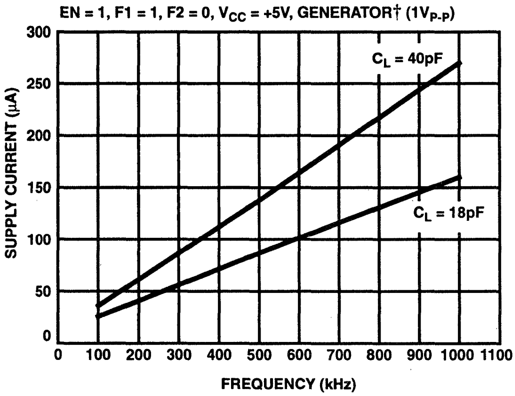


FIGURE 21. SUPPLY CURRENT vs FREQUENCY

EN = 1, F1 = 1, F2 = 1, V_{CC} = +5V, GENERATOR† ($1V_{P-P}$)

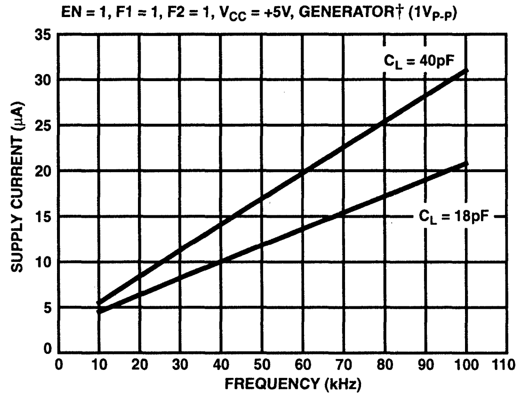


FIGURE 22. SUPPLY CURRENT vs FREQUENCY

†Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

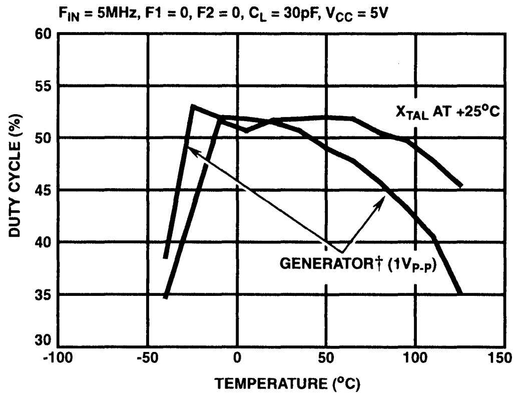


FIGURE 23. DUTY CYCLE vs TEMPERATURE

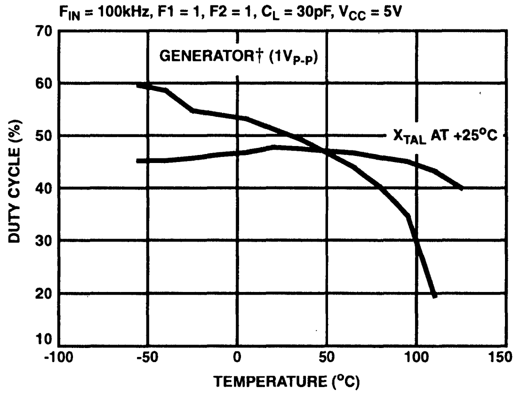


FIGURE 24. DUTY CYCLE vs TEMPERATURE

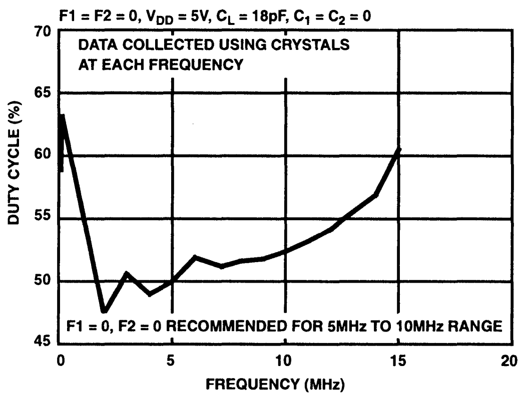


FIGURE 25. DUTY CYCLE vs FREQUENCY

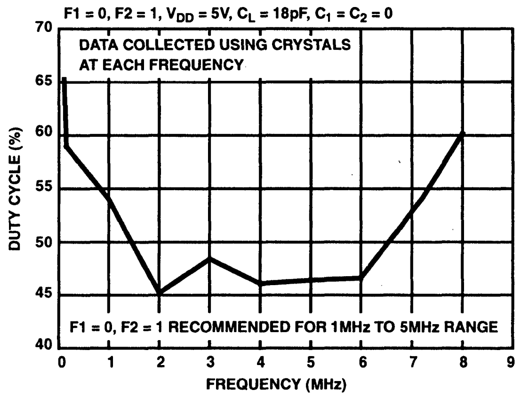


FIGURE 26. DUTY CYCLE vs FREQUENCY

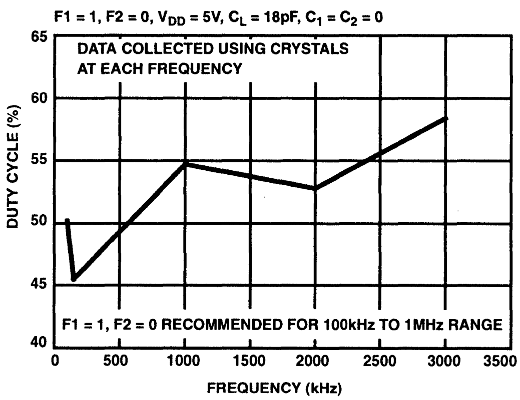


FIGURE 27. DUTY CYCLE vs FREQUENCY

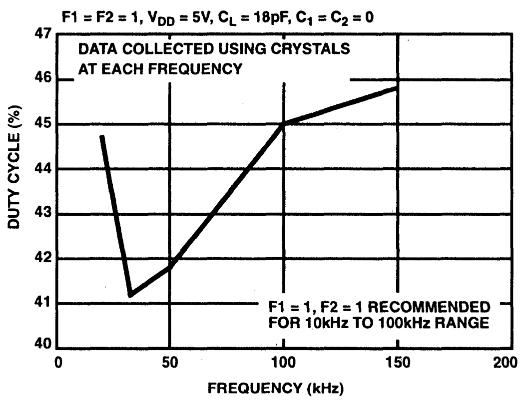


FIGURE 28. DUTY CYCLE vs FREQUENCY

†Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

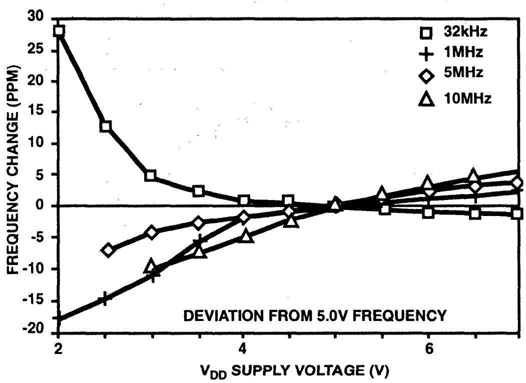


FIGURE 29. FREQUENCY CHANGE vs V_{DD}

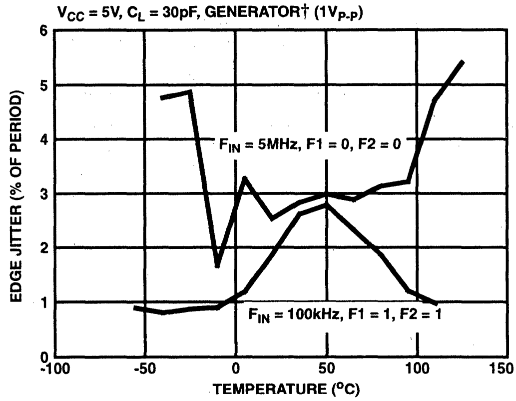


FIGURE 30. EDGE JITTER vs TEMPERATURE

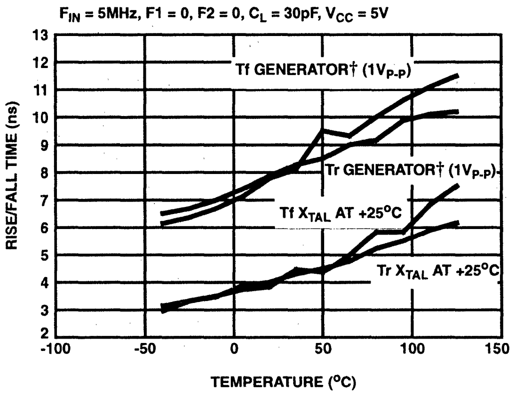


FIGURE 31. RISE/FALL TIME vs TEMPERATURE

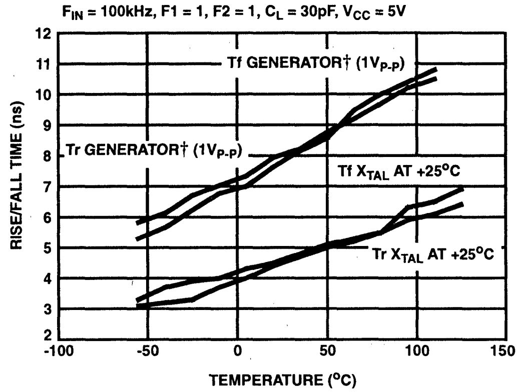


FIGURE 32. RISE/FALL TIME vs TEMPERATURE

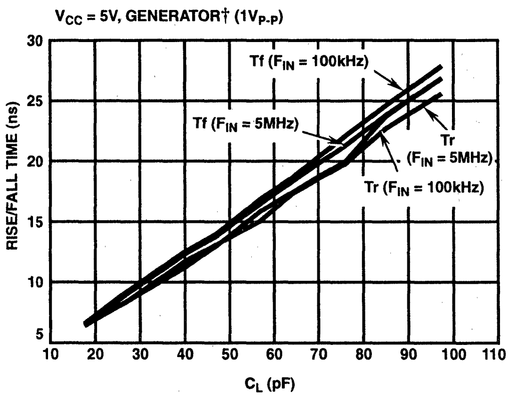


FIGURE 33. RISE/FALL TIME vs C_L

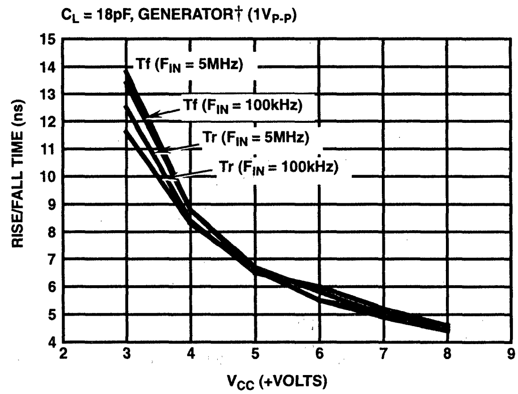


FIGURE 34. RISE/FALL TIME vs V_{CC}

†Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

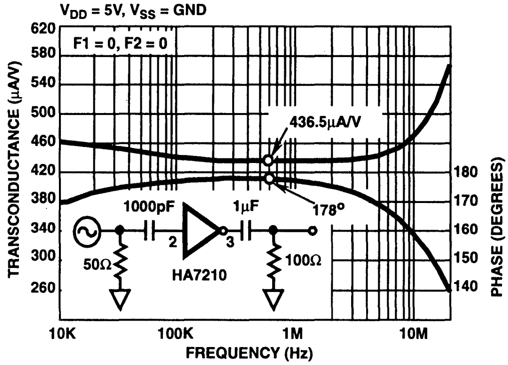


FIGURE 35. TRANSCONDUCTANCE vs FREQUENCY

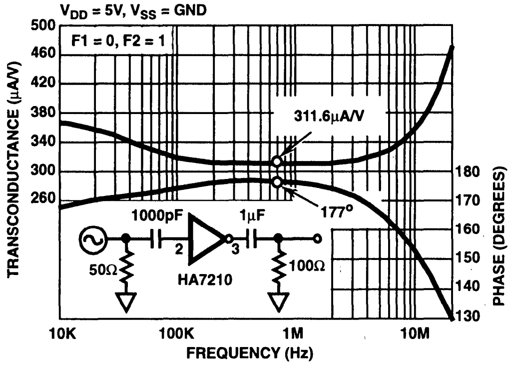


FIGURE 36. TRANSCONDUCTANCE vs FREQUENCY

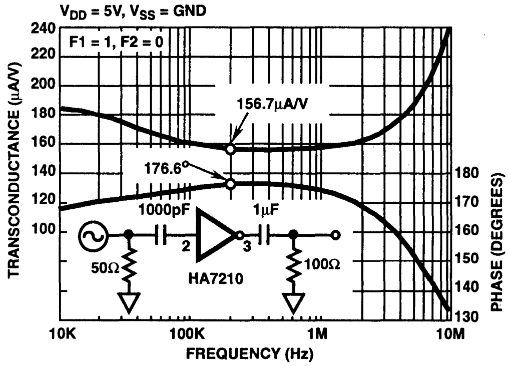


FIGURE 37. TRANSCONDUCTANCE vs FREQUENCY

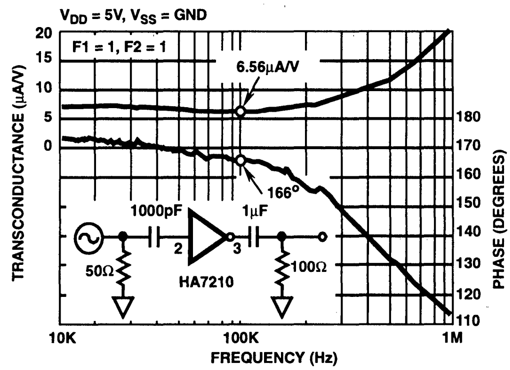


FIGURE 38. TRANSCONDUCTANCE vs FREQUENCY

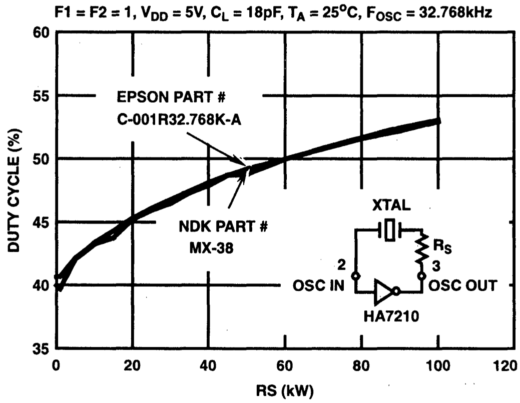


FIGURE 39. DUTY CYCLE vs R_S at 32kHz

NOTE: Figure 39 (Duty Cycle vs R_S at 32kHz) should only be used for 32kHz crystals. R_S may be used at other frequencies to adjust Duty Cycle but experimentation will be required to find an appropriate value. The R_S value will be proportional to the effective series resistance of the crystal being used.

HARRIS SEMICONDUCTOR

HFA3046, HFA3096, HFA3127, HFA3128

July 1995

Ultra High Frequency Transistor Array

Features

- NPN Transistor (f_T) 8GHz
- NPN Current Gain (h_{FE}) 70
- NPN Early Voltage (V_A) 50V
- PNP Transistor (f_T) 5.5GHz
- PNP Current Gain (h_{FE}) 40
- PNP Early Voltage (V_A) 25V
- Noise Figure (50Ω) at 1.0GHz 3.5dB
- Collector-to-Collector Leakage .... <1pA
- Complete Isolation Between Transistors
- Pin Compatible with Industry Standard 3XXX Series Arrays

Applications

- VHF/UHF Amplifiers
- VHF/UHF Mixers
- IF Converters
- Synchronous Detectors

Description

The HFA3046, HFA3096, HFA3127 and the HFA3128 are Ultra High Frequency Transistor Arrays that are fabricated from Harris Semiconductor's complementary bipolar UHF-1 process. Each array consists of five dielectrically isolated transistors on a common monolithic substrate. The NPN transistors exhibit a f_T of 8GHz while the PNP transistors provide a f_T of 5.5GHz. Both types exhibit low noise (3.5dB), making them ideal for high frequency amplifier and mixer applications.

The HFA3046 and HFA3127 are all-NPN arrays while the HFA3128 has all PNP transistors. The HFA3096 is a NPN-PNP combination. Access is provided to each of the terminals for the individual transistors for maximum application flexibility. Monolithic construction of these transistor arrays provides close electrical and thermal matching of the five transistors.

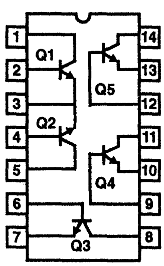
For PSPICE models, please request AnswerFAX document number 663046. Harris also provides an Application Note illustrating the use of these devices as RF amplifiers (request AnswerFAX document 99315).

Ordering Information

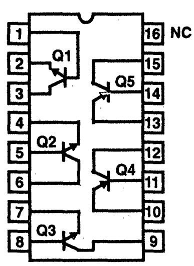
PART NUMBER	PACKAGE
HFA3046B	14 Lead Plastic SOIC (N)
HFA3096B, HFA3127B, HFA3128B	16 Lead Plastic SOIC (N)
HFA3046Y, HFA3096Y	Die
HFA3127Y, HFA3128Y	Die

Pinouts

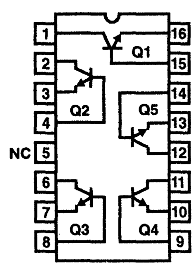
HFA3046
TOP VIEW



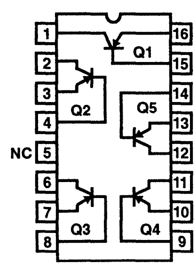
HFA3096
TOP VIEW



HFA3127
TOP VIEW



HFA3128
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3076.6

Absolute Maximum Ratings

Collector to Emitter Voltage (Open Base) 8.0V
Collector to Base Voltage (Shorted Base) 12.0V
Emitter to Base Voltage (Reverse Bias) 5.5V
Collector Current 15.5mA
Storage Temperature Range . . . . -65°C to +150°C
Operating Temperature Range . . . . -55°C to +125°C
Junction Temperature (Die) . . . . +175°C
Junction Temperature (Plastic Package) . . . . +150°C
Lead Temperature (Soldering 10s) (Lead Tips Only . . . . +300°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic 14 Lead SOIC Package . . . . 120°C/W
Plastic 16 Lead SOIC Package . . . . 115°C/W
Maximum Package Power Dissipation at +75°C
Plastic 14 Lead SOIC Package 0.63W
Plastic 16 Lead SOIC Package 0.66W
Any One Transistor 0.15W
Derating Factor Above +75°C
Plastic 14 Lead SOIC Package . . . . 8.4mW/°C
Plastic 16 Lead SOIC Package . . . . 8.7mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Static NPN Characteristics at T_A = +25°C

PARAMETERS	TEST CONDITIONS	DIE MIN	DIE TYP	DIE MAX	SOIC MIN	SOIC TYP	SOIC MAX	UNITS
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$	I_C = 100µA, I_E = 0	12	18	-	12	18	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CEO}$	I_C = 100µA, I_B = 0	8	12	-	8	12	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$	I_C = 100µA, Base Shorted to Emitter	10	20	-	10	20	-	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$	I_E = 10µA, I_C = 0	5.5	6	-	5.5	6	-	V
Collector-Cutoff-Current, I_{CEO}	V_{CE} = 6V, I_B = 0	-	2	100	-	2	100	nA
Collector-Cutoff-Current, I_{CBO}	V_{CB} = 8V, I_E = 0	-	0.1	10	-	0.1	10	nA
Collector-to-Emitter Saturation Voltage, $V_{CE(SAT)}$	I_C = 10mA, I_B = 1mA	-	0.3	0.5	-	0.3	0.5	V
Base-to-Emitter Voltage, V_{BE}	I_C = 10mA	-	0.85	0.95	-	0.85	0.95	V
DC Forward-Current Transfer Ratio, h_{FE}	I_C = 10mA V_{CE} = 2V	40	70	-	40	70	-	
Early Voltage, V_A	I_C = 1mA, V_{CE} = 3.5V	20	50	-	20	50	-	V
Base-to-Emitter Voltage Drift	I_C = 10mA	-	-1.5	-	-	-1.5	-	mV/°C
Collector-to-Collector Leakage		-	1	-	-	1	-	pA

Dynamic NPN Characteristics at T_A = +25°C

PARAMETERS	TEST CONDITIONS	DIE MIN	DIE TYP	DIE MAX	SOIC MIN	SOIC TYP	SOIC MAX	UNITS
Noise Figure	f = 1.0GHz, V_{CE} = 5V, I_C = 5mA, Z_S = 50Ω	-	3.5	-	-	3.5	-	dB
f_T Current Gain-Bandwidth Product	I_C = 1mA, V_{CE} = 5V	-	5.5	-	-	5.5	-	GHz
	I_C = 10mA, V_{CE} = 5V	-	8	-	-	8	-	GHz
Power Gain-Bandwidth Product, f_{MAX}	I_C = 10mA, V_{CE} = 5V	-	6	-	-	2.5	-	GHz
Base-to-Emitter Capacitance	V_{BE} = -3V	-	200	-	-	500	-	fF
Collector-to-Base Capacitance	V_{CB} = 3V	-	200	-	-	500	-	fF

Static PNP Characteristics at $T_A = +25^oC$

PARAMETERS	TEST CONDITIONS	DIE			SOIC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$	$I_C = -100\mu A$, $I_E = 0$	10	15	-	10	15	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CEO}$	$I_C = -100\mu A$, $I_B = 0$	8	15	-	8	15	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CES}$	$I_C = -100\mu A$, Base Shorted to Emitter	10	15	-	10	15	-	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$	$I_E = -10\mu A$, $I_C = 0$	4.5	5	-	4.5	5	-	V
Collector-Cutoff-Current, I_{CEO}	$V_{CE} = -6V$, $I_B = 0$	-	2	100	-	2	100	nA
Collector-Cutoff-Current, I_{CBO}	$V_{CB} = -8V$, $I_E = 0$	-	0.1	10	-	0.1	10	nA
Collector-to-Emitter Saturation Voltage, $V_{CE(SAT)}$	$I_C = -10mA$, $I_B = -1mA$	-	0.3	0.5	-	0.3	0.5	V
Base-to-Emitter Voltage, V_{BE}	$I_C = -10mA$	-	0.85	0.95	-	0.85	0.95	V
DC Forward-Current Transfer Ratio, h_{FE}	$I_C = -10mA$, $V_{CE} = -2V$	25	40	-	25	40	-	
Early Voltage, V_A	$I_C = -1mA$, $V_{CE} = -3.5V$	10	25	-	10	25	-	V
Base-to-Emitter Voltage Drift	$I_C = -10mA$	-	-1.5	-	-	-1.5	-	mV/^{o}C
Collector-to-Collector Leakage		-	1	-	-	1	-	pA

Dynamic PNP Characteristics at $T_A = +25^oC$

PARAMETERS	TEST CONDITIONS	DIE			SOIC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Noise Figure	$f = 1.0GHz$, $V_{CE} = -5V$, $I_C = -5mA$, $Z_S = 50\Omega$	-	3.5	-	-	3.5	-	dB
f_T Current Gain-Bandwidth Product	$I_C = -1mA$, $V_{CE} = -5V$	-	2	-	-	2	-	GHz
	$I_C = -10mA$, $V_{CE} = -5V$	-	5.5	-	-	5.5	-	GHz
Power Gain-Bandwidth Product	$I_C = -10mA$, $V_{CE} = -5V$	-	3	-	-	2	-	GHz
Base-to-Emitter Capacitance	$V_{BE} = 3V$	-	200	-	-	500	-	fF
Collector-to-Base Capacitance	$V_{CB} = -3V$	-	300	-	-	600	-	fF

Differential Pair Matching Characteristics for the HFA3046

PARAMETERS	TEST CONDITIONS	DIE			SOIC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$I_C = 10mA$, $V_{CE} = 5V$	-	1.5	5.0	-	1.5	5.0	mV
Input Offset Current	$I_C = 10mA$, $V_{CE} = 5V$	-	5	25	-	5	25	μA
Input Offset Voltage TC	$I_C = 10mA$, $V_{CE} = 5V$	-	0.5	-	-	0.5	-	μV/^{o}C

S-Parameter and PSPICE model data is available from Harris Sales Offices.

Common Emitter S-Parameters of NPN 3µm x 50µm Transistor

FREQ. (Hz)	IS11I	PHASE(S11)	IS12I	PHASE(S12)	IS21I	PHASE(S21)	IS22I	PHASE(S22)
V_{CE} = 5V and I_C = 5mA								
1.0E+08	0.83	-11.78	1.41E-02	78.88	11.07	168.57	0.97	-11.05
2.0E+08	0.79	-22.82	2.69E-02	68.63	10.51	157.89	0.93	-21.35
3.0E+08	0.73	-32.64	3.75E-02	59.58	9.75	148.44	0.86	-30.44
4.0E+08	0.67	-41.08	4.57E-02	51.90	8.91	140.36	0.79	-38.16
5.0E+08	0.61	-48.23	5.19E-02	45.50	8.10	133.56	0.73	-44.59
6.0E+08	0.55	-54.27	5.65E-02	40.21	7.35	127.88	0.67	-49.93
7.0E+08	0.50	-59.41	6.00E-02	35.82	6.69	123.10	0.62	-54.37
8.0E+08	0.46	-63.81	6.27E-02	32.15	6.11	119.04	0.57	-58.10
9.0E+08	0.42	-67.63	6.47E-02	29.07	5.61	115.57	0.53	-61.25
1.0E+09	0.39	-70.98	6.63E-02	26.45	5.17	112.55	0.50	-63.96
1.1E+09	0.36	-73.95	6.75E-02	24.19	4.79	109.91	0.47	-66.31
1.2E+09	0.34	-76.62	6.85E-02	22.24	4.45	107.57	0.45	-68.37
1.3E+09	0.32	-79.04	6.93E-02	20.53	4.15	105.47	0.43	-70.19
1.4E+09	0.30	-81.25	7.00E-02	19.02	3.89	103.57	0.41	-71.83
1.5E+09	0.28	-83.28	7.05E-02	17.69	3.66	101.84	0.40	-73.31
1.6E+09	0.27	-85.17	7.10E-02	16.49	3.45	100.26	0.39	-74.66
1.7E+09	0.25	-86.92	7.13E-02	15.41	3.27	98.79	0.38	-75.90
1.8E+09	0.24	-88.57	7.17E-02	14.43	3.10	97.43	0.37	-77.05
1.9E+09	0.23	-90.12	7.19E-02	13.54	2.94	96.15	0.36	-78.12
2.0E+09	0.22	-91.59	7.21E-02	12.73	2.80	94.95	0.35	-79.13
2.1E+09	0.21	-92.98	7.23E-02	11.98	2.68	93.81	0.35	-80.09
2.2E+09	0.20	-94.30	7.25E-02	11.29	2.56	92.73	0.34	-80.99
2.3E+09	0.20	-95.57	7.27E-02	10.64	2.45	91.70	0.34	-81.85
2.4E+09	0.19	-96.78	7.28E-02	10.05	2.35	90.72	0.33	-82.68
2.5E+09	0.18	-97.93	7.29E-02	9.49	2.26	89.78	0.33	-83.47
2.6E+09	0.18	-99.05	7.30E-02	8.96	2.18	88.87	0.33	-84.23
2.7E+09	0.17	-100.12	7.31E-02	8.47	2.10	88.00	0.33	-84.97
2.8E+09	0.17	-101.15	7.31E-02	8.01	2.02	87.15	0.33	-85.68
2.9E+09	0.16	-102.15	7.32E-02	7.57	1.96	86.33	0.33	-86.37
3.0E+09	0.16	-103.11	7.32E-02	7.16	1.89	85.54	0.33	-87.05

Common Emitter S-Parameters of NPN 3μm x 50μm Transistor (Continued)

FREQ. (Hz)	IS11I	PHASE(S11)	IS12I	PHASE(S12)	IS21I	PHASE(S21)	IS22I	PHASE(S22)
V_{CE} = 5V and I_C = 10mA								
1.0E+08	0.72	-16.43	1.27E-02	75.41	15.12	165.22	0.95	-14.26
2.0E+08	0.67	-31.26	2.34E-02	62.89	13.90	152.04	0.88	-26.95
3.0E+08	0.60	-43.76	3.13E-02	52.58	12.39	141.18	0.79	-37.31
4.0E+08	0.53	-54.00	3.68E-02	44.50	10.92	132.57	0.70	-45.45
5.0E+08	0.47	-62.38	4.05E-02	38.23	9.62	125.78	0.63	-51.77
6.0E+08	0.42	-69.35	4.31E-02	33.34	8.53	120.37	0.57	-56.72
7.0E+08	0.37	-75.26	4.49E-02	29.47	7.62	116.00	0.51	-60.65
8.0E+08	0.34	-80.36	4.63E-02	26.37	6.86	112.39	0.47	-63.85
9.0E+08	0.31	-84.84	4.72E-02	23.84	6.22	109.36	0.44	-66.49
1.0E+09	0.29	-88.83	4.80E-02	21.75	5.69	106.77	0.41	-68.71
1.1E+09	0.27	-92.44	4.86E-02	20.00	5.23	104.51	0.39	-70.62
1.2E+09	0.25	-95.73	4.90E-02	18.52	4.83	102.53	0.37	-72.28
1.3E+09	0.24	-98.75	4.94E-02	17.25	4.49	100.75	0.35	-73.76
1.4E+09	0.22	-101.55	4.97E-02	16.15	4.19	99.16	0.34	-75.08
1.5E+09	0.21	-104.15	4.99E-02	15.19	3.93	97.70	0.33	-76.28
1.6E+09	0.20	-106.57	5.01E-02	14.34	3.70	96.36	0.32	-77.38
1.7E+09	0.20	-108.85	5.03E-02	13.60	3.49	95.12	0.31	-78.41
1.8E+09	0.19	-110.98	5.05E-02	12.94	3.30	93.96	0.31	-79.37
1.9E+09	0.18	-113.00	5.06E-02	12.34	3.13	92.87	0.30	-80.27
2.0E+09	0.18	-114.90	5.07E-02	11.81	2.98	91.85	0.30	-81.13
2.1E+09	0.17	-116.69	5.08E-02	11.33	2.84	90.87	0.30	-81.95
2.2E+09	0.17	-118.39	5.09E-02	10.89	2.72	89.94	0.29	-82.74
2.3E+09	0.16	-120.01	5.10E-02	10.50	2.60	89.06	0.29	-83.50
2.4E+09	0.16	-121.54	5.11E-02	10.13	2.49	88.21	0.29	-84.24
2.5E+09	0.16	-122.99	5.12E-02	9.80	2.39	87.39	0.29	-84.95
2.6E+09	0.15	-124.37	5.12E-02	9.49	2.30	86.60	0.29	-85.64
2.7E+09	0.15	-125.69	5.13E-02	9.21	2.22	85.83	0.29	-86.32
2.8E+09	0.15	-126.94	5.13E-02	8.95	2.14	85.09	0.29	-86.98
2.9E+09	0.15	-128.14	5.14E-02	8.71	2.06	84.36	0.29	-87.62
3.0E+09	0.14	-129.27	5.15E-02	8.49	1.99	83.66	0.29	-88.25

Common Emitter S-Parameters of PNP 3mm^2 x 50mm^2 Transistor

FREQ. (Hz)	IS11I	PHASE(S11)	IS21I	PHASE(S21)	IS12I	PHASE(S12)	IS22I	PHASE(S22)
V_{CE} = -5V and I_C = -5mA								
1.0E+08	0.72	-16.65	10.11	166.77	1.66E-02	77.18	0.96	-10.76
2.0E+08	0.68	-32.12	9.44	154.69	3.10E-02	65.94	0.90	-20.38
3.0E+08	0.62	-45.73	8.57	144.40	4.23E-02	56.39	0.82	-28.25
4.0E+08	0.57	-57.39	7.68	135.95	5.05E-02	48.66	0.74	-34.31
5.0E+08	0.52	-67.32	6.86	129.11	5.64E-02	42.52	0.67	-38.81
6.0E+08	0.47	-75.83	6.14	123.55	6.07E-02	37.66	0.61	-42.10
7.0E+08	0.43	-83.18	5.53	118.98	6.37E-02	33.79	0.55	-44.47
8.0E+08	0.40	-89.60	5.01	115.17	6.60E-02	30.67	0.51	-46.15
9.0E+08	0.38	-95.26	4.56	111.94	6.77E-02	28.14	0.47	-47.33
1.0E+09	0.36	-100.29	4.18	109.17	6.91E-02	26.06	0.44	-48.15
1.1E+09	0.34	-104.80	3.86	106.76	7.01E-02	24.33	0.41	-48.69
1.2E+09	0.33	-108.86	3.58	104.63	7.09E-02	22.89	0.39	-49.05
1.3E+09	0.32	-112.53	3.33	102.72	7.16E-02	21.67	0.37	-49.26
1.4E+09	0.30	-115.86	3.12	101.01	7.22E-02	20.64	0.36	-49.38
1.5E+09	0.30	-118.90	2.92	99.44	7.27E-02	19.76	0.34	-49.43
1.6E+09	0.29	-121.69	2.75	98.01	7.32E-02	19.00	0.33	-49.44
1.7E+09	0.28	-124.24	2.60	96.68	7.35E-02	18.35	0.32	-49.43
1.8E+09	0.28	-126.59	2.47	95.44	7.39E-02	17.79	0.31	-49.40
1.9E+09	0.27	-128.76	2.34	94.29	7.42E-02	17.30	0.30	-49.38
2.0E+09	0.27	-130.77	2.23	93.19	7.45E-02	16.88	0.30	-49.36
2.1E+09	0.26	-132.63	2.13	92.16	7.47E-02	16.52	0.29	-49.35
2.2E+09	0.26	-134.35	2.04	91.18	7.50E-02	16.20	0.28	-49.35
2.3E+09	0.26	-135.96	1.95	90.24	7.52E-02	15.92	0.28	-49.38
2.4E+09	0.25	-137.46	1.87	89.34	7.55E-02	15.68	0.28	-49.42
2.5E+09	0.25	-138.86	1.80	88.48	7.57E-02	15.48	0.27	-49.49
2.6E+09	0.25	-140.17	1.73	87.65	7.59E-02	15.30	0.27	-49.56
2.7E+09	0.25	-141.39	1.67	86.85	7.61E-02	15.15	0.26	-49.67
2.8E+09	0.25	-142.54	1.61	86.07	7.63E-02	15.01	0.26	-49.81
2.9E+09	0.24	-143.62	1.56	85.31	7.65E-02	14.90	0.26	-49.96
3.0E+09	0.24	-144.64	1.51	84.58	7.67E-02	14.81	0.26	-50.13

Common Emitter S-Parameters of PNP $3mm^2$ x $50mm^2$ Transistor (Continued)

FREQ. (Hz)	IS11I	PHASE(S11)	IS21I	PHASE(S21)	IS12I	PHASE(S12)	IS22I	PHASE(S22)
V_{CE} = -5V, I_C = -10mA								
1.0E+08	0.58	-23.24	13.03	163.45	1.43E-02	73.38	0.93	-13.46
2.0E+08	0.53	-44.07	11.75	149.11	2.58E-02	60.43	0.85	-24.76
3.0E+08	0.48	-61.50	10.25	137.78	3.38E-02	50.16	0.74	-33.10
4.0E+08	0.43	-75.73	8.88	129.12	3.90E-02	42.49	0.65	-38.83
5.0E+08	0.40	-87.36	7.72	122.49	4.25E-02	36.81	0.58	-42.63
6.0E+08	0.37	-96.94	6.78	117.33	4.48E-02	32.59	0.51	-45.07
7.0E+08	0.35	-104.92	6.01	113.22	4.64E-02	29.39	0.47	-46.60
8.0E+08	0.33	-111.64	5.39	109.85	4.76E-02	26.94	0.43	-47.49
9.0E+08	0.32	-117.36	4.87	107.05	4.85E-02	25.04	0.40	-47.97
1.0E+09	0.31	-122.27	4.44	104.66	4.92E-02	23.55	0.37	-48.18
1.1E+09	0.30	-126.51	4.07	102.59	4.97E-02	22.37	0.35	-48.20
1.2E+09	0.30	-130.21	3.76	100.76	5.02E-02	21.44	0.33	-48.11
1.3E+09	0.29	-133.46	3.49	99.14	5.06E-02	20.70	0.32	-47.95
1.4E+09	0.29	-136.33	3.25	97.67	5.09E-02	20.11	0.31	-47.77
1.5E+09	0.28	-138.89	3.05	96.33	5.12E-02	19.65	0.30	-47.58
1.6E+09	0.28	-141.17	2.87	95.10	5.15E-02	19.29	0.29	-47.39
1.7E+09	0.28	-143.21	2.70	93.96	5.18E-02	19.01	0.28	-47.23
1.8E+09	0.28	-145.06	2.56	92.90	5.21E-02	18.80	0.27	-47.09
1.9E+09	0.27	-146.73	2.43	91.90	5.23E-02	18.65	0.27	-46.98
2.0E+09	0.27	-148.26	2.31	90.95	5.26E-02	18.55	0.26	-46.91
2.1E+09	0.27	-149.65	2.20	90.05	5.28E-02	18.49	0.26	-46.87
2.2E+09	0.27	-150.92	2.10	89.20	5.30E-02	18.46	0.25	-46.87
2.3E+09	0.27	-152.10	2.01	88.37	5.33E-02	18.47	0.25	-46.90
2.4E+09	0.27	-153.18	1.93	87.59	5.35E-02	18.50	0.25	-46.97
2.5E+09	0.27	-154.17	1.86	86.82	5.38E-02	18.55	0.24	-47.07
2.6E+09	0.26	-155.10	1.79	86.09	5.40E-02	18.62	0.24	-47.18
2.7E+09	0.26	-155.96	1.72	85.38	5.42E-02	18.71	0.24	-47.34
2.8E+09	0.26	-156.76	1.66	84.68	5.45E-02	18.80	0.24	-47.55
2.9E+09	0.26	-157.51	1.60	84.01	5.47E-02	18.91	0.24	-47.76
3.0E+09	0.26	-158.21	1.55	83.35	5.50E-02	19.03	0.23	-48.00

Die Characteristics

PROCESS:
UHF-1

DIE DIMENSIONS:
53 x 52 x 19 ± 1mils
1340μm x 1320μm ± 25.4μm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

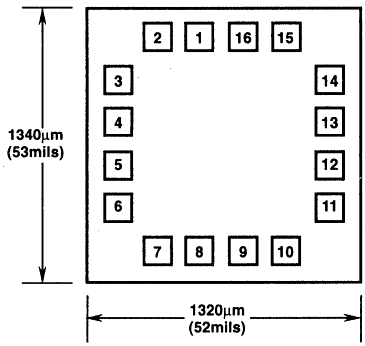
GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

DIE ATTACH:
Material: Epoxy

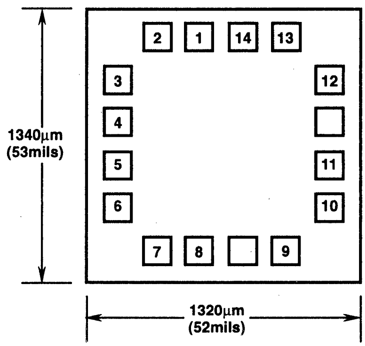
WORST CASE CURRENT DENSITY:
1.39×10^5 A/cm^2

Metallization Mask Layout

HFA3096, HFA3127, HFA3128



HFA3046



Pad numbers correspond to package part pin out.

Typical Performance Curves

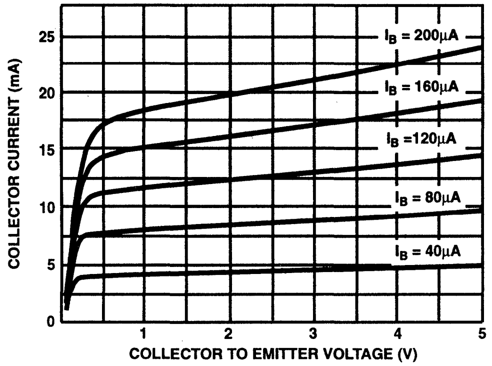


FIGURE 1. NPN COLLECTOR CURRENT vs COLLECTOR TO EMITTER VOLTAGE

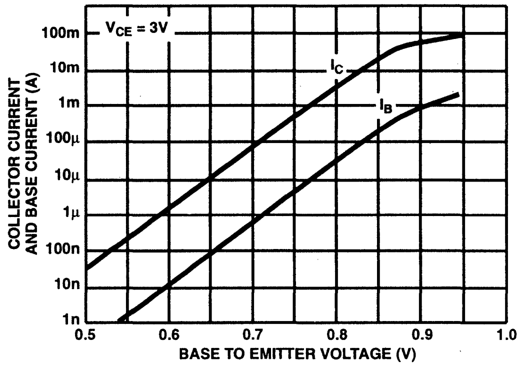


FIGURE 2. NPN COLLECTOR CURRENT AND BASE CURRENT TO EMITTER VOLTAGE

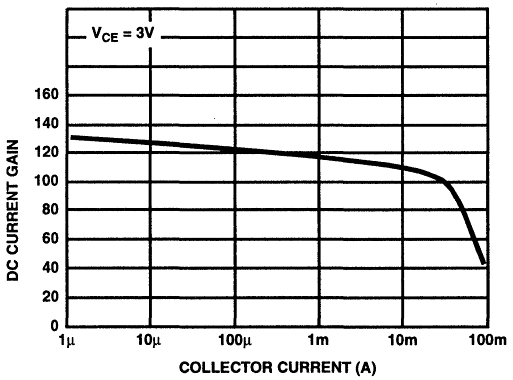


FIGURE 3. NPN DC CURRENT GAIN vs COLLECTOR CURRENT

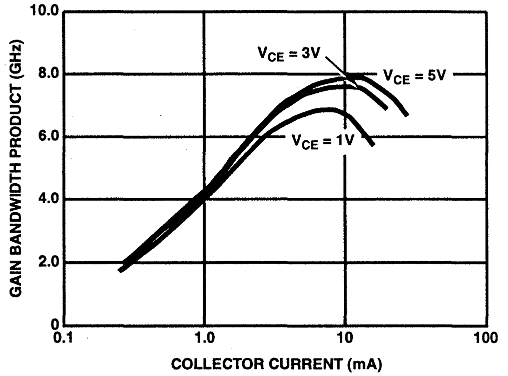


FIGURE 4. NPN GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT (UHF 3 x 50 WITH BOND PADS)

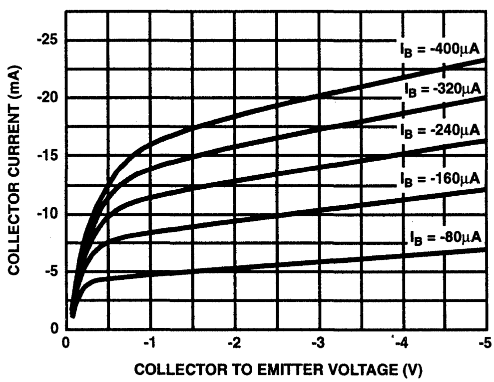


FIGURE 5. PNP COLLECTOR CURRENT vs COLLECTOR TO EMITTER VOLTAGE

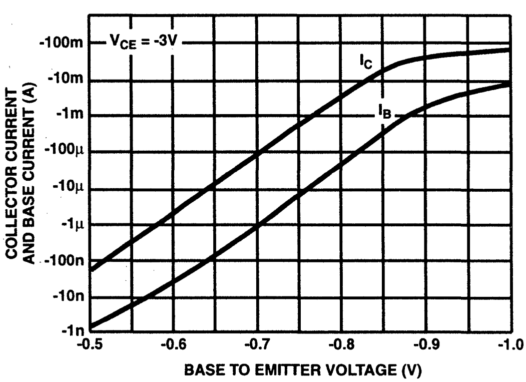


FIGURE 6. PNP COLLECTOR CURRENT AND BASE CURRENT TO EMITTER VOLTAGE

Typical Performance Curves (Continued)

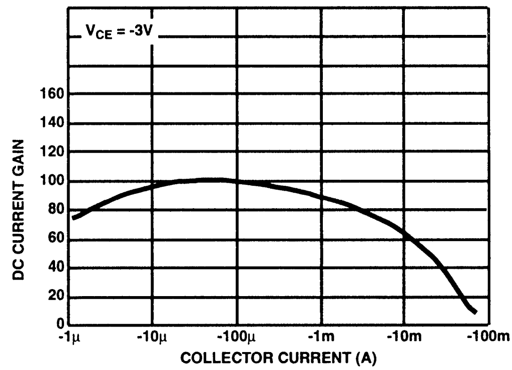


FIGURE 7. PNP DC CURRENT GAIN vs COLLECTOR CURRENT

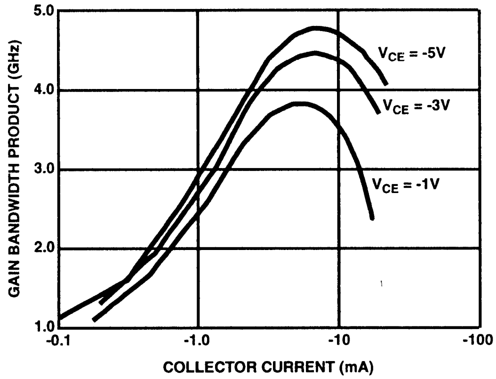


FIGURE 8. PNP GAIN BANDWIDTH PRODUCT vs COLLECTOR CURRENT (UHF 3 x 50 WITH BOND PADS)

9

SPECIAL ANALOG CIRCUITS

HFA3101

SEMICONDUCTOR

July 1995

Gilbert Cell UHF Transistor Array

Features

- High Gain Bandwidth Product (f_T) 10GHz
- High Power Gain Bandwidth Product 5GHz
- Current Gain (h_{FE}) . . . . Typically 70
- Low Noise Figure (Transistor) 3.5dB
- Excellent h_{FE} and V_{BE} Matching
- Low Collector Leakage Current . . . . <0.01nA
- Pin-to-Pin Compatible to UPA101

Applications

- Balanced Mixers
- Multipliers
- Demodulators/Modulators
- Automatic Gain Control Circuits
- Phase Detectors
- Fiber Optic Signal Processing
- Wireless Communication Systems
- Wide Band Amplification Stages
- Radio and Satellite Communications
- High Performance Instrumentation

Description

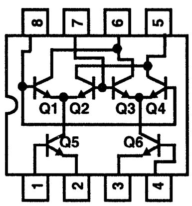
The HFA3101 is an all NPN transistor array configured as a Multiplier Cell. Based on Harris bonded wafer UHF-1 SOI process, this array achieves very high f_T (10GHz) while maintaining excellent h_{FE} and V_{BE} matching characteristics that have been maximized through careful attention to circuit design and layout, making this product ideal for communication circuits. For use in mixer applications, the cell provides high gain and good cancellation of 2nd order distortion terms.

Ordering Information

PART NUMBER	PACKAGE
HFA3101Y	DIE
HFA3101B	8 Lead Plastic SOIC (N)
HFA3101B96	8 Lead Plastic SOIC (N) - Tape and Reel

Pinout

HFA3101 (SOIC)
TOP VIEW



NOTE: Q5 and Q6 - 2 Paralleled 3μm x 50μm Transistors
Q1, Q2, Q3, Q4 - Single 3μm x 50μm Transistors

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3663.2**

Absolute Maximum Ratings

V_{CEO}, Collector to Emitter Voltage 8.0V
V_{CBO}, Collector to Base Voltage 12.0V
V_{EBO}, Emitter to Base Voltage 5.5V
I_C, Collector Current 30mA
T_{STG}, Storage Temperature Range . . . . . -65°C to +150°C
Operating Temperature Range . . . . . -40°C to +85°C
T_J, Junction Temperature (DIE) . . . . . +175°C
T_J, Junction Temperature (Plastic Package) . . . . . +150°C
Lead Temperature (Soldering 10s) (Lead Tips Only) . . . . . +300°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic 8 Lead SOIC Package . . . . . 185°C/W
Maximum Package Power Dissipation at +75°C
Plastic 8 Lead SOIC Package 0.4W
Derating Factor Above +75°C
Plastic 8 Lead SOIC Package . . . . . 5.4mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications at +25°C

PARAMETER		TEST CONDITIONS	(NOTE 1) TEST LEVEL	ALL GRADES MIN	TYP	MAX	UNITS
Collector-to-Base Breakdown Voltage, $V_{(BR)CBO}$, Q1 thru Q6		I_C = 100µA, I_E = 0	A	12	18	-	V
Collector-to-Emitter Breakdown Voltage, $V_{(BR)CEO}$, Q5 and Q6		I_C = 100µA, I_B = 0	A	8	12	-	V
Emitter-to-Base Breakdown Voltage, $V_{(BR)EBO}$, Q1 thru Q6		I_E = 10µA, I_C = 0	A	5.5	6	-	V
Collector Cutoff Current, I_{CBO}, Q1 thru Q4		V_{CB} = 8V, I_E = 0	A	-	0.1	10	nA
Emitter Cutoff Current, I_{EBO}, Q5 and Q6		V_{EB} = 1V, I_C = 0	A	-	-	200	nA
DC Current Gain, h_{FE}, Q1 thru Q6		I_C = 10mA, V_{CE} = 3V	A	40	70	-	
Collector-to-Base Capacitance, C_{CB}	Q1 thru Q4	V_{CB} = 5V, f = 1MHz	C	-	0.300	-	pF
	Q5 and Q6			-	0.600	-	pF
Emitter-to-Base Capacitance, C_{EB}	Q1 thru Q4	V_{EB} = 0, f = 1MHz	B	-	0.200	-	pF
	Q5 and Q6			-	0.400	-	pF
Current Gain-Bandwidth Product, f_T	Q1 thru Q4	I_C = 10mA, V_{CE} = 5V	C	-	10	-	GHz
	Q5 and Q6	I_C = 20mA, V_{CE} = 5V	C	-	10	-	GHz
Power Gain-Bandwidth Product, f_{MAX}	Q1 thru Q4	I_C = 10mA, V_{CE} = 5V	C	-	5	-	GHz
	Q5 and Q6	I_C = 20mA, V_{CE} = 5V	C	-	5	-	GHz
Available Gain at Minimum Noise Figure, G_{NFMIN}, Q5 and Q6		I_C = 5mA, V_{CE} = 3, f = 0.5GHz	C	-	17.5	-	dB
		f = 1.0GHz	C	-	11.9	-	dB
Minimum Noise Figure, NF_{MIN}, Q5 and Q6		I_C = 5mA, V_{CE} = 3V, f = 0.5GHz	C	-	1.7	-	dB
		f = 1.0GHz	C	-	2.0	-	dB
50Ω Noise Figure, $NF_{50\Omega}$, Q5 and Q6		I_C = 5mA, V_{CE} = 3V, f = 0.5GHz	C	-	2.25	-	dB
		f = 1.0GHz	C	-	2.5	-	dB
DC Current Gain Matching, h_{FE1}/h_{FE2}, Q1 and Q2, Q3 and Q4, and Q5 and Q6		V_{CE} = 3V, I_C = 10mA	A	0.9	1.0	1.1	
Input Offset Voltage, V_{OS}, (Q1 and Q2), (Q3 and Q4), (Q5 and Q6)		I_C = 10mA, V_{CE} = 3V	A	-	1.5	5	mV
Input Offset Current, I_C, (Q1 and Q2), (Q3 and Q4), (Q5 and Q6)		I_C = 10mA, V_{CE} = 3V	A	-	5	25	µA
Input Offset Voltage TC, dV_{OS}/dT, (Q1 and Q2, Q3 and Q4, Q5 and Q6)		I_C = 10mA, V_{CE} = 3V	C	-	0.5	-	µV/°C
Collector-to-Collector Leakage, $I_{TRENCH-LEAKAGE}$		ΔV_{TEST} = 5V	B	-	0.01	-	nA

NOTE:
1. Test Level: A. Production Tested, B. Guaranteed Limit or Typical Based on Characterization, C. Design Typical for Information Only.

PSPICE Model for a 3μm x 50μm Transistor

+ (IS = 1.840E-16	XTI = 3.000E+00	EG = 1.110E+00	VAF = 7.200E+01
+ VAR = 4.500E+00	BF = 1.036E+02	ISE = 1.686E-19	NE = 1.400E+00
+ IKF = 5.400E-02	XTB = 0.000E+00	BR = 1.000E+01	ISC = 1.605E-14
+ NC = 1.800E+00	IKR = 5.400E-02	RC = 1.140E+01	CJC = 3.980E-13
+ MJC = 2.400E-01	VJC = 9.700E-01	FC = 5.000E-01	CJE = 2.400E-13
+ MJE = 5.100E-01	VJE = 8.690E-01	TR = 4.000E-09	TF = 10.51E-12
+ ITF = 3.500E-02	XTF = 2.300E+00	VTF = 3.500E+00	PTF = 0.000E+00
+ XCJC = 9.000E-01	CJS = 1.689E-13	VJS = 9.982E-01	MJS = 0.000E+00
+ RE = 1.848E+00	RB = 5.007E+01	RBM = 1.974E+00	KF = 0.000E+00
+ AF = 1.000E+00)			

Common Emitter S-Parameters of 3μm x 50μm Transistor

FREQ. (Hz)	IS11I	PHASE(S11)	IS12I	PHASE(S12)	IS21I	PHASE(S21)	IS22I	PHASE(S22)
V_{CE} = 5V and I_C = 5mA								
1.0E+08	0.83	-11.78	1.41E-02	78.88	11.07	168.57	0.97	-11.05
2.0E+08	0.79	-22.82	2.69E-02	68.63	10.51	157.89	0.93	-21.35
3.0E+08	0.73	-32.64	3.75E-02	59.58	9.75	148.44	0.86	-30.44
4.0E+08	0.67	-41.08	4.57E-02	51.90	8.91	140.36	0.79	-38.16
5.0E+08	0.61	-48.23	5.19E-02	45.50	8.10	133.56	0.73	-44.59
6.0E+08	0.55	-54.27	5.65E-02	40.21	7.35	127.88	0.67	-49.93
7.0E+08	0.50	-59.41	6.00E-02	35.82	6.69	123.10	0.62	-54.37
8.0E+08	0.46	-63.81	6.27E-02	32.15	6.11	119.04	0.57	-58.10
9.0E+08	0.42	-67.63	6.47E-02	29.07	5.61	115.57	0.53	-61.25
1.0E+09	0.39	-70.98	6.63E-02	26.45	5.17	112.55	0.50	-63.96
1.1E+09	0.36	-73.95	6.75E-02	24.19	4.79	109.91	0.47	-66.31
1.2E+09	0.34	-76.62	6.85E-02	22.24	4.45	107.57	0.45	-68.37
1.3E+09	0.32	-79.04	6.93E-02	20.53	4.15	105.47	0.43	-70.19
1.4E+09	0.30	-81.25	7.00E-02	19.02	3.89	103.57	0.41	-71.83
1.5E+09	0.28	-83.28	7.05E-02	17.69	3.66	101.84	0.40	-73.31
1.6E+09	0.27	-85.17	7.10E-02	16.49	3.45	100.26	0.39	-74.66
1.7E+09	0.25	-86.92	7.13E-02	15.41	3.27	98.79	0.38	-75.90
1.8E+09	0.24	-88.57	7.17E-02	14.43	3.10	97.43	0.37	-77.05
1.9E+09	0.23	-90.12	7.19E-02	13.54	2.94	96.15	0.36	-78.12
2.0E+09	0.22	-91.59	7.21E-02	12.73	2.80	94.95	0.35	-79.13
2.1E+09	0.21	-92.98	7.23E-02	11.98	2.68	93.81	0.35	-80.09
2.2E+09	0.20	-94.30	7.25E-02	11.29	2.56	92.73	0.34	-80.99
2.3E+09	0.20	-95.57	7.27E-02	10.64	2.45	91.70	0.34	-81.85
2.4E+09	0.19	-96.78	7.28E-02	10.05	2.35	90.72	0.33	-82.68
2.5E+09	0.18	-97.93	7.29E-02	9.49	2.26	89.78	0.33	-83.47
2.6E+09	0.18	-99.05	7.30E-02	8.96	2.18	88.87	0.33	-84.23

Common Emitter S-Parameters of 3µm x 50µm Transistor (Continued)

FREQ. (Hz)	IS11I	PHASE(S11)	IS12I	PHASE(S12)	IS21I	PHASE(S21)	IS22I	PHASE(S22)
2.7E+09	0.17	-100.12	7.31E-02	8.47	2.10	88.00	0.33	-84.97
2.8E+09	0.17	-101.15	7.31E-02	8.01	2.02	87.15	0.33	-85.68
2.9E+09	0.16	-102.15	7.32E-02	7.57	1.96	86.33	0.33	-86.37
3.0E+09	0.16	-103.11	7.32E-02	7.16	1.89	85.54	0.33	-87.05
V_{CE} = 5V and I_C = 10mA								
1.0E+08	0.72	-16.43	1.27E-02	75.41	15.12	165.22	0.95	-14.26
2.0E+08	0.67	-31.26	2.34E-02	62.89	13.90	152.04	0.88	-26.95
3.0E+08	0.60	-43.76	3.13E-02	52.58	12.39	141.18	0.79	-37.31
4.0E+08	0.53	-54.00	3.68E-02	44.50	10.92	132.57	0.70	-45.45
5.0E+08	0.47	-62.38	4.05E-02	38.23	9.62	125.78	0.63	-51.77
6.0E+08	0.42	-69.35	4.31E-02	33.34	8.53	120.37	0.57	-56.72
7.0E+08	0.37	-75.26	4.49E-02	29.47	7.62	116.00	0.51	-60.65
8.0E+08	0.34	-80.36	4.63E-02	26.37	6.86	112.39	0.47	-63.85
9.0E+08	0.31	-84.84	4.72E-02	23.84	6.22	109.36	0.44	-66.49
1.0E+09	0.29	-88.83	4.80E-02	21.75	5.69	106.77	0.41	-68.71
1.1E+09	0.27	-92.44	4.86E-02	20.00	5.23	104.51	0.39	-70.62
1.2E+09	0.25	-95.73	4.90E-02	18.52	4.83	102.53	0.37	-72.28
1.3E+09	0.24	-98.75	4.94E-02	17.25	4.49	100.75	0.35	-73.76
1.4E+09	0.22	-101.55	4.97E-02	16.15	4.19	99.16	0.34	-75.08
1.5E+09	0.21	-104.15	4.99E-02	15.19	3.93	97.70	0.33	-76.28
1.6E+09	0.20	-106.57	5.01E-02	14.34	3.70	96.36	0.32	-77.38
1.7E+09	0.20	-108.85	5.03E-02	13.60	3.49	95.12	0.31	-78.41
1.8E+09	0.19	-110.98	5.05E-02	12.94	3.30	93.96	0.31	-79.37
1.9E+09	0.18	-113.00	5.06E-02	12.34	3.13	92.87	0.30	-80.27
2.0E+09	0.18	-114.90	5.07E-02	11.81	2.98	91.85	0.30	-81.13
2.1E+09	0.17	-116.69	5.08E-02	11.33	2.84	90.87	0.30	-81.95
2.2E+09	0.17	-118.39	5.09E-02	10.89	2.72	89.94	0.29	-82.74
2.3E+09	0.16	-120.01	5.10E-02	10.50	2.60	89.06	0.29	-83.50
2.4E+09	0.16	-121.54	5.11E-02	10.13	2.49	88.21	0.29	-84.24
2.5E+09	0.16	-122.99	5.12E-02	9.80	2.39	87.39	0.29	-84.95
2.6E+09	0.15	-124.37	5.12E-02	9.49	2.30	86.60	0.29	-85.64
2.7E+09	0.15	-125.69	5.13E-02	9.21	2.22	85.83	0.29	-86.32
2.8E+09	0.15	-126.94	5.13E-02	8.95	2.14	85.09	0.29	-86.98
2.9E+09	0.15	-128.14	5.14E-02	8.71	2.06	84.36	0.29	-87.62
3.0E+09	0.14	-129.27	5.15E-02	8.49	1.99	83.66	0.29	-88.25

Typical Performance Curves for Transistors

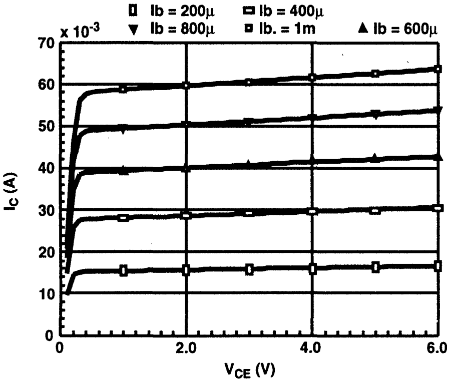


FIGURE 1. I_C vs V_{CE}

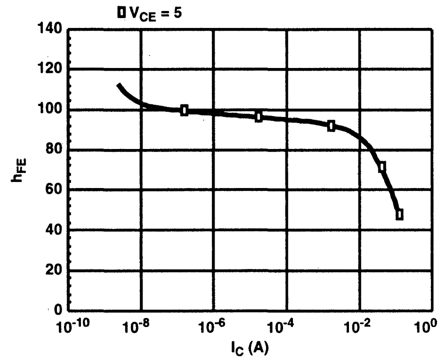


FIGURE 2. H_{FE} vs I_C

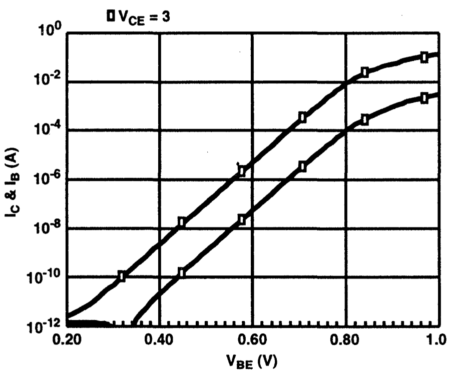


FIGURE 3. GUMMEL PLOT

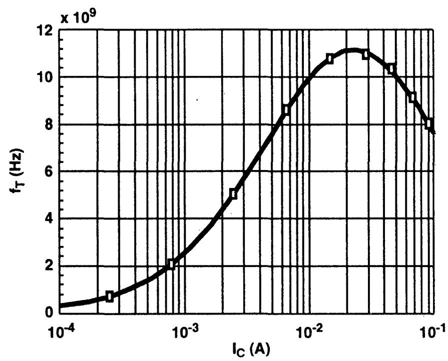


FIGURE 4. F_T vs I_C

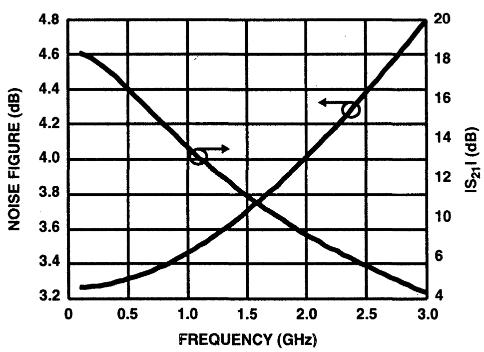


FIGURE 5. GAIN AND NOISE FIGURE vs FREQUENCY

NOTE: Figures 14 through 18 are only for Q5 and Q6.

Die Characteristics

PROCESS
UHF-1

DIE DIMENSIONS:
53 x 52 x 14 ±1mils
1340μm x 1320μm x 355.6μm ±25.4μm

METALLIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.5kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

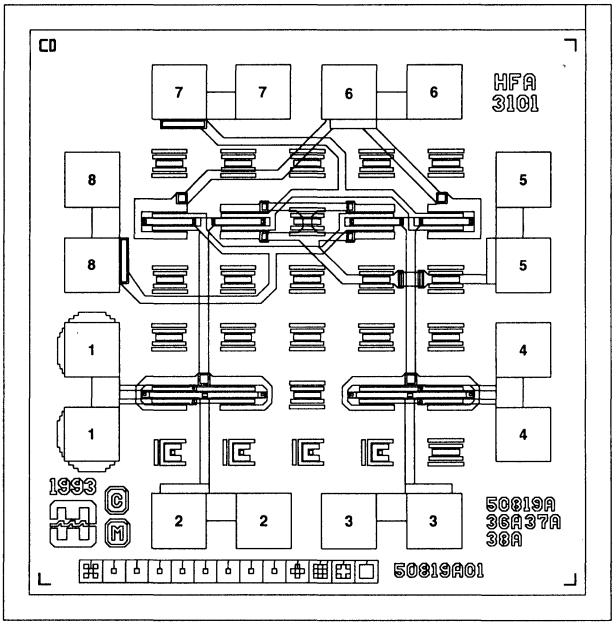
GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

DIE ATTACH:
Material: Epoxy

WORST CASE CURRENT DENSITY:
1.3636×10^5 A/cm^2

Metallization Mask Layout

HFA3101



Application Information

The HFA3101 array is a very versatile RF Building block. It has been carefully laid out to improve its matching properties, bringing the distortion due to area mismatches, thermal distribution, betas and ohmic resistances to a minimum.

The cell is equivalent to two differential stages built as two "variable transconductance multipliers" in parallel, with their outputs cross coupled. This configuration is well known in the industry as a Gilbert Cell which enables a four quadrant multiplication operation.

Due to the input dynamic range restrictions for the input levels at the upper quad transistors and lower tail transistors, the HFA3101 cell has restricted use as a linear four quadrant multiplier. However, its configuration is well suited for uses where its linear response is limited to one of the inputs only, as in modulators or mixer circuit applications. Examples of these circuits are up converters, down converters, frequency doublers and frequency/phase detectors.

Although linearization is still an issue for the lower pair input, emitter degeneration can be used to improve the dynamic range and consequent linearity. The HFA3101 has the lower pair emitters brought to external pins for this purpose.

In modulators applications, the upper quad transistors are used in a switching mode where the pairs Q1/Q2 and Q3/Q4 act as non saturating high speed switches. These switches are controlled by the signal often referred as the carrier input. The signal driving the lower pair Q5/Q6 is commonly used as the modulating input. This signal can be linearly transferred to the output by either the use of low signal levels (Well below the thermal voltage of 26mV) or by the use of emitter degeneration. The chopped waveform appearing at the output of the upper pair (Q1 to Q4) resembles a signal that is multiplied by +1 or -1 at every half cycle of the switching waveform.

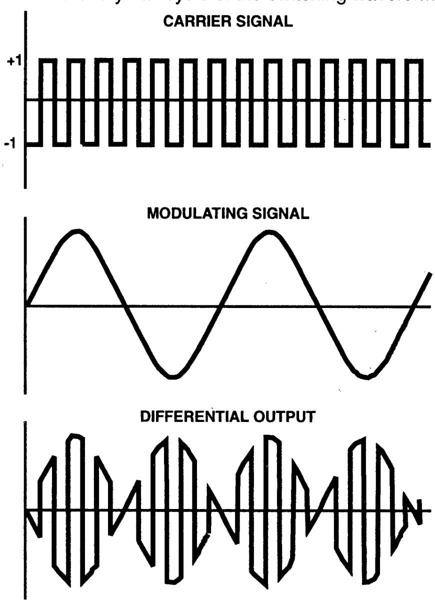


FIGURE 6. TYPICAL MODULATOR SIGNALS

Figure 6 shows the typical input waveforms where the frequency of the carrier is higher than the modulating signal. The output waveform shows a typical suppressed carrier output of an up converter or an AM signal generator.

Carrier suppression capability is a property of the well known Balanced modulator in which the output must be zero when one or the other input (carrier or modulating signal) is equal to zero. however, at very high frequencies, high frequency mismatches and AC offsets are always present and the suppression capability is often degraded causing carrier and modulating feedthrough to be present.

Being a frequency translation circuit, the balanced modulator has the properties of translating the modulating frequency (ω_M) to the carrier frequency (ω_C), generating the two side bands $\omega_U = \omega_C + \omega_M$ and $\omega_L = \omega_C - \omega_M$. Figure 7 shows some translating schemes being used by balanced mixers.

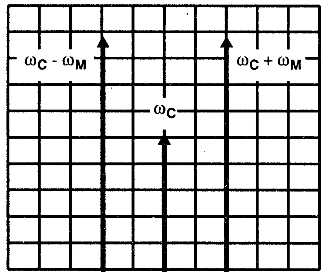


FIGURE 7A. UP CONVERSION OR SUPPRESSED CARRIER AM

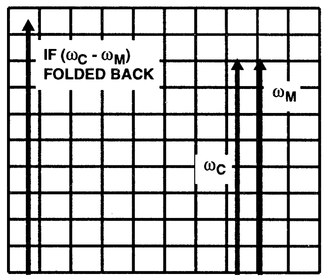


FIGURE 7B. DOWN CONVERSION

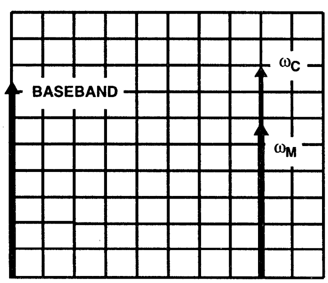


FIGURE 7C. ZERO IF OR DIRECT DOWN CONVERSION

FIGURE 7. MODULATOR FREQUENCY SPECTRUM

The use of the HFA3101 as modulators has several advantages when compared to its counterpart, the diode double-balanced mixer, in which it is required to receive enough energy to drive the diodes into a switching mode and has also some requirements depending on the frequency range desired, of different transformers to suit specific frequency responses. The HFA3101 requires very low driving capabilities for its carrier input and its frequency response is limited by the F_T of the devices, the design and the layout techniques being utilized.

Up conversion uses, for UHF transmitters for example, can be performed by injecting a modulating input in the range of 45MHz to 130MHz that carries the information often called IF (Intermediate frequency) for up conversion (The IF signal has been previously modulated by some modulation scheme from a baseband signal of audio or digital information) and by injecting the signal of a local oscillator of a much higher frequency range from 600MHz to 1.2GHz into the carrier input. Using the example of a 850MHz carrier input and a 70MHz IF, the output spectrum will contain a upper side band of 920MHz, a lower side band of 780MHz and some of the carrier (850MHz) and IF (70MHz) feedthrough. A Band pass filter at the output can attenuate the undesirable signals and the 920MHz signal can be routed to a transmitter RF power amplifier.

Down conversion, as the name implies, is the process used to translate a higher frequency signal to a lower frequency range conserving the modulation information contained in the higher frequency signal. One very common typical down conversion use for example, is for superheterodyne radio receivers where a translated lower frequency often referred as intermediate frequency (IF) is used for detection or demodulation of the baseband signal. Other application uses include down conversion for special filtering using frequency translation methods.

An oscillator referred as the local oscillator (LO) drives the upper quad transistors of the cell with a frequency called ω_C. The lower pair is driven by the RF signal of frequency ω_M to be translated to a lower frequency IF. The spectrum of the IF output will contain the sum and difference of the frequencies ω_C and ω_M. Notice that the difference can become negative when the frequency of the local oscillator is lower than the incoming frequency and the signal is folded back as in Figure 7.

NOTE: The acronyms RF, IF and LO are often interchanged in the industry depending on the application of the cell as mixers or modulators. The output of the cell also contains multiples of the frequency of the signal being fed to the upper quad pair of transistors because of the switching action equivalent to a square wave multiplication. In practice, however, not only the odd multiples in the case of a symmetrical square wave but some of the even multiples will also appear at the output spectrum due to the nature of the actual switching waveform and high frequency performance. By-products of the form $M^*\omega_C + N^*\omega_M$ with M and N being positive or negative integers are also expected to be present at the output and their levels are carefully examined and minimized by the design. This distortion is considered one of the figures of merit for a mixer application.

The process of frequency doubling is also understood by having the same signal being fed to both modulating and carrier ports. The output frequency will be the sum of ω_C and ω_M which is equivalent to the product of the input frequency by 2 and a zero Hz or DC frequency equivalent to the difference of ω_C and ω_M. Figure 7 also shows one technique in use today where a process of down conversion named zero IF is made by using a local oscillator with a very pure signal frequency equal to the incoming RF frequency signal that contains a baseband (audio or digital signal) modulation. Although complex, the extraction or detection of the signal is straightforward.

Another useful application of the HFA3101 is its use as a high frequency phase detector where the two signals are fed to the carrier and modulation ports and the DC information is extracted from its output. In this case, both ports are utilized in a switching mode or overdrive, such that the process of multiplication takes place in a quasi digital form (2 square waves). One application of a phase detector is frequency or phase demodulation where the FM signal is split before the modulating and carrier ports. The lower input port is always 90 degrees apart from the carrier input signal through a high Q tuned phase shift network. The network, being tuned for a precise 90 degrees shift at a nominal frequency, will set the two signals 90 degrees apart and a quiescent output DC level will be present at the output. When the input signal is frequency modulated, the phase shift of the signal coming from the network will deviate from 90 degrees proportional to the frequency deviation of the FM signal and a DC variation at the output will take place, resembling the demodulated FM signal.

The HFA3101 could also be used for quadrature detection, (I/Q demodulation), AGC control with limited range, low level multiplication to name a few other applications.

Biasing

Various biasing schemes can be employed for use with the HFA3101. Figure 8 shows the most common schemes. The biasing method is a choice of the designer when cost, thermal dependence, voltage overheads and DC balancing properties are taken into consideration.

Figure 8A shows the simplest form of biasing the HFA3101. The current source required for the lower pair is set by the voltage across the resistor R_{BIAS} less a V_{BE} drop of the lower transistor. To increase the overhead, collector resistors are substituted by a RF choke as the upper pair functions as a current source for AC signals. The bases of the upper and lower transistors are biased by RB1 and RB2 respectively. The voltage drop across the resistor R2 must be higher than a V_{BE} with an increase sufficient to assure that the collector to base junctions of the lower pair are always reverse biased. Notice that this same voltage also sets the V_{CE} of operation of the lower pair which is important for the optimization of gain. Resistors R_{EE} are nominally zero for applications where the input signals are well below 25mV peak. Resistors R_{EE} are used to increase the linearity of the circuit upon higher level signals. The drop across R_{EE} must be taken into consideration when setting the current source value.

Figure 8B depicts the use of a common resistor sharing the current through the cell which is used for temperature compensation as the lower pair V_{BE} drop at the rate of -2mV/^{o}C.

Figure 8C uses a split supply.

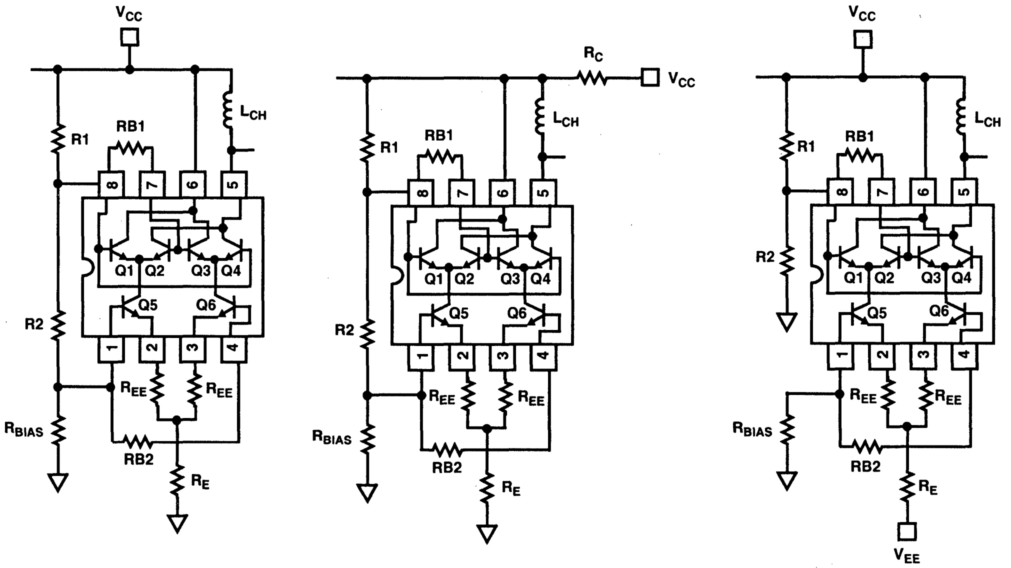


FIGURE 8A. FIGURE 8B. FIGURE 8C.

FIGURE 8.

Design Example: Down Converter Mixer

Figure 9 shows an example of a low cost mixer for cellular applications.

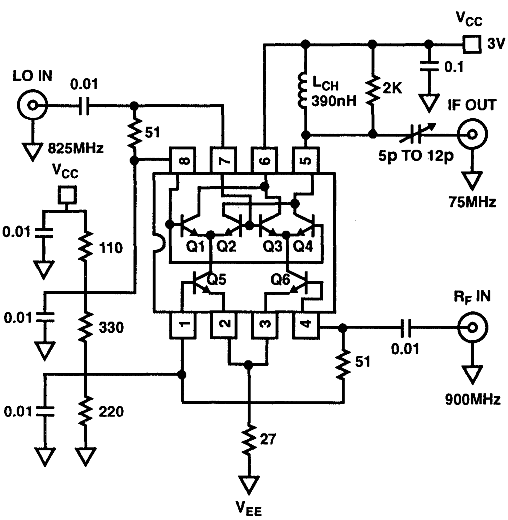


FIGURE 9. 3V DOWN CONVERTER APPLICATION

The design flexibility of the HFA3101 is demonstrated by a low cost, and low voltage mixer application at the 900MHz range. The choice of good quality chip components with their self resonance outside the boundaries of the application are important. The design has been optimized to accommodate the evaluation of the same layout for various quiescent current values and lower supply voltages. The choice of R_E became important for the available overhead and also for maintaining an AC true impedance for high frequency signals. The value of 27Ω has been found to be the optimum minimum for the application. The input impedances of the HFA3101 base input ports are high enough to permit their termination with 50Ω resistors. Notice the AC termination by decoupling the bias circuit through good quality capacitors.

The choice of the bias has been related to the available power supply voltage with the values of R1, R2 and R_{BIAS} splitting the voltages for optimum V_{CE} values. For evaluation of the cell quiescent currents, the voltage at the emitter resistor R_E has been recorded.

The gain of the circuit, being a function of the load and the combined emitter resistances at high frequencies have been kept to a maximum by the use of an output match network. The high output impedance of the HFA3101 permits broadband match if so desired at 50Ω (R_L = 50Ω to 2kΩ) as well as with tuned medium Q matching networks (L, T etc.).

Stability

The cell, by its nature, has very high gain and precautions must be taken to account for the combination of signal reflections, gain, layout and package parasitics. The rule of thumb of avoiding reflected waves must be observed. It is important to assure good matching between the mixer stage and its front end. Laboratory measurements have shown some susceptibility for oscillation at the upper quad transistors input. Any LO prefiltering has to be designed such the return loss is maintained within acceptable limits specially at high frequencies. Typical off the shelf filters exhibits very poor return loss for signals outside the passband. It is suggested that a "pad" or a broadband resistive network be used to interface the LO port with a filter. The inclusion of a parallel 2K resistor in the load decreases the gain slightly which improves the stability factor and also improves the distortion products (output intermodulation or 3rd order intercept). The employment of good RF techniques shall suffice the stability requirements.

Evaluation

The evaluation of the HFA3101 in a mixer configuration is presented in Figures 11 to Figure 16, Table 1 and Table 2. The layout is depicted in Figure 10.

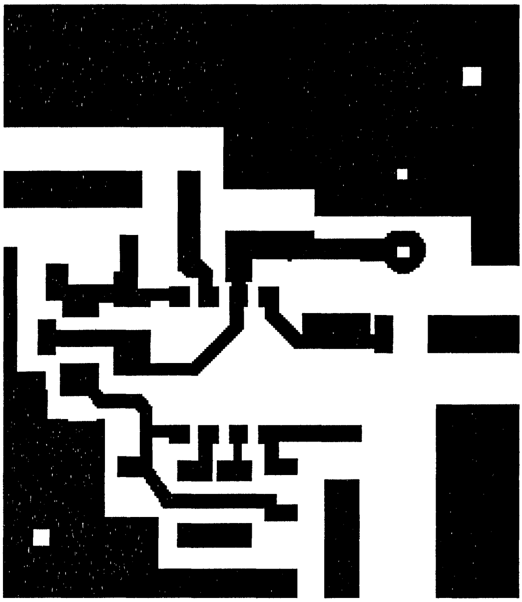


FIGURE 10. UP/DOWN CONVERTER LAYOUT, 400%. MATERIAL G10, 0.031

The output matching network has been designed from data taken at the output port at various test frequencies with the setup as in Table 1. S22 characterization is enough to assure the calculation of L, T or transmission line matching networks.

TABLE 1. S22 PARAMETERS FOR DOWN CONVERSION, $L_{CH} = 10\mu H$

FREQUENCY	RESISTANCE	REACTANCE
10MHz	265Ω	615Ω
45MHz	420Ω	- 735Ω
75MHz	122Ω	- 432Ω
100MHz	67Ω	- 320Ω

TABLE 2. S22 PARAMETERS FOR DOWN CONVERSION, $L_{CH} = 10\mu H$

PARAMETER	LO LEVEL	$V_{CC} = 3V$ $I_{BIAS} = 8mA$
Power Gain	-6dBm	8.5dB
TOI Output	-6dBm	11.5dBm
NF SSB	-6dBm	14.5dB
Power Gain	0dBm	8.6dB
TOI Output	0dBm	11dBm
NF SSB	0dBm	15dB

PARAMETER	LO LEVEL	$V_{CC} = 4V$ $I_{BIAS} = 19mA$
Power Gain	-6dBm	10dB
TOI Output	-6dBm	13dBm
NF SSB	-6dBm	20dB
Power Gain	0dBm	11dB
TOI Output	0dBm	12.5dBm
NF SSB	0dBm	24dB

TABLE 3. TYPICAL VALUES OF S22 FOR THE OUTPUT PORT. $L_{CH} = 390nH$ $I_{BIAS} = 8mA$ (SET UP OF FIGURE 11)

FREQUENCY	RESISTANCE	REACTANCE
300MHz	22Ω	-115Ω
600MHz	7.5Ω	-43Ω
900MHz	5.2Ω	-14Ω
1.1GHz	3.9Ω	0Ω

TABLE 4. TYPICAL VALUES OF S22. $L_{CH} = 390nH$, $I_{BIAS} = 18mA$

FREQUENCY	RESISTANCE	REACTANCE
300MHz	23.5Ω	-110Ω
600MHz	10.3Ω	-39Ω
900MHz	8.7Ω	-14Ω
1.1GHz	8Ω	0Ω

Up Converter Example

An application for a up converter as well as a frequency multiplier can be demonstrated using the same layout, with an addition of matching components. The output port S22 must be characterized for proper matching procedures and depending on the frequency desired for the output, transmission line transformations can be designed. The return loss of the input ports maintain acceptable values in excess of 1.2GHz which can permit the evaluation of a frequency doubler to 2.4GHz if so desired.

The addition of the resistors R_{EE} can increase considerably the dynamic range of the up converter as demonstrated at Figure 18. The evaluation results depicted in Table 5 have been obtained by a triple stub tuner as a matching network for the output due to the layout constraints. Based on the evaluation results it is clear that the cell requires a higher Bias current for overall performance.

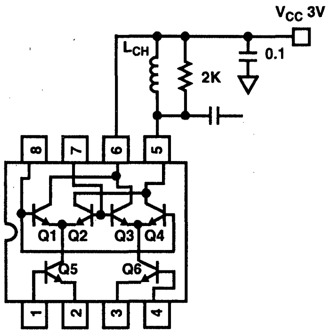


FIGURE 11. OUTPUT PORT S22 TEST SET UP

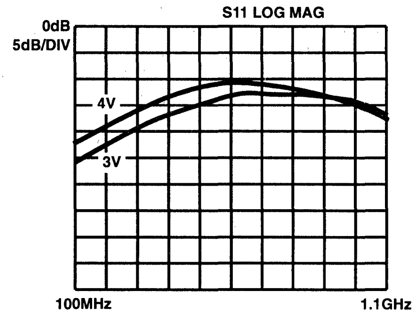


FIGURE 12. LO PORT RETURN LOSS

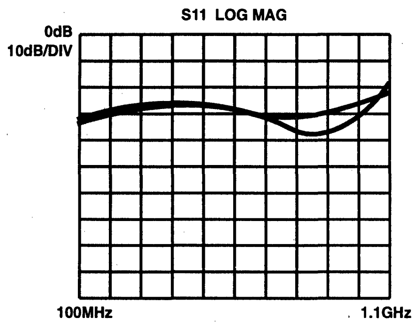


FIGURE 13. RF PORT RETURN LOSS

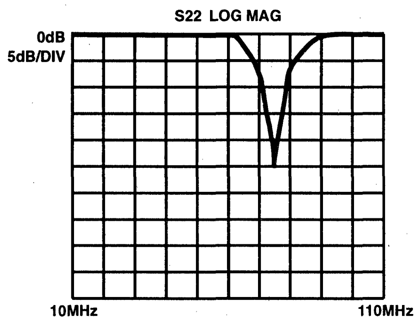


FIGURE 14. IF PORT RETURN LOSS, WITH MATCHING NETWORK

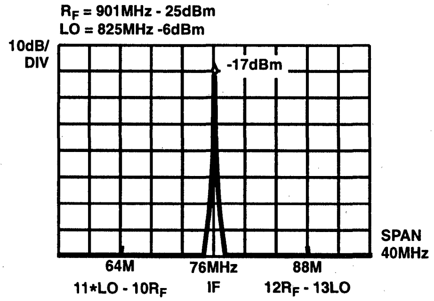


FIGURE 15. TYPICAL IN BAND OUTPUT SPECTRUM, V_{CC} = 3V

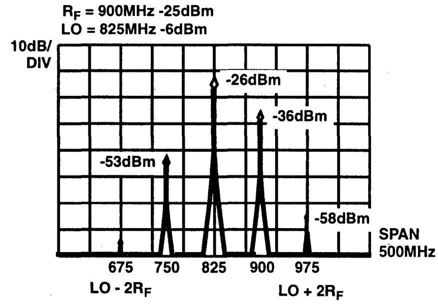


FIGURE 16. TYPICAL OUT OF BAND OUTPUT SPECTRUM

Design Example: Up Converter Mixer

Figure 17 shows an example of a up converter for cellular applications.

Conclusion

The HFA3101 offers the designer a number of choices and different applications as a powerful RF building block. Although isolation is degraded from the theoretical results for the cell due to the unbalanced, nondifferential input schemes being used, a number of advantages can be taken into consideration like cost, flexibility, low power and small outline when deciding for a design.

TABLE 5. TYPICAL PARAMETERS FOR AN UP CONVERTER EXAMPLE

PARAMETER	V_{CC} = 3V I_{BIAS} = 8mA	V_{CC} = 4V I_{BIAS} = 18mA
Power Gain, LO = -6dBm	3dB	5.5dBm
Power Gain, LO = 0dBm	4dB	7.2dB
R_F Isolation, LO = 0dBm	15dBc	22dBc
LO Isolation, LO = 0dBm	28dBc	28dBc

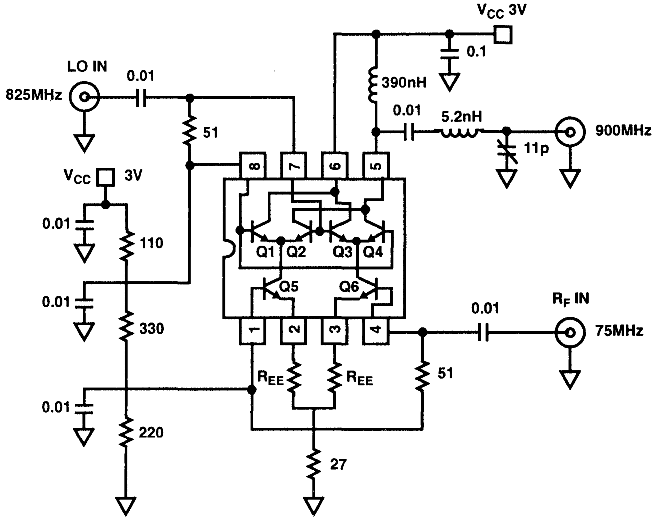


FIGURE 17.

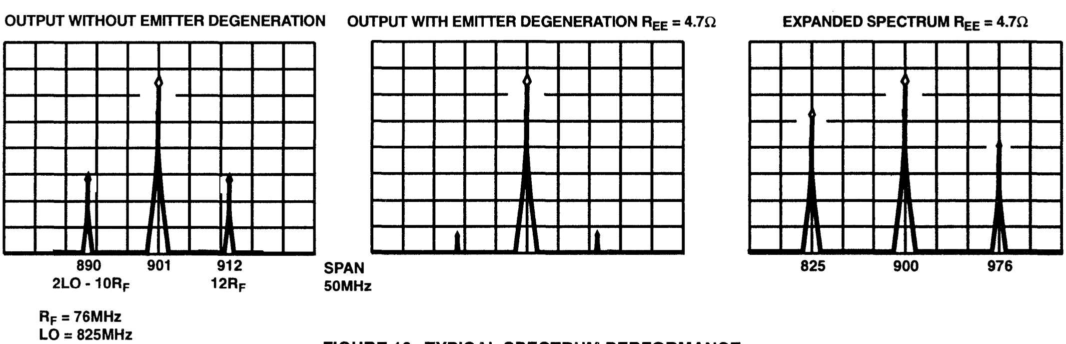


FIGURE 18. TYPICAL SPECTRUM PERFORMANCE

HARRIS SEMICONDUCTOR

HFA3102

August 1994

Dual Long-Tailed Pair Transistor Array

Features

- High Gain-Bandwidth Product (f_T) 10GHz
- High Power Gain-Bandwidth Product 5GHz
- High Current Gain (h_{FE}) 70
- Noise Figure (Transistor) 3.5dB
- Low Collector Leakage Current . . . . <0.01nA
- Excellent h_{FE} and V_{BE} Matching
- Pin-to-Pin to UPA102G

Applications

- Single Balanced Mixers
- Wide Band Amplification Stages
- Differential Amplifiers
- Multipliers
- Automatic Gain Control Circuits
- Frequency Doublers, Tripplers
- Oscillators
- Constant Current Sources
- Wireless Communication Systems
- Radio and Satellite Communications
- Fiber Optic Signal Processing
- High Performance Instrumentation

Description

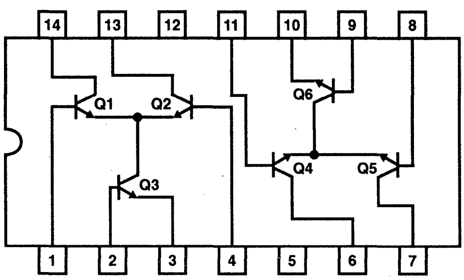
The HFA3102 is an all NPN transistor array configured as dual differential amplifiers with tail transistors. Based on Harris bonded wafer UHF-1 SOI process, this array achieves very high f_T (10GHz) while maintaining excellent h_{FE} and V_{BE} matching characteristics over temperature. Collector leakage currents are maintained to under 0.01nA.

Ordering Information

PART NUMBER	PRODUCT DESCRIPTION
HFA3102Y	Die
HFA3102B	14 Lead Plastic SOIC (N)
HFA3102B96	14 Lead Plastic SOIC (N) - Tape and Reel

Pinout/Functional Diagram

HFA3102
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 3635.1

Absolute Maximum Ratings

V_{CEO} Collector to Emitter Voltage 8.0V
V_{CBO} Collector to Base Voltage 12.0V
V_{EBO} Emitterr to Base Voltage 12.0V
I_C, Collector Current 30mA
T_{STG}, Storage Temperature Range .... -65°C to +150°C
Operating Temperature Range .... -40°C to +85°C
T_J, Junction Temperature (Die) .... +175°C
T_J, Junction Temperature (Plastic Package) .... +150°C
Lead Temperature (Soldering 10s) .... +300°C
(Lead Tips Only)

Thermal Information

Thermal Resistance θ_{JA}
Plastic SOIC Package .... 125°C/W
Maximum Package Power Dissipation at +75°C
Any One Transistor 0.25W
Plastic SOIC Package 0.6W
Derating Factor Above +75°C
Plastic SOIC Package .... 8mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications at +25°C

SYMBOLS	PARAMETER	TEST CONDITIONS	TEST LEVEL	ALL GRADES MIN	TYP	MAX	UNITS
$V_{(BR)CBO}$	Collector-to-Base Breakdown Voltage (Q_1, Q_2, Q_4, and Q_5)	$I_C = 100\mu A$, $I_E = 0$	A	12	18	-	V
$V_{(BR)CEO}$	Collector-to-Emitter Breakdown Voltage (Q_1 thru Q_6)	$I_C = 100\mu A$, $I_B = 0$	A	8	12	-	V
$V_{(BR)EBO}$	Emitter-to-Base Breakdown Voltage (Q_3 and Q_6)	$I_E = 50\mu A$, $I_C = 0$	A	5.5	6	-	V
I_{CBO}	Collector Cutoff Current (Q_1, Q_2, Q_4, and Q_5)	$V_{CB} = 5V$, $I_E = 0$	A	-	0.1	10	nA
I_{EBO}	Emitter Cutoff Current (Q_3 and Q_6)	$V_{EB} = 1V$, $I_C = 0$	A	-	-	100	nA
h_{FE}	DC Current Gain (Q_1 thru Q_6)	$I_C = 10mA$, $V_{CE} = 3$ V	A	40	70	-	-
C_{CB}	Collector-to-Base Capacitance	$V_{CB} = 5V$, f = 1MHz	B	-	300	-	fF
C_{EB}	Emitter-to-Base Capacitance	$V_{EB} = 0$, f = 1MHz	B	-	200	-	fF
f_T	Current Gain-Bandwidth Product	$I_C = 10mA$, $V_{CE} = 5V$	C	-	10	-	GHz
f_{MAX}	Power Gain-Bandwidth Product	$I_C = 10mA$, $V_{CE} = 5V$	C	-	5	-	GHz
G_{NFMIN}	Available Gain at Minimum Noise Figure	$I_C = 3mA$, $V_{CE} = 3$	C	-	-	-	-
		f = 0.5GHz	-	-	17.5	-	dB
		f = 1.0GHz	-	-	12.4	-	-
NF_{MIN}	Minimum Noise Figure	$I_C = 3mA$, $V_{CE} = 3V$	C	-	-	-	-
		f = 0.5GHz	-	-	1.8	-	dB
		f = 1.0GHz	-	-	2.1	-	-
$NF_{50\Omega}$	50Ω Noise Figure	$I_C = 3mA$, $V_{CE} = 3V$	C	-	-	-	-
		f = 0.5GHz	-	-	3.3	-	dB
		f = 1.0GHz	-	-	3.5	-	-
h_{FE1}/h_{FE2}	DC Current Gain Matching (Q_1 and Q_2, Q_4 and Q_5)	$V_{CE} = 3V$, $I_C = 10mA$	A	0.9	1.0	1.1	-
V_{OS}	Input Offset Voltage (Q_1 and Q_2), (Q_4 and Q_5)	$I_C = 10mA$, $V_{CE} = 3V$	A	-	1.5	5	mV
I_{OS}	Input Offset Current (Q_1 and Q_2), (Q_4 and Q_5)	$I_C = 10mA$, $V_{CE} = 3V$	A	-	5	25	µA
dV_{OS}/dT	Input Offset Voltage TC (Q_1 and Q_2, Q_4 and Q_5)	$I_C = 10mA$, $V_{CE} = 3V$	C	-	0.5	-	µV/°C
$I_{TRENCH-LEAKAGE}$	Collector-to-Collector Leakage (Pin 6, 7, 13, and 14)	$\Delta V_{TEST} = 5V$	B	-	0.01	-	nA

Test Level: A. Production Tested B. Guaranteed Limit or Typical Based on Characterization C. Design Typical for Information Only

Performance Curves

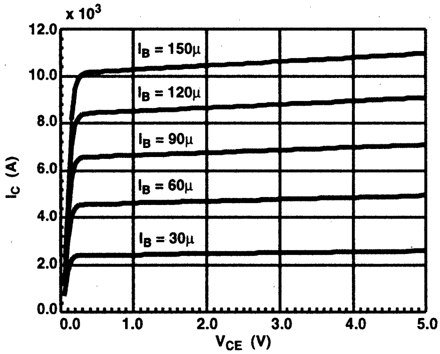


FIGURE 1. I_C vs V_{CE}

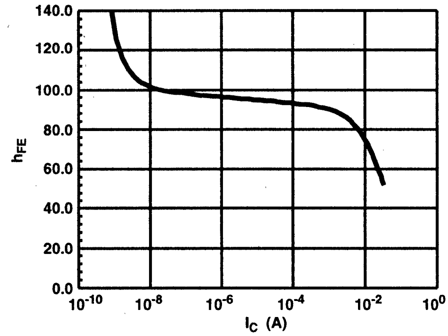


FIGURE 2. h_{FE} vs I_C

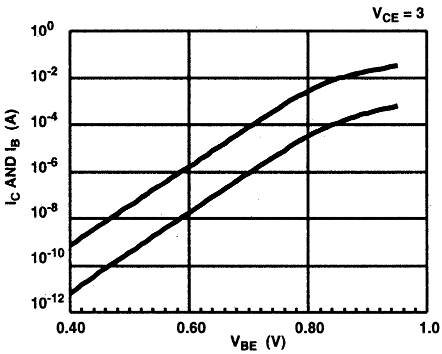


FIGURE 3. GUMMEL PLOT

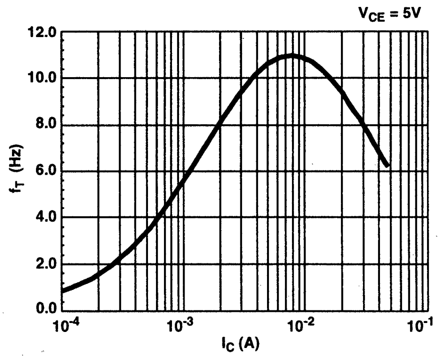


FIGURE 4. f_T vs I_C

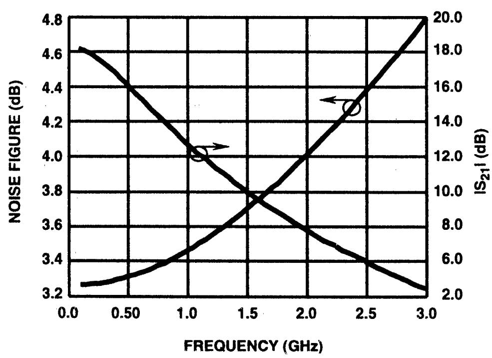


FIGURE 5. GAIN AND NOISE FIGURE vs FREQUENCY

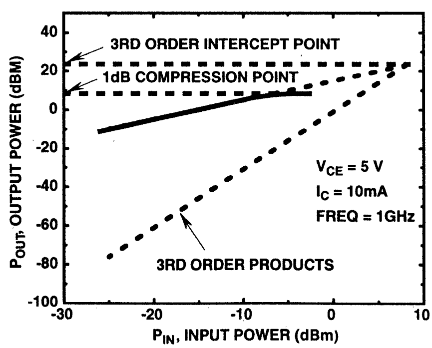


FIGURE 6. P_{1dB} AND 3RD ORDER INTERCEPT

PSPICE Model for a Single Transistor

```
+ ( IS= 1.840E-16   XTI= 3.000E+00   EG= 1.110E+00   VAF= 7.200E+01
+ VAR= 4.500E+00   BF= 1.036E+02   ISE= 1.686E-19   NE= 1.400E+00
+ IKF= 5.400E-02   XTB= 0.000E+00   BR= 1.000E+01   ISC= 1.605E-14
+ NC= 1.800E+00   IKR= 5.400E-02   RC= 1.140E+01   CJC= 3.980E-13
+ MJC= 2.400E-01   VJC= 9.700E-01   FC= 5.000E-01   CJE= 2.400E-13
+ MJE= 5.100E-01   VJE= 8.690E-01   TR= 4.000E-09   TF= 10.51E-12
+ ITF= 3.500E-02   XTF= 2.300E+00   VTF= 3.500E+00   PTF= 0.000E+00
+ XCJC= 9.000E-01   CJS= 1.689E-13   VJS= 9.982E-01   MJS= 0.000E+00
+ RE= 1.848E+00   RB= 5.007E+01   RBM= 1.974E+00   KF= 0.000E+00
+ AF= 1.000E+00)
```

Common Emitter S-Parameters

V_{CE} = 5V and I_C = 5mA

FREQ. (Hz)	|S11|	PHASE(S11)	|S12|	PHASE(S12)	|S21|	PHASE(S21)	|S22|	PHASE(S22)
1.0E+08	0.833079	-11.7873	1.418901E-02	78.8805	11.0722	168.576	0.976833	-11.0509
2.0E+08	0.791776	-22.8290	2.695740E-02	68.6355	10.5177	157.897	0.930993	-21.3586
3.0E+08	0.734911	-32.6450	3.750029E-02	59.5861	9.75379	148.443	0.868128	-30.4451
4.0E+08	0.672811	-41.0871	4.572138E-02	51.9018	8.91866	140.361	0.799886	-38.1641
5.0E+08	0.612401	-48.2370	5.194147E-02	45.5043	8.10511	133.569	0.734033	-44.5998
6.0E+08	0.557126	-54.2780	5.659943E-02	40.2112	7.35944	127.882	0.674392	-49.9370
7.0E+08	0.508133	-59.4102	6.009507E-02	35.8226	6.69712	123.102	0.622181	-54.3777
8.0E+08	0.465361	-63.8123	6.274213E-02	32.1594	6.11750	119.047	0.577269	-58.1022
9.0E+08	0.428238	-67.6313	6.477134E-02	29.0743	5.61303	115.571	0.538952	-61.2587
1.0E+09	0.396034	-70.9834	6.634791E-02	26.4506	5.17405	112.556	0.506365	-63.9647
1.1E+09	0.368032	-73.9591	6.758932E-02	24.1974	4.79104	109.913	0.478663	-66.3116
1.2E+09	0.343589	-76.6285	6.857937E-02	22.2441	4.45546	107.570	0.455091	-68.3702
1.3E+09	0.322155	-79.0462	6.937837E-02	20.5358	4.15997	105.472	0.435008	-70.1958
1.4E+09	0.303268	-81.2548	7.003020E-02	19.0293	3.89845	103.576	0.417872	-71.8314
1.5E+09	0.286542	-83.2880	7.056718E-02	17.6908	3.66577	101.849	0.403238	-73.3108
1.6E+09	0.271660	-85.1723	7.101343E-02	16.4930	3.45770	100.262	0.390735	-74.6609
1.7E+09	0.258359	-86.9292	7.138717E-02	15.4143	3.27074	98.7956	0.380056	-75.9030
1.8E+09	0.246420	-88.5759	7.170231E-02	14.4370	3.10197	97.4307	0.370947	-77.0544
1.9E+09	0.235659	-90.1265	7.196964E-02	13.5469	2.94897	96.1533	0.363195	-78.1288
2.0E+09	0.225923	-91.5925	7.219757E-02	12.7319	2.80969	94.9515	0.356623	-79.1377
2.1E+09	0.217085	-92.9836	7.239274E-02	11.9824	2.68243	93.8156	0.351081	-80.0903
2.2E+09	0.209034	-94.3076	7.256046E-02	11.2901	2.56573	92.7373	0.346442	-80.9942
2.3E+09	0.201678	-95.5713	7.270498E-02	10.6480	2.45837	91.7097	0.342599	-81.8557
2.4E+09	0.194939	-96.7803	7.282977E-02	10.0503	2.35928	90.7271	0.339458	-82.6802
2.5E+09	0.188747	-97.9395	7.293764E-02	9.49212	2.26756	89.7844	0.336942	-83.4719
2.6E+09	0.183044	-99.0530	7.303093E-02	8.96908	2.18243	88.8775	0.334982	-84.2347
2.7E+09	0.177780	-100.124	7.311157E-02	8.47753	2.10322	88.0026	0.333518	-84.9716
2.8E+09	0.172909	-101.156	7.318117E-02	8.01430	2.02934	87.1565	0.332499	-85.6853
2.9E+09	0.168394	-102.152	7.324107E-02	7.57661	1.96027	86.3366	0.331879	-86.3781
3.0E+09	0.164200	-103.114	7.329243E-02	7.16204	1.89556	85.5404	0.331620	-87.0518

V_{CE} = 5V and I_C = 10mA

FREQ. (Hz)	|S11|	PHASE(S11)	|S12|	PHASE(S12)	|S21|	PHASE(S21)	|S22|	PHASE(S22)
1.0E+08	0.728106	-16.4319	1.273920E-02	75.4177	15.1273	165.227	0.959692	-14.2688
2.0E+08	0.670836	-31.2669	2.342300E-02	62.8941	13.9061	152.045	0.886232	-26.9507
3.0E+08	0.600268	-43.7663	3.132521E-02	52.5891	12.3970	141.185	0.796016	-37.3172
4.0E+08	0.531768	-54.0028	3.681579E-02	44.5019	10.9257	132.570	0.708892	-45.4503
5.0E+08	0.471795	-62.3880	4.057046E-02	38.2308	9.62995	125.781	0.633146	-51.7704
6.0E+08	0.421506	-69.3569	4.316292E-02	33.3405	8.53559	120.378	0.570209	-56.7206
7.0E+08	0.379961	-75.2612	4.499071E-02	29.4764	7.62375	116.005	0.518803	-60.6598
8.0E+08	0.345693	-80.3608	4.631140E-02	26.3755	6.86423	112.398	0.476987	-63.8540
9.0E+08	0.317301	-84.8420	4.728948E-02	23.8481	6.22797	109.365	0.442915	-66.4948
1.0E+09	0.293608	-88.8381	4.803091E-02	21.7581	5.69057	106.771	0.415044	-68.7193
1.1E+09	0.273680	-92.4452	4.860515E-02	20.0070	5.23257	104.518	0.392146	-70.6269
1.2E+09	0.256782	-95.7336	4.905871E-02	18.5224	4.83873	102.532	0.373261	-72.2899
1.3E+09	0.242344	-98.7555	4.942344E-02	17.2505	4.49716	100.759	0.357640	-73.7620
1.4E+09	0.229918	-101.551	4.972158E-02	16.1506	4.19854	99.1602	0.344698	-75.0832
1.5E+09	0.219152	-104.150	4.996903E-02	15.1915	3.93554	97.7028	0.333974	-76.2840
1.6E+09	0.209767	-106.577	5.017730E-02	14.3490	3.70234	96.3629	0.325102	-77.3877
1.7E+09	0.201539	-108.851	5.035491E-02	13.6040	3.49428	95.1215	0.317789	-78.4122
1.8E+09	0.194288	-110.988	5.050825E-02	12.9411	3.30758	93.9633	0.311800	-79.3715
1.9E+09	0.187867	-113.001	5.064218E-02	12.3482	3.13919	92.8761	0.306940	-80.2768
2.0E+09	0.182157	-114.902	5.076045E-02	11.8151	2.98658	91.8500	0.303051	-81.1365
2.1E+09	0.177056	-116.698	5.086598E-02	11.3338	2.84766	90.8766	0.300003	-81.9578
2.2E+09	0.172484	-118.399	5.096107E-02	10.8974	2.72068	89.9494	0.297686	-82.7460
2.3E+09	0.168370	-120.012	5.104755E-02	10.5001	2.60420	89.0626	0.296007	-83.5057
2.4E+09	0.164656	-121.542	5.112690E-02	10.1373	2.49697	88.2115	0.294889	-84.2405
2.5E+09	0.161293	-122.996	5.120031E-02	9.80479	2.39793	87.3920	0.294266	-84.9533
2.6E+09	0.158239	-124.378	5.126876E-02	9.49919	2.30619	86.6007	0.294081	-85.6466
2.7E+09	0.155458	-125.694	5.133304E-02	9.21750	2.22098	85.8348	0.294285	-86.3223
2.8E+09	0.152919	-126.947	5.139381E-02	8.95716	2.14162	85.0916	0.294836	-86.9822
2.9E+09	0.150595	-128.140	5.145164E-02	8.71595	2.06753	84.3690	0.295696	-87.6275
3.0E+09	0.148463	-129.279	5.150697E-02	8.49194	1.99820	83.6651	0.296834	-88.2595

Die Characteristics

PROCESS:
UHF-1

DIE DIMENSIONS:
53 x 52 x 14 ±1mils
1340μm x 1320μm x 355.6μm ± 25.4μm

METALIZATION:
Type: Metal 1: AlCu(2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.5kÅ
Type: Metal 2: AlCu(2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

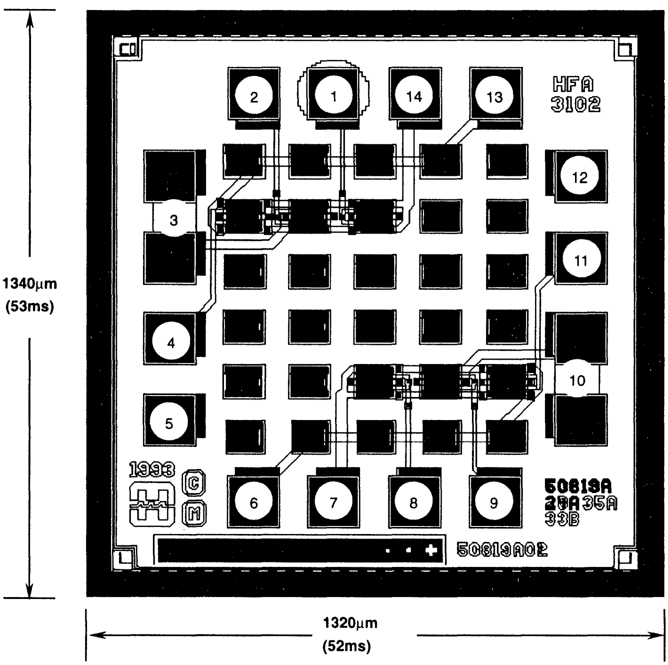
GLASSIVATION:
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

DIE ATTACH:
Material: Epoxy

WORST CASE CURRENT DENSITY:
1.50×10^5 A/cm^2

Metallization Mask Layout

HFA3102
TOP VIEW



Pad numbers correspond to the 14 pin SOIC pinout.

HARRIS SEMICONDUCTOR

HFA3600

March 1995

Low-Noise Amplifier/Mixer

Features

- **LNA**
  - **Low Noise Figure . . . . 2.3dB at 900MHz**
  - **High Power Gain. . . . . 12.8dB at 900MHz**
  - **High Intercept . . . . +12.8dBm at Output**
- **MIXER**
  - **Low Noise Figure . . . . 12.1dB at 900MHz**
  - **High Power Gain. . . . . 7.0dB at 900MHz**
  - **High Intercept . . . . +3.2dBm at Output**
  - **Low LO Drive . . . . - 3dBm**
- **LNA + MIXER**
  - **Low Noise Figure . . . . 3.97dB at 900MHz**
  - **High Power Gain. . . . . 19.8dB at 900MHz**
  - **High Intercept . . . . -16.7dBm at Input**
  - **Low Operating Power 5V/11.3mA**
  - **Low Shutdown Power 5V/250μA**
  - **Small Package: 14 Lead SOIC (Plastic, Small Outline Package, 150 Mil Width, 50 Mil Lead Spacing)**

Applications

- **Portable Cellular Telephone (AMPS, IS-54, GSM, JDC)**
- **Wireless Data Com. (ISM, Narrowband PCS)**
- **UHF and Mobile Radio Receiver**
- **900MHz Digital Cordless Telephone (CT-2, ISM)**
- **Wireless Telemetry**

Description

The HFA3600 is a silicon Low-Noise Amplifier with high performance characteristics allowing the design of very sensitive, wide dynamic-range 900MHz receivers with minimal external components.

The LNA, Mixer RF, and LO inputs are internally matched to 50Ω. The Mixer IF output is open collector allowing flexibility in choosing the IF output impedance, with 1000Ω operation fully characterized. The mixer performance is optimized for low LO drive (-3dBm) applications.

Power consumption is kept to a minimum, making the device ideal for battery-powered hand-held communication equipment. An integrated power-down feature maximizes battery life and eliminates the need for external shut down circuitry. Although fully characterized under 5V single supply, the HFA3600 is operable down to 4V with slight performance differences.

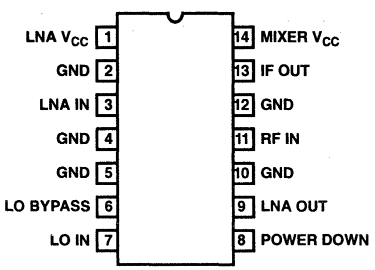
The HFA3600 is part of a complete solution including application circuit schematics, S-parameters, noise figure, third-order intercept characterization data and PC board artwork. Evaluation boards are also available through local Harris Sales offices.

Ordering Information

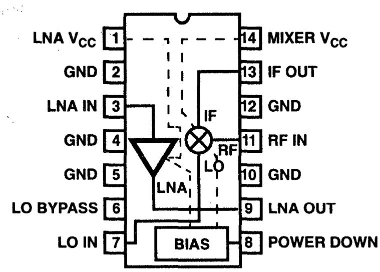
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA3600IB	-40°C to +85°C	14 Lead Plastic SOIC (N)
HFA3600IB96	-40°C to +85°C	14 Lead Plastic SOIC (N) in Tape and Reel

Pinout

HFA3600 (SOIC)
TOP VIEW



Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC handling procedures.

File Number **3655.2**

Absolute Maximum Ratings

Supply Voltage . . . . -0.3 to +6.0V
Voltage on Any Other Pin . . . . -0.3 to V_{CC}+0.3V
V_{CC} to V_{CC} Decouple . . . . -0.3 to +0.3V
Any GND to GND . . . . -0.3 to +0.3V
Package Power Dissipation at 25°C. 1W
Junction Temperature (Plastic Package) . . . . +150°C

Operating Conditions

Thermal Resistance θ_{JA}
SOIC Package. . . . . 125°C/W
Operating Temperature Range . . . . -40°C ≤ T_A ≤ +85°C
Storage Temperature Range. . . . . -65°C ≤ T_A ≤ +150°C
Lead Temperature (Soldering 10s) . . . . +300°C
(Lead Tips Only)
Supply Voltage Range. . . . . 4.0 to 5.5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

SYMBOL	PARAMETER	CONDITION	TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
I_{CC}	Total Supply Current at 5V	Normal PD = 2V	A	+25°C	-	11.3	12.5	mA
		Shutdown PD=0.8V	A	+25°C	-	250	375	µA
V_{IH}	Shutdown Logic High	Normal Mode	A	+25°C	2	-	V_{CC}	V
V_{IL}	Shutdown Logic Low	Shutdown Mode	A	+25°C	-0.3	-	0.8	V
I_{IL}	Shutdown Input Current	PD = 0.4V	A	+25°C	-200	-150	-100	µA
I_{IH}	Shutdown Input Current	PD = 2.4V	A	+25°C	-45	-24	-3	µA
V_{LNA-IN}	LNA Input DC Level	Normal Mode	A	+25°C	-	0.79	-	V
		Shutdown Mode	A	+25°C	-	0.0	-	V
$V_{LNA-OUT}$	LNA Output DC Level	Normal Mode	A	+25°C	-	4.9	-	V
		Shutdown Mode	A	+25°C	-	5.0	-	V
V_{MX-RF}	Mixer RFIN DC Level	Normal Mode	A	+25°C	-	0.79	-	V
		Shutdown Mode	A	+25°C	-	0.0	-	V
V_{MX-LO}	Mixer LO_{IN} DC Level	Normal Mode	A	+25°C	-	2.1	-	V
		Shutdown Mode	A	+25°C	-	0.0	-	V
$t_{OFF, ON}$	Shutdown On-Off-On Time		B	+25°C	-	10	-	µs

AC Electrical Specifications

All Characterization Results have been Obtained with the Use of a Standard Evaluation Board.

SYMBOL	PARAMETER	TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
LNA (V_{CC} = +5V, T_A = +25°C, Test Figure 1 and f = 900MHz Unless Otherwise Noted In Characterization Curves)							
S_{21LNA}	LNA Gain	B	+25°C	11.8	12.8	13.8	dB
S_{12LNA}	LNA Reverse Isolation	B	+25°C	-	23	-	dB
S_{11LNA}	LNA Input Return Loss	B	+25°C	6.0	7.3	-	dB
S_{22LNA}	LNA Output Return Loss	B	+25°C	10.0	13.0	-	dB
$P_{-1dBLNA}$	LNA Output 1-dB Gain Compression Point	B	+25°C	-	-2.0	-	dBm
IP_{3LNA}	LNA Output 3rd-Order Intercept	B	+25°C	+11.2	+12.8	-	dBm
NF_{LNA}	LNA Noise Figure	B	+25°C	-	2.30	2.60	dB
MIXER (V_{CC} = 5V, T_A = +25°C, f_{LO} = 825MHz at -3dBm, f_{RF} = 900MHz, f_{IF} = 75MHz and Test Figure 1, Unless Otherwise Noted)							
PG_C	MIXER Power Conversion Gain	B	+25°C	5.9	7.0	8.1	dB
S_{11RF}	MIXER RF Input Return Loss	B	+25°C	8.0	11.0	-	-
S_{11LO}	MIXER LO Input Return Loss	B	+25°C	18.0	26	-	dB
NF_{MIXER}	MIXER SSB Noise Figure	B	+25°C	-	12.1	13.9	dB
$P_{-1dBMIX}$	MIXER Output 1-dB Gain Compression	B	+25°C	-	-7.5	-	dBm
IP_{3MIX}	MIXER Output 3rd-Order Intercept	B	+25°C	+1.0	+3.2	-	dBm
C_{OUTMIX}	MIXER IF Output Capacitance	B	+25°C	-	2.3	-	pF

AC Electrical Specifications All Characterization Results have been Obtained with the Use of a Standard Evaluation Board. **(Continued)**

SYMBOL	PARAMETER	TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
$G_{RF\text{-}IF}$	MIXER RF-IF Isolation (Includes Matching Network)	B	+25°C	-	25	-	dB
$G_{LO\text{-}IF}$	MIXER LO-IF Isolation (Includes Matching Network)	B	+25°C	-	16	-	dB
$G_{LO\text{-}RF}$	MIXER LO-RF Isolation	B	+25°C	16	21	-	dB
$G_{LO\text{-}LNAIN}$	Mixer LO-LNA_{IN} Isolation	B	+25°C	42	50	-	dB
$G_{LNAOUT\text{-}RF}$	LNAOUT-Mixer RFIN Isolation	B	+25°C	35	40	-	dB
(LNA + MIXER) V_{CC} = 5V, T_A = +25°C, f_{LO} = 825MHz at -3dBm, f_{RF} = 900MHz, f_{IF} = 75MHz and Idealized Lossless External Filters							
CPG_C	Power Conversion Gain	B	+25°C	-	19.8	-	dB
CNF	Noise Figure	B	+25°C	-	3.97	-	dB
CIP_3	Input 3rd-Order Intercept	B	+25°C	-	-16.7	-	dBm

NOTE:

Test Level: A. Production Tested.
B. Guaranteed Limit or Typical Based on Characterization.

Test Circuits

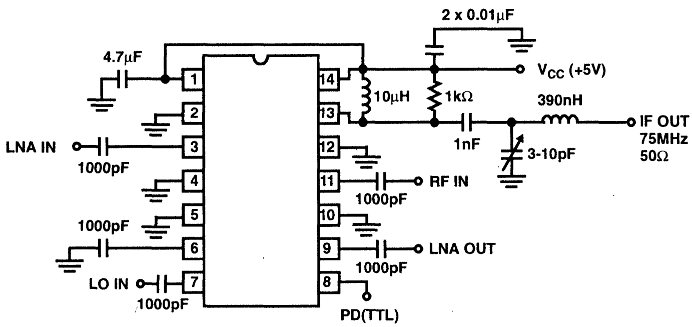


FIGURE 1. EVALUATION TEST CIRCUIT

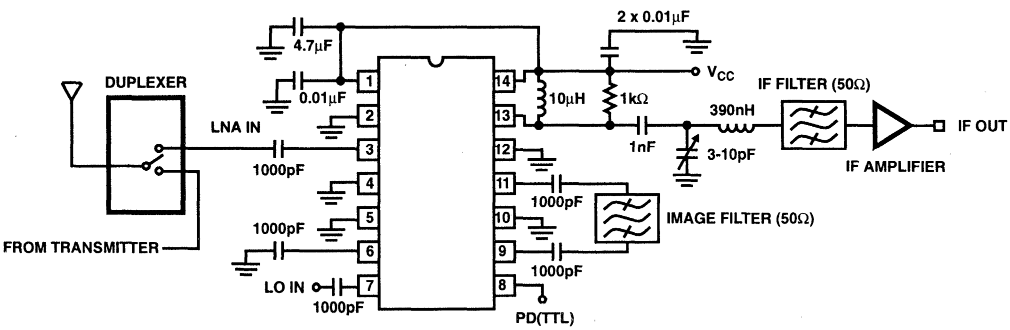


FIGURE 2. TYPICAL APPLICATION CIRCUIT

TABLE 1. TYPICAL CELLULAR FRONT-END CASCADED PERFORMANCE

	DUPLEXER	LNA	IMAGE FILTER	MIXER	IF FILTER	IF AMP	UNITS
Noise Figure	3.0	2.3	3.0	12.1	8.0	3.0	dB
Gain	-3.0	12.8	-3.0	7.0	-8.0	20.0	dB
OUTPUT IP3	100.0	12.8	100.0	3.2	Not Applicable (Note)		dBm
Cascaded Noise Figure = 8.55dB			Cascaded Gain = 25.8dB			Input IP3 = -10.8dBm	

NOTE: Cascaded results are using 100.0dBm for IP3

Supply Characteristics

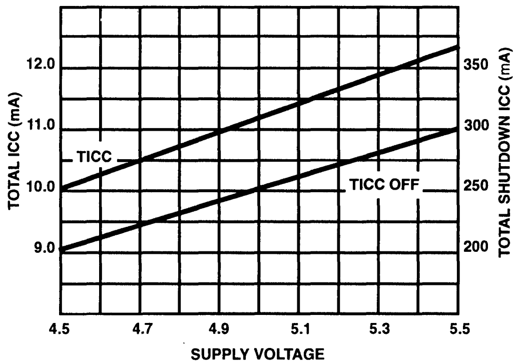


FIGURE 3. TOTAL ICC vs SUPPLY VOLTAGE

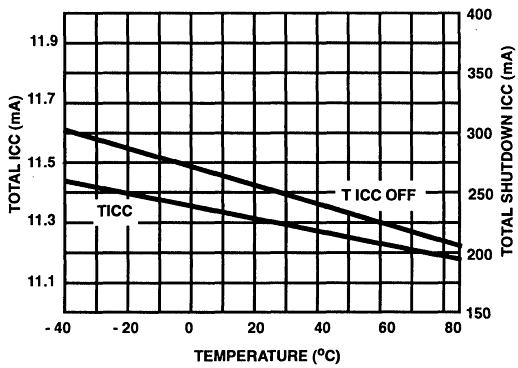


FIGURE 4. TOTAL ICC vs TEMPERATURE

LNA Characteristics

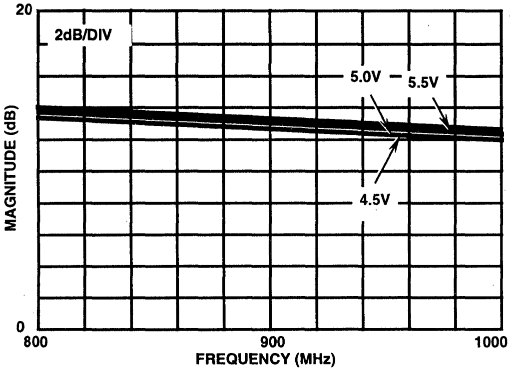


FIGURE 5. LNA S21 vs FREQUENCY AND V_{CC}

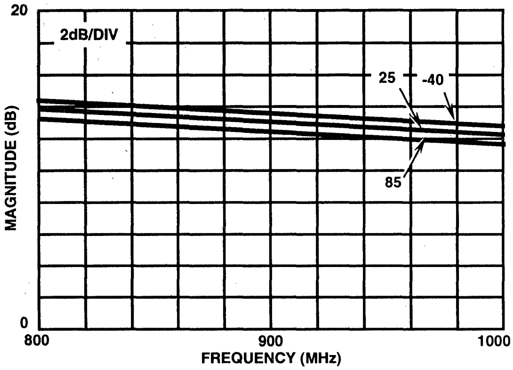


FIGURE 6. LNA S21 vs FREQUENCY AND TEMPERATURE

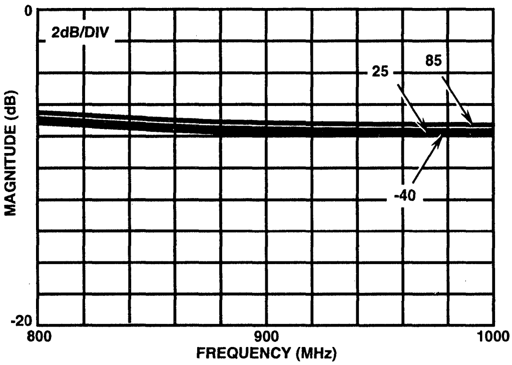


FIGURE 7. LNA S11 vs FREQUENCY AND TEMPERATURE

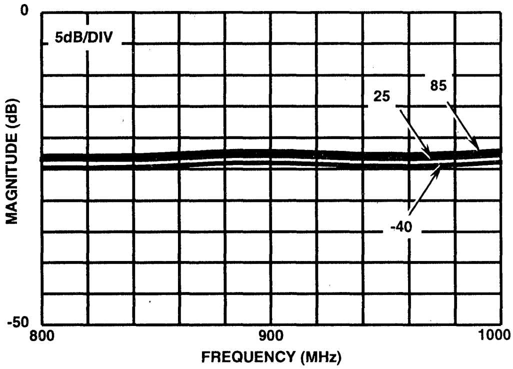


FIGURE 8. LNA S12 vs FREQUENCY AND TEMPERATURE

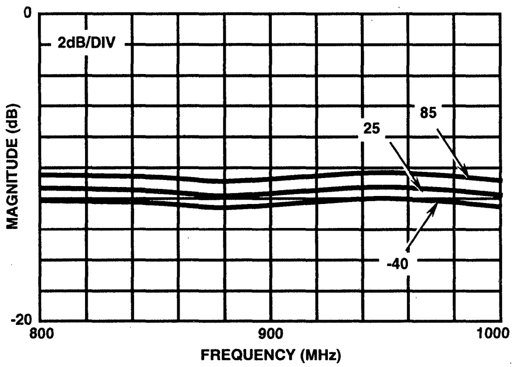


FIGURE 9. LNA S22 vs FREQUENCY AND TEMPERATURE

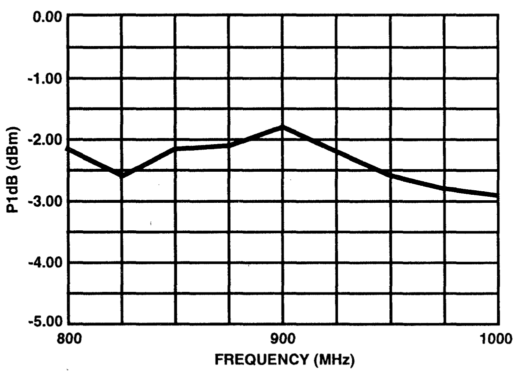


FIGURE 10. LNA OUTPUT 1dB COMPRESSION vs FREQUENCY

LNA Characteristics (Continued)

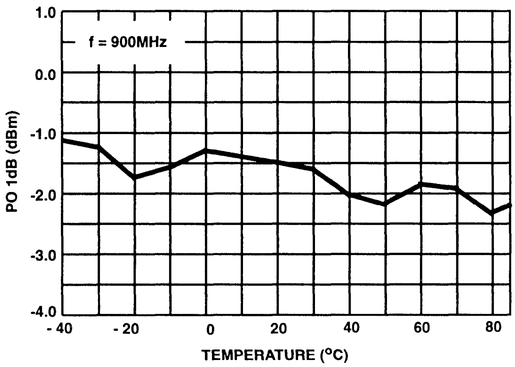


FIGURE 11. LNA OUTPUT 1DB COMPRESSION vs TEMPERATURE

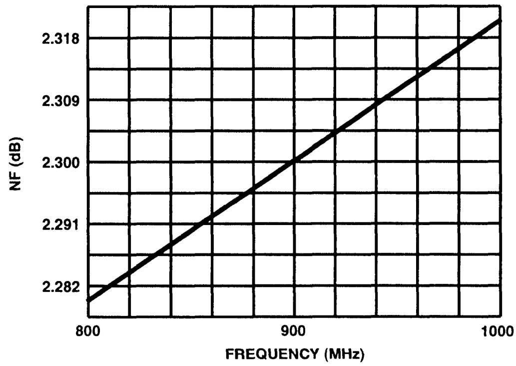


FIGURE 12. LNA 50Ω NF vs FREQUENCY

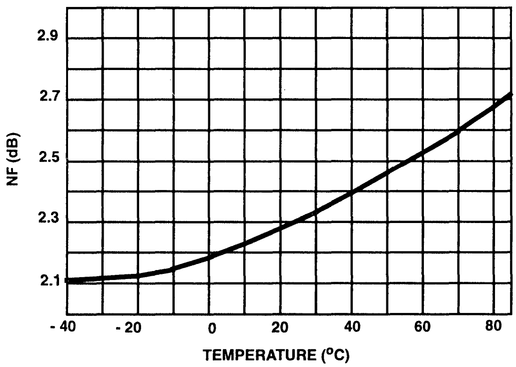


FIGURE 13. LNA 50Ω NF vs TEMPERATURE

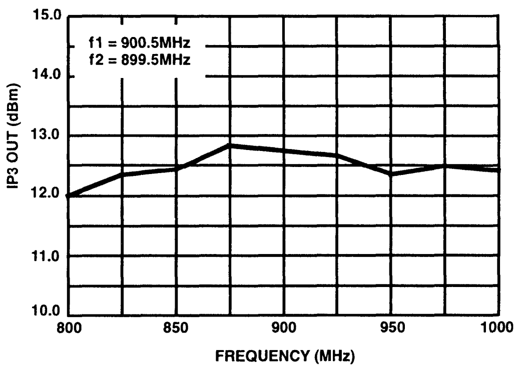


FIGURE 14. LNA OUTPUT IP3 vs FREQUENCY

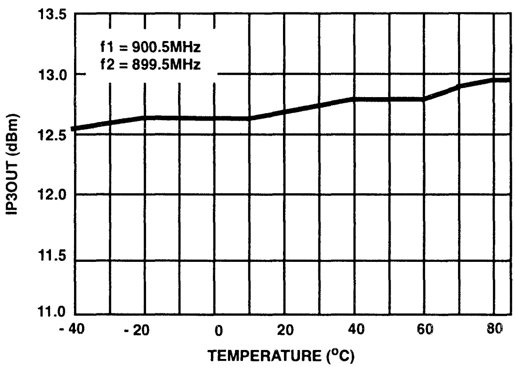


FIGURE 15. LNA OUTPUT IP3 vs TEMPERATURE

FREQ	S11		S21		S22		S12	
MHz	dB	deg	dB	deg	dB	deg	dB	deg
800	-6.7	153	13.7	11.4	-11.9	-170	-23.8	-41
850	-7.0	143	13.3	1.5	-12.0	171	-23.1	-48
900	-7.3	133	12.8	-7.7	-13.0	155	-23.0	-56
950	-7.4	123	12.6	-18	-12.0	137	-23.1	-65
1000	-7.6	113	12.2	-27	-11.8	120	-22.8	-70

FIGURE 16. LNA S-PARAMETERS

Mixer Characteristics

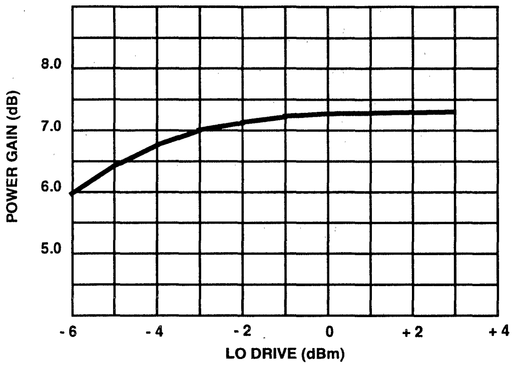


FIGURE 17. MIXER PG vs LO DRIVE

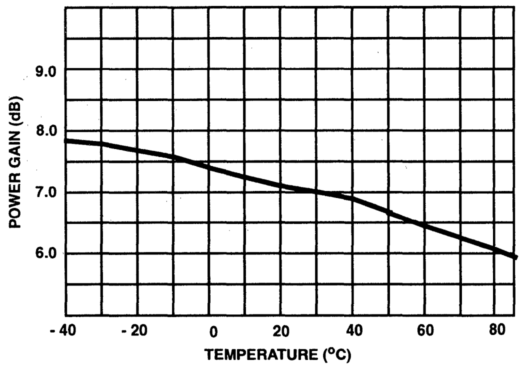


FIGURE 18. MIXER PG vs TEMPERATURE

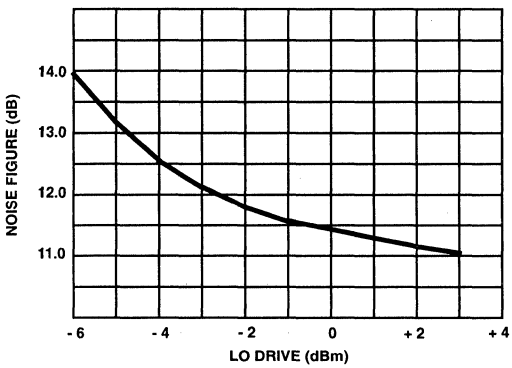


FIGURE 19. MIXER NF vs LO DRIVE

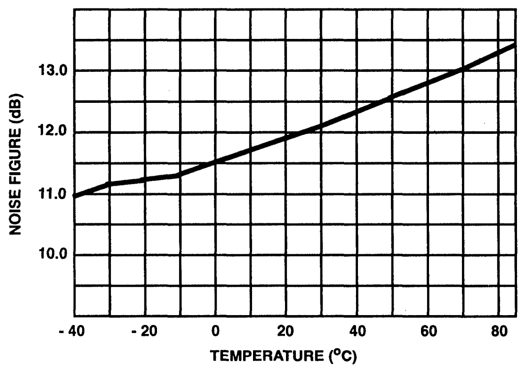


FIGURE 20. MIXER NF vs TEMPERATURE

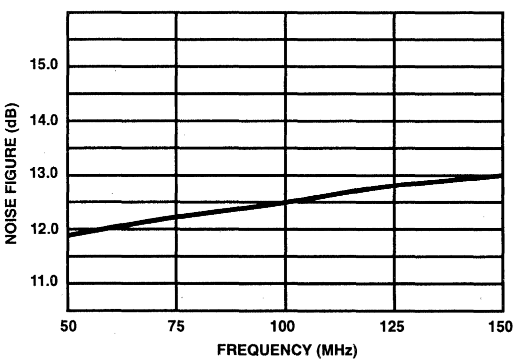


FIGURE 21. MIXER NF vs IF FREQUENCY, RF = 900MHz, FLO < FRF

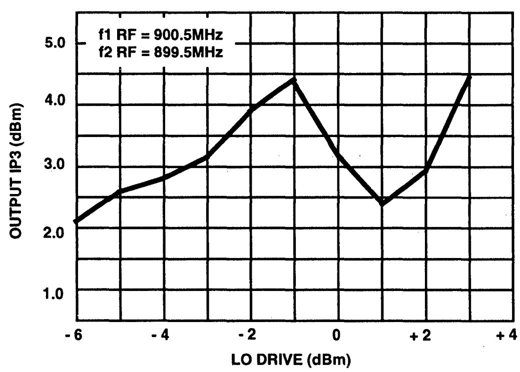


FIGURE 22. MIXER OUTPUT IP3 vs LO DRIVE

Mixer Characteristics (Continued)

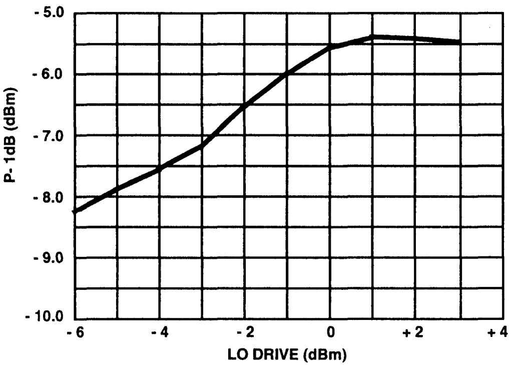


FIGURE 23. MIXER 1dB COMPRESSION vs LO DRIVE

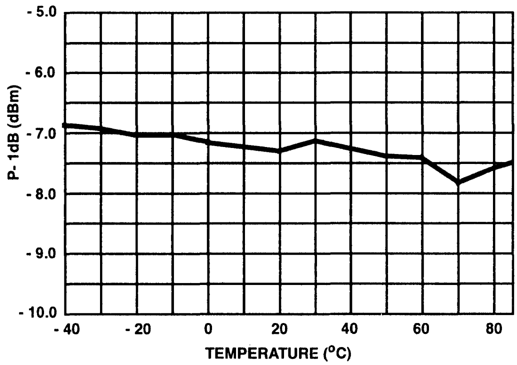


FIGURE 24. MIXER 1dB COMPRESSION vs TEMPERATURE

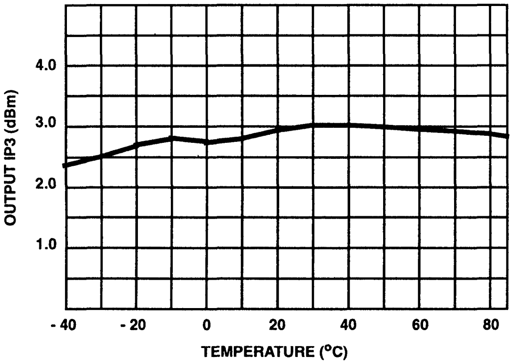


FIGURE 25. MIXER OUTPUT IP3 vs TEMPERATURE

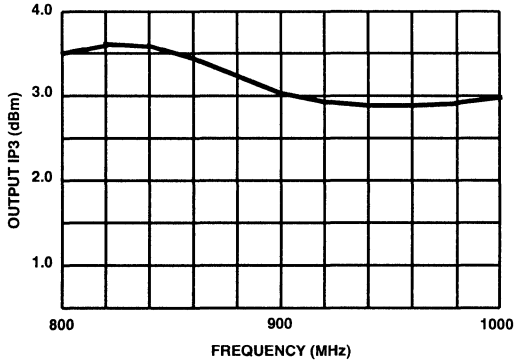


FIGURE 26. MIXER OUTPUT IP3 vs RF FREQUENCY

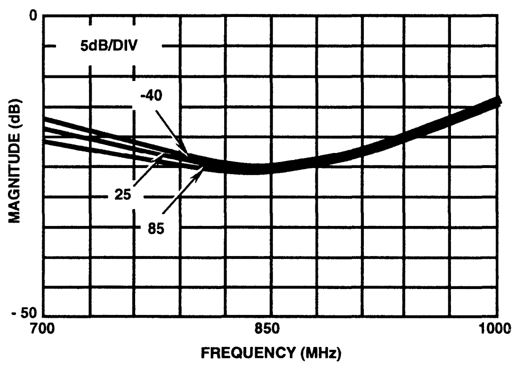


FIGURE 27. MIXER LO S11 vs FREQUENCY AND TEMPERATURE

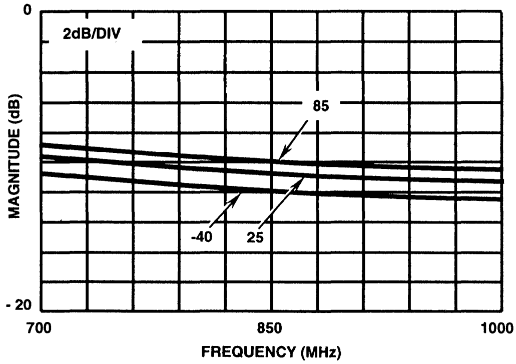


FIGURE 28. MIXER RF S11 vs FREQUENCY AND TEMPERATURE

9

SPECIAL ANALOG CIRCUITS

Isolation Characteristics

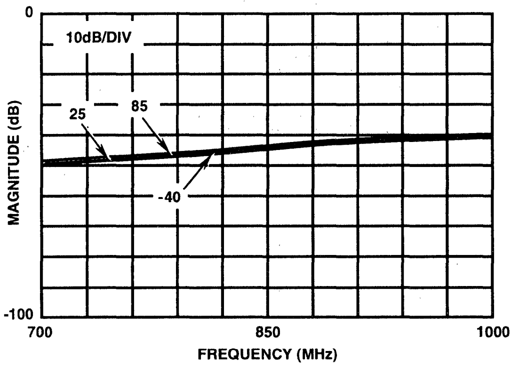


FIGURE 29. LNA OUT TO MIXER RF ISOLATION vs FREQUENCY AND TEMPERATURE

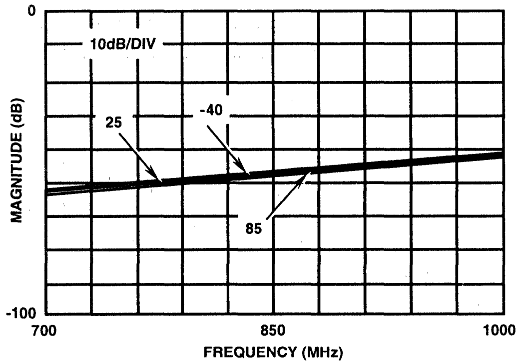


FIGURE 30. MIXER LO IN TO LNA IN ISOLATION vs FREQUENCY AND TEMPERATURE

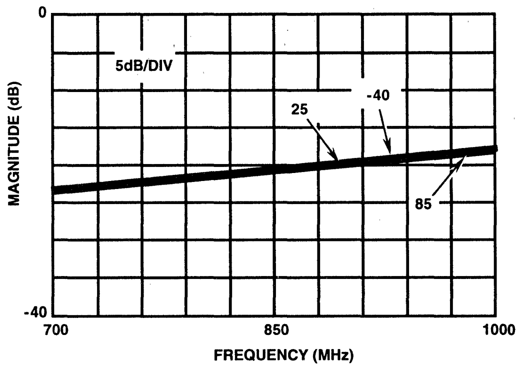


FIGURE 31. MIXER LO TO RF ISOLATION vs FREQUENCY AND TEMPERATURE

LNA Noise and Gain Characteristics

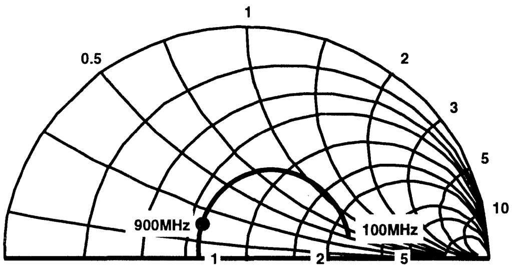


FIGURE 32. LNA GAMMA OPTIMUM vs FREQUENCY

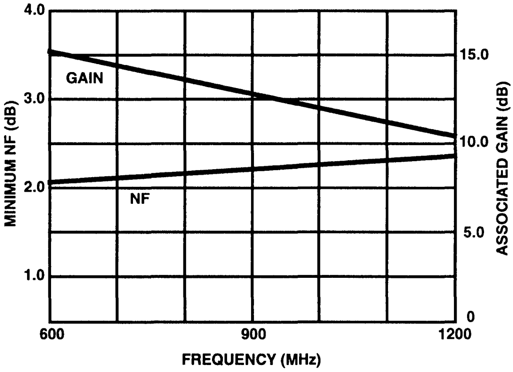


FIGURE 33. MINIMUM NOISE FIGURE AND ASSOCIATED GAIN vs FREQUENCY

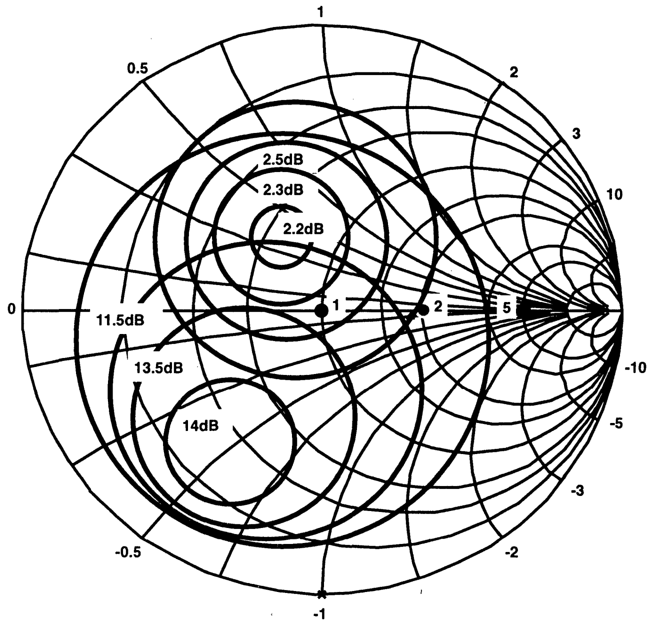


FIGURE 34. LNA NOISE AND GAIN CIRCLES AT 900MHz

Evaluation Board Layout Information

Component List.

R1 Res, fixed 1kΩ

L1 Ind., fixed 10μH

L2 Ind., fixed 390nH

C3,C4,C5,C7,C10,C11 Cap, fixed 1nF

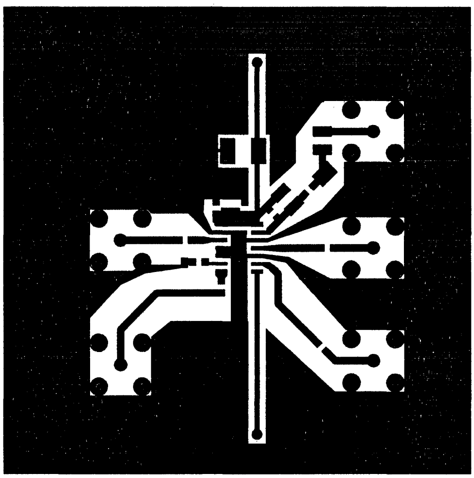
C1,C6 Cap, fixed.01μF

C2 Cap, fixed Tantalum. 4.7μF

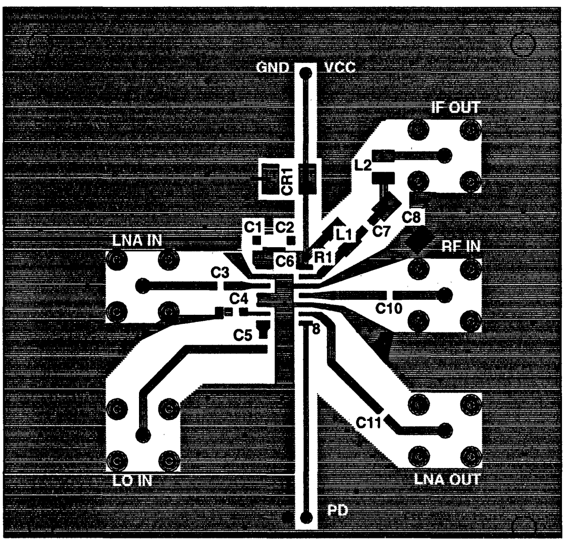
C8 Cap, var. 3pF to 10pF

Cr1 Diode DL4001

EVALUATION BOARD LAYOUT. SCALE X1
TOP VIEW



EVALUATION BOARD COMPONENT PLACEMENT



NOTE: See Evaluation Board testing information.

Pin Description

LNA V_{CC}

Supply voltage for the Low Noise amplifier.

LNA In

LNA input. Requires AC coupling. Minimum coupling capacitor value of 100pF is suggested. This input is optimized for 50W match in the 800MHz to 1000MHz range.

LO Bypass

Mixer LO Bypass. Capacitor required to assure a good AC ground. Placement is critical. The bypass capacitance should be located close to the device with low ground impedance. Minimum coupling capacitor value of 100pF is suggested.

LO In

Local oscillator input. Requires AC coupling. Input is optimized for 50W match in the 700MHz to 1000MHz range.Minimum coupling capacitor value of 100pF is suggested.

Power Down

Power down control with internal pull up. A low TTL or CMOS level disables the bias network, shutting down both the LNA and the MIXER within 10ms.The internal pull up is provided for users that do not require the power down feature. Provided for Time Division Multiplex Systems and/or power savings.

LNA Out

Output of the LNA. Requires AC coupling. This output has been optimized for 50W match in the 800MHz to 1000MHz range. Minimum coupling capacitor value of 100pF is suggested.

RF In

RF input to the MIXER. Requires AC coupling. Input optimized for 50W match in the 800MHz to 1000MHz range. Minimum coupling capacitor value of 100pF is suggested.

IF Out

Open collector output of the MIXER. Output capacitance is 2.3pF typical. The use of a RF choke maximizes the voltage output swing but is not mandatory. An output resistance controls the conversion gain as well as IP3 within the useful range of 300W to 1500W. It also affects the output impedance required for the next filter stage and facilitates any output matching network design requirements. Conversion gain is reduced upon use of low value resistors.

Mixer V_{CC}

Supply voltage for the MIXER and the Bias Network.

Characterization Information

The curves and data depicted in the Specifications Section are the result of the design characterization performed by the use of a standard evaluation board and a statistically significant sample procedure which reflects the HARRIS UHF-1 process variation.

The use of standard RF techniques have been employed throughout the characterization process with special emphasis on noise figures, gains and LO level performances.

Special attention has been given to the Local oscillator signal purity and integrity throughout the low and high frequency spectrum.

The use of low Excess Noise Ratio (ENR) noise sources have been employed to guarantee a good 50Ω noise source output impedance during the LNA noise measurements.

The use of attenuators for most of the setups have assured output impedances of signals closer to 50W when the use of power splitters and filters with poor return loss were necessary.

50Ω environment measurements have been carried throughout the characterization process including the IF output from the MIXER.

Device Description

The HFA3600 is fabricated in the HARRIS UHF-1 Bonded wafer, Silicon on Insulator process. ft characteristics of 10GHz and Power bandwidth product of 6GHz together with the robustness of the SOI process ensure high reliability for high frequency volume production. The process features low parasitic capacitances and very low leakages.

LNA

The LNA uses a single stage topology with a collector spiral inductor to improve the stability at lower frequencies and to optimize the power gain in the 900MHz range. Typical noise figure of 2.3dB, gain of 12.8dB and third order output intercept point of +12.8dBm are the main features. Bias currents are laser trimmed for optimum performances and for tight distribution among production lots. Under a 50Ω environment, the LNA input return loss is 7.3dB and the output return loss is 13dB. Characteristics of the gamma optimum, which is shown in the specifications section, suggests that the optimum source impedance driving the LNA for minimum noise figure is located close to 50Ω. The trade-off between gain and noise figures at 900MHz are shown in the gain and noise circles representation of the specification section.

Mixer

The HFA3600 Mixer uses a single balanced topology. This topology features an open collector with an output capacitance in the order of 2.3pF. Bias settings are also laser trimmed for optimum performance and tight distribution among production lots. The open collector output permits direct interface to moderate impedance IF filters as well as 50W input filters after a simple "L" impedance matching network. A collector resistor of 1K has been used throughout the characterization together with an impedance matching network for 50W load measurements. With a low -3dBm LO level, a typical SSB noise figure of 12.1dB, conversion gain of 7.0dB and a third order output intercept point of +3.2dBm are the main features. The LO input return loss is typically of 26dBm and the RF input return loss has a typical value of 11dB.

Bias Network and Power Down

The Bias Network is responsible for the accurate setting of both LNA and MIXER operating currents. The LNA operating current is accurately set to 5mA while the MIXER is set to 4mA. Laser trimming procedures and a temperature independent performance of the bias cell, assure the worst case operating current variation of the LNA and MIXER of 1% over the operating temperature range.

The Bias network is powered by the Mixer VCC pin and has a built in feature of disabling both the LNA and the MIXER stages. The cell can be powered up and down within 10ms. Power down total current consumption is in the order of 250mA.The simplified schematic of the power down input circuit is shown below.

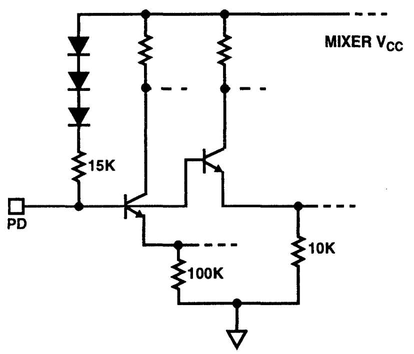


FIGURE 35. ENABLE PIN INPUT CIRCUIT

Low Voltage Operation

Low voltage operation is possible with the HFA3600. The HFA3600 has been characterized with V_{CC} of 4V and only moderate degradations have been observed compared to the AC performance at a V_{CC} of 5V. The LNA gain shows a 0.8dB decrease and a 1.5dB degradation in the output intercept point with no measurable impact on noise figure.

The MIXER behavior at 4V can be summarized with a degradation of conversion gain and output intercept point of 0.8dB and a slight improvement in noise figure of 0.6dB.

Other relevant 4V performance characteristics include:

- **Total ICC: typical drop of 2.2mA**
- **LNA Input Return Loss: degraded by 0.6dB**
- **LNA Reverse Isolation: degraded by 1dB**
- **LNA Output Return Loss: degraded by 1dB**
- **RF to IF Isolation: no change**
- **LOin to LNAin Isolation: improvement by 2dB**
- **LNAOUT to Mixer RFIN Isolation: improvement by 0.2dB**
- **Mixer LO to RF Isolation: no change**
- **Mixer LO to IF Isolation: degrades by 0.5dB**
- **Mixer RF input Return Loss: degrades by 1dB**
- **Mixer LO Input Return Loss: degrades by 0.3dB at 800MHz and 1dB at 700MHz**

Layout Considerations

The HFA3600 evaluation board layout has been carefully designed for an accurate RF characterization of the device. 50Ω microstrip lines have been provided to permit the connection of the LNA and MIXER independently and facilitate the user interface for testing. Top ground planes were used to assure adequate isolation between critical traces.

The HA3600 package pinout has been laid out for best isolation and overall device performance which also permits the placement and connection of ground planes at pins 2, 4, 5, 10 and 12. Pin 4 and Pin 5 assure a low impedance ground return for the LNA and also helps the isolation between the LNA input and the LO input. The LNA output pin is isolated from the RF input port with a good ground connection between the top and back ground planes terminated at pin 10. A series of plated through holes resembling a stitch pattern are sufficient and important for the LNA_{-OUT} and RF_{-IN} ports isolation, so the designer can rely on the full characteristics of rejection of the image filter. Similar isolation pattern is drawn and terminated in pin 12 to isolate the RF_{-IN} from the IF_{-OUT} port.

A ground pad has been laid down beneath the package with a series of plated through holes to minimize the inductance to the ground plane and improve the device gain characteristics.

All device grounds must be connected as close to the package as possible and the same applies to both V_{CC} inputs and all V_{CC} bypass capacitors. A small 4.7μF tantalum capacitor at the V_{CC} line will prevent supply coupling to the bias network if the device is subjected to strong low frequency interference signals.

A protection diode has been added to the demonstration board for extra protection and is not needed in an actual application.

Evaluation Board Testing Information

The following paragraphs contain information related to the evaluation of the HFA3600 LNA/Mixer noise figure and common errors encountered during individual and cascaded performance verification. A simple cascaded arrangement using a simple Π network as an intermediate filter is included.

Background

Active single balanced mixers are low cost, low power dissipation devices which require low local oscillator levels to operate. As single balanced mixers lack high isolation from the RF and LO input ports to the IF output and operate with moderate feedthrough from the LO input to the RF input, special precautions must be taken when evaluating these devices with test set ups, specifically filtering, and cabling hook ups. These constraints, although important during the evaluation of the device, are not major issues in the design of the overall system.

Poor isolation from the RF input to the IF output results in direct amplification (not only frequency translation) of undesired signals at the RF input port. For example, any noise within the IF passband generated by a previous active system block (LNA or any other amplifier) is directly transferred and amplified to the IF output. This lack of isolation can considerably degrade the translated signal to noise ratio of the IF output. An image filter placed before the mixer RF input port can solve the problem. Image filters are normally implemented as narrow bandpass filters which are tuned to pass only the desired (LO+IF) or (LO-IF) frequency of interest. Consequently, the role of rejecting noise at frequencies within the IF passband is accomplished.

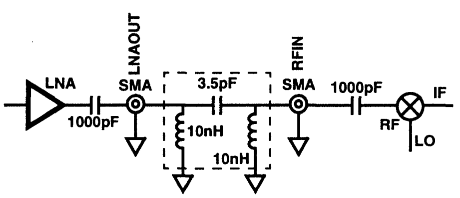
Poor isolation from the LO input to IF output can also slightly degrade the translated signal to noise ratio of the IF output in two distinct ways: the noise generated by the local oscillator at the IF frequency band is directly coupled to the IF port, and the noise at the RF and image RF passbands (LO SSB noise) gets translated to the IF passband and appears in the IF output. To overcome these problems, the use of a band pass filter is recommended between the local oscillator and the LO input for optimization of the mixer noise figure.

The lack of isolation from the LO input port back to the RF input port can cause constructive or destructive interference at the RF port which can affect noise and conversion (translation) gain performance.

Cascaded Evaluation

The cascaded evaluation of the HFA3600 demo-board must be carried out with a filter network between the LNA and the mixer when noise figure or sensitivity measurements are made. Any bandpass/highpass implementation must be utilized to function as either an image or noise rejection filter.

To remove the IF noise being generated or amplified by the LNA, a low cost Π or "T" high pass filter can be utilized. This simple high pass filter can be used for a cascaded noise evaluation of the HFA3600. Although this implementation does not remove the image signal nor the image noise being generated by the LNA, this filter gives an overall cascaded performance that closely approximates the results obtained by calculation. The large contribution of the LNA gain at the IF frequency (from a white noise source at its input and its own IF noise), to the overall noise figure measurement is practically eliminated by the high pass filter. Figure 1 shows an implementation of a high pass filter network used to filter out the incoming IF noise from the LNA. A rider board can be built to connect the **LNAOUT** and the **RFIN** SMA connectors of the demo-board. The 1000pF decoupling capacitors are included in the demo-board.



Π COMPONENTS SHOWN ARE FOR 900MHz RF
A "T" FILTER CAN ELIMINATE THE 1000pF COUPLING CAPACITORS

FIGURE 36. HFA3600 HIGH PASS FILTER IMPLEMENTATION

Tuning of the Π network, if necessary, is done by changing the value of the 3.5pF capacitor. This low value of capacitance may be dependent on the rider layout. The value may be optimized for low insertion loss and, therefore, for optimum cascaded noise figure.

Figure 37 and Tables 2 and 3 illustrate the overall performance of the HFA3600 in a cascaded form at 915MHz RF input and 75MHz IF frequency:

TABLE 2. SSB MEASUREMENT SET UP (BANDPASS INPUT FILTER) (NOTES 1, 3)

IMAGE FILTER	NF (dB)	GAIN (dB)	COMMENTS
Saw, 3dB Loss	5.1	16.0	Gain reduced by the filter loss
Short/No Filter	14.4	N/A	NF degrades due to the IF noise from the LNA
Π Filter, No Loss at the RF Frequency	5.2	19.0	Note the increase in cascaded gain

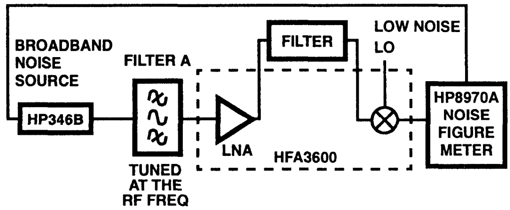


FIGURE 37A. SSB NOISE FIGURE MEASUREMENT

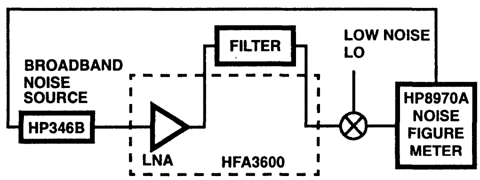


FIGURE 37B. DSB NOISE FIGURE MEASUREMENT

TABLE 3. DSB MEASUREMENT SET UP (NO INPUT BANDPASS FILTER)

IMAGE FILTER	NF (dB)	GAIN (dB)	COMMENTS
Saw, 3dB Loss	5.1	16.0	Equivalent to SSB measurement
Short/No Filter	1.8	31	Invalid measurement
Π Filter, No Loss at the RF Frequency	3.6	19.0	Note 2

NOTES:

1. The single side band input filter (filter A) loss is accounted for and removed in the Noise figure and gain values.
2. The difference of a DSB to a SSB noise figure is theoretically 3dB. The expected value of 2.2dB NF for a DSB measurement is degraded to 3.6db due to a small attenuation of the Π filter at the image frequency.
3. The cascaded results presented in the AC Specifications Table of the data sheet are calculated assuming the use of an ideal image filter (no loss) and a SSB measurement.

9 SPECIAL ANALOG CIRCUITS

HFA3600 Mixer Evaluation Notes

The evaluation of the HFA3600 mixer by itself is facilitated by the demo-board design which provides access to the 3 ports by SMA connectors. As discussed before, RF to IF feedthrough and LO to RF/IF ports moderate isolation can cause errors during noise measurements.

The inherent RF to IF feedthrough of the single balanced mixer mandates that noise measurements be single side band only (with an appropriate band pass filter at the RF frequency of interest). Because of this lack of isolation, the incoming energy located at the IF passband from a broadband noise source for example, will feedthrough and cause significant noise figure measurement errors.

As noise measurement equipment often makes use of broadband noise sources with energy covering a wide spectrum, SSB measurements are made using a band pass filter in front of the RF port. The role of the band pass filter is to prevent the image and IF noise energy from being fed to the mixer.

However, band pass filters exhibit poor return losses at frequencies outside their passbands. Because a moderate amount of power from a local oscillator is transferred back to the RF port in many active mixers, and this returned LO signal is outside the passband of the SSB filter being used, the signal will get reflected back again to the RF port due to impedance mismatch between the filter and the RF port. This impedance mismatch occurs at the LO frequency and these multiple signal reflections can affect gain and noise performance of the mixer. This situation, although not a problem for the actual receiver design, can become a source of error during mixer noise measurements.

To minimize the problem, the simplest method is to provide a short connection (well below $\lambda/4$ of the LO frequency) between the filter and the RF port. In case a coaxial cable connection is required, it maybe necessary to provide a length of cable which assures minimum degradation to the noise figure reading. Long cables above 3 feet can provide the required standing wave dissipation for measurements in the 800MHz to 1GHz range. Note that long cable losses must be taken into account for the purpose of noise figure measurements. Adjustable line stretchers or isolators at the RF input port could also be used to optimize noise figure readings as an option for the mixer evaluation.

And finally, the recommendation of filtering the local oscillator signal before applying it to the LO port is important for accuracy of noise measurements when evaluating the mixer by itself, due to the typical LO to IF feedthrough in single balanced mixers.

HFA3600 LNA Evaluation Notes

The evaluation of the LNA is straightforward. SMA connectors are provided in the demo-board. There are no recommendations for evaluating the LNA block other than using typical RF amplifier test techniques.

Final Note

The cascaded evaluation of the HFA3600 LNA and mixer blocks including an image rejection or high pass filter is the best method to obtain accurate results. The gain and noise performance contribution of the LNA and filter to the cascaded results surpass considerably the performance contribution of the mixer. The data collected by cascading the blocks together reflects the performance at the system level which includes the filter of choice for a required design.

HARRIS SEMICONDUCTOR

HFA5253

PRELIMINARY

June 1995

Ultra High-Speed Monolithic Pin Driver

Features

- High Digital Data Rate 800MHz
- Very Fast Rise/Fall Times 500ps
- Wide Output Range .... +8V to -3V
- Precise 50Ω Output Impedance
- High Impedance, Three-State Output Control
- Slew Rate Control

Applications

- IC Tester Pin Electronics
- Pattern Generators
- Pulse Generators
- Level Comparator/Translator

Description

The HFA5253 is a very high speed monolithic pin driver solution for high performance test systems. The device will switch at high data rates between two input voltage levels providing variable amplitude pulses. Slew Rate Control pins provide independent control over positive and negative slew rate allowing the customer to optimize the pin driver speed for their application. The output impedance is trimmed to achieve a precision 50Ω source for impedance matching. Two differential ECL/TTL compatible inputs control the operation of the HFA5253, one controlling the V_{HIGH}/V_{LOW} switching and the other controlling the output's high-impedance state. The HFA5253's 800MHz data rate makes it compatible with today's high-speed VLSI test systems and the +8V to -3V output swing satisfies the most stringent testing requirements of all common logic families.

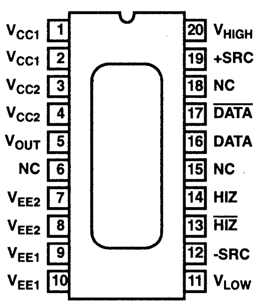
The HFA5253 is manufactured in Harris' proprietary complementary bipolar UHF-1 process.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HFA5253Y	$T_{JUNCTION}$ <150°C	DIE Form
HFA5253CB	0°C to 50°C	20 Lead PSOP

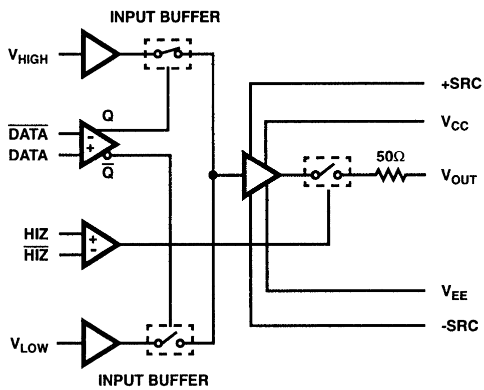
Pinout

HFA5253 (PSOP)
TOP VIEW



POWER PSOP PACKAGE
(HEAT SLUG SURFACE IS ELECTRICALLY FLOATING)

Block Diagram



TRUTH TABLE FOR V_{OUT}

		DATA	
		0	1
HIZ	0	V_{LOW}	V_{HIGH}
	1	HIZ	HIZ

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4003**

Pin Descriptions

NAME	FUNCTION
V_{CC1}	Positive Supply. Nominal value is 11.2V ±0.2V. Reducing supply voltage below 11.0V will reduce positive output voltage swing. The total supply voltage from V_{CC1} to V_{EE1} should not exceed 18.0V for normal operation or exceed 19.0V to prevent damage. Harris recommends two wire bonds to this pad to provide the lowest possible impedance. In addition, power supply decoupling chip capacitors of 470pF, 0.1μF and a 10μF tantalum are recommended. Do not connect the V_{CC1} and V_{CC2} pins together immediately, rather run separate traces until they can be joined at a large by-pass capacitor (0.1μF ll 10.0μF).
V_{EE1}	Negative Supply. Nominal value is -6.4V ±0.2V. A supply voltage more positive than -6.2V will reduce negative output voltage swing. The total supply voltage from V_{CC1} to V_{EE1} should not exceed 18.0V for normal operation or exceed 19.0V to prevent damage. Harris recommends two wire bonds to this pad to provide the lowest possible impedance. In addition, power supply decoupling chip capacitors of 470pF, 0.1μF and a 10μF tantalum are recommended. Do not connect the V_{EE1} and V_{EE2} pins together immediately, rather run separate traces until they can be joined at a large by-pass capacitor (0.1μF ll 10.0μF).
V_{CC2}	Output Stage Positive Supply. Nominal voltage and cautions are the same as for V_{CC1}. Having decoupling chip capacitors close to V_{CC2} and V_{EE2} is essential since large AC current will flow through this pad to the output during transients. Harris recommends two wire bonds for this pad. Do not connect the V_{CC1} and V_{CC2} pins together immediately, rather run separate traces until they can be joined at a large by-pass capacitor (0.1μF ll 10.0μF).
V_{EE2}	Output Stage Negative Supply. Nominal voltage and cautions are the same as for V_{EE1}. Having decoupling chip capacitors close to V_{CC2} and V_{EE2} is essential since large AC current will flow through this pad to the output during transients. Harris recommends two wire bonds for this pad. Do not connect the V_{EE1} and V_{EE2} pins together immediately, rather run separate traces until they can be joined at a large by-pass capacitor (0.1μF ll 10.0μF).
V_{HIGH}	Input Voltage High is used to set the output high level V_{OH}. V_{HIGH} is sensitive to capacitively coupled AC noise. Protection from high frequency noise can be achieved with a low pass filter consisting of a 50Ω chip resistor and a 470pF chip capacitor. Without this precaution the pin driver may oscillate due to feedback from the output through the PC board ground.
V_{LOW}	Input Voltage Low is used to set the output low level V_{OL}. V_{LOW} is sensitive to capacitively coupled AC noise. Protection from high frequency noise can be achieved with a low pass filter consisting of a 50Ω chip resistor and a 470pF chip capacitor. Without this precaution the pin driver may oscillate due to feedback from the output through the PC board ground.
V_{OUT}	Driver Output. The output impedance has been laser trimmed to match a 50Ω transmission line ±2Ω. Custom output impedance trimming is available (contact sales office for details) to provide the best match possible to your 50Ω system.
$\overline{DATA}$, DATA	Differential Digital Inputs used to switch V_{OUT} to the V_{HIGH} or V_{LOW} level. Harris recommends this input pair be driven by complementary ECL signals to provide optimal switching speeds and timing accuracy. However a large Common Mode and Differential Voltage Range is provided to accommodate a variety of signals including single ended TTL and CMOS. When using single ended signals the other input must be tied to an appropriate threshold voltage.
$\overline{HIZ}$, HIZ	Differential Digital Inputs used to switch V_{OUT} from an Active to a High Impedance State. Harris recommends that this input pair be driven by complementary ECL signals to provide optimal switching speeds and timing accuracy. However a large Common Mode and Differential Voltage Range is provided to accommodate a variety of signals including single ended TTL and CMOS. When using single ended signals the other input must be tied to an appropriate threshold voltage.
+SRC	The Positive Slew Rate Control Pin adjusts the rising edge slew rate with an external current I_{STEAL}. I_{STEAL} draws current (0mA to 10mA) from an internal current source limiting the rate of change of the high impedance node. Typically an external resistor to GND is sufficient to set the slew rate at a desired level. Leaving the +SRC Pin open will give the highest speed performance. The external current I_{STEAL} for a resistor R_{STEAL} connected from +SRC to GND may be calculated by: $I_{STEAL} = (V_{CC} - 0.35)/R_{STEAL}$.
-SRC	The Negative Slew Rate Control Pin adjusts the falling edge slew rate with an external current I_{STEAL}. I_{STEAL} supplies current (0mA to 10mA) to an internal current source limiting the amount of current being drawn from the circuit and thus limiting the rate of change of the high impedance node. Typically an external resistor to GND is sufficient to set the slew rate at a desired level. Leaving the -SRC Pin open will give the highest speed performance. The external current I_{STEAL} for a resistor R_{STEAL} connected from -SRC to GND may be calculated by: $I_{STEAL} = (V_{EE} + 0.35)/R_{STEAL}$.

Absolute Maximum Ratings

Supply Voltage 19.0V
Differential Input Voltage (DATA and HIZ) 5.0V
Output Current Continuous (Note 1). . . . 160mA
Maximum Junction Temperature . . . . +150°C
Lead Temperature (Soldering 10s) . . . . 300°C
(PSOP - Lead Tips Only)
Input Voltage (Any pin except as specified) . . . . V_{CC} to V_{EE}
V_{OUT} Voltage (Note 2) . . . . 9V to -4V
V_{HIGH} Voltage . . . . V_{CC} to -4V

V_{LOW} Voltage . . . . 9V to V_{EE}
V_{HIGH} to V_{LOW} Voltage . . . . 11V to 0V (V_{HIGH} > V_{LOW})
Slew Rate Control Current (+SRC, -SRC) 12mA
Operating Temperature Range . . . . 0°C to +50°C
Storage Temperature Range . . . . -65°C to +150°C
Typical Thermal Resistance (°C/W) θ_{JA} θ_{JC}
20 Lead Power SOP Package 49 2
(θ_{JC} Measured At Copper Slug Top Center with Infinite Heat Sink)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{CC} = +11.2V; V_{EE} = -6.4V; V_{IH} = -0.9V; V_{IL} = -1.75V; +SRC and -SRC are Not Connected Unless Otherwise Specified

PARAMETER	(NOTE 3) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS (V_{HIGH}, V_{LOW})						
V_{HIGH} Input Offset Voltage	A	25°C	-150	-50	+50	mV
V_{LOW} Input Offset Voltage	A	25°C	-150	-50	+50	mV
V_{HIGH} Input Bias Current (V_{HIGH} = -3.25V to +8.5V)	A	25°C	-50	110	400	μA
V_{LOW} Input Bias Current (V_{LOW} = -3.5V to +8.25V)	A	25°C	-400	-110	50	μA
V_{HIGH} Voltage Range	A	25°C	-3.25	-	8.5	V
V_{LOW} Voltage Range	A	25°C	-3.5	-	8.25	V
V_{HIGH} to V_{LOW} Differential Voltage Range ($V_{HIGH} \geq V_{LOW}$)	A	25°C	0	-	9.5	V
V_{HIGH}/V_{LOW} Interaction at 500mV (Notes 4, 16)	A	25°C	-	2	4	mV
V_{HIGH}/V_{LOW} Interaction at 250mV (Notes 4, 16)	A	25°C	-	20	40	mV
LOGIC INPUT CHARACTERISTICS (DATA, $\overline{DATA}$, HIZ, $\overline{HIZ}$)						
Logic Input Voltage Range	B	25°C	-3	-	8	V
Logic Differential Input Voltage	B	25°C	0.4	-	5	V
DATA/$\overline{DATA}$ Logic Input High Current (V_{IH} = 0V, V_{IL} = -2V)	A	25°C	-50	110	700	μA
DATA/$\overline{DATA}$ Logic Input Low Current (V_{IH} = 0V, V_{IL} = -2V)	A	25°C	-700	-300	50	μA
HIZ/$\overline{HIZ}$ Logic Input High Current (V_{IH} = 0V, V_{IL} = -2V)	A	25°C	-50	70	400	μA
HIZ/$\overline{HIZ}$ Logic Input Low Current (V_{IH} = 0V, V_{IL} = -2V)	A	25°C	-400	-80	50	μA
TRANSFER CHARACTERISTICS						
V_{HIGH} Voltage Gain (V_{HIGH} = -1V to 6.5V)	A	25°C	0.95	0.97	1	V/V
V_{LOW} Voltage Gain (V_{LOW} = -1.5V to 6V)	A	25°C	0.95	0.97	1	V/V
V_{HIGH}/V_{LOW} Linearity Error (Fullscale = 5V, Note 5)	A	25°C	-0.2	-	0.2	%
V_{HIGH}/V_{LOW} Linearity Error (Fullscale = 10.5V, Note 6)	A	25°C	-0.4	-	0.4	%
V_{HIGH}/V_{LOW} -3dB Bandwidth (200mV$_{P-P}$)	B	25°C	-	100	-	MHz

Electrical Specifications V_{CC} = +11.2V; V_{EE} = -6.4V; V_{IH} = -0.9V; V_{IL} = -1.75V; +SRC and -SRC are Not Connected Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 3) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
Typical Slew Rate Control Range (I_{STEAL} = 0mA to 10mA, 5V step)	B	25°C	1.0	-	2.8	V/ns
+SRC Pin Voltage	C	25°C	-	V_{CC} - 0.35	-	V
-SRC Pin Voltage	C	25°C	-	V_{EE} + 0.35	-	V
SWITCHING CHARACTERISTICS (Z_{LOAD} = 16 inches of RG-58 Terminated with 50Ω)						
Propagation Delay (Notes 7, 9)	B	25°C	1	-	2	ns
Propagation Delay Match (Rising to Falling Edge, Notes 7, 9)	B	25°C	-100	-	100	ps
Rising Edge Propagation Delay vs Duty Cycle (Notes 8, 9)	B	25°C	-120	-20	80	ps
Falling Edge Propagation Delay vs Duty Cycle (Notes 8, 9)	B	25°C	-80	20	120	ps
Active to HIZ Delay (Note 9)	B	25°C	1.5	2.0	2.5	ns
HIZ to Active Delay (Note 9)	B	25°C	2.8	3.3	3.8	ns
TRANSIENT RESPONSE (Z_{LOAD} = 16 inches of RG-58 Terminated with 5pF)						
Rise/Fall Time (1V_{P-P}, 20% - 80%) (Note 10)	B	25°C	350	450	500	ps
Rise/Fall Time (3V_{P-P}, 10% - 90%) (Note 10)	B	25°C	700	890	1000	ps
Rise/Fall Time (5V_{P-P}, 10% - 90%) (Note 11)	A	25°C	1.1	1.3	1.7	ns
Rise/Fall Time Match (Note 11)	A	25°C	-	100	200	ps
Minimum Pulse Width (1V_{P-P}) (Note 12)	B	25°C	-	1.0	-	ns
Minimum Pulse Width (3V_{P-P}) (Note 12)	B	25°C	-	1.2	-	ns
Minimum Pulse Width (5V_{P-P}) (Note 12)	B	25°C	-	2.0	-	ns
Overshoot/Undershoot/Preshoot (3V_{P-P})	B	25°C	-	5	-	%
Data Settling Time 1% (Note 13)	B	25°C	-	10	-	ns
OUTPUT CHARACTERISTICS						
Output Voltage Swing, No Load at V_{CC} = 11V, V_{EE} = -6.2V	A	25°C	-3	-	8	V
Output Amplitude Voltage (V_{OH} - V_{OL})	A	25°C	0.25	-	9.0	V
DC Output Resistance (-3V to 8V) (Note 14)	A	25°C	45	47	49	Ω
Output Leakage - HIZ (-3V to 8V)	A	25°C	-100	-	100	nA
Output Capacitance - HIZ	C	25°C	-	5	-	pF
Output Current - Active	A	25°C	80	100	-	mA
Output Short Circuit Range (Note 2)	A	25°C	-4.0	-	9.0	V

Electrical Specifications V_{CC} = +11.2V; V_{EE} = -6.4V; V_{IH} = -0.9V; V_{IL} = -1.75V; +SRC and -SRC are Not Connected Unless Otherwise Specified **(Continued)**

PARAMETER	(NOTE 3) TEST LEVEL	TEMP	ALL GRADES MIN	TYP	MAX	UNITS
POWER SUPPLY CHARACTERISTICS (V_{HIGH} = 5V Active, No Load)						
V_{HIGH} Power Supply Rejection Ratio (Note 15)	A	25°C	-	14	40	mV/V
V_{LOW} Power Supply Rejection Ratio (Note 15)	A	25°C	-	14	40	mV/V
Total Supply Current	A	25°C	90	96	98	mA
I_{CC1}/I_{EE1} Supply Current	B	25°C	-	74	-	mA
I_{CC2}/I_{EE2} Supply Current	B	25°C	-	22	-	mA
Supply Voltage Range (V_{CC})	A	25°C	11.0	11.2	11.4	V
Supply Voltage Range (V_{EE})	A	25°C	-6.6	-6.4	-6.2	V
Supply Voltage Range (V_{CC} - V_{EE})	A	25°C	17.2	-	18.0	V
Power Dissipation (V_{CC} = 11.2V, V_{EE} = -6.4V, No Load)	A	25°C	-	-	1.72	W

NOTES:

1. Internal Power Dissipation may limit Output Current below 160mA.
2. Shorting the output to a voltage outside the specified range may damage the output.
3. Test Level: A = 100% production tested, B = Typical or limit based on lab characterization of a limited number of lots, C = Design Information, goal or condition.
4. V_{HIGH} to V_{LOW} Interaction is measured as the change in V_{OUT} (the active channel) due to a change in the inactive channel. V_{HIGH} Interaction at 250mV is measured as the deviation from 1V as V_{LOW} is changed from 0V to 750mV (Referred to V_{OUT}). V_{LOW} Interaction at 250mV is measured as the deviation from 0V as V_{HIGH} is changed from 1V to 250mV (Referred to V_{OUT}).
5. For V_{HIGH} = 0V to 5V, for V_{LOW} = 0V to 5V, Fullscale = 5V, 0.1% = 5mV. Output Amplitude (V_{HIGH} - V_{LOW}) = $1V_{P-P}$.
6. For V_{HIGH} = -2.5V to 8V, for V_{LOW} = -3.0V to 7.5V, Fullscale = 10.5V, 0.1% = 10.5mV. Output Amplitude (V_{HIGH} - V_{LOW}) = $1V_{P-P}$.
7. 3V Step, 50% duty cycle, 200ns period.
8. 0V to 3V Step, 200ns period, Pulse Width is varied from 5ns to 195ns.
9. Test is performed into a 50Ω load with a 3V step. Measurement is made from the 50% of the input to 50% of output.
10. Limit based on calculation. Not 100% tested.
11. 5V Step, 50% duty cycle, 100ns period. 100% Tested.
12. Minimum Pulse Width is measured 50% to 50% of specified amplitude with pulse peak at 100% of amplitude.
13. 3V Step, measured from 50% of input to ±1% of reference value at 50ns.
14. Dynamic Output Resistance will be higher (typ 48.5Ω) than DC Output Resistance. DC Output Resistance is measured at 0V with I_{OUT} set from 0mA to 40mA.
15. V_{HIGH} = 2.6V, V_{LOW} = 2.3V, V_{CC} = 10.2V to 11.2V, V_{EE} = -5.4V to -6.4V.
16. Input voltages V_{HIGH} and V_{LOW} are corrected for Offset Voltage and Gain Error.

Die Characteristics

DIE DIMENSIONS:

2670µm x 1730µm x 525µm ±25.4µm

METALLIZATION:

Type: Metal 1: Cu (2%) SiAl/TiW
Thickness: Metal 1: 8kÅ ±0.4kÅ
Backside: Gold
Type: Metal 2: Cu (2%) Al
Thickness: Metal 2: 16kÅ ±0.8kÅ

GLASSIVATION:

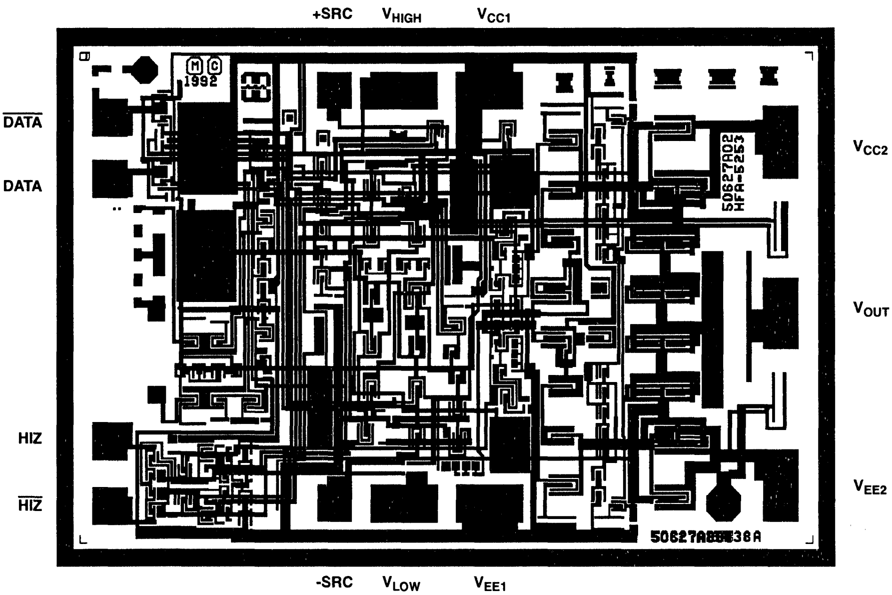
Nitride, 4kÅ ±0.5kÅ

TRANSISTOR COUNT: 113

SUBSTRATE POTENTIAL: Floating

Metallization Mask Layout

HFA5253



Definition of Terms

V_{OH} and V_{OL}

Output High Voltage and Output Low Voltage. V_{OH} is the voltage at V_{OUT} when the HIZ input is low and the DATA input is high. V_{OL} is the voltage at V_{OUT} when HIZ is low and DATA is low. The V_{OH} and V_{OL} levels are set with the V_{HIGH} and V_{LOW} inputs respectively.

Offset Voltage

Offset Voltage is the DC error between the voltage placed on V_{HIGH} or V_{LOW} and the resulting V_{OH} and V_{OL}. V_{HIGH} Offset Voltage Error is obtained by measuring V_{OH} with V_{HIGH} set to 0V and V_{LOW} set to -2.5V to minimize interaction effects. V_{LOW} Offset Voltage Error is the measurement of V_{OL} with V_{LOW} set to 0V and V_{HIGH} set to +7.5V.

Gain

Gain is defined as the ratio of output voltage change to input voltage change for a defined range. V_{HIGH} Gain is calculated with the following equation with V_{LOW} fixed at -2.5V:

$$V_{HIGH}GAIN = \frac{V_{OH}(V_{HIGH}\text{at } 6.5V) - V_{OH}(V_{HIGH}\text{at } -1V)}{7.5}$$

V_{LOW} Gain is calculated in a similar manner.

$$V_{LOW}GAIN = \frac{V_{OL}(V_{LOW}\text{at } 6V) - V_{OL}(V_{LOW}\text{at } -1.5V)}{7.5}$$

V_{HIGH} is held fixed at 7.5V. These Gain calculations minimize the effects of Interaction and End Point Nonlinearities.

Linearity Error

Linearity Error is a measure of output voltage worst case deviation from a straight line that has been corrected for offset and 7.5V Gain. Linearity Error is given as a percentage of fullscale and is done in two ranges, 5V and 10.5V. DATA is measure at 0.5V steps from -2.5V to 8V for V_{HIGH} and -3V to 7.5V for V_{LOW}. The Linearity Error equation is as follows for 10.5V fullscale:

$$V_{OUT}(\text{IDEAL}) = V_{IN} \times \text{Gain} + \text{Offset}$$

$$\text{Linearity Error} = \frac{V_{OUT} - V_{OUT}(\text{IDEAL})}{10.5}$$

The Linearity Error equation is as follows for 5V fullscale:

$$\text{Linearity Error} = \frac{V_{OUT} - V_{OUT}(\text{IDEAL})}{5}$$

Linearity Error is calculated for every data point in the range and the worst case value is recorded.

V_{HIGH} to V_{LOW} Interaction

V_{HIGH} to V_{LOW} Interaction is the change in V_{OUT} (the active channel) due to the inactive channel. V_{HIGH} Interaction is measured as the change in V_{OH} from 1V as V_{LOW} is moved from 0V to 750mV (V_{LOW} is corrected for gain and offset errors). V_{LOW} Interaction is measured as the change in V_{OL} from 0V as V_{HIGH} is moved from 1V to 250mV (with V_{HIGH} corrected for gain and offset errors). The minimum recommended difference between V_{HIGH} and V_{LOW} for the HFA5253 is 250mV.

Typical Performance Curves

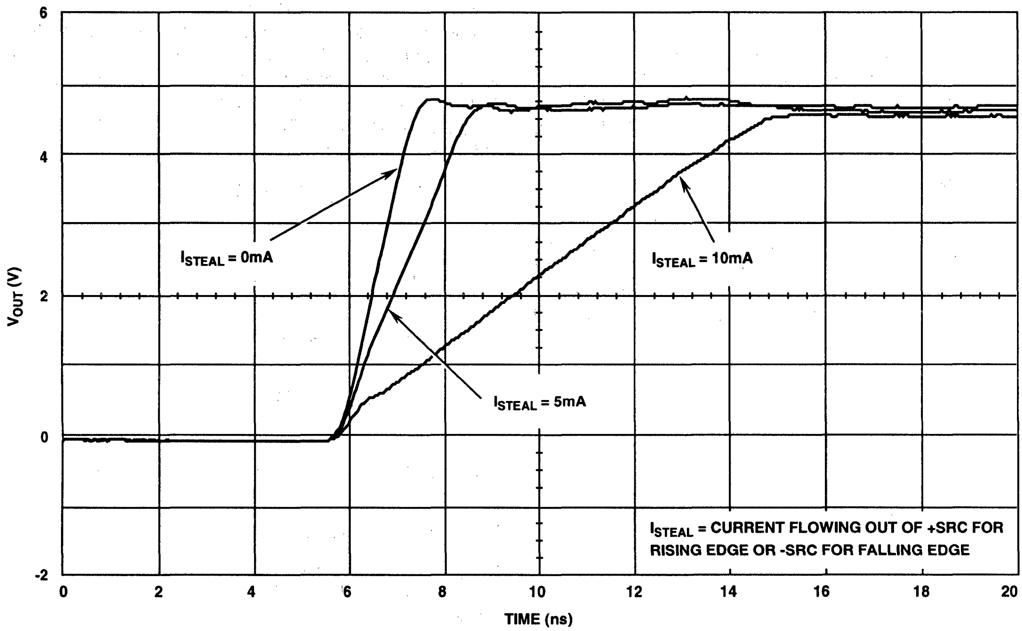


FIGURE 1. 5V STEP RESPONSE vs SLEW RATE CONTROL

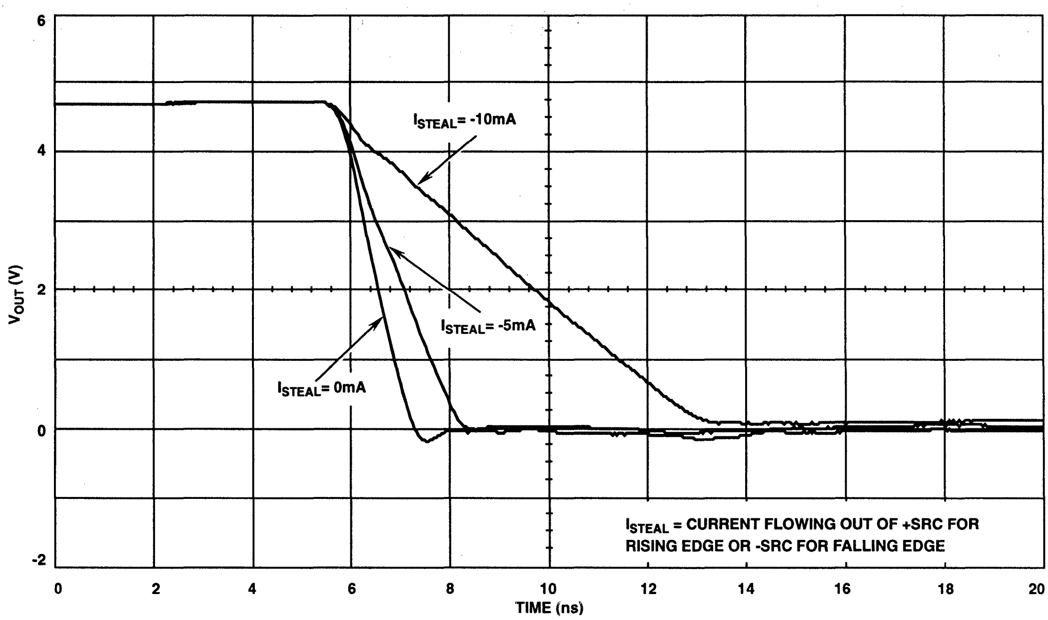


FIGURE 2. 5V STEP RESPONSE vs SLEW RATE CONTROL

Typical Performance Curves (Continued)

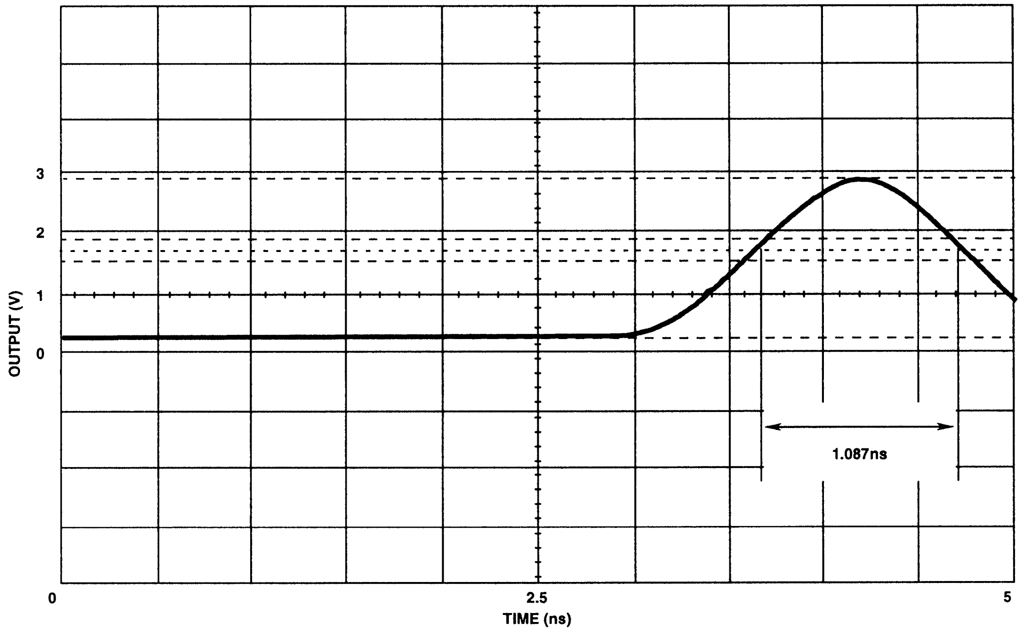


FIGURE 3. MINIMUM PULSE WIDTH, 1V/DIV; 500ps/DIV

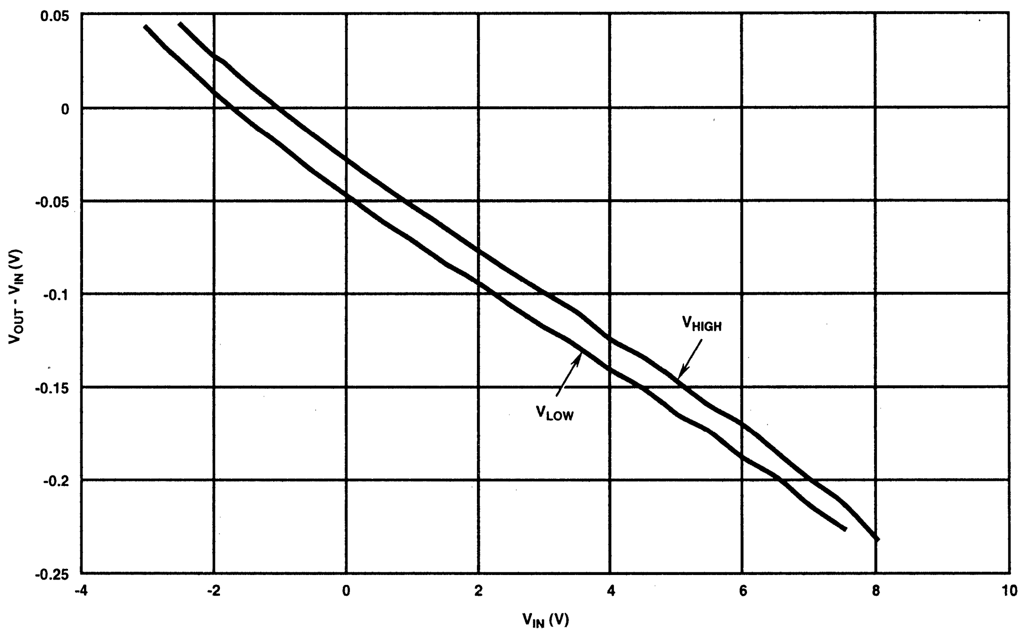


FIGURE 4. V_{OUT} ERROR vs V_{IN}

Typical Performance Curves (Continued)

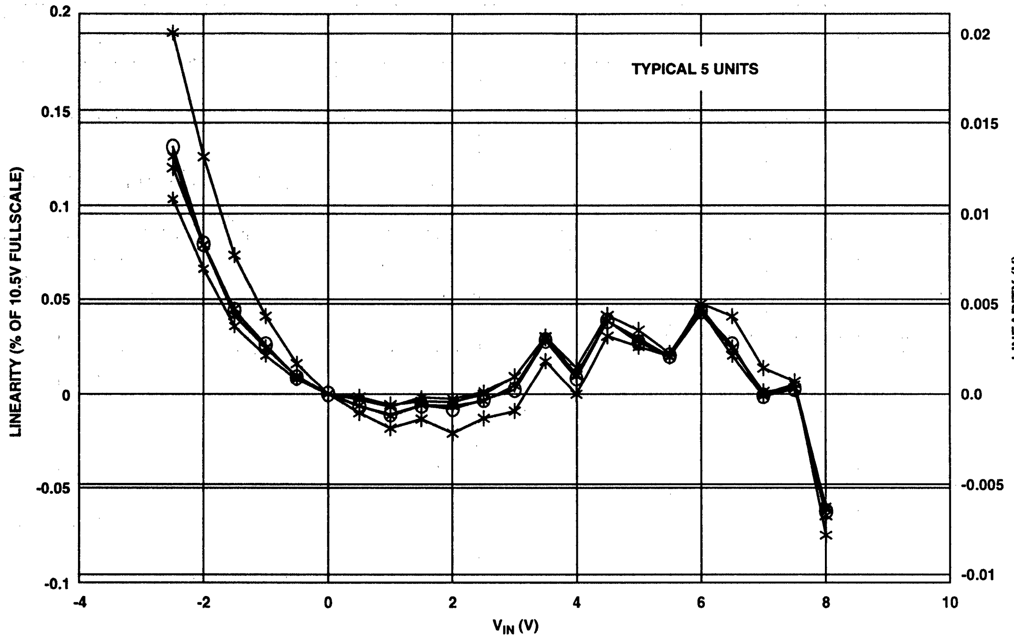


FIGURE 5. V_{HIGH} LINEARITY ERROR 10.5V FULLSCALE

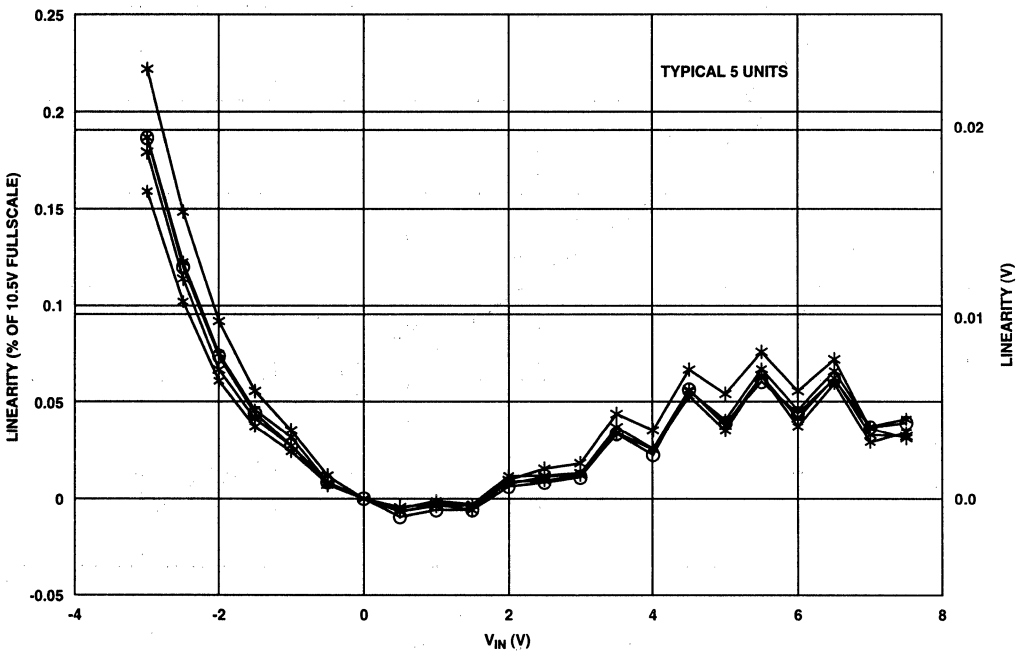


FIGURE 6. V_{LOW} LINEARITY ERROR 10.5V FULLSCALE

Typical Performance Curves (Continued)

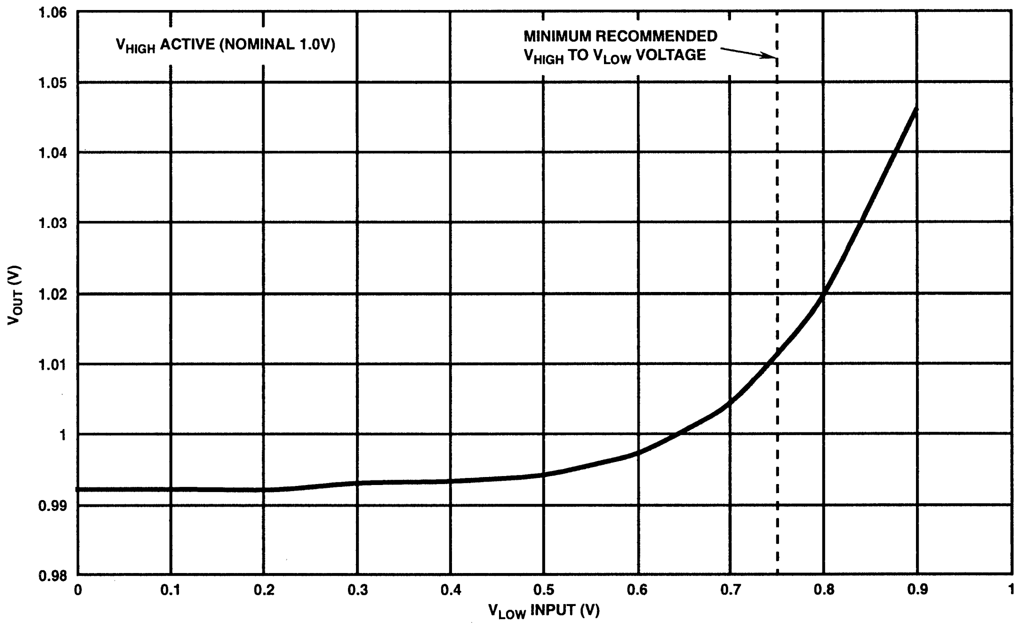


FIGURE 7. V_{HIGH}/V_{LOW} INTERACTION

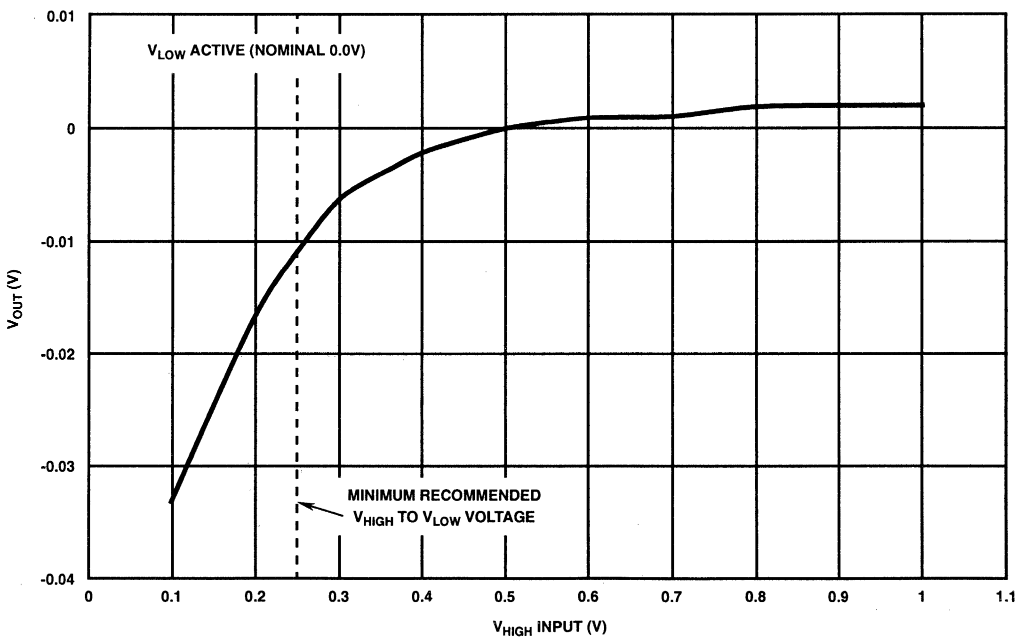


FIGURE 8. V_{HIGH}/V_{LOW} INTERACTION

Typical Performance Curves (Continued)

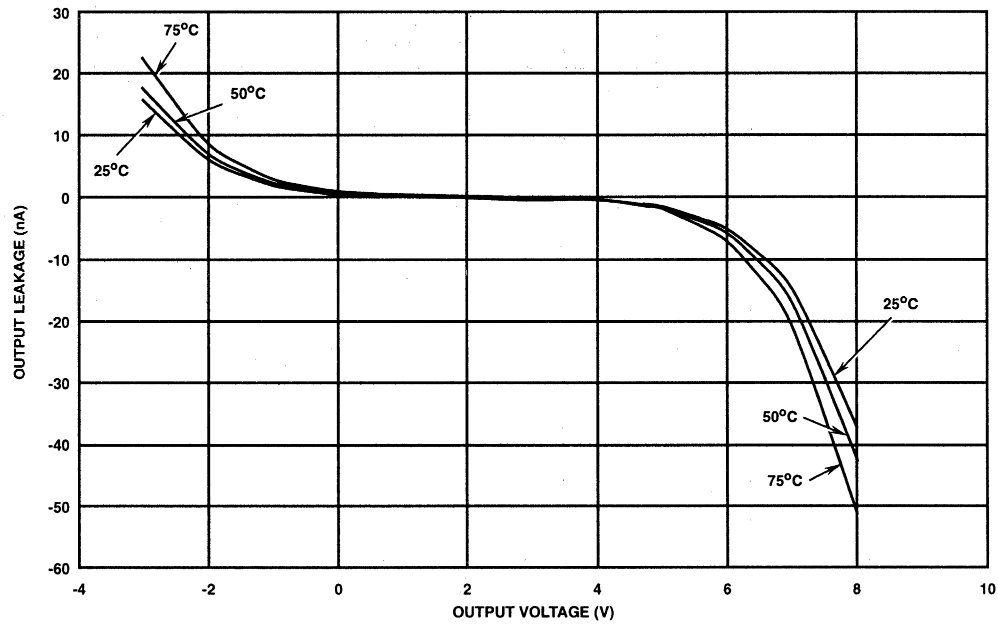


FIGURE 9. HIZ OUTPUT LEAKAGE

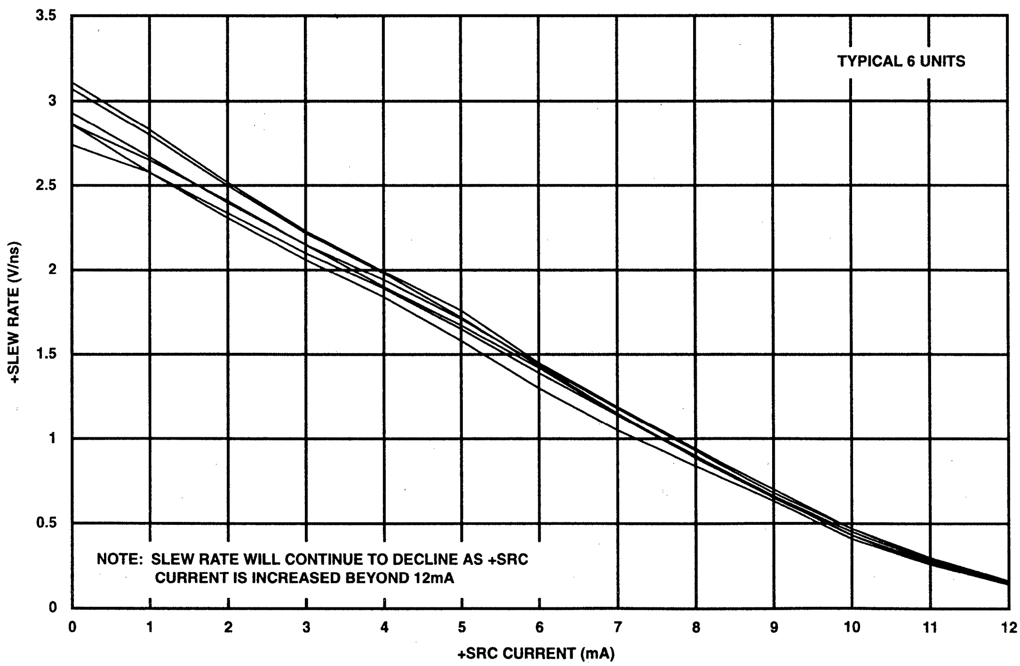


FIGURE 10. (+) SLEW RATE vs I_{STEAL}

Typical Performance Curves (Continued)

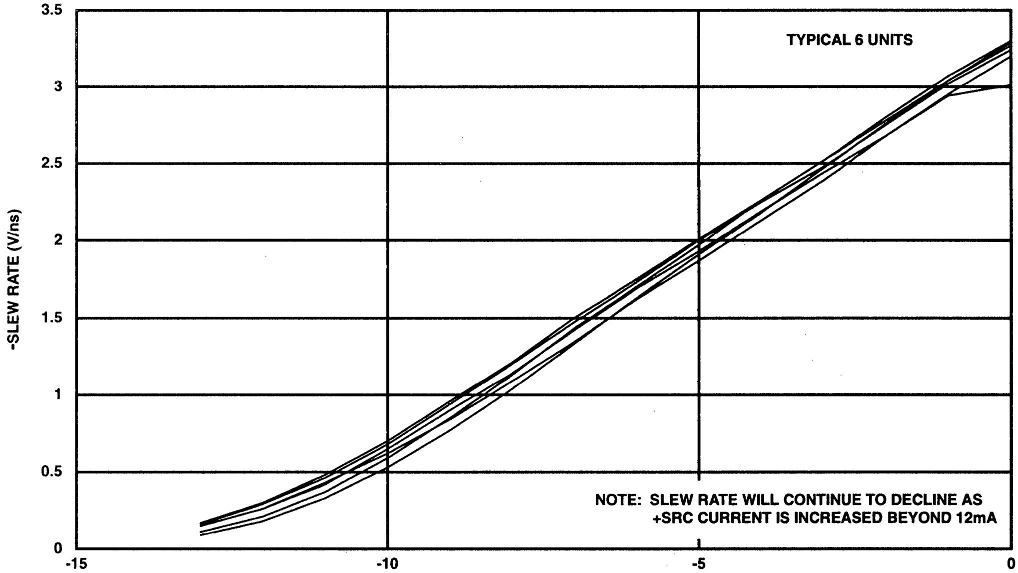
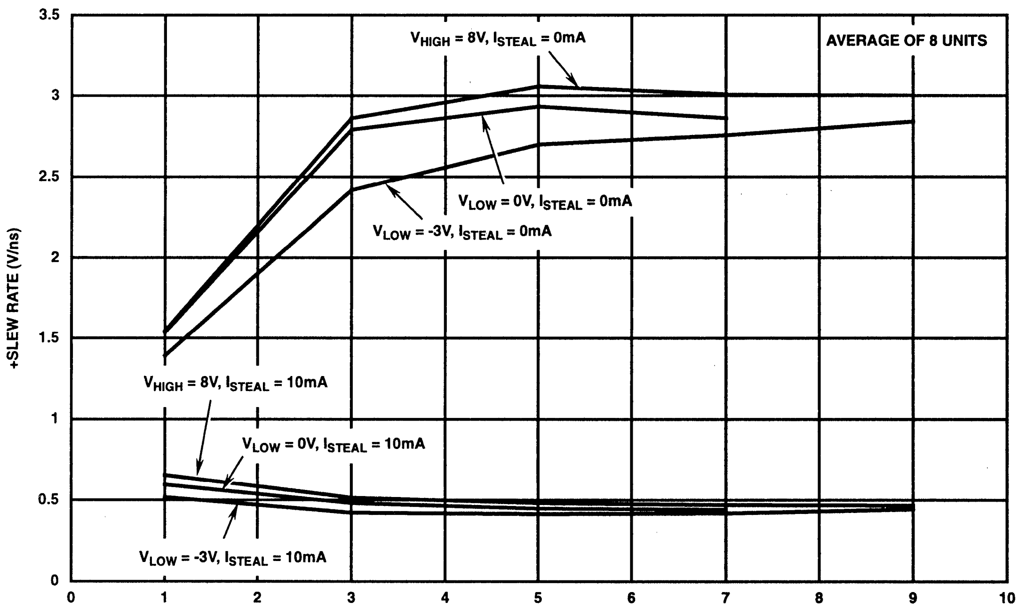


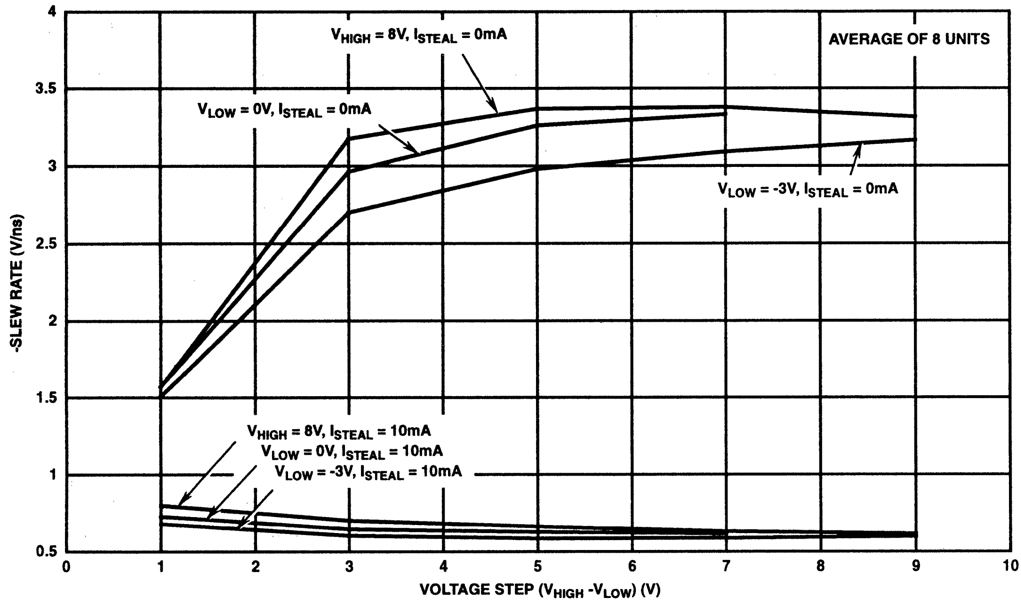
FIGURE 11. (-) SLEW RATE vs I_{STEAL}



NOTE: The family of curves shows slew rate as a function of common mode voltage. A voltage is provided for each trace specifying one level of the voltage step for which slew rate is measured. Example 1: Top Trace (V_{HIGH} = 8V, I_{STEAL} = 0mA). A voltage step of 1V goes from V_{LOW} = 7V to V_{HIGH} = 8V and a voltage step of 9V goes from V_{LOW} = -1V to V_{HIGH} = 8V. Example 2: Trace (V_{LOW} = -3V, I_{STEAL} = 0mA). A voltage step of 1V goes from V_{LOW} = -3V to V_{HIGH} = -2V and a voltage step of 9V goes from V_{LOW} = -3V to V_{HIGH} = 6V.

FIGURE 12. (+) SLEW RATE vs AMPLITUDE

Typical Performance Curves (Continued)



NOTE: The family of curves shows slew rate as a function of common mode voltage. A voltage is provided for each trace specifying one level of the voltage step for which slew rate is measured. Example 1: Top Trace (V_{HIGH} = 8V, I_{STEAL} = 0mA). A voltage step of 1V goes from V_{HIGH} = 8V to V_{LOW} = 7V and a voltage step of 9V goes from V_{HIGH} = 8V to V_{LOW} = -1V. Example 2: Trace (V_{LOW} = -3V, I_{STEAL} = 0mA). A voltage step of 1V goes from V_{HIGH} = -2V to V_{LOW} = -3V and a voltage step of 9V goes from V_{HIGH} = 6V to V_{LOW} = -3V.

FIGURE 13. (-) SLEW RATE vs AMPLITUDE

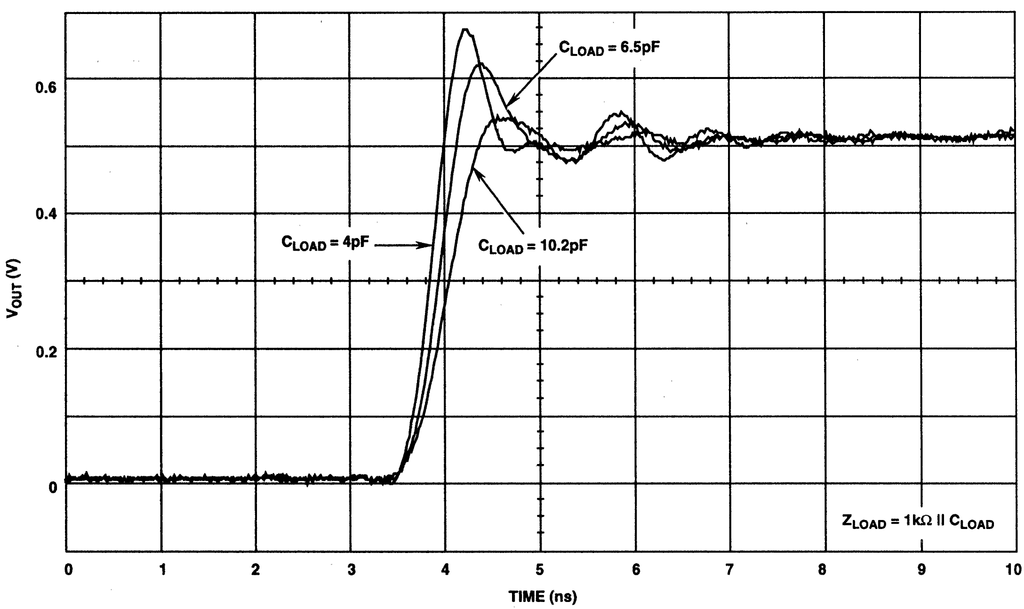


FIGURE 14. 0.5V STEP RESPONSE vs C_{LOAD}

Typical Performance Curves (Continued)

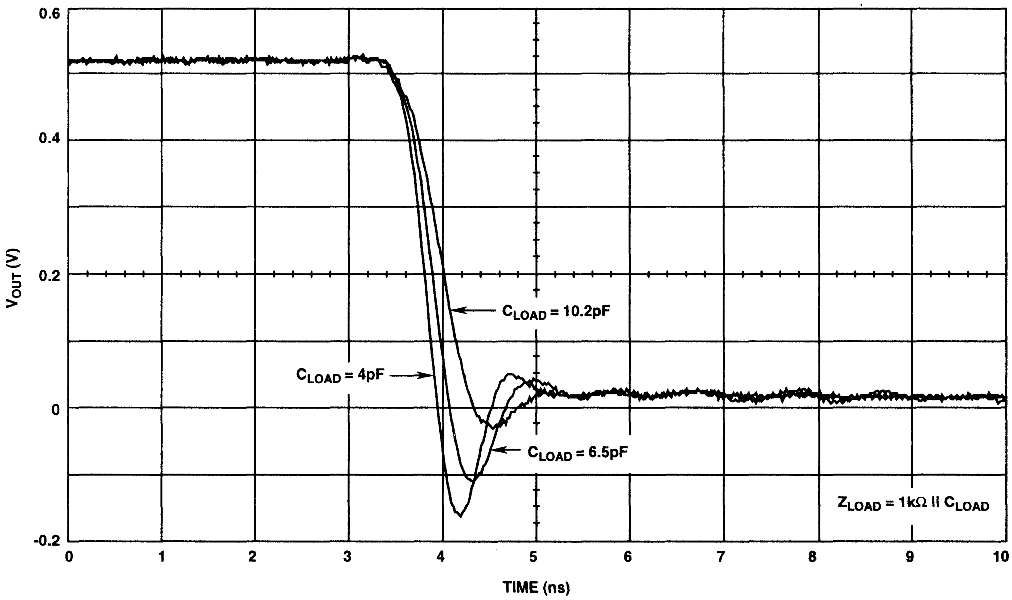


FIGURE 15. 0.5V STEP RESPONSE vs C_{LOAD}

Application Information

The HFA5253 is a pin driver designed for use in automatic test equipment (ATE) and high speed pulse generators. Pin drivers, especially those with very high-speed performance, have generally been implemented with discrete transistors (sometimes GaAs) on a circuit board or in a hybrid. Recent IC process improvements, specifically Harris' UHF1 process[2], have enabled the manufacturing of the 500MHz and 800MHz silicon monolithic pin drivers, HFA5250, HFA5251 and now the HFA5253.

The ultra high speed performance of the HFA5253 is a result of UHF1 process leverages: low parasitic collector-to-substrate capacitance of the bonded wafer, low collector-to-base parasitic capacitance of the self-aligned base/emitter technology and ultra high f_T NPN (8GHz) and PNP (5.5GHz) poly-silicon transistors.

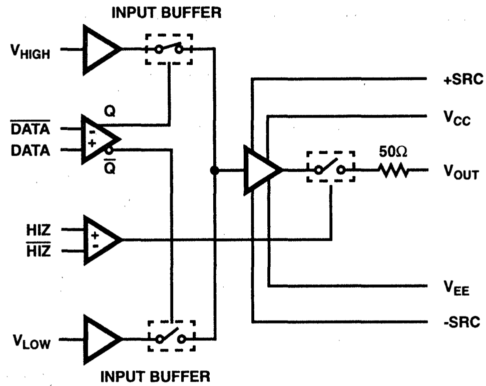


FIGURE 16. BLOCK DIAGRAM

Functional Block Diagram

The HFA5253 functional block diagram is shown in Figure 16.

The control inputs, DATA and $\overline{DATA}$, determines the output level. If DATA is at logic "1" and $\overline{DATA}$ is at logic "0", the output level will be the same as V_{HIGH}. If DATA is at logic "0" and $\overline{DATA}$ is at logic "1", the output will be the same as V_{LOW}. The control inputs, HIZ and $\overline{HIZ}$, cause the output to become either active or high-impedance. If HIZ is at logic "1" and $\overline{HIZ}$ is at logic "0", the output will be in high impedance mode. If HIZ is at logic "0" and $\overline{HIZ}$ is at logic "1", the output will be enabled. The output impedance in the enabled mode is trimmed to 50Ω.

Circuit Schematic

The Pin Driver circuit consists of a switch, an output buffer, and two differential control elements as shown in Figure 17.

A two stage approach, separating the switch from the output buffer, allows the speed and accuracy requirements of the switch to be de-coupled from the load driving capability of the buffer.

The patented switch circuitry[3] uses cascaded emitter followers as input buffers and also to switch the input V_{HIGH} and V_{LOW} to node VSO. Dual differential pairs controlled by the data timing (DATA and $\overline{DATA}$) direct current to select

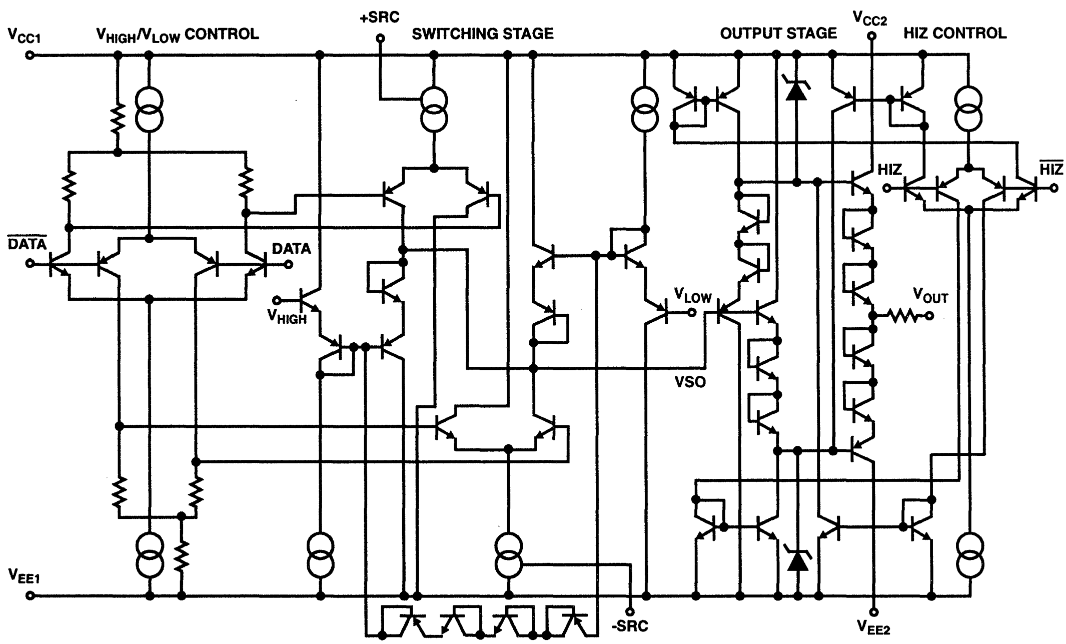


FIGURE 17. CIRCUIT SCHEMATIC

either the V_{HIGH} or V_{LOW} switch. Matching transistor types and transdiodes improve linearity and lowers the voltage offset and offset drift. Stacking two emitter-base junctions allows the V_{HIGH} to V_{LOW} range to be extended to two Emitter - Base breakdown voltages of the process. The speed of the pin driver is largely determined by the current flowing through the switch stage and the collector-base capacitance of the output stage transistors connected to the node VSO. The Slew Rate Control Pins, +SRC and -SRC, allow the user to control the amount of current available in the V_{HIGH} and V_{LOW} switch, respectively and thus the slew rate of node VSO.

The output stage consists of cascaded emitter followers constructed in a typical push-pull manner as shown in Figure 17. However, transdiodes are added to increase the voltage breakdown characteristics of the output during high impedance mode. HIZ and $\overline{HIZ}$ control the mode of the output stage. A trimmed, NiCr resistor is added to provide the 50Ω output impedance.

Overall, a symmetry of device types and paths is constructed to improve slew and delay symmetry. Both the V_{HIGH} to V_{OUT} path and the V_{LOW} to V_{OUT} path contain three NPN and three PNP transistors operating at similar collector currents. Thus the transient response of V_{HIGH} to V_{LOW} and V_{LOW} to V_{HIGH} are kept symmetrical. Also, a trimmable current reference (not shown) allows the AC parameters to be adjusted to maintain unit to unit consistency.

Speed Advantage

Harris Pin Drivers on bonded-wafer technology definitely have a speed advantage, coming from the low collector-to-substrate capacitance and the high f_T of the transistors. In addition, the patented switching stage which fits uniquely to Harris' UHF1 process is another big contributor for the high speed. This switching circuitry requires low series-resistance NPN and PNP transdiodes available in UHF1. The rise and fall times of the pin driver are largely determined by the slew rate at the node VSO in Figure 17. The dominant mechanism for the slew rate is the charging/discharging of the collector-base capacitors of the transistors connected to the node VSO. The charging/discharging currents are coming from the switching stage current sources. The fast rise and fall times are achieved because of the negligible collector-to-substrate capacitance and the small base-collector capacitance due to the self-aligned recessed oxide [2].

The DATA/$\overline{DATA}$ differential stage is not a factor for the speed if its current sources have enough current not to bottleneck the transient. However it should be noted that the propagation delay mismatch is determined by this stage. Sufficient current is allocated to the differential stage current sources to best match the low-to-high and high-to-low transient propagation delays.

The specified load condition is a 16 inch 50Ω SMA cable with a 5pF capacitor at the end of the cable. This load simulates a typical ATE environment for a DUT (Device Under Test) with high impedance (>1kΩ) digital inputs. The rise/fall time for HFA5253 with $5V_{P-P}$ is typically 1.3ns. Pin drivers, built out of the same circuit structure as shown in Figure 17, can be made faster by trimming for a higher power supply current. Currently the pin driver has rise/fall times of less than 1ns (10% to 90% of $5V_{P-P}$) when I_{CC} is trimmed to 125mA. Further speed enhancement will be made if there is a market demand.

Basic ATE System Application

Figure 18 shows a pin driver in a typical per-pin ATE system. The pin driver works closely with the Dual-Level Comparator and the Active Load. When the DUT pin acts as an input waiting for a series of digital signals, the pin driver becomes active with a logic "0" applied on the HIZ pin and provides

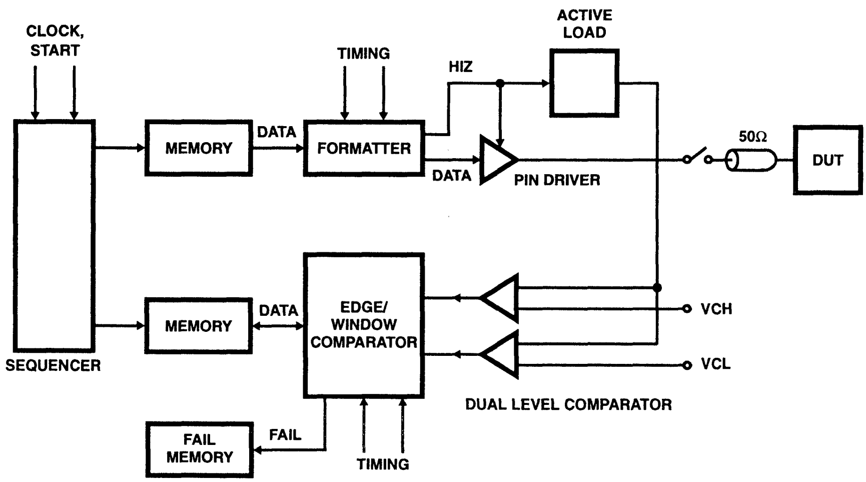


FIGURE 18. TYPICAL ATE SYSTEM

the DUT pin with digital signals. When the DUT pin acts as an output, the pin driver output will be in high impedance mode (HIZ) with a logic "1" applied to the "HIZ" pin. During this high impedance mode the pin driver presents a capacitance of less than 5pF to the DUT. Special care has to be taken to match the impedance (to 50Ω) at the pin driver output to minimize reflections.

The Dual-Level Comparator detects the logic levels of the DUT pin when it acts as an output. The comparator has two threshold level inputs, VCH and VCL. The logic level information of the DUT pin output is sent to the edge/window comparator through the Dual-Level Comparator. The edge/window comparator interprets this information in terms of corresponding transient performance in conjunction with the timing information. Thus it detects any possible failure transients.

The formatter sends a sequence of digital information to the pin driver which contains logic information over time. The Active Load is enabled when the DUT pin acts as an output. It simulates the load of the DUT pin by sinking or sourcing programmed current. Finally the sequencer controls the overall activities of the automatic testing.

Decoupling Circuit for Oscillation-Free Operation

To ensure oscillation-free operation in ATE or pulse generator applications, the pin driver needs an appropriate decoupling circuit on a printed circuit board which consists of chip capacitors and chip resistors. Figures 19, 20, and 21 refer to a proven decoupling circuit currently working in the lab and a 1X scale film of its associated PC board (metal level). Do not connect the V_{CC1} and V_{CC2} pins or the V_{EE1} and V_{EE2} pins together immediately, rather run separate traces until they can be joined at a large by-pass capacitor (0.1μF II 10.0μF).

PARTS LIST

QTY	VALUE	COMPONENT
6	470pF	Chip Cap: 0805
4	0.1μF	Chip Cap: 0805
2	10μF	Tant.
8	50Ω	Chip Res: 0805
2	100Ω	Chip Res: 0805
7	SMA Jacks	Wide Body
1	20 Lead PSOP	HFA5253
4	4-40	1" Standoff
4	4-40	1/4" Screws
2	Twisted Wire Assemblies with 4 Wires Each: One for V_{CC}, V_{HIGH}, +SRC, GND; and 1 for V_{EE}, V_{LOW}, -SRC, GND.	

The control pins, DATA, $\overline{\text{DATA}}$, HIZ, and $\overline{\text{HIZ}}$ are fed ECL signals through 50Ω micro-strip lines terminated with 50Ω for impedance matching since the input impedance at these pins is much higher than 50Ω. At the end of the micro-strip lines there is usually a high-speed pulse generator with an output impedance of 50Ω. A 50Ω micro-strip line is connected to each of the pins, $\overline{\text{DATA}}$ and $\overline{\text{HIZ}}$ through a 50Ω chip resistor to monitor the pulse signals.

The input pins, V_{HIGH}, V_{LOW}, +SRC, and -SRC need to be protected from any capacitively coupled AC noise. Normally this protection can be achieved by having a low pass filter consisting of a 50Ω chip resistor and a chip capacitor, 470pF for V_{HIGH}/V_{LOW} and 0.1μF for +SRC/-SRC. Without this protection circuit the pin driver may oscillate due to signals fed back from the output through the PC board ground.

The power supply pins, V_{CC1}, V_{CC2}, V_{EE1}, and V_{EE2}, require decoupling chip capacitors of 470pF, 0.1μF, 10μF. Having decoupling capacitors close to V_{CC2} and V_{EE2} is essential since large AC current will flow through either V_{CC2} or V_{EE2} during transients.

The output of the pin driver is usually connected to the device-under-test (DUT) through 50Ω micro-strip line and coaxial cable which carries the signal to a high input impedance DUT pin.

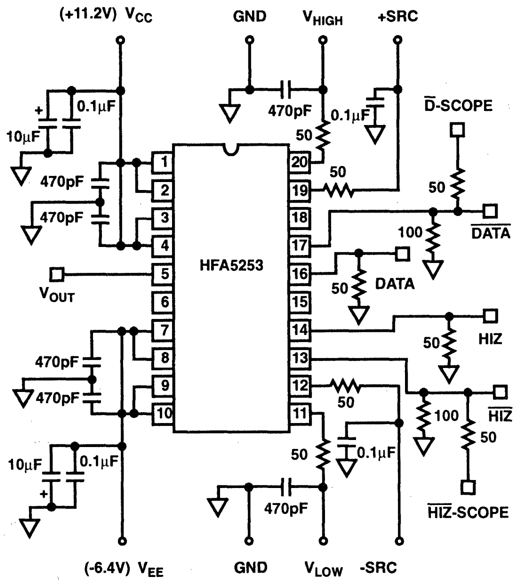


FIGURE 19. DECOUPLING CIRCUIT SCHEMATIC

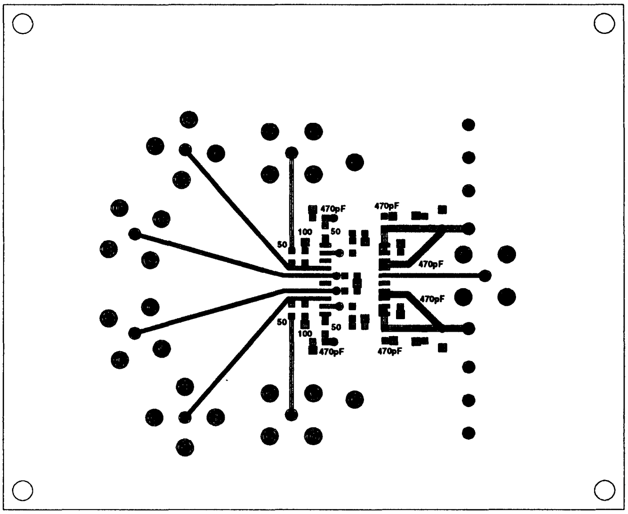


FIGURE 20. 1X PC BOARD LAYOUT (BOTTOM VIEW)

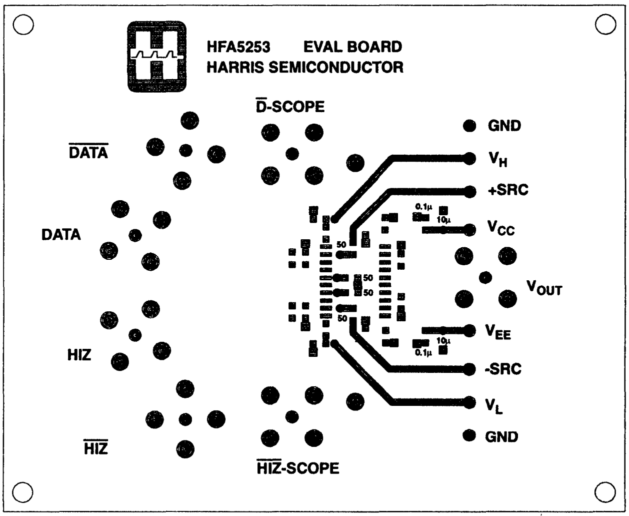


FIGURE 21. 1X PC BOARD LAYOUT (TOP VIEW)

References

[1] Taewon Jung and Donald K. Whitney Jr., "A 500MHz ATE Pin Driver," Bipolar Circuits and Technology Meeting Proceedings, pp 238-241, October 1992.

[2] Chris K. Davis et. al., "UHF1: A High Speed Complementary Bipolar Analog Process on SOI," Bipolar Circuits and Technology Meeting Proceedings, pp 260-263, October 1992.

[3] Donald K. Whitney Jr., "Symmetrical, High Speed, Voltage Switching Circuit," United States Patent Pending, Filed November 1991.

SIGNAL PROCESSING NEW RELEASES 10

DSP FILTERS

PAGE

DSP FILTER DATA SHEETS

10

DSP FILTERS

HSP43124

July 1995

Serial I/O Filter

Features

- 45MHz Clock Rate
- 256 Tap Programmable FIR Filter
- 24-Bit Data, 32-Bit Coefficients
- Cascade of up to 5 Half Band Filters
- Decimation from 1 to 256
- Two Pin Interface for Down Conversion by $F_S/4$
- Multiplier for Mixing or Scaling Input with an External Source
- Serial I/O Compatible with Most DSP Microprocessors

Applications

- Low Cost FIR Filter
- Filter Co-Processor
- Digital Tuner

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43124PC-45	0°C to +70°C	28 Lead Plastic DIP
HSP43124PC-33	0°C to +70°C	28 Lead Plastic DIP
HSP43124SC-45	0°C to +70°C	28 Lead Plastic SOIC (W)
HSP43124SC-33	0°C to +70°C	28 Lead Plastic SOIC (W)
HSP43124SI-40	-40°C to +85°C	28 Lead Plastic SOIC (W)

Description

The Serial I/O Filter is a high performance filter engine that is ideal for off loading the burden of filter processing from a DSP microprocessor. It supports a variety of multistage filter configurations based on a user programmable filter and fixed coefficient halfband filters. These configurations include a programmable FIR filter of up to 256 taps, a cascade of from one to five halfband filters, or a cascade of halfband filters followed by a programmable FIR. The half band filters each decimate by a factor of two, and the FIR filter decimates from one to eight. When all six filters are selected, a maximum decimation of 256 is provided.

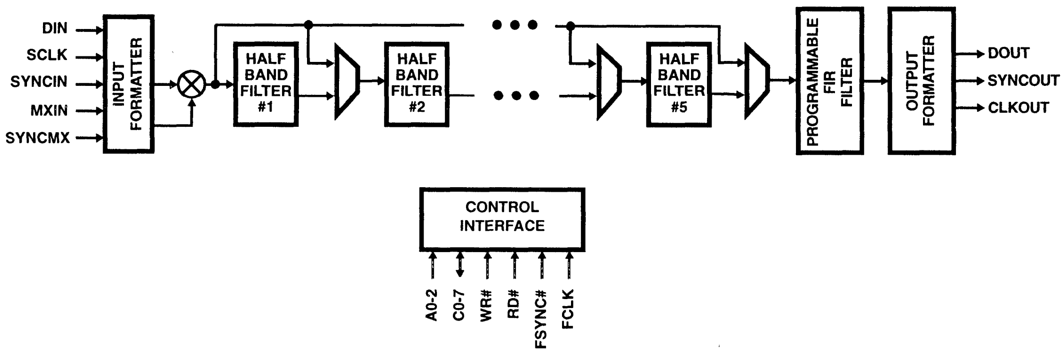
For digital tuning applications, a separate multiplier is provided which allows the incoming data stream to be multiplied, or mixed, by a user supplied mix factor. A two pin interface is provided for serially loading the mix factor from an external source or selecting the mix factor from an on-board ROM. The on-board ROM contains samples of a sinusoid capable of spectrally shifting the input data by one quarter of the sample rate, $F_S/4$. This allows the chip to function as a digital down converter when the filter stages are configured as a low-pass filter.

The serial interface for input and output data is compatible with the serial ports of common DSP microprocessors. Coefficients and configuration data are loaded over a bidirectional eight bit interface.

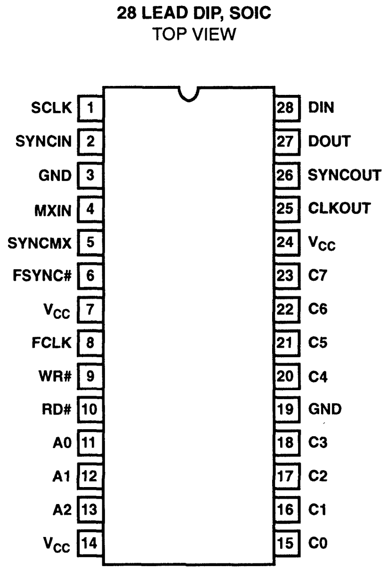
10

DSP FILTERS

Block Diagram



Pinout


28 LEAD DIP, SOIC
TOP VIEW
SCLK 1
SYNCIN 2
GND 3
MXIN 4
SYNCMX 5
FSYNC# 6
V_{CC} 7
FCLK 8
WR# 9
RD# 10
A0 11
A1 12
A2 13
V_{CC} 14
28 DIN
27 DOUT
26 SYNCOUT
25 CLKOUT
24 V_{CC}
23 C7
22 C6
21 C5
20 C4
19 GND
18 C3
17 C2
16 C1
15 C0

Pin Description

NAME	PDIP, SOIC PIN	TYPE	DESCRIPTION
V_{CC}	7, 14, 24	-	+5V Power Supply
GND	3, 19	-	Ground
DIN	28	I	Serial Data Input. The bit value present on this input is sampled on the rising edge of SCLK. A "HIGH" on this input represents a "1", and a low on this input represents "0". The word format and operation of serial interface are contained in the Data Input Section.
SYNCIN	2	I	Data Sync. The HSP43124 is synchronized to the beginning of a new data word on DIN when SCLK samples SYNCIN "HIGH" one SCLK before the first bit of the new word. Note: SYNCIN should not maintain a "HIGH" state for longer than one SCLK cycle.
SCLK	1	I	Serial Input CLK. The rising edge of SCLK clocks data on DIN and MXIN into the part. The following signals are synchronous to this clock: DIN, SYNCIN, MXIN, SYNCMX.
MXIN	4	I	Mix Factor Input. MXIN is the serial input for the mix factor. It is sampled on the rising edge of SCLK. A "HIGH" on this input represents a "1", and a low on this input represents "0". Also used to specify the Weaver Modulator ROM output. Details on word format and operation are contained in the Mix Factor Section.
SYNCMX	5	I	Mix Factor Sync. The HSP43124 is synchronized to the beginning of a serially input mix factor when SCLK samples SYNCMX "HIGH" one SCLK before the first bit of the new mix factor. Note: SYNCMX should only pulse "HIGH" for one SCLK cycle. Also used to specify Weaver Modulator ROM output.
FCLK	8	I	Filter Clock. The filter clock determines the processing speed of the Filter Compute Engine. Clock rate requirements on FCLK for particular filter configurations is discussed in the Filter Compute Engine Section. This clock may be asynchronous to the serial input clock (SCLK). FSYNC# is synchronous to this clock.
FSYNC#	6	I	Filter Sync. This input, when sampled low by the rising edge of FCLK, resets the filter compute engine so that the data sample following the next SYNCIN cycle is the first data sample into the filter structure. If a data stream is currently being input, the current sum of products and the input data are "canceled" and the DIN pin is ignored until the next SYNCIN cycle occurs.
WR#	9	I	Write. The falling edge of WR# loads data present on C0-7 into the configuration or coefficient register specified by the address on A0-2. The WR# signal is asynchronous to all other clocks. Note: WR# should not be low when RD# is low.
RD#	10	I	Read. The falling edge of RD# accesses the control registers or coefficient RAM addressed by A0-2 and places the contents of that memory location on C0-7. When RD# returns "HIGH" the C0-7 bus functions as an input bus.The RD# pin is asynchronous to all other clocks. Note: RD# should not be low when WR# is low.
A0-2	11, 12, 13	I	Address Bus. The A0-2 inputs are decoded on the falling edge of both RD# and WR#. Table 1 shows the address map for the control registers.
C0-7	15, 16, 17, 18, 20, 21, 22, 23	I/O	Control and Coefficient bus. This bi-directional bus is used to access the control registers and coefficient RAM.
CLKOUT	25	O	Output Clock. Programmable bit clock for serial output. Note: assertion of FILTSYNC# initializes CLKOUT to a high state.
SYNCOUT	26	O	Output Data Sync. SYNYOUT is asserted HIGH for one CLKOUT cycle before the first bit of a new output sample is available on DOUT.
DOUT	27	O	Serial Data Output. The bit stream is synchronous to the rising edge of CLKOUT. See the Serial Output Formatter section for additional details.

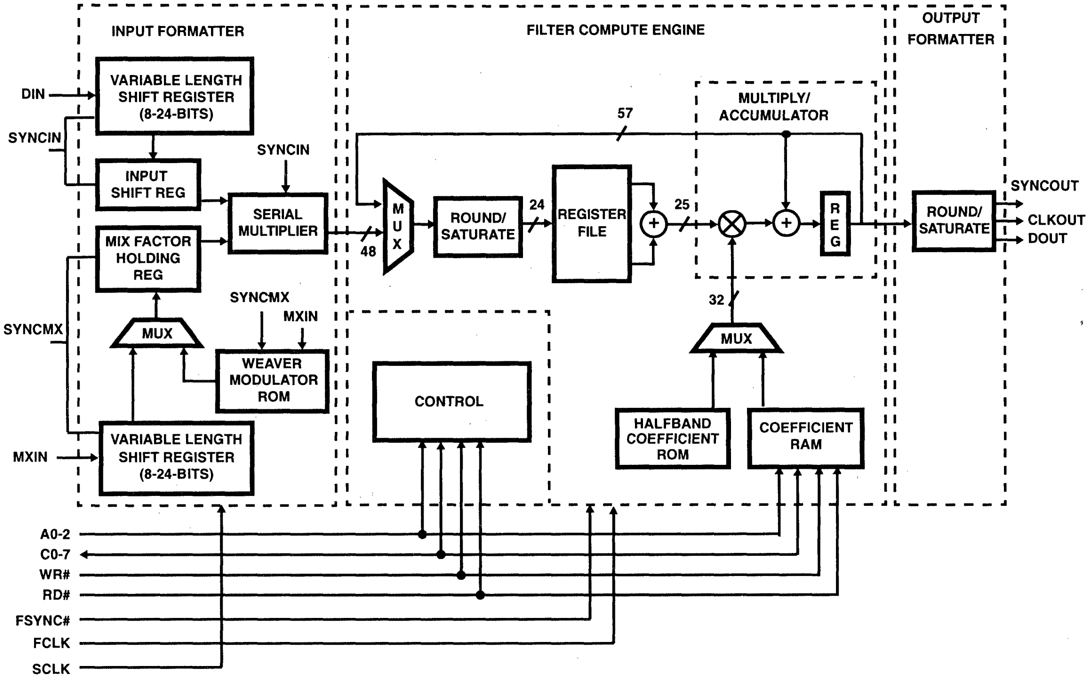


FIGURE 1. SERIAL FILTER BLOCK DIAGRAM

Functional Description

The HSP43124 is a high performance digital filter designed to process a data stream which is input serially. A second serial input is provided for inputting mix factors which are multiplied by the input samples as shown in Figure 1. The result of this operation is passed to the Filter Compute Engine for processing.

The Filter Compute Engine centers around a single multiply/ accumulator (MAC). The MAC performs the sum-of-products required by a particular filter configuration. The processing rate of the MAC is determined by the filter clock, FCLK. Increasing FCLK relative to the input sample rate increases the length of filter that can be realized.

The filtered results are passed to the Output Formatter where they are rounded or truncated to a user defined bit width. The Output Formatter then generates the timing and synchronization signals required to serially transmit the data to an external device.

Filter Configuration

The HSP43124 is configured for operation by writing a series of control registers. These registers are written through a bidirectional interface which is also used for reading the control registers. The interface consists of an 8-bit data bus, C0-7, a 3-bit address bus, A0-2, and read/write lines, RD# and WR#. The address map for the control registers is shown in Table 1.

Data is written to the control registers on the falling edge of the WR# input. This requires that the address, A0-2, and data, C0-7, be set up to the falling edge of the WR# as shown in Figure 2. Note: WR# should not be active low when RD# is active low.

Data is read from the control registers on the falling edge of the RD# input. The contents of a particular register are accessed by setting up an address, A0-2, to the falling edge of RD# as shown in Figure 2. The data is output on C0-7. The data on C0-7 remains valid until RD# returns HIGH, at which point the C0-7 bus is Three-Stated and functions as an input. For proper operation, the address on A0-2 must be held until RD# returns "high" as shown in Figure 2. Note: RD# should not be active low when WR# is active low.

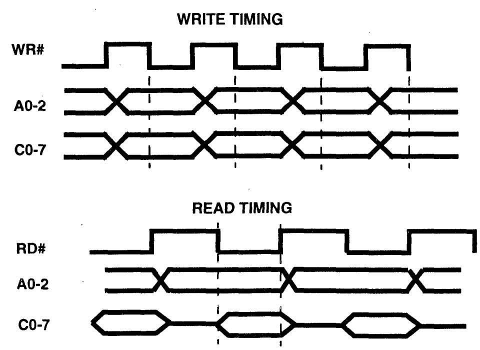


FIGURE 2. READ/WRITE TIMING

TABLE 1. CONFIGURATION REGISTERS

ADDRESS	REGISTER DESCRIPTION	BIT POSITIONS	BIT FUNCTION
000	Filter Configuration	2-0	Specifies the number of halfbands to use. Number ranges from 0 to 5. Other values are invalid.
		3	Filter Enable bit. 1 = Enable.
		4	Coefficient read enable. When set to 1, enables reading and disables writing of coefficient RAM. Note: this bit must be set to 0 prior to writing the Coefficient RAM.
		7-5	Decimation Rate. Range is 1-8 (8 = 000).
001	Programmable Filter Length	7-0	Number of Taps in the Programmable Filter. For even or odd symmetric filters, values range from 4- 256, 1 to 3 are invalid, and 0000000 = 256. For asymmetric filters, the value loaded in this register must be two times the actual number of coefficients.
010	Coefficient RAM Access	7-0	Coefficient RAM is loaded by multiple writes to this address. See Writing Coefficients section for additional details.
011	Input Format	4-0	Number of bits in input data word, from 8 (01000) to 24 (11000). Values outside the range of 8 - 24 are invalid.
		5	Number System. 0 = Two's Complement, 1 = Offset Binary.
		6	Serial Format. 1 = MSB First, 0 = LSB First.
		7	Unused
100	Output Timing	4-0	Number of FCLKS per CLKOUT. Range 1 to 32. (00000 = 32 FCLKS)
		5	1 = MSB First, 0 = LSB First.
		6-7	Unused
101	Output Format	4-0	Number of bits in output data word, from 8 to 32. A value of 32 is represented by 00000, and values from 1 to 7 are invalid.
		5	Round Select. 0 = Round to Selected Number of Bits, 1 = Truncate.
		6	Number System. 0 = Two's Complement, 1 = Offset Binary.
		7	Gain Correction. 1 = Apply scale factor of 2 to data. 0 = No Scaling.
110	Filter Symmetry	1-0	00 = Even Symmetric FIR Coefficients 01 = Non-Symmetric Coefficients 10 = Odd Symmetric FIR
		7-2	Reserved: Must be 0.
111	Mix Factor Format	4-0	Number of bits in mix factor, from 8 (01000) to 24 (11000). Values outside the range of 8 - 24 are invalid.
		5	Serial Format. 1 = MSB First, 0 = LSB First.
		6	Mix Factor Select. 1 = Serial Input, 0 = Weaver modulator look-up-table.
		7	Unused

Writing Coefficients

The HSP43124 provides a register bank to store filter coefficients for configurations which use the programmable filter. The register bank consists of 128 thirty-two-bit registers. Each register is loaded by 4 one byte writes to the bidirectional interface used for loading the configuration registers. The coefficients are loaded in order from least significant byte (LSB) to most significant byte (MSB).

The coefficient registers are loaded by first setting the coefficient read enable bit to "0" (bit 4 of the Filter Configuration Register). Next, coefficients are loaded by setting the A2-0 address to 010 (binary) and writing one byte at a time as shown in Figure 3. The down loaded bytes are stored in a holding register until the 4th write cycle. On completion of the fourth write cycle, the contents of the holding register are loaded into the Coefficient RAM, and the write pointer is incremented to the next register. If the user attempts to write more than 128 coefficients, the pointer halts at the 128th register location, and writing is disabled. The coefficient address pointer is reset when any other configuration register is written or read. Note: a new coefficient set may be loaded during a filter calculation at the risk of corrupting output data until the load is complete.

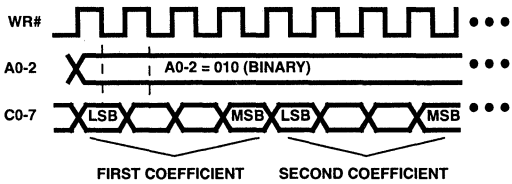
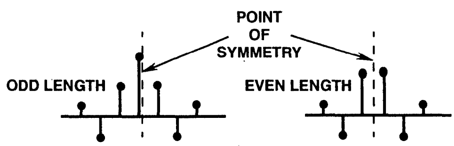


FIGURE 3. COEFFICIENT LOADING

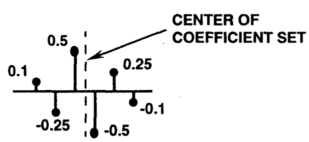
The number of coefficients that must be loaded is dependent on whether the coefficient set exhibits even symmetry, odd symmetry, or asymmetry (see Figure 4).

EVEN SYMMETRIC



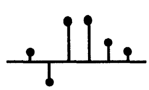
NOTE: Filters with even symmetric coefficients exhibit symmetry about the center of the coefficient set. Most FIR filters have coefficients which are symmetric in nature.

ODD SYMMETRIC



NOTE: Odd symmetric coefficients have a coefficient envelope which has the characteristics of an odd function (i.e. coefficients which are equidistant from the center of the coefficient set are equal in magnitude but opposite in sign). Coefficients designed to function as a differentiator or Hilbert Transform exhibit these characteristics.

ASYMMETRIC



NOTE: Asymmetric Coefficient sets exhibit no symmetry.

FIGURE 4. COEFFICIENT CHARACTERISTICS

For filters that exhibit either even or odd symmetry, only the unique half of the coefficient set must be loaded. The coefficients are loaded in order starting with the first filter tap and ending with the center tap. The coefficient associated with the first tap is the first to be multiplied by an incoming data sample as shown in Figure 5. For even/odd symmetric filters of length N, N/2 coefficients must be loaded if the filter length is even, and (N+1)/2 coefficients must be loaded if the filter length is odd. For example, a 17 tap symmetric filter would require the loading of 9 coefficients. Enough storage is provided for a 256 tap symmetric filter.

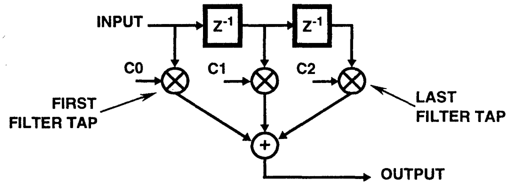


FIGURE 5. THREE TAP TRANSVERSAL FILTER ARCHITECTURE

For asymmetric filters the entire coefficient set must be loaded. The coefficients are loaded in order starting with the first tap and ending with the final filter tap (see Figure 5 for tap/coefficient association). Enough storage is provided for a 128 tap asymmetric filter. For asymmetric filters the value loaded into the Programmable Filter Length Register addressed must be twice the actual number of coefficients.

Reading Coefficients

The coefficients are read from the storage registers one byte at a time via C0-7 as shown in Figure 6. To read the coefficients, the user first sets the Coefficient Read Enable bit to 1 (bit 4 of Filter Configuration Register). Setting this bit resets the RAM read pointer and disables the RAM from being written. Next, with A2-0 = 010, multiple "high" to "low" transitions of RD#, output the coefficients on C0-7, one byte at a time, in the order they were written. Note: RD# should not be "low" when WR# is "low".

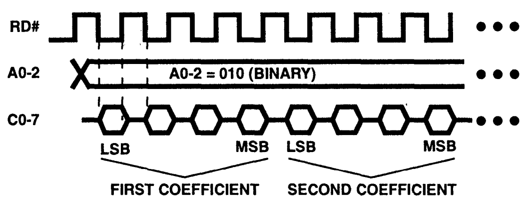
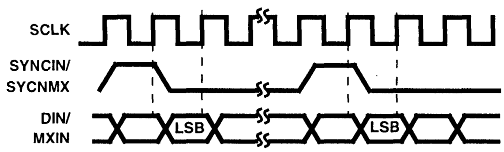


FIGURE 6. COEFFICIENT READING

Data Input

Data is serially input to the HSP43124 through the DIN input. On the rising edge of SCLK, the bit value present at DIN is clocked into the Variable Length Shift Register. The beginning of a serial data word is designated by asserting SYNCIN "high" one SCLK prior to the first data bit as shown in Figure 7. On the following SCLK, the first data bit is clocked into the Variable Length Shift Register. Data bits are clocked into the shift register until the data word, of user programmable length (8 to 24-bits), is complete. At this point, the shifting of data into the register is disabled and its contents are held until SYNCIN is asserted on the rising edge of SCLK. When this occurs, the contents of the Variable Length Shift Register are transferred to the Input Holding Register, and the shift register is enabled to accept serial data on the following SCLK. The serial data word may be two's complement or offset binary and may be input most significant bit (MSB) first or least significant bit (LSB) first as defined in the Input Format Register (see Table 1). If a data word is specified to be less than 24-bits, the least significant bits of the Input Holding Register are zeroed. Note: SYNCIN should not be "high" for longer than one SCLK cycle.



NOTE: Assumes data is being loaded LSB first.

FIGURE 7. SERIAL INPUT TIMING FOR EITHER DIN OR MXIN INPUTS

Mix Factor

The HSP43124 provides a second serial interface for loading values which are multiplied by the input samples in the serial multiplier. These values, or mix factors, are input using the MXIN and SYNCMX pins. Aside from being used as a serial input, this interface can also be used to select mix factors from the Weaver Modulator ROM. The mix factor source is specified in the Mix Factor Format Register (see Table 1). Note: data is passed unmodified through the serial multiplier by selecting the Weaver Modulation ROM as the mix factor source and tieing both SYNCMX and MXIN "high".

The procedure for loading mix factors serially is similar to that for the loading of data via the DIN input. The bit value present on MXIN is clocked into the Variable Length Shift register by the rising edge of SCLK. The beginning of the serial word is designated by the assertion of SYNCMX one SCLK prior to the first bit of the serial word as shown in Figure 7. After the serial word has been clocked into the shift register, the shifting of bits into the register is disabled and its contents are held until the next assertion of SYNCMX. When SYNCMX is asserted on the rising edge of SCLK, the contents of the Variable Length Shift register are transferred into the Mix Factor Holding Register. The parallel output of the Mix Factor Holding Register feeds directly into the serial multiplier. The mix factor data word is programmable in length from 8 to 24-bits and may be input MSB or LSB first as specified in the Mix Factor Format Register. If a data word is specified to be less than 24-bits, the least significant bits of the Mix Factor Holding Register are zeroed.

In configurations which use the Weaver Modulator ROM to generate the mix factors, the MXIN and SYNCMX inputs function as ROM addresses. These inputs are latched on the rising edge of SCLK when SYNCIN is high as shown in Figure 9. The mapping of SYNCIN and MXIN to ROM outputs is given in Table 2. When SYNCIN is high on the rising edge of SCLK, the output of the ROM is transferred to the Mix Factor holding register, and the SYNCMX and MXIN inputs are decoded to produce a new ROM output. As a result, there is a latency of one SYNCIN cycle between when the SYNCMX and MXIN inputs are decoded and when the ROM output is loaded into the Mix Factor Holding register.

TABLE 2. WEAVER MODULATOR ROM DECODING

SYNCMX	MXIN	MIX FACTOR
0	0	0
0	1	-1
1	0	0
1	1	1

Serial Multiplier

The Serial Multiplier multiplies the Mix Factor Holding register by the contents of the Input Holding register. The multiplication cycle is initiated when SYNCIN is sampled high by the rising edge of SCLK. This transfers the contents of the Variable Length Shift register to the Input Holding Register, and loads the output of the Mix Factor Holding Register into the Serial Multiplier. On subsequent SCLKs, the contents of the Input Holding Register are shifted into the Serial Multiplier for processing. When the last data bit is shifted into the multiplier, the multiplication cycle is complete and the result is written to the Register File on the next rising edge of FCLK.

The synchronization between a data sample and the mix factor it is to be multiplied by is dependent on which mix factor source is specified. For mix factors which are input serially, the mix factor is loaded concurrently with the data sample to be multiplied (see Figure 8).

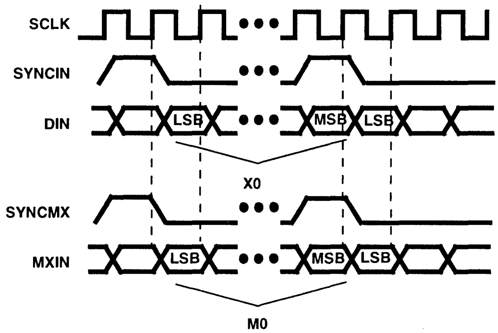


FIGURE 8. DATA/MIX FACTOR SYNCHRONIZATION FOR SERIALLY INPUT MIX FACTORS

NOTE: Figure 8 shows the loading of a data sample, X0, such that it will be multiplied by a mix factor designated by M0. For mix factor bit widths which are less than the input bit width, SYNCMX may be asserted before SYNCIN if desired.

10

DSP FILTERS

If the mix factor is generated by the Weaver Modulator ROM, the mix factor must be specified on MXIN and SYNCMX one SYNCIN before that which precedes the target data word (see Figure 9).

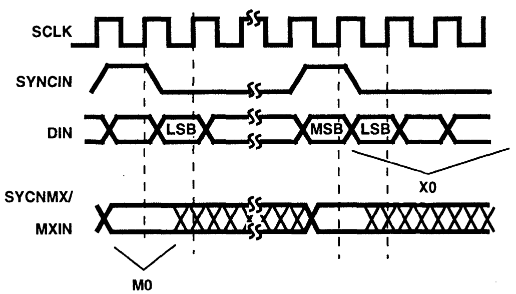


FIGURE 9. DATA/MIX FACTOR SYNCHRONIZATION WEAVER MODULATOR MIX FACTORS

NOTE: Figure 9 shows the specification of a ROM based mix factor, M0, so that it will be multiplied with the target data sample designated by X0.

Filter Compute Engine

The Filter Compute Engine centers around a multiply accumulator which is used to perform the sum-of-products required for a variety of filtering configurations. These configurations include a cascade of up to 5 halfband filters, a single symmetric filter of up to 256 taps, a single asymmetric filter of up to 128 taps, or a cascade of halfband filters followed by a programmable filter. The filter configuration is specified by programming the Filter Configuration Register (see Table 1).

The cascade of up to five halfband filters is an efficient decimating filter structure. Each fixed coefficient filter in the chain introduces a decimation of two, and the aggregate decimation rate of the entire halfband filtering stage is given by

$$DEC_{HB} = 2^{(\text{NUMBER OF HALFBAND FILTERS SELECTED})}.$$

Thus, a cascade of 3 halfband filters would decimate the input sample stream by a factor of 8.

The frequency responses of the five filters is presented graphically in Figure 10 and in tabular form in Table 3. The transition band for the fifth halfband filter, HB5, is the narrowest while that for the first halfband filter, HB1, is the widest. The cascade of the halfband filters always terminates with HB5 and is preceded by filters in order of increasing transition bandwidth. For example, if the HSP43124 is configured to operate with three halfbands, the chain of filters would consist of HB3 followed by HB4 and terminated with HB5. If only one halfband is selected, HB5 is used.

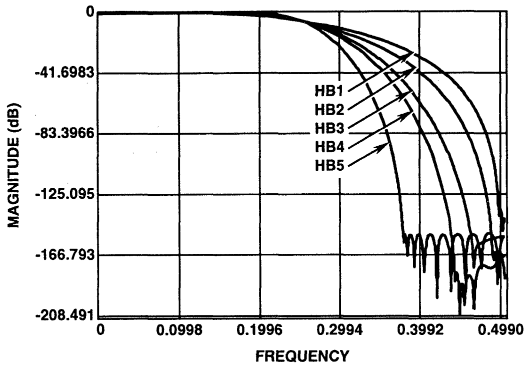


FIGURE 10. COMPOSITE RESPONSE OF FIXED COEFFICIENT HALFBAND FILTERS

The coefficients for each of the halfband filters is given in Table 4. These values are the 32-bit, two's complement, integer representation of the filter coefficients. Scaling these values by 2^{-31} yields the fractional two's complement coefficients used to achieve unity gain in the Filter Processor.

If a specific frequency response is desired, a programmable filter may be activated. The filter compute engine takes advantage of symmetry in FIR coefficients is by summing data samples sharing a common coefficient prior to multiplication. In this manner, two filter taps are calculated per multiply accumulate cycle. If an asymmetric filter is specified, only one tap per multiply accumulate cycle is calculated.

The processing rate of the Filter Compute Engine is proportional to FCLK. As a result, the frequency of FCLK must exceed a minimum value to insure that a filter calculation is complete before the result is required for output. In configurations which do not use decimation, one input sample period is available for filter calculation before an output is required. For configurations which employ decimation, up to 256 input sample periods may be available for filter calculation. The following equation specifies the minimum FCLK rate required for configurations which use the programmable filter as an FIR filter.

$$\text{Min FCLK} = (14F_S/DEC_{HB})(TAPS/(2^*DEC_{FIR}) + HB_{CLKS} + 1)$$

In this equation F_S is the sample rate, TAPS is the number of taps in the FIR filter (0 to 256), DEC_{FIR} is the decimation rate of the programmable FIR (1 to 8), and HB_{CLKS} is a compute clock factor based on the number of halfband filters in the configuration (see Table 5). The term DEC_{HB} is the aggregate decimation rate for the cascade of halfband filters (see Table 5). For example, if the input sample rate is 800kHz, a 128 tap FIR filter with no decimation is selected, and a cascade of 2 halfband filters is used, a minimum FCLK rate of 19.6MHz would be required.

NOTE: For configurations in which the halfband filters are used, the FCLK rate must exceed $14F_S$.

TABLE 3. FREQUENCY RESPONSE OF HALFBAND FILTERS

NORMALIZED FREQUENCY	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
0.000000	-0.000000	0.000000	0.000000	-0.000000	-0.000000
0.007812	0.000000	-0.000000	-0.000000	-0.000000	-0.000000
0.015625	-0.000113	-0.000000	-0.000000	-0.000000	-0.000000
0.023438	-0.000677	-0.000006	-0.000000	-0.000000	-0.000000
0.031250	-0.002243	-0.000052	-0.000000	-0.000000	-0.000000
0.039062	-0.005569	-0.000227	-0.000000	-0.000000	0.000000
0.046875	-0.011596	-0.000719	-0.000001	0.000000	-0.000000
0.054688	-0.021433	-0.001859	-0.000009	-0.000000	-0.000000
0.062500	-0.036333	-0.004165	-0.000041	-0.000000	-0.000000
0.070312	-0.057670	-0.008391	-0.000149	-0.000001	-0.000000
0.078125	-0.086916	-0.015557	-0.000448	-0.000012	-0.000000
0.085938	-0.125619	-0.026983	-0.001175	-0.000066	-0.000000
0.093750	-0.175382	-0.044301	-0.002767	-0.000258	-0.000000
0.101562	-0.237843	-0.069457	-0.005963	-0.000815	-0.000000
0.109375	-0.314663	-0.104701	-0.011924	-0.002208	-0.000000
0.117188	-0.407509	-0.152566	-0.022368	-0.005313	-0.000000
0.125000	-0.518045	-0.215834	-0.039695	-0.011613	-0.000000
0.132812	-0.647925	-0.297499	-0.067100	-0.023435	-0.000031
0.140625	-0.798791	-0.400727	-0.108640	-0.044186	-0.000287
0.148438	-0.972266	-0.528809	-0.169262	-0.078552	-0.001468
0.156250	-1.169959	-0.685131	-0.254777	-0.132639	-0.005427
0.164062	-1.393465	-0.873129	-0.371785	-0.214009	-0.016180
0.171875	-1.644372	-1.096269	-0.527552	-0.331613	-0.041152
0.179688	-1.924262	-1.358019	-0.729872	-0.495620	-0.092409
0.187500	-2.234728	-1.661842	-0.986908	-0.717181	-0.187497
0.195312	-2.577375	-2.011181	-1.307047	-1.008144	-0.349593
0.203125	-2.953834	-2.409468	-1.698769	-1.380771	-0.606862
0.210938	-3.365774	-2.860128	-2.170548	-1.847495	-0.991193
0.218750	-3.814917	-3.366593	-2.730783	-2.420719	-1.536664
0.226562	-4.303048	-3.932319	-3.387764	-3.112694	-2.278126
0.234375	-4.832037	-4.560817	-4.149669	-3.935463	-3.250174
0.242188	-5.403856	-5.255675	-5.024594	-4.900864	-4.486639
0.250000	-6.020599	-6.020600	-6.020600	-6.020600	-6.020600
0.257812	-6.684504	-6.859450	-7.145791	-7.306352	-7.884833
0.265625	-7.397981	-7.776287	-8.408404	-8.769932	-10.112627
0.273438	-8.163642	-8.775419	-9.816921	-10.423476	-12.738912
0.281250	-8.984339	-9.861469	-11.380193	-12.279667	-15.801714
0.289062	-9.863195	-11.039433	-13.107586	-14.352002	-19.344007
0.296875	-10.803663	-12.314765	-15.009147	-16.655094	-23.416153
0.304688	-11.809574	-13.693460	-17.095793	-19.205034	-28.079247
0.312500	-12.885208	-15.182171	-19.379534	-22.019831	-33.409992
0.320312	-14.035372	-16.788332	-21.873730	-25.119940	-39.508194
0.328125	-15.265501	-18.520315	-24.593418	-28.528942	-46.509052
0.335938	-16.581776	-20.387625	-27.555685	-32.274414	-54.604954
0.343750	-17.991278	-22.401131	-30.780161	-36.389088	-64.087959
0.351562	-19.502172	-24.573368	-34.289623	-40.912403	-75.444221
0.359375	-21.123947	-26.918915	-38.110786	-45.892738	-89.610390
0.367188	-22.867725	-29.454887	-42.275345	-51.390583	-108.973686
0.375000	-24.746664	-32.201569	-46.821358	-57.483341	-152.503693
0.382812	-26.776485	-35.183285	-51.795181	-64.272881	-153.443375
0.390625	-28.976198	-38.429543	-57.254162	-71.898048	-158.914017

10

DSP FILTERS

TABLE 3. FREQUENCY RESPONSE OF HALFBAND FILTERS (Continued)

NORMALIZED FREQUENCY	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
0.398438	-31.369083	-41.976673	-63.270584	-80.556969	-156.960175
0.406250	-33.984089	-45.870125	-69.937607	-90.550629	-153.317627
0.414062	-36.857830	-50.167850	-77.378593	-102.379677	-161.115540
0.421875	-40.037594	-54.945438	-85.762718	-117.007339	-153.504684
0.429688	-43.585945	-60.304272	-95.332924	-136.890198	-158.650345
0.437500	-47.588165	-66.385063	-106.462181	-185.130432	-154.637756
0.445312	-52.164894	-73.392075	-119.793030	-187.297241	-153.870453
0.453125	-57.495132	-81.640152	-136.802948	-182.300125	-161.882385
0.460938	-63.861992	-91.658478	-175.030167	-203.460876	-152.278915
0.468750	-71.755898	-104.468010	-158.939362	-174.691895	-164.329758
0.476562	-82.156616	-122.641861	-157.095886	-174.737076	-153.535690
0.484375	-97.627930	-166.537369	-155.613434	-175.108841	-153.507477
0.492188	-139.751450	-165.699081	-154.708450	-169.966568	-167.665482

TABLE 4. HALFBAND FILTER COEFFICIENTS (32-BITS, UN-NORMALIZED)

COEFFICIENT	HALFBAND #1	HALFBAND #2	HALFBAND #3	HALFBAND #4	HALFBAND #5
C0	-67230275	12724188	624169	-197705	23964
C1	0	0	0	0	0
C2	604101076	-105279784	-6983862	2303514	-242570
C3	1073741823	0	0	0	0
C4	604101076	629426509	38140187	-13225905	1306852
C5	0	1073741827	0	0	0
C6	-67230275	629426509	-145867861	51077176	-4942818
C7		0	0	0	0
C8		-105279784	650958284	-161054660	14717750
C9		0	1073741793	0	0
C10		12724188	650958284	657968488	-37027884
C11			0	1073741825	0
C12			-145867861	657968488	84032070
C13			0	0	0
C14			38140187	-161054660	-191585682
C15			0	0	0
C16			-6983862	51077176	670589251
C17			0	0	1073741824
C18			624169	-13225905	670589251
C19				0	0
C20				2303514	-191585682
C21				0	0
C22				-197705	84032070
C23					0
C24					-37027884
C25					0
C26					14717750
C27					0
C28					-4942818
C29					0
C30					1306852
C31					0
C32					-242570
C33					0
C34					23964

TABLE 5. PERFORMANCE ENVELOPE PARAMETERS

NUMBER OF HALFBANDS	HB_{CLKS}	DEC_{HB}
0	0	1
1	13	2
2	33	4
3	69	8
4	125	16
5	221	32

The longest length FIR filter realizable for a particular configuration is determined by solving the above equation for TAPS. The resulting expression is given below.

Max TAPS = $2DEC_{FIR}((FCLK/F_S)DEC_{HB} - HB_{CLKS} - 1)$

The maximum throughput sample rate may be specified by solving the above equation for F_S. The resulting equation is

Max $F_S = FCLK{*}DEC_{HB} /(TAPS/(2{*}DEC_{FIR}) + HB_{CLKS} + 1)$.

NOTE: For configurations using filters with asymmetric coefficients, the term TAPS in the above equations should be multiplied by two in order to determine the correct FCLK.

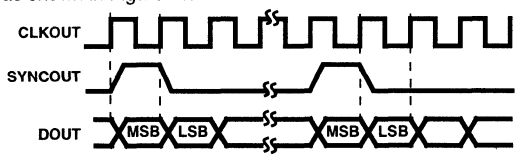
The Filter Compute Engine is synchronized with an incoming data stream by asserting the FYSNC# input. When this input is sampled low by the rising edge of FCLK, the Compute Engine is reset, and the data word following the next assertion of SYNCIN is recognized as the first data sample input to the filter structure.

Serial Output Formatter

The Output Formatter serializes the parallel output of the filter compute engine while generating the timing and synchronization signals required to support a serial interface. The Formatter produces serial data words with programmable lengths from 8 to 32-bits. The data words may be organized with either most or least significant bit first. Also, the data word may be rounded or truncated to the desired length and the format of the output data may be specified as either two's complement or offset binary. To simplify applications where the Serial I/O Filter is used as a down converter, the output formatter can be configured to scale the output by a factor of 2. The above options are programmed via the Output Format and Output Timing Registers given in Table 1.

The HSP43124 outputs a bit stream through DOUT which is synchronous to a programmable clock signal output on CLKOUT. The output clock, CLKOUT, is derived from FCLK and has a programmable rate from 1 to $^1/_{32}$ times FCLK. The duty cycle of CLKOUT is 50% for rates that have an even number of FCLKs per CLKOUT. For rates that have and odd number of FCLKs per CLKOUT the high portion of the CLKOUT waveform spans (n+1)/2 FCLKs and the low portion spans (n-1)/2 FCLKs where n is the number of FCLKs.

External devices synchronize to the beginning of an output data word by monitoring SYNCOUT. This output is asserted "high" one CLKOUT prior to the first bit of the next data word as shown in Figure 11.



NOTE: Assumes data is being output LSB first.

FIGURE 11. SERIAL OUTPUT TIMING

Input and Output Data Formats

The data formats for the input, output and coefficients are fractional two's complement. The bit weightings in the data words are given in Figure 12. Input or output data words programmed to have less than 24-bits, map to the most significant bit positions of the 24-bit word. For example, an input word defined to be 8-bits wide would map to the bit positions with weightings from -2^0 to 2^{-7}.

FRACTIONAL TWO'S COMPLEMENT FORMAT FOR 24-BIT INPUT AND OUTPUT

24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
$-2^0.$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}

FRACTIONAL TWO'S COMPLEMENT FORMAT FOR 32-BIT COEFFICIENTS

32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
$-2^0.$	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}	2^{-19}	2^{-20}	2^{-21}	2^{-22}	2^{-23}	2^{-24}	2^{-25}	2^{-26}	2^{-27}	2^{-28}	2^{-29}	2^{-30}	2^{-31}

FIGURE 12. DATA FORMATS

Absolute Maximum Ratings

Supply Voltage . . . .+7.0V
Input, Output Voltage . . . . .GND -0.5V to V_{CC} +0.5V
Storage Temperature . . . . -65°C to +150°C
ESD . . . . Class 1
Junction Temperature. . . . . +150°C (SOIC, PDIP)
Lead Temperature (Soldering 10s). +300°C
(SOIC - Lead Tips Only)
Gate Count. 40,304

Thermal Information (Typical)

Thermal Resistance θ_{JA}
SOIC Package. . . . . 65°C/W
Plastic DIP Package . . . . 55°C/W
Maximum Package Power Dissipation
SOIC Package (Commercial) +70°C. 1.23W
Plastic DIP Package (Commercial) +70°C 1.45W
SOIC Package (Industrial) +85°C 1.00W
Plastic DIP Package (Industrial) +85°C. 1.18W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range (Commercial). . . . . .4.75V to 5.25V
Operating Voltage Range (Industrial) . . . . .4.75V to 5.25V
Operating Temperature Range (Commercial). . . . . . . 0°C to +70°C
Operating Temperature Range (Industrial) . . . .-40°C to +85°C

DC Electrical Specifications (V_{CC} = 5.0V ±5%, T_A = 0° to +70°C)

PARAMETER	SYMBOL	MIN	MAX	UNITS	TEST CONDITIONS
Power Supply Current	I_{CCOP}	-	203	mA	V_{CC} = Max, FCLK = SCLK = 45MHz Notes 1, 2
Standby Power Supply Current	I_{CCSB}	-	500	uA	V_{CC} = Max, Outputs Not Loaded
Input Leakage Current	I_I	-10	10	uA	V_{CC} = Max, Input = 0V or V_{CC}
Output Leakage Current	I_O	-10	10	μA	V_{CC} = Max, Input = 0V or V_{CC}
Clock Input High	V_{IHC}	3.0	-	V	V_{CC} = Max, FCLK and SCLK
Clock Input Low	V_{ILC}	-	0.8	V	V_{CC} = Min, FCLK and SCLK
Logical One Input Voltage	V_{IH}	2.0	-	V	V_{CC} = Max
Logical Zero Input Voltage	V_{IL}	-	0.8	V	V_{CC} = Min
Logical One Output Voltage	V_{OH}	2.6	-	V	I_{OH} = -5mA, V_{CC} = Min
Logical Zero Output Voltage	V_{OL}	-	0.4	V	I_{OL} = 5mA, V_{CC} = Min
Input Capacitance	C_{IN}	-	10	pF	FCLK = SCLK = 1MHz All Measurements Referenced to GND. T_A = +25°C, Note 3
Output Capacitance	C_{OUT}	-	10	pF	

NOTES:

1. Power supply current is proportional to frequency. Typical rating is 4.5mA/MHz.
2. Output load per test circuit and C_L = 40pF.
3. Not tested, but characterized at initial design and at major process/design changes.

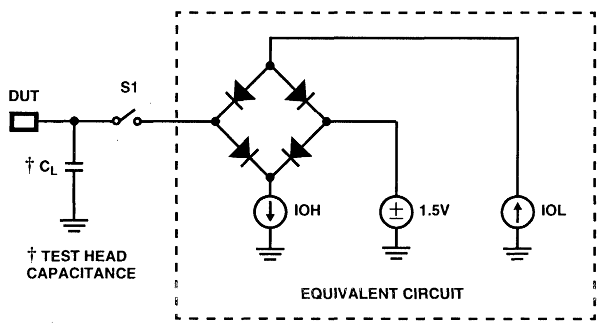
AC Electrical Specifications (Note 1) V_{CC} = +4.75V to +5.25V, T_A = 0°C to +70°C (Commercial)
V_{CC} = +4.75V to +5.25V, T_A = -40°C to +85°C (Industrial)

PARAMETER	SYMBOL	45MHz		40MHz		33MHz		COMMENTS
		MIN	MAX	MIN	MAX	MIN	MAX	
FCLK, SCLK Period	T_{CP}	22	-	25	-	30	-	ns
FCLK, SCLK High	T_{CH}	8	-	10	-	12	-	ns
FCLK, SCLK Low	T_{CL}	8	-	10	-	12	-	ns
Setup Time DIN, MXIN, SYNCIN, SYNCMX to SCLK	T_{DS}	8	-	8	-	9	-	ns
Hold Time DIN, MXIN, SYNCIN, SYNCMX from SCLK	T_{DH}	0	-	0	-	0	-	ns
Setup Time FSYNC to FCLK	T_{SS}	8	-	8	-	8	-	ns
Hold Time FSYNC from FCLK	T_{SH}	0	-	0	-	0	-	ns
Setup Time C0-7, A0-2 to Falling Edge of WR#	T_{WS}	10	-	10	-	10	-	ns
Hold Time C0-7, A0-2 from Falling Edge of WR#	T_{WH}	3	-	3	-	3	-	ns
Setup Time A0-2 to Falling Edge of RD#	T_{RS}	10	-	10	-	10	-	ns
Hold Time A0-2 from Rising Edge of RD#	T_{RH}	0	-	0	-	0	-	ns
WR# High	T_{WRH}	10	-	10	-	12	-	ns
WR# Low	T_{WRL}	10	-	10	-	12	-	ns
RD# High	T_{RDH}	10	-	10	-	10	-	ns
RD# Low to Data Valid	T_{RDO}	-	25	-	25	-	25	ns
RD# High to Output Disable	T_{OD}	-	6	-	6	-	6	ns
FCLK to CLKOUT	T_{FOC}	-	12	-	13	-	14	ns
CLKOUT to SYNCOUT, DOUT	T_{DO}	-	8	-	9	-	10	ns
Output Rise, Fall Time	T_{RF}	-	3	-	3	-	3	ns, Note 2

NOTES:

1. AC tests performed with C_L = 40pF, I_{OL} = 5mA, and I_{OH} = -5mA. Input reference level for FCLK and SCLK is 2.0V, all other inputs 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V.
2. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.

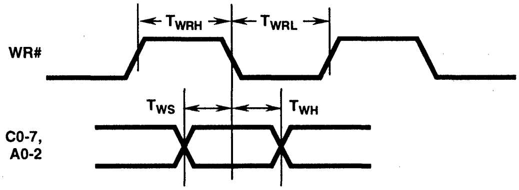
AC Test Load Circuit



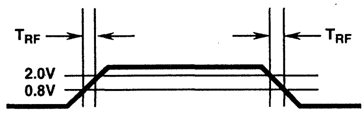
SWITCH S1 OPEN FOR I_{CCSB} AND I_{CCOP}

Waveforms

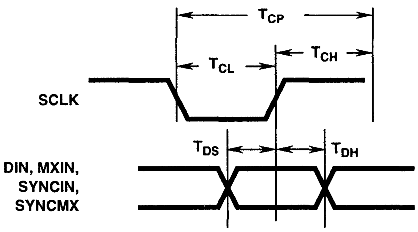
TIMING RELATIVE TO WR#



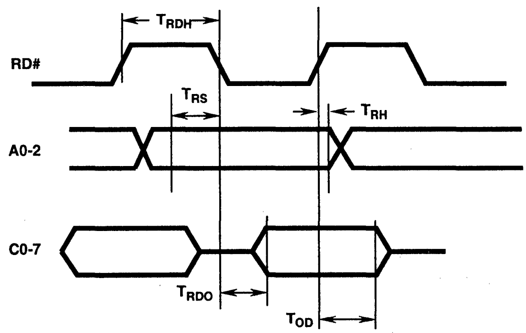
OUTPUT RISE AND FALL TIMES



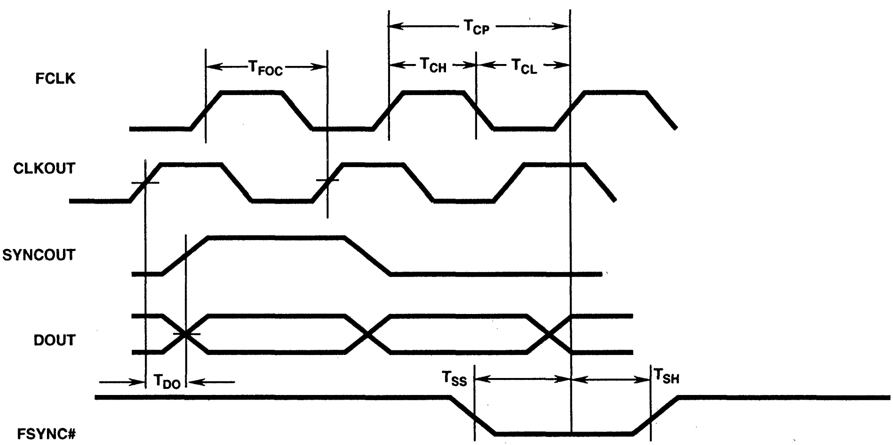
INPUT DATA TIMING



TIMING RELATIVE TO READ



TIMING RELATIVE TO FLCK AND CLKOUT



HARRIS SEMICONDUCTOR

HSP43168

July 1995

Dual FIR Filter

Features

- Two Independent 8-Tap FIR Filters Configurable as a Single 16-Tap FIR
- 10-Bit Data and Coefficients
- On-Board Storage for 32 Programmable Coefficient Sets
- Up To: 256 FIR Taps, 16 x 16 2-D Kernels, or 10 x 19-Bit Data and Coefficients
- Programmable Decimation to 16
- Programmable Rounding on Output
- Standard Microprocessor Interface

Applications

- Quadrature, Complex Filtering
- PolyPhase Filtering
- Image Processing
- Adaptive Filtering

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HSP43168VC-33	0°C to +70°C	100 Lead Plastic MQFP
HSP43168VC-40	0°C to +70°C	100 Lead Plastic MQFP
HSP43168VC-45	0°C to +70°C	100 Lead Plastic MQFP
HSP43168JC-33	0°C to +70°C	84 Lead PLCC
HSP43168JC-40	0°C to +70°C	84 Lead PLCC
HSP43168JC-45	0°C to +70°C	84 Lead PLCC
HSP43168GC-33	0°C to +70°C	84 Lead CPGA
HSP43168GC-45	0°C to +70°C	84 Lead CPGA

Description

The HSP43168 Dual FIR Filter consists of two independent 8-tap FIR filters. Each filter supports decimation from 1 to 16 and provides on-board storage for 32 sets of coefficients. The Block Diagram shows two FIR cells each fed by a separate coefficient bank and one of two separate inputs. The outputs of the FIR cells are either summed or multiplexed by the MUX/Adder. The compute power in the FIR Cells can be configured to provide quadrature filtering, complex filtering, 2-D convolution, 1-D/2-D correlations, and interpolating/decimating filters.

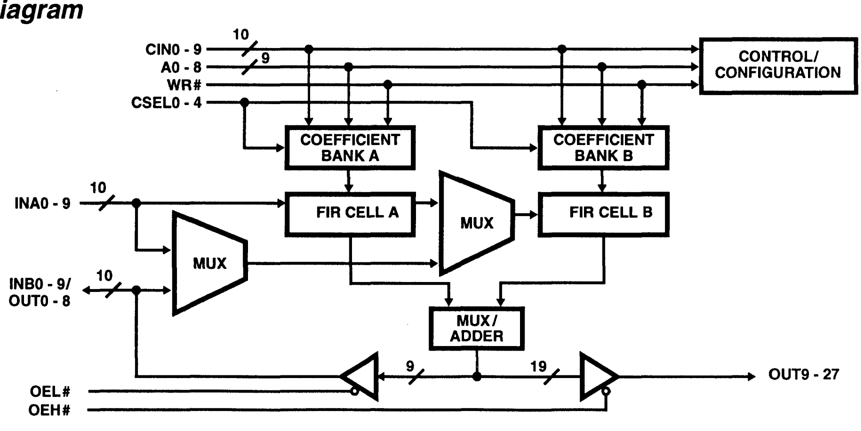
The FIR cells take advantage of symmetry in FIR coefficients by pre-adding data samples prior to multiplication. This allows an 8-tap FIR to be implemented using only 4 multipliers per filter cell. These cells can be configured as either a single 16-tap FIR filter or dual 8-tap FIR filters. Asymmetric filtering is also supported.

Decimation of up to 16 is provided to boost the effective number of filter taps from 2 to 16 times. Further, the decimation registers provide the delay necessary for fractional data conversion and 2-D filtering with kernels to 16x16.

The flexibility of the Dual is further enhanced by 32 sets of user programmable coefficients. Coefficient selection may be changed asynchronously from clock to clock. The ability to toggle between coefficient sets further simplifies applications such as polyphase or adaptive filtering.

The HSP43168 is a low power fully static design implemented in an advanced CMOS process. The configuration of the device is controlled through a standard microprocessor interface.

Block Diagram



10

DSP FILTERS

File Number 2808.5

Pinouts

84 LEAD PGA BOTTOM VIEW

	11	10	9	8	7	6	5	4	3	2	1
A	RVRS#	WR#	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8
B	SHFTEN#	MUX0	MUX1	A0	A3	A2	V_{CC}	CSEL2	CIN9	CIN7	CIN5
C	TXFR#	FWRD#			A5	A6	CSEL0			CIN6	CIN4
D	V_{CC}	ACCEN								GND	CIN3
E	OEH#	GND	CLK						CIN2	CIN1	CIN0
F	OUT27	OUT22	OUT26						INA8	INA9	V_{CC}
G	OUT24	OUT23	OUT25						INA7	INA5	INA6
H	OUT21	OUT20								INA3	INA4
J	OUT19	OUT17			OUT9	OEL#	INB3			INA0	INA2
K	OUT18	V_{CC}	OUT16	OUT13	V_{CC}	INB0	INB2	GND	INB7	INB8	INA1
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9

PIN 'A1' ID

HSP43168 BOTTOM VIEW

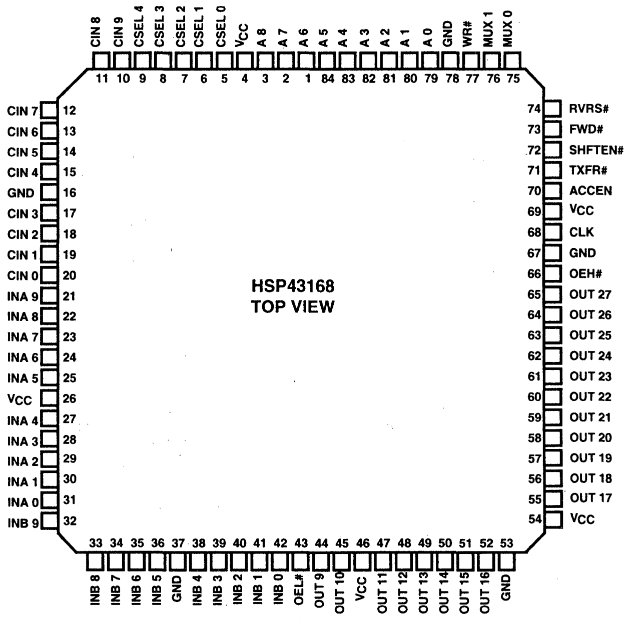
84 LEAD PGA TOP VIEW

	11	10	9	8	7	6	5	4	3	2	1
L	GND	OUT15	OUT14	OUT12	OUT10	OUT11	INB1	INB4	INB5	INB6	INB9
K	OUT18	V_{CC}	OUT16	OUT13	V_{CC}	INB0	INB2	GND	INB7	INB8	INA1
J	OUT19	OUT17			OUT9	OEL#	INB3			INA0	INA2
H	OUT21	OUT20								INA3	INA4
G	OUT24	OUT23	OUT25						INA7	INA5	INA6
F	OUT27	OUT22	OUT26						INA8	INA9	V_{CC}
E	OEH#	GND	CLK						CIN2	CIN1	CIN0
D	V_{CC}	ACCEN								GND	CIN3
C	TXFR#	FWRD#			A5	A6	CSEL0			CIN6	CIN4
B	SHFTEN#	MUX0	MUX1	A0	A3	A2	V_{CC}	CSEL2	CIN9	CIN7	CIN5
A	RVRS#	WR#	GND	A1	A4	A7	A8	CSEL1	CSEL3	CSEL4	CIN8

PIN 'A1' ID

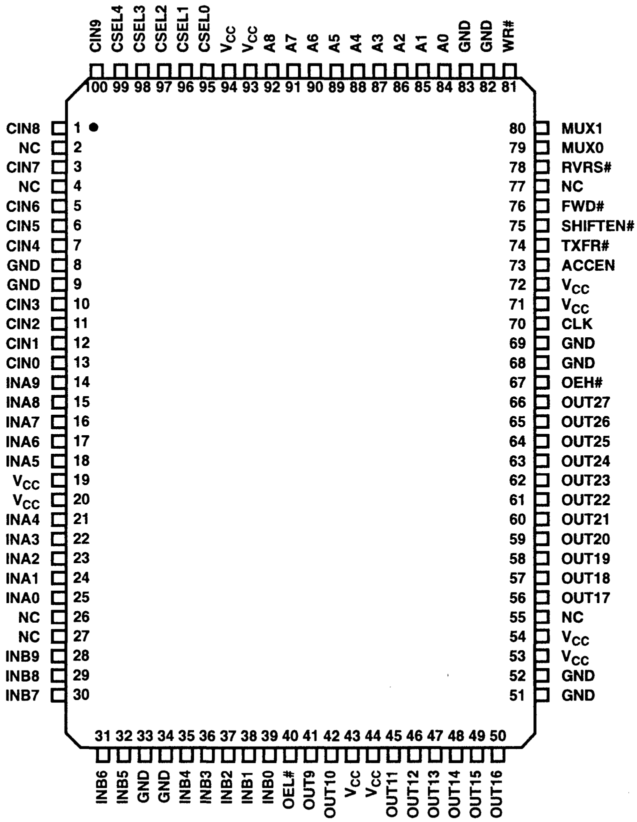
HSP43168 TOP VIEW

84 LEAD PLCC TOP VIEW



Pinouts (Continued)

100 LEAD MQFP
TOP VIEW



10
DSP FILTERS

Pin Description

SYMBOL	PIN NUMBER	TYPE	DESCRIPTION
V_{CC}	B5, D11, K10, K7, F1		V_{CC}: +5V power supply pin.
GND	A9, E10, L11, K4, D2		Ground.
CIN0-9	E1-3, D1, C1-2, B1-3, A1	I	Control/Coefficient Data Bus. Processor interface for loading control data and coefficients. CIN0 is the LSB.
A0-8	A5-8, B6-8, C6-7	I	Control/Coefficient Address Bus. Processor interface for addressing control and coefficient registers. A0 is the LSB.
WR#	A10	I	Control/Coefficient Write Clock. Data is latched into the control and coefficient registers on the rising edge of WR#.
CSEL0-4	A2-4, B4, C5	I	Coefficient Select. This input determines which of the 32 coefficient sets are to be used by FIR A and B. This input is registered and CSEL0 is the LSB.
INA0-9	K1, J1-2, H1-2, G1-3, F2-3	I	Input to FIR A. INA0 is the LSB.
INB0-9	L1-5, K2-3, K5-6, J5	I/O	Bidirectional Input for FIR B. INB0 is the LSB and is input only. When used as output, INB1-9 are the LSBs of the output bus, and INB9 is the MSB of these bits.
OUT9-27	F9-11, G9-11, H10-11, J10-11, J7, K11, K8-9, L6-10	O	19 MSBs of Output Bus. Data format is either unsigned or two's complement depending on configuration. OUT27 is the MSB.
SHFTEN#	B11	I	Shift Enable. This active low input enables clocking of data into the part and shifting of data through the decimation registers.
FWRD#	C10	I	Forward ALU Input Enable. When active low, data from the forward decimation path is input to the ALUs through the "a" input. When high, the "a" inputs to the ALUs are zeroed.
RVRS#	A11	I	Reverse ALU Input Enable. When active low, data from the reverse decimation path is input to the ALUs through the "b" input. When high, the "b" inputs to the ALUs are zeroed.
TXFR#	C11	I	Data Transfer Control. This active low input switches the LIFO being read into the reverse decimation path with the LIFO being written from the forward decimation path (see Figure 1).
MUX0-1	B9-10	I	Adder/Mux Control. This input controls data flow through the output Adder/Mux. Table 4 lists the various configurations.
CLK	E9	I	Clock. All inputs except those associated with the processor interface (CIN0-9, A0-8, WR#) and the output enables (OEL#, OEH#) are registered by the rising edge of CLK.
OEL#	J6	I	Output Enable Low. This three-state control enables the LSBs of the output bus to INB1-9 when OEL# is low.
OEH#	E11	I	Output Enable High. This three-state control enables OUT9-27 when OEH# is low.
ACCEN	D10	I	Accumulate Enable. This active high input allows accumulation in the FIR Cell Accumulator. A low on this input latches the FIR Accumulator contents into the Output Holding Registers while zeroing the feedback pass in the Accumulator.

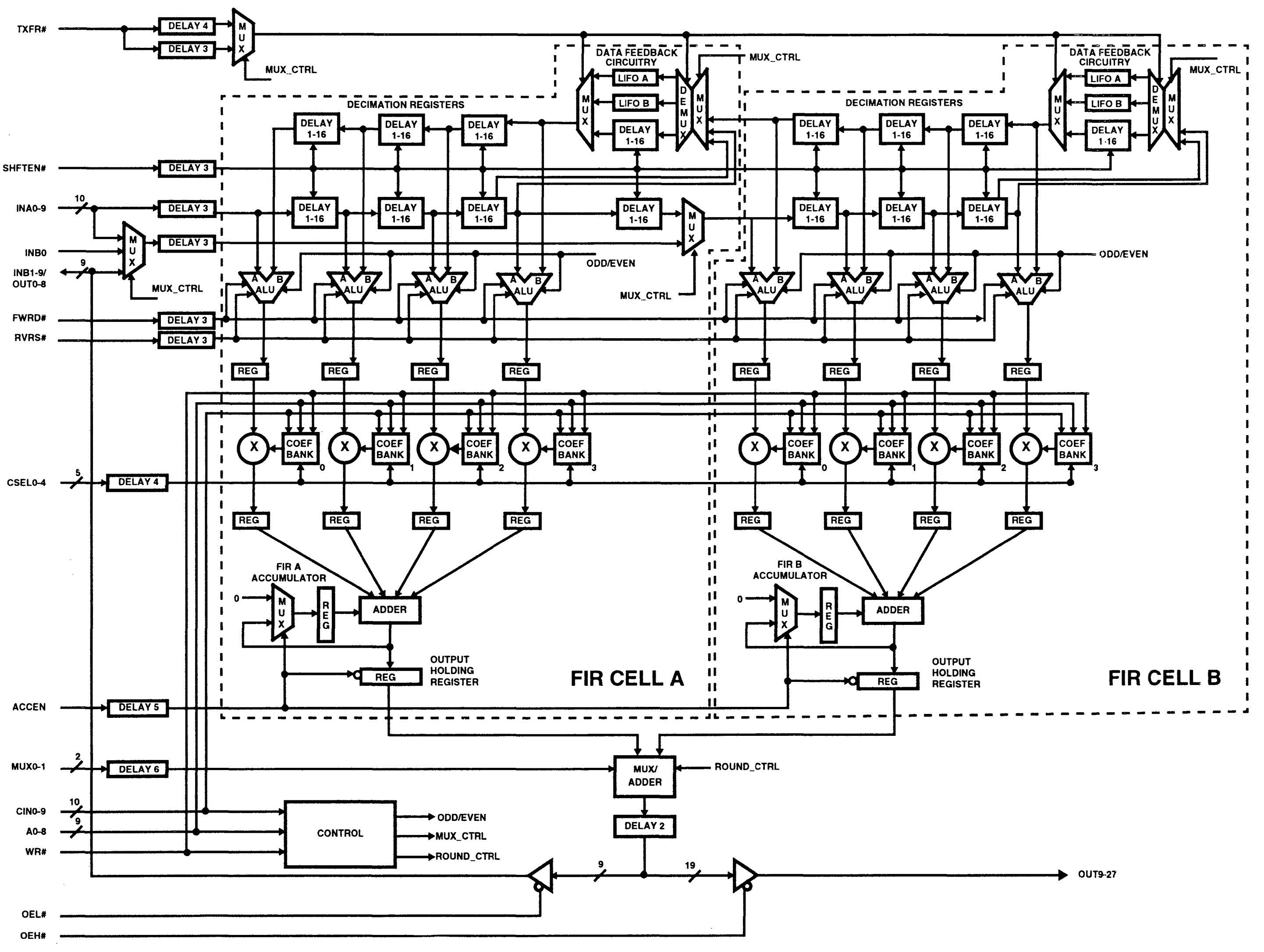


FIGURE 1. DUAL FIR FILTER

Functional Description

As shown in Figure 1, the HSP43168 consists of two 4-multiplier FIR filter cells which process 10-bit data and coefficients. The FIR cells can operate as two independent 8-tap FIR filters or two 4-tap asymmetric filters at maximum I/O rates. A single filter mode is provided which allows the FIR cells to operate as one 16-tap FIR filter or one 8-tap asymmetric filter. On board coefficient storage for up to 32 sets of 8 coefficients is provided. The coefficient sets are user selectable and are programmed through a microprocessor interface. Programmable decimation to 16 is also provided. By utilizing decimation registers together with the coefficient sets, polyphase filters are realizable which allow the user to trade data rate for filter taps. The MUX/ Adder can be configured to either add or multiplex the outputs of the filter cells depending upon whether the cells are operating in single or dual filter mode. In addition, a shifter in the MUX/ Adder is provided for implementation of filters with 10-bit data and 20-bit coefficients or vice versa.

Microprocessor Interface

The Dual FIR has a 20 pin write only microprocessor interface for loading data into the Control Block and Coefficient Bank. The interface consists of a 10-bit data bus (CIN0-9), a 9-bit address bus (A0-8), and a write input (WR#) to latch the data into the on-board registers. The control and coefficient data can be loaded asynchronously to CLK.

Control Block

The Dual FIR is configured by writing to the registers within the Control Block. These registers are memory mapped to address 000H (H = Hexadecimal) and 001H on A0-8. The format of these registers is shown in Table 1 and Table 2. Writing the Control/Configuration registers causes a reset which lasts for 6 CLK cycles following the assertion of WR#. The reset caused by writing registers in the Control Block will not clear the contents of the Coefficient Bank.

TABLE 1.

CONTROL ADDRESS 000H		
BITS	**FUNCTION**	**DESCRIPTION**
3-0	Decimation Factor	0000 = No Decimation 1111 = Decimation by 16
4	Mode Select	0 = Single FIlter Mode 1 = Dual FIlter Mode
5	Odd/Even Symmetry	0 = Even symmetric coefficients 1 = Odd symmetric coefficients
6	FIR A odd/even taps	0 = Odd number of taps in filter 1 = Even number of taps in filter
7	FIR B odd/even taps	(Defined same as FIR A above)
8	FIR B Input Source	0 = Input from INA0-9 1 = Input from INB0-9
9	Not Used	Set to 0 for proper operation

The 4 LSBs of the control word loaded at address 000H are used to select the decimation factor. For example, if the 4 LSBs are programmed with a value of 0010, the forward and reverse shifting decimation registers are each configured with a delay of 3. Bit 4 is used to select whether the FIR cells operate as two independent filters or one extended length filter. Coefficient symmetry is selected by bit 5. Bits 6 and 7 are programmed to configure the FIR cells for odd or even filter lengths. Bit 8 selects the FIR B input source when the FIR cells are configured for independent operation. Bit 9 must be programmed to 0.

The 4 LSBs of the control word loaded at address 001H are used to configure the format of the FIR cell's data and coefficients. Bit 4 is programmed to enable or disable the reversal of data sample order prior to entering the backward shifting decimation registers. Bits 5-9 are used to support programmable rounding on the output.

TABLE 2.

CONTROL ADDRESS 001H		
BITS	**FUNCTION**	**DESCRIPTION**
0	FIR A Input Format	0 = Unsigned 1 = Two's Complement
1	FIR A Coefficient Format	(Defined same as FIR A input)
2	FIR B Input Format	(Defined same as FIR A input)
3	FIR B Coefficient	(Defined same as FIR A input)
4	Data Reversal Enable	0 = Enabled 1 = Disabled
8-5	Round Position	0000 = 2^{-10} 1011 = 2^{1}
9	Round Enable	0 = Enabled 1 = Disabled

NOTE: Address locations 002H to 011H are reserved, and writing to these locations will have unpredictable effects on part configuration.

FIR Filter Cells

Each FIR filter cell is based on an array of four 11x10-bit two's complement multipliers. The multipliers get one input from the ALUs which combine data shifting through the forward and backward decimation registers. The second input comes from the user programmable coefficient bank. The multiplier outputs feed an accumulator whose result is passed to the output section where it is multiplexed or added.

Decimation Registers

The forward and backward shifting registers are configurable for decimation by 1 to 16 (see Table 1). The backward shifting registers are used to take advantage of symmetry in linear phase filters by aligning data at the ALUs for pre-addition prior to multiplication by the common coefficient. When the FIR cells are configured in single filter mode, the decimation registers in each cell are cascaded. This lengthened delay path allows computation of a filter which is twice the size of that capable in a single cell. The decimation registers also provide data storage for poly-phase or 2-D filtering applications (See Applications Examples section).

The Data Feedback Circuitry in each FIR cell is responsible for transferring data from the forward to the backward shifting decimation registers. This circuitry feeds blocks of samples into the backward shifting decimation path in either reversed or non-reversed sample order. The MUX/DEMUX structure at the input to the Feedback Circuitry routes data to the LIFOs or the delay stage depending on configuration. The MUX on the Feedback Circuitry Output selects the storage element which feeds the backward shifting decimation registers.

In applications requiring reversal of sample order, such as FIR filtering with decimation, the FIR cells are configured with data reversal enabled (see Table 2). In this mode, data is transferred from the forward to the backward shifting registers through a ping-ponged LIFO structure. While one LIFO is being read into the backward shifting path, the other is written with data samples. The MUX/DEMUX controls which LIFO is being written, and the MUX on the Feedback Circuitry output controls which LIFO is being read. A low on TXFR# and SHIFTEN#, switches the LIFOs being read and written, which causes the block of data read from the structure to be reversed in sample order (See Example 4 in the Application Examples section).

The frequency with which TXFR# is asserted determines size of the data blocks in which sample order is reversed. For example, if TXFR# is asserted once every three CLKs, blocks of 3 data samples with order reversed, would be fed into the backward decimation registers. Note: altering the frequency or phase of TXFR# assertion once a filtering operation has been started will cause unknown results.

In applications which do not require sample order reversal, the FIR cells must be configured with data reversal disabled (see Table 2). In addition, TXFR# must be asserted to ensure proper data flow. In this configuration, data to the backward shifting decimation path is routed though a delay stage instead of the ping-pong LIFOs. The number of registers in the delay stage is based on the programmed decimation factor. Note: data reversal must be disabled and TXFR# must be asserted for filtering applications which do not use decimation.

The shifting of data through the forward and reverse decimation registers is enabled by asserting the SHFTEN# input. When SHFTEN# transitions high, data shifting is disabled, and the data sample latched into the part on the previous clock is the last input to the forward decimation path. When SHFTEN# is asserted, shifting of data through the decimation paths is enabled. The data sample at the part input when SHFTEN# is asserted will be the next data sample into the forward decimation path.

When operating the FIR cells as two independent filters, FIR A receives input data via INA0-9 and FIR B receives data from either INA0-9 or INB0-9 depending on the configuration (Table 1). When the FIR cells are configured as a single extended length filter, the forward and backward decimation paths are cascaded. In this mode, data is transferred from the forward decimation path to the backward decimation path by the Data Feedback Circuitry in FIR B. Thus, the manner in which data is read into the backward shifting decimation path is determined by FIR B's configuration.

When the decimation paths are cascaded, data is routed through the delay stage in FIR A's Data Feedback Circuitry.

The configuration of the FIR cells as even or odd length filters determines the point in the forward decimation path from which data is multiplexed to the Data Feedback Circuitry. For example, if the FIR cell is configured as an odd length filter, data prior to the last register in the third forward decimation stage is routed to the Feedback Circuitry. If the FIR cell is configured as an even length filter, data output from the third forward decimation stage is multiplexed to the Feedback Circuitry. This is required to insure proper data alignment with symmetric filter coefficients (See Application Examples).

ALUs

Data shifting through the forward and reverse decimation path feeds the "a" and "b" inputs of the ALUs respectively. The ALUs perform an "b+a" operation if the FIR cell is configured for even symmetric coefficients or an "b-a" operation if configured for odd symmetric coefficients.

For applications in which a pre-add or subtract is not required, the "a" or "b" input can be zeroed by disabling FWRD# or RVRS# respectively. This has the effect of producing an ALU output which is either "a", "-a", or "b" depending on the filter symmetry chosen. For example, if the FIR cell is configured for an even symmetric filter with FWRD# low and RVRS# high, the data shifting through the forward decimation registers would appear on the ALU output.

Coefficient Bank

The output of the ALU is multiplied by a coefficient from one of 32 user programmable coefficient sets. Each set consists of 8 coefficients (4 coefficients for FIR A and 4 for FIR B). The active coefficient set is selected using CSEL0-4. The coefficient set may be switched every clock to support polyphase filtering operations.

The coefficients are loaded into on-board registers using the microprocessor interface, CIN0-9, A0-8, and WR#. Each multiplier within the FIR Cells is driven by a coefficient bank with one of 32 coefficients. These coefficients are addressed as shown in Table 3. The inputs A0-1 specify the Coefficient Bank for one of the four multipliers in each FIR Cell; A2 specifies FIR Cell A or B; Bits A7-3 specify one of 32 sets in which the coefficient is to be stored. For example, an address of 10dH would access the coefficient for the second multiplier in FIR B in the second coefficient set.

TABLE 3.

A8	A7-3	A2	A1-0	FIR	BANK
1	xxxxx	0	00	A	0
1	xxxxx	0	01	A	1
1	xxxxx	0	10	A	2
1	xxxxx	0	11	A	3
1	xxxxx	1	00	B	0
1	xxxxx	1	01	B	1
1	xxxxx	1	10	B	2
1	xxxxx	1	11	B	3

FIR Cell Accumulator

The registered outputs from the multipliers in each FIR cell feed the FIR cell's accumulator. The ACCEN input controls each accumulator's running sum and the latching of data from the accumulator into the Output Holding Registers. When ACCEN is low, feedback from the accumulator adder is zeroed which disables accumulation. Also, output from the accumulator is latched into the Output Holding Registers. When ACCEN is asserted, accumulation is enabled and the contents of the Output Holding Registers remain unchanged.

Output MUX/Adder

The contents of each FIR Cell's Output Holding Register is summed or multiplexed in the Mux/Adder. The operation of the Mux/Adder is controlled by the MUX1-0 inputs as shown in Table 4. Applications requiring 10-bit data and 20-bit coefficients or 20-bit data and 10-bit coefficients are made possible by configuring the MUX/Adder to scale FIR B's output by 2^{-10} prior to summing with FIR A. When the Dual FIR is configured as two independent filters, the MUX1-0 inputs would be used to multiplex the filter outputs of each cell. For applications in which FIR A and B are configured as a single filter, the MUX/Adder is configured to sum the output of each FIR cell.

TABLE 4.

MUX1-0 DECODING	
MUX1-0	**OUT0-27**
00	FIRA + FIRB (FIR B Scaled by 2^{-10})
01	FIRA + FIRB
10	FIRA
11	FIRB

Input/Output Formats

The Dual FIR supports mixed mode arithmetic with both unsigned and two's complement data and coefficients. The input and output formats for both data types is shown below. If the Dual FIR is configured as an even symmetric filter with unsigned data and coefficients, the output will be unsigned. Otherwise, the output will be two's complement.

INPUT DATA FORMAT INA0-9, INB0-9
FRACTIONAL TWO'S COMPLEMENT

9	8	7	6	5	4	3	2	1	0
-2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT9-27
FRACTIONAL TWO'S COMPLEMENT

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
-2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT0-8
FRACTIONAL TWO'S COMPLEMENT

8	7	6	5	4	3	2	1	0
2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}

INPUT DATA FORMAT INA0-9, INB0-9
FRACTIONAL UNSIGNED

9	8	7	6	5	4	3	2	1	0
2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT9-27
FRACTIONAL UNSIGNED

27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9
2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	$.2^{-1}$	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}

OUTPUT DATA FORMAT OUT0-8
FRACTIONAL UNSIGNED

8	7	6	5	4	3	2	1	0
2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}	2^{-16}	2^{-17}	2^{-18}

The MUX/Adder can be configured to implement programmable rounding at bit locations 2^{-10} through 2^{1}. The round is implemented by adding a 1 to the specified location (see Table 2). For example, to configure the part such that the output is rounded to the 10 MSBs, OUT18 - 27, the round position would be chosen to be 2^{-1}.

Application Examples

In this section a number of examples which show even, odd, symmetric, asymmetric and decimating filters are presented. These examples are intended to show different operational modes of the HSP43168. The examples are all based on a dual filter configuration. However, the same principles apply when the part is configured with both FIR cells operating as a single filter.

Example 1. Even-Tap Symmetric Filter Example

The HSP43168 may be configured as two independent 8-tap symmetric filters as shown by the block diagram in Figure 2. Each of the FIR cells takes advantage of symmetric filter coefficients by pre-adding data samples common to a given coefficient. As a result, each FIR cell can implement an 8-tap symmetric filter using only four multipliers. Similarly, when the HSP43168 is configured in single filter mode a 16-tap symmetric filter is possible by using the multipliers in both cells.

The operation of the FIR cell is better understood by comparing the data and coefficient alignment for a given filter output, Figure 3, with the data flow through the FIR cell, as shown in Figure 4. The block diagrams in Figure 4 are a simplification of the FIR cell shown in Figure 1. For simplicity, the ALUs and FIR Cell Accumulators were replaced by adders, and the pipeline delay registers were omitted.

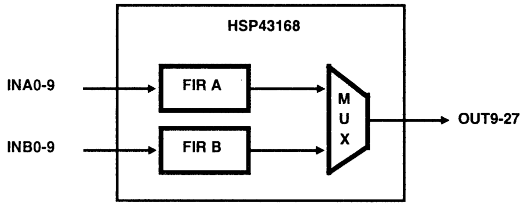


FIGURE 2. USING HSP43168 AS TWO INDEPENDENT FILTERS

In Figure 4, the order of the data samples within the filter cell is shown by the numbers in the forward and backward shifting decimation paths. The output of the filter cell is given by the equation at the bottom of each block diagram. Figure 4a shows the data sample alignment at the pre-adders for the data/coefficient alignment shown in Figure 3.

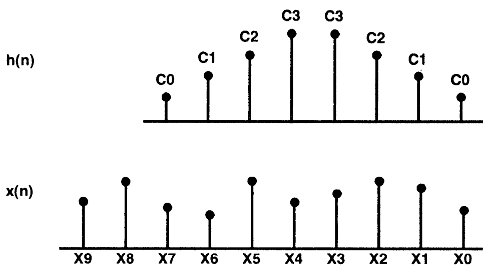


FIGURE 3. DATA/COEFFICIENT ALIGNMENT FOR 8-TAP EVEN SYMMETRIC FILTER

The dual filter application is configured by writing 1d0H to address 000H via the microprocessor interface, CIN0-9, A0-8, and WR#. Since this application does not use decimation, the 4th bit of the control register at address 001H must be set to disable data reversal (see Table 2). Failure to disable data reversal will produce erroneous results.

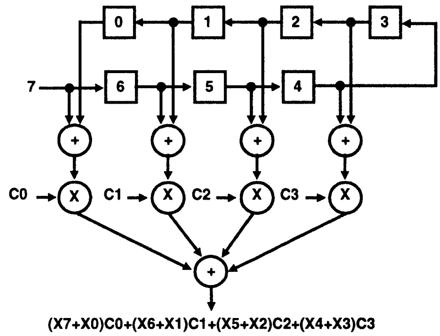


FIGURE 4A. DATA FLOW AS DATA SAMPLE 7 IS CLOCKED INTO THE FEED FORWARD STAGE

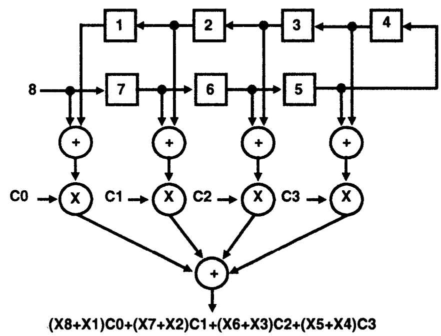


FIGURE 4B. DATA FLOW AS DATA SAMPLE 8 IS CLOCKED INTO THE FEED FORWARD STAGE

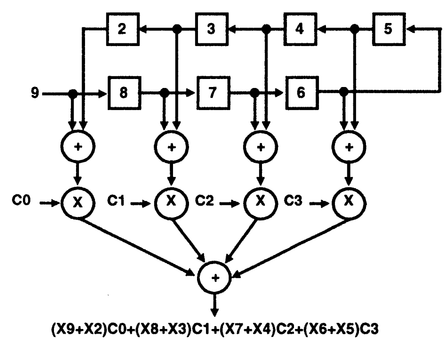


FIGURE 4C. DATA FLOW AS DATA SAMPLE 9 IS CLOCKED INTO THE FEED FORWARD STAGE

FIGURE 4. DATA FLOW DIAGRAMS FOR 8-TAP SYMMETRIC FILTER

Using this architecture, only the unique coefficients need to be stored in the Coefficient Bank. For example, the above filter would be stored in the first coefficient set for FIR A by writing C0, C1, C2, and C3 to address 100H, 101H, 102H, and 103H respectively. To write the same filter to the first coefficient set for FIR B, the address sequence would change to 104H, 105H, 106H, and 107H.

To operate the HSP43168 in this mode, TXFR# is tied low to ensure proper data flow; both FWRD# and RVRS# are tied low to enable data samples from the forward and reverse data paths to the ALUs for pre-adding; ACCEN is tied low to prevent accumulation over multiple CLKs; SHFTEN# is tied low to allow shifting of data through the decimation registers; MUX0-1 is programmed to multiplex the output the of either FIR A or FIR B; CSEL0-4 is programmable to access the stored coefficient set, in this example CSEL = 00000.

Example 2. Odd-Tap Symmetric Filter Example

The HSP43168 may be configured as two independent 7-tap symmetric filters with a functional block diagram resembling Figure 2. As in the 8-tap filter example, the HSP43168 implements the filtering operation by summing data samples sharing a common coefficient prior to multiplication by that coefficient. However, for odd length filters the pre-addition requires that the center coefficient be scaled by 1/2.

The operation of the FIR cell for odd length filters is better understood by comparing the data/coefficient alignment in Figure 5 with the data flow diagrams in Figure 6. The block diagrams in Figure 6 are a simplification of the FIR cell shown in Figure 1.

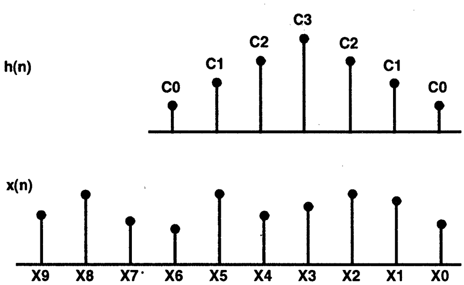


FIGURE 5. DATA/COEFFICIENT ALIGNMENT FOR 7-TAP SYMMETRIC FILTER

For odd length filters, proper data/coefficient alignment is ensured by routing data entering the last register in the third forward decimation stage to the backward shifting registers. In this configuration, the center coefficient must be scaled by 1/2 to compensate for the summation of the same data sample from both the forward and backward shifting registers.

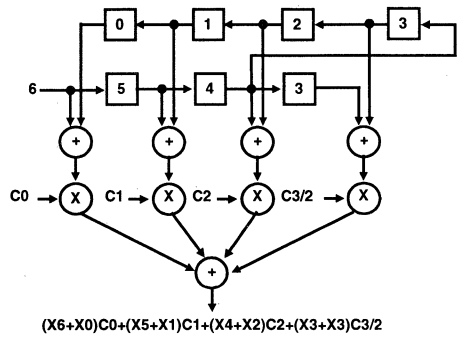


FIGURE 6A. DATA FLOW AS DATA SAMPLE 6 IS CLOCKED INTO THE FEED FORWARD STAGE

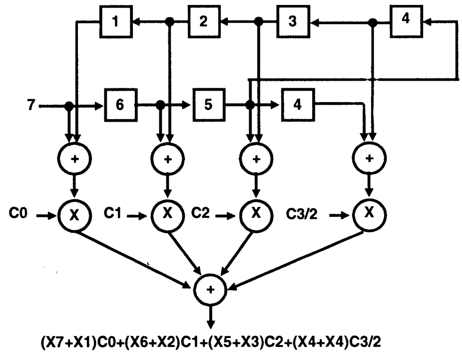


FIGURE 6B. DATA FLOW AS DATA SAMPLE 7 IS CLOCKED INTO THE FEED FORWARD STAGE

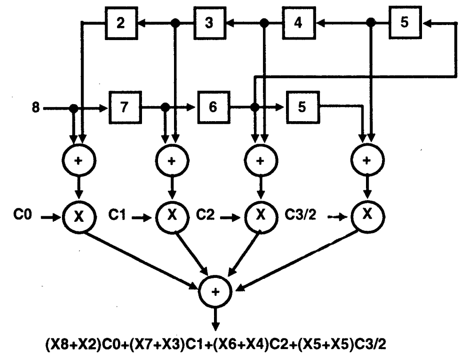


FIGURE 6C. DATA FLOW AS DATA SAMPLE 8 IS CLOCKED INTO THE FEED FORWARD STAGE

FIGURE 6. DATA FLOW DIAGRAMS FOR 7-TAP SYMMETRIC FILTER

In the data flow diagrams of Figure 6, the order of the data samples input in to the filter cell is shown by the numbers in the forward and backward shifting decimation paths. The output of the filter cell is given by the equation at the bottom of the block. The diagram in Figure 6a shows data sample alignment at the pre-adders for the data/coefficient alignment shown in Figure 5.

This dual filter application is configured by writing 110H to address 000H via the microprocessor interface, CIN0-9, A0-8, and WR#. Also, data reversal must be disabled by setting bit 4 of the control register at address 0001H. As in the 8-tap example, only the unique coefficients need to be stored in the Coefficient Bank. These coefficients are stored in the first coefficient set for FIR A by writing C0, C1, C2, and C3 to address 100H, 101H, 102H, and 103H respectively. To write the same filter to the first coefficient set for FIR B, the address sequence would change to 104H, 105H, 106H, and 107H. The control signals TXFR#, FWRD#, RVRS#, ACCEN, SHFTEN#, and CSEL0-4 are controlled as described in Example 1.

Example 3. Asymmetric Filter Example

The FIR cells within the HSP43168 can each calculate 4 asymmetric taps on each clock. Thus, a single FIR cell can implement an 8-tap asymmetric filter if the HSP43168 is clocked at twice the input data rate. Similarly, if the Dual is configured as a single filter, a 16-tap asymmetric filter is realizable.

For this example, the FIR cells are configured as two 8-tap asymmetric filters which are clocked at twice the input data rate. New data is shifted into the forward and backward decimation paths every other CLK by the assertion of SHFTEN#. The filter output is computed by passing data from each decimation path to the multipliers on alternating clocks. Two sets of coefficients are required, one for data on the forward decimation path, and one for data on the reverse path. The filter output is generated by accumulating the multiplier outputs for two CLKs.

The operation of this configuration is better understood by comparing the data/coefficient alignment in Figure 7 with the data flow diagrams in Figure 8. The ALUs have been omitted from the FIR cell diagrams because data is fed to the multipliers directly from the forward and reverse decimation paths. The data samples within the FIR cell are shown by the numbers in the decimation paths.

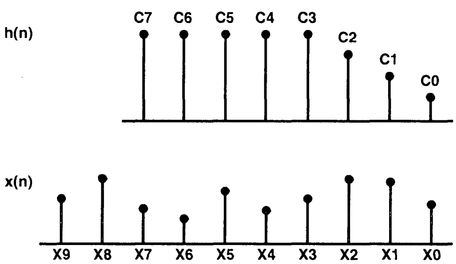


FIGURE 7. DATA/COEFFICIENT ALIGNMENT FOR 8-TAP ASYMMETRIC FILTER

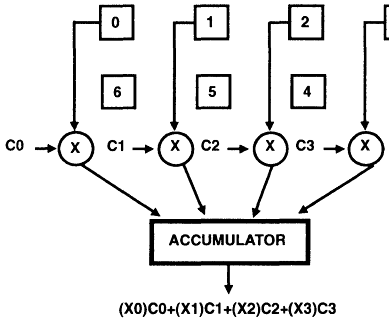


FIGURE 8A. DATA SHIFTING DISABLED, BACKWARD SHIFTING DECIMATION REGISTERS FEEDING MULTIPLIERS

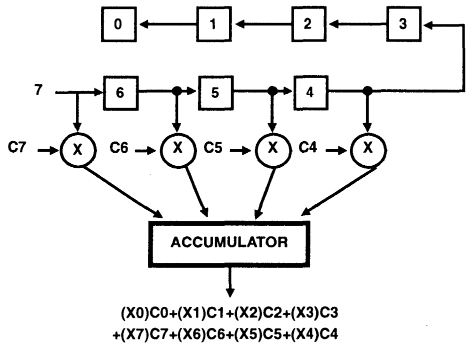


FIGURE 8B. SHIFTING OF DATA SAMPLE 7 INTO FIR CELL ENABLED, FORWARD SHIFTING REGISTERS FEEDING MULTIPLIERS

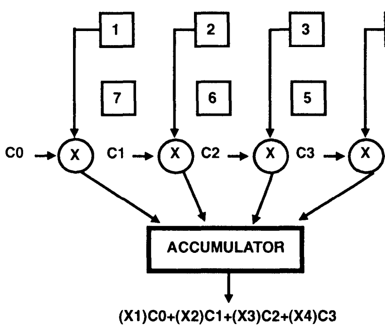


FIGURE 8C. DATA SHIFTING DISABLED, BACKWARD SHIFTING DECIMATION REGISTERS FEEDING MULTIPLIERS

FIGURE 8. DATA FLOW DIAGRAMS FOR 8-TAP ASYMMETRIC FILTER

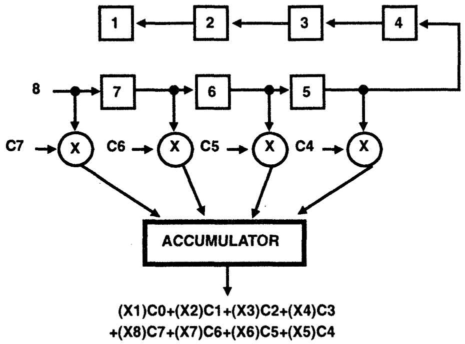


FIGURE 8D. SHIFTING OF DATA SAMPLE 8 INTO FIR CELL ENABLED, FORWARD SHIFTING REGISTERS FEEDING MULTIPLIERS

FIGURE 8. DATA FLOW DIAGRAMS FOR 8-TAP ASYMMETRIC FILTER CONTINUED

For this application, each filter cell is configured as an odd length filter by writing 110H to the control register at address 000H. Even though an even tap filter is being implemented, the filter cells must be configured as odd length to ensure proper data flow. Also, the 4th bit at control address 001H must be set to enable data reversal, and TXFR# must be tied low. Since an 8-tap asymmetric filter is being implemented, two sets of coefficients must be stored. These eight coefficients could be loaded into the first two coefficient sets for FIR A by writing C0, C1, C2, C3, C7, C6, C5, and C4 to address 100H, 101H, 102H, 103H, 108H, 109H, 10aH, and 10bH respectively.

The sum of products required for this 8-tap filter require dynamic control over FWRD#, RVRS#, ACCEN, and CSEL0-4. The relative timing of these signals is shown in Figure 9.

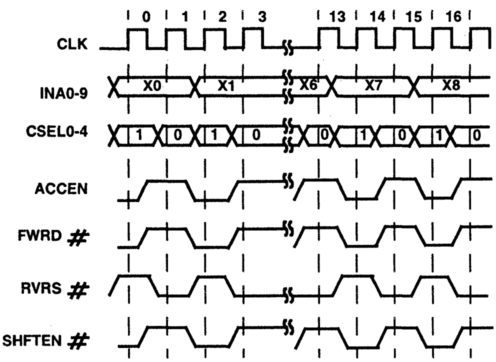


FIGURE 9. CONTROL TIMING FOR 8-TAP ASYMMETRIC FILTER

Example 4. Even-Tap Decimating Filter Example

The HSP43168 supports filtering applications requiring decimation to 16. In these applications the output data rate is reduced by a factor of N. As a result, N clock cycles can be used for the computation of the filter output. For example, each FIR cell can calculate 8 symmetric or 4 asymmetric taps in one clock. If the application requires decimation by two, the filter output can be calculated over two clocks thus boosting the number of taps per FIR cell to 16 symmetric or 8 asymmetric. For this example, each FIR cell is configured as an independent 24-tap decimate x3 filter.

The alignment of data relative to the 24 filter coefficients for a particular output is depicted graphically in Figure 10. As in previous examples, the HSP43168 implements the filtering operation by summing data samples prior to multiplication by the common coefficient. In this example an output is required every third CLK which allows 3 CLKs for computation. On each CLK, one of three sets of coefficients are used to calculate 8 of the filter taps. The block diagrams in Figure 12 show the data flow and accumulator output for the data/coefficient alignment in Figure 10.

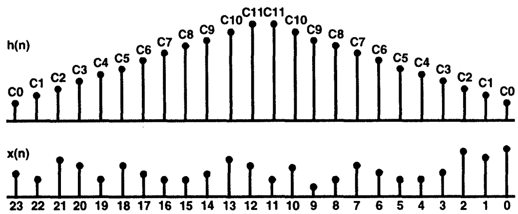
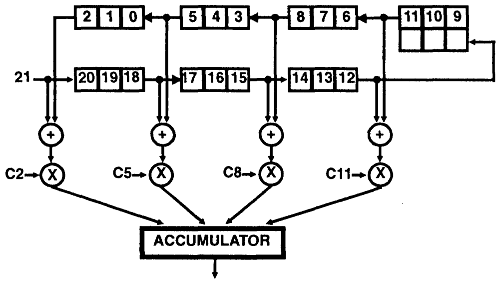


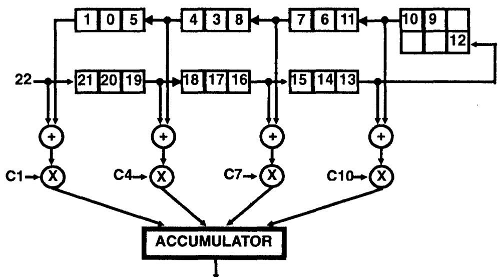
FIGURE 10. DATA/COEFFICIENT ALIGNMENT FOR 24-TAP DECIMATE BY 3 FIR FILTER

Proper data and coefficient alignment is achieved by asserting TXFR# once every three CLKs to switch the LIFOs which are being read and written. This has the effect of feeding blocks of three samples into the backward shifting decimation path which are reversed in sample order. In addition, ACCEN is deasserted once every three clocks to allow accumulation over three CLKs. The three sets of coefficients required in the calculation of a 24-tap symmetric filter are cycled through using CSEL0-4. The timing relationship between the CSEL0-4, ACCEN, and TXFR# are shown in Figure 12.



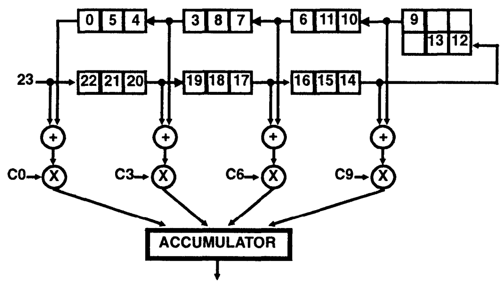
(X2+X21)C2+(X5+X18)C5+(X8+X15)C8+(X11+X12)C11

FIGURE 11A. COMPUTATIONAL FLOW AS DATA SAMPLE 21 IS CLOCKED INTO THE FEED FORWARD STAGE



(X1+X22)C1+(X4X19)C4+(X7+X16)C7+(X10+X13)C10
+(X2+X21)C2+(X5+X18)C5+(X8+X15)C8+(X11+X12)C11

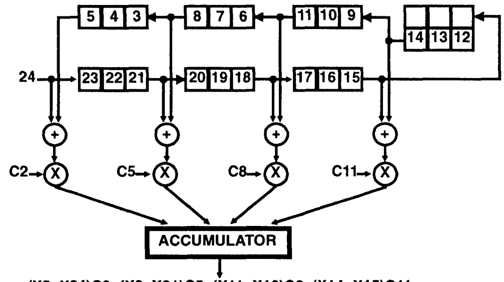
FIGURE 11B. COMPUTATIONAL FLOW AS DATA SAMPLE 22 IS CLOCKED INTO THE FEED FORWARD STAGE



(X0+X23)C0+(X3+X20)C3+(X6+X17)C6+(X9+X14)C9
+(X1+X22)C1+(X4+X19)C4+(X7+X16)C7+(X10+X13)C10
+(X2+X21)C2+(X5+X18)C5+(X8+X15)C8+(X11+X12)C11

FIGURE 11C. COMPUTATIONAL FLOW AS DATA SAMPLE 23 IS CLOCKED INTO THE FEED FORWARD STAGE

To operate in this mode the Dual is configured by writing 1d2 to address 000H via the microprocessor interface, CIN0-9, A0-8, and WR#. Data reversal must be enabled see (Table 2). The 12 unique coefficients for this example are stored as three sets of coefficients for either FIR cell. For FIR A, the coefficients are loaded into the Coefficient Bank by writing C2, C5, C8, C11, C1, C4, C7, C10, C0, C3, C6, and C9 to address 100H, 101H, 102H, 103H, 108H, 109H, 10aH, 10bH, 110H, 111H, 112H, and 113H, respectively.



(X5+X24)C0+(X8+X21)C5+(X11+X18)C8+(X14+X15)C11

FIGURE 11D. COMPUTATIONAL FLOW AS DATA SAMPLE 24 IS CLOCKED INTO THE FEED FORWARD STAGE

FIGURE 11. DATA FLOW DIAGRAMS FOR 24-TAP DECIMATE BY 3 FIR FILTER

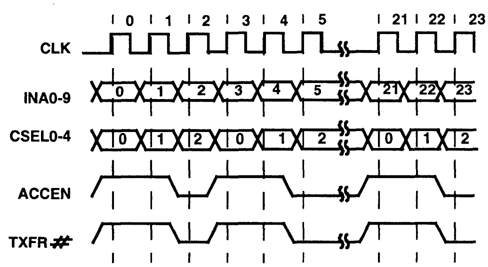


FIGURE 12. CONTROL SIGNAL TIMING FOR 24-TAP DECIMATE X3 FILTER

Example 5. Odd-Tap Decimating Symmetric Filter

This example highlights the use of the HSP43168 as two independent, 23-tap, symmetric, decimate by 3 filters. In this example, the operational differences in the control signals and data reversal structure may be compared to the previously discussed even-tap decimating filter.

As in the 24-tap example, an output is required every third CLK which allows 3 CLKs for computation. On each CLK, one of three sets of coefficients are used to calculate the filter taps. Since this is an odd length filter, the center coefficient must be scaled by 1/2 to compensate for the summation of the same data sample from the forward and backward shifting decimation paths.The block diagrams in Figure 14 show the data flow and accumulator output for the data coefficient alignment in Figure 13.

Proper data and coefficient alignment is achieved by asserting TXFR# once every three CLKs to switch the LIFOs which are being read and written. For odd length filters, data prior to the last register in the forward decimation path is routed to the Feedback Circuitry. As a result, TXFR# should be asserted one cycle prior to the input data samples which align with the center tap. The timing relationship between the CSEL0-5, ACCEN, and TXFR# are shown in Figure 15.

10
DSP FILTERS

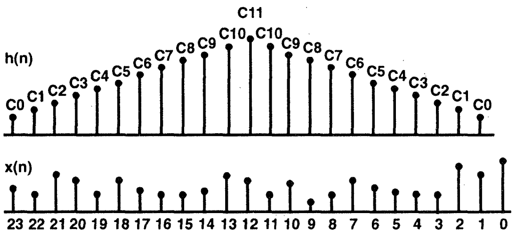
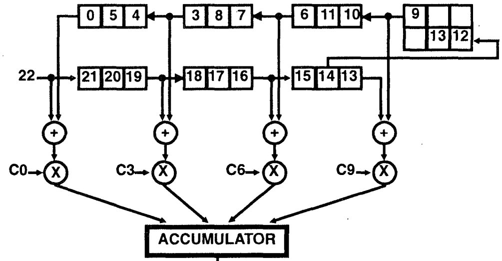
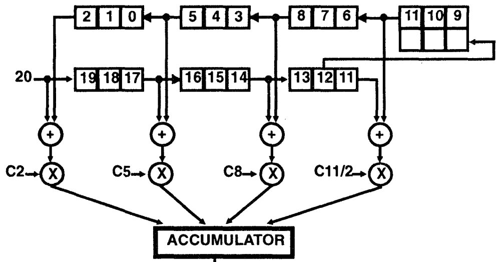


FIGURE 13. DATA/COEFFICIENT ALIGNMENT FOR 23-TAP DECIMATE BY 3 SYMMETRIC FILTER



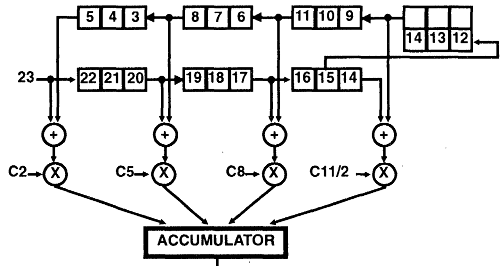
(X0+X22)C0+(X3+X19)C3+(X6+X16)C6+(X9+X13)C9
+(X1+X21)C1+(X4+X18)C4+(X7+X15)C7+(X10+X12)C10
+(X2+X20)C2+(X5+X17)C5+(X8+X14)C8+(X11+X11)C11/2

FIGURE 14C. COMPUTATIONAL FLOW AS DATA SAMPLE 22 IS CLOCKED INTO THE FEED FORWARD STAGE



(X2+X20)C2+(X5+X17)C5+(X8+X14)C8+(X11+X11)C11/2

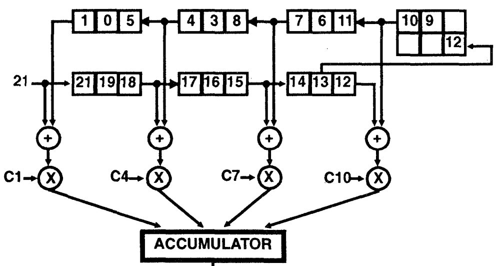
FIGURE 14A. COMPUTATIONAL FLOW AS DATA SAMPLE 20 IS CLOCKED INTO THE FEED FORWARD STAGE



(X5+X23)C2+(X8+X20)C5+(X11+X17)C8+(X14+X14)C11/2

FIGURE 14D. COMPUTATIONAL FLOW AS DATA SAMPLE 23 IS CLOCKED INTO THE FEED FORWARD STAGE

FIGURE 14. DATA FLOW DIAGRAMS FOR 23-TAP DECIMATE BY 3 SYMMETRIC FILTER



(X1+X21)C1+(X4+X18)C4+(X7+X15)C7+(X10+X12)C10
+(X2+X20)C2+(X5+X17)C5+(X8+X14)C8+(X11+X11)C11/2

FIGURE 14B. COMPUTATIONAL FLOW AS DATA SAMPLE 21 IS CLOCKED INTO THE FEED FORWARD STAGE

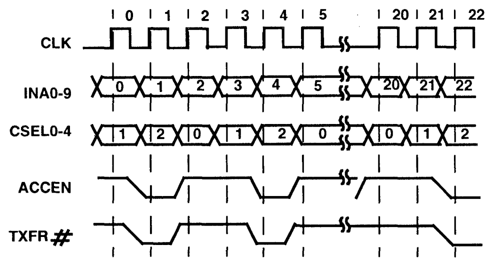


FIGURE 15. CONTROL SIGNAL TIMING FOR 23-TAP SYMMETRIC FILTER

To operate in this mode, the Dual is configured by writing 112H to address 000H via the microprocessor interface, CIN0-9, A0-8, and WR#. Data reversal must be enabled (see Table 2.0). The 12 unique coefficients for this example are stored as three sets of coefficients for either FIR cell. For FIR A, the coefficients are loaded into the Coefficient Bank by writing C2, C5, C8, (C11)/ 2, C1, C4, C7, C10, C0, C3, C6, and C9 to address 100H, 101H, 102H, 103H, 108H, 109H, 10aH, 10bH, 110H, 111H, 112H, and 113H, respectively.

Absolute Maximum Ratings

Supply Voltage . . . . . . +8.0V
Input, Output or I/O Voltage . . . . . . GND-0.5V to V_{CC}+0.5V
Storage Temperature Range . . . . . . -65°C to +150°C
Junction Temperature. +175°C (CPGA), +150°C (MQFP and PLCC)
Lead Temperature (Soldering 10s) . . . . . . +300°C
(MQFP and PLCC - Leads Only)
ESD Classification . . . . . . Class 1
Gate Count. 32529

Thermal Information (Typical)

Thermal Resistance	θ_{JA}	θ_{JC}
MQFP	33.0°C/W	N/A
PLCC	22.0°C/W	N/A
PGA	33.5°C/W	7.5°C/W

Maximum Package Power Dissipation at +70°C
MQFP 2.4W
PLCC 3.6W
CPGA 3.1W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range, Commercial . . . . . . 5V ±5%
Operating Temperature Range, Commercial . . . . . . 0°C to +70°C

DC Electrical Specifications

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
I_{CCOP}	Power Supply Current	-	363	mA	V_{CC} = Max CLK Frequency 33MHz Note 2, Note 3, Note 4
I_{CCSB}	Standby Power Supply Current	-	500	μA	V_{CC} = Max, Outputs Not Loaded
I_I	Input Leakage Current	-10	10	μA	V_{CC} = Max, Input = 0V or V_{CC}
I_O	Output Leakage Current	-10	10	μA	V_{CC} = Max, Input = 0V or V_{CC}
V_{IH}	Logical One Input Voltage	2.0	-	V	V_{CC} = Max
V_{IL}	Logical Zero Input Voltage	-	0.8	V	V_{CC} = Min
V_{OH}	Logical One Output Voltage	2.6	-	V	I_{OH} = -400μA, V_{CC} = Min
V_{OL}	Logical Zero Output Voltage	-	0.4	V	I_{OL} = 2mA, V_{CC} = Min
V_{IHC}	Clock Input High	3.0	-	V	V_{CC} = Max
V_{ILC}	Clock Input Low	-	0.8	V	V_{CC} = Min
C_{IN}	Input Capacitance	-	12	pF	CLK Frequency 1MHz All measurements referenced to GND. T_A = +25°C, Note 1
C_{OUT}	Output Capacitance	-	12	pF	

NOTES:

1. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.
2. Power Supply current is proportional to operating frequency. Typical rating for I_{CCOP} is 11mA/MHz.
3. Output load per test load circuit and C_L = 40pF.
4. Maximum junction temperature must be considered when operating part at high clock frequencies.

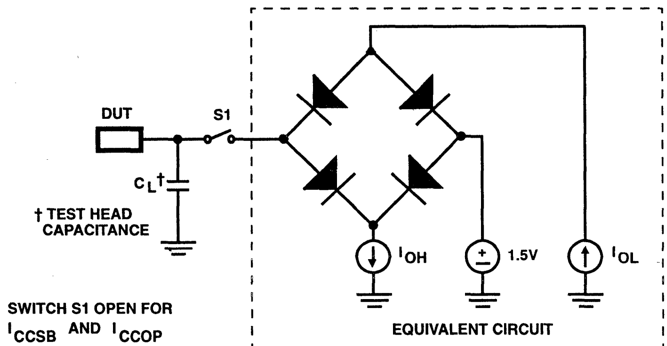
AC Electrical Specifications V_{CC} = +4.75V to +5.25V, T_A = 0°C to +70°C (Note 1)

SYMBOL	PARAMETER	-33(33MHz) MIN	-33(33MHz) MAX	-40(40.8MHz) MIN	-40(40.8MHz) MAX	-45(45MHz) MIN	-45(45MHz) MAX	COMMENTS
T_{CP}	CLK Period	30	-	24.5	-	22	-	ns
T_{CH}	CLK High	12	-	10	-	8	-	ns
T_{CL}	CLK Low	12	-	10	-	8	-	ns
T_{WP}	WR# Period	30	-	24.5	-	22	-	ns
T_{WH}	WR# High	12	-	10	-	10	-	ns
T_{WL}	WR# Low	12	-	10	-	10	-	ns
T_{AWS}	Set-up Time A0-8 to WR# Going Low	10	-	8	-	8	-	ns
T_{AWH}	Hold Time A0-8 from WR# Going High	0	-	0	-	0	-	ns
T_{CWS}	Set-up Time CIN0-9 to WR# Going High	12	-	11	-	10	-	ns
T_{CWH}	Hold Time CIN0-9 from WR# Going High	1	-	1	-	1	-	ns
T_{WLCL}	Set-up Time WR# Low to CLK Low	5	-	4	-	3	-	ns, Note 2
T_{CVCL}	Set-up Time CIN0-9 to CLK Low	7	-	7	-	7	-	ns, Note 2
T_{ECS}	Set-up Time CSEL0-5, SHFTEN#, FWRD#, RVRS#, TXFR#, INA0-9, INB0-9, ACCEN, MUX0-1 to CLK Going High	15	-	13	-	12	-	ns
T_{ECH}	Hold Time CSEL0-5, SHFTEN#, FWRD#, RVRS#, TXFR#, INA0-9, INB0-9, ACCEN, MUX0-1 to CLK Going High	0	-	0	-	0	-	ns
T_{DO}	CLK to Output Delay OUT0-27	-	14	-	13	-	12	ns
T_{OE}	Output Enable Time	-	12	-	12	-	12	ns
T_{OD}	Output Disable Time	-	12	-	12	-	12	ns, Note 3
T_{RF}	Output Rise, Fall Time	-	6	-	6	-	6	ns, Note 3

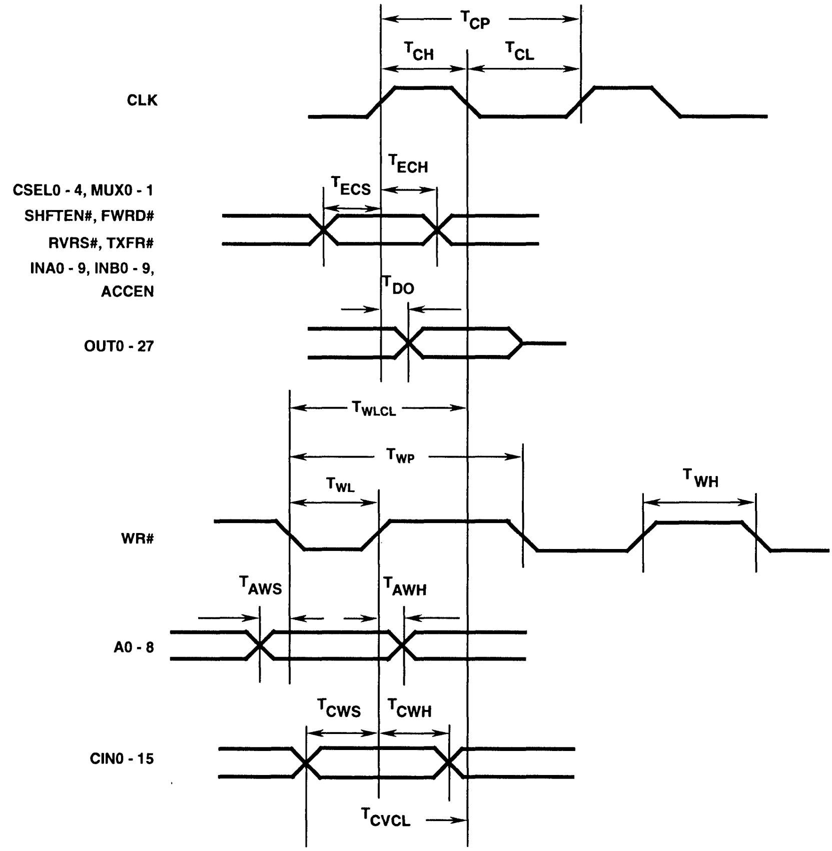
NOTES:

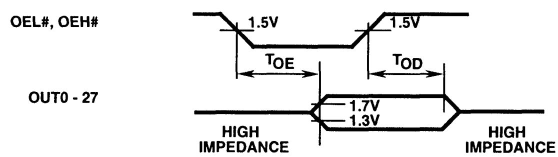
1. AC tests performed with CL = 40pF, I_{OL} = 2mA, and I_{OH} = -400μA. Input reference level CLK = 2.0V. Input reference level for all other inputs is 1.5V. Test V_{IH} = 3.0V, V_{IHC} = 4.0V, V_{IL} = 0V, V_{ILC} = 0V.
2. Set-up time requirement for loading of data on CIN0-9 to guarantee recognition on the following clock.
3. Controlled via design or process parameters and not directly tested. Characterized upon initial design and after major process and/or changes.

AC Test Load Circuit

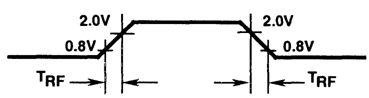


Waveforms





OUTPUT ENABLE, DISABLE TIMING



OUTPUT RISE AND FALL TIMES

SIGNAL PROCESSING NEW RELEASES 11

DIGITAL VIDEO CAPTURE

HARRIS SEMICONDUCTOR

HMP8100

ADVANCE INFORMATION

June 1995

NTSC and PAL Video Decoder with 2 Dimensional Up/Down Scaler

Features

- **High Quality 2-D Comb Filtering for Y/C Separation providing Superior Luminance Bandwidth and Reduced Display Artifacts**
- **Fully Filtered Horizontal and Vertical Up/Down Scaling Eliminating Pixel Dropping While Improving Compression Performance**
- **Multi-Standard NTSC M, PAL B, D, G, H, I, M, N and Special PAL N Decoding Offer World-Wide Compatibility**
- **Composite or S-Video Input**
- **Accepts any 20 - 40MHz Source Clock Allowing Single Crystal Operation**
- **384 x 16 Programmable Depth Data FIFO with Full Flag Control to Ease Frame Buffer Interfacing**
- **User Selectable Color Trap and Low Pass Video Filters**
- **User Selectable Hue, Color Saturation, Contrast, Sharpness, and Brightness Controls**
- **Vertical Upscaling from 240 to 288 Lines Per Field for H.261 Specification Compatibility**
- **CCIR601, CIF, QCIF and SIF Output Data Formats**
- **4:2:2, 4:2:0 YC_BC_R Pre-Compression Output Data Formats Supporting JPEG, MPEG1, MPEG2, H.261/263**
- **Area of Interest Selection, with Horizontal and Vertical Cropping Capability**
- **Byte Wide Microprocessor Control Interface**

Applications

- **Multimedia**
- **Video Conferencing**
- **Video Capture**
- **LCD Projection Video Panels**
- **JPEG, MEPG1, MPEG2 Compression**
- **Video Security Systems**
- **Professional/Broadcast Video**
- **Medical Imaging**

Description

The HMP8100 is a high quality, 8-bit, digital video color decoder with output scaling capability. The Video Decoder Scaler (VDS) is compatible with NTSC M, PAL B, D, G, H, I, M, N and special case PAL N video standards. Both composite (CVBS) and S-Video (Y/C) video input formats are supported. A two line comb filter, plus user selectable Chrominance trap filter provide high quality Chroma/Luma separation. Following the decode function, various adjustments can be made to customize the video content such as Brightness, Contrast, Color Saturation, Hue and Sharpness functions. Video synchronization is achieved with a 4 x f_{SC} chroma burst lock PLL for color demodulation and line lock PLL for correct pixel alignment.

The 2 Dimensional scaling allows lines to be downscaled in 2 pixel increments and fields to be downscaled in single line increments. Vertical upscaling from 240 lines/field to 288 lines/field are provided to support video conferencing applications. All downscaling is properly filtered from 1:1 to 1:32 image size reduction. Two Chrominance sub-sampling schemes are provided (4:2:2 or 4:2:0) to reduce image bandwidth. Multiple downscaled image sizes that support JPEG, MPEG1, MPEG2 and H.261/263 are provided. The video output data port provides seamless DRAM, or VRAM serial port interfacing with a programmable 384 x 16 deep FIFO.

The HMP8100 can be used for video capture input within a video system. The high quality chrominance/luminance separation and control, fully filtered scaling, and integrated phase locked loops are ideal for use with todays powerful compression processors. The HMP8100 operates from a single +5V supply; is TTL/CMOS compatible and is available in a Commercial grade, 100 lead plastic MQFP.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HMP8100CV	0^oC to 70^oC	100 Lead Plastic MQFP

11

DIGITAL VIDEO CAPTURE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number 4023

SIGNAL PROCESSING NEW RELEASES 12

TELECOMMUNICATIONS

PAGE

TELECOMMUNICATION DATA SHEET

HARRIS SEMICONDUCTOR

HC-5513

PRELIMINARY

July 1995

Subscriber Line Interface Circuit

Features

- DI Monolithic High Voltage Process
- Programmable Current Feed
- Programmable Loop Current Detector Threshold and Battery Feed Characteristics
- Ground Key and Ring trip Detection
- Compatible with Industry Standards Types
- Thermal Shutdown
- On-Hook Transmission
- Wide Battery Voltage Range (-24V to -56V)
- Low Standby Power
- Meets TR-NWT-000057 Transmission Requirements
- -40°C to +85°C Ambient Temperature Range

Applications

- Digital Loop Carrier Systems
- Fiber-In-The-Loop ONUs

Description

The HC-5513 is a subscriber line interface circuit design to match industry standard PBL3764 for PBX and DLC applications. Enhancements include: lower noise and absence of false signaling in the presence of longitudinal currents.

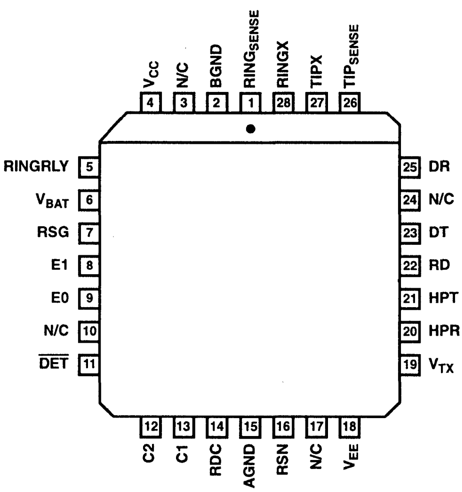
The HC-5513 is fabricated in a High Voltage Dielectrically Isolated (DI) Bipolar Process that eliminates leakage currents and device latch-up problems normally associated with junction isolated ICs. The elimination of the leakage currents results in improved circuit performance for wide temperature extremes. The latch free benefit of the DI process guarantees operation under adverse transient conditions. This process feature makes the HC-5513 ideally suited for use in harsh outdoor environments.

Ordering Information

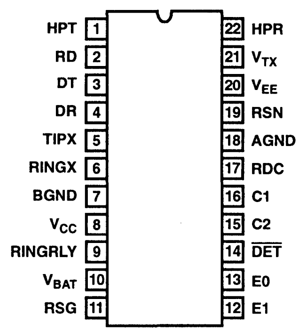
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HC5513IMA02	-40°C to +85°C	28 Lead PLCC
HC5513IPA02	-40°C to +85°C	22 Lead Plastic DIP

Pinouts

HC5513
(PLCC)
TOP VIEW



HC-5513
(DIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3963**

Absolute Maximum Ratings

Temperature
- Storage Temperature Range . . . . -65°C to +150°C
- Operating Temperature Range . . . . -40°C to +110°C
- Operating JunctionTemperature Range . . . . -40°C to +150°C

Power Supply ($-40^oC \leq T_A \leq +85^oC$)
- Supply Voltage V_{CC} to GND . . . . 0.5V to 7V
- Supply Voltage V_{EE} to GND . . . . -7V to 0.5V
- Supply Voltage V_{BAT} to GND . . . . -70V to 0.5V

Ground
- Voltage between AGND and BGND . . . . . -0.3V to 0.3V

Relay Driver
- Ring Relay Supply Voltage . . . . 0V to V_{BAT} +75V
- Ring Relay Current 50mA

Ring Trip Comparator
- Input Voltage . . . . V_{BAT} to 0V
- Input Current . . . . -5mA to 5mA

Digital Inputs, Outputs (C1, C2, E0, E1, $\overline{DET}$)
- Input Voltage . . . . 0V to V_{CC}
- Output Voltage ($\overline{DET}$ not Active) . . . . . 0V to V_{CC}
- Output Current($\overline{DET}$) 5mA

Tipx and Ringx Terminals ($-40^oC \leq T_A \leq +85^oC$)
- Tipx or Ringx Voltage, Continous (Referenced to GND) . V_{BAT} to+2V
- Tipx or Ringx , Pulse <10ms, t_{REP} >10s . . . . . V_{BAT}-20V to+5V
- Tipx or Ringx , Pulse <10μs, t_{REP} >10s . . . . . V_{BAT}-40V to+10V
- Tipx or Ringx , Pulse <250ns, t_{REP} >10s . . . . V_{BAT}-70V to+15V
- Tipx or Ringx Current 70mA
- Gate Count . . . . 543 Transistors, 51 Diodes

Thermal Information (Typical)

Thermal Resistance — θ_{JA}
- 22 Lead Plastic DIP . . . . 75°C/W
- 28 Lead PLCC . . . . 65°C/W

Package Power Dissipation at +70°C
- 22 Lead Plastic DIP 1.06W
- 28 Lead PLCC 1.23W

Derate Above +70°C
- Plastic DIP . . . . 13.3mW/°C
- PLCC . . . . 15.4mW/°C

Lead Temperature (Soldering 10s) . . . . +300°C
(PLCC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Typical Operating Conditions

These represent the conditions under which the part was developed and are suggested as guidelines.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Case Temperature		-40	-	100	
V_{CC} with Respect to AGND	-40°C to +85°C	4.75	-	5.25	V
V_{EE} with Respect to AGND	-40°C to +85°C	-5.25	-	-4.75	V
V_{BAT} with Respect to BGND	-40°C to +85°C	-58	-	-24	V

Electrical Specifications

T_A = -40°C to +85°C, V_{CC} = +5V ±5%, V_{EE} = +5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, $R_{DC1} = R_{DC2}$ = 41.2kΩ, R_D = 39kΩ, $R_{SG} = \infty$, C_{HP} = 10nF, C_{DC} = 1.5μF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Overload Level	1% THD, Z_L = 600Ω, 2.16μF (Note 1, Figure 1)	3.1	-	-	V_{PEAK}
Longitudinal Impedance (Tip/Ring)	0 < f < 100Hz (Note 2, Figure 2)	-	20	35	Ω/Wire

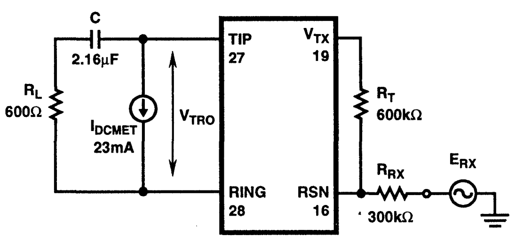


FIGURE 1. OVERLOAD LEVEL (TWO-WIRE PORT)

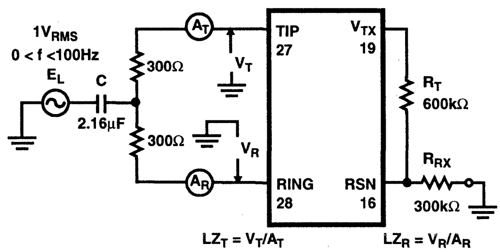


FIGURE 2. LONGITUDINAL IMPEDANCE

Electrical Specifications T_A = -40°C to +85°C, V_{CC} = +5V ±5%, V_{EE} = +5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LONGITUDINAL CURRENT LIMIT (TIP/RING)					
Off Hook (Active)	No False Detections, (GND Key, Loop Current), LB > 45dB (Note 3, Figure 3A)	-	-	20	mA_{PEAK} /Wire
On Hook (Standby), R_L = ∞	No False Detections (GND Key, Loop Current) (Note 4, Figure 3B)	-	-	5	mA_{PEAK} /Wire

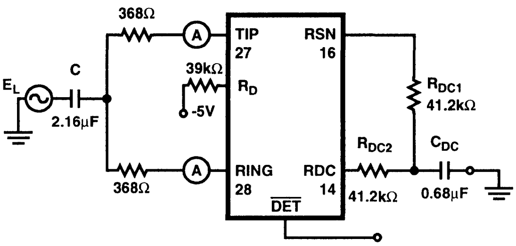


FIGURE 3A. OFF-HOOK

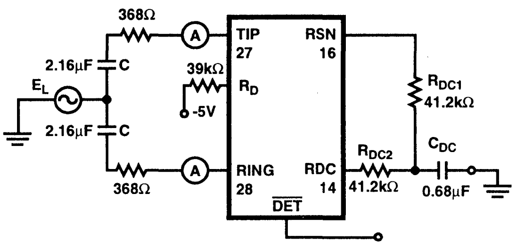
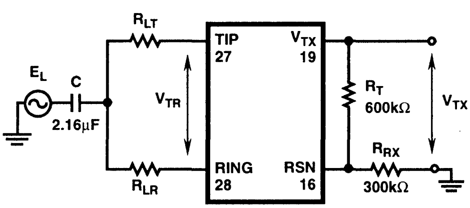


FIGURE 3B. ON-HOOK

FIGURE 3. LONGITUDINAL CURRENT LIMIT

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OFF-HOOK LONGITUDINAL BALANCE					
Longitudinal to Metallic	IEEE 455 - 1985, R_{LR}, R_{LT} = 368Ω 0.2kHz < f < 4.0kHz (Note 5, Figure 4)	55	70	-	dB
Longitudinal to Metallic	R_{LR}, R_{LT} = 300Ω, 0.2kHz < f < 4.0kHz (Note 5, Figure 4)	55	70	-	dB
Metallic to Longitudinal	FCC Part 68, Para 68.310 0.2kHz < f < 1.0kHz	50	55	-	dB
	1.0kHz < f < 4.0kHz (Note 6)	50	55	-	dB
Longitudinal to 4-Wire	0.2kHz < f < 4.0kHz (Note 7, Figure 4)	55	70	-	dB
Metallic to Longitudinal	R_{LR}, R_{LT} = 300Ω, 0.2kHz < f < 4.0kHz (Note 8, Figure 5)	50	55	-	dB
4-Wire to Longitudinal	0.2kHz < f < 4.0kHz (Note 9, Figure 5)	50	55	-	dB



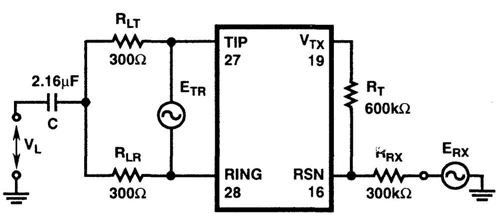


FIGURE 4. LONGITUDINAL TO METALLIC AND LONGITUDINAL TO 4-WIRE BALANCE

FIGURE 5. METALLIC TO LONGITUDINAL AND 4-WIRE TO LONGITUDINAL BALANCE

Electrical Specifications T_A = -40°C to +85°C, V_{CC} = +5V ±5%, V_{EE} = +5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, C_{HP} = 10nF, C_{DC} = 1.5μF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2-Wire Return Loss	0.2kHz to 0.5kHz (Note 10, Figure 8)	25	-	-	dB
	0.5kHz to 1.0kHz (Note 10, Figure 8)	27	-	-	dB
	1.0kHz to 3.4kHz (Note 10, Figure 8)	23	-	-	dB
TIP IDLE VOLTAGE					
Active, I_L = 0		-	-4		V
Standby, I_L = 0		-	<0		V
RING IDLE VOLTAGE					
Active, I_L = 0			-24	-	V
Standby, I_L = 0			-28	-	V
4-WIRE TRANSMIT PORT (V_{TX})					
Overload Level	(Z_L > 20kΩ, 1% THD) (Note 11, Figure 9)	3.1	-	-	V_{PEAK}
Output Offset Voltage	E_G = 0, Z_L= •, (Note 12, Figure 9)	-30	-	30	mV
Output Impedance (Guaranteed by Design)	0.2kHz < f < 03.4kHz	-	5	20	Ω
2- to 4-Wire (Metallic to V_{TX}) Voltage Gain	0.3kHz < f < 03.4kHz (Note 13, Figure 9)	0.98	1.0	1.02	V/V

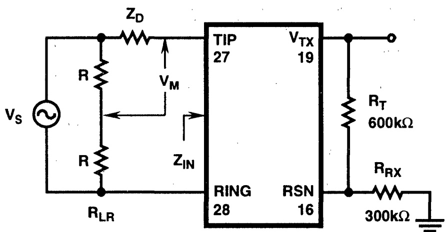


FIGURE 8. TWO-WIRE RETURN LOSS

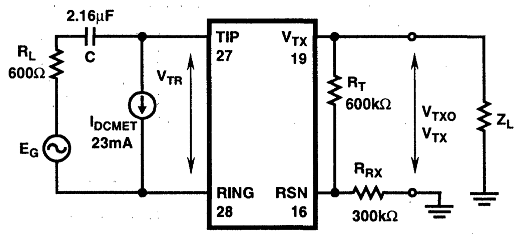


FIGURE 9. OVERLOAD LEVEL (4-WIRE TRANSMIT PORT), OUTPUT OFFSET VOLTAGE, 2-WIRE TO 4-WIRE VOLTAGE GAIN AND HARMONIC DISTORTION

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
4-WIRE RECEIVE PORT (RSN)					
DC Voltage	I_{RSN} = 0mA	-	0	-	V
R_X Sum Node Impedance	0.3kHz < f < 3.4kHz	-	-	20	Ω
Current Gain-RSN to Metallic	0.3kHz < f < 3.4kHz (Note 14, Figure 10)	980	1000	1020	Ratio
FREQUENCY RESPONSE (OFF HOOK)					
2-Wire to 4-Wire	0dBm at 1.0kHz, E_{RX} = 0V 0.3kHz < f < 3.4kHz (Note 15, Figure 11)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm at 1.0kHz, E_G = 0V 0.3kHz < f < 3.4kHz (Note 16, Figure 11)	-0.2	-	0.2	dB
4-Wire to 4-Wire	0dBm at 1.0kHz, E_G = 0V 0.3kHz < f < 3.4kHz (Note 17, Figure 11)	-0.2	-	0.2	dB
INSERTION LOSS					
2-Wire to 4-Wire	0dBm, 1kHz (Note 18, Figure 11)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm, 1kHz (Note 19, Figure 11)	-0.2	-	0.2	dB

Electrical Specifications T_A = -40°C to +85°C, V_{CC} = +5V ±5%, V_{EE} = +5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, C_{HP} = 10nF, C_{DC} = 1.5μF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GAIN TRACKING (Ref = -10dBm, at 1.0kHz)					
2-Wire to 4-Wire	-40dBm to +3dBm (Note 20, Figure 11)	-0.1	-	0.1	dB
2-Wire to 4-Wire	-55dBm to -40dBm (Note 20, Figure 11)	-	±0.03	-	dB
4-Wire to 2-Wire	-40dBm to +3dBm (Note 21, Figure 11)	-0.1	-	0.1	dB
4-Wire to 2-Wire	-55dBm to -40dBm (Note 21, Figure 11)	-	±0.03	-	dB

$$K = I_M\left(\frac{(R_{DC1}+R_{DC2})}{V_{RDC}-V_{RSN}}\right)$$

Where K ≈ 1000

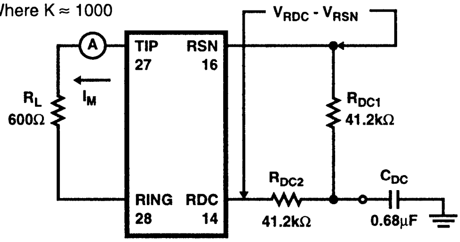


FIGURE 10. CURRENT GAIN -RSN TO METALLIC

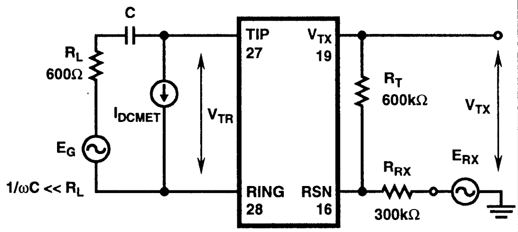


FIGURE 11. FREQUENCY RESPONSE, INSERTION LOSS, GAIN TRACKING AND HARMONIC DISTORTION

NOISE					
Idle Channel Noise at 2-Wire	C-Message Weighting (Note 22, Figure 12)	-	7.5	8.9	dBrnC
Idle Channel Noise at 4-Wire	C-Message Weighting (Note 23, Figure 12)	-	-	8.9	dBrnC
HARMONIC DISTORTION					
2-Wire to 4-Wire	0dBm, 1kHz (Note 24, Figure 9)	-	-65	-54	dB
4-Wire to 2-Wire	0dBm, 0.3kHz to 3.4kHz (Note 25, Figure 11)	-	-65	-54	dB
BATTERY FEED CHARACTERISTICS					
Constant Loop Current Tolerance R_{DCX} = 41.2kΩ	I_L =2500/(R_{DC1} + R_{DC2}), -40°C to +85°C (Note 26)	$0.9I_L$	I_L	$1.1I_L$	mA
Loop Current Tolerance (Standby)	I_L =(V_{BAT}-3)/(R_L+1800), -40°C to +85°C (Note 27)	$0.8I_L$	I_L	$1.2I_L$	mA
Open Circuit Voltage (V_{TIP} - V_{RING})	-40°C to +85°C, (Active)	15	-	19	V
LOOP CURRENT DETECTOR					
On Hook to Off Hook	R_D = 39kΩ -40°C to +85°C	372/R_D	465/R_D	558/R_D	mA
Off Hook to On Hook	R_D = 39kΩ -40°C to +85°C	325/R_D	405/R_D	485/R_D	mA
Loop Current Hysteresis	R_D = 39kΩ -40°C to +85°C	25/R_D	60/R_D	95/R_D	mA

12

TELECOMMUNI-CATIONS

Electrical Specifications T_A = -40°C to +85°C, V_{CC} = +5V ±5%, V_{EE} = +5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GROUND KEY DETECTOR					
Tip/Ring Current Difference - Trigger	(Note 28, Figure 13)	8	12	17	mA
Tip/Ring Current Difference - Reset	(Note 28, Figure 13)	3	7	12	mA
Hysteresis	(Note 28, Figure 13)	0	5	9	mA

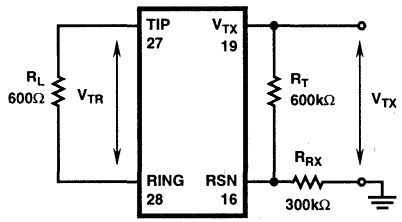


FIGURE 12. IDLE CHANNEL NOISE

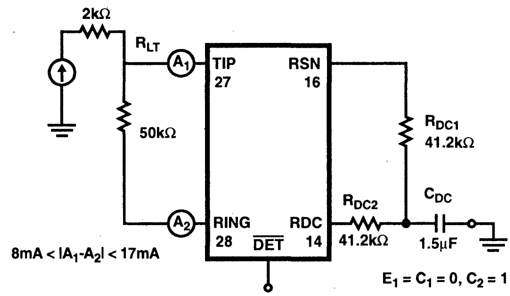


FIGURE 13. GROUND KEY DETECT

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RING TRIP DETECTOR (DT, DR)					
Offset Voltage	Source Res = 0	-20	-	20	mV
Input Bias Current	Source Res = 0	-500	-	500	nA
Input Common-Mode Range	Source Res = 0	V_{BAT}+1	-	0	V
Input Resistance	Source Res = 0 Balanced	3	-	-	MΩ
RING RELAY DRIVER					
V_{SAT} at 25mA	I_{OL} = 25mA	-	1.0	1.5	V
Off-State Leakage Current	V_{OH} = 12V	-	-	10	µA
DIGITAL INPUTS (E0, E1, C1, C2)					
Input Low Voltage, V_{IL}		0	-	0.8	V
Input High Voltage, V_{IH}		2	-	V_{CC}	V
Input Low Current, I_{IL}: C1,C2	V_{IL}=0.4V	-200	-	-	µA
Input Low Current, I_{IL}: E0,E1	V_{IL}=0.4V	-100	-	-	µA
Input High Current	V_{IH}=2.4V	-	-	40	µA
DETECTOR OUTPUT ($\overline{DET}$)					
Output Low Voltage, V_{OL}	I_{OL} = 2mA	-	-	0.45	V
Output High Voltage, V_{OH}	I_{OH} = 100µA	2.7	-	-	V
Internal Pull-up Resistor		10	15	20	kΩ
Power Dissipation					
Open Circuit State	C1 = C2 = 0	-	-	23	mW
On Hook, Standby	C1 = C2 = 1	-	-	30	mW

Electrical Specifications T_A = -40°C to +85°C, V_{CC} = +5V ±5%, V_{EE} = +5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, C_{HP} = 10nF, C_{DC} = 1.5µF, Z_L = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. **(Continued)**

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook, Active	C1 = 0, C2 = 1, R_L = High Impedance	-	-	150	mW
Off Hook, Active	R_L = 0Ω	-	-	1.0	W
	R_L = 300Ω	-	-	0.72	W
	R_L = 600Ω	-	-	0.45	W
TEMPERATURE GUARD					
Thermal Shutdown		150	-	180	°C
SUPPLY CURRENTS (V_{BAT} = -28V)					
I_{CC}, On Hook	Open Circuit State (C1, 2 = 0, 0)	-	-	1.5	mA
	Standby State (C1, 2 = 1, 1)	-	-	1.7	mA
	Active State (C1, 2 = 0,1)	-	-	5.5	mA
I_{EE}, On Hook	Open Circuit State (C1, 2 = 0, 0)	-	-	0.8	mA
	Standby State (C1, 2 = 1, 1)	-	-	0.8	mA
	Active State (C1, 2 = 0, 1)	-	-	2.2	mA
I_{BAT}, On Hook	Open Circuit State (C1, 2 = 0, 0)	-	-	0.4	mA
	Standby State (C1, 2 =1, 1)	-	-	0.6	mA
	Active State (C1, 2 = 0, 1)	-	-	3.9	mA
PSRR					
V_{CC} to 2 or 4-Wire port	(Note 29, Figure 14)	-	50	-	dB
V_{EE} to 2 or 4-Wire port	(Note 29, Figure 14)	-	50	-	dB
V_{BAT} to 2 or 4-Wire port	(Note 29, Figure 14)	-	50	-	dB

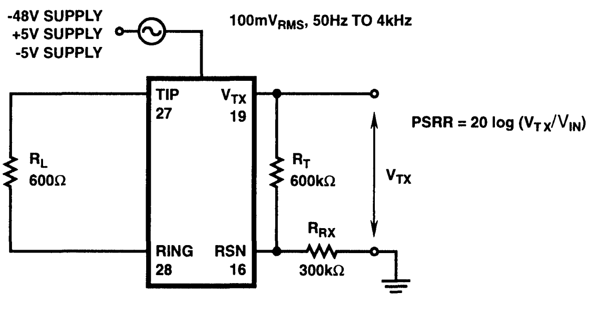


FIGURE 14. POWER SUPPLY REJECTION RATIO

12

TELECOMMUNI-
CATIONS

NOTES:

1. **Overload Level (Two-Wire port)** - The overload level is specified at the 2-wire port (V_{TR0}) with the signal source at the 4-wire receive port (E_{RX}). I_{DCMET} = 23mA, increase the amplitude of E_{RX} until 1% THD is measured at V_{TRO}. Reference Figure 1.
2. **Longitudinal Impedance** - The longitudinal impedance is computed using the following equations, where TIP and RING voltages are referenced to ground. L_{ZT}, L_{ZR}, V_T, V_R, A_R and A_T are defined in Figure 2.

   (TIP) $L_{ZT} = V_T/A_T$

   (RING) $L_{ZR} = V_R/A_R$

   where: $E_L = 1V_{RMS}$ (0Hz to 100Hz)
3. **Longitudinal Current Limit (Off Hook Active)** - Off Hook (Active, C1 = 1, C2 = 0) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3a) until the 2-wire longitudinal balance drops below 45dB. $\overline{DET}$ pin remains high (no false detection).
4. **Longitudinal Current Limit (On Hook Standby)** - On Hook (Active, C1 = 1, C2 = 1) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3b) until the 2-wire longitudinal balance drops below 45dB. $\overline{DET}$ pin remains high (no false detection).
5. **Longitudinal to Metallic Balance** - The longitudinal to metallic balance is computed using the following equation.

   BLME = 20 • log (E_L/V_{TR}), where: E_L and V_{TR} are defined in Figure 4.
6. **Metallic to Longitudinal FCC Part 68, Para 68.310** - The metallic to longitudinal balance is defined in the above mentioned spec.
7. **Longitudinal to Four-Wire Balance** - The longitudinal to 4-wire balance is computed using the following equation.

   BLFE = 20 • log (E_L/V_{TX}),: E_L and V_{TX} are defined in Figure 4.
8. **Metallic to Longitudinal Balance** - The metallic to longitudinal balance is computed using the following equation.

   BMLE = 20 • log (E_{TR}/V_L), E_{RX} = 0

   where: E_{TR}, V_L and E_{RX} are defined in Figure 5.
9. **Four-Wire to Longitudinal Balance** - The 4-wire to longitudinal balance is computed using the following equation.

   BFLE = 20 • log (E_{RX}/V_L), E_{TR} = source is removed.

   where: E_{RX}, V_L and E_{TR} are defined in Figure 5.
10. **Two-Wire Return Loss** - The 2-wire return loss is computed using the following equation.

    r = -20 • log ($2V_M/V_S$)

    where: Z_D = The desired impedance; e.g., the characteristic impedance of the line, nominally 600Ω. (Reference Figure 8).
11. **Overload Level (4-Wire port)** - The overload level is specified at the 4-wire transmit port (V_{TXO}) with the signal source (E_G) at the 2-wire port, I_{DCMET} = 23mA, ZL = 20kΩ (Reference Figure 9). Increase the amplitude of E_G until 1% THD is measured at V_{TXO}. Note that the gain from the 2-wire port to the 4-wire port is equal to 1.
12. **Output Offset Voltage** - The output offset voltage is specified with the following conditions: E_G = 0, I_{DCMET} = 23mA, ZL = ∞ and is measured at V_{TX}. E_G, I_{DCMET}, V_{TX} and Z_L are defined in Figure 9.
13. **Two-Wire to Four-Wire (Metallic to V_{TX}) Voltage Gain** - The 2-wire to 4-wire (metallic to V_{TX}) voltage gain is computed using the following equation.

    $G_{2-4} = V_{TX}/V_{TR}$), E_G = 0dBm0, V_{TX}, V_{TR}, and E_G are defined in Figure 9.
14. **Current Gain RSN to Metallic** - The current gain RSN to Metallic is computed using the following equation.

    $K = I_M [(R_{DC1} + R_{DC2})/(V_{RDC} - V_{RSN})]$ K, I_M, R_{DC1}, R_{DC2}, V_{RDC} and V_{RSN} are defined in Figure 10.
15. **Two-Wire to Four-Wire Frequency Response** - The 2-wire to 4-wire frequency response is measured with respect to E_G = 0dBm at 1.0kHz, E_{RX} = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation.

    F_{2-4} = 20 • log (V_{TX}/V_{TR}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX}, V_{TR}, and E_G are defined in Figure 11.
16. **Four-Wire to Two-Wire Frequency Response** - The 4-wire to 2-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz, E_G = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation.

    F_{4-2} = 20 • log (V_{TR}/E_{RX}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TR} and E_{RX} are defined in Figure 11.
17. **Four-Wire to Four-Wire Frequency Response** - The 4-wire to 4-wire frequency response is measured with respect to E_{RX} = 0dBm at 1.0kHz,E_G = 0V, I_{DCMET} = 23mA. The frequency response is computed using the following equation.

    F_{4-4} = 20 • log (V_{TX}/E_{RX}), vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.

    V_{TX} and E_{RX} are defined in Figure 11.

18. **Two-Wire to Four-Wire Insertion Loss** - The 2-wire to 4-wire Insertion loss is measured with respect to E_G = 0dBm at 1.0kHz input signal, E_{RX} = 0, I_{DCMET} = 23mA and is computed using the following equation.

$L_{2-4} = 20 \bullet \log (V_{TX}/V_{TR})$

where: V_{TX}, V_{TR}, and E_G are defined in Figure 11. (Note: The fuse resistors, R_F, impact the insertion loss. The specified insertion loss is for R_F = 0).

19. **Four-Wire to Two-Wire Insertion Loss** - The 4-wire to 2-wire Insertion loss is measured based upon E_{RX} = 0dBm, 1.0kHz input signal, E_G = 0, I_{DCMET} = 23mA and is computed using the following equation.

$L_{4-2} = 20 \bullet \log (V_{TR}/E_{RX})$

where: V_{TR} and E_{RX} are defined in Figure 11.

20. **Two-Wire to Four-Wire Gain Tracking** - The 2-wire to 4-wire gain tracking is referenced to measurements taken for E_G =-10dBm, 1.0kHz signal, E_{RX} = 0, I_{DCMET} = 23mA and is computed using the following equation.

$G_{2-4} = 20 \bullet \log (V_{TX}/V_{TR})$ vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

V_{TX} and V_{TR} are defined in Figure 11.

21. **Four-Wire to Two-Wire Gain Tracking** - The 4-wire to 2-wire gain tracking is referenced to measurements taken for E_{RX} = -10dBm, 1.0kHz signal, E_G = 0, I_{DCMET} = 23mA and is computed using the following equation.

$G_{4-2} = 20 \bullet \log (V_{TR}/E_{RX})$ vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.

V_{TR} and E_{RX} are defined in Figure 11. The level is specified at the 4-wire receive port and referenced to a 600Ω impedance level.

22. **Two-Wire Idle Channel Noise** - The 2-wire idle channel noise at V_{TR} is specified with the 2-wire port terminated in 600Ω (R_L) and with the 4-wire receive port grounded (Reference Figure 12).

23. **Four-Wire Idle Channel Noise** - The 4-wire idle channel noise at V_{TX} is specified with the 2-wire port terminated in 600Ω (R_L). The noise specification is with respect to a 600Ω impedance level at V_{TX}. The 4-wire receive port is grounded (Reference Figure 12).

24. **Harmonic Distortion (2-Wire to 4-Wire)** - The harmonic distortion is measured with the following conditions. E_G = OdBm at 1kHz, I_{DCMET} = 23mA. Measurement taken at V_{TX}. (Reference Figure 9).

25. **Harmonic Distortion (4-Wire to 2-Wire)** - The harmonic distortion is measured with the following conditions. E_{RX} = OdBm0. Vary frequency between 300Hz and 3.4kHz, I_{DCMET} = 23mA. Measurement taken at V_{TR}. (Reference Figure 11).

26. **Constant Loop Current** - The constant loop current is calculated using the following equation.

$I_L = 2500 / (R_{DC1} + R_{DC2})$

27. **Standby State Loop Current** - The Standby state loop current is calculated using the following equation.

$I_L = [|V_{BAT}| - 3] / [R_L + 1800]$, $T_{amb} = 25^oC$

28. **Ground Key Detector** - (TRIGGER) Increase the input current to verify that if $A_1 - A_2 > 8mA$ then $\overline{DET}$ goes Low. A_1 and A_2 are defined in Figure 13.

(RESET) Decrease the input current to verify that if $A_1 - A_2 < 3mA$ then $\overline{DET}$ goes high. A_1 and A_2 are defined in Figure 13

(Hysteresis) Compare difference between trigger and reset.

29. **Power Supply Rejection Ratio** - Inject a $100mV_{RMS}$ signal (50Hz to 4kHz) on V_{BAT}, V_{CC} and V_{EE} supplies. PSRR is computed using the following equation.

$PSRR = 20 \bullet \log (V_{TX}/V_{IN})$. V_{TX} and V_{IN} are defined in Figure 14.

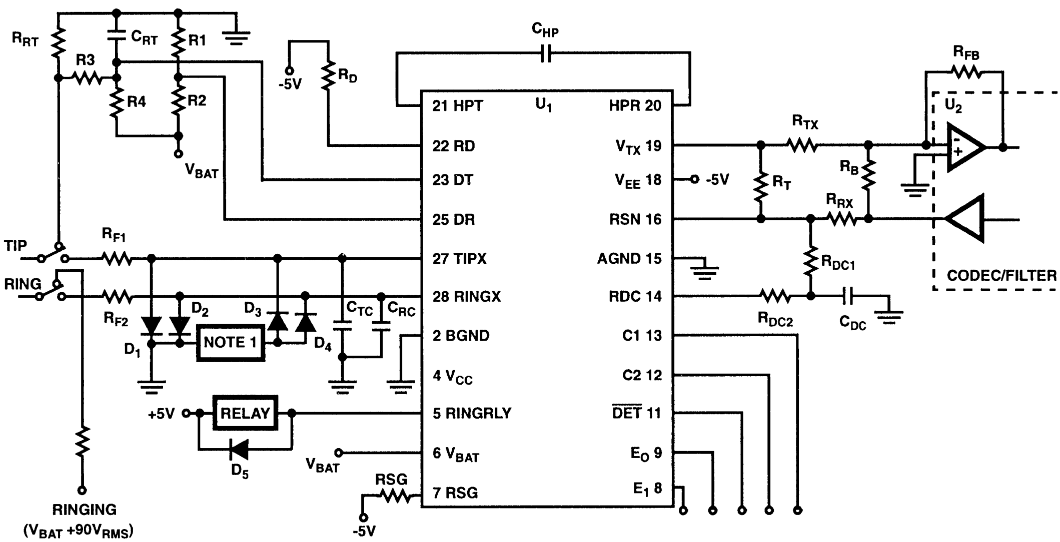
Pin Descriptions

PLCC	PDIP	SYMBOL	DESCRIPTION
1		$RING_{SENSE}$	Internally connected to output of RING power amplifier.
2	7	$\overline{BGND}$	Battery Ground - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from AGND but it is recommended that it is connected to the same potential as AGND
4	8	V_{CC}	+5V power supply.
5	9	RINGRLY	Ring relay driver output.
6	10	V_{BAT}	Battery supply voltage, -48V to -56V.
7	11	RSG	Saturation guard programming resistor pin.

Pin Descriptions (Continued)

PLCC	PDIP	SYMBOL	DESCRIPTION
8	12	E1	TTL compatible logic input. The logic state of E1 in conjunction with the logic state of C1 determines which detector is gated to the $\overline{DET}$ (pin 11) output.
9	13	E0	TTL compatible logic input. Enables the $\overline{DET}$ (pin 11) output when set to logic level zero and disables $\overline{DET}$ output when set to a logic level one.
11	14	DET	Detector output. TTL compatible logic output. A zero logic level indicates that the selected detector was triggered (see truth table for selection of Ground Key detector, Loop Current detector or the Ring Trip detector). The $\overline{DET}$ output is an open collector with an internal pull-up of approximately 15kΩ to V_{CC}
12	15	C2	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
13	16	C1	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
14	17	RDC	DC feed current programming resistor pin. Constant current feed is programmed by resistors R_{DC1} and R_{DC2} connected in series from this pin to the receive summing node (RSN, pin16). The resistor junction point is decoupled to AGND to isolate the AC signal components.
15	18	AGND	Analog ground.
16	19	RSN	Receive Summing Node. The AC and DC current flowing into this pin establishes the metallic loop current that flows between TIP (pin 27) and RING (pin 28). The magnitude of the metallic loop current is 1000 times greater than the current into the RSN pin. The constant current programming resistors and the networks for program receive gain and 2-wire impedance all connect to this pin.
18	20	V_{EE}	-5V power supply.
19	21	V_{TX}	Transmit audio output. This output is equivalent to the TIP to RING metallic Voltage. The network for programming the 2-wire input impedance connects between this pin and RSN (pin 16).
20	22	HPR	RING side of AC/DC separation capacitor C_{HP}. C_{Hp} is required to properly separate the RING AC current from the DC loop current. The other end of C_{HP} is connected to pin 21 HPT.
21	1	HPT	TIP side of AC/DC separation capacitor C_{HP}. C_{Hp} is required to properly separate the TIP AC current from the DC loop current. The other end of C_{HP} is connected to pin 20 HPR.
22	2	RD	Loop current programming resistor. Resistor R_D sets the trigger level for the loop current detect circuit. A filter capacitor C_D is also connected between this pin and V_{EE} (pin 18).
23	3	DT	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT (pin 23) and DR (pin 25).
25	4	DR	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT (pin 23) and DR (pin 25).
26		TIP_{SENSE}	Internally connected to output of TIP power amplifier.
27	5	TIPX	Output of TIP power amplifier.
28	6	RINGX	Output of RING power amplifier.
3, 10, 17, 24		$\overline{N/C}$	No internal connection.

Applications Diagram



U1	SLIC (SUBSCRIBER LINE INTERFACE CIRCUIT) HC-5513
U2	COMBINATION CODEC/FILTER E.G. CD22354A OR PROGRAMMABLE CODEC/ FILTER, E.G. SLAC
C_{DC}	1.5μF, 20%,10V
C_{HP}	10nF, 20%,100V
C_{RT}	0.39μF, 20%,100V
C_{TC}, C_{RC}	2200pF, 20%,10V
RELAY	RELAY, 2C CONTACTS, 12V COIL
D_1 - D_4	DIODE, 100V, 3A
D_5	DIODE 1N4454

R_{F1}, R_{F2}	LINE RESISTOR, 20Ω, 1% MATCH
R_1, R_3	200kΩ, 5%, 1/4W
R_2	910kΩ, 5%, 1/4W
R_4	1.2MΩ, 5%, 1/4W
R_B	75.5kΩ,1%, 1/4W
R_D	39kΩ, 5%, 1/4W
R_{DC1}, R_{DC2}	41.2kΩ, 5%, 1/4W
R_{FB}	20.0kΩ, 1%, 1/4W
R_{RX}	300kΩ, 1%, 1/4W
R_T	600kΩ, 1%, 1/4W
R_{TX}	20kΩ, 1%, 1/4W
R_{RT}	150Ω, 5%, 2W
R_{SG}	Open Circuit

NOTE:

1. The anodes of D_3 and D_4 may be connected directly to the V_{BAT} supply if the application is exposed to only low energy transients. For harsher environments it is recommended that the anodes of D_3 and D_4 be shorted to ground through a transzorb or surgector.

SLIC Operating States

STATE	E0	E1	C1	C2	SLIC OPERATING STATE	ACTIVE DETECTOR	$\overline{\text{DET}}$ OUTPUT
1	0	0	0	0	Open Circuit	No Active Detector	Logic Level High
2	0	0	0	1	Active	Ground Key Detector	Ground Key Status
3	0	0	1	0	Ringing	No Active Detector	Logic Level High
4	0	0	1	1	Standby	Ground Key Detector	Ground Key Status
5	0	1	0	0	Open Circuit	No Active Detector	Logic Level High
6	0	1	0	1	Active	Loop Current Detector	Loop Current Status
7	0	1	1	0	Ringing	Ring Trip Detector	Ring Trip Status
8	0	1	1	1	Standby	Loop Current Detector	Loop Current Status
9	1	0	0	0	Open Circuit	No Active Detector	Logic Level High
10	1	0	0	1	Active	Ground Key Detector	
11	1	0	1	0	Ringing	No Active Detector	
12	1	0	1	1	Standby	Ground Key Detector	
13	1	1	0	0	Open Circuit	No Active Detector	
14	1	1	0	1	Active	Loop Current Detector	
15	1	1	1	0	Ringing	Ring Trip Detector	
16	1	1	1	1	Standby	Loop Current Detector	

HARRIS QUALITY AND RELIABILITY

PAGE

Harris Quality

Introduction

Success in the integrated circuit industry means more than simply meeting or exceeding the demands of today's market. It also includes anticipating and accepting the challenges of the future. It results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force – from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of the Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX, Quality professionals support other continuous improvement tools such as control charts, measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs – with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

The Improvement Process

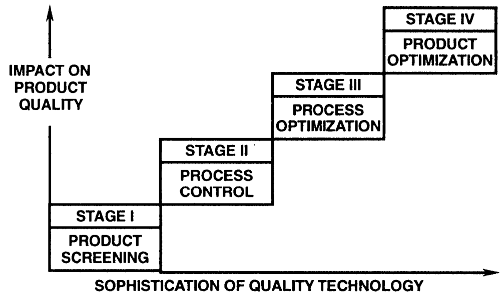


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage III to Stage IV, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

ISO 9000 Certification

The manufacturing operations of Harris Semiconductor have all received ISO certification. The ISO 9000 series of standards were very consistent with our goals to build an even stronger quality system foundation.

Qualified Manufacturing List (QML)

Harris Semiconductor has supplied military grade integrated circuits for over 20 years. The government's certifying body had audited and granted approval to ship JAN, 883 compliant, and Source Military Drawing parts used in ground and space applications. The discipline required to manufacture high reliability components has been beneficial to the commercial product lines. Harris has now taken the next evolutionary step by transitioning into QML as defined in MIL-PRF-38535. These guidelines incorporate the best commercial practices for semiconductor manufacturing.

Designing for Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Wafer Fab	• Internal Audits		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Junction Depth	X	
	- Sheet Resistivities	X	
	- Defect Density	X	X
	- Critical Dimensions	X	X
	- Visual Inspection	X	X
	- Lot Acceptance	X	X
	• Process		
	- Film Thickness	X	X
	- Implant Dosages	X	
	- Capacitance Voltage Changes	X	X
	- Conformance to Specification	X	X
	• Equipment		
	- Repeatability	X	X
	- Profiles	X	X
	- Calibration		X
	- Preventive Maintenance	X	X
Assembly	• Internal Audits		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Documentation Check		X
	- Dice Inspection	X	X
	- Wire Bond Pull Strength/Controls	X	X
	- Ball Bond Shear/Controls		X
	- Die Shear Controls		X
	- Post-Bond/Pre-Seal Visual	X	X
	- Fine/Gross Leak	X	X
	- PIND Test	X	X
	- Lead Finish Visuals, Thickness	X	X
	- Solderability	X	X
	• Process		
	- Operator Quality Performance	X	X
	- Saw Controls	X	X
	- Die Attach Temperatures	X	X
	- Seal Parameters	X	X
	- Seal Temperature Profile	X	X
	- Sta-Bake Profile	X	X
	- Temp Cycle Chamber Temperature	X	X
	- ESD Protection	X	X
	- Plating Bath Controls	X	X
	- Mold Parameters	X	X

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (Continued)

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Test	• Internal Audits		X
	• Temperature/Humidity	X	X
	• ESD Controls	X	X
	• Temperature Test Calibration	X	X
	• Test System Calibration	X	X
	• Test Procedures		X
	• Control Unit Compliance	X	X
	• Lot Acceptance Conformance	X	X
	• Group A Lot Acceptance		X
Probe	• Internal Audits		X
	• Wafer Repeat Correlation	X	X
	• Visual Requirements	X	X
	• Documentation	X	X
	• Process Performance	X	X
Burn-In	• Internal Audits		X
	• Functionality Board Check	X	X
	• Oven Temperature Controls	X	X
	• Procedural Conformance		X
Brand	• Internal Audits		X
	• ESD Controls	X	X
	• Brand Permanency	X	X
	• Temperature/Humidity	X	X
	• Procedural Conformance		X
QCI Inspection	• Internal Audits		X
	• Group B Conformance		X
	• Group C and D Conformance		X

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).

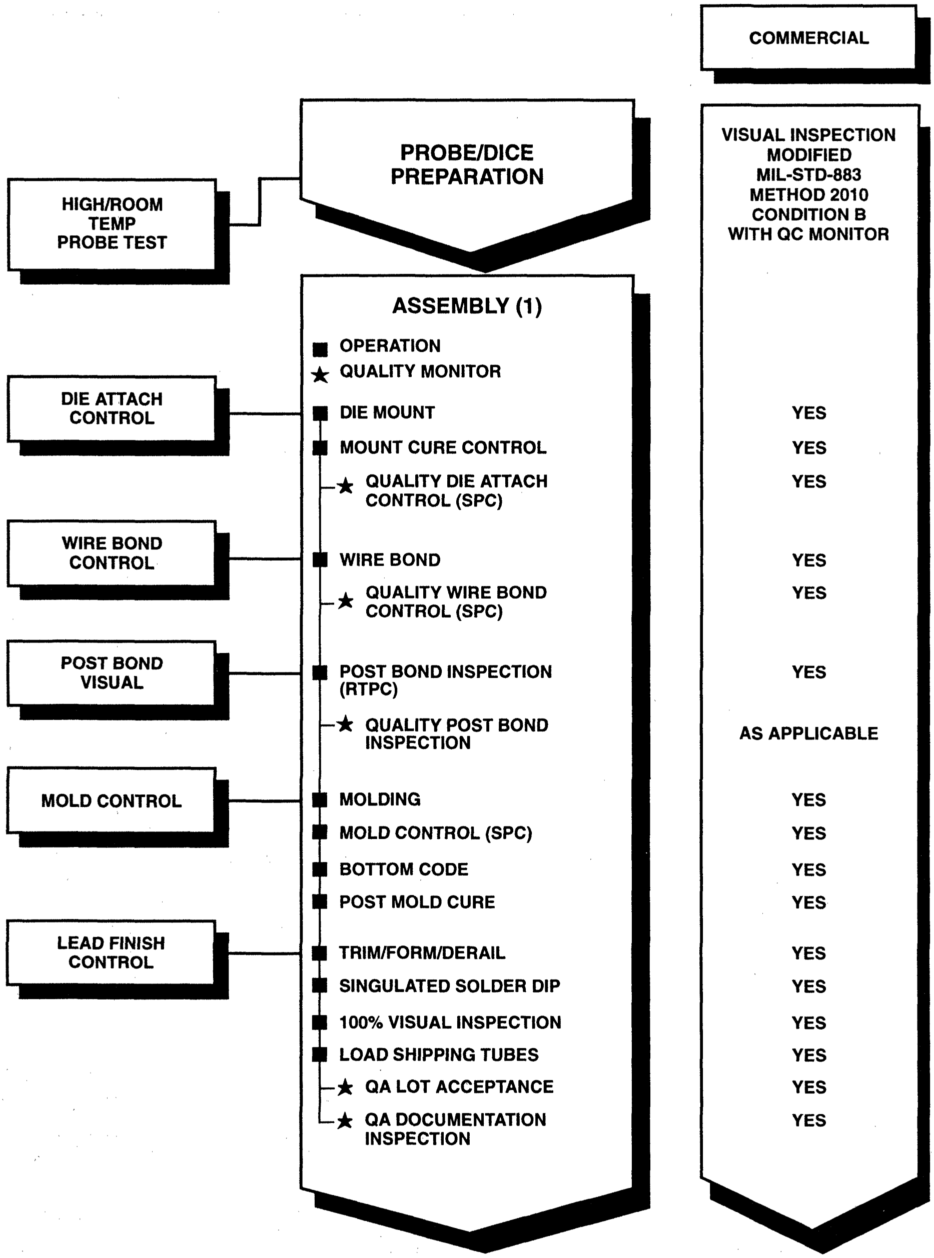
Special Testing

Harris Semiconductor offers several standard screen flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than +25°C. The flow shown in Figure 2 and Figure 3 indicates the Harris standard processing flow for a commercial linear part in a PDIP package. In addition, Harris can supply products tested to customer specifications both for electrical requirements and for nonstandard environmental stress screening. Consult your field sales representative for details.

TABLE 2. HARRIS I.C. DESIGN TOOLS

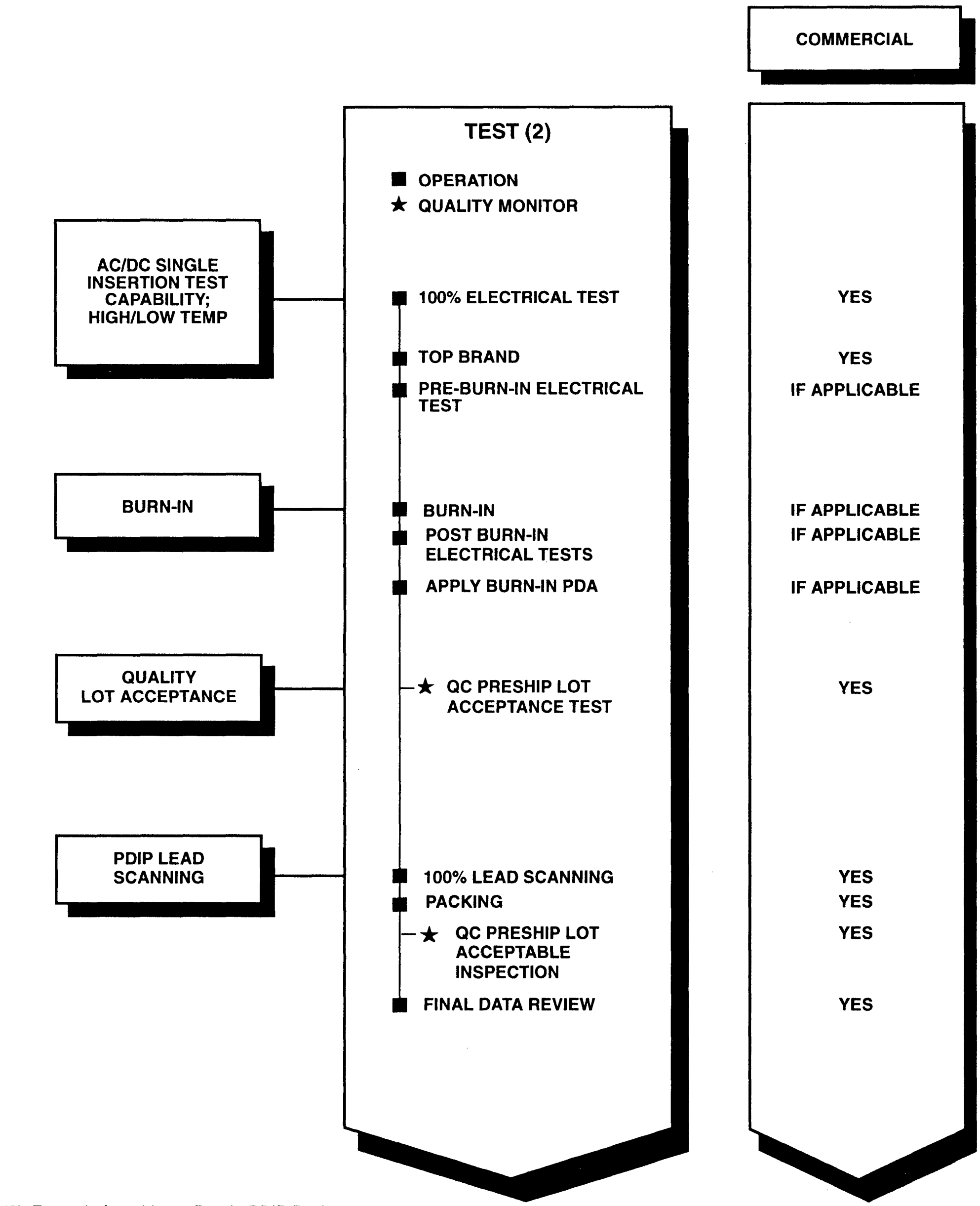
DESIGN STEP	PRODUCTS	
	ANALOG	DIGITAL
Functional Simulation	Cds Spice	Cds Spice Verilog
Parametric Simulation	Cds Spice Monte Carlo	Cds Spice
Schematic Capture	Cadence	Cadence
Functional Checking	Cadence	Cadence
Rules Checking	Cadence	Cadence
Parasitic Extraction	Cadence	Cadence

Harris Semiconductor Standard Processing Flow



(1) Example for a PDIP Package Part

FIGURE 2.



(2) Example for a Linear Part in PDIP Package

FIGURE 3.

TABLE 3. SUMMARIZING CONTROL APPLICATIONS

FAB			
• Diffusion - Junction Depth - Sheet Resistivities - Oxide Thickness - Implant Dose Calibration - Uniformity	• Thin Film - Film Thickness - Uniformity - Refractive Index - Film Composition - Particles Added	• Photo Resist - Critical Dimension - Resist Thickness - Etch Rates - Energy Monitor (E_O)	• Measurement Equipment - Critical Dimension - Film Thickness - Resistivity
ASSEMBLY			
• Pre-Seal - Die Prep Visuals - Yields - Die Attach Heater Block - Die Shear - Wire Pull - Ball Bond Shear - Saw Blade Wear - Pre-Cap Visuals	• Post-Seal - Internal Package Moisture - Tin Plate Thickness - PIND Defect Rate - Solder Thickness - Leak Tests - Module Rm. Solder Pot Temp. - Seal - Temperature Cycle	• Measurement - XRF - Radiation Counter - Thermocouples - GM-Force Measurement	
TEST			
	- Handlers/Test System - Defect Pareto Charts - Lot % Defective - ESD Failures per Month	- Monitor Failures - Lead Strengthening Quality - After Burn-In PDA	
OTHER			
• IQC - Vendor Performance - Material Criteria - Quality Levels	• Environment - Water Quality - Clean Room Control - Temperature - Humidity	• IQC Measurement/Analysis - XRF - ADE - 4 Point Probe - Chemical Analysis Equipment	

Controlling and Improving the Manufacturing Process - SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use control charts to determine the normal variabilities in processes, materials, and products. Critical process variables and performance characteristics are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicates a nonrandom pattern inside the limits. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

SPC is important, but still considered only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost (see Table 4).

TABLE 4. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

STAGE		APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at upgrading process performance by studying the key variables controlling the process, and optimizing the procedures or design to yield the best result. This approach is a more time-consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in ANSI/ASQC Z1.4, MIL-STD-883 and MIL-PRF-38535 are used by our quality inspectors.

The focus on this quality parameter has resulted in a continuous improvement to less than 100 PPM, and the goal is to continue improvement toward 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of Harris statisticians, private consultants, and internally developed programs, training of engineers, facilitators, and operators/technicians has been an ongoing activity in Harris Semiconductor.

Over the past years, Harris has also deployed a comprehensive training program for hourly operators and facilitators in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

Incoming Materials

Improving the quality and reducing the variability of critical incoming materials is essential to product quality enhancement, yield improvement, and cost control. With the use of statistical techniques, the influence of silicon, chemicals, gases and other materials on manufacturing is highly measurable. Current measurements indicate that results are best achieved when materials feeding a statistically controlled manufacturing line have also been produced by statistically controlled vendor processes.

To assure optimum quality of all incoming materials, Harris has initiated an aggressive program, linking key suppliers with our manufacturing lines. This user-supplier network is the Harris Vendor Certification process by which strategic vendors, who have performance histories of the highest quality, participate with Harris in a lined network; the vendor's factory acts as if it were a beginning of the Harris production line.

SPC seminars, development of open working relationships, understanding of Harris's manufacturing needs and vendor capabilities, and continual improvement programs are all part of

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	TOPICS COVERED
SPC, Basic	Manufacturing Operators, Non-Manufacturing Personnel	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts
SPC, Intermediate	Manufacturing Supervisors, Technicians	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Introduction to Capability
SPC, Advanced	Manufacturing Engineers, Manufacturing Managers	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Advanced Control Charts, Variance Component Analysis, Capability Analysis
Design of Experiments (DOX)	Engineers, Managers	Factorial and Fractional Designs, Blocking Designs, Nested Models, Analysis of Variance, Normal Probability Plots, Statistical Intervals, Variance Component Analysis, Multiple Comparison Procedures, Hypothesis Testing, Model Assumptions/Diagnostics
Regression	Engineers, Managers	Simple Linear Regression, Multiple Regression, Coefficient Interval Estimation, Diagnostic Tools, Variable Selection Techniques
Response Surface Methods (RSM)	Engineers, Managers	Steepest Ascent Methods, Second Order Models, Central Composite Designs, Contour Plots, Box-Behnken Designs
Capability Studies	Techs, Faciitators, Engineers	Capability Indices (C_P and C_{PK}), Variance Components, Nested Models, Fixed and Random Effects

the certification process. The sole use of engineering limits no longer is the only quantitative requirement of incoming materials. Specified requirements include centered means, statistical control limits, and the requirement that vendors deliver their products from their own statistically evaluated, in-control manufacturing processes.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts - Oxygen - Resistivity • Control Charts Related to - Enhanced Gettering - Total Thickness Variation - Total Indicated Reading - Particulates • Certificate of Analysis for all Critical Parameters • Control Charts from On-Line Processing • Certificate of Conformance
Chemicals/Photoresists/ Gases	• Chemicals - Assay - Major Contaminants • Molding Compounds - Spiral Flow - Thermal Characteristics • Gases - Impurities • Photoresists - Viscosity - Film Thickness - Solids - Pinholes	• Certificate of Analysis on all Critical Parameters • Certificate of Conformance • Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Water - Selected Parameters • Control Charts - Assay - Contaminants • Control Charts on - Photospeed - Thickness - UV Absorbance - Filterability - Water - Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Dimensional Characteristics • Certificate of Analysis for all Critical Parameters • Certificate of Conformance
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Certificate of Conformance • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

Calibration Laboratory

Another important resource in the product assurance system is a calibration lab in each Harris Semiconductor operation site. These labs are responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both production and engineering areas. The accuracy of instruments used at Harris is traceable to a national standards. Each lab maintains a system which conforms to the current revision of ANSI/NCSL Z540-1.

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Manufacturing Science - CAM, JIT, TPM

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened - in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

The major focus of JIT is cycle time reduction and linear production. Significant improvements in these areas result in large benefits to the customer. JIT is a part of the Total Quality Management philosophy at Harris and includes Employee Involvement, Total Quality Control, and the total elimination of waste.

Some key JIT methods used for improvement are sequence of events analysis for the elimination of non-value added activities, demand/pull to improve production flow, TQC check points and Employee Involvement Teams using root cause analysis for problem solving.

JIT implementations at Harris Semiconductor have resulted in significant improvements in cycle time and linearity. The benefits from these improvements are better on time delivery, improved yield, and a more cost effective operation.

JIT, SPC, and TPM are complementary methodologies and used in conjunction with each other create a very powerful force for manufacturing improvement.

Total Productive Maintenance (TPM)

TPM or Total Productive Maintenance is a specific methodology which utilizes a definite set of principles and tools focusing on the improvement of equipment utilization. It focuses on the total elimination of the six major losses which are equipment failures, setup and adjustment, idling and minor stoppages, reduced speed, process defects, and reduced yield. A key measure of progress within TPM is the overall equipment effectiveness which indicates what percentage of the time is a particular equipment producing good parts. The basic TPM principles focus on maximum equipment utilization, autonomous maintenance, cross functional team involvement, and zero defects. There are some key tools within the TPM technical set which have proven to be very powerful to solve long standing problems. They are initial clean, P-M analysis, condition based maintenance, and quality maintenance.

Utilization of TPM has shown significant increases in utilization on many tools across the Sector and is rapidly becoming widespread and recognized as a very valuable tool to improve manufacturing competitiveness.

The major benefits of TPM are capital avoidance, reduced costs, increased capability, and increased quality. It is also very compatible with SPC techniques since SPC is a good stepping stone to TPM implementation and it is in turn a good stepping stone to JIT because a high overall equipment effectiveness guarantees the equipment to be available and operational at the right time as demanded by JIT.

Harris Reliability

Introduction

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing processes. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life.

Reliability Engineering

The Reliability Engineering department is responsible for all aspects of reliability assurance at Harris Semiconductor:

- Charter
  - To ensure that Harris is recognized by our customers and competitors as a company that consistently delivers products with high reliability.
- Mission
  - To develop systems for assessing, enhancing, and assuring that quality and reliability are integrated into all aspects of our business.
- Vision
  - To establish excellence and integrity through all design and manufacturing processes as it relates to quality and reliability.

Values

- To be considered responsive and service oriented by our customers.
- To be acknowledged by Harris as a highly qualified resource for reliability assurance, product analysis, and electronic materials characterization.
- To successfully utilize the organization's talents through trained, empowered employees/employee team participation.
- To maintain an attitude of integrity, dignity and respect for all.

Strategy

- To provide quantitative assessments of product reliability focusing on the identification and timely elimination of design and processing deficiencies that degrade product performance and operating life expectancy.
- To provide systems for continuous improvement of reliability and quality through the assessment of existing processes, products, and packages.
- To perform product analysis as a means of problem solving and feedback to our customers, both internal and external.
- To exercise full authority over the internal qualifications of new products, processes, and packages.

The reliability organization is comprised of a team that possesses a broad cross section of expertise in these areas:

- Custom Military (Radiation Hardened)
- Automotive ASICs
- Harsh Environment Plastic Packaging
- Advanced Methods for Design for Reliability (DFR)
- Strength in Power Semiconductor
- Chemical/Surface Analysis Capabilities
- Failure Analysis Capabilities

The reliability focus is customer satisfaction (external and internal) and is accomplished through the development of standards, performance metrics, and service systems. These major systems are summarized below:

- A process and product development system known as ACT PTM (Applying Concurrent Teams to Product-To-Market) has been established. The ACT PTM philosophy is one of new product development through a team that pursues customer involvement. The team has the authority, responsibility, and training necessary to successfully bring the product to market. This not only includes product definition and design, but also all manufacturing capabilities as well.
- Standard test vehicles (over 100) have been developed for process characterization of wear-out failure mechanisms. These vehicles are used for conventional stresses (for modeling failure rates) and for wafer level reliability characterization during development.
- Common qualification standards have been established for all sites.
- A reliability monitoring system (also known as the Matrix monitoring system) is utilized for products in production to ensure ongoing reliability and verification of continuous improvement.
- The field return system is designed to handle a variety of customer issues in a timely manner. Product issues are often handled by routing the product into the PFAST (Product Failure Analysis Solution Team) system. Return authorizations (RAs) are issued where an entire lot of product needs to be returned to Harris. The Customer Return Services (CRS) group is responsible for the administration of this system (see Customer Return Services.)
- The PFAST system has been established to expedite failure analysis, failure root cause determination, and corrective actions for field returns. PFAST is a team effort involving many functional areas at all Harris sites. The purpose of this system is to enable Harris's Field Sales and Quality operations to properly route, track, and respond to our customer's needs as they relate to product analysis.

Design for Reliability (Wear-Out Characterization)

The concept of "Design for Reliability" focuses on moving reliability assessment away from tests on sample product to a point much earlier in the design cycle. Effort is directed at building in and verifying the reliability of a new process well before manufacture of the first shippable product that uses that technology. This gives these first new products a higher probability of success and achieves reduced product-to-market cycle times.

In practice, a set of standardized test vehicles containing special test structures are transferred to the new process using the layout ground rules specified for that process. Each test structure is designed for a specific wear-out failure mechanism. Highly accelerated stress tests are performed on these structures and the results can be extrapolated to customer use conditions. Generally, log-normal statistics are used to define wear-out distributions for the life prediction models. The results are used to establish reliability design ground rules and critical node lists for each process. These ground rules and critical nodes ensure that wear-out failures do not occur during the customer's projected use of the product.

Process/Product/Package Qualifications

Once the new process has successfully completed wear-out characterization, the final qualification consists of more conventional testing (e.g. biased life, storage life, temp cycle etc.). These tests are performed on the first new product designs (sampled across multiple wafer production lots). Successful completion of the final qualification tests concurrently qualifies the new process and the new products that were used in the qualification. Subsequent products designed within the now-established ground rules are qualified individually prior to introduction. New package configurations are also qualified individually prior to being available for use with new products.

Harris's qualification procedures are specified via controlled documentation and the same standard is used at Harris's sites worldwide. Figure 4 gives more information on the new process/product development and life cycle.

Product/Package Reliability Monitors

Many of the accelerated stress-tests used during initial reliability qualification are also employed during the routine monitoring of standard product. Harris's continuing reliability monitoring program consists of three groups of stress tests, labeled Matrix I, II and III. Table 6 outlines the Matrix tests used to monitor plastic packaged ICs in Harris's off-shore assembly plants, where each wafer fab technology is sampled. Matrix I consists of highly accelerated, short duration (typically 48 hours) tests, sampled biweekly, which provide real-time feedback on product reliability. Matrix II consists of the more conventional, longer term stress-tests, sampled monthly, which are similar to those used for product qualification. Finally, Matrix III, performed monthly on each package style, monitors the mechanical reliability aspects of the package. Any failures occurring on the Matrix monitors are fully analyzed and the failure mechanisms identified, with containment and corrective actions obtained from Manufacturing and Engineering. This information along with all of the test results are routinely transmitted to a central data base in Reliability Engineering, where failure rate trends are analyzed and tracked on an ongoing basis. These data are used to drive product improvements, to ensure that failure rates are continuously being reduced over time.

Reliability data, including the Matrix Monitor results, can be obtained by contacting your local Harris sales office.

TABLE 7. PLASTIC PACKAGED IC MONITORING TESTS

MATRIX I

TEST	CONDITIONS	DURATION	SAMPLE/ LTPD
Autoclave	+121°C, 100%RH, 15PSIG	96 Hours	45/5
Biased Life	+175°C	48 Hours	45/5
Biased Life	+125°C	48 Hours	45/5
HAST	+135°C, 85% RH	48 Hours	45/5
Thermal Shock	-65°C to +150°C	200 Cycles	45/5

MATRIX II

TEST	CONDITIONS	DURATION	SAMPLE/ LTPD
Autoclave	+121°C, 100%RH, 15PSIG	192 Hours	45/5
Biased Humidity	+85°C, 85% RH	1000 Hours	45/5
Biased Life	+125°C	1000 Hours	45/5
Dynamic Life	+125°C	1000 Hours	45/5
Storage Life	+150°C	1000 Hours	45/5
Temp. Cycle	-65°C to +150°C	1000 Cycles	45/5

MATRIX III

TEST	CONDITIONS	SAMPLE/LTPD
Brand Adhesion	MIL-STD-883/2015	15/15
Flammability	(UL-94 Vertical Burn)	11/20
Lead Fatigue	MIL-STD-883/2004	15/15
Physical Dimensions	MIL-STD-883/2016	11/20
Solderability	MIL-STD-883/2003	45/15

FLOW - PROCESS/PRODUCT DEVELOPMENT	RELIABILITY FOCUS
PRODUCT DEFINITION REVIEW	• Assumes process development required * * *
CONCEPT REVIEW	• Evaluate reliability risks factors • Attain commitment for test vehicle development * * *
DESIGN REVIEW	• Review test vehicle development and stress test plan • Review package requirements and ESD requirements • Review latent random failure mechanism history and design for elimination • Review ground rules for design and elimination of wear-out mechanisms • Review process characterization, statistical control and capability and critical node list • Review device modeling and simulations • Review process variability and producibility • Define wafer level reliability vehicles * * *
LAYOUT REVIEW	• Evaluate design of chip to package risk factors • Review Design ground Rule Checks (DRCs) • Establish reliability test, stress and failure analysis capabilities • Project failure rate based on test vehicle data • Review burn-in diagrams for production and qualification • Review overall qualification plan * * *
TEST VEHICLE FABRICATION	• Test vehicles and/or product constructed • Conduct wear-out characterization and/or product stress testing * * *
EVALUATION REVIEW	• Review test vehicle stress results • Verify wear-out mechanisms are eliminated by design and Statistical Process Control (test vehicle + SPC) • Review product characterization to data sheet, ESD, latch-up and Destructive Physical Analysis (DPA) results and define corrective actions • Review of life test data and failure mechanisms. Define corrective actions • Utilize statistical Design Of Experiments (DOX) if required to adjust process or design • Define necessary changes to eliminate any systematic failure mechanism • If mature process - grant generic release * * *
NEW PRODUCT TRANSFER	• Qualification requirements complete and presented. Meet FIT rate requirements • Review infant mortality burn-in results • Initiate reliability monitor plan * * *
MANUFACTURE	• Reliability Monitors: - Matrix monitor assessment - Military quality conformance testing • Trend analysis of reliability performance used to develop product improvements • Yield management support * * *
SHIPMENT	• High quality and reliable products shipped to Harris customers * * *
CONTINUOUS IMPROVEMENT	• Failure Analysis - Determine assignable cause of failure • Closed loop corrective action process • Continuous improvement objectives in product reliability and quality

FIGURE 4. NEW PROCESS/PRODUCT DEVELOPMENT AND LIFE CYCLE

Customer Return Services

Harris places a high priority on resolving customer return issues. The Customer Return Services (CRS) department is responsible for determining the best manner to handle a return issue as illustrated in Figure 5.

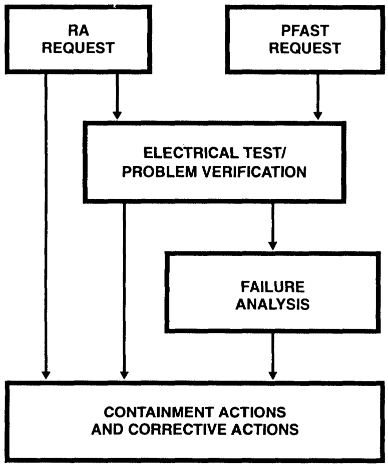


FIGURE 5. GENERAL RETURN FLOW

The diversity of return reasons requires that many different organizations be involved to test, analyze, and correct field return issues. The CRS group coordinates the responses from the supporting organizations to drive closure of issues within the customer response time requirements, see Table 7. The results from the work performed on customer returns are used to initiate corrective actions and continuous improvements within the factories. When the work on a return is completed, the customer is contacted to be certain all issues have been satisfactorily resolved.

The two methods used to return devices are by a RA (Return Authorization) request or by a PFAST (Product Failure Analysis Solution Team) request. The main difference between RA and PFAST is that the PFAST requests often require extensive analysis and a more formal response to the customer. All returns follow the same general procedure from the customer's perspective as seen in steps one to five of the customer return procedure.

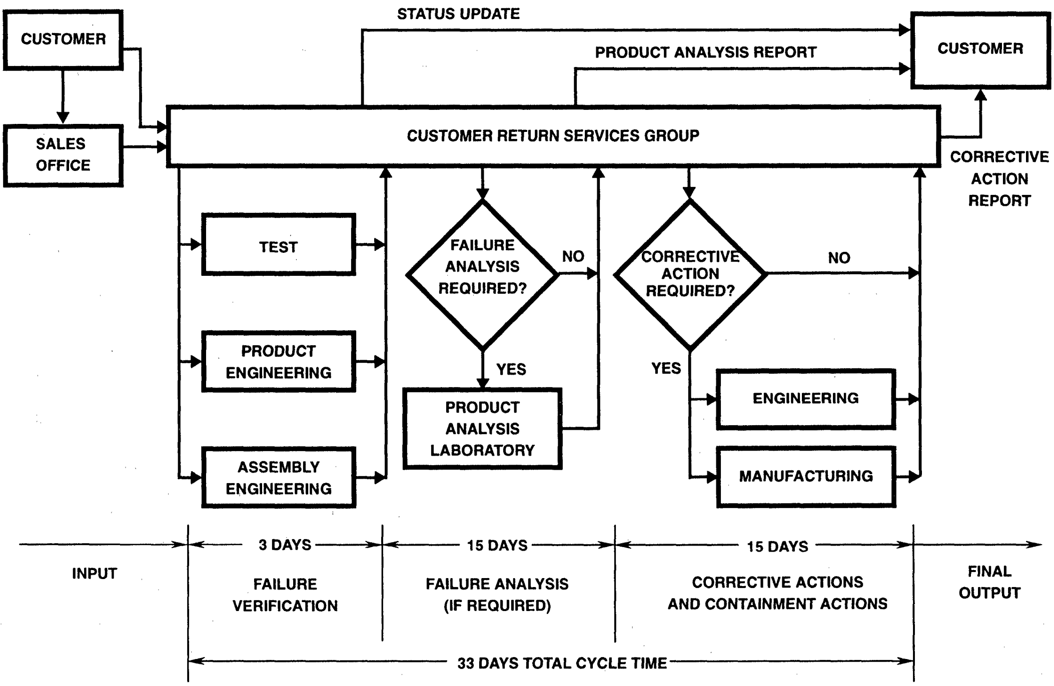
- **Step 1** - Customer or Sales office contacts the Customer Return Services department. If a return is to be routed into the PFAST system, then a PFAST Action Request (see the PFAST form in this section) needs to be completed to understand the customer's issue and direct the analysis efforts.
  - **Phone Number: (407)-724-7400**
  - **FAX Number: (407)-724-7658**
  - **Internet: creturn@huey.mis.semi.harris.com**
  - **PROFS: CRETURN**
- **Step 2** - The Customer Return Services department notifies all affected sales, factory, and engineering organizations of the issue.
- **Step 3** - When product is received, the issue is verified and any required analysis is performed. Where applicable, a preliminary analysis report is sent to the customer.
- **Step 4** - A determination of the root cause of failure initiates the corrective actions to address the source of the problem. A final corrective action report is sent to the customer if requested.
- **Step 5** - The Customer Return Services department contacts the customer to confirm that all issues have been handled properly and the customer is satisfied that the return is completed.

The RA request is used to return and replace an entire lot of product. The lot is returned to Harris for replacement or credit. Once the product is received various tests and evaluations will be performed to determine the appropriate actions that should be taken to resolve any problems or issues.

A PFAST request is used to return a small sample for analysis of a problem. The ultimate outcome of both types of requests is to determine corrective actions that would preclude the same problem occurring in the future. Where appropriate, a containment plan is also implemented to prevent a reoccurrence of the problem in the field. The customer return flow diagram (Figure 6) provides the typical activities and cycle times for processing a PFAST request.

TABLE 8. CUSTOMER RETURN SERVICES

CHARTER	MISSION	RESPONSIBILITIES
To resolve product quality issues while providing feedback to both external and internal customers to facilitate corrective actions and continuous improvement of the product.	To provide a single point interface between the customer and the factory for resolving technical problems, issues, and field returns.	1. Maintain customer return history. 2. Track returns through the factory. 3. Establish a history library of problems and corrective actions. 4. Ensure closure with customers.



NOTE: The days indicated are the typical number of 'working days' not calendar days. Analysis difficulty and the nature of the corrective actions may either improve or degrade the total cycle time.

FIGURE 6. CUSTOMER RETURN FLOW DIAGRAM

HARRIS SEMICONDUCTOR

PFAST ACTION REQUEST

(Product Failure Analysis Solution Team)

Request # ___________

Date: ___________

Originator ___________	Customer ___________
Company/Phone No. ___________	Location ___________
Device Type/Part No. ___________	Customer's Reference No. ___________
No. Samples Returned ___________	Quantity Received ___________

Instructions and requirements are on the back of this form.

Has Field Applications been contacted for assistance? ☐ No ☐ Yes - Who was contacted ___________

SOURCE OF PROBLEM

(Enter the sequence of events in the boxes provided)

1. Visual/Mechanical
   ☐ Describe ___________
2. Incoming Test ☐ Not Performed
   ☐ 100% Tested ☐ Sample Tested
   No. Tested _______ No. of Rejects _______
   Are results representative of previous lots?
   ☐ YES ☐ NO
3. In Process/Manufacturing Failure
   ☐ Board Test ☐ System Test
   How many units failed? ________
   Failed after ________hours of testing
   Was unit retested at incoming inspection?
   ☐ YES ☐ NO
   Are results representative of previous lots?
   ☐ YES ☐ NO
4. Field Failure
   Failed after ________hours operation
   Estimated failure rate________ % per _______
   End User______________ Location ___________
   Min. _____°C Ave. ______°C Max. _______°C
5. Other

ACTION REQUESTED BY CUSTOMER

Specific Action Requested (Contact PFAST Coordinator for other options)

☐ Test Sample for Correlation Only
☐ Test Sample for Product Return >$5k
☐ Failure Analysis
☐ Other

Impact of Failed Units on Customer's Situation: ___________

Customer Contact with Specific Knowledge of Rejects

Name ___________

Position ___________ Phone___________

REASON FOR ELECTRICAL REJECT

(Where appropriate serialize units and specify for each)

Test Conditions Relating to Failure

Tester Used (Mfgr/Model) ___________

Test Temperature ___________

Test Time ☐ Continuous (T = ______sec)
☐ One Shot (T = _______sec)

Describe any observed condition to which failure appears sensitive ___________

1. ☐ DC Failure
   ☐ Open ☐ Short ☐ Leakage
   ☐ Power Drain ☐ Input Level ☐ Output Level
   Pin Number___________
2. ☐ AC Failure
   Power Supply Voltages = ______V
   Input Voltages V_{IH} = _______V V_{IL} = _______V
   Pin Number________
   Failing characteristics ___________
3. ☐ RAM and ROM Failures (ROM failures must be returned with a good master unit if failure analysis is requested).
   Address of Failing Location ___________

   Describe Pattern Used (If not standard patterns, give very complete description including address sequence). ___________

Include timing diagrams and circuit schematic if available.

ROM Programmer Used (If purchased unprogrammed) ___________

Conformal Coating (Mfgr/Model) ___________

Additional Comments:

FIGURE 7. PFAST ACTION REQUEST

INSTRUCTIONS FOR COMPLETING PFAST ACTION REQUEST FORM

The purpose of this form is to help us provide you with a more accurate, complete, and timely response to failures which may occur. Accurate and complete information is essential to ensure that the appropriate corrective action can be implemented. Due to this need for accurate and complete information, requests without a completed PFAST Action Request form will be returned.

Source of Problem:

This section requests the product flow leading to the failure. Mark an 'X' in the appropriate boxes up to and including the step which detected the failure. Also mark an 'X' in the appropriate box under "ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?" to indicate whether this is a rare failure or a repeated problem.

Example 1. No incoming electrical test was performed; the units were installed onto boards; the boards functioned correctly for two hours and then 1 unit failed. The customer rarely has a failure due to the Harris device.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE ____________
2. INCOMING TEST ☒ NOT PERFORMED
   ☐ 100% TESTED ☐ SAMPLE TESTED
   NO. TESTED ______ NO. OF REJECTS ______
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ☒ BOARD TEST ☐ SYSTEM TEST
   HOW MANY UNITS FAILED? __1__
   FAILED AFTER __2__ HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ☒ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☒ NO
4. FIELD FAILURE
   FAILED AFTER ______ HOURS OPERATION
   ESTIMATED FAILURE RATE ______% PER ______
   END USER ______ LOCATION ______
   MIN. ____°C AVE. ____°C MAX. ____°C
5. OTHER ____________

Example 2. 100 out of the 500 units shipped were tested at incoming and all passed. The units were installed into boards and the boards passed. The boards were installed into the system and the system failed immediately when turned on. There were 3 system failures due to this part. The customer frequently has failures of this Harris device. The 3 units were not retested at incoming.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE ____________
2. INCOMING TEST ☐ NOT PERFORMED
   ☐ 100% TESTED ☒ SAMPLE TESTED
   NO. TESTED __100__ NO. OF REJECTS __0__
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☒ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ☒ BOARD TEST ☒ SYSTEM TEST
   HOW MANY UNITS FAILED? __3__
   FAILED AFTER __0__ HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ☒ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☒ YES ☐ NO
4. FIELD FAILURE
   FAILED AFTER ______ HOURS OPERATION
   ESTIMATED FAILURE RATE ______% PER ______
   END USER ______ LOCATION ______
   MIN. ____°C AVE. ____°C MAX. ____°C
5. OTHER ____________

Action Requested by Customer:

This section should be completed with the customer's expectations. This information is essential for an appropriate response.

Reason for Electrical Reject:

This section should be completed if the type of failure could be identified. If this information is contained in attached customer correspondence there is no need to transpose onto the PFAST Action Request form.

PFAST REQUIREMENTS

The value of returning failing products is in the corrective actions that are generated. Failure to meet the following requirements can cause erroneous conclusion and corrective action; therefore, failure to meet these requirements will result in the request being returned. Contact the local PFAST Coordinator if you have any questions.

Units with conformal coating should include the coating manufacturer and model. This is requested since the coating must be removed in order to perform electrical and hermeticity testing.

1. Units must be returned with proper ESD protection (ESD-safe shipping tubes within shielding box/bag or inserted into conductive foam within shielding box/bag). No tape, paper bags, or plastic bags should be used. This requirement ensures that the devices are not damaged during shipment back to Harris.
2. Units must be intact (lid not removed and at least part of each package lead present). This is a requirement since the parts must be intact in order to perform electrical test. Also, opening the package can remove evidence of the cause of failure and lead to an incorrect conclusion.
3. Programmable parts (ROMs, PROMs, UVEPROMs, and EEPROMs) must include a master unit with the same pattern. This requirement is to provide the pattern so all failing locations can be identified. A master unit is required if a failure analysis is requested.

FIGURE 7. PFAST ACTION REQUEST (Continued)

Product Analysis Lab

The Product Analysis Laboratory capabilities and charter encompass the isolation and identification of failure modes and mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. The primary activities of the Product Analysis Lab are electrical verification/characterization of the failure, package inspection/analysis, die inspection/analysis, and circuit isolation/probing. A variety of tools and techniques have been developed to ensure the accuracy and integrity of the product analysis. This section lists some of the tools and techniques that are employed during a typical analysis.

The electrical verification/characterization of devices failing electrical parameters is essential prior to performing an analysis. The information obtained from the electrical verification provides a direction for the analysis efforts. The following electrical verification/characterization equipment may be used to obtain electrical data on a device:

- LV500 ASIC verification system
- LTS2020 Analog tester
- Curve Tracer
- Parametric Analyzer

Prior to die level analysis, package inspection and analysis are performed. These steps are performed routinely since valuable data may not be obtainable once the package is opened. The package inspection and analysis may require the use of some of the following lab equipment:

- X-ray
- C-mode Scanning Acoustic Microscope (C-SAM)
- Optical inspection microscopes
- Package opening tools and techniques

Once the device has been opened, die inspection and analysis can be performed. Depending on the type of failure, several tools and techniques may be used to identify the failure mechanism. Usually the faster and easier to use operations are performed first in an attempt to expedite the analysis. The list of equipment and techniques for performing die inspection and analysis is as follows:

- Optical microscopes
- Liquid crystal
- Emission microscope
- Scanning electron microscopes - SEM

The final step of circuit isolation is ready to be performed when an area of the circuit has been identified as the source of the problem through one of the previous analysis efforts. Circuit analysis is performed using the following probing and isolation tools:

- Mechanical probing
- Laser cutter and isolation
- E-beam probing
- Cross sectioning and chemical deprocessing

A typical analysis flow is shown in the Figure 8 below. The exact analysis steps and sequence are determined as the situation dictates. For the analysis to be conclusive, it is essential that the failure mechanism correlates to the initial product failure conditions. Some failure mechanisms require elemental and chemical analysis to identify the root cause within the manufacturing process. Elemental and chemical analysis tasks are sent to the Analytical Services Lab for further evaluation.

The results of each analysis are entered into a computer data base. This data base is used to search for specific types of problems, to identify trends, and to verify that the corrective actions were effective.

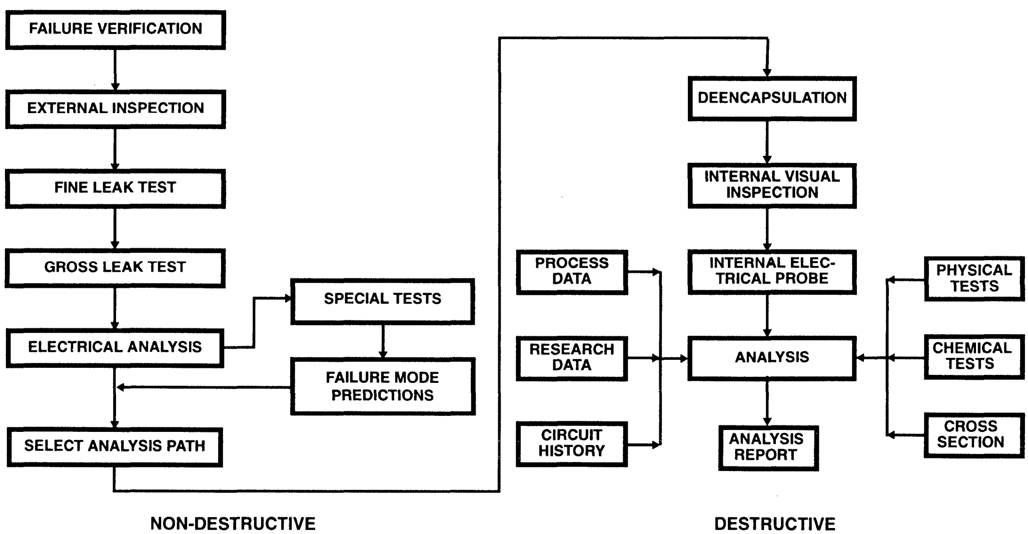


FIGURE 8. ANALYSIS SEQUENCE

13

QUALITY AND RELIABILITY

Analytical Services Laboratory

Chemical and physical analysis of materials and processes is an integral part of Harris' Total Quality/Continuous Improvement efforts to build reliability into processes and products. Manufacturing operations are supported with real-time analyses to help maintain robust processes. Analyses are run in cooperation with raw material suppliers to help them provide controlled materials in dock-to-stock procurement programs.

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies.

The department also maintains ongoing working arrangements with commercial laboratories, universities, and equipment manufacturers to obtain any materials analysis in cases where instrumental capabilities are not available in our own facility.

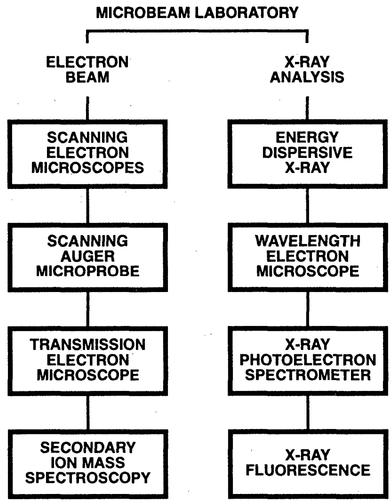


FIGURE 9. MICROBEAM LABORATORY

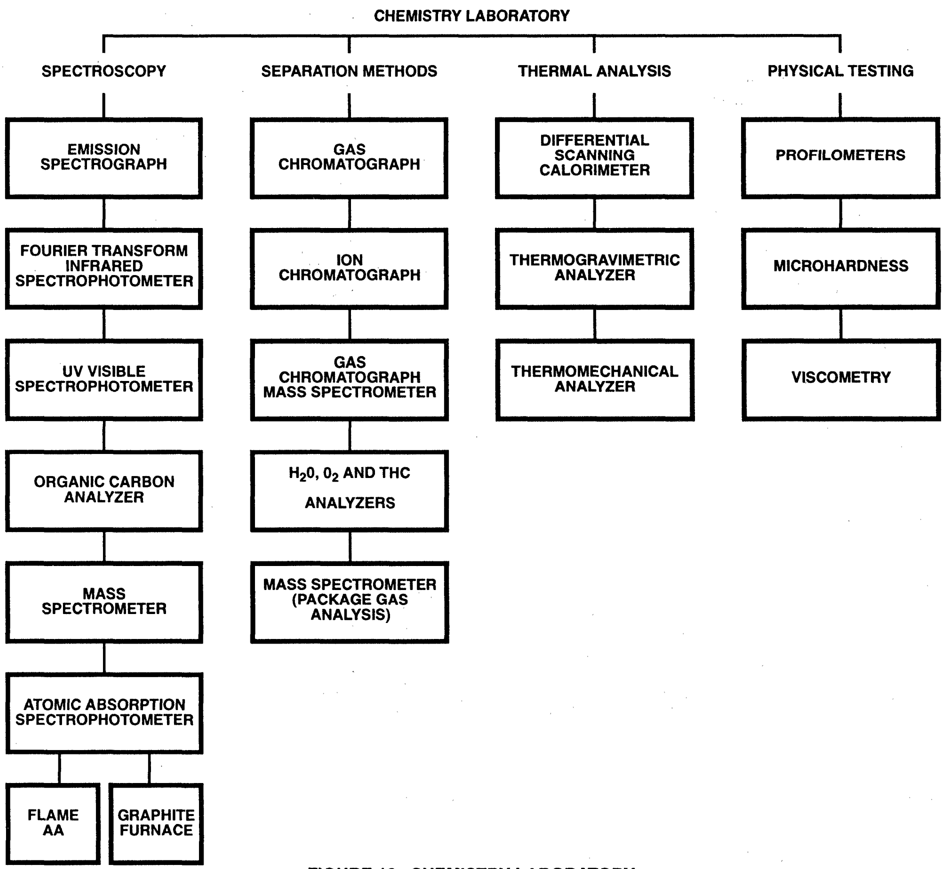


FIGURE 10. CHEMISTRY LABORATORY

Reliability Fundamentals and Calculation of Failure Rate

Table 9 defines some of the more important terminology used in describing the lifetime of integrated circuits. Of prime importance is the concept of "failure rate" and its calculation.

Failure Rate Calculations

Since reliability data can be accumulated from a number of different life tests with several different failure mechanisms, a comprehensive failure rate is desired. The failure rate calculation can be complicated if there are more than one failure mechanism in a life test, since the failure mechanisms are thermally activated at different rates The equation below accounts for these considerations along with a statistical factor to obtain the upper confidence level (UCL) for the resulting failure rate.

$$\lambda = \left[\sum_{i=1}^{\beta} \frac{x_i}{\sum_{j=1}^{k} TDH_j\, AF_{ij}} \right] \times \frac{M \times 10^9}{\sum_{i=1}^{\beta} x_i}$$

where,

λ = failure rate in FITs (Number fails in 10^9 device hours)

β = number of distinct possible failure mechanisms

k = number of life tests being combined

x_i = number of failures for a given failure mechanism $i = 1, 2, \ldots \beta$

TDH_j = Total device hours of test time (unaccelerated) for Life Test j, $j = 1, 2, 3, \ldots k$

AF_{ij} = Acceleration factor for appropriate failure mechanism $i = 1, 2, \ldots k$

$M = X^2_{(\alpha,\, 2r+2)}/2$

where,

X^2 = chi square factor for 2r + 2 degrees of freedom

r = total number of failures ($\Sigma\, x_i$)

α = risk associated with UCL;

i.e. α = (100-UCL(%))/100

In the failure rate calculation, Acceleration Factors (AF_{ij}) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. Although no standard exists, a temperature of +55°C has been popular. Harris Semiconductor Reliability Reports will derate to +55°C and will express failure rates at 60% UCL. Other derating temperatures and UCLs are available upon request.

TABLE 9. FAILURE RATE PRIMER

TERMS	DEFINITIONS/DESCRIPTION
Failure Rate λ	Measure of failure per unit of time. The early life failure rate is typically higher, decreases slightly, and then becomes relatively constant over time. The onset of wear-out will show an increasing failure rate, which should occur well beyond useful life. The useful life failure rate is based on the exponential life distribution.
FIT (Failure In Time)	Measure of failure rate in 10^9 device hours; e.g., 1 FIT = 1 failure in 10^9 device hours, 100 FITS = 100 failure in 10^9 device hours, etc.
Device Hours	The summation of the number of units in operation multiplied by the time of operation.
MTTF (Mean Time To Failure)	Mean of the life distribution for the population of devices under operation or expected lifetime of an individual, MTTF = $1/\lambda$, which is the time where 63.2% of the population has failed. Example: For λ = 10 FITS (or 10 E-9/Hr.), MTTF = $1/\lambda$ = 100 million hours.
Confidence Level (or Limit)	Probability level at which population failure rate estimates are derived from sample life test: 10 FITs at 95% UCL means that the population failure rate is estimated to be no more that 10 FITs with 95% certainty. The upper limit of the confidence interval is used.
Acceleration Factor (AF)	A constant derived from experimental data which relates the times to failure at two different stresses. The AF allows extrapolation of failure rates from accelerated test conditions to use conditions.

Acceleration Factors

Acceleration factor is determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and has been found to be an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP\left[\frac{E_a}{k}\left(\frac{1}{T_{USE}} - \frac{1}{T_{STRESS}}\right)\right]$$

where,

AF = Acceleration Factor

E_a = Thermal Activation Energy (See Table 10)

k = Boltzmann's Constant (8.63 x 10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature.

Activation Energy

The Activation Energy (E_a) of a failure mechanism is determined by performing at least two tests at different levels of stress (temperature and/or voltage). The stresses will provide the time to failure (t_f) for the two (or more) populations thus allowing the simultaneous solution for the activation energy as follows:

$$\ln(t_{f1}) = C + \frac{E_a}{kT_1} \qquad \ln(t_{f2}) = C + \frac{E_a}{kT_2}$$

By subtracting the two equations and solving for the activation energy, the following equation is obtained:

$$E_a = \frac{k[\ln(t_{f1}) - \ln(t_{f2})]}{(1/T1 - 1/T2)}$$

where,

E_a = Thermal Activation Energy (See Table 10)

k = Boltzmann's Constant (8.63 x 10^{-5} eV/°K)

T_1, T_2 = Life test temperatures in degrees Kelvin

TABLE 10. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3eV - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3eV - 0.5eV	HTOL and voltage stress screens.	Vendor statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress testing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5eV - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistical Process Control of assembly processes, proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation.
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles, Statistical Process Control of photoresist/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test and HTOL.	Statistical Process Control of C-V data, oxide/ interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL and oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

SIGNAL PROCESSING NEW RELEASES 14

PACKAGING INFORMATION

PAGE

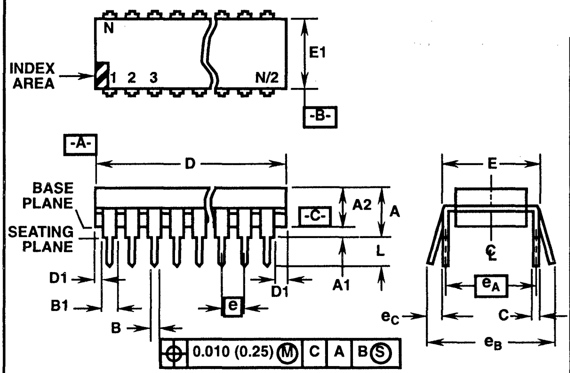
New Releases Package Selection Guide

PART NUMBER	PDIP	SOIC	SSOP	PLCC	MQFP	CERDIP	CPGA	SIDEBRAZE
DG401	E16.3	M16.15				F16.3		
DG403	E16.3	M16.15				F16.3		
DG405	E16.3	M16.15				F16.3		
HA4201	E8.3	M8.15						
HA4314	E14.3	M14.15						
HA4344	E16.3	M16.15						
HA4404	E16.3	M16.15						
HA4600	E8.3	M8.15						
HA5013	E14.3	M14.15						
HA5020	E8.3	M8.15				F8.3A		
HA5022	E16.3	M16.15				F16.3		
HA5023	E8.3	M8.15				F8.3A		
HA5024	E20.3	M20.3						
HA5025	E14.3	M14.15						
HA5351	E8.3	M8.15						
HA5352	E14.3	M16.3						
HA7211		M8.15						
HC5513	E22.4			N28.45				
HFA1102	E8.3	M8.15						
HFA1103	E8.3	M8.15						
HFA1105	E8.3	M8.15				F8.3A		
HFA1106	E8.3	M8.15				F8.3A		
HFA1109	E8.3	M8.15						
HFA1112	E8.3	M8.15				F8.3A		
HFA1113	E8.3	M8.15				F8.3A		
HFA1114	E8.3	M8.15						
HFA1115	E8.3	M8.15				F8.3A		
HFA1118	E8.3	M8.15						
HFA1119	E8.3	M8.15						
HFA1135	E8.3	M8.15				F8.3A		
HFA1145	E8.3	M8.15				F8.3A		
HFA1149	E8.3	M8.15						
HFA1205	E8.3	M8.15						
HFA1212	E8.3	M8.15				F8.3A		
HFA1245	E14.3	M14.15				F14.3		

New Releases Package Selection Guide (Continued)

PART NUMBER	PDIP	SOIC	SSOP	PLCC	MQFP	CERDIP	CPGA	SIDEBRAZE
HFA1405		M14.15						
HFA1412	E14.3	M14.15				F14.3		
HFA3046		M14.15						
HFA3096		M16.15						
HFA3101		M8.15						
HFA3102		M14.15						
HFA3127		M16.15						
HFA3128		M16.15						
HFA3600		M14.15						
HFA5253		M20.3A						
HI1179					Q32.7x7-S			
HI3050					Q64.14x20-S			
HI5702		M28.3						
HI5703		M28.3						
HI5710					Q48.7x7-S			
HI5714		M24.3						
HI5721	E28.6	M28.3						
HI5780					Q32.7x7-S			
HI5800								D40.6
HI5805		M28.3						
HI7188	E40.6				Q44.10x10			
HI7190	E20.3	M20.3				F20.3		
HIN200		M20.3						
HIN201		M16.3						
HIN202	E16.3	M16.3						
HIN204		M16.3						
HIN206	E24.3	M24.3	M24.209					
HIN207	E24.3	M24.3	M24.209					
HIN208	E24.3	M24.3	M24.209					
HIN209	E24.3	M24.3						
HIN211		M28.3	M28.209					
HIN213		M28.3	M28.209					
HSP43124	E28.6	M28.3						
HSP43168				N84.1.15	Q100.14x20		G84.A	
HMP8100					Q100.14x20			

Dual-In-Line Plastic Packages (PDIP)



NOTES:

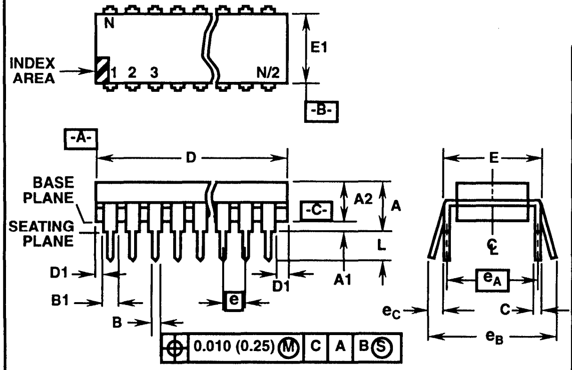
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{\text{-C-}}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (PDIP)



NOTES:

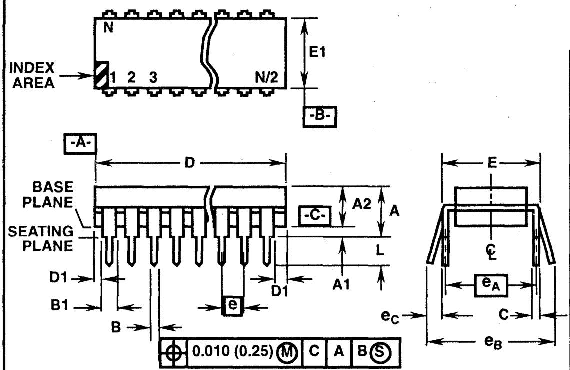
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{-C-}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (PDIP)



E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

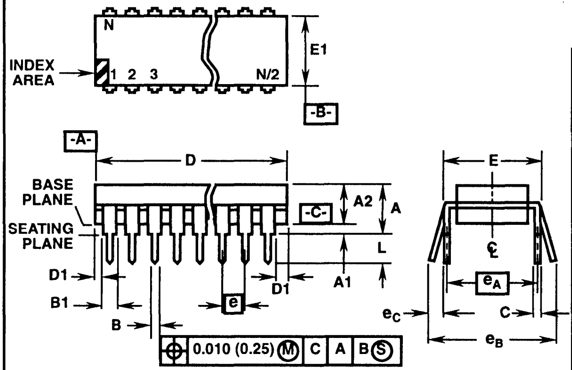
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{-C-}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

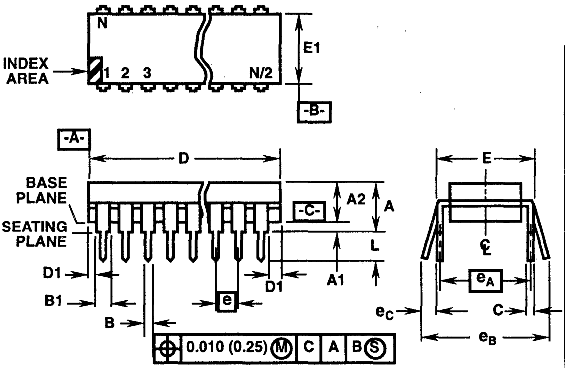
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{-C-}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



E22.4 (JEDEC MS-010-AA ISSUE C)
22 LEAD DUAL-IN-LINE PLASTIC PACKAGE

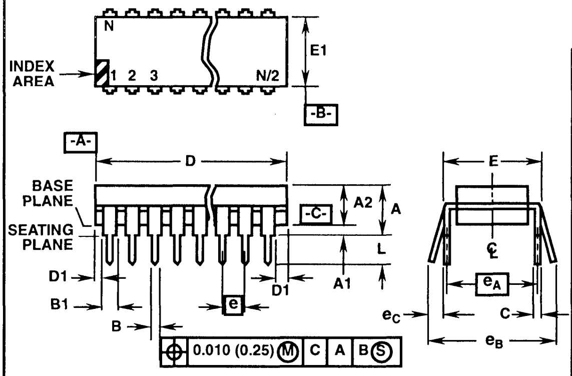
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.065	1.15	1.65	8
C	0.009	0.015	0.229	0.381	-
D	1.065	1.120	27.06	28.44	5
D1	0.005	-	0.13	-	5
E	0.390	0.425	9.91	10.79	6
E1	0.330	0.390	8.39	9.90	5
e	0.100 BSC		2.54 BSC		-
e_A	0.400 BSC		10.16 BSC		6
e_B	-	0.500	-	12.70	7
L	0.115	0.160	2.93	4.06	4
N	22		22		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{-C-}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (PDIP)



NOTES:

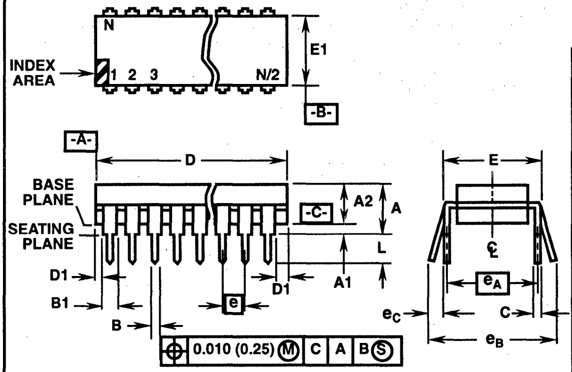
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{-C-}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E24.3 (JEDEC MS-001-AF ISSUE D)
24 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	1.230	1.280	31.24	32.51	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	24		24		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (PDIP)



NOTES:

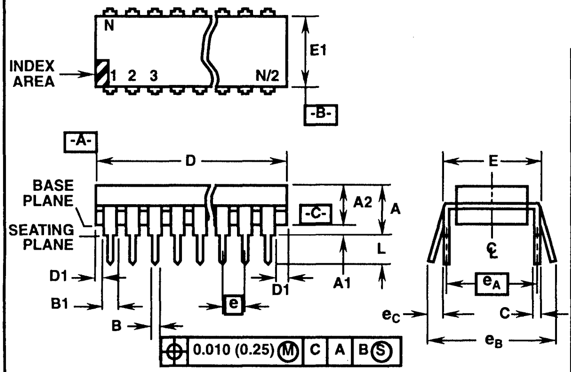
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{-C-}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (PDIP)



E40.6 (JEDEC MS-011-AC ISSUE B)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

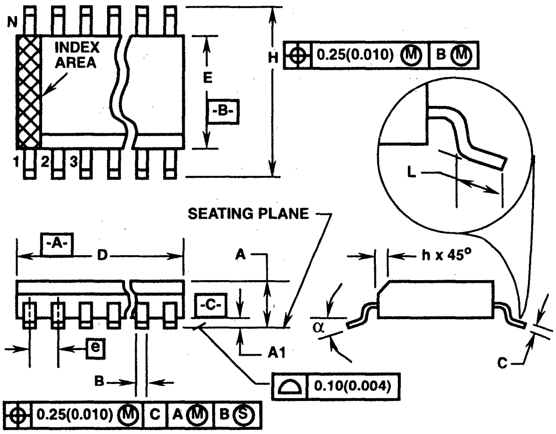
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{-C-}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Small Outline Plastic Packages (SOIC)



M8.15 (JEDEC MS-012-AA ISSUE C)

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

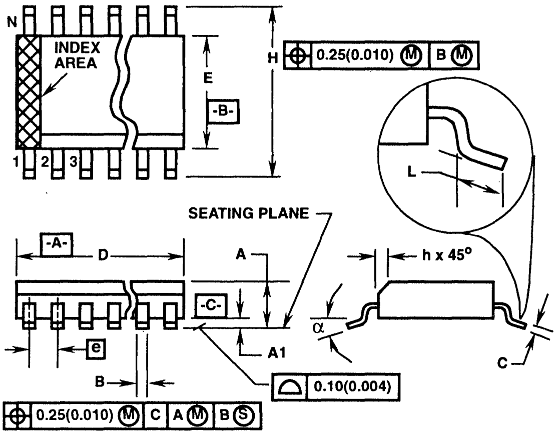
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



NOTES:

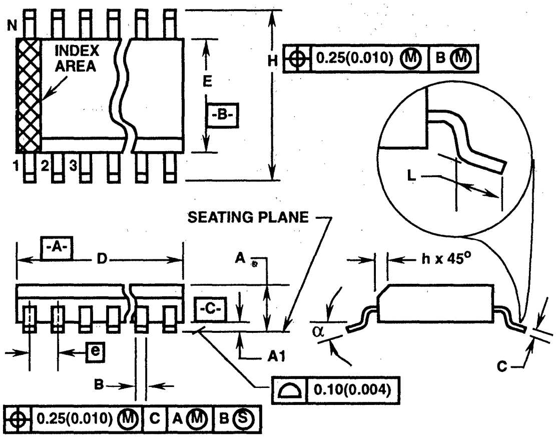
1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



NOTES:

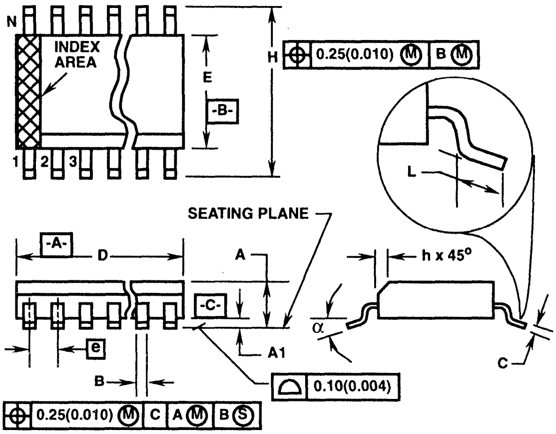
1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

Small Outline Plastic Packages (SOIC)



M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

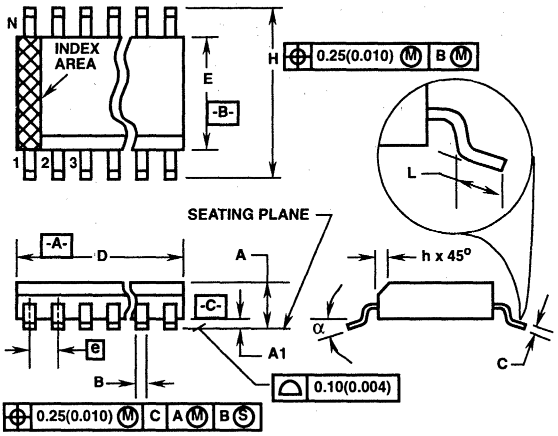
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

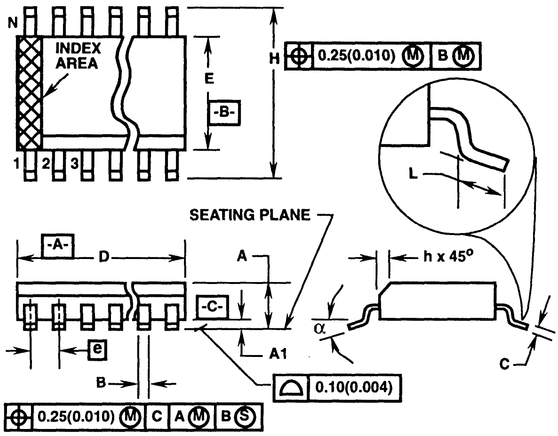
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

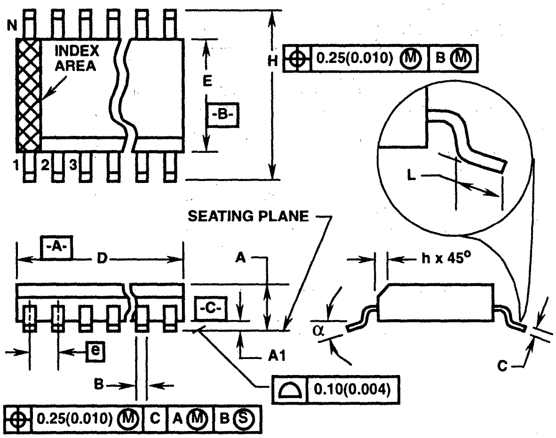
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

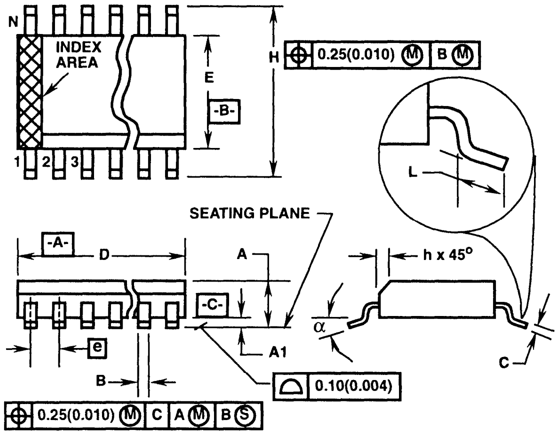
M28.3 (JEDEC MS-013-AE ISSUE C)

28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

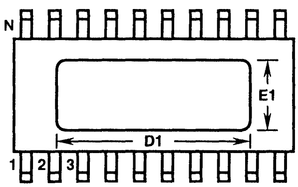
	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

Power Small Outline Plastic Packages (PSOP)



TOP VIEW



POWER SOP PACKAGE
(HEAT SLUG SURFACE IS ELECTRICALLY FLOATING)

M20.3A

20 LEAD POWER SMALL OUTLINE PLASTIC PACKAGE

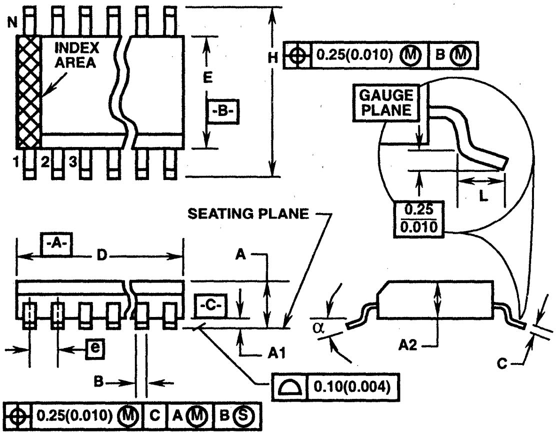
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
D1	0.325	0.340	8.25	8.63	10
E	0.2914	0.2992	7.40	7.60	4
E1	0.175	0.190	4.44	4.82	10
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 0 6/95

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Exposed copper heat slug flush with top surface of package. All other dimensions conform to JEDEC MS-013AC Issue C.
11. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)



NOTES:

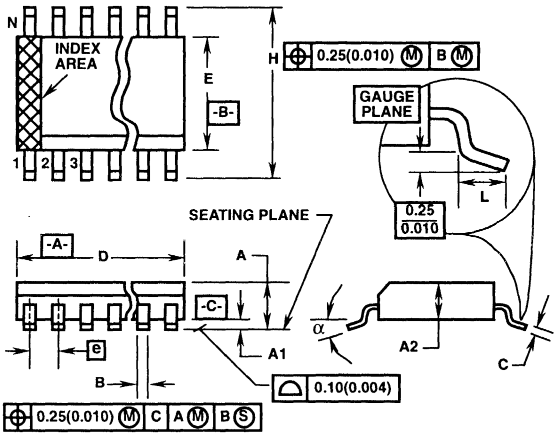
1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.209 (JEDEC MO-150-AG ISSUE B)
24 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.312	0.334	7.90	8.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

Rev. 1 3/95

Shrink Small Outline Plastic Packages (SSOP)



M28.209 **(JEDEC MO-150-AH ISSUE B)**

28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.078	-	2.00	-
A1	0.002	-	0.05	-	-
A2	0.065	0.072	1.65	1.85	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.009	0.09	0.25	-
D	0.390	0.413	9.90	10.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.022	0.037	0.55	0.95	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 1 3/95

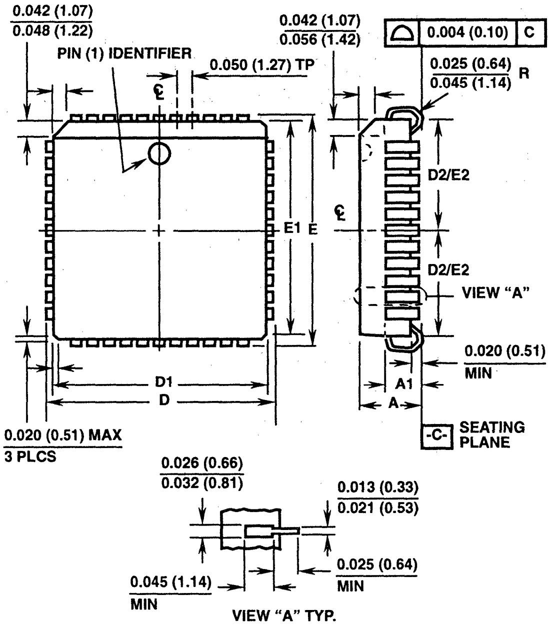
NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.13mm (0.005 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

14

PACKAGING INFORMATION

Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

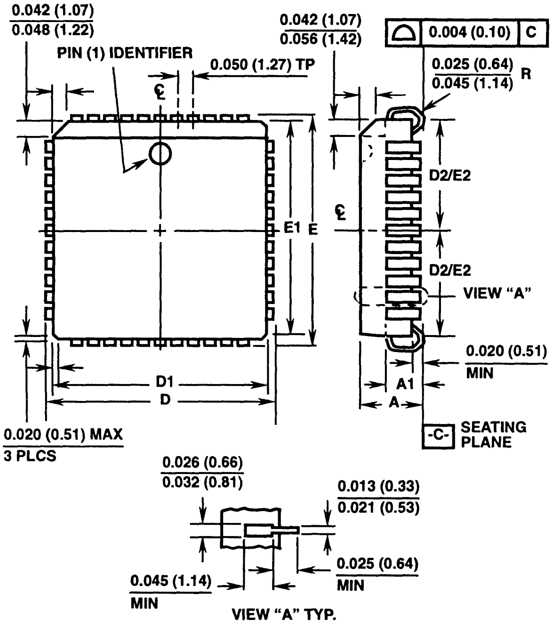
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Plastic Leaded Chip Carrier Packages (PLCC)



N84.1.15 (JEDEC MS-018AF ISSUE A)
84 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	1.185	1.195	30.10	30.35	-
D1	1.150	1.158	29.21	29.41	3
D2	0.541	0.569	13.75	14.45	4, 5
E	1.185	1.195	30.10	30.35	-
E1	1.150	1.158	29.21	29.41	3
E2	0.541	0.569	13.75	14.45	4, 5
N	84		84		6

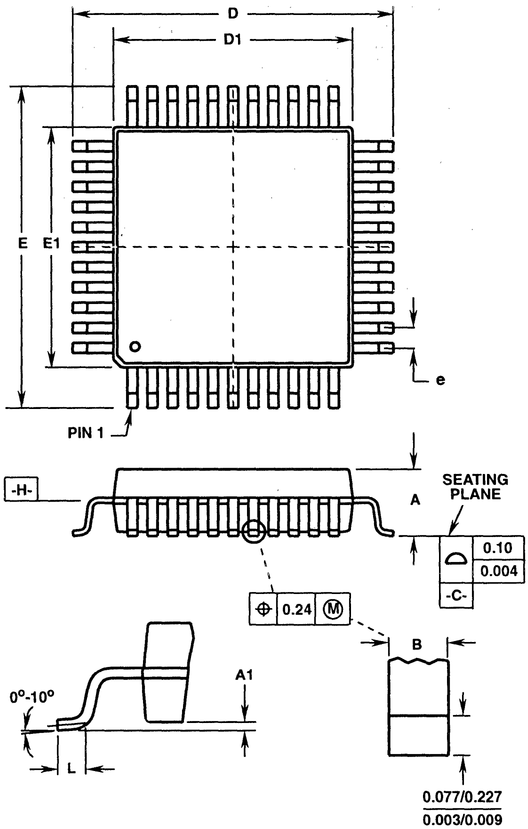
Rev. 1 3/95

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

14 PACKAGING INFORMATION

Metric Plastic Quad Flatpack Packages (MQFP)



Q32.7x7-S

32 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

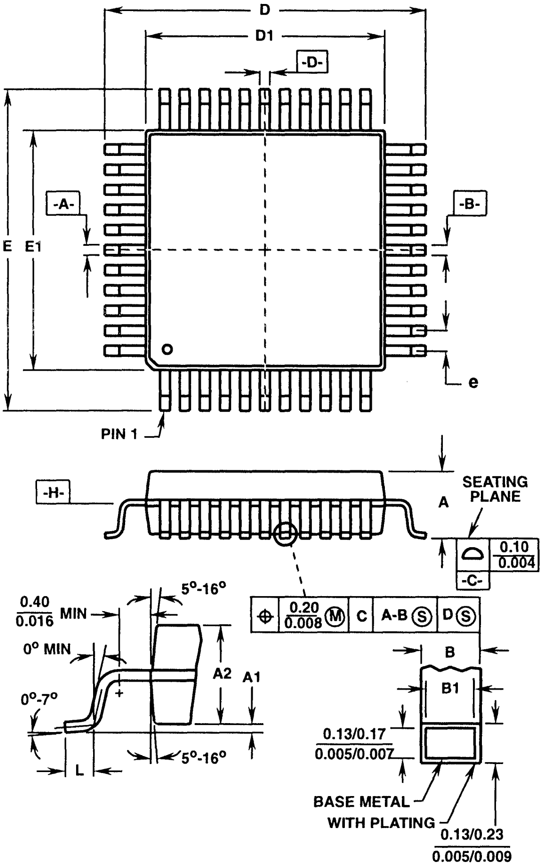
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.054	0.072	1.35	1.85	-
A1	0.000	0.011	0.00	0.30	-
B	0.008	0.017	0.20	0.45	5
D	0.347	0.362	8.80	9.20	2
D1	0.272	0.287	6.90	7.30	3, 4
E	0.347	0.362	8.80	9.20	2
E1	0.272	0.287	6.90	7.30	3, 4
L	0.012	0.027	0.30	0.70	-
N	32		32		6
e	0.032 BSC		0.80 BSC		-

Rev. 2 4/95

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP)



Q44.10x10 (JEDEC MO-108AA-2 ISSUE A)

44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

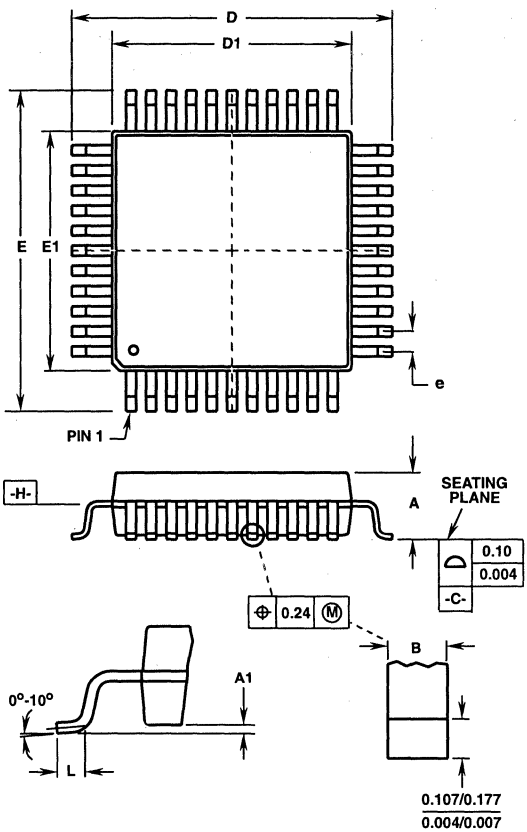
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.093	-	2.35	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.510	0.530	12.95	13.45	3
D1	0.390	0.398	9.90	10.10	4, 5
E	0.510	0.530	12.95	13.45	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

Rev. 1 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP)



Q48.7x7-S

48 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

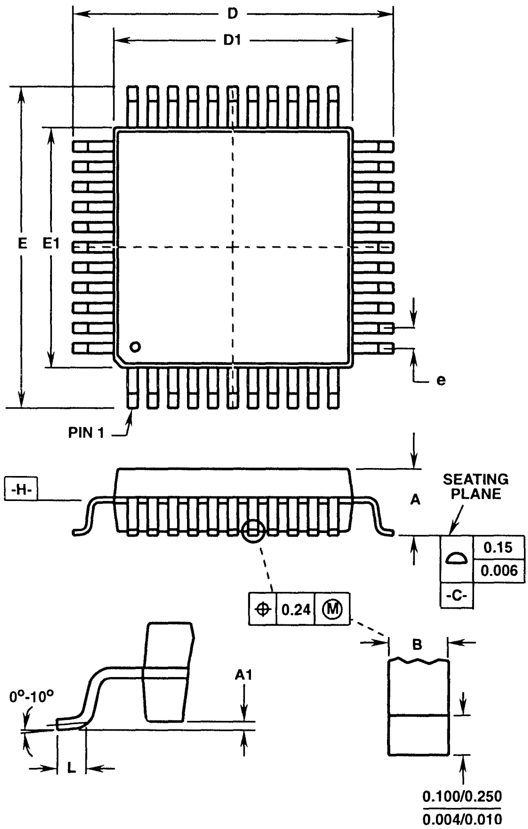
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.056	0.066	1.40	1.70	-
A1	0.000	0.007	0.00	0.20	-
B	0.006	0.010	0.15	0.26	5
D	0.347	0.362	8.80	9.20	2
D1	0.272	0.279	6.90	7.10	3, 4
E	0.347	0.362	8.80	9.20	2
E1	0.272	0.279	6.90	7.10	3, 4
L	0.012	0.027	0.30	0.70	-
N	48		48		6
e	0.020 BSC		0.500 BSC		-

Rev. 1 4/95

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C- .
3. Dimensions D1 and E1 to be determined at datum plane -H- .
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (MQFP)



Q64.14x20-S

64 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.103	0.122	2.60	3.10	-
A1	0.002	0.011	0.05	0.30	-
B	0.012	0.021	0.30	0.55	5
D	0.926	0.956	23.50	24.30	2
D1	0.784	0.803	19.90	20.40	3, 4
E	0.689	0.720	17.50	18.30	2
E1	0.548	0.566	13.90	14.40	3, 4
L	0.024	0.039	0.60	1.00	-
N	64		64		6
e	0.039 BSC		1.00 BSC		-
ND	19		19		-
NE	13		13		-

Rev. 1 4/95

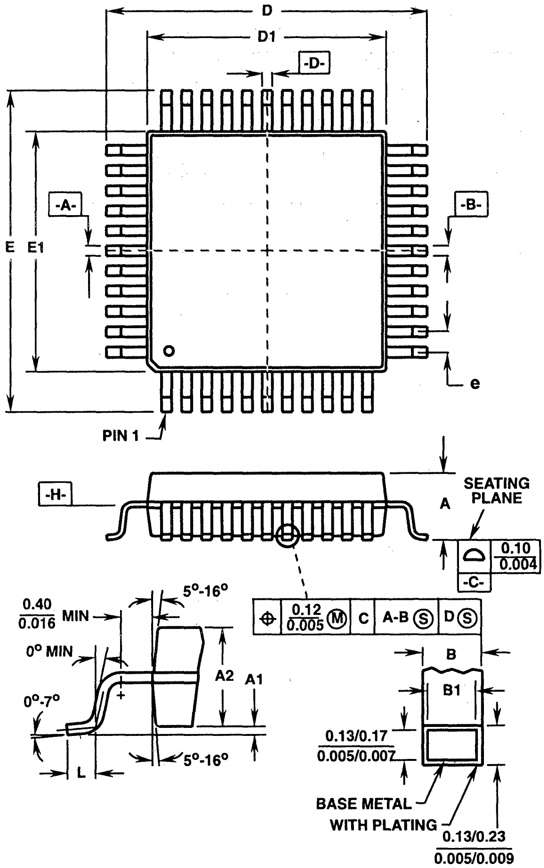
NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

14

PACKAGING INFORMATION

Metric Plastic Quad Flatpack Packages (MQFP)



Q100.14x20 (JEDEC MO-108CC-1 ISSUE A)

100 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

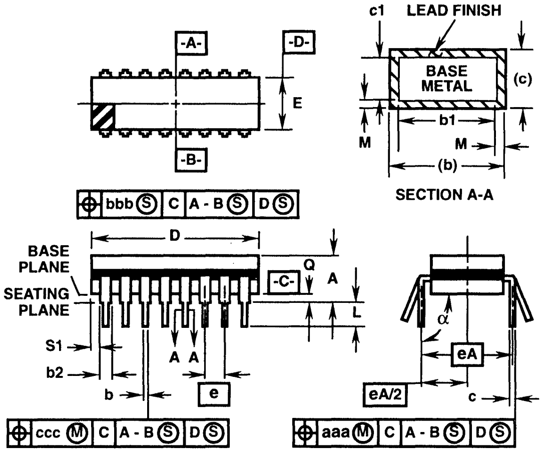
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.134	-	3.40	-
A1	0.010	-	0.25	-	-
A2	0.100	0.120	2.55	3.05	-
B	0.009	0.015	0.22	0.38	6
B1	0.009	0.013	0.22	0.33	-
D	0.904	0.923	22.95	23.45	3
D1	0.783	0.791	19.90	20.10	4, 5
E	0.667	0.687	16.95	17.45	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	100		100		7
e	0.026 BSC		0.65 BSC		-
ND	30		30		-
NE	20		20		-

Rev. 0 1/94

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F8.3A MIL-STD-1835 GDIP1-T8 (D-4, CONFIGURATION A)
8 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

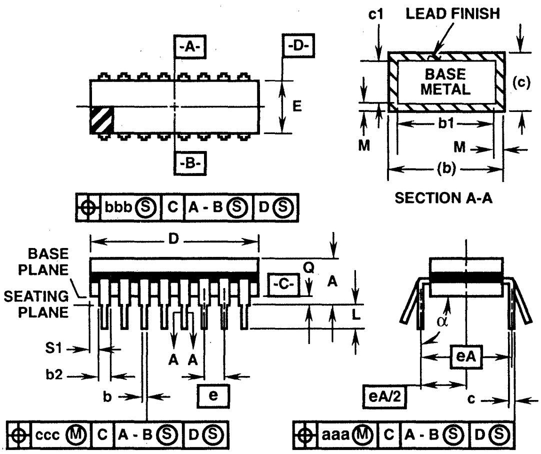
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	8		8		8

Rev. 0 4/94

14

PACKAGING INFORMATION

Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE)

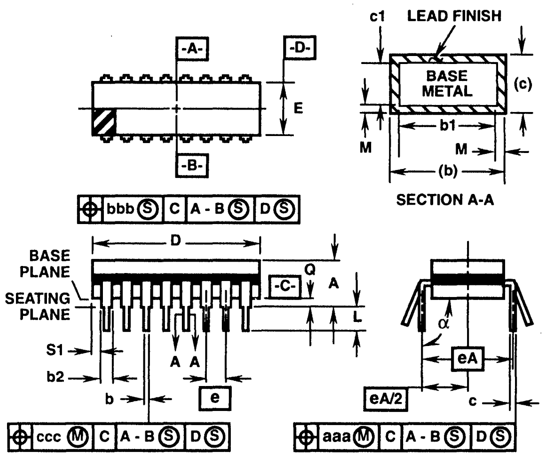
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

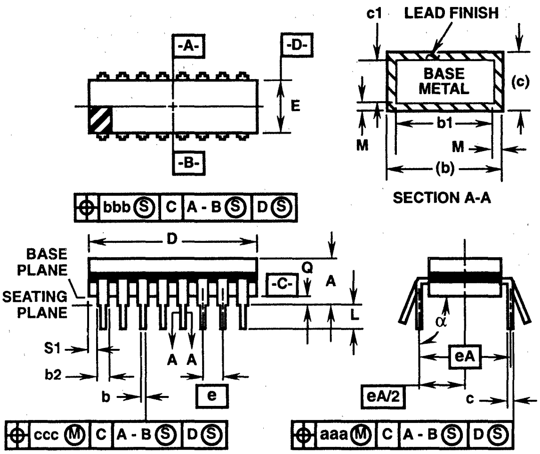
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Frit Seal Packages (CerDIP)



NOTES:

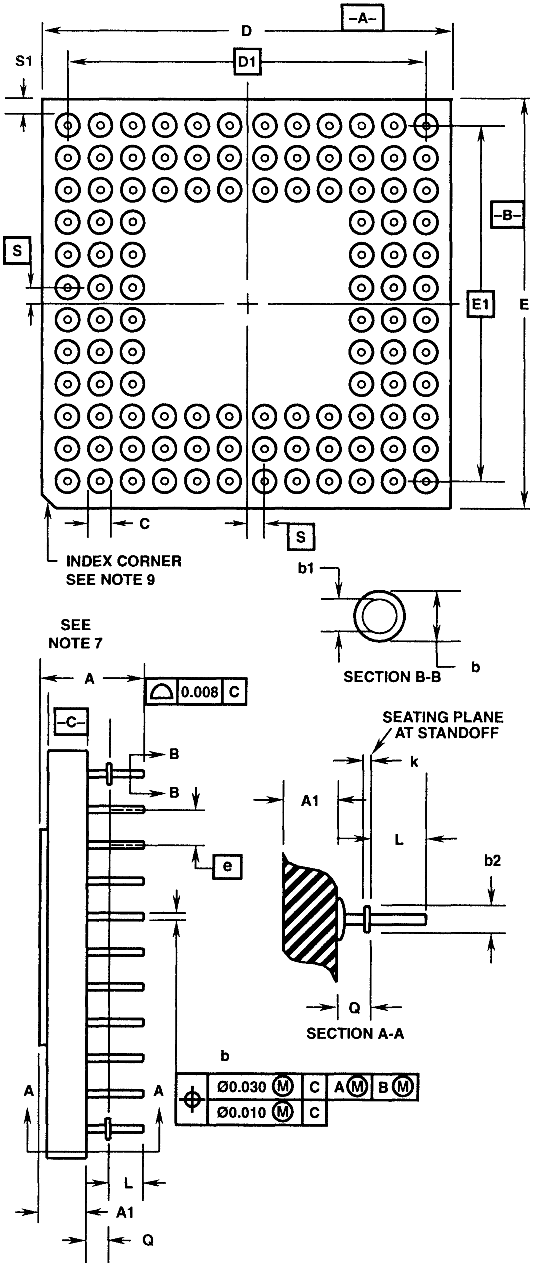
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F20.3 MIL-STD-1835 GDIP1-T20 (D-8, CONFIGURATION A)
20 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.060	-	26.92	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	20		20		8

Rev. 0 4/94

Ceramic Pin Grid Array Packages (CPGA)



G84.A MIL-STD-1835 CMGA3-P84C (P-AC)
84 LEAD CERAMIC PIN GRID ARRAY PACKAGE

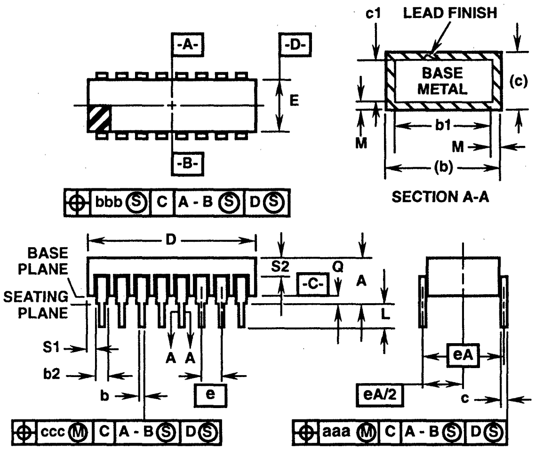
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	0.215	0.345	5.46	8.76	-
A1	0.070	0.145	1.78	3.68	3
b	0.016	0.0215	0.41	0.55	8
b1	0.016	0.020	0.41	0.51	-
b2	0.042	0.058	1.07	1.47	4
C	-	0.080	-	2.03	-
D	1.140	1.180	28.96	29.97	-
D1	1.000 BSC		25.4 BSC		-
E	1.140	1.180	28.96	29.97	-
E1	1.000 BSC		25.4 BSC		-
e	0.100 BSC		2.54 BSC		6
k	0.008 REF		0.20 REF		-
L	0.120	0.140	3.05	3.56	-
Q	0.040	0.060	1.02	1.52	5
S	0.000 BSC		0.00 BSC		10
S1	0.003	-	0.08	-	-
M	11		11		1
N	-	121	-	121	2

Rev. 1 6/28/95

NOTES:

1. "M" represents the maximum pin matrix size.
2. "N" represents the maximum allowable number of pins. Number of pins and location of pins within the matrix is shown on the pinout listing in this data sheet.
3. Dimension "A1" includes the package body and Lid for both cavity-up and cavity-down configurations. This package is cavity up. Dimension "A1" does not include heatsinks or other attached features.
4. Standoffs are intrinsic and shall be located on the pin matrix diagonals. The seating plane is defined by the standoffs at dimensions Q.
5. Dimension "Q" applies to cavity-up configurations only.
6. All pins shall be on the 0.100 inch grid.
7. Datum C is the plane of pin to package interface for both cavity up and down configurations.
8. Pin diameter includes solder dip or custom finishes. Pin tips shall have a radius or chamfer.
9. Corner shape (chamfer, notch, radius, etc.) may vary from that shown on the drawing. The index corner shall be clearly unique.
10. Dimension "S" is measured with respect to datums A and B.
11. Dimensioning and tolerancing per ANSI Y14.5M-1982.
12. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D40.6 MIL-STD-1835 CDIP2-T40 (D-5, CONFIGURATION C)
40 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	2.096	-	53.24	4
E	0.510	0.620	12.95	15.75	4
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	40		40		8

Rev. 0 4/94

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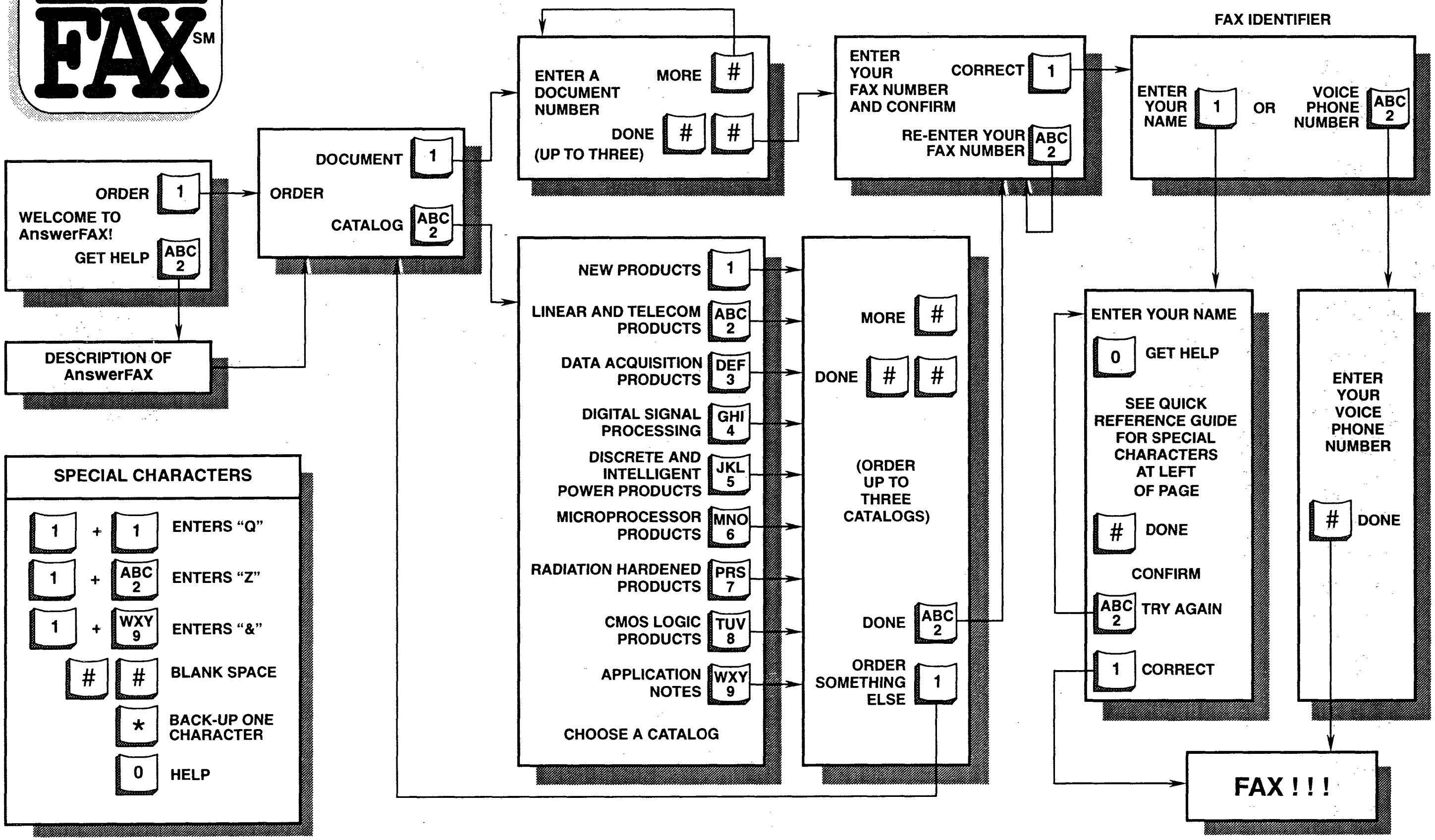

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	DB235B	**RADIATION HARDENED** (1993: 2,232pp) Harris technologies used include dielectric isolation (DI), Silicon-on-Sapphire (SOS), and Silicon-on-Insulator (SOI). The Harris radiation-hardened products include the CD4000, HCS/HCTS and ACS/ACTS logic families, SRAMs, PROMs, op amps, analog multiplexers, the 80C85/80C86 microprocessor family, analog switches, gate arrays, standard cells and custom devices.
	DB260.2	**CDP6805 CMOS MICROCONTROLLERS & PERIPHERALS** (1995: 436pp) This data book represents the full line of Harris Semiconductor CDP6805 products for commercial applications and supersedes previously published CDP6805 data books under the Harris, GE, RCA or Intersil names.
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	DB302B	**DIGITAL SIGNAL PROCESSING** (1994: 528pp) Product specifications on one-dimensional and two-dimensional filters, signal synthesizers, multipliers, special function devices (such as address sequencers, binary correlators, histogrammer).
	DB303	**MICROPROCESSOR PRODUCTS** (1992: 1,156pp) For commercial and military applications. Product specifications on CMOS microprocessors, peripherals, data communications, and memory ICs.
	DB304.1	**INTELLIGENT POWER ICs** (1994: 946pp) This data book includes a complete set of data sheets for product specifications, application notes with design details for specific applications of Harris products, and a description of the Harris quality and high reliability program.
	DB309.1	**MCT/IGBT/DIODES** (1995: 706pp) This MCT/IGBT/Diodes Databook represents the full line of these products made by Harris Semiconductor Discrete Power Products for commercial applications.
	DB314	**SIGNAL PROCESSING NEW RELEASES** (1995: 690pp) This data book represents the newest products made by Harris Semiconductor Data Acquisition Products, Linear Products, Telecom Products and Digital Signal Processing Products for commercial applications.
	DB450.4	**TRANSIENT VOLTAGE SUPPRESSION DEVICES** (1995: 400pp) Product specifications of Harris varistors and surgectors. Also, general informational chapters such as: "Voltage Transients - An Overview," "Transient Suppression - Devices and Principles," "Suppression - Automotive Transients."
	DB500B	**LINEAR AND TELECOM ICs** (1993: 1,312pp) Product specifications for: op amps, comparators, S/H amps, differential amps, arrays, special analog circuits, telecom ICs, and power processing circuits.
	Digital Military	**DIGITAL MILITARY** (1989: 680pp) Harris CMOS digital ICs – microprocessors, peripherals, data communications and memory – are included in this data book.
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	DB312	**ANALOG MILITARY DATA BOOK SUPPLEMENT** (1994: 432pp) The 1994 Military Data Book Supplement, combined with the 1989 Analog Military Product Data Book, contain detailed technical information on the extensive line of Harris Semiconductor Linear and Data Acquisition products for Military (MIL-STD-883, DESC SMD and JAN) applications and supersedes all previously published Linear and Data Acquisition Military data books. For applications requiring Radiation Hardened products, please refer to the 1993 Harris Radiation Hardened Product Data Book (document #DB235B)
	PSG201.22	**PRODUCT SELECTION GUIDE** (1995: 816pp) Key product information on all Harris Semiconductor devices. Sectioned (Linear, Data Acquisition, Digital Signal Processing, Telecom, Intelligent Power, Discrete Power, Digital Microprocessors and Hi-Rel/Military and Rad Hard) for easy use and includes cross references and alphanumeric part number index.
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