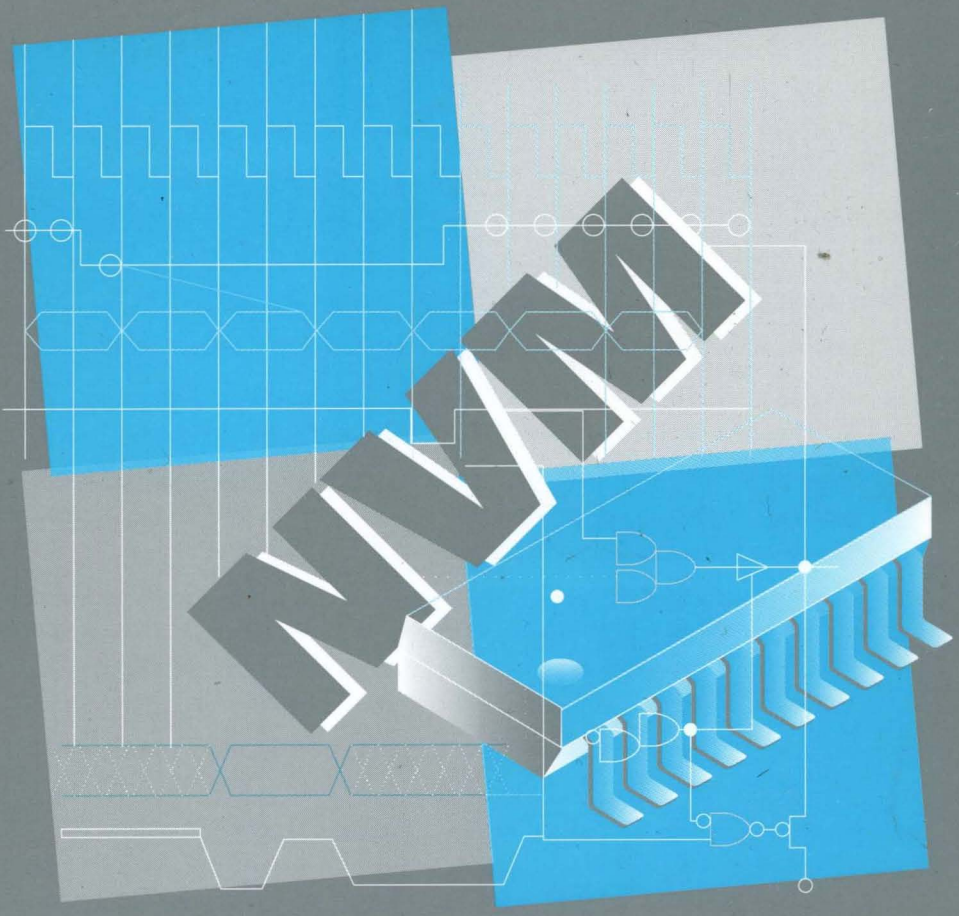
Nonvolatile Memory

Data Book



HITACHI

Nonvolatile Memory
Data Book

HITACHI

Contents

Part 1 EEPROM

64K EEPROM

HN58C65 Series

8,192-word × 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

Rev. 1.0
April 12, 1995

The Hitachi HN58C65 is an electrically erasable and programmable ROM organized as 8,192-word × 8-bit. It realizes high speed, low power consumption, and a high level of reliability, employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 32-byte page programming function to make its erase and write operations faster.

Features

- Single 5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (32 bytes): 10 ms max
- Fast access time: 250 ns max
- Low power dissipation:
  - 20 mW/MHz typ (active)
  - 2.0 mW typ (standby)
- $\overline{Data}$ polling, RDY/$\overline{Busy}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 year data retention

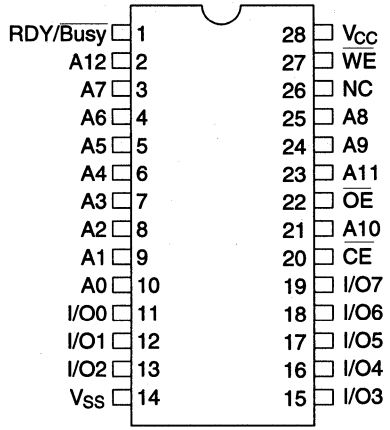
Ordering Information

Type No.	Access time	Package
HN58C65P-25	250 ns	600 mil 28-pin plastic DIP (DP-28)
HN58C65FP-25	250 ns	28-pin *1 plastic SOP (FP-28D/DA)

Notes: T is added to the end of Type No. for a SOP of 3.0 mm (max) thickness.

Pin Arrangement

HN58C65P/FP Series

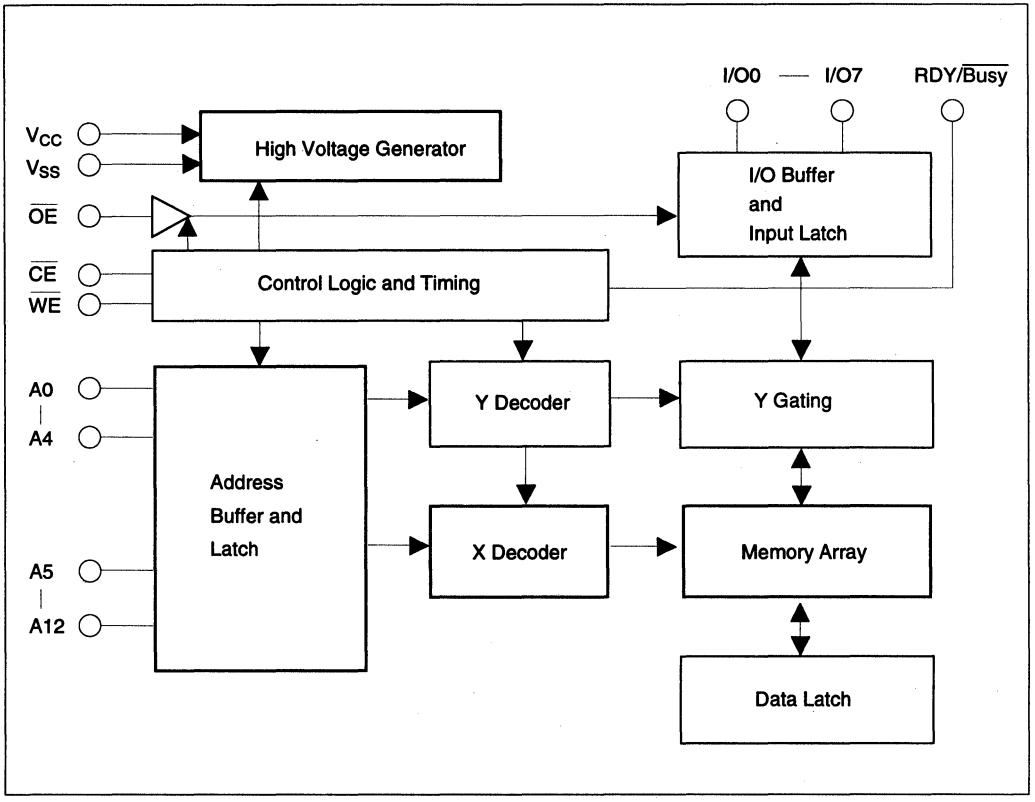


(Top View)

Pin Description

Pin name	Function
A0–A12	Address input
I/O0–I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No connection
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$

Block Diagram



Mode Selection

Pin Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	High-Z	Dout
Standby	V_{IH}	×*1	×	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	High-Z
Write inhibit	×	×	V_{IH}	High-Z	—
	×	V_{IL}	X	High-Z	—
$\overline{Data}$ polling	V_{IL}	V_{IL}	V_{IH}	V_{OL}	Data out (I/O7)

Note: 1. × = Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage *1	V_{CC}	–0.6 to +7.0	V
Input voltage *1	Vin	–0.5*2 to +7.0	V
Operating temperature range*3	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. With respect to V_{SS}
2. Vin min = –3.0 V for pulse width ≤ 50 ns
3. Including electrical characteristics and data retention.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IL}	–0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC} + 1	V
Operating temperature	Topr	0	—	70	°C

DC Characteristics (Ta=0 to +70°C, V_{CC} = 5 V ±10 %)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	1	mA	$\overline{CE}$ = V_{IH}, $\overline{CE}$ = V_{CC}
V_{CC} current (active)	I_{CC2}	—	—	8	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 5.5 V
		—	—	25	mA	Iout = 0 mA, Duty = 100%, Cycle = 250 ns at V_{CC} = 5.5 V
Input low voltage	V_{IL}	–0.3*[1]	—	0.8	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} + 1	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Note: 1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance*[1]	Cin	—	—	6	pF	Vin = 0 V
Output capacitance*[1]	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100 % tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10 %)

Test Conditions

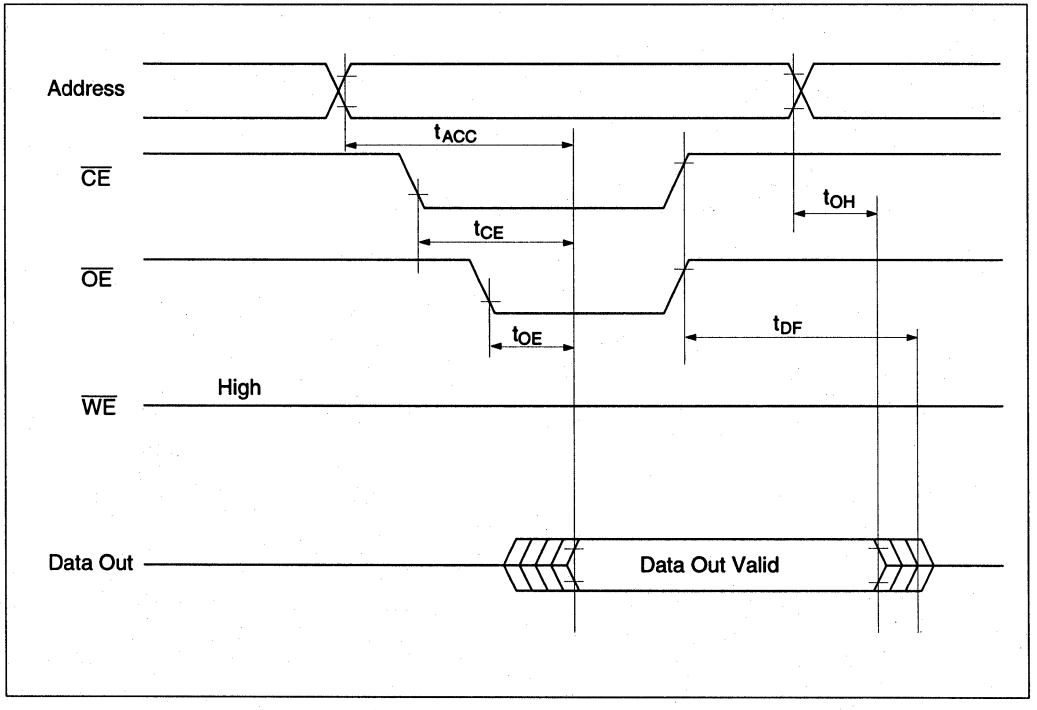
- Input pulse levels : 0.4 V to 2.4 V
- Input rise and fall time : ≤ 20 ns
- Output load : 1TTL Gate +100 pF
- Reference levels for measuring timing: 0.8 V and 2.0 V

Read Cycle

Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	250	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	100	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$, $\overline{CE}$ high to output float*1	t_{DF}	0	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined at which the outputs achieve the open circuit condition and are no longer driven.

Read Timing Waveform

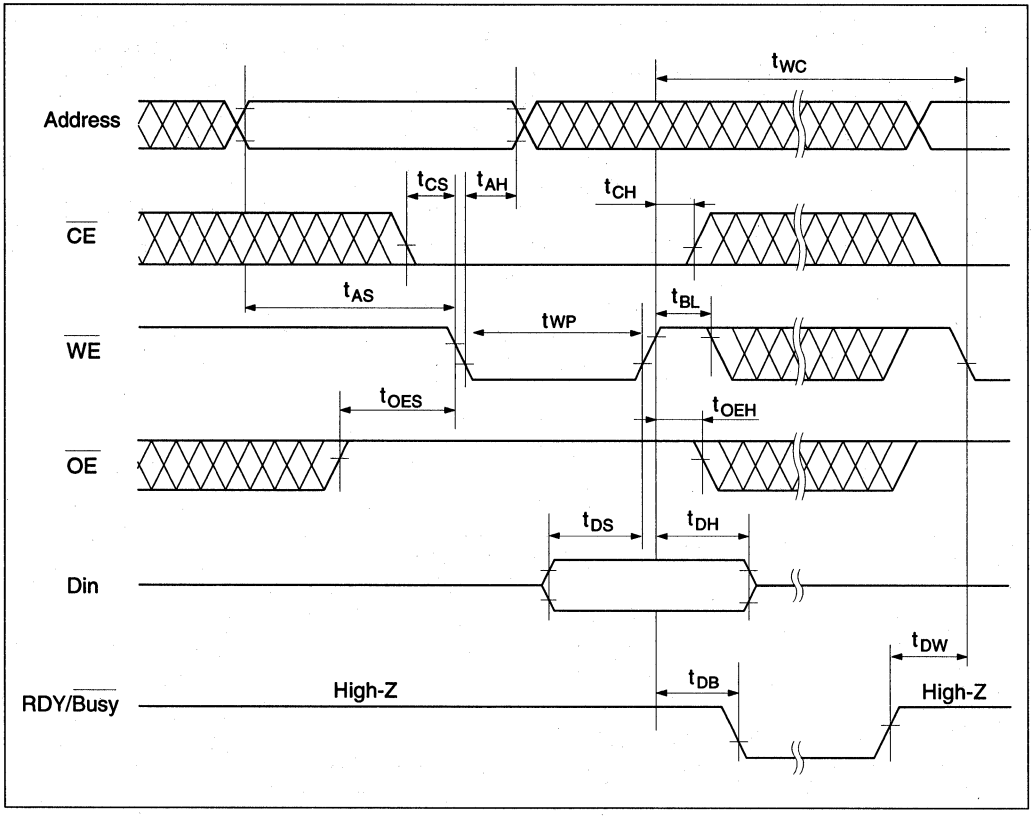


Write Cycle

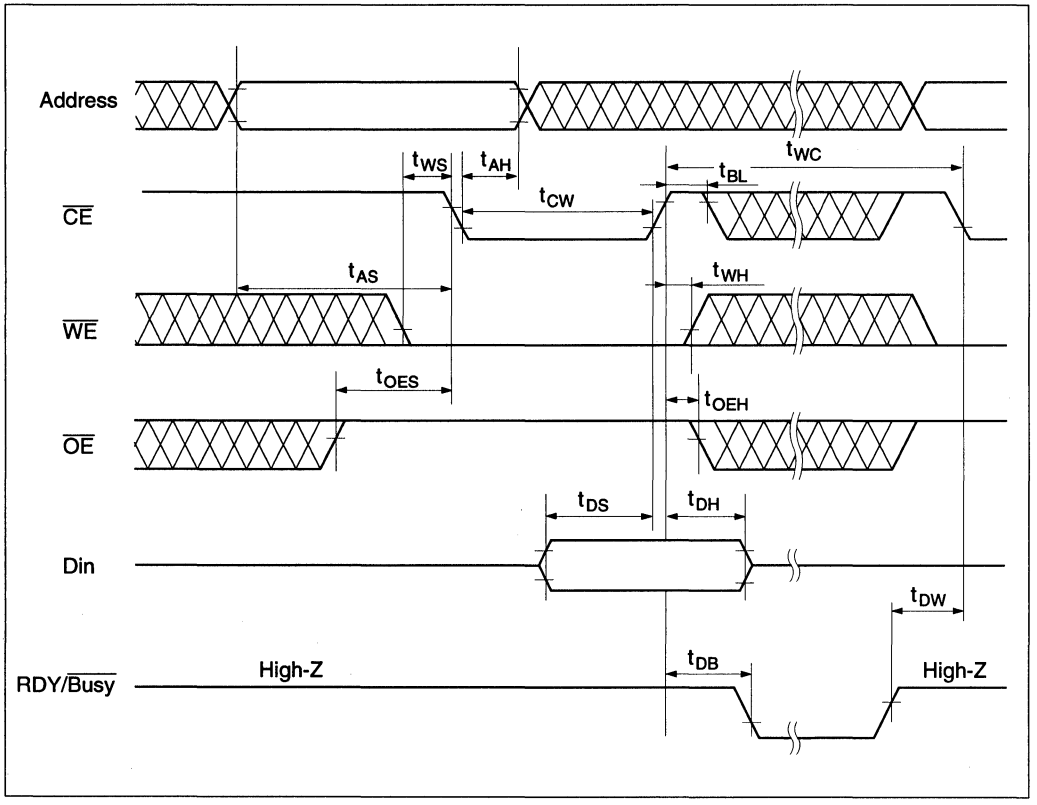
Parameter	Symbol	Min*1	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	20	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	200	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	200	—	—	ns	
Data latch time	t_{DL}	100	—	—	ns	
Byte lode cycle	t_{BLC}	0.30	—	30	µs	
Byte lode window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*2	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	150	—	—	ns	

Note: 1. Use this device in longer cycle than this value.
2. t_{WC} must be longer than this value unless polling technique is used. This device automatically completes the internal write operation within this value.

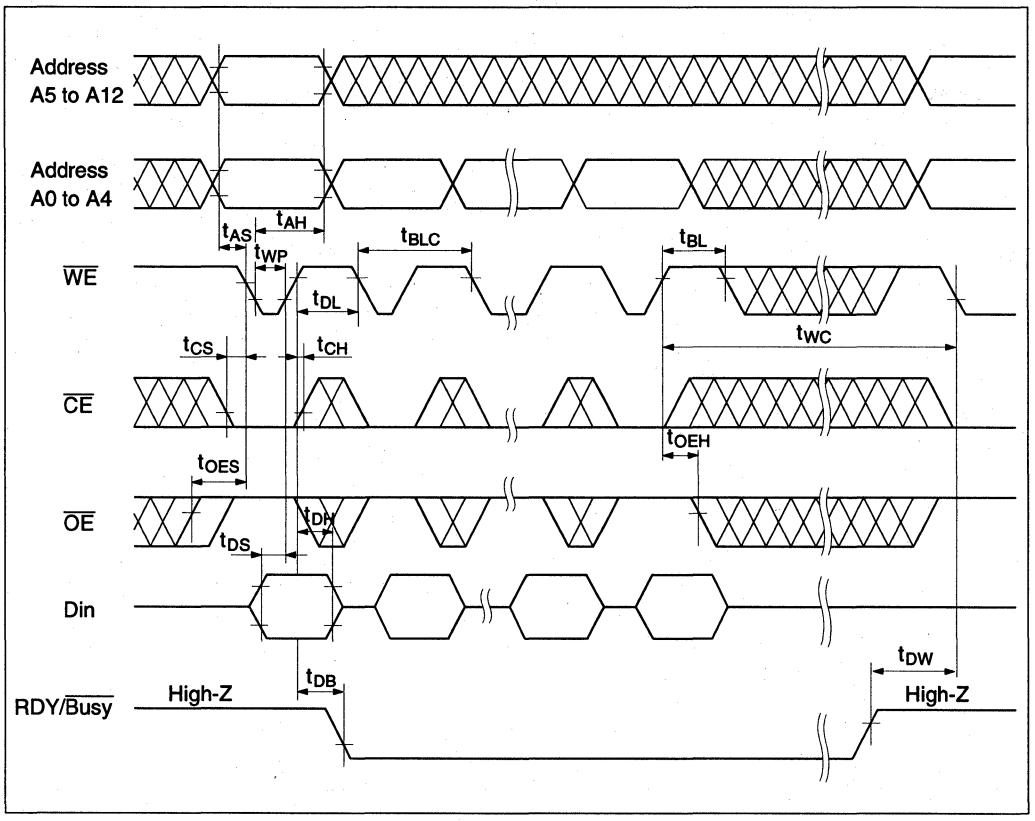
Byte Write Timing Waveform(1) ($\overline{WE}$ Controlled)



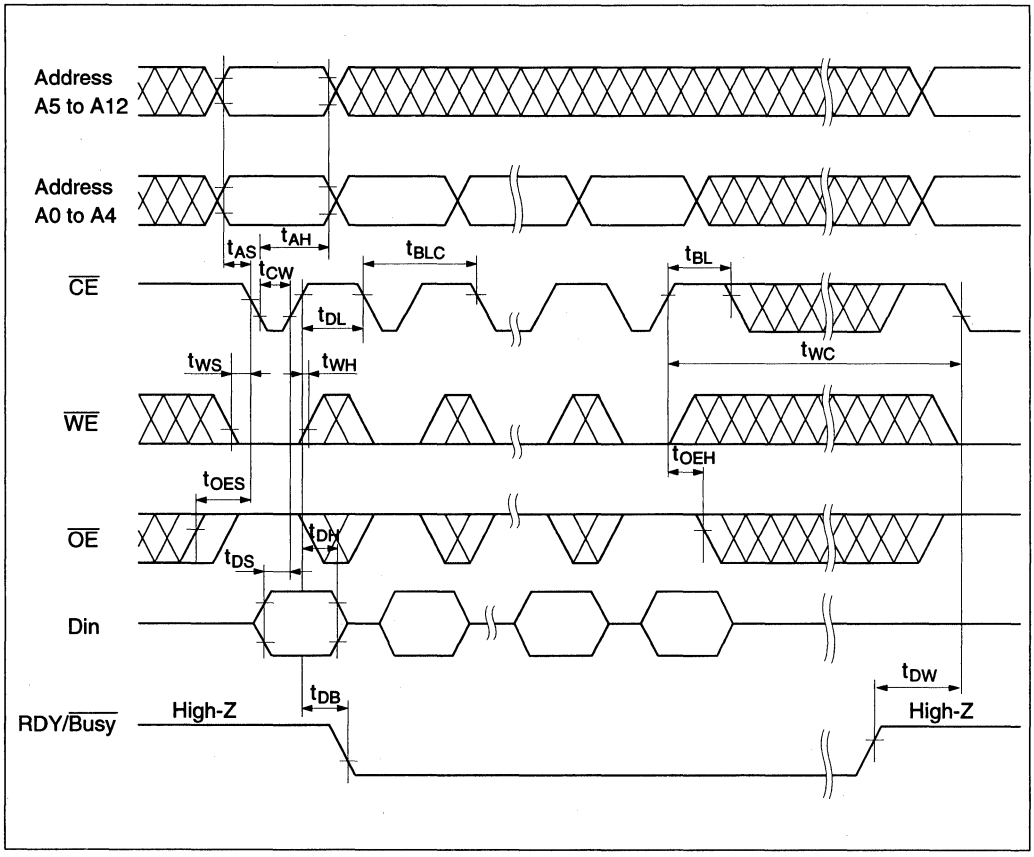
Byte Write Timing Waveform(2) ($\overline{CE}$ Controlled)



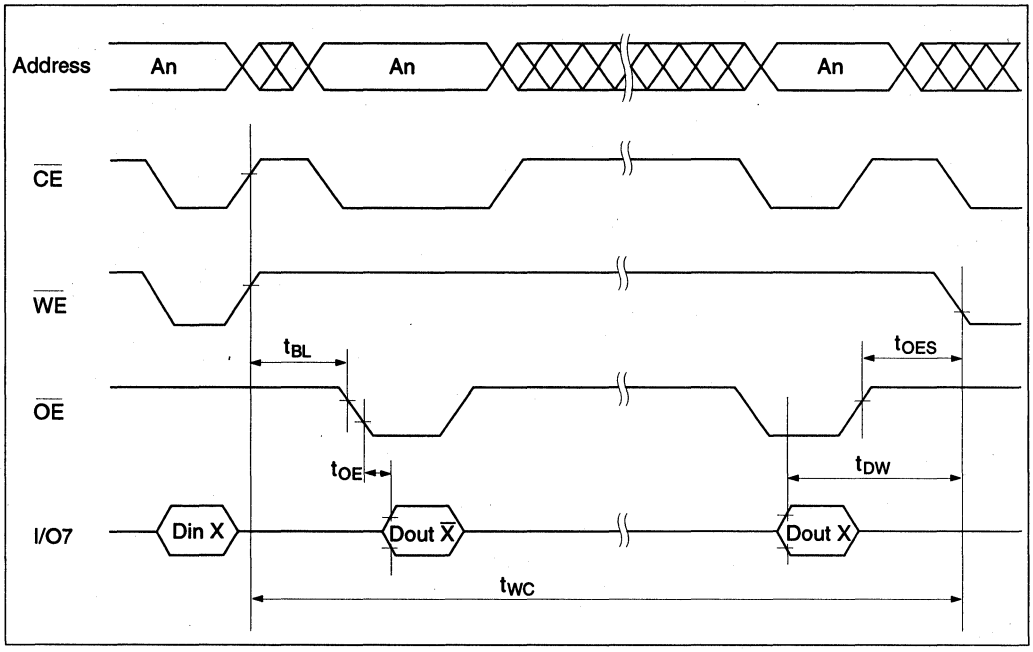
Page Write Timing Waveform(1) ($\overline{WE}$ Controlled)



Page Write Timing Waveform(2) ($\overline{CE}$ Controlled)



Data Polling Timing Wavefome



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 31 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs of the preceding rising edge of $\overline{WE}$. When $\overline{CE}$ or $\overline{WE}$ is high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{Data}$ Polling

$\overline{Data}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{Busy}$ Signal

RED/$\overline{Busy}$ signal also allows the status of the EEPROM to be determined. The RDY/$\overline{Busy}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{Busy}$ signal changes state to high impedance.

$\overline{WE}$,$\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

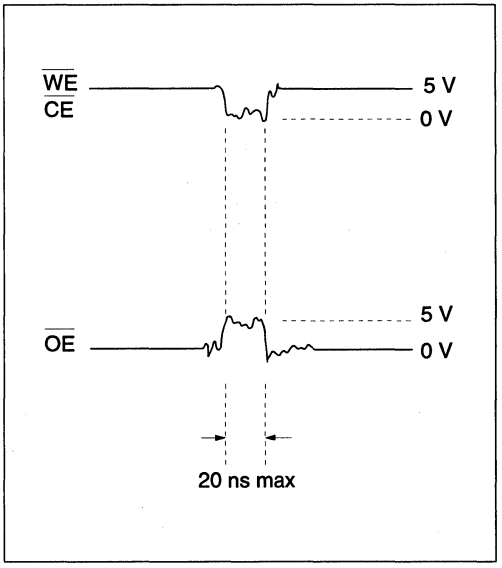
Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 3×10^3 cycles in case of byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

Data Protection

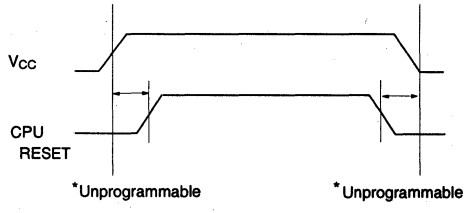
1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to program mode by mistake.
To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less in program mode.
Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at V_{CC} On/Off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.



*The EEPROM should be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.

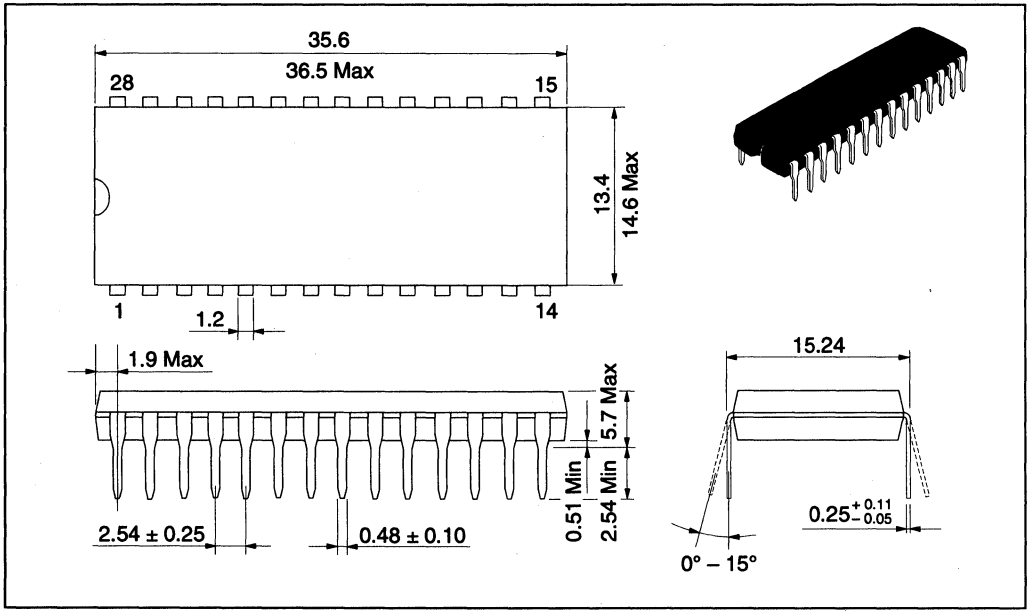
In addition, when V_{CC} is turned on or off, the input level of control pins must be held as shown in the table below.

$\overline{CE}$	V_{CC}	×	×
$\overline{OE}$	×	V_{SS}	×
$\overline{WE}$	×	×	V_{CC}

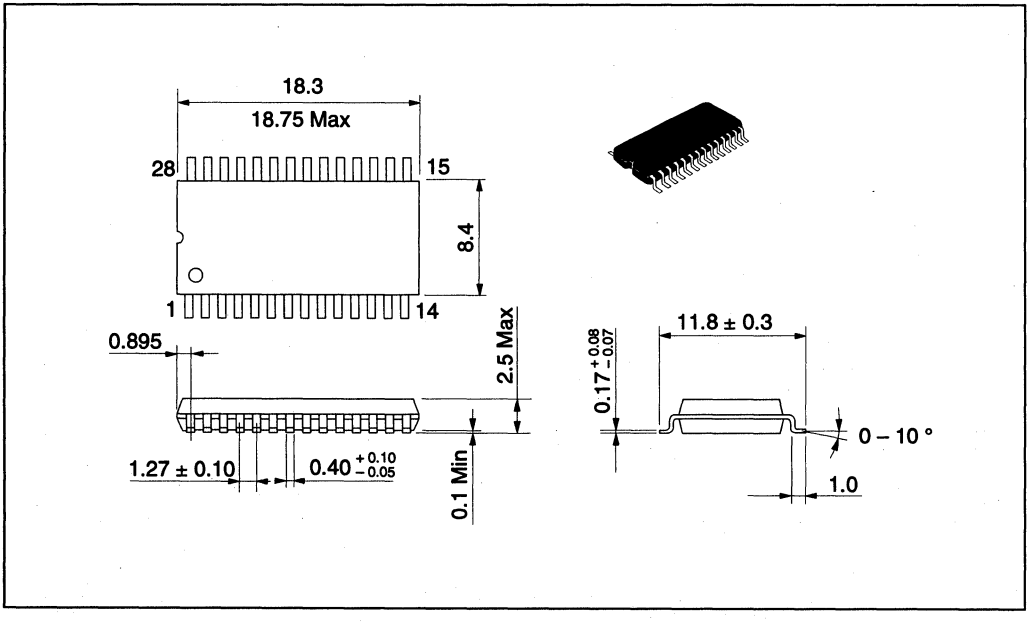
×: Don't care.
V_{CC}: Pull-up to V_{CC} level.
V_{SS}: Pull-down to V_{SS} level.

Package Dimensions

HN58C65P Series (DP-28) **Unit : mm**

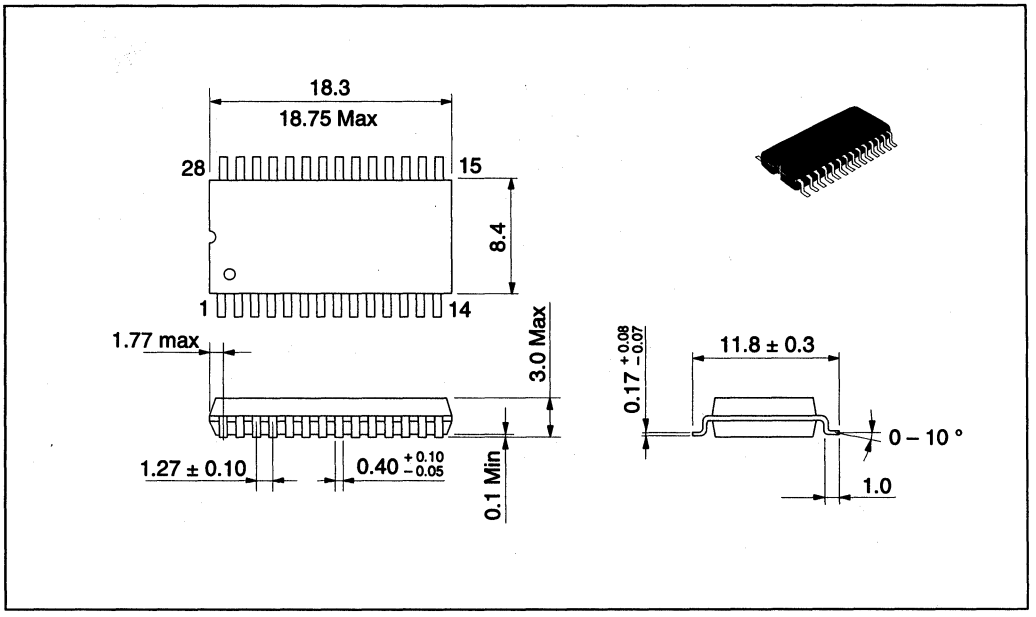


HN58C65FP Series (FP-28D) **Unit : mm**



Package Dimensions (cont)

HN58C65FP Series (FP-28DA) **Unit : mm**



HN58C65PJ/FPI

8,192-word × 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

Rev. 1.0
June 20, 1995

The Hitachi HN58C65 is an electrically erasable and programmable ROM organized as 8,192-word × 8-bit. It realizes high speed, low power consumption, and a high level of reliability, employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 32-byte page programming function to make its erase and write operations faster.

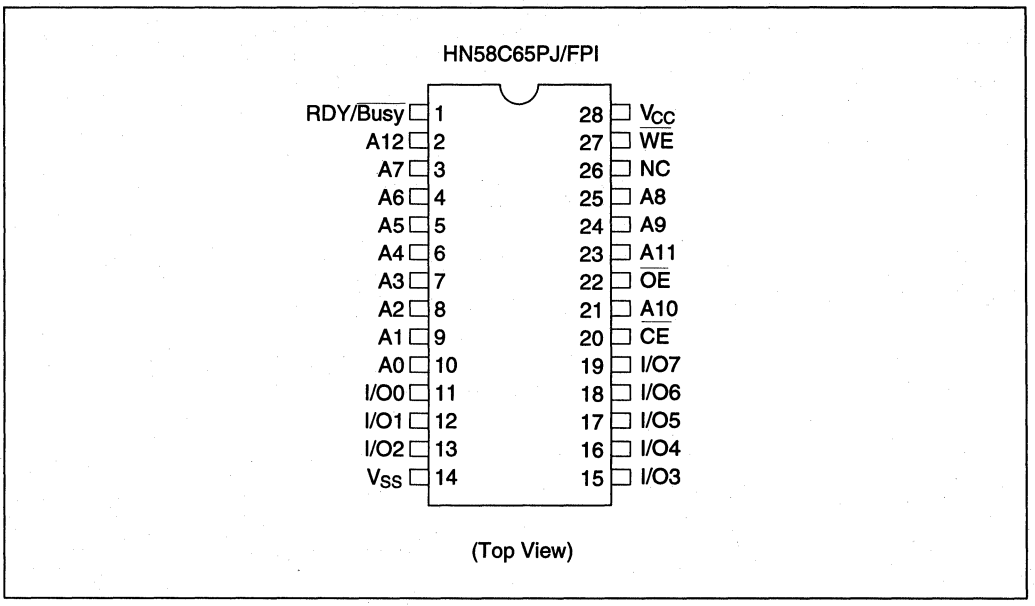
Features

- Single 5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (32 bytes): 10 ms max
- Fast access time: 250 ns max
- Low power dissipation:
  - 20 mW/MHz typ (active)
  - 2.0 mW typ (standby)
- $\overline{\text{Data}}$ polling, RDY/$\overline{\text{Busy}}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 year data retention
- Operating temperature: –40 to 85°C

Ordering Information

Type No.	Access time	Package
HN58C65PJ-25	250 ns	600 mil 28-pin plastic DIP (DP-28)
HN58C65FPI-25T	250 ns	400 mil 28-pin plastic SOP (FP-28DA)

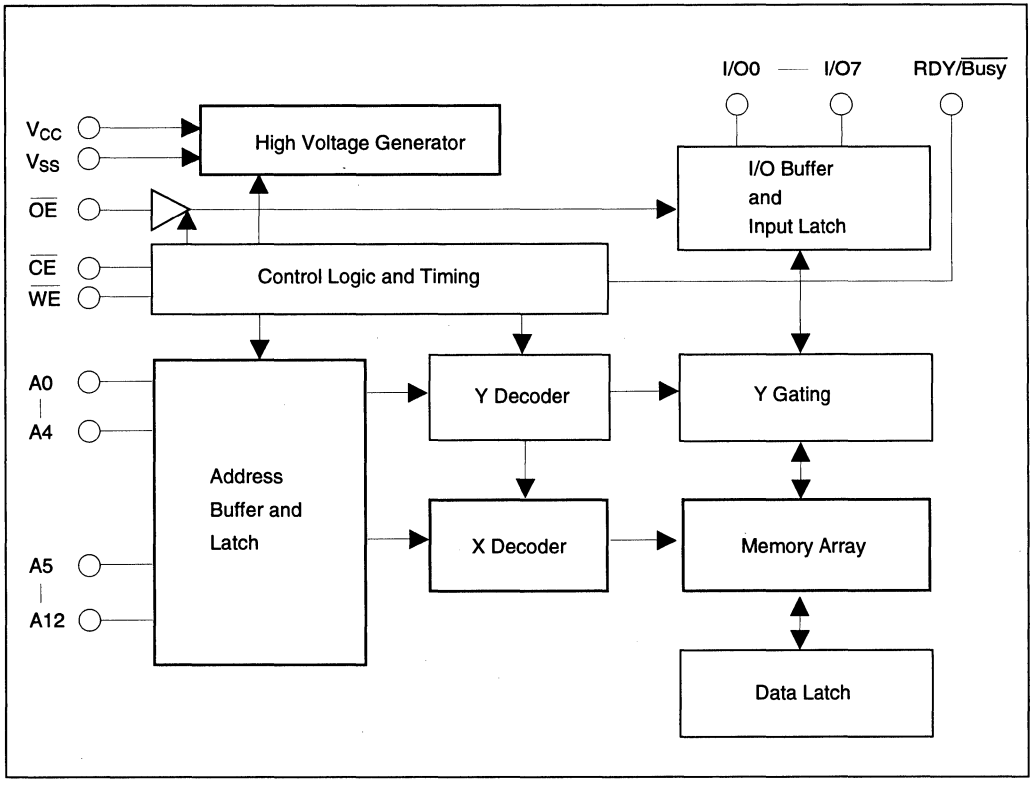
Pin Arrangement



Pin Description

Pin name	Function
A0–A12	Address input
I/O0–I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power (+5 V)
V_{SS}	Ground
NC	No connection
RDY/$\overline{Busy}$	Ready/$\overline{Busy}$

Block Diagram



Mode Selection

Pin Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	High-Z	Dout
Standby	V_{IH}	×*1	×	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	High-Z
Write inhibit	×	×	V_{IH}	High-Z	—
	×	V_{IL}	×	High-Z	—
$\overline{Data}$ polling	V_{IL}	V_{IL}	V_{IH}	V_{OL}	Data out (I/O7)

Note: 1. × = Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage *1	V_{CC}	–0.6 to +7.0	V
Input voltage *1	Vin	–0.5*2 to +7.0	V
Operating temperature range*3	Topr	–40 to +85	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. With respect to V_{SS}
2. Vin min = –3.0 V for pulse width ≤ 50 ns
3. Including electrical characteristics and data retention.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IL}	–0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC} + 1	V
Operating temperature	Topr	–40	—	85	°C

DC Characteristics (Ta=–40 to +85°C, V_{CC} = 5 V ±10 %)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	1	mA	$\overline{CE}$ = V_{IH}, $\overline{CE}$ = V_{CC}
V_{CC} current (active)	I_{CC2}	—	—	8	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 5.5 V
		—	—	25	mA	Iout = 0 mA, Duty = 100%, Cycle = 250 ns at V_{CC} = 5.5 V
Input low voltage	V_{IL}	–0.3*1	—	0.8	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} + 1	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Note: 1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance*1	Cin	—	—	6	pF	Vin = 0 V
Output capacitance*1	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100 % tested.

AC Characteristics (Ta = – 40 to +85°C, V_{CC} = 5 V ± 10 %)

Test Conditions

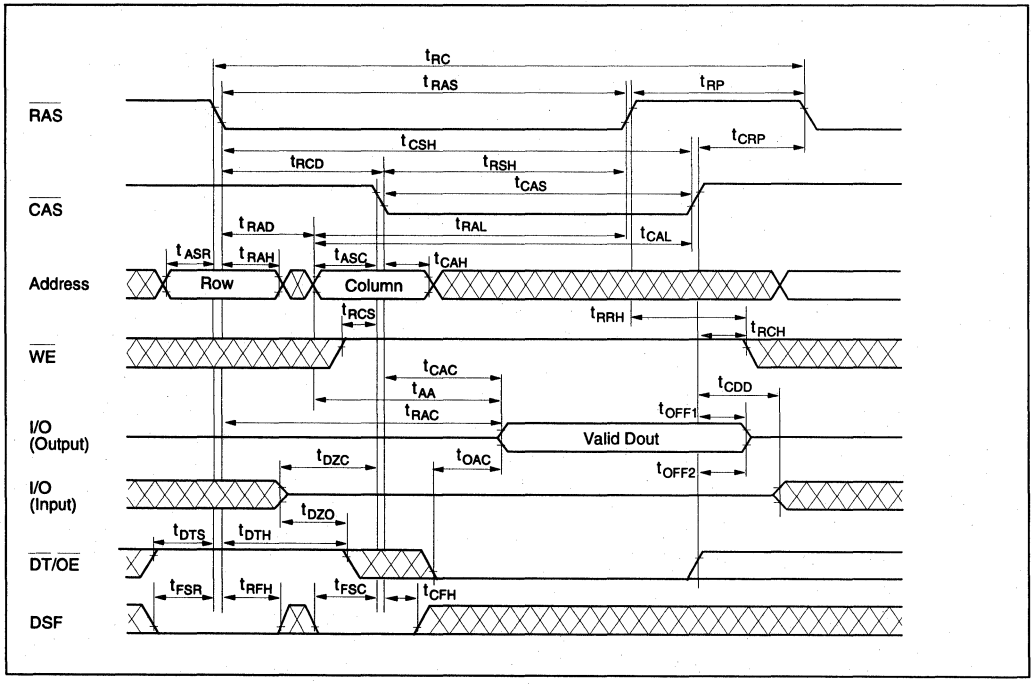
- Input pulse levels : 0.4 V to 2.4 V
- Input rise and fall time : ≤ 20 ns
- Output load : 1TTL Gate +100 pF
- Reference levels for measuring timing: 0.8 V and 2.0 V

Read Cycle

Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	250	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	100	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$, $\overline{CE}$ high to output float*1	t_{DF}	0	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined at which the outputs achieve the open circuit condition and are no longer driven.

Read Timing Waveform



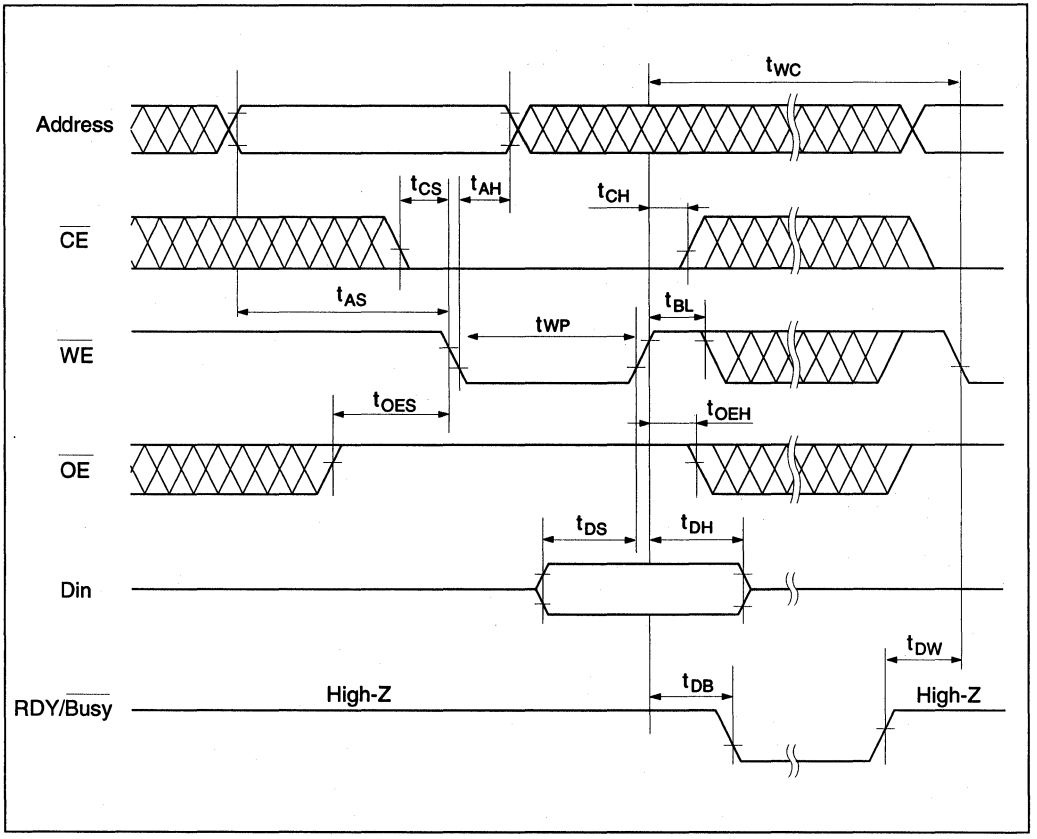
Write Cycle

Parameter	Symbol	Min*1	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	120	—	—	ns	
Data hold time	t_{DH}	30	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	200	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	200	—	—	ns	
Data latch time	t_{DL}	100	—	—	ns	
Byte lode cycle	t_{BLC}	0.30	—	30	µs	
Byte lode window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*2	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	150	—	—	ns	

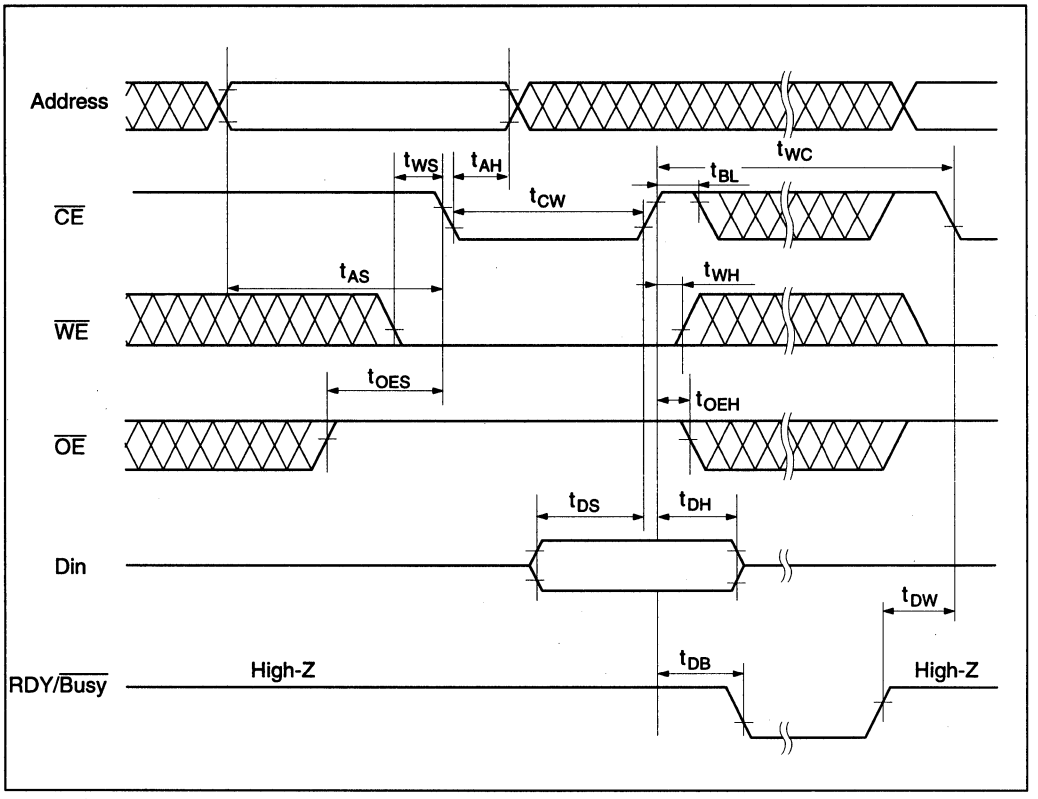
Note: 1. Use this device in longer cycle than this value.

2. t_{WC} must be longer than this value unless polling technique is used. This device automatically completes the internal write operation within this value.

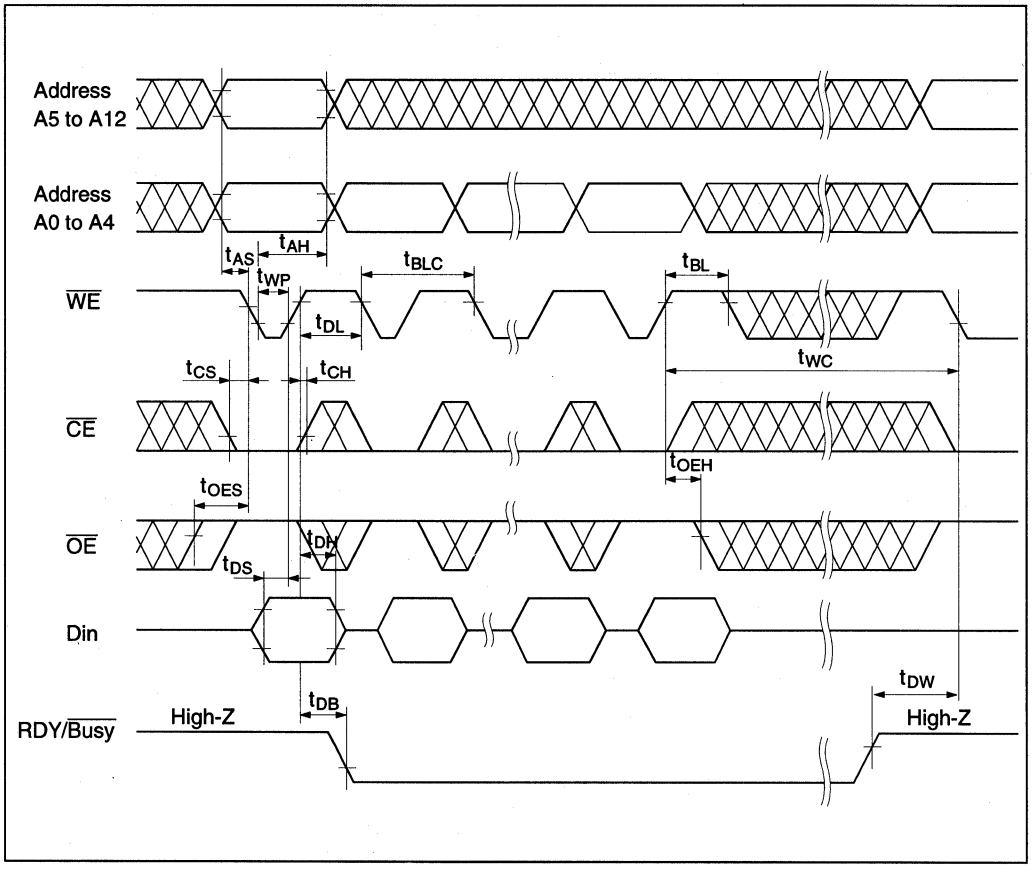
Byte Write Timing Waveform(1) ($\overline{WE}$ Controlled)



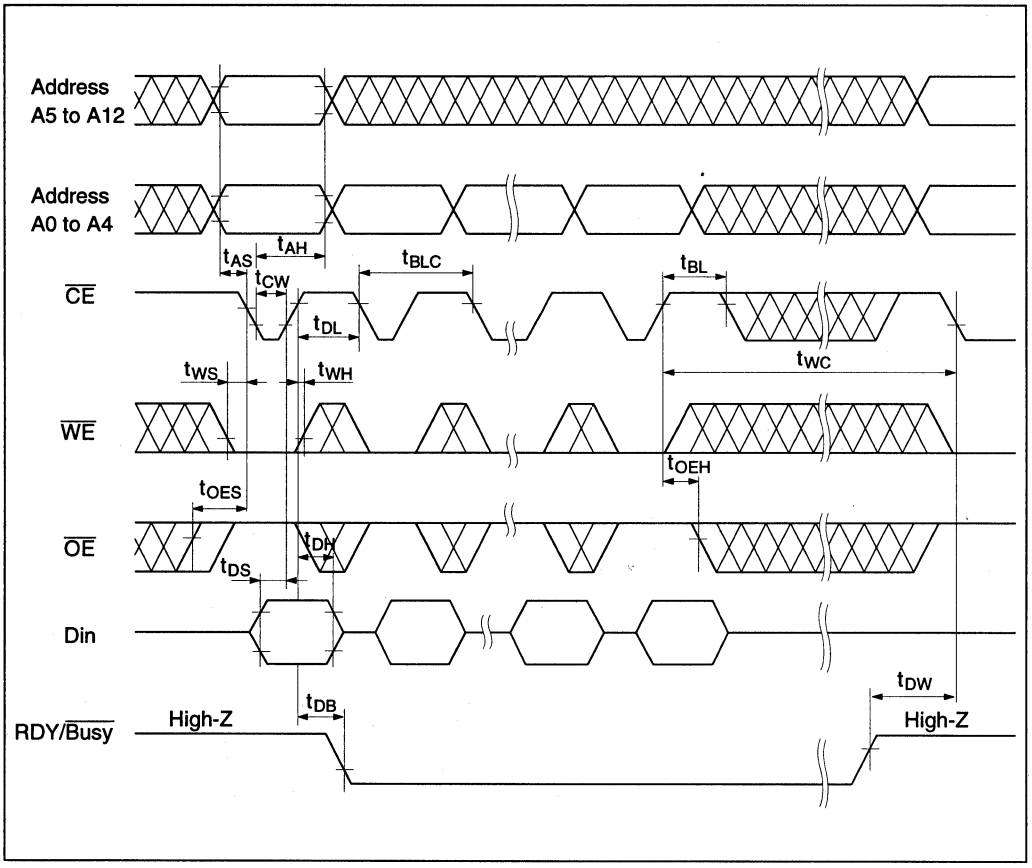
Byte Write Timing Waveform(2) ($\overline{CE}$ Controlled)



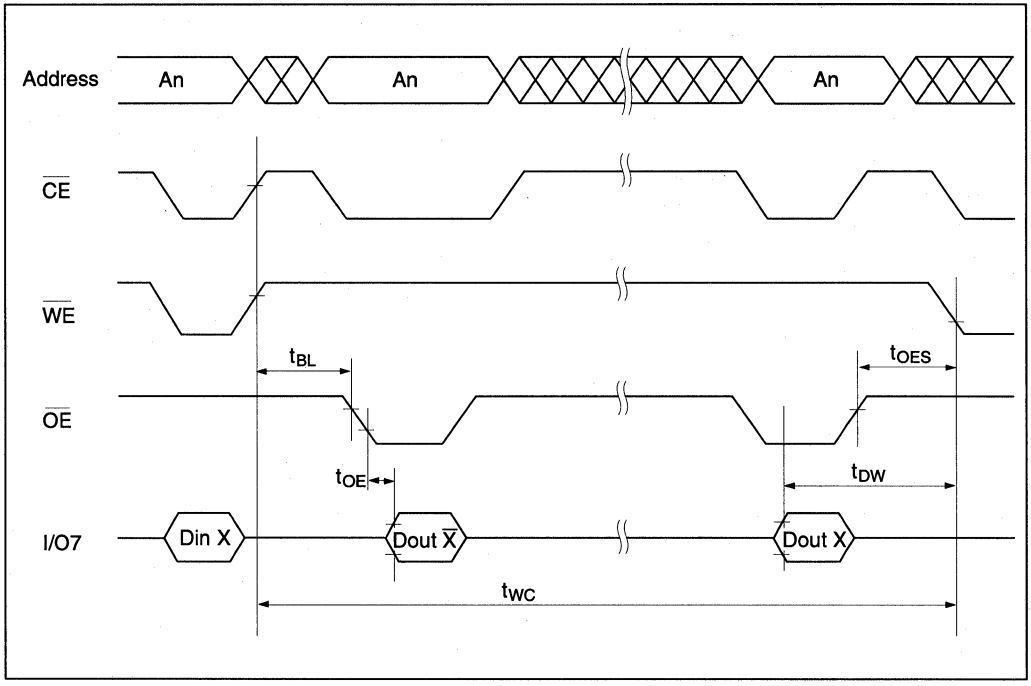
Page Write Timing Waveform(1) ($\overline{WE}$ Controlled)



Page Write Timing Waveform(2) ($\overline{CE}$ Controlled)



$\overline{\text{Data}}$ Polling Timing Waveform



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 31 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs of the preceding rising edge of $\overline{WE}$. When $\overline{CE}$ or $\overline{WE}$ is high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{\text{Data}}$ Polling

$\overline{\text{Data}}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{\text{Busy}}$ Signal

RED/$\overline{\text{Busy}}$ signal also allows the status of the EEPROM to be determined. The RDY/$\overline{\text{Busy}}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{\text{Busy}}$ signal changes state to high impedance.

$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 3×10^3 cycles in case of byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

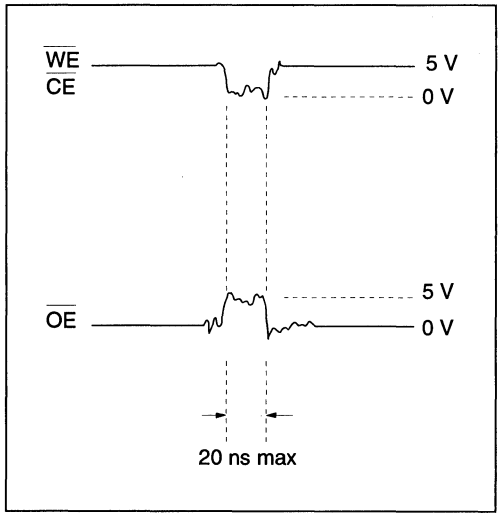
Data Protection

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to program mode by mistake.

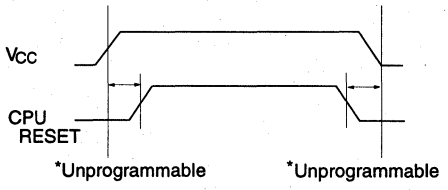
To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less in program mode.

Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at V_{CC} On/Off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.



*The EEPROM shoud be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.

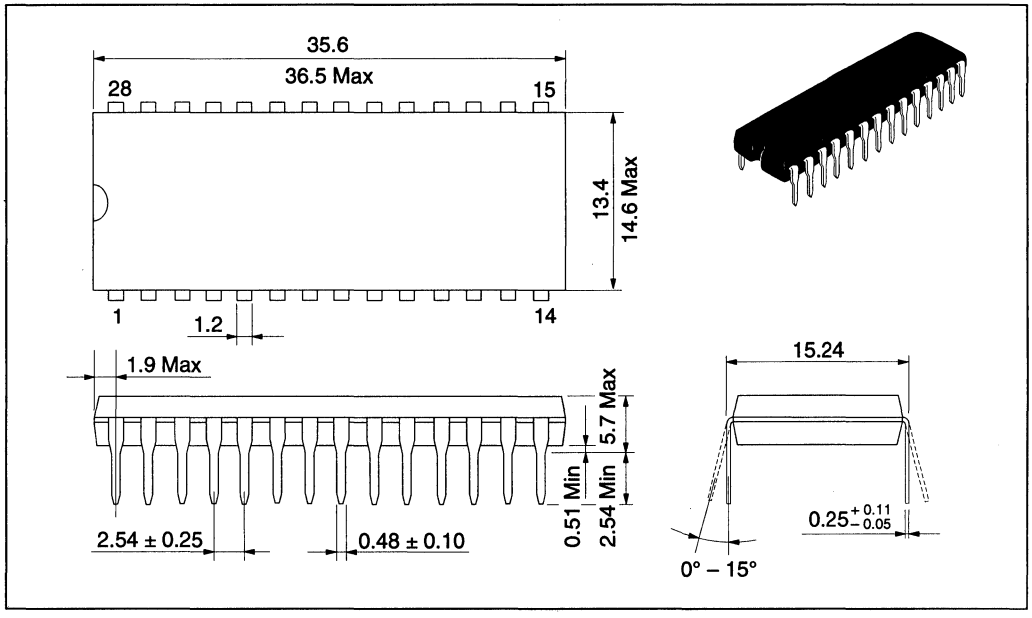
In addition, when V_{CC} is turned on or off, the input level of control pins must be held as shown in the table below.

$\overline{CE}$	V_{CC}	×	×
$\overline{OE}$	×	V_{SS}	×
$\overline{WE}$	×	×	V_{CC}

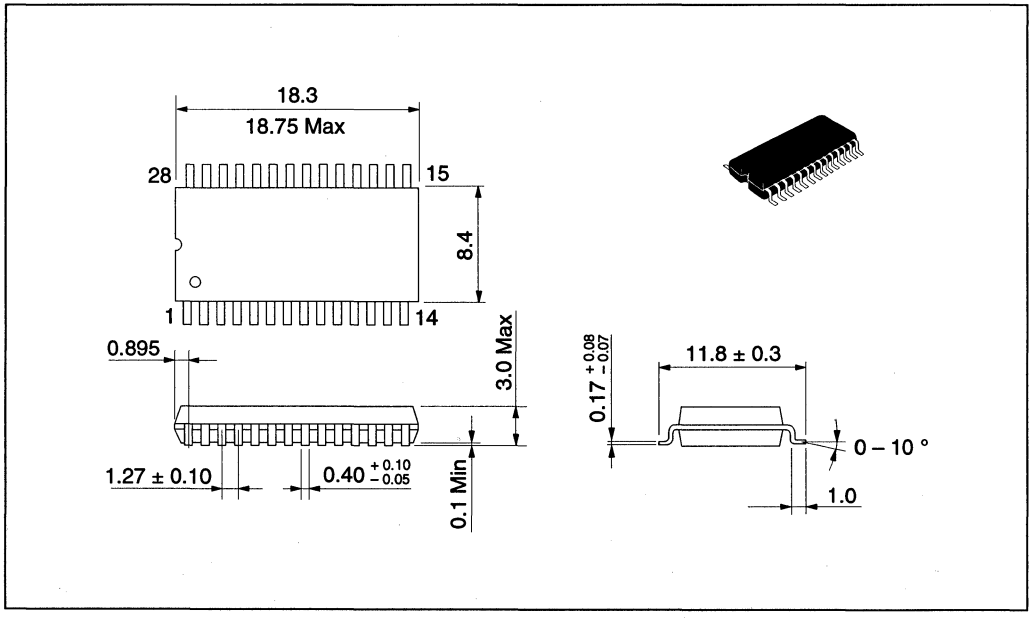
×: Don't care.
V_{CC}: Pull-up to V_{CC} level.
V_{SS}: Pull-down to V_{SS} level.

Package Dimensions

HN58C65PJ Series (DP-28) **Unit : mm**



HN58C65FPI Series (FP-28DA) **Unit : mm**



HN58C66 Series

8,192-word × 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

Rev. 6.0
April 12, 1995

The Hitachi HN58C66 is an electrically erasable and programmable ROM organized as 8,192-word × 8-bit. It realizes high speed, low power consumption, and a high level of reliability, employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 32-byte page programming function to make its erase and write operations faster.

Features

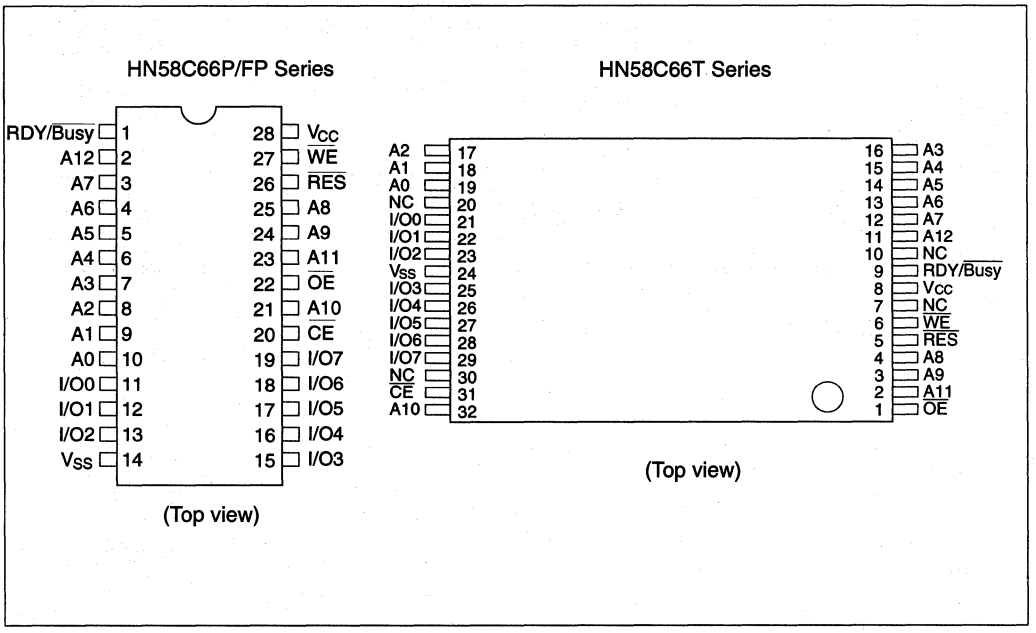
- Single 5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (32 bytes): 10 ms max
- Fast access time: 250 ns max
- Low power dissipation:
  - 20 mW/MHz typ (active)
  - 2.0 mW typ (standby)
- $\overline{Data}$ polling, RDY/$\overline{Busy}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5 erase/write cycles (in page mode)
- 10 years data retention
- Write protection by $\overline{RES}$ pin

Ordering Information

Type no.	Access time	Package
HN58C66P-25	250 ns	600 mil 28-pin plastic DIP (DP-28)
HN58C66FP-25	250 ns	28-pin *1 plastic SOP (FP-28D/DA)
HN58C66T-25	250 ns	32-pin plastic TSOP (TFP-32DA)

Notes: 1. T is added to the end of Type No. for a SOP of 3.00 mm (max) thickness.

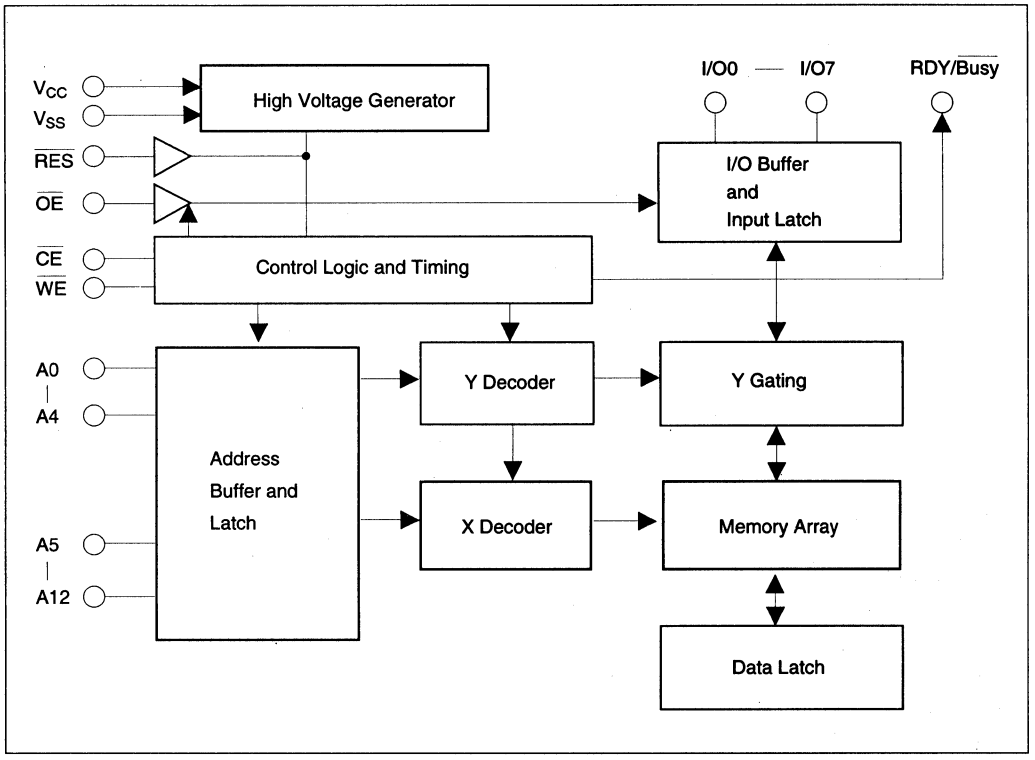
Pin Arrangement



Pin Description

Pin name	Function
A0–A12	Address inputs
I/O0–I/O7	Data Input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power (+5 V)
V_{SS}	Ground
$\overline{RES}$	Reset
NC	No connection
RDY/$\overline{Busy}$	Ready /$\overline{Busy}$

Block Diagram



Mode Selection

Pin Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	RDY/$\overline{Busy}$	$\overline{RES}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	High-Z	V_H*1	Dout
Standby	V_{IH}	×*2	×	High-Z	×	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	High-Z to V_{OL}	V_H	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	High-Z	V_H	High-Z
Write inhibit	×	×	V_{IH}	High-Z	×	—
	×	V_{IL}	×			
$\overline{Data}$ polling	V_{IL}	V_{IL}	V_{IH}	V_{OL}	V_H	Data out (I/O7)
Program reset	×	×	×	High-Z	V_{IL}	High-Z

Note: 1. Refer to the recommended DC operating condition.
2. × = Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage *1	V_{CC}	–0.6 to +7.0	V
Input voltage *1	Vin	–0.5*2 to +7.0	V
Operationg temperature range *3	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. With respect to V_{SS}
2. Vin min = –3.0 V for pulse width ≤ 50 ns
3. Including electrical characteristics and data retention

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IL}	–0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC} + 1.0	V
	V_H	V_{CC} – 0.5	—	V_{CC} + 1.0	V
Operating temperature	Topr	0	—	70	°C

DC Characteristics (Ta=0 to +70°C, V_{CC} = 5.0 V ± 10 %)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2*1	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	1	mA	$\overline{CE}$ = V_{IH}, $\overline{CE}$ = V_{CC}
V_{CC} current (active)	I_{CC2}	—	—	8	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 5.5 V
		—	—	25	mA	Iout = 0 mA, Duty = 100%, Cycle = 250 ns at V_{CC} = 5.5 V
Input low voltage	V_{IL}	–0.3*2	—	0.8	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} + 1.0	V	
	V_H	V_{CC}–0.5	—	V_{CC} + 1.0	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Note: 1. I_{LI} on $\overline{RES}$ = 100 µA max
2. V_{IL} min = –1.0 V for pulse width ≤ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin*1	—	—	6	pF	Vin = 0 V
Output capacitance	Cout*1	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5.0 V ± 10 %)

Test Conditions

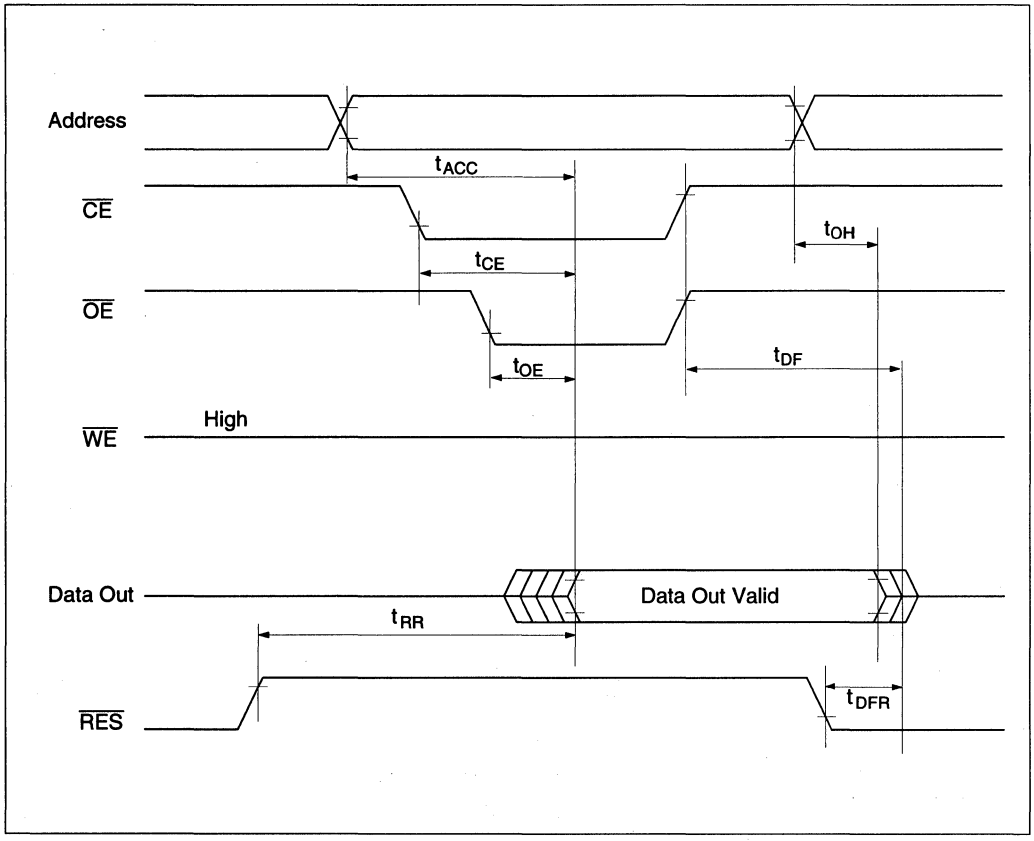
- Input pulse levels : 0.4 V to 2.4 V
  0V to V_{CC} ($\overline{RES}$ pin)
- Input rise and fall time : ≤ 20 ns
- Output load : 1TTL Gate +100 pF
- Reference levels for measuring timing : 0.8 V, 2.0 V

Read Cycle

Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	250	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	100	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float*1	t_{DF}	0	90	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ low to output float*1	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Data output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay	t_{RR}	0	450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF}, t_{DFR} are defined at which the outputs achieve the open circuit conditions and are no longer driven.

Read Timing Waveform

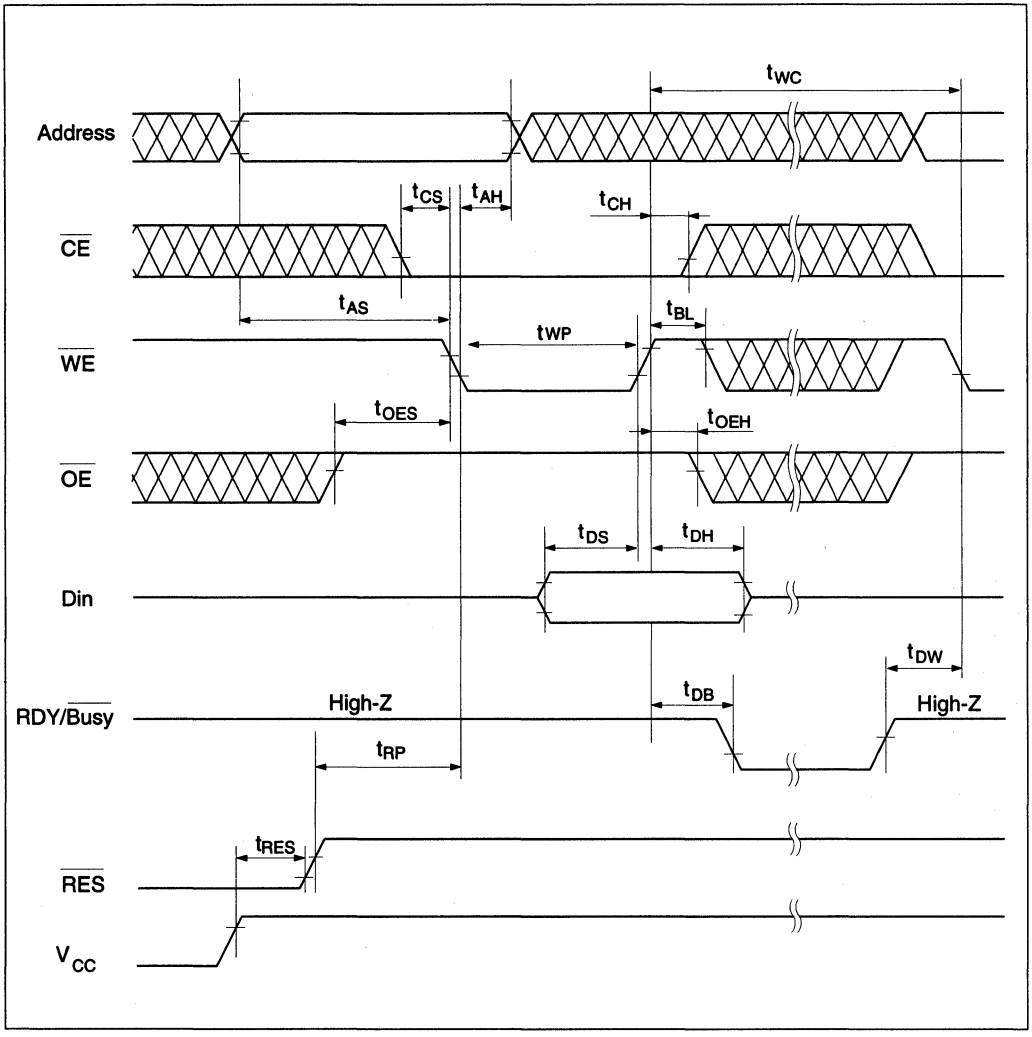


Write Cycle

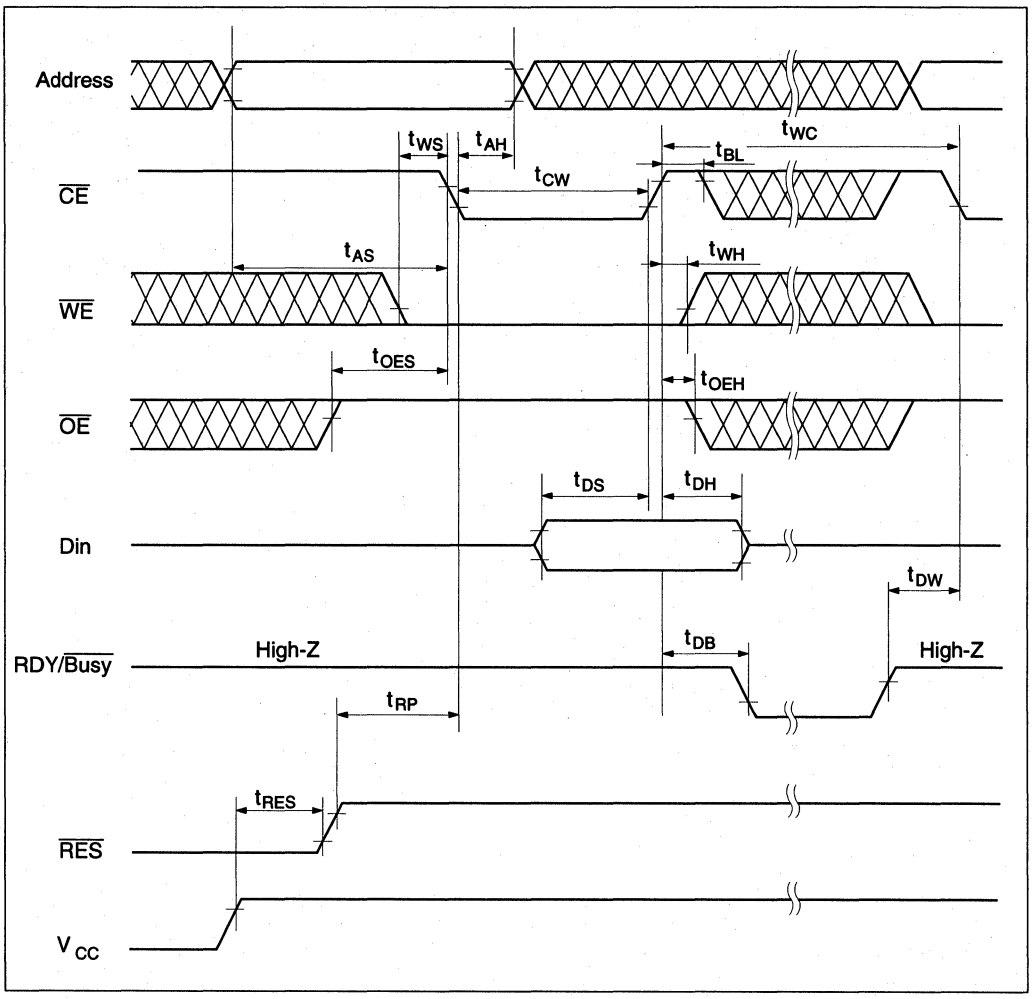
Parameter	Symbol	Min*1	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	20	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	200	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	200	—	—	ns	
Data latch time	t_{DL}	100	—	—	ns	
Byte load cycle	t_{BLC}	0.30	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*2	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	150*3	—	—	ns	
Reset protect time	t_{RP}	100	—	—	µs	
Reset high time	t_{RES}	1	—	—	µs	

Note: 1. Use this device in longer cycle than this value.
2. t_{WC} must be longer than this value unless polling technique or RDY/$\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.
3. Next read or write operation can be initiated after t_{DW} if polling technique or RDY/$\overline{Busy}$ are used.

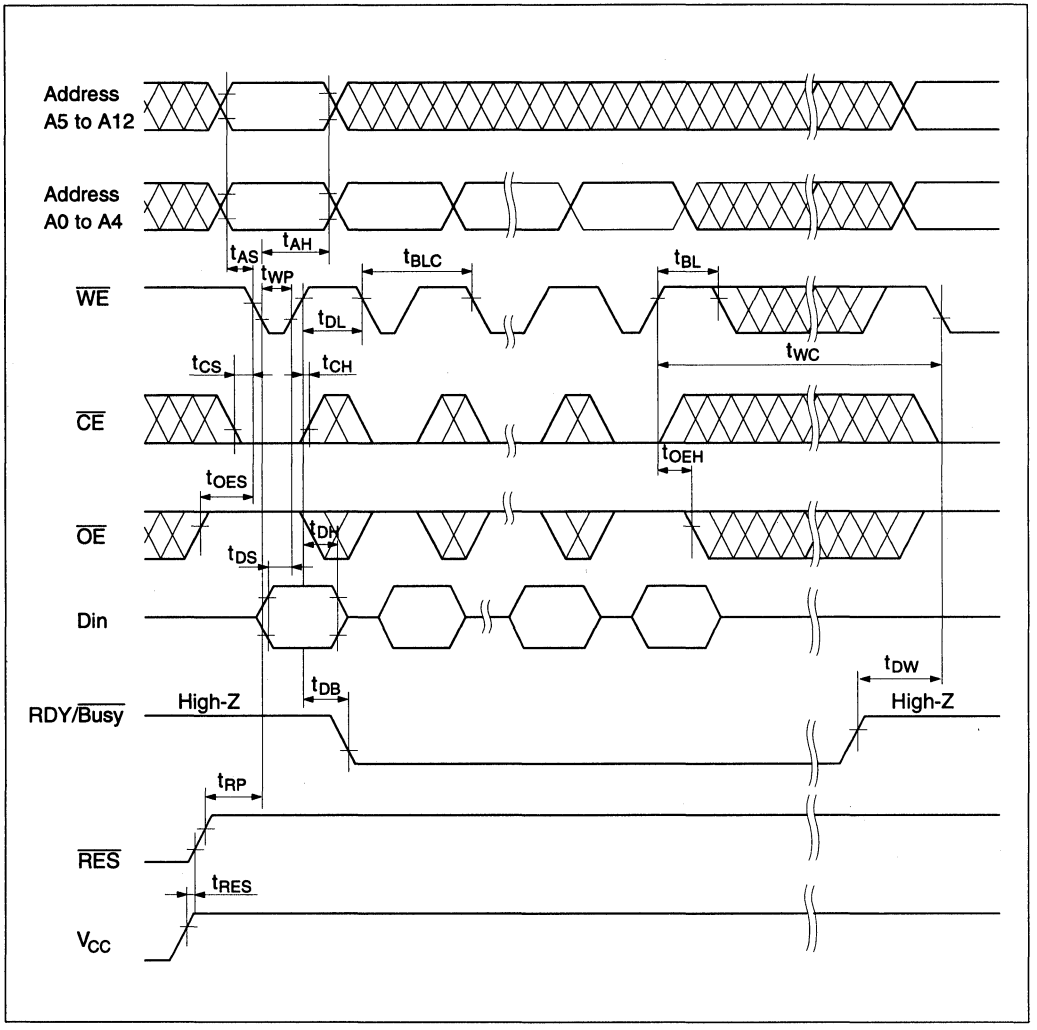
Byte Write Timing Waveform(1) ($\overline{WE}$ Controlled)



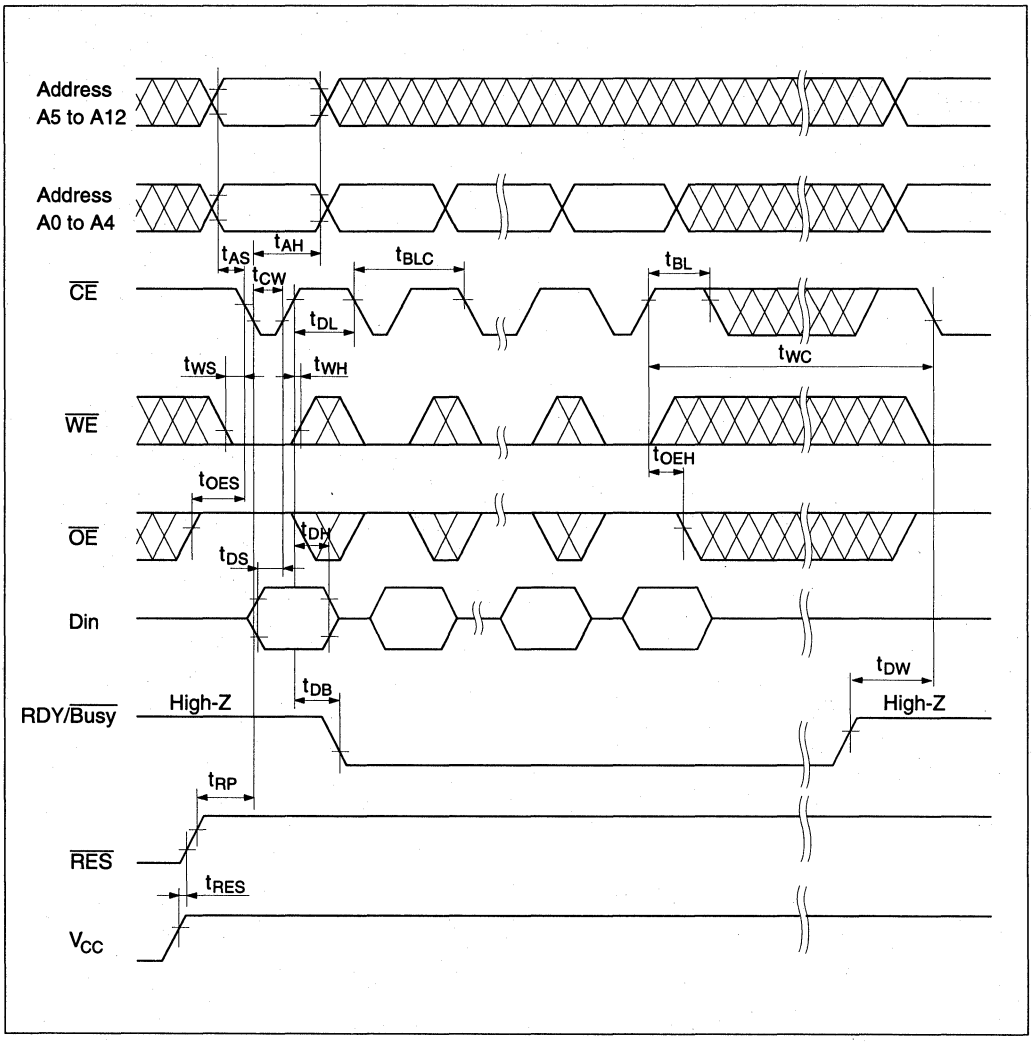
Byte Write Timing Waveform(2) ($\overline{CE}$ Controlled)



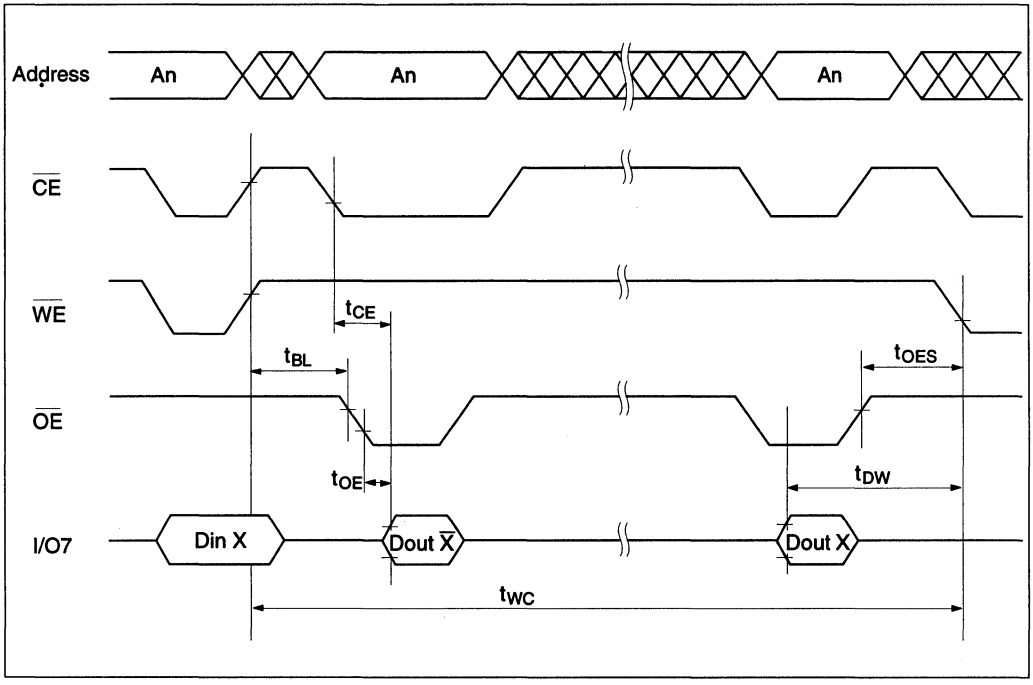
Page Write Timing Waveform (1)($\overline{WE}$ Controlled)



Page Write Timing Waveform (2)($\overline{CE}$ Controlled)



$\overline{\text{Data}}$ Polling Timing Waveform



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 31 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{\text{Data}}$ Polling

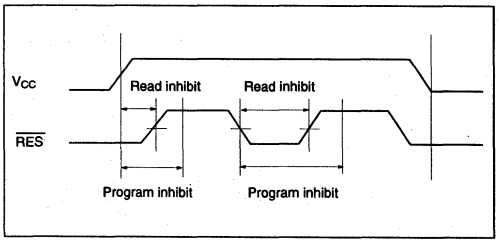
$\overline{\text{Data}}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{\text{Busy}}$ Signal

RDY/$\overline{\text{Busy}}$ signal also allows the status of the EEPROM to be determined. The RDY/$\overline{\text{Busy}}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{\text{Busy}}$ signal changes state to high impedance.

$\overline{\text{RES}}$ Signal

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it dosen't provide a latch function.



$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

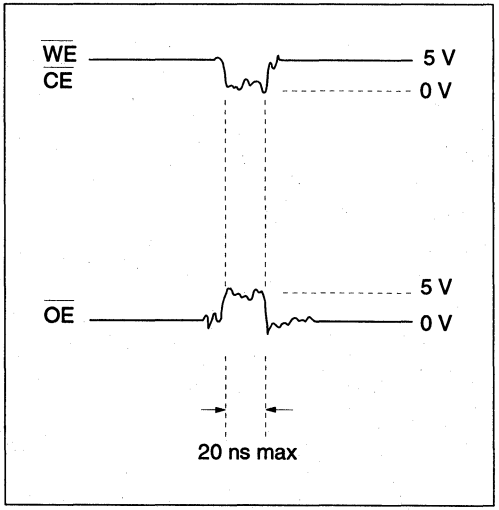
Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 3×10^3 cycles in case of byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

Data Protection

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

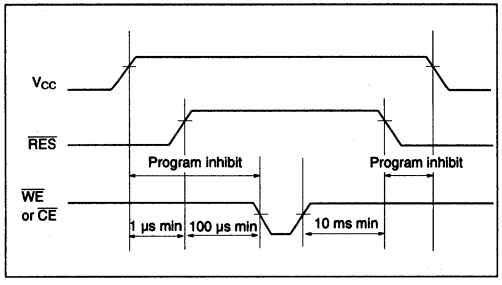
During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.
To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less in program mode.
Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data Protection at V_{CC} On/Off

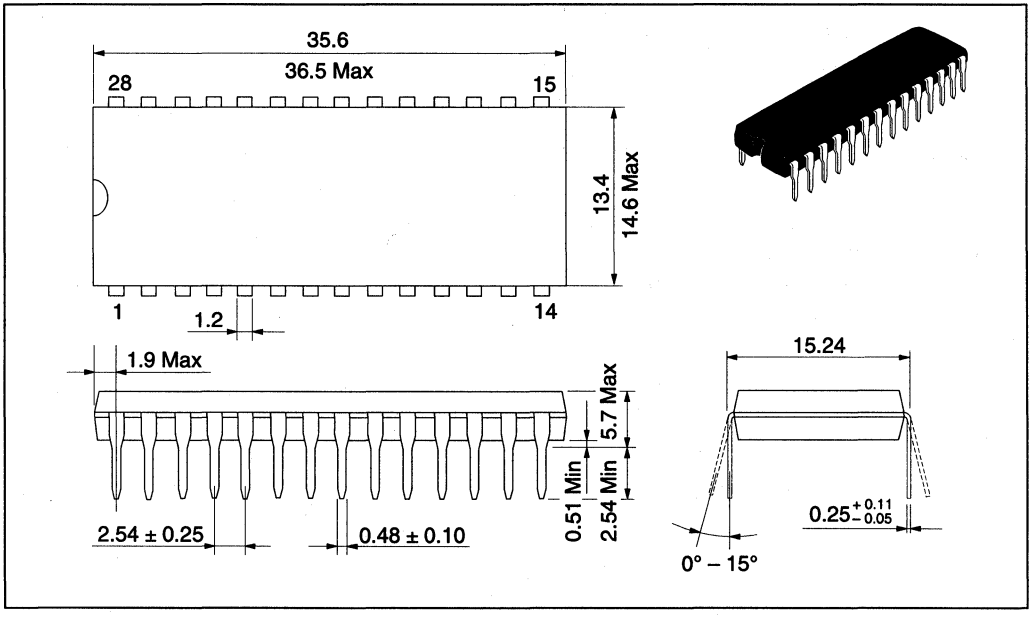
When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in unprogrammable state by using a CPU reset signal to $\overline{RES}$ pin. $\overline{RES}$ pin should be kept at V_{SS} level when V_{CC} is turned on or off.

The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.

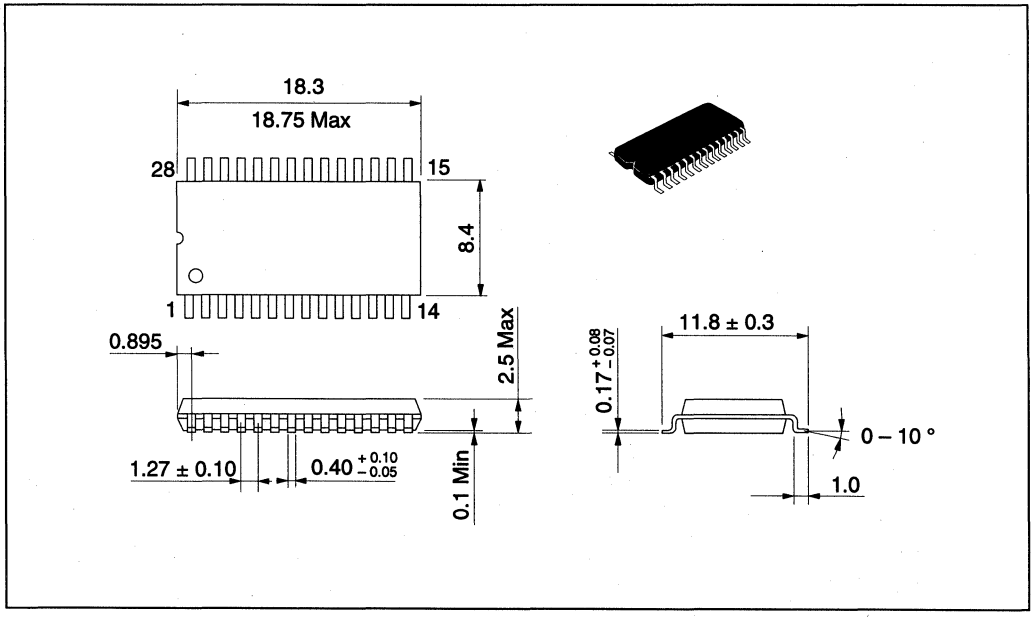


Package Dimensions

HN58C66P Series (DP-28) **Unit : mm**

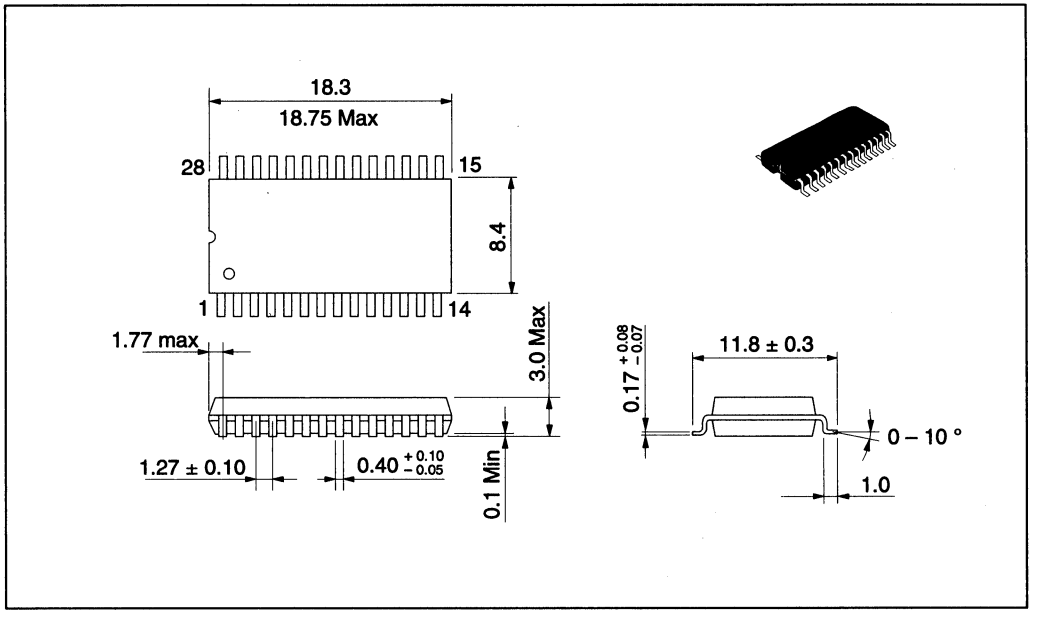


HN58C66FP Series (FP-28D) **Unit : mm**

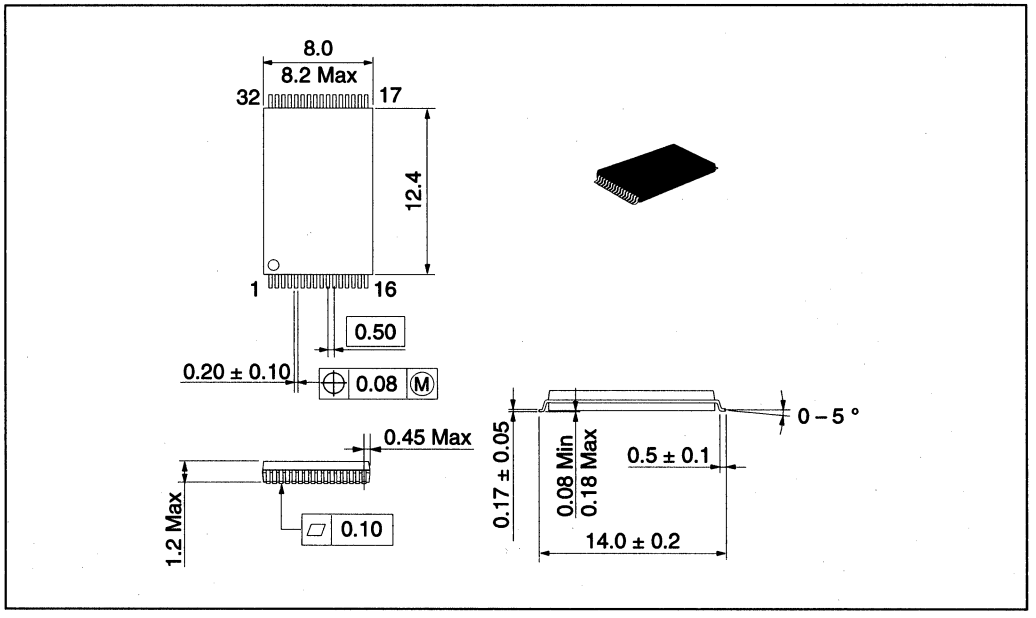


Package Dimensions (cont)

HN58C66FP Series (FP-28DA) **Unit : mm**



HN58C66T Series (TFP-32DA) **Unit : mm**



256K EEPROM

ADE-203-410 (Z)

HN58C256A / HN58C257A Series

32,768-word × 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

Preliminary
Rev. 0.0
June 19, 1995

The Hitachi HN58C256A and HN58C257A are electrically erasable and programmable EEPROMs organized as 32,768-word × 8-bit and employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

Features

- Single 5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (64 bytes): 10 ms max
- Fast access time: 85/100 ns max
- Low power dissipation: 20 mW/MHz, typ (active)
  110 µW max (standby)
- Ready/$\overline{Busy}$ (♦)*1
- $\overline{Data}$ polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{RES}$ pin (♦)*1

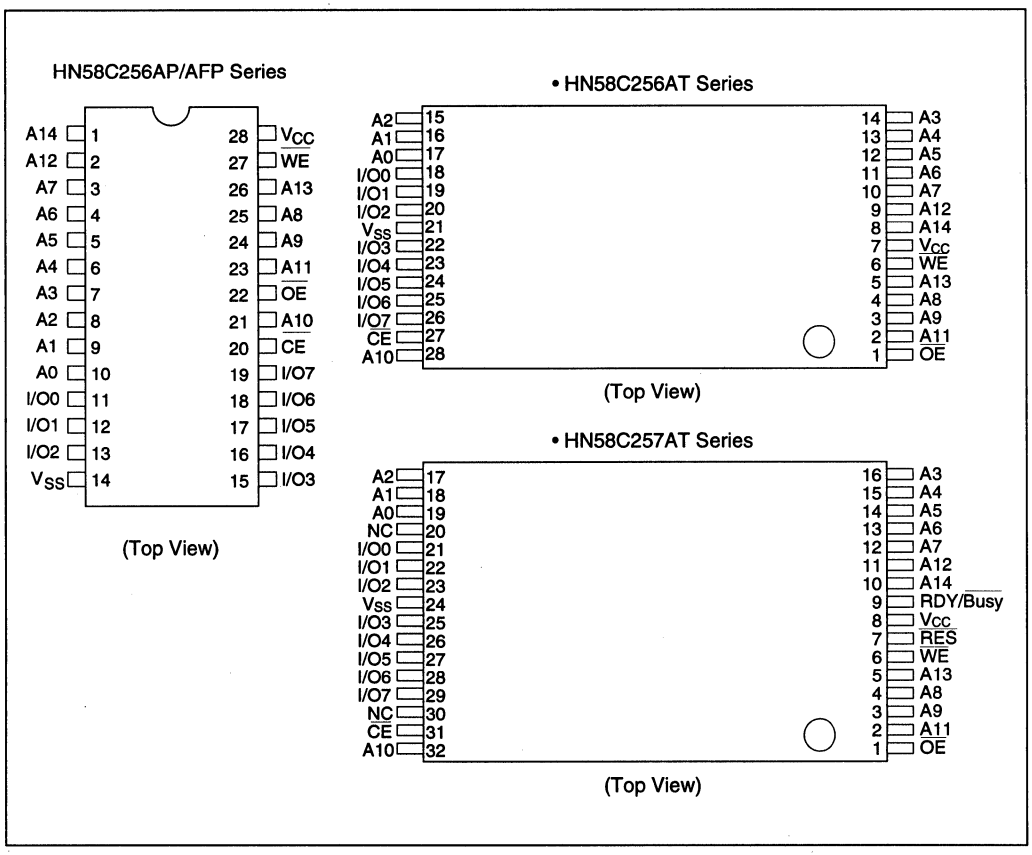
Notes: 1. All through this datasheet, the mark (♦) indicates the function supported by only the HN58C257A series (32 pin package).

Ordering Information

Type No.	Compatible Type No.*1	Operating Voltage	Temperature Range	Access Time	Package
HN58C256AP-85 HN58C256AP-10	HN58C256P-20	4.5 to 5.5 V	0 to 70°C	85 ns 100 ns	600 mil 28-pin plastic DIP(DP-28)
HN58C256AFP-85 HN58C256AFP-10	HN58C256FP-20	4.5 to 5.5V	0 to 70°C	85 ns 100 ns	400 mil 28-pin plastic SOP (FP-28D)
HN58C256AT-85 HN58C256AT-10		4.5 to 5.5 V	0 to 70°C	85 ns 100 ns	28-pin plastic TSOP (TFP-28DB)
HN58C257AT-85 HN58C257AT-10	HN58C257T-20	4.5 to 5.5 V	0 to 70°C	85 ns 100 ns	8 × 14 mm 32-pin plastic TSOP (TFP-32DA)

Notes: 1. This type No. can be replaced by the corresponding A–version. (ex. HN58C256P to HN58C256AP)

Pin Arrangement

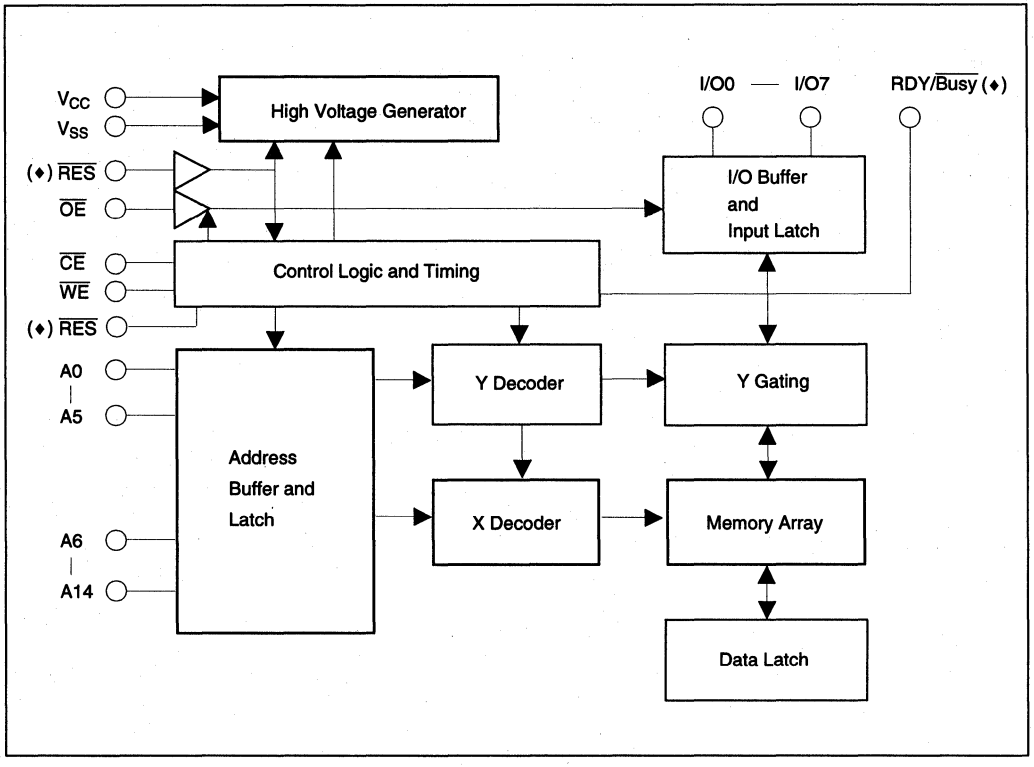


Pin Description

Pin name	Function
A0 to A14	Address inputs
I/O0 to I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable

Pin name	Function
$\overline{WE}$	Write enable
V_{CC}	Power (+ 5.0 V)
V_{SS}	Ground
RDY/$\overline{Busy}$ (♦)	Ready busy
$\overline{RES}$ (♦)	Reset

Block Diagram



Mode Selection

Pin Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$ (♦)	RDY/$\overline{Busy}$ (♦)	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H*1	High-Z	Dout
Standby	V_{IH}	×*2	×	×	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	×	×	V_{IH}	×	—	—
	×	V_{IL}	×	×	—	—
Data Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data out (I/O7)
Program reset	×	×	×	V_{IL}	High-Z	High-Z

Note: 1. Refer to the recommended DC operating condition.
2. ×: Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage *1	V_{CC}	–0.6 to +7.0	V
Input voltage *1	Vin	–0.5*2 to +7.0	V
Operating temperature range *3	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. With respect to V_{SS}.
2. Vin min : –3.0 V for pulse width ≤ 50 ns.
3. Including electrical characteristics and data retention.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IL}	–0.3*1	—	0.6	V
	V_{IH}	3.0	—	V_{CC} + 0.3*2	V
	$V_{H}(\blacklozenge)$	V_{CC} – 0.5	—	V_{CC} + 1.0	V
Operating temperature	Topr	0	—	70	°C

Notes: 1. V_{IL} min: –1.0 V for pulse width ≤ 50 ns.
2. V_{IH} max: V_{CC} + 1.0 V for pulse width ≤ 50 ns.

DC Characteristics

Supply voltage range (V_{CC}), temperature range (Topr) and input voltage ($V_{IH}/V_{IL}/V_H$) are referred to the table of Recommended DC Operating Conditions.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2*1	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
V_{CC} current (active)	I_{CC3}	—	—	12	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 5.5 V
		—	—	30	mA	Iout = 0 mA, Duty = 100%, Cycle = 85 ns at V_{CC} = 5.5 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	V_{CC} × 0.8	—	—	V	I_{OH} = –400 µA

Note: 1. I_{LI} on $\overline{RES}$: 100 µA max (♦)

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin*1	—	—	6	pF	Vin = 0 V
Output capacitance	Cout*1	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics

Supply voltage (V_{CC}) and temperature range (Topr) are referred to the table of 'Recommended DC Operating Conditions'.

Test Conditions

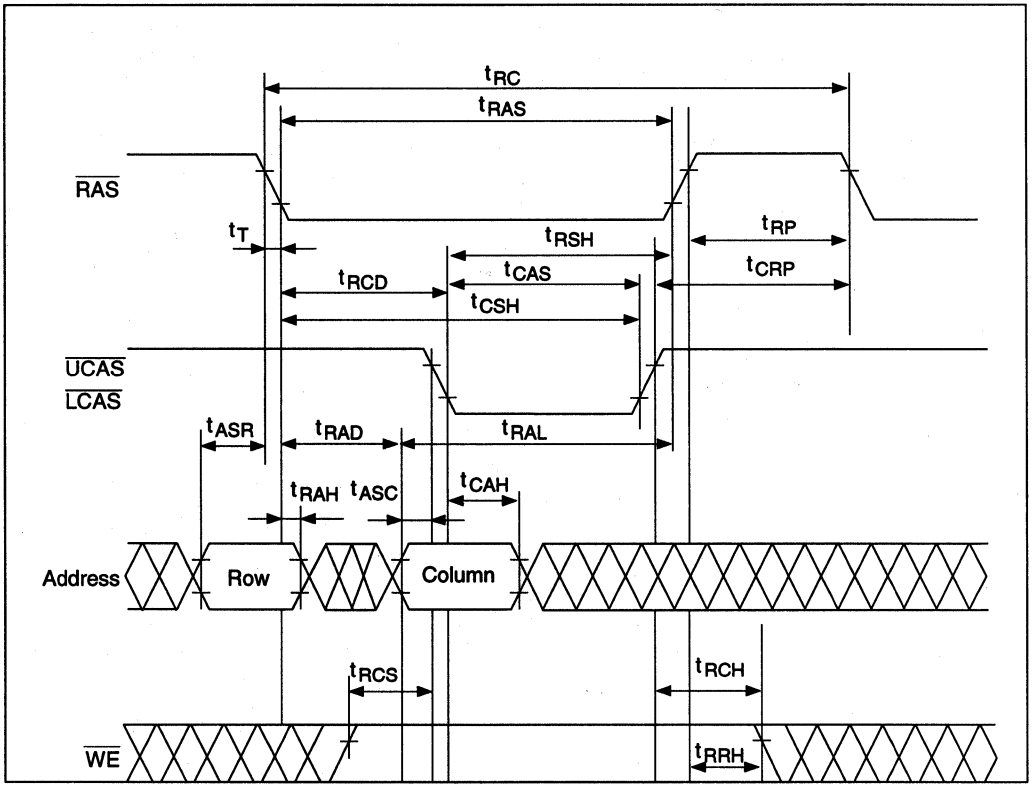
- Input pulse levels : 0 V to 3.0 V
  0 V to V_{CC} ($\overline{RES}$ pin)
- Input rise and fall time : ≤ 20 ns
- Input timing reference levels : 0.8, 2.0 V
- Output load : 1TTL Gate +100 pF
- Output reference levels : 1.5 V, 1.5 V

Read Cycle

		HN58C256A, HM58C257A					
		-85		-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test conditions**
Address to output delay	t_{ACC}	—	85	—	100	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	85	—	100	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	40	10	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float*1	t_{DF}	0	40	0	40	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ low to output float*1(♦)	t_{DFR}	0	350	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay(♦)	t_{RR}	0	450	0	450	ns	$\overline{CE}$ = $\overline{OE}$= V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.

Read Timing Waveform



Write Cycle

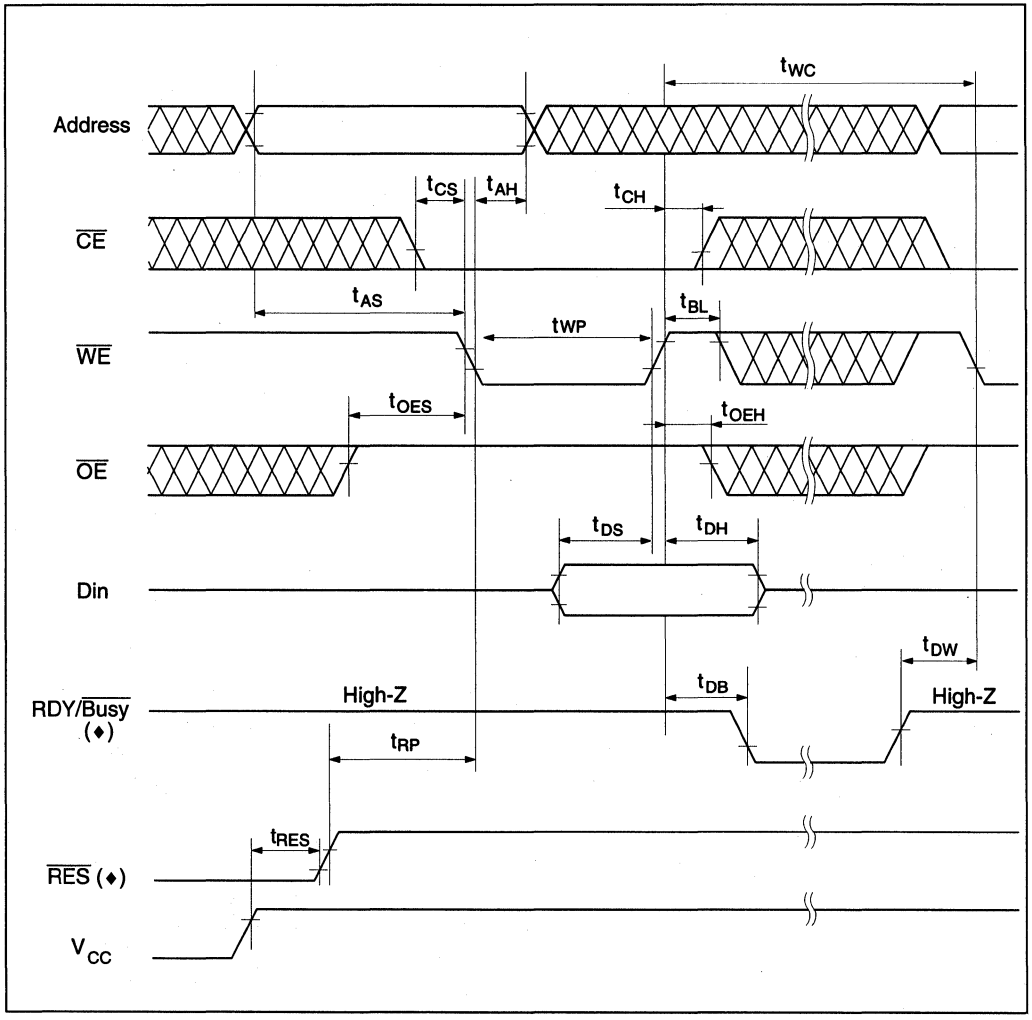
Parameter	Symbol	Min[*1]	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	50	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	50	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	100	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	100	—	—	ns	
Data latch time	t_{DL}	50	—	—	ns	
Byte load cycle	t_{BLC}	0.2	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10[*2]	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	0[*3]	—	—	ns	
Reset protect time (♦)	t_{RP}	100	—	—	µs	
Reset low time (♦)	t_{RES}	1	—	—	µs	

Note: 1. Use this device in longer cycle than this value.

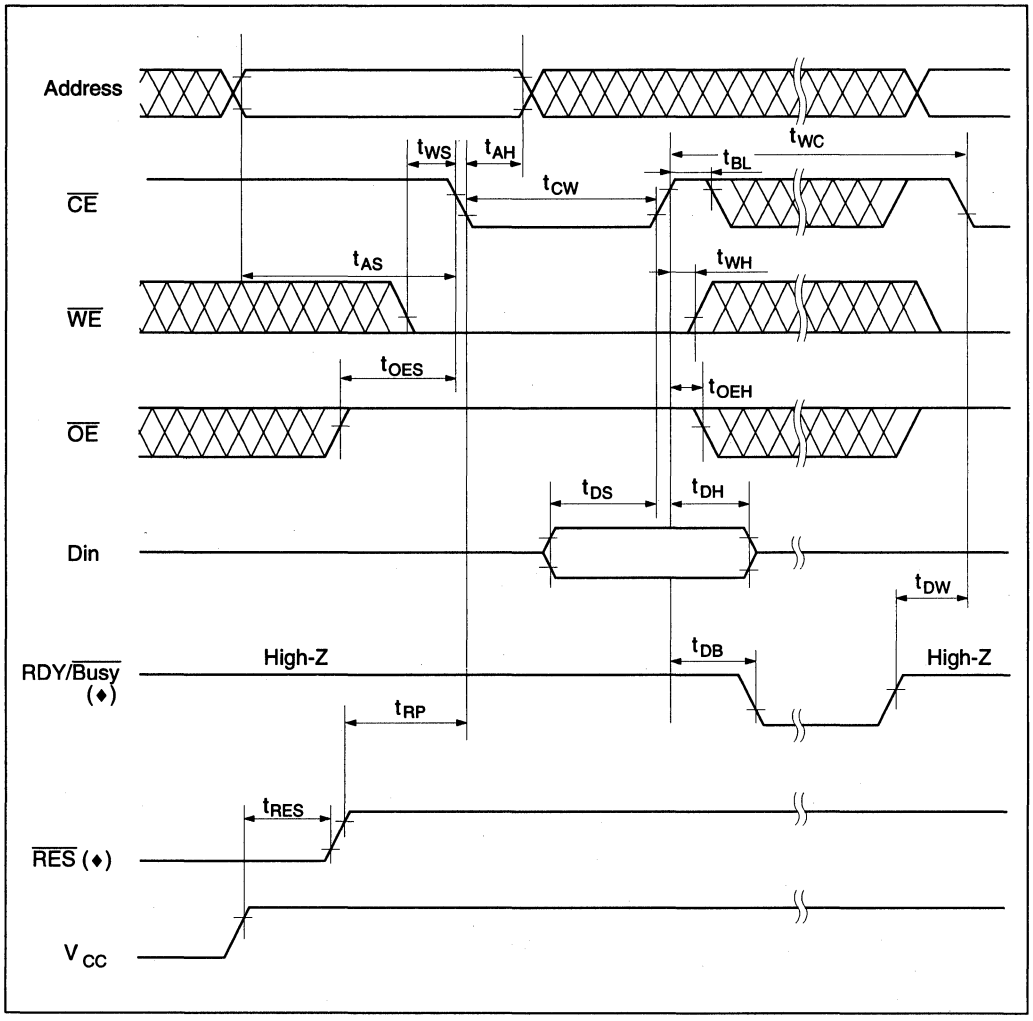
2. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{Busy}$ (♦) are used. This device automatically completes the internal write operation within this value.

3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{Busy}$ (♦) are used.

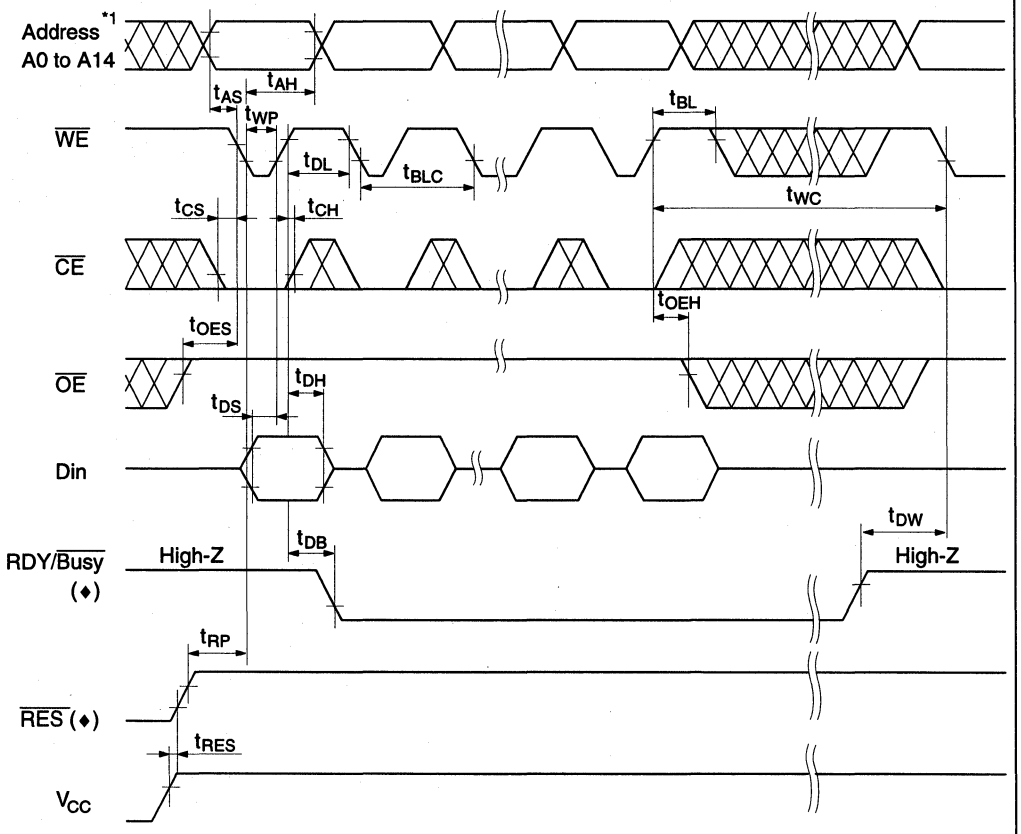
Byte Write Timing Waveform(1) ($\overline{WE}$ Controlled)



Byte Write Timing Waveform(2) ($\overline{CE}$ Controlled)

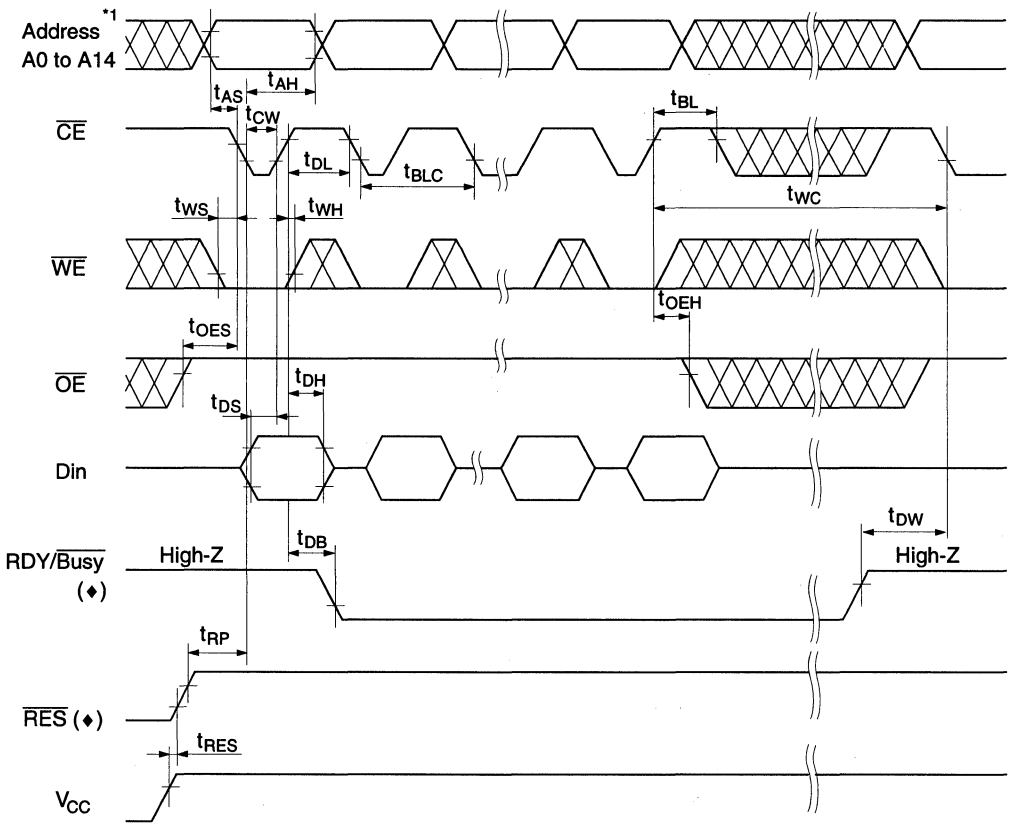


Page Write Timing Waveform(1) ($\overline{WE}$ Controlled)



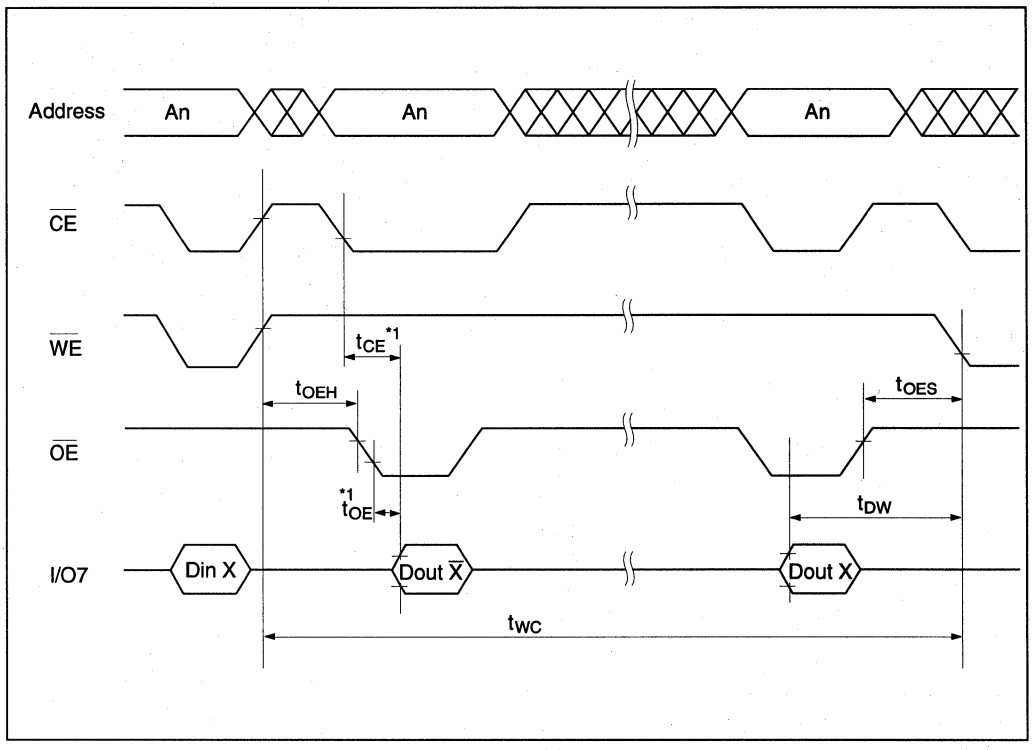
Note: 1. A6 through A14 are page address and these address are latched at the first falling edge of $\overline{WE}$

Page Write Timing Waveform(2) ($\overline{CE}$ Controlled)



Note: 1. A6 through A14 are page address and these address are latched at the first falling edge of $\overline{CE}$

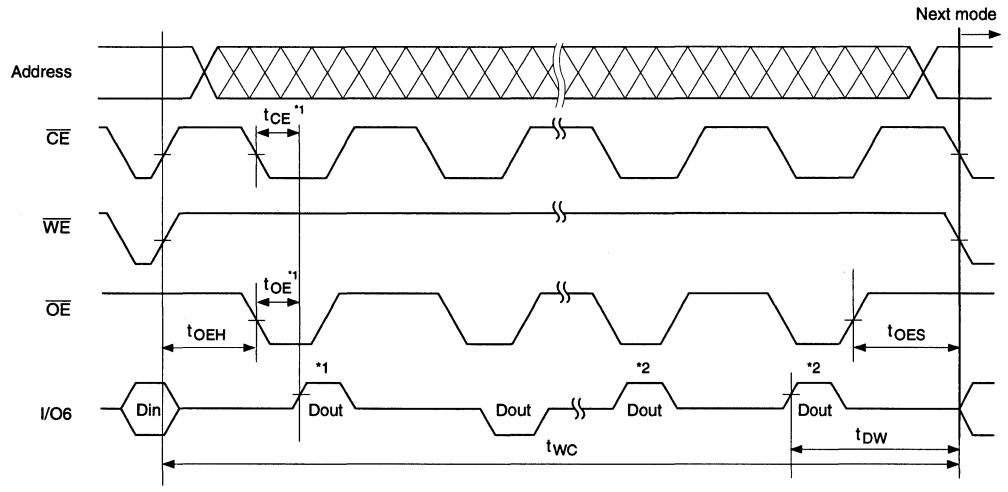
$\overline{\text{Data}}$ Polling Timing Wavefome



Toggle bit

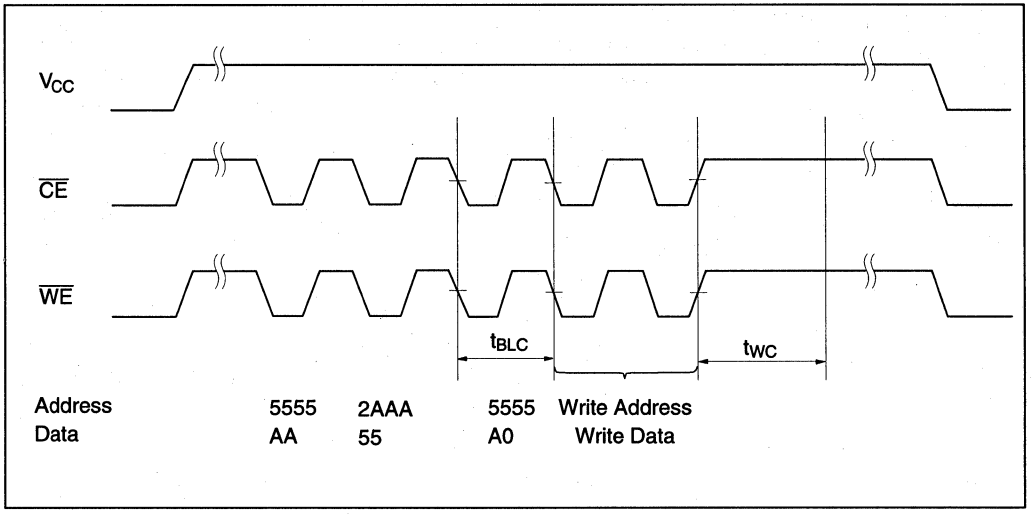
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle bit Wavefome

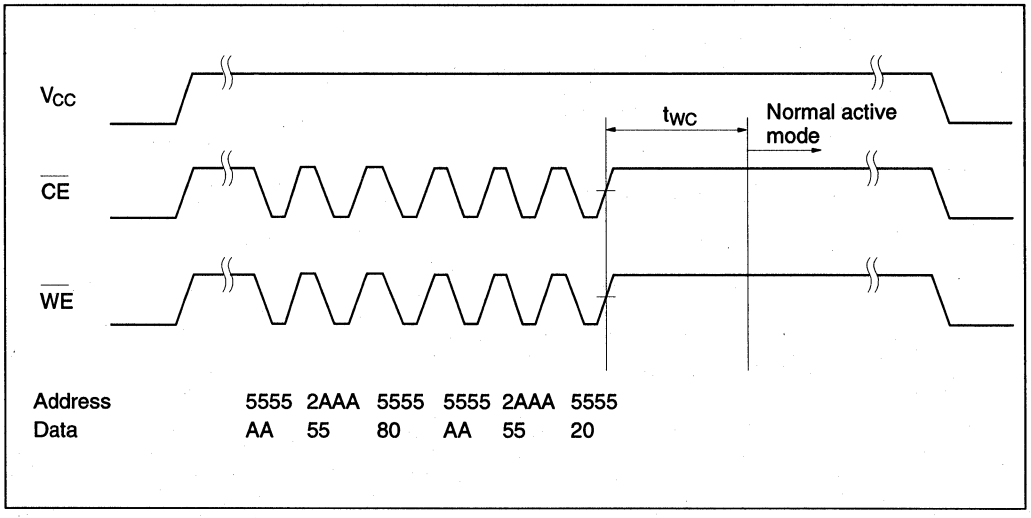


Notes: 1. I/O6 biginning state is "1".
2. I/O7 ending state will vary.
3. See AC read characteristics.

Software Data Protection Timing Waveform(1) (in protection mode)



Software Data Protection Timing Waveform(2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is kept high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{Data}$ Polling

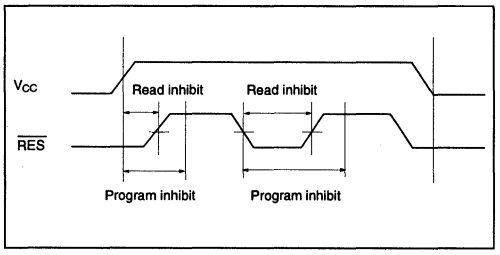
$\overline{Data}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{Busy}$ Signal (♦)

RDY/$\overline{Busy}$ signal also allows status of the EEPROM to be determined. The RDY/$\overline{Busy}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{Busy}$ signal changes state to high impedance.

$\overline{RES}$ Signal (♦)

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it doesn't provide a latch function.



$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

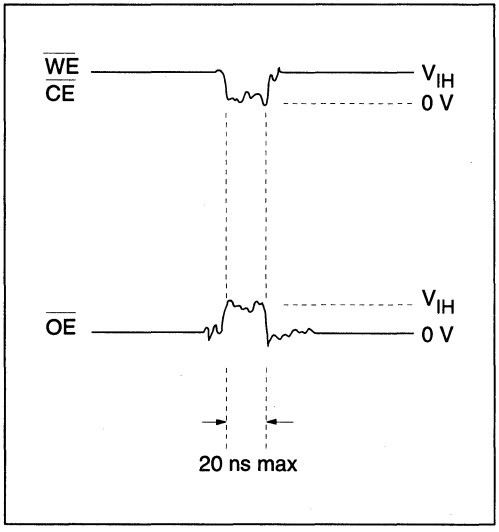
Data Protection

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

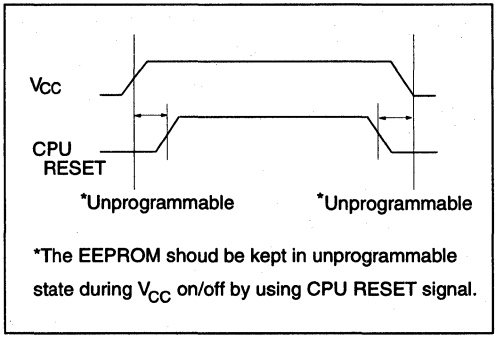
To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less in programming mode.

Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.



(1)Protection by $\overline{CE}$, $\overline{OE}$, $\overline{WE}$

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

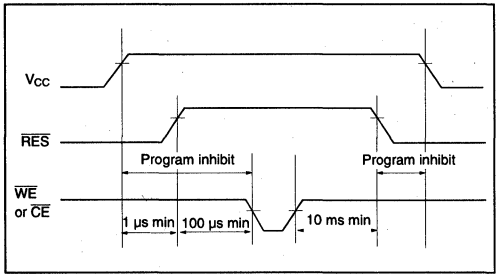
$\overline{CE}$	V_{CC}	×	×
$\overline{OE}$	×	V_{SS}	×
$\overline{WE}$	×	×	V_{CC}

×: Don't care.
V_{CC}: Pull-up to V_{CC} level.
V_{SS}: Pull-down to V_{SS} level.

(2) Protection by $\overline{RES}$ (♦)

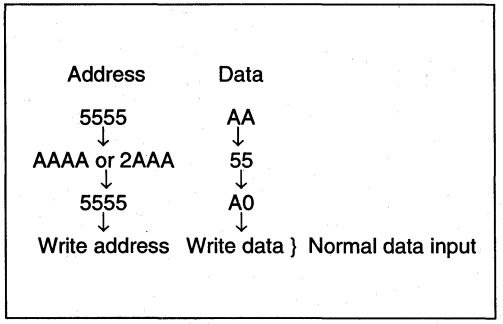
The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's $\overline{RES}$ pin. $\overline{RES}$ should be kept VSS level during V_{CC} on/off.

The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.

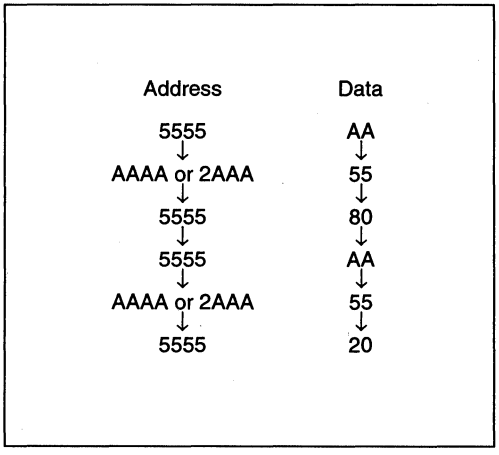


3. Software data protection

To prevent unintentional programming caused by noise generated by external circuits, This device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode.



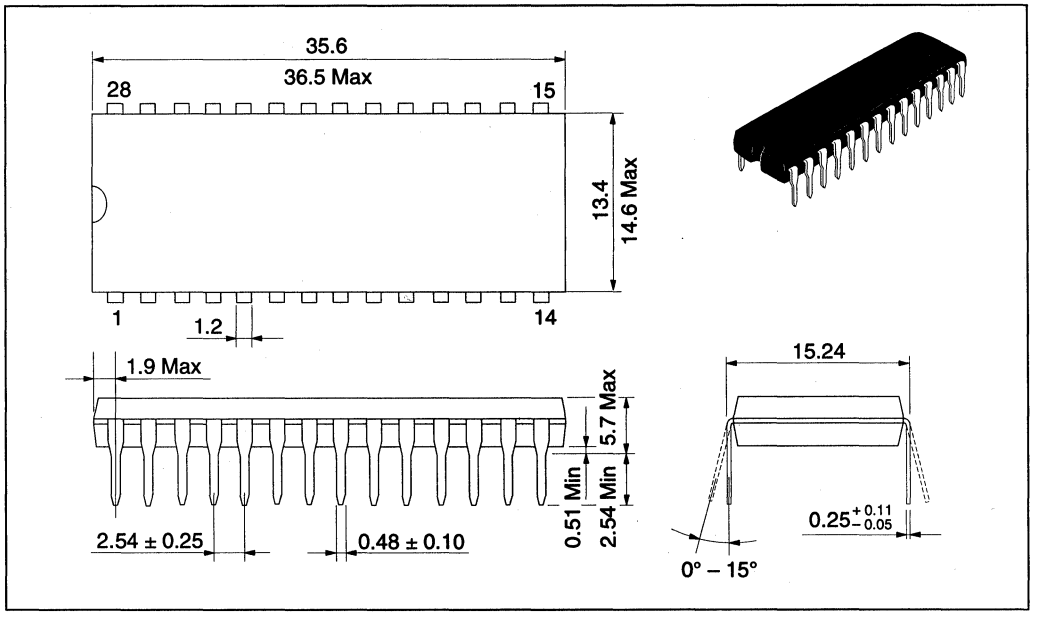
Software data protection mode can be canceled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the canceling cycle, the data cannot be written.



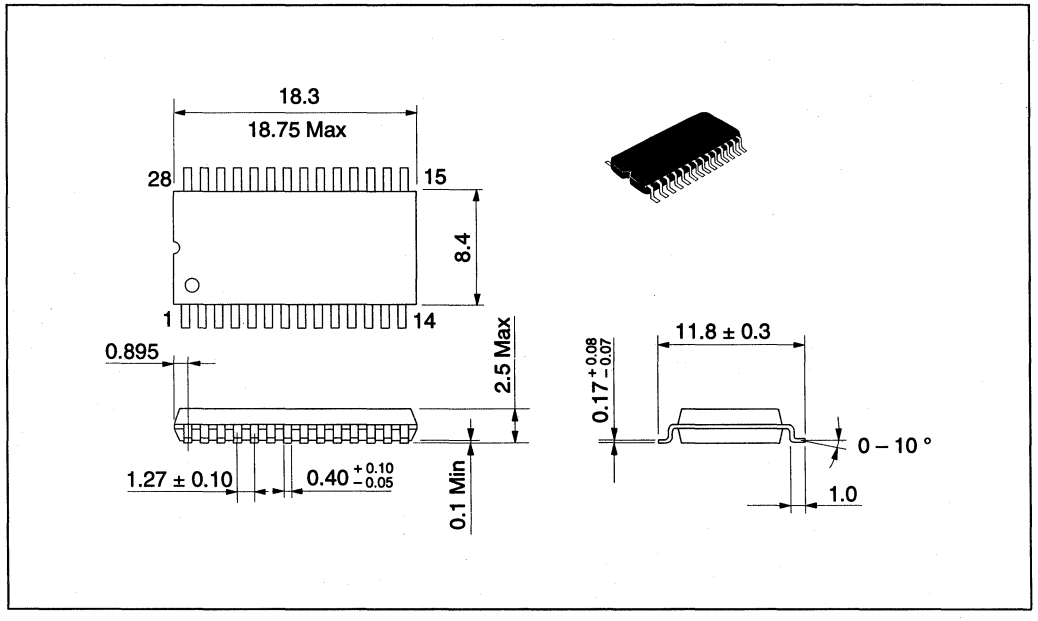
The software data protection is not enabled at the shipment.

Package Dimensions

HN58C256AP Series (DP-28) **Unit : mm**

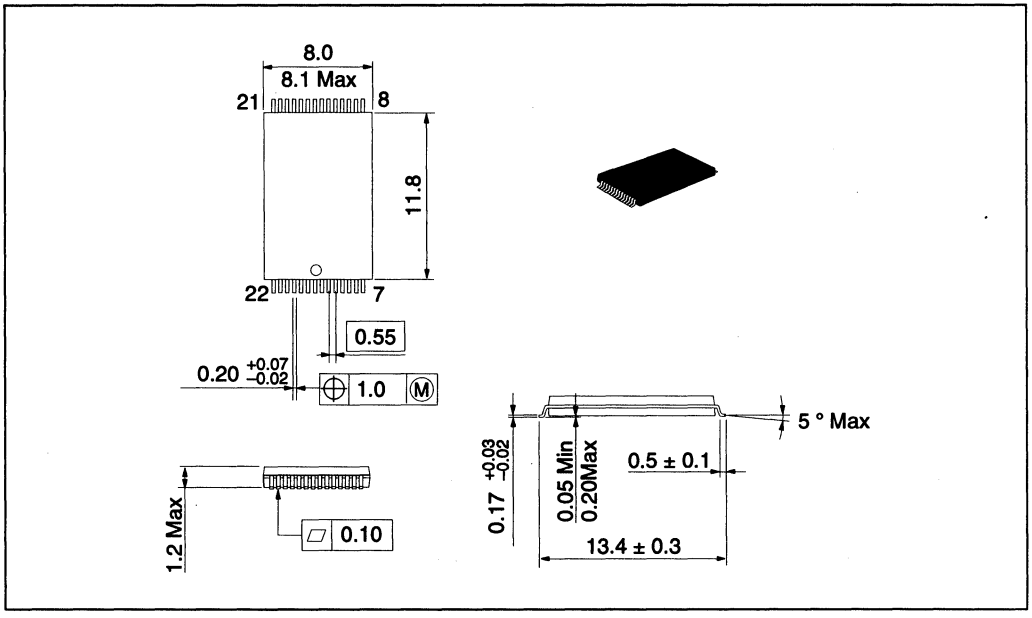


HN58C256AFP Series (FP-28D) **Unit : mm**

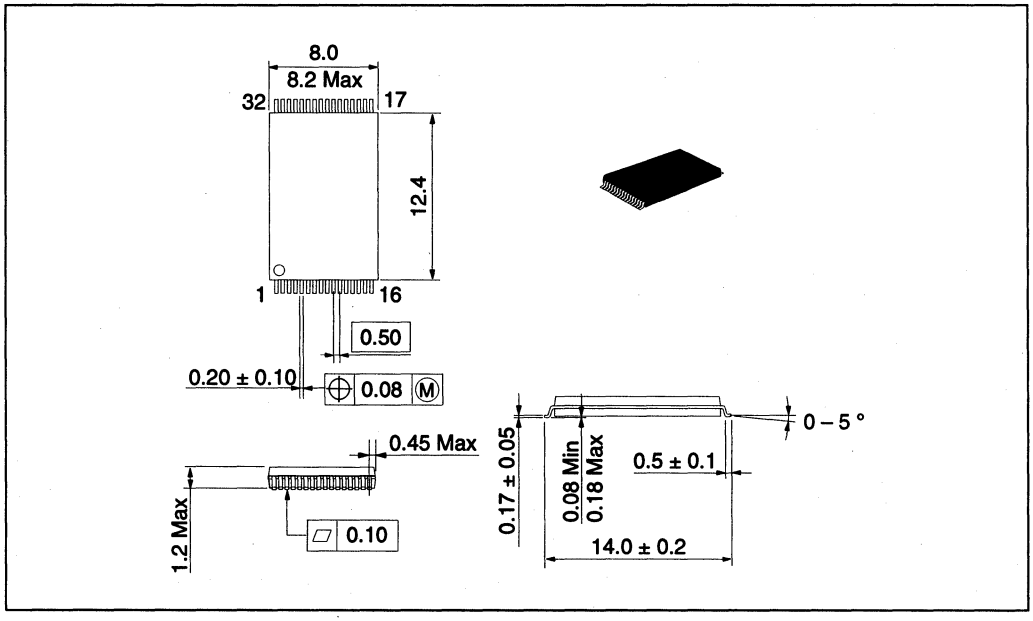


Package Dimensions (cont)

HN58C256AT Series (TFP-28DB) **Unit : mm**



HN58C257AT Series (TFP-32DA) **Unit : mm**



ADE-203-357A (Z)

HN58V256A / HN58V257A Series

32,768-word × 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

Preliminary
Rev. 0.1
August 7, 1995

The Hitachi HN58V256A and HN58V257A are electrically erasable and programmable EEPROMs organized as 32,768-word × 8-bit and employing advanced MNOS memory technology and CMOS process and circuitry technology. They also have a 64-byte page programming function to make their write operations faster.

Features

- Single 2.7 to 5.5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (64 bytes): 10 ms max
- Fast access time: 120 ns max
- Low power dissipation: 20 mW/MHz, (typ) (active)
  110 µW (max) (standby)
- $\overline{Ready/Busy}$ (♦)*1
- $\overline{Data}$ polling and Toggle bit
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^5erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{RES}$ pin (♦)*1

Notes: 1. All through this datasheet, the mark (♦) indicates the function supported by only the HN58V257A series (32 pin package).

Notes: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

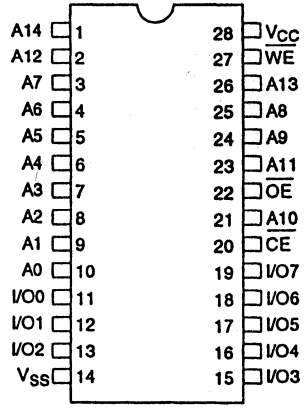
Ordering Information

Type No.	Compatible Type No.*1	Operating Voltage	Temperature Range	Access Time	Package
HN58V256AFP-12 HN58V256AFP-15		2.7 to 5.5V	0 to 70°C	120 ns 150 ns	400 mil 28-pin plastic SOP (FP-28D)
HN58V256AT-12 HN58V256AT-15		2.7 to 5.5 V	0 to 70°C	120 ns 150 ns	28-pin plasticTSOP (TFP-28DB)
HN58V257AT-12 HN58V257AT-15	HN58V257T-35	2.7 to 5.5 V	0 to 70°C	120 ns 150 ns	8 x 14 mm 32-pin plastic TSOP (TFP-32DA)

Notes: 1. This type No. can be replaced by the corresponding A-version. (ex. HN58C256P to HN58V256AP)

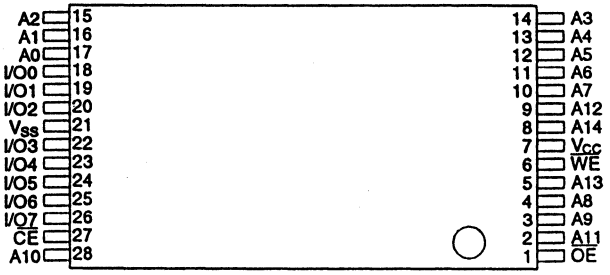
Pin Arrangement

HN58V256AFP Series



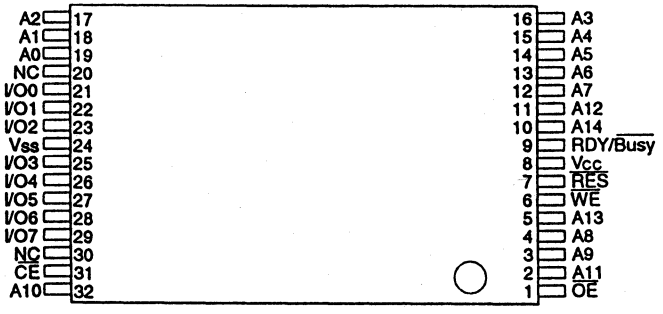
(Top View)

• HN58V256AT Series



(Top View)

• HN58V257AT Series

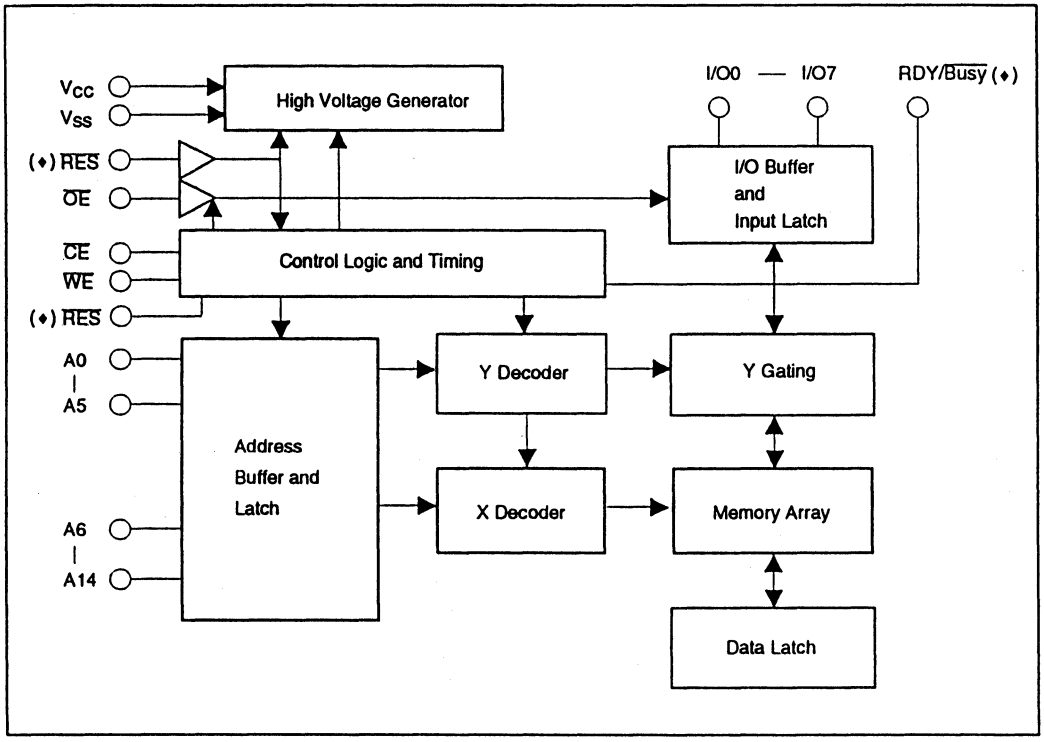


(Top View)

Pin Description

Pin name	Function
A0 to A14	Address inputs
I/O0 to I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
$\overline{WE}$	Write enable
V_{CC}	Power (+2.7 to 5.5 V)
V_{SS}	Ground
RDY/$\overline{Busy}$ (♦)	Ready busy
$\overline{RES}$ (♦)	Reset
NC	No connection

Block Diagram



Mode Selection

Pin Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$ (♦)	RDY/$\overline{Busy}$ (♦)	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H *1	High-Z	Dout
Standby	V_{IH}	×*2	×	×	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	×	×	V_{IH}	×	—	—
	×	V_{IL}	×	×	—	—
Data Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data out (I/O7)
Program reset	×	×	×	V_{IL}	High-Z	High-Z

Note: 1. Refer to the recommended DC operating condition.
2. × : Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage *1	V_{CC}	−0.6 to +7.0	V
Input voltage *1	Vin	−0.5*2 to +7.0	V
Operating temperature range *3	Topr	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C

Notes: 1. With respect to V_{SS}.
2. Vin min : −3.0 V for pulse width ≤ 50 ns.
3. Including electrical characteristics and data retention.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	5.5	V
Input voltage	V_{IL}	−0.3*1	—	0.6	V
	V_{IH}	2.4*2	—	V_{CC} + 0.3*3	V
	V_H(♦)	V_{CC} − 0.5	—	V_{CC} + 1.0	V
Operating temperature	Topr	0	—	70	°C

Notes: 1. V_{IL} min: −1.0 V for pulse width ≤ 50 ns.
2. V_{IH} min for V_{CC} = 3.6 to 5.5 V is 3.0 V.
3. V_{IH} max: V_{CC} + 1.0 V for pulse width ≤ 50 ns.

DC Characteristics (Ta = 0 to + 70°C, V_{CC} = 2.7 to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2*1	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
V_{CC} current (active)	I_{CC3}	—	—	8	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 3.6 V
		—	—	12	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 5.5 V
		—	—	20	mA	Iout = 0 mA, Duty = 100%, Cycle = 120 ns at V_{CC} = 3.6 V
		—	—	30	mA	Iout = 0 mA, Duty = 100%, Cycle = 120 ns at V_{CC} = 5.5 V
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	V_{CC} × 0.8	—	—	V	I_{OH} = −400 µA

Note: 1. I_{LI} on $\overline{RES}$: 100 µA max (♦)

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance	Cin*1	—	—	6	pF	Vin = 0 V
Output capacitance	Cout*1	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics (Ta = 0 to + 70°C, V_{CC} = 2.7 to 5.5 V)

Test Conditions

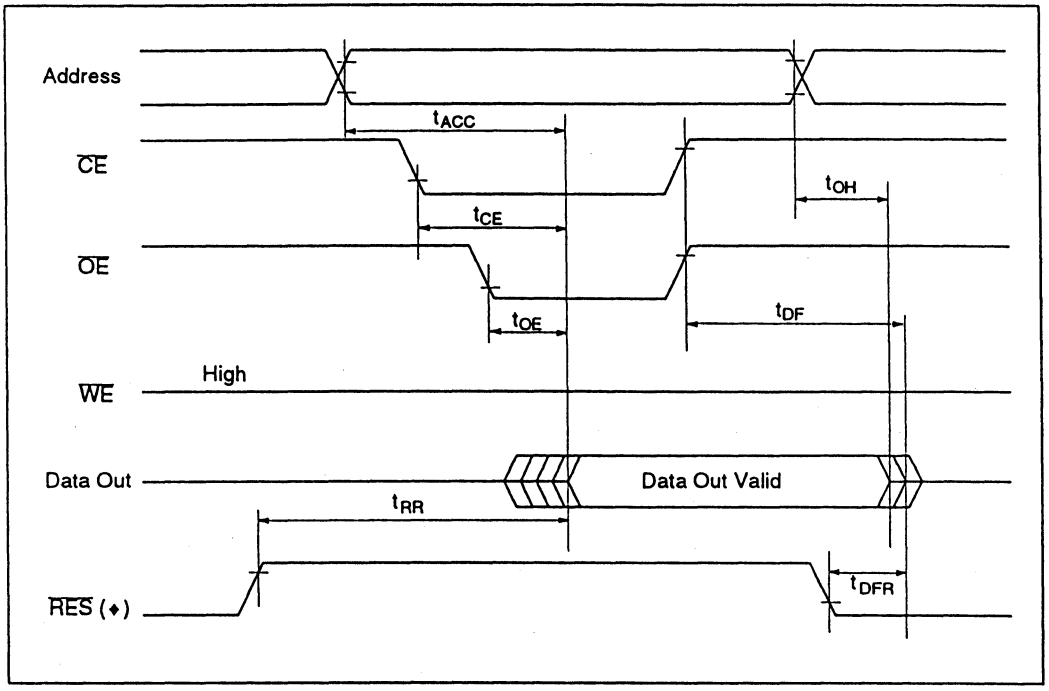
- Input pulse levels : 0 V to 3.0 V
  0 V to V_{CC} ($\overline{RES}$ pin)
- Input rise and fall time : ≤ 20 ns
- Input timing reference levels : 0.8, 1.8 V
- Output load : 1TTL Gate +100 pF
- Output reference levels : 1.5 V, 1.5 V

Read Cycle

		HN58V256A, 257A					
		-12		-15			
Parameter	Symbol	Min	Max	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	120	—	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	120	—	150	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	60	10	60	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float*1	t_{DF}	0	40	0	40	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ low to output float*1(♦)	t_{DFR}	0	350	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay(♦)	t_{RR}	0	600	0	600	ns	$\overline{CE}$ = $\overline{OE}$= V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.

Read Timing Waveform



Write Cycle

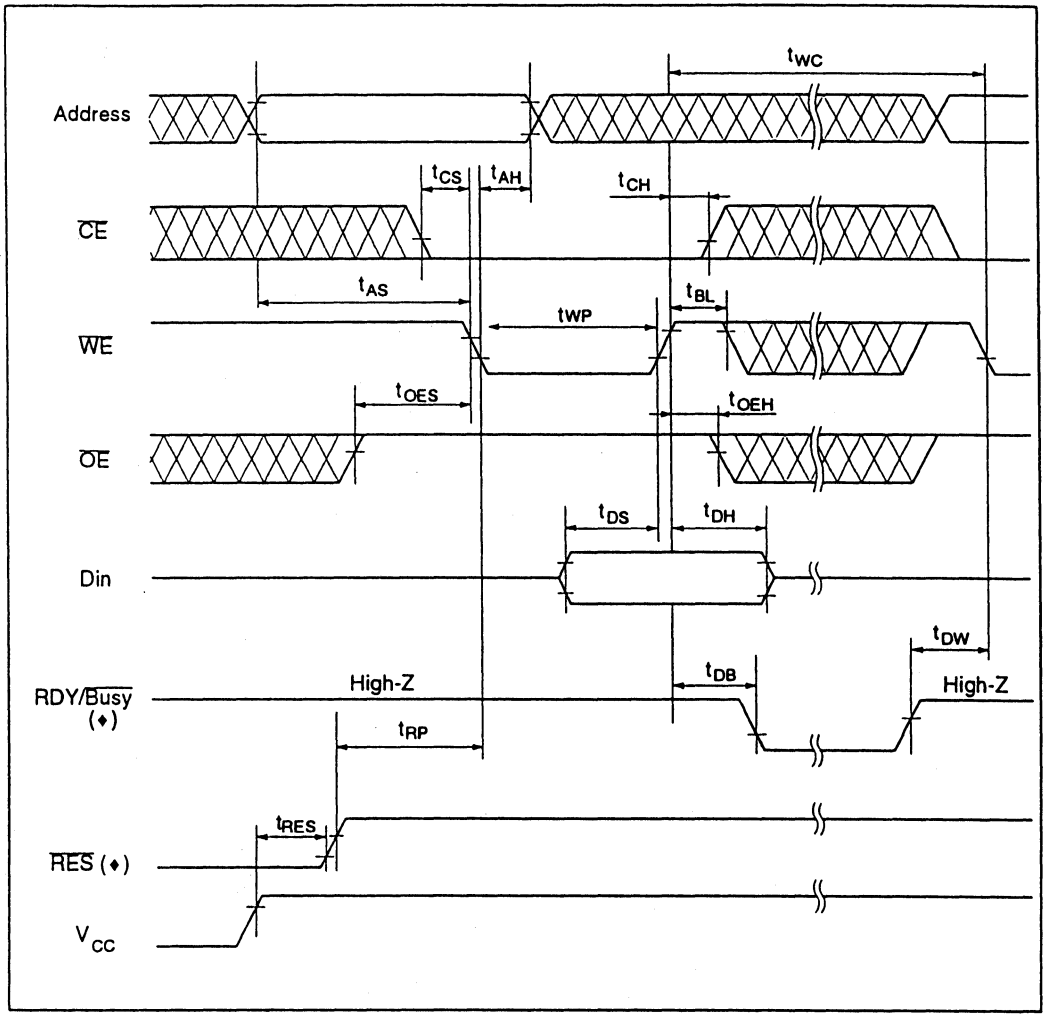
Parameter	Symbol	Min*1	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	50	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	50	—	—	ns	
Data hold time	t_{DH}	0	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	200	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	200	—	—	ns	
Data latch time	t_{DL}	100	—	—	ns	
Byte load cycle	t_{BLC}	0.3	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*2	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	0*3	—	—	ns	
Reset protect time (♦)	t_{RP}	100	—	—	µs	
Reset high time (♦)	t_{RES}	1	—	—	µs	

Note: 1. Use this device in longer cycle than this value.

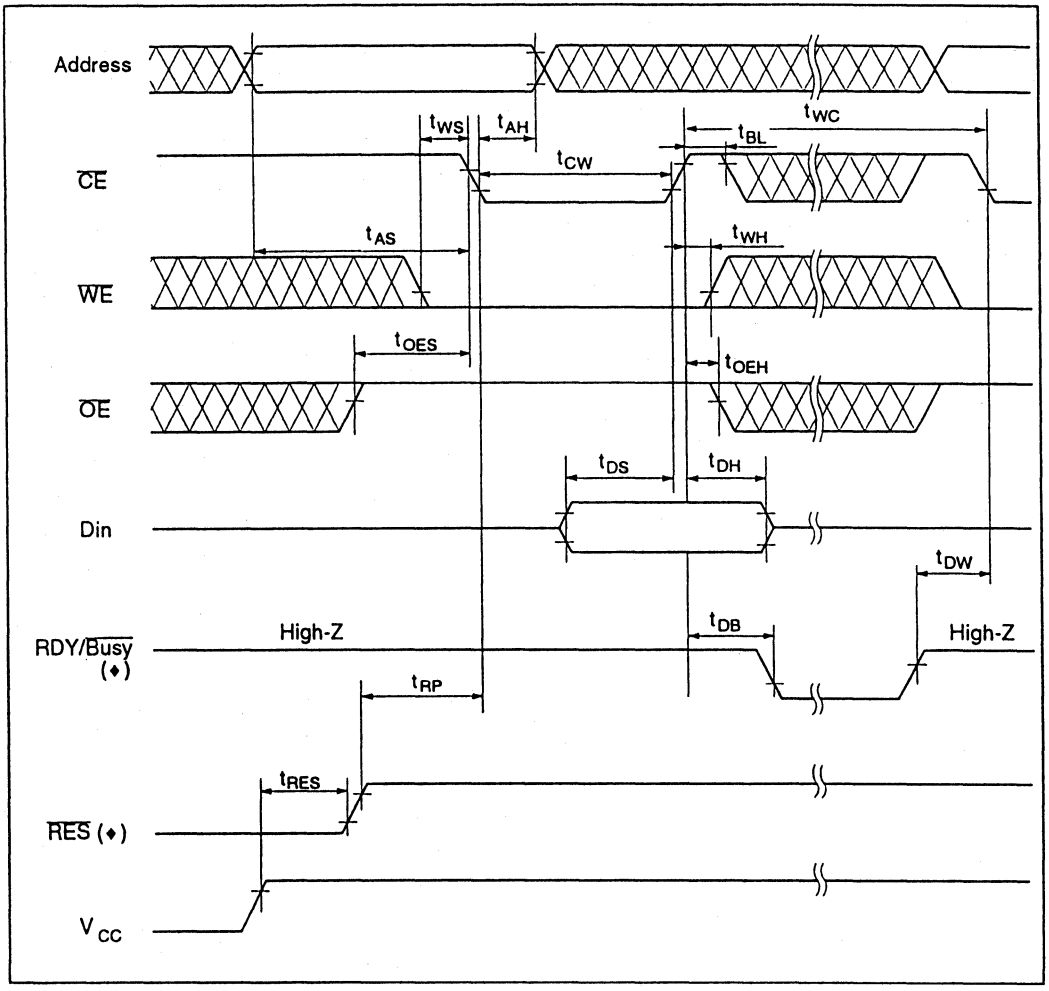
2. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{Busy}$ (♦) are used. This device automatically completes the internal write operation within this value.

3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{Busy}$ (♦) are used.

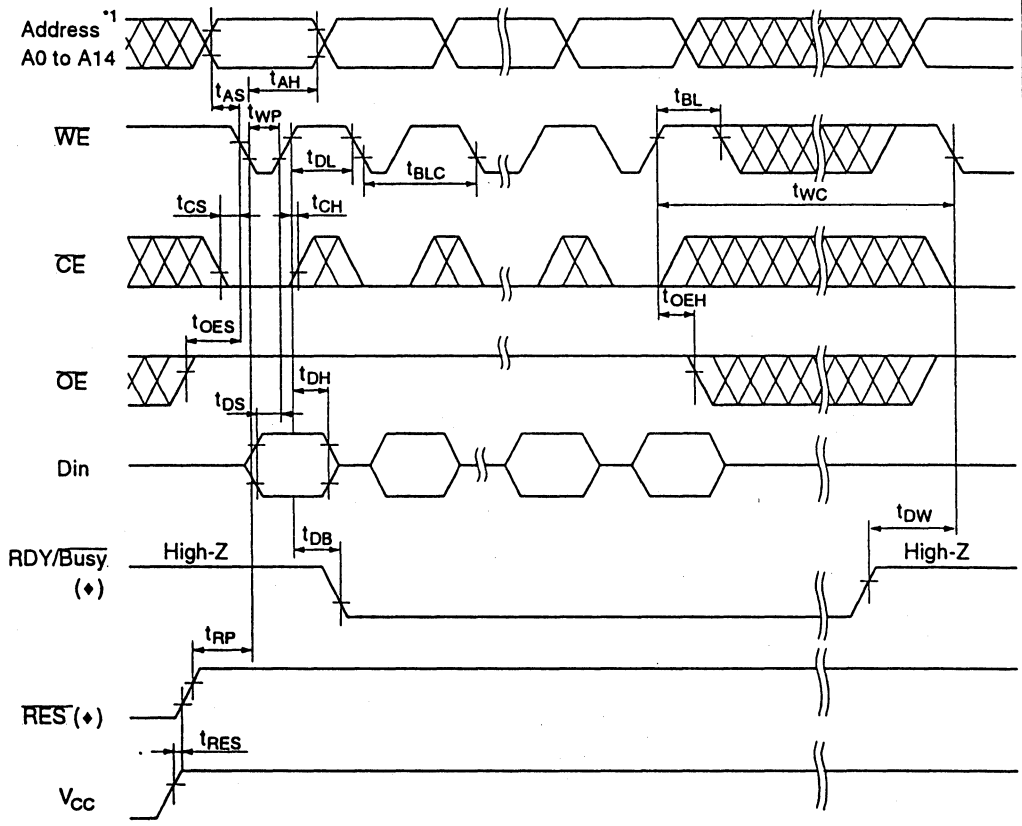
Byte Write Timing Waveform(1) ($\overline{WE}$ Controlled)



Byte Write Timing Waveform(2) ($\overline{CE}$ Controlled)

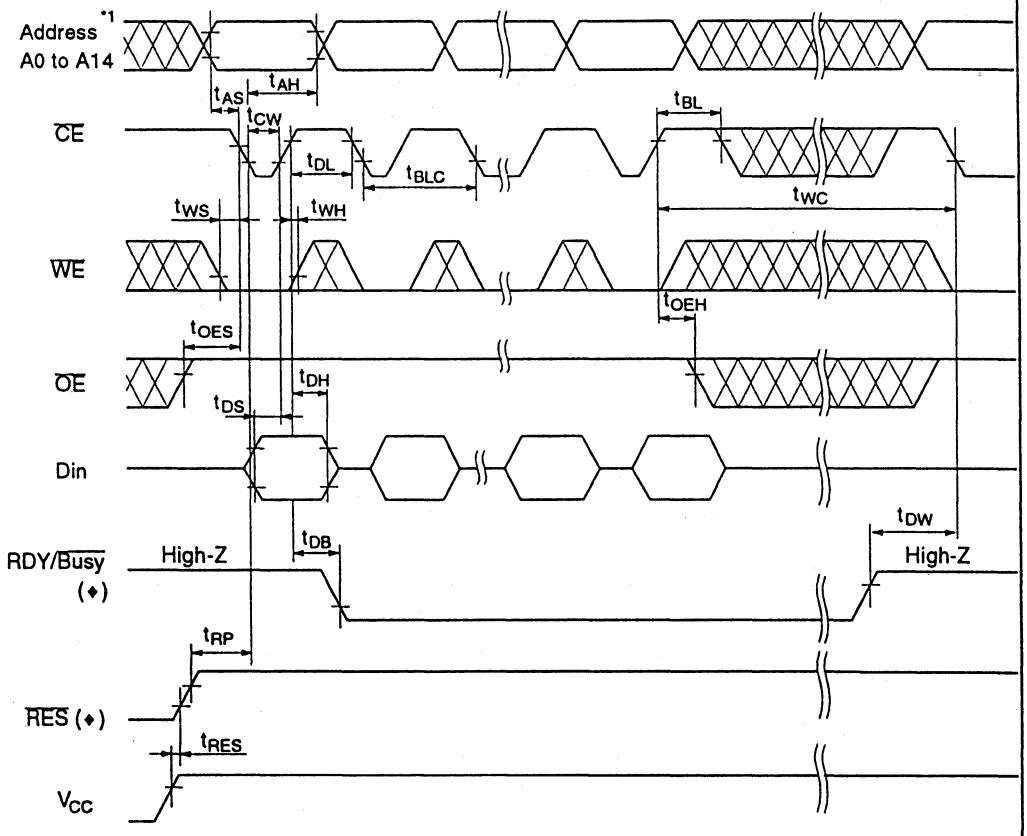


Page Write Timing Waveform(1) ($\overline{WE}$ Controlled)



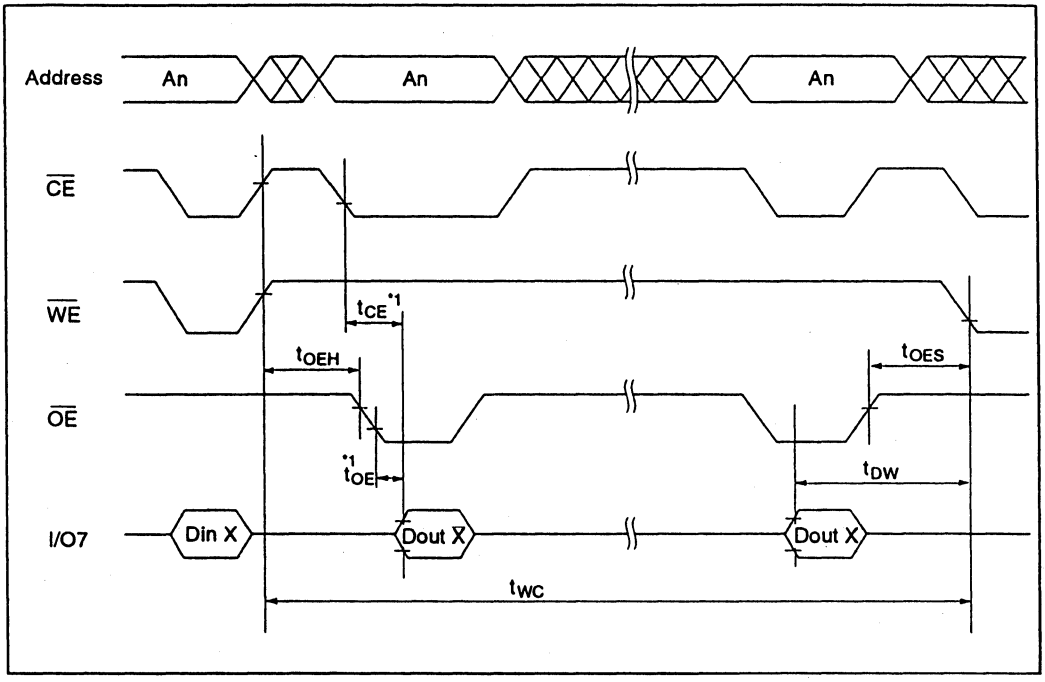
Note: 1. A6 through A14 are page address and these address are latched at the first falling edge of $\overline{WE}$

Page Write Timing Waveform(2) ($\overline{CE}$ Controlled)



Note: 1. A6 through A14 are page address and these address are latched at the first falling edge of $\overline{CE}$

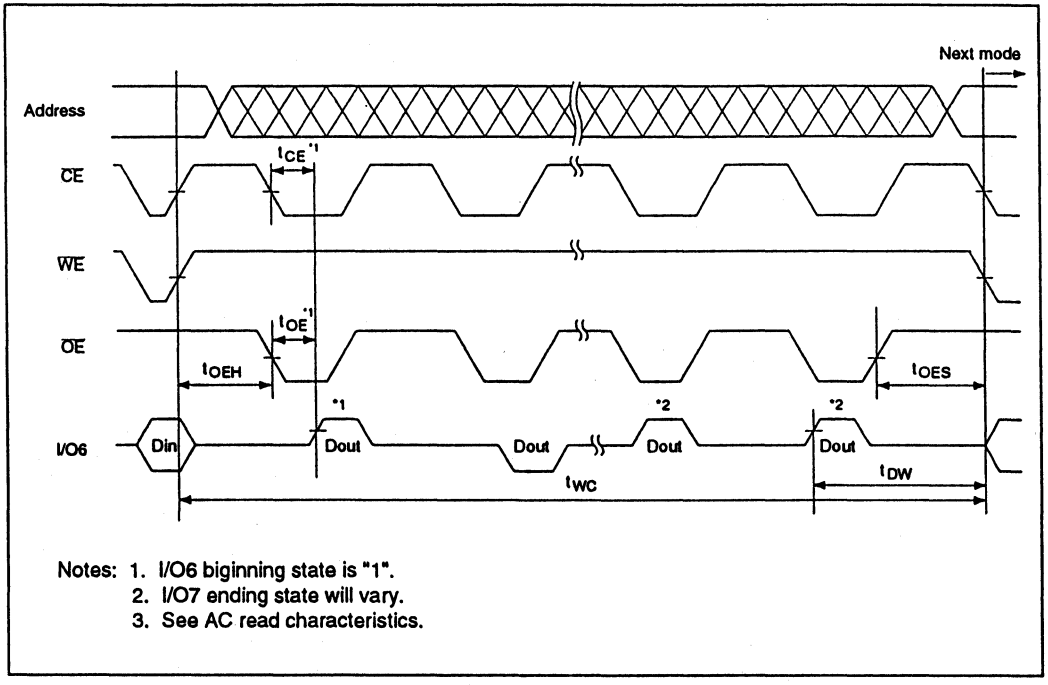
$\overline{\text{Data}}$ Polling Timing Wavefome



Toggle bit

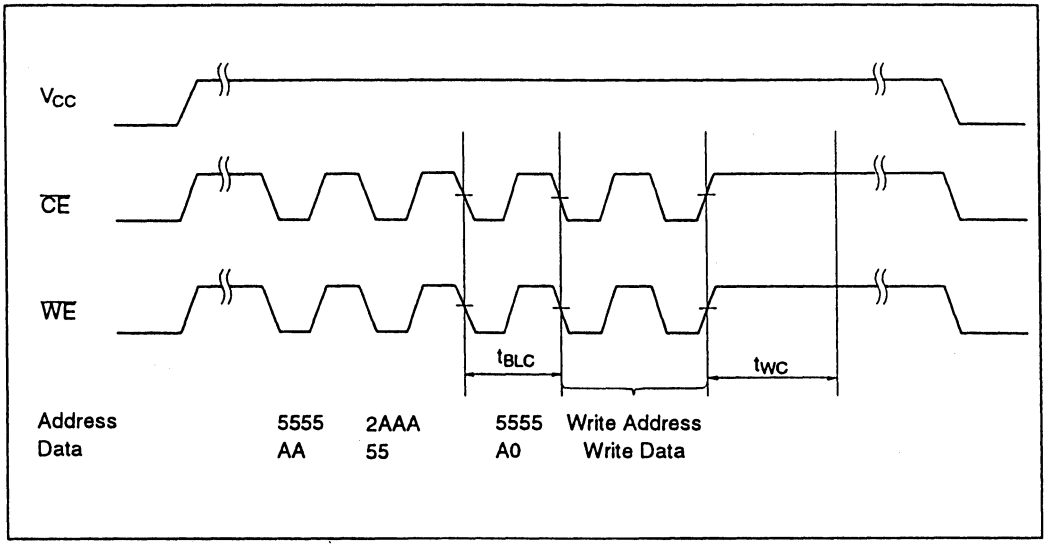
This device provide another function to determine the internal programming cycle. If the EEPROM is set to read mode during the internal programming cycle, I/O6 will charge from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle bit Wavefome

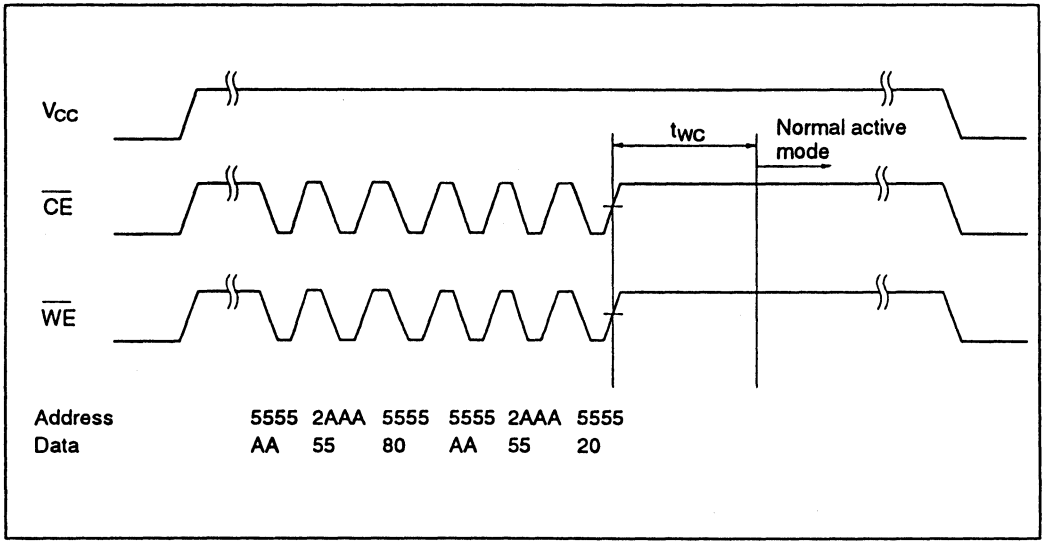


Notes: 1. I/O6 biginning state is "1".
2. I/O7 ending state will vary.
3. See AC read characteristics.

Data Protection Timing Waveform(1) (in protection mode)



Software Data Protection Timing Waveform(2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 64 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 63 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is kept high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{Data}$ Polling

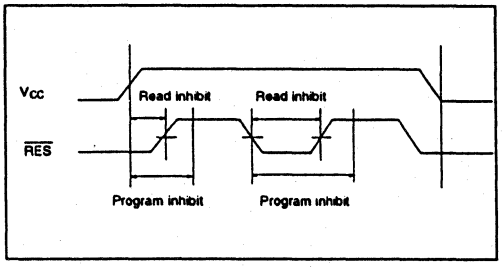
$\overline{Data}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operation.

RDY/$\overline{Busy}$ Signal (♦)

RDY/$\overline{Busy}$ signal also allows status of the EEPROM to be determined. The RDY/$\overline{Busy}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{Busy}$ signal changes state to high impedance.

$\overline{RES}$ Signal (♦)

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it doesn't provide a latch function.



$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

Write/Erase Endurance and Data Retention Time

The endurance is 10^5 cycles in case of the page programming and 10^4 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

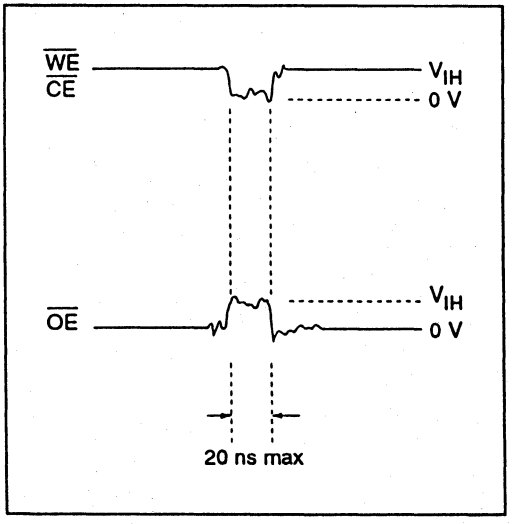
Data Protection

1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.

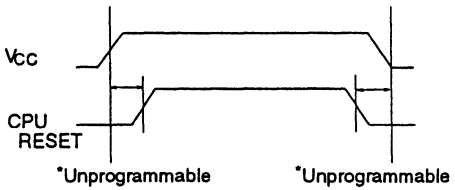
To prevent this phenomenon, this device has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode.

Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may act as a trigger and turn the EEPROM to program mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable state while the CPU is in an unstable state.



*The EEPROM shoud be kept in unprogrammable state during V_{CC} on/off by using CPU RESET signal.

(1)Protection by $\overline{CE}$, $\overline{OE}$, $\overline{WE}$

To realize the unprogrammable state, the input level of control pins must be held as shown in the table below.

$\overline{CE}$	V_{CC}	×	×
$\overline{OE}$	×	V_{SS}	×
$\overline{WE}$	×	×	V_{CC}

×: Don't care.
V_{CC}: Pull-up to V_{CC} level.
V_{SS}: Pull-down to V_{SS} level.

(2) Protection by $\overline{RES}$ (♦)

The unprogrammable state can be realized by that the CPU's reset signal inputs directly to the EEPROM's $\overline{RES}$ pin. $\overline{RES}$ should be kept V_{SS} level during V_{CC} on/off.

The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.

3. Software data protection

To prevent unintentional programming caused by noise generated by external circuits, This device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode.

Address	Data	
5555	AA	
↓	↓	
AAAA or 2AAA	55	
↓	↓	
5555	A0	
↓	↓	
Write address	Write data }	Normal data input

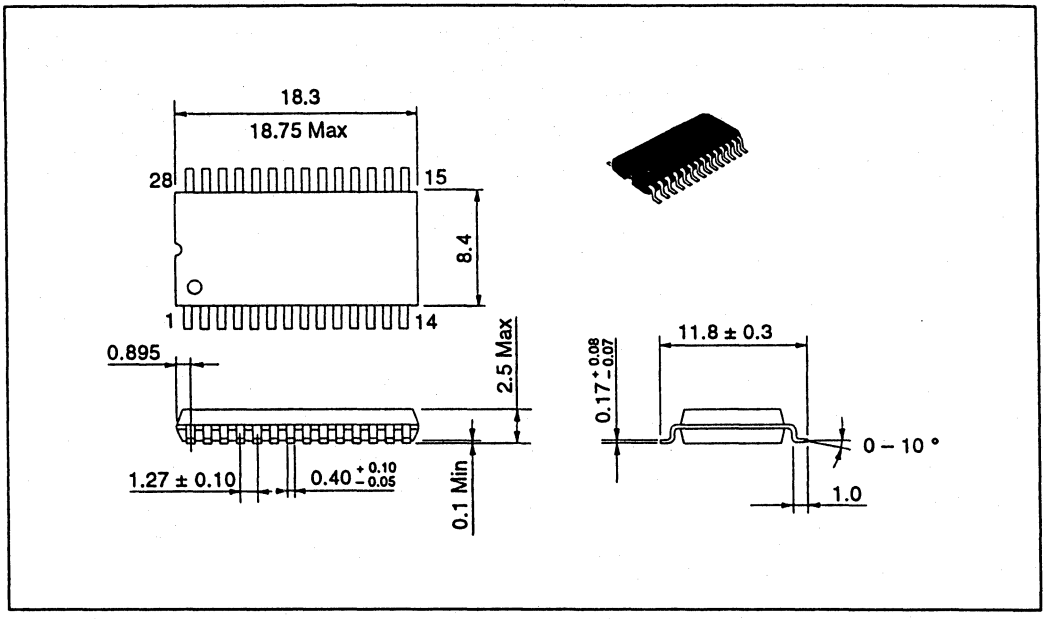
Software data protection mode can be cancelled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the cancelling cycle, the data cannot be written.

Address	Data
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	80
↓	↓
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	20

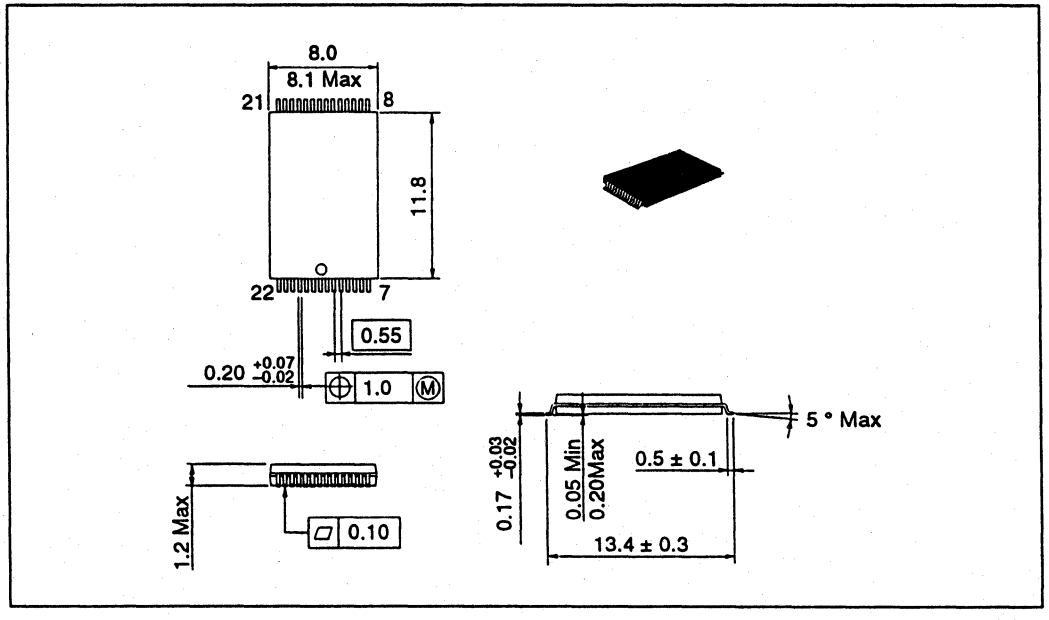
The software data protection is not enabled at the shipment.Package Dimensions

Package Dimensions

HN58V256AFP Series (FP-28D) **Unit : mm**

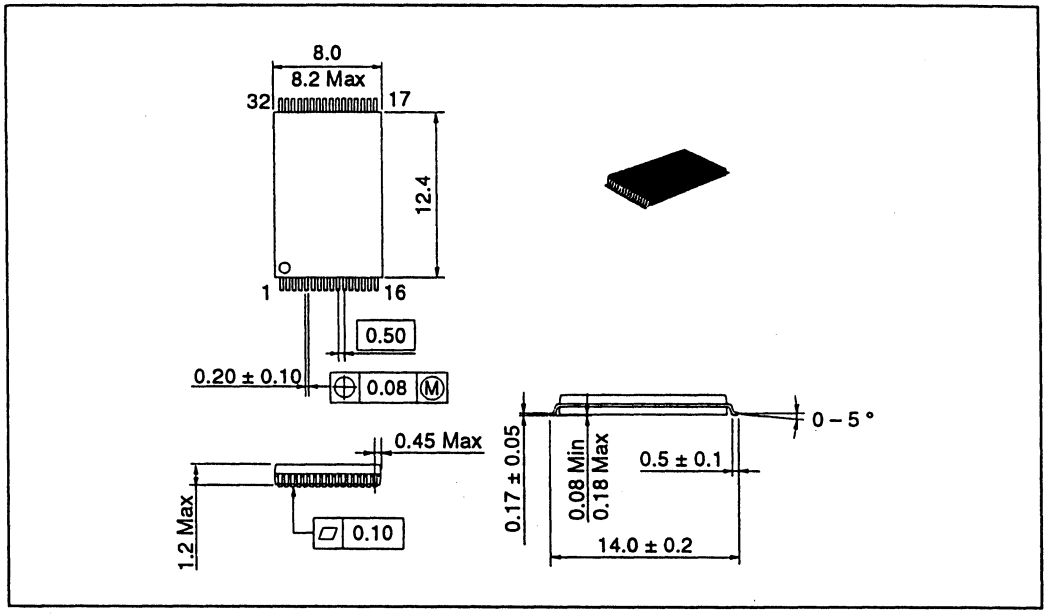


HN58V256AT Series (TFP-28DB) **Unit : mm**



Package Dimensions (cont)

HN58V257AT Series (TFP-32DA) **Unit : mm**



1M EEPROM

HN58C1001 Series

131,072-word × 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

Rev. 5.0
May 23, 1995

The Hitachi HN58C1001 is an electrically erasable and programmable EEPROM organized as 131,072-word × 8-bit. It realizes high speed, low power consumption, and a high level of reliability, employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 128-byte page programming function to make its erase and write operations faster.

Features

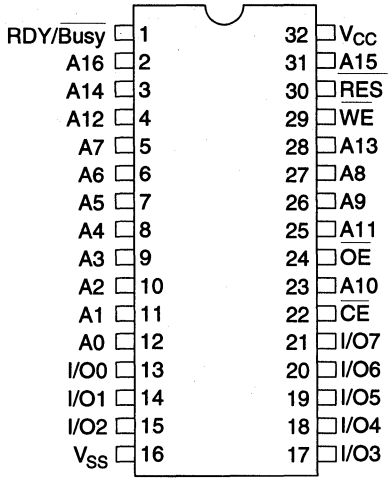
- Single 5 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 10 ms max
- Automatic page write (128 bytes): 10 ms max
- Fast access time: 150 ns max
- Low power dissipation: 20 mW/MHz, typ (active)
  110 µW max (standby)
- $\overline{Data}$ polling and RDY/$\overline{Busy}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^4erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{RES}$ pin

Ordering Information

Type no.	Access time	Package
HN58C1001P-15	150 ns	600 mil 32-pin plastic DIP(DP-32)
HN58C1001FP-15	150 ns	525 mil 32-pin plastic SOP (FP-32D)
HN58C1001T-15	150 ns	8 × 14 mm 32-pin plastic TSOP (TFP-32DA)

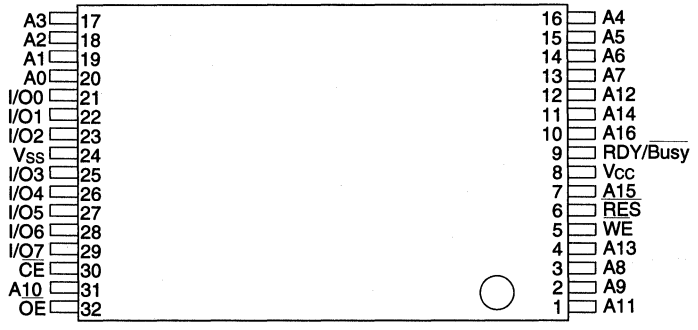
Pin Arrangement

• HN58C1001P/FP Series



(Top View)

• HN58C1001T Series



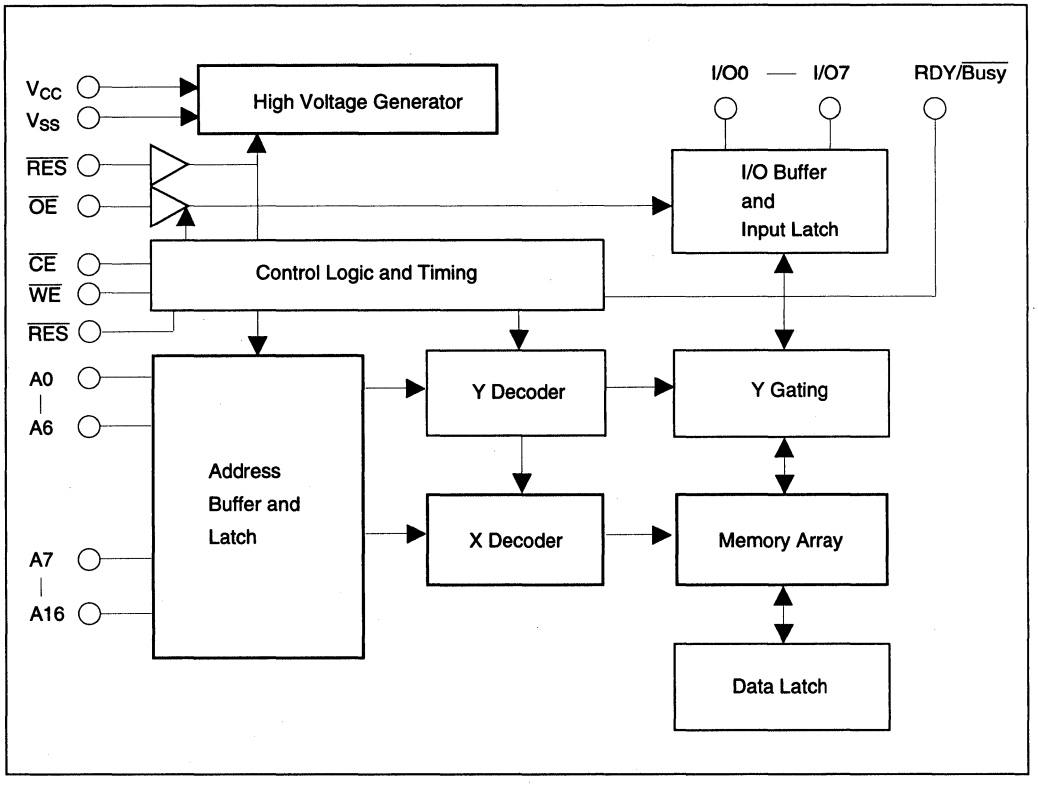
(Top View)

Pin Description

Pin name	Function
A0-A16	Address inputs
I/O0-I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable

Pin name	Function
$\overline{WE}$	Write enable
V_{CC}	Power (+5 V)
V_{SS}	Ground
RDY/$\overline{Busy}$	Ready busy
$\overline{RES}$	Reset

Block Diagram



Mode Selection

Pin Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	Dout
Standby	V_{IH}	×	×	×	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	×	×	V_{IH}	×	—	—
	×	V_{IL}	×	×	—	—
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data Out (I/O7)
Program Reset	×	×	×	V_{IL}	High-Z	High-Z

Note: 1. ×: Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage *1	V_{CC}	–0.6 to +7.0	V
Input voltage *1	Vin	–0.5*2 to +7.0	V
Operating temperature range *3	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. With respect to V_{SS}
2. Vin min : –3.0 V for pulse width ≤ 50 ns
3. Including electrical characteristics and data retention.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IL}	–0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_H	V_{CC} – 0.5	—	V_{CC} + 1.0	V
Operating temperature	Topr	0	—	70	°C

DC Characteristics (Ta=0 to +70°C, V_{CC} = 5 V ± 10 %)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2*1	µA	V_{CC} = 5.5 V, Vin = 5.5 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 5.5 V, Vout = 5.5/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
V_{CC} current (active)	I_{CC3}	—	—	15	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 5.5 V
		—	—	50	mA	Iout = 0 mA, Duty = 100%, Cycle = 150 ns at V_{CC} = 5.5 V
Input low voltage	V_{IL}	–0.3*2	—	0.8	V	
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V	
	V_H	V_{CC}–0.5	—	V_{CC} + 1.0	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –400 µA

Note: 1. I_{LI} on $\overline{RES}$: 100 µA max
2. V_{IL} min : –1.0 V for pulse width ≤ 50 ns

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance*1	Cin	—	—	6	pF	Vin = 0 V
Output capacitance*1	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%)

Test Conditions

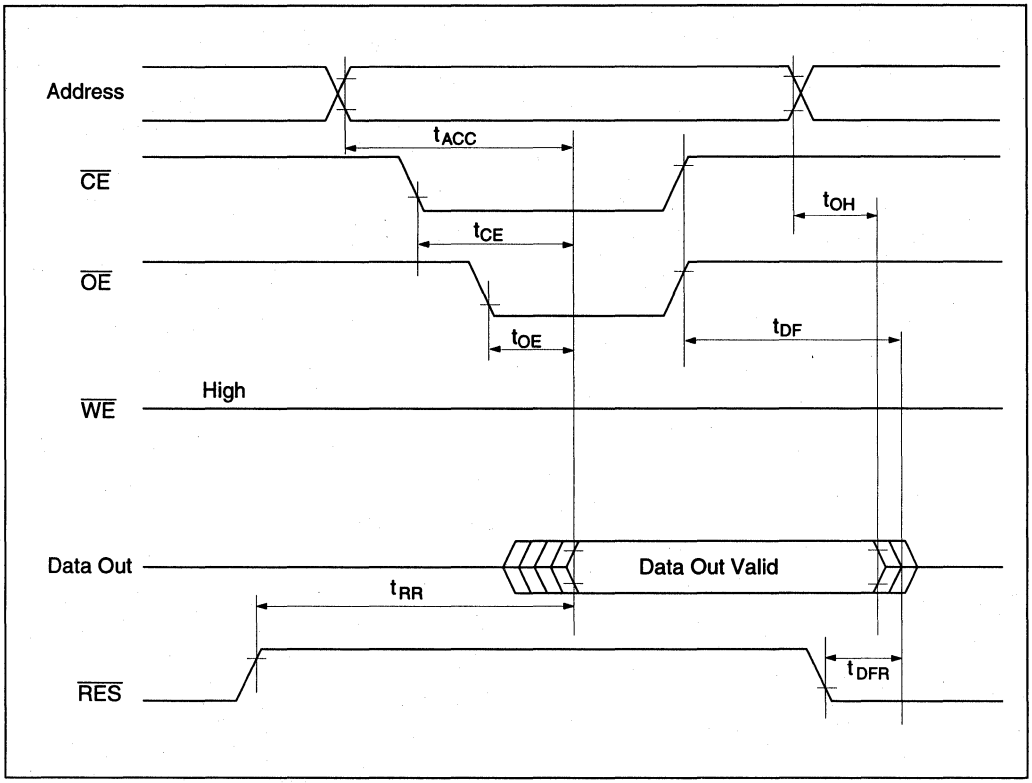
- Input pulse levels : 0.4 V to 2.4 V
  0 V to V_{CC} ($\overline{RES}$ pin)
- Input rise and fall time : ≤ 20 ns
- Output load : 1TTL Gate +100 pF
- Reference levels for measuring timing : 0.8 V, 2.0 V

Read Cycle

Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	150	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	75	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float*1	t_{DF}	0	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ low to output float*1	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay	t_{RR}	0	450	ns	$\overline{CE}$ = $\overline{OE}$= V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.

Read Timing Waveform



Write Cycle

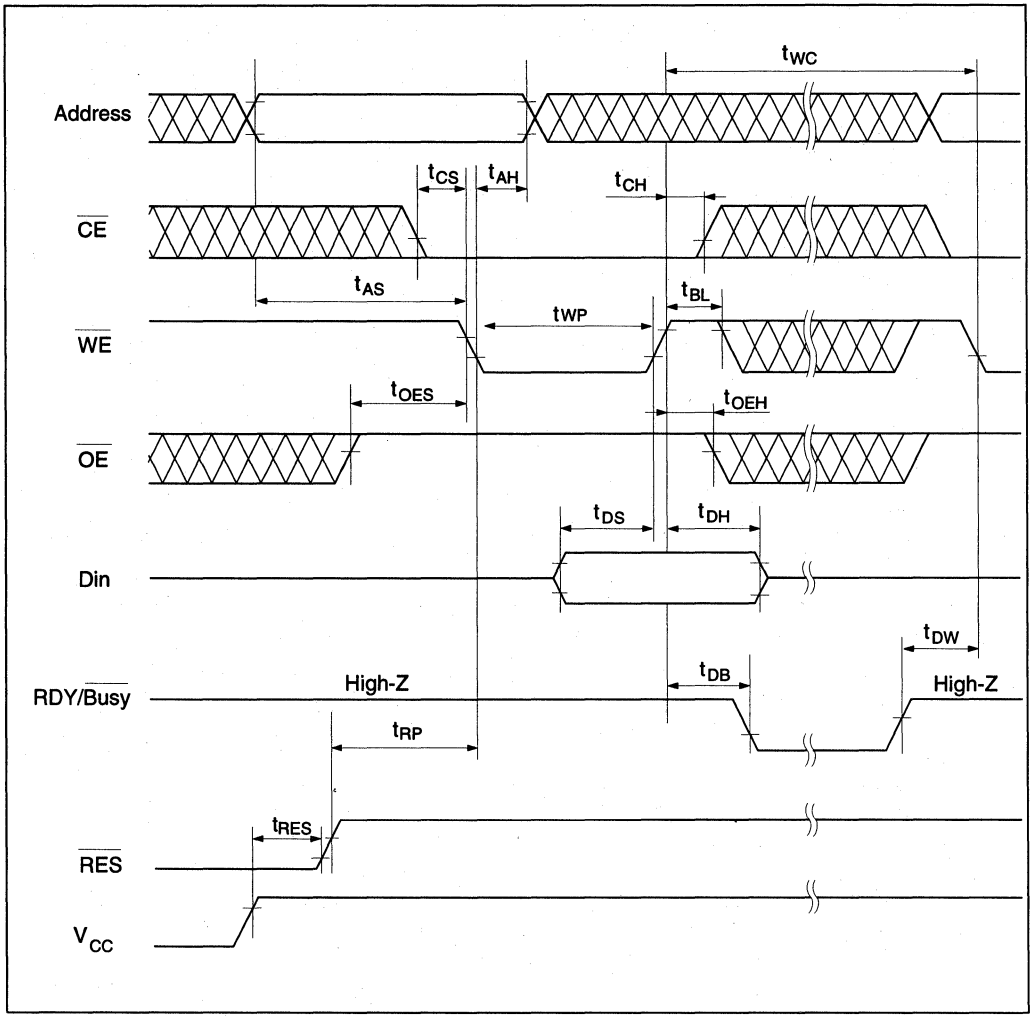
Parameter	Symbol	Min*1	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	10	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	250	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	250	—	—	ns	
Data latch time	t_{DL}	300	—	—	ns	
Byte load cycle	t_{BLC}	0.55	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	10*2	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	150*3	—	—	ns	
Reset protect time	t_{RP}	100	—	—	µs	
Reset low time	t_{RES}	1	—	—	µs	

Note: 1. Use this device in longer cycle than this value.

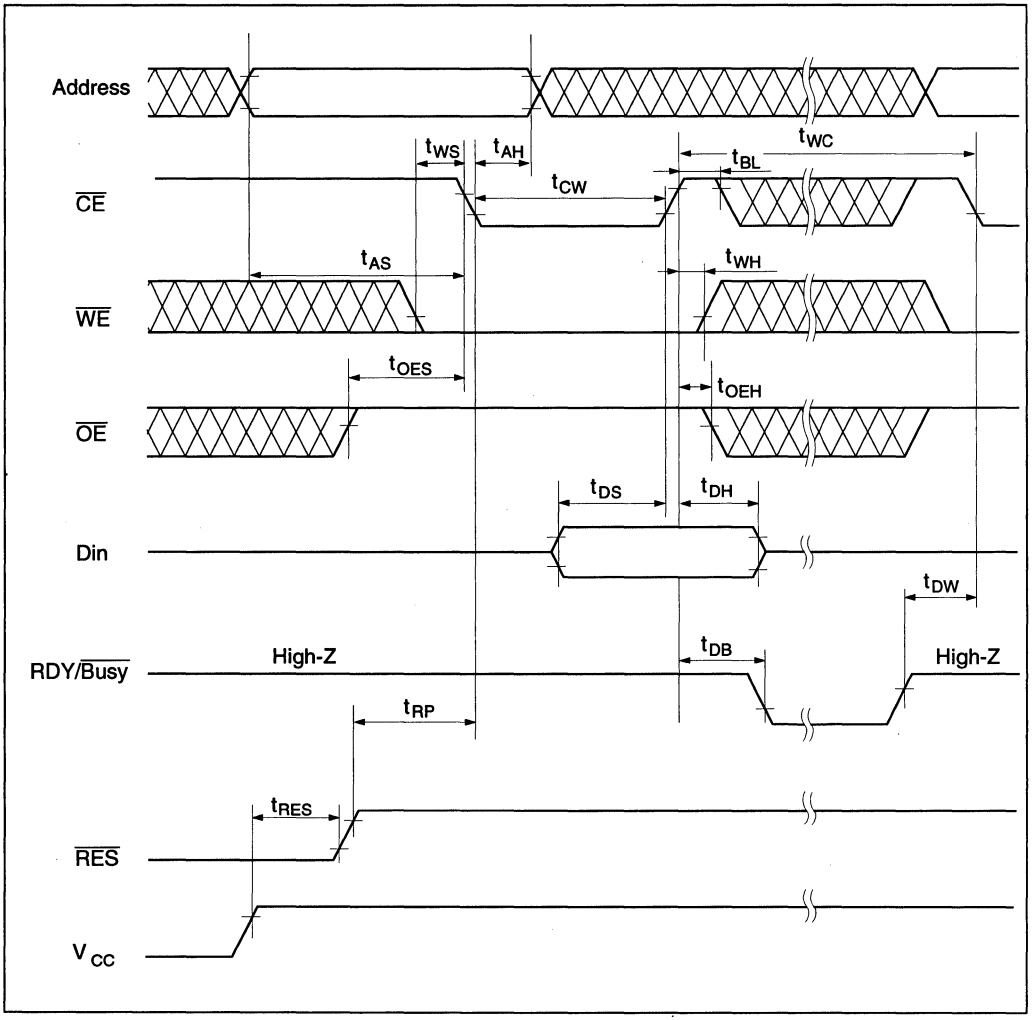
2. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.

3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{Busy}$ are used.

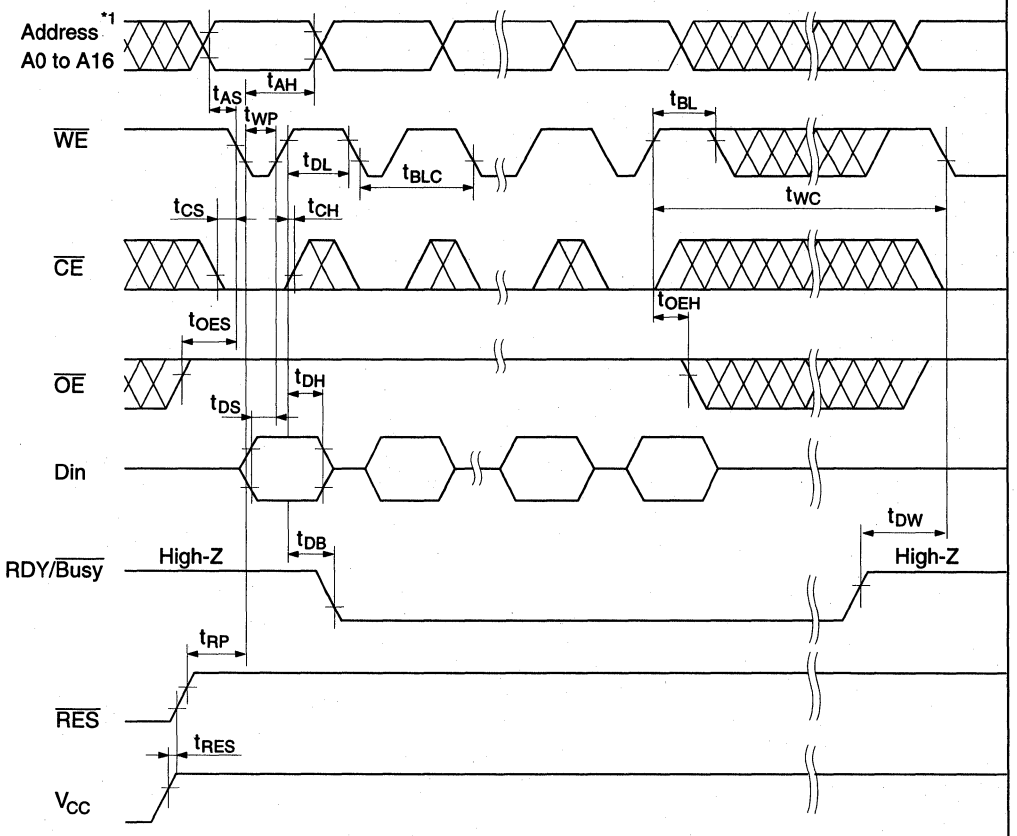
Byte Write TimingWaveform(1) ($\overline{WE}$ Controlled)



Byte Write Timing Waveform (2) ($\overline{CE}$ Controlled)

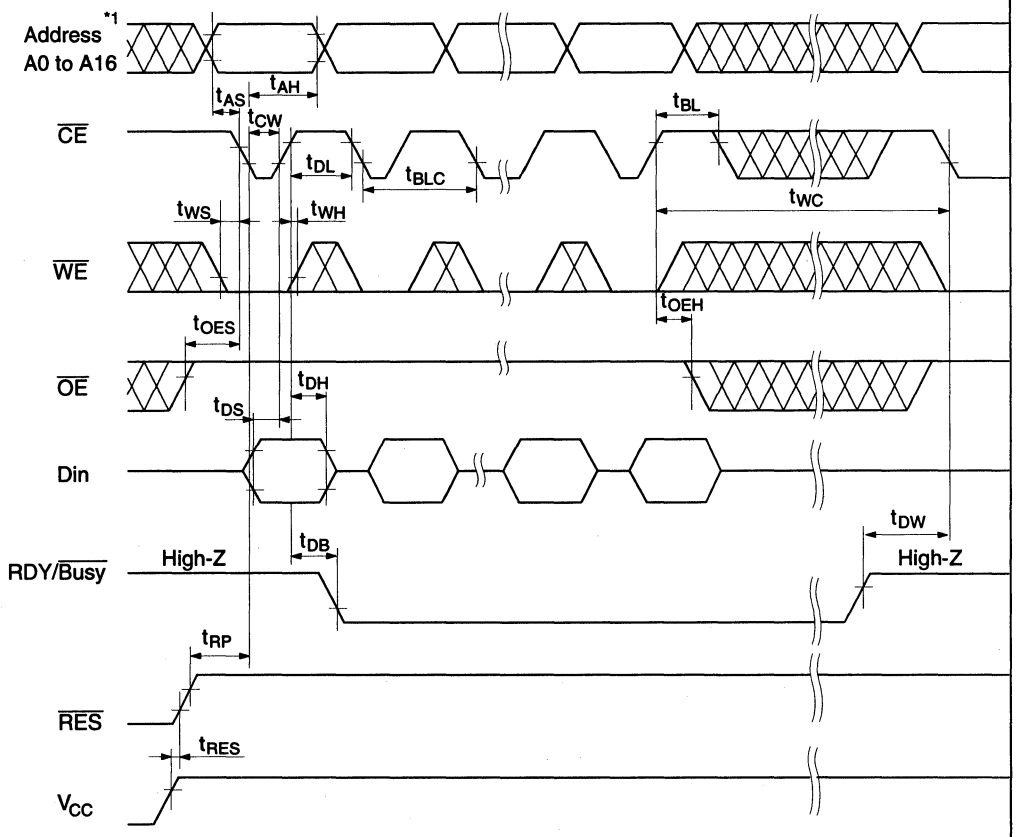


Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)



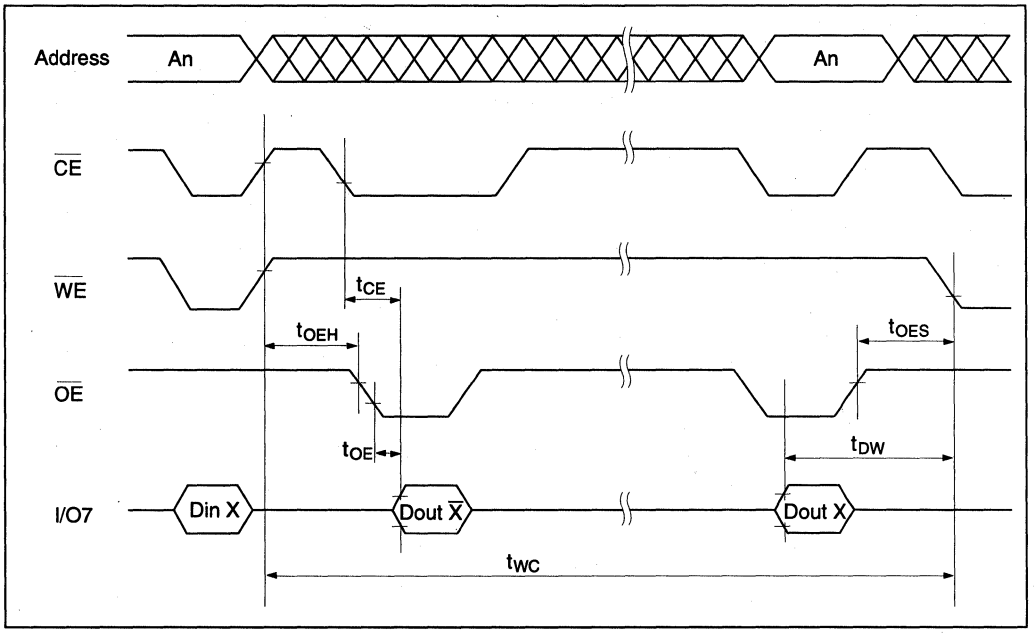
Note: 1. A7 to A16 are page addresses and must be same within the page write operation.

Page Write Timing Waveform (2) ($\overline{CE}$ Controlled)



Note: 1. A7 to A16 are page addresses and must be same within the page write operation.

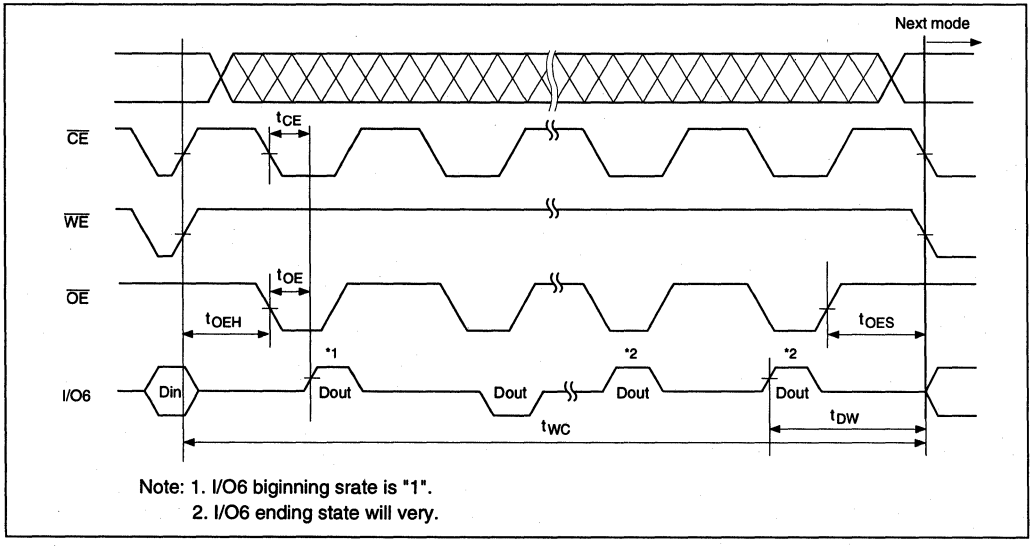
Data Polling Timing Waveform



Toggle bit

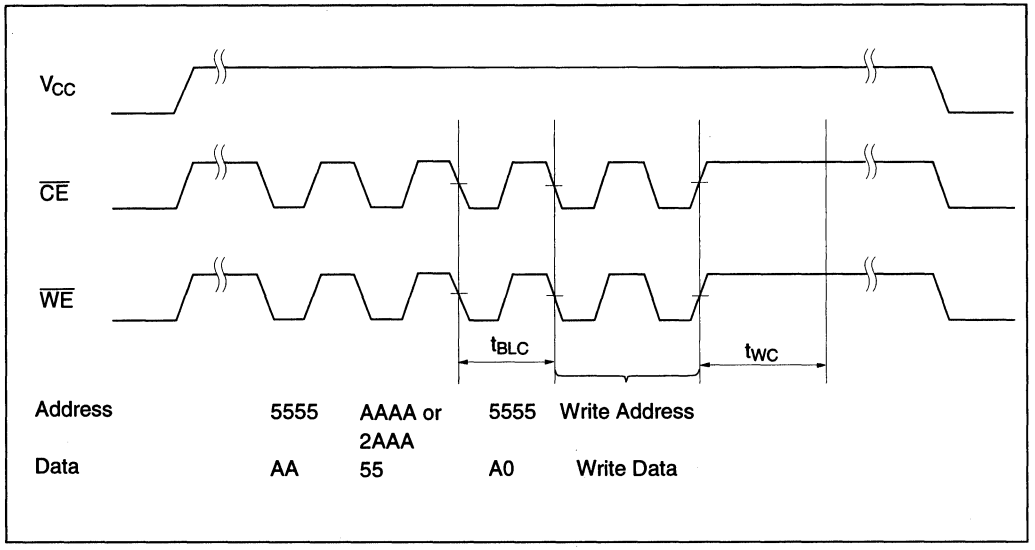
This device provide another function to determine the internal programming cycle. If EEPROM set to read mode during the internal programming cycle, I/O6 will charge from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

Toggle Bit Waveform

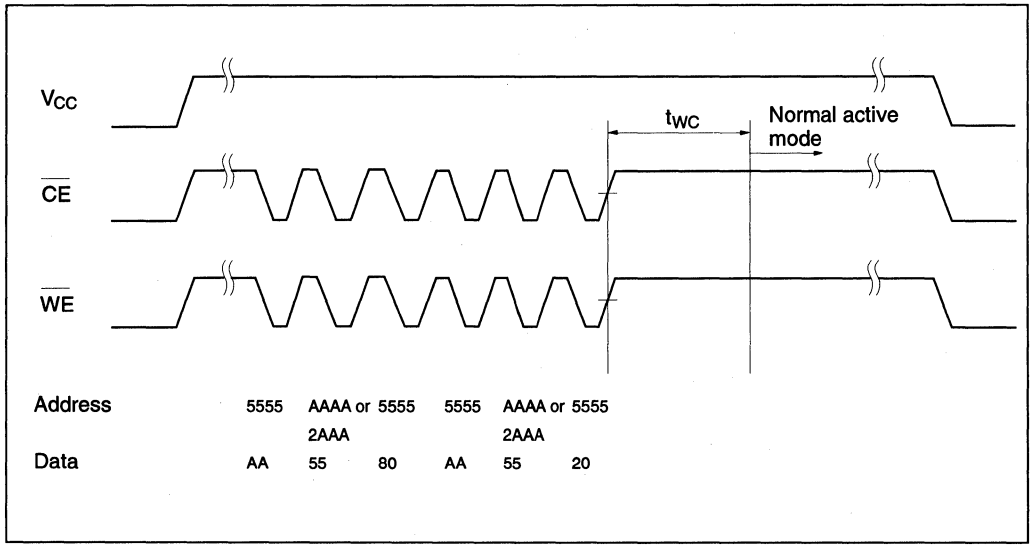


Note: 1. I/O6 biginning srate is "1".
2. I/O6 ending state will very.

Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 128 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 128 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is kept high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{Data}$ Polling

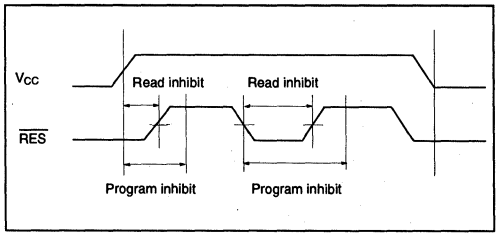
Data polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operartion.

RDY/$\overline{Busy}$ Signal

RDY/$\overline{Busy}$ signal also allows status of the EEPROM to be determined. The RDY/$\overline{Busy}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{Busy}$ signal changes state to high impedance.

$\overline{RES}$ Signal

When $\overline{RES}$ is low, the EEPROM cannot be read or programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{CC} is switched. $\overline{RES}$ should be high during read and programming because it dosen't provide a latch function.



$\overline{WE}$, $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

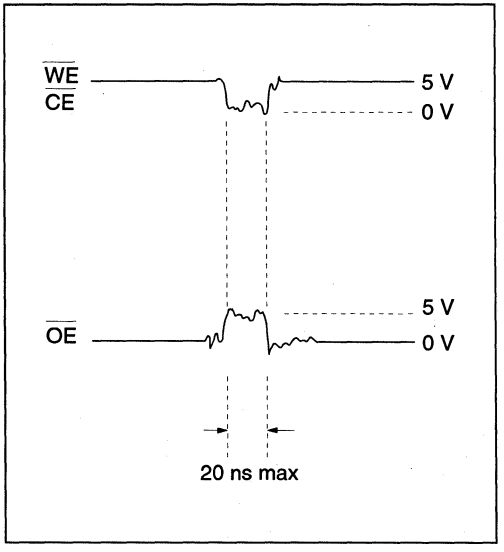
Write/Erase Endurance and Data Retention Time

The endurance is 10^4 cycles in case of the page programming and 10^3 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

Data Protection

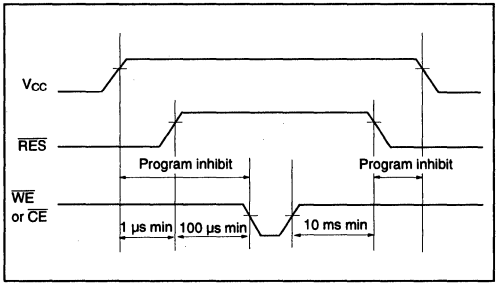
1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.
To prevent this phenomenon, the this device has a noise cancelation function that cuts noise if its width is 20 ns or less in programming mode.
Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in unprogrammable state by using a CPU reset signal to $\overline{RES}$ pin. $\overline{RES}$ pin should be kept at V_{SS} level when V_{CC} is turned on or off.
The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 10 ms after the last data input.



3. Software data protection

To prevent unintentional programming caused by noise generated by external circuits, This device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode.

Address	Data	
5555	AA	
↓	↓	
AAAA or 2AAA	55	
↓	↓	
5555	A0	
↓	↓	
Write address	Write data	} Normal data input

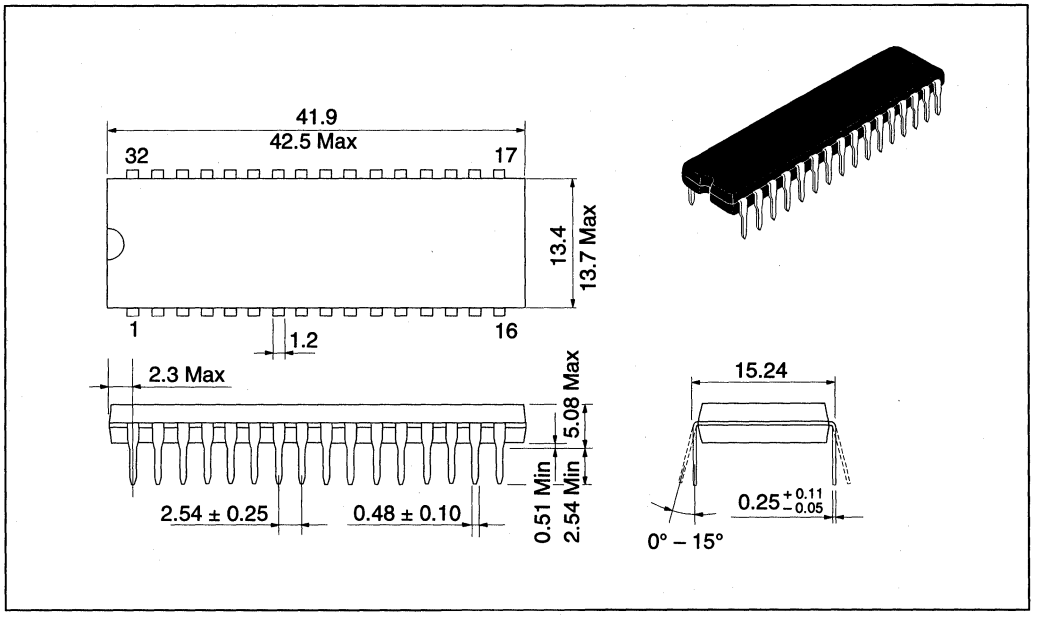
Software data protection mode can be canceled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the canceling cycle, the data cannot be written.

Address	Data
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	80
↓	↓
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	20

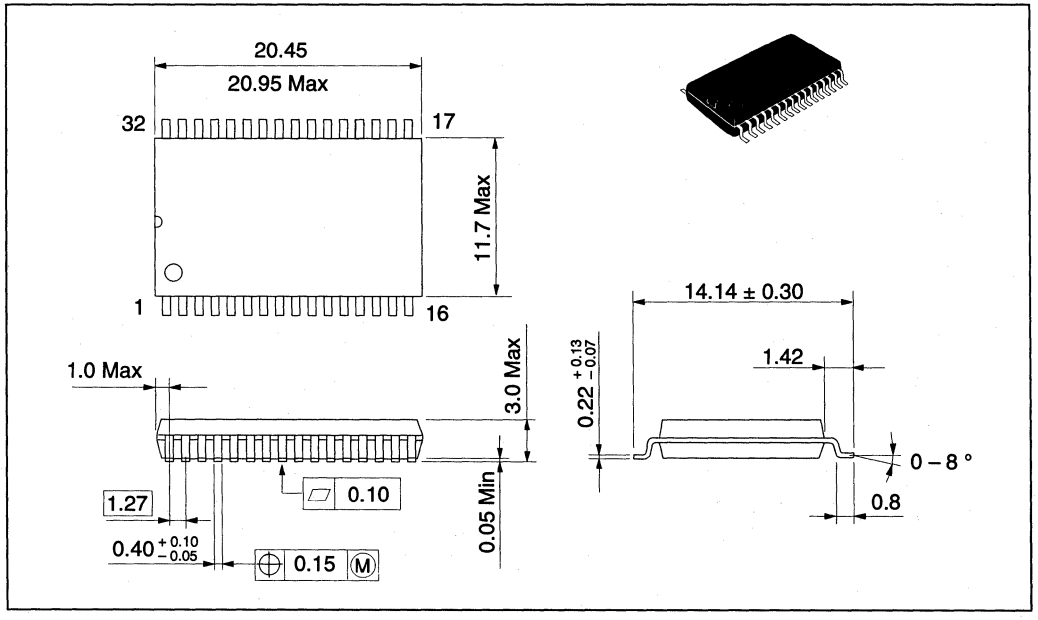
The software data protection is not enabled at the shipment.

Package Dimensions

HN58C1001P Series (DP-32) **Unit : mm**

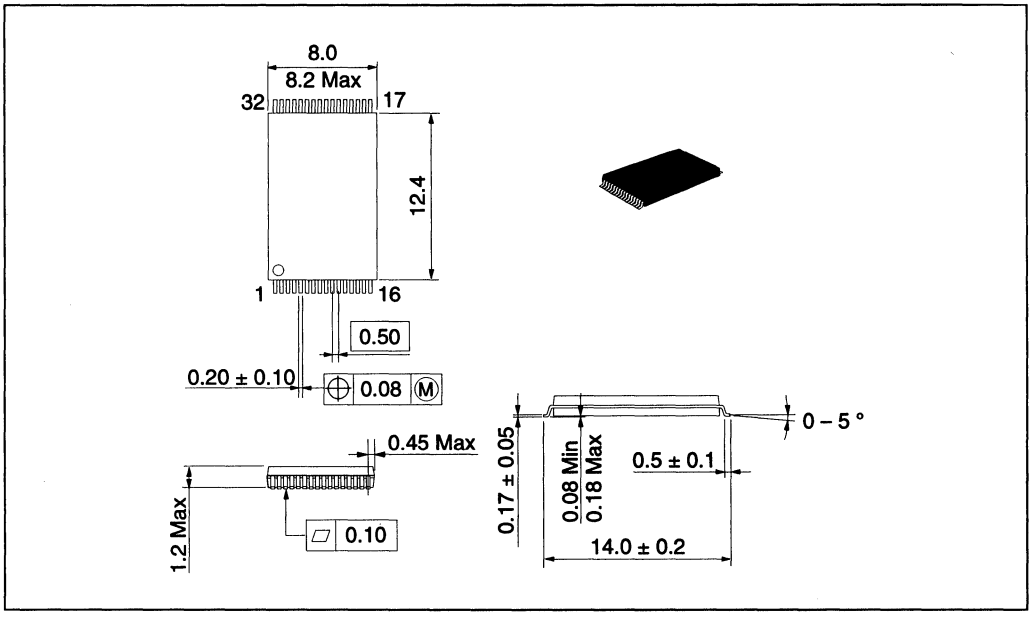


HN58C1001FP Series (FP-32D) **Unit : mm**



Package Dimensions (cont)

HN58C1001T Series (TFP-32DA) **Unit : mm**



HN58V1001 Series

131,072-word × 8-bit Electrically Erasable and Programmable CMOS ROM

HITACHI

Rev. 5.0
May 23, 1995

The Hitachi HN58V1001 is an electrically erasable and programmable EEPROM organized as 131,072-word × 8-bit. It realizes high speed, low power consumption, and a high level of reliability, employing advanced MNOS memory technology and CMOS process and circuitry technology. It also has a 128-byte page programming function to make its erase and write operations faster.

Features

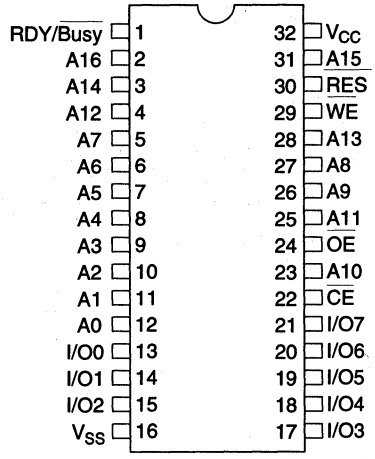
- Single 3 V supply
- On-chip latches: address, data, $\overline{CE}$, $\overline{OE}$, $\overline{WE}$
- Automatic byte write: 15 ms max
- Automatic page write (128 bytes): 15 ms max
- Fast access time: 250 ns max
- Low power dissipation: 20 mW/MHz, typ (active)
  110 µW max (standby)
- $\overline{Data}$ polling and RDY/$\overline{Busy}$
- Data protection circuit on power on/off
- Conforms to JEDEC byte-wide standard
- Reliable CMOS with MNOS cell technology
- 10^4erase/write cycles (in page mode)
- 10 years data retention
- Software data protection
- Write protection by $\overline{RES}$ pin

Ordering Information

Type no.	Access time	Package
HN58V1001P-25	250 ns	600 mil 32-pin plastic DIP(DP-32)
HN58V1001FP-25	250 ns	525 mil 32-pin plastic SOP (FP-32D)
HN58V1001T-25	250 ns	8 × 14 mm 32-pin plastic TSOP (TFP-32DA)

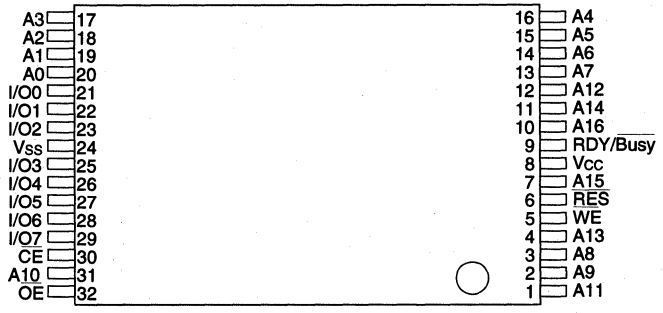
Pin Arrangement

• HN58V1001P/FP Series



(Top View)

• HN58V1001T Series



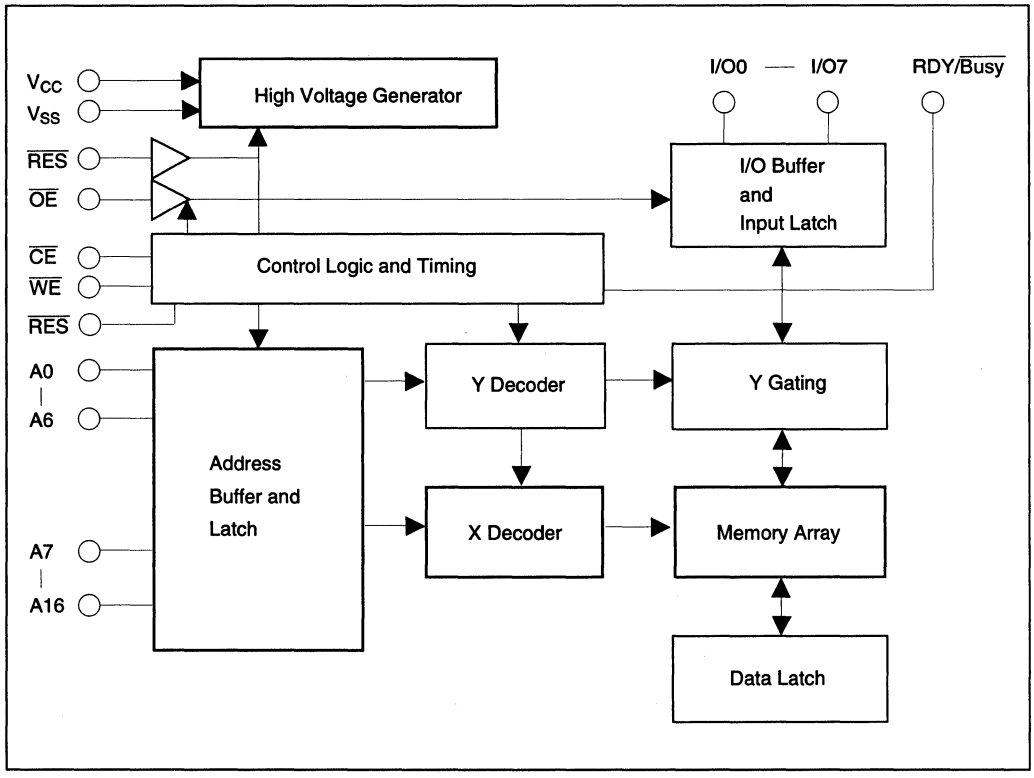
(Top View)

Pin Description

Pin name	Function
A0-A16	Address inputs
I/O0-I/O7	Data input/output
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable

Pin name	Function
$\overline{WE}$	Write enable
V_{CC}	Power (+3 V)
V_{SS}	Ground
RDY/$\overline{Busy}$	Ready busy
$\overline{RES}$	Reset

Block Diagram



Mode Selection

Pin Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	Dout
Standby	V_{IH}	×*1	×	×	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z to V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	×	×	V_{IH}	×	—	—
	×	V_{IL}	×	×	—	—
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data out (I/O7)
Program reset	×	×	×	V_{IL}	High-Z	High-Z

Note: 1. ×: Don't care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage *1	V_{CC}	–0.6 to +7.0	V
Input voltage *1	Vin	–0.5*2 to +7.0	V
Operating temperature range *3	Topr	0 to +70	°C
Storage temperature range	Tstg	–55 to +125	°C

Notes: 1. With respect to V_{SS}
2. Vin min : –3.0 V for pulse width ≤ 50 ns
3. Including electrical characteristics and data retention.

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	5.5	V
Input voltage	V_{IL}	–0.3	—	0.8	V
	V_{IH}	1.9	—	V_{CC} + 0.3	V
	V_H	V_{CC} – 0.5	—	V_{CC} + 1.0	V
Operating temperature	Topr	0	—	70	°C

DC Characteristics (Ta=0 to +70°C, V_{CC} = 2.7 to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2*1	µA	V_{CC} = 3.6 V, Vin = 3.6 V
Output leakage current	I_{LO}	—	—	2	µA	V_{CC} = 3.6 V, Vout = 3.6/0.4 V
V_{CC} current (standby)	I_{CC1}	—	—	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	—	—	1	mA	$\overline{CE}$ = V_{IH}
V_{CC} current (active)	I_{CC3}	—	—	6	mA	Iout = 0 mA, Duty = 100%, Cycle = 1 µs at V_{CC} = 3.3 V
		—	—	15	mA	Iout = 0 mA, Duty = 100%, Cycle = 250 ns at V_{CC} = 3.3 V
Input low voltage	V_{IL}	–0.3*2	—	0.8	V	
Input high voltage	V_{IH}	1.9*3	—	V_{CC} + 0.3	V	
	V_H	V_{CC}–0.5	—	V_{CC} + 1.0	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2.1 mA
Output high voltage	V_{OH}	V_{CC} × 0.8	—	—	V	I_{OH} = –400 µA

Note: 1. I_{LI} on $\overline{RES}$: 100 µA max
2. V_{IL} min : –1.0 V for pulse width ≤ 50 ns
3. V_{IH} min : 2.2 V for V_{CC} = 3.6 to 5.5 V.

Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test condition
Input capacitance*1	Cin	—	—	6	pF	Vin = 0 V
Output capacitance*1	Cout	—	—	12	pF	Vout = 0 V

Note: 1. This parameter is periodically sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 2.7 to 5.5 V)

Test Conditions

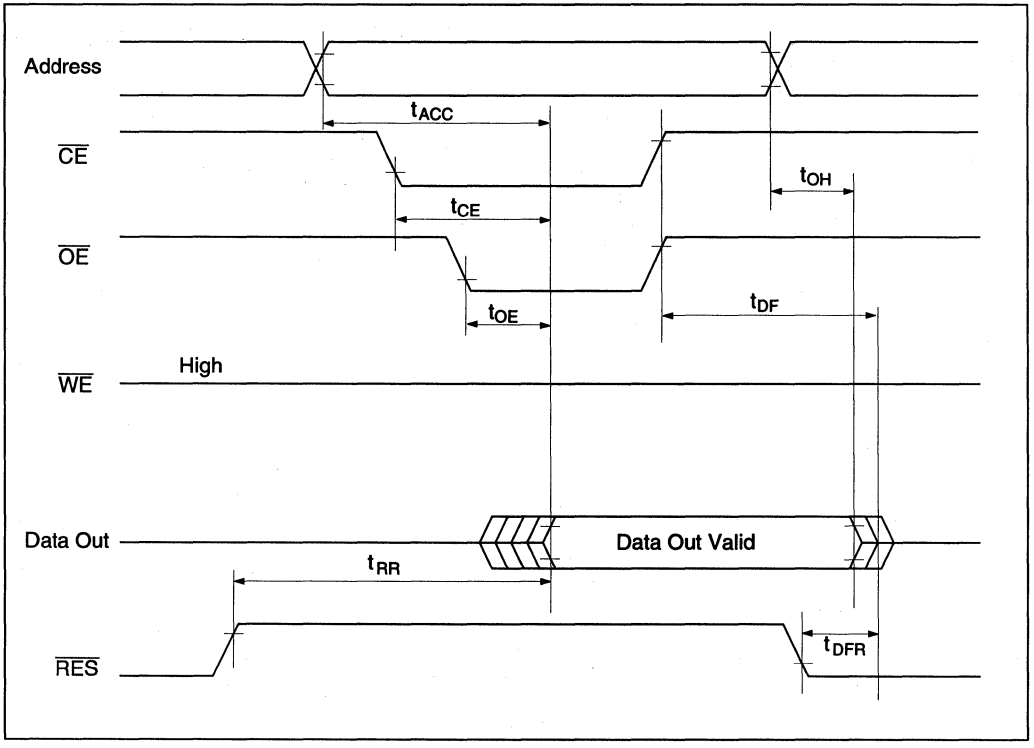
- Input pulse levels : 0.4 V to 2.4 V
  0 V to V_{CC} ($\overline{RES}$ pin)
- Input rise and fall time : ≤ 20 ns
- Output load : 1TTL Gate +100 pF
- Reference levels for measuring timing : 0.8 V, 1.8 V

Read Cycle

Parameter	Symbol	Min	Max	Unit	Test conditions
Address to output delay	t_{ACC}	—	250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{CE}$ to output delay	t_{CE}	—	250	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ to output delay	t_{OE}	10	120	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Address to output hold	t_{OH}	0	—	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{OE}$ ($\overline{CE}$) high to output float*1	t_{DF}	0	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ low to output float*1	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to output delay	t_{RR}	0	600	ns	$\overline{CE}$ = $\overline{OE}$= V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} and t_{DFR} are defined as the time at which the outputs achieve the open circuit conditions and are no longer driven.

Read Timing Waveform



Write Cycle

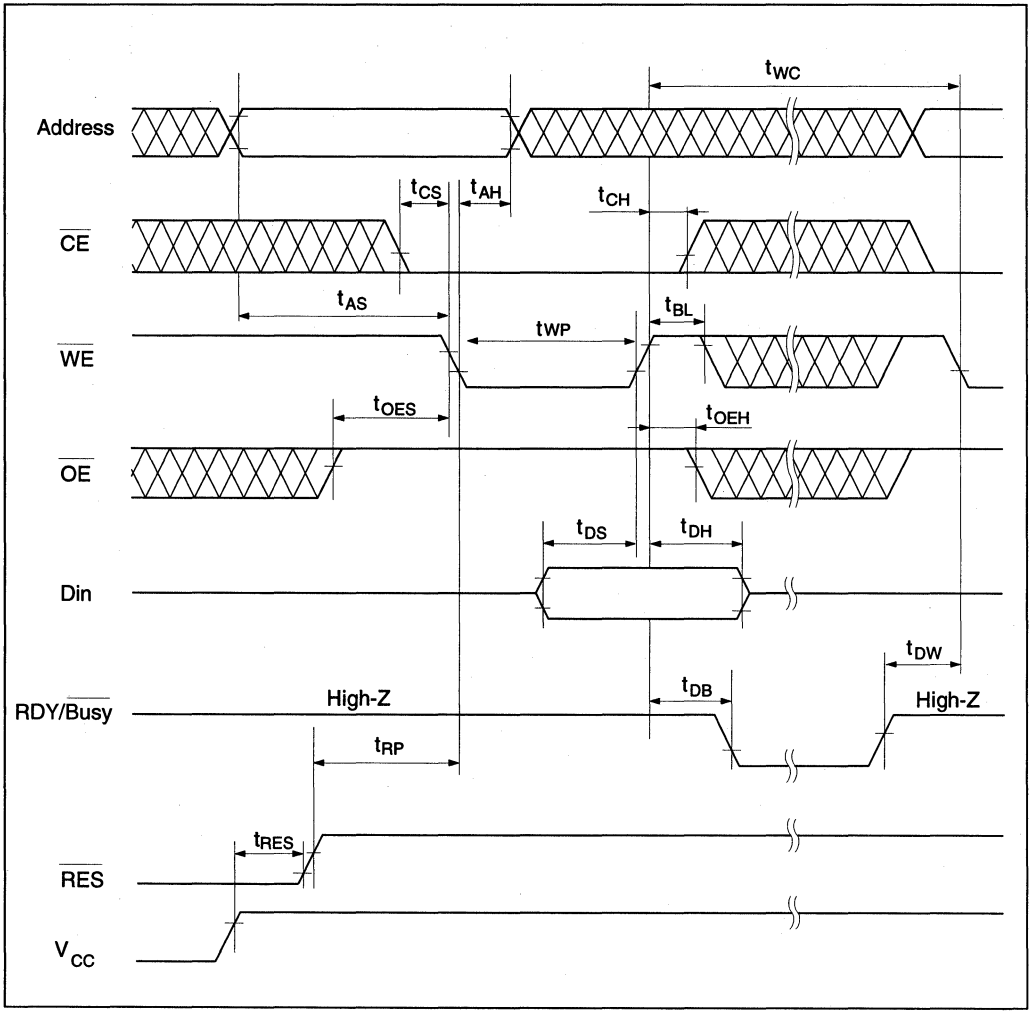
Parameter	Symbol	Min*1	Typ	Max	Unit	Test conditions
Address setup time	t_{AS}	0	—	—	ns	
Address hold time	t_{AH}	150	—	—	ns	
$\overline{CE}$ to write setup time ($\overline{WE}$ controlled)	t_{CS}	0	—	—	ns	
$\overline{CE}$ hold time ($\overline{WE}$ controlled)	t_{CH}	0	—	—	ns	
$\overline{WE}$ to write setup time ($\overline{CE}$ controlled)	t_{WS}	0	—	—	ns	
$\overline{WE}$ hold time ($\overline{CE}$ controlled)	t_{WH}	0	—	—	ns	
$\overline{OE}$ to write setup time	t_{OES}	0	—	—	ns	
$\overline{OE}$ hold time	t_{OEH}	0	—	—	ns	
Data setup time	t_{DS}	100	—	—	ns	
Data hold time	t_{DH}	10	—	—	ns	
$\overline{WE}$ pulse width ($\overline{WE}$ controlled)	t_{WP}	250	—	—	ns	
$\overline{CE}$ pulse width ($\overline{CE}$ controlled)	t_{CW}	250	—	—	ns	
Data latch time	t_{DL}	750	—	—	ns	
Byte load cycle	t_{BLC}	1.0	—	30	µs	
Byte load window	t_{BL}	100	—	—	µs	
Write cycle time	t_{WC}	—	—	15*2	ms	
Time to device busy	t_{DB}	120	—	—	ns	
Write start time	t_{DW}	250*3	—	—	ns	
Reset protect time	t_{RP}	100	—	—	µs	
Reset low time	t_{RES}	1	—	—	µs	

Note: 1. Use this device in longer cycle than this value.

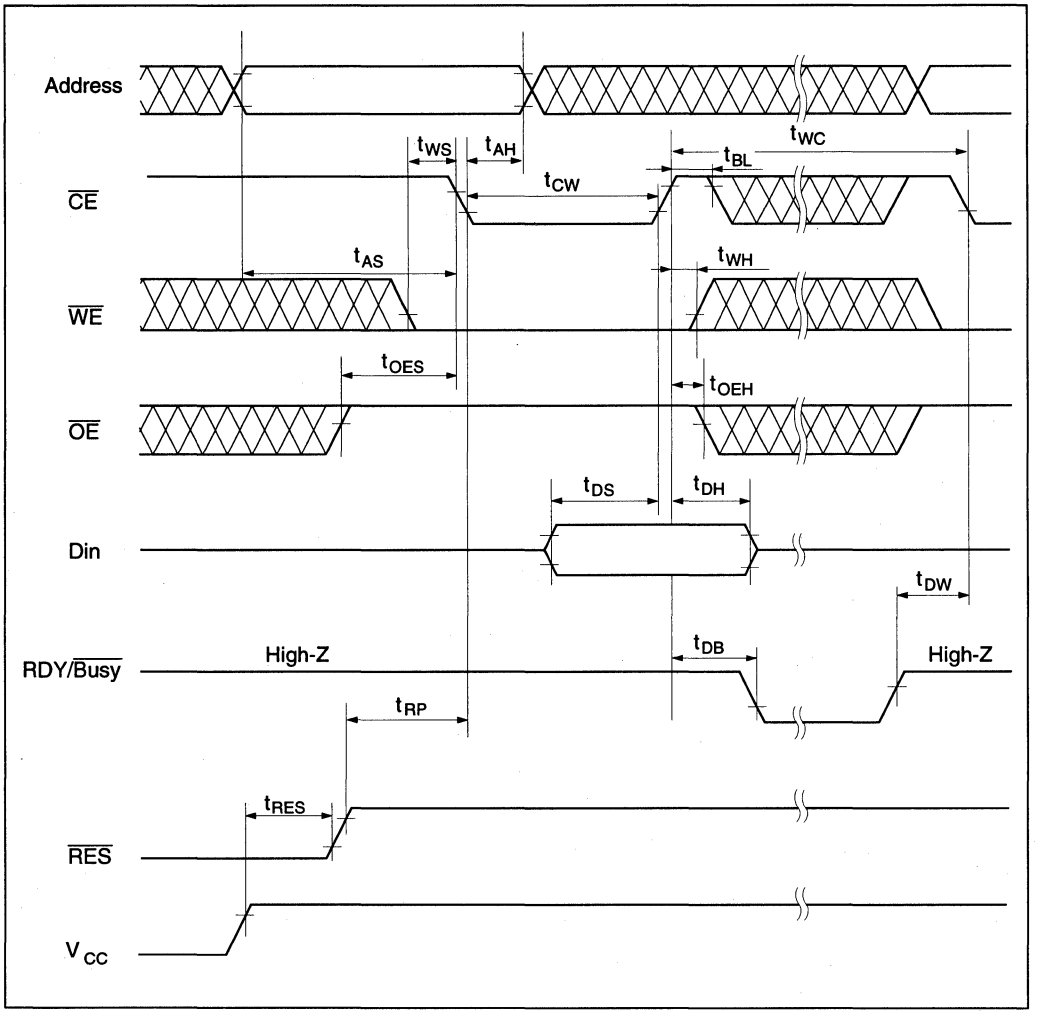
2. t_{WC} must be longer than this value unless polling techniques or RDY/$\overline{Busy}$ are used. This device automatically completes the internal write operation within this value.

3. Next read or write operation can be initiated after t_{DW} if polling techniques or RDY/$\overline{Busy}$ are used.Read Timing Waveform (2)*3 *4 *6

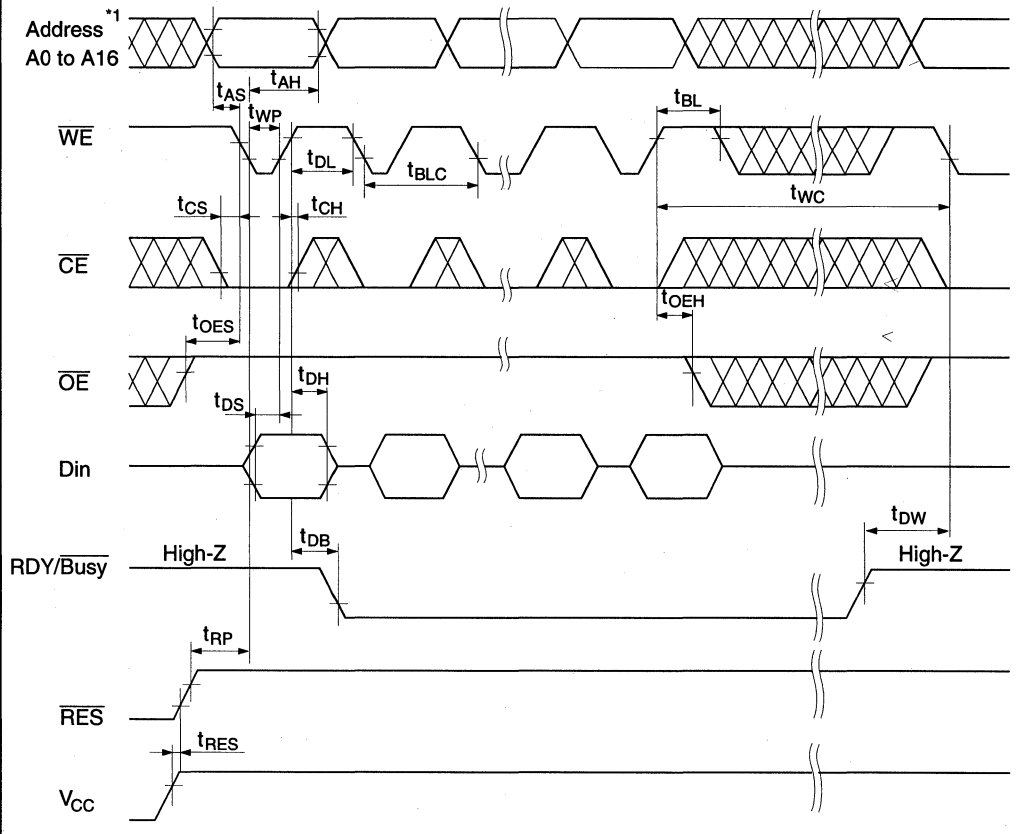
Byte Write TimingWaveform(1) ($\overline{WE}$ Controlled)



Byte Write TimingWaveform(2) ($\overline{CE}$ Controlled)

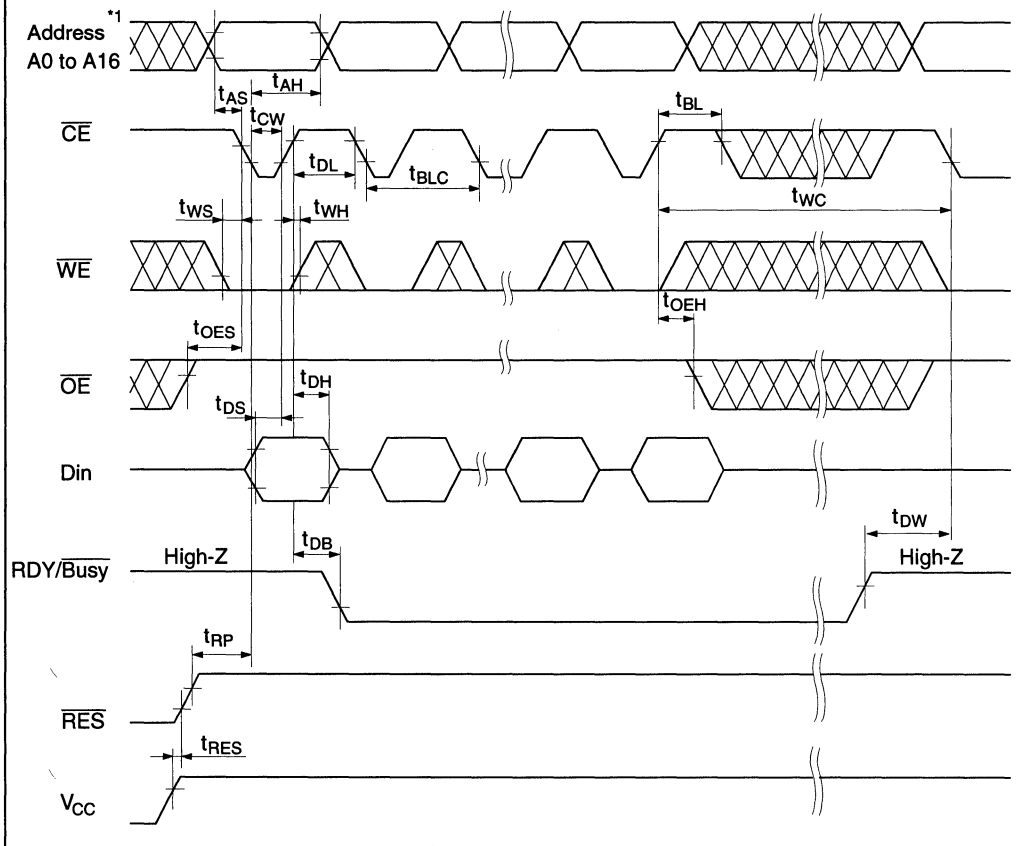


Page Write Timing Waveform (1) ($\overline{WE}$ Controlled)



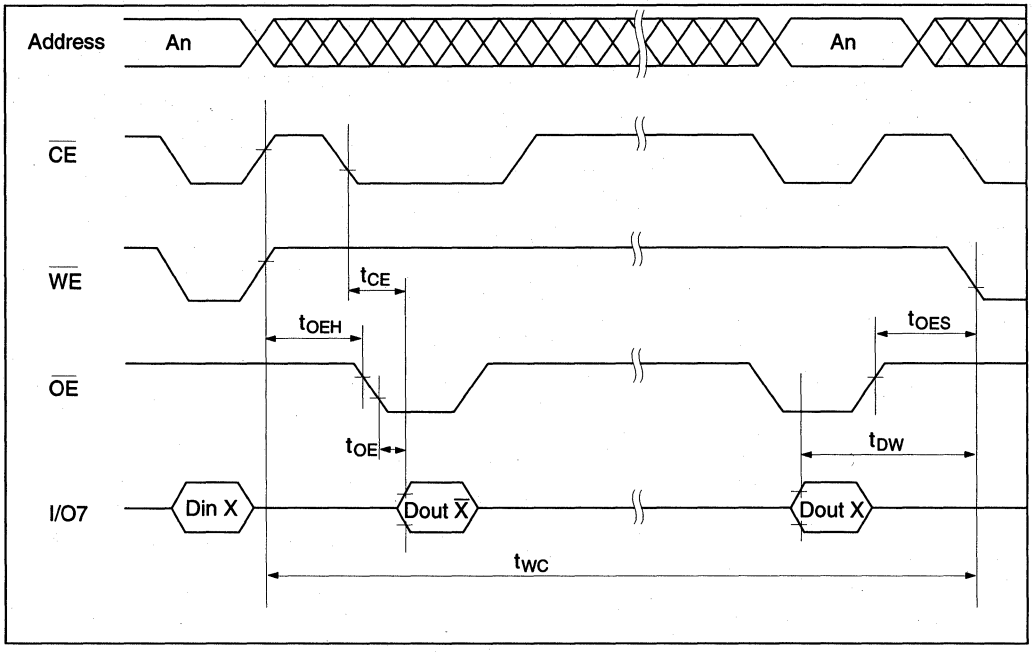
Note: 1. A7 to A16 are page addresses and must be same within the page write operation.

Page Write Timing Waveform (2) ($\overline{CE}$ Controlled)



Note: 1. A7 to A16 are page addresses and must be same within the page write operation.

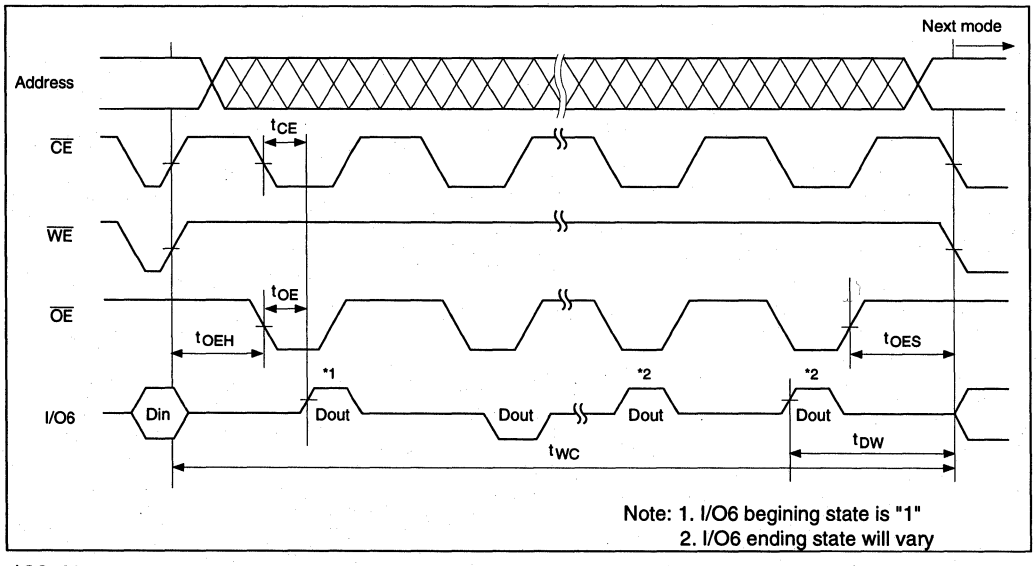
$\overline{\text{Data}}$ Polling Timing Waveform



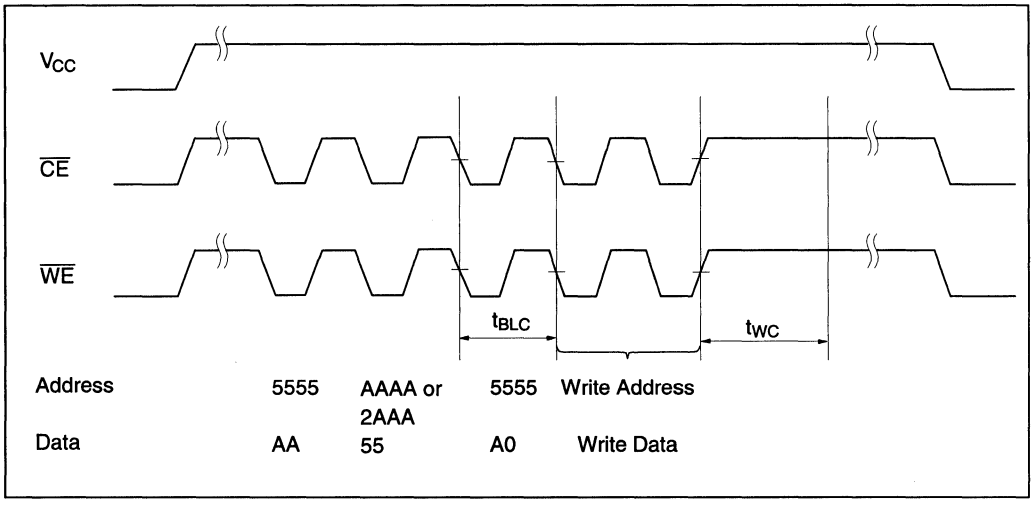
Toggle bit

This device provide another function to determine the internal programming cycle. If the EEPROM set to read mode during the internal programming cycle, I/O6 will charge from "1" to "0" (toggling) for each read. When the internal programming cycle is finished, toggling of I/O6 will stop and the device can be accessible for next read or program.

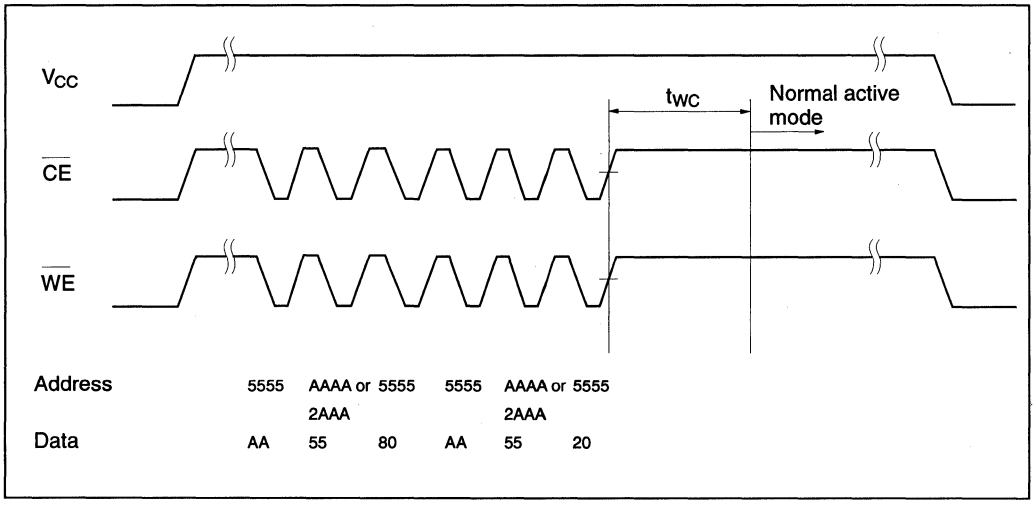
Toggle Bit Waveform



Software Data Protection Timing Waveform (1) (in protection mode)



Software Data Protection Timing Waveform (2) (in non-protection mode)



Functional Description

Automatic Page Write

Page-mode write feature allows 1 to 128 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 128 bytes can be written in the same manner. Each additional byte load cycle must be started within 30 µs from the preceding falling edge of $\overline{WE}$ or $\overline{CE}$. When $\overline{CE}$ or $\overline{WE}$ is kept high for 100 µs after data input, the EEPROM enters write mode automatically and the input data are written into the EEPROM.

$\overline{\text{Data}}$ Polling

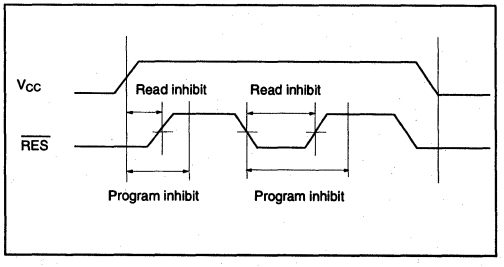
$\overline{\text{Data}}$ polling allows the status of the EEPROM to be determined. If EEPROM is set to read mode during a write cycle, an inversion of the last byte of data to be loaded outputs from I/O7 to indicate that the EEPROM is performing a write operartion.

RDY/$\overline{\text{Busy}}$ Signal

RDY/$\overline{\text{Busy}}$ signal also allows status of the EEPROM to be determined. The RDY/$\overline{\text{Busy}}$ signal has high impedance except in write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, the RDY/$\overline{\text{Busy}}$ signal changes state to high impedance.

$\overline{\text{RES}}$ Signal

When $\overline{\text{RES}}$ is low, the EEPROMcannot be read or programmed. Therefore, data can be protected by keeping $\overline{\text{RES}}$ low when V_{CC} is switched. $\overline{\text{RES}}$ should be high during read and programming because it dosen't provide a latch function.



$\overline{\text{WE}}$,$\overline{\text{CE}}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

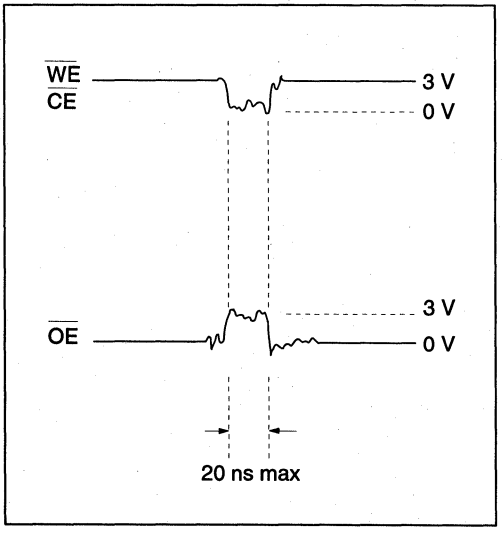
Write/Erase Endurance and Data Retention Time

The endurance is 10^4 cycles in case of the page programming and 10^3 cycles in case of the byte programming (1% cumulative failure rate). The data retention time is more than 10 years when a device is page-programmed less than 10^4 cycles.

Data Protection

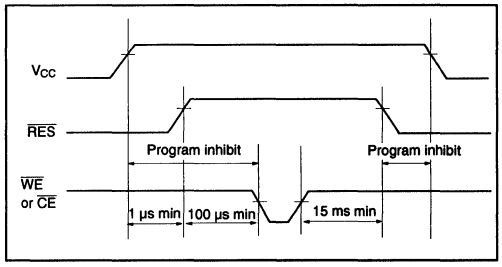
1. Data Protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation

During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake.
To prevent this phenomenon, this device has a noise cancelation function that cuts noise if its width is 20 ns or less in programming mode.
Be careful not to allow noise of a width of more than 20 ns on the control pins.



2. Data protection at V_{CC} on/off

When V_{CC} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in unprogrammable state by using a CPU reset signal to $\overline{RES}$ pin. $\overline{RES}$ pin should be kept at VSS level when V_{CC} is turned on or off.
The EEPROM breaks off programming operation when $\overline{RES}$ becomes low, programming operation doesn't finish correctly in case that $\overline{RES}$ falls low during programming operation. $\overline{RES}$ should be kept high for 15 ms after the last data input.



3. Software data protection

To prevent unintentional programming caused by noise generated by external circuits, This device has the software data protection function. In software data protection mode, 3 bytes of data must be input before write data as follows. And these bytes can switch the non-protection mode to the protection mode.

Address	Data	
5555	AA	
↓	↓	
AAAA or 2AAA	55	
↓	↓	
5555	A0	
↓	↓	
Write address	Write data }	Normal data input

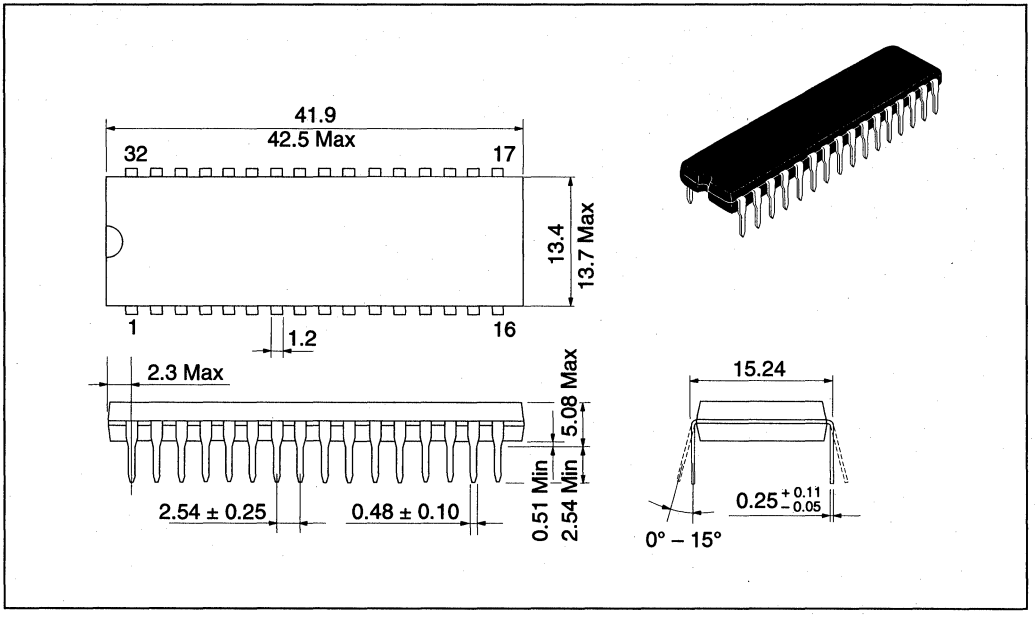
Software data protection mode can be canceled by inputting the following 6 bytes. After that, this device turns to the non-protection mode and can write data normally. But when the data is input in the canceling cycle, the data cannot be written.

Address	Data
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	80
↓	↓
5555	AA
↓	↓
AAAA or 2AAA	55
↓	↓
5555	20

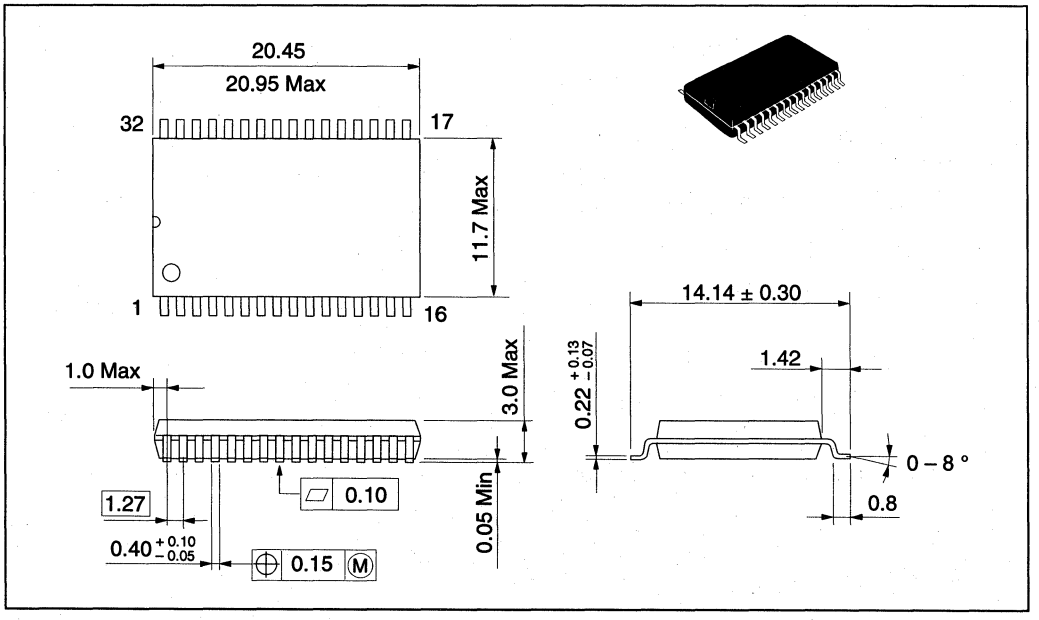
The software data protection is not enabled at the shipment.

Package Dimensions

HN58V1001P Series (DP-32) **Unit : mm**

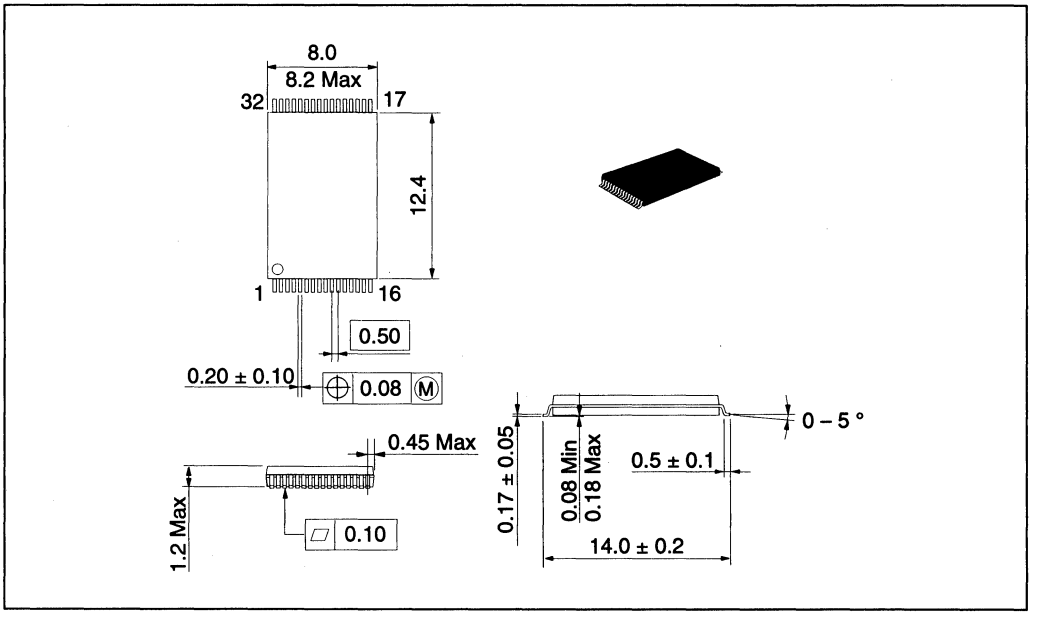


HN58V1001FP Series (FP-32D) **Unit : mm**



Package Dimensions (cont)

HN58V1001T Series (TFP-32DA) **Unit : mm**



Part 2 Mask ROM

4M Mask ROM

HN62434 Series

262,144-word × 16-bit / 524,288-word × 8-bit CMOS Programmable Mask ROM

HITACHI

Rev. 2.0
September 12, 1995

The HN62434 is a 4-Mbit CMOS Programmable Mask ROM organized either as 262,144 words by 16 bits or as 524,288 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation.

Features

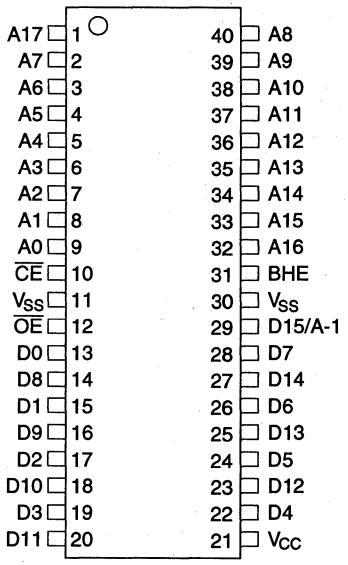
- Single +5 V power supply
- Access time: 120/150 ns (max)
- Low power consumption: 100 mW (typ) active
  5 µW (typ) standby
- Byte-wide or word-wide data organization with BHE
- Wired OR is permitted for the output in three status
- TTL compatible

Ordering Information

Type No.	Access time	Package
HN62434P-12 HN62434P-15	120 ns 150 ns	600 mil 40-pin plastic DIP (DP-40)
HN62434F-12 HN62434F-15	120 ns 150 ns	48-pin plastic SOP (FP-48DA)
HN62434FA-12 HN62434FA-15	120 ns 150 ns	40-pin plastic SOP (FP-40D)
HN62434TT-12 HN62434TT-15	120 ns 150 ns	44-pin plastic TSOP II (TTP-44D)

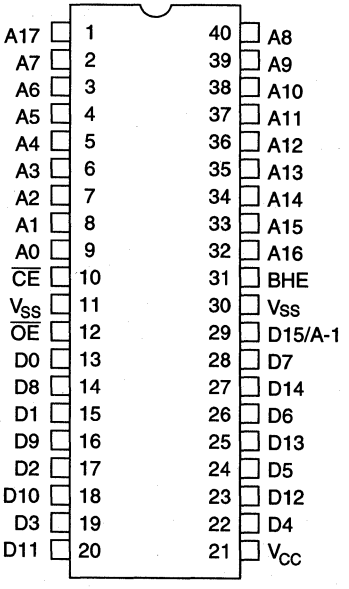
Pin Arrangement

HN62434P Series



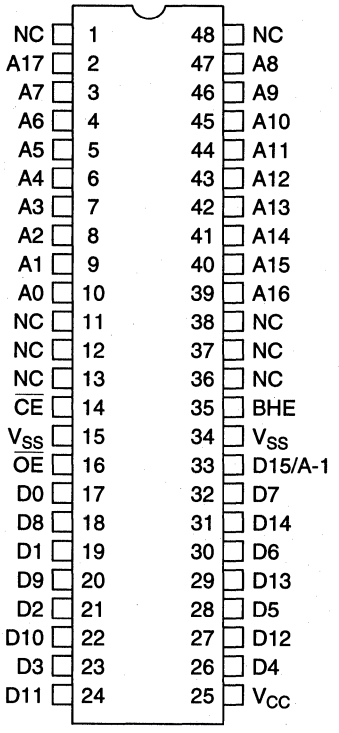
(Top View)

HN62434FA Series



(Top View)

HN62434F Series

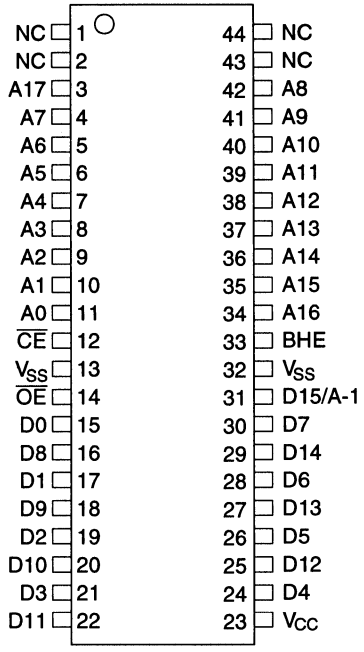


(Top View)

11-12-13 pin and 36-37-38 pin are connected to inner lead frame.

Pin Arrangement (cont.)

HN62434TT Series

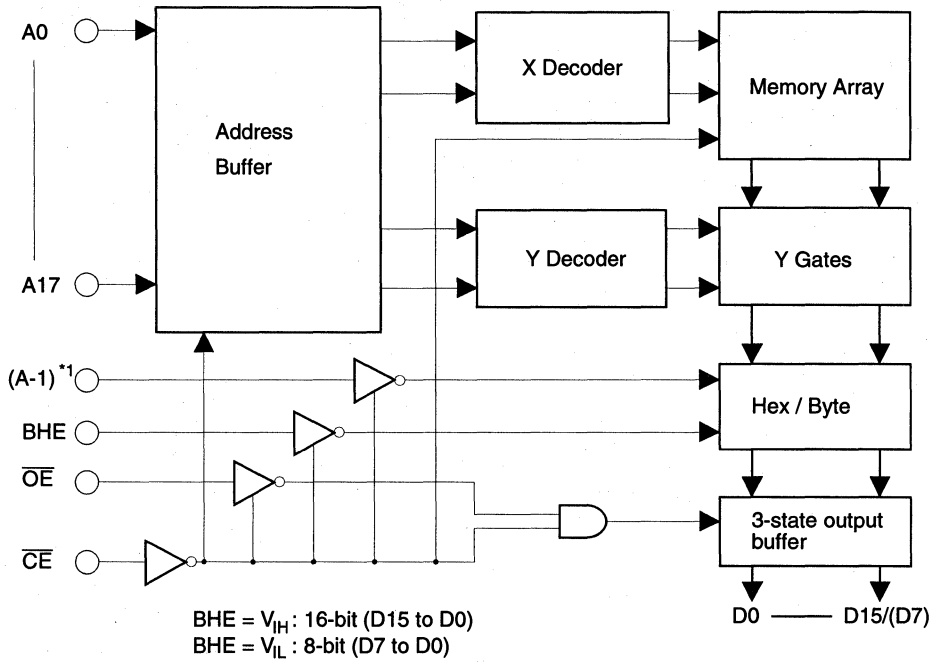


(Top View)

Pin Description

Pin name	Function
A0 to A17	Address input
D0 to D14	Data out
D15/A-1	Data out/address input
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
BHE	Byte/word select
NC	No connection
V_{CC}	Power (+5 V)
V_{SS}	Ground

Block Diagram



Note: 1. A-1 is least significant address.
When BHE is 'low', D14 to D8 goes the high impedance state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	–0.3 to +7.0	V	1
All input and output voltage	Vin, Vout	–0.3 to V_{CC} + 0.3	V	1
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, IDout = 0 mA, t_{RC} = Min
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
		I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\|I_{LI}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{LO}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = +25°C, Vin = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70 °C)

Test Condition

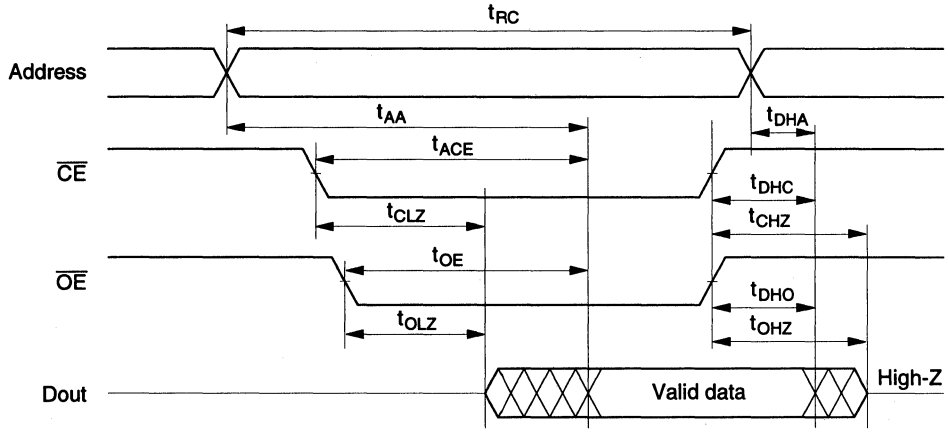
- Output load: 1 TTL gate + C_L = 100 pF (including jig)
- Input pulse level: 0.8 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 10 ns

		HN62434-12		HN62434-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	120	—	150	—	ns	
Address access time	t_{AA}	—	120	—	150	ns	
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	60	—	70	ns	
BHE access time	t_{BHE}	—	120	—	150	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	0	—	ns	
$\overline{CE}$ to output in high Z	t_{CHZ}	—	60	—	70	ns	1
$\overline{OE}$ to output in high Z	t_{OHZ}	—	60	—	70	ns	1
BHE to output in high Z	t_{BHZ}	—	60	—	70	ns	1
$\overline{CE}$ to output in low Z	t_{CLZ}	5	—	10	—	ns	
$\overline{OE}$ to output in low Z	t_{OLZ}	5	—	10	—	ns	
BHE to output in low Z	t_{BLZ}	5	—	10	—	ns	

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

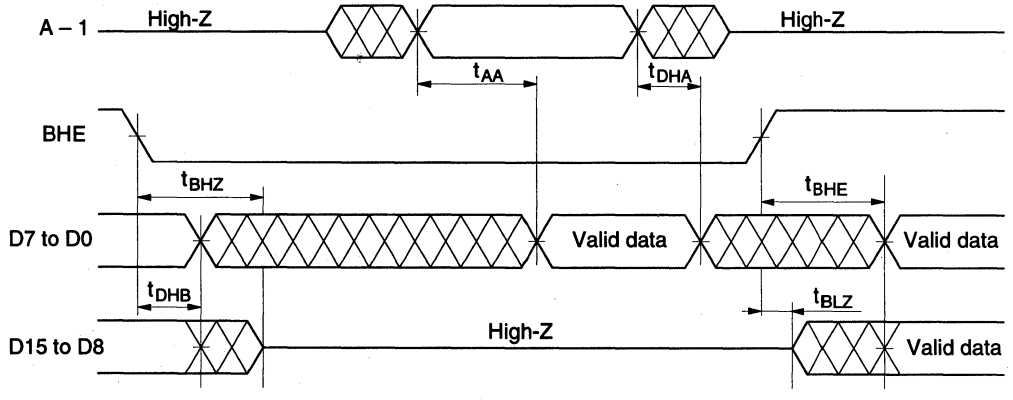
Timing Waveform

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



Note: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

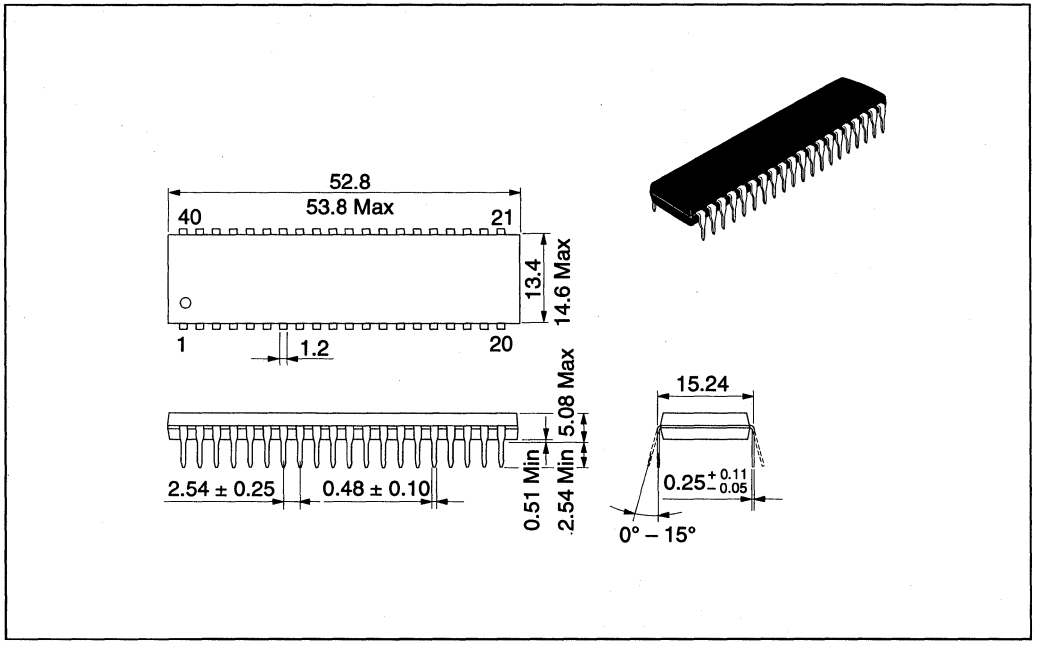
Word Mode, Byte Mode Switch



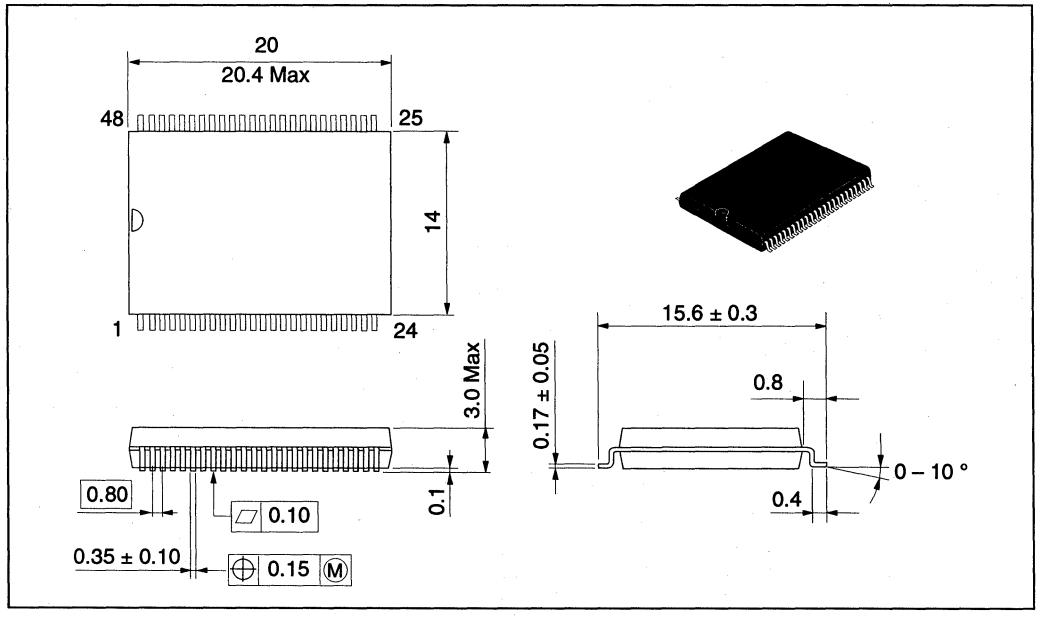
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable A17 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

Package Dimensions

HN62434P Series (DP-40) **Unit: mm**

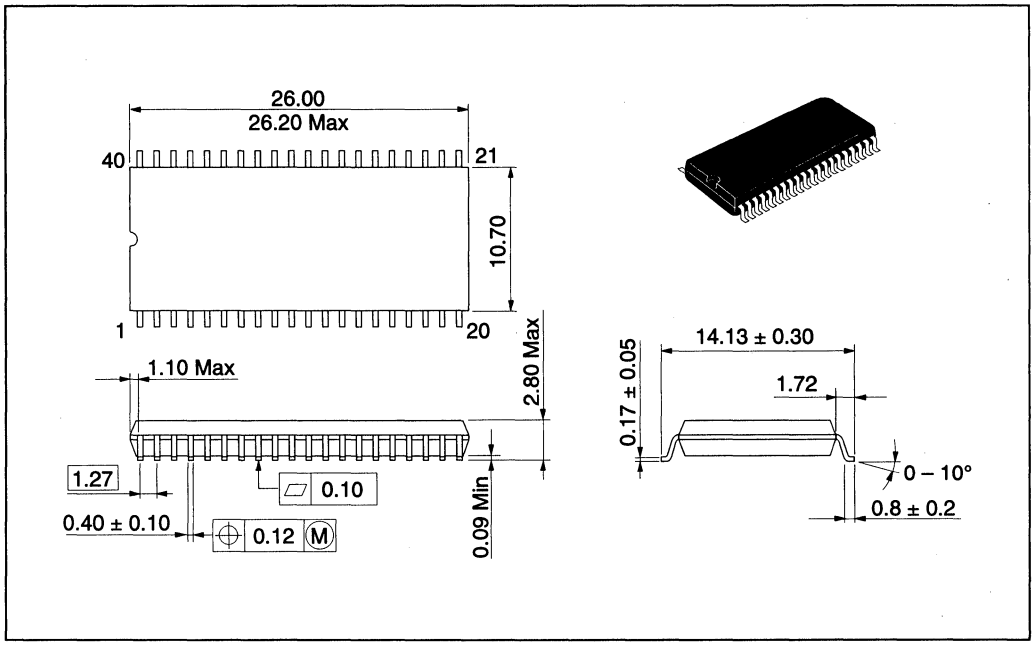


HN62434F Series (FP-48DA) **Unit: mm**

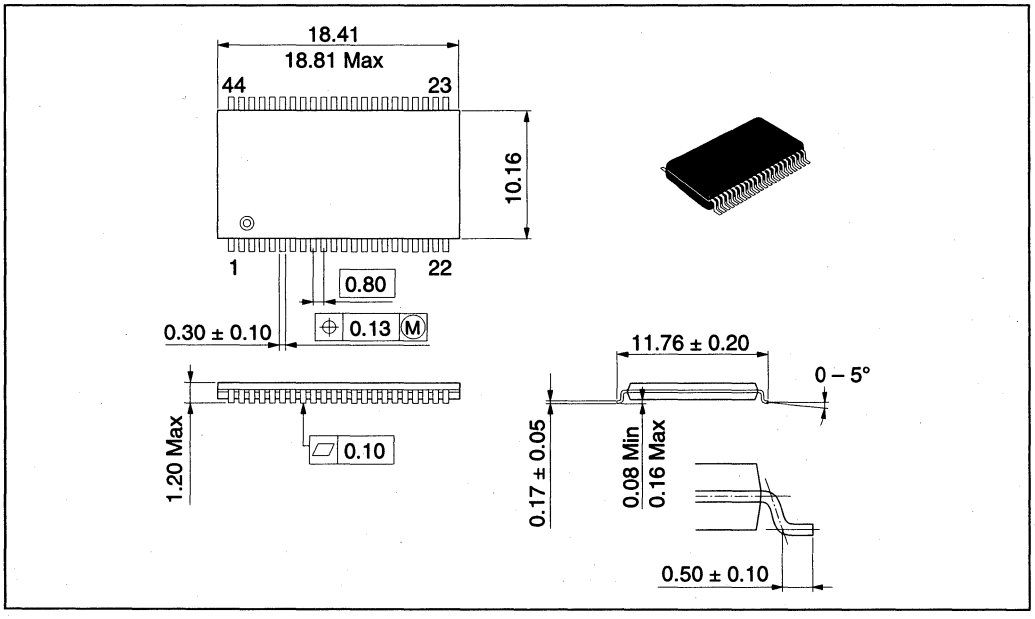


Package Dimensions (cont.)

HN62434FA Series (FP-40D) **Unit: mm**



HN62434TT Series (TTP-44D) **Unit: mm**



HN62435 Series

262,144-word × 16-bit / 524,288-word × 8-bit CMOS Programmable Mask ROM

HITACHI

Rev. 1.0
November 16, 1995

The HN62435 is a 4-Mbit CMOS Programmable Mask ROM organized either as 262,144 words by 16 bits or 524,288 words by 8 bits.

Realizing low power consumption, this memory is allowed for battery operation.

Features

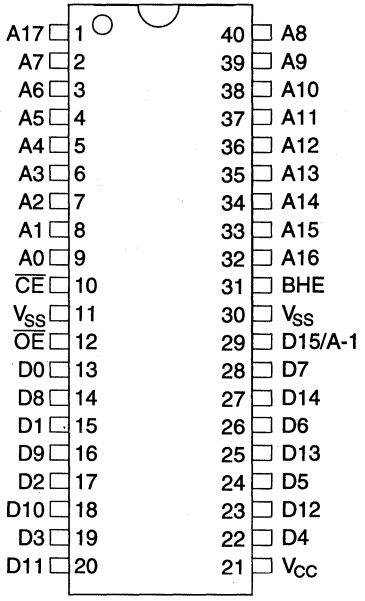
- Single 5 V supply
- High speed
  Access time: 120/150 ns (max)
- Low power
  Active: 275 mW (max)
  Standby: 165 µW (max)
- Byte-wide or word-wide data organization
  (Switched by BHE terminal)
- Three-state data output for or-tying
- Directly TTL compatible
  All inputs and outputs
- Pin compatible with 4 Mbit EPROM
  (HN27C4000G/FP)

Ordering Information

Type No.	Access time	Package
HN62435P-12 HN62435P-15	120 ns 150 ns	600 mil 40-pin plastic DIP (DP-40)
HN62435FA-12 HN62435FA-15	120 ns 150 ns	525 mil 40-pin plastic SOP (FP-40D)
HN62435TT-12 HN62435TT-15	120 ns 150 ns	400 mil 44-pin plastic TSOP II (TTP-44D)

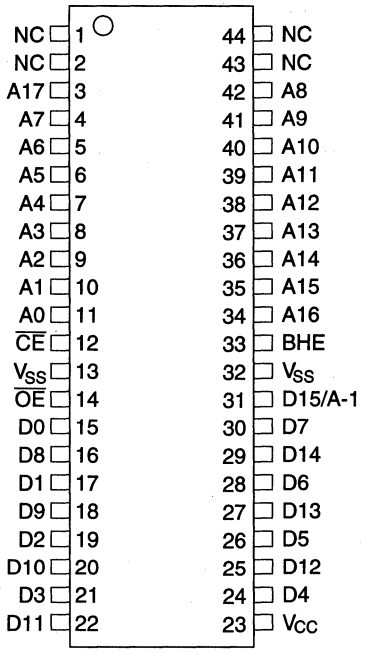
Pin Arrangement

HN62435P Series
HN62435FA Series



(Top View)

HN62435TT Series

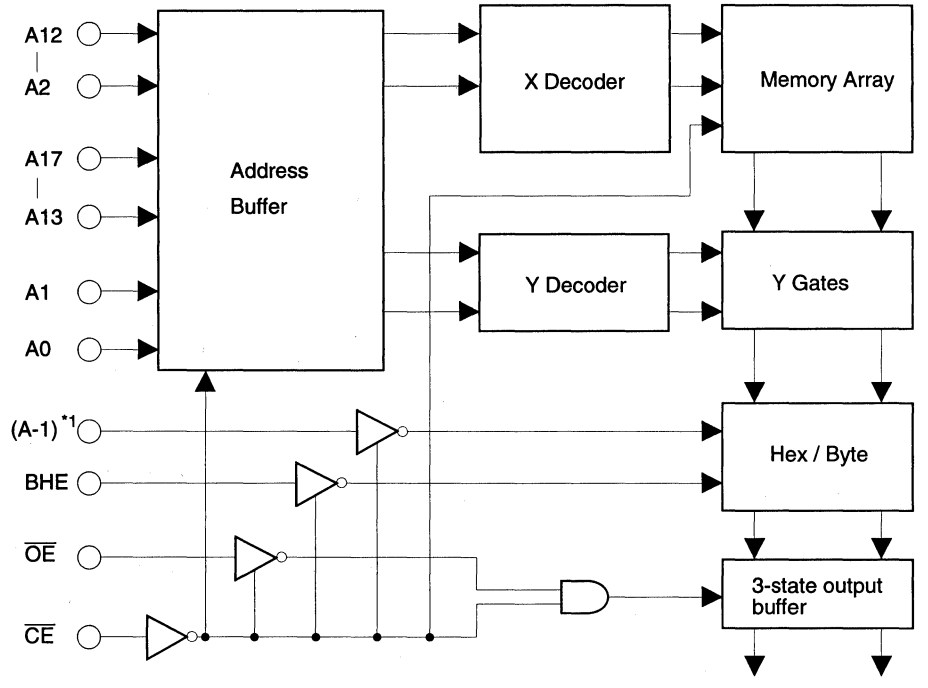


(Top View)

Pin Description

Symbol	Function
A-1, A0 to A17	Address inputs
D0 to D15	Data outputs
BHE	8/16 bit (byte/word) mode switch
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



BHE = V_{IH}: 16-bit (D15 to D0)
BHE = V_{IL} : 8-bit (D7 to D0)

Note: 1. A-1 is least significant address.

When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.

Mode Selection

	Pin							
					Data output		Address input	
Mode	$\overline{CE}$	$\overline{OE}$	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	×*1	×	×	High-Z*2	High-Z	—	—
Output disable	L	H	×	×	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A17
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A17
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A17

Notes: 1. ×: Don't care.
2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{CC}	− 0.3 to + 7.0	V
All input and output voltage*1	Vin, Vout	− 0.3 to V_{CC} + 0.3	V
Operating temperature range	Topr	0 to + 70	°C
Storage temperature range	Tstg	− 55 to + 125	°C
Temperature under bias	Tbias	− 20 to + 85	°C

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	− 0.3	—	0.8	V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

Parameter		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ - 0.2 V
	Standby	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = – 205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

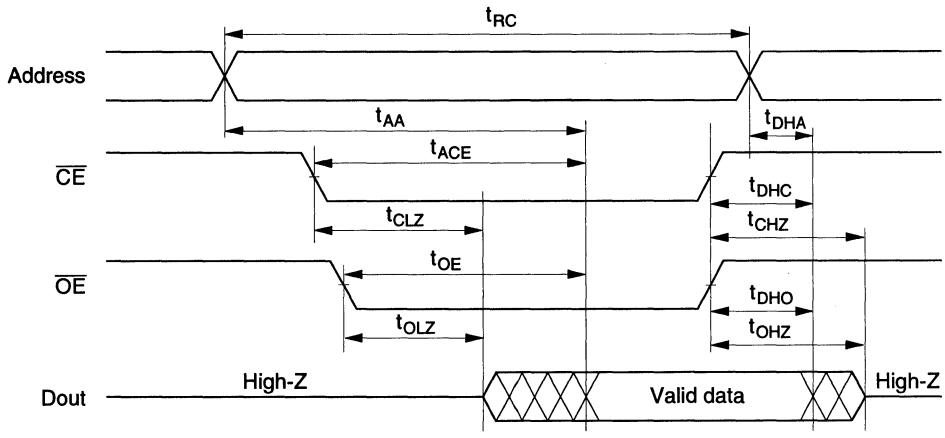
- Output load: 1TTL + C_L = 100 pF (including jig)
- Input pulse level: 0.6 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 5ns

		HN62435-12		HN62435-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	120	—	150	—	ns	
Address access time	t_{AA}	—	120	—	150	ns	
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	60	—	70	ns	
BHE access time	t_{BHE}	—	120	—	150	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	60	—	70	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	60	—	70	ns	1
BHE to output in high-Z	t_{BHZ}	—	60	—	70	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns	

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

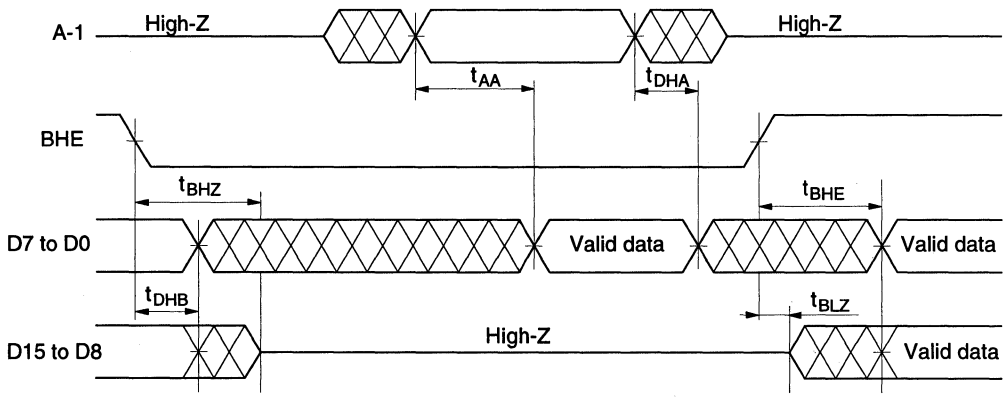
Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

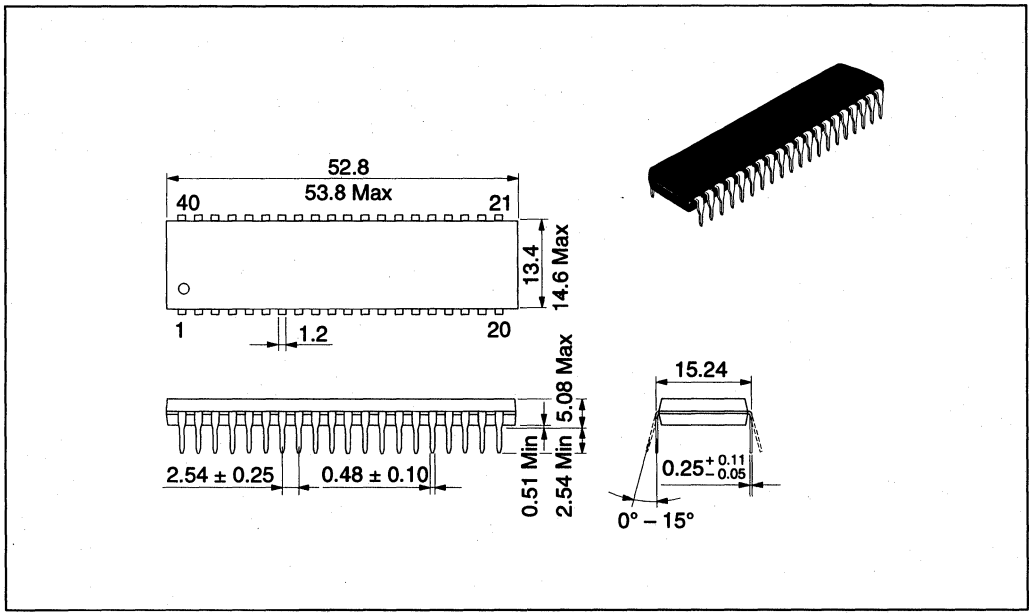
Word Mode, Byte Mode Switch



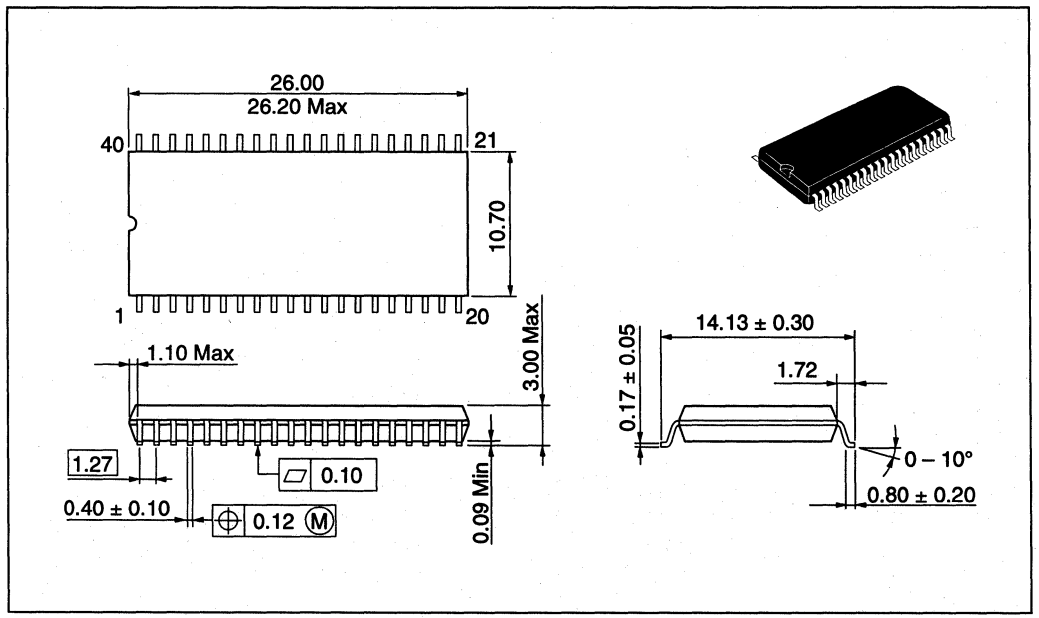
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable, A19 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

Package Dimensions

HN62435P Series (DP-40) **Unit: mm**

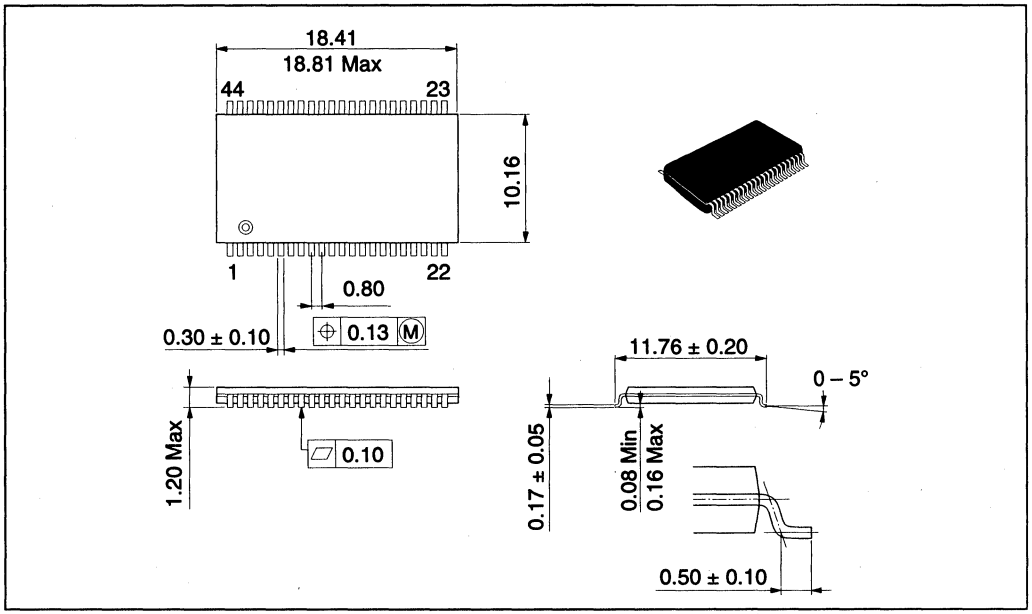


HN62435FA Series (FP-40D) **Unit: mm**



Package Dimensions (cont)

HN62435TT Series (TTP-44D) **Unit: mm**



ADE-203-402A (Z)

HN62454 Series

524,288-word × 8-bit / 262,144-word × 16-bit CMOS Programmable Mask ROM

HITACHI

Preliminary
Rev. 0.1
July 19, 1995

The HN62454 is a 4-Mbit CMOS Programmable Mask ROM organized either as 262,144 words by 16 bits or 524,288 words by 8 bits.

Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 85/100 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Features

- Single 5 V supply
- High speed
  Normal access time: 85/100 ns (max)
- Low power
  Active: 440 mW (max)
  Standby: 165 µW (max)
- Byte-wide or word-wide data organization
  (Switched by BHE terminal)
- Three-state data output for or-tying
- Directly TTL compatible
  All inputs and outputs
- Pin compatible with 4 Mbit EPROM
  (HN27C4000G/FP)

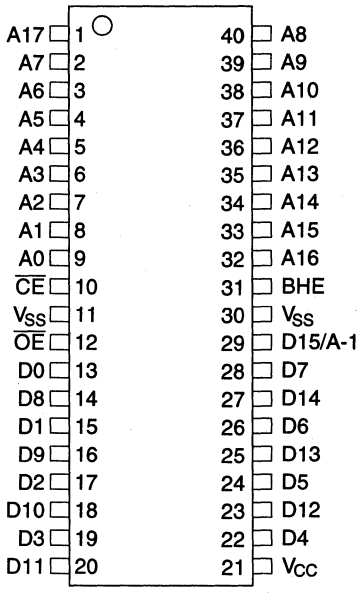
Ordering Information

Type No.	Access time	Package
HN62454P-85 HN62454P-10	85 ns 100 ns	600 mil 40-pin plastic DIP (DP-40)
HN62454FA-85 HN62454FA-10	85 ns 100 ns	525 mil 40-pin plastic SOP (FP-40D)
HN62454TT-85 HN62454TT-10	85 ns 100 ns	400 mil 44-pin plastic TSOP II (TTP-44D)

Preliminary: This document contains information on a new product. Specifiactions and information contained herein are subject to change without notice.

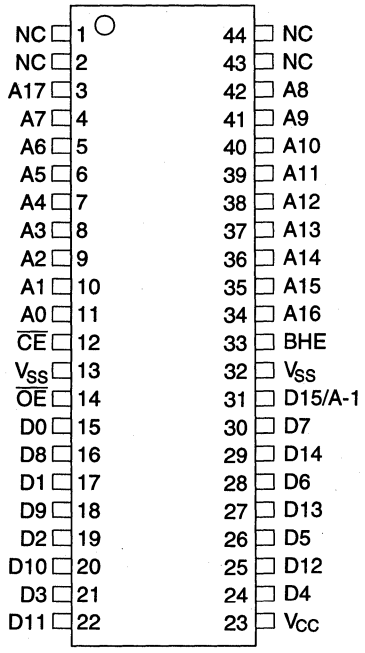
Pin Arrangement

HN62454PSeries



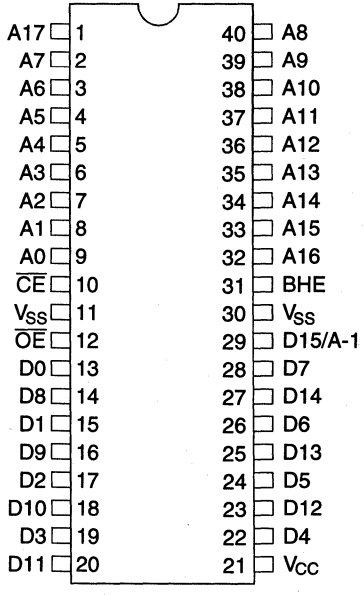
(Top View)

HN62454TT Series



(Top View)

HN62454FA Series

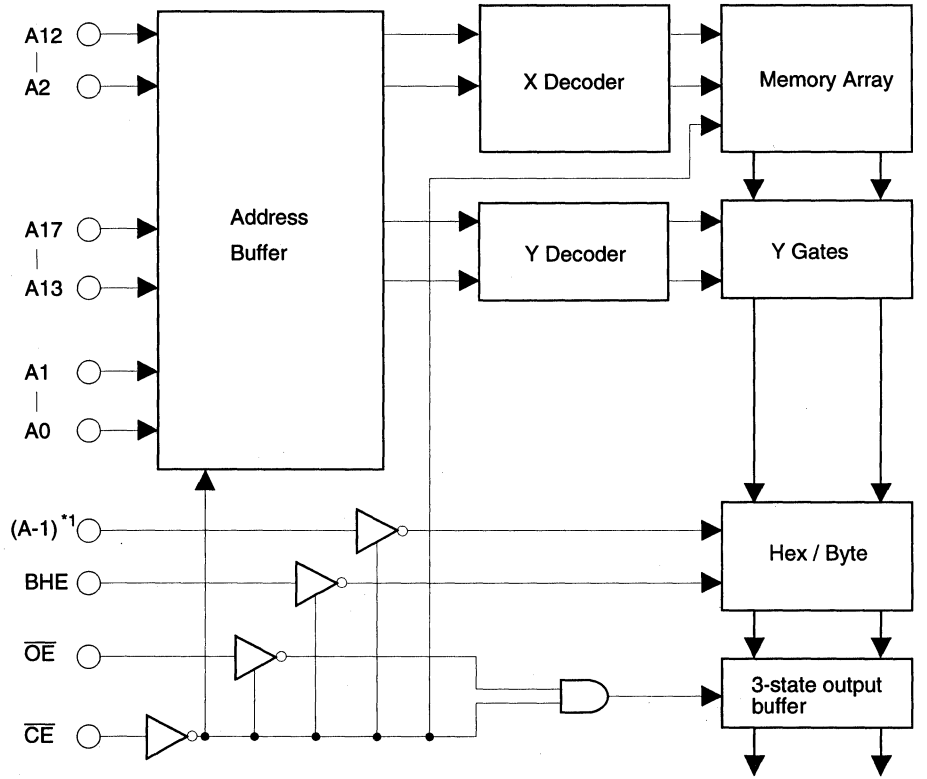


(Top View)

Pin Description

Symbol	Function
A-1, A0 to A17	Address inputs
D0 to D15	Data outputs
BHE	8/16 bit (byte/word) mode switch
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



BHE = V_{IH}: 16-bit (D15 to D0)
BHE = V_{IL} : 8-bit (D7 to D0)

Note: 1. A-1 is least significant address.

When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.

Mode Selection

	Pin							
					Data output		Address input	
Mode	$\overline{CE}$	$\overline{OE}$	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	×*1	×	×	High-Z*2	High-Z	—	—
Output disable	L	H	×	×	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A17
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A17
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A17

notes: 1. ×: Don't care.
2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{CC}	− 0.3 to + 7.0	V
All input and output voltage*1	Vin, Vout	− 0.3 to V_{CC} + 0.3	V
Operating temperature range	Topr	0 to + 70	°C
Storage temperature range	Tstg	− 55 to + 125	°C
Temperature under bias	Tbias	− 20 to + 85	°C

Notes: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	− 0.3	—	0.8	V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

Parameter		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{CC}	—	80/60	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = 85/100 ns
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ - 0.2 V
	Standby	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = – 205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

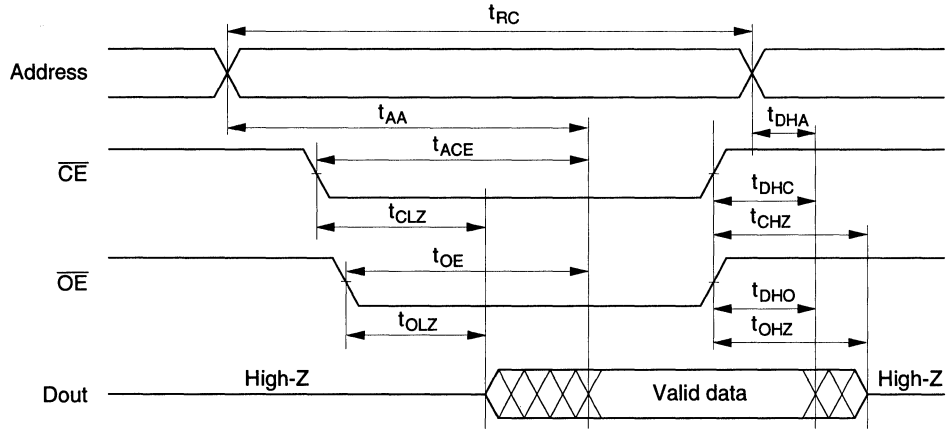
- Output load: 1TTL + C_L = 100 pF (including jig)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 5ns

		HN62454-85		HN62454-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	85	—	100	—	ns	
Address access	t_{AA}	—	85	—	100	ns	
$\overline{CE}$ access time	t_{ACE}	—	85	—	100	ns	
$\overline{OE}$ access time	t_{OE}	—	35	—	40	ns	
BHE access time	t_{BHE}	—	85	—	100	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	30	—	30	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	30	—	30	ns	1
BHE to output in high-Z	t_{BHZ}	—	30	—	30	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns	

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

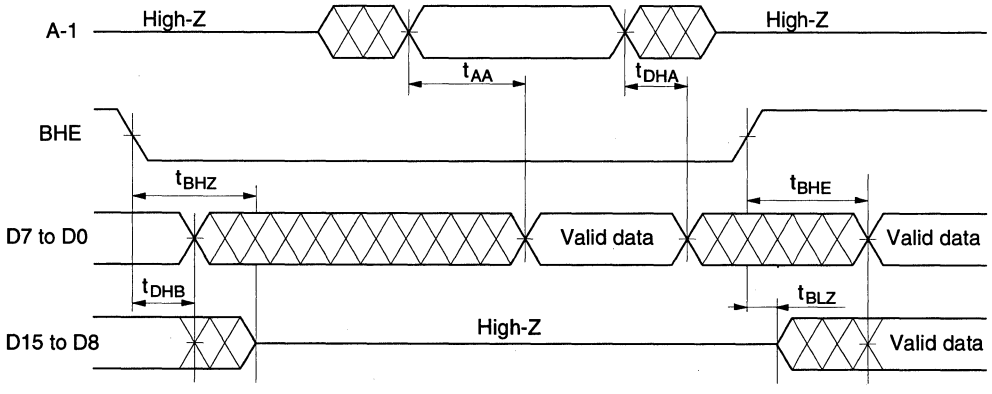
Timing Waveforms

Word mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



Note: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

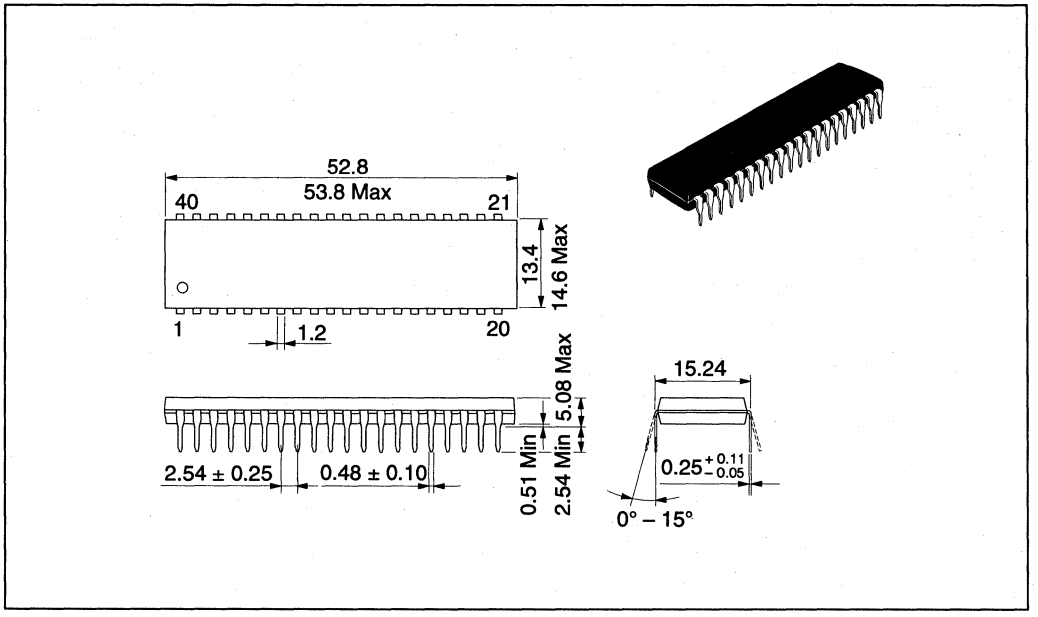
Word Mode, Byte Mode Switch



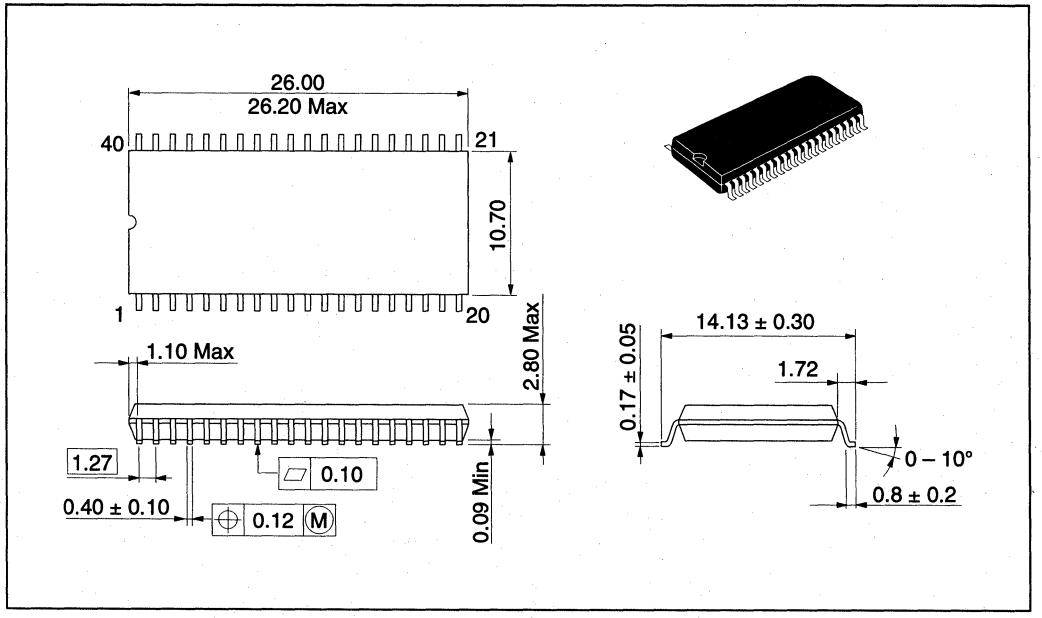
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable A17 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

Package Dimensions

HN62454P Series (DP-40) **Unit: mm**

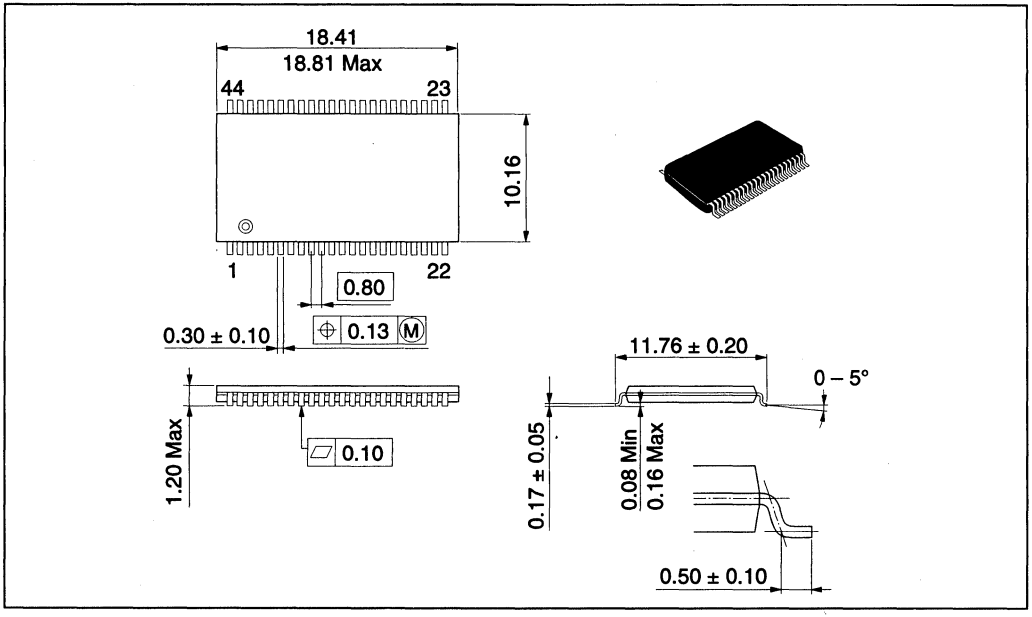


HN62454FA Series (FP-40D) **Unit: mm**



Package Dimensions (cont)

HN62454TT Series (TTP-44D) **Unit: mm**



ADE-203-471 (Z)

HN62454B Series

262,144-word × 16-bit CMOS Programmable Mask ROM

HITACHI

Preliminary
Rev. 0.0
October 25, 1995

The HN62454B is a 262,144 words by 16 bits CMOS Programmable Mask ROM. A high speed access of 85/100 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Features

- Single 5 V supply
- High speed
  Access time: 85/100 ns (max)
- Low power
  Active: 440 mW (max)
  Standby: 165 μW (max)
- Directly TTL compatible
  All inputs and outputs
- Pin compatible with 4 Mbit EPROM
  (HN27C4096G/CC/CP)

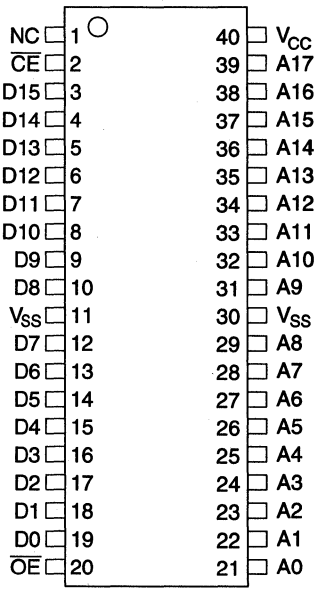
Ordering Information

Type No.	Access time	Package
HN62454BP-85 HN62454BP-10	85 ns 100 ns	600 mil 40-pin plastic DIP (DP-40)
HN62454BCP-85 HN62454BCP-10	85 ns 100 ns	44-pin plastic PLCC (CP-44)

Preliminary: This document contains information on a new product. Specifiactions and information contained herein are subject to change without notice.

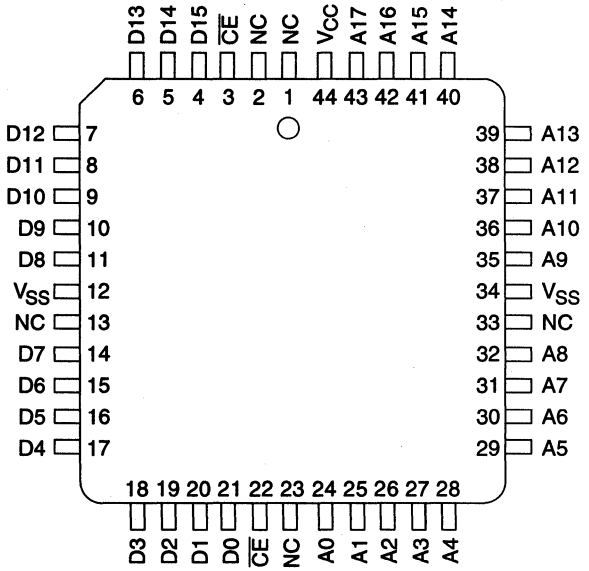
Pin Arrangement

HN62454BPSeries



(Top View)

HN62454BCP Series



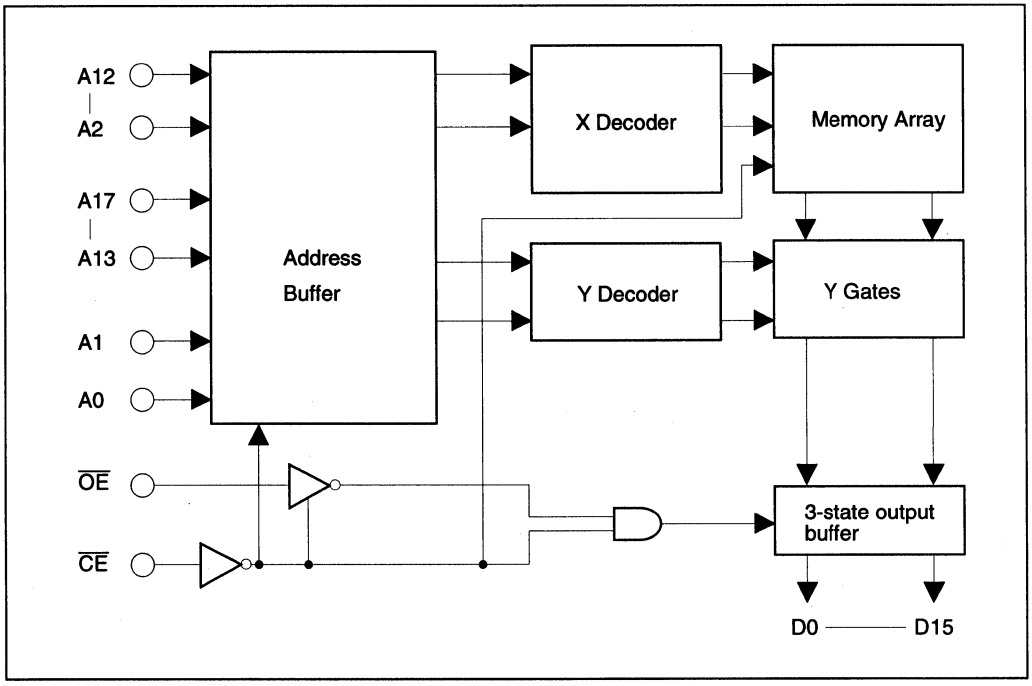
(Top View)

Pin Description

Symbol	Function
A0 to A17	Address inputs
D0 to D15	Data outputs
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable

Symbol	Function
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Mode Selection

	Pin			Address input	
Mode	**$\overline{CE}$**	**$\overline{OE}$**	**Data output**	**LSB**	**MSB**
Standby	H	×*1	High-Z*2	—	—
Output disable	L	H	High-Z	—	—
Read	L	L	Dout	A0	A17

Notes: 1. ×: Don't care.
2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{CC}	– 0.3 to + 7.0	V
All input and output voltage*1	Vin, Vout	– 0.3 to V_{CC} + 0.3	V
Operating temperature range	Topr	0 to + 70	°C
Storage temperature range	Tstg	– 55 to + 125	°C
Temperature under bias	Tbias	– 20 to + 85	°C

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	– 0.3	—	0.8	V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

Parameter		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{CC}	—	80/60	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = 85/100 ns
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
	Standby	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = – 400 µA
		V_{OL}	—	0.4	V	I_{OL} = 2.1 mA

Capacitance (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested.

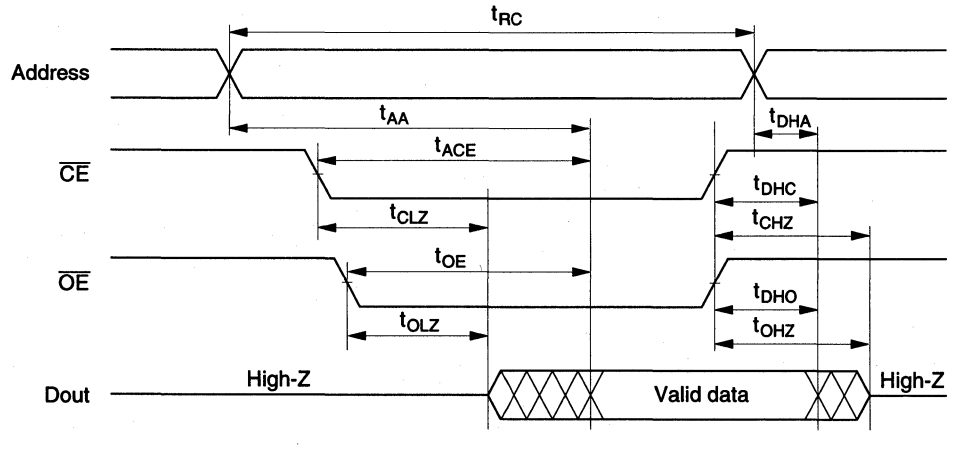
AC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

- Output load: 1TTL + C_L = 100 pF (including jig)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 5 ns

		HN62454B-85		HN62454B-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	85	—	100	—	ns	
Address access	t_{AA}	—	85	—	100	ns	
$\overline{CE}$ access time	t_{ACE}	—	85	—	100	ns	
$\overline{OE}$ access time	t_{OE}	—	35	—	40	ns	
Output hold time from address change	t_{DHA}	5	—	5	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	30	—	30	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	30	—	30	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns	

Note: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

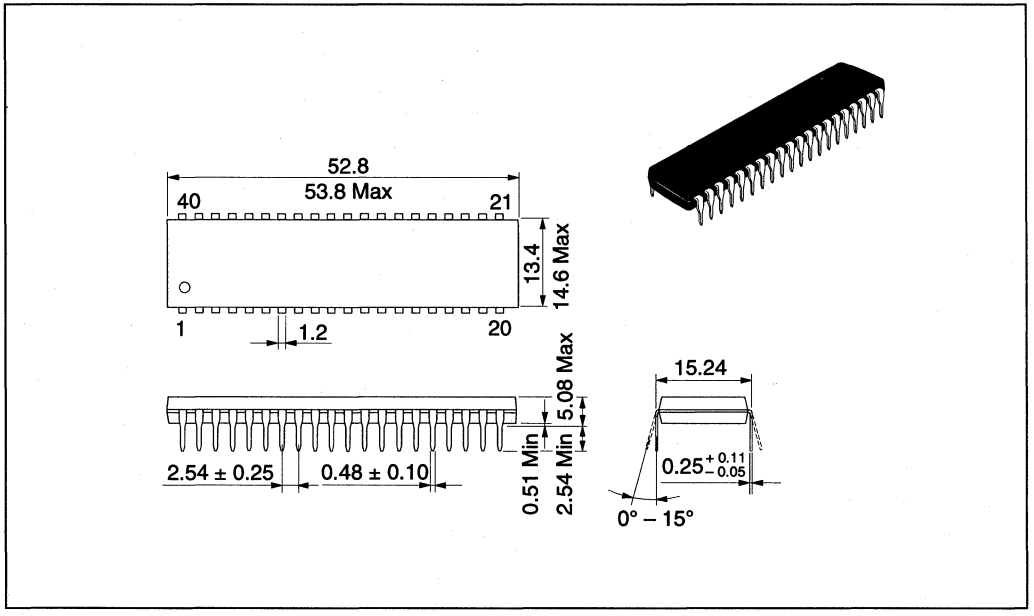
Timing Waveform



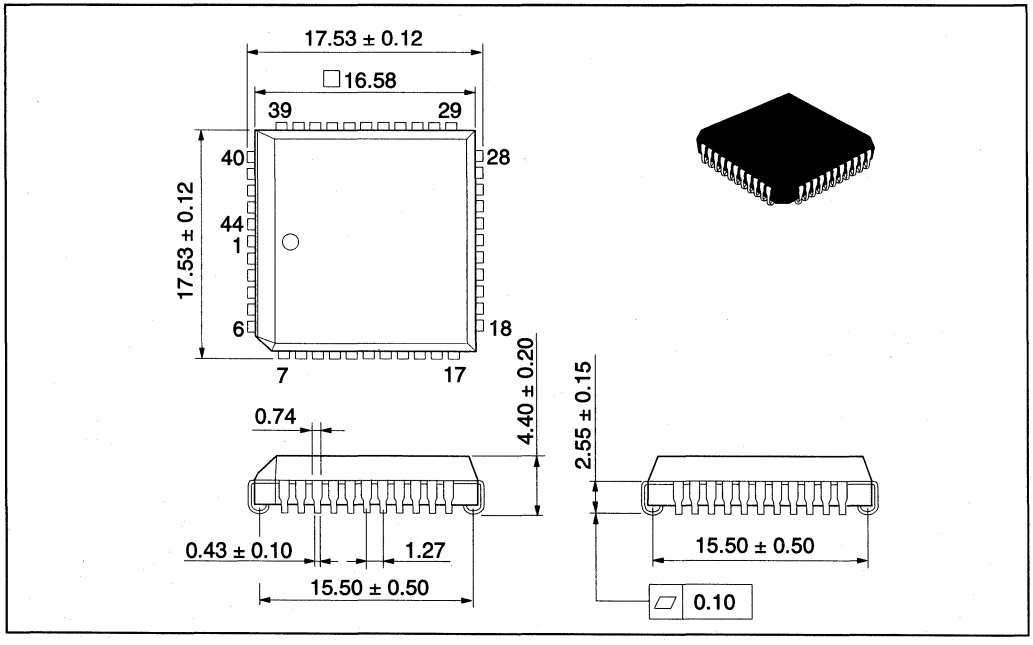
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Package Dimensions

HN62454BP Series (DP-40) **Unit: mm**



HN62454BCP Series (CP-44) **Unit: mm**



HN62454BN Series

262,144-word × 16-bit CMOS Programmable Mask ROM

HITACHI

Preliminary
Rev. 0.0
October 25, 1995

The HN62454BN is a 262,144-word by 16-bit CMOS Programmable Mask ROM featuring page access mode to get very high speed 4-word serial access. A high speed access of 85/100 ns (max) and page access of 35/40 ns (max) is the most suitable to the system using a high speed microcomputer by 16 bits.

Features

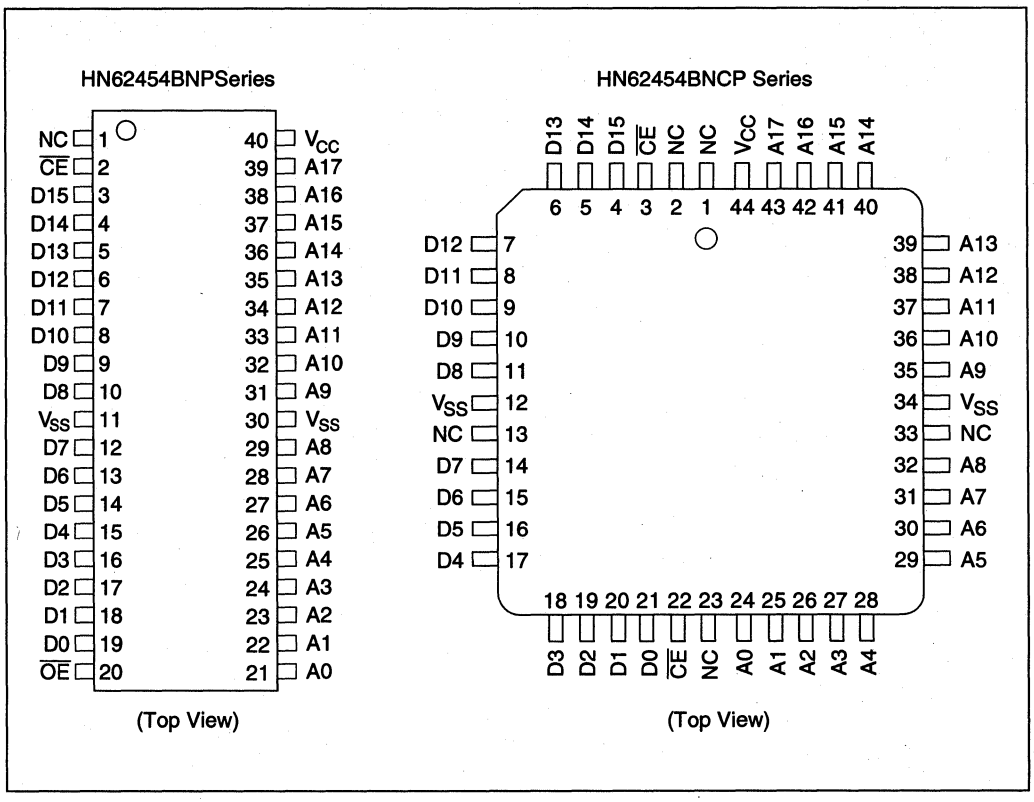
- Single 5 V supply
- High speed
  Normal access time: 85/100 ns (max)
  Page access time: 35/40 ns (max)
- Low power
  Active: 660 mW (max)
  Standby: 165 µW (max)
- 4 word page access on word-wide mode
- Directly TTL compatible
  All inputs and outputs
- Pin compatible with 4 Mbit EPROM
  (HN27C4096AG/ACC/ACP)

Ordering Information

Type No.	Access time	Package
HN62454BNP-85 HN62454BNP-10	85 ns 100 ns	600 mil 40-pin plastic DIP (DP-40)
HN62454BNCP-85 HN62454BNCP-10	85 ns 100 ns	44-pin plastic PLCC (CP-44)

Preliminary: This document contains information on a new product. Specifiactions and information contained herein are subject to change without notice.

Pin Arrangement

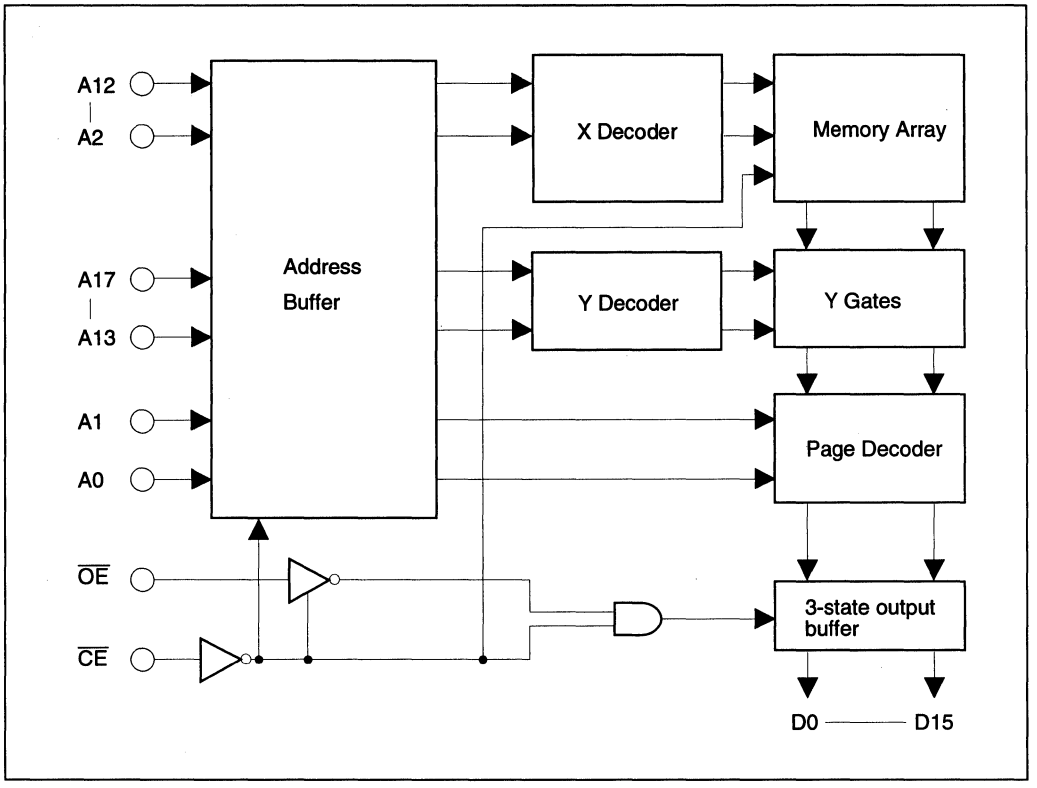


Pin Description

Symbol	Function
A2 to A17	Address inputs
A0, A1	Page address inputs
D0 to D15	Data outputs
$\overline{CE}$	Chip enable

Symbol	Function
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



Mode Selection

	Pin				
				Address input	
Mode	$\overline{CE}$	$\overline{OE}$	Data output	LSB	MSB
Standby	H	×*1	High-Z*2	—	—
Output disable	L	H	High-Z	—	—
Read	L	L	Dout	A0	A17

Notes: 1. ×: Don't care.
2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{CC}	− 0.3 to + 7.0	V
All input and output voltage*1	Vin, Vout	− 0.3 to V_{CC} + 0.3	V
Operating temperature range	Topr	0 to + 70	°C
Storage temperature range	Tstg	− 55 to + 125	°C
Temperature under bias	Tbias	− 20 to + 85	°C

Notes: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	− 0.3	—	0.8	V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

Parameter		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{CC}	—	120/100	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = 85/100 ns
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
	Standby	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = − 400 µA
		V_{OL}	—	0.4	V	I_{OL} = 2.1 mA

Capacitance (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

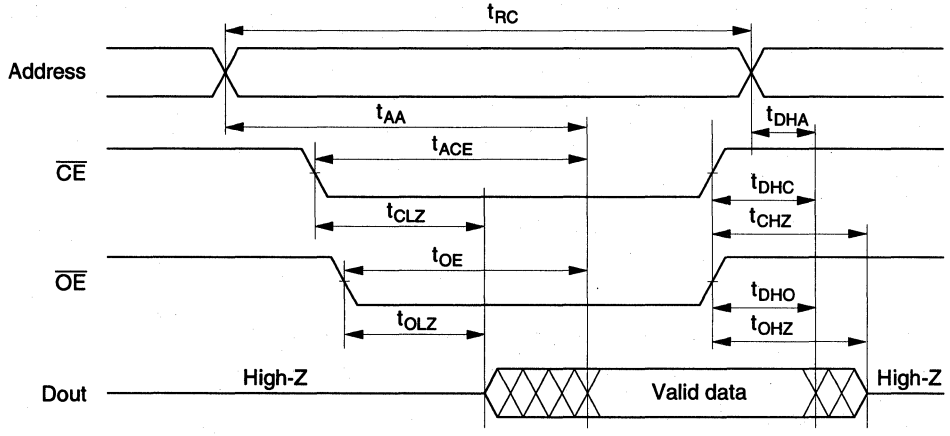
- Output load: 1TTL + C_L = 100 pF (including jig)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 5 ns

		HN62454BN-85		HN62454BN-10			
Parameter	Symbol	Min	Max	Min	Max	Unit	Note
Read cycle time	t_{RC}	85	—	100	—	ns	
Page read cycle time	t_{PC}	35	—	40	—	ns	
Address access	t_{AA}	—	85	—	100	ns	
Page address access time	t_{PA}	—	35	—	40	ns	
$\overline{CE}$ access time	t_{ACE}	—	85	—	100	ns	
$\overline{OE}$ access time	t_{OE}	—	35	—	40	ns	
Output hold time from address change	t_{DHA}	5	—	5	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	30	—	30	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	30	—	30	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns	

Note: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

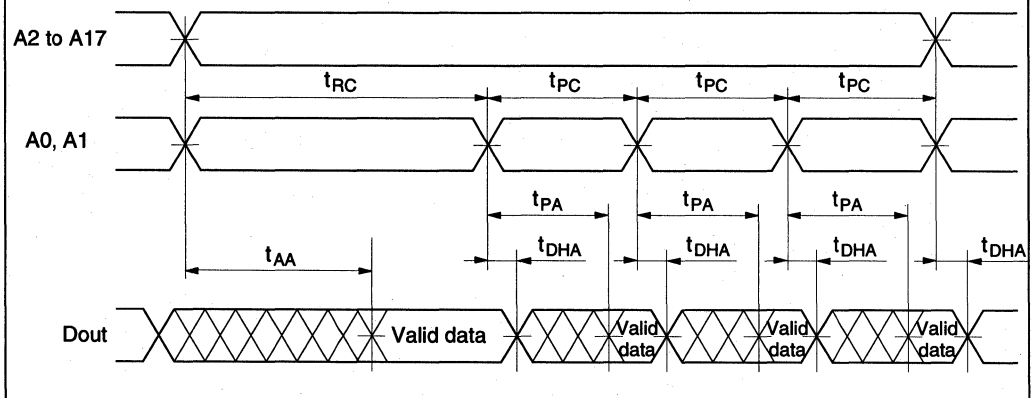
Timing Waveforms

Normal mode



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

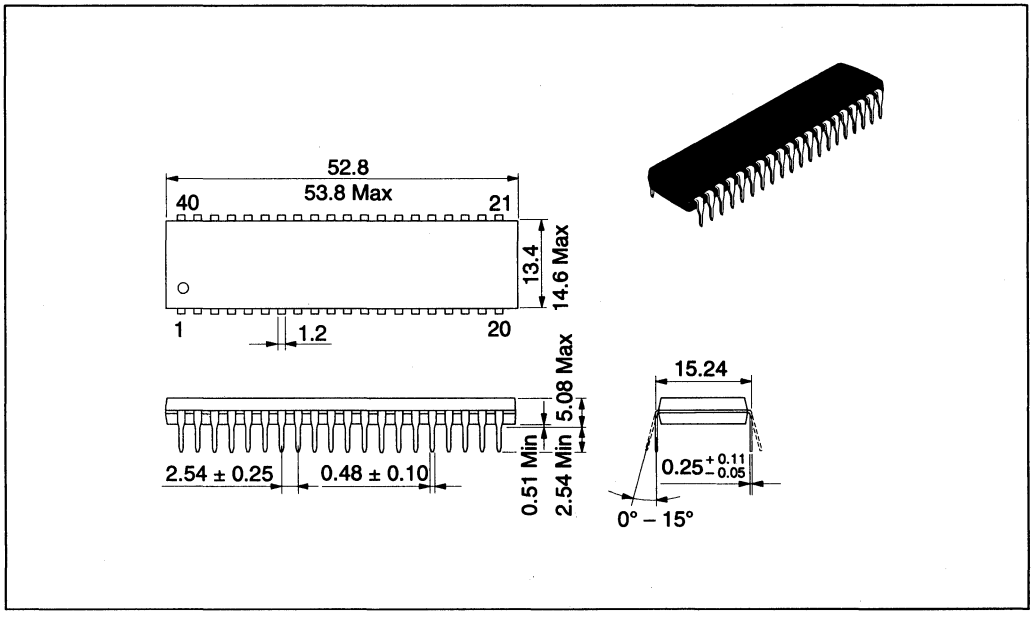
Page mode



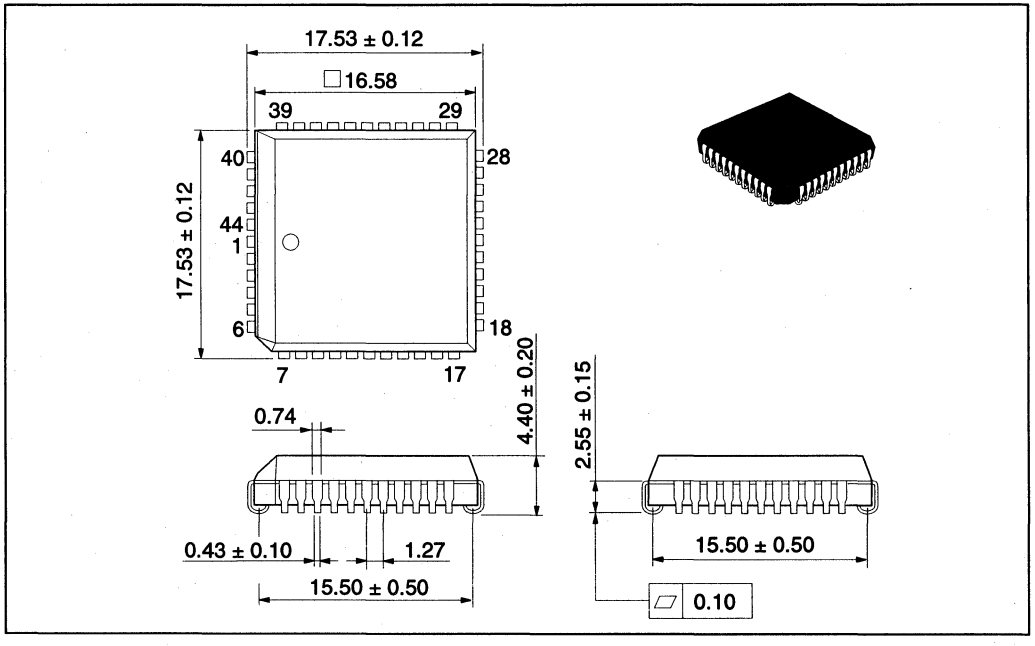
Note: 1. $\overline{CE}$ and $\overline{OE}$ are enable.

Package Dimensions

HN62454BNP Series (DP-40) **Unit: mm**



HN62454BNCP Series (CP-44) **Unit: mm**



ADE-203-404A (Z)

HN62454N Series

524,288-word × 8-bit / 262,144-word × 16-bit CMOS Programmable Mask ROM

HITACHI

Preliminary
Rev. 0.1
July 19, 1995

The HN62454N is a 4-Mbit CMOS Programmable Mask ROM organized either as 262,144 words by 16 bits or 524,288 words by 8 bits.

Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 85/100 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Features

- Single 5 V supply
- High speed
  Normal access time: 85/100 ns (max)
  Page access time: 35/40 ns (max)
- Low power
  Active: 660 mW (max)
  Standby: 165 µW (max)
- Byte-wide or word-wide data organization
  (Switched by BHE terminal)
- 4 word page access on word-wide mode
- 8 byte page access on byte-wide mode
- Three-state data output for or-tying
- Directly TTL compatible
  All inputs and outputs
- Pin compatible with 4 Mbit EPROM
  (HN27C4000G/FP)

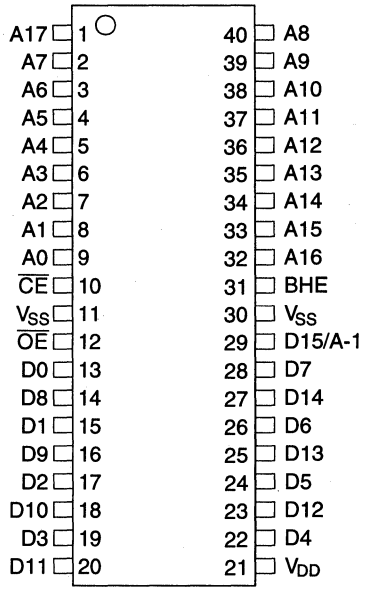
Ordering Information

Type No.	Access time	Package
HN62454NP-85 HN62454NP-10	85 ns 100 ns	600 mil 40-pin plastic DIP (DP-40)
HN62454NFA-85 HN62454NFA-10	85 ns 100 ns	525 mil 40-pin plastic SOP (FP-40D)
HN62454NTT-85 HN62454NTT-10	85 ns 100 ns	400 mil 44-pin plastic TSOP II (TTP-44D)

Preliminary: This document contains information on a new product. Specifiactions and information contained herein are subject to change without notice.

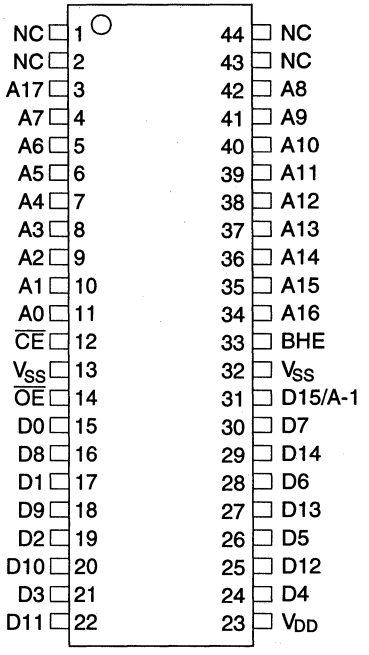
Pin Arrangement

HN62454NPSeries



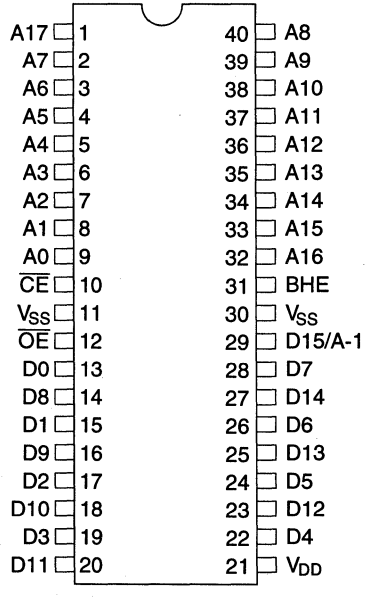
(Top View)

HN62454NTT Series



(Top View)

HN62454NFA Series

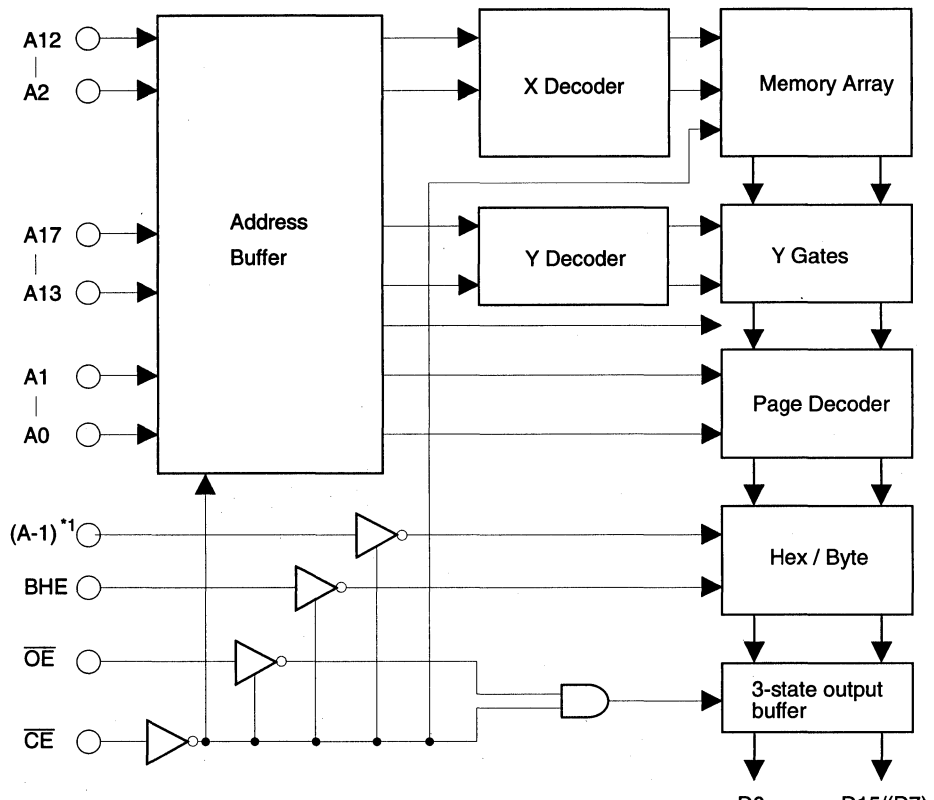


(Top View)

Pin Description

Symbol	Function
A2 to A17	Address inputs
A-1, A0, A1	Page address inputs
D0 to D15	Data outputs
BHE	8/16 bit (byte/word) mode switch
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



BHE = V_{IH}: 16-bit (D15 to D0)
BHE = V_{IL} : 8-bit (D7 to D0)

Note: 1. A-1 is least significant address.

When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.

Mode Selection

	Pin							
					Data output		Address input	
Mode	$\overline{CE}$	$\overline{OE}$	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	×*1	×	×	High-Z*2	High-Z	—	—
Output disable	L	H	×	×	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A17
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A17
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A17

notes: 1. ×: Don't care.
2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{CC}	− 0.3 to + 7.0	V
All input and output voltage*1	Vin, Vout	− 0.3 to V_{CC} + 0.3	V
Operating temperature range	Topr	0 to + 70	°C
Storage temperature range	Tstg	− 55 to + 125	°C
Temperature under bias	Tbias	− 20 to + 85	°C

Notes: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	− 0.3	—	0.8	V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

Parameter		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{CC}	—	120/100	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = 85/100 ns
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ - 0.2 V
	Standby	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = – 205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

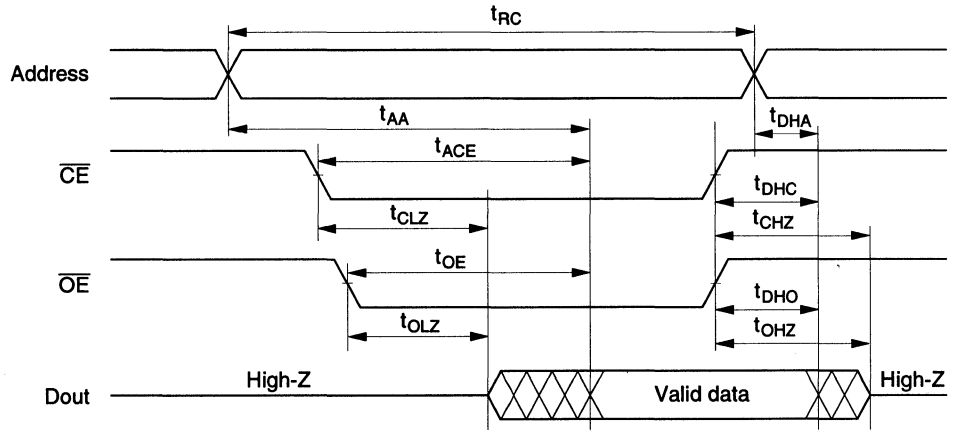
- Output load: 1TTL + C_L = 100 pF (including jig)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 5ns

		HN62454N-85		HN62454N-10			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	85	—	100	—	ns	
Page read cycle time	t_{PC}	35	—	40	—	ns	
Address access	t_{AA}	—	85	—	100	ns	
Page address access time	t_{PA}	—	35	—	40	ns	
$\overline{CE}$ access time	t_{ACE}	—	85	—	100	ns	
$\overline{OE}$ access time	t_{OE}	—	35	—	40	ns	
BHE access time	t_{BHE}	—	85	—	100	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	30	—	30	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	30	—	30	ns	1
BHE to output in high-Z	t_{BHZ}	—	30	—	30	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns	

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

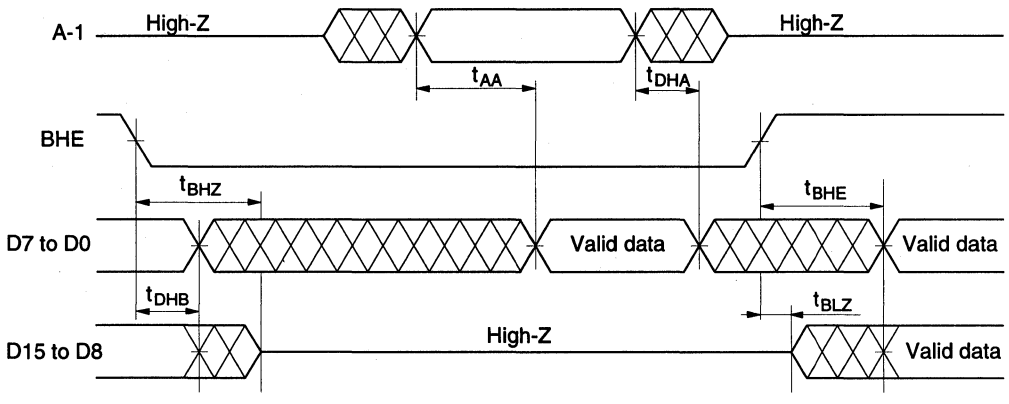
Timing Waveforms

Word mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



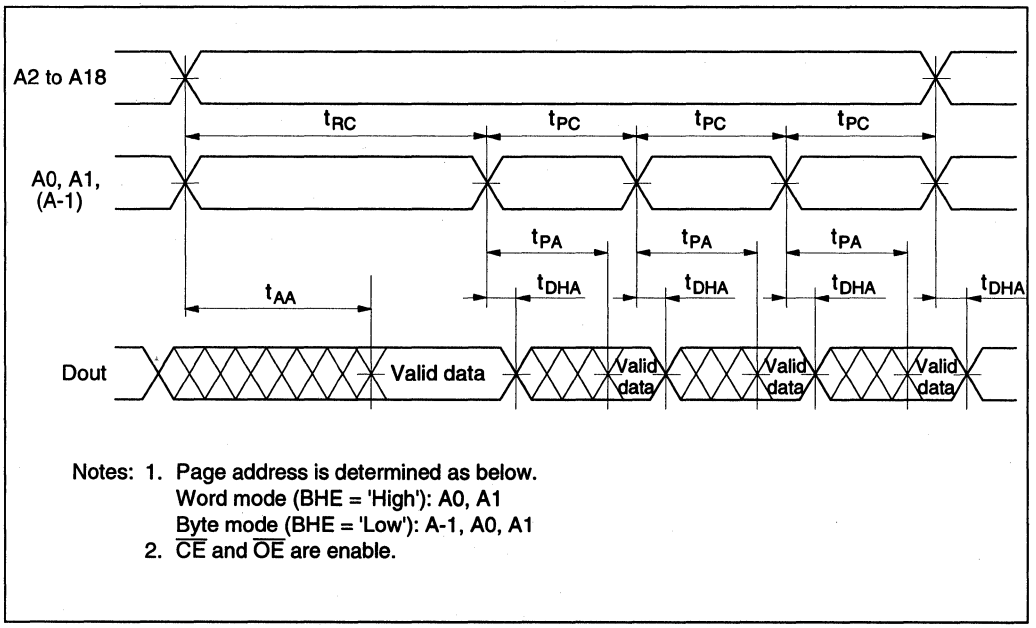
Note: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Word Mode, Byte Mode Switch



Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable, A17 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

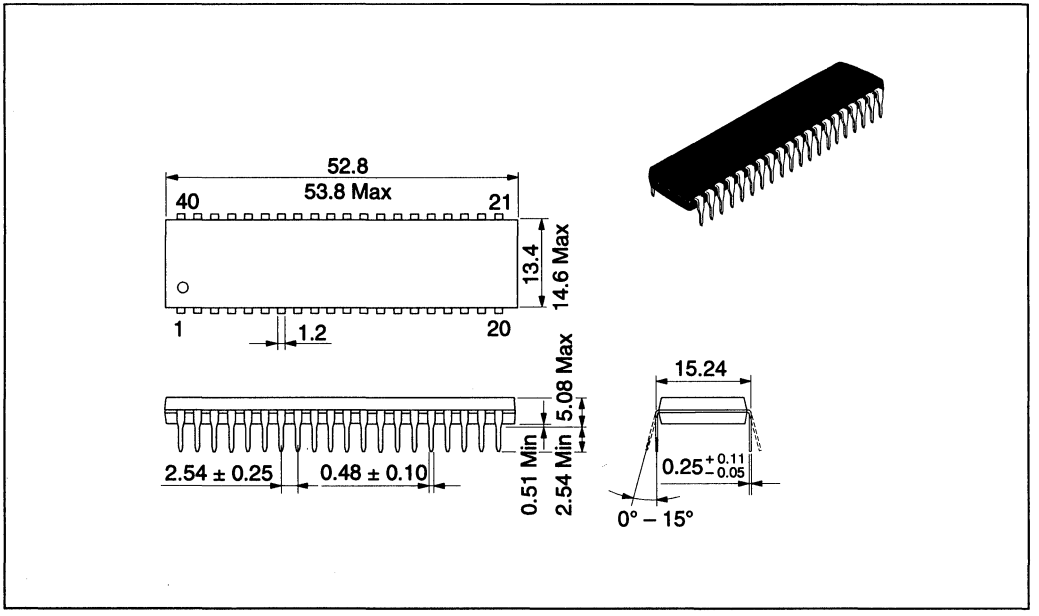
Page mode



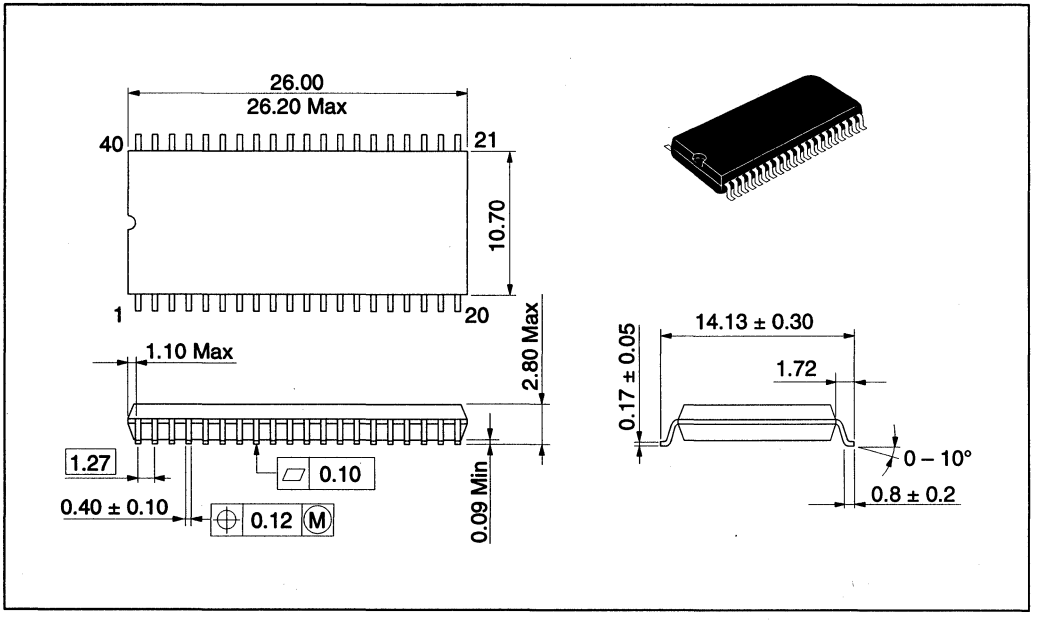
Notes: 1. Page address is determined as below.
Word mode (BHE = 'High'): A0, A1
Byte mode (BHE = 'Low'): A-1, A0, A1
2. $\overline{CE}$ and $\overline{OE}$ are enable.

Package Dimensions

HN62454NP Series (DP-40) **Unit: mm**

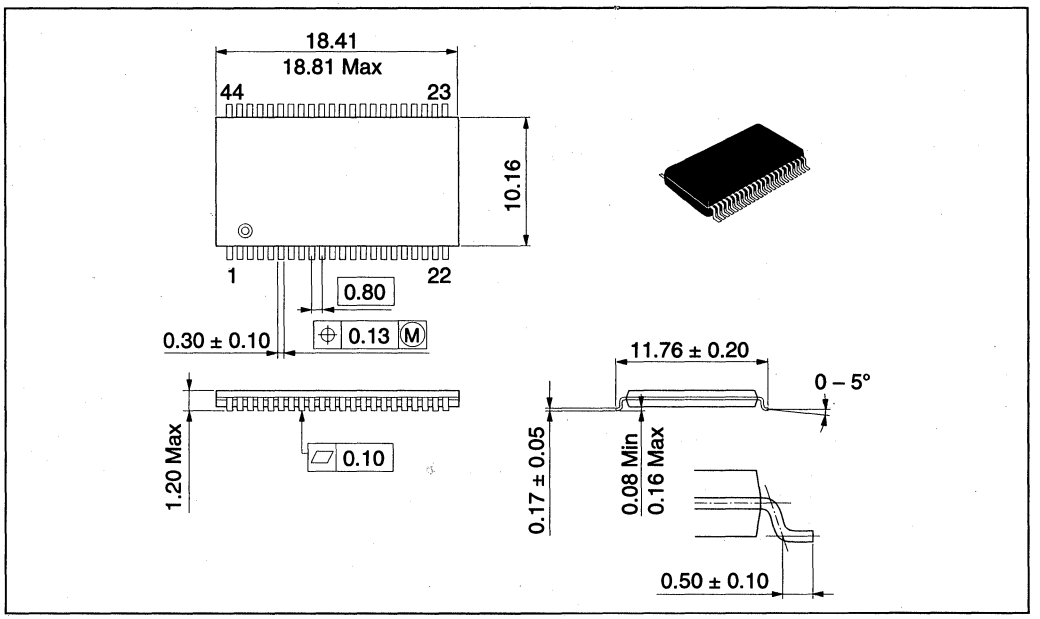


HN62454NFA Series (FP-40D) **Unit: mm**



Package Dimensions (cont)

HN62454NTT Series (TTP-44D) **Unit: mm**



HN62W454 Series

524,288-word × 8-bit / 262,144-word × 16-bit CMOS Programmable Mask ROM

HITACHI

Preliminary
Rev. 0.0
June 21, 1995

The HN62W454 is a 4-Mbit CMOS Programmable Mask ROM organized either as 262,144 words by 16 bits or 524,288 words by 8 bits.

Realizing low power consumption, this memory is allowed for battery operation. A high speed access of 120 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Features

- Low voltage operation
  Operating supply voltage: + 3.0 V to 3.6 V
- High speed
  Normal access time: 120/150 ns (max)
- Low power
  Active: 216 mW (max)
  Standby: 108 µW (max)
- Byte-wide or word-wide data organization
  (Switched by BHE terminal)
- Three-state data output for or-tying
- Directly LV-TTL compatible
  All inputs and outputs

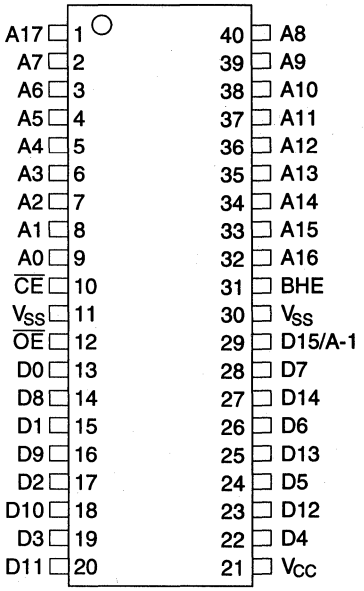
Ordering Information

Type No.	Access time	Package
HN62W454P-12 HN62W454P-15	120 ns 150 ns	600 mil 40-pin plastic DIP (DP-40)
HN62W454FA-12 HN62W454FA-15	120 ns 150 ns	525 mil 40-pin plastic SOP (FP-40D)
HN62W454TT-12 HN62W454TT-15	120 ns 150 ns	400 mil 44-pin plastic TSOP II (TTP-44D)

Preliminary: This document contains information on a new product. Specifiactions and information contained herein are subject to change without notice.

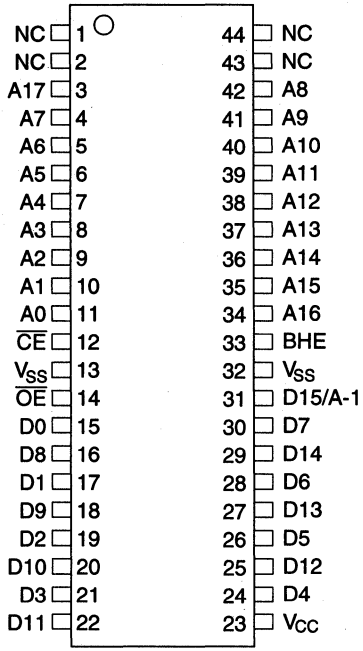
Pin Arrangement

HN62W454PSeries



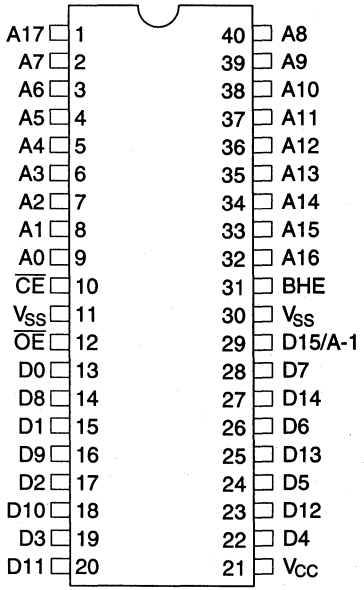
(Top View)

HN62W454TT Series



(Top View)

HN62W454FA Series

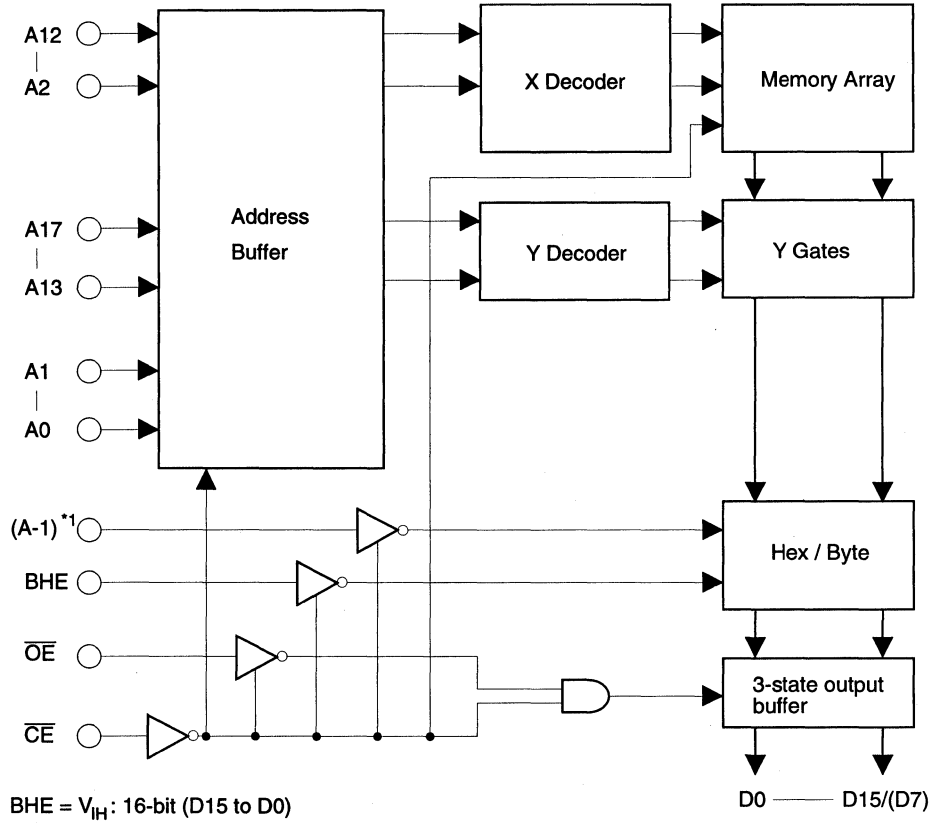


(Top View)

Pin Description

Symbol	Function
A-1, A0 to A17	Address inputs
D0 to D15	Data outputs
BHE	8/16 bit (byte/word) mode switch
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
NC	No connection
V_{DD}	Power supply
V_{SS}	Ground

Block Diagram



BHE = V_{IH}: 16-bit (D15 to D0)
BHE = V_{IL} : 8-bit (D7 to D0)

Note: 1. A-1 is least significant address.

When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.

Mode Selection

	Pin							
					Data output		Address input	
Mode	$\overline{CE}$	$\overline{OE}$	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	×*1	×	×	High-Z*2	High-Z	—	—
Output disable	L	H	×	×	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A17
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A17
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A17

notes: 1. ×: Don't care.
2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{DD}	− 0.3 to + 5.5	V
All input and output voltage*1	Vin, Vout	− 0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr	0 to + 70	°C
Storage temperature range	Tstg	− 55 to + 125	°C
Temperature under bias	Tbias	− 20 to + 85	°C

Notes: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	V_{DD} + 0.3	V
	V_{IL}	− 0.3	—	0.8	V

DC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to + 70°C)

Parameter		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{DD}	—	60/50	mA	V_{DD} = 3.6 V, I_{DOUT} = 0 mA, t_{RC} = 120/150ns
	Standby	I_{SB1}	—	30	µA	V_{DD} = 3.6 V, $\overline{CE} \geq V_{DD}$ - 0.2 V
	Standby	I_{SB2}	—	3	mA	V_{DD} = 3.6 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{DD}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{DD}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = – 2.0 mA
		V_{OL}	—	0.4	V	I_{OL} = 2.0 mA

Capacitance (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to + 70°C)

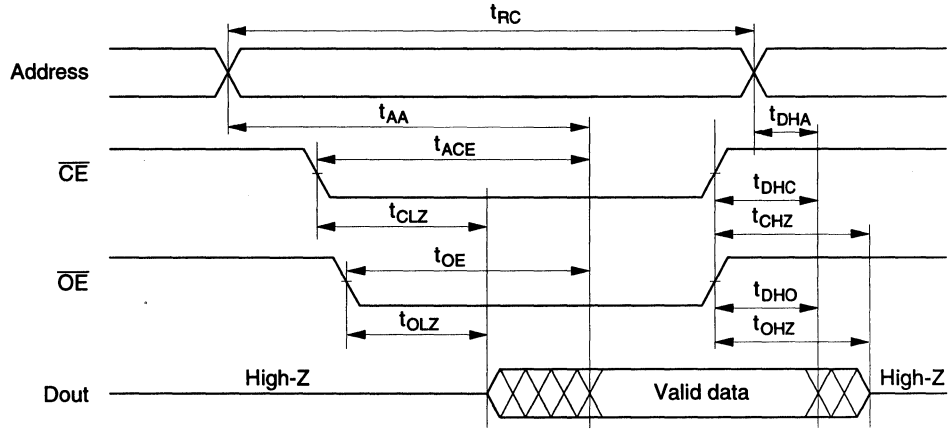
- Output load: 1TTL + C_L = 100 pF (including jig)
- Input pulse level: 0.4 to 2.4 V
- Input and output timing reference level: 1.4 V
- Input rise and fall time: 5ns

		HN62W454-12		HN62W454-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	120	—	150	—	ns	
Address access	t_{AA}	—	120	—	150	ns	
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	60	—	70	ns	
BHE access time	t_{BHE}	—	120	—	150	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	50	—	60	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	50	—	60	ns	1
BHE to output in high-Z	t_{BHZ}	—	50	—	60	ns	1
$\overline{CE}$ to output in low-Z	t_{CHZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns	

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

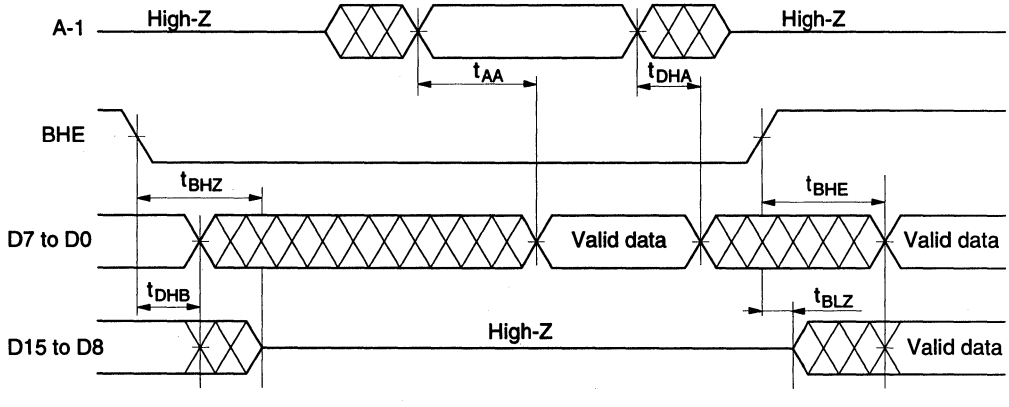
Timing Waveforms

Word mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



Note: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

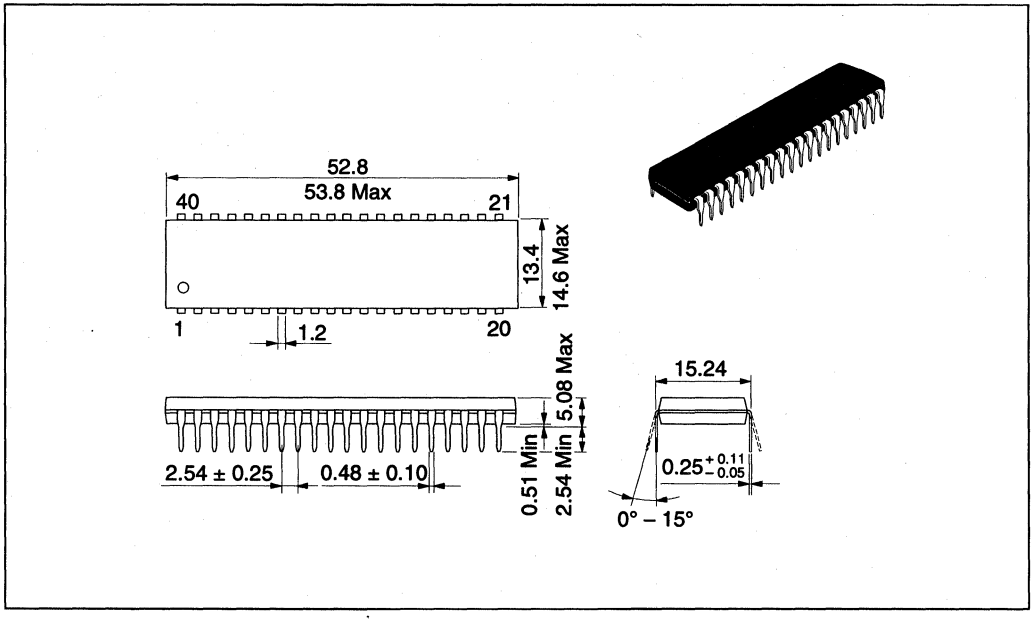
Word Mode, Byte Mode Switch



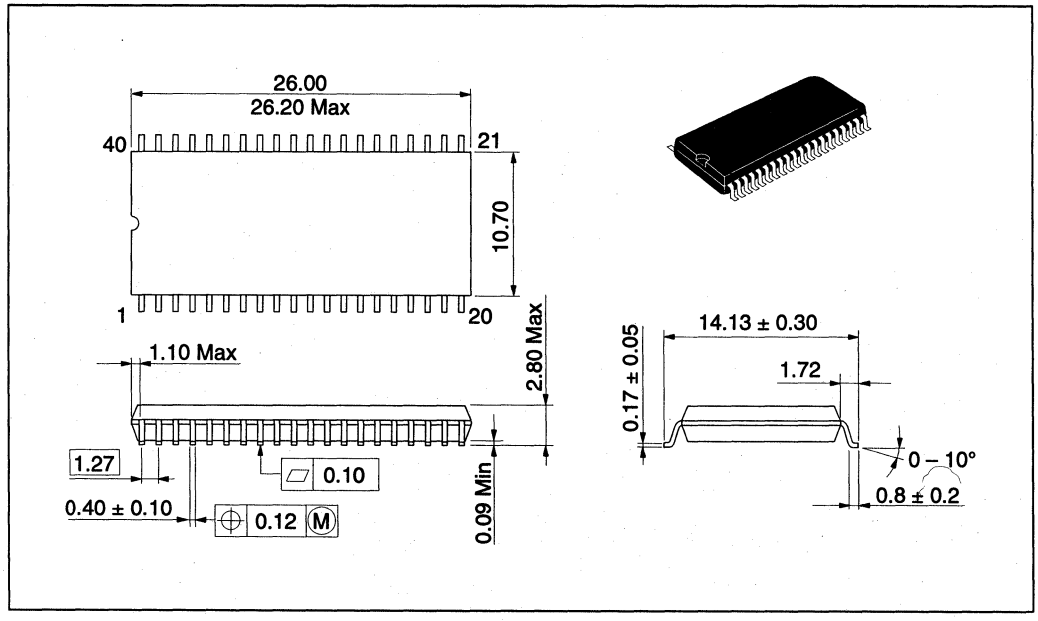
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable, A17 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

Package Dimensions

HN62W454P Series (DP-40) **Unit: mm**

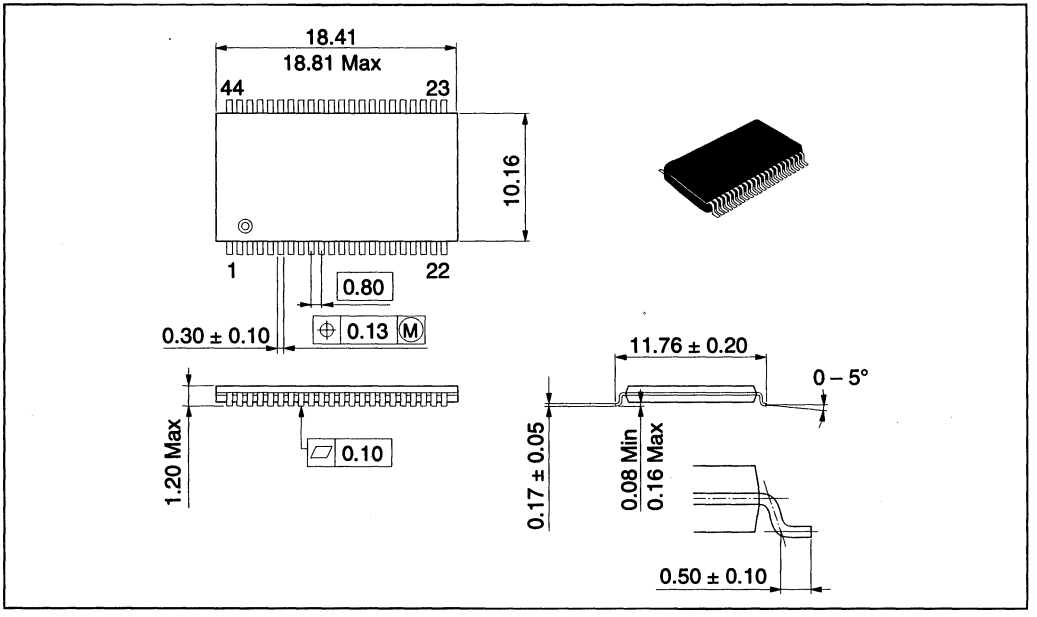


HN62W454FA Series (FP-40D) **Unit: mm**



Package Dimensions (cont)

HN62W454TT Series (TTP-44D) **Unit: mm**



8M Mask ROM

HN62338B Series

1,048,576-word x 8-bit CMOS Mask Programmable ROM

HITACHI

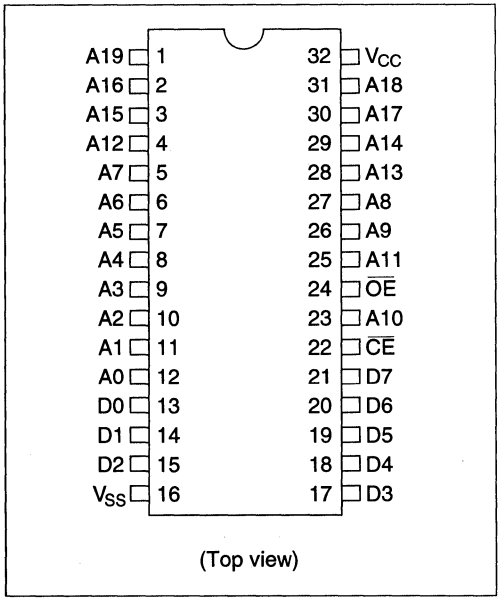
Under Development

The HN62338B is a 8-Mbit CMOS Programmable Mask ROM organized as 1,048,576 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62338B, which provides large capacity of 8M bits, is ideally suited for kanji character generators.

Features

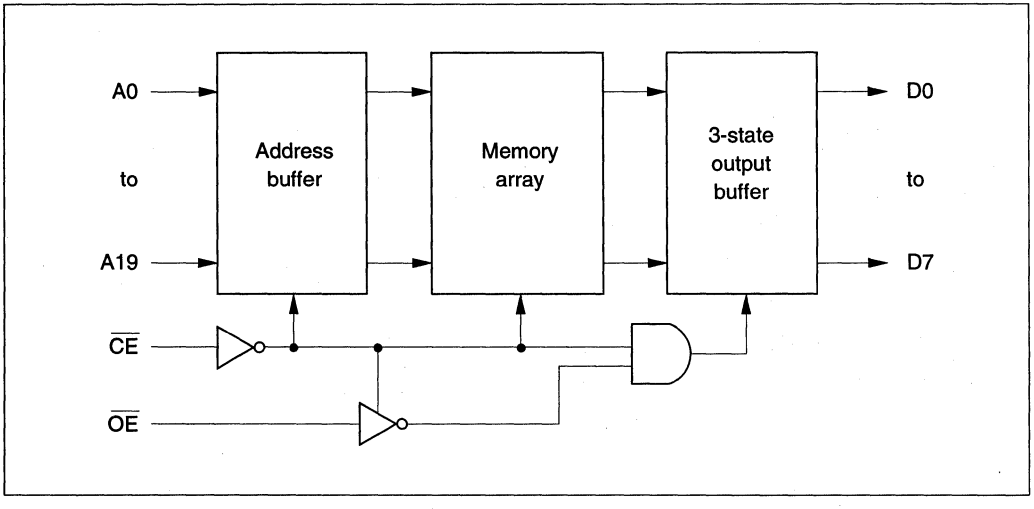
- Single +5V power supply
- Maximum access time: 120 ns (max)
- Low power consumption: 250 mW (typ) active
  5 µW (typ) standby
- Byte-wide data organization
- Pin compatible with JEDEC

Pin Arrangement



(Top view)

Block Diagram



Ordering Information

Type No.	Access time	Package
HN62338BP-12	120 ns	600 mil 32-pin plastic DIP (DP-32)
HN62338BF-12	120 ns	32-pin plastic SOP (FP-32D)
HN62338BTT-12	120 ns	32-pin plastic TSOP-II (TTP-32D)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	–0.3 to +7.0	V	1
All input and output voltage	Vin, Vout	–0.3 to V_{CC} + 0.3	V	1
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	80	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
Input leakage current		$\|I_{IL}\|$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.4 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, V_{IN} = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	Cin	—	15	pF
Output capacitance	Cout	—	15	pF

Note: This parameter is sampled and not 100% tested.

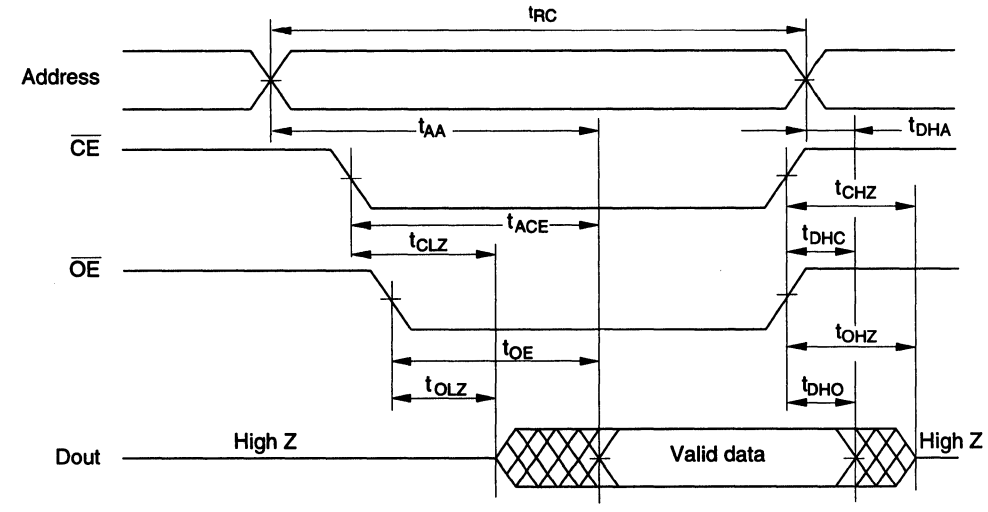
AC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

- Output load: 1TTL gate + C_L = 100 pF (including jig capacitance)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 5 ns

		HN62338B-12		
Item	**Symbol**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	120	—	ns
Address access time	t_{AA}	—	120	ns
$\overline{CE}$ access time	t_{ACE}	—	120	ns
$\overline{OE}$ access time	t_{OE}	—	60	ns
Output hold time from address change	t_{DHA}	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns
$\overline{CE}$ to output in high Z	t_{CHZ}*1	—	40	ns
$\overline{OE}$ to output in high Z	t_{OHZ}*1	—	40	ns
$\overline{CE}$ to output in low Z	t_{CLZ}	5	—	ns
$\overline{OE}$ to outpu in low Z	t_{OLZ}	5	—	ns

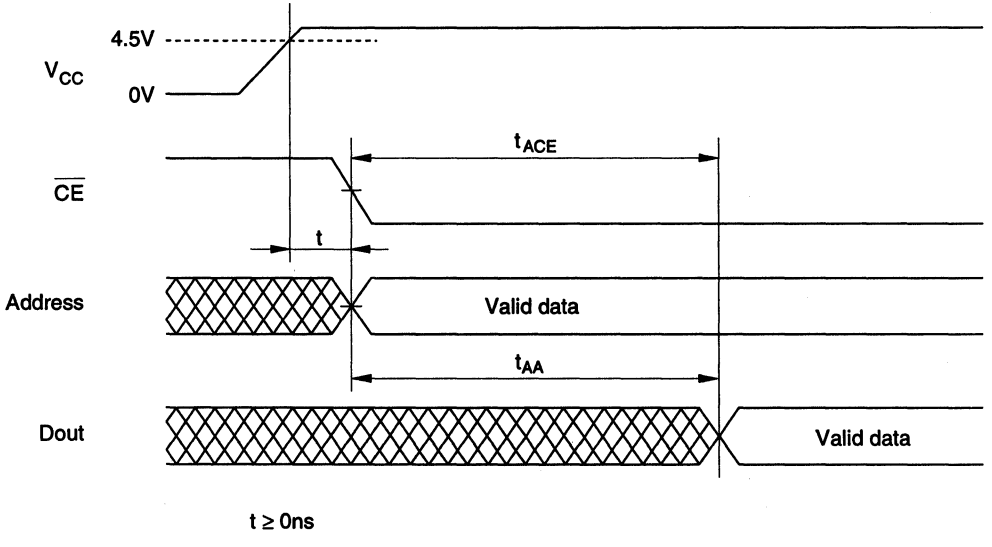
Note: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

Timing Diagram



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

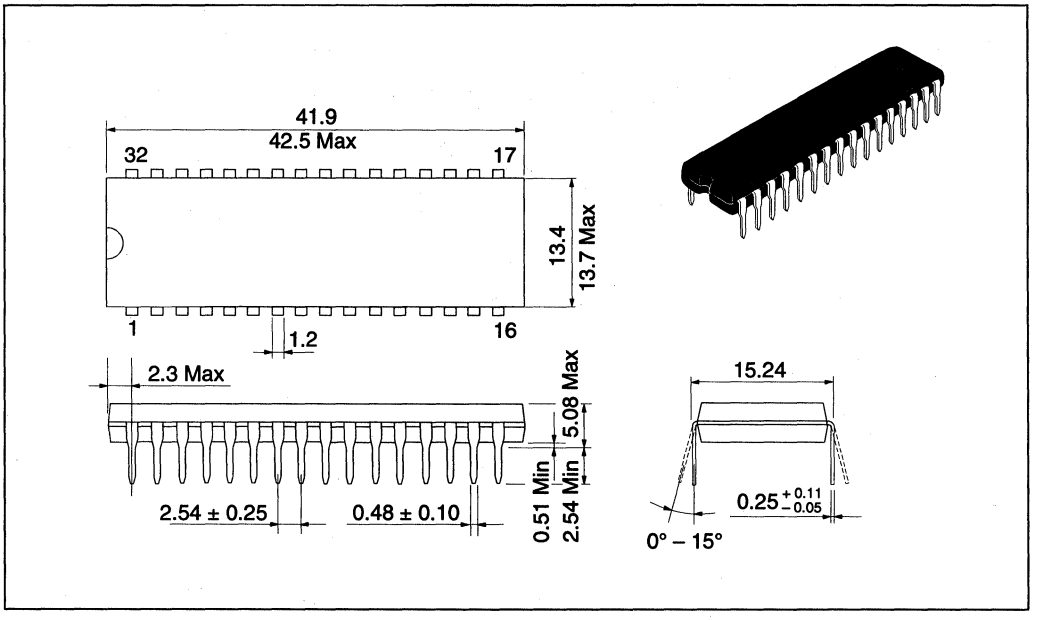
Power Up Sequence



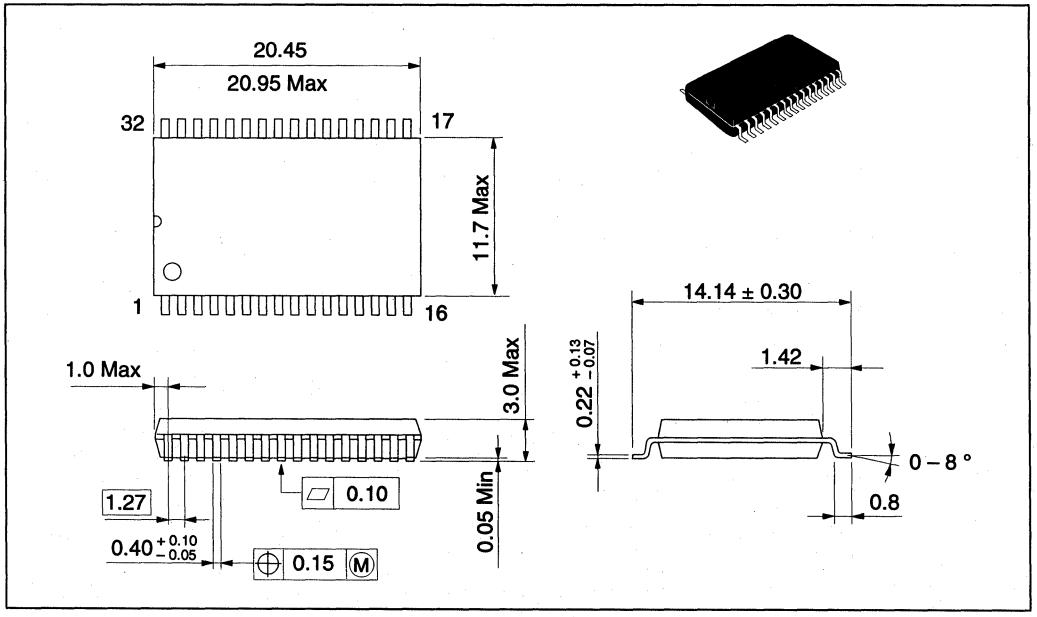
Note: This device is used ATD (Address Transient Detector). Therefore, Transfer either $\overline{CE}$ or address after power up to 4.5 V.

Package Dimensions

HN62338BP Series (DP-32) **Unit : mm**

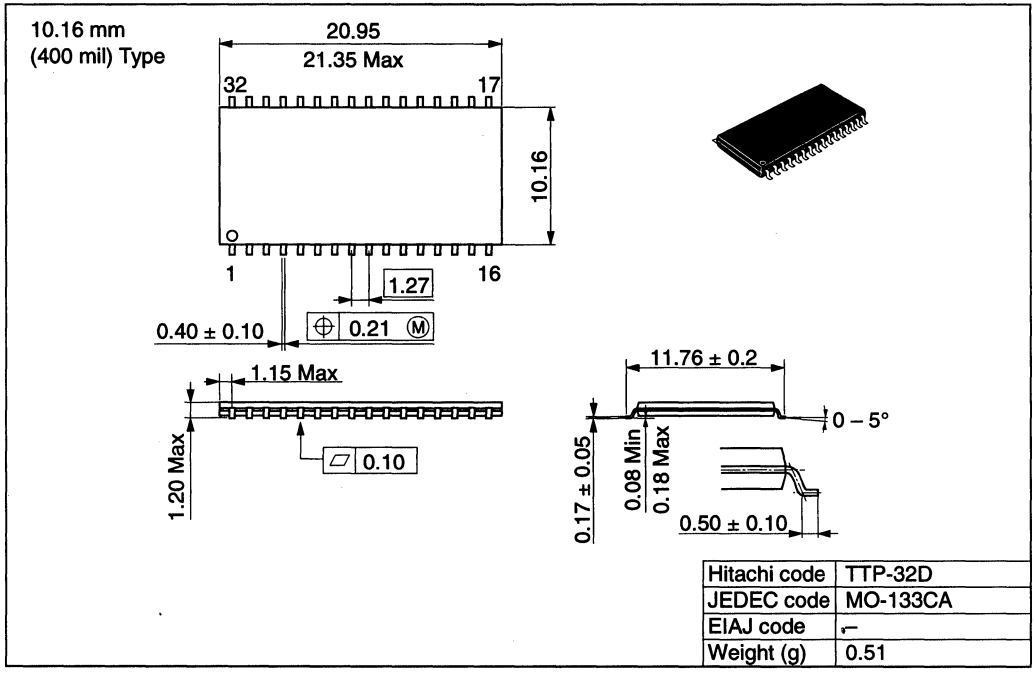


HN62338BF Series (FP-32D) **Unit : mm**



Package Dimensions (cont)

HN62338BTT Series (TTP-32D) **Unit : mm**



Hitachi code	TTP-32D
JEDEC code	MO-133CA
EIAJ code	—
Weight (g)	0.51

HN62428 Series

524,288-word x 16-bit / 1,048,576-word x 8-bit CMOS Programmable Mask ROM

HITACHI

The HN62428 Series is a 8-Mbit CMOS Programmable Mask ROM organized either as 524,288 words by 16 bits or as 1,048,576 words by 8 bits. It can be operated with a battery because of low power consumption.

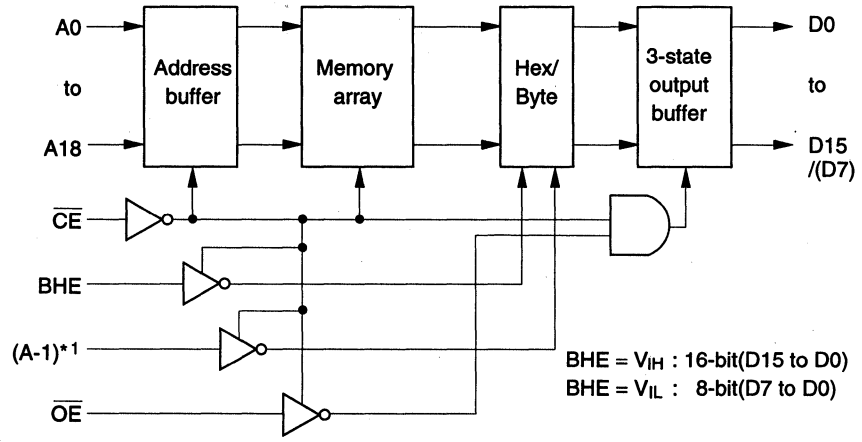
Features

- Single 5 V
- Wired OR is permitted for the output in three states.
- TTL compatible
- Address access time: 150/200 ns (max)
- Low power consumption: 100 mW (typ) active
  5 µW (typ) standby
- Byte-wide or word-wide data organization (switched by BHE terminal)

Ordering Information

Type No.	Access time	Package
HN62428P-15/-20	150/200 ns	600 mil 42-pin plastic DIP (DP-42)
HN62428TT-15/-20	150/200 ns	44-pin plastic TSOP-II (TTP-44D)
HN62428FB-15/-20	150/200 ns	44-pin plastic SOP (FP-44D)

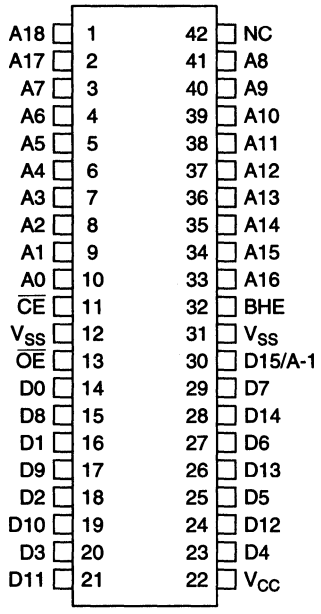
Block Diagram



Note: 1. A-1 is least significant address. When BHE is 'low', D14 to D8 goes the high impedance state.

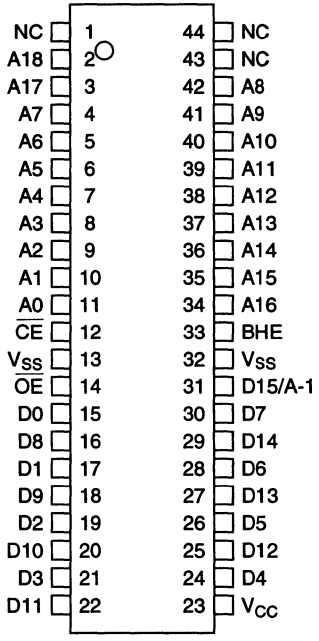
Pin Arrangement

HN62428P



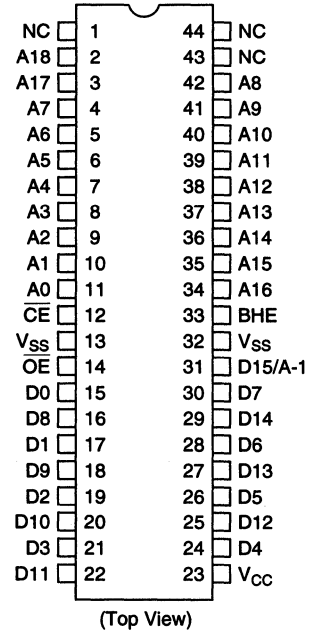
(Top View)

HN62428TT



(Top View)

HN62428FB



(Top View)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	–0.3 to +7.0	V
Terminal voltage	Vin, Vout	–0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C
Bias temperature	Tbias	–20 to +85	°C

Note: With respect to V_{SS}.

Recommended DC Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test conditions
Power supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
Input leak current		$\|I_{LI}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leak current		$\|I_{LO}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, V_{IN} = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	Cin	—	15	pF
Output capacitance	Cout	—	15	pF

Note: This parameter is sampled and not 100% tested.

AC Operating Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Test Conditions

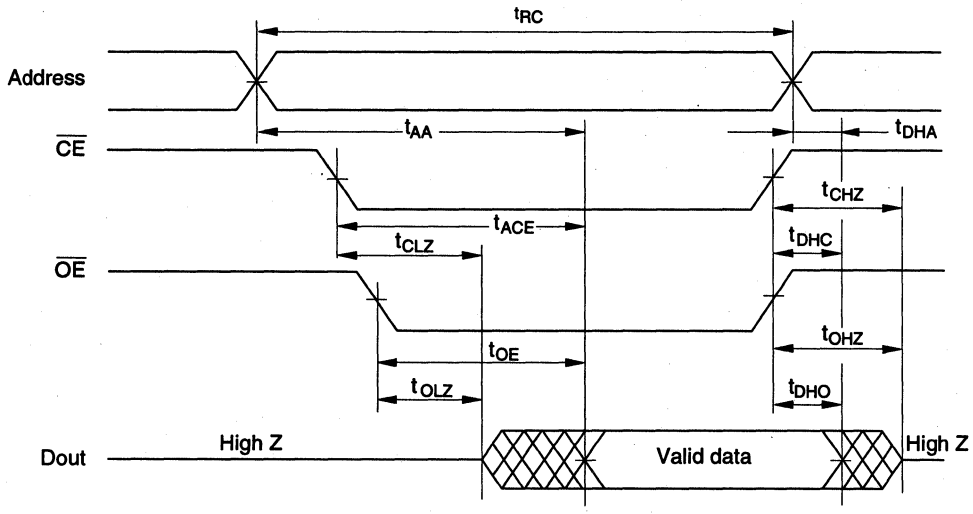
- Input pulse level: 0.8 to 2.4 V
- I/O timing reference level: 1.5 V
- Input rise/fall time: 10 ns
- Output load: 1 TTL gate + C_L = 100 pF (including jig capacitance)

		HN62428-15		HN62428-20		
Item	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Cycle time	t_{RC}	150	—	200	—	ns
Address access time	t_{AA}	—	150	—	200	ns
$\overline{CE}$ access time	t_{ACE}	—	150	—	200	ns
$\overline{OE}$ access time	t_{OE}	—	70	—	100	ns
BHE access time	t_{BHE}	—	150	—	200	ns
Output hold time from address change	t_{DHA}	0	—	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to output in high-Z	t_{CHZ}*1	—	70	—	70	ns
$\overline{OE}$ to output in high-Z	t_{OHZ}*1	—	70	—	70	ns
BHE to output in high-Z	t_{BHZ}*1	—	70	—	70	ns
$\overline{CE}$ to output in low-Z	t_{CLZ}	10	—	10	—	ns
$\overline{OE}$ to output in low-Z	t_{OLZ}	10	—	10	—	ns
BHE to output in low-Z	t_{BLZ}	10	—	10	—	ns

Note: *1 t_{CHZ}, t_{OHZ} and t_{BHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage level.

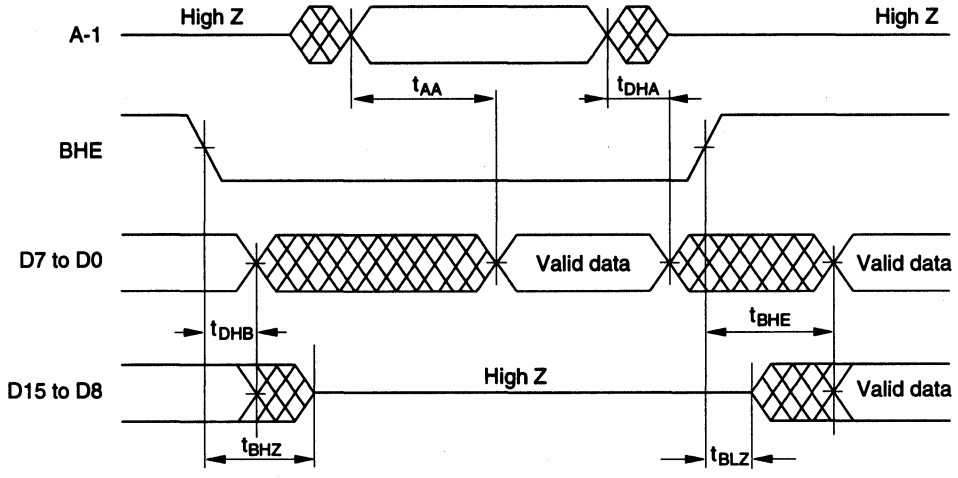
Timing Waveform

Word Mode (BHE = "V_{IH}") or Byte Mode (BHE = "V_{IL}")



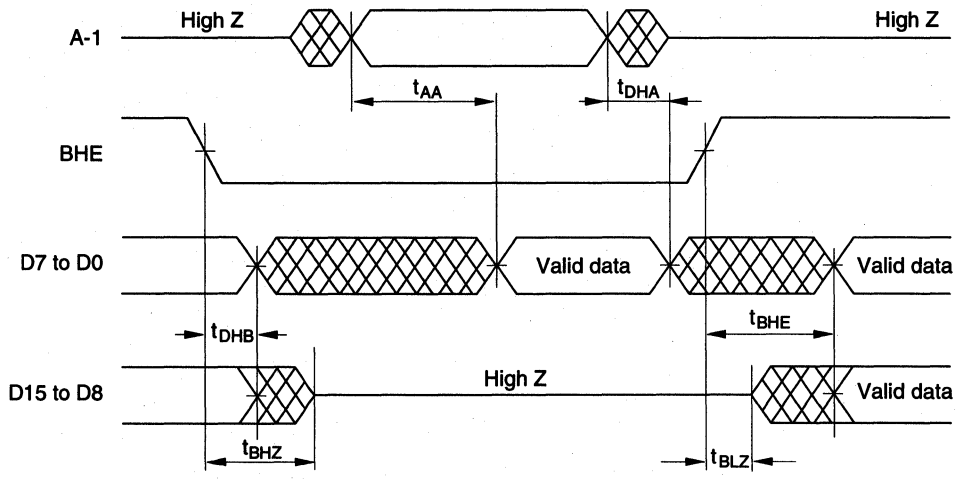
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO} : Determined by whichever is faster.
2. t_{AA}, t_{ACE}, t_{OE} : Determined by whichever is slower.
3. t_{CLZ}, t_{OLZ} : Determined by whichever is slower.

Switching between Word Mode and Byte Mode



Notes: 1. $\overline{CE}$, $\overline{OE}$ are of selected status. A18 – A0 are fixed.
2. D15/A-1 terminal is of output state when BHE = V_{IH}, $\overline{CE}$ and $\overline{OE}$ are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

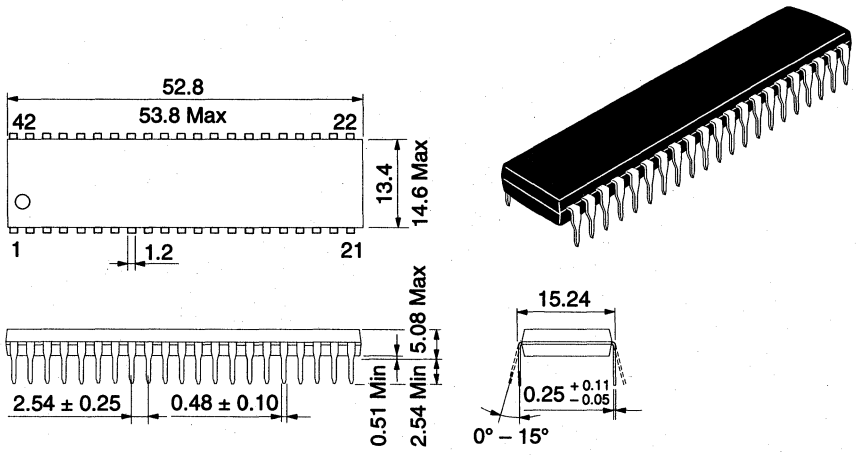
Switching between Word Mode and Byte Mode



Notes: 1. $\overline{CE}$, $\overline{OE}$ are of selected status. A18 – A0 are fixed.
2. D15/A-1 terminal is of output state when BHE = V_{IH}, $\overline{CE}$ and $\overline{OE}$ are of selected state. At this time, an input signal that is of the inverse phase to the output should not be impressed.

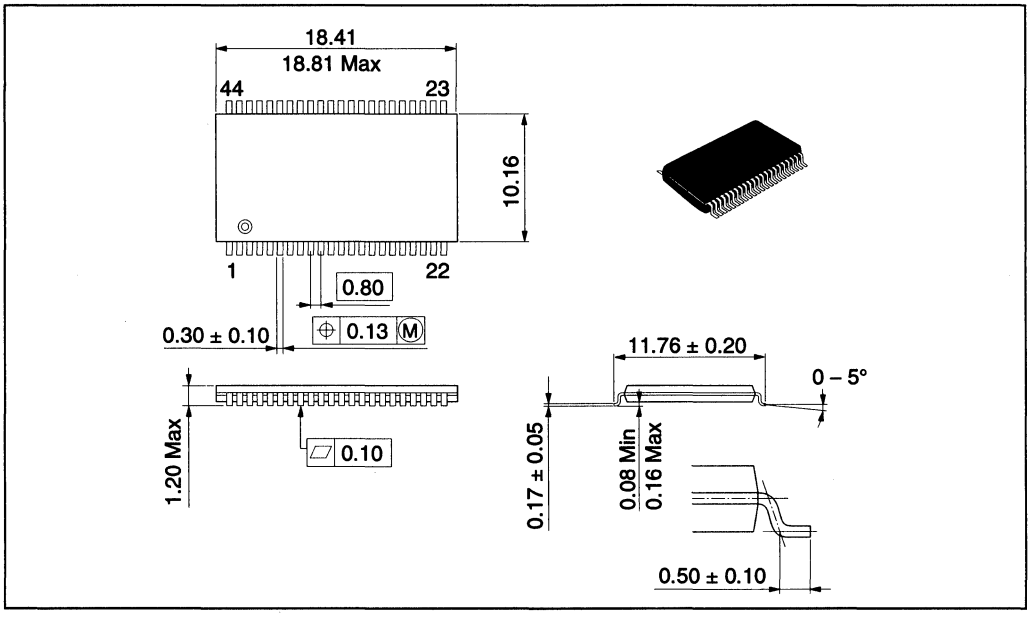
Package Dimensions

HN62428P Series (DP-42) **Unit : mm**

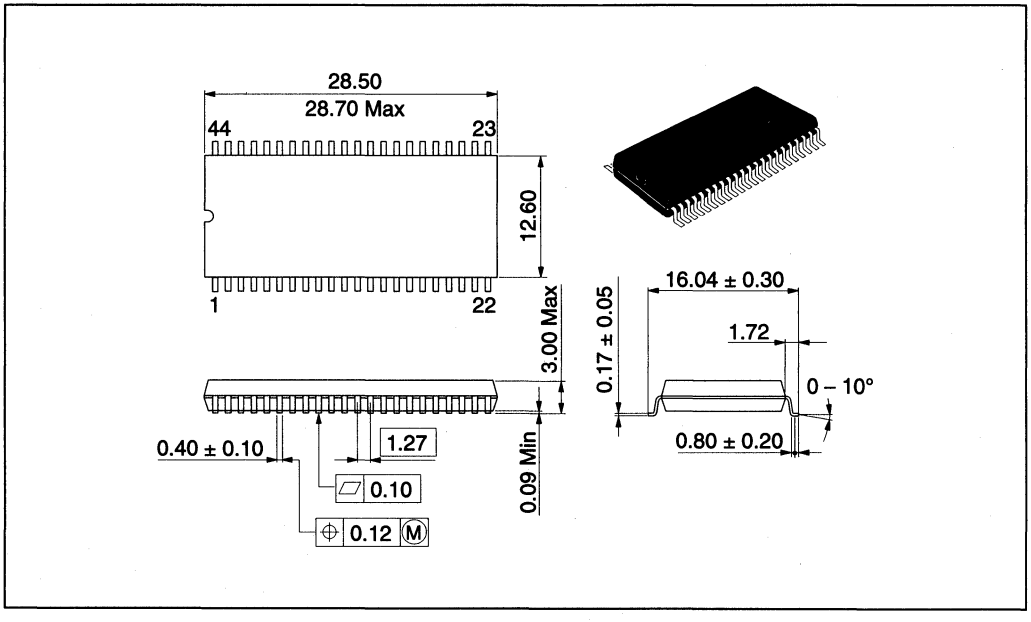


Package Dimensions (cont)

HN62428TT Series (TTP-44D) **Unit : mm**



HN62428FB Series (FP-44D) **Unit : mm**



HN62W428 Series

524,288-word × 16-bit / 1,048,576-word x 8-bit CMOS Programmable Mask ROM

HITACHI

The HN62W428 is a 8-Mbit CMOS Programmable Mask ROM organized either as 524,288 words by 16 bits or as 1,048,576 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation.

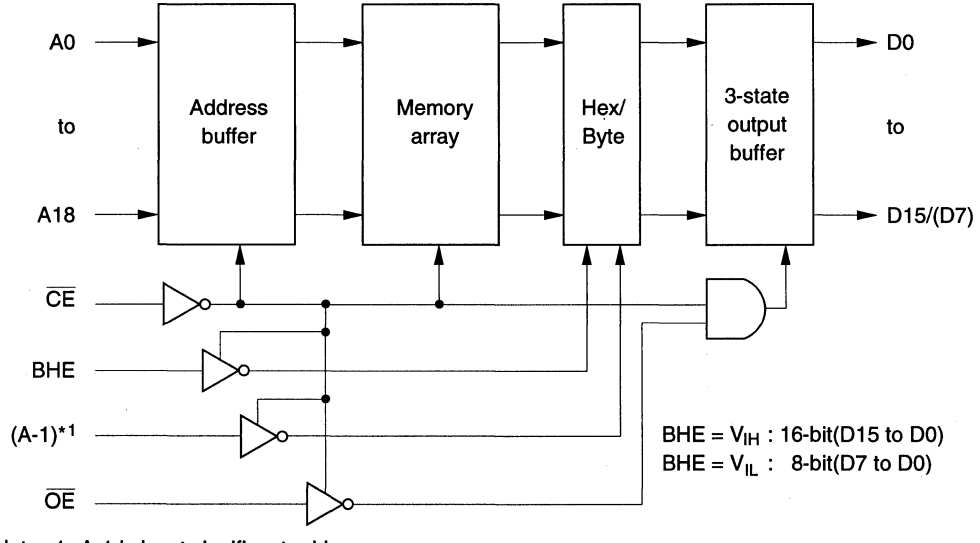
Features

- Low voltage and wide range operation: 3.0 to 5.5 V
- Maximum access time: 300 ns (max)
- Low power consumption: 100 mW (typ) active
  5 µW (typ) standby
- Byte-wide or word-wide data organization with BHE

Ordering Information

Type No.	Access time	Package
HN62W428P	300 ns	600 mil 42-pin plastic DIP (DP-42)
HN62W428FB	300 ns	44-pin plastic SOP (FP-44D)
HN62W428TT	300 ns	44-pin plastic TSOP-II (TTP-44D)

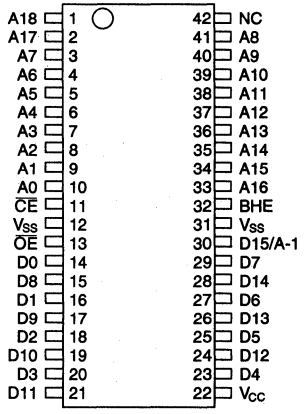
Block Diagram



Note: 1. A-1 is least significant address.
When BHE is 'low', D14 to D8 goes the high impedance state.

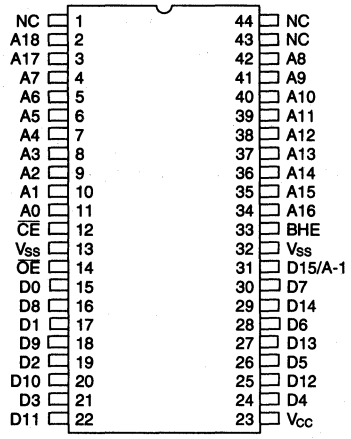
Pin Arrangement

HN62W428P



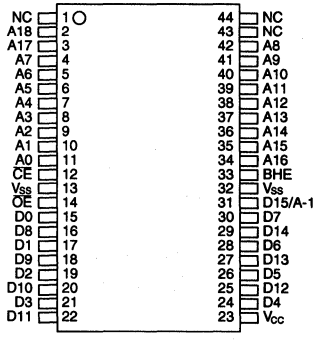
(Top view)

HN62W428FB



(Top view)

HN62W428TT



(Top view)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	–0.3 to +7.0	V	1
All input and output voltage	Vin, Vout	–0.3 to V_{CC} + 0.3	V	1
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.6	V

DC Electrical Characteristics (V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	50	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min
	Active	I_{CC}	—	25	mA	V_{CC} = 3.0 V, I_{DOUT} = 0 mA, t_{RC} = min
	Standby	I_{SB}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2V$
Input leakage current		$\lvert I_{IL} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leakage current		$\lvert I_{OL} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, Ta = 25°C, V_{IN} = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	Cin	—	15	pF
Output capacitance	Cout	—	15	pF

Note: This parameter is sampled and not 100% tested.

AC Electrical Characteristics (V_{CC} = 3.0 to 5.5 V, V_{SS} = 0 V, Ta = 0 to +70°C)

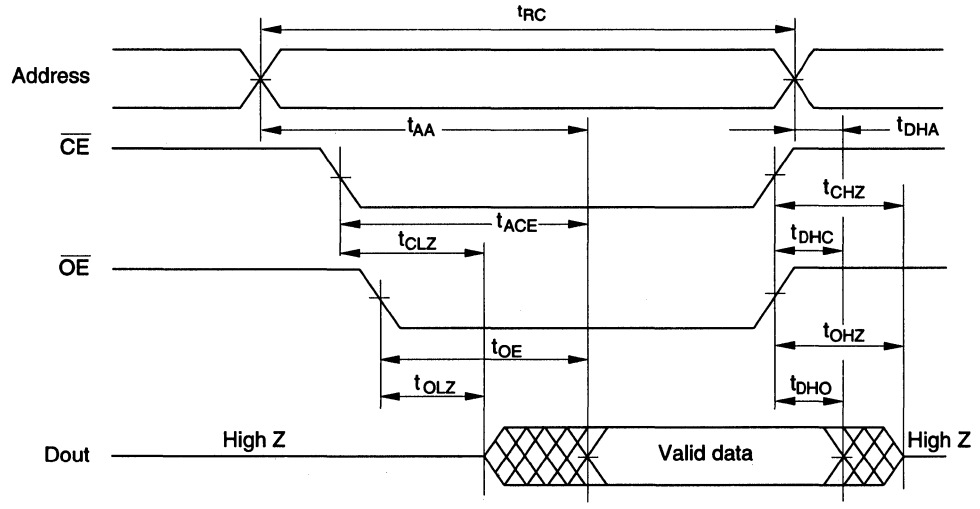
- Output load: 1TTL gate + C_L = 100 pF (including jig capacitance)
- Input pulse level: 0.6 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 10 ns

Item	Symbol	Min	Max	Unit
Read cycle time	t_{RC}	300	—	ns
Address access time	t_{AA}	—	300	ns
$\overline{CE}$ access time	t_{ACE}	—	300	ns
$\overline{OE}$ access time	t_{OE}	—	150	ns
BHE access time	t_{BHE}	—	300	ns
Output hold time from address change	t_{DHA}	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	ns
$\overline{CE}$ to output in high Z	t_{CHZ}*1	—	100	ns
$\overline{OE}$ to output in high Z	t_{OHZ}*1	—	100	ns
BHE to output in high Z	t_{BHZ}*1	—	100	ns
$\overline{CE}$ to output in low Z	t_{CLZ}	10	—	ns
$\overline{OE}$ to output in low Z	t_{OLZ}	10	—	ns
BHE to output in low Z	t_{BLZ}	10	—	ns

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

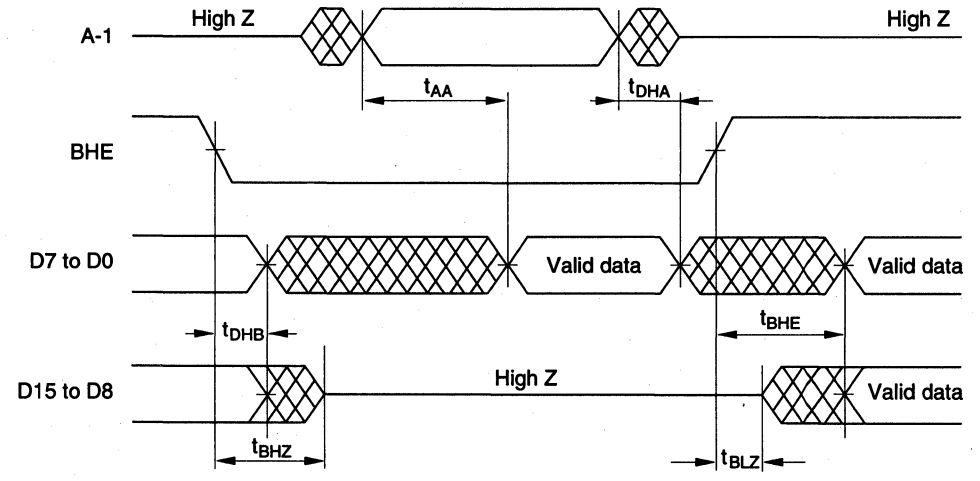
Timing Diagram

(1) Word mode (BHE = 'V_{IH}') or Byte mode (BHE = 'V_{IL}')



Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

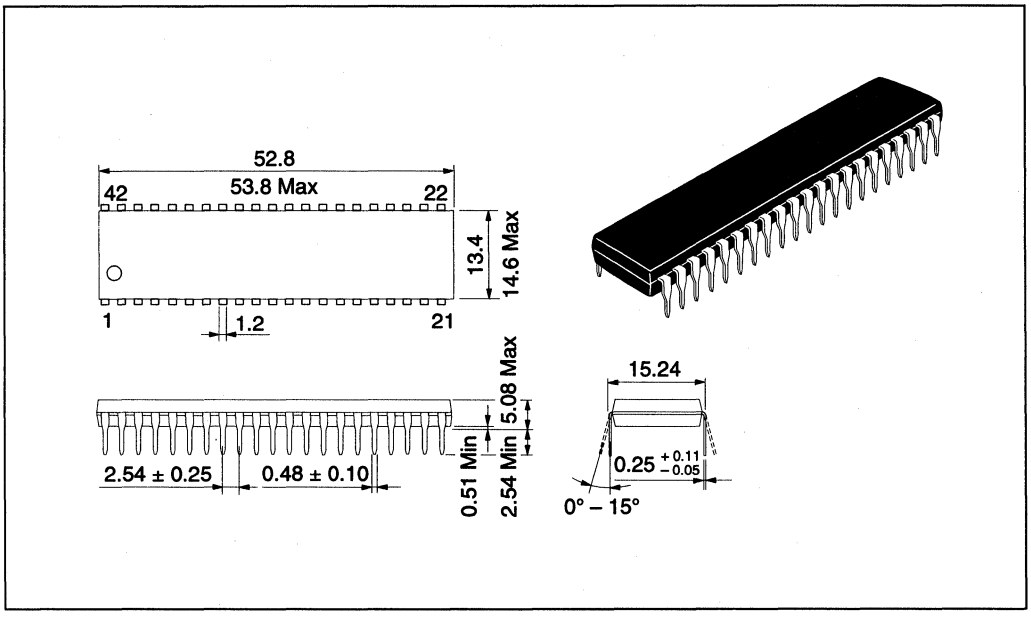
(2) Word mode, Byte mode switch



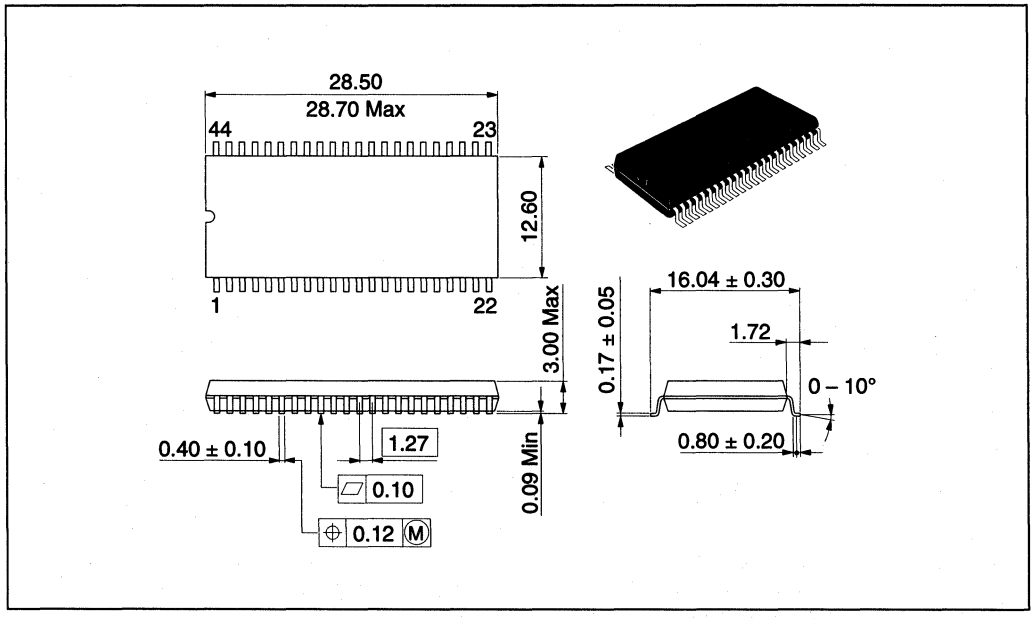
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable A18 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must not be applied to them.

Package Dimensions

HN62W428P Series (DP-42) **Unit : mm**

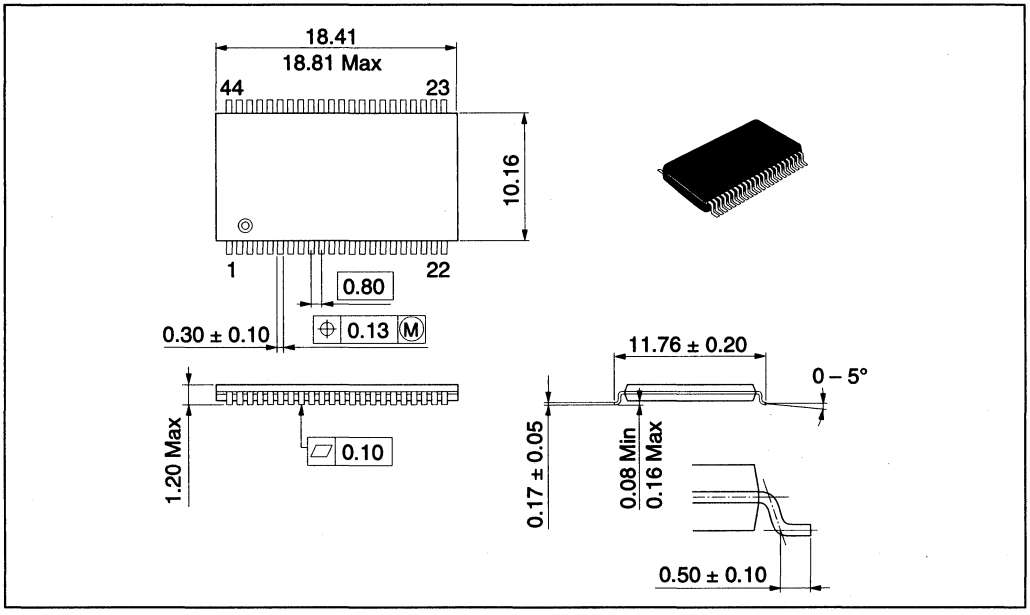


HN62W428FB Series (FP-44D) **Unit : mm**



Package Dimensions (cont)

HN62W428TT Series (TTP-44D) **Unit : mm**



HN62448 Series

524,288-word × 16-bit / 1,048,576-word × 8-bit CMOS Programmable Mask ROM

HITACHI

Rev. 1.0
June 13, 1995

The Hitachi HN62448 is a 8-Mbit CMOS Programmable Mask ROM organized either as 524,288 words by 16 bits or as 1,048,576 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. A high speed access of 100/120 ns is the most suitable to the system using a high speed microcomputer by 16 bits as 8,086 and 68,000 e.t.c.

Features

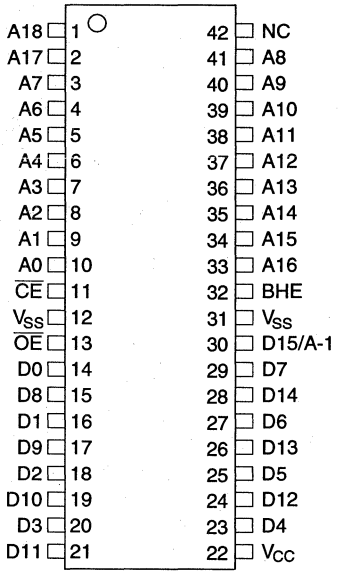
- Single + 5V power supply
- Access time: 100 ns/120 ns (max)
- Low power dissipation: 300 mW typ (active)
  5 µW typ (standby)
- Byte-wide or word-wide data organization with BHE

Ordering Information

Type No.	Access time	Package
HN62448P-10	100 ns	600mil 42-pin plastic DIP (DP-42)
HN62448P-12	120 ns	
HN62448FB-10	100 ns	44-pin plastic SOP (FP-44D)
HN62448FB-12	120 ns	
HN62448TT-10	100 ns	44-pin plastic TSOP II (TTP-44D)
HN62448TT-12	120 ns	

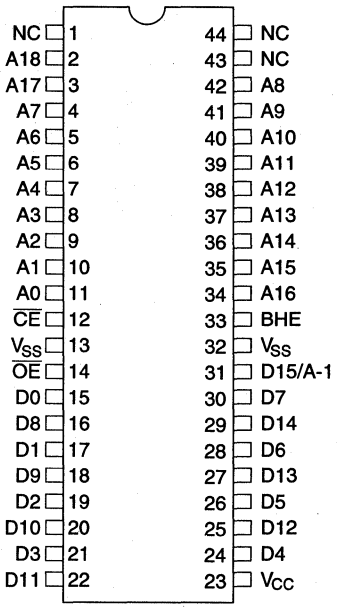
Pin Arrangement

HN62448P Series



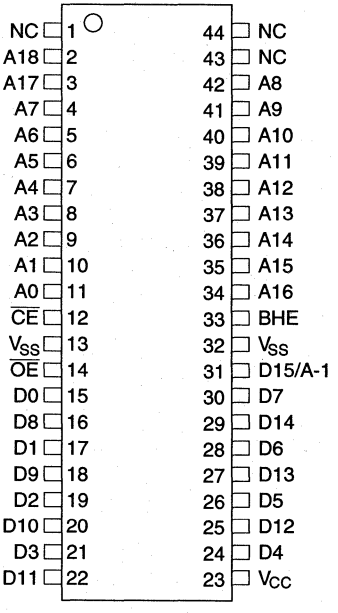
(Top View)

HN62448FB Series



(Top View)

HN62448TT Series

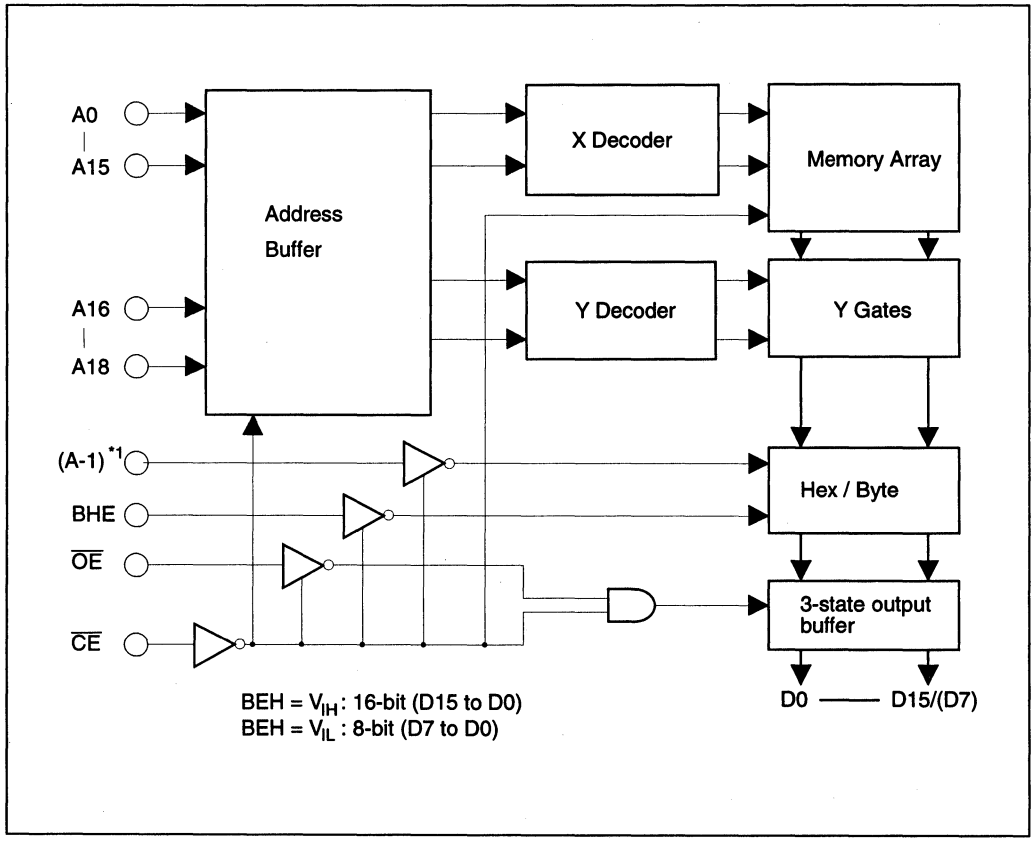


(Top View)

Pin Description

Pin name	Function
A0 to A18	Address
D0 to D14	Output
D15/A-1	Output/address
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
BHE	Byte/word selection
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	–0.3 to 7.0	V	1
All input and output voltage	Vin, Vout	–0.3 to V_{CC} +0.3	V	1
Operating temperature range	Topr	0 to 70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Notes: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{CC}	—	100/80	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ –0.2 V
	Standby	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.4 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Notes: 1. This Parameter is periodically sampled and not 100% tested.

AC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

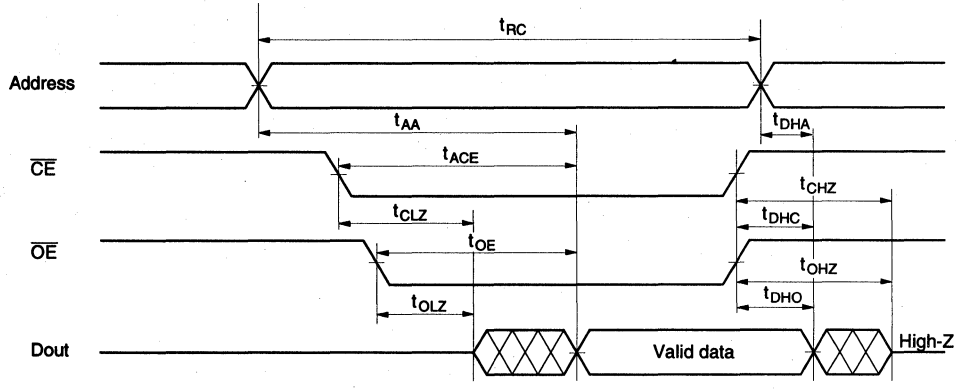
- Output load: 1TTL gate + C_L = 100 pF (including scope & jig)
- Input pulse levels: 0.45 to 2.4 V
- Input and output timing reference level: 1.5V
- Input rise and fall times: 5 ns

		HN62448-10		HN62448-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	100	—	120	—	ns
Address access time	t_{AA}	—	100	—	120	ns
$\overline{CE}$ access time	t_{ACE}	—	100	—	120	ns
$\overline{OE}$ access time	t_{OE}	—	40	—	50	ns
BHE access time	t_{BHE}	—	100	—	120	ns
Output hold time from address change	t_{DHA}	0	—	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to output in high-Z	t_{CHZ}*1	—	40	—	40	ns
$\overline{OE}$ to output in high-Z	t_{OHZ}*1	—	40	—	40	ns
BHE to output in high-Z	t_{BHZ}*1	—	40	—	40	ns
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

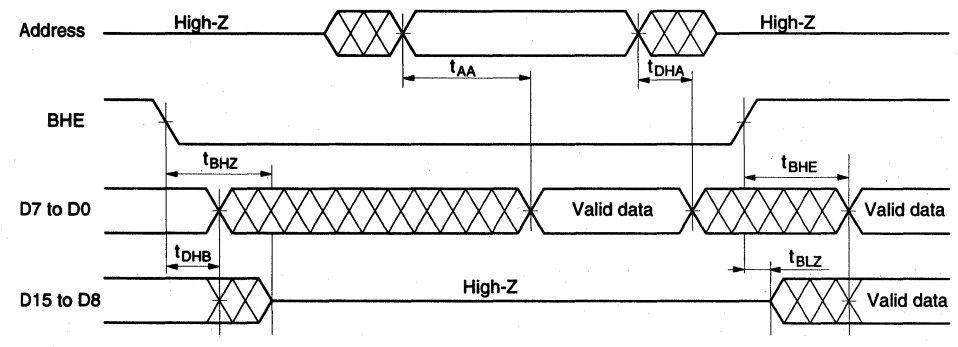
Timing Waveform

Word mode (BHE = 'V_{IH}') or Byte mode (BHE = 'V_{IL}')



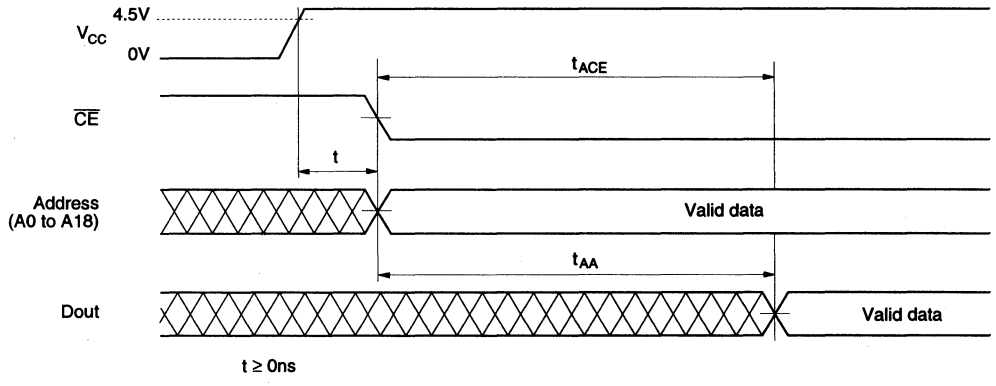
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Word mode, Byte mode switch



Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable A18 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

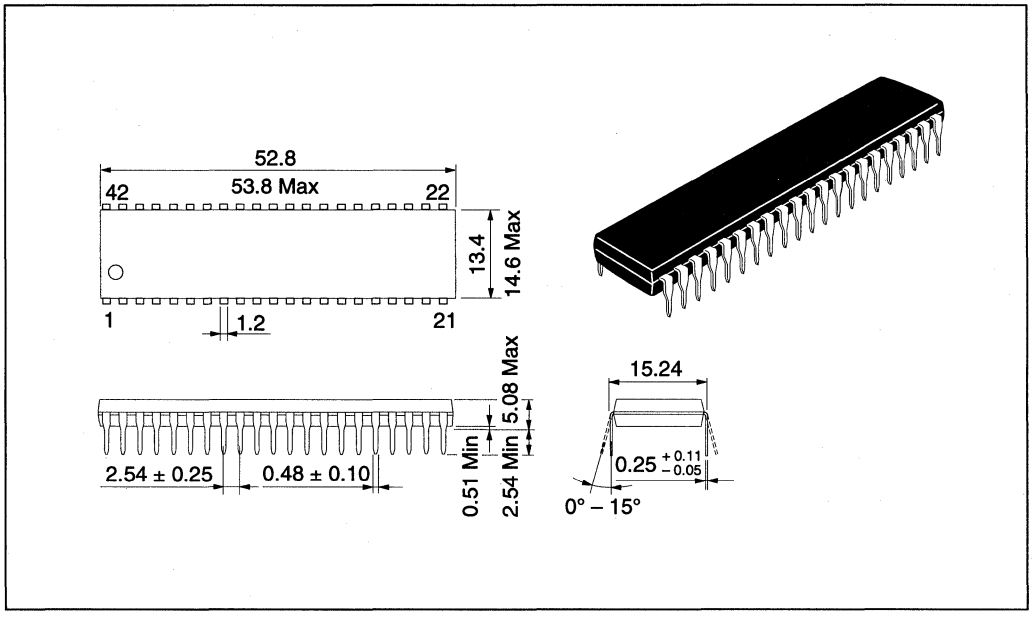
Power Up Sequence



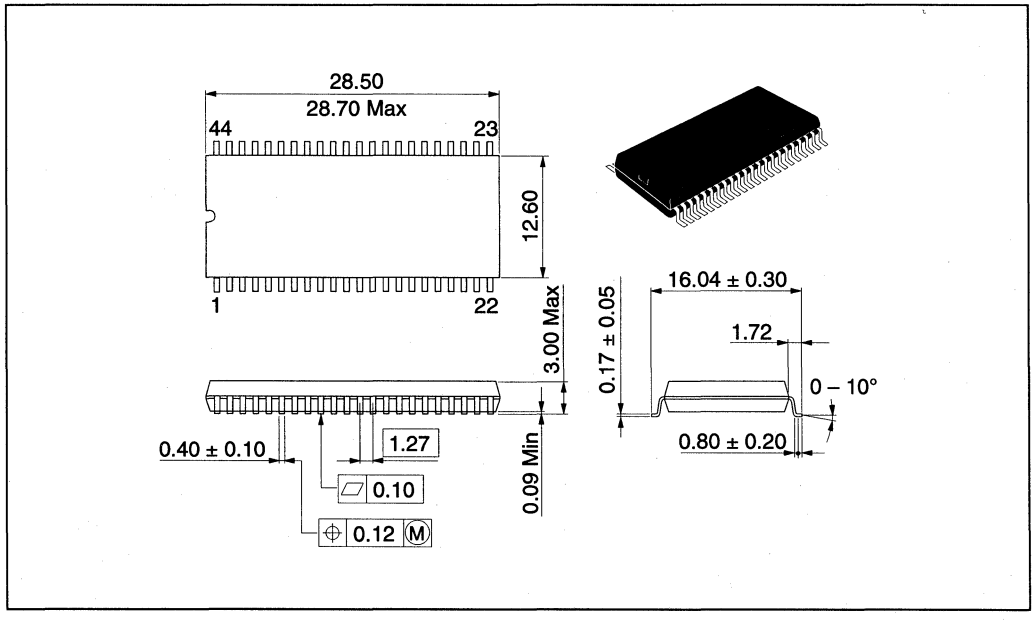
Notes: This device is used ATD (Address Transient Detector).
Therefore, transfer either $\overline{CE}$ or address (A0 to A18) after power up to 4.5 V.

Package Dimensions

HN62448P Series (DP-42) **Unit : mm**

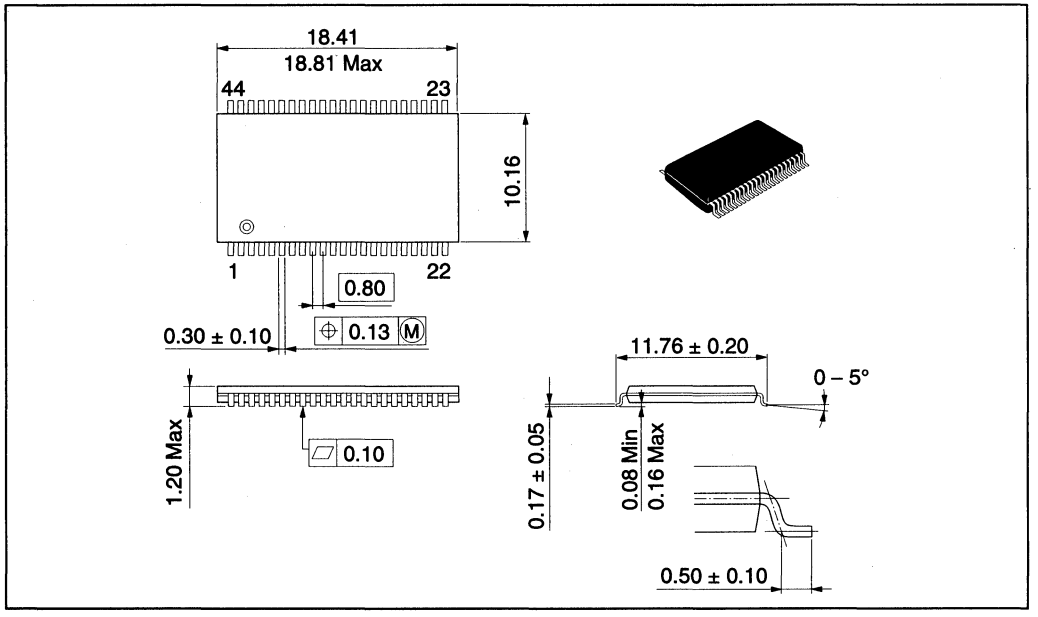


HN62448FB Series (FP-44D) **Unit : mm**



Package Dimensions (cont)

HN62448TT Series (TTP-44D) **Unit : mm**



HN62448N Series

524,288-word × 16-bit / 1,048,576-word × 8-bit CMOS Programmable Mask ROM

HITACHI

Rev. 1.0
May 23, 1995

The Hitachi HN62448N is a 8-Mbit CMOS Programmable Mask ROM organized either as 524,288 words by 16 bits or as 1,048,576 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. A high speed access of 100/120 ns is the most suitable to the system using a high speed microcomputer by 16 bits as 8,086 and 68,000 e.t.c.

Features

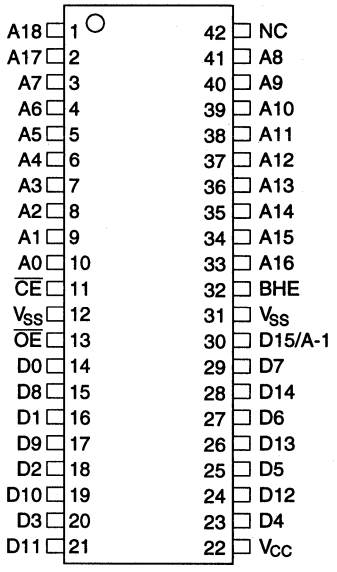
- Single + 5V power supply
- Normal access time: 100 ns/120 ns (max)
- Page access time: 40 ns/50 ns (max)
- Low power dissipation: 300 mW typ (active)
  5 µW typ (standby)
- Byte-wide or word-wide data organization with BHE

Ordering Information

Type No.	Access time	Package
HN62448NP-10	100 ns	600mil 42-pin plastic DIP (DP-42)
HN62448NP-12	120 ns	
HN62448NFB-10	100 ns	44-pin plastic SOP (FP-44D)
HN62448NFB-12	120 ns	
HN62448NTT-10	100 ns	44-pin plastic TSOP II (TTP-44D)
HN62448NTT-12	120 ns	

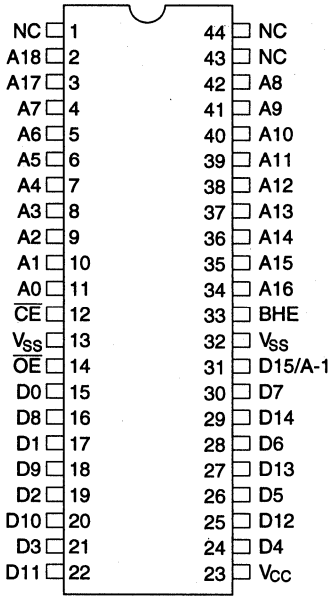
Pin Arrangement

HN62448NP Series



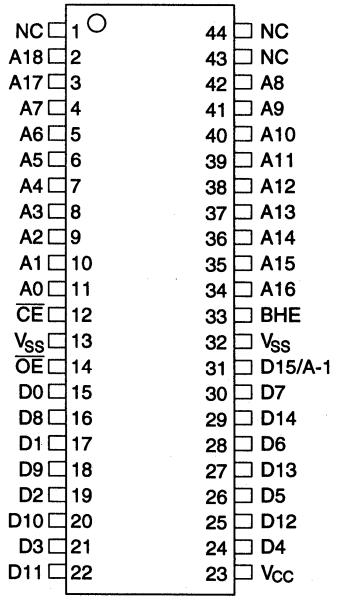
(Top View)

HN62448NFB Series



(Top View)

HN62448NTT Series

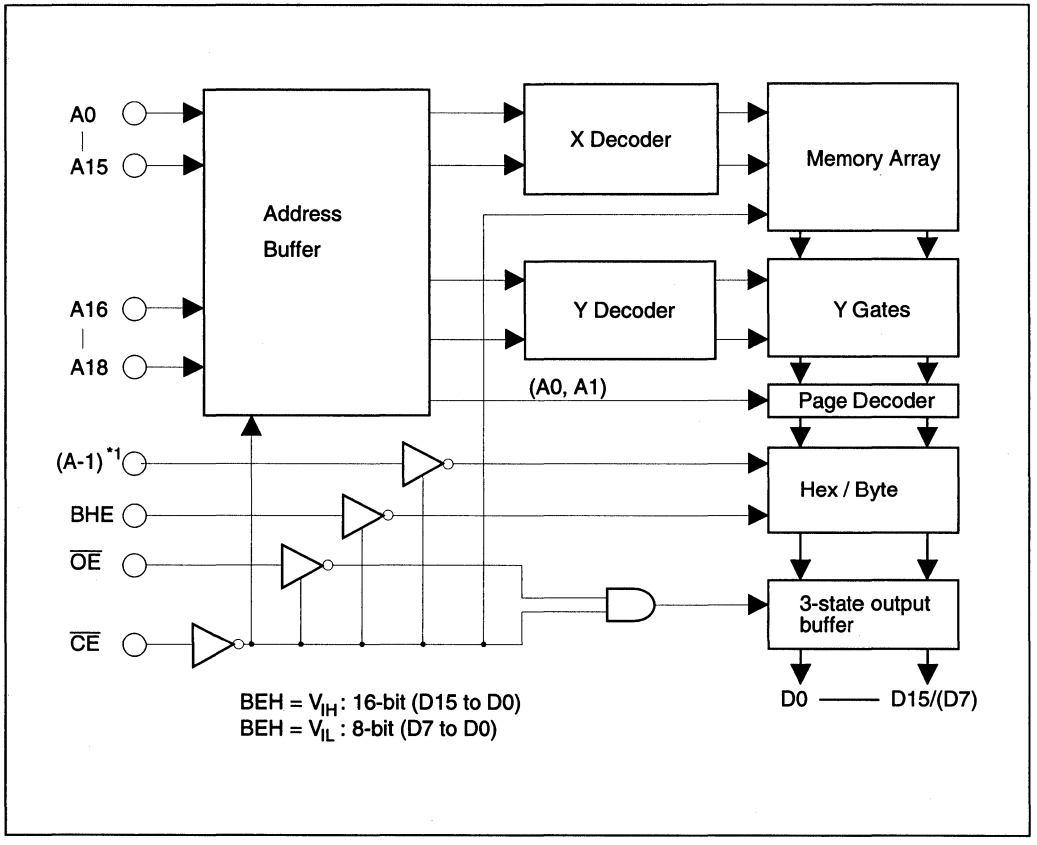


(Top View)

Pin Description

Pin name	Function
A0 to A18	Address
D0 to D14	Output
D15/A-1	Output/address
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
BHE	Byte/word selection
V_{CC}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	–0.3 to 7.0	V	1
All input and output voltage	Vin, Vout	–0.3 to V_{CC} +0.3	V	1
Operating temperature range	Topr	0 to 70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Notes: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} +0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{CC}	—	120/100	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = min
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ –0.2 V
	Standby	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.4 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	15	pF
Output capacitance*1	Cout	—	15	pF

Notes: 1. Tins Parameter is periodically sampled and not 100% tested.

AC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

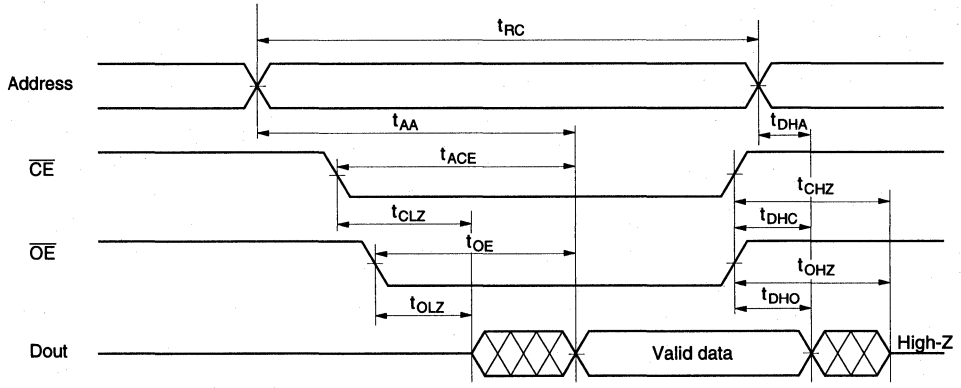
- Output load: 1TTL gate + C_L = 100 pF (including scope & jig)
- Input pulse levels: 0.45 to 2.4 V
- Input and output timing reference level: 1.5V
- Input rise and fall times: 5 ns

		HN62448N-10		HN62448N-12		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	100	—	120	—	ns
Page read cycle time	t_{PC}	40	—	50	—	ns
Address access time	t_{AA}	—	100	—	120	ns
Page address access time	t_{PA}	—	40	—	50	ns
$\overline{CE}$ access time	t_{ACE}	—	100	—	120	ns
$\overline{OE}$ access time	t_{OE}	—	40	—	50	ns
BHE access time	t_{BHE}	—	100	—	120	ns
Output hold time from address change	t_{DHA}	0	—	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to output in high-Z	t_{CHZ}*1	—	40	—	40	ns
$\overline{OE}$ to output in high-Z	t_{OHZ}*1	—	40	—	40	ns
BHE to output in high-Z	t_{BHZ}*1	—	40	—	40	ns
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

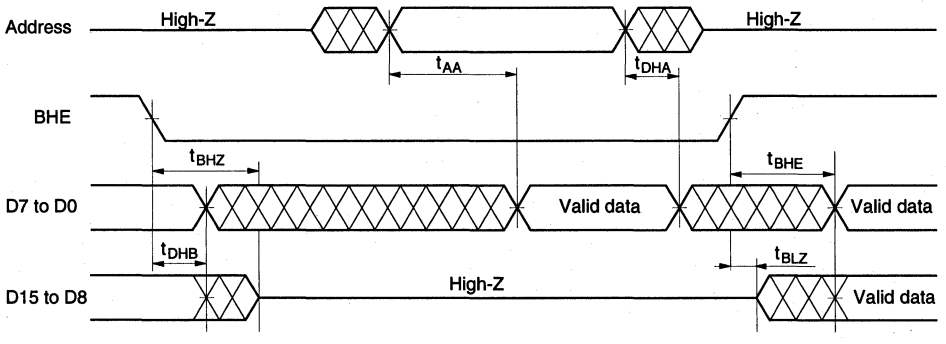
Timing Waveform

Word mode (BHE = 'V_{IH}') or Byte mode (BHE = 'V_{IL}')



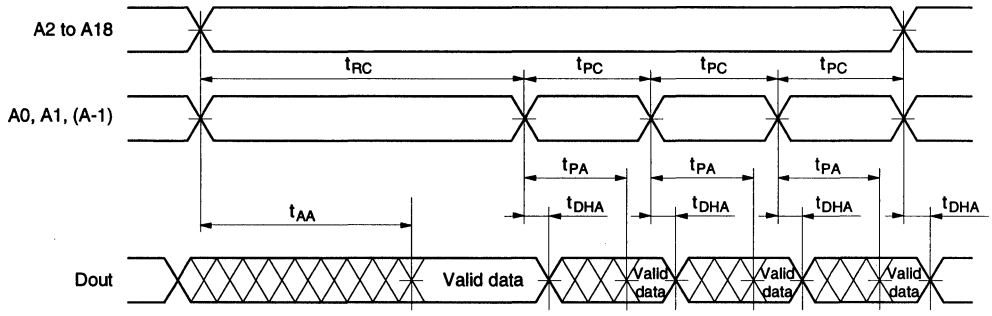
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Word mode, Byte mode switch



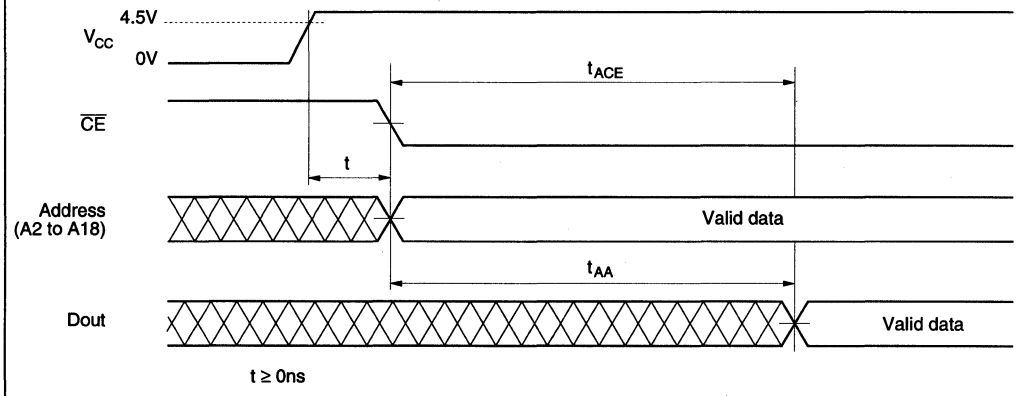
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable A18 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

Page mode



Notes: $\overline{CE}$ and $\overline{OE}$ are enable.

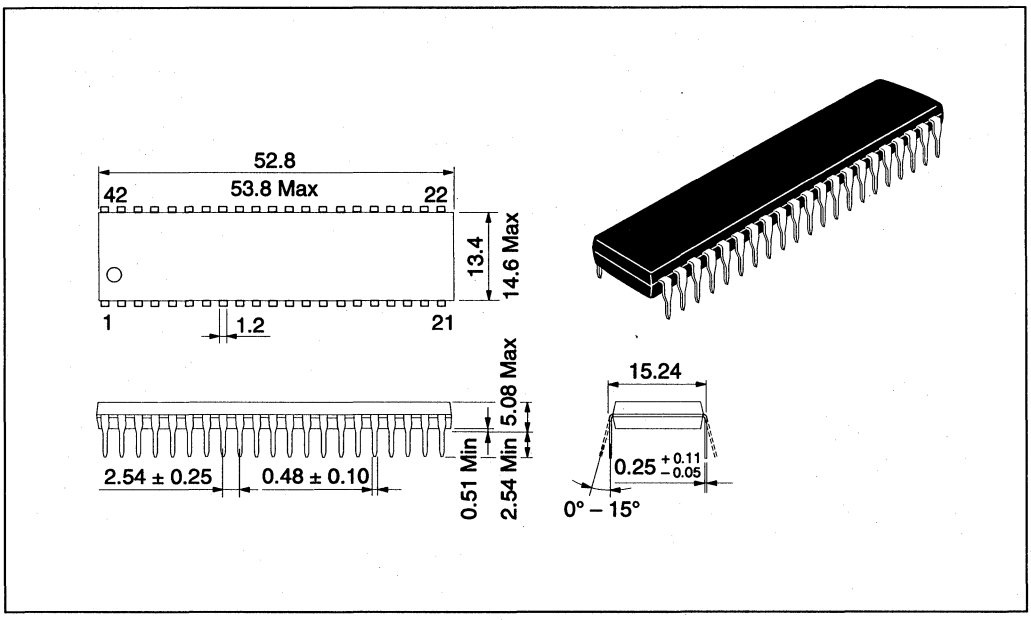
Power Up Sequence



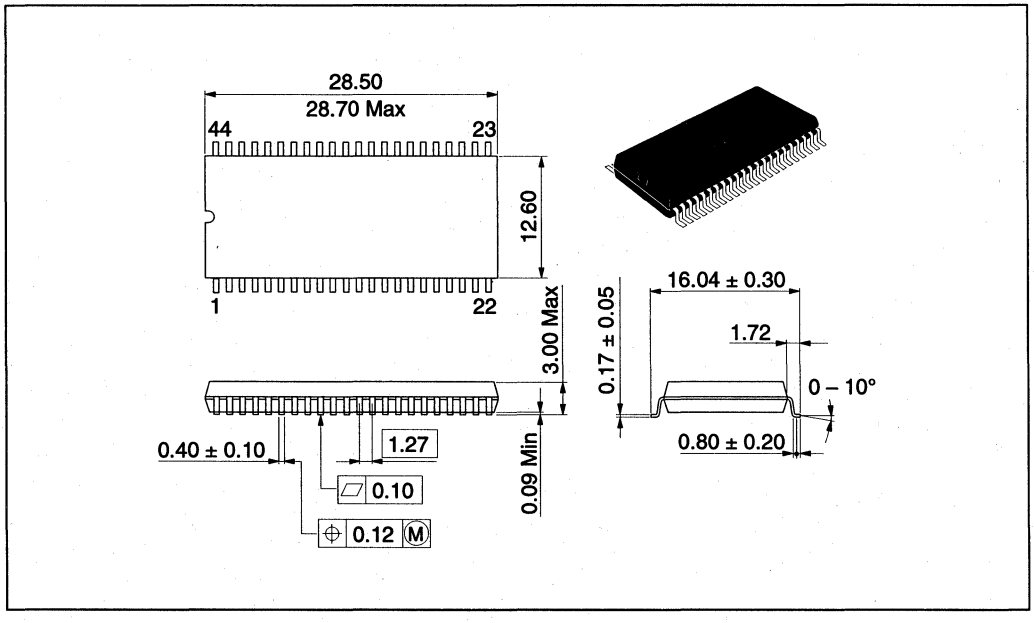
Notes: This device is used ATD (Address Transient Detector). Therefore,
@ @ @ Transfer either $\overline{CE}$ or address (A2 to A18) after power up to 4.5 V.

Package Dimensions

HN62448NP Series (DP-42) **Unit : mm**

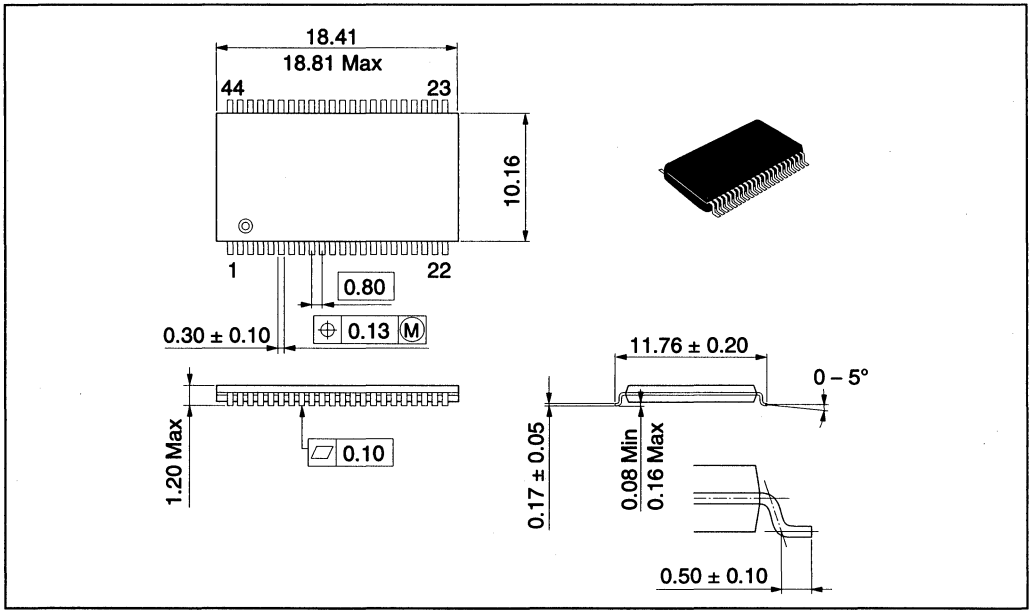


HN62448NFB Series (FP-44D) **Unit : mm**



Package Dimensions (cont)

HN62448NTT Series (TTP-44D) **Unit : mm**



HN62W448N Series

524,288-word × 16-bit / 1,048,576-word × 8-bit CMOS Programmable Mask ROM

HITACHI

Preliminary
Rev. 0.0
November 22, 1995

The Hitachi HN62W448N is a 8-Mbit CMOS Programmable Mask ROM organized either as 524,288 words by 16 bits or as 1,048,576 words by 8 bits. Realizing low power consumption with low voltage operation, this memory is allowed for battery operation. And low voltage high speed page access of 60/70 ns and normal access of 120/150 ns are realized.

Features

- Low voltage operation : 3.3 V ± 0.3 V
- Normal access time: 120/150 ns (max)
- Page access time: 60/70 ns (max)
- Low power dissipation
  Active: 220 mW (max)
  Standby: 3 µW (max)
- Byte-wide or word-wide data organization
  (Switched by BHE terminal)
- 4-word page access mode
- Three-state data output for wired or-tying
- Directly LV-TTL compatible
  All inputs and outputs

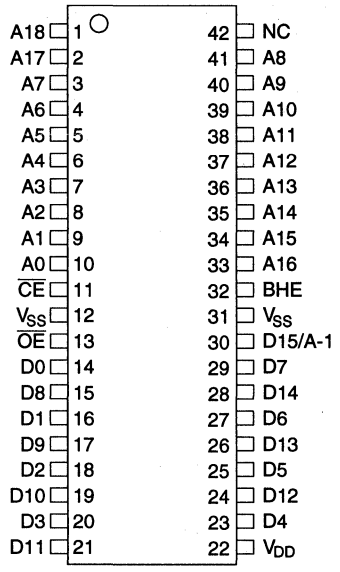
Ordering Information

Type No.	Access time	Package
HN62W448NP-12	120 ns	600mil 42-pin plastic DIP (DP-42)
HN62W448NP-15	150 ns	
HN62W448NFB-12	120 ns	44-pin plastic SOP (FP-44D)
HN62W448NFB-15	150 ns	
HN62W448NTT-12	120 ns	44-pin plastic TSOP II (TTP-44D)
HN62W448NTT-15	150 ns	

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

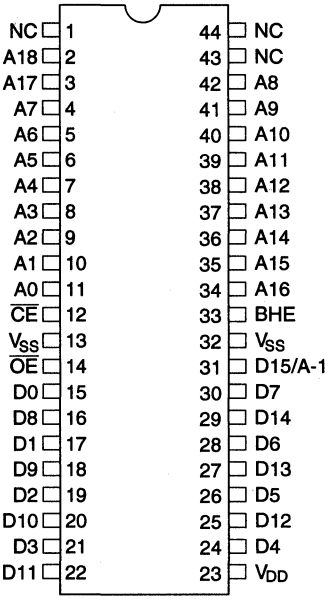
Pin Arrangement

HN62W448NP Series



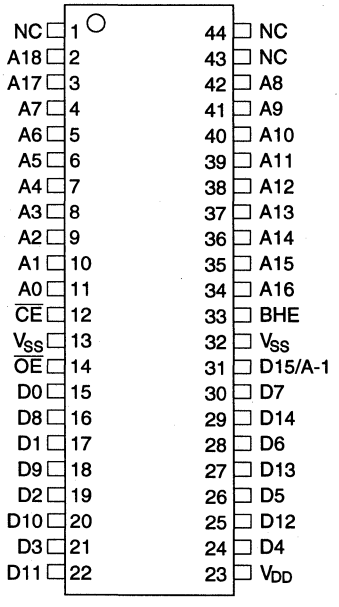
(Top View)

HN62W448NFB Series



(Top View)

HN62W448NTT Series

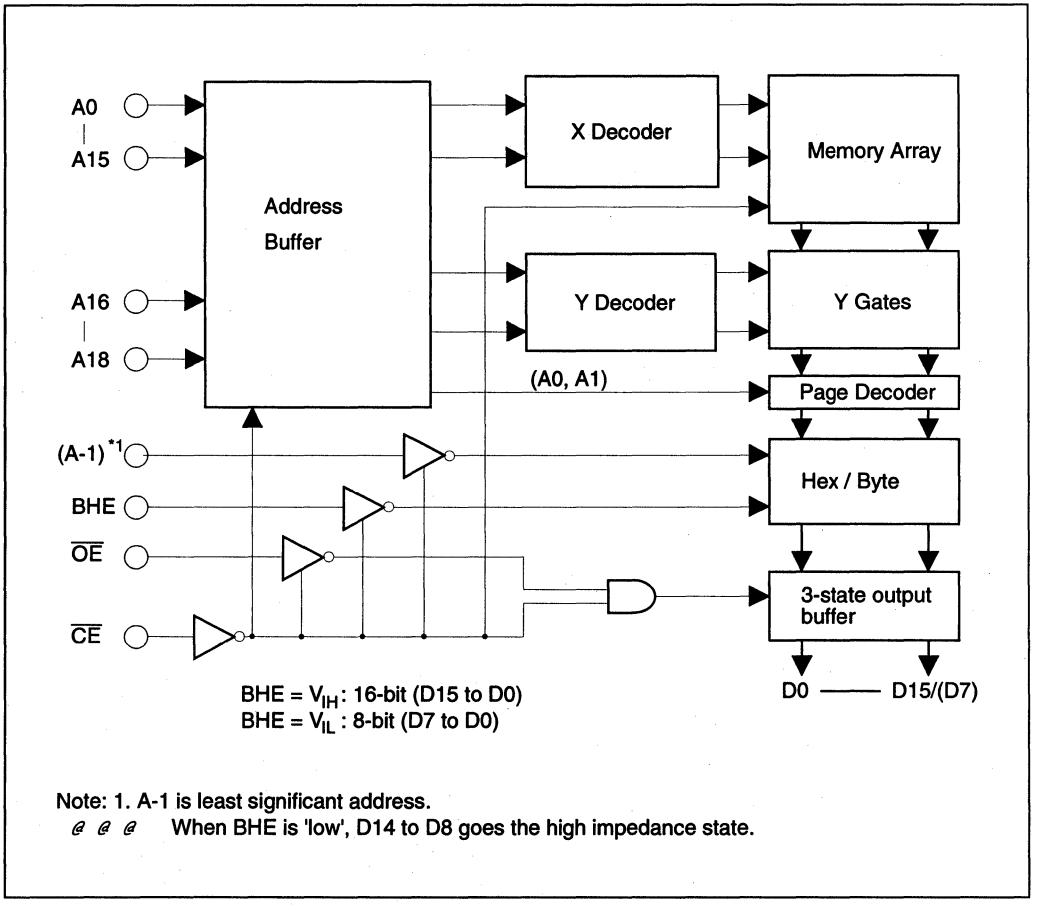


(Top View)

Pin Description

Pin name	Function
A0 to A18	Address
D0 to D14	Output
D15/A-1	Output/address
$\overline{OE}$	Output enable
$\overline{CE}$	Chip enable
BHE	Byte/word selection
V_{DD}	Power supply
V_{SS}	Ground
NC	No connection

Block Diagram



Note: 1. A-1 is least significant address.

@ @ @ When BHE is 'low', D14 to D8 goes the high impedance state.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{DD}	–0.3 to +5.5	V	1
All input and output voltage	Vin, Vout	–0.3 to V_{DD} +0.3	V	1
Operating temperature range	Topr	0 to 70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to +70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{DD} +0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{DD} = 3.3 V ± 0.3V, V_{SS} = 0 V, Ta = 0 to +70°C)

Parameter		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{DD}	—	60	mA	V_{DD} = 3.6 V, I_{DOUT} = 0 mA, t_{RC} = 120/150 ns
	Standby	I_{SB1}	—	30	µA	V_{DD} = 3.6 V, $\overline{CE} \geq V_{DD}$ –0.2 V
	Standby	I_{SB2}	—	3	mA	V_{DD} = 3.6 V, $\overline{CE}$ = 2.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{DD}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{DD}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –2.0 mA
		V_{OL}	—	0.4	V	I_{OL} = 2.0 mA

Capacitance (V_{DD} = 3.3 V ± 0.3V, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. Tins Parameter is periodically sampled and not 100% tested.

AC Characteristics (V_{DD} = 3.3 V ± 0.3V, V_{SS} = 0 V, Ta = 0 to + 70°C)

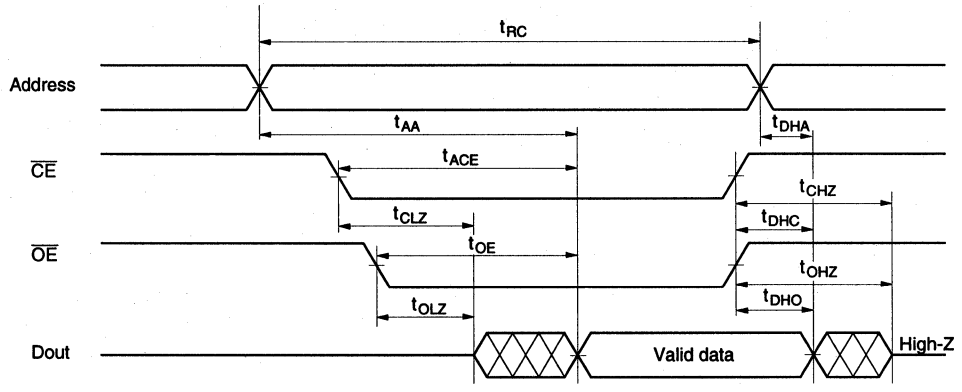
- Output load: 1TTL gate + C_L = 100 pF (including scope & jig)
- Input pulse levels: 0.4 to 2.4 V
- Input and output timing reference level: 1.4V
- Input rise and fall time: 5 ns

		HN62W448N-12		HN62W448N-15		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
Read cycle time	t_{RC}	120	—	150	—	ns
Page read cycle time	t_{PC}	60	—	70	—	ns
Address access time	t_{AA}	—	120	—	150	ns
Page address access time	t_{PA}	—	60	—	70	ns
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns
$\overline{OE}$ access time	t_{OE}	—	60	—	70	ns
BHE access time	t_{BHE}	—	120	—	150	ns
Output hold time from address change	t_{DHA}	0	—	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to output in high-Z	t_{CHZ}*1	—	60	—	70	ns
$\overline{OE}$ to output in high-Z	t_{OHZ}*1	—	60	—	70	ns
BHE to output in high-Z	t_{BHZ}*1	—	60	—	70	ns
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

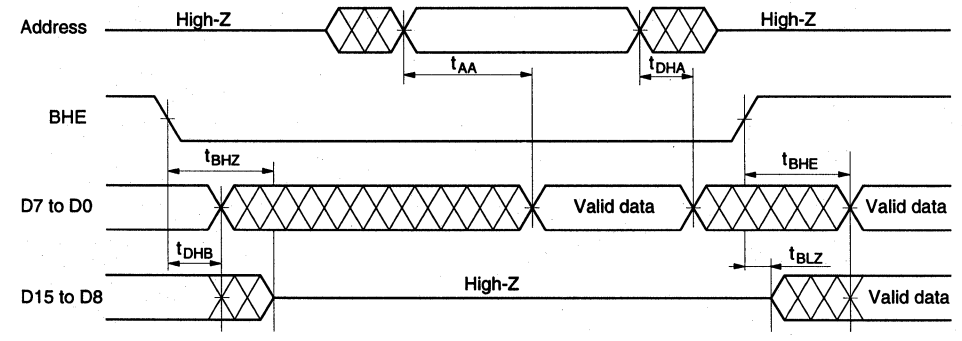
Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



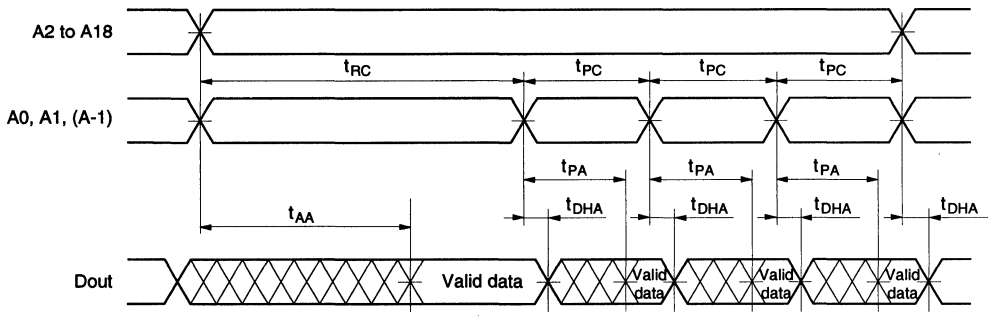
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Word Mode, Byte Mode Switch



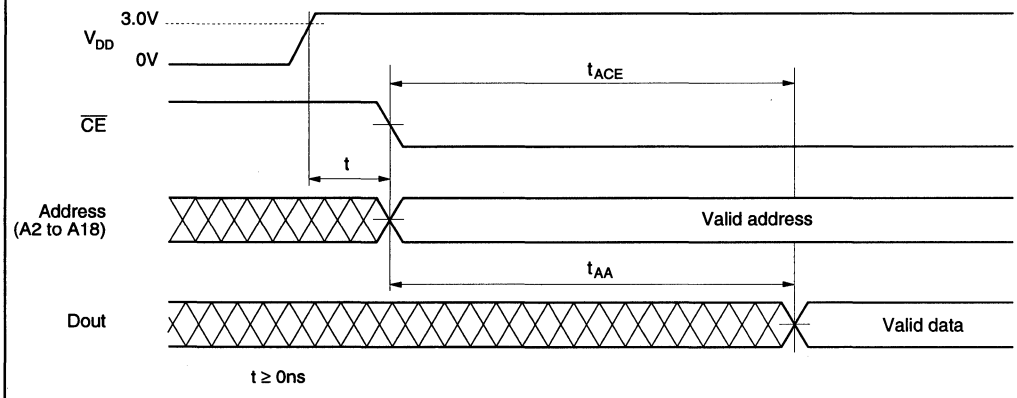
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable A18 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

Page Mode



Notes: $\overline{CE}$ and $\overline{OE}$ are enable.

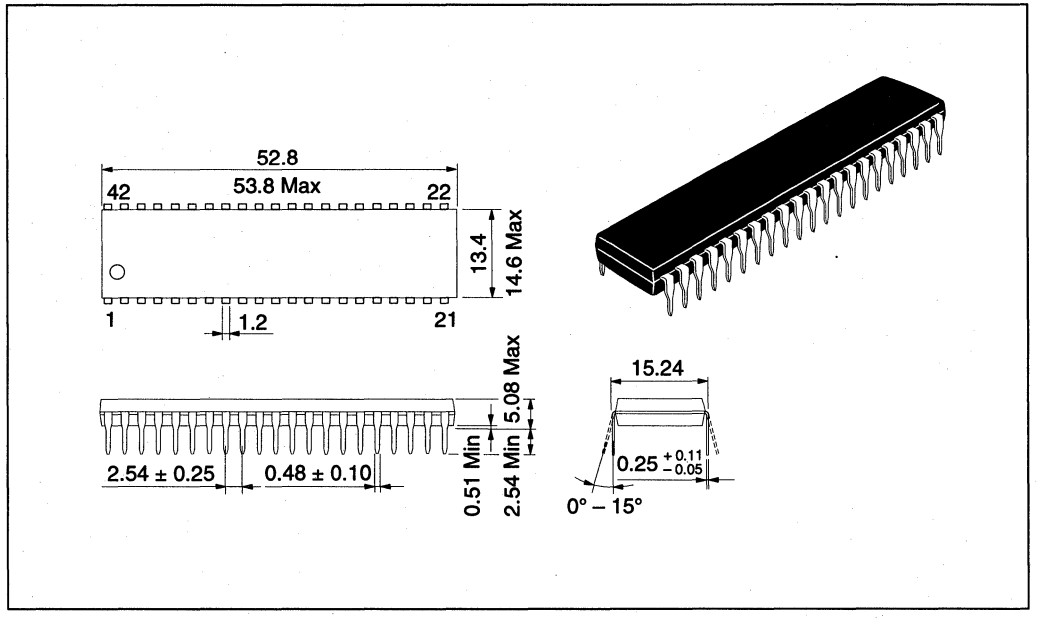
Power Up Sequence



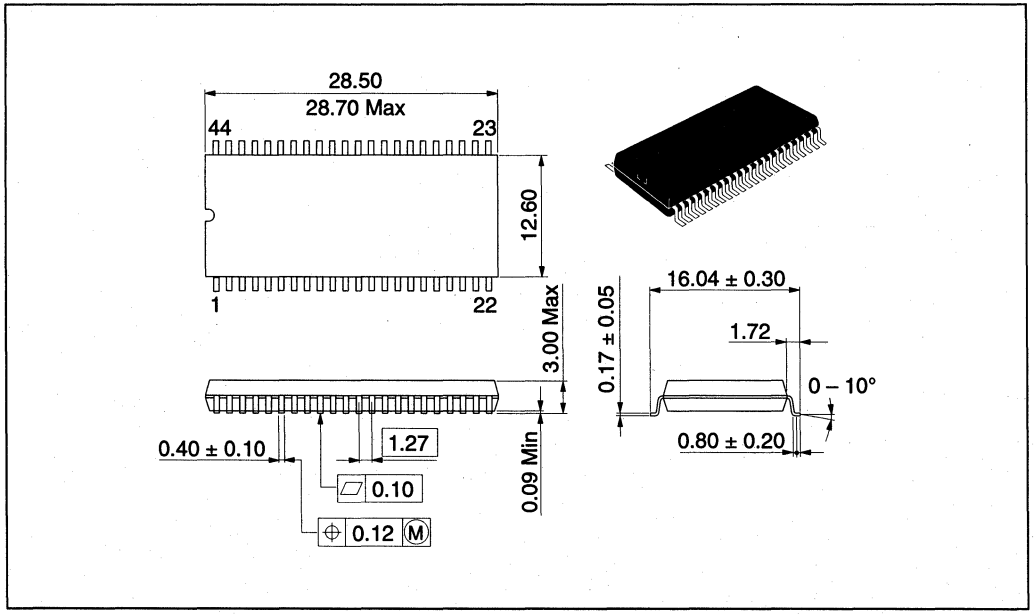
Notes: This device is used ATD (Address Transient Detector). Therefore,
@ @ @ Transfer either $\overline{CE}$ or address (A2 to A18) after power up to 3.0 V.

Package Dimensions

HN62W448NP Series (DP-42) **Unit : mm**

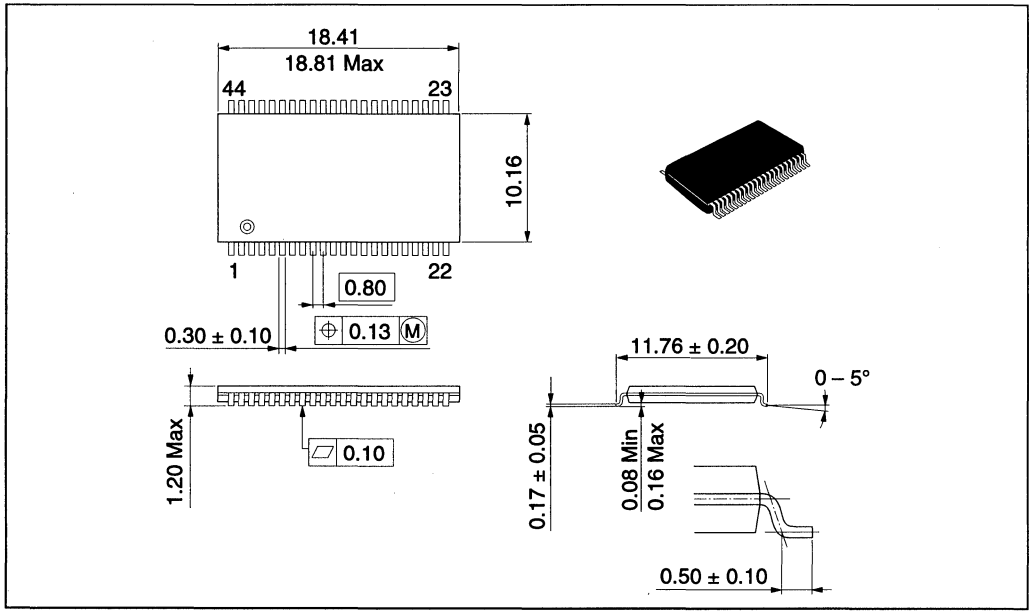


HN62W448NFB Series (FP-44D) **Unit : mm**



Package Dimensions (cont)

HN62W448NTT Series (TTP-44D) **Unit : mm**



16M Mask ROM

ADE-203-447 (Z)

HN62W4018M Series

1,048,576-word × 16-bit CMOS Programmable Mask ROM

HITACHI

Preliminary
Rev. 0.0
November 1, 1995

The HN62W4018M is a 16-Mbit CMOS Programmable Mask ROM organized as 1,048,576 words by 16 bits. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 120/150 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Ordering Information

Type No.	Access time	Package
HN62W4018MTA-12	120 ns	48 pin plastic TSOP - II (TTP-48D)
HN62W4018MTA-15	150 ns	

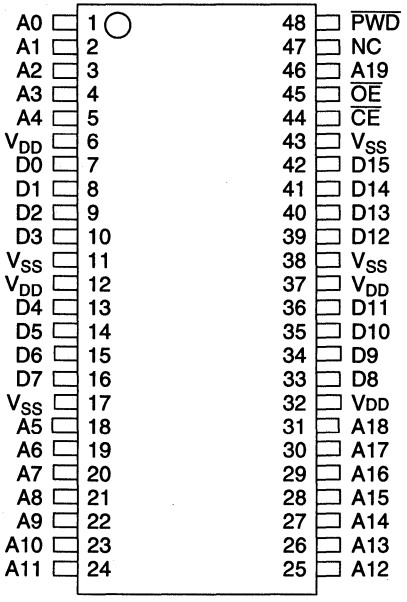
Features

- Low voltage operation: 3.3 V ± 0.3 V
- High speed
  Normal access time: 120 ns/150 ns (max)
  Page access time: 40 ns/50 ns (max)
- Low power consumption
  Active : 360 mW (max)
  Standby : 0.72 mW (max)
  Power down mode : 36 µW (max)
- 8-word page access mode
- Three-state data output for or-tying
- LV-TTL compatible

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Pin Arrangement

HN62W4018MTA



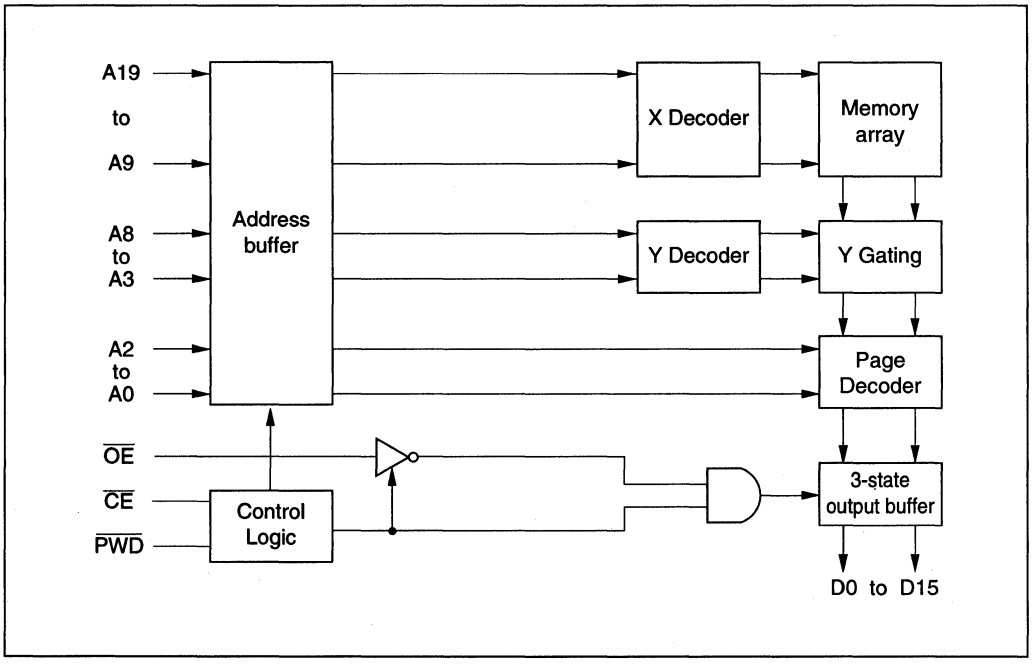
(Top view)

Pin Description

Pin name	Function
A3 to A19	Address inputs
A0 to A2	Page address inputs
D0 to D15	Data output
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable

Pin name	Function
$\overline{PWD}$	Power down input
NC	No connection
V_{DD}	Power supply
V_{SS}	Ground

Block Diagram



Mode Selection

	Pin					
				Data output	Address input	
Mode	**$\overline{PWD}$**	**$\overline{CE}$**	**$\overline{OE}$**	**D0-D15**	**LSB**	**MSB**
Power down	L	×[*1]	×	High-Z[*2]	—	—
Standby	H	H	×	High-Z	—	—
Output disable	H	L	H	High-Z	—	—
Read (16-bit)	H	L	L	D0 to D15	A0	A19

Notes: 1. ×: Don't care.
2. High-Z: High impedance.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{DD}	–0.3 to +5.5	V	1
All input and output voltage	Vin, Vout	–0.3 to V_{DD} + 0.3	V	1
Operating temperatue range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}

Recommended DC Operating Conditions (V_{SS} = 0 V, Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IH}	2.2	—	V_{DD} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Test condition
Active supply current	I_{DD}	—	100	mA	V_{DD} = 3.6 V, I_{DOUT} = 0 mA, t_{RC} = min
Standby power supply current	I_{SB1}	—	200	µA	V_{DD} = 3.6 V, $\overline{CE} \geq V_{DD} - 0.2$ V
	I_{SB2}	—	3	mA	V_{DD} = 3.6 V, $\overline{CE} \geq 2.2$ V
Power down supply current	I_{PWD}	—	10	µA	V_{DD} = 3.6 V, $\overline{PWD} \leq 0.2$ V
Input leakage current	$\|I_{IL}\|$	—	10	µA	Vin = 0 V to V_{DD}
Output leakage current	$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 V to V_{DD}
Output voltage	V_{OH}	2.4	—	V	I_{OH} = –2 mA
	V_{OL}	—	0.4	V	I_{OL} = 2 mA

Capacitance (V_{DD} = 3.3 V ±0.3 V, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70°C)

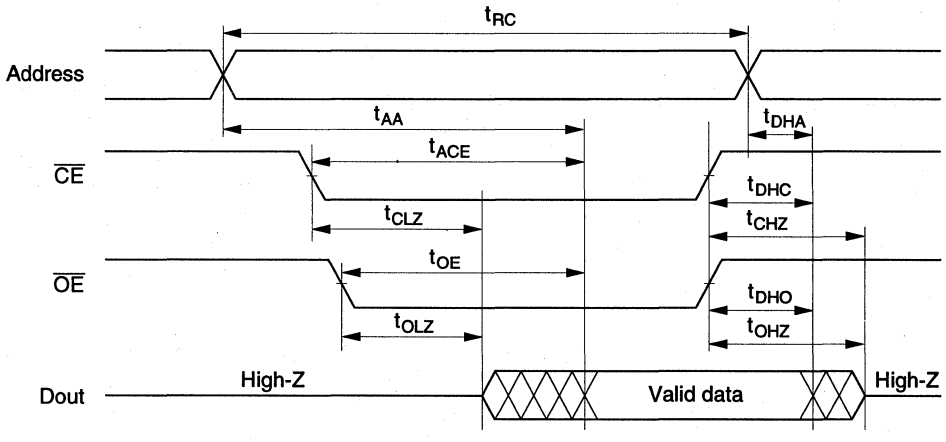
- Output load: 1TTL + C_L = 100 pF (including jig capacitance)
- Input pulse level: 0.4 V to 2.4 V
- Input and output timing reference level: 1.4 V
- Input rise and fall time: 5 ns

		HN62W4018M-12		HN62W4018M-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	120	—	150	—	ns	
Page read cycle time	t_{PC}	40	—	50	—	ns	
Address access time	t_{AA}	—	120	—	150	ns	
Page address access time	t_{PA}	—	40	—	50	ns	
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	40	—	50	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from $\overline{PWD}$	t_{DHP}	0	—	0	—	ns	
$\overline{CE}$ to output in high Z	t_{CHZ}	—	40	—	50	ns	1
$\overline{OE}$ to output in high Z	t_{OHZ}	—	40	—	50	ns	1
$\overline{CE}$ to output in low Z	t_{CLZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low Z	t_{OLZ}	5	—	5	—	ns	
Recovery time from $\overline{PWD}$	t_R	10	—	10	—	µs	

Note: 1. t_{CHZ} and t_{OHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

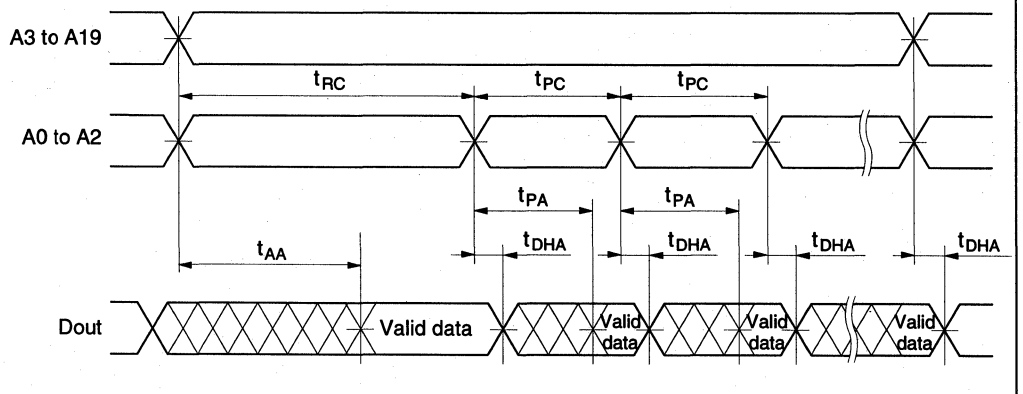
Timing Waveform

Normal Mode



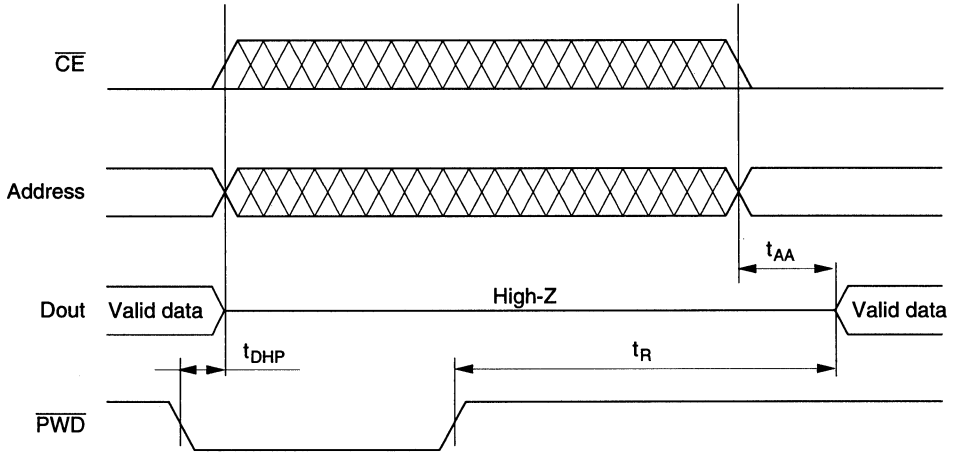
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Page Mode

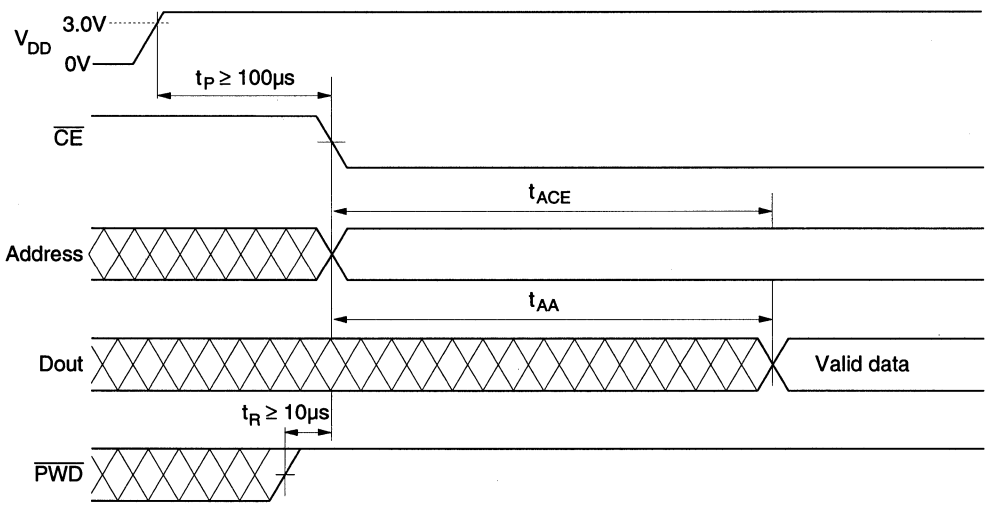


Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable.

Power Down Mode



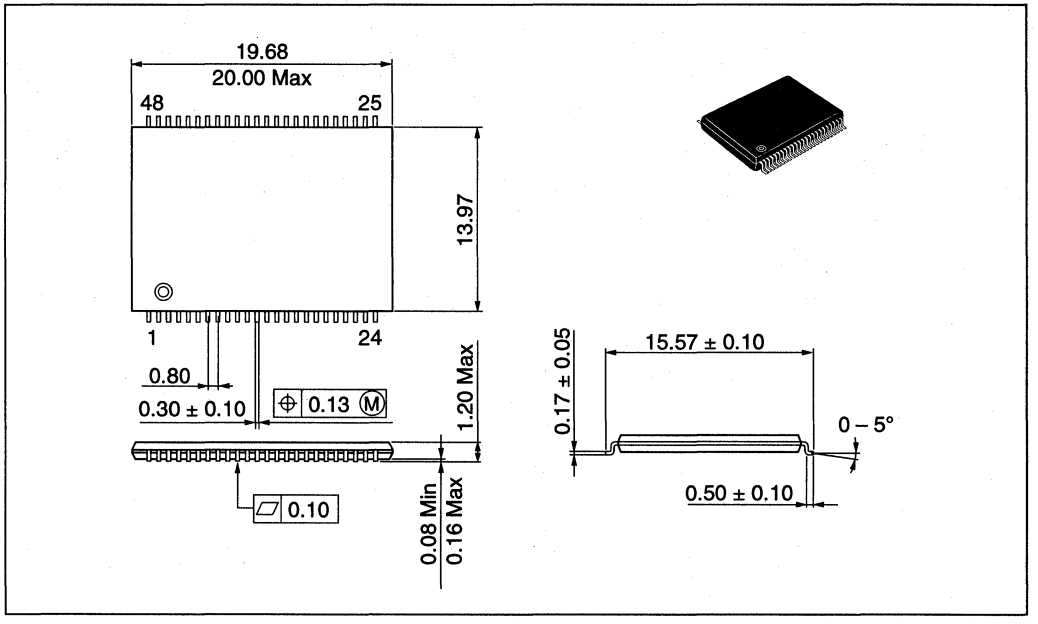
Power Up Sequence



Notes: 1. This device is used ATD(Address Transition Detector). Therefore, transfer either $\overline{CE}$ or address(A19 to A3) after power up to 3.0 V.
2. t_P, t_R: Determined by slower.

Package Dimensions

HN62W4018MTA Series (TTP-48D) **Unit : mm**



HN624316 Series

1,048,576-word × 16-bit / 2,097,152 × 8-bit CMOS Programmable Mask ROM

HITACHI

The HN624316 is a 16-Mbit CMOS Programmable Mask ROM organized either as 1,048,576 words by 16 bits or as 2,097,152 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 120/150 ns is the most suitable to the system using a high speed microcomputer by 16 bits as 8,086 and 68,000, etc.

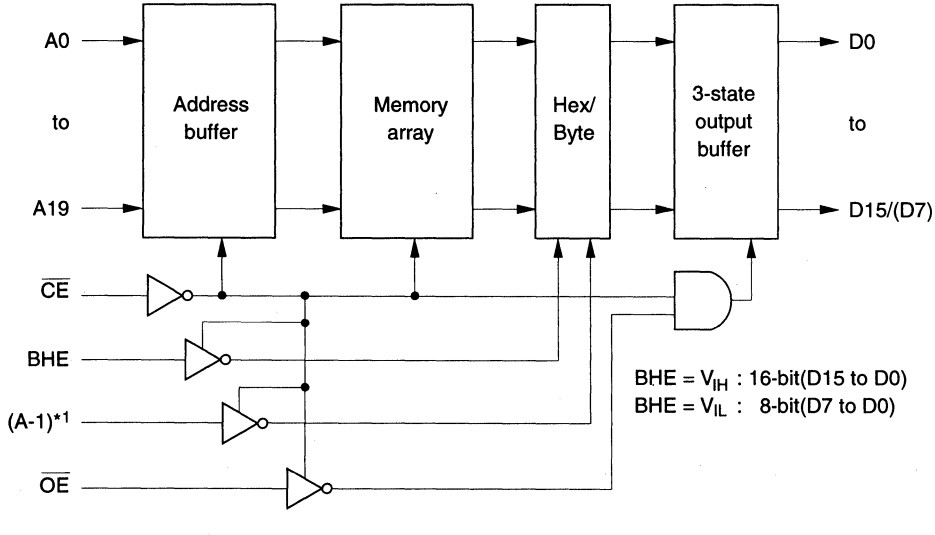
Features

- Single +5 V power supply
- Maximum access time: 120/150 ns (max)
- Low power consumption: 300 mW (typ) active
  5 μW (typ) standby
- Byte-wide or word-wide data organization with BHE

Ordering Information

Type No.	Access time	Package
HN624316P-12	120 ns	600 mil 42-pin plastic DIP (DP-42)
HN624316P-15	150 ns	
HN624316FB-12	120 ns	44-pin plastic SOP (FP-44D)
HN624316FB-15	150 ns	
HN624316TA-12	120 ns	48-pin plastic TSOP-II (TTP-48D)
HN624316TA-15	150 ns	

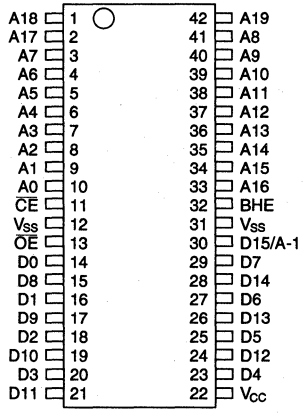
Block Diagram



Note: 1. A-1 is least significant address.
When BHE is 'low', D14 to D8 goes the high impedance state.

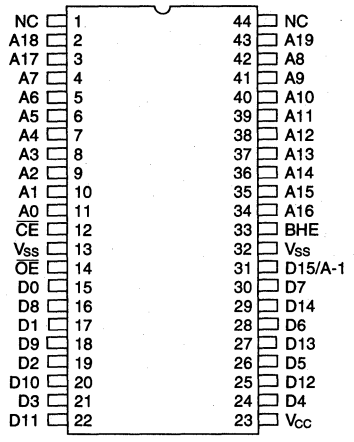
Pin Arrangement

HN624316P



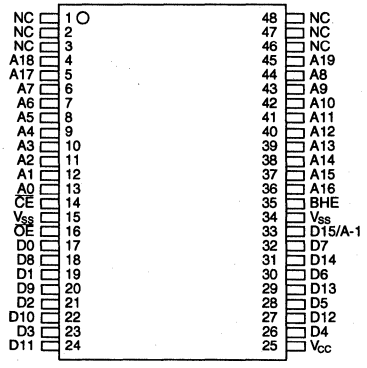
(Top view)

HN624316FB



(Top view)

HN624316TA



(Top view)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	–0.3 to +7.0	V	1
All input and output voltage	Vin, Vout	–0.3 to V_{CC} + 0.3	V	1
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

Item		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	90/80	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = 120 ns/150 ns
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
	Standby	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\lvert I_{IL} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leakage current		$\lvert I_{OL} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta =25°C, V_{IN} = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	Cin	—	15	pF
Output capacitance	Cout	—	15	pF

Note: This parameter is sampled and not 100% tested.

AC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

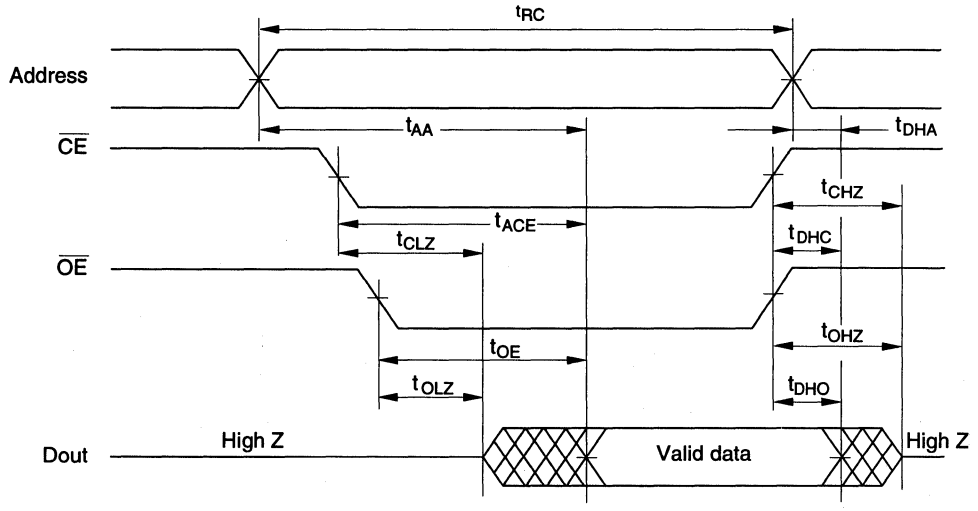
- Output load: 1TTLgate + C_L = 100 pF (including jig capacitance)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 5 ns

		HN624316-12		HN624316-15		
Item	Symbol	Min	Max	Min	Max	Unit
Read cycle time	t_{RC}	120	—	150	—	ns
Address access time	t_{AA}	—	120	—	150	ns
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns
$\overline{OE}$ access time	t_{OE}	—	55	—	70	ns
BHE access time	t_{BHE}	—	120	—	150	ns
Output hold time from address change	t_{DHA}	0	—	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to output in high Z	t_{CHZ}*1	—	40	—	70	ns
$\overline{OE}$ to output in high Z	t_{OHZ}*1	—	40	—	70	ns
BHE to output in high Z	t_{BHZ}*1	—	40	—	70	ns
$\overline{CE}$ to output in low Z	t_{CLZ}	5	—	5	—	ns
$\overline{OE}$ to output in low Z	t_{OLZ}	5	—	5	—	ns
BHE to output in low Z	t_{BLZ}	5	—	5	—	ns

Note: 1. t_{CHZ} and t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

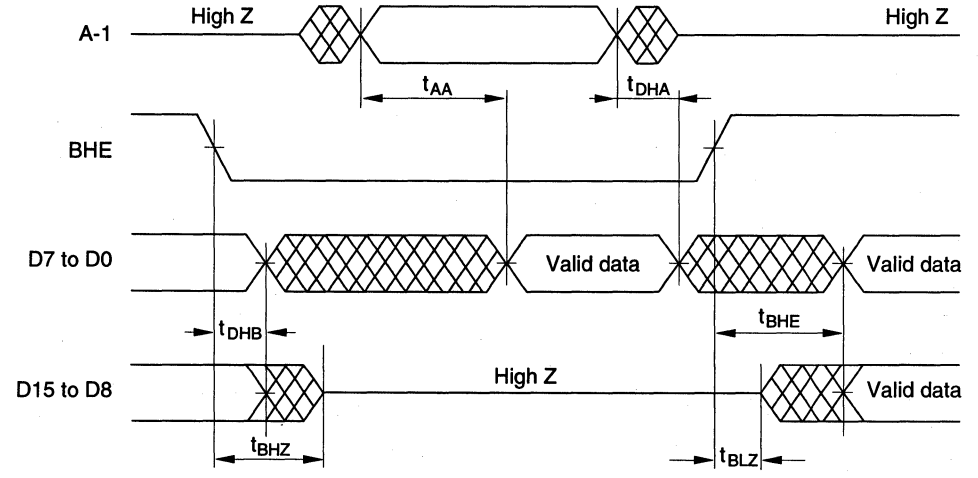
Timing Diagram

(1) Word mode (BHE = 'V_{IH}') or Byte mode (BHE = 'V_{IL}')



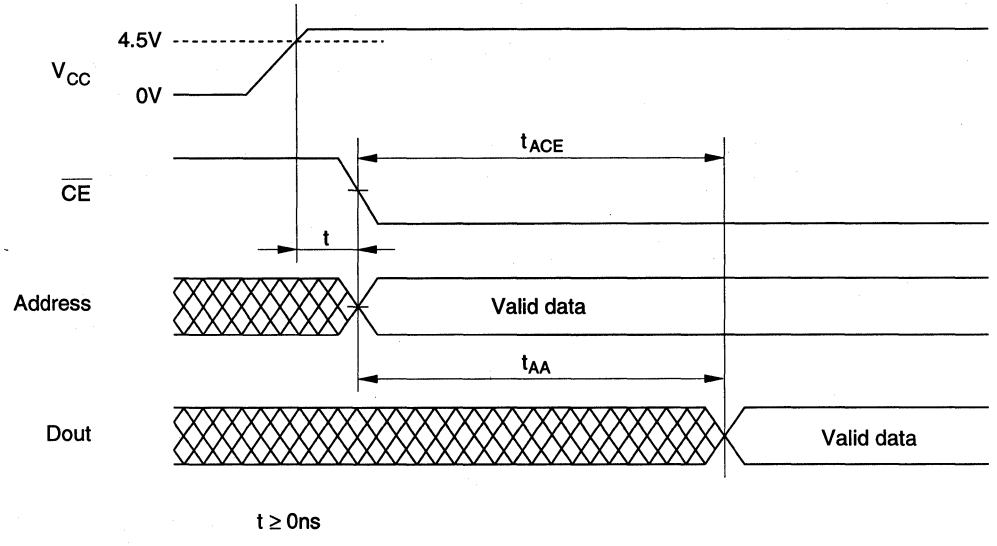
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

(2) Word mode, Byte mode switch



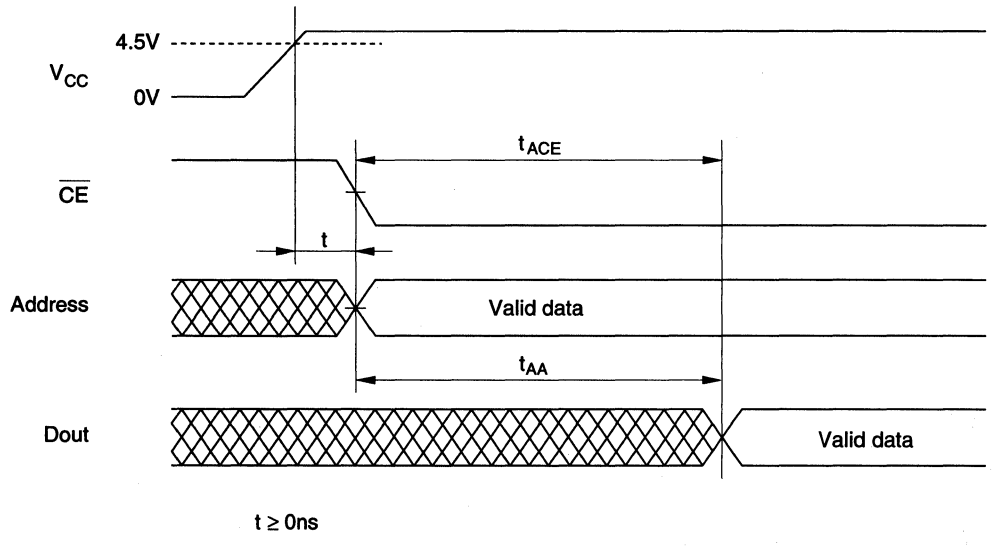
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable A19 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must not be applied to them.

Power Up Sequence



Note: This device is used ATD (Address Transient Detector). Therefore, transfer either $\overline{CE}$ or address after power up to 4.5 V.

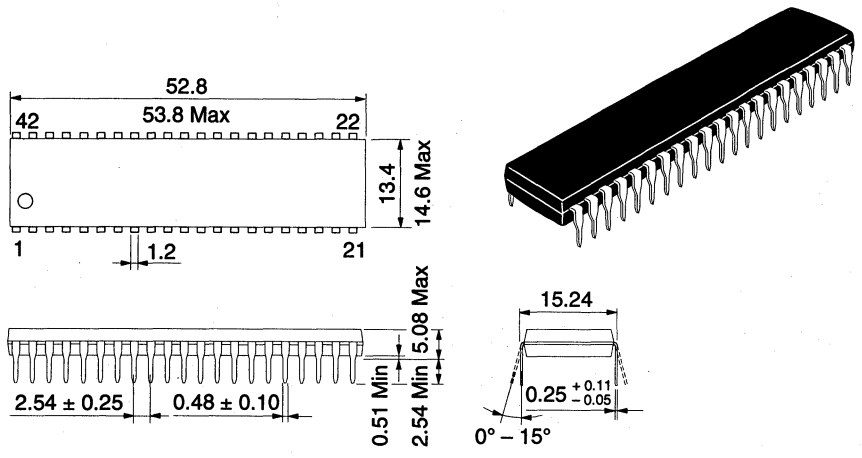
Power Up Sequence



Note: This device is used ATD (Address Transient Detector). Therefore, transfer either $\overline{CE}$ or address after power up to 4.5 V.

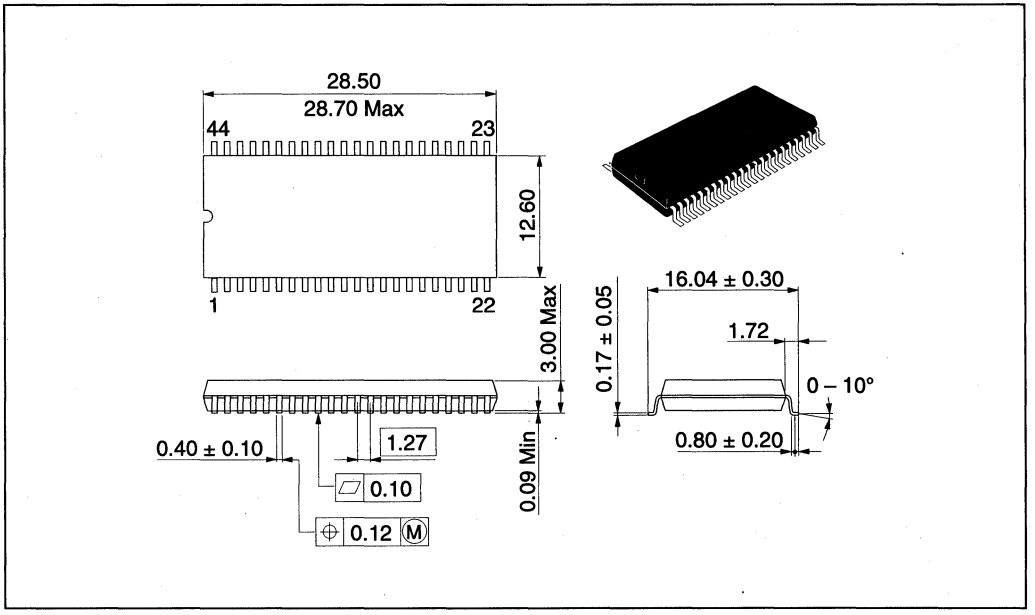
Package Dimensions

HN624316P Series (DP-42) **Unit : mm**

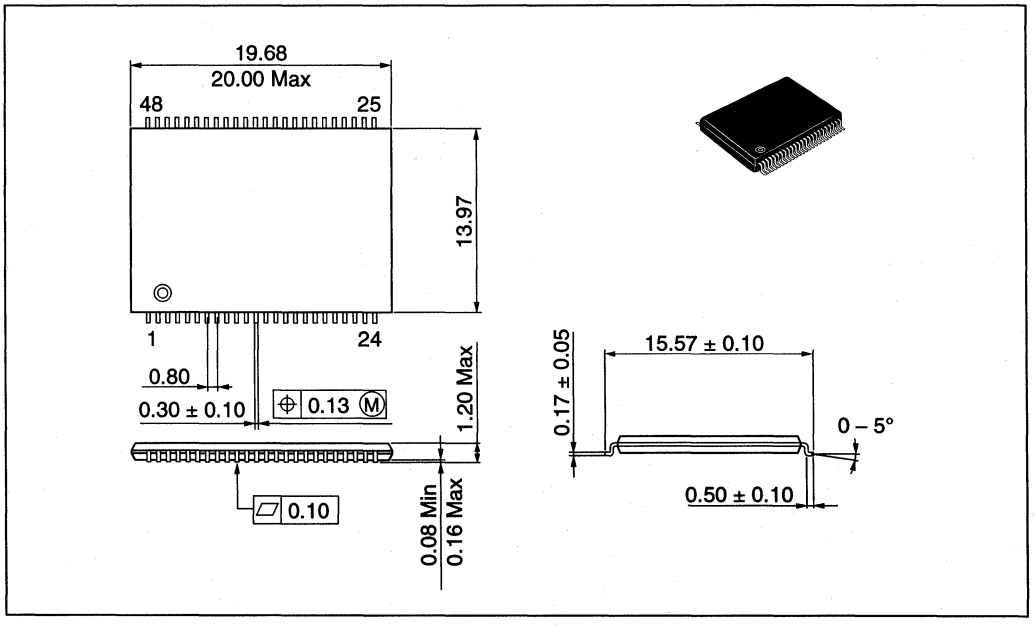


Package Dimensions (cont)

HN624316FB Series (FP-44D) **Unit : mm**



HN624316TA Series (TTP-48D) **Unit : mm**



HN624316N Series

1,048,576-word × 16-bit / 2,097,152–word × 8-bit CMOS Programmable Mask ROM

HITACHI

The HN624316N is a 16-Mbit CMOS Programmable Mask ROM organized either as 1,048,576 words by 16 bits or as 2,097,152 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 120/150 ns is the most suitable to the system using a high speed microcomputer by 16 bits as 8,086 and 68,000, etc.

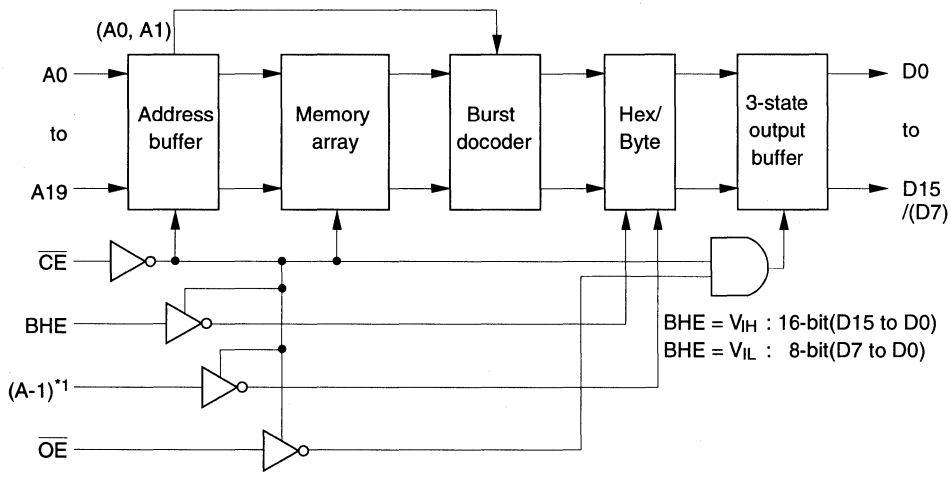
Features

- Single +5 V power supply
- Normal access time: 120 ns/150 ns (max)
- Burst access time: 60 ns/70 ns (max)
- Low power consumption: 300 mW (typ) active
  5 μW (typ) standby
- Byte-wide or word-wide data organization with BHE

Ordering Information

Type No.	Access time	Package
HN624316NP-12	120 ns	600 mil 42-pin plastic DIP (DP-42)
HN624316NP-15	150 ns	
HN624316NFB-12	120 ns	44-pin plastic SOP (FP-44D)
HN624316NFB-15	150 ns	
HN624316NTA-12	120 ns	48-pin plastic TSOP-II (TTP-48D)
HN624316NTA-15	150 ns	

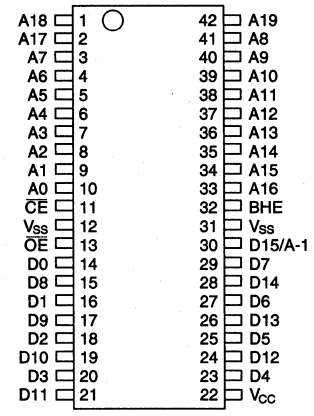
Block Diagram



Note: 1. A-1 is least significant address. When BHE is 'low', D14 to D8 goes the high impedance state.

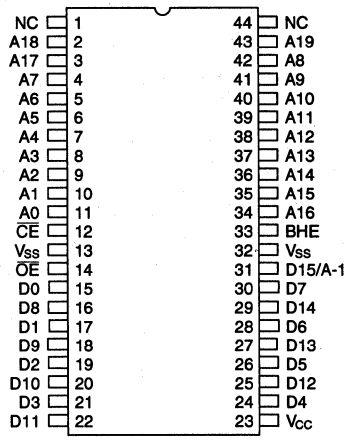
Pin Arrangement

HN624316NP



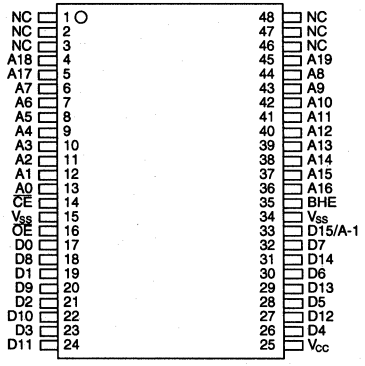
(Top view)

HN624316NFB



(Top view)

HN624316NTA



(Top view)

Absolute Maximum Ratings

Item	Symbol	Value	Unit	Note
Supply voltage	V_{CC}	–0.3 to +7.0	V	1
All input and output voltage	Vin, Vout	–0.3 to V_{CC} + 0.3	V	1
Operating temperature range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (V_{SS} = 0 V, Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70 °C)

Item		Symbol	Min	Max	Unit	Test conditions
Supply current	Active	I_{CC}	—	120/ 110	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = 120 ns/150 ns
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC} - 0.2$ V
	Standby	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\lvert I_{IL} \rvert$	—	10	µA	V_{IN} = 0 to V_{CC}
Output leakage current		$\lvert I_{OL} \rvert$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = –205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 25°C, V_{IN} = 0 V, f = 1 MHz)

Item	Symbol	Min	Max	Unit
Input capacitance	Cin	—	15	pF
Output capacitance	Cout	—	15	pF

Note: This parameter is sampled and not 100% tested.

AC Electrical Characteristics (V_{CC} = 5 V ± 10%, V_{SS} = 0 V, Ta = 0 to +70°C)

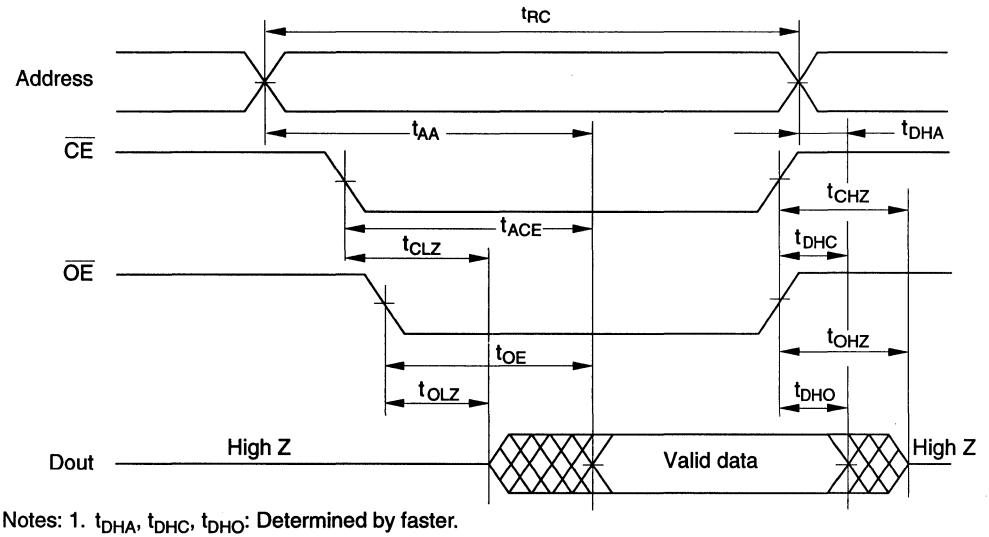
- Output load: 1TTLgate + C_L = 100 pF (including jig capacitance)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 5 ns

		HN624316N-12		HN624316N-15		
Item	Symbol	Min	Max	Min	Max	Unit
Read cycle time	t_{RC}	120	—	150	—	ns
Burst read cycle time	t_{BC}	60	—	70	—	ns
Address access time	t_{AA}	—	120	—	150	ns
Burst address access time	t_{BA}	—	55	—	70	ns
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns
$\overline{OE}$ access time	t_{OE}	—	55	—	70	ns
BHE access time	t_{BHE}	—	120	—	150	ns
Output hold time from address change	t_{DHA}	0	—	0	—	ns
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns
Output hold time from BHE	t_{DHB}	0	—	0	—	ns
$\overline{CE}$ to output in high Z	t_{CHZ}*1	—	40	—	70	ns
$\overline{OE}$ to output in high Z	t_{OHZ}*1	—	40	—	70	ns
BHE to output in high Z	t_{BHZ}*1	—	40	—	70	ns
$\overline{CE}$ to output in low Z	t_{CLZ}	5	—	5	—	ns
$\overline{OE}$ to output in low Z	t_{OLZ}	5	—	5	—	ns
BHE to output in low Z	t_{BLZ}	5	—	5	—	ns

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

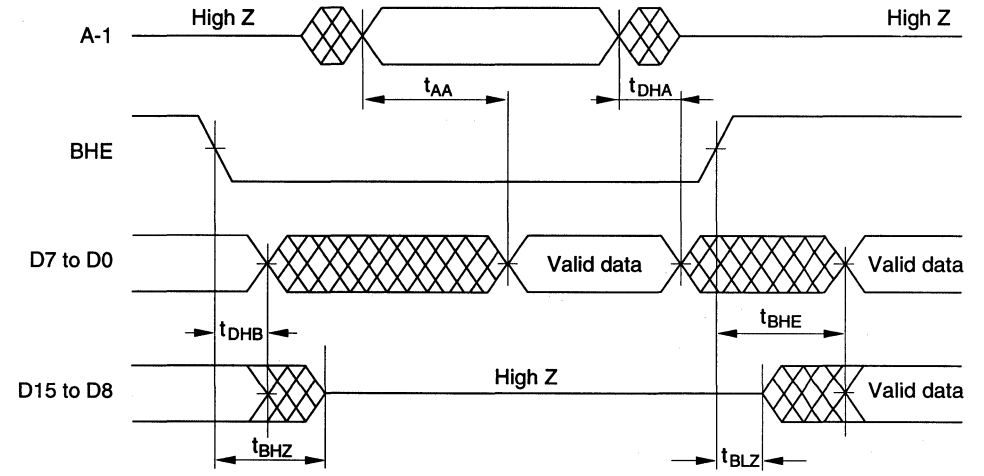
Timing Diagram

(1) Word mode (BHE = 'V_{IH}') or Byte mode (BHE = 'V_{IL}')



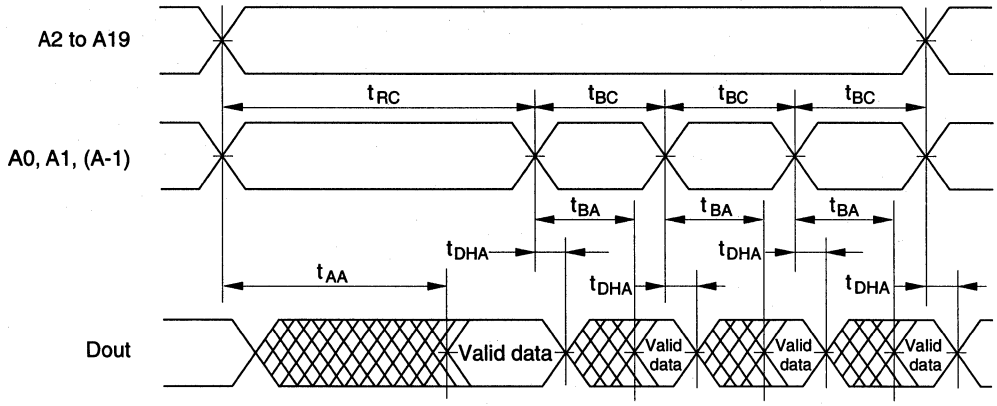
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

(2) Word mode, Byte mode switch



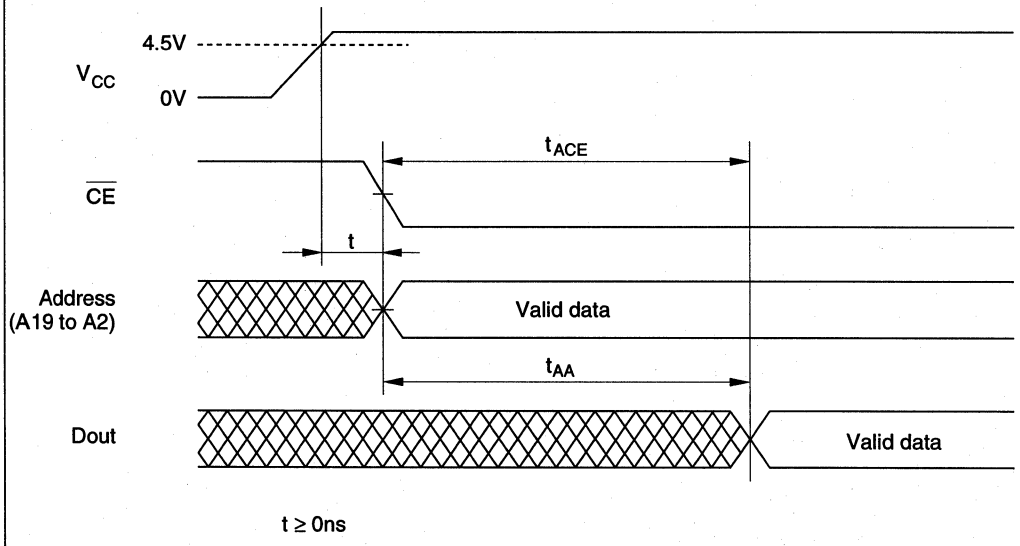
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable A19 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable. Therefore, the input signals of opposite phase to the output must not be applied to them.

(3) Burst mode



Note: $\overline{CE}$ and $\overline{OE}$ are enable.

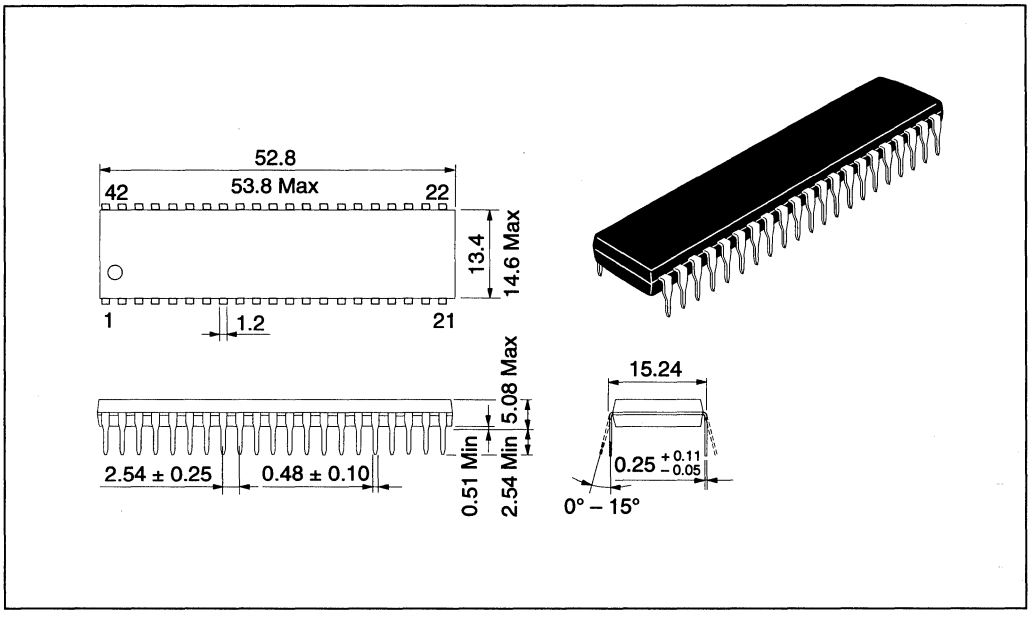
Power Up Sequence



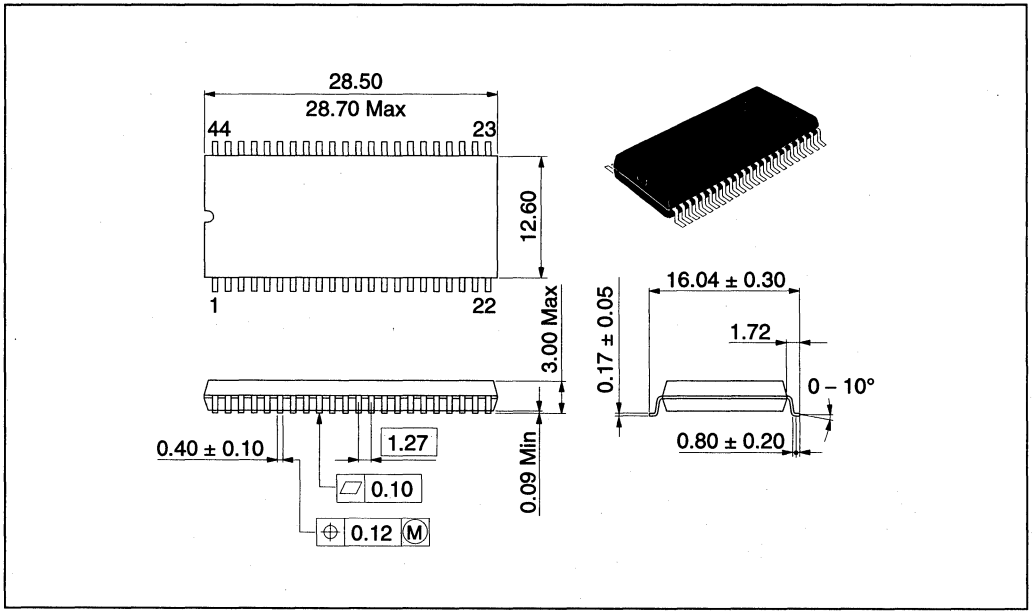
Note: This device is used ATD (Address Transient Detector). Therefore, Transfer either $\overline{CE}$ or address

Package Dimensions

HN624316NP Series (DP-42) **Unit : mm**

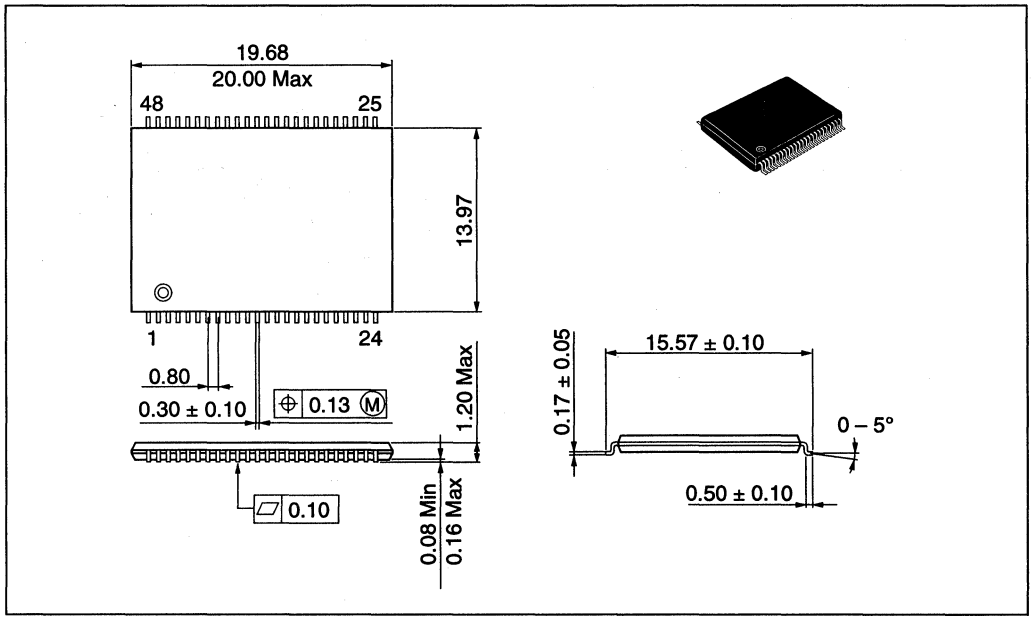


HN624316NFB Series (FP-44D) **Unit : mm**



Package Dimensions (cont)

HN624316NTA Series (TTP-48D) **Unit : mm**



HN624416 Series

1,048,576-word × 16-bit / 2,097,152-word × 8-bit CMOS Programmable Mask ROM

HITACHI

Preliminary
Rev. 0.0
November 20, 1995

The HN624416 is a 16-Mbit CMOS Programmable Mask ROM organized either as 1,048,576 words by 16 bits or 2,097,152 words by 8 bits.

Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 100/120 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Features

- Single 5 V supply
- High speed
  Access time: 100/120 ns (max)
- Low power
  Active: 660 mW (max)
  Standby: 165 μW (max)
- Byte-wide or word-wide data organization
  (Switched by BHE terminal)
- Three-state data output for or-tying
- Directly TTL compatible
  All inputs and outputs
- Pin compatible with 8 Mbit Mask ROM
  (HN62448)

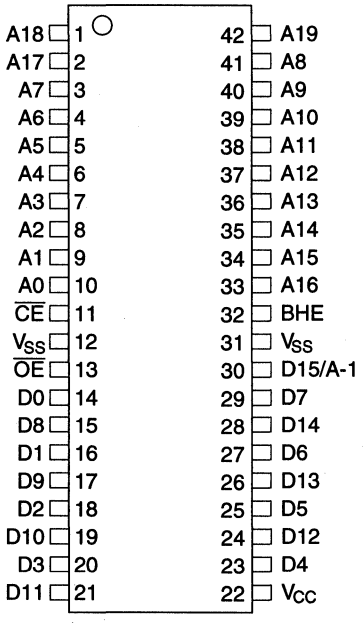
Ordering Information

Type No.	Access time	Package
HN624416P-10 HN624416P-12	100 ns 120 ns	600 mil 42-pin plastic DIP (DP-42)
HN624416FB-10 HN624416FB-12	100 ns 120 ns	600 mil 44-pin plastic SOP (FP-44D)
HN624416TT-10 HN624416TT-12	100 ns 120 ns	400 mil 44-pin plastic TSOP II (TTP-44D)

Preliminary: This document contains information on a new product. Specifiactions and information contained herein are subject to change without notice.

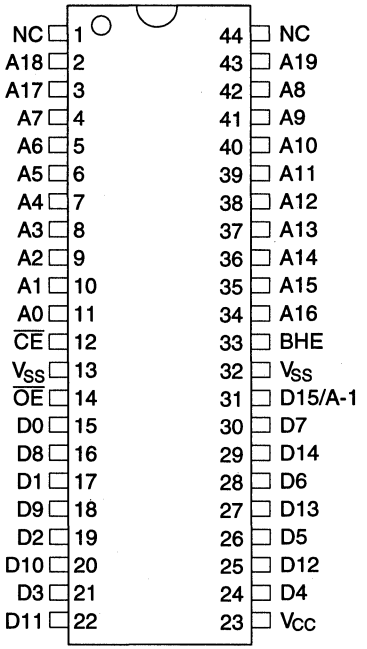
Pin Arrangement

HN624416P Series



(Top View)

HN624416FB Series
HN624416TT Series

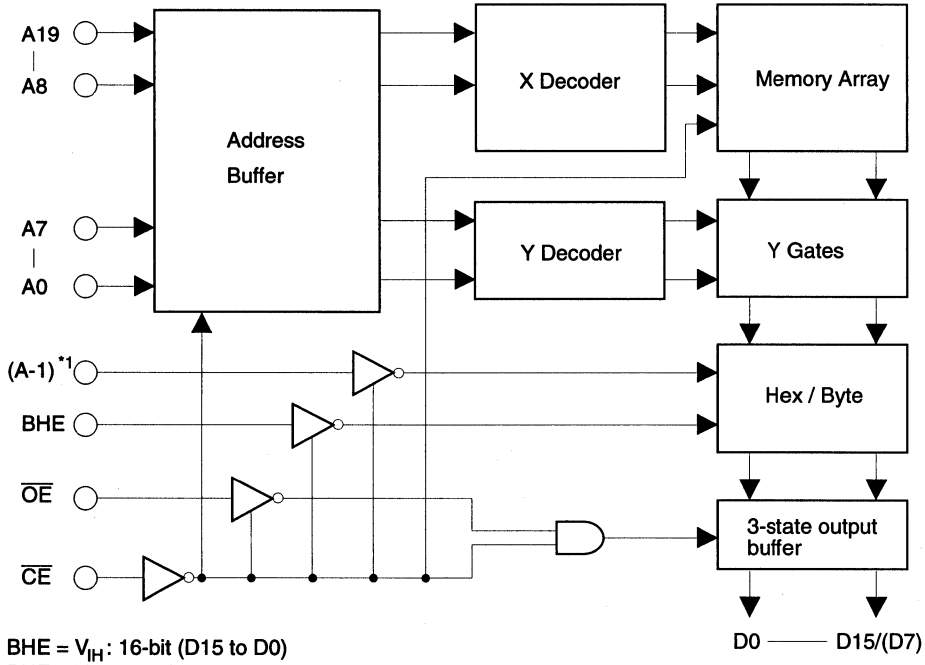


(Top View)

Pin Description

Symbol	Function
A-1, A0 to A19	Address inputs
D0 to D15	Data outputs
BHE	8/16 bit (byte/word) mode switch
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



BHE = V_{IH}: 16-bit (D15 to D0)
BHE = V_{IL} : 8-bit (D7 to D0)

Note: 1. A-1 is least significant address.

When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.

Mode Selection

	Pin							
					Data output		Address input	
Mode	$\overline{CE}$	$\overline{OE}$	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	×*1	×	×	High-Z*2	High-Z	—	—
Output disable	L	H	×	×	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A19
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A19
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A19

Notes: 1. ×: Don't care.
2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{CC}	− 0.3 to + 7.0	V
All input and output voltage*1	Vin, Vout	− 0.3 to V_{CC} + 0.3	V
Operating temperature range	Topr	0 to + 70	°C
Storage temperature range	Tstg	− 55 to + 125	°C
Temperature under bias	Tbias	− 20 to + 85	°C

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	− 0.3	—	0.8	V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

Parameter		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{CC}	—	120/100	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = 100/120 ns
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ - 0.2 V
	Standby	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = – 205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

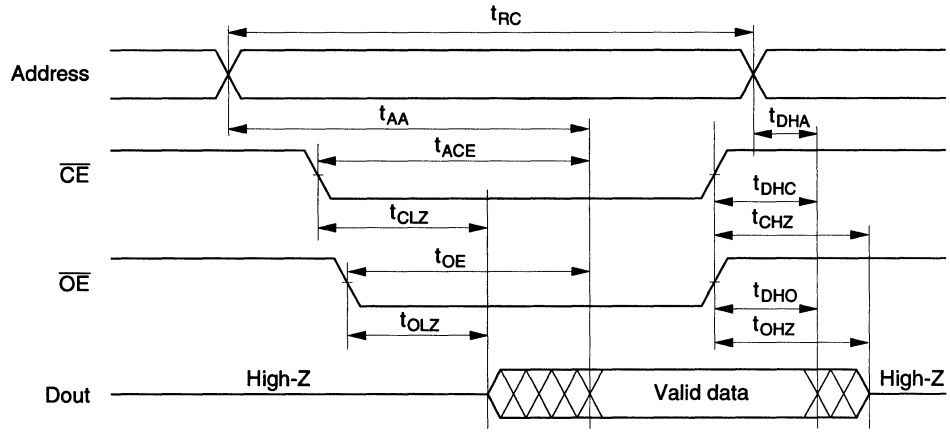
- Output load: 1TTL + C_L = 100 pF (including jig)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 5ns

		HN624416-10		HN624416-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	100	—	120	—	ns	
Address access time	t_{AA}	—	100	—	120	ns	
$\overline{CE}$ access time	t_{ACE}	—	100	—	120	ns	
$\overline{OE}$ access time	t_{OE}	—	40	—	50	ns	
BHE access time	t_{BHE}	—	100	—	120	ns	
Output hold time from address change	t_{DHA}	5	—	5	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	30	—	30	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	30	—	30	ns	1
BHE to output in high-Z	t_{BHZ}	—	30	—	30	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns	

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

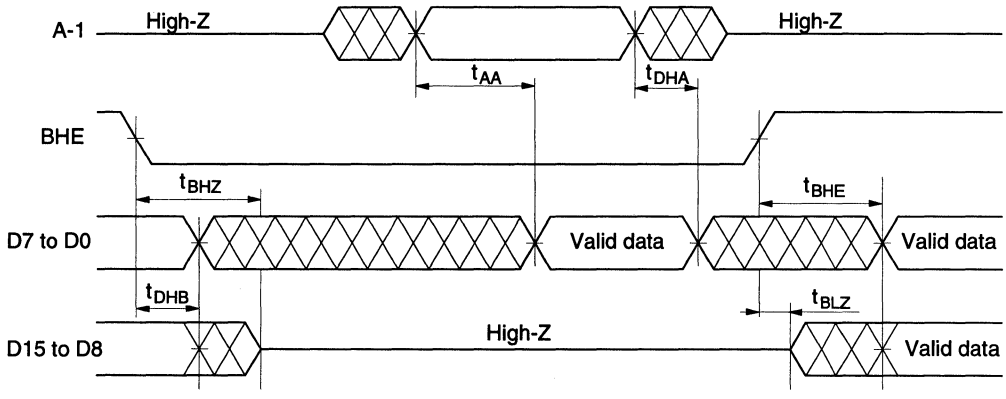
Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



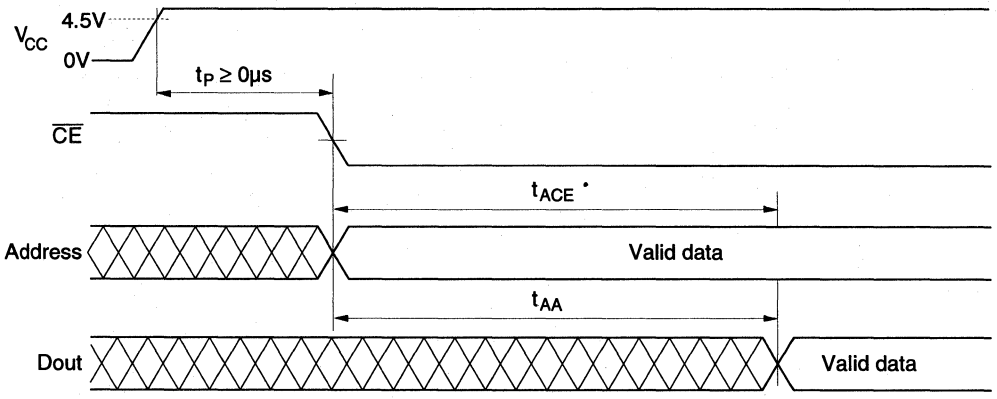
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Word Mode, Byte Mode Switch



Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable, A19 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

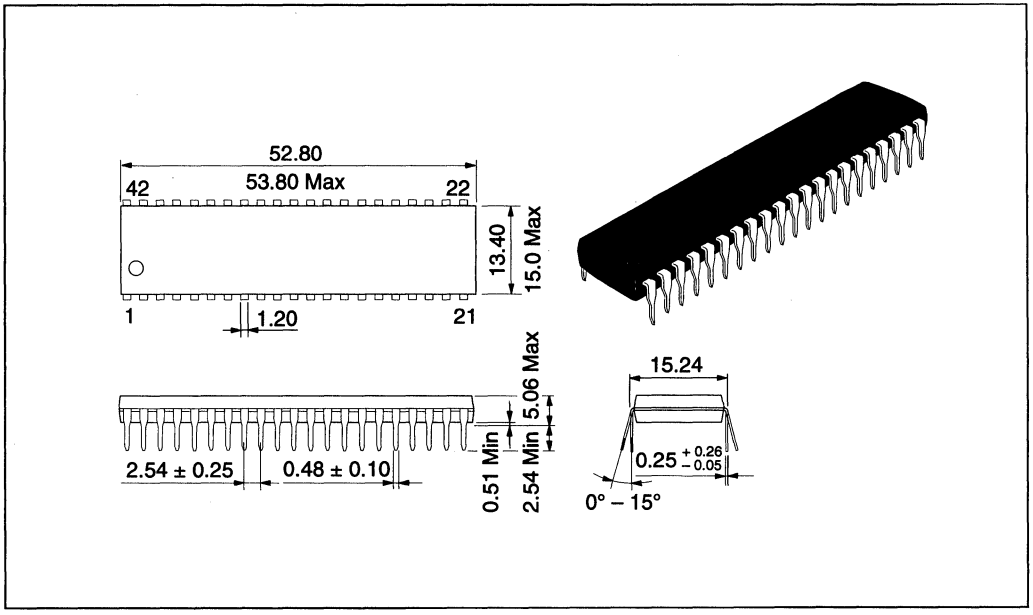
Power Up Sequence



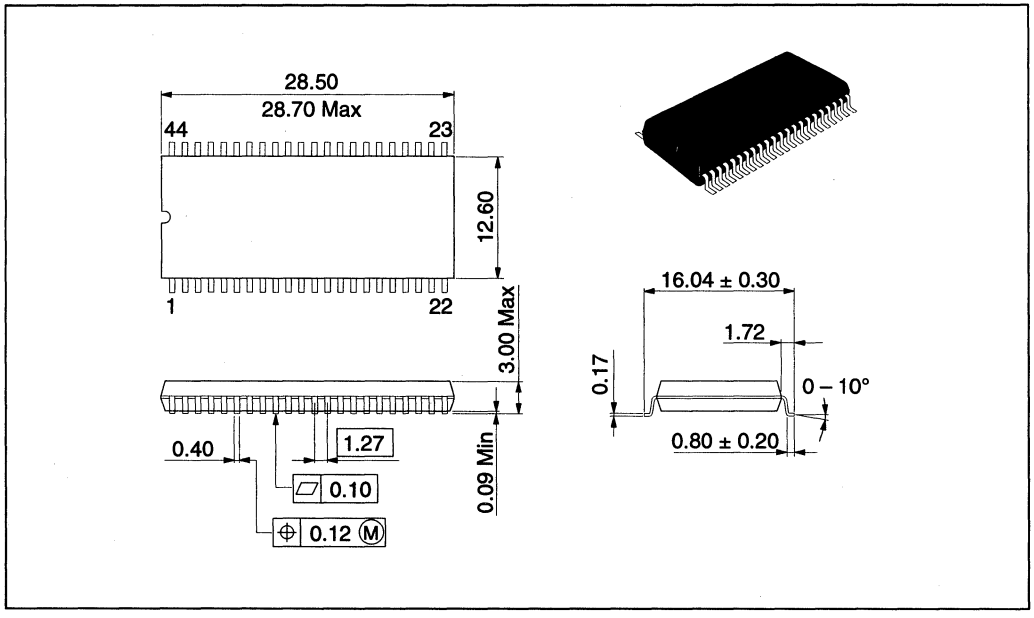
Notes: 1. This device is used ATD (Address Transition Detecter). Therefore, transfer either $\overline{CE}$ or address (A19 to A0) after power up to 4.5V.

Package Dimensions

HN624416P Series (DP-42) **Unit: mm**

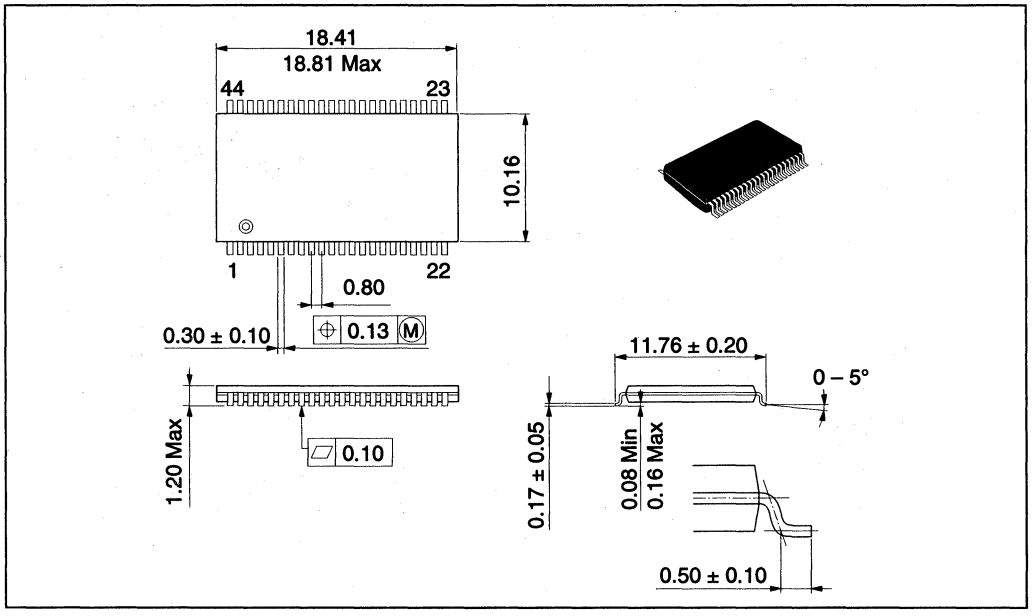


HN624416FB Series (FP-44D) **Unit: mm**



Package Dimensions (cont)

HN624416TT Series (TTP-44D) **Unit: mm**



HN624416N Series

1,048,576-word × 16-bit / 2,097,152-word × 8-bit CMOS Programmable Mask ROM

HITACHI

Preliminary
Rev. 0.0
October 18, 1995

The HN624416N is a 16-Mbit CMOS Programmable Mask ROM organized either as 1,048,576 words by 16 bits or 2,097,152 words by 8 bits.

Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 100/120 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Features

- Single 5 V supply
- High speed
  Normal access time: 100/120 ns (max)
  Page access time: 40/50 ns (max)
- Low power
  Active: 770 mW (max)
  Standby: 165 µW (max)
- Byte-wide or word-wide data organization
  (Switched by BHE terminal)
- 4 word page access on word-wide mode
- 8 byte page access on byte-wide mode
- Three-state data output for or-tying
- Directly TTL compatible
  All inputs and outputs
- Pin compatible with 8 Mbit Mask ROM
  (HN62448)

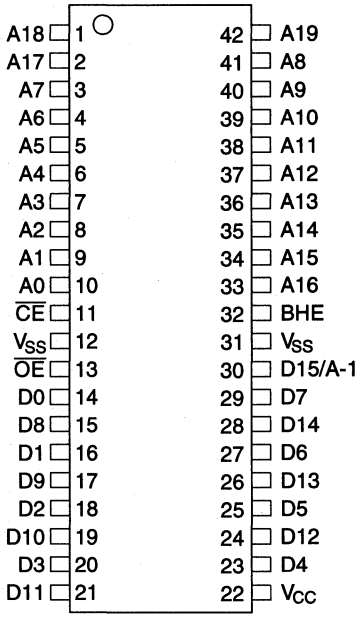
Ordering Information

Type No.	Access time	Package
HN624416NP-10 HN624416NP-12	100 ns 120 ns	600 mil 42-pin plastic DIP (DP-42)
HN624416NFB-10 HN624416NFB-12	100 ns 120 ns	600 mil 44-pin plastic SOP (FP-44D)
HN624416NTT-10 HN624416NTT-12	100 ns 120 ns	400 mil 44-pin plastic TSOP II (TTP-44D)

Preliminary: This document contains information on a new product. Specifiactions and information contained herein are subject to change without notice.

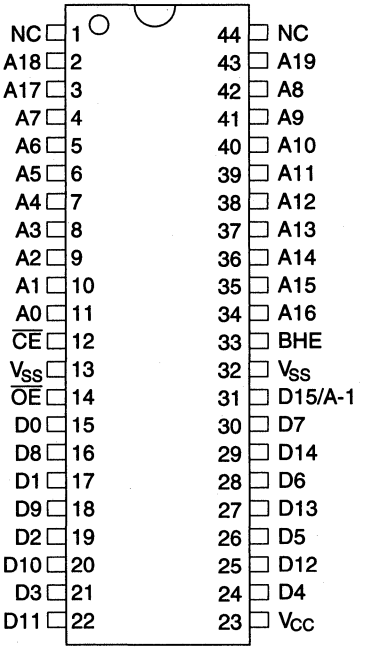
Pin Arrangement

HN624416NPSeries



(Top View)

HN624416NFB Series
HN624416NTT Series

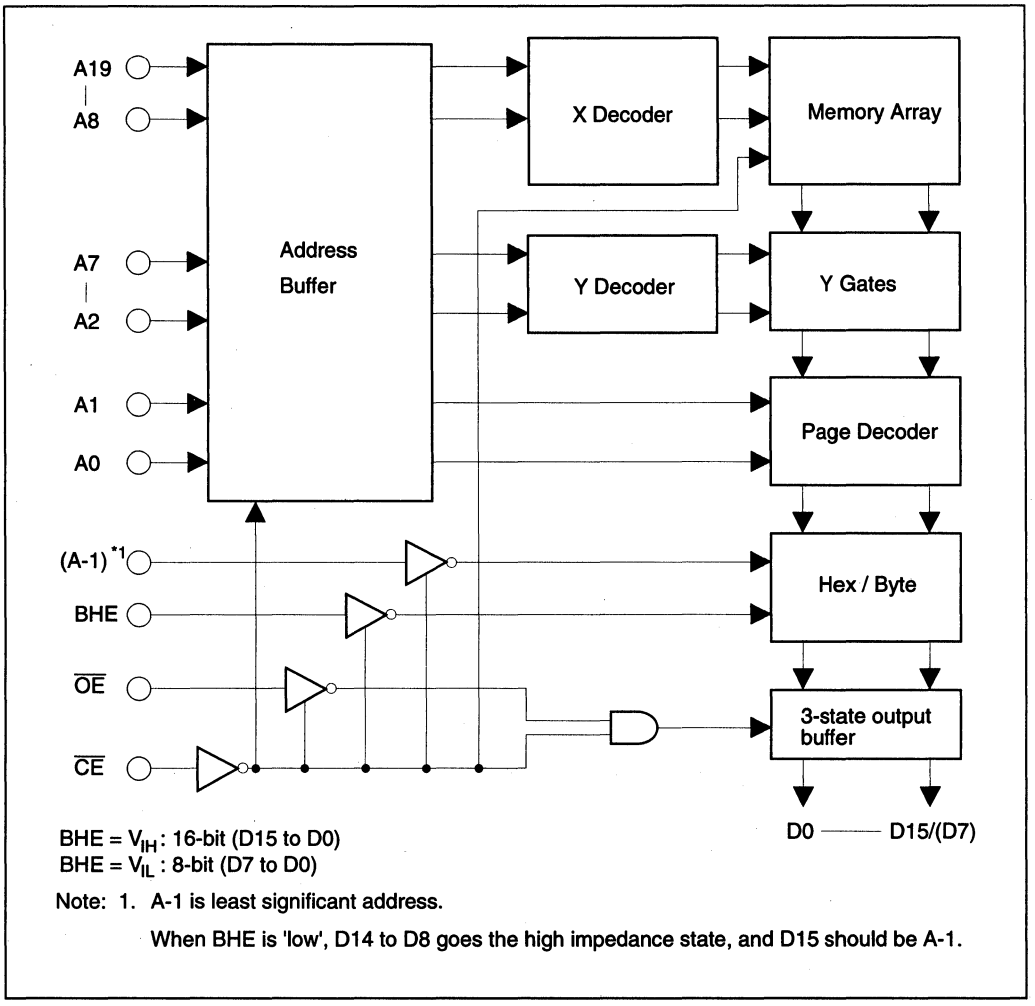


(Top View)

Pin Description

Symbol	Function
A2 to A19	Address inputs
D0 to D15	Data outputs
A-1, A0, A1	Page address inputs
BHE	8/16 bit (byte/word) mode switch
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
NC	No connection
V_{CC}	Power supply
V_{SS}	Ground

Block Diagram



BHE = V_{IH} : 16-bit (D15 to D0)
BHE = V_{IL} : 8-bit (D7 to D0)

Note: 1. A-1 is least significant address.

When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.

Mode Selection

	Pin							
					Data output		Address input	
Mode	$\overline{CE}$	$\overline{OE}$	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	×*1	×	×	High-Z*2	High-Z	—	—
Output disable	L	H	×	×	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A19
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A19
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A19

Notes: 1. ×: Don't care.
2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{CC}	− 0.3 to + 7.0	V
All input and output voltage*1	Vin, Vout	− 0.3 to V_{CC} + 0.3	V
Operating temperature range	Topr	0 to + 70	°C
Storage temperature range	Tstg	− 55 to + 125	°C
Temperature under bias	Tbias	− 20 to + 85	°C

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
	V_{IL}	− 0.3	—	0.8	V

DC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

Parameter		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{CC}	—	140/120	mA	V_{CC} = 5.5 V, I_{DOUT} = 0 mA, t_{RC} = 100/120 ns
	Standby	I_{SB1}	—	30	µA	V_{CC} = 5.5 V, $\overline{CE} \geq V_{CC}$ - 0.2 V
	Standby	I_{SB2}	—	3	mA	V_{CC} = 5.5 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{CC}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{CC}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = – 205 µA
		V_{OL}	—	0.4	V	I_{OL} = 1.6 mA

Capacitance (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics (V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = 0 to + 70°C)

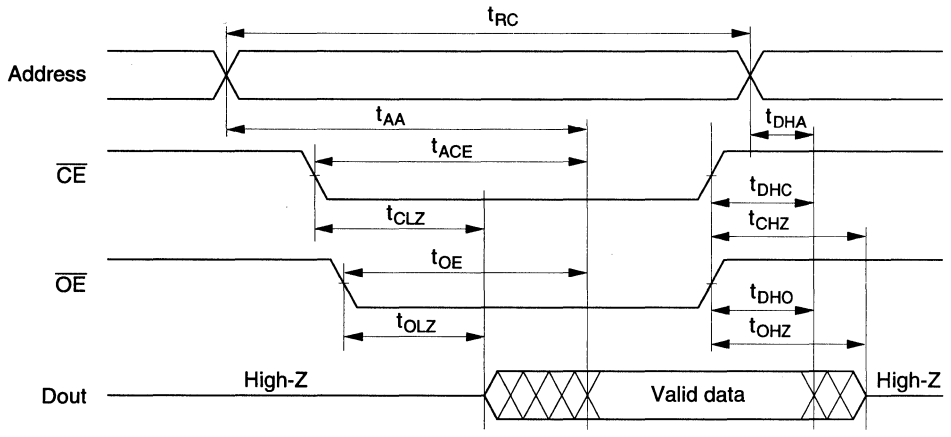
- Output load: 1TTL + C_L = 100 pF (including jig)
- Input pulse level: 0.45 to 2.4 V
- Input and output timing reference level: 1.5 V
- Input rise and fall time: 5ns

		HN624416N-10		HN624416N-12			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	100	—	120	—	ns	
Page read cycle time	t_{PC}	40	—	50	—	ns	
Address access time	t_{AA}	—	100	—	120	ns	
Page address access time	t_{PA}	—	40	—	50	ns	
$\overline{CE}$ access time	t_{ACE}	—	100	—	120	ns	
$\overline{OE}$ access time	t_{OE}	—	40	—	50	ns	
BHE access time	t_{BHE}	—	100	—	120	ns	
Output hold time from address change	t_{DHA}	5	—	5	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	30	—	30	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	30	—	30	ns	1
BHE to output in high-Z	t_{BHZ}	—	30	—	30	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	5	—	ns	

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

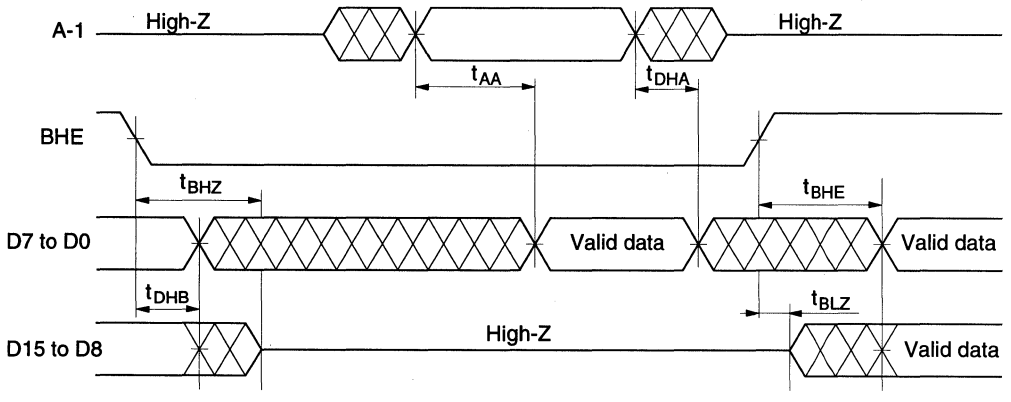
Timing Waveforms

Word mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



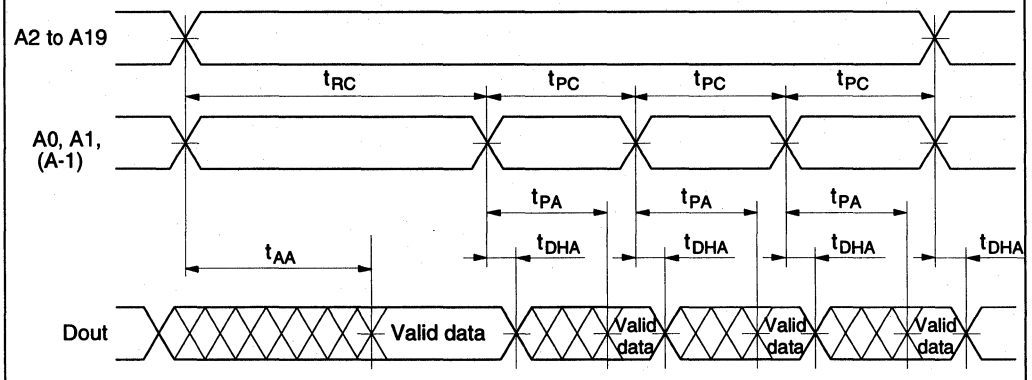
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Word Mode, Byte Mode Switch



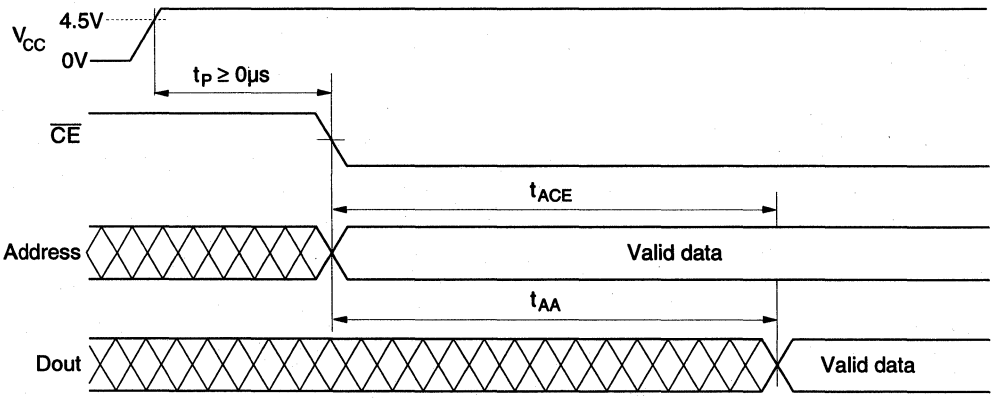
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable, A19 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

Page mode



Notes: 1. Page address is determined as below.
Word mode (BHE = 'High'): A0, A1
Byte mode (BHE = 'Low'): A-1, A0, A1
2. $\overline{CE}$ and $\overline{OE}$ are enable.

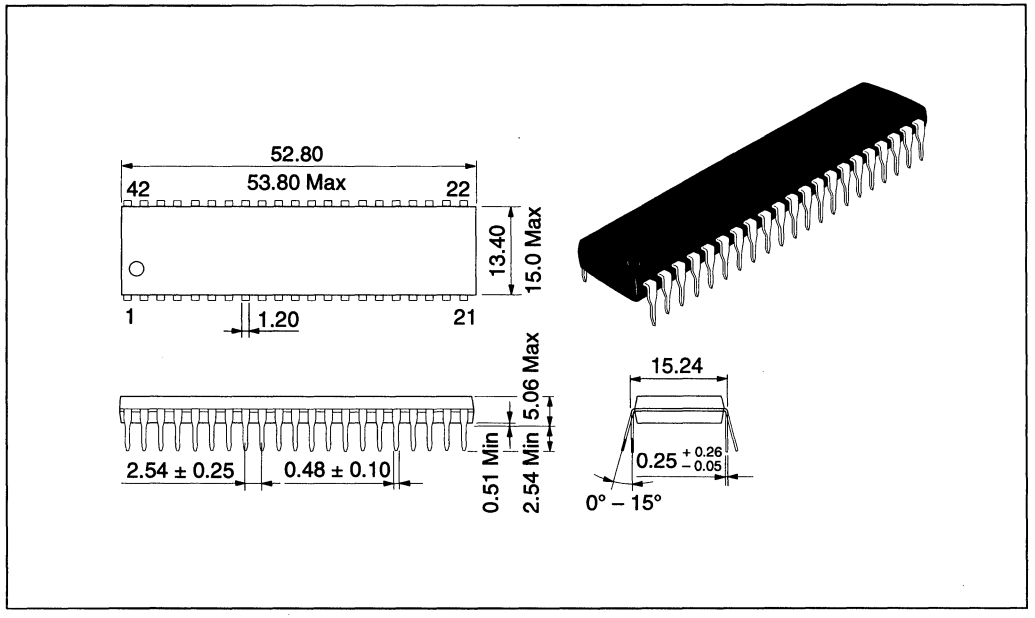
Power up sequence



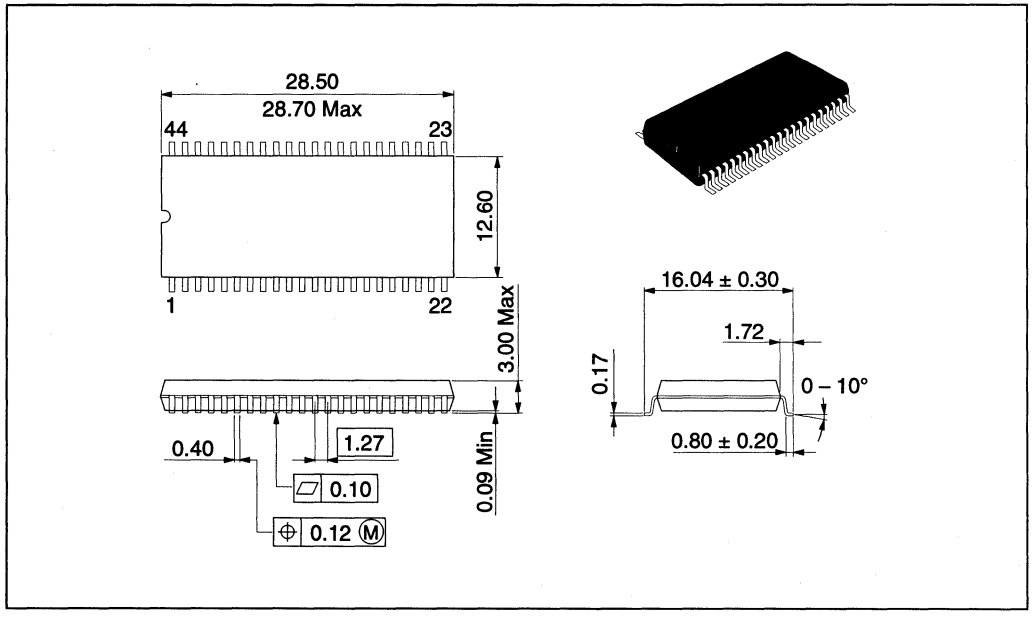
Notes: 1. This device is used ATD (Address Transition Detecter). Therefore, transfer either $\overline{CE}$ or address (A19 to A2) after power up to 4.5V.

Package Dimensions

HN624416NP Series (DP-42) **Unit: mm**

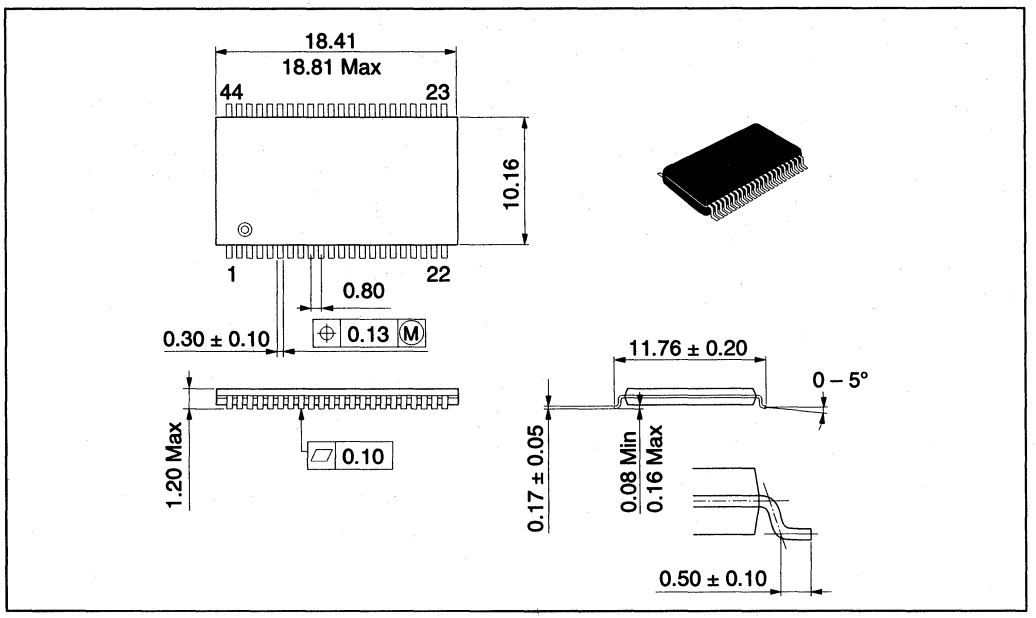


HN624416NFB Series (FP-44D) **Unit: mm**



Package Dimensions (cont)

HN624416NTT Series (TTP-44D) **Unit: mm**



HN62W4416 Series

1,048,576-word × 16-bit / 2,097,152-word × 8-bit CMOS Programmable Mask ROM

HITACHI

Preliminary
Rev. 0.0
November 20, 1995

The HN62W4416 is a 16-Mbit CMOS Programmable Mask ROM organized either as 1,048,576 words by 16 bits or 2,097,152 words by 8 bits.

Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 150 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Features

- Low voltage operation Mask ROM
  Single 3.3 V supply
- High speed
  Access time: 150 ns (max)
- Low power
  Active: 216 mW (max)
  Standby: 108 µW (max)
- Byte-wide or word-wide data organization
  (Switched by BHE terminal)
- Three-state data output for or-tying
- Directly LV-TTL compatible
  All inputs and outputs

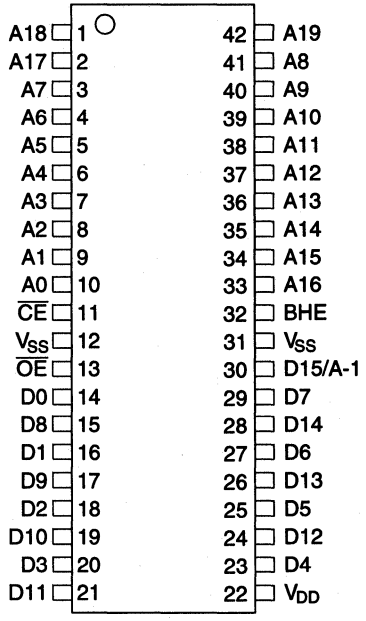
Ordering Information

Type No.	Access time	Package
HN62W4416P-15	150 ns	600 mil 42-pin plastic DIP (DP-42)
HN62W4416FB-15	150 ns	600 mil 44-pin plastic SOP (FP-44D)
HN62W4416TT-15	150 ns	400 mil 44-pin plastic TSOP II (TTP-44D)

Preliminary: This document contains information on a new product. Specifiactions and information contained herein are subject to change without notice.

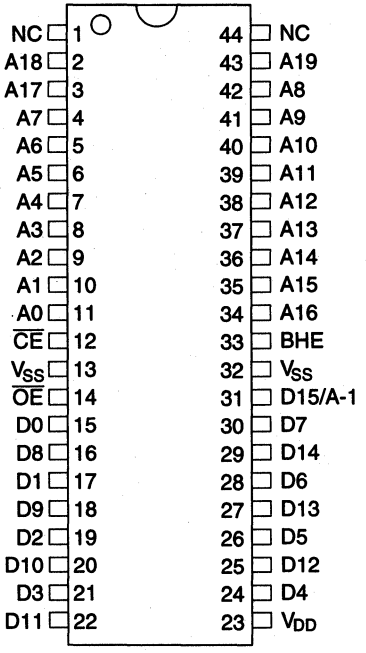
Pin Arrangement

HN62W4416P Series



(Top View)

HN62W4416FB Series
HN62W4416TT Series

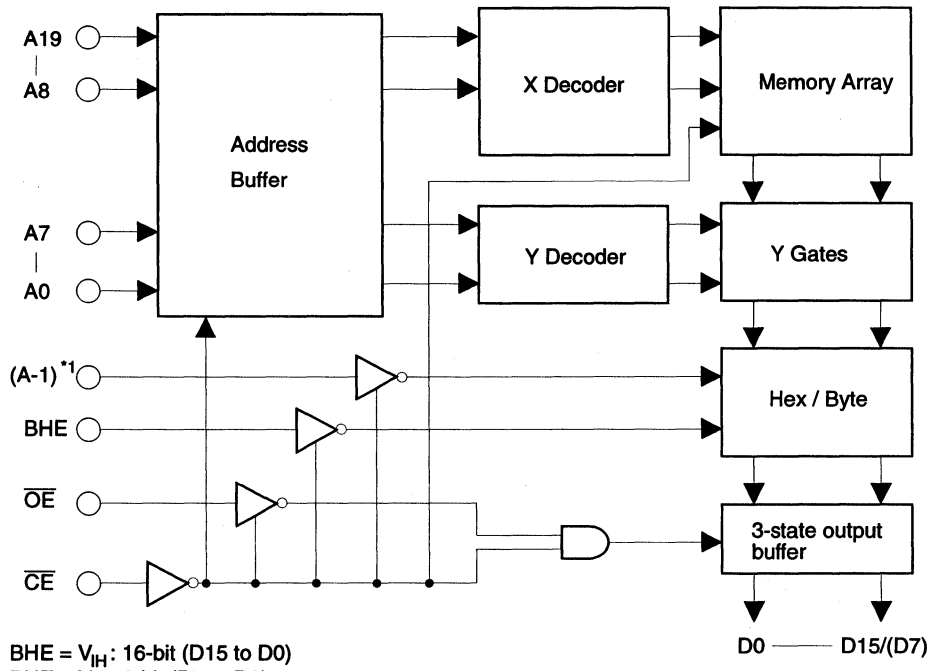


(Top View)

Pin Description

Symbol	Function
A-1, A0 to A19	Address inputs
D0 to D15	Data outputs
BHE	8/16 bit (byte/word) mode switch
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
NC	No connection
V_{DD}	Power supply
V_{SS}	Ground

Block Diagram



BHE = V_{IH} : 16-bit (D15 to D0)
BHE = V_{IL} : 8-bit (D7 to D0)

Note: 1. A-1 is least significant address.
When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.

Mode Selection

	Pin							
					Data output		Address input	
Mode	$\overline{CE}$	$\overline{OE}$	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	×*1	×	×	High-Z*2	High-Z	—	—
Output disable	L	H	×	×	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A19
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A19
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A19

Notes: 1. ×: Don't care.
2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{DD}	− 0.3 to + 5.5	V
All input and output voltage*1	Vin, Vout	− 0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr	0 to + 70	°C
Storage temperature range	Tstg	− 55 to + 125	°C
Temperature under bias	Tbias	− 20 to + 85	°C

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{DD} + 0.3	V
	V_{IL}	− 0.3	—	0.8	V

DC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to + 70°C)

Parameter		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{DD}	—	60	mA	V_{DD} = 3.6 V, I_{DOUT} = 0 mA, t_{RC} = 150 ns
	Standby	I_{SB1}	—	30	µA	V_{DD} = 3.6 V, $\overline{CE} \geq V_{DD}$ - 0.2 V
	Standby	I_{SB2}	—	3	mA	V_{DD} = 3.6 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{DD}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{DD}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = – 2.0 mA
		V_{OL}	—	0.4	V	I_{OL} = 2.0 mA

Capacitance (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to + 70°C)

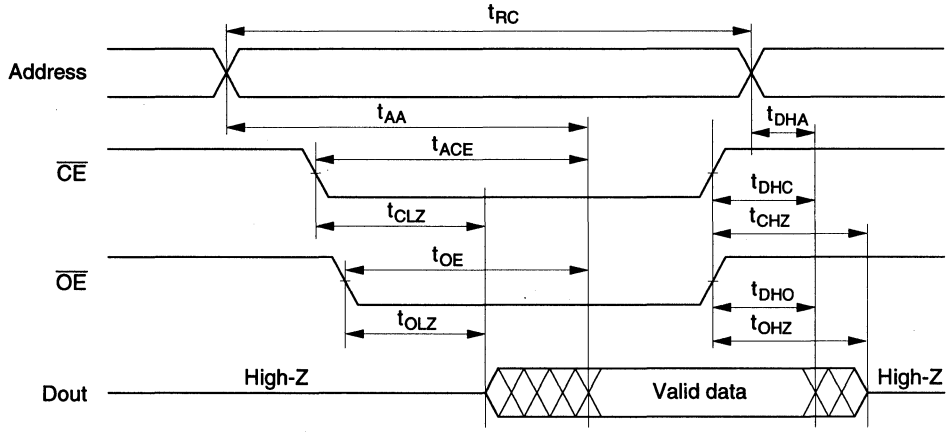
- Output load: 1TTL + C_L = 100 pF (including jig)
- Input pulse level: 0.4 to 2.4 V
- Input and output timing reference level: 1.4 V
- Input rise and fall time: 5ns

		HN62W4416M-15			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	150	—	ns	
Address access time	t_{AA}	—	150	ns	
$\overline{CE}$ access time	t_{ACE}	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	50	ns	
BHE access time	t_{BHE}	—	150	ns	
Output hold time from address change	t_{DHA}	5	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	50	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	50	ns	1
BHE to output in high-Z	t_{BHZ}	—	30	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	ns	

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

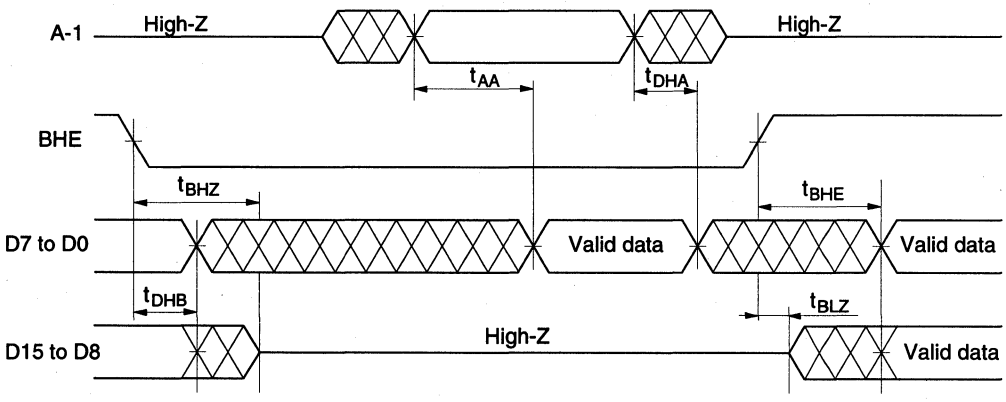
Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



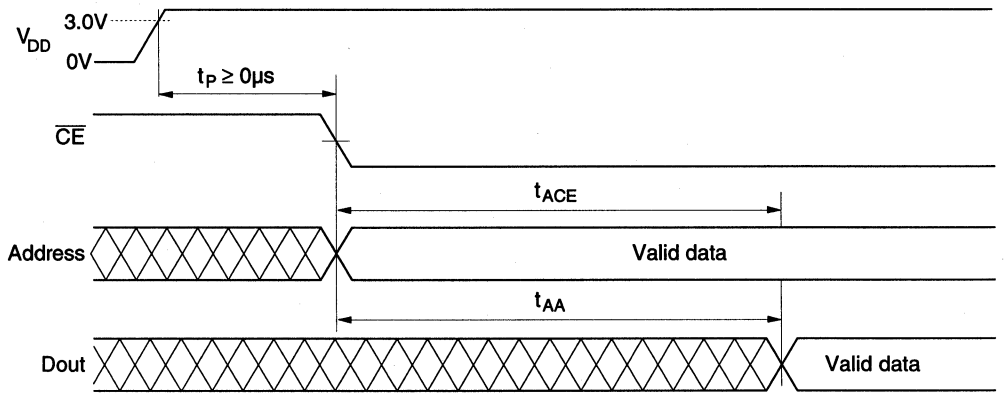
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Word Mode, Byte Mode Switch



Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable, A19 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

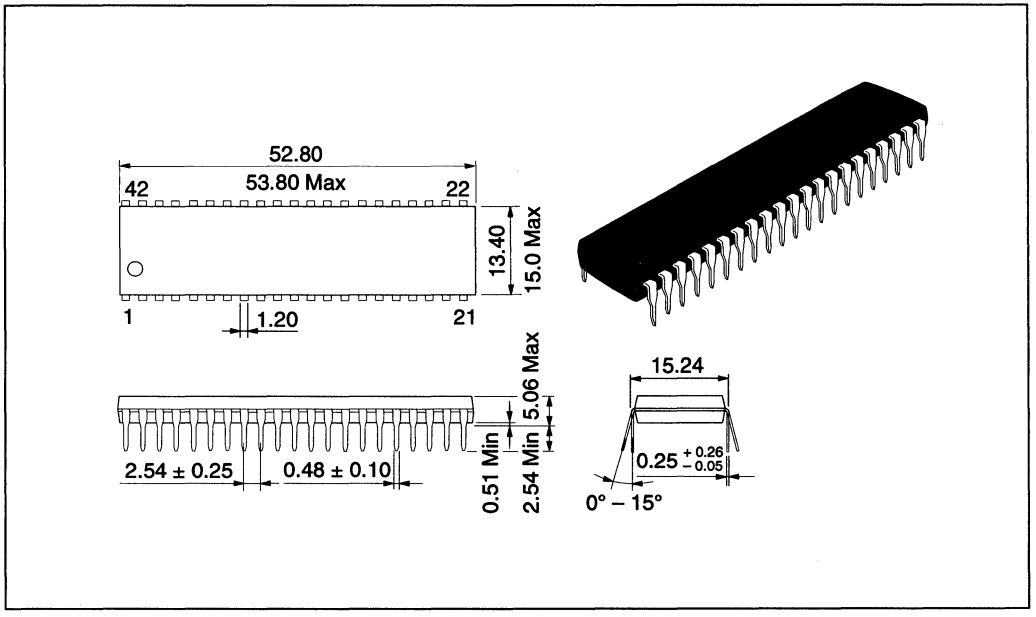
Power Up Sequence



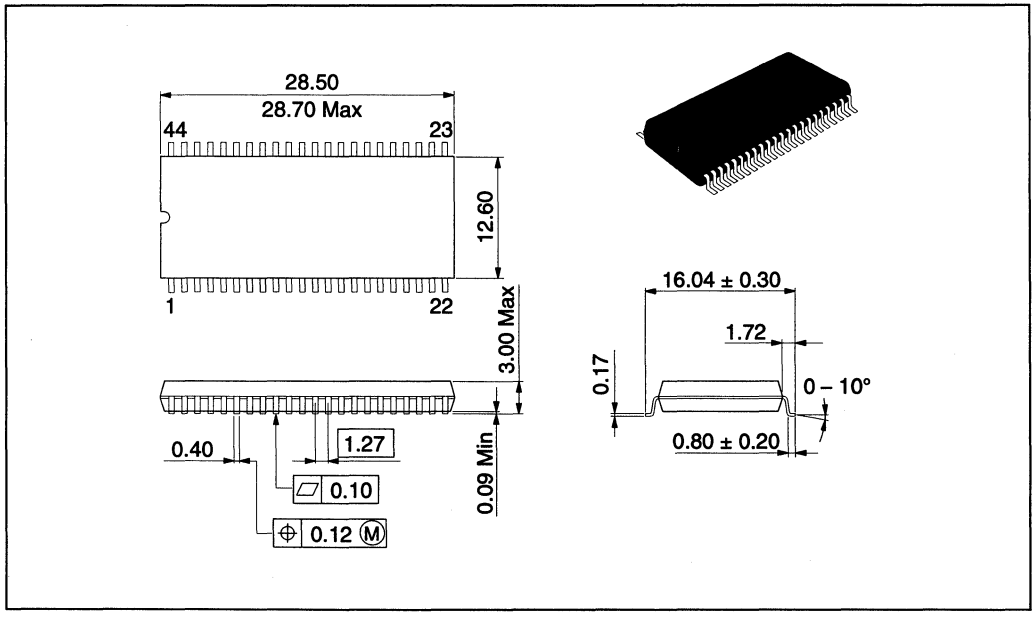
Notes: 1. This device is used ATD (Address Transition Detecter). Therefore, transfer either $\overline{CE}$ or address (A19 to A0) after power up to 3.0V.

Package Dimensions

HN62W4416P Series (DP-42) **Unit: mm**

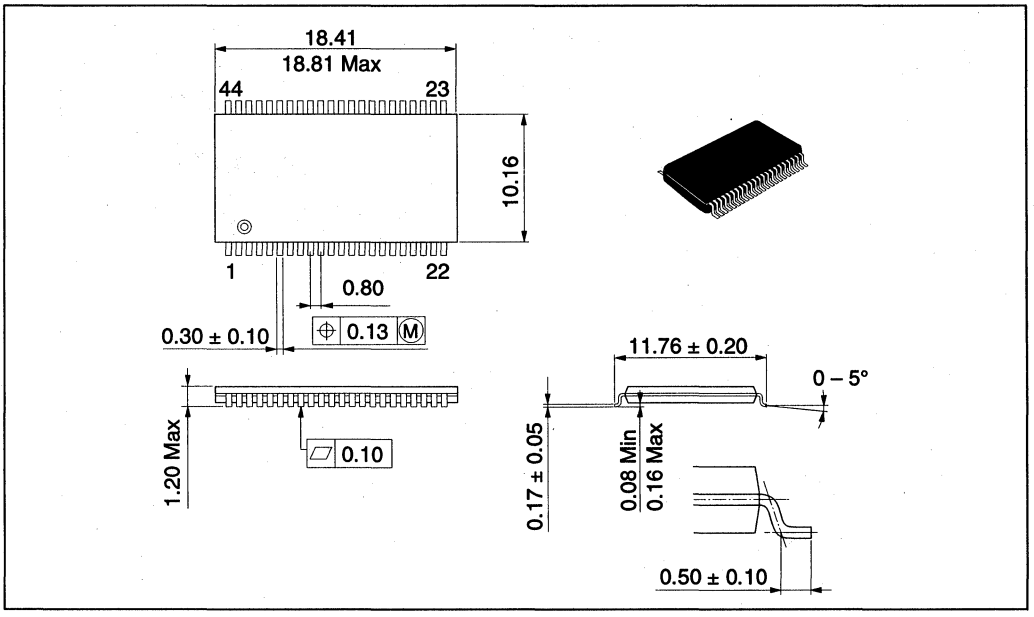


HN62W4416FB Series (FP-44D) **Unit: mm**



Package Dimensions (cont)

HN62W4416TT Series (TTP-44D) **Unit: mm**



HN62W4416N Series

1,048,576-word × 16-bit / 2,097,152-word × 8-bit CMOS Programmable Mask ROM

HITACHI

Preliminary
Rev. 0.0
November 20, 1995

The HN62W4416N is a 16-Mbit CMOS Programmable Mask ROM organized either as 1,048,576 words by 16 bits or 2,097,152 words by 8 bits.

Realizing low power consumption, this memory is allowed for battery operation. And a high speed access of 150 ns (max) is the most suitable to the system using a high speed micro-computer by 16 bits.

Features

- Low voltage operation Mask ROM
  Single 3.3 V supply
- High speed
  Normal access time: 150 ns (max)
  Page access time: 50 ns (max)
- Low power
  Active: 252 mW (max)
  Standby: 108 μW (max)
- Byte-wide or word-wide data organization
  (Switched by BHE terminal)
- 4 word page access on word-wide mode
- 8 byte page access on byte-wide mode
- Three-state data output for or-tying
- Directly LV-TTL compatible
  All inputs and outputs

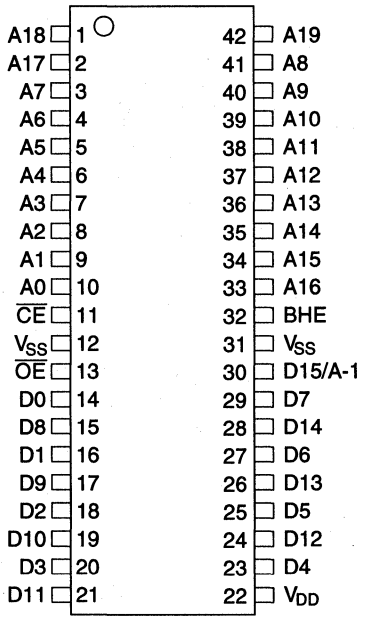
Ordering Information

Type No.	Access time	Package
HN62W4416NP-15	150 ns	600 mil 42-pin plastic DIP (DP-42)
HN62W4416NFB-15	150 ns	600 mil 44-pin plastic SOP (FP-44D)
HN62W4416NTT-15	150 ns	400 mil 44-pin plastic TSOP II (TTP-44D)

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

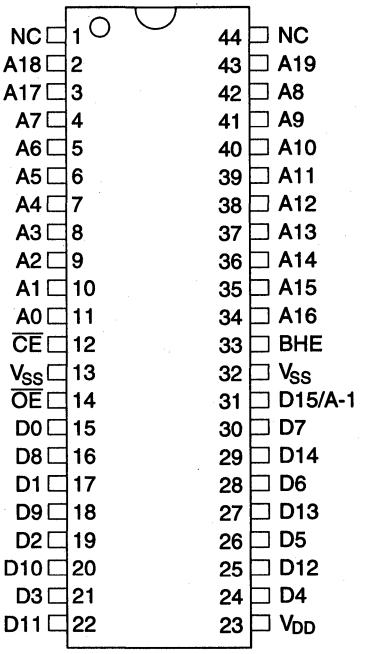
Pin Arrangement

HN62W4416NP Series



(Top View)

HN62W4416NFB Series
HN62W4416NTT Series

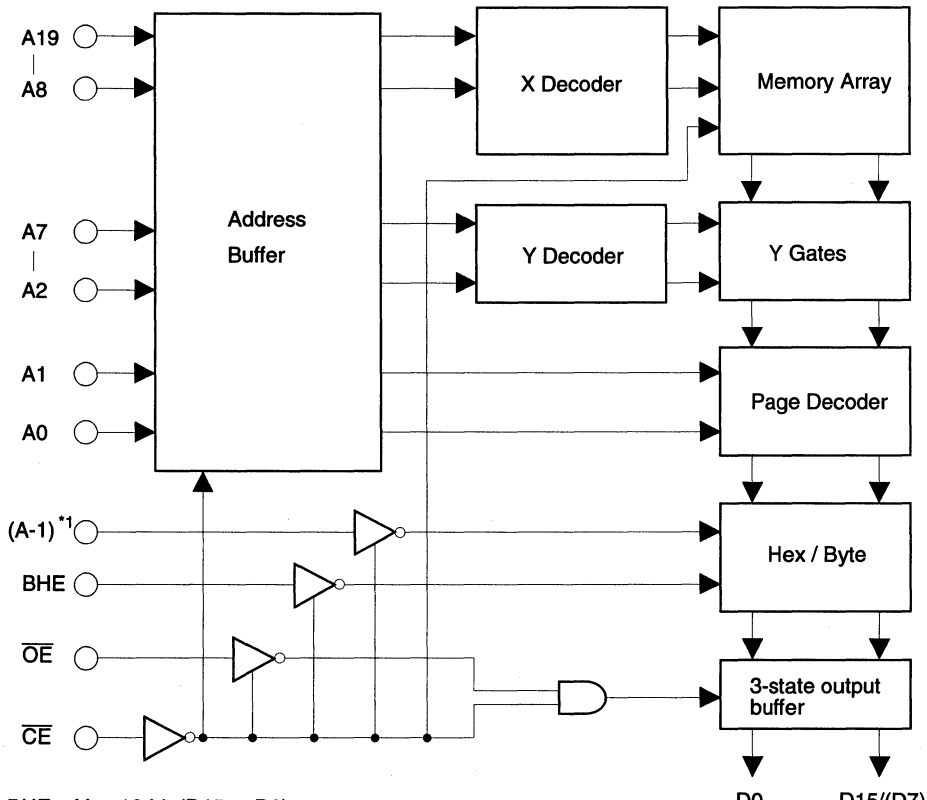


(Top View)

Pin Description

Symbol	Function
A2 to A19	Address inputs
D0 to D15	Data outputs
A-1, A0, A1	Page address inputs
BHE	8/16 bit (byte/word) mode switch
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
NC	No connection
V_{DD}	Power supply
V_{SS}	Ground

Block Diagram



BHE = V_{IH} : 16-bit (D15 to D0)
BHE = V_{IL} : 8-bit (D7 to D0)

Note: 1. A-1 is least significant address.

When BHE is 'low', D14 to D8 goes the high impedance state, and D15 should be A-1.

Mode Selection

	Pin							
					Data output		Address input	
Mode	$\overline{CE}$	$\overline{OE}$	BHE	D15/A-1	D0-D7	D8-D15	LSB	MSB
Standby	H	×*1	×	×	High-Z*2	High-Z	—	—
Output disable	L	H	×	×	High-Z	High-Z	—	—
Read (16-bit)	L	L	H	Dout	D0 to D7	D8 to D15	A0	A19
Read (8-bit)	L	L	L	L	D0 to D7	High-Z	A-1	A19
Read (8-bit)	L	L	L	H	D8 to D15	High-Z	A-1	A19

Notes: 1. ×: Don't care.
2. High-Z: High impedance

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage*1	V_{DD}	− 0.3 to + 5.5	V
All input and output voltage*1	Vin, Vout	− 0.3 to V_{DD} + 0.3	V
Operating temperature range	Topr	0 to + 70	°C
Storage temperature range	Tstg	− 55 to + 125	°C
Temperature under bias	Tbias	− 20 to + 85	°C

Note: 1. With respect to V_{SS}.

Recommended DC Operating Conditions (Ta = 0 to + 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
	V_{SS}	0	0	0	V
Input voltage	V_{IH}	2.2	—	V_{DD} + 0.3	V
	V_{IL}	− 0.3	—	0.8	V

DC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to + 70°C)

Parameter		Symbol	Min	Max	Unit	Test condition
Supply current	Active	I_{DD}	—	70	mA	V_{DD} = 3.6 V, I_{DOUT} = 0 mA, t_{RC} = 150 ns
	Standby	I_{SB1}	—	30	µA	V_{DD} = 3.6 V, $\overline{CE} \geq V_{DD}$ - 0.2 V
	Standby	I_{SB2}	—	3	mA	V_{DD} = 3.6 V, $\overline{CE} \geq$ 2.2 V
Input leakage current		$\|I_{IL}\|$	—	10	µA	Vin = 0 to V_{DD}
Output leakage current		$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, Vout = 0 to V_{DD}
Output voltage		V_{OH}	2.4	—	V	I_{OH} = – 2.0 mA
		V_{OL}	—	0.4	V	I_{OL} = 2.0 mA

Capacitance (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 25°C, Vin = 0 V, f = 1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D15/A-1 pin is output.

AC Characteristics (V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to + 70°C)

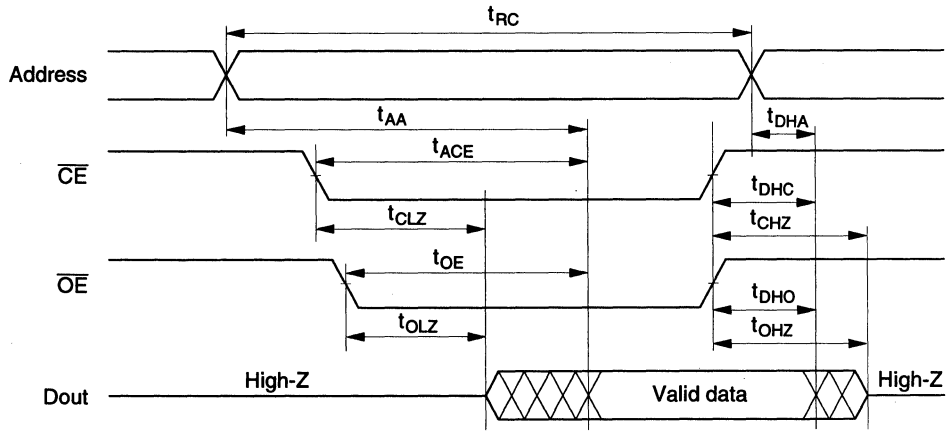
- Output load: 1TTL + C_L = 100 pF (including jig)
- Input pulse level: 0.4 to 2.4 V
- Input and output timing reference level: 1.4 V
- Input rise and fall time: 5ns

		HN62W4416N-15			
Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	150	—	ns	
Page read cycle time	t_{PC}	50	—	ns	
Address access time	t_{AA}	—	150	ns	
Page address access time	t_{PA}	—	50	ns	
$\overline{CE}$ access time	t_{ACE}	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	50	ns	
BHE access time	t_{BHE}	—	150	ns	
Output hold time from address change	t_{DHA}	5	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	ns	
Output hold time from BHE	t_{DHB}	0	—	ns	
$\overline{CE}$ to output in high-Z	t_{CHZ}	—	50	ns	1
$\overline{OE}$ to output in high-Z	t_{OHZ}	—	50	ns	1
BHE to output in high-Z	t_{BHZ}	—	50	ns	1
$\overline{CE}$ to output in low-Z	t_{CLZ}	5	—	ns	
$\overline{OE}$ to output in low-Z	t_{OLZ}	5	—	ns	
BHE to output in low-Z	t_{BLZ}	5	—	ns	

Note: 1. t_{CHZ}, t_{OHZ} and t_{BHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

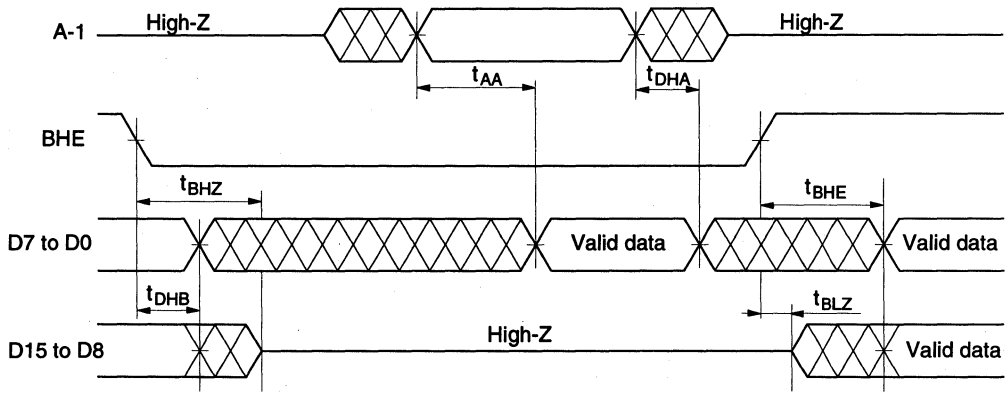
Timing Waveforms

Word Mode (BHE = 'V_{IH}') or Byte Mode (BHE = 'V_{IL}')



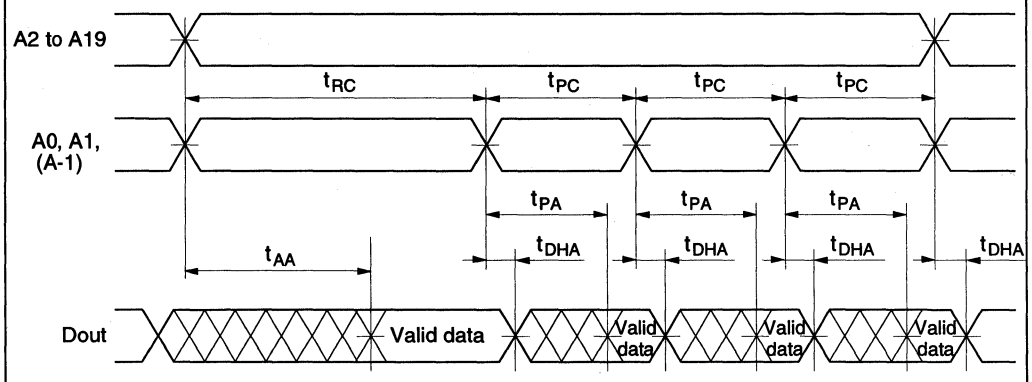
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Word Mode, Byte Mode Switch



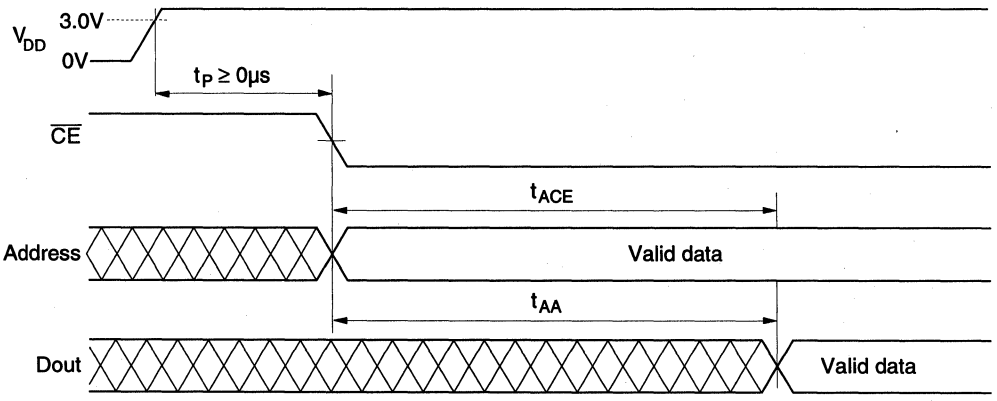
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable, A19 to A0 are valid.
2. D15/A-1 pin is in the output state when BHE is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

Page Mode



Notes: 1. Page address is determined as below.
Word mode (BHE = 'High'): A0, A1
Byte mode (BHE = 'Low'): A-1, A0, A1
2. $\overline{CE}$ and $\overline{OE}$ are enable.

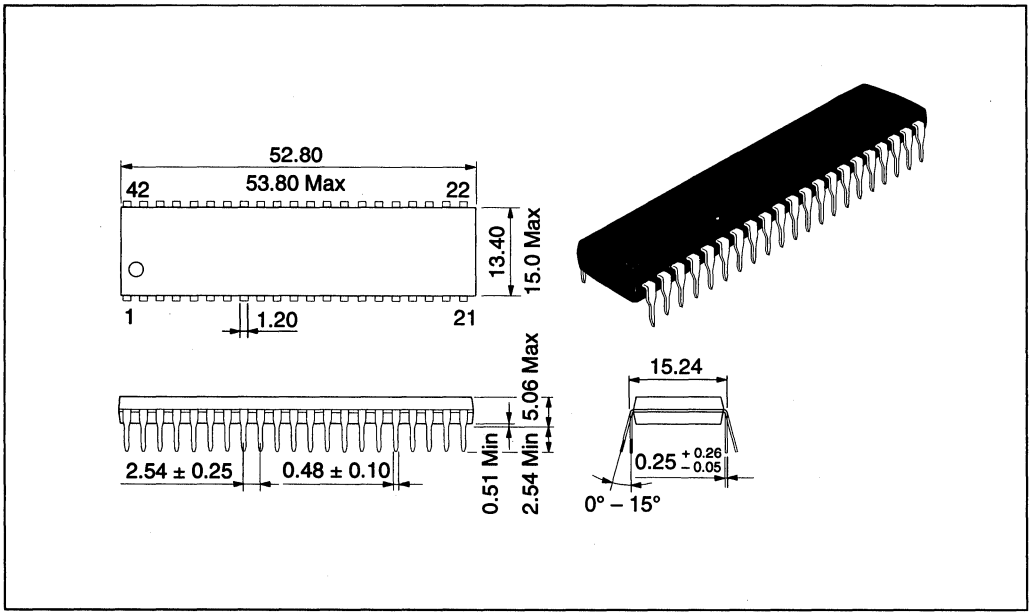
Power Up Sequence



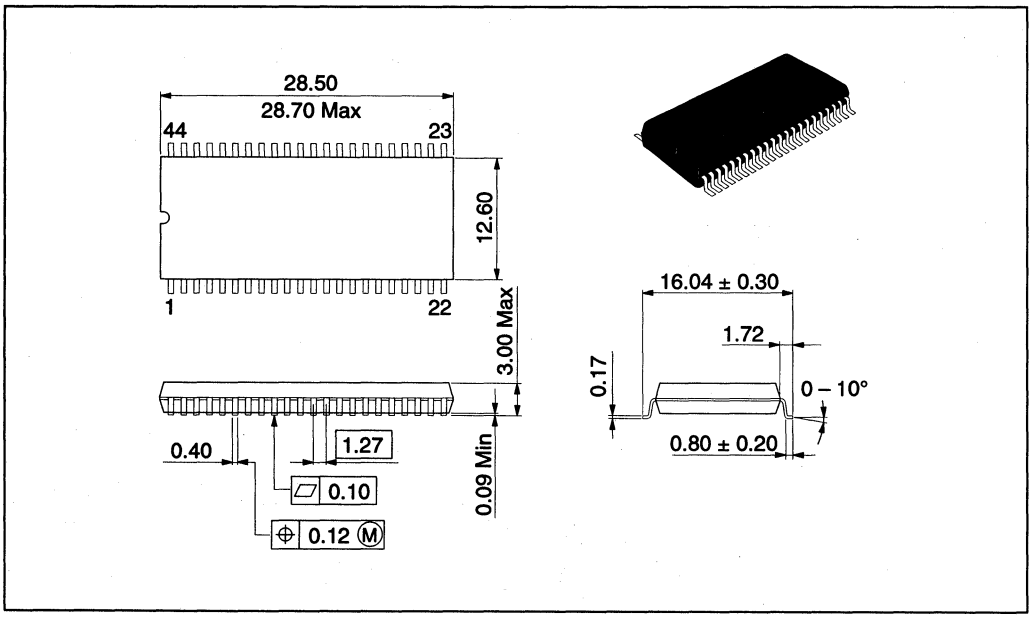
Notes: 1. This device is used ATD (Address Transition Detecter). Therefore, transfer either $\overline{CE}$ or address (A19 to A2) after power up to 3.0V.

Package Dimensions

HN62W4416NP Series (DP-42) **Unit: mm**

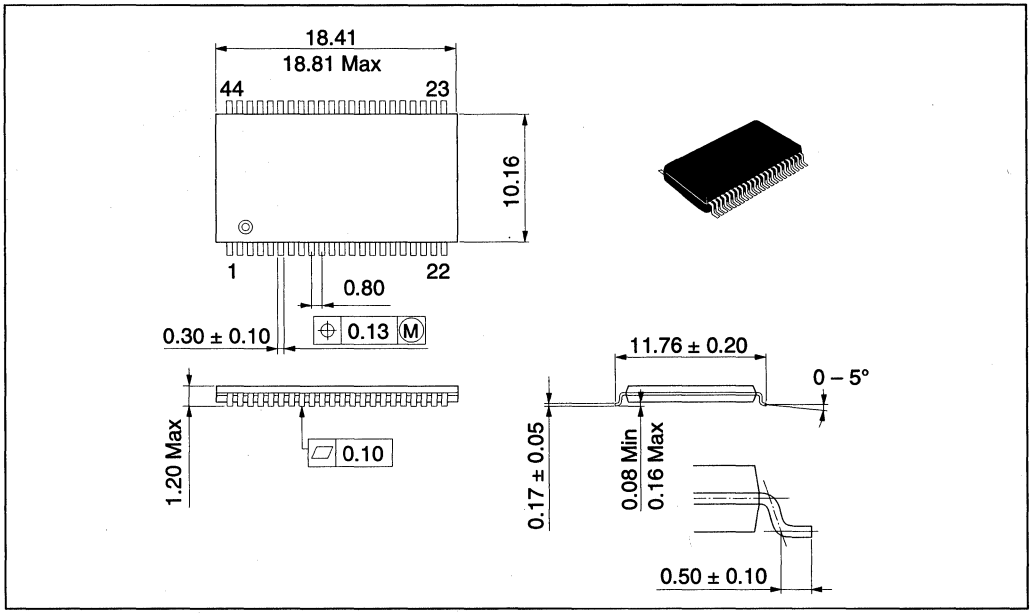


HN62W4416NFB Series (FP-44D) **Unit: mm**



Package Dimensions (cont)

HN62W4416NTT Series (TTP-44D) **Unit: mm**



HN62W5016N Series

524,288-word × 32-bit / 1,048,576-word × 16-bit CMOS Programmable Mask ROM

HITACHI

Preliminary
Rev. 0.0
October 4, 1995

The HN62W5016N is a 16-Mbit CMOS Programmable Mask ROM organized either as 524,288 words by 32 bits or as 1,048,576 words by 16 bits. Realizing low power consumption, this memory is allowed for battery operation. A high speed access of 120/150 ns is the most suitable to the system using a high speed micro-computer by 32 bits.

Ordering Information

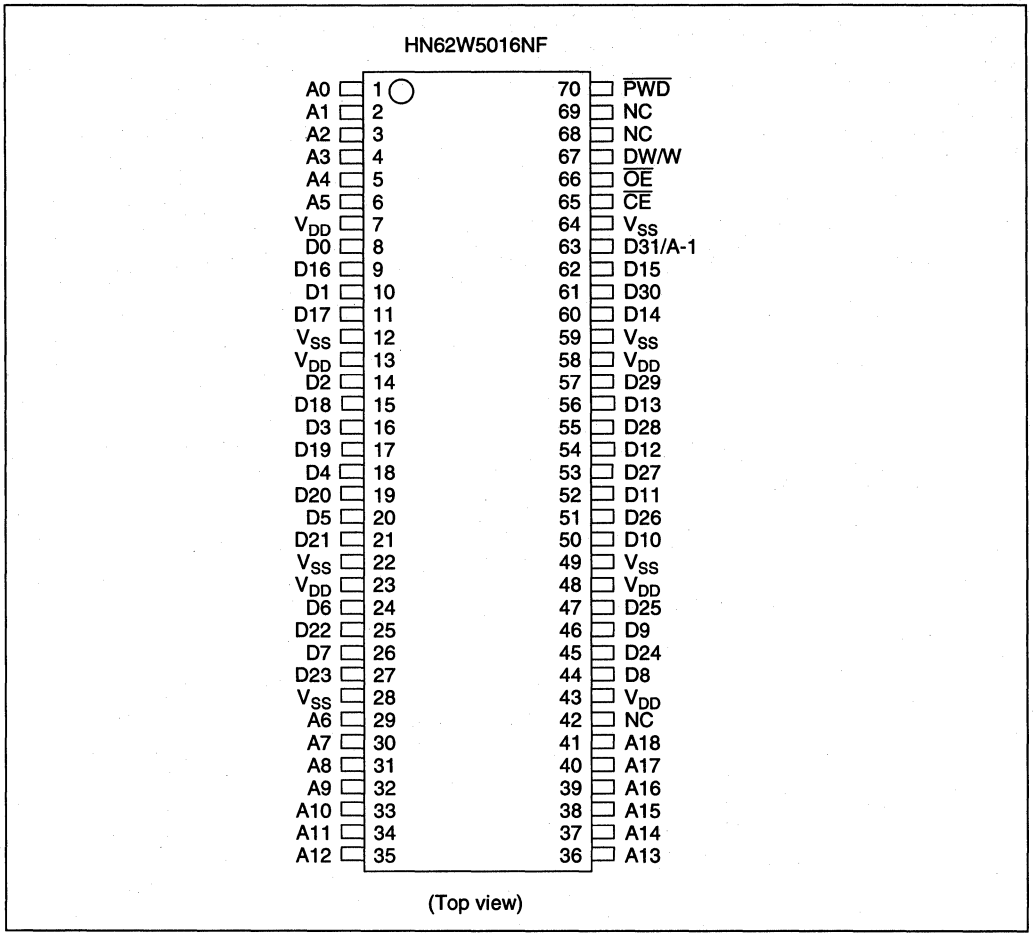
Type No.	Access time	Package
HN62W5016NF-12	120 ns	70 pin plastic SSOP (FP-70DS)
HN62W5016NF-15	150 ns	

Features

- Low voltage operation: 3.3 V ± 0.3 V
- High speed
  Normal access time: 120 ns/150 ns (max)
  Page access time: 40 ns/50 ns (max)
- Low power consumption
  Active : 360 mW (max)
  Standby : 0.72 mW (max)
  Power down mode : 36 μW (max)
- Double word-wide or word-wide data organization with DW/W
- 4 double-word page access on double word-wide mode
- 8 word page access on word-wide mode
- Three-state data output for or-tying
- LV-TTL compatible

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

Pin Arrangement

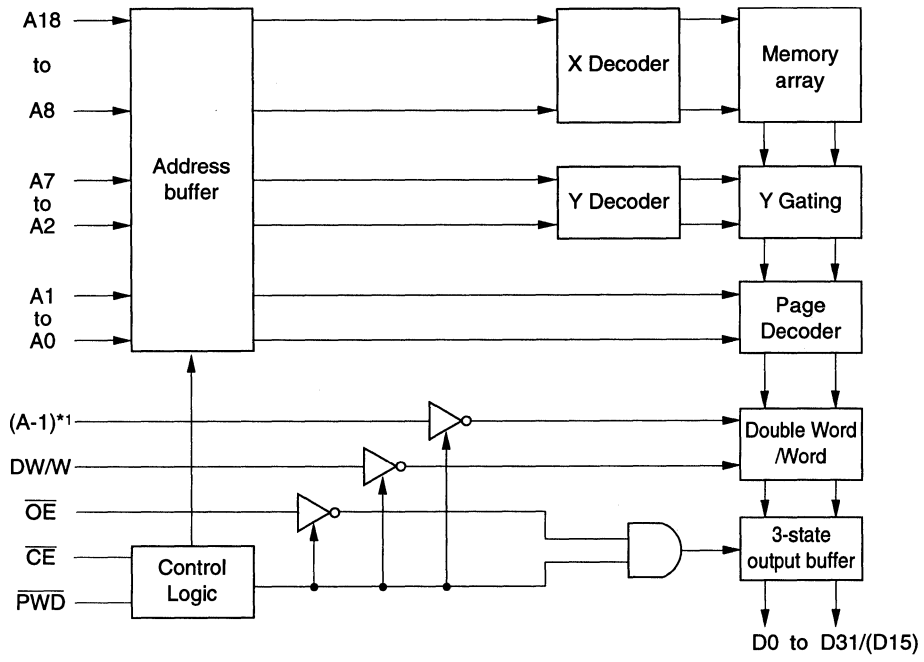


Pin Description

Pin name	Function
A2 to A18	Address inputs
A-1, A0 to A1	Page address inputs
D0 to D31	Data output
DW/W	32/16 bit (Double word/word) mode switch inputs
$\overline{CE}$	Chip enable

Pin name	Function
$\overline{OE}$	Output enable
$\overline{PWD}$	Power down input
NC	No connection
V_{DD}	Power supply
V_{SS}	Ground

Block Diagram



Note: 1. A-1 is least signifcant address.
When DW/W is 'low', D30 to D16 goes to high impedance state and D31 should be A-1.

$DW/W = V_{IH}$: 32-bit(D31 to D0)
$DW/W = V_{IL}$: 16-bit(D15 to D0)

Mode Selection

	Pin								
						Data output		Address input	
Mode	$\overline{PWD}$	$\overline{CE}$	$\overline{OE}$	DW/W	D31/A-1	D0-D15	D16-D31	LSB	MSB
Power down	L	×*1	×	×	×	High-Z*2	High-Z	—	—
Standby	H	H	×	×	×	High-Z	High-Z	—	—
Output disable	H	L	H	×	×	High-Z	High-Z	—	—
Read (32-bit)	H	L	L	H	Dout	D0 to D15	D16 to D31	A0	A18
Read (16-bit)	H	L	L	L	L	D0 to D15	High-Z	A-1	A18
Read (16-bit)	H	L	L	L	H	D16 to D31	High-Z	A-1	A18

Notes: 1. ×: Don't care.
2. High-Z: High impedance.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{DD}	–0.3 to +5.5	V	1
All input and output voltage	Vin, Vout	–0.3 to V_{DD} + 0.3	V	1
Operating temperatue range	Topr	0 to +70	°C	
Storage temperature range	Tstg	–55 to +125	°C	
Temperature under bias	Tbias	–20 to +85	°C	

Note: 1. With respect to V_{SS}

Recommended DC Operating Conditions (V_{SS} = 0 V, Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	3.0	3.3	3.6	V
Input voltage	V_{IH}	2.2	—	V_{DD} + 0.3	V
	V_{IL}	–0.3	—	0.8	V

DC Characteristics (V_{DD} = 3.3 ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70°C)

Parameter	Symbol	Min	Max	Unit	Test condition
Operating power supply current	I_{DD}	—	100	mA	V_{DD} = 3.6 V, I_{DOUT} = 0 mA, t_{RC} = min
Standby power supply current	I_{SB1}	—	200	µA	V_{DD} = 3.6 V, $\overline{CE} \geq V_{DD} - 0.2$ V
	I_{SB2}	—	3	mA	V_{DD} = 3.6 V, $\overline{CE} \geq 2.2$ V
Power down supply current	I_{PWD}	—	10	µA	V_{DD} = 3.6 V, $\overline{PWD} \leq 0.2$ V
Input leakage current	$\|I_{IL}\|$	—	10	µA	V_{IN} = 0 V to V_{DD}
Output leakage current	$\|I_{OL}\|$	—	10	µA	$\overline{CE}$ = 2.2 V, V_{OUT} = 0 V to V_{DD}
Output voltage	V_{OH}	2.4	—	V	I_{OH} = –2 mA
	V_{OL}	—	0.4	V	I_{OL} = 2 mA

Capacitance (V_{DD} = 3.3 ±0.3 V, V_{SS} = 0 V, Ta = 25°C, V_{IN} = 0 V, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance*1	Cin	—	10	pF
Output capacitance*1	Cout	—	15	pF

Note: 1. This parameter is sampled and not 100% tested. D31/ A-1 pin is output.

AC Characteristics (V_{DD} = 3.3 ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70°C)

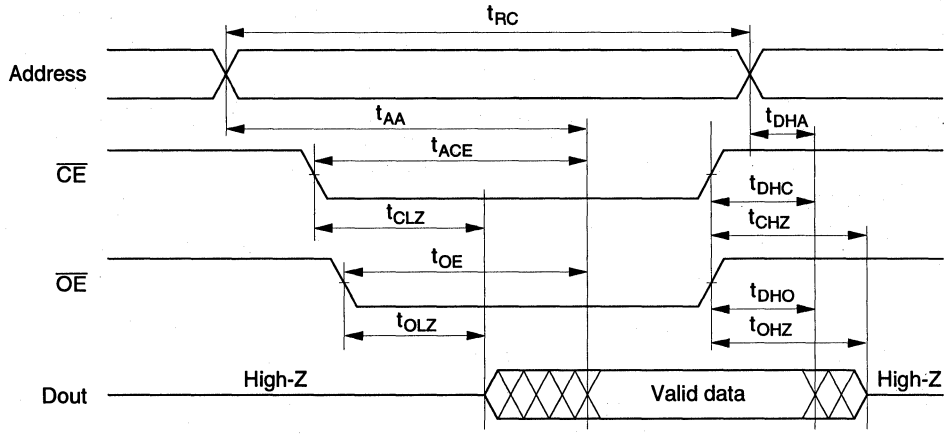
- Output load: 1TTL + C_L = 100 pF (including jig capacitance)
- Input pulse level: 0.4 V to 2.4 V
- Input and output timing reference level: 1.4 V
- Input rise and fall time: 5 ns

		HN62W5016N-12		HN62W5016N-15			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Note**
Read cycle time	t_{RC}	120	—	150	—	ns	
Page read cycle time	t_{PC}	40	—	50	—	ns	
Address access time	t_{AA}	—	120	—	150	ns	
Page address access time	t_{PA}	—	40	—	50	ns	
$\overline{CE}$ access time	t_{ACE}	—	120	—	150	ns	
$\overline{OE}$ access time	t_{OE}	—	40	—	50	ns	
DW/W access time	t_{DWW}	—	120	—	150	ns	
Output hold time from address change	t_{DHA}	0	—	0	—	ns	
Output hold time from $\overline{CE}$	t_{DHC}	0	—	0	—	ns	
Output hold time from $\overline{OE}$	t_{DHO}	0	—	0	—	ns	
Output hold time from DW/W	t_{DHD}	0	—	0	—	ns	
Output hold time from $\overline{PWD}$	t_{DHP}	0	—	0	—	ns	
$\overline{CE}$ to output in high Z	t_{CHZ}	—	40	—	50	ns	1
$\overline{OE}$ to output in high Z	t_{OHZ}	—	40	—	50	ns	1
DW/W to output in high Z	t_{DHZ}	—	40	—	50	ns	1
$\overline{CE}$ to output in low Z	t_{CLZ}	5	—	5	—	ns	
$\overline{OE}$ to output in low Z	t_{OLZ}	5	—	5	—	ns	
DW/W to output in low Z	t_{DLZ}	5	—	5	—	ns	
Recovery time from $\overline{PWD}$	t_R	10	—	10	—	µs	

Note: 1. t_{CHZ}, t_{OHZ} and t_{DHZ} are defined as the time at which the output achieves the open circuit conditions and are not referred to output voltage levels.

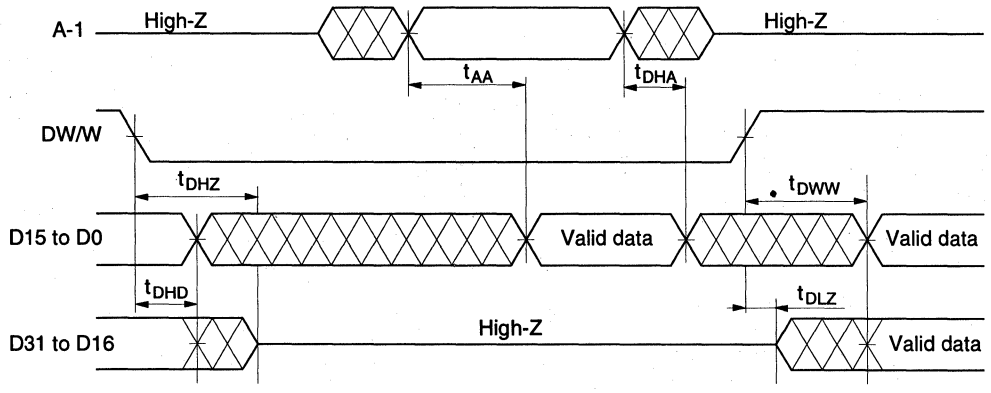
Timing Waveform

Double word mode (DW/W = 'V_{IH}') **or Word mode** (DW/W = 'V_{IL}')



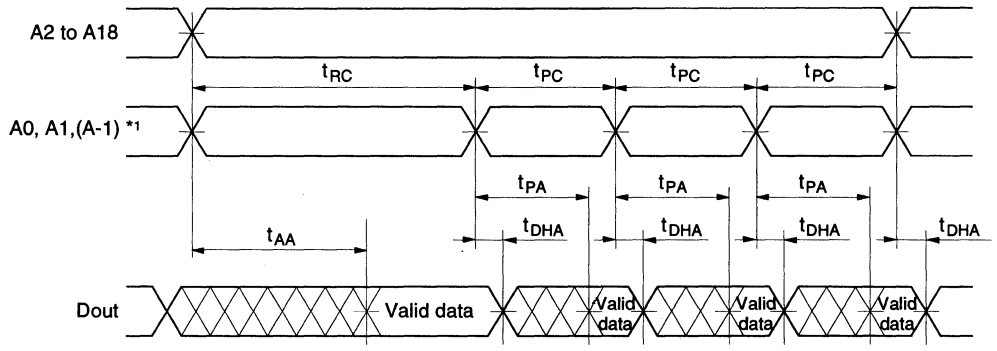
Notes: 1. t_{DHA}, t_{DHC}, t_{DHO}: Determined by faster.
2. t_{AA}, t_{ACE}, t_{OE}: Determined by slower.
3. t_{CLZ}, t_{OLZ}: Determined by slower.

Double Word Mode, Word mode switch



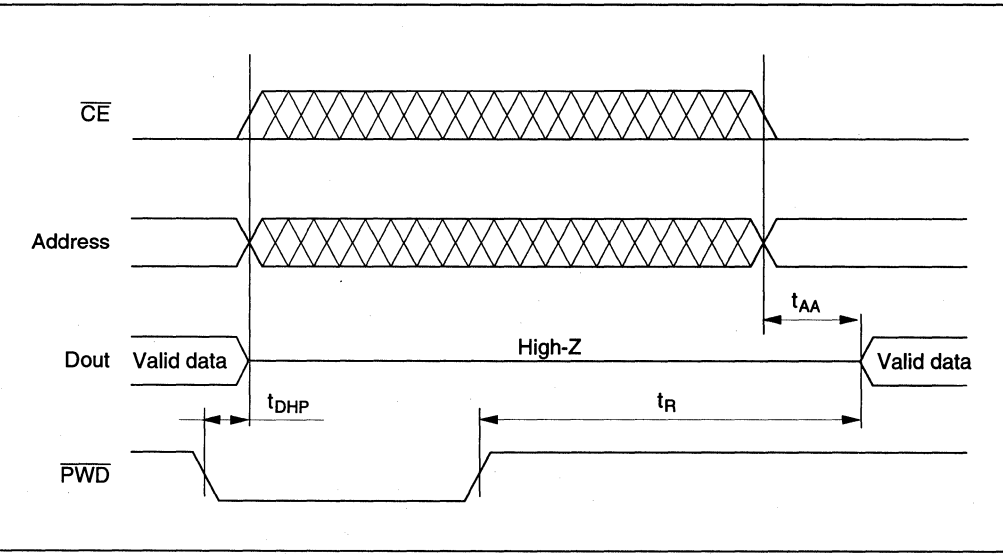
Notes: 1. $\overline{CE}$ and $\overline{OE}$ are enable, A18 to A0 are valid.
2. D31/A-1 pin is in the output state when DW/W is high, $\overline{CE}$ and $\overline{OE}$ are enable.
Therefore, the input signals of opposite phase to the output must not be applied to them.

Page mode

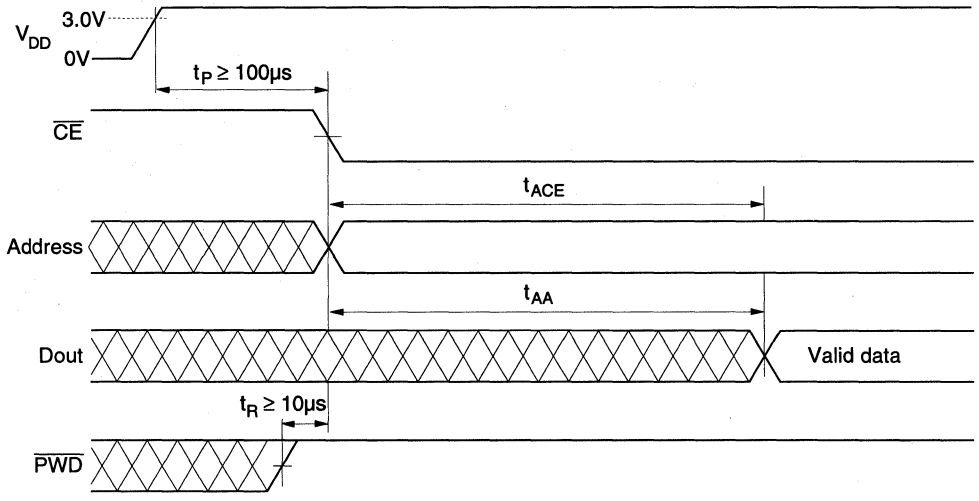


Notes: 1. Page address is determind as below
Double word mode (DW/W = 'VIH'): A0, A1
Word mode (DW/W = 'VIL'): A-1, A0, A1
2. $\overline{CE}$ and $\overline{OE}$ are enable.

Power down mode



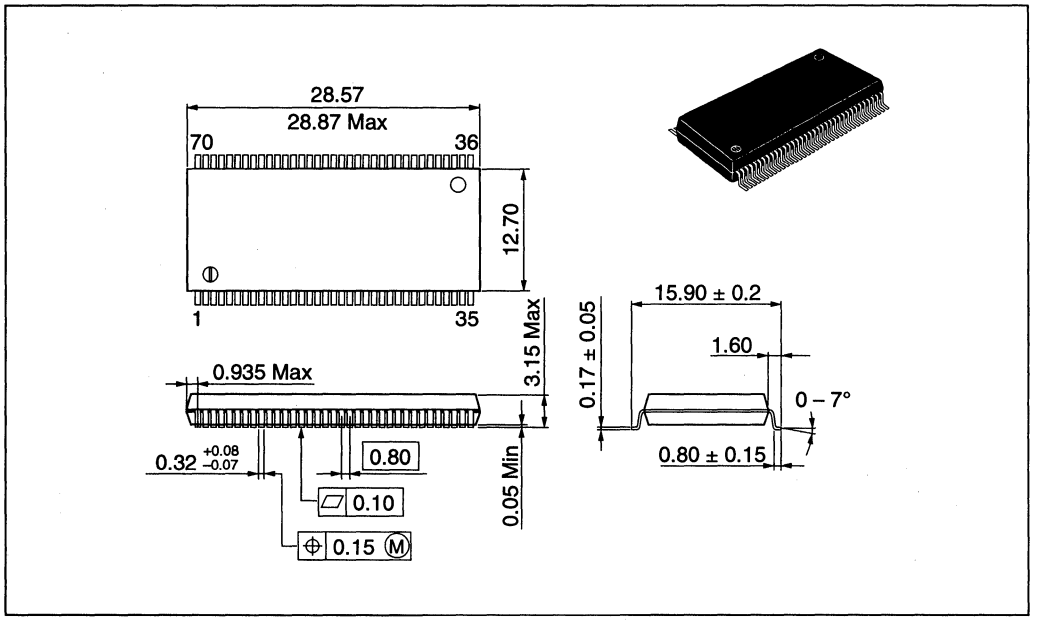
Power Up Sequence



Notes: 1. This device is used ATD(Address Transition Detector). Therefore, transfer either $\overline{CE}$ or address(A18 to A2) after power up to 3.0 V.
2. t_P, t_R: Determined by slower.

Package Dimensions

HN62W5016NF Series (FP-70DS) **Unit : mm**



NOTES

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