HITACHI GATE ARRAY

HITACHI

1600Gates CMOS HD61L Series

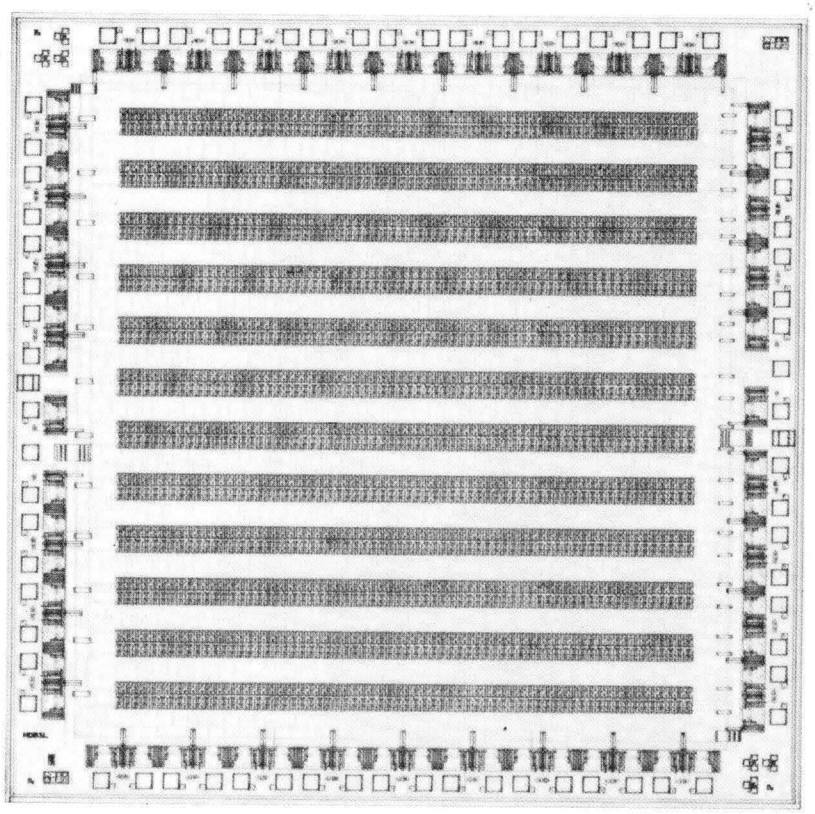
The HD61L is a master slice CMOS gate array using 2-layer metal process. The HD61L has 1,584 internal 2-NAND equivalent gates, and 68 input/output buffers that are directly compatible with TTL. These gates are interconnected to meet customer's system requirement.
The LSI design is automated by DA (Design Automation) system.

The custom LSI is developed in a short lead time and at a low cost, that exactly matches the logic diagram and test pattern supplied by the customer.
The HD61L Series are best suited for redesigning conventional TTL or CMOS standard logic ICs to an LSI configuration.
HD61L makes customer's systems low cost, compact, light-weight, and reliable.

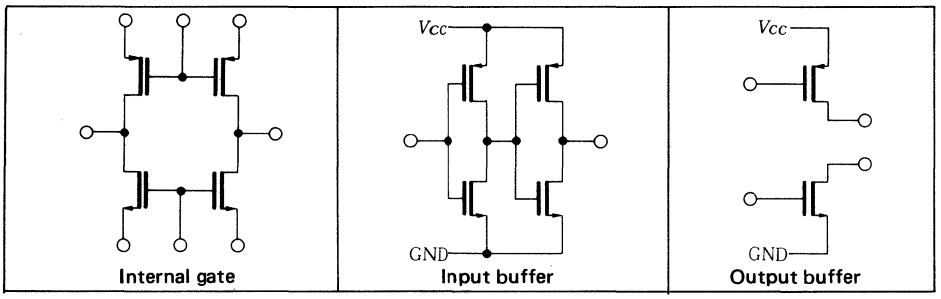
■ FEATURES

- Fast operation . . . . . .
  Internal gates 5ns/gate (typ.)
  Input buffers 15ns (typ.)
  Output buffers 40ns (typ., C_L = 130pF)
- Low power dissipation . . . . . .
  100 μW/gate (typ., 10 MHz)
- Logic blocks . . . . .56 kinds
- Input/output format . . . . . .
  All 68 pins selectable for INPUT/OUTPUT/INPUT-OUTPUT
  Outputs selectable for CMOS/OPEN DRAIN/3-STATE
- Reliable package . . . . . .
  Ceramic DIP 28 pin/ceramic DIP 40 pin/Ceramic axial 72 pin/Plastic DIP 28 pin/Plastic DIP 40 pin/Plastic Flat 80 pin
- Simple customer interface . . . . . .
  Logical diagrams and test patterns only
- Short development time and low development cost
- Suitable for production of proliferated types in a small quantity

■ CHIP LAYOUT

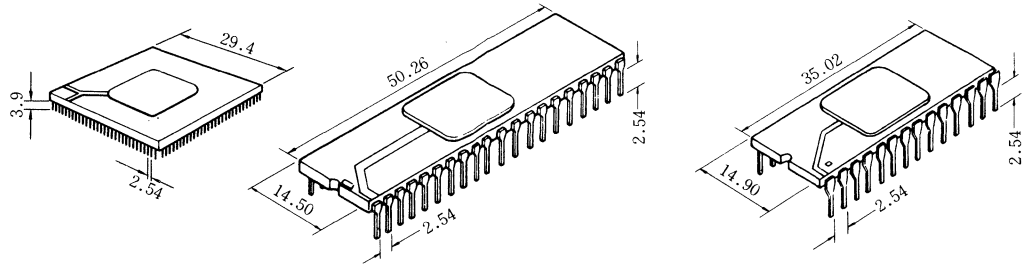


■ BASIC CELL

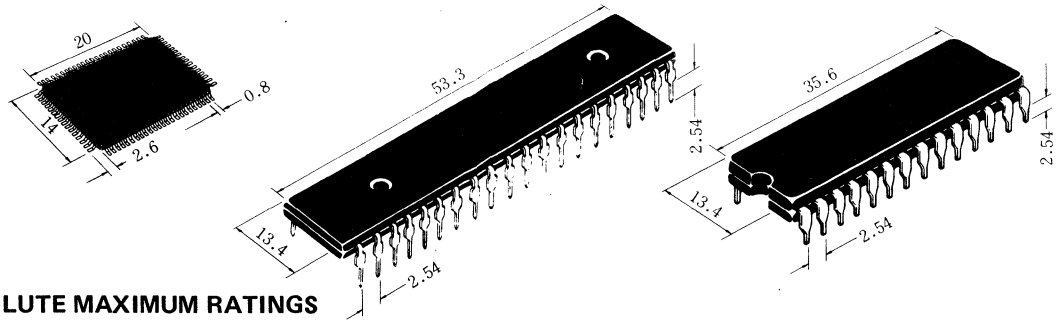


■ PACKAGE

- Ceramic Axial 72 Pin
- Ceramic DIP 40 Pin
- Ceramic DIP 28 Pin



- Plastic FP 80 Pin
- Plastic DIP 40 Pin
- Plastic DIP 28 Pin



■ ABSOLUTE MAXIMUM RATINGS

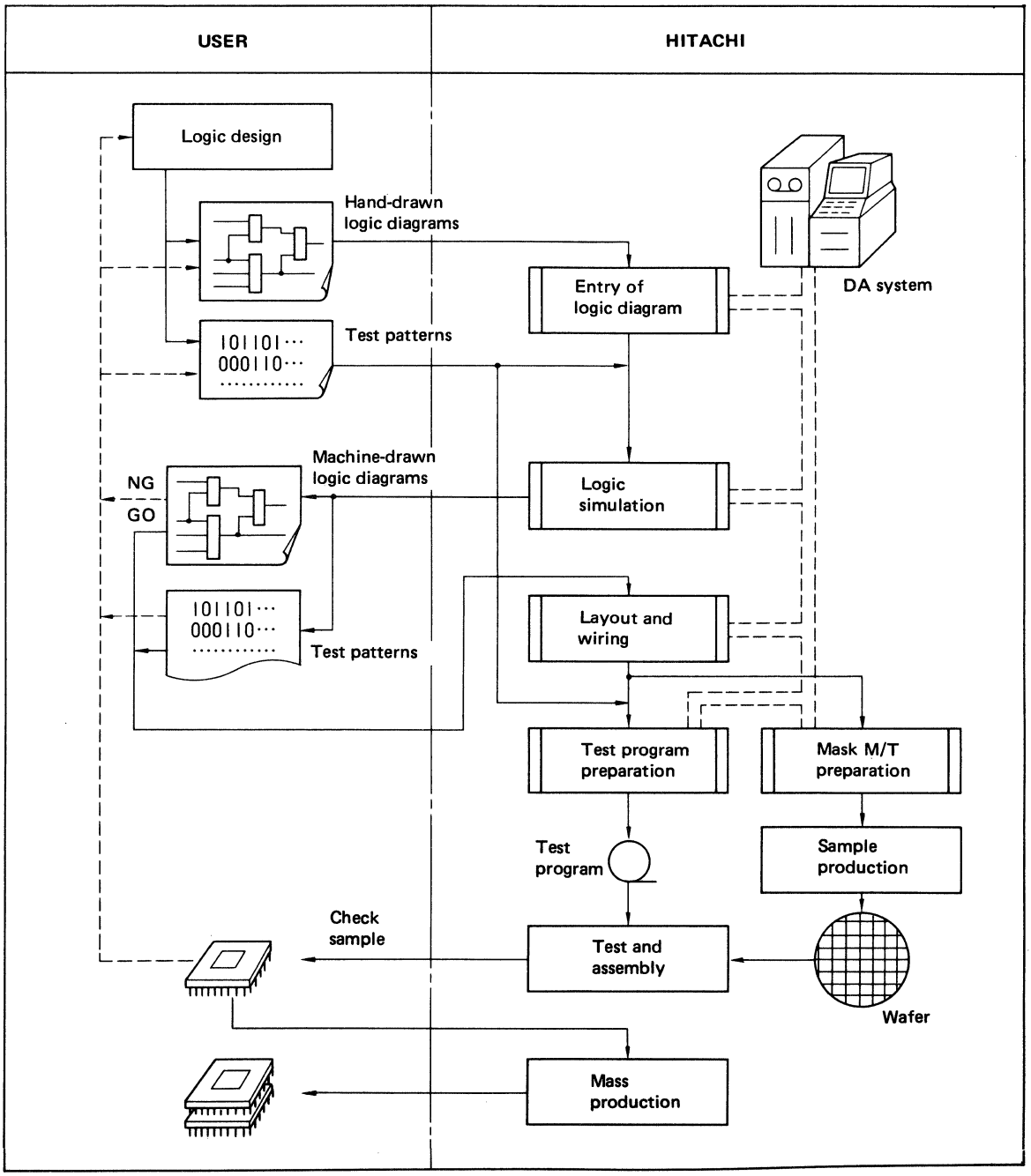
Item	Symbol	Rating	Unit
Supply Voltage	V_{CC}	−0.3 ~ +6.7	V
Terminal Voltage	V_T	−0.3 ~ V_{CC} + 0.3	V
Operating Temperature	T_{opr}	−20 ~ +75	°C
Storage Temperature	T_{stg}	−55 ~ +150	°C

■ ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±5%, Ta = −20 to +75°C unless otherwise specified)

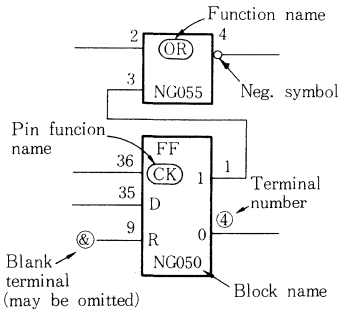
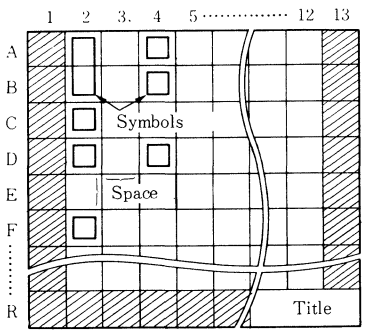
Item		Symbol	Test Conditions	min.	typ.	max.	Unit
Input Voltage		V_{IH}		2.0	–	V_{CC} + 0.3	V
		V_{IL}		−0.3	–	0.8	V
Output Voltage		V_{OH}	I_{OH} = −2 mA	2.4	–	–	V
		V_{OL}	I_{OL} = 2 mA	–	–	0.4	V
Input Leakage Current		I_{IL}		–	–	1.0	μA
Output Leakage Current		I_{OL}	V_{CC} = 5.25V, at high impedance output	–	–	1.0	μA
Delay Time	Internal	t_{pd}	Average/gate (reference only)	–	5	–	ns
	Input		F.O. = 16	–	15	–	
	Output		C_L = 130 pF	–	40	–	
Power Dissipation	Operating	I_{CC}	V_{CC} = 5V, internal gate	–	20	–	μA/gate
	Standby	I_{CCS}	V_{CC} = 5V, internal gate	–	10	–	μA

■ DEVELOPMENT FLOW

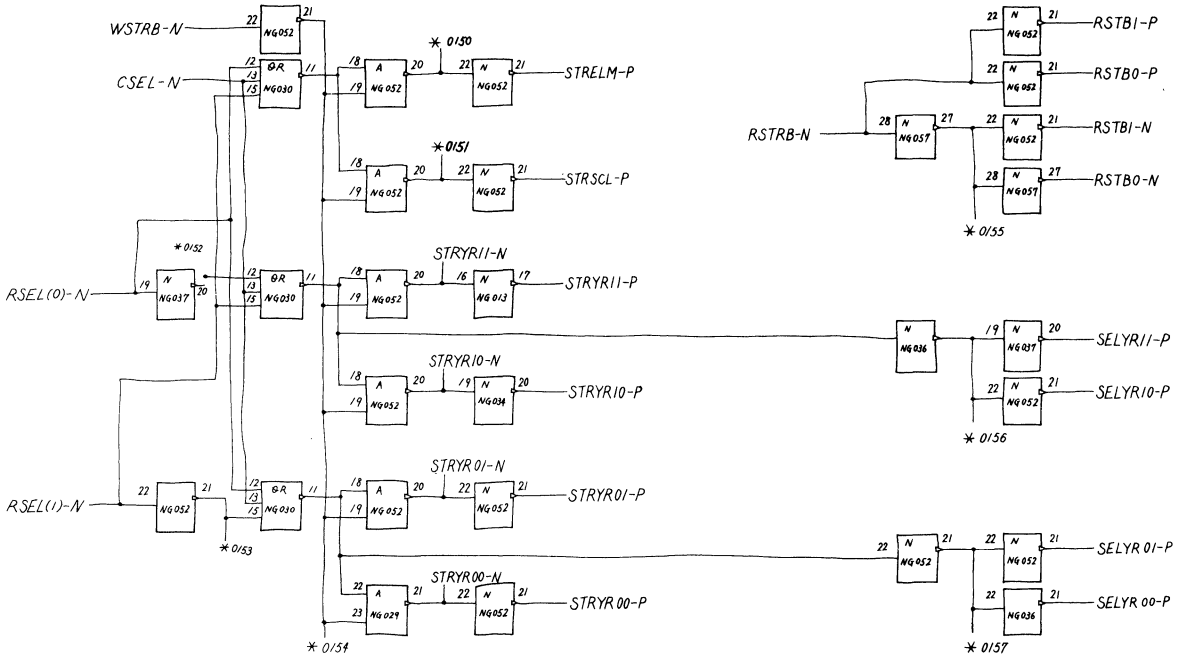
Gate arrays will be developed in conformity to the flow shown. The interface between user and Hitachi is based on hand-drawn logical diagrams and test patterns. Hitachi will submit these data into computer for logic simulation, layout, wiring, and test program preparation. After that, a sample will be produced. In the process, the machine-drawn logic diagrams and the result of the logic simulation are to be verified by the user to Hitachi will perform delay simulation (such as critical path) on request.



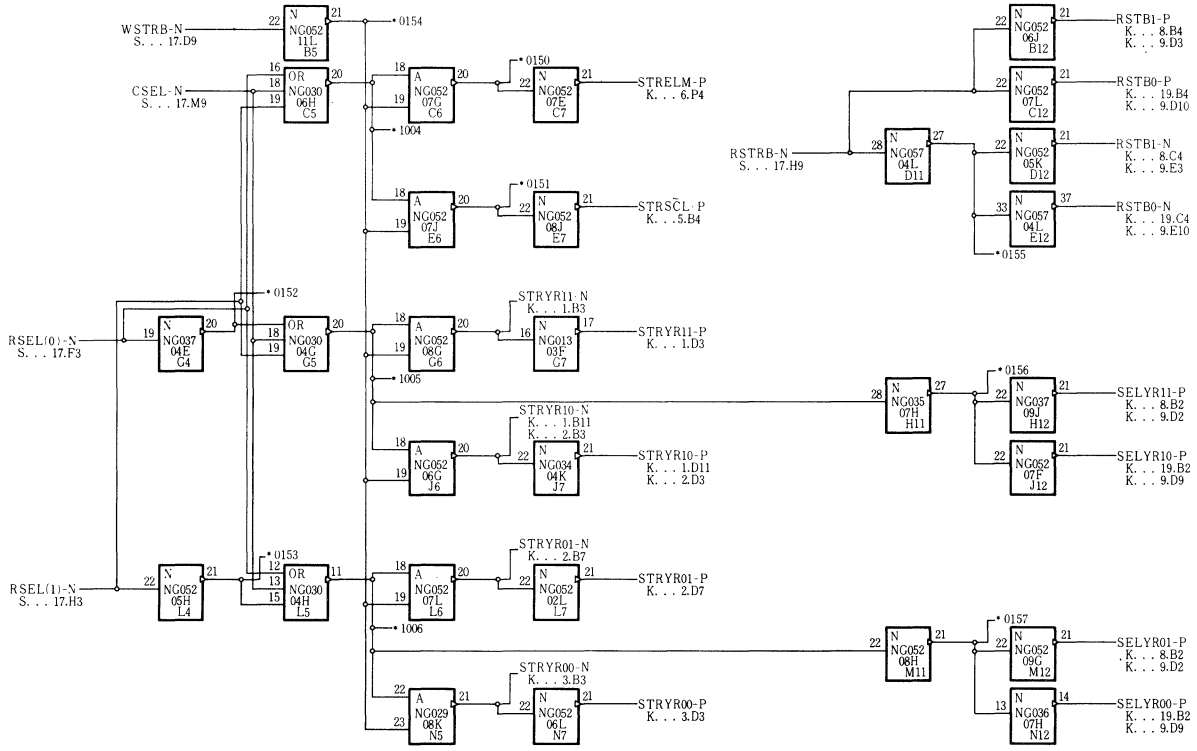
■ DRAWING LOGIC DIAGRAMS

NO.	ITEM	RULES
1	Forms	Size A-3 forms supplied by Hitachi.
2	Characters	(1) 2 ~ 3 mm or larger alphanumerics and special characters [/ (slant), = (equal), — (minus), ((left parenthesis), , (comma),) (right parenthesis)] (2) The alphabetics shown must be written as in the bottom column. Alphabet: I J O U Script: i j $\bar{o}$ u
3	Signal name	(1) The following signals must be accompanied by the corresponding signal name. (i) LSI input/output signals: up to 14 characters beginning with an alphabetic character (ii) Signals extending over two or more diagrams: up to 10 characters beginning with an alphabetic character (2) LSI internal signals terminating within one diagram: (i) up to 10 characters beginning with an alphabetic character (ii) a 4-digit number preceded by an asterisk(*) * ○ ○ ○ ○ — serial number within page (50 ~ 99); page of diagram (01 ~ 49)
4	Logic symbol	(1) Use templates supplied by Hitachi. (2) Affix the following information to each logical symbol: (i) Function name (A, OR, FF) (ii) Block name (iii) Pin function name (S, R, CK) (iv) Negation symbol (○ or ▷) (v) Block terminal number 
5	Signal line	(1) LSI input/output signals must be shown by □ with LSI pin number given in [ ]. (2) Up to three lines can be led out at one junction point. 
6	Symbol layout	(1) A signal must be drawn from left to right like a stream. (2) No symbol must be placed in columns 1 and 13 and in row R (hatched portions shown). (3) No symbol must be placed in 5 or more consecutive rows to provide a path for signal lines. (4) No symbol must be placed in two or more consecutive columns to provide an area accommodating signal names and cross reference information. 
7	Cross reference	(1) If a signal extends over two or more machine-drawn logical diagrams, the following information is given under the signal name: K – 15, B10 — B10: Logical coordinates of the destination; 15: Logic diagram page of the destination; K: Terminal specification of the destination (K : sink, S : source, Z : 3-state output, N : 3-state control)

• MANUAL-DRAWN LOGIC DIAGRAM



• MACHINE-DRAWN LOGIC DIAGRAM

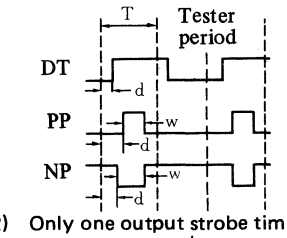


■ DESCRIBING TEST PATTERNS

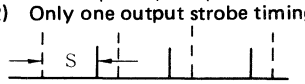
1 Timing definition

RULES

(1) Three input signal formats are used:



(2) Only one output strobe timing is used:



EXAMPLE OF DESCRIPTION

Tester period		300 ns		
	Timing No.	Format	d (ns)	w (ns)
Input	I0	DT	0	–
	I1	DT	20	–
	I2	PP	50	100
	⋮	⋮	⋮	⋮
	I6	NP	100	100
Common	B1	I0		
	B2	I1		
Output	O1	200 ns		

[Notes]
1. Number of input timing pulses: up to 7
2. All I0 must be DT format with d = 0.
3. What input format to be used must be specified.

2 Test pattern

RULES

(1) Specify pattern layout and timing.
signal name 1 timing No.
signal name 2 timing No.
⋮ ⋮
signal name n timing No.

(2) Pattern must be drawn with time set vertically and by using the following characters:

Input	DT format	0, 1
	PP format	0, P
	NP format	N, 1
Output		H, L, Z, X

[Notes]
1. Z . . . Hi-Z; X . . . undefined, mask
2. Blank may be used when signals do not change.

(3) If the same pattern is repeated, draw as follows:

#REPT count-1;
Repeated pattern
#REND:

EXAMPLE OF DESCRIPTION

```
INP-1      I2
 ⋮         ⋮
BUS-1      B1
 ⋮         ⋮
OUT-1      O1
 ⋮         ⋮
```

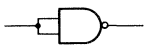
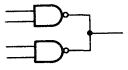
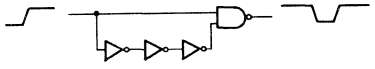
INP-1 is input at timing I2.

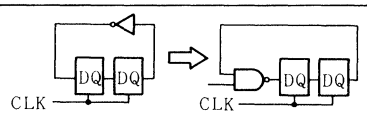
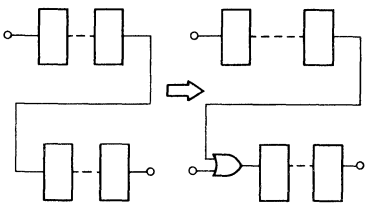
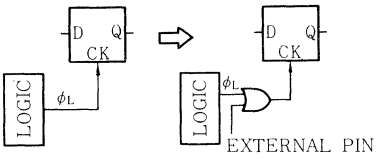
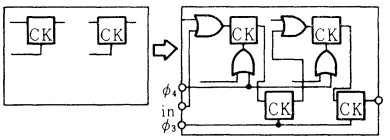
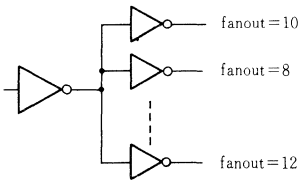
```
1  0  1  1  0  X  X  X  X
#REPT 5;
1  0  1  0  0  X  X  H  L   } Repeated
1  1  0  0  0  X  X  H  L   } (5 + 1)
0  1  1  0  1  X  X  H  L   } times
#REND;
0  1  0  0  1  Z  Z  H  L
1  0  1  0  0  1  0  L  L
1  1  0  1  0  0  0  L  L
0  1  0  0  0  1  1  L  H
0  0  0  1  0  Z  Z  H  H
1  0  1  1  1  H  L  L  H
0  1  1  0  0  L  L  H  L
                0  H  H  H  H
```

3 Logical simulation

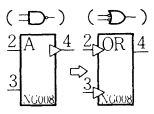
Test patterns are also used for logical simulation. If the result of simulation contains LSI internal signals you want to output, list all of their names.

■ LOGIC DESIGN PRECAUTIONS

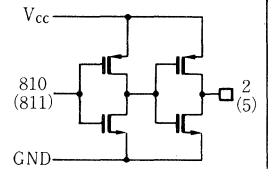
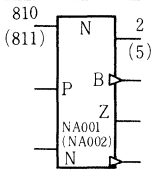
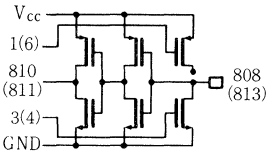
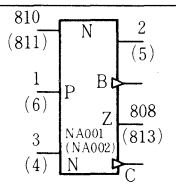
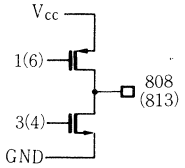
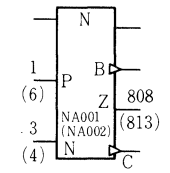
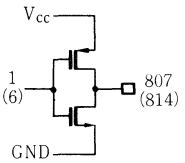
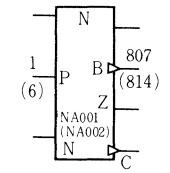
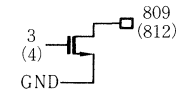
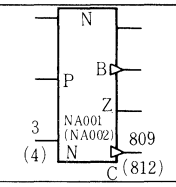
NO.	ITEM	CONTENTS	EXAMPLES
1	Don'ts	Multiple same input within the same macro cell is inhibited.	
		Output-to-output connection is inhibited (except for 3-state output buffer).	
		Chopper circuit using delay of macro cell is inhibited.	

NO.	ITEM	CONTENTS	EXAMPLES
2	Recommendations for improved detection rate	Use circuits that can be initialized from outside not those which cannot be initialized.	
		Use externally controllable terminals in proper positions for serial multistage connection of such as shift registers and counters.	
		Use externally controllable terminals in circuits using, as clock input, those signals (ϕ_L) which are long in time interval as compared with base clock.	
		Consider adding a test circuit which permits detection of internal latching by input of test signals and clocks from external pin. (scanpath design)	
3	Recommendations for improved characteristics	Clock distribution Drive capability that can be derived from one buffer is limited. It is recommended that clock buffer output with high fanout be distributed to some buffers as shown.	

■ INSTRUCTIONS ON BLOCK LIBRARY

NO.	ITEM	INSTRUCTIONS	
1	Maximum packaging density	For efficient automatic design, the packaging density should preferably be 90 ~ 95% of the maximum design density (1,584 gates).	
2	Macro cell	Using macro cells dedicated to the HD61L, perform logic design in accordance with the format specified in advance.	
3	Product-sum conversion	If you want to use the same macro cells (such as NAND and NOR) shown in the block library table as product-sum converted ones, change the positions of the function name and negation symbols as shown.	 Example of product-sum converted logic symbols
4	Propagation delay time	Calculation of propagation delay time is supported by DA. However, if you want to obtain critical path and other important factors by pencil-and-paper calculation, apply the equations shown at the right according to the block library table.	$t_{PLH} = t_{OLH} + K_{LH} \cdot C_L$ $t_{PHL} = t_{OHL} + K_{HL} \cdot C_L$ where, 0.4 pF/fanout must be used for calculation of load capacitance C_L.
5	Total number of gates	The total number of gates to be used can be calculated by obtaining the total sum of the equivalent gates. This can check whether or not the maximum packaging density (see 1 above) is exceeded.	Total number of gates = $\sum_i$ [ni] gates

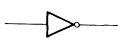
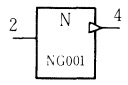
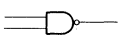
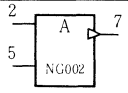
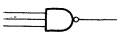
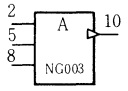
• I/O Buffer

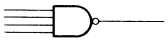
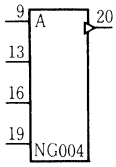
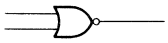
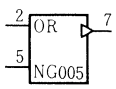
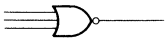
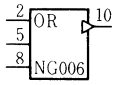
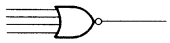
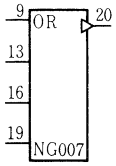
Macro Cell: Functional block name	Macro Cell: Equivalent circuit	Macro Cell: Symbolic diagram	Symbol No.	Propagation delay time: Input terminal name	Propagation delay time: Output terminal name	t_{PLH} (ns): t_{OLH}	t_{PLH} (ns): K_{LH}	t_{PHL} (ns): t_{OHL}	t_{PHL} (ns): K_{HL}
Input buffer NA001 or NA002 (Note 1)			8	810 (811)	2 (5)	7.7	2.0	6.7	1.0
3-state output & input buffer NA001 or NA002 (Note 1)			8	Input: See "Input Buffer".					
				Output: See "3-stage Buffer".					
3-state output NA001 or NA002 (Note 1)			8	1 (PMOS) 3 (NMOS) (6 (PMOS) 4 (NMOS))	808 (813)	1.5	0.17	2.5	0.34
Inverted output NA001 or NA002 (Note 1)			8	1 (6)	807 (814)	2.0	0.17	4.0	0.34
Open drain output NA001 or NA002 (Note 1)			8	3 (4)	809 (812)	—	—	2.5	0.34

(Note 1) NA001 . . . . . applies to pins 11 ~ 18, 27 ~ 37, 45 ~ 52, 61 ~ 64, 66 ~ 70 — 60, 65 = VCC
NA002 . . . . . applies to pins 1 ~ 10, 19 ~ 26, 38 ~ 43, 53 ~ 59, 71 — 44, 72 = GND

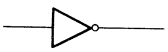
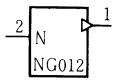
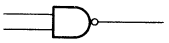
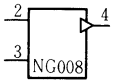
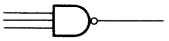
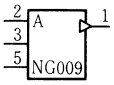
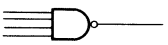
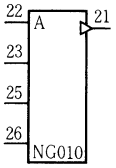
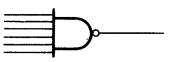
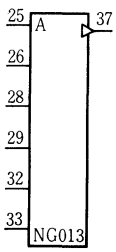
(Note 2) Pin No. of chips to which parenthesized terminals apply:
1, 2, 3, 8, 9, 11, 12, 14, 15, 17, 18, 19, 20, 21, 27, 28, 29, 32, 33, 35, 36, 37, 40, 41, 42, 45, 48, 52, 55, 56, 57, 58, 59, 63

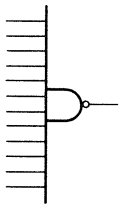
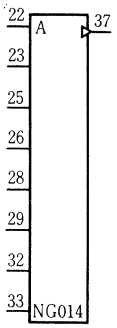
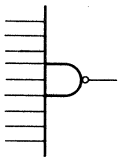
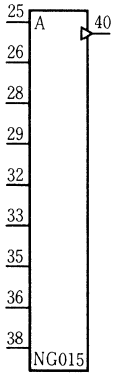
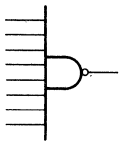
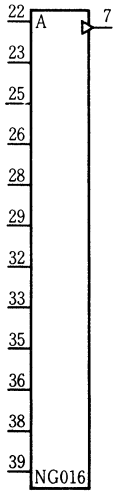
• Power Gate

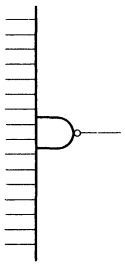
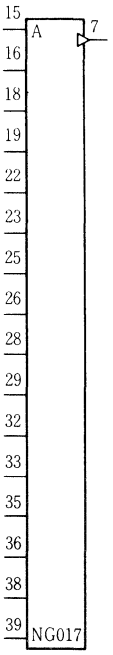
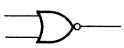
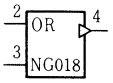
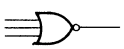
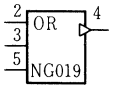
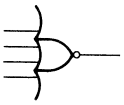
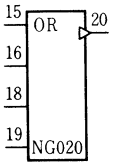
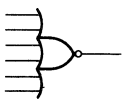
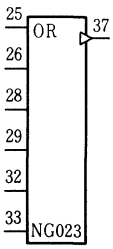
Macro Cell: Functional block name	Macro Cell: Equivalent circuit	Macro Cell: No. of equivalent gate	Symbolic diagram	Symbol No.	Propagation delay time: t_{PLH} (ns): t_{OLH}	t_{PLH} (ns): K_{LH}	t_{PHL} (ns): t_{OHL}	t_{PHL} (ns): K_{HL}
Power inverter NG001		1		11	1.2	1.5	0.9	1.5
Power-2 input NAND NG002		2		11	1.3	1.9	1.2	1.3
Power-3 input NAND NG003		3		11	2.1	2.0	1.9	1.7

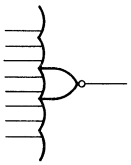
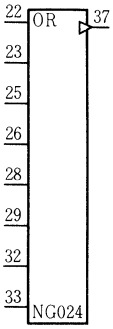
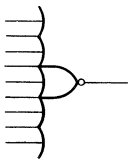
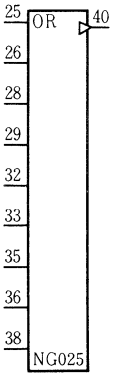
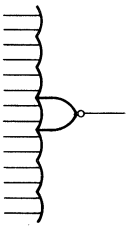
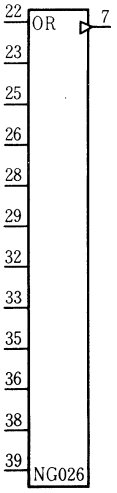
Macro Cell				Symbol No.	Propagation delay time			
Functional block name	Equivalent circuit	No. of equivalent gate	Symbolic diagram		t_{PLH} (ns)		t_{PHL} (ns)	
					t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
Power-4 input NAND NG004		4		8	2.7	2.2	2.9	2.1
Power-2 input NOR NG005		2		11	1.9	2.5	0.9	1.5
Power-3 input NOR NG006		3		11	3.7	3.3	1.5	1.5
Power-4 input NOR NG007		4		8	6.1	4.3	1.8	1.5

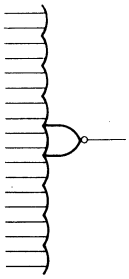
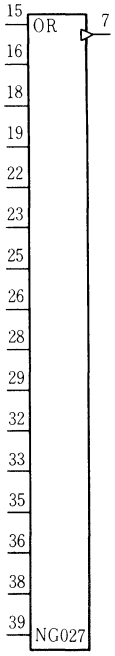
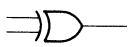
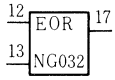
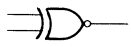
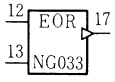
- **Gate**

Macro Cell				Symbol No.	Propagation delay time			
Functional block name	Equivalent circuit	No. of equivalent gate	Symbolic diagram		t_{PLH} (ns)		t_{PHL} (ns)	
					t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
Inverter NG012		0.5		11	0.6	3.0	0.4	2.2
2 input NAND NG008		1.0		11	1.3	3.6	1.0	2.7
3 input NAND NG009		1.5		11	2.0	3.9	1.9	3.4
4 input NAND NG010		2.0		8	2.9	4.3	3.2	4.1
6 input NAND NG013		4.5		6	4.1	2.7	6.0	2.0

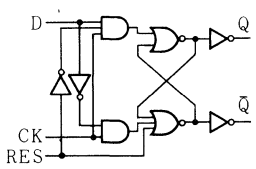
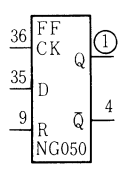
Macro Cell			Symbolic diagram	Symbol No.	Propagation delay time			
Functional block name	Equivalent circuit	No. of equivalent gate			t_{PLH} (ns)		t_{PHL} (ns)	
					t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
8 input NAND NG014		5.5		5	4.7	2.9	7.7	2.0
9 input NAND NG015		6.5		7	4.6	2.9	8.2	2.2
12 input NAND NG016		8.0		9	5.0	3.0	9.9	2.2

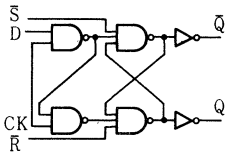
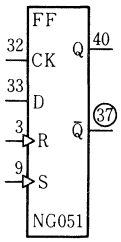
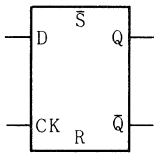
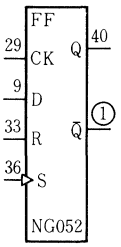
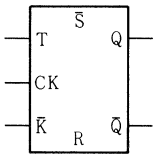
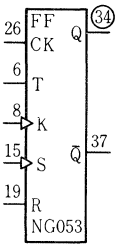
Macro Cell			Symbolic diagram	Symbol No.	Propagation delay time			
					t_{PLH} (ns)		t_{PHL} (ns)	
Functional block name	Equivalent circuit	No. of equivalent gate			t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
16 input NAND NG017		10.5		10	5.3	3.0	12.5	2.5
2 input NOR NG018		1.0		11	1.8	4.7	1.0	2.7
3 input NOR NG019		1.5		11	3.7	6.8	1.4	2.7
4 input NOR NG020		2.0		8	6.5	8.5	1.5	3.1
6 input NOR NG023		4.5		6	7.6	2.6	3.6	2.1

Macro Cell			Symbolic diagram	Symbol No.	Propagation delay time			
					t_{PLH} (ns)		t_{PHL} (ns)	
Functional block name	Equivalent circuit	No. of equivalent gate			t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
8 input NOR NG024		5.5		5	10.5	2.8	3.7	2.0
9 input NOR NG025		6.5		7	8.6	2.8	4.2	2.1
12 input NOR NG026		8.0		9	12.1	2.8	4.5	2.0

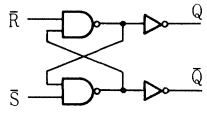
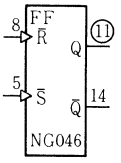
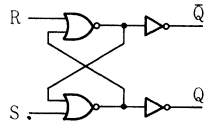
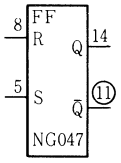
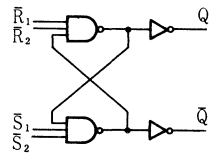
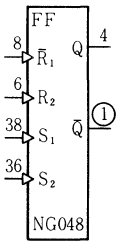
Macro Cell: Functional block name	Macro Cell: Equivalent circuit	Macro Cell: No. of equivalent gate	Symbolic diagram	Symbol No.	Propagation delay time: t_{PLH} (ns): t_{OLH}	Propagation delay time: t_{PLH} (ns): K_{LH}	Propagation delay time: t_{PHL} (ns): t_{OHL}	Propagation delay time: t_{PHL} (ns): K_{HL}
16 input NOR NG027		10.5		10	13.2	3.0	4.9	2.1
2 input EOR NG032		2.5		11	4.2	4.5	3.9	2.0
2 input ENOR NG033		2.5		11	3.2	2.5	3.2	3.0

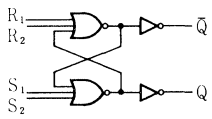
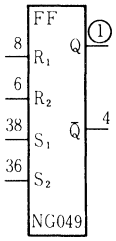
- **Flip-flop**

Macro Cell: Functional block name	Macro Cell: Equivalent circuit	Macro Cell: No. of equivalent gate	Symbolic diagram	Symbol No.	Input terminal name	Output terminal name	Propagation delay time: t_{PLH} (ns): t_{OLH}	Propagation delay time: t_{PLH} (ns): K_{LH}	Propagation delay time: t_{PHL} (ns): t_{OHL}	Propagation delay time: t_{PHL} (ns): K_{HL}
DFF (Level) NG050		6		17	CK R D	Q	4.5 5.0 4.3	2.8	8.3 6.6 9.6	2.3
					CK R D	$\bar{Q}$	3.3 3.8 5.1	2.6	10.0 10.6 9.1	2.5

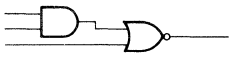
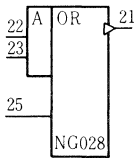
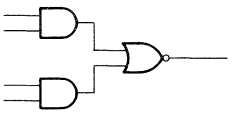
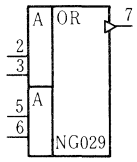
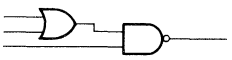
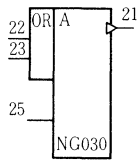
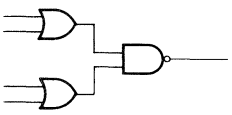
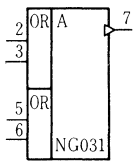
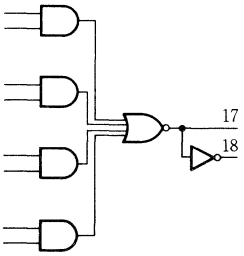
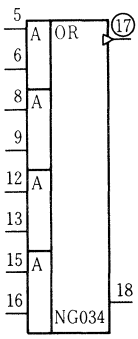
Macro Cell: Functional block name	Macro Cell: Equivalent circuit	Macro Cell: No. of equivalent gate	Symbolic diagram	Symbol No.	Propagation delay time: Input terminal name	Propagation delay time: Output terminal name	Propagation delay time: t_{PLH} (ns) t_{OLH}	Propagation delay time: t_{PLH} (ns) K_{LH}	Propagation delay time: t_{PHL} (ns) t_{OHL}	Propagation delay time: t_{PHL} (ns) K_{HL}
DFF (Level) NG051		6		15	CK	Q	8.6	2.7	5.3	1.9
					S		6.6		–	
					R		4.5		3.4	
					D		9.1		6.8	
					CK	$\bar{Q}$	9.1	2.7	5.3	1.8
					S		4.5		3.1	
					R		7.3		–	
					D		10.5		5.6	
DFF (Edge) NG052		10.5		15	CK	Q	10.3	2.7	7.0	1.8
					S		6.9		–	
					R		6.2		4.5	
					CK	$\bar{Q}$	10.6	2.7	6.8	1.9
					S		4.7		3.4	
					R		8.0		–	
					D	–	–	–	–	–
TKFF NG053		12		15	CK	Q	7.2	2.3	7.5	5.8
					S		3.0		3.0	
					R		–		7.2	
					CK	$\bar{Q}$	4.7	2.3	10.1	5.8
					S		–		5.7	
					R		4.4		4.5	
					$J.\bar{K}$	–	–	–	–	–

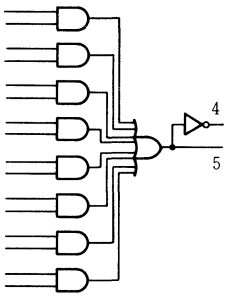
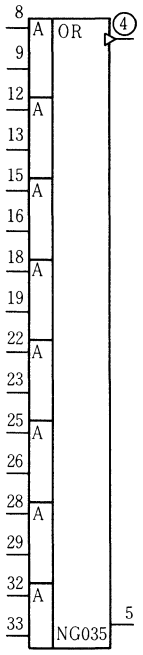
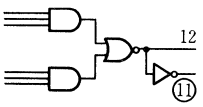
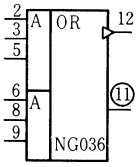
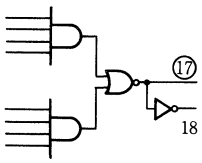
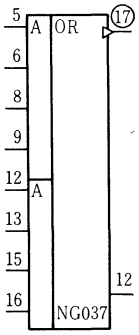
- **Latch**

Macro Cell: Functional block name	Macro Cell: Equivalent circuit	Macro Cell: No. of equivalent gate	Symbolic diagram	Symbol No.	Propagation delay time: Input terminal name	Propagation delay time: Output terminal name	Propagation delay time: t_{PLH} (ns) t_{OLH}	Propagation delay time: t_{PLH} (ns) K_{LH}	Propagation delay time: t_{PHL} (ns) t_{OHL}	Propagation delay time: t_{PHL} (ns) K_{HL}
$\bar{R}\bar{S}$LCH NG046		3		17	$\bar{S}$	Q	5.1	2.5	–	1.5
					$\bar{R}$		3.0		3.3	
					$\bar{S}$	$\bar{Q}$	3.4	2.3	2.9	1.5
					$\bar{R}$		5.6		–	
RSLCH NG047		3		17	S	Q	2.9	2.3	4.0	1.8
					R		–		5.5	
					S	$\bar{Q}$	–	2.3	5.8	1.8
					R		3.0		4.2	
$\bar{R}\bar{S}$LCH NG048		4		15	$\bar{S}$	Q	7.2	2.6	–	1.6
					$\bar{R}$		4.5		3.4	
					$\bar{S}$	$\bar{Q}$	4.4	2.6	3.7	1.7
					$\bar{R}$		6.9		–	

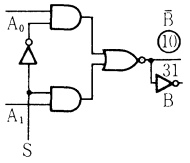
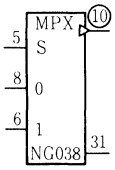
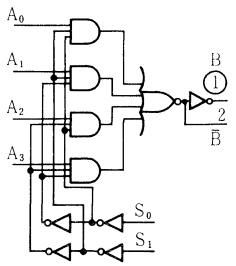
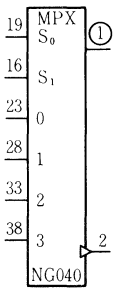
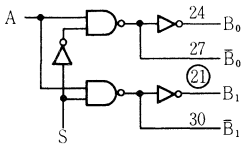
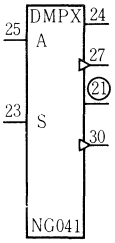
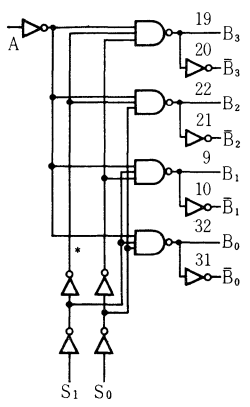
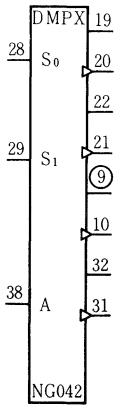
Macro Cell			Symbolic diagram	Symbol No.	Propagation delay time					
Functional block name	Equivalent circuit	No. of equivalent gate			Input terminal name	Output terminal name	t_{PLH} (ns)		t_{PHL} (ns)	
							t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
RSLCH		4		15	S	Q	3.3	2.3	6.4	2.2
					R		–		7.5	
NG049					S R	$\overline{Q}$	– 3.3	2.3	7.5 6.6	2.2

• AND-NOR Gate

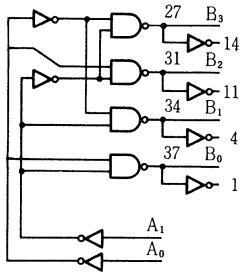
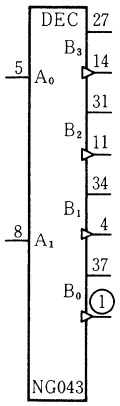
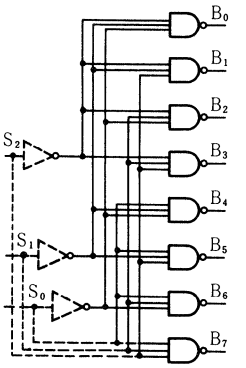
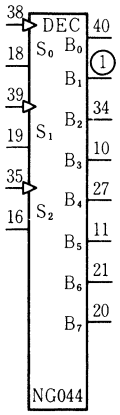
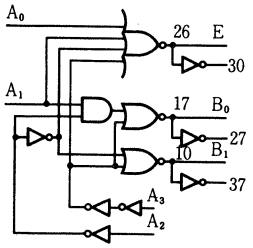
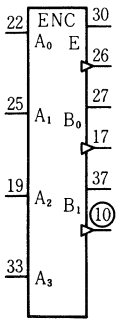
Macro Cell			Symbolic diagram	Symbol No.	Propagation delay time					
Functional block name	Equivalent circuit	No. of equivalent gate			Input terminal name	Output terminal name	t_{PLH} (ns)		t_{PHL} (ns)	
							t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
2 AND-NOR		1.5		4	AND input		2.6	5.5	1.4	2.9
NG028					NOR input		2.0	–	1.4	–
2 wide-2 input AND-NOR		2.0		2			3.0	4.1	2.2	2.8
NG029										
2 OR-NAND		1.5		4	OR input		2.5	5.0	1.9	3.8
NG030					NAND input		1.9	–	1.2	–
2 wide-2 input OR-NAND		2.0		2			3.8	5.0	1.8	2.7
NG031										
4 wide-2 input AND-NOR		4.5		3		NOR	8.5	5.1	3.8	2.6
NG034						Inverter	5.6	3.5	9.0	3.5

Macro Cell			Symbolic diagram	Symbol No.	Propagation delay time					
Functional block name	Equivalent circuit	No. of equivalent gate			Input terminal name	Output terminal name	t_{PLH} (ns)		t_{PHL} (ns)	
							t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
8 wide-2 input AND-NOR NG035		9.5		1		Inverter	11.8	3.4	6.8	2.4
						OR	6.3	2.5	10.5	3.2
2 wide-3 input AND-NOR NG036		3.5		2		NOR	4.4	2.9	4.5	3.1
						Inverter	6.2	4.0	5.0	2.8
2 wide-4 input AND-NOR NG037		4.5		3		NOR	4.5	2.6	7.2	3.8
						Inverter	9.4	4.9	5.1	2.9

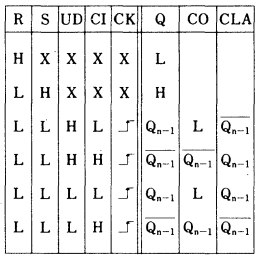
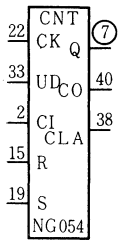
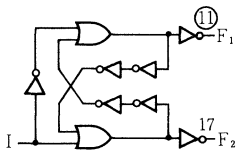
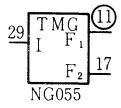
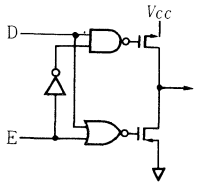
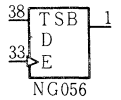
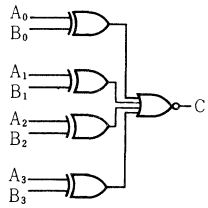
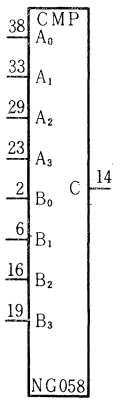
• Multiplexer

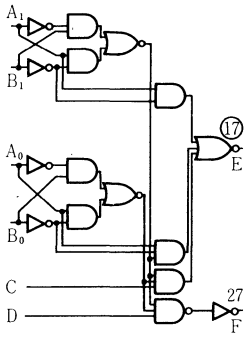
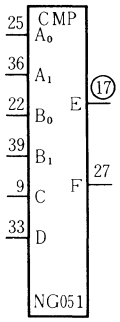
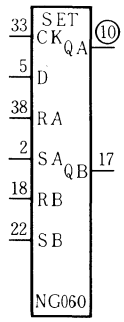
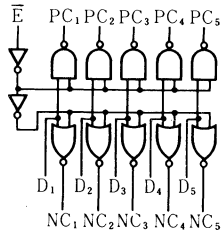
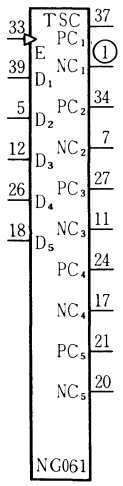
Macro Cell: Functional block name	Equivalent circuit	No. of equivalent gate	Symbolic diagram	Symbol No.	Propagation delay time: Input terminal name	Output terminal name	t_{PLH} (ns)		t_{PHL} (ns)	
							t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
2 input MPX		3		17	A_0	$\overline{B}$	4.4		2.0	
					A_1		3.3	4.2	3.1	2.6
					S		3.8		2.4	
					A_0	B	3.3		5.0	
					A_1		4.4	3.2	3.8	2.8
NG038					S		3.8		4.7	
4 input MPX		8.5		13	A_0	$\overline{B}$	9.5	4.8	9.3	3.7
					A_1		8.6		9.6	
					A_2		6.2		6.8	
					A_3		4.8		5.8	
					S_0		11.3		15.5	
					S_1		10.5		13.0	
					A_0		8.5	6.7	7.5	3.5
					A_1		8.8		6.3	
					A_2		6.0		4.6	
					A_3		5.0		3.3	
NG040					S_0		15.1		8.5	
					S_1		12.0		7.2	
2 output DMPX		3.5		14	A	B_0	3.4	3.4	2.6	2.2
					S		4.2		3.5	
					A	B_1	2.7	3.5	2.3	2.3
					S		2.9		3.1	
					A	$\overline{B}_0$	2.0	2.3	2.0	2.7
					S		2.8		3.1	
					A	$\overline{B}_1$	1.6	2.3	1.6	2.3
NG041					S		2.5		1.8	
4 output DMPX		10.5		12	A	B_3	4.3	2.1	5.3	3.1
					S_0		5.2		5.3	
					S_1		5.4		5.2	
					A	B_2	4.3	2.4	5.1	3.2
					S_0		3.3		4.6	
					S_1		5.3		5.3	
					A	B_1	3.5	2.6	4.9	3.2
					S_0		5.2		5.7	
					S_1		3.7		4.7	
					A	B_0	4.0	2.4	5.1	2.9
					S_0		3.6		4.6	
					S_1		4.0		5.1	
					A	$\overline{B}_3$	6.5	4.1	4.9	2.6
					S_0		6.3		5.5	
					S_1		6.4		5.7	
					A	$\overline{B}_2$	6.2	3.9	4.8	2.5
					S_0		5.9		3.8	
					S_1		6.0		6.0	
					A	$\overline{B}_1$	6.4	4.2	4.0	2.8
					S_0		6.8		6.1	
					S_1		6.1		4.0	
					A	$\overline{B}_0$	5.8	4.3	3.8	2.3
					S_0		6.2		4.2	
NG042					S_1		6.1		4.7	

• Decoder/Encoder

Macro Cell: Functional block name	Macro Cell: Equivalent circuit	Macro Cell: No. of equivalent gate	Symbolic diagram	Symbol No.	Propagation delay time: Input terminal name	Propagation delay time: Output terminal name	Propagation delay time: t_{PLH} (ns)		Propagation delay time: t_{PHL} (ns)	
							t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
2-bit decoder		8		12	A_0 A_1	B_0	3.3 3.4	2.3	4.0 3.9	2.3
					A_0 A_1	B_1	4.9 3.7	2.3	4.7 3.8	2.3
					A_0 A_1	B_2	3.7 4.9	2.4	4.1 4.7	2.3
					A_0 A_1	B_3	5.1 5.1	2.2	4.7 4.8	2.3
					A_0 A_1	$\overline{B}_0$	4.9 4.6	3.6	4.0 4.0	2.1
					A_0 A_1	$\overline{B}_1$	5.8 4.6	3.6	5.5 4.3	2.2
					A_0 A_1	$\overline{B}_2$	5.0 5.6	3.7	4.4 5.2	2.5
NG043					A_0 A_1	$\overline{B}_3$	5.6 5.8	3.3	5.6 5.4	2.4
3-bit decoder		12		12	S, $\overline{S}$	B	2.0	3.9	1.9	3.4
NG044	(dotted elements are not included in the cell)									
4-bit priority encoder 4 PENC		8		16	A_0 A_1 A_2 A_3	E	3.0 3.0 5.5 5.0	3.2	7.6 6.8 11.3 7.7	3.2
					A_1 A_2 A_3	B_0	3.3 4.7 5.0	3.4	3.9 5.1 6.5	2.8
					A_2 A_3	B_1	4.7 4.9	2.8	5.6 5.8	2.8
					A_0 A_1 A_2 A_3	$\overline{E}$	7.7 6.4 10.3 7.4	8.6	1.9 1.8 4.5 4.1	1.7
					A_1 A_2 A_3	$\overline{B}_0$	3.2 4.5 5.9	4.4	2.5 3.5 3.5	2.6
NG045					A_2 A_3	$\overline{B}_1$	5.2 5.2	4.3	3.7 3.8	1.6

• Others

Macro Cell: Functional block name	Macro Cell: Equivalent circuit	Macro Cell: No. of equivalent gate	Symbolic diagram	Symbol No.	Propagation delay time: Input terminal name	Propagation delay time: Output terminal name	Propagation delay time: t_{PLH} (ns) t_{OLH}	Propagation delay time: t_{PLH} (ns) K_{LH}	Propagation delay time: t_{PHL} (ns) t_{OHL}	Propagation delay time: t_{PHL} (ns) K_{HL}
1-bit counter NG054	 R S UD CI CK Q CO CLA H X X X X L L H X X X H L L H L ⌐ Q_{n-1} L $\overline{Q_{n-1}}$ L L H H ⌐ $\overline{Q_{n-1}}$ $\overline{Q_{n-1}}$ Q_{n-1} L L L L ⌐ Q_{n-1} L Q_{n-1} L L L H ⌐ $\overline{Q_{n-1}}$ Q_{n-1} $\overline{Q_{n-1}}$	12	 CNT 22 CK Q ⑦ 33 UD CO 40 2 CI CLA 38 15 R 19 S NG054	15	CK S R	Q	14.0 9.5 10.0	4.6	13.2 4.3	2.0
					CK S R CI UD	CO	15.3 5.7 7.8 3.5 4.0	4.3	15.4 11.1 11.8 3.0 3.4	3.2
					CK S R UD	CLA	15.3 10.4 11.2 2.5	5.0	12.6 3.9 5.1 2.0	2.3
2-phase clock generator NG055	 ⑪ F_1 I 17 F_2	5.5	 TMG 29 I F_1 ⑪ F_2 17 NG055	11	I	F_1	3.4	2.5	6.5	2.0
						F_2	2.0	2.3	8.2	2.2
3-state buffer NG056	 V_{CC} D E	3.5	 38 TSB 1 33 D E NG056	11	E		3.9	–	2.9	–
					D		2.4	2.3	3.0	1.7
4-bit equivalent comparator NG058	 A_0 B_0 A_1 B_1 A_2 B_2 A_3 B_3 C	12	 CMP 38 A_0 33 A_1 29 A_2 23 A_3 2 B_0 C 14 6 B_1 16 B_2 19 B_3 NG058	12	A_0 A_1 A_2 A_3 B_0 B_1 B_2 B_3	C	11.1	9.0	6.9	1.9

Macro Cell			Symbolic diagram	Symbol No.	Propagation delay time					
Functional block name	Equivalent circuit	No. of equivalent gate			Input terminal name	Output terminal name	t_{PLH} (ns)		t_{PHL} (ns)	
							t_{OLH}	K_{LH}	t_{OHL}	K_{HL}
2-bit comparator		12		16	A_0	E	11.0	6.0	9.0	3.7
					A_1		9.5		10.3	
					B_0		9.5		8.8	
					B_1		8.4		10.0	
					D		8.0		4.3	
					A_0	F	8.8	2.7	7.4	1.8
					A_1		9.3		7.5	
					B_0		8.4		7.2	
					B_1		8.9		7.1	
NG059					D		4.0		2.9	
2-bit shift register	Truth table RA RB SA SB CK D QA QB H X X X X X L X X H X X X X X L L X H X L X QA_{n-1} X L X H X H X H X X L X H L X X QB_{n-1} X L X H H X X H L L L L ↓ L L QA_{n-1} L L L L ↓ H H QA_{n-1}	12		16	CK	QA	8.8	4.4	8.2	1.9
					RA				3.1	
					SA		13.8			
					CK	QB	8.8	4.4	8.2	1.9
					RB		13.2		2.0	
NG060					SB		13.8			
3-state output control		12		18	E	PC1 ~ PC5	3.2	2.3	4.2	2.4
					D1 ~ D5		2.0		1.6	
					E	NC0 ~ NC5	5.9	4.3	4.0	1.9
					D1 ~ D5		2.2		1.3	
NG061										

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